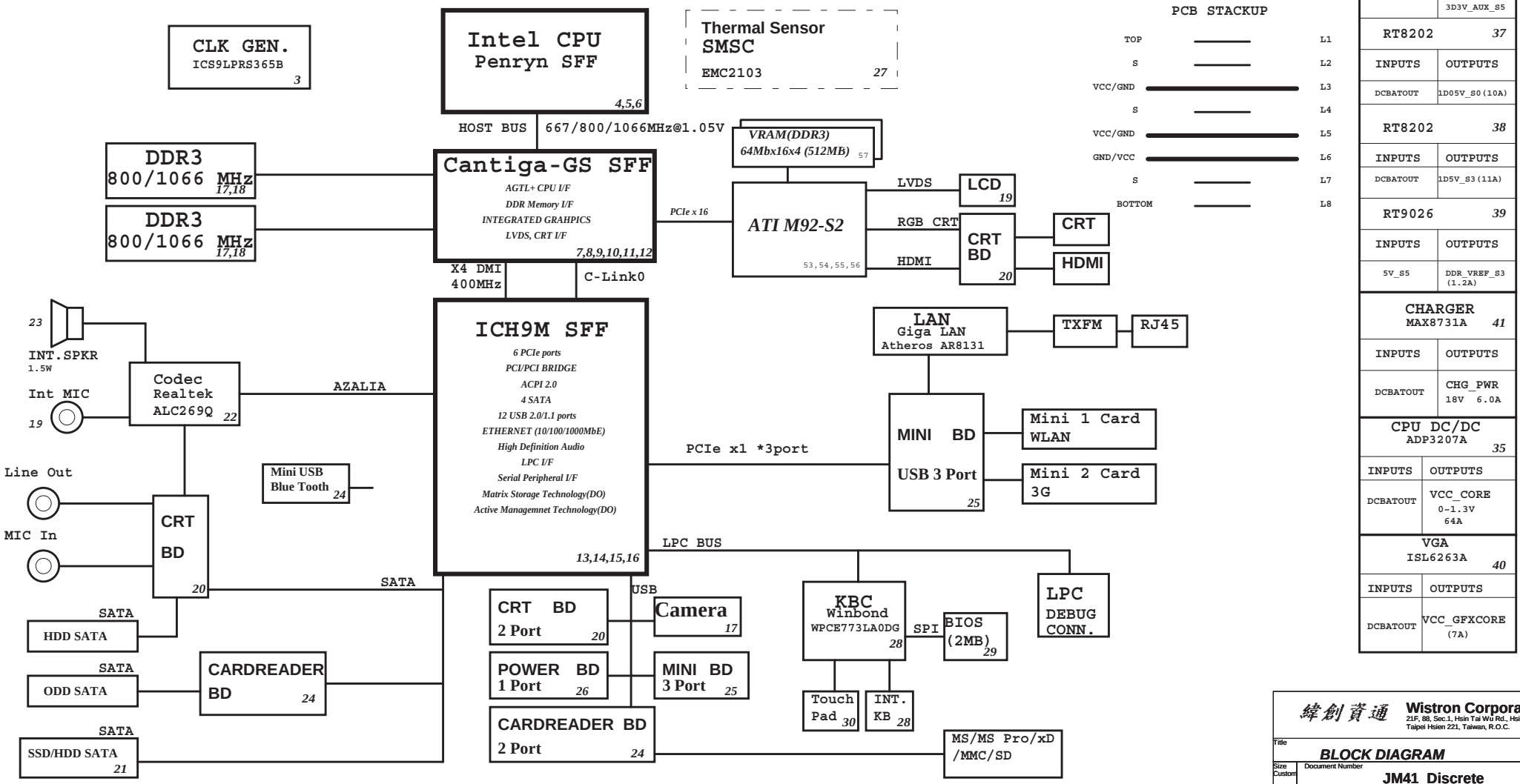
JM41 Discrete Block Diagram

Project code: 91.4CQ01.001
PCB P/N : 48.4CQ01.0SA
REVISION : 08274-SA



PCB STACKUP

TOP		L1
S		L2
VCC/GND		L3
S		L4
VCC/GND		L5
GND/VCC		L6
S		L7
BOTTOM		L8

SYSTEM DC/DC TPS51125 — 36

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(5A) 5V_AUX_S5 3D3V_AUX_S5

RT8202 — 37

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A)

RT8202 — 38

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3(11A)

RT9026 — 39

INPUTS	OUTPUTS
5V_S5	DDR_VREF_S3 (1.2A)

CHARGER MAX8731A — 41

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ADP3207A — 35

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 64A

VGA ISL6263A — 40

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

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Title: BLOCK DIAGRAM
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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

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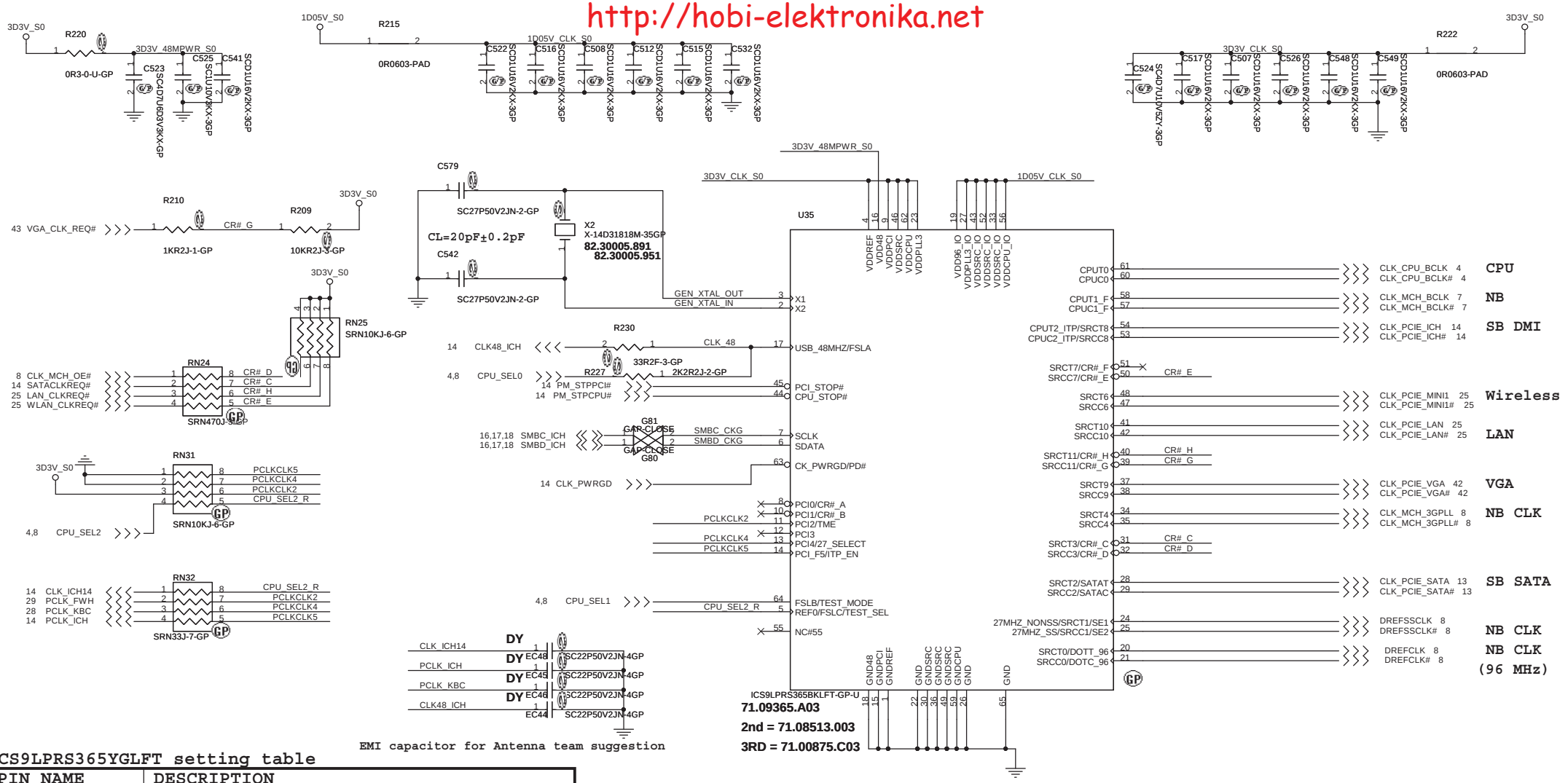

EMI capacitor for Antenna team suggestion

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Size	Document Number	Rev
	JM41_Discrete	SB

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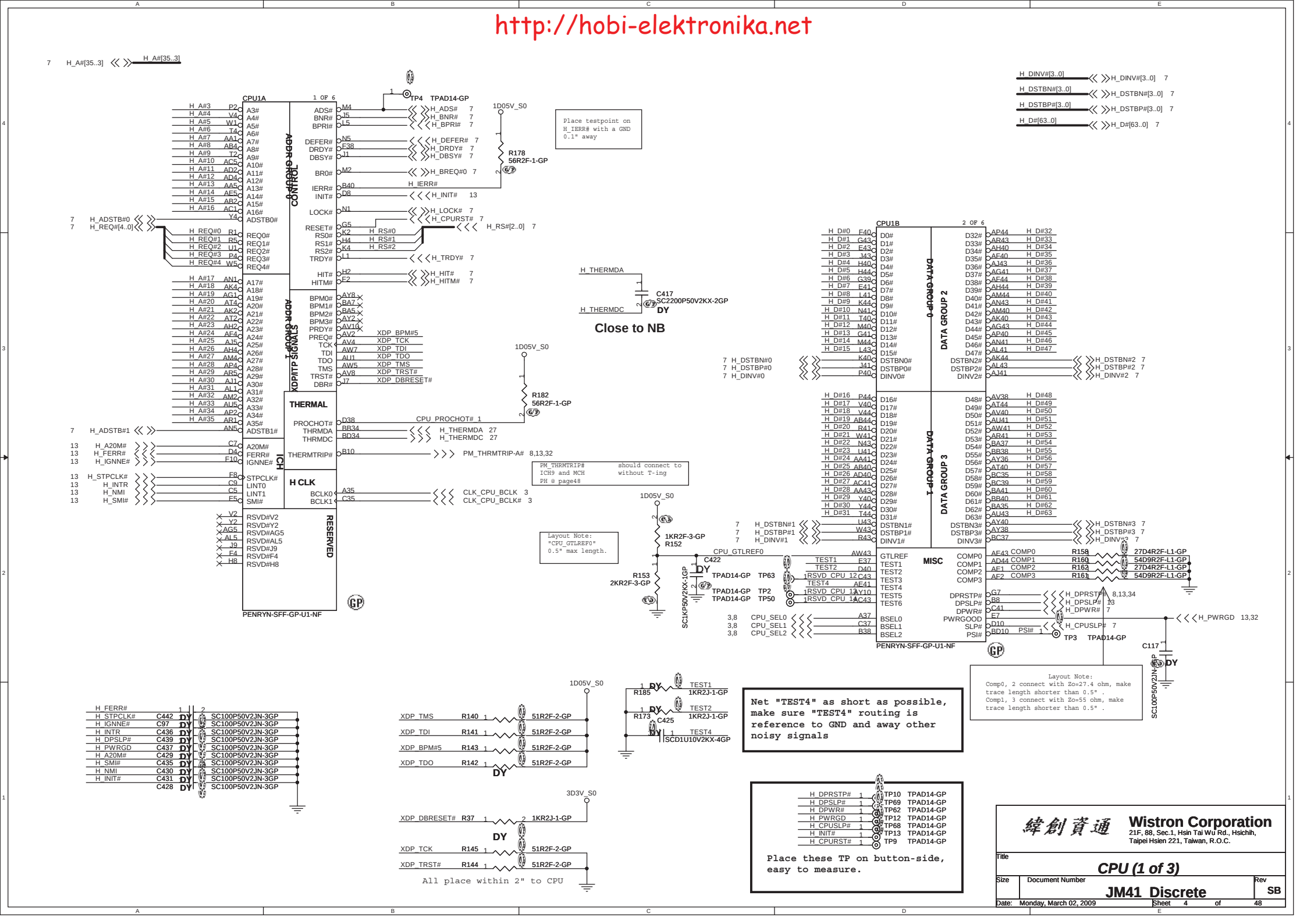

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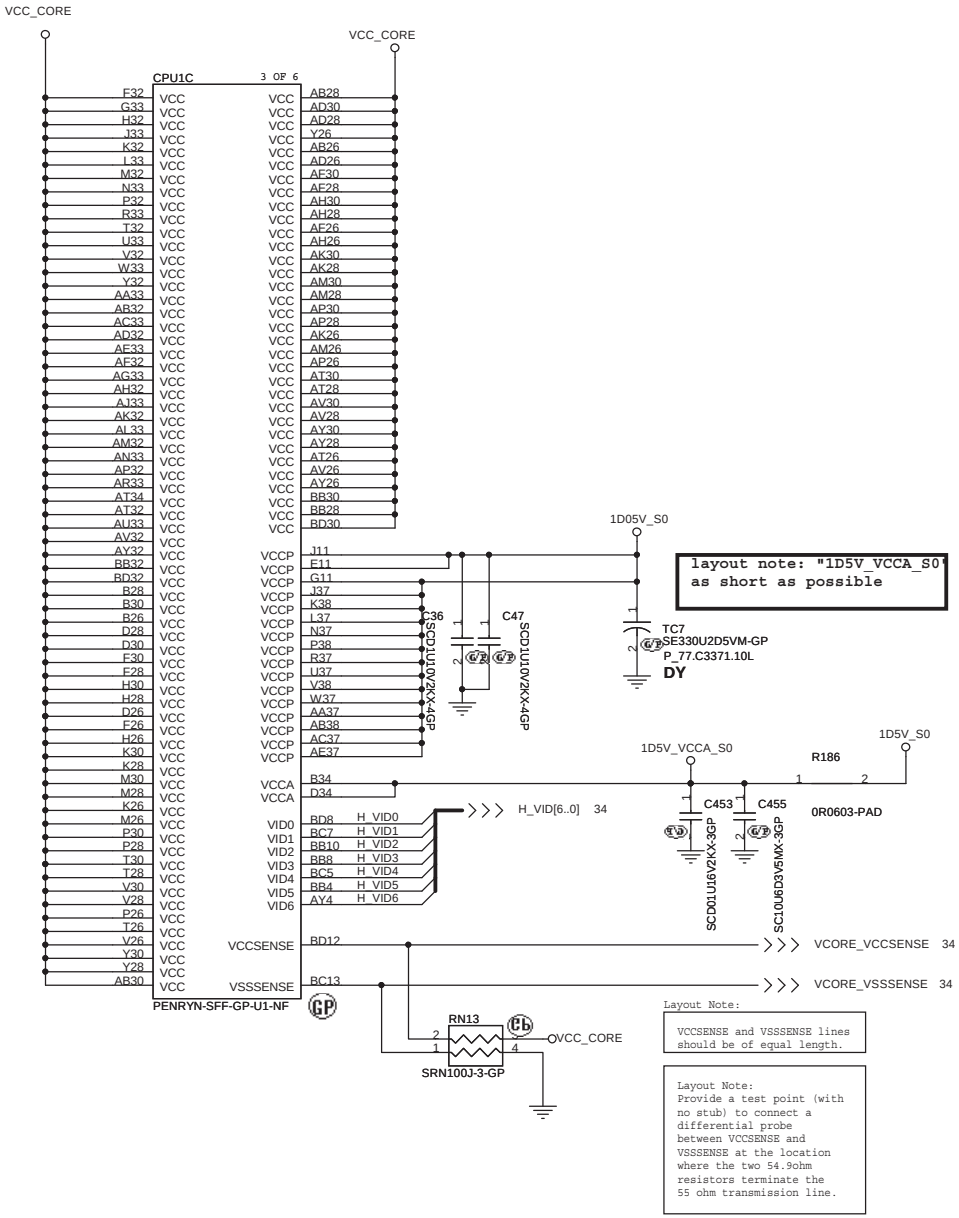

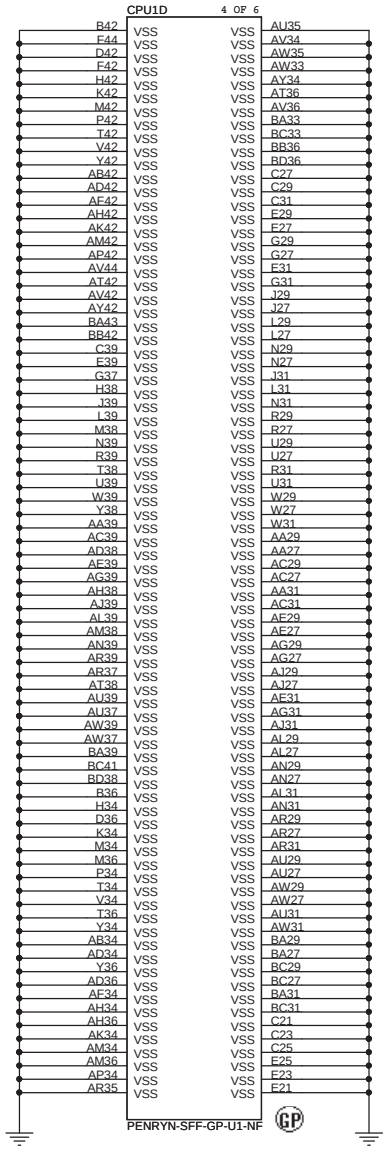

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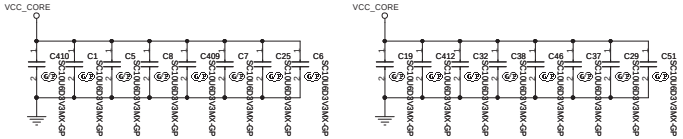
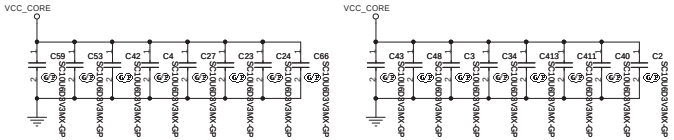
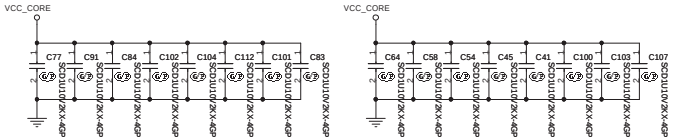
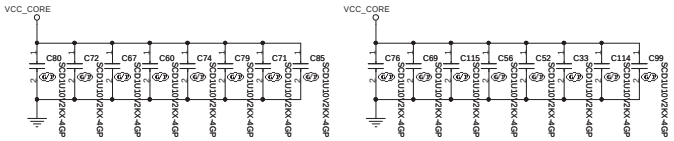
Place these inside socket cavity on L8(North side Secondary)

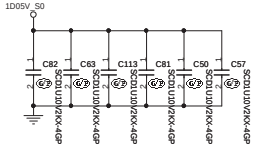


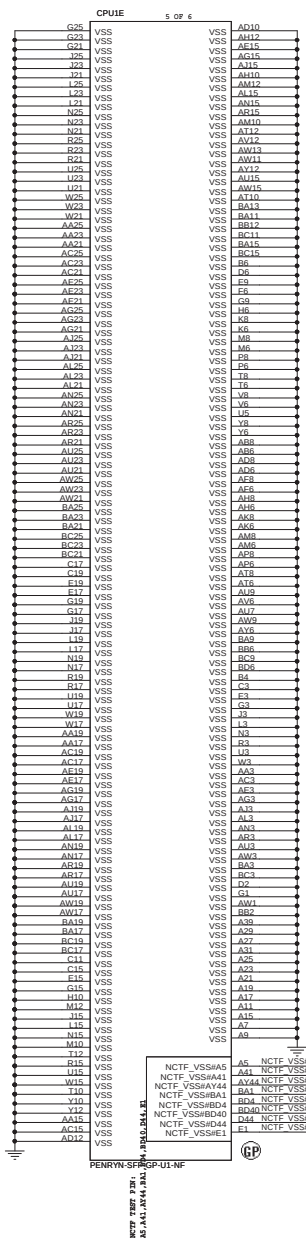


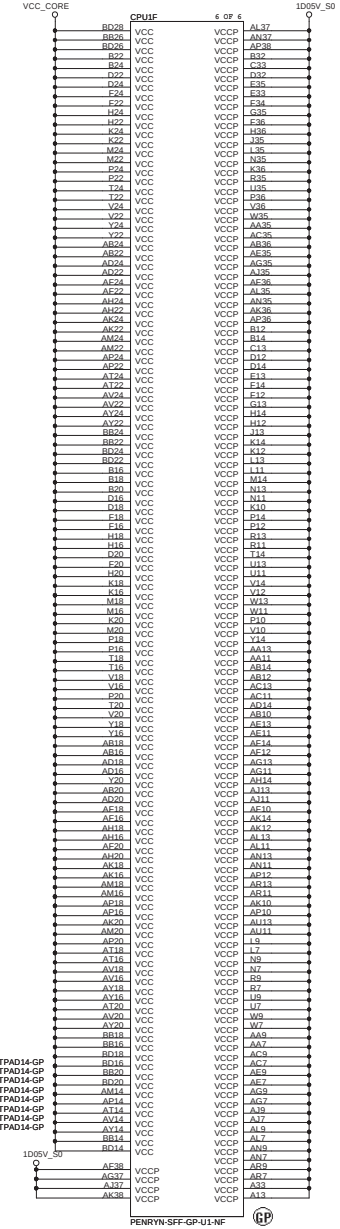




Place these inside socket cavity on L8(North side Secondary)







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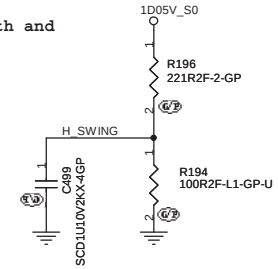
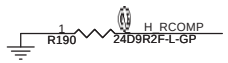
H_SWING routing Trace width and Spacing use 10 / 20 mil

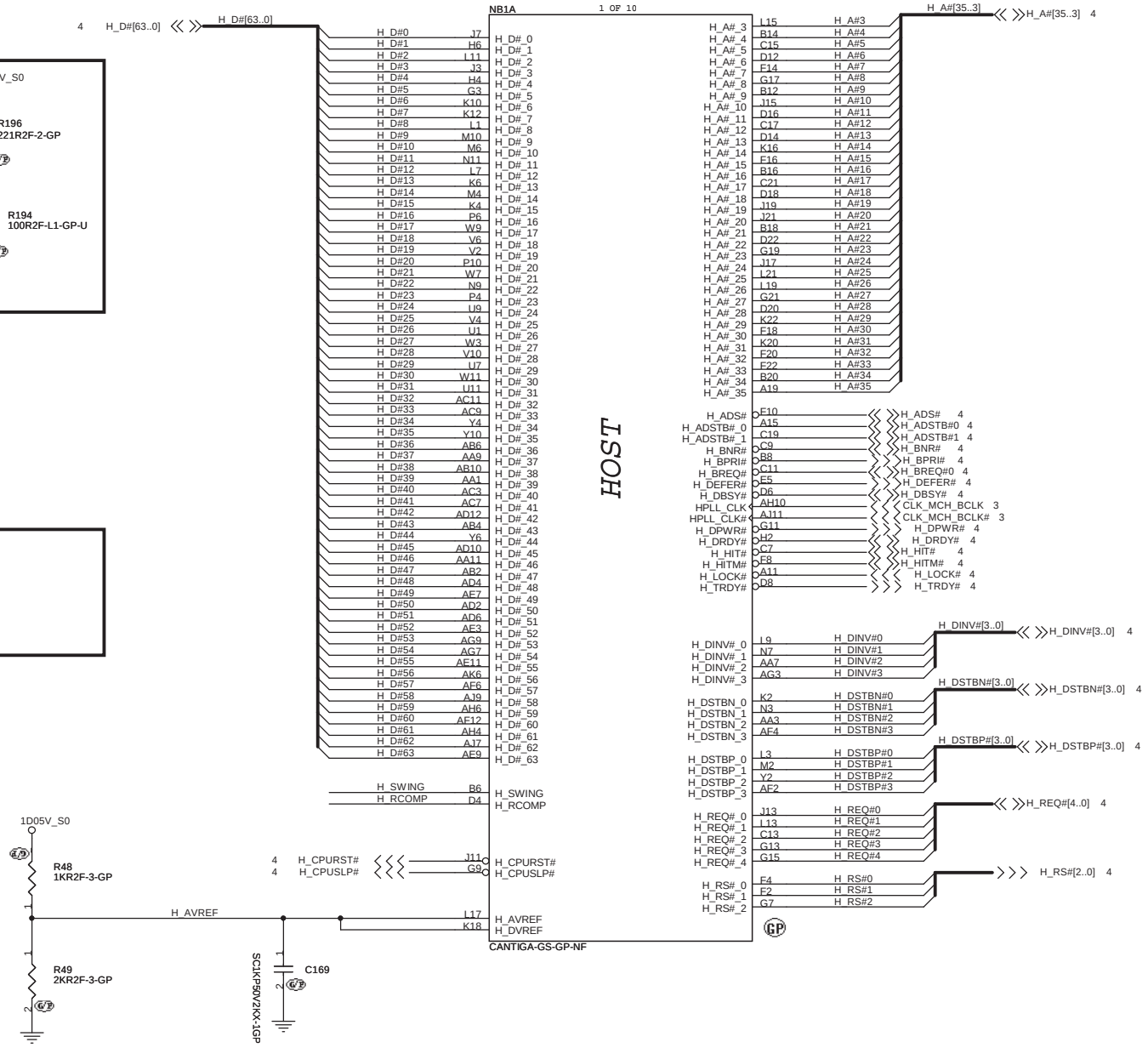
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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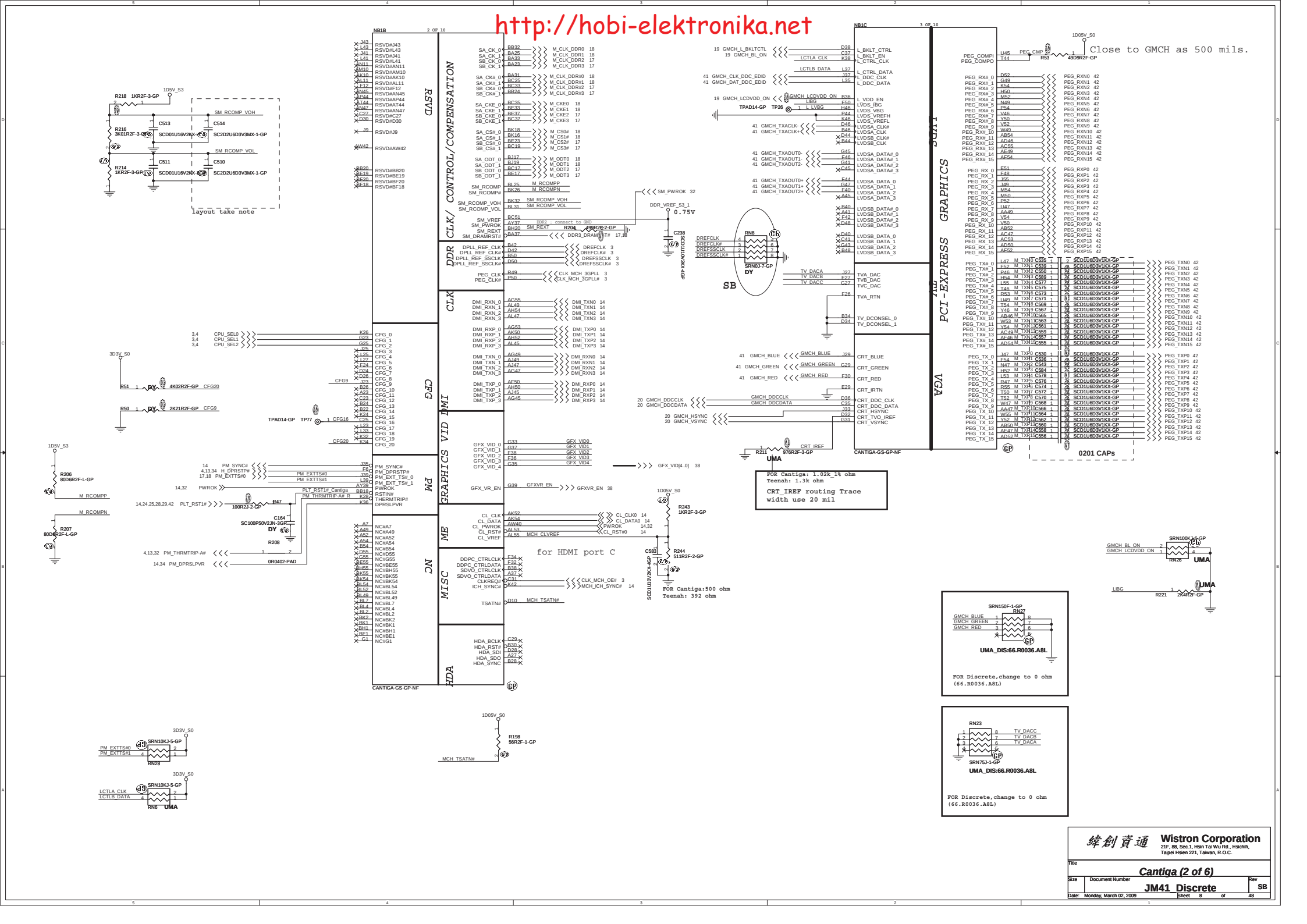

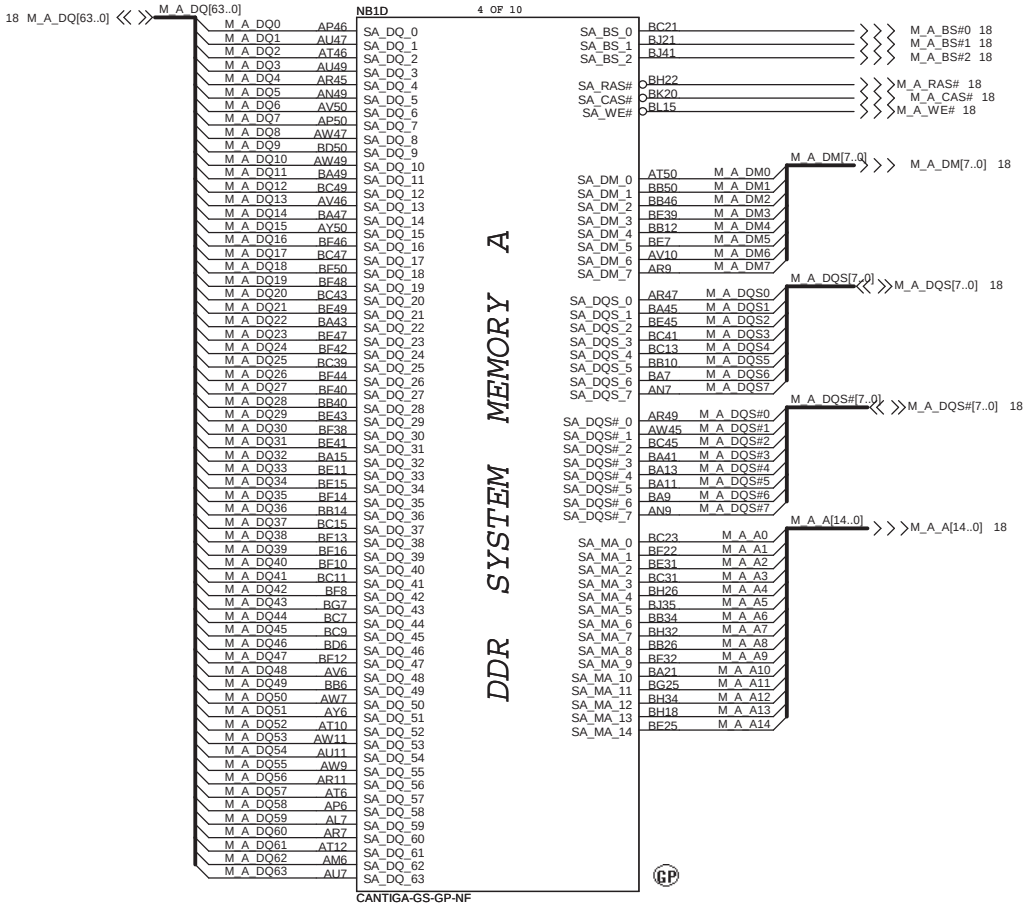

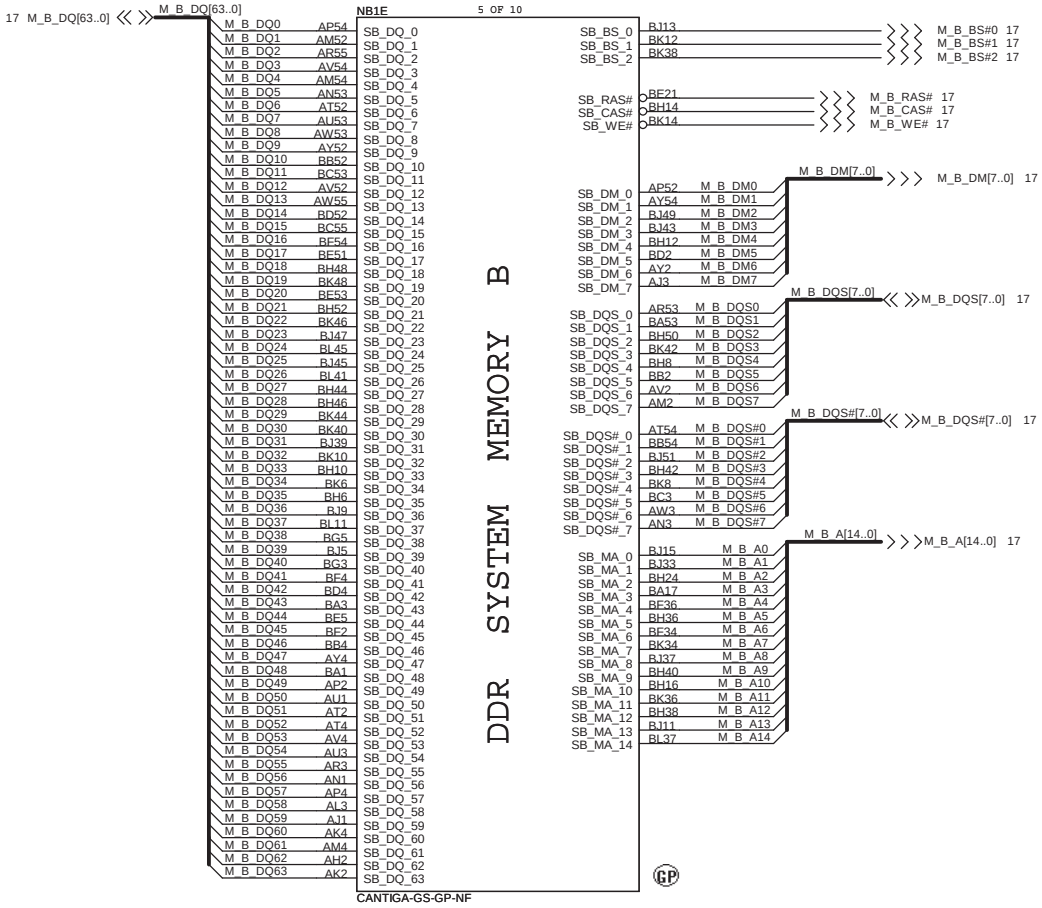

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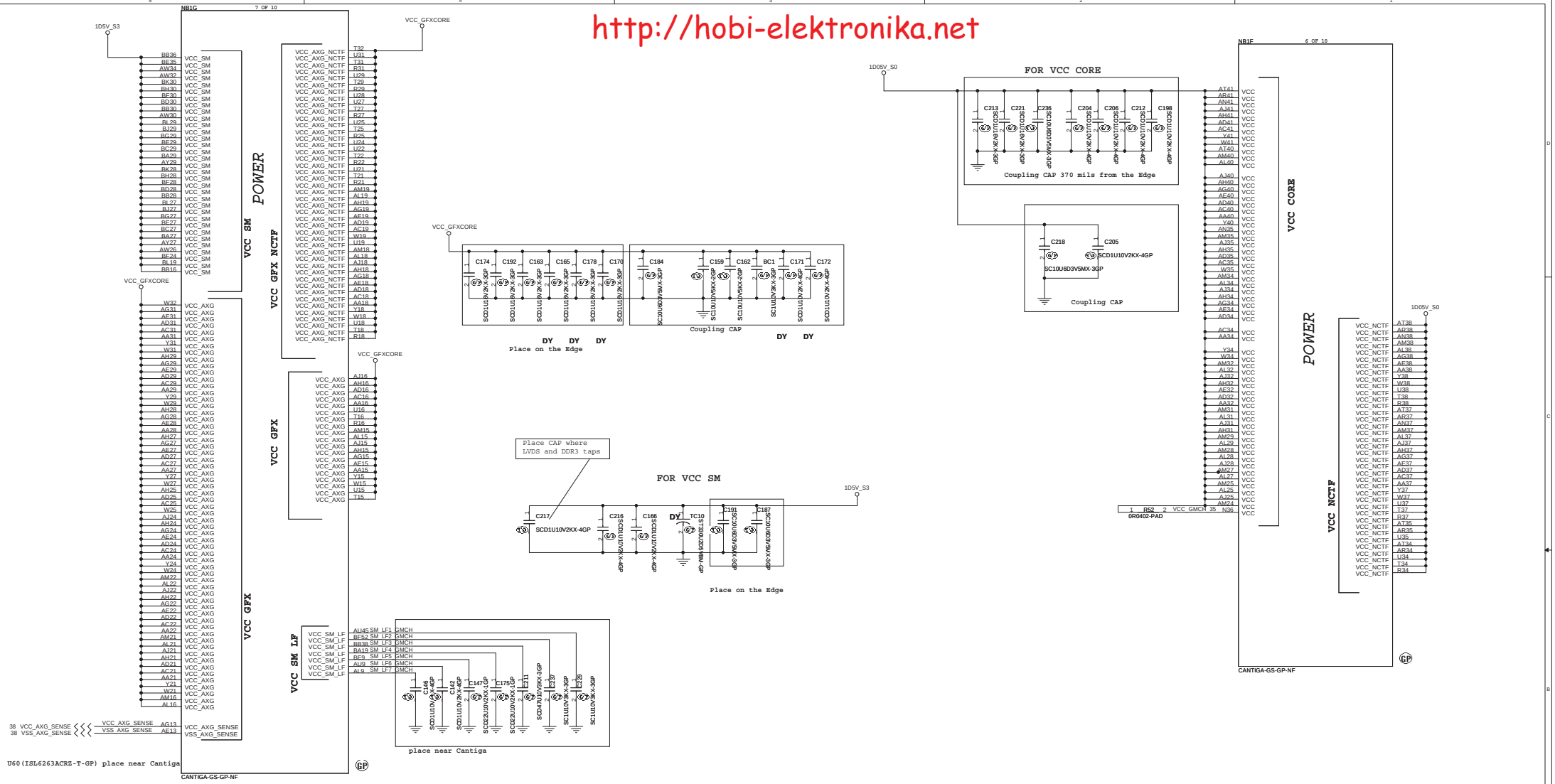

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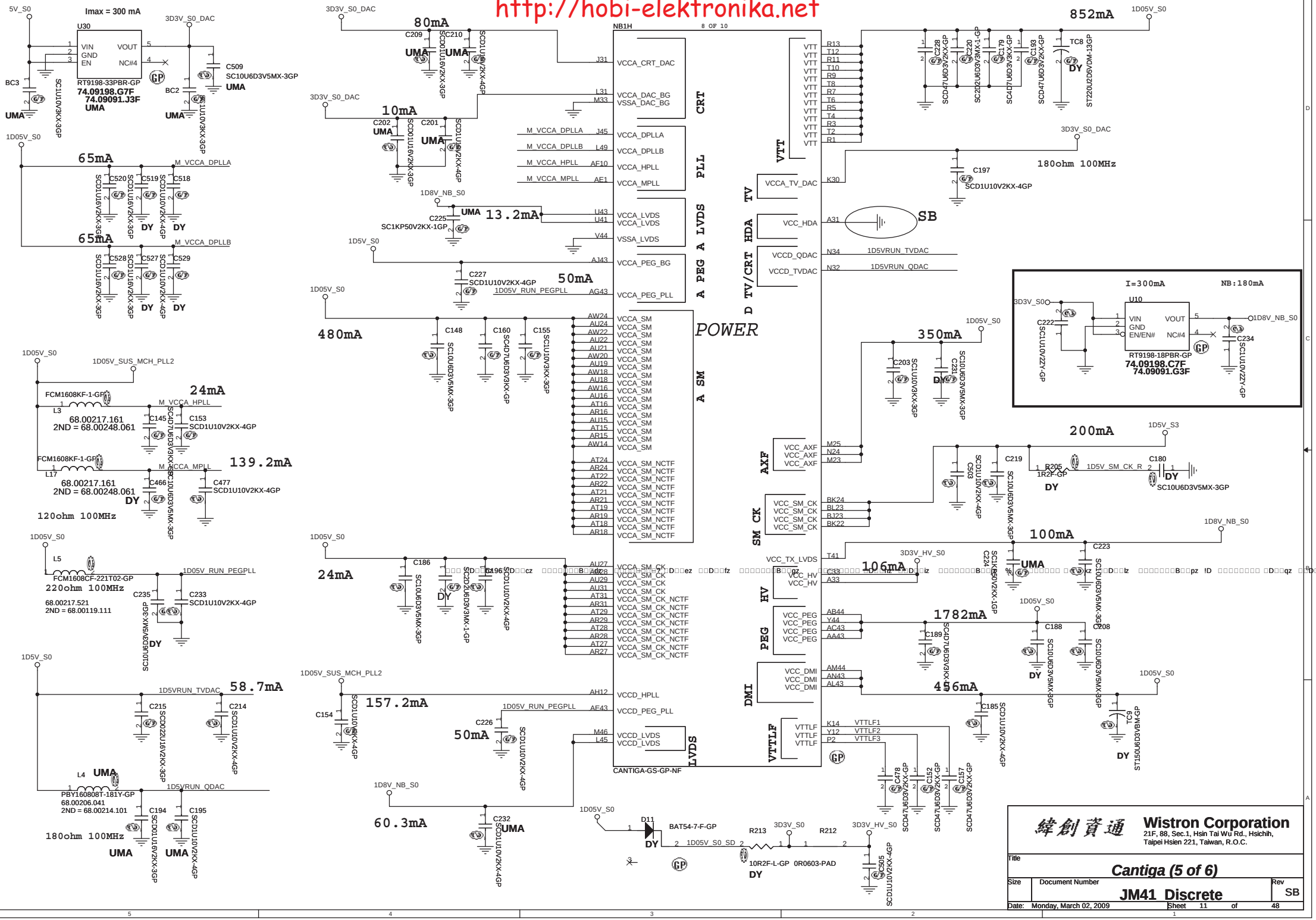

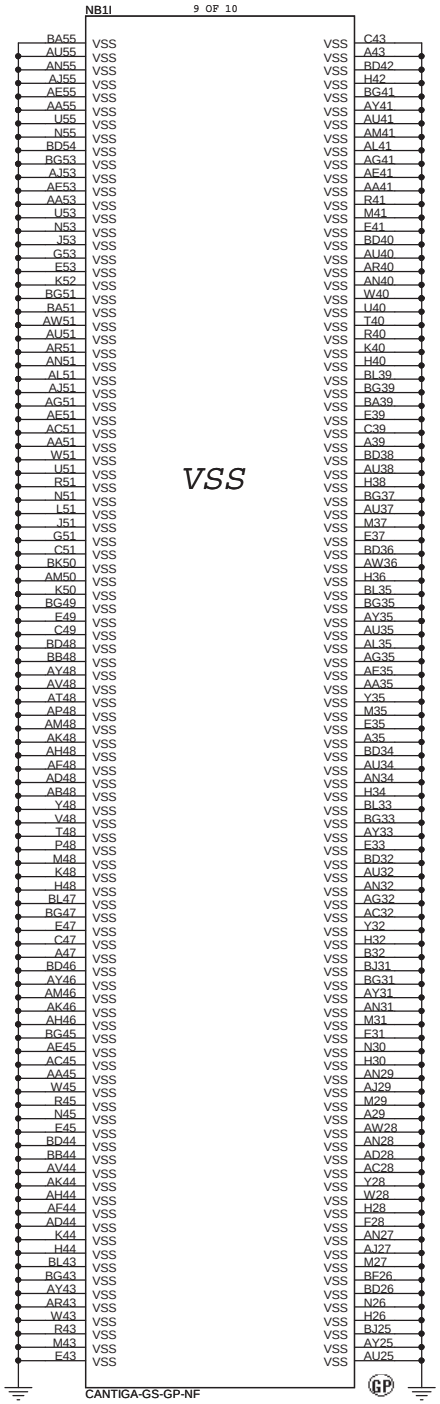

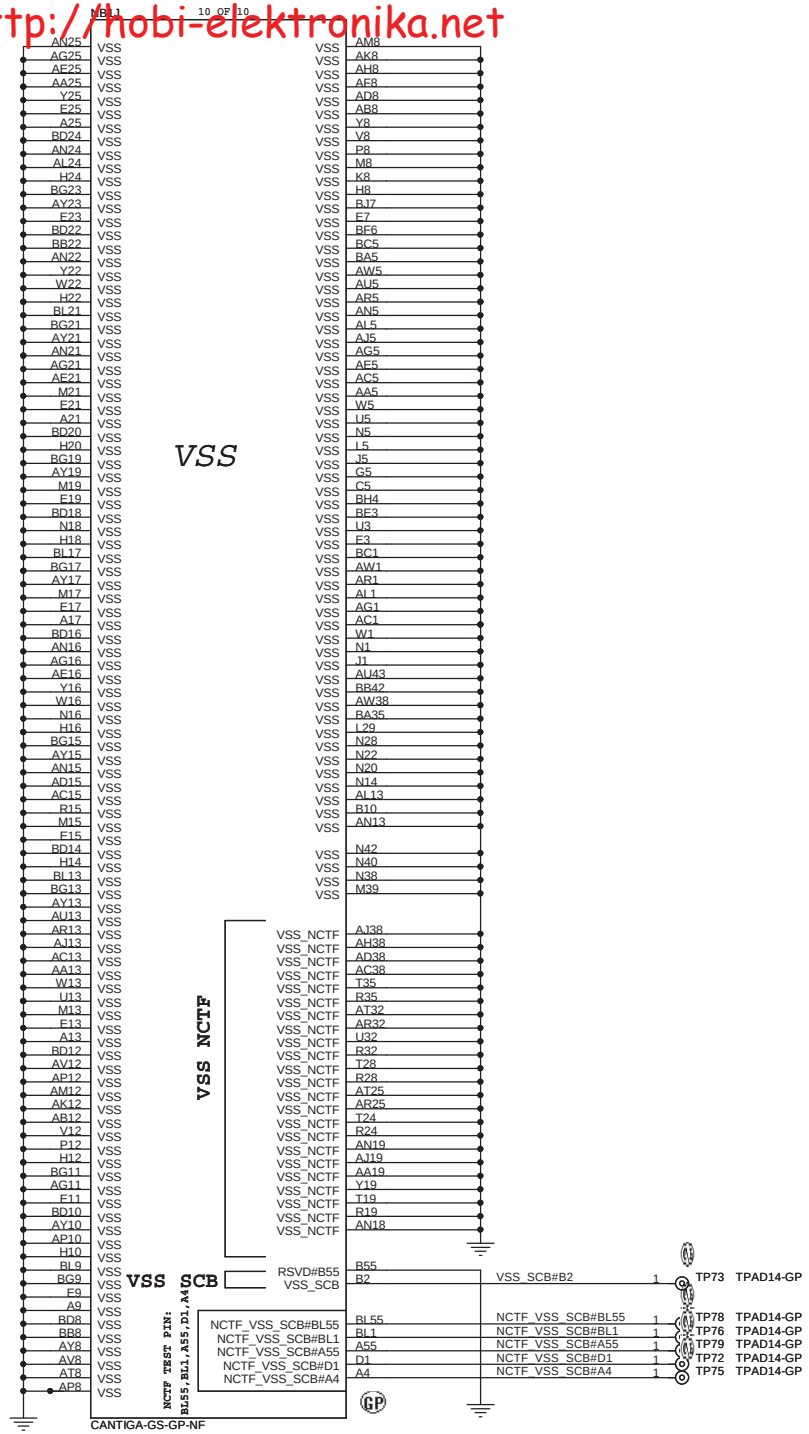

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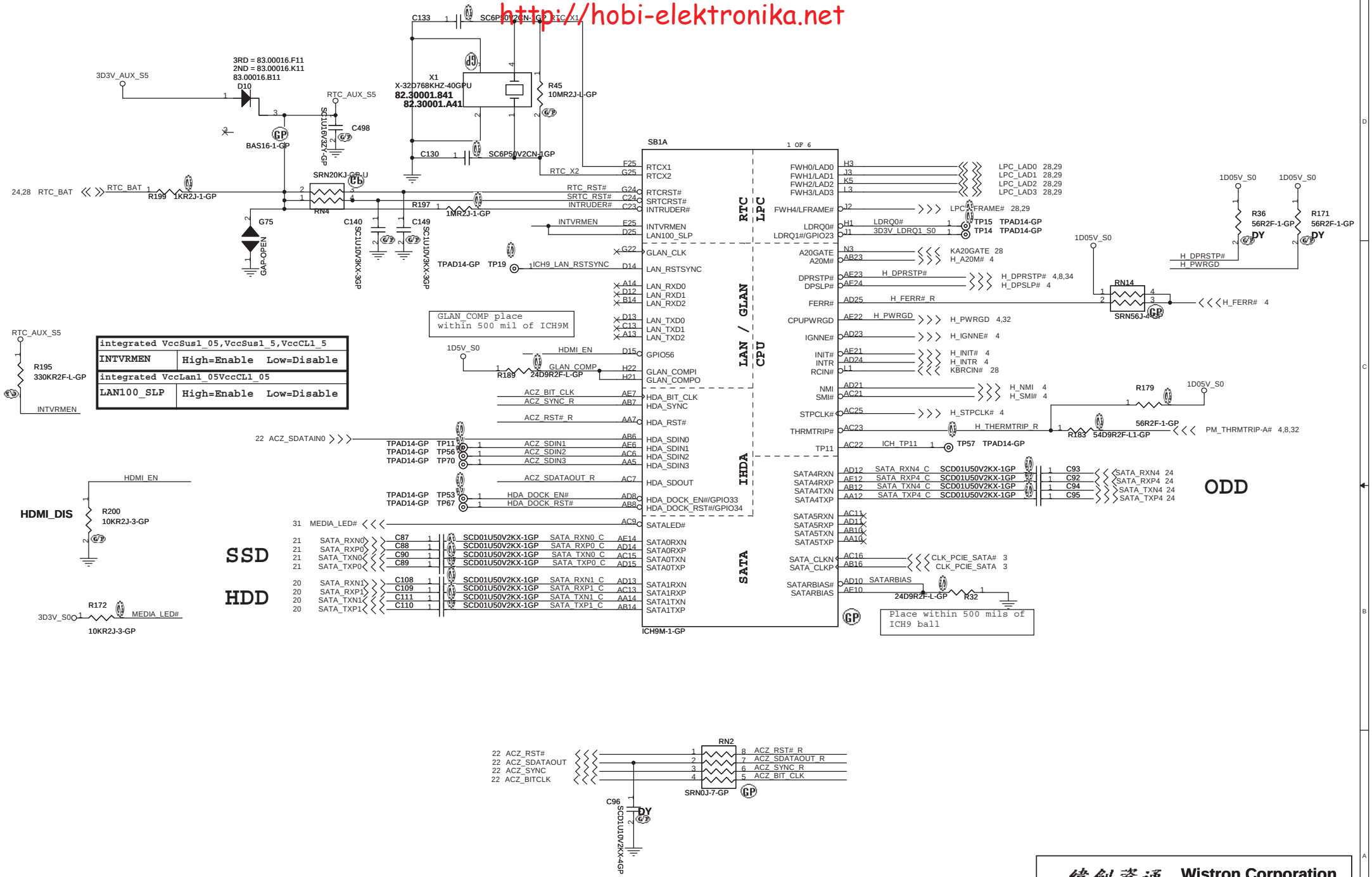

PCI_GNT#0 and SPI_CS1# have weak internal Pull up

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

GPIO049 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

USB

Pair	Device
0	USB2
1	USB3
2	USB4
3	WiMAX
4	WEBCAM
5	NC
6	NC
7	BLUETOOTH
8	NC
9	USB1
10	MINIC2
11	Cardreader

These R need close SB within 600 mils

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Size:	Document Number: JM41_Discrete Rev: SB
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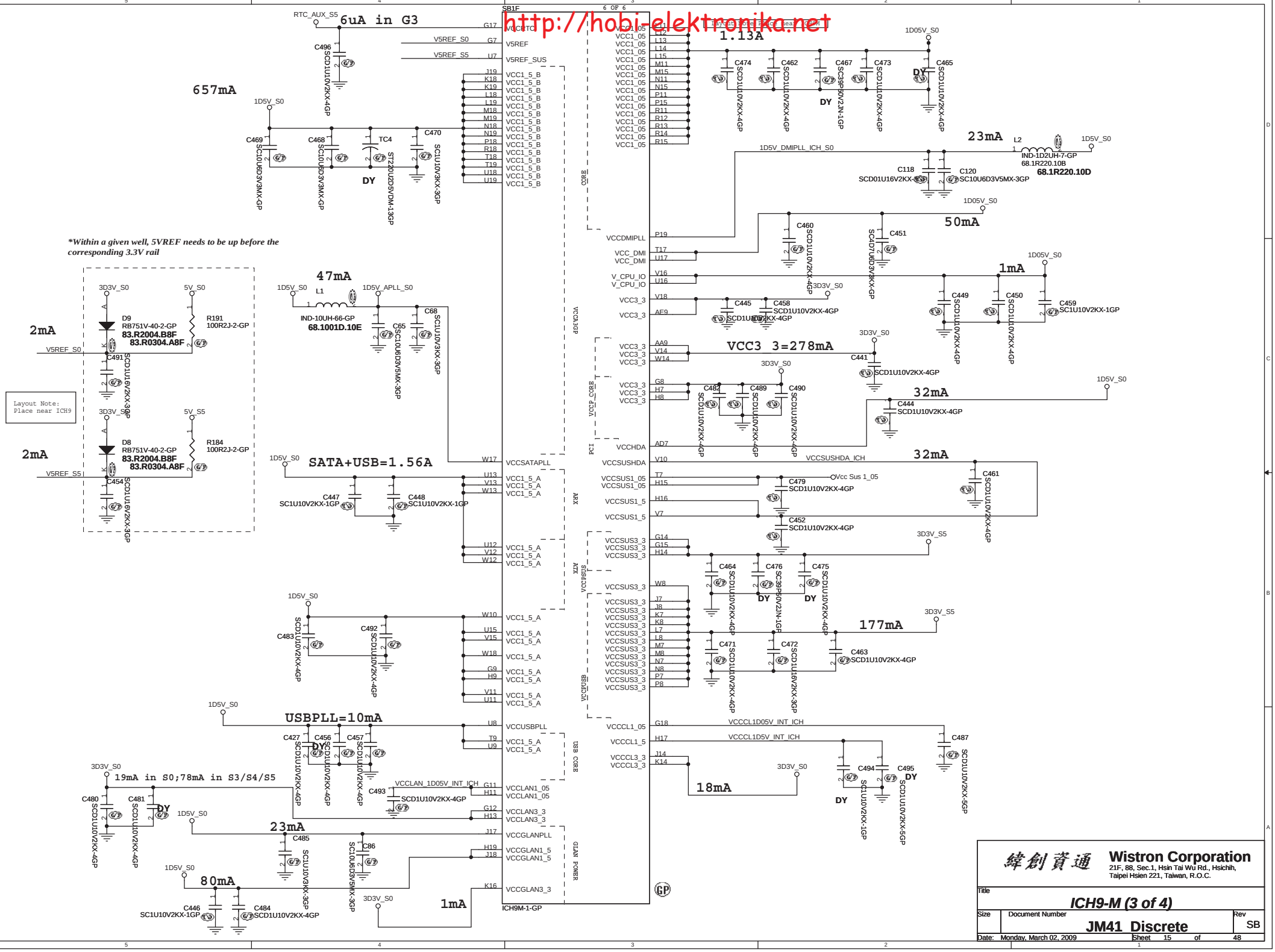

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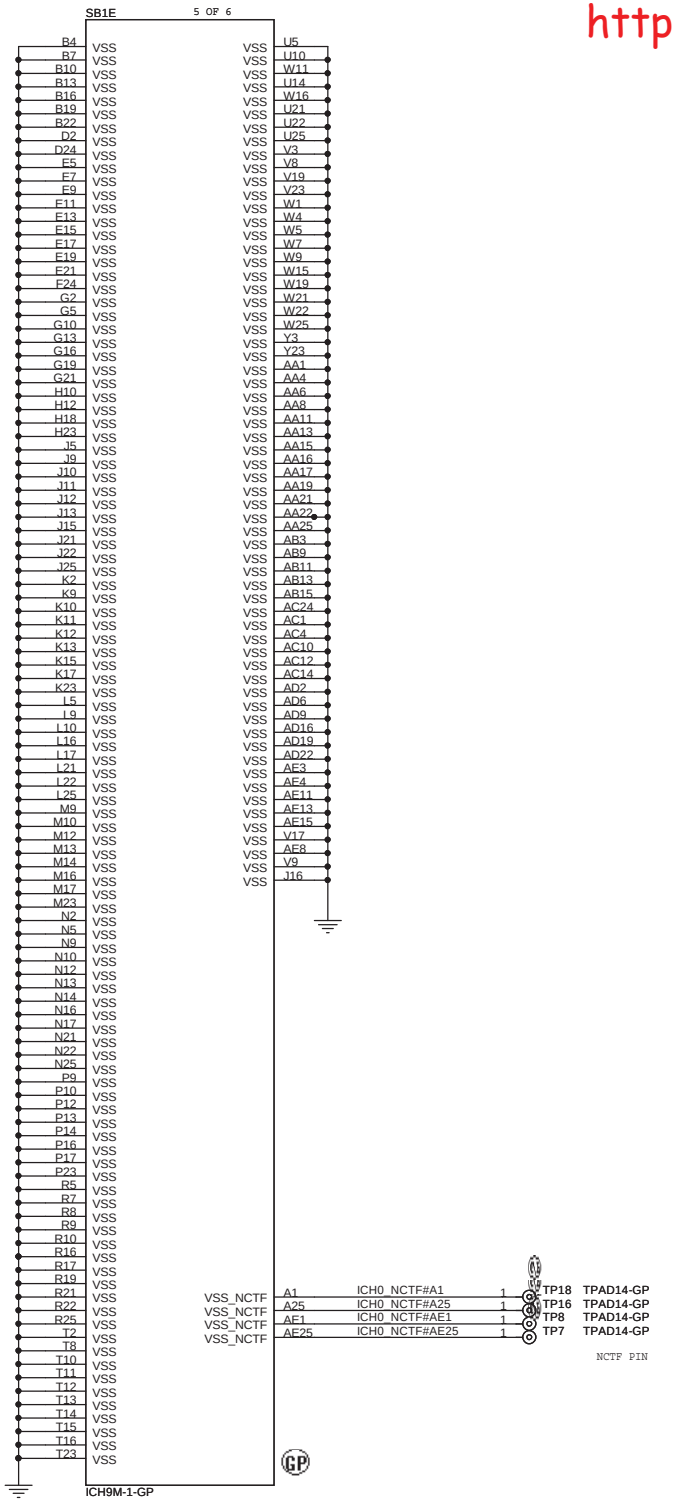

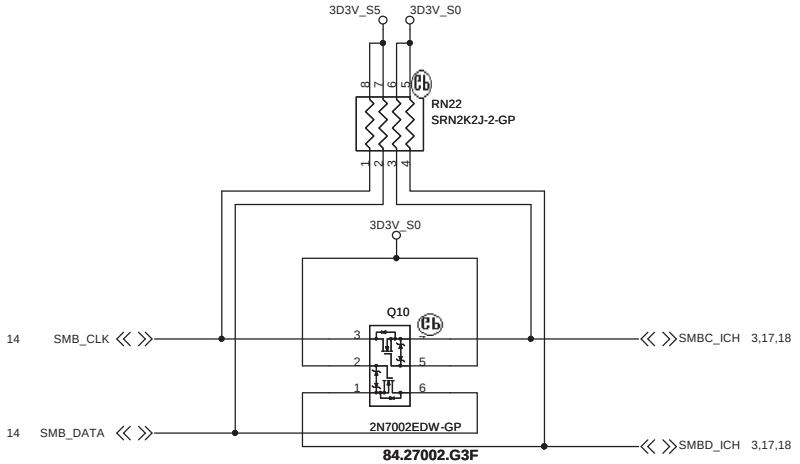

SMBUS

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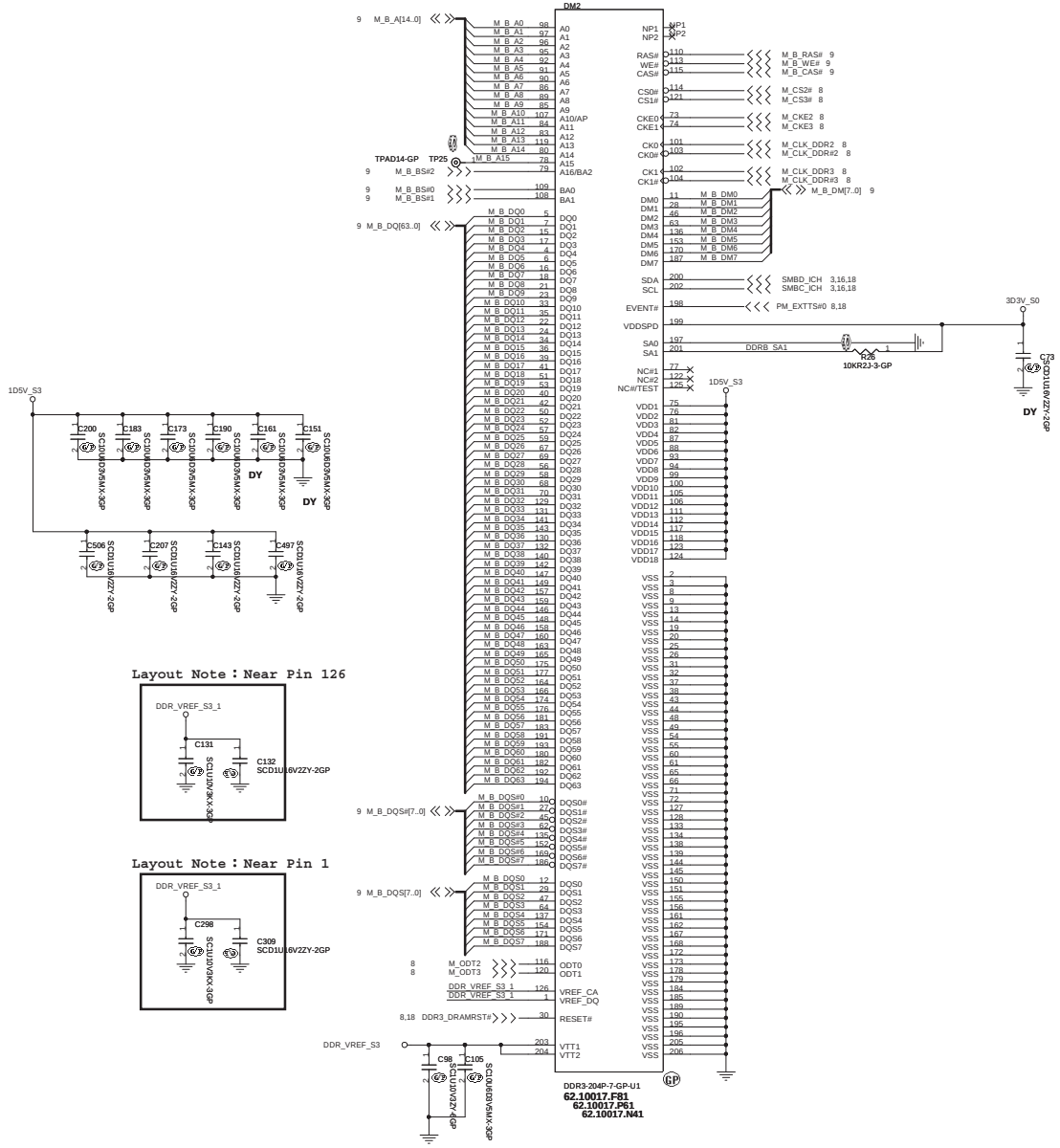
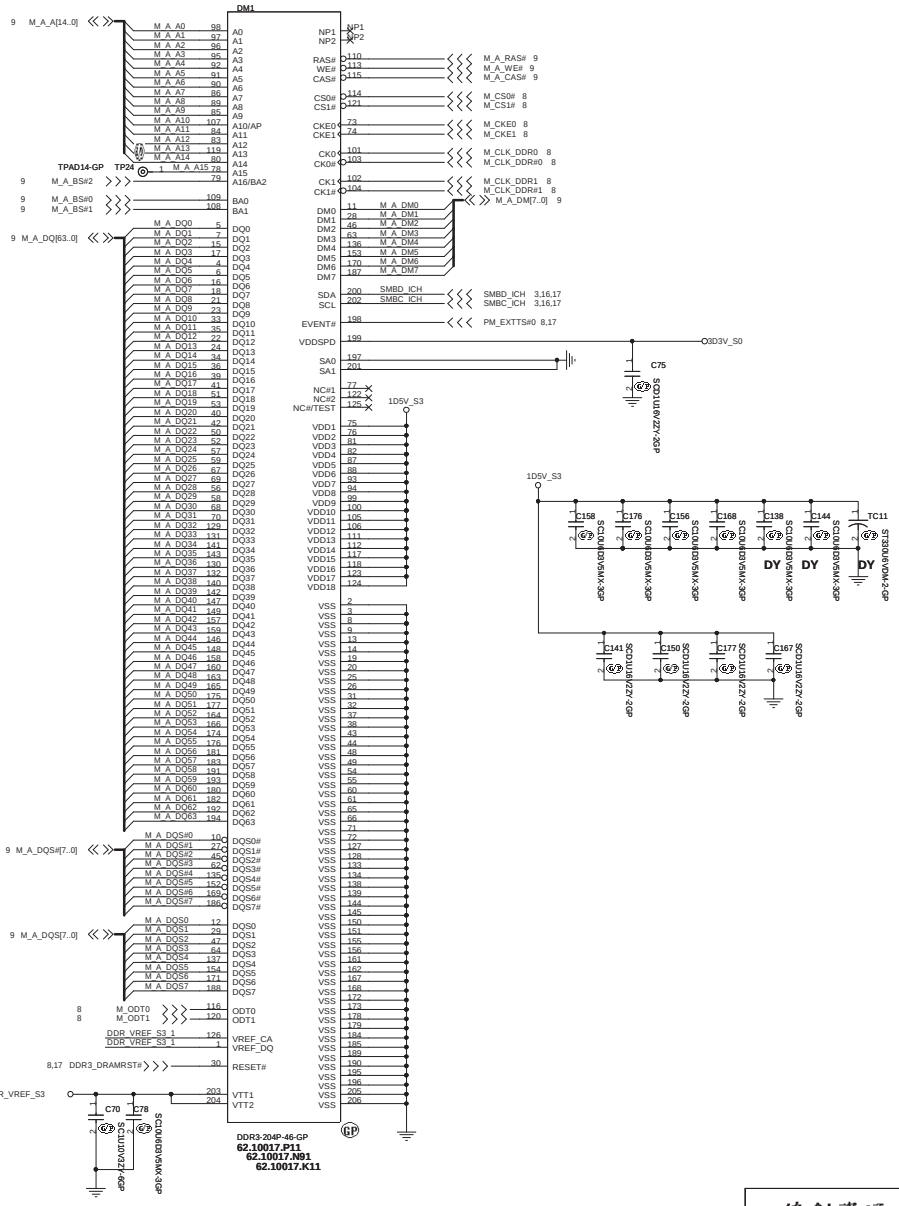
DDR3 SOCKET_1

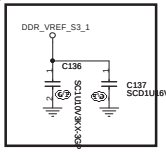


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	DDR3 Socket1		
Size	Document Number	Rev	
	JM41_Discrete	SB	
Date: Monday, March 02, 2009	Sheet 17 of 48		

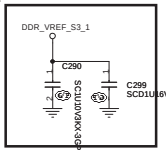
DDR3 SOCKET_2



Layout Note : Near Pin 126



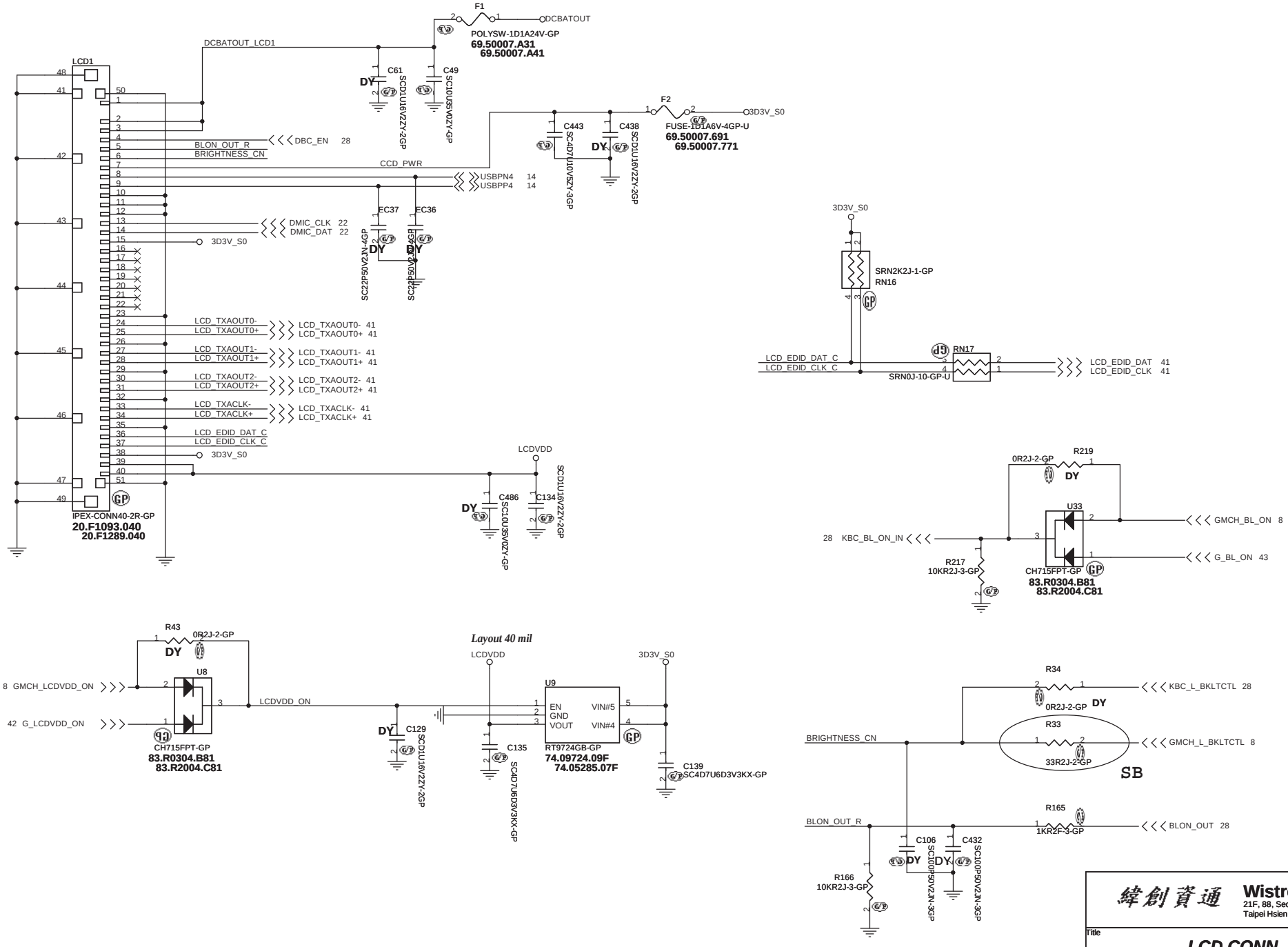
Layout Note : Near Pin 1



緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DDR3 Socket2	
Size	Document Number: JM41_Discrete	Rev: SB
Date: Monday, March 02, 2009	Sheet 18 of 48	

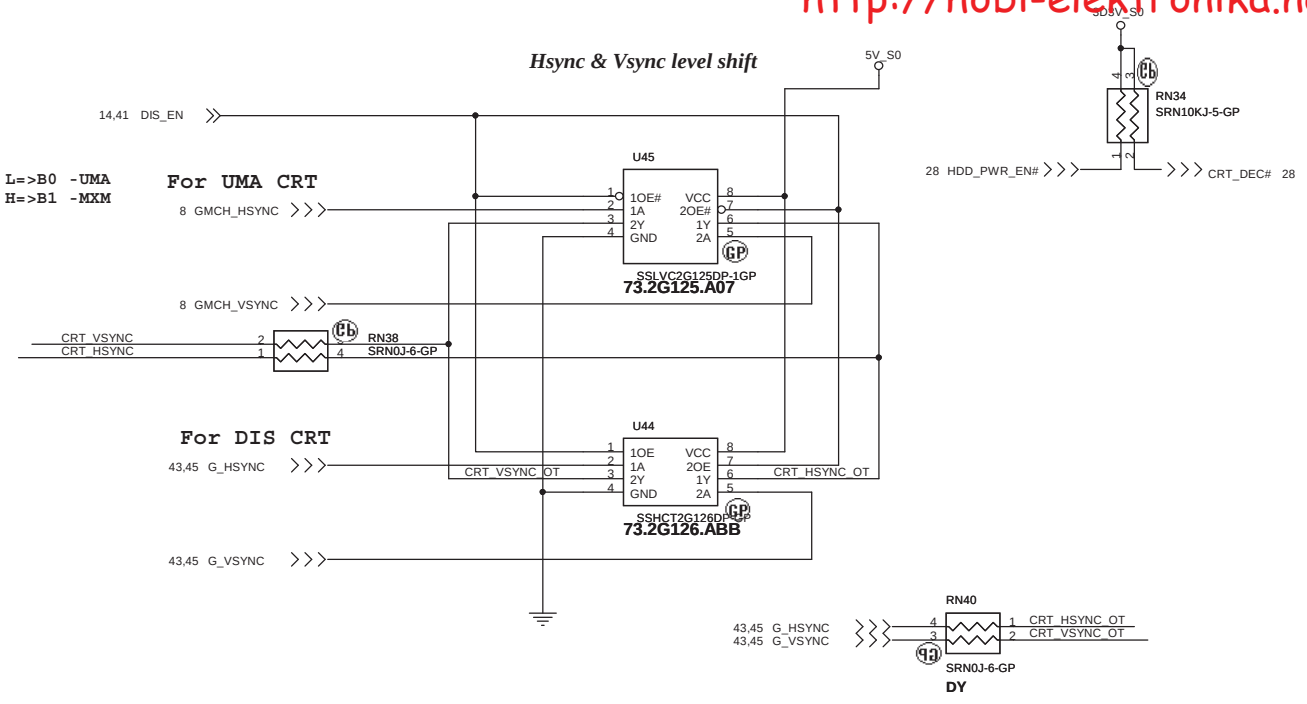
LCD/CCD CONN

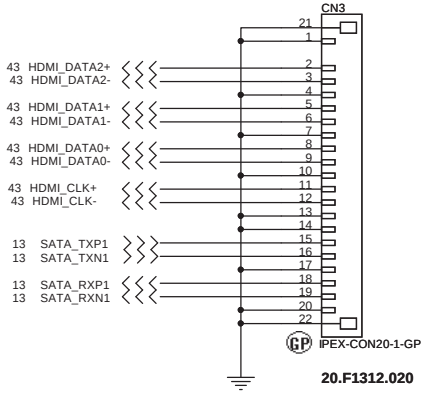
Internal MIC



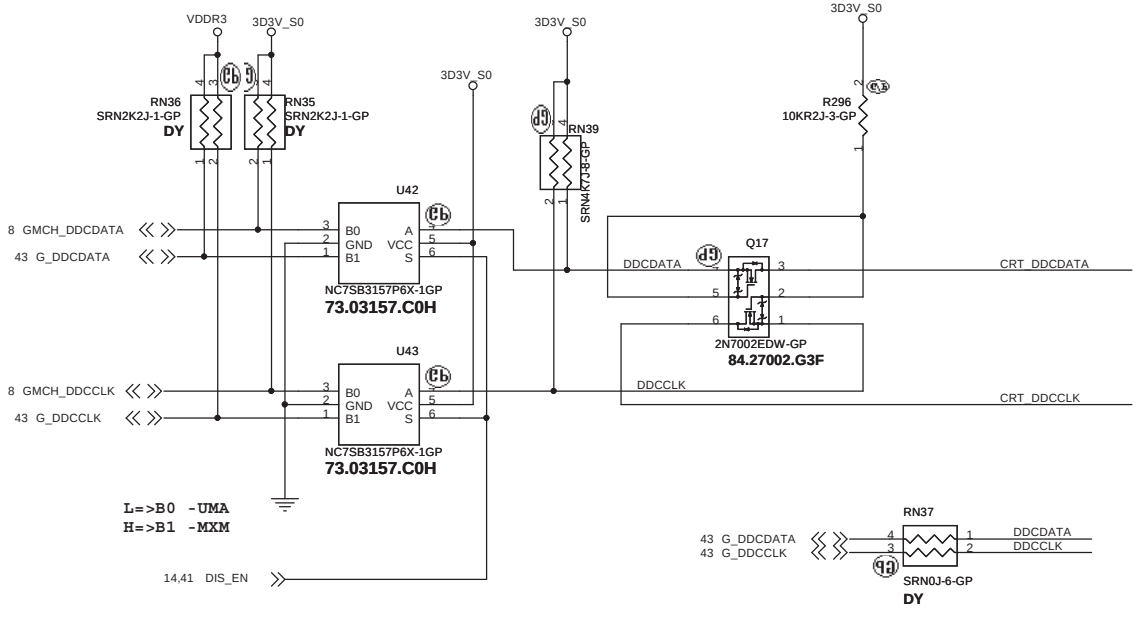
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LCD CONN**	
Size	Document Number **JM41 Discrete**	Rev SB
Date: Monday, March 02, 2009	Sheet 19 of 48	

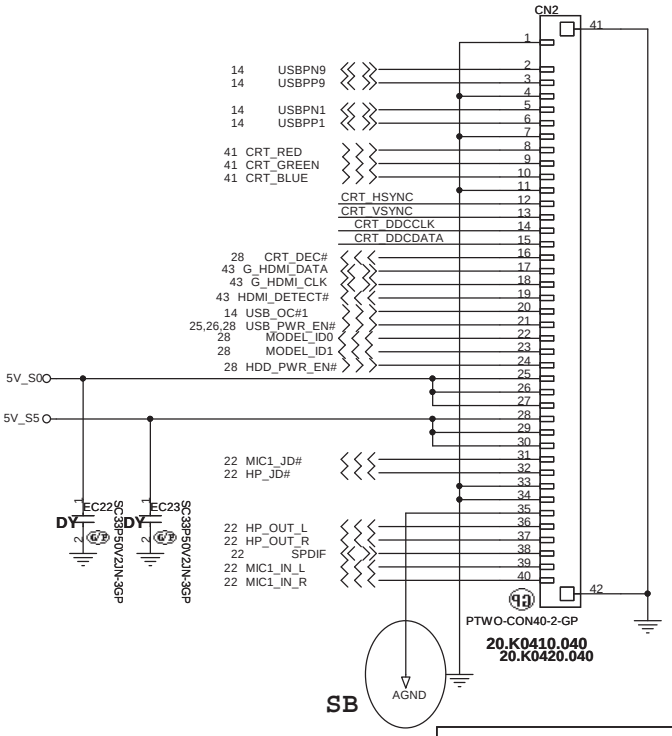
Hsync & Vsync level shift





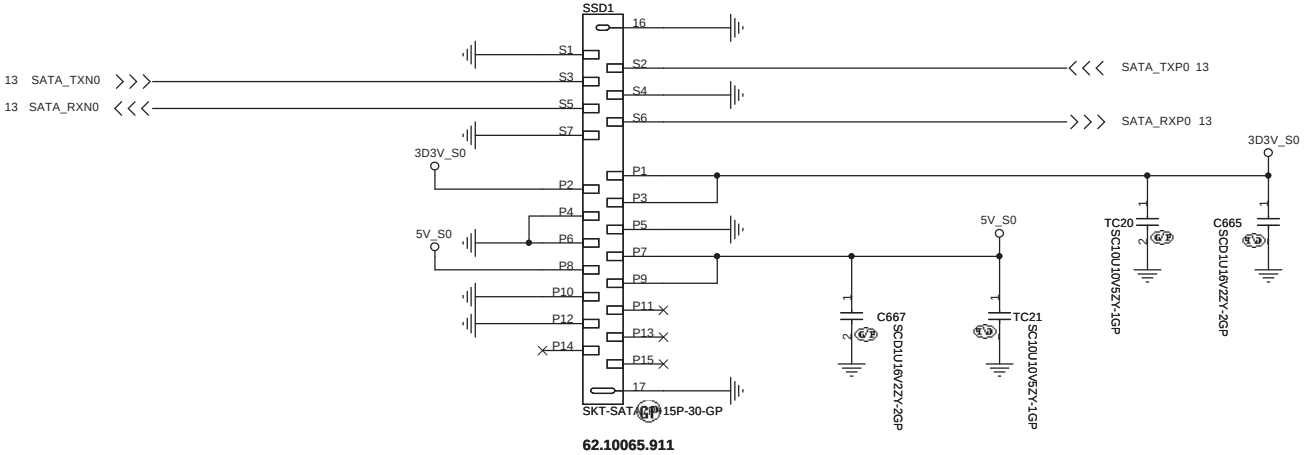
DDC_CLK & DATA level shift



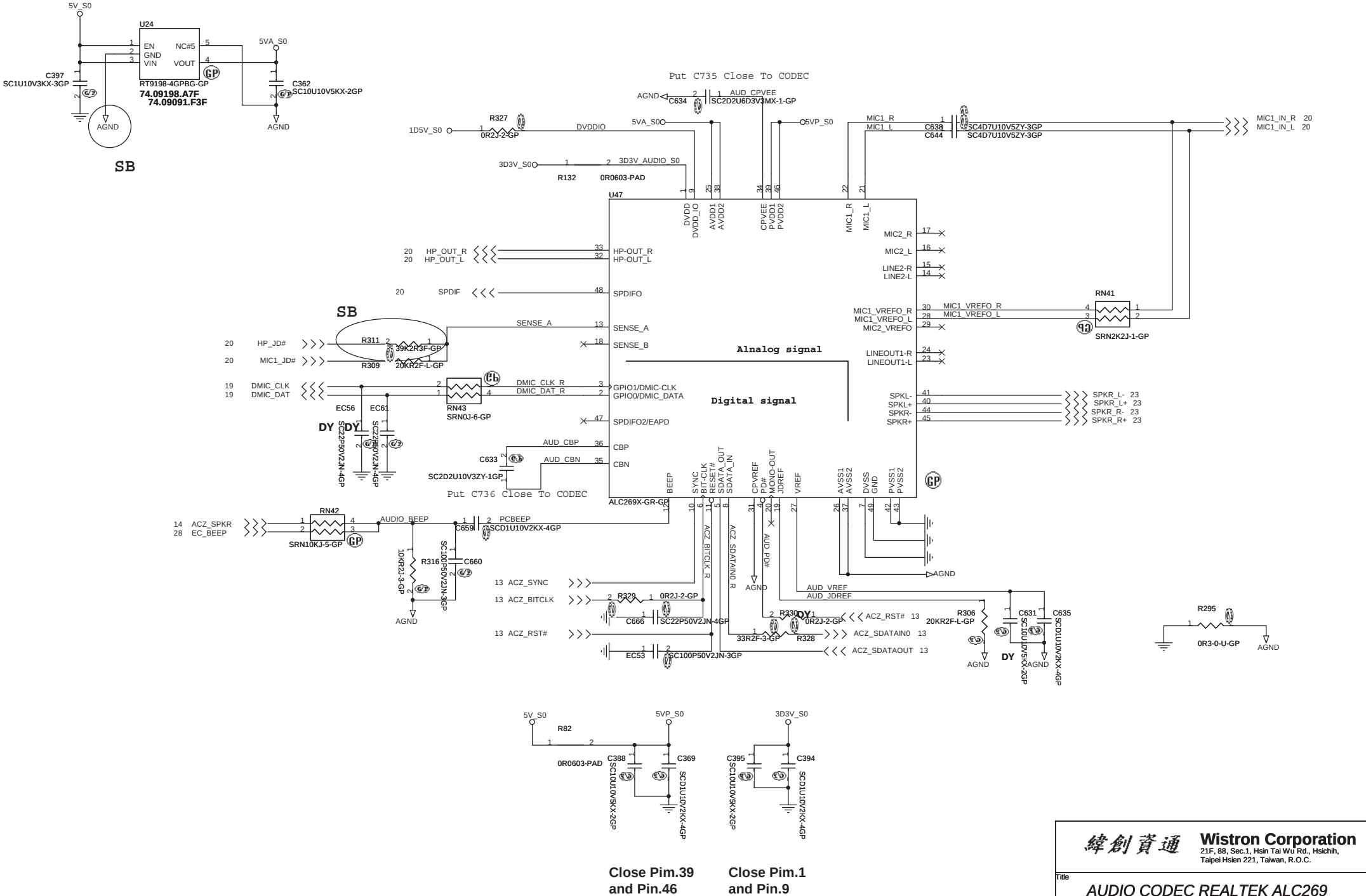


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*CRT BD CONN*	
Size	Document Number: JM41_Discrete	Rev: SB
Date: Monday, March 02, 2009	Sheet 20 of 48	

SSD SATA Connector



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD CONN		
Size	Document Number: JM41 Discrete	Rev: SB
Date: Monday, March 02, 2009	Sheet 21 of 48	



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO CODEC REALTEK ALC269*

Size	Document Number	Rev
	JM41_Discrete	SB

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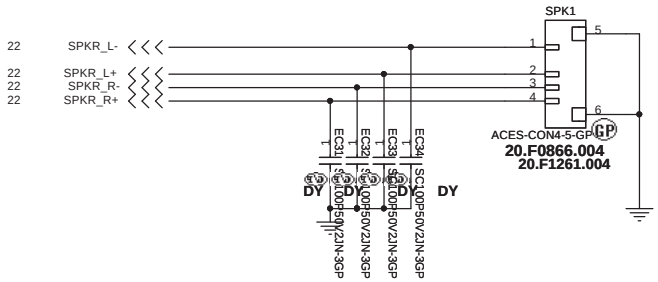
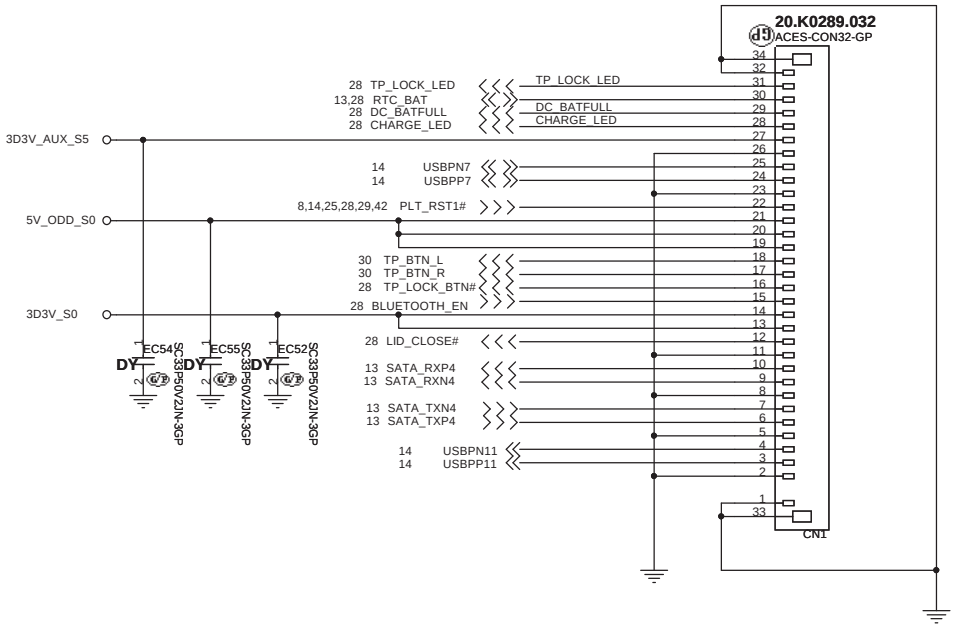
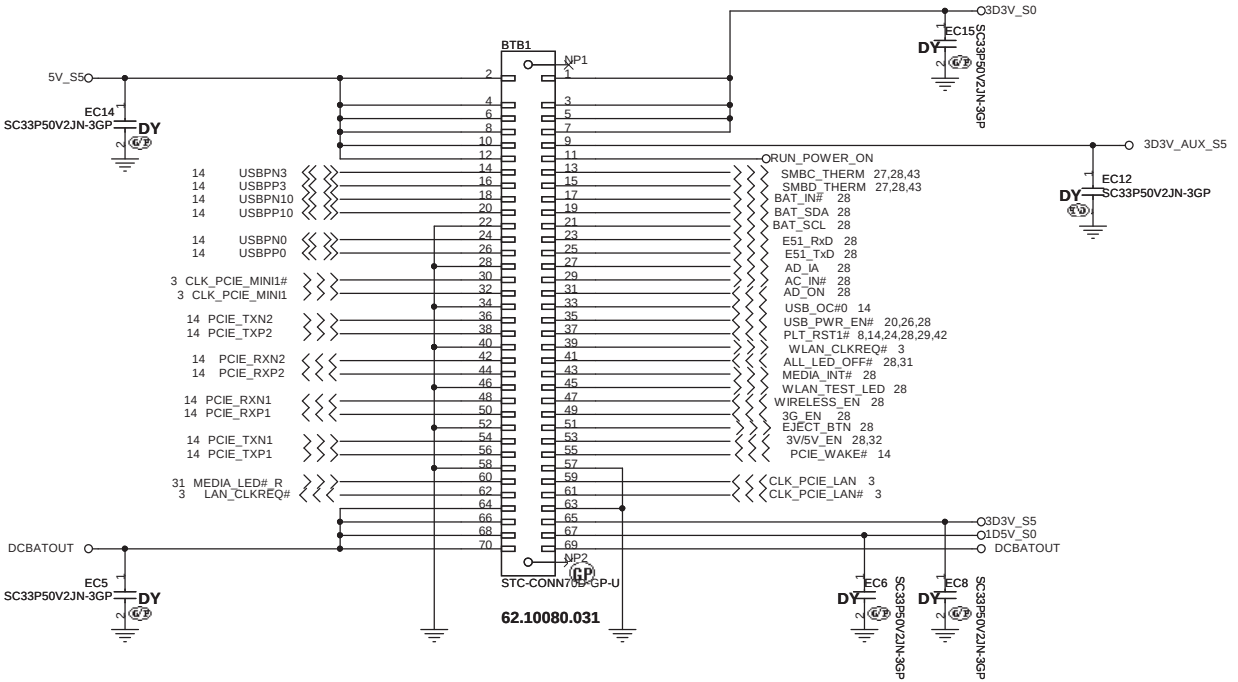
Internal Speaker



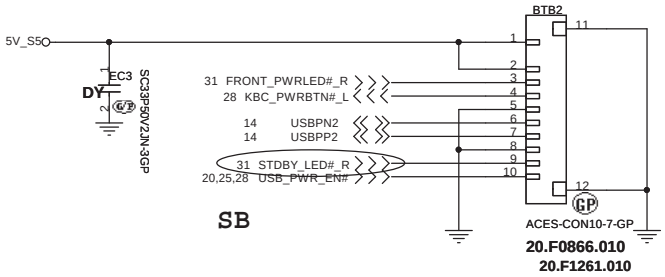
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO JACK*		
Size	Document Number: JM41_Discrete	Rev: SB
Date: Monday, March 02, 2009	Sheet 23 of 48	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*CARDREADER BD CONN*	
Size	Document Number: JM41 Discrete	Rev: SB
Date: Wednesday, March 04, 2009	Sheet 24 of 48	



緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: MINI BD CONN		
Size: A3	Document Number: JM41_Discrete	Rev: SB
Date: Tuesday, March 03, 2009	Sheet 25 of 48	



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER BUTTON CONN

Size	Document Number	Rev
A3	JM41_Discrete	SB

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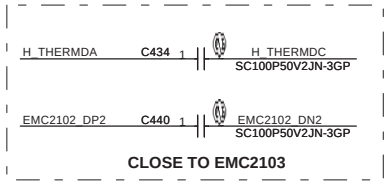
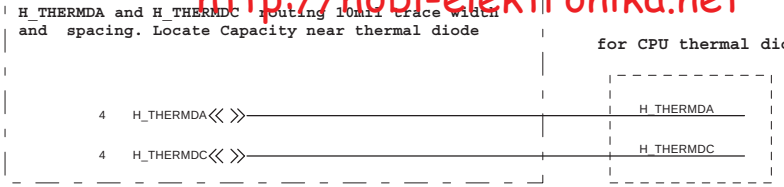
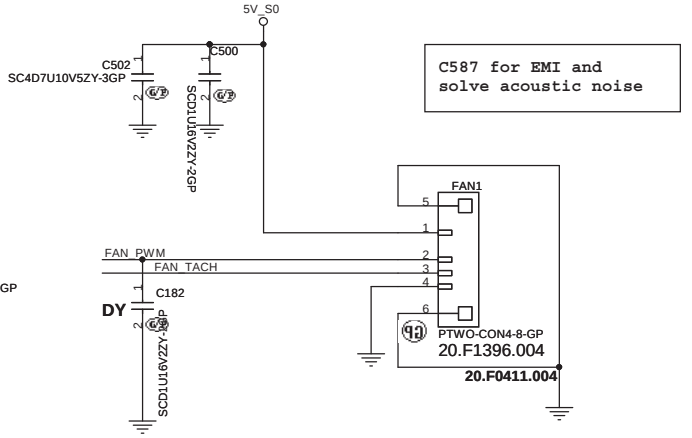


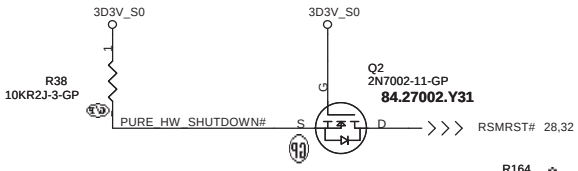
CPU TEMP:

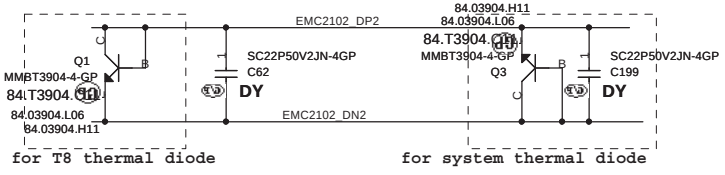
H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near thermal diode

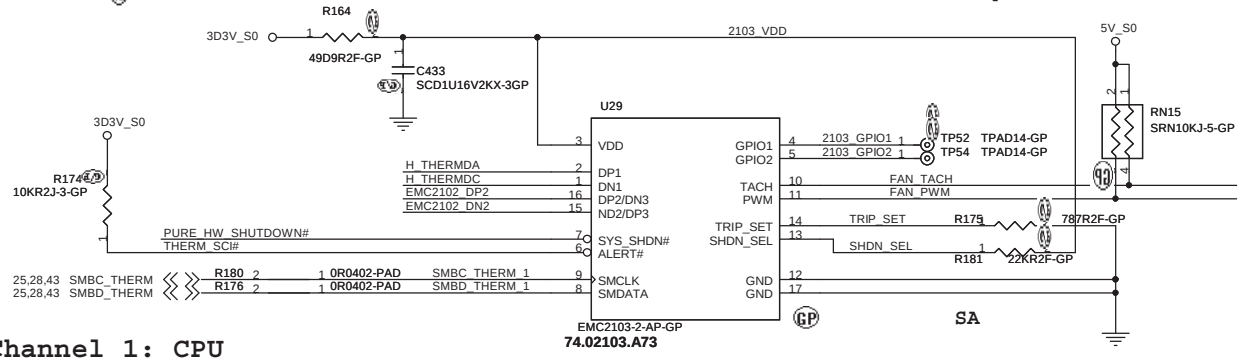




ps. FAN1 POWER TRACE WIDTH MAY BE IN 25 MIL







Channel 1: CPU
Channel 2: Palmrest
Channel 3: T8

SHDN_SEL

PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED,REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED,REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED,REC ENABLED

TRIP_SET

Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor
Size: Document Number: JM41 Discrete
Rev: SB
Date: Monday, March 02, 2009
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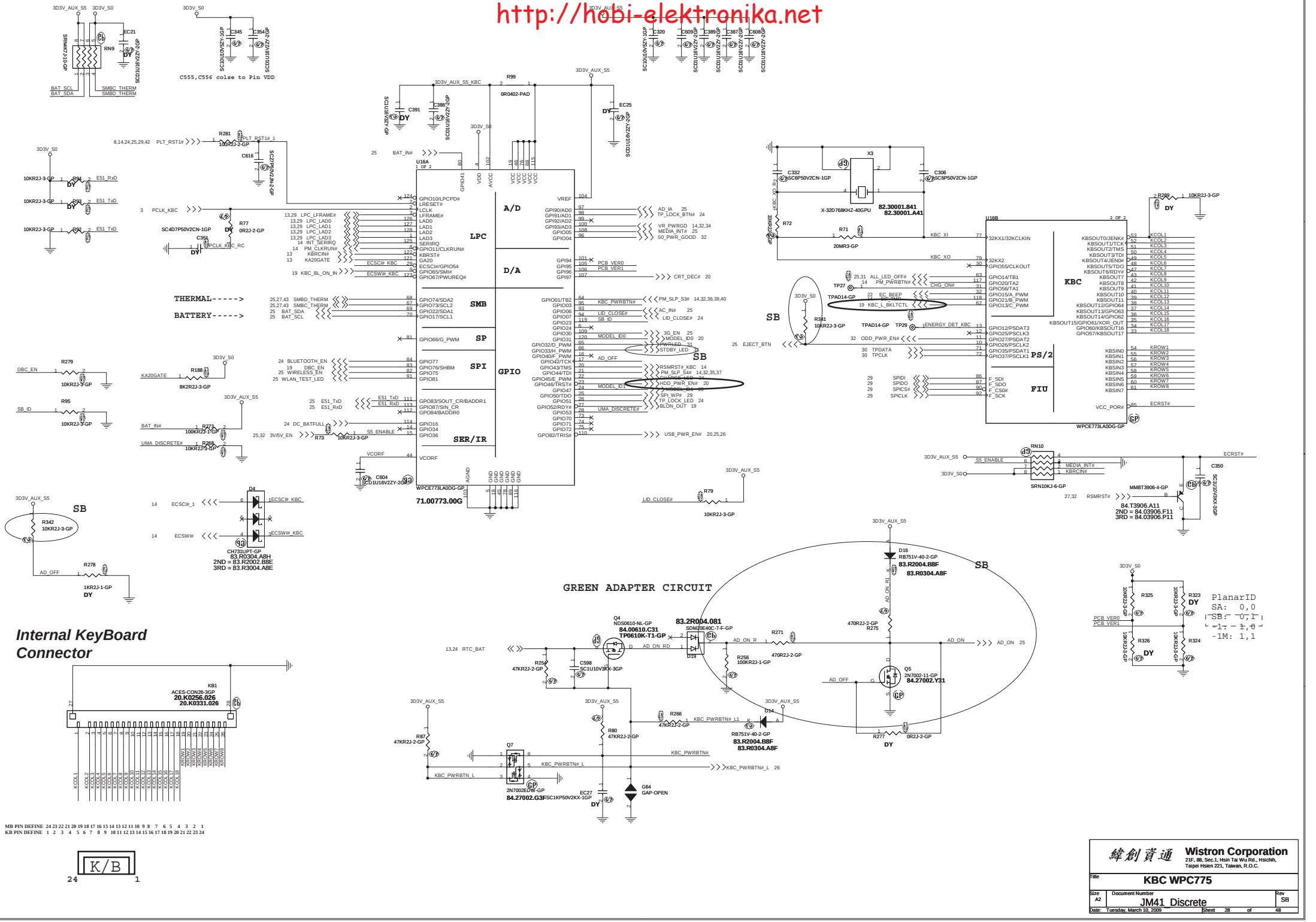
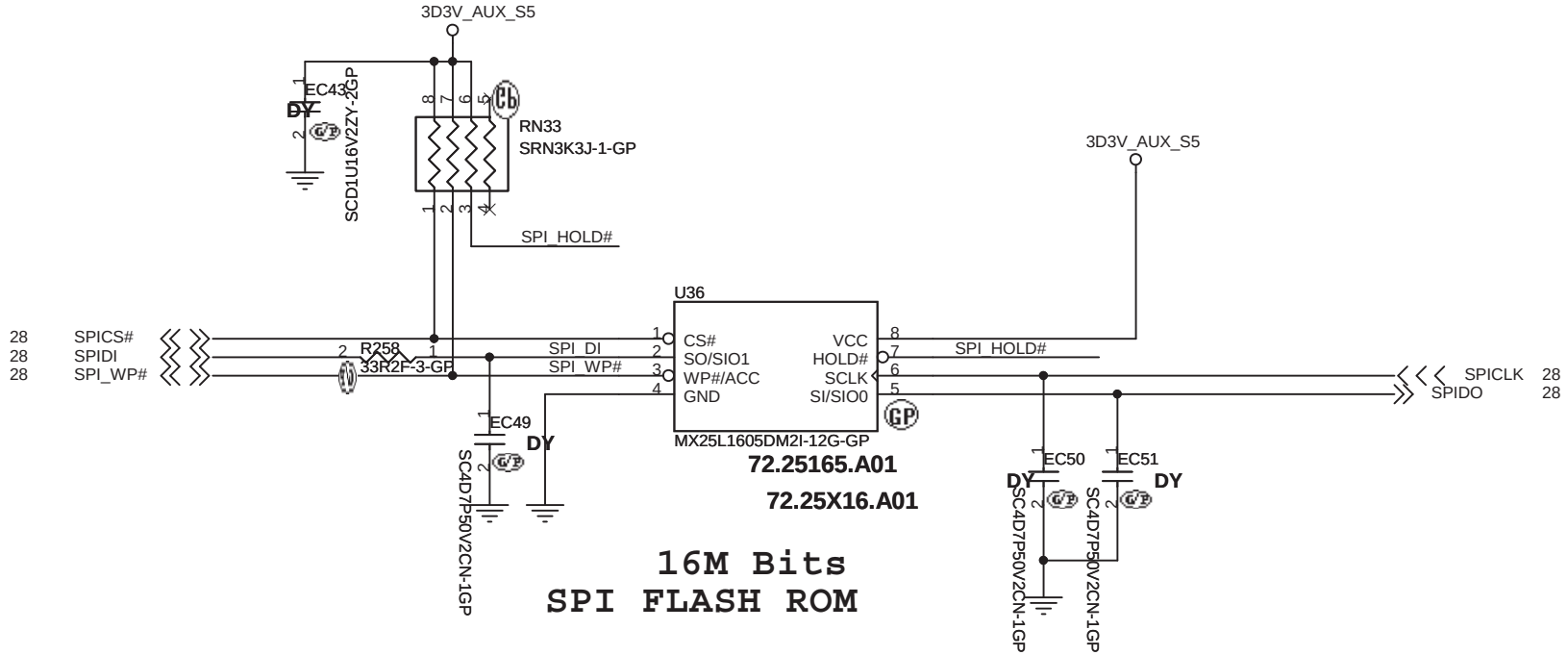
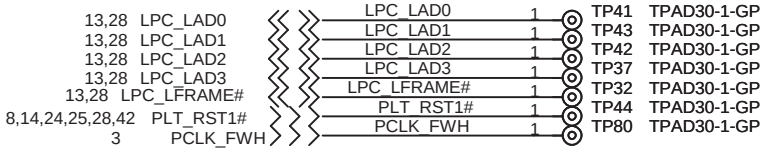
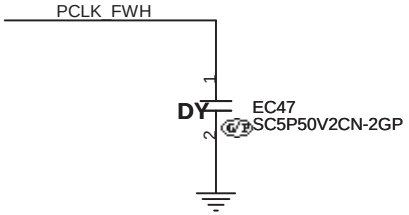




GOLDEN FINGER FOR DEBUG BOARD

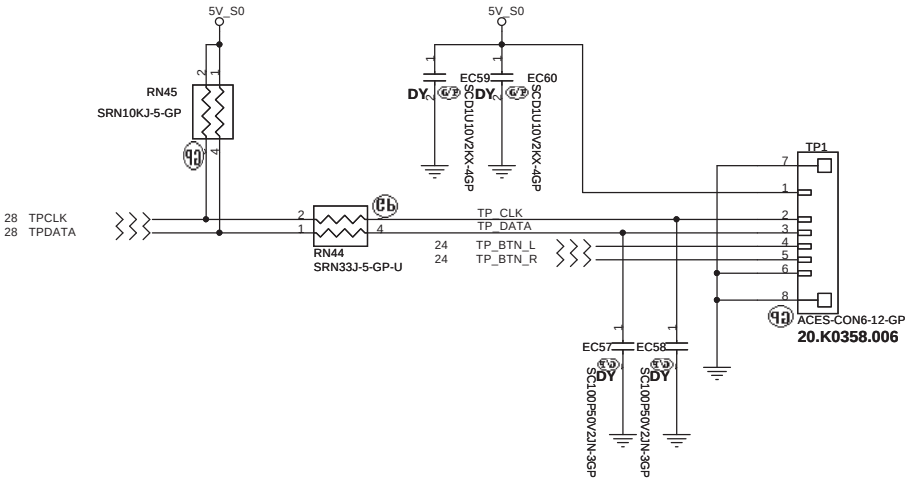




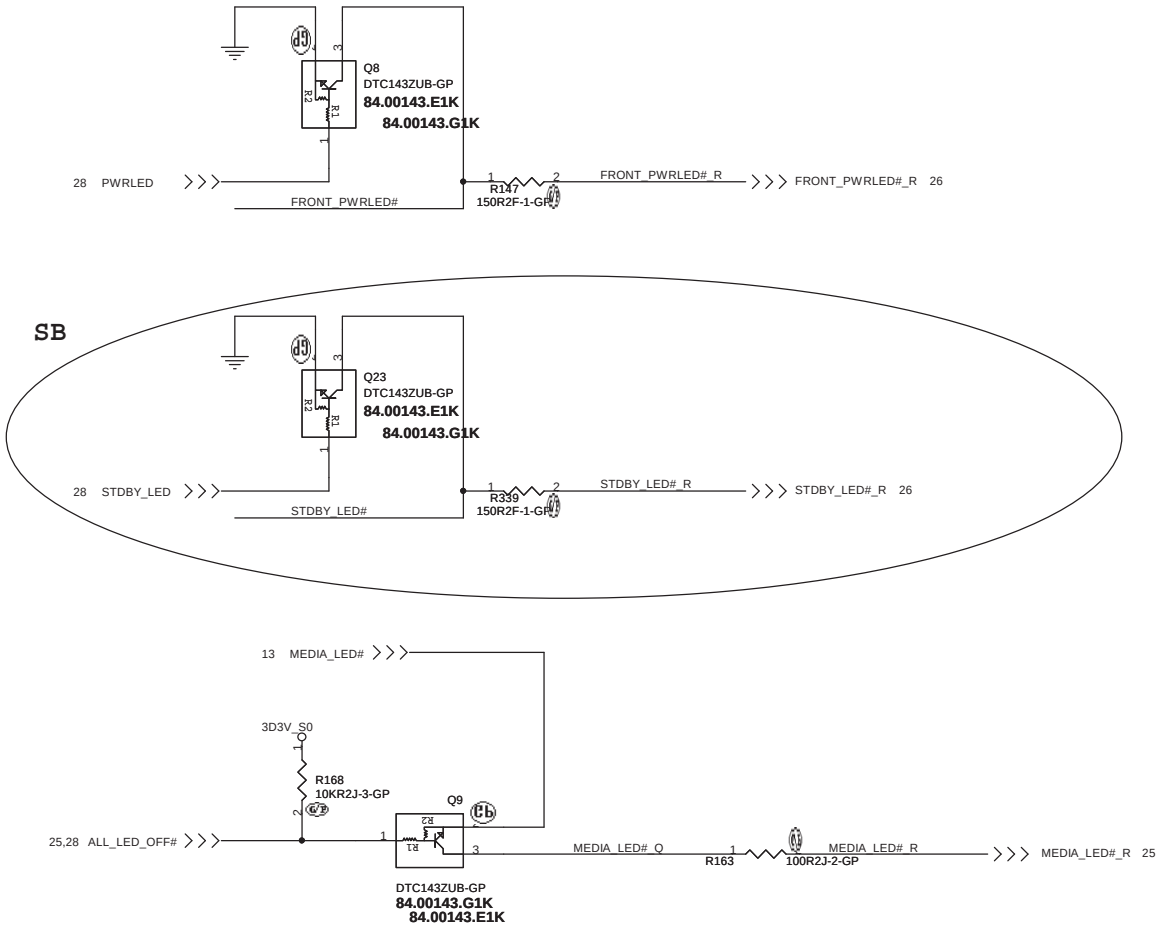
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BIOS***	
Size	Document Number **JM41 Discrete**	Rev SB
Date: Monday, March 02, 2009	Sheet 29 of 48	

TOUCH PAD

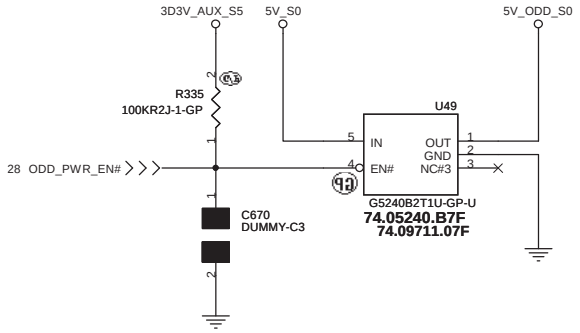


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Touch PAD*		
Size	Document Number: JM41_Discrete	Rev: SB
Date: Monday, March 02, 2009	Sheet 30 of 48	

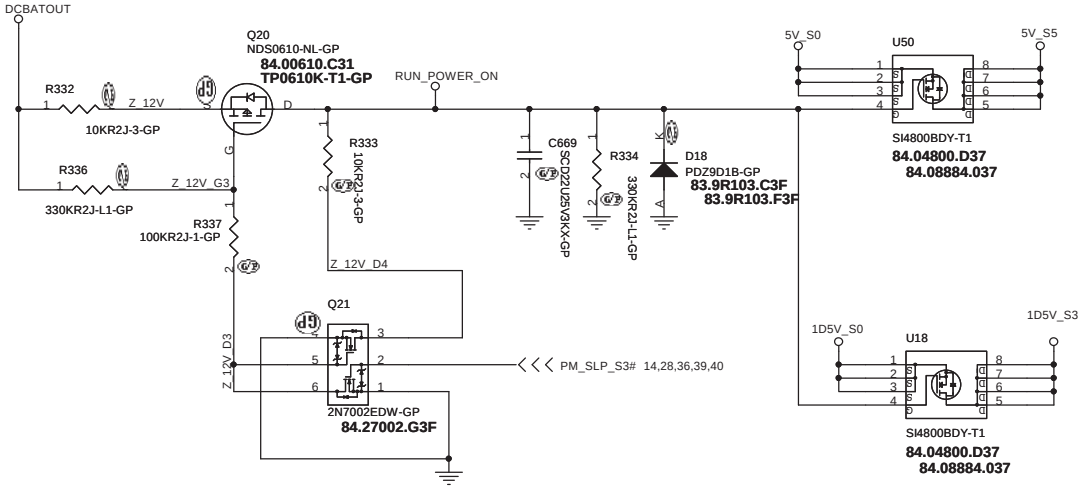


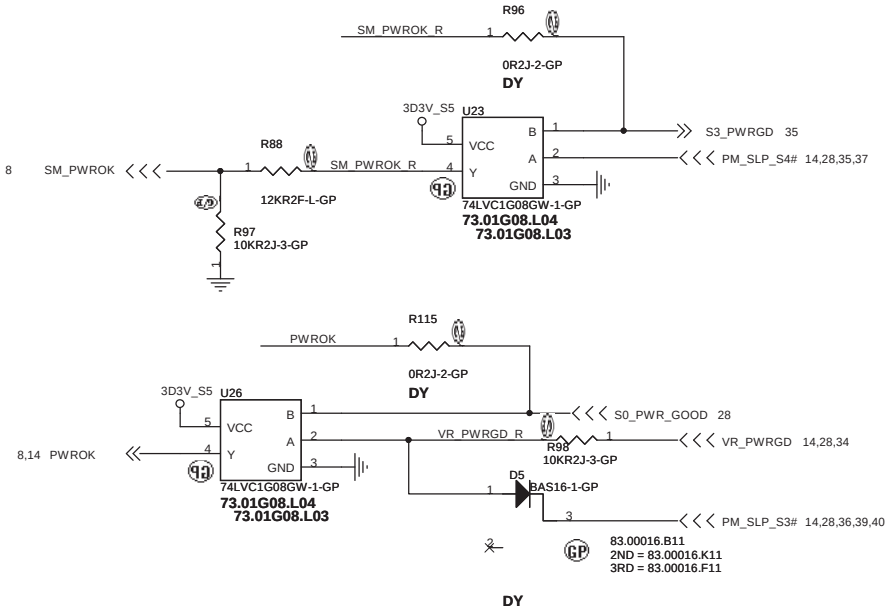
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LED**	
Size	Document Number **JM41_Discrete**	Rev SB
Date: Monday, March 02, 2009	Sheet 31 of 48	

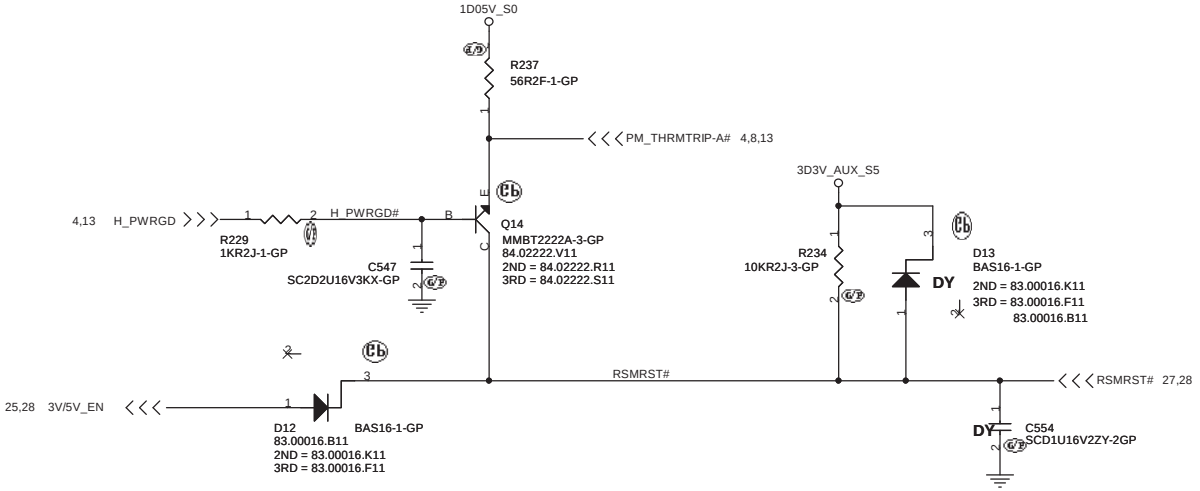
ODD Power



Run Power







緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	RUN & ODD POWER	
Size	Document Number JM41_Discrete	Rev SB
Date: Monday, March 09, 2009	Sheet 32 of 48	

CPU_CORE
ISL6261A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6261A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

Output Power
VCC_CORE_PWR(O)

VR_PWROK
VCC_CORE(Imax=18A)

RT8202 1D05V_S0

DCBATOUT_8202_1D05V
PM_SLP_S3#

VIN
EN
1D5V(O)
PGOOD

1D05V_S0 (10A)
CPUCORE_ON

RT8202 1D5V_S3

DCBATOUT_8202_1D5V
PM_SLP_S4#

VIN
EN
1D5V(O)
PGOOD

1D5V_S3 (11A)
CPUCORE_ON

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT_6263A

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

Output Power
VGFXCORE (O)

CPUCORE_ON
VCC_GFXCORE(7A)

RT9026 0D9V_S0

5V_S5
1D5V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5
VTT
VTTREF

0D75V_S3 (1.2A)
0D75V_S3_1

Charger MAX8731A

CHG_ON#
24750_CELLS

AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA
BT+
DCBATOUT

TPS51125
5V/3D3V

DCBATOUT_51125
S5_ENABLE
ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (5A)
5V_AUX_S5
3D3V_AUX_S5

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence Logic

Size: B | Document Number: JM41_Discrete | Rev: SB

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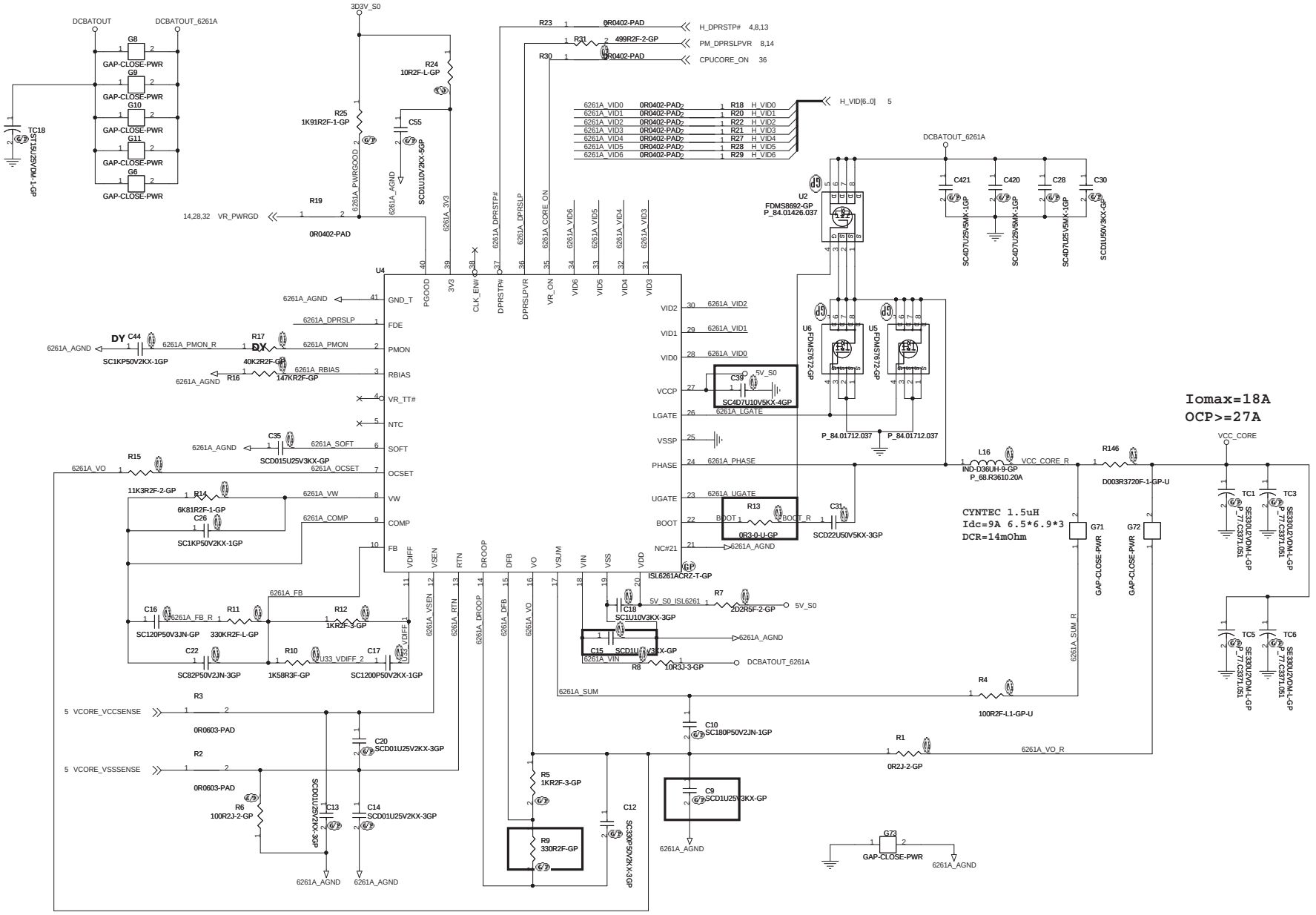
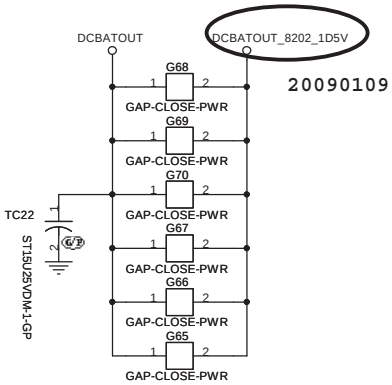
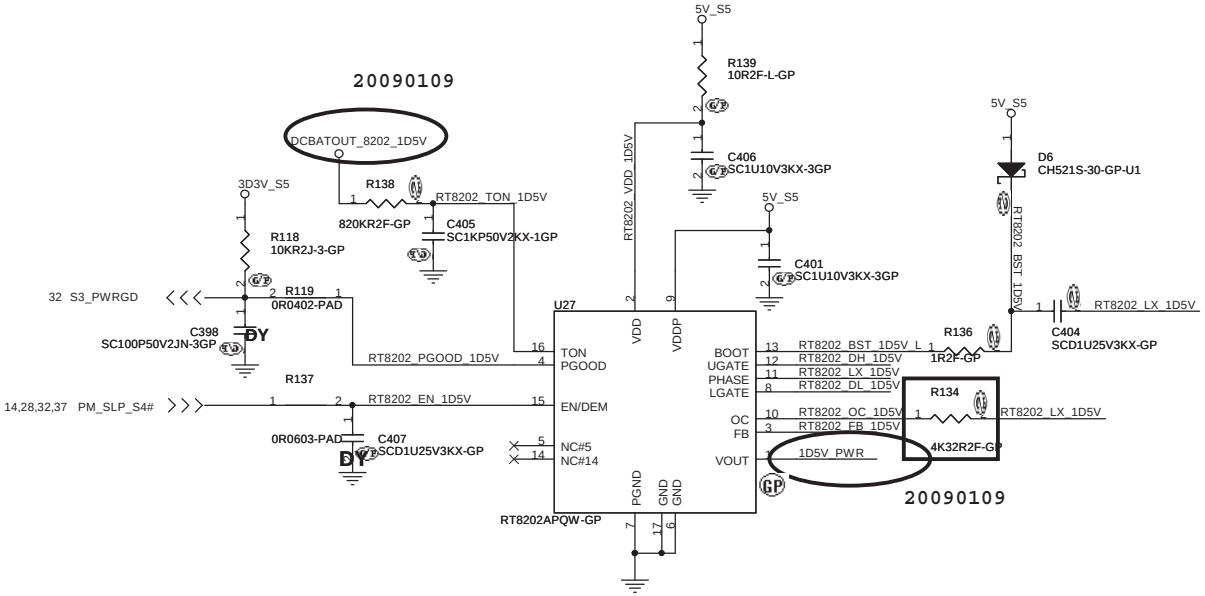
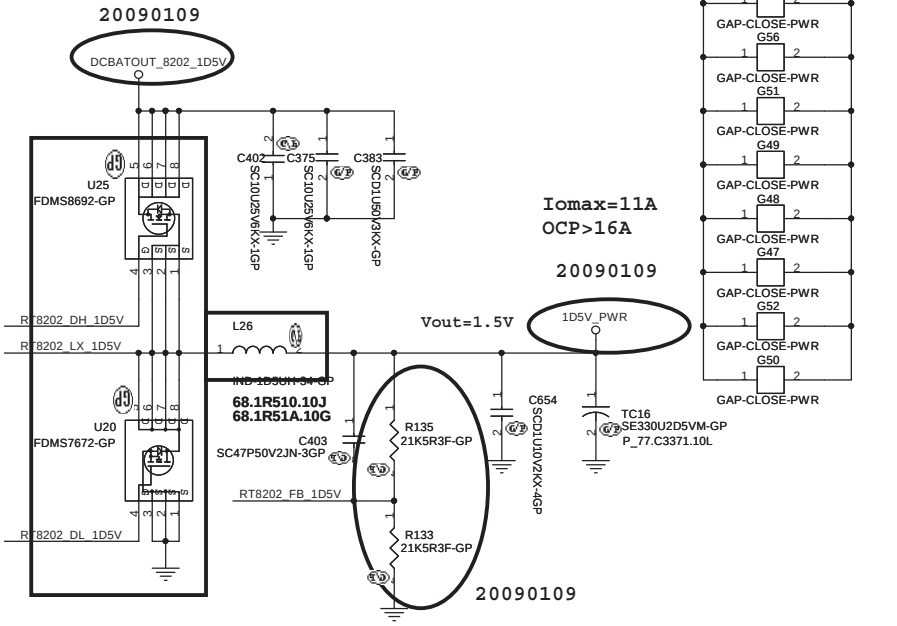


緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ISL6261A_CPU CORE	
Size: Custom	Document Number: JM41_Discrete	Rev: SB
Date: Monday, March 02, 2009	Sheet 34 of 48	

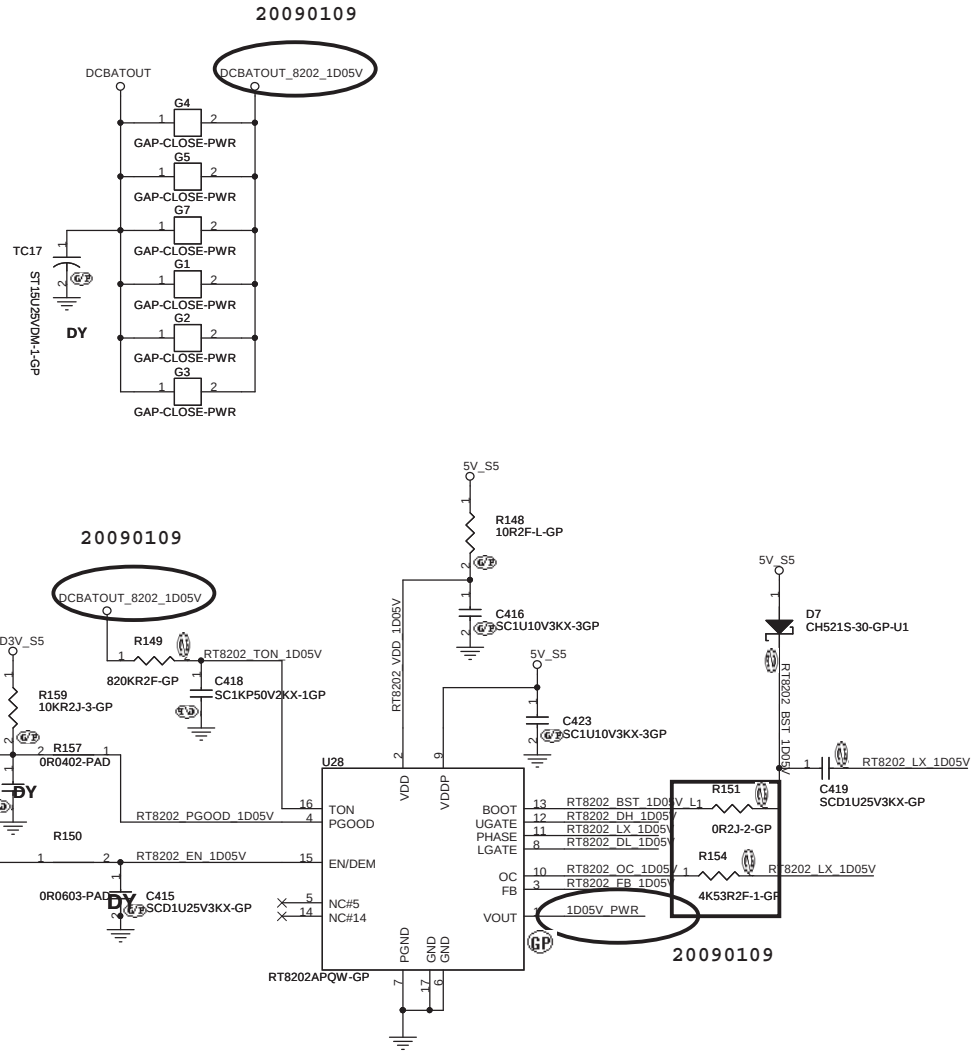






Vout=0.75*(1+Rh/Rl)

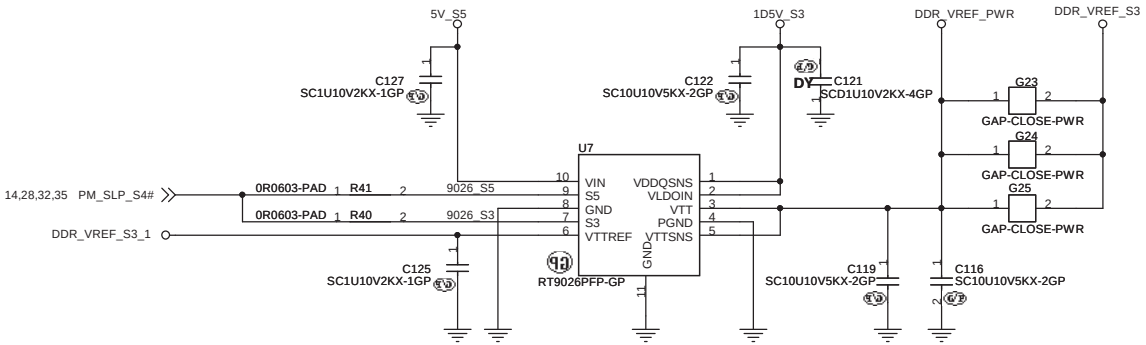
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RT8202_1D5V		
Size: A3	Document Number: JM41_Discrete	Rev: SB
Date: Thursday, March 05, 2009	Sheet 35 of 48	



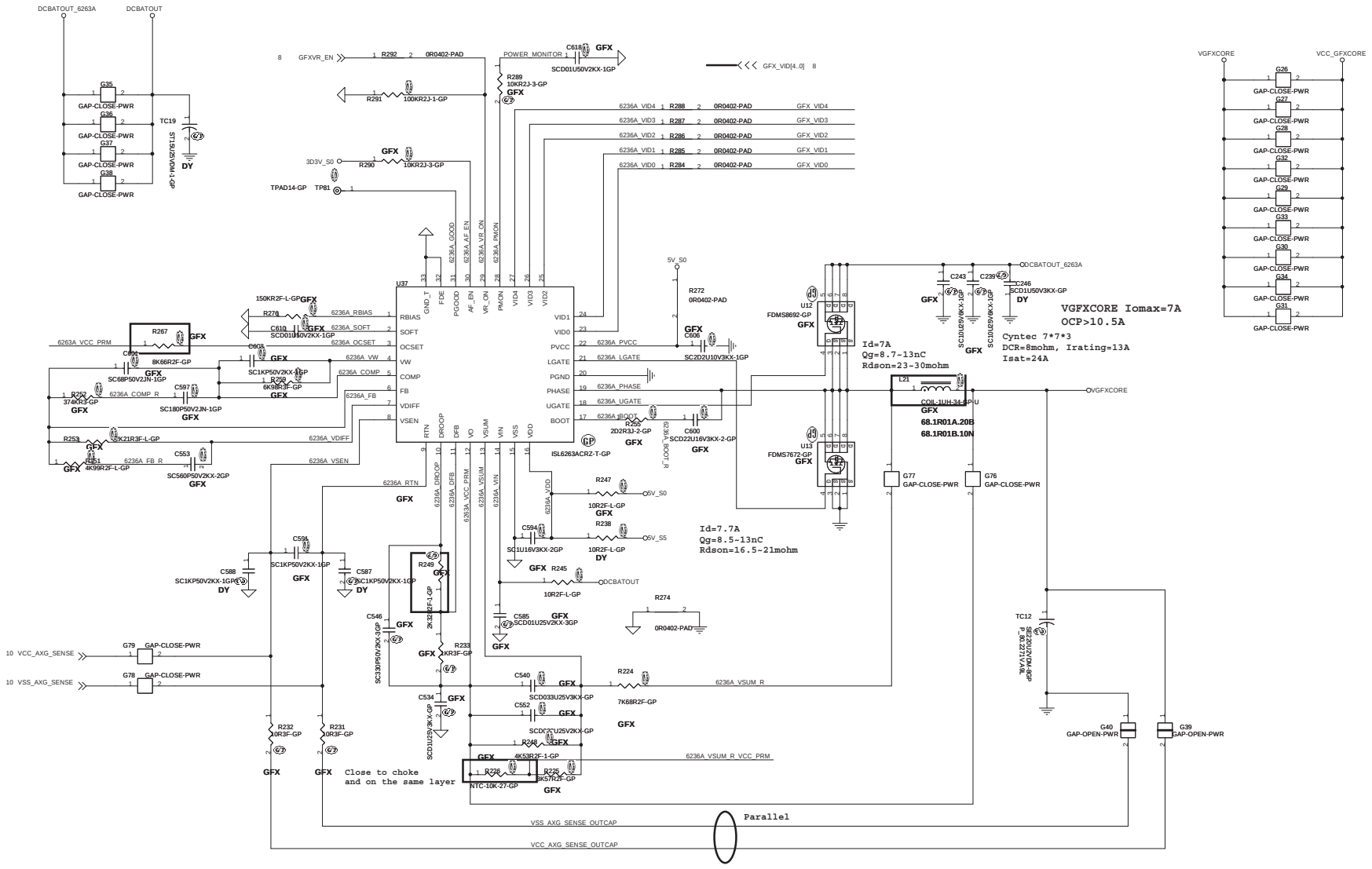
Vout=0.75*(1+Rh/Rl)

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: RT8202_1D05V		
Size: A3	Document Number: JM41_Discrete	Rev: SB
Date: Thursday, March 05, 2009	Sheet 36 of 48	

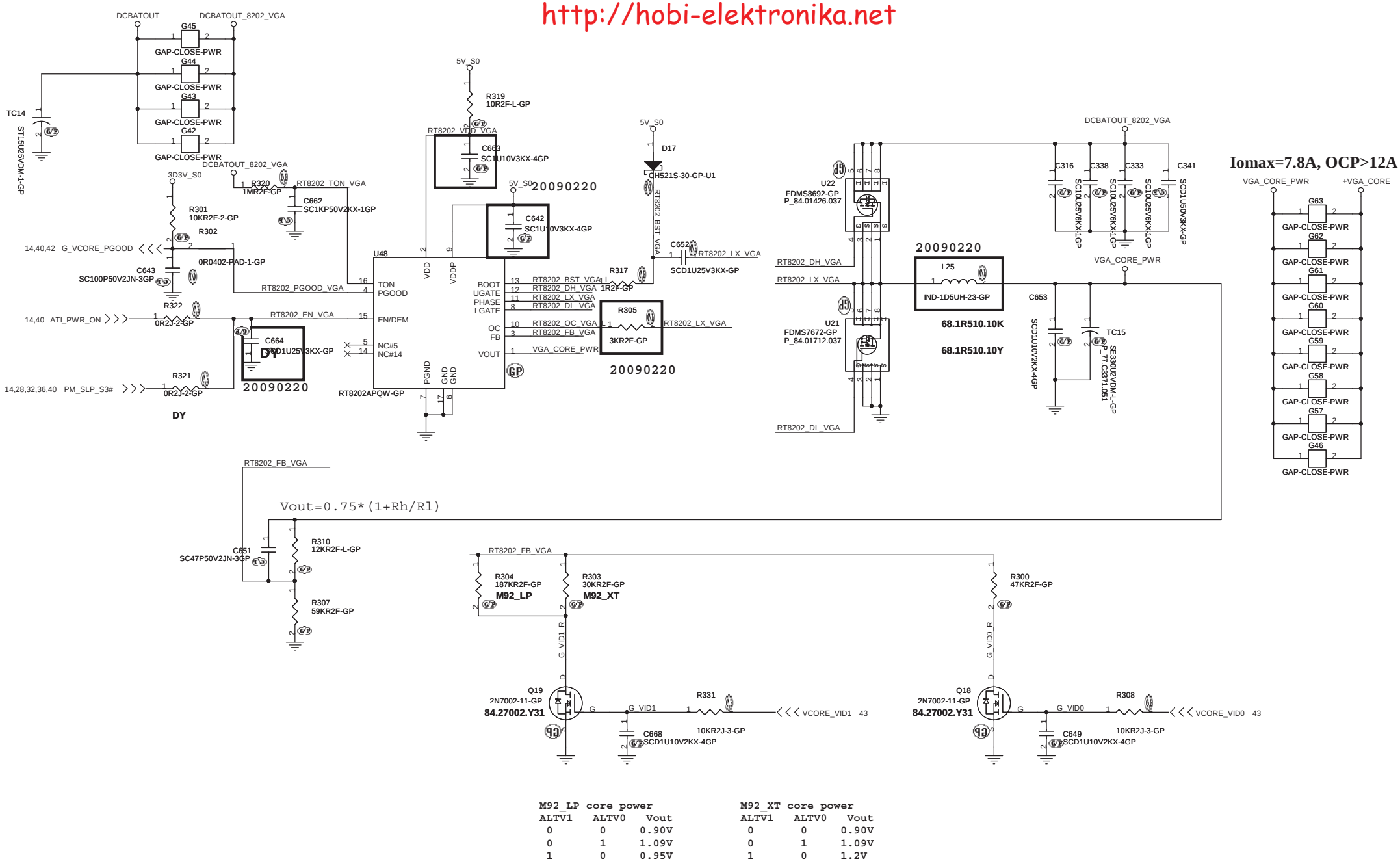
Iomax=1.2A
OCP>2A



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RT9026_0D75V***	
Size A3	Document Number **JM41_Discrete**	Rev **SB**
Date: Monday, March 02, 2009	Sheet 37 of 48	



Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: ISL6263A_GFX CORE			
Size: A2	Document Number: JM41_Discrete	Rev: SB	
Date: Thursday, March 05, 2009	Sheet 38 of 48		



M92_LP core power

ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	0.95V

M92_XT core power

ALTV1	ALTV0	Vout
0	0	0.90V
0	1	1.09V
1	0	1.2V

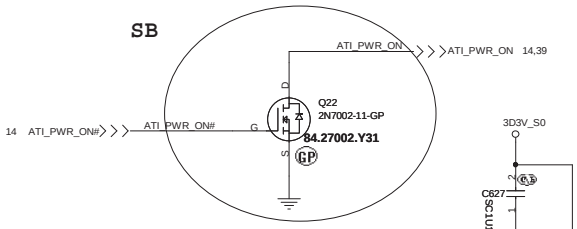
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8202A VGA CORE

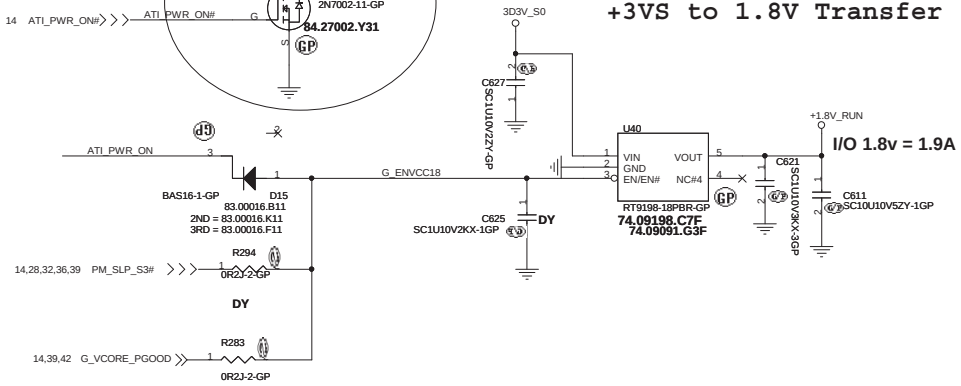
Size: A3 | Document Number: JM41 Discrete | Rev: SB

Date: Thursday, March 05, 2009 | Sheet 39 of 48

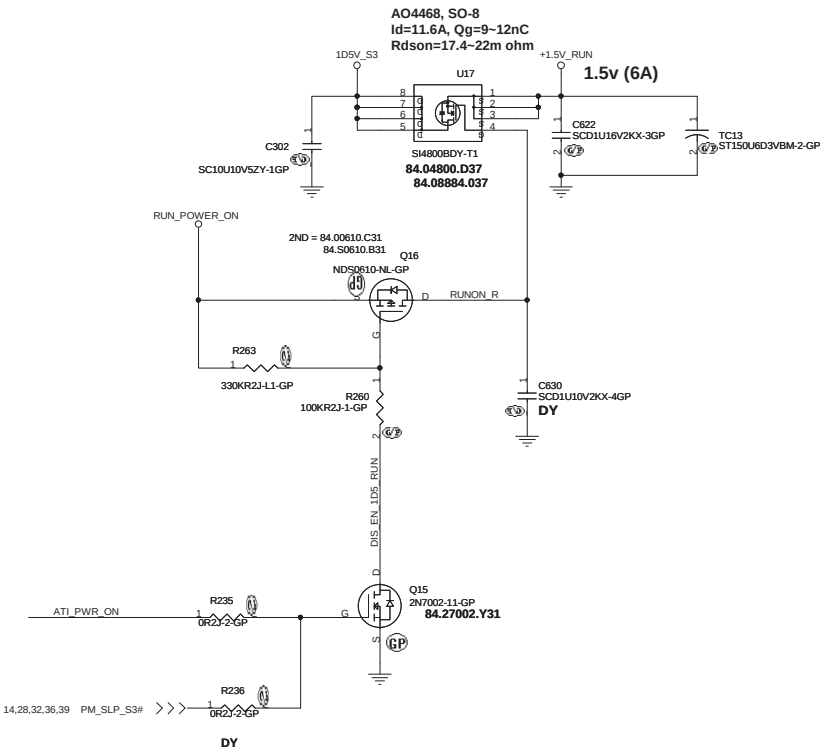
SB



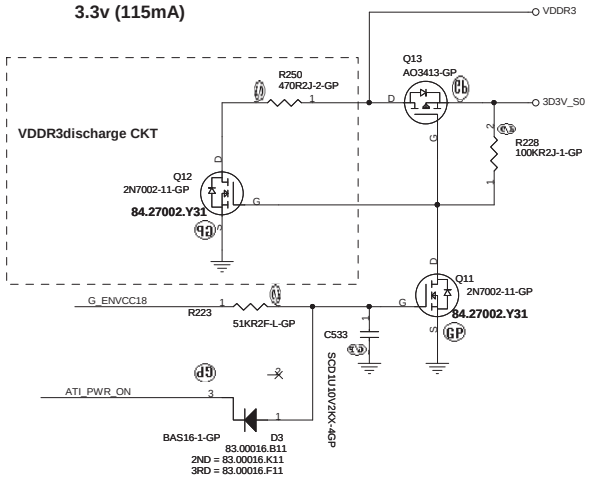
+3VS to 1.8V Transfer



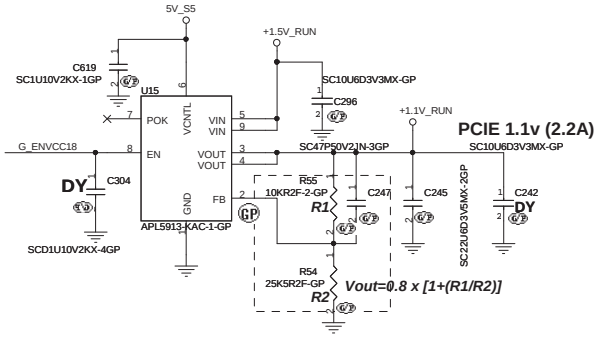
+1.5V to +1.5VS_RUN Transfer



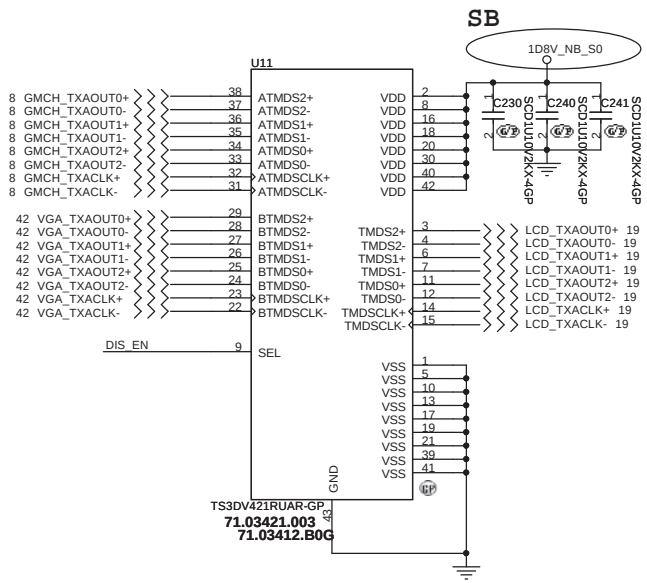
+3VS to 3.3V_DELAY Transfer



+1.5v to PCIE 1.1V Transfer

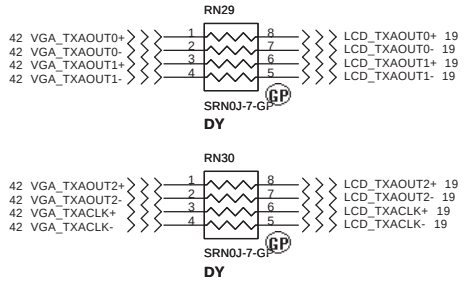


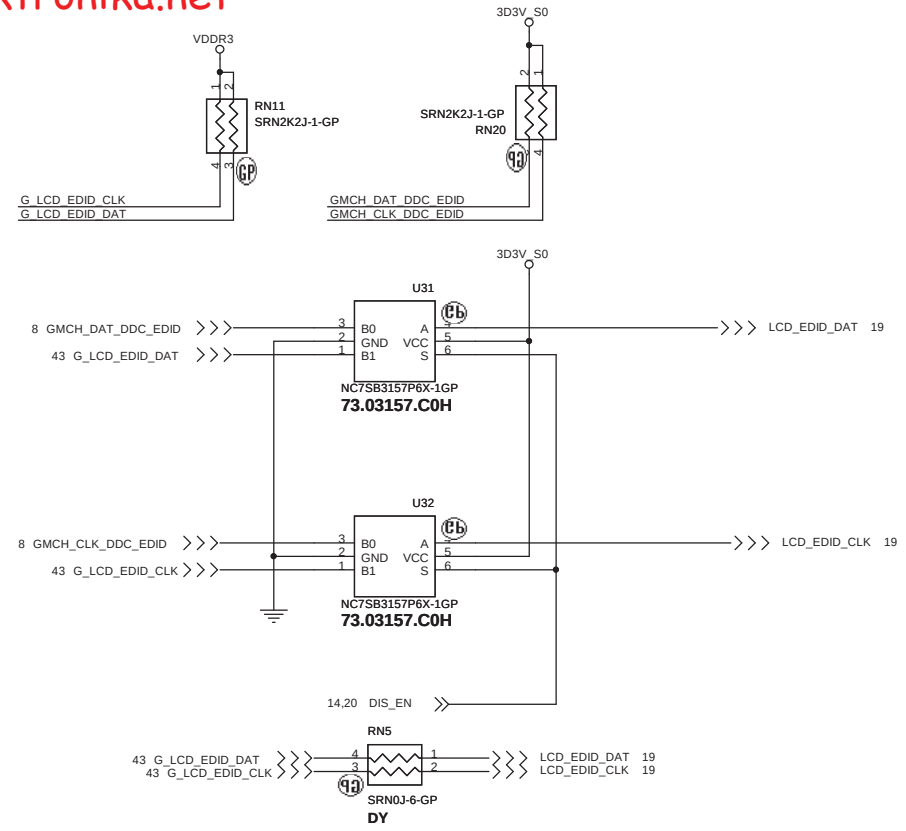
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***M92S2 power***	
Size: Custom	Document Number: **JM41_Discrete**	Rev: **SB**
Date: Monday, March 09, 2009	Sheet 40 of 48	



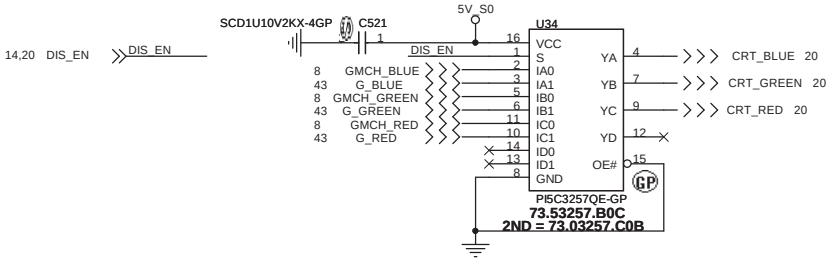
FUNCTION TABLE

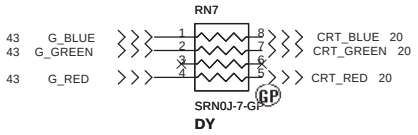
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-





$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1





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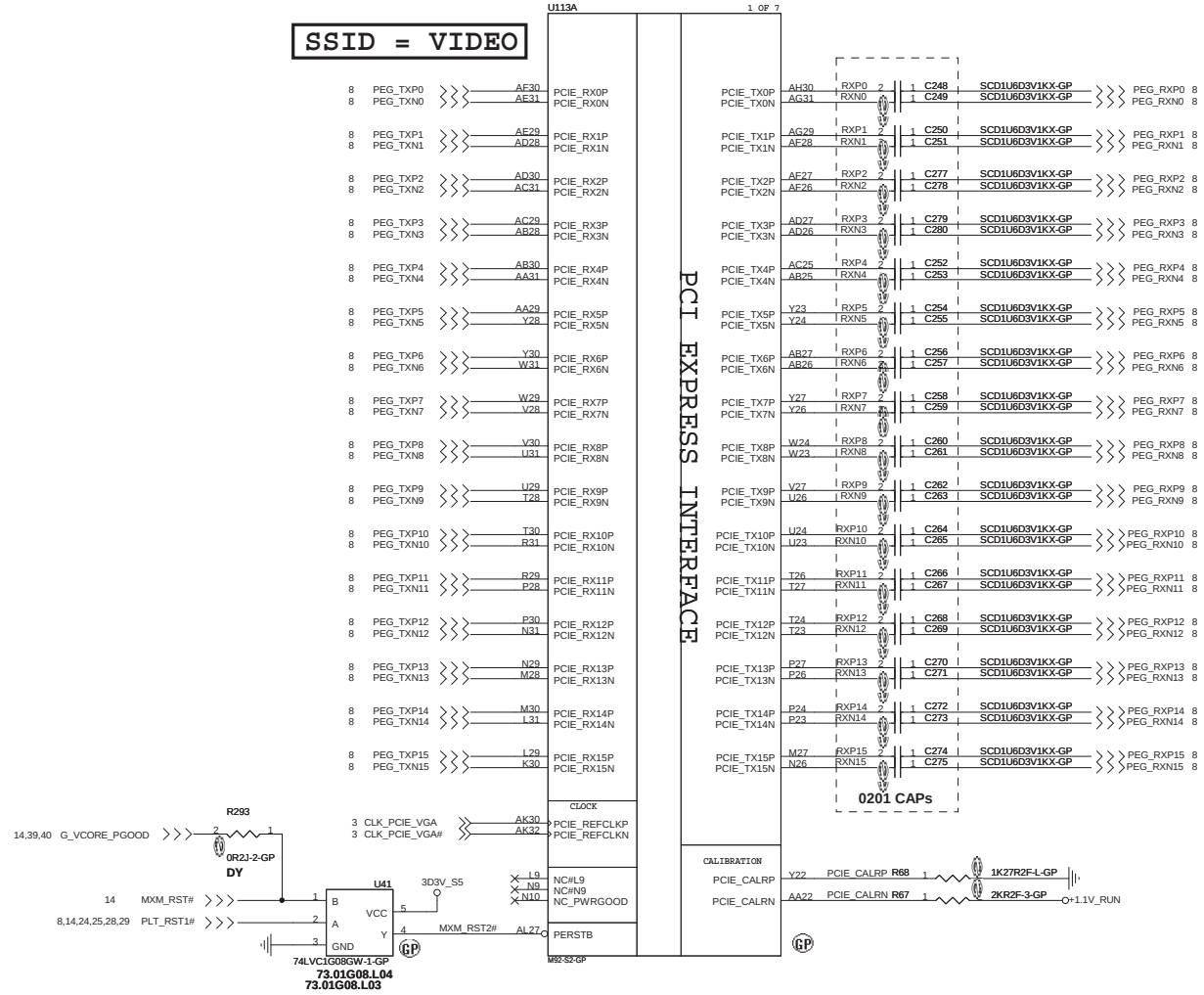
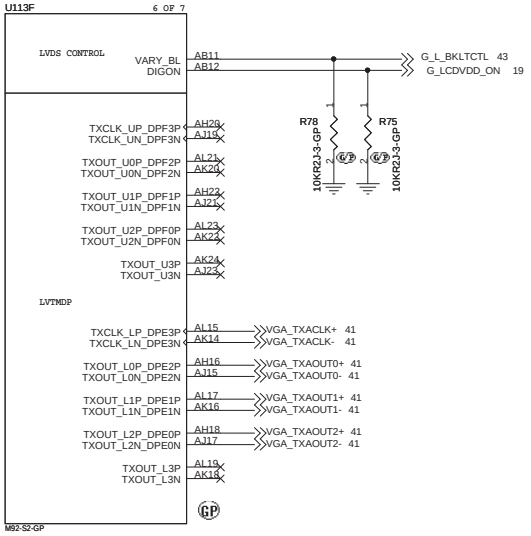
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PX_SWITCH**

Size	Document Number	Rev
A3		SB

Date: Monday, March 02, 2009 Sheet 41 of 48





緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-PCIE/LVDS(1/4)

Size	Document Number	Rev
Custom	JM41_Discrete	SB

Date: Monday, March 02, 2009 Sheet 42 of 48

SSID = VIDEO

DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung

+1.8V_RUN

R120 10KR2J-3-GP Samsung — DVPDATA23
R101 10KR2J-3-GP Hynix — DVPDATA22
R121 10KR2J-3-GP DY — DVPDATA21
R100 10KR2J-3-GP DY — DVPDATA20
R116 10KR2J-3-GP Hynix — DVPDATA20
R102 10KR2J-3-GP Samsung — DVPDATA21
R117 10KR2J-3-GP — DVPDATA22
R86 10KR2J-3-GP — DVPDATA23

STRAPS	PIN	DESCRIPTION
MEM_TYPE	DVPDATA(23:20) (Internal PD)	MEMORY TYPE,MAKE AND SIZE INFO 0000 - GDDR3 16Mx32 Qimonda 0001 - GDDR3 32Mx32 Hynix 0010 - GDDR3 32Mx32 Qimonda 0011 - GDDR3 32Mx32 Samsung

U113B — MUTI GFX

DVPCNTL_MVP_0 AA1
DVPCNTL_MVP_1 Y4
DVPCNTL_0 AC7
DVPCNTL_1 Y2
DVPCNTL_2 U5
DVPCLK U1
DVPDATA_0 Y7
DVPDATA_1 V2
DVPDATA_2 Y8
DVPDATA_3 V4
DVPDATA_4 AB7
DVPDATA_5 W1
DVPDATA_6 AB8
DVPDATA_7 W3
DVPDATA_8 AB9
DVPDATA_9 W5
DVPDATA_10 AC6
DVPDATA_11 W6
DVPDATA_12 AD7
DVPDATA_13 AA3
DVPDATA_14 AC8
DVPDATA_15 AA5
DVPDATA_16 AE8
DVPDATA_17 AA6
DVPDATA_18 AE9
DVPDATA_19 AB4
DVPDATA_20 AD9
DVPDATA_21 AB2
DVPDATA_22 AC10
DVPDATA_23 AC5

HDMI (DPA)

PLACE THESE CAPACITOR CLOSE TO CONNECTOR

DPA
TXCAP_DPA3P AE2 — G_HDMI_D_CLK+ — C376 — SCD1U10V2KX-4GP — HDMI_CLK+ 20
TXCAM_DPA3N AF4 — G_HDMI_D_CLK- — C372 — SCD1U10V2KX-4GP — HDMI_CLK- 20
TX0P_DPA2P AG3 — G_HDMI_TX2+ — C390 — SCD1U10V2KX-4GP — HDMI_DATA0+ 20
TX0M_DPA2N AG5 — G_HDMI_TX2- — C384 — SCD1U10V2KX-4GP — HDMI_DATA0- 20
TX1P_DPA1P AH3 — G_HDMI_TX1+ — C396 — SCD1U10V2KX-4GP — HDMI_DATA1+ 20
TX1M_DPA1N AH1 — G_HDMI_TX1- — C392 — SCD1U10V2KX-4GP — HDMI_DATA1- 20
TX2P_DPA0P AK3 — G_HDMI_TX0+ — C400 — SCD1U10V2KX-4GP — HDMI_DATA2+ 20
TX2M_DPA0N AK1 — G_HDMI_TX0- — C399 — SCD1U10V2KX-4GP — HDMI_DATA2- 20
TXCBP_DPB3P AK5
TXCBM_DPB3N AM3
DPB
TX3P_DPB2P AK6
TX3M_DPB2N AM5
TX4P_DPB1P AJ7
TX4M_DPB1N AH6
TX5P_DPB0P AK8
TX5M_DPB0N AL7

PLACE THESE RESISTORS CLOSE TO DIFF. PAIRS AND AVOID STUBS TO ALL DIFF. TRACES.

MINIMIZE THE DISTANCE BETWEEN THESE RES. AND 100nF AC CAPS

CRT

DAC1
R AM26 — G_RED — R63 150R2F-1-GP — G_RED 41
RB AK26
G AL25 — G_GREEN — R64 150R2F-1-GP — G_GREEN 41
GB AJ25
B AH24 — G_BLUE — R69 150R2F-1-GP — G_BLUE 41
BB AG25
HSYNC AH26 — G_HSYNC 20,45
VSYNC AJ27 — G_VSYNC 20,45
RSET AD22 — VGA_RSET — R70 499R2F-2-GP (Placed between this pin and AVSSQ)
70mA AVDD AG24 — +DAC1_AVDD — M92_AVSSQ — GAP-CLOSE G41
AVSSQ AE22
45mA VDD1DI AE23 — +DAC1_VDD1DI
VSS1DI AF23

DAC2
R2 AM12
R2B AK12
G2 AL11
G2B AJ11
B2 AK10
B2B AL9
C AH13
Y AM10
COMP AJ9
H2SYNC AL13
V2SYNC AJ13
40mA VDD2DI AD19 — +1.8V_RUN
VSS2DI AC19
65mA A2VDD AE20 — VDDR3
2mA A2VDDQ AE17 — +1.8V_RUN
A2VSSQ AE19
R2SET AG13 — VGA_R2SET — R76 715R2F-GP

DDC/AUX
DDC1CLK AE6 — G_DDCCLK 20
DDC1DATA AE5 — G_DDCDATA 20
AUX1P AD2
AUX1N AD4
DDC2CLK AC11 — G_HDMI_CLK 20
DDC2DATA AC13 — G_HDMI_DATA 20
AUX2P AD13
AUX2N AD11
NC#AB22 AB23
NC#AC22 AC23
DDCAUX5P AE16
DDCAUX5N AD16
DDC6CLK AC1 — G_HDMI_CLK
DDC6DATA AC3 — G_HDMI_DATA
NC_DDCAUX7P AD20
NC_DDCAUX7N AC20

VDDR3 — RN12 SRN1K5J-GP

I2C
41 G_LCD_EDID_CLK — R1 — SCL
41 G_LCD_EDID_DAT — R3 — SDA

GENERAL PURPOSE I/O
GPIO_0 U6 — 45 G_GPIO_0
GPIO_1 U10 — 45 G_GPIO_1
GPIO_2 T10 — 45 G_GPIO_2
GPIO_3_SMBDATA U8
GPIO_4_SMBCLK U7
GPIO_5_AC_BATT T9 — 45 G_GPIO_5 — TP38 — BL_ON_R — 19 G_BL_ON
GPIO_6 T8
GPIO_7_BLON T7
GPIO_8_ROMSO P10 — 45 G_GPIO_8
GPIO_9_ROMSI P4 — 45 G_GPIO_9
GPIO_10_ROMSCK P2
GPIO_11 N6 — 45 G_GPIO_11
GPIO_12 N5 — 45 G_GPIO_12
GPIO_13 N3 — 45 G_GPIO_13 — TP36
GPIO_14_HPD2 Y9
GPIO_15_PWRCNTL_0 N1 — 39 VCORE_VID0
GPIO_16_SSIN M4 — TP87 — CLK_VID_27M_SS
GPIO_17_THERMAL_INT R6 — VGA_THERM#
GPIO_18_HPD3 W10 — TP33 — G_TEMP_FAIL
GPIO_19_CTF M2
GPIO_20_PWRCNTL_1 P8 — 39 VCORE_VID1
GPIO_21_BB_EN P7
GPIO_22_ROMCSB N8 — 45 G_GPIO_22 — R109 10KR2J-3-GP — VGA_CLK_REQ#
GPIO_23_CLKREQB N7
GPIO_29_DRM_0 T11
GPIO_30_DRM_1 R11

JTAG_TRSTB L6
JTAG_TRSTB L5
JTAG_TDI L3 — TP85
JTAG_TCK L1 — TP83
JTAG_TMS K4 — TP84
JTAG_TDO AE24 — TP82
TESTEN

GENERICA AB13 — TP30
GENERICB W8 — TP40
GENERICC W9 — TP35
GENERICD W7 — TP39
GENERICE_HPD4 AD10 — TP34 — G_HDMI_DETECT# AC14

HPD1

VREFG AC16

PLL/CLOCK
DPLL_PVDD 120mA AF14 AE14
DPLL_PVSS
DPLL_VDDC 300mA AD14
XTALIN AM28
XTALOUT AK28

DPLUS DMINUS THERMAL
GPU_TEMP+ T4
GPU_TEMP- T2

TS_FDO R5
TSVDD 20mA AD17 AC17
TSVSS

M92-S3-GP

R89 0R2J-2-GP — 42 G_L_BKLTCTL
R90 0R2J-2-GP DY — 19 G_BL_ON
TP86 — G_TEMP_FAIL
R124 10KR2J-3-GP
TP45 — VGA_THERM#
R128 10KR2J-3-GP — VGA_CLK_REQ# 3
R81 4K99R2F-L-GP — 20 HDMI_DETECT#
R84 10KR2J-3-GP
R131 1KR2J-1-GP — JTAG_TESTEN
R66 1KR2J-1-GP
TP30 TP40 TP35 TP39 TP34

L24 BLM15BD121SN1D-GP — +1.8V_RUN — +DPLL_PVDD
SC10U6D2V3MX-GP C648
SC1U10V2KX-1GP C647
SCD1U16V2KX-3GP C357
R299 499R2F-2-GP — +1.8V_RUN
VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = .6V)
C331 SCD1U16V2KX-3GP
R74 249R2F-GP

L23 BLM15BD121SN1D-GP — +1.1V_RUN — +DPLL_VDDC
SC10U6D2V3MX-GP C640
SC1U10V2KX-1GP C639
SCD1U16V2KX-3GP C344

+DPLL_PVDD
+DPLL_VDDC

C612 SC22P50V2JN-4GP
82.30034.611
2ND = 82.30034.421
X4 XTAL-27MHZ-74-GP
1MR2F-GP R282
C624 SC27P50V2JN-2GP

L22 BLM15BD121SN1D-GP — +1.8V_RUN
TP88 — +TSVDD
SC1U10V2KX-1GP C329
C330
SCD1U16V2KX-3GP

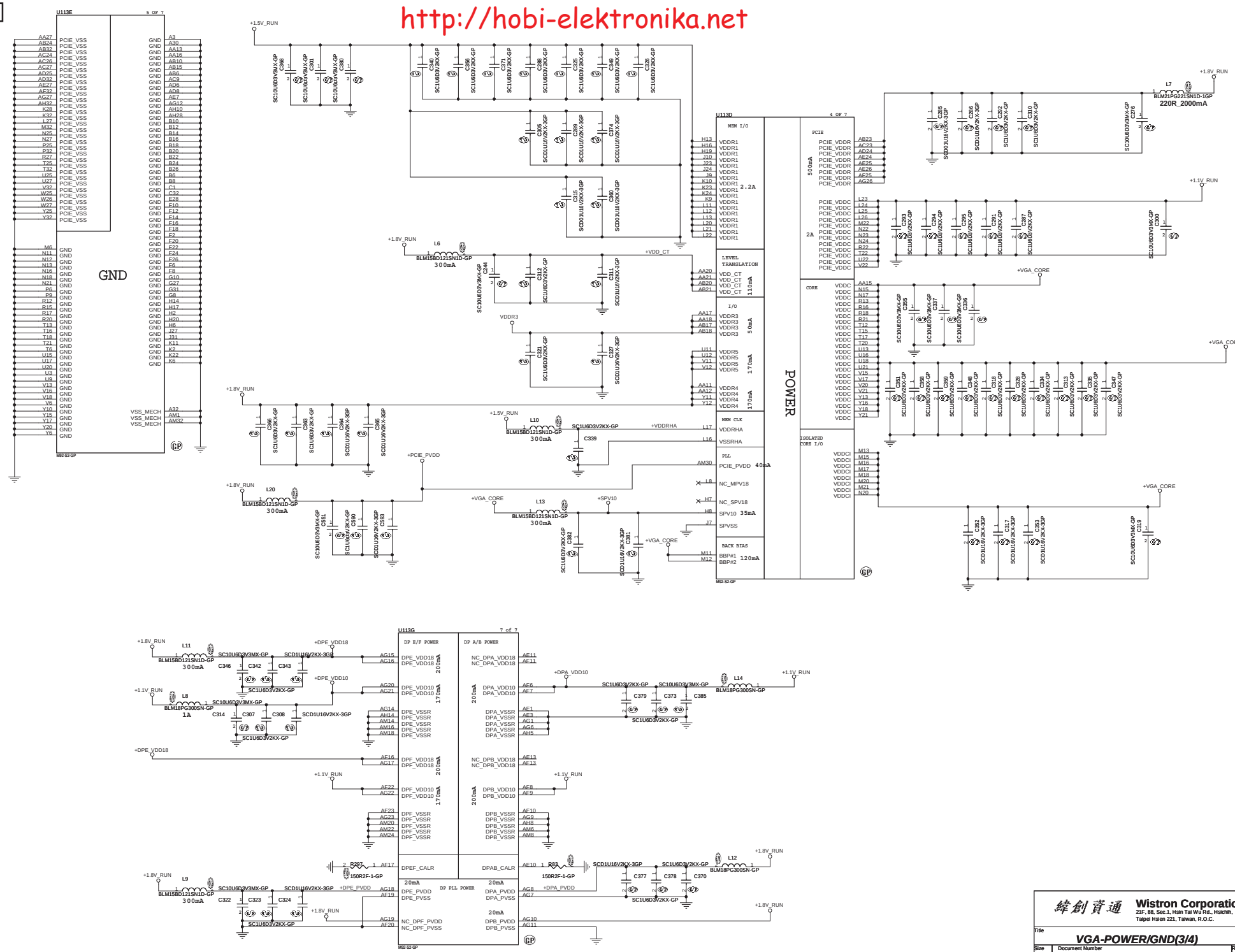
+DAC1_AVDD — +1.8V_RUN
L18 BLM15BD121SN1D-GP
C297 SCD1U16V2KX-3GP
C545 SCD1U16V2KX-3GP
C538 SCD1U16V2KX-3GP
C537 SC47U16D6V3MX-3GP
+DAC1_VDD1DI — +1.8V_RUN
L19 BLM15BD121SN1D-GP
C544 SCD1U16V2KX-3GP
C303 SCD1U16V2KX-3GP
C537 SC1U10V2KX-1GP

VDDR3
C614 SCD1U16V2KX-3GP
25,27,28 SMBC_THERM — G83 G84 GAP-CLOSE G82 — KBC_THERM_G781_CLK
25,27,28 SMBD_THERM — KBC_THERM_G781_DAT
U38 G781P8F-GP
SMBCLK SMBDATA ALERT# GND VCC DXP DXN THERM#
G781_ALERT#
GPU_THERM#
GPU_TEMP+
GPU_TEMP-
C607 SC2200P50V2KX-2GP
R262 2K2R2F-GP
R264 2K2R2F-GP
VDDR3

GPU DIE TEMP:
REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing.

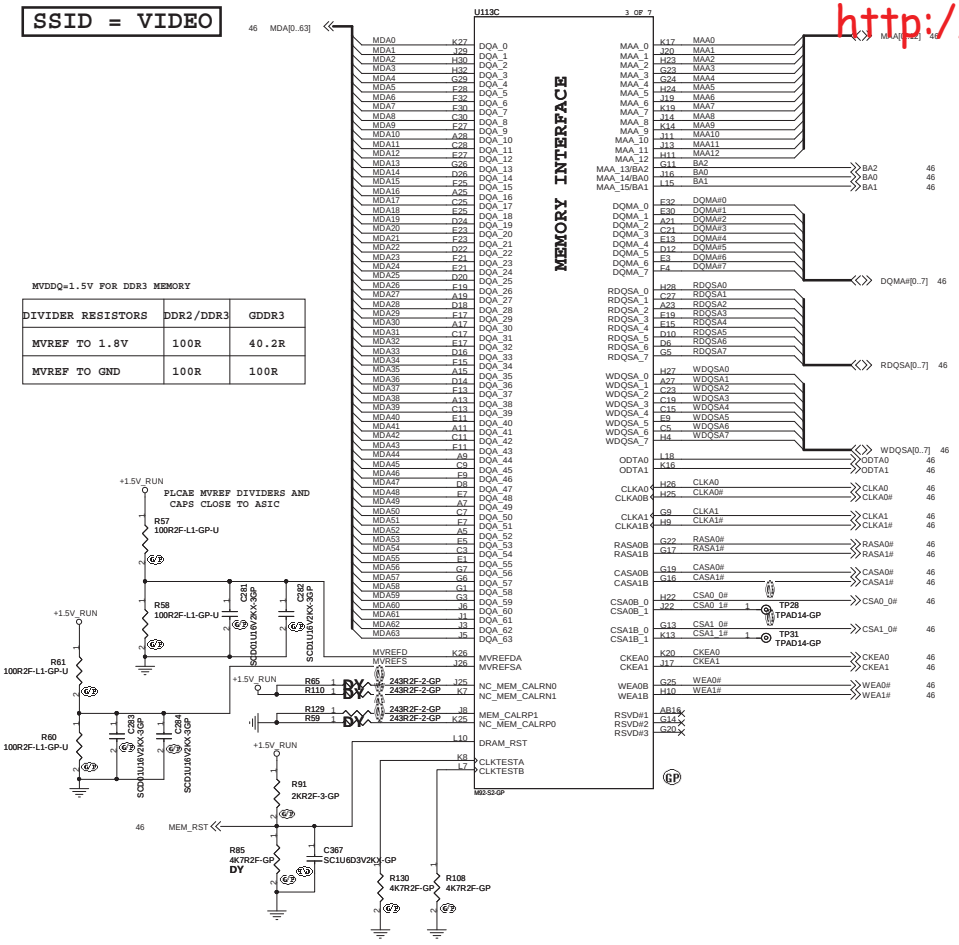
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	VGA-TV/CRT/DP PORT(2/4)		
Size C	Document Number JM41 Discrete		Rev SB
Date: Monday, March 02, 2009		Sheet 43 of 48	

SSID = VIDEO



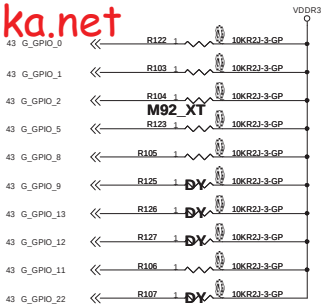
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: VGA-POWER/GND(3/4)	
Size: A2	Document Number: JM41 Discrete	Rev: SB
Date: Monday, March 02, 2009	Sheet 44 of 48	

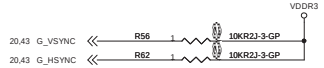
SSID = VIDEO



MVDDQ=1.5V FOR DDR3 MEMORY

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R





ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO3 , H2SYNC , V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[9,13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

V

STRAPS	PIN	DESCRIPTION
TX_PWRS_ENB (Internal PD)	GPIO0	Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing V
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled V
BIF_GEN2_EN_A	GPIO2	V 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s
BIF_CLK_PM_EN	GPIO8	0= Disable CLKREQ#power management capability 1= Enable CLKREQ# power management capability V
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size
BIOS_ROM_EN (Internal PD)	GPIO_22_ROMCSB	Enable external BIOS ROM device V 0= Disable external BIOS ROM device 1= Enable external BIOS ROM device
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI V

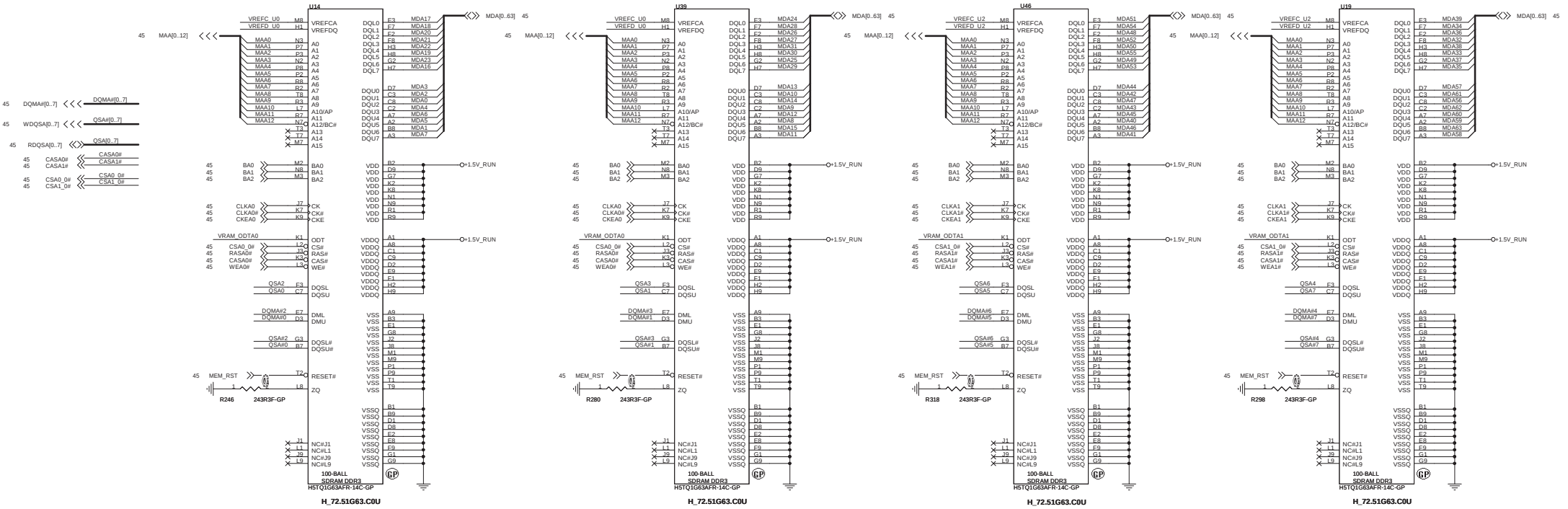
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

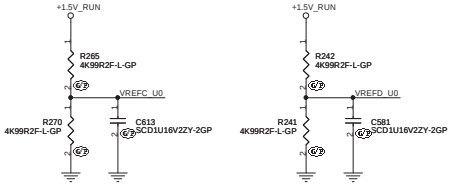
Title: VGA-MEMORY/STRAPS(4/4)

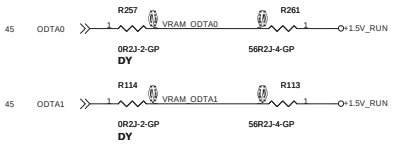
Size: A2 | Document Number: JM41 Discrete | Rev: SB

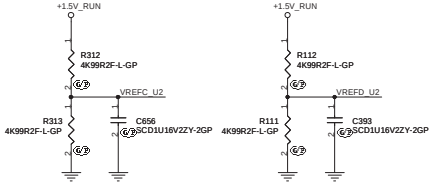
Date: Monday, March 02, 2009 | Sheet 45 of 48

512MB DDR3









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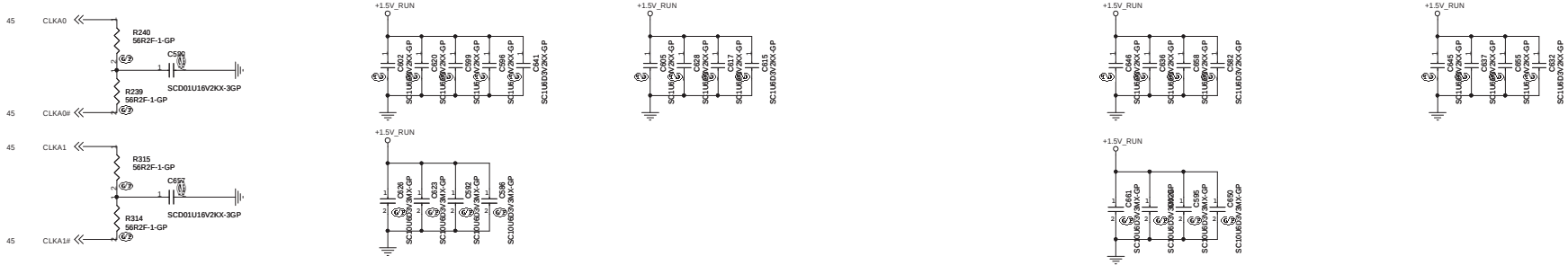

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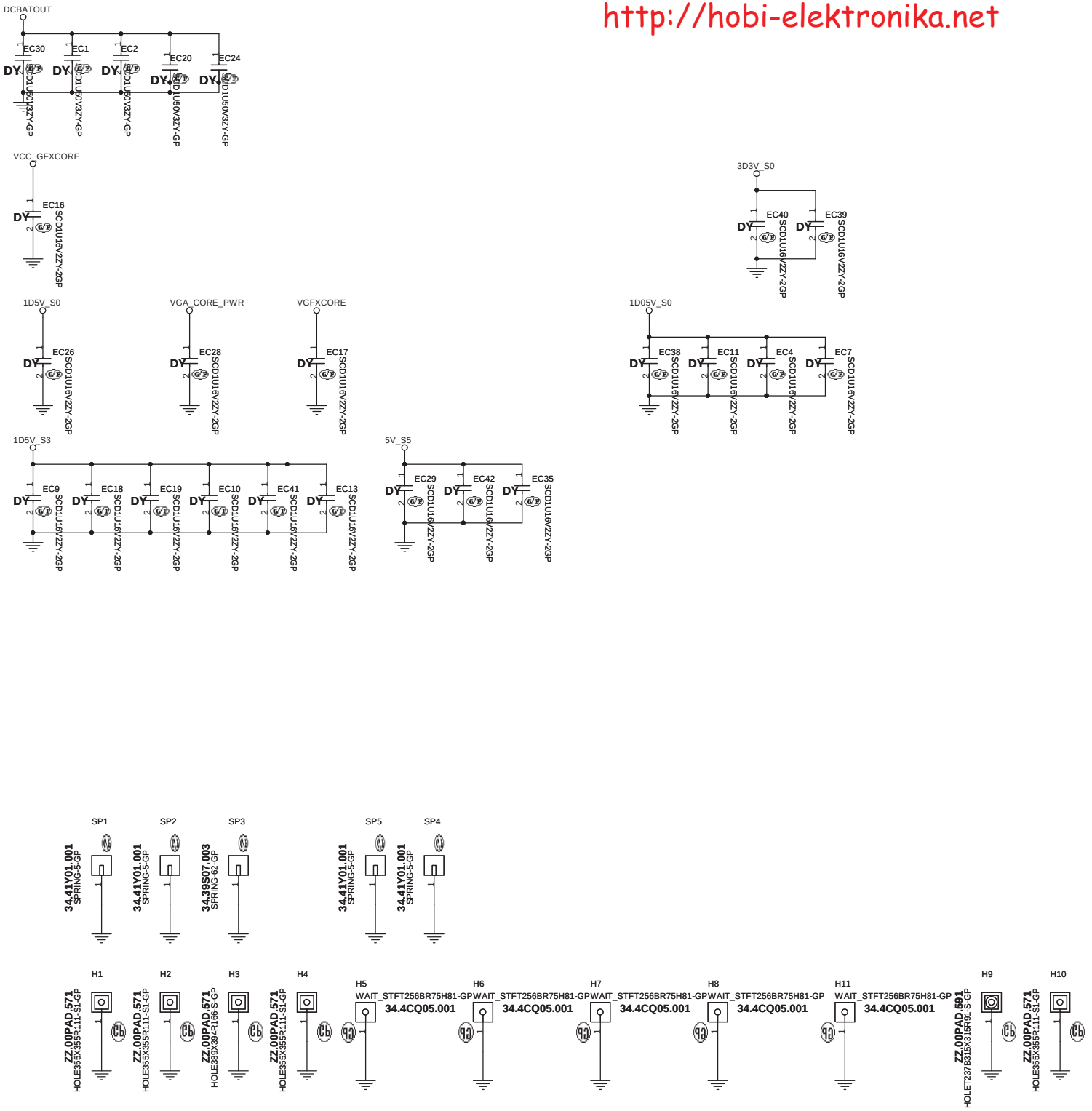

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