# ZD1(CHAPALA) SYSTEM BLOCK DIAGRAM

X'TAL 14.318MHZ
CLOCK GENERATOR
SELGO: SLG8SP512K05
P2

Merom 479 uFCPGA
P3, P4

CPU Thermal Sensor
P3

FSB 667/800 Mhz

VCORE(ISL6262A) P33
+1.2V/+1.25V/1.5V/2.5V P37
5V/3.3V (ISL6236) P33
BATTERYCHARGER (ISL6251) P32
DISCHARGE P37
+1.8V / +1.05V P35, 36

TVOUT CRT P19

TFT LCD Panel
WXGA
WSXGA+
WUXGA
P18

VGA
LVDS

NB Crestline PM965
P5, P6, P7, P8, P9, P10, P11

Dual Channel DDR2 533/667 MHz
DDRII SO-DIMM 0 SO-DIMM 1
P16

PCI-Express 16X Lan
DVI
LVDS
VGA/TV out
MXM-NB8P-GS ( nVidia )
VRAM 256M
VRAM 512M
P17

X4 DMI interface

HDD (SATA) P24
ODD (PATA) P24

SATA0
SATA1
PATA

SB ICH8M
P12, P13, P14, P15

USB 2.0 Azalia

PCI-Express
PCI Bus

USB6
Mini Card / WLAN / 3G(TV)
P22
PCIE-2
PCIE-4

USB5
New Card
P23
PCIE-1

Robson
P29
PCIE-5

PCIE-6
X'TAL 25M
BROADCOM
10/100/1G LAN
5787M
P20

Transformer P20
RJ45 P21
Fan Header P21, P30

Bluetooth USB4 P21
USB Port x 4 USB0~3 P25
CCD USB7 P21

X'TAL 32.768KHZ

X'TAL24.576MHZ
1394 +Cardreader Controller
R5C832/833
P28

IEEE 1394 Port P28
Media Card Reader P28

Int MIC P27
Azalia Audio Controller ALC268&888 P26
Audio Amplifier P27

LPC

X'TAL 32.768K
EC (WPC8769LDG)
P31

SPI ROM P31
VR P26
Touch Pad P30
CIR P21
K/B COON. P30

MIC Jack P27
Line in P27
Connector
Speaker P27
Phone Jack P27
MDC 1.5 P26

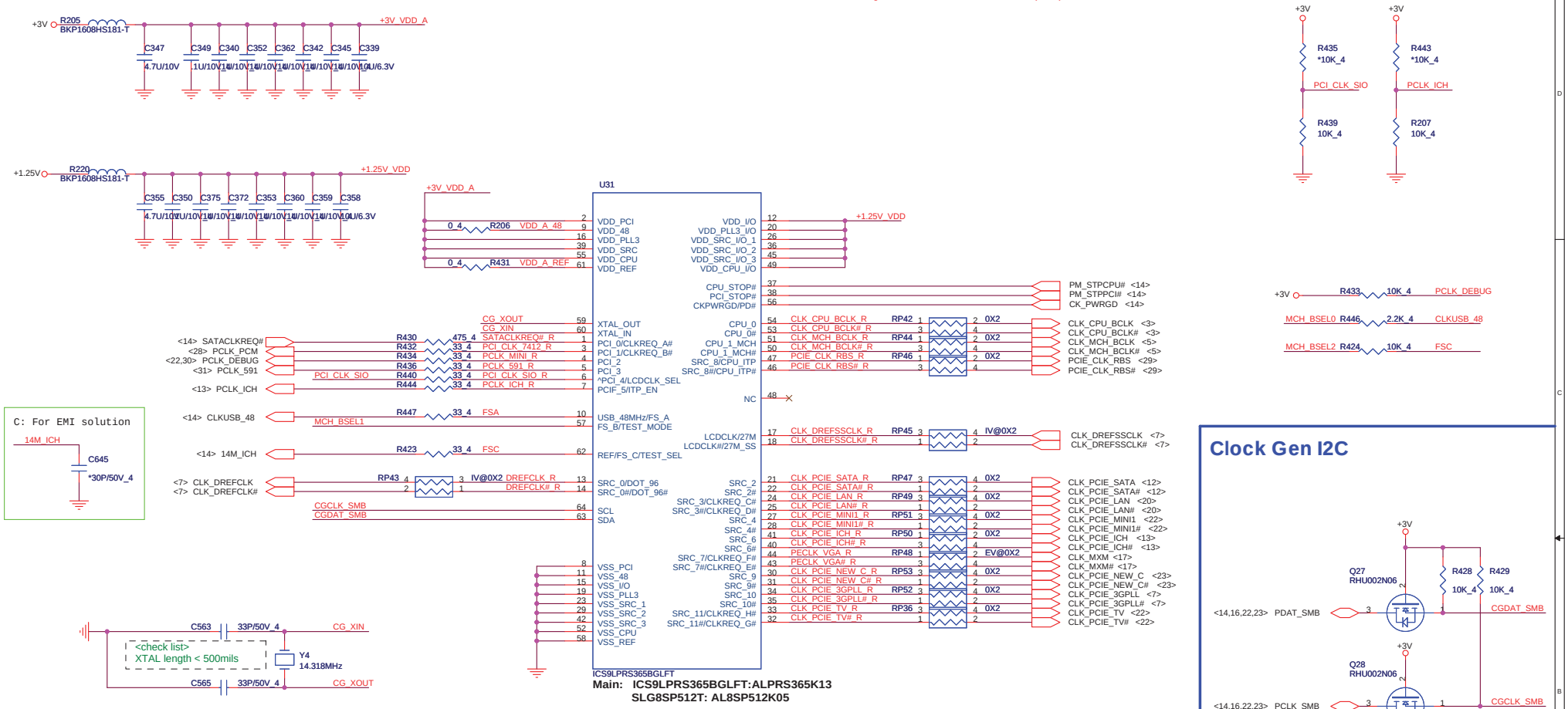
BOM MARK
EV@ EXT VGA 要打
IV@ INT VGA 要打
268@ AUDIO 268 要打
888@ AUDIO 888要打

PROJECT : ZD1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | Block Diagram | E |
| Date: Wednesday, April 25, 2007 | Sheet 1 of 38 | |

# Clock Generator

Change list:
B-test
1.Change U31 P/N to ALPRS365K13 (ICS)




Main: ICS9LPRS365BGLFT:ALPRS365K13
SLG8SP512T: AL8SP512K05



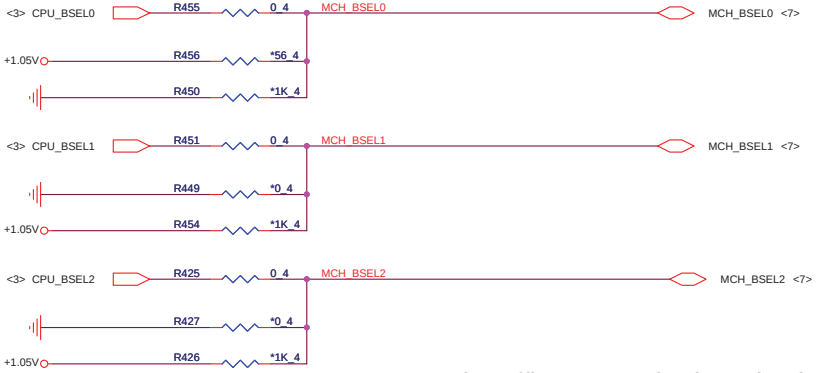




## Clock Gen I2C




# CPU Clock select



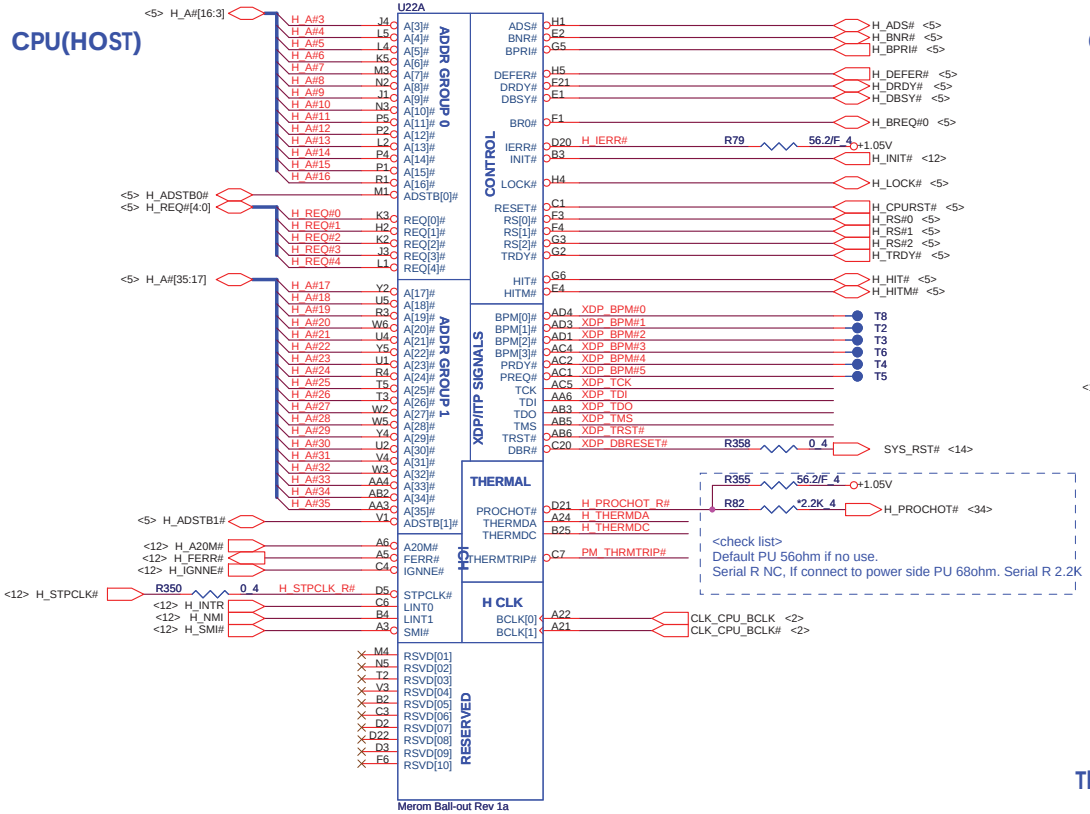

### BSEL Frequency Select Table

| FSC | FSB | FSA | Frequency |
|---|---|---|---|
| 0 | 0 | 0 | 266Mhz |
| 0 | 0 | 1 | 133Mhz |
| 0 | 1 | 1 | 166Mhz |
| 0 | 1 | 0 | 200Mhz |
| 1 | 1 | 0 | 400Mhz |
| 1 | 1 | 1 | Reserved |
| 1 | 0 | 1 | 100Mhz |
| 1 | 0 | 0 | 333Mhz |

PROJECT : ZD1
Quanta Computer Inc.

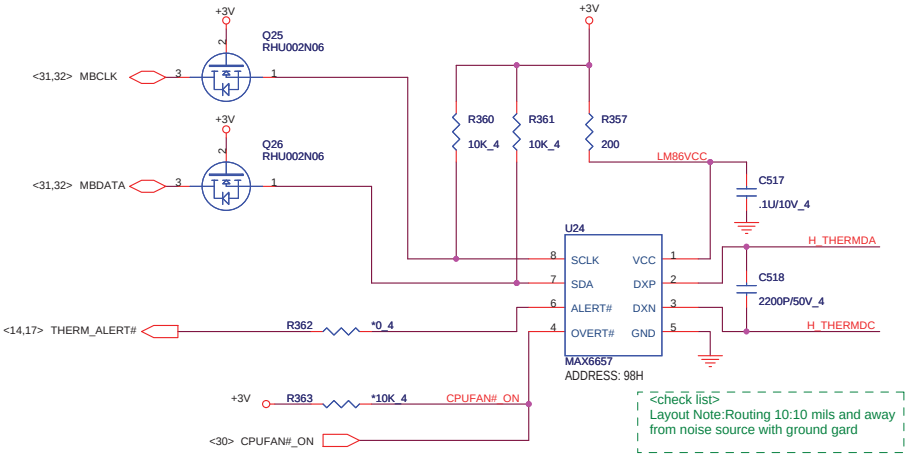
| Size | Document Number | Rev |
|---|---|---|
| | CLOCK GENERATOR CK505 W/REGULATOR | E |
| Date: Monday, May 07, 2007 | Sheet 2 of 38 | |

## CPU(HOST)



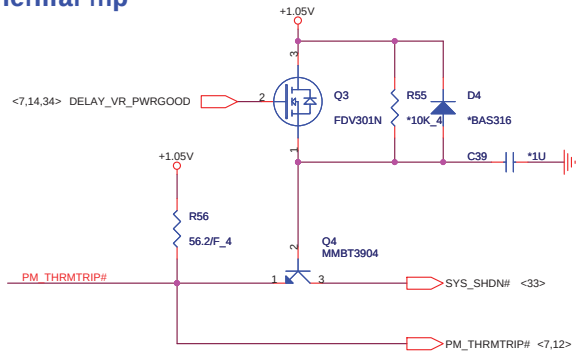

<check list>
Default PU 56ohm if no use.
Serial R NC, If connect to power side PU 68ohm. Serial R 2.2K

## CPU Thermal monitor



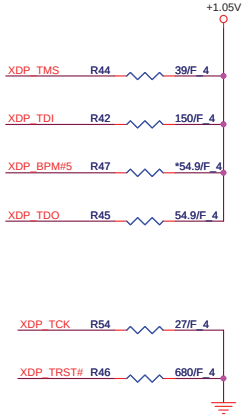

<check list>
Layout Note:Routing 10:10 mils and away from noise source with ground gard

## Thermal Trip

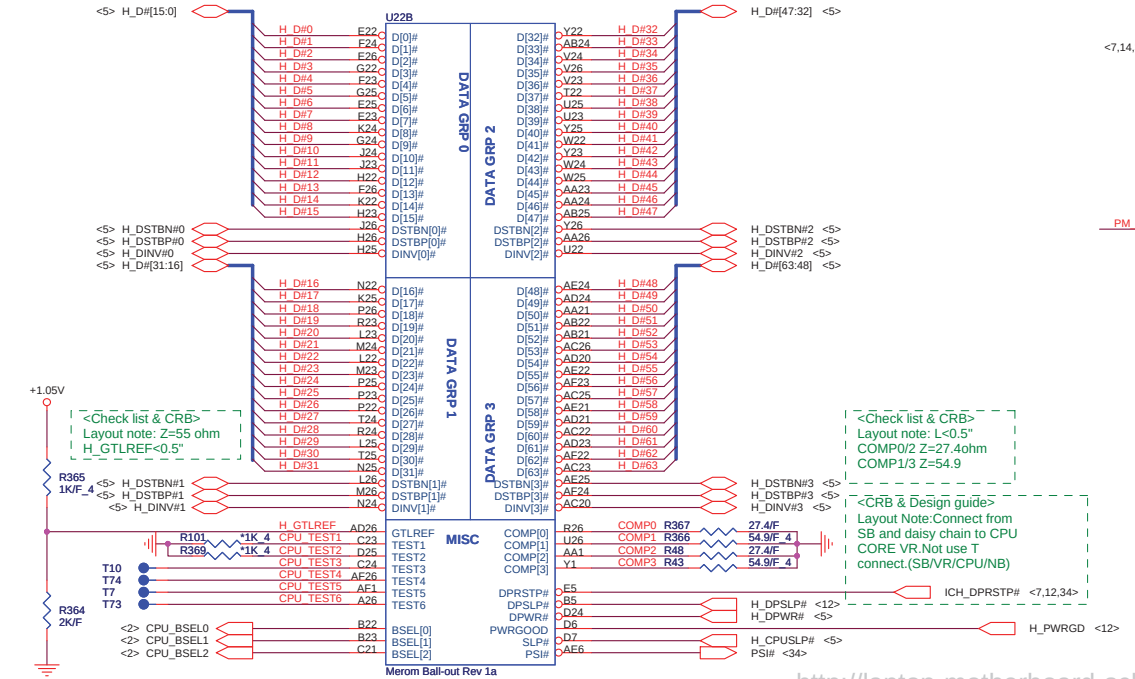



<CRB & Design guide>
Layout Note: Thermal trip should connect to ICH8 & GMCH without T-ing (ZS1 default NC)

## PU/PD (ITP700)




## Merom Ball-out Rev 1a




<Check list & CRB>
Layout note: Z=55 ohm
H_GTLREF<0.5"

<Check list & CRB>
Layout note: L<0.5"
COMP0/2 Z=27.4ohm
COMP1/3 Z=54.9

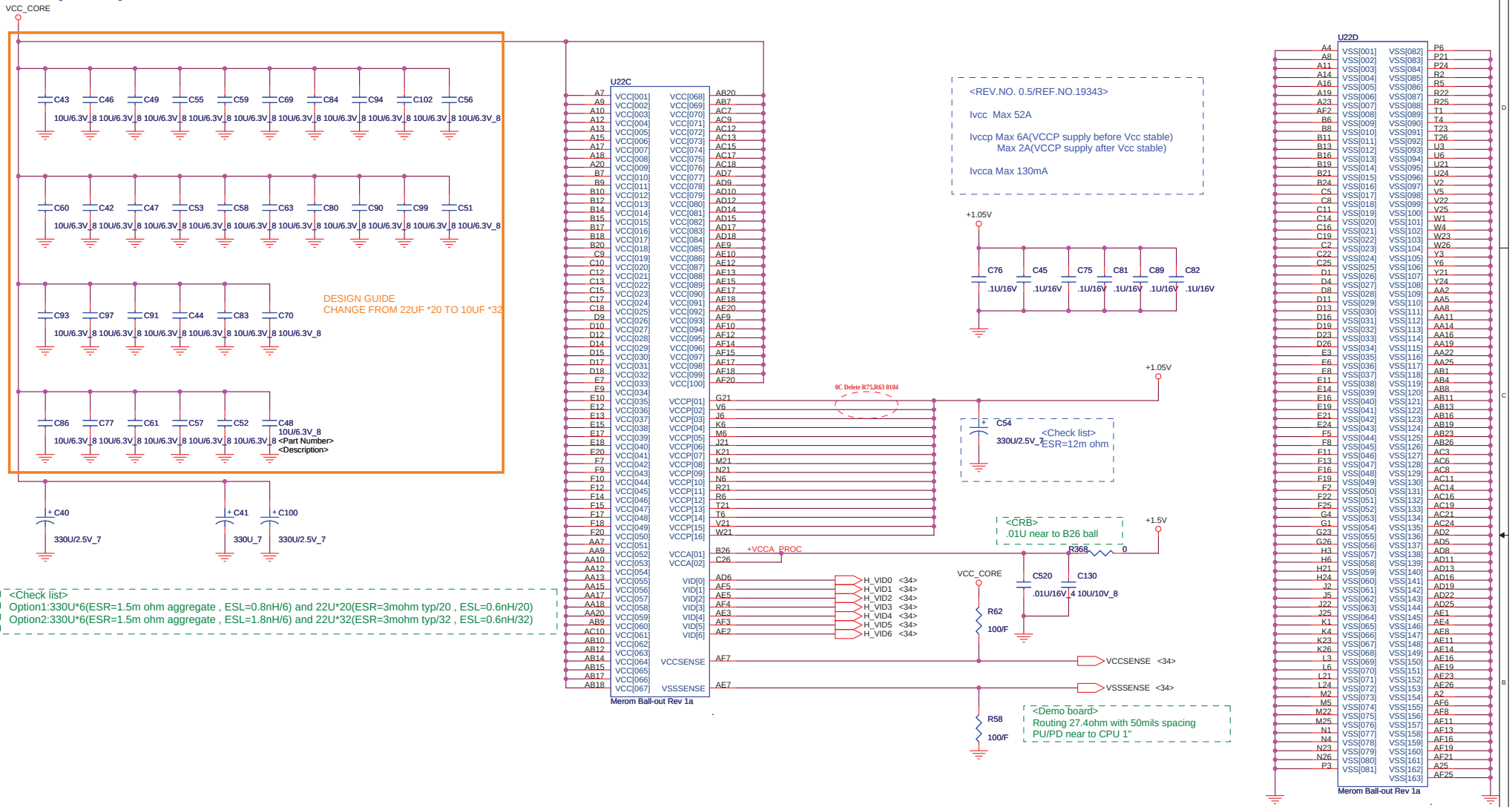
<CRB & Design guide>
Layout Note:Connect from SB and daisy chain to CPU CORE VR.Not use T connect.(SB/VR/CPU/NB)



PROJECT : ZD1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | CPU(1 of 2)/FAN/Thermal | E |
| Date: Monday, May 07, 2007 | Sheet 3 of 38 | |

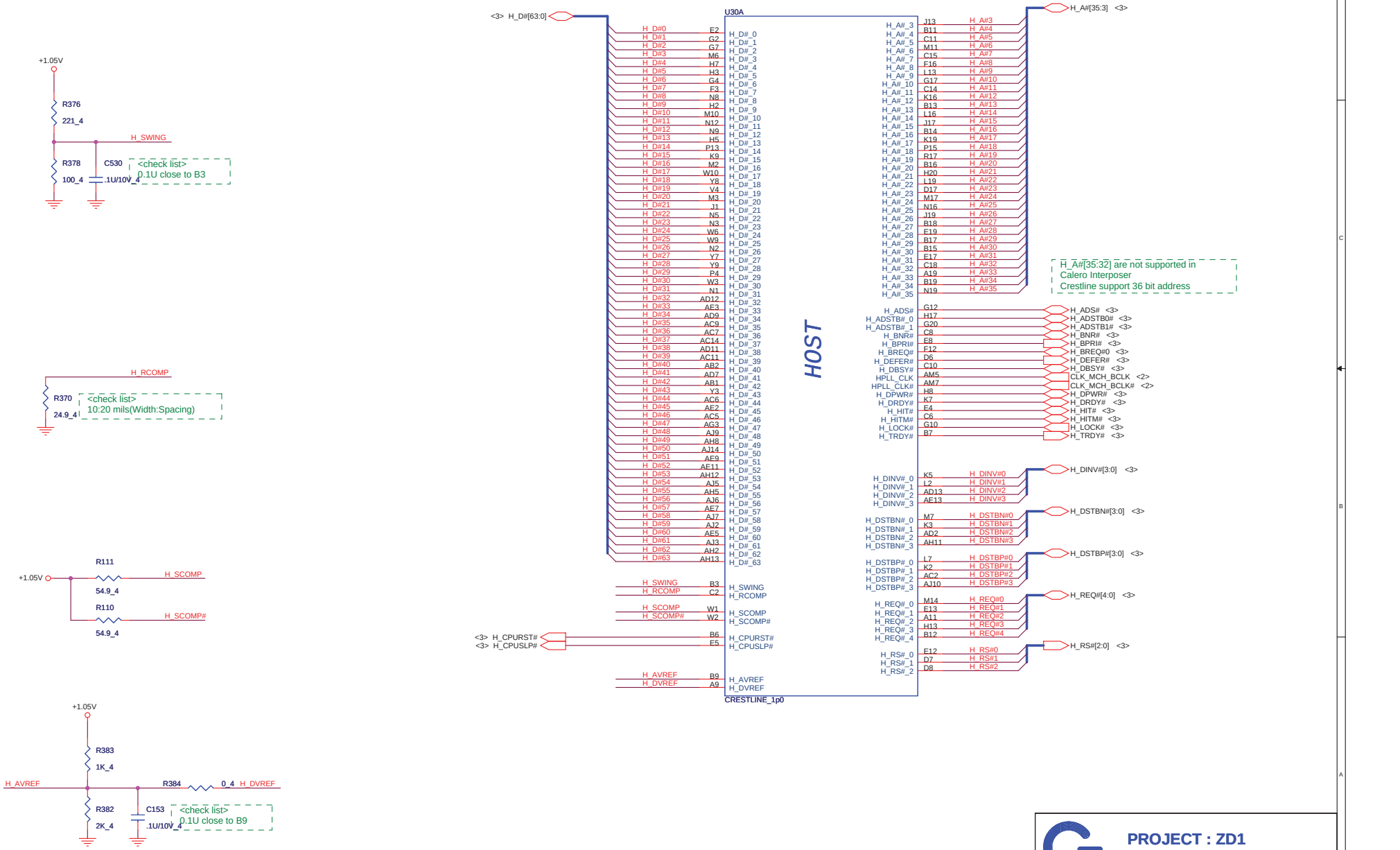
# CPU(Power)




<Check list>
Option1:330U*6(ESR=1.5m ohm aggregate , ESL=0.8nH/6) and 22U*20(ESR=3mohm typ/20 , ESL=0.6nH/20)
Option2:330U*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U*32(ESR=3mohm typ/32 , ESL=0.6nH/32)

| | | | |
|---|---|---|---|
| PROJECT : ZD1 | | | |
| Quanta Computer Inc. | | | |
| Size | Document Number: CPU(2 of 2) | | Rev: E |
| Date: Monday, May 07, 2007 | Sheet 4 of 38 | | |

# NB(HOST)



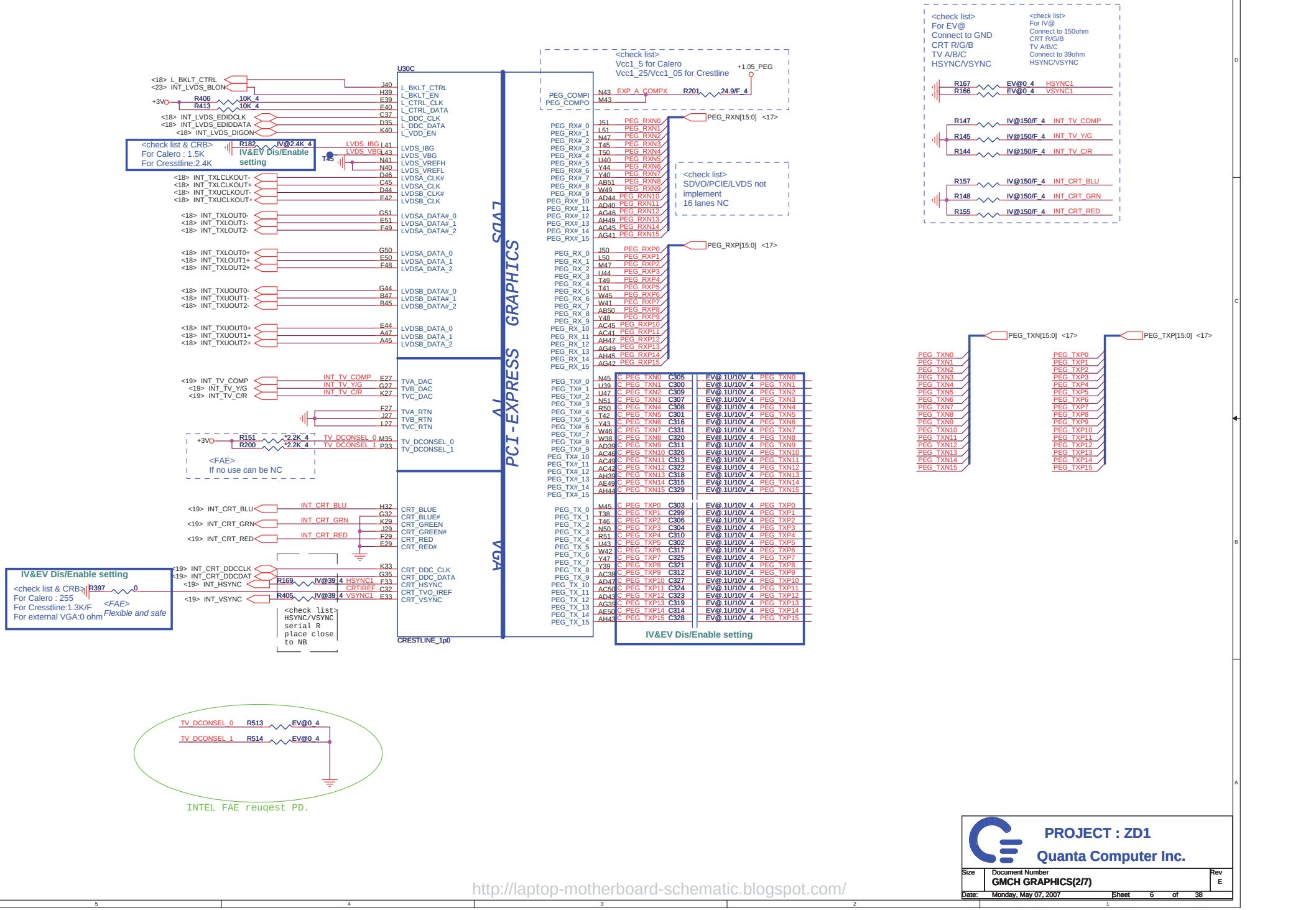



PROJECT : ZD1

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | GMCH HOST(1/7) | E |

Date: Monday, May 07, 2007 Sheet 5 of 38






PROJECT : ZD1

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | GMCH GRAPHICS(2/7) | E |

Date: Monday, May 07, 2007 Sheet 6 of 38

## Strapping table

All strap are sampled with respect to the leading edge of the GMCH power ok signal
CFG[17:3] have internal pull-up
CFG[18:19] have internal pull-down
Any CFG signal strapping option not list below should be left NC pin

| Pin Name | Strap Description | Configuration |
|---|---|---|
| CFG[2:0] | FSB Frequency Select | 010 = FSB 800MHz<br>011 = FSB 667MHz |
| CFG[4:3] | Reserved | |
| CFG5 | DMI X2 Select | 0 = DMI X2<br>1 = DMI X4 (Default) |
| CFG6 | Reserved | |
| CFG7 | CPU Strap | 0 = Reserved<br>1 = Mobile CPU (Default) |
| CFG8 | Low Power PCI Express | 0 = Normal mode<br>1 = Low Power mode |
| CFG9 | PCI Express Graphics Lane Reversal | 0 = Reserved Lanes<br>1 = Normal operation (Default) |
| CFG[11:10] | Reserved | |
| CFG[13:12] | XOR/ ALLZ/ Clock Un gating | 00 = Clock gating disable<br>01 = ALL-Z Mode Enable<br>10 = XOR Mode Enable<br>11 = Normal Cperation (Default) |
| CFG[15:14] | Reserved | |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT disable<br>1 = Dynamic ODT Enable (Default) |
| CFG[18:17] | Reserved | |
| CFG19 | DMI Lane Reversal | 0 = Normal operation<br>1 = Reverse Lanes (Default) |
| CFG20 | SDVO/PCIe concurrent | 0 = Only SDVO or PCIE x1 is operation (Default)<br>1 = SDVO and PCIE x1 are operating simultaneously via the PEG port |
| SDVO_CTRLDATA | SDVO Present | 0 = No SDVO Card present (Default)<br>1 = SDVO Card Present |

INTEL CRB
CRESSTLINE SHOULD USE 20OHM

<check list & CRB>
R Value select
For Calero : 80.6ohm
For Cresstline:20ohm
But check list use 80.6ohm

M_RCOMP# — R387 20/F_4 — <FAE> 80.6ohm — R388 20/F_4 — +1.8VSUS
M_RCOMP

INTEL CRB
ADD 0.1UF
C165 .1U/10V_4

U30B

RSVD
P36 RSVD1
P37 RSVD2
R35 RSVD3
N35 RSVD4
AR12 RSVD5
AR13 RSVD6
AM12 RSVD7
AN13 RSVD8
J12 RSVD9
AR37 RSVD10
AM36 RSVD11
AL36 RSVD12
AM37 RSVD13
D20 RSVD14

H10 RSVD20
B51 RSVD21
BJ20 RSVD22
BK22 RSVD23
BF19 RSVD24
BH20 RSVD25
BK18 RSVD26
BJ18 RSVD27
BF23 RSVD28
BG23 RSVD29
BC23 RSVD30
BD24 RSVD31

BH39 RSVD32
AW20 RSVD33
BK20 RSVD34
C48 RSVD35
D47 RSVD36
B44 RSVD37
C44 RSVD38
A35 RSVD39
B37 RSVD40
B36 RSVD41
B34 RSVD42
C34 RSVD43

DDR MUXING
SM_CK_0 AV29 M_CLK0 <16>
SM_CK_1 BB23 M_CLK1 <16>
SM_CK_3 BA25 M_CLK2 <16>
SM_CK_4 AV23 M_CLK3 <16>
SM_CK#_0 AW30 M_CLK#0 <16>
SM_CK#_1 BA23 M_CLK#1 <16>
SM_CK#_3 AW25 M_CLK#2 <16>
SM_CK#_4 AW23 M_CLK#3 <16>
SM_CKE_0 BE29 M_CKE0 <16>
SM_CKE_1 AY32 M_CKE1 <16>
SM_CKE_3 BD39 M_CKE2 <16>
SM_CKE_4 BG37 M_CKE3 <16>
SM_CS#_0 BG20 M_CS#0 <16>
SM_CS#_1 BK16 M_CS#1 <16>
SM_CS#_2 BG16 M_CS#2 <16>
SM_CS#_3 BE13 M_CS#3 <16>
SM_ODT_0 BH18 M_ODT0 <16>
SM_ODT_1 BJ15 M_ODT1 <16>
SM_ODT_2 BJ14 M_ODT2 <16>
SM_ODT_3 BE16 M_ODT3 <16>
SM_RCOMP BL15 M_RCOMP
SM_RCOMP# BK14 M_RCOMP#
SM_RCOMP_VOH BK31 SM_RCOMP_VOH
SM_RCOMP_VOL BL31 SM_RCOMP_VOL
SM_VREF_0 AR49 +SM_VREF_MCH
SM_VREF_1 AW4

CLK
DPLL_REF_CLK B42 CLK_DREFCLK
DPLL_REF_CLK# C42 CLK_DREFCLK#
DPLL_REF_SSCLK H48 CLK_DREFSSCLK
DPLL_REF_SSCLK# H47 CLK_DREFSSCLK#
PEG_CLK K44 CLK_PCIE_3GPLL
PEG_CLK# K45 CLK_PCIE_3GPLL#
CLK_DREFCLK <2>
CLK_DREFCLK# <2>
CLK_DREFSSCLK <2>
CLK_DREFSSCLK# <2>
CLK_PCIE_3GPLL <2>
CLK_PCIE_3GPLL# <2>

DMI
DMI_RXN_0 AN47 DMI_TXN0
DMI_RXN_1 AJ38 DMI_TXN1
DMI_RXN_2 AN42 DMI_TXN2
DMI_RXN_3 AN46 DMI_TXN3
DMI_TXN[3:0] <13>
DMI_RXP_0 AM47 DMI_TXP0
DMI_RXP_1 AJ39 DMI_TXP1
DMI_RXP_2 AN41 DMI_TXP2
DMI_RXP_3 AN45 DMI_TXP3
DMI_TXP[3:0] <13>
DMI_TXN_0 AJ46 DMI_RXN0
DMI_TXN_1 AJ41 DMI_RXN1
DMI_TXN_2 AM40 DMI_RXN2
DMI_TXN_3 AM44 DMI_RXN3
DMI_RXN[3:0] <13>
DMI_TXP_0 AJ47 DMI_RXP0
DMI_TXP_1 AJ42 DMI_RXP1
DMI_TXP_2 AM39 DMI_RXP2
DMI_TXP_3 AM43 DMI_RXP3
DMI_RXP[3:0] <13>

CFG
<2> MCH_BSEL0 P27 CFG_0
<2> MCH_BSEL1 N27 CFG_1
<2> MCH_BSEL2 N24 CFG_2
MCH_CFG_3 C21 CFG_3
T30 MCH_CFG_4 C23 CFG_4
T75 MCH_CFG_5 F23 CFG_5
MCH_CFG_6 N23 CFG_6
T34 MCH_CFG_7 G23 CFG_7
T24 MCH_CFG_8 J20 CFG_8
T29 MCH_CFG_9 C20 CFG_9
MCH_CFG_10 R24 CFG_10
T37 MCH_CFG_11 L23 CFG_11
T28 MCH_CFG_12 J23 CFG_12
MCH_CFG_13 E23 CFG_13
MCH_CFG_14 E20 CFG_14
T25 MCH_CFG_15 K23 CFG_15
T27 MCH_CFG_16 M20 CFG_16
MCH_CFG_17 M24 CFG_17
T32 MCH_CFG_18 L32 CFG_18
T40 MCH_CFG_19 N33 CFG_19
MCH_CFG_20 L35 CFG_20

GRAPHICS VID
GFX_VID_0 E35 MCH_GFX_VID_0 T41
GFX_VID_1 A39 MCH_GFX_VID_1 T42
GFX_VID_2 C38 MCH_GFX_VID_2 T43
GFX_VID_3 B39 MCH_GFX_VID_3 T44
GFX_VR_EN E36 R183 *0_4 SUS#_B <14,31>

PM
<14> PM_BMBUSY# R184 0_4 PM_BMBUSY#_R G41 PM_BM_BUSY#
<3,12,34> ICH_DPRSTP# R177 0_4 ICH_DPRSTP#_R L39 PM_DPRSTP#
<16> PM_EXTTS#0 R401 0_4 PM_EXTTS#0_R L36 PM_EXT_TS#_0
<16> PM_EXTTS#1 R150 0_4 PM_EXTTS#1_R J36 PM_EXT_TS#_1
<3,14,34> DELAY_VR_PWRGOOD AW49 PWROK
<13> PLTRST#_NB R140 100_4 RST_IN#_MCH AV20 RSTIN#
<3,12> PM_THRMTRIP# R130 *0_4 PM_THRMTRIP#_GMCH N20 THERMTRIP#
<14,34> PM_DPRSLPVR R407 0_4 PM_DPRSLPVR_GMCH G36 DPRSLPVR

ME
CL_CLK AM49 CL_CLK0 <14>
CL_DATA AK50 CL_DATA0 <14>
CL_PWROK AT43 MPWROK <14,31>
CL_RST# AN49 CL_RST#0 <14>
CL_VREF AM50 +1.25V_CL_VREF

NC
BJ51 NC_1
BK51 NC_2
BK50 NC_3
BL50 NC_4
BL49 NC_5
BL3 NC_6
BL2 NC_7
BK1 NC_8
BJ1 NC_9
E1 NC_10
A5 NC_11
C51 NC_12
B50 NC_13
A50 NC_14
A49 NC_15
BK2 NC_16

MISC
SDVO_CTRL_CLK H35
SDVO_CTRL_DATA K36
CLK_REQ# G39 CLK_MCH_OE#
ICH_SYNC# G40 MCH_ICH_SYNC# <14>
TEST_1 A37 GMCH_TEST1 R178 0_4
TEST_2 R32 GMCH_TEST2 R168 20K_4

CRESTLINE_1p0

+3V
R170 10K_4 CLK_MCH_OE#
R395 10K_4 PM_EXTTS#0
R149 10K_4 PM_EXTTS#1

MCH_CFG_5 R138 *4.02K/F_4
MCH_CFG_9 R127 *4.02K/F_4
MCH_CFG_12 R139 *4.02K/F_4
MCH_CFG_13 R137 *4.02K/F_4
MCH_CFG_16 R129 *4.02K/F_4

+3V
MCH_CFG_19 R171 *4.02K/F_4
MCH_CFG_20 R174 *4.02K/F_4

+1.25V
R422 1K/F_4
C559 .1U/10V_4
R420 392/F

+1.8VSUS
+SMDDR_VREF
R416 *1K/F_4
R417 BK1608LL121
+SM_VREF_MCH
R418 *1K/F_4
C295 .1U/10V_4
C143 1U/10V_4

+1.8VSUS
R154 1K/F_4 SM_RCOMP_VOH
R165 3.01K/F_4
C241 .01U/16V_4
C232 2.2U/6.3V
SM_RCOMP_VOL
R163 1K/F_4
C250 .01U/16V_4
C233 2.2U/6.3V

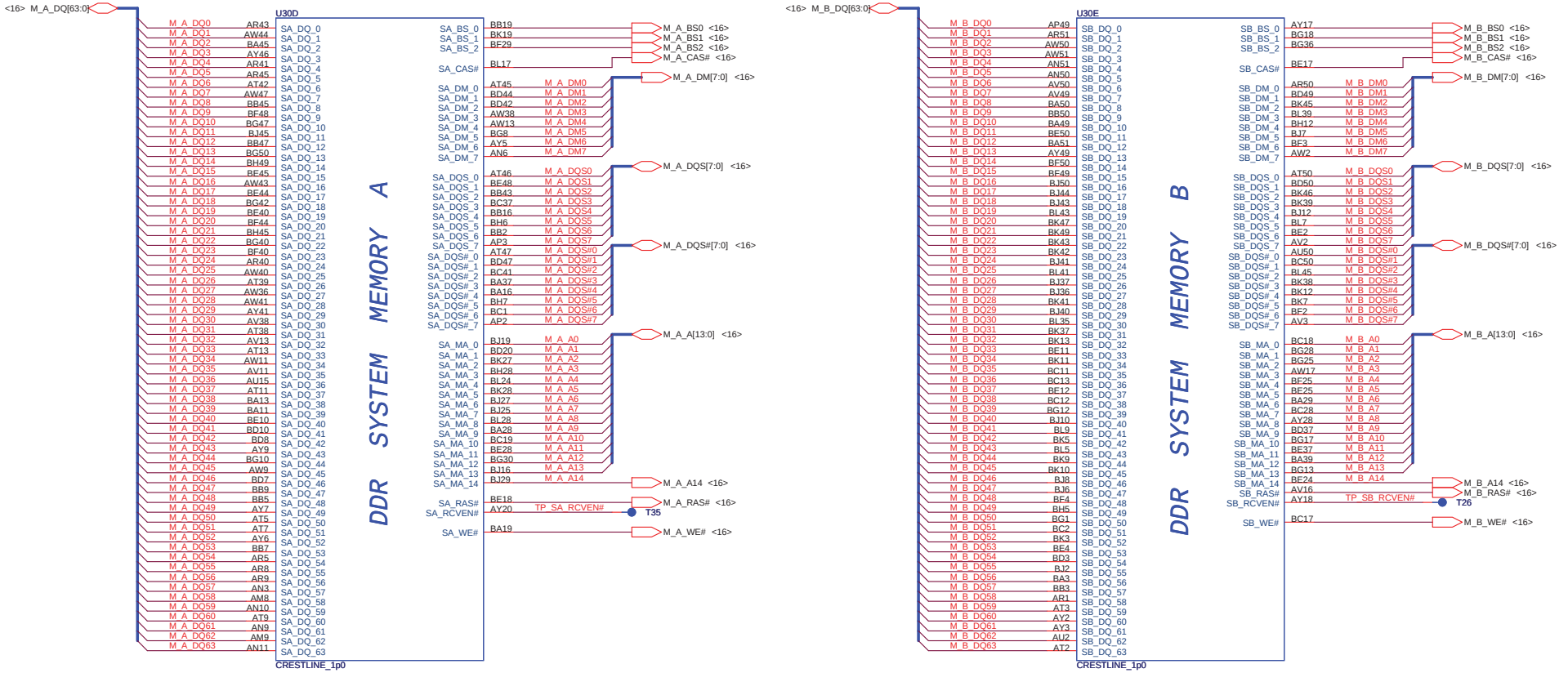
+1.25V
CLK_DREFCLK R409 *4.7K_4
CLK_DREFCLK# R529 EV@0_4
R531 EV@0_4
CLK_DREFSSCLK R411 *4.7K_4
CLK_DREFSSCLK# R532 EV@0_4
R533 EV@0_4
DC Delete R410 and R408 0110

INTEL FAE suggest PD for external graphics



PROJECT : ZD1
Quanta Computer Inc.
Size | Document Number: GMCH (STRAPPING/OTHER 3/7) | Rev: E
Date: Monday, May 07, 2007 | Sheet 7 of 38

# NB(Memory controller)

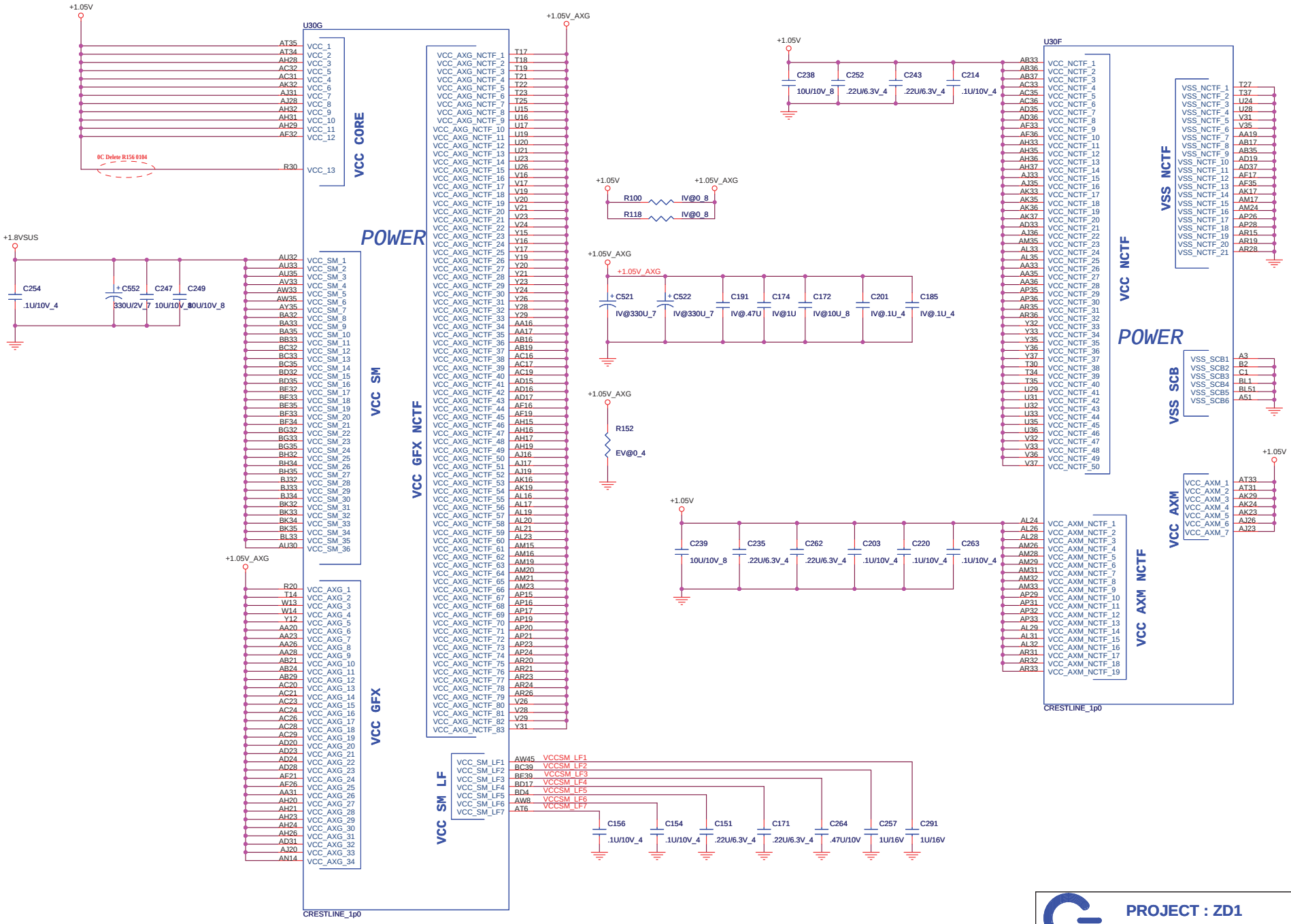



PROJECT : ZD1

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | GMCH DDR(4/7) | E |
| Date: Monday, May 07, 2007 | Sheet 8 of 38 | |

# NB(Power-1)






PROJECT : ZD1

Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | GMCH Power-1(5/7) | E |
| Date: Wednesday, April 25, 2007 | Sheet 9 of 38 | |

# NB(Power-2)

## CRT/TV Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

| Ball | Enable | Disable | Ball | Enable | Disable |
|---|---|---|---|---|---|
| VCCA_CRT | 3.3V | GND | VCCA_C_TVO | 3.3V | GND |
| VCCD_CRT | 1.5V | GND | VCCD_TVO | 1.5V | 1.5V |
| VCCDQ_CRT | 1.5V | GND | VCCABG_DAC | 3.3V | GND |
| VCCA_A_TVO | 3.3V | GND | VSSABG_DAC | GND | GND |
| VCCA_B_TVO | 3.3V | GND | VCC_SYNC | 3.3V | GND |

## LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

| Signal | If SDVO Disable LVDS Disable | If SDVO enable LVDS Disable | If SDVO enable LVDS enable |
|---|---|---|---|
| VCCD_LVDS | GND | 1.8V | 1.8V |
| VCCA_LVDS | GND | GND | 1.8V |
| VCCTX_LVDS | GND | GND | 1.8V |

EXTERNAL INTERNAL

<FAE>
INT VGA disable
VCCSYNC connect to GND

IV&EV Dis/Enable setting

CRB RECOMMEND
180OHM@100MHz
Rdc= 0.09OHM (max)

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCD_TVDAC still +1.5V

Change to
100 ohm Resistor

Use site for filter cap with Gfx enabled CS

IV&EV Dis/Enable setting

<FAE>
VCC_RXR_DMI and VCC_PEG connect to+1.05V

<CRB>
+1.25V AND +1.25M shall be +1.5V for Calero Interposer

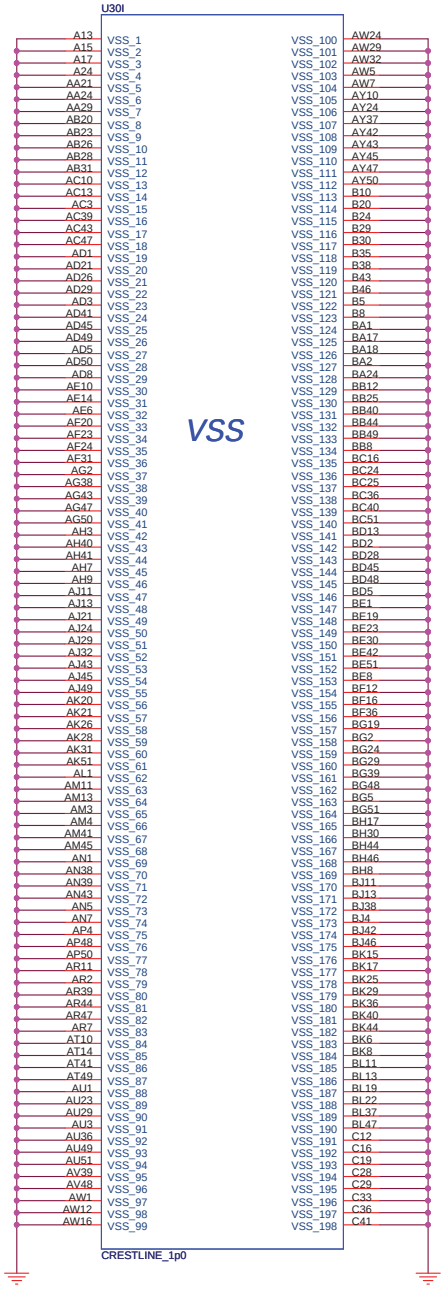
CRESTLINE_1p0

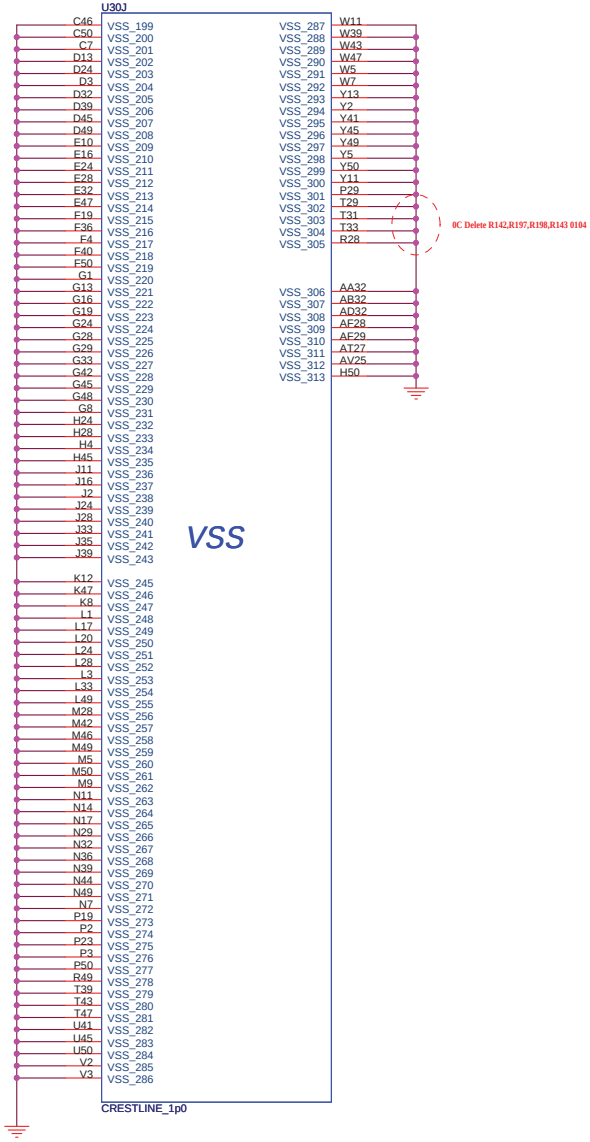


PROJECT : ZD1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | GMCH Power-2(6/7) | E |
| Date: Wednesday, April 25, 2007 | Sheet 10 of 38 | |

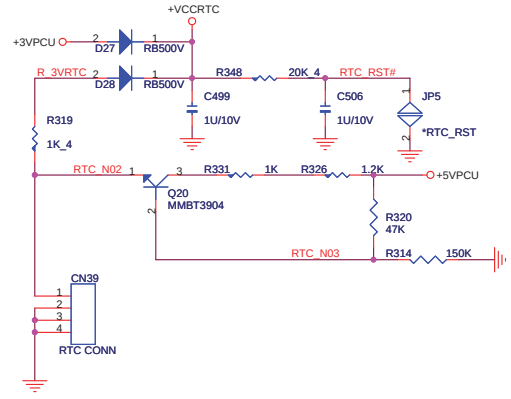
# NB(Power-3)




| | | |
|---|---|---|
| PROJECT : ZD1 | | |
| Quanta Computer Inc. | | |
| Size | Document Number: GMCH Power-3(7/7) | Rev: E |
| Date: Wednesday, April 25, 2007 | Sheet 11 of 38 | |

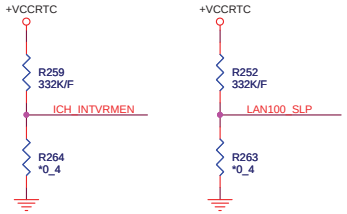
## RTC



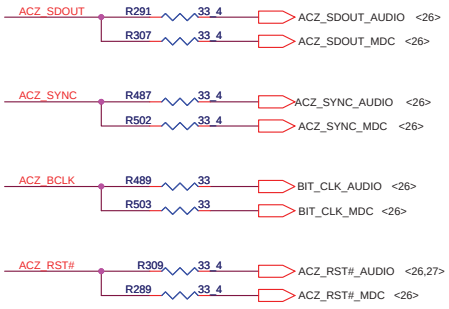

## SB Strap

| | |
|---|---|
| INTVRMEN | Low = Internal VR disable<br>High = Internal VR enable(Default) |

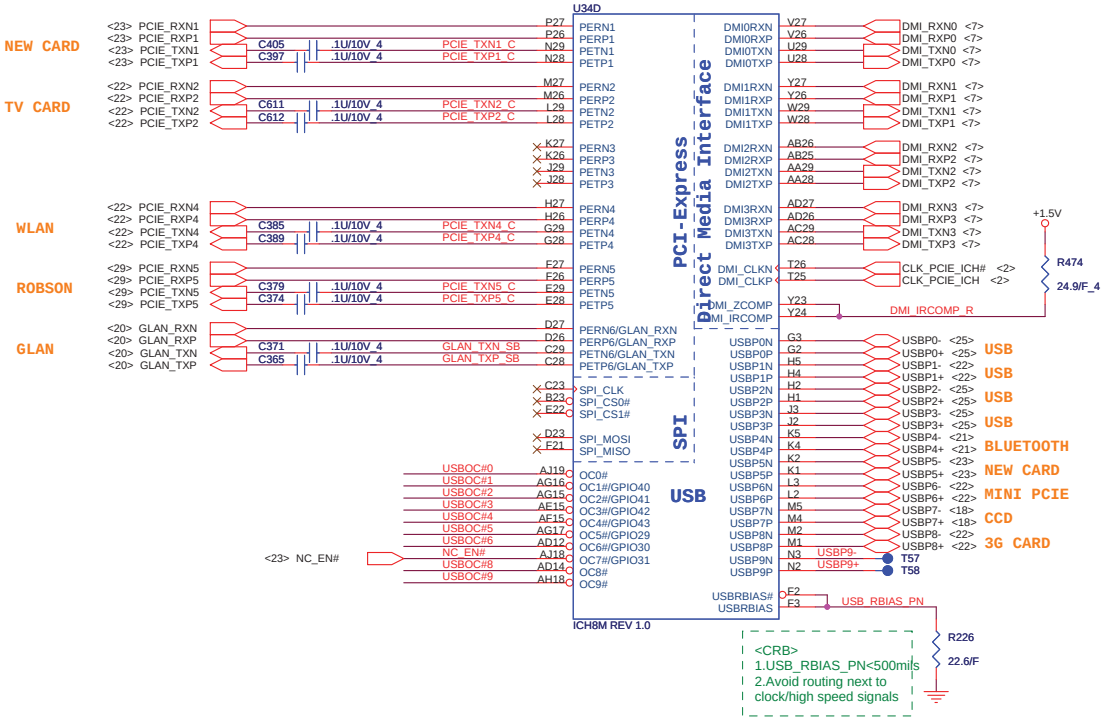
| | |
|---|---|
| LAN100_SLP | Low = Internal VR disable<br>High = Internal VR enable(Default) |



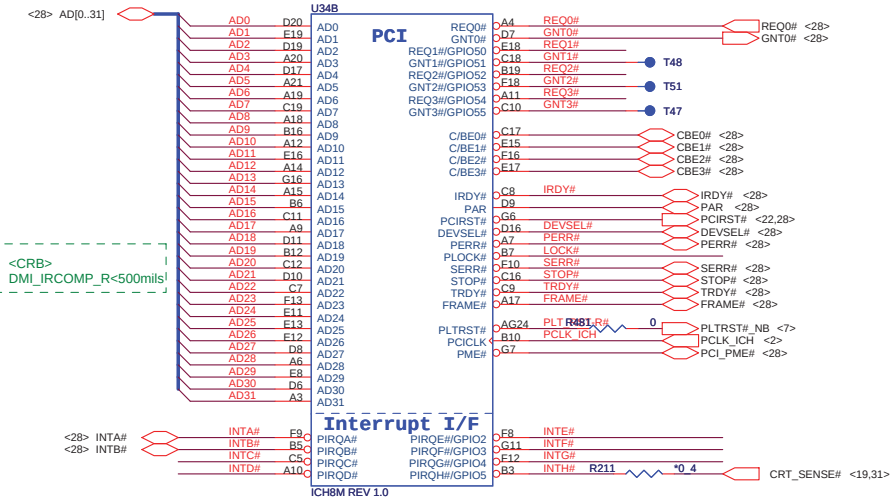

## HDA



## SB-PCIE/USB/DMI



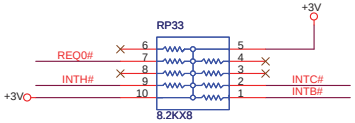

## SB-PCI

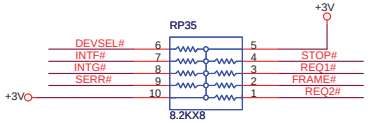



### A16 SWAP Override strap

| PCI_GNT#3 | Low = A16 swap override enabled<br>High = Default |
|---|---|

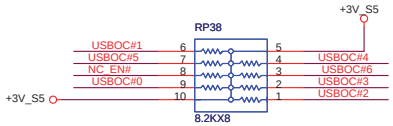
GNT3# R217 *1K_4

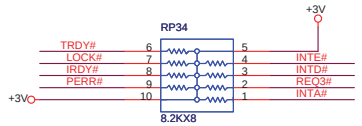


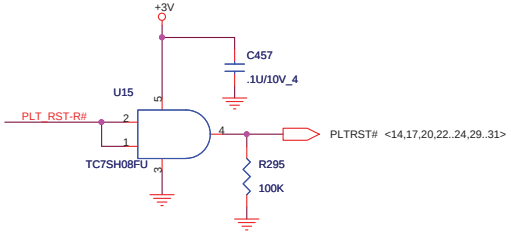




USBOC#8 R248 8.2K_4 +3V_S5

USBOC#9 R491 8.2K_4 +3V_S5



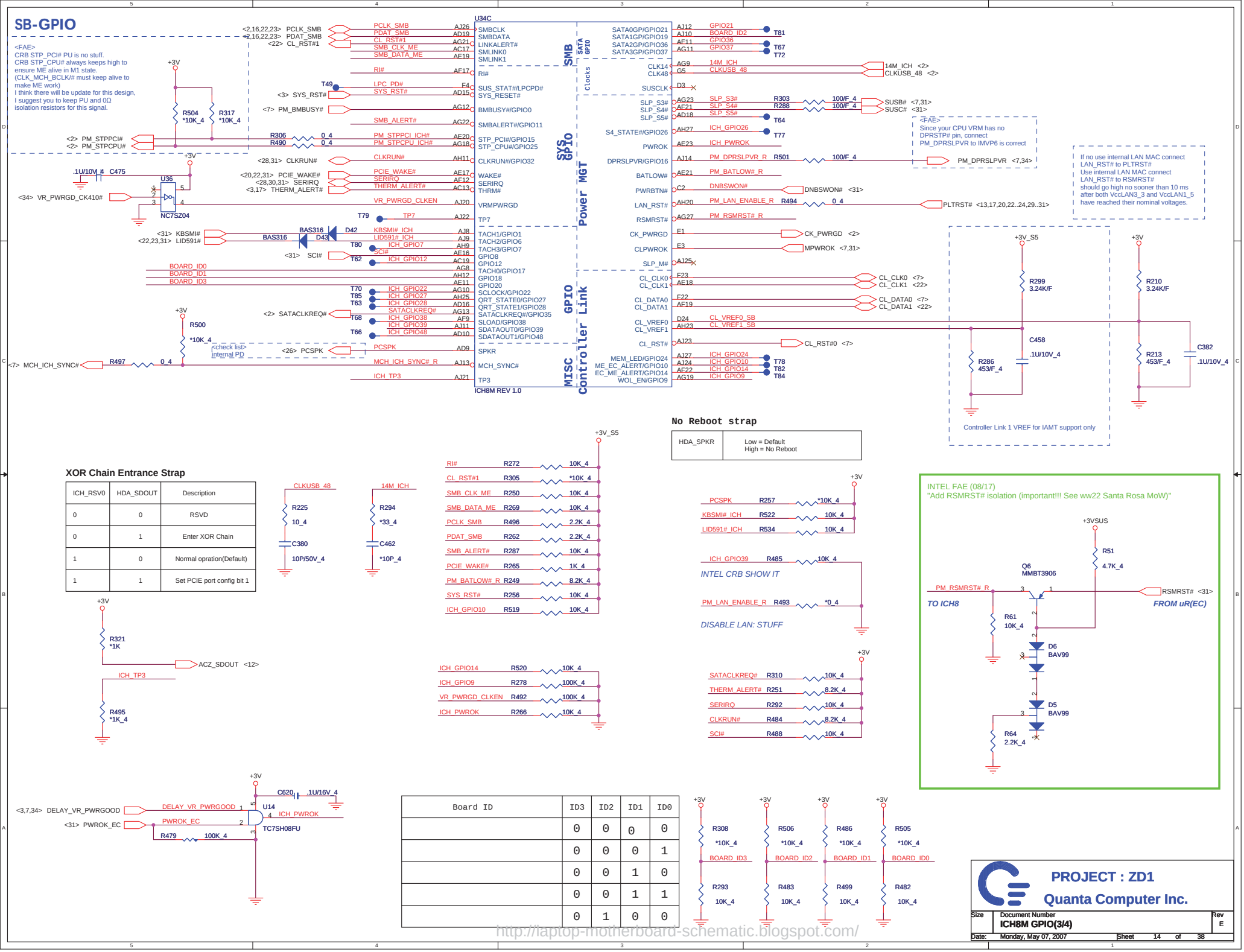






PROJECT : ZD1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | ICH8M PCIE\PCI\USB(2/4) | E |
| Date: Monday, May 07, 2007 | Sheet 13 of 38 | |

# SB-GPIO




<FAE>
CRB STP_PCI# PU is no stuff.
CRB STP_CPU# always keeps high to ensure ME alive in M1 state.
(CLK_MCH_BCLK/# must keep alive to make ME work)
I think there will be update for this design, I suggest you to keep PU and 0Ω isolation resistors for this signal.

<FAE>
Since your CPU VRM has no DPRSTP# pin, connect PM_DPRSLPVR to IMVP6 is correct

If no use internal LAN MAC connect
LAN_RST# to PLTRST#
Use internal LAN MAC connect
LAN_RST# to RSMRST#
should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.

## No Reboot strap

| HDA_SPKR | Low = Default<br>High = No Reboot |
|---|---|

## XOR Chain Entrance Strap

| ICH_RSV0 | HDA_SDOUT | Description |
|---|---|---|
| 0 | 0 | RSVD |
| 0 | 1 | Enter XOR Chain |
| 1 | 0 | Normal opration(Default) |
| 1 | 1 | Set PCIE port config bit 1 |




INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"







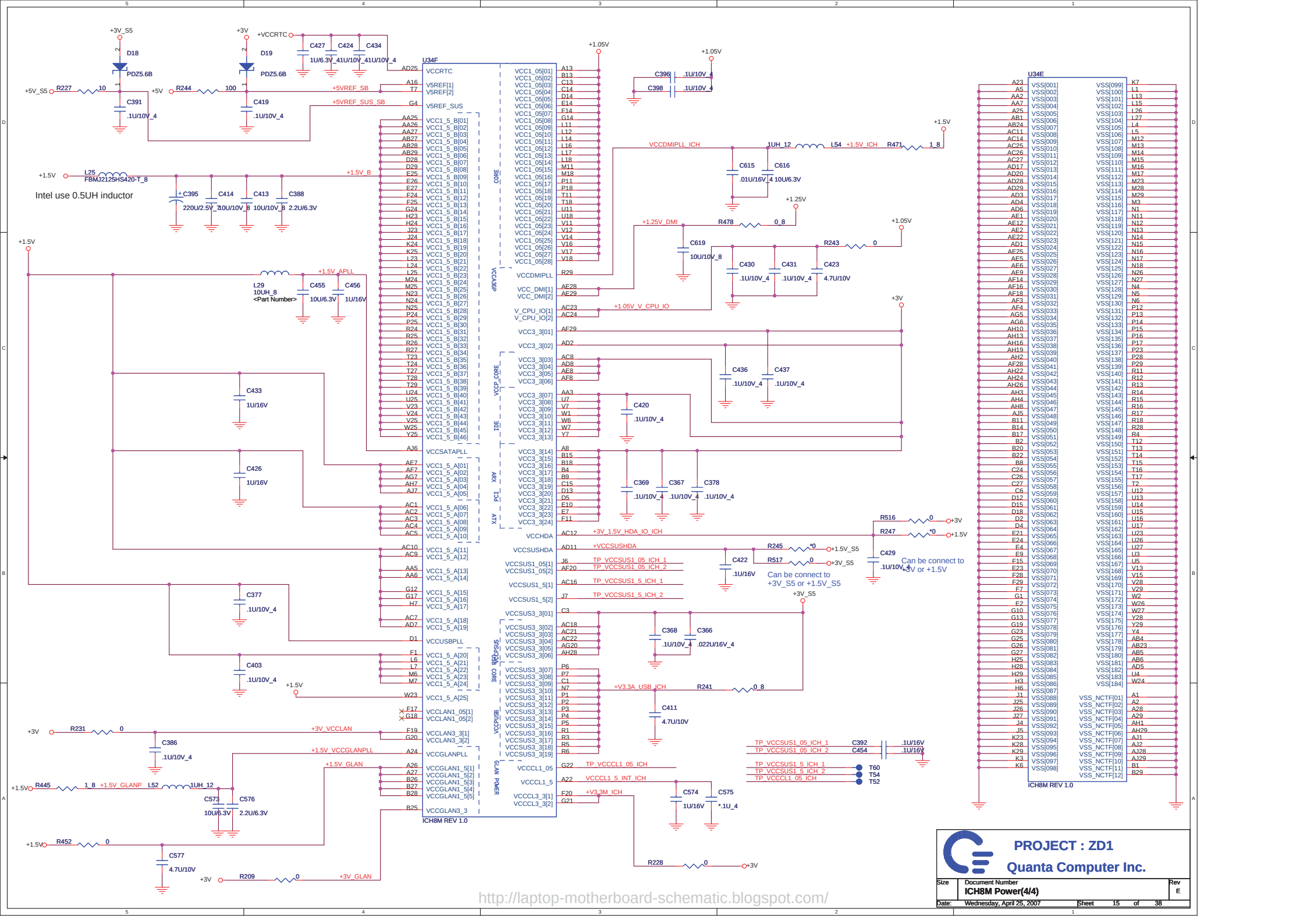
| Board ID | ID3 | ID2 | ID1 | ID0 |
|---|---|---|---|---|
| | 0 | 0 | 0 | 0 |
| | 0 | 0 | 0 | 1 |
| | 0 | 0 | 1 | 0 |
| | 0 | 0 | 1 | 1 |
| | 0 | 1 | 0 | 0 |

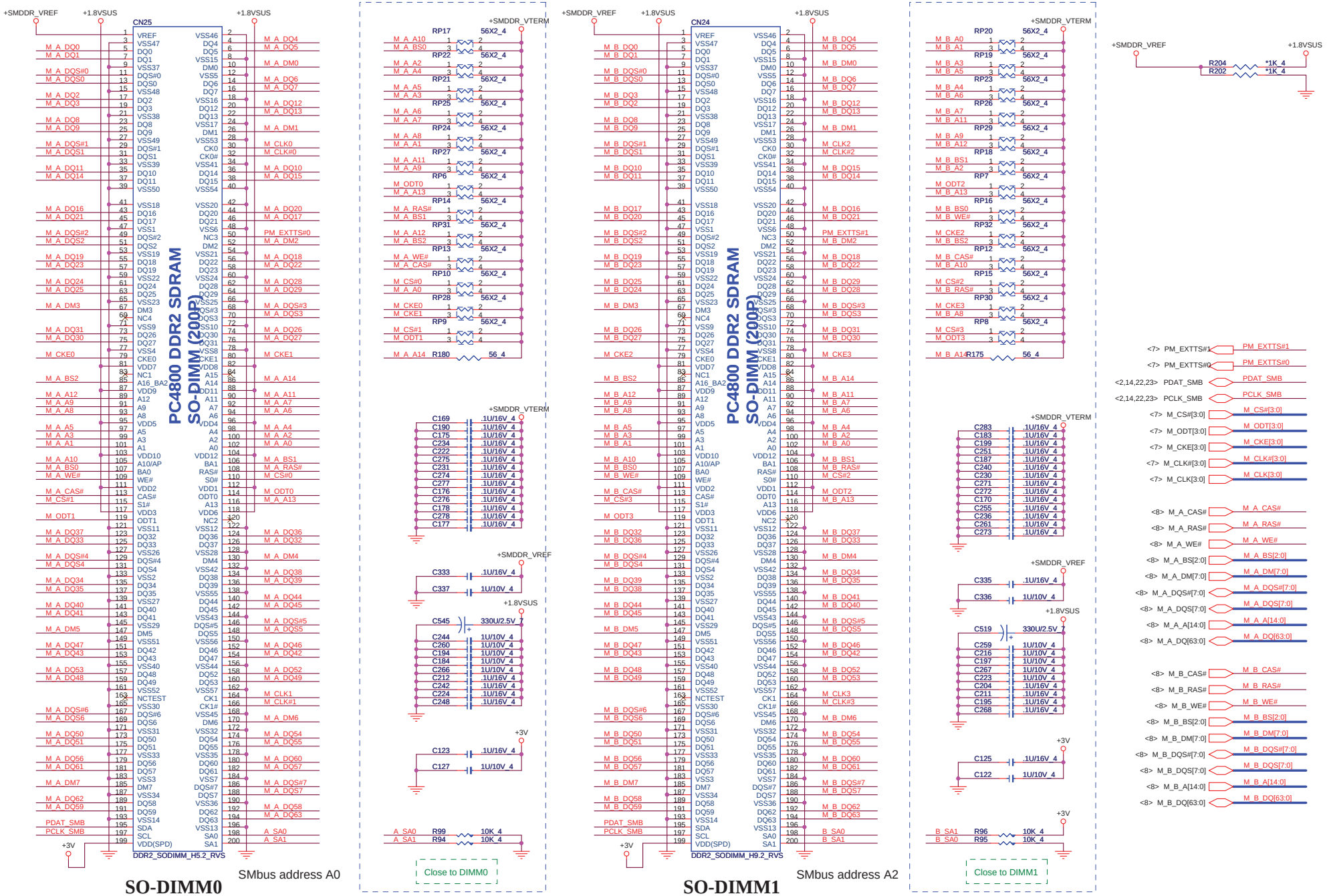





PROJECT : ZD1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | ICH8M GPIO(3/4) | E |
| Date: Monday, May 07, 2007 | Sheet 14 of 38 | |


U34F
ICH8M REV 1.0
U34E
ICH8M REV 1.0
Intel use 0.5UH inductor
L25 FBMJ2125HS420-T_8
L29 10UH_8 <Part Number>
D18 PDZ5.6B
D19 PDZ5.6B
Can be connect to +3V or +1.5V
Can be connect to +3V_S5 or +1.5V_S5
PROJECT : ZD1
Quanta Computer Inc.
Document Number
ICH8M Power(4/4)
Rev E
Date: Wednesday, April 25, 2007
Sheet 15 of 38
http://laptop-motherboard-schematic.blogspot.com/



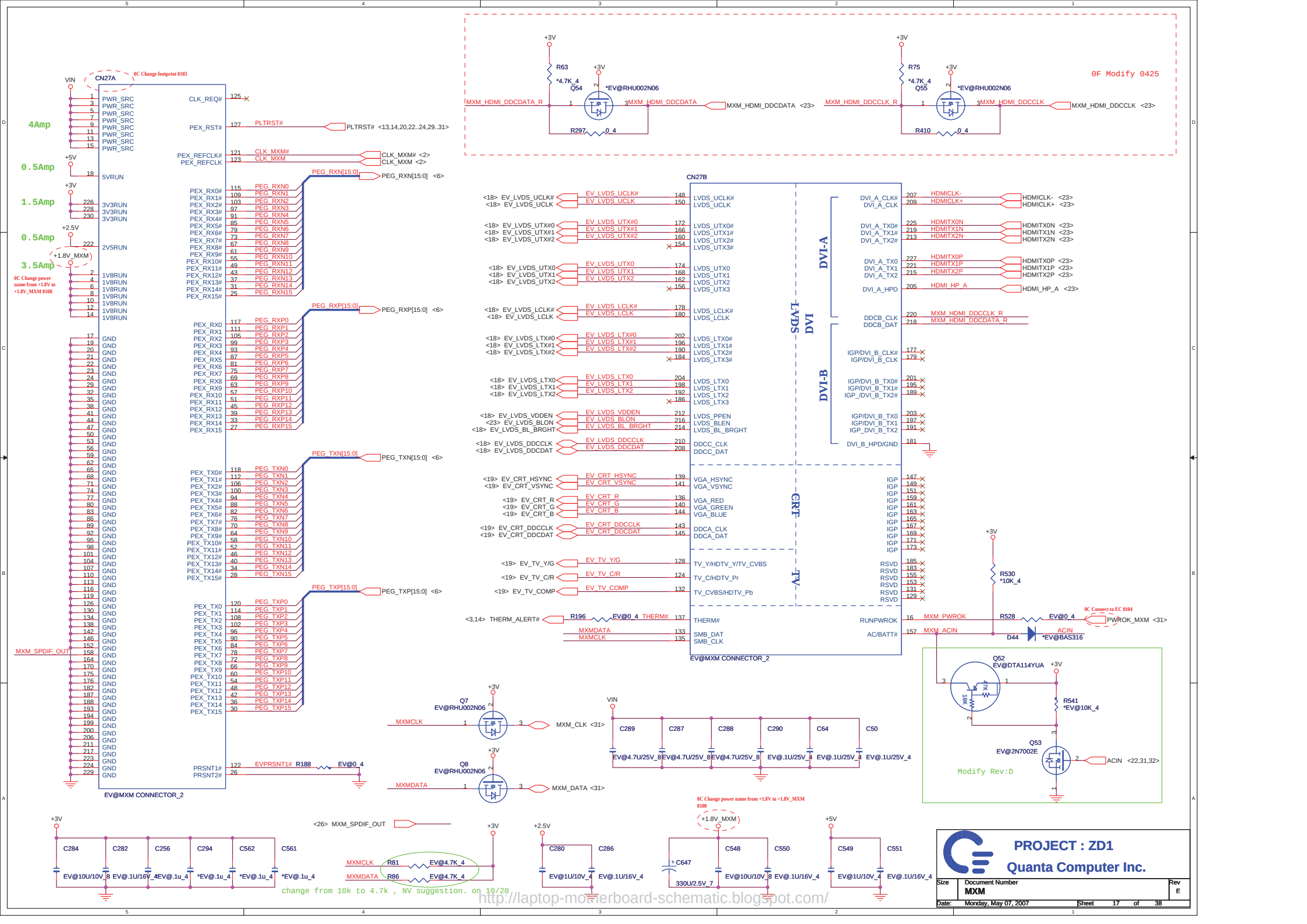



PROJECT : ZD1

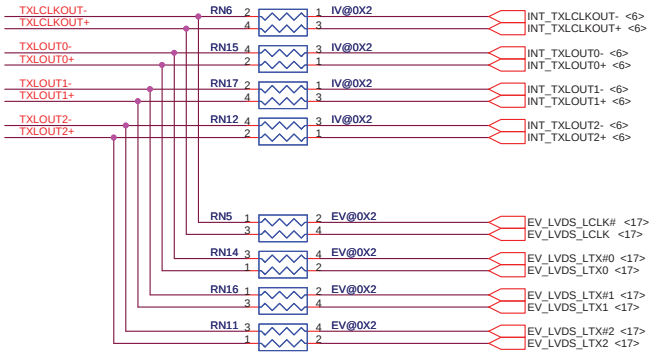
Quanta Computer Inc.

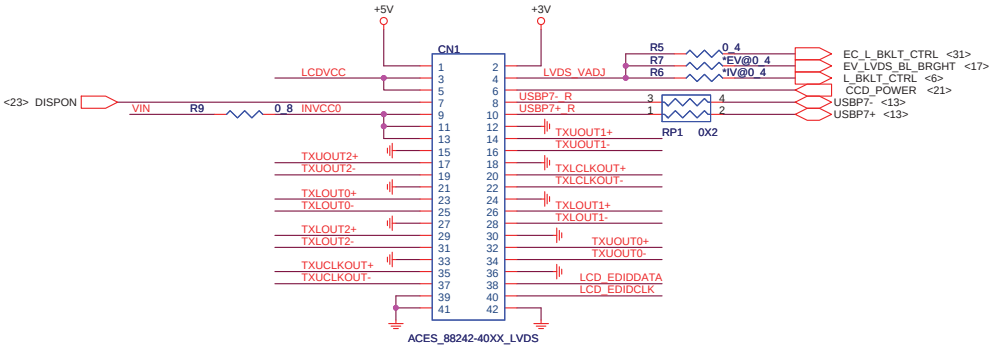
| Size | Document Number | Rev |
|---|---|---|
| | DDRII SO-DIMM | E |

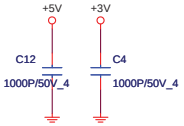
Date: Monday, May 07, 2007 Sheet 16 of 38

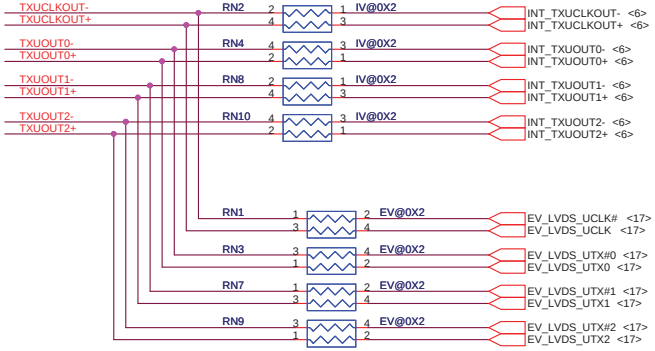

CN27A
0C Change footprint 0103
EV@MXM CONNECTOR_2
CN27B
EV@MXM CONNECTOR_2
0F Modify 0425
Q54 *EV@RHU002N06
Q55 *EV@RHU002N06
R63 *4.7K_4
R75 *4.7K_4
R297 0_4
R410 0_4
MXM_HDMI_DDCDATA_R
MXM_HDMI_DDCDATA
MXM_HDMI_DDCCLK_R
MXM_HDMI_DDCCLK
4Amp
0.5Amp
1.5Amp
0.5Amp
3.5Amp
0C Change power name from +1.8V to +1.8V_MXM 0108
LVDS
DVI
DVI-A
DVI-B
CRT
TV
Q7 EV@RHU002N06
Q8 EV@RHU002N06
MXMCLK
MXMDATA
MXM_CLK <31>
MXM_DATA <31>
Q52 EV@DTA114YUA
Q53 EV@2N7002E
R530 *10K_4
R541 *EV@10K_4
R528 EV@0_4
D44 *EV@BAS316
0C Connect to EC 0104
PWROK_MXM <31>
ACIN <22,31,32>
Modify Rev:D
MXM_SPDIF_OUT
change from 10k to 4.7k , NV suggestion. on 10/20
http://laptop-motherboard-schematic.blogspot.com/
PROJECT : ZD1
Quanta Computer Inc.
Size
Document Number
MXM
Rev
E
Date: Monday, May 07, 2007
Sheet 17 of 38

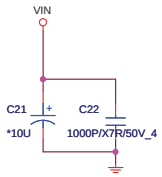
# LVDS

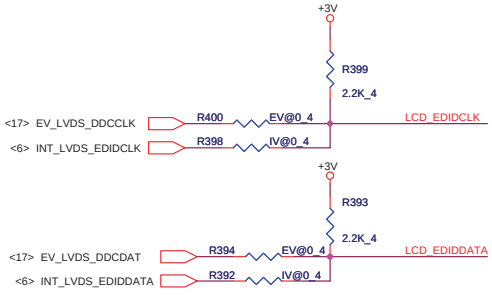


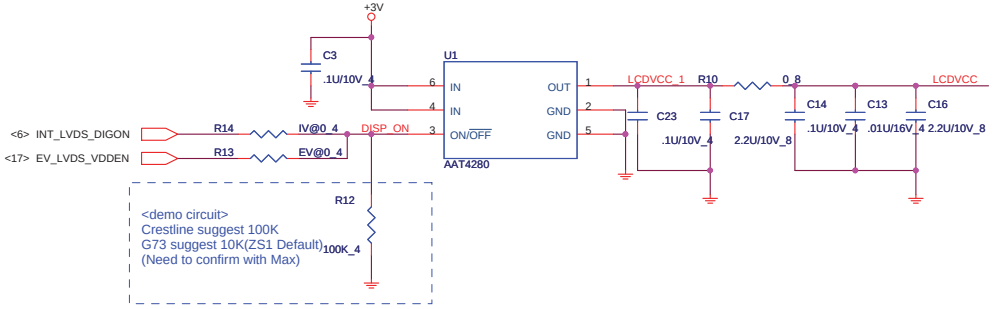



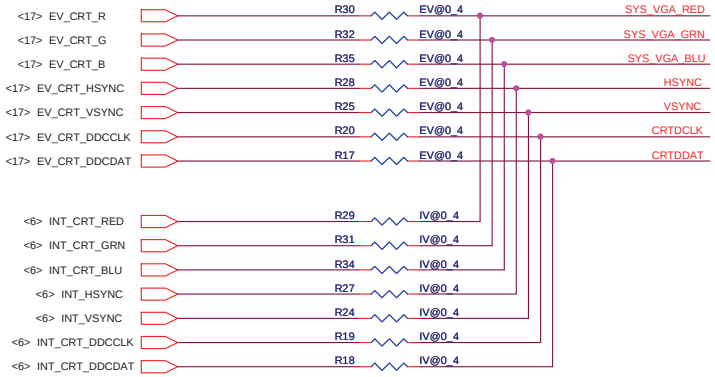

PROJECT : ZD1

Quanta Computer Inc.

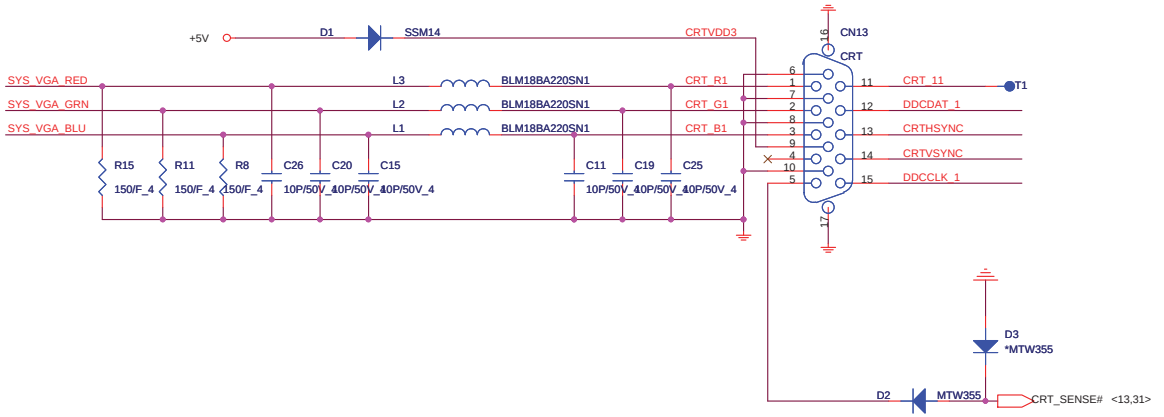
| Size | Document Number | Rev |
|---|---|---|
| | LVDS | E |

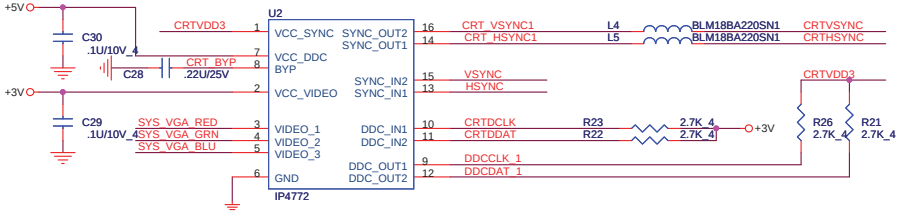
Date: Monday, May 07, 2007 Sheet 18 of 38

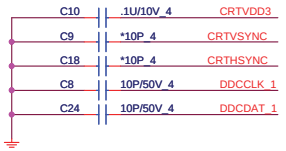
## CRT Select



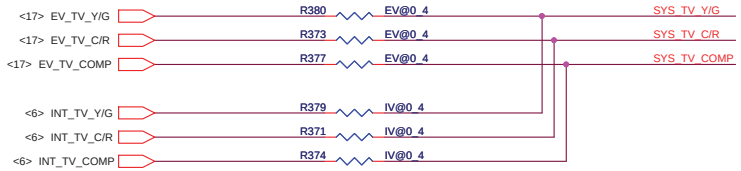

## CRT CONNECTOR AND ESD

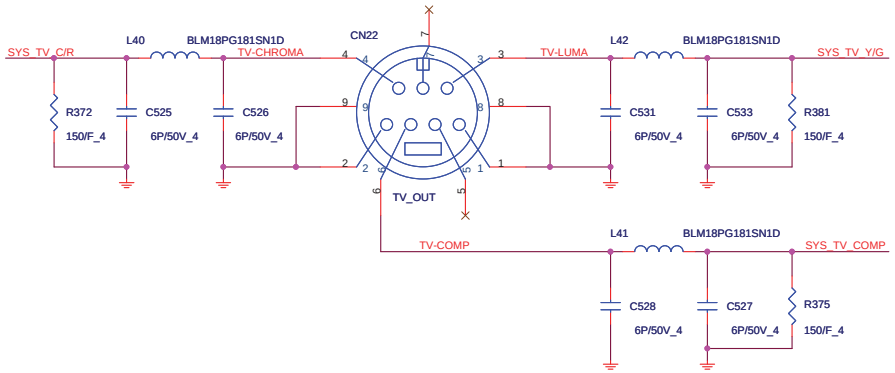


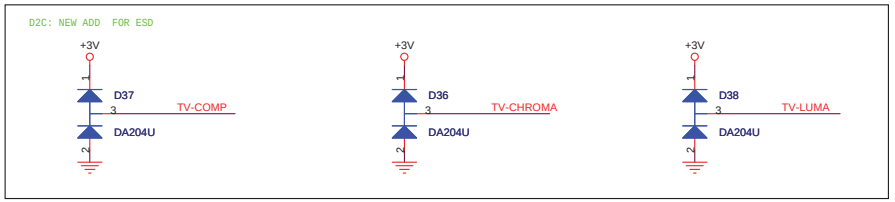




## TV Out (SVHS) MiniDIN 7-pin



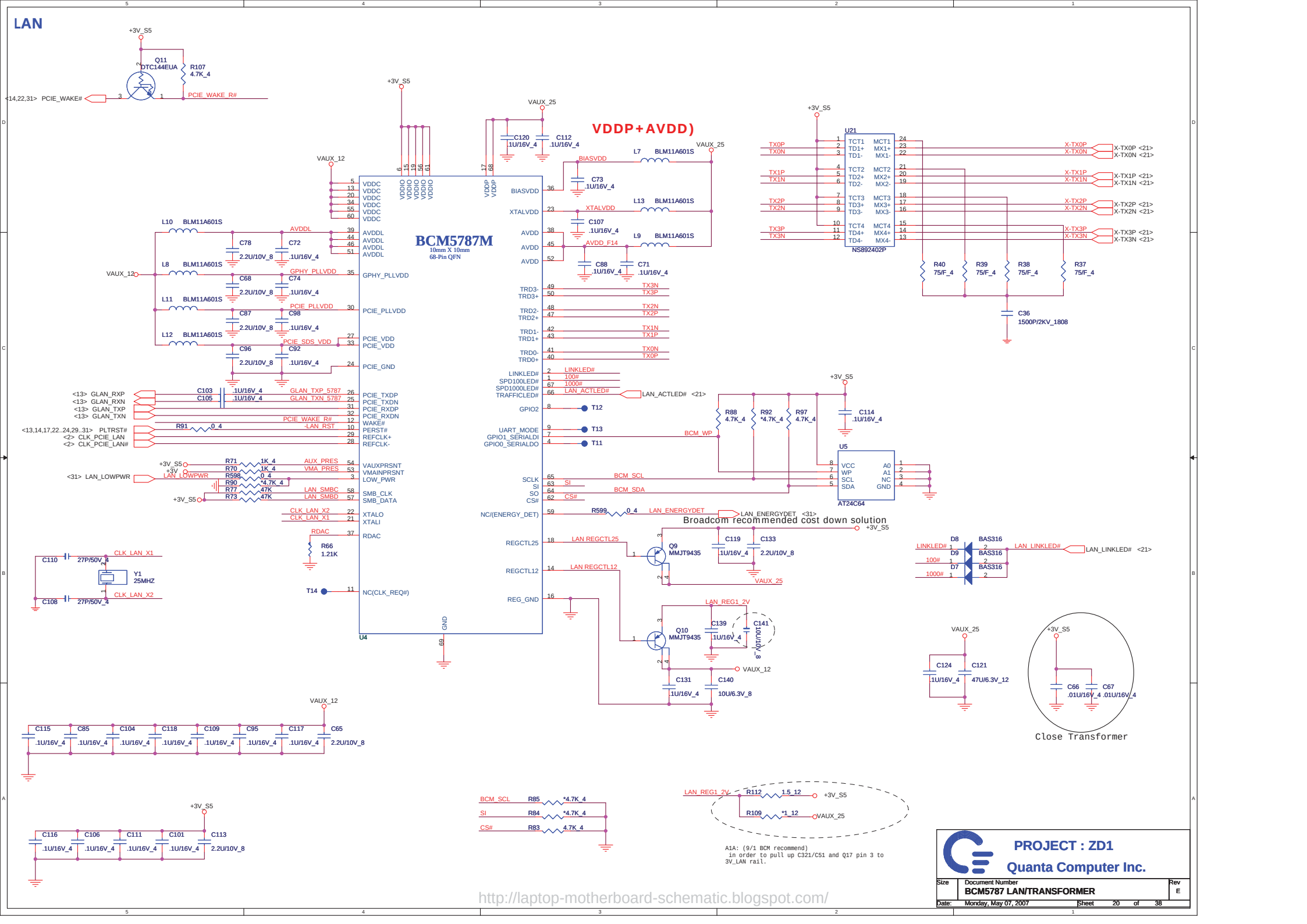




**PROJECT : ZD1**

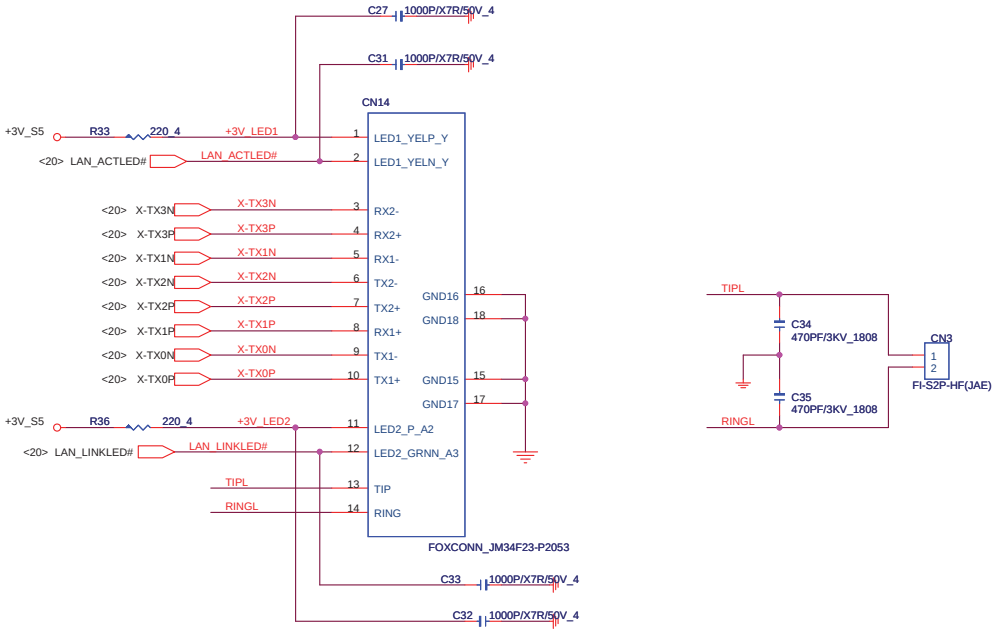
**Quanta Computer Inc.**

| Size | Document Number | Rev |
|---|---|---|
| | CRT/TVOUT | E |
| Date: Monday, May 07, 2007 | Sheet 19 of 38 | |

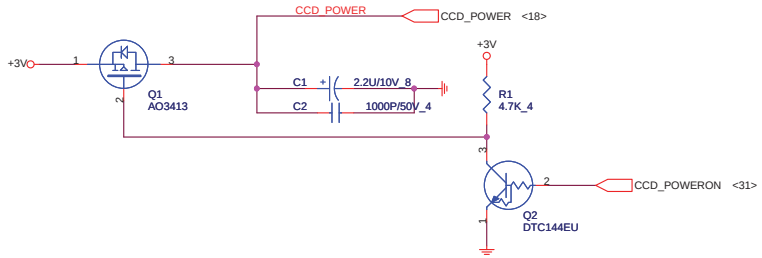
# LAN



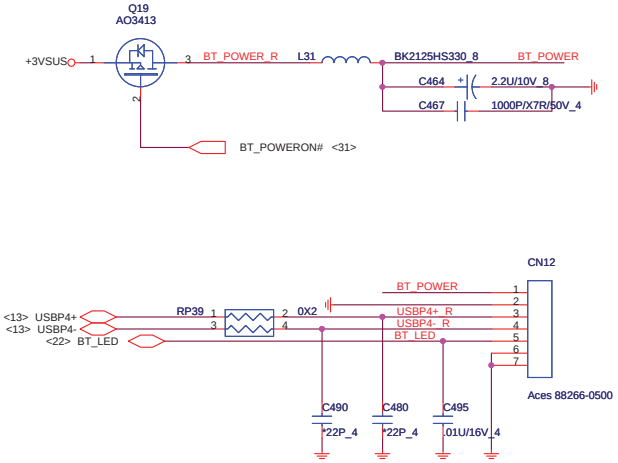
## RJ45-11



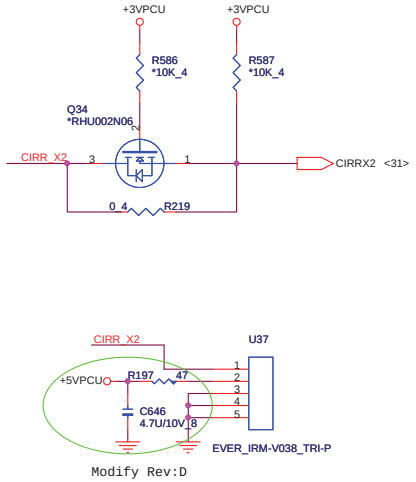

## CAMERA MODULE CONNECTOR



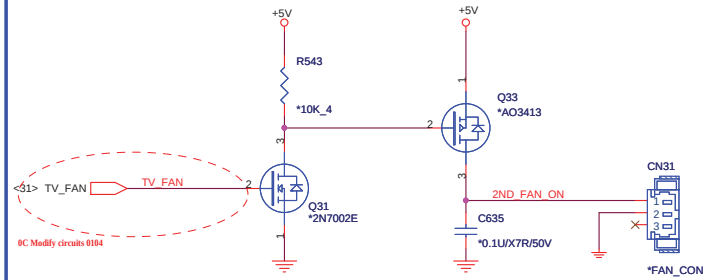

## BLUETOOTH MODULE CONNECTOR




## CIR




## 2nd FAN



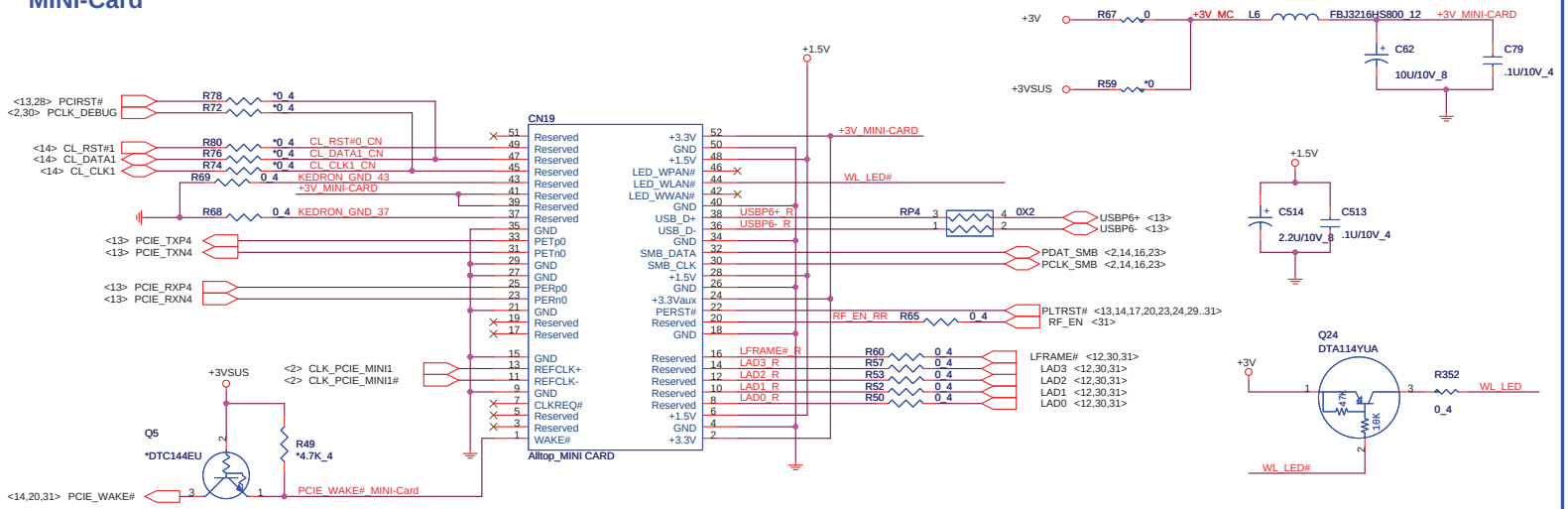



**PROJECT : ZD1**

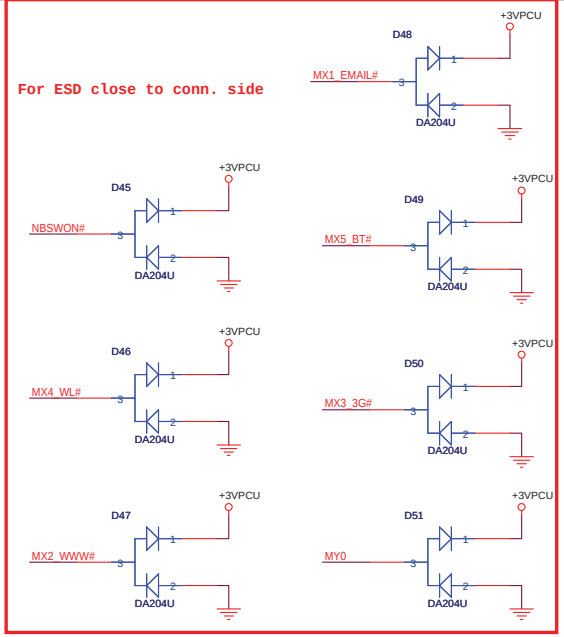
**Quanta Computer Inc.**

| Size | Document Number | Rev |
|---|---|---|
| | BT/CCD/RJ45-11/CIR/2nd FAN | E |
| Date: Monday, May 07, 2007 | Sheet 21 of 38 | |

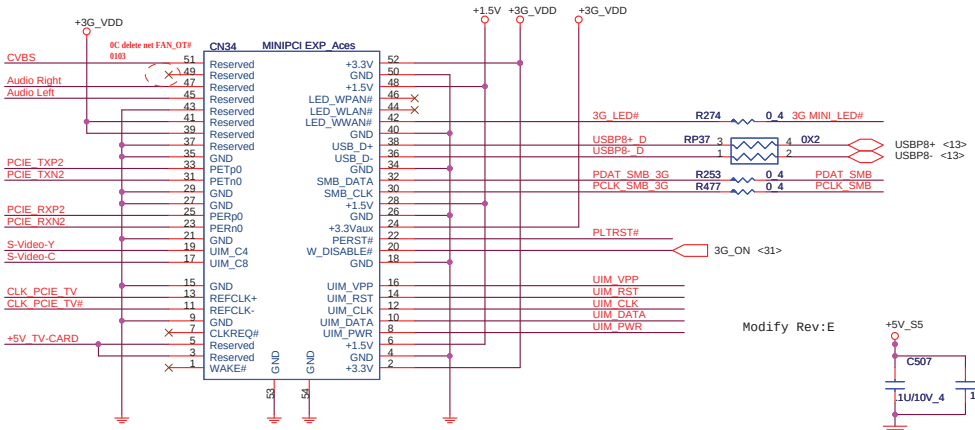
# MINI-Card



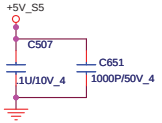

**For ESD close to conn. side**

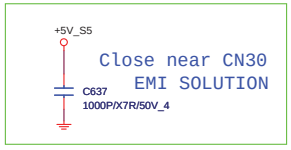


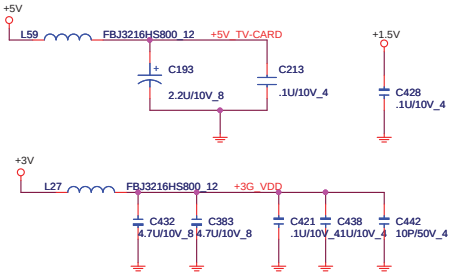

# 3G/TV MINI CARD

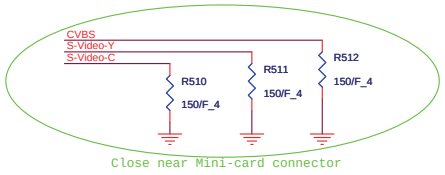



Modify Rev:E

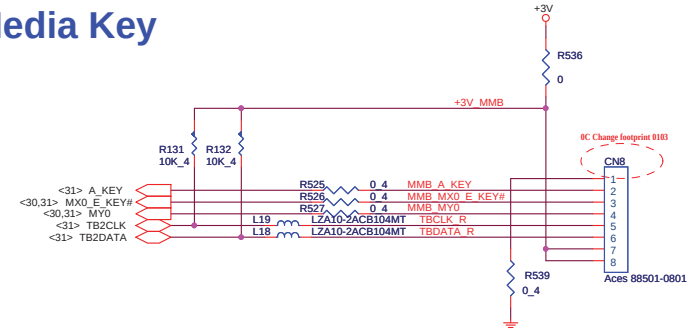


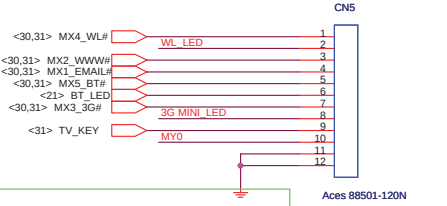



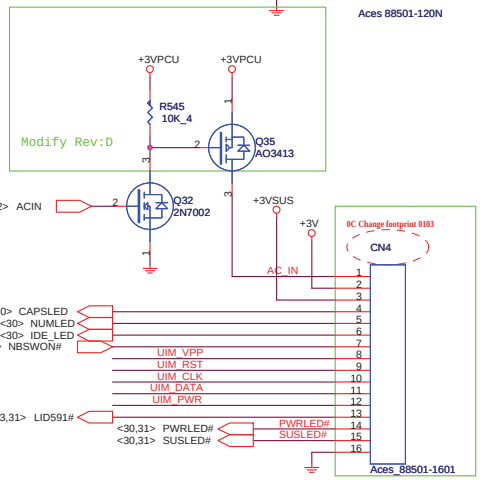



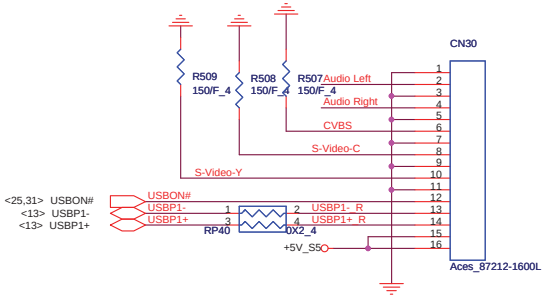




# Media Key

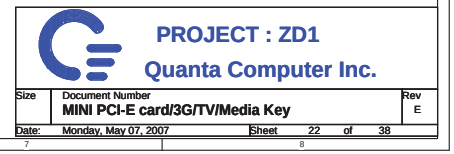






## New card

CN9

<13> PCIE_TXP1
<13> PCIE_TXN1
<13> PCIE_RXP1
<13> PCIE_RXN1
<2> CLK_PCIE_NEW_C
<2> CLK_PCIE_NEW_C#
<13> NC_EN#
C381
C376
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
<13> USBP5+
<13> USBP5-
R441 0_4 USBP5+_R
R442 0_4 USBP5-_R

GND5 GND1 PETp0 PETn0 GND2 PERp0 PERn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND6 GND27 GND28

*Aces_NEW CARD

CN44

PCIE_TXP1
PCIE_TXN1
PERP3
PERN3
CLK_PCIE_NEW_C
CLK_PCIE_NEW_C#
NC_EN#
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
USBP5+_R
USBP5-_R

GND1 GND2 PETp0 PETn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND29 GND30 GND27 GND28

*Taitwun_NEW CARD

CN43

PCIE_TXP1
PCIE_TXN1
PERP3
PERN3
CLK_PCIE_NEW_C
CLK_PCIE_NEW_C#
NC_EN#
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
USBP5+_R
USBP5-_R

GND1 GND2 PETp0 PETn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND29 GND30 GND27 GND28

FOX_EXPCARD

## NEW CARD'S POWER SWITCH

U33
QFN-TPS2231RGP

+3V → 3.3VIN 3.3VIN → 3.3VOUT 3.3VOUT → +NEW_3V 1.3A
+3V_S5 → AUXIN → AUXOUT → +NEW_3VAUX 275mA
+1.5V → 1.5VIN 1.5VIN → 1.5VOUT 1.5VOUT → +NEW_1.5V 650mA
PLTRST#_NEW → *SYSRST# *SHDN# → *STBY# *CPPE# *CPUSB# → NC_EN#
*RCLKEN NC GND GNDPAD → PERST# OC# → PERST#

REV:B MODIFY
0C Connect to NC_EN# 0103
TI : AL002231001
RICOH : AL005538001
GMT : AL000577008

<13,14,17,20,22,24,29..31> PLTRST#
Q37 2N7002
PLTRST#_NEW
REV:B MODIFY

+3V_S5: C599 .1U/10V_4
+3V: C581 .1U/10V_4, C582 .1U/10V_4
+1.5V: C598 .1U/10V_4, C597 .1U/10V_4
+NEW_3VAUX: C351 .1U/10V_4
+NEW_3V: C579 2.2U/10V_8, C354 .1U/10V_4, C357 .1U/10V_4
+NEW_1.5V: C348 2.2U/10V_8, C344 .1U/10V_4

+NEW_3V
Q30 2N7002E
RP41 10KX2_4
<2,14,16,22> PDAT_SMB
NEW_SMDATA

+NEW_3V
Q29 2N7002E
<2,14,16,22> PCLK_SMB
NEW_SMCLK

## LID SWITCH

+3V
R194 100K_4
<18> DISPON
DISPON D11 BAS316 LID591# <14,22,31>
D10 BAS316 R190 IV@0_4 INT_LVDS_BLON <6>
R189 EV@0_4 EV_LVDS_BLON <17>
R192 *1K_4
R191 100K_4
<demo circuit>
Crestline suggest 100K
G73 suggest 10K(ZS1 Default)
(Need confirm with Max)
Q12 DTC144EU
EC_FPBACK# <31>

## HDMI

+5V
D35 BAS316 D34 BAS316
NV suggestion near HDMI connector
R354 2K_4 R353 2K_4
<17> MXM_HDMI_DDCCLK → L39 220R_100MHZ → HDMI_DDCCLK
C515 *.1U_4
<17> MXM_HDMI_DDCDATA → L38 220R_100MHZ → HDMI_DDCDATA
C516 *.1U_4

+5V
C632 .1U/16V_4 C631 .1U/16V_4 C633 .1U/16V_4

CN21 0C Change footprint 0103
<17> HDMITX2P HDMITX2N HDMITX1P HDMITX1N HDMITX0P HDMITX0N HDMICLK+ HDMICLK-
HDMI_DDCCLK HDMI_DDCDATA
D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET
SHELL1 SHELL2 GND GND
HDMI CON

<17> HDMI_HP_A
R359 EV@10K_4 R602 1K_4 HP_DET
R356 EV@10K_4

HDMI monitor default have PU to 5V.So ZY3 PD for level change.And serial R for current limited

U26 *RClamp0514M_AG
HDMITX0P HDMITX0N HDMI_HP_A → VCC GND

U27 *RClamp0514M_AG
HDMITX2P HDMITX2N HDMITX1P HDMITX1N → VCC GND

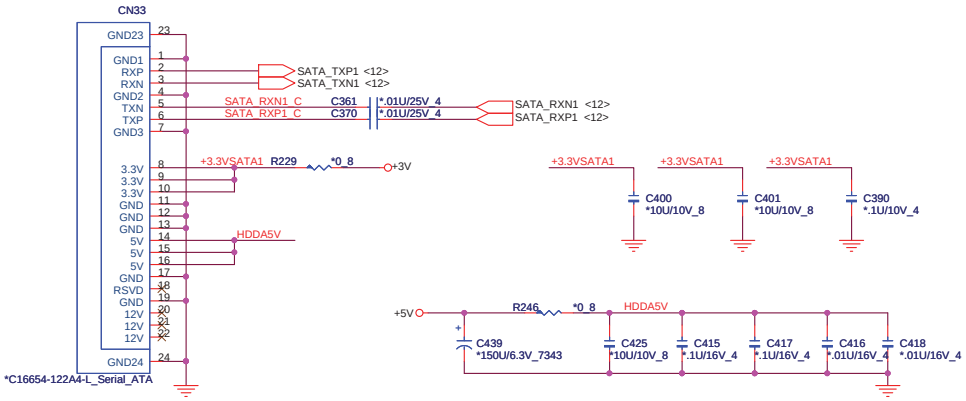
U25 *RClamp0514M_AG
HDMICLK+ HDMICLK- HDMI_DDCDATA → VCC GND → HDMI_DDCCLK



PROJECT : ZD1
Quanta Computer Inc.

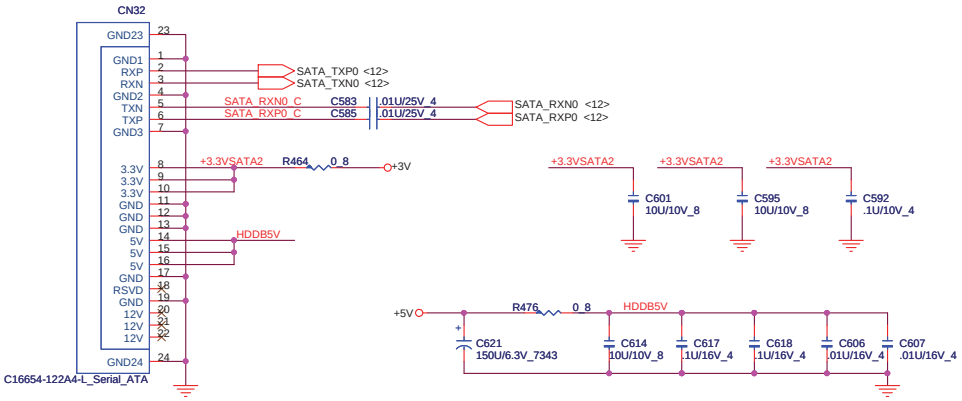
| Size | Document Number | Rev |
|---|---|---|
| | NEW CARD/HDMI/LID | E |
| Date: Monday, May 07, 2007 | Sheet 23 of 38 | |

## SATA HDD1

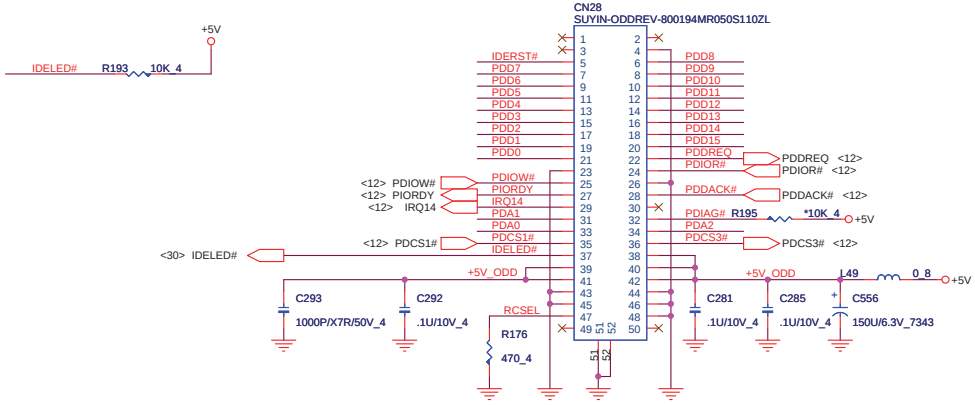


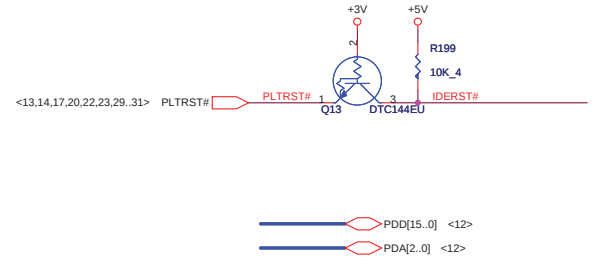

## SATA HDD2

Main




## ODD (PATA)



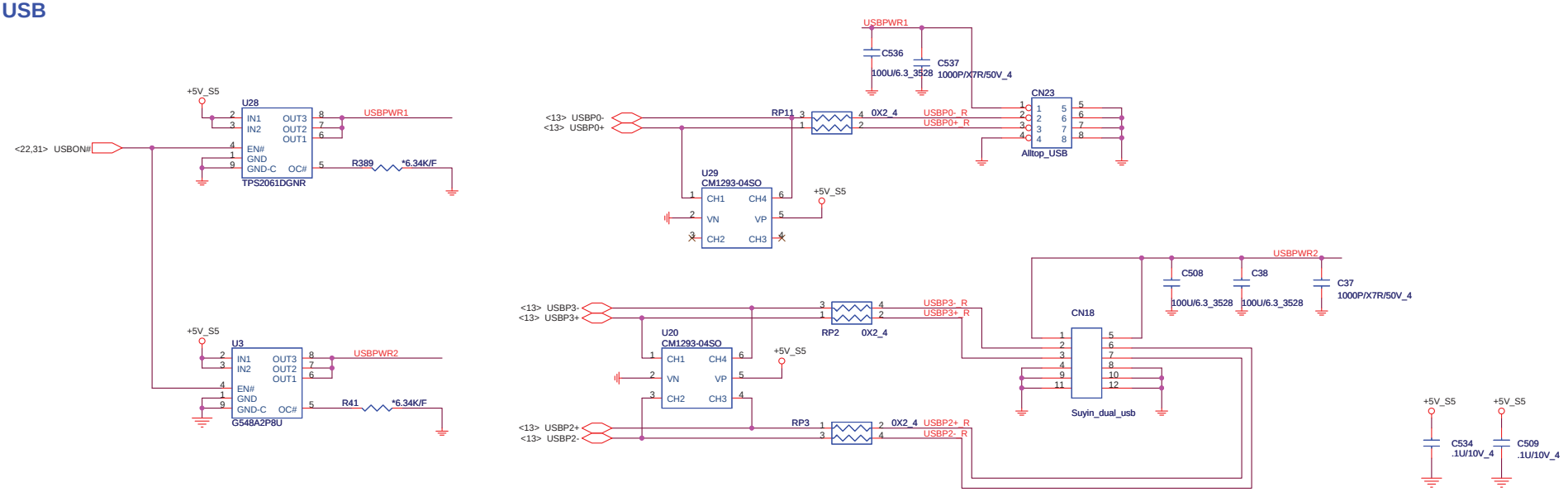




PROJECT : ZD1

Quanta Computer Inc.

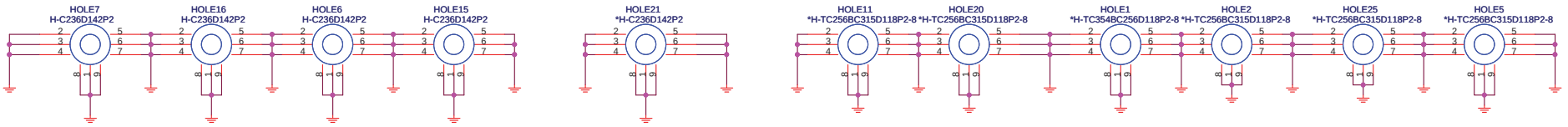
| Size | Document Number | Rev |
|---|---|---|
| | SATA-HDD & PATA-ODD | E |
| Date: Monday, May 07, 2007 | Sheet 24 of 38 | |

# USB

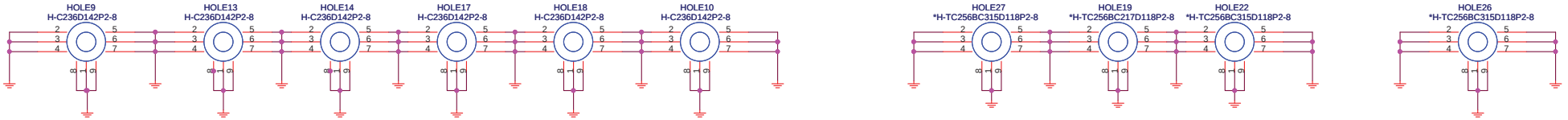



# HOLES

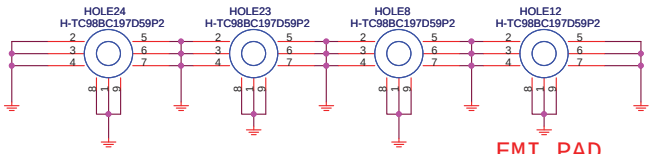
## CPU NUT



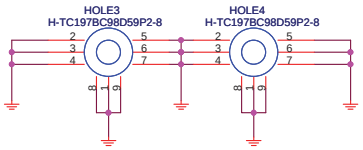

## MXM NUT



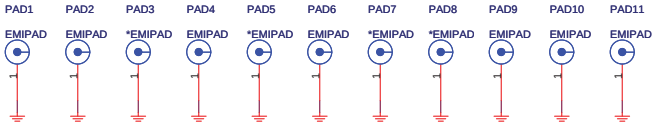

## MINI CARD NUT

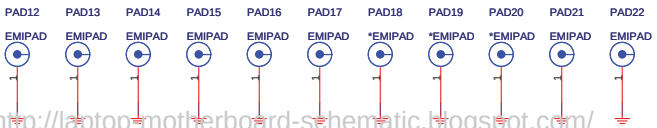



## MDC NUT



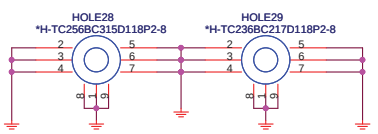

## EMI PAD



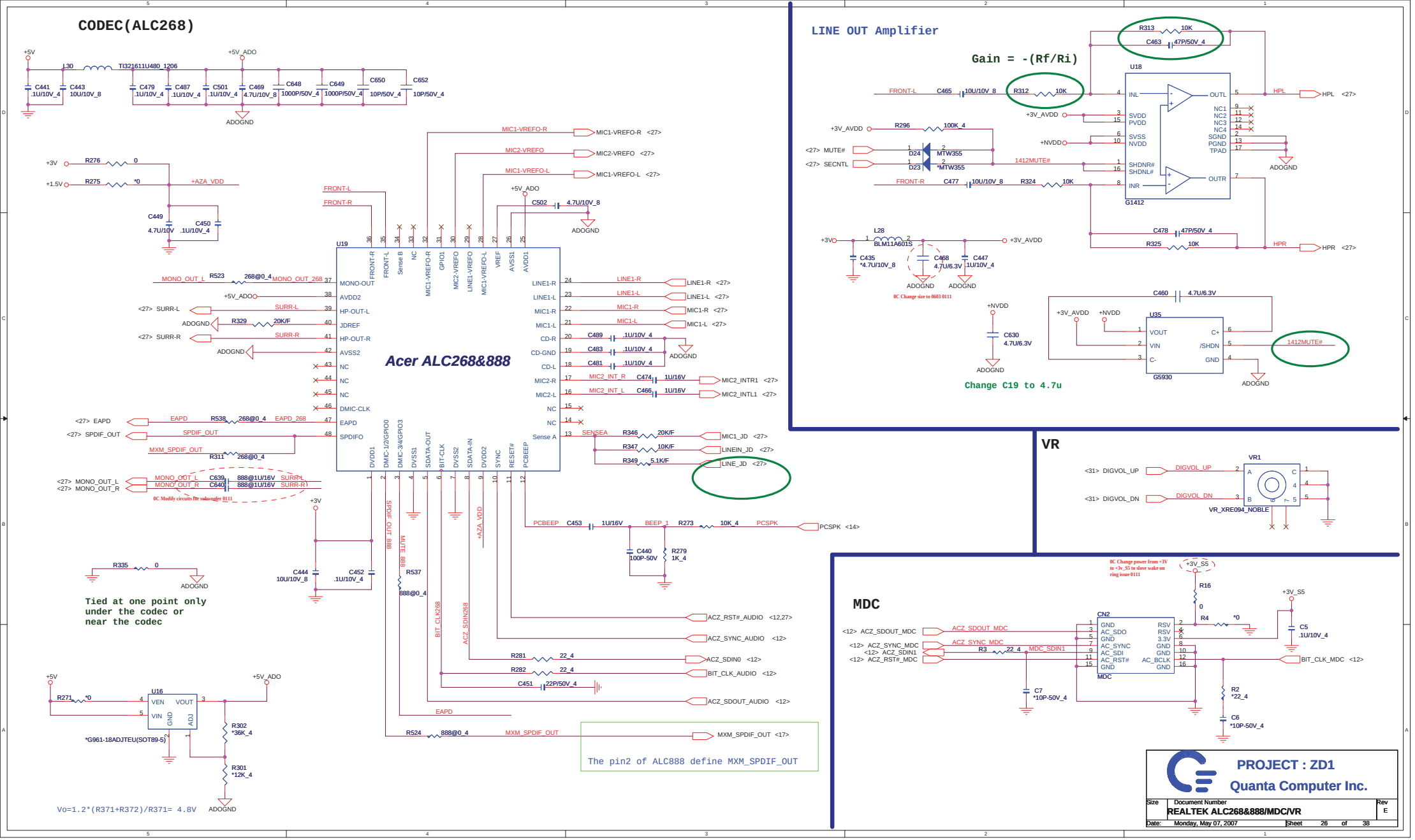

Footprint error: PAD15 , PAD4 ,PAD16:
emipad97x87

Modify Rev:E

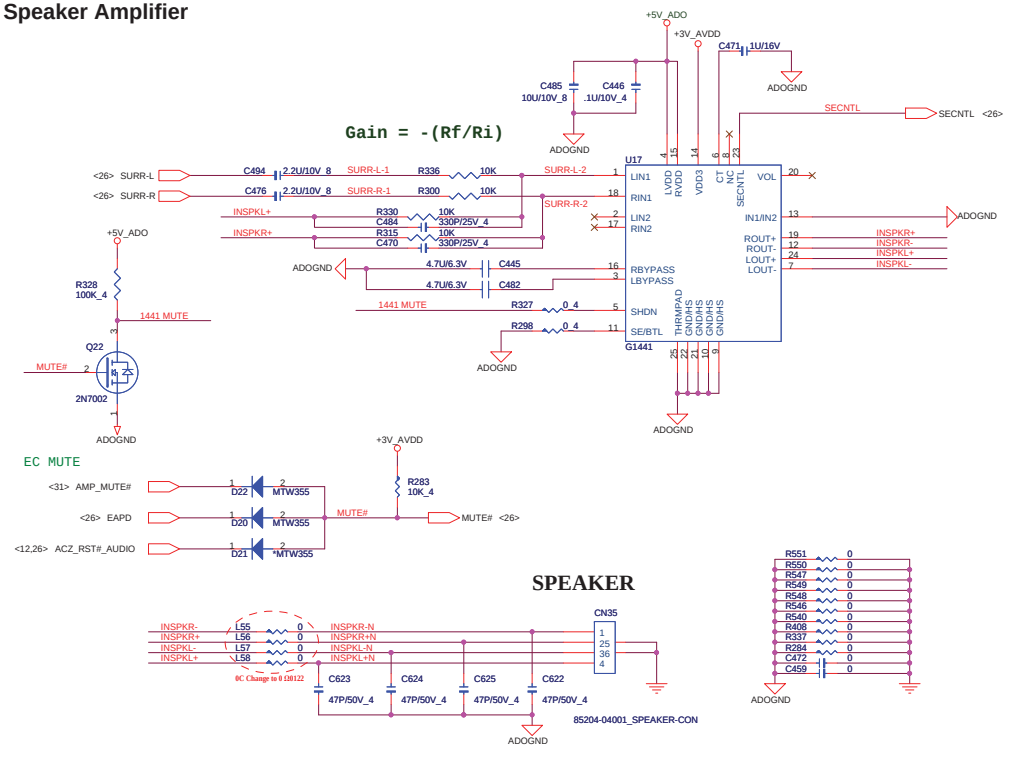



PROJECT : ZD1
Quanta Computer Inc.

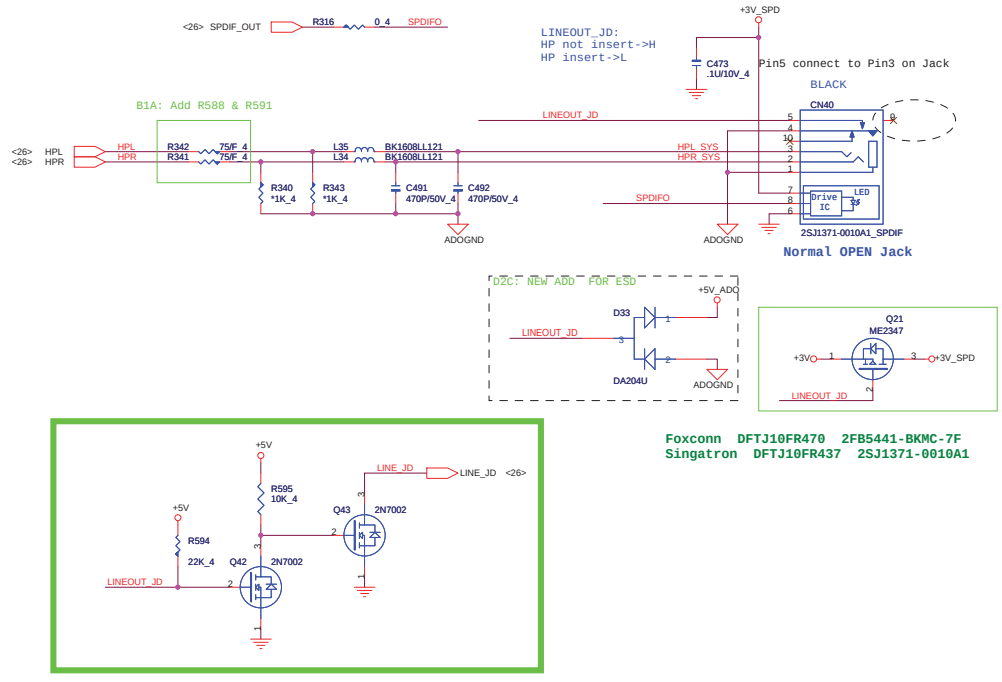
| Size | Document Number | Rev |
|---|---|---|
| | USB/HOLE | E |
| Date: Monday, May 07, 2007 | Sheet 25 of 38 | |



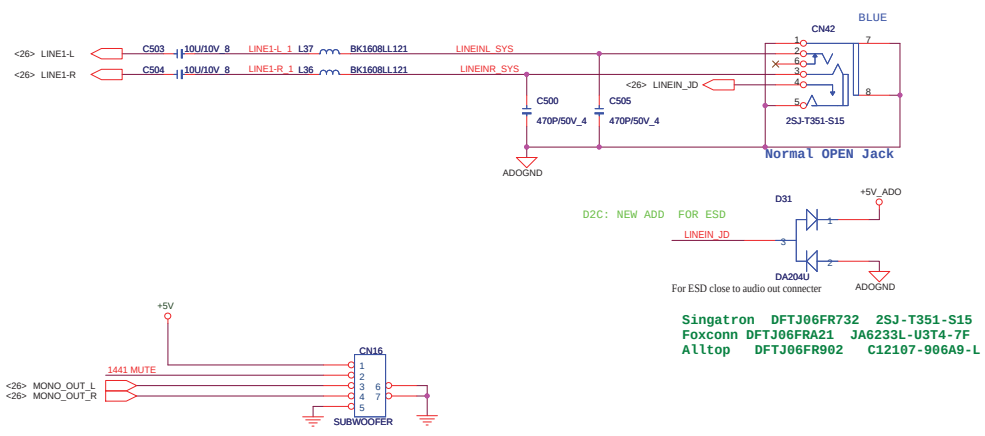
## Speaker Amplifier



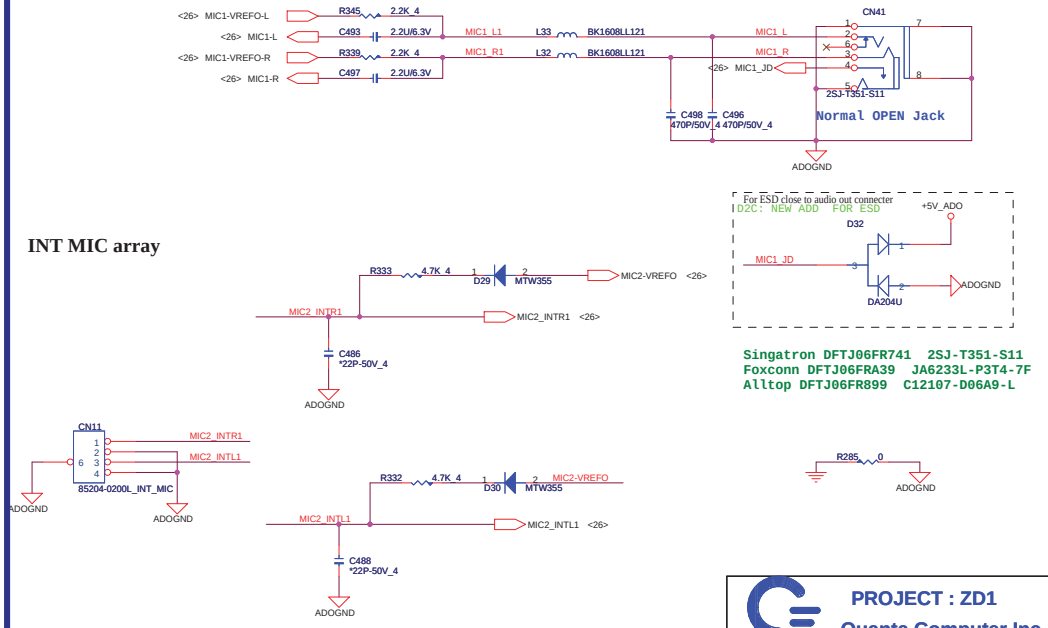

## SYSTEM LINE OUT/SPDIF




## SYSTEM LINE IN/SUBWOOFER

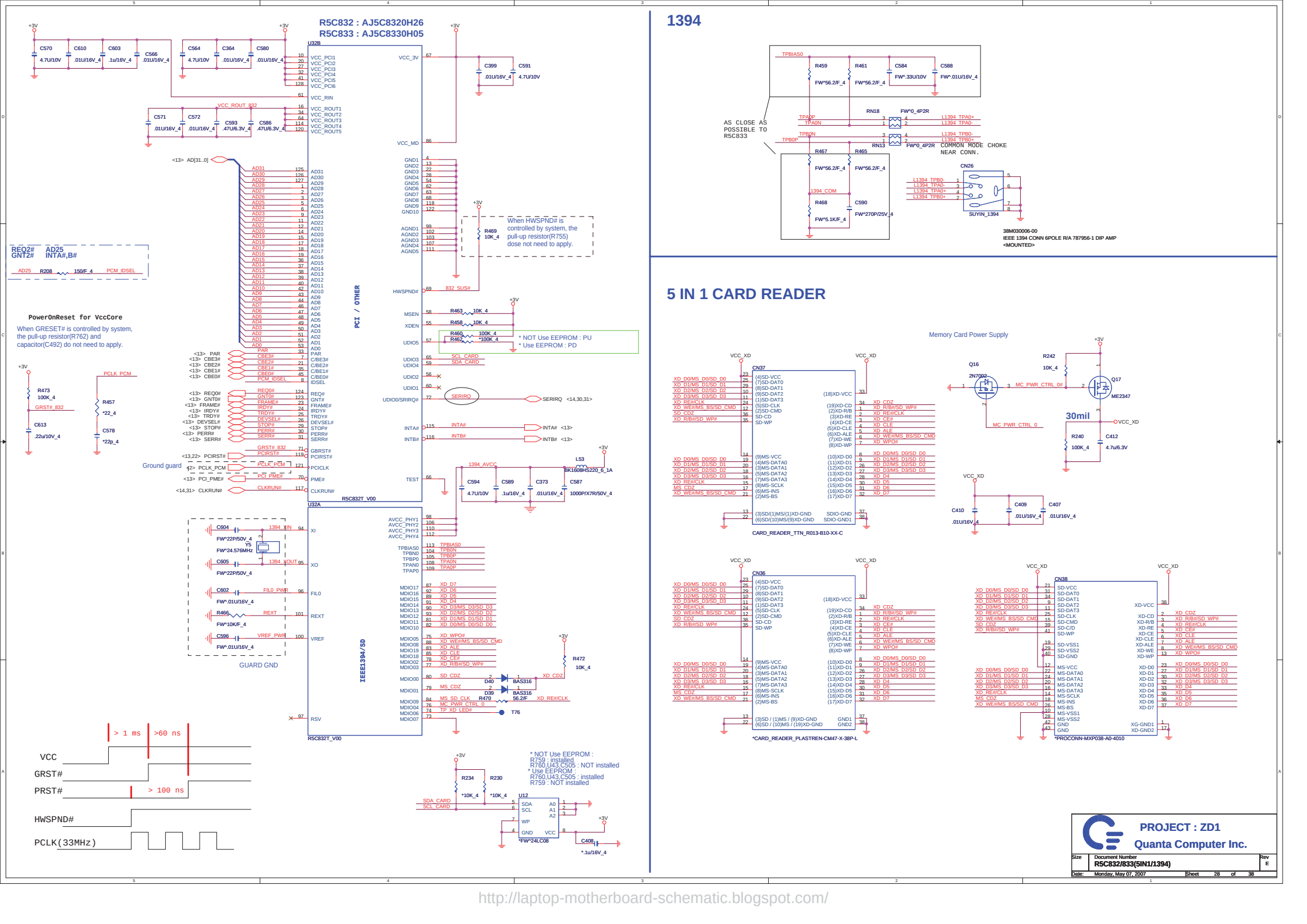



## MIC



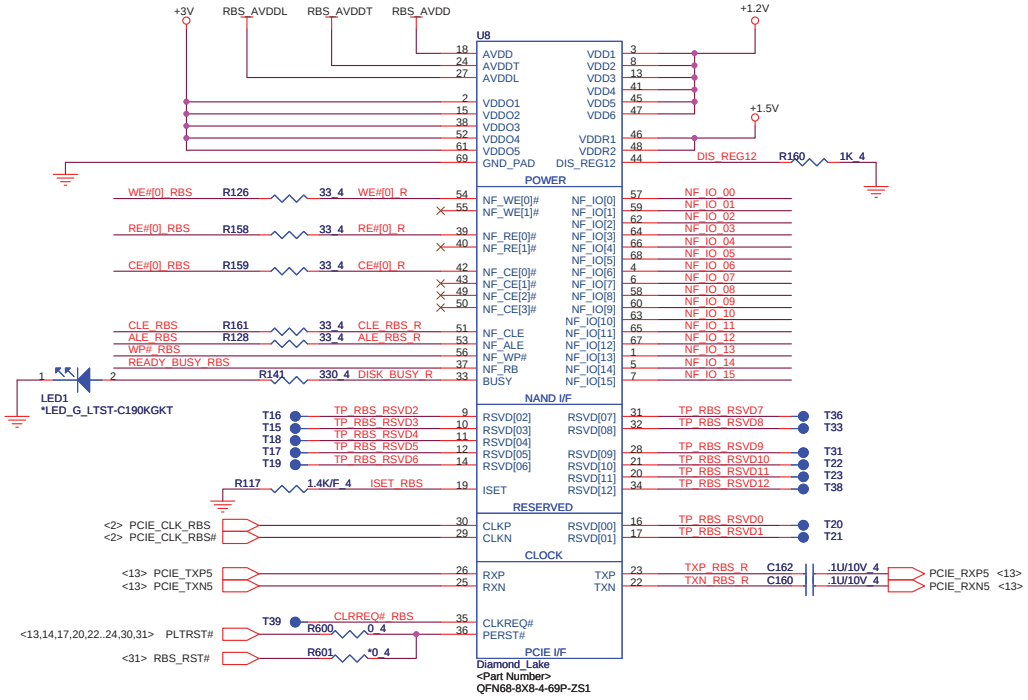

PROJECT : ZD1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | AMP /AUDIO JACK CONN | E |
| Date: Monday, May 07, 2007 | Sheet 27 of 38 | |

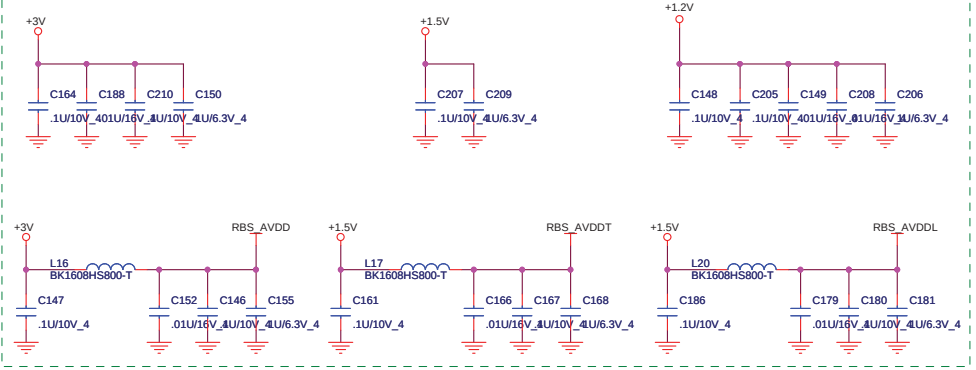


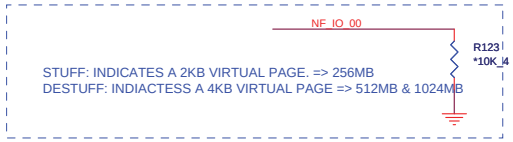
# ROBSON

## DIAMOND-LAKE ASIC




PLACE AS CLOSE AS POSSIBLE TO DIAMOND-LAKE ASIC.

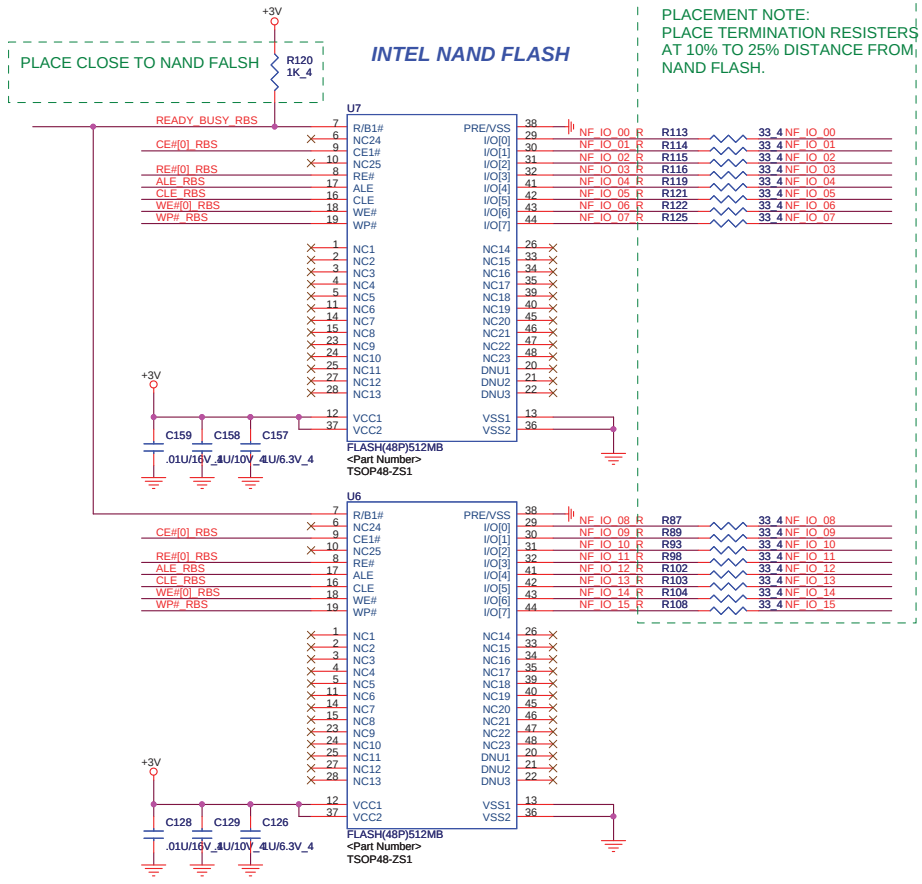



PLACE CLOSE TO NAND FALSH

## INTEL NAND FLASH

PLACEMENT NOTE:
PLACE TERMINATION RESISTERS AT 10% TO 25% DISTANCE FROM NAND FLASH.

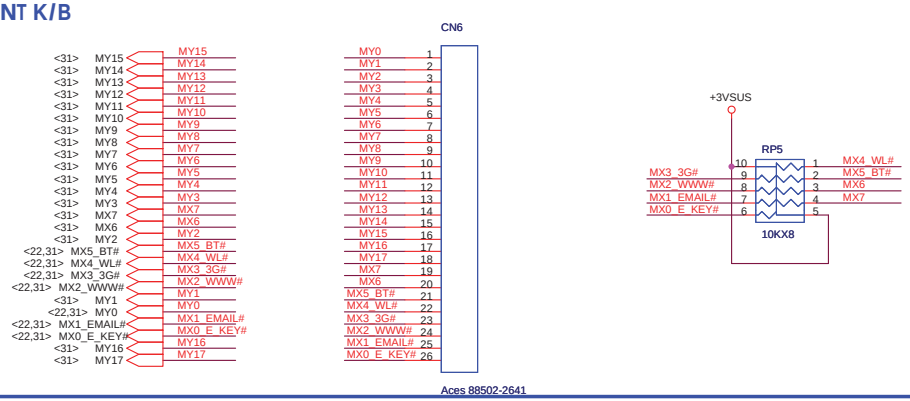



LAYOUT NOTE:
ANY VIA ADDED BENEATH THE NAND FLASH NEEDS TO HAVE A SOLDERMASK ON IT.

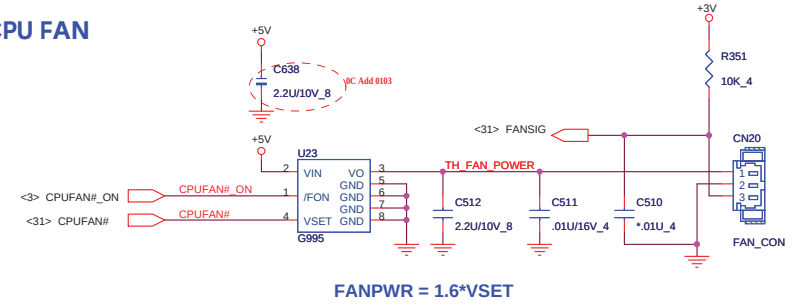
PROJECT : ZD1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | ROBSON | E |
| Date: Monday, May 07, 2007 | Sheet 29 of 38 | |

## INT K/B

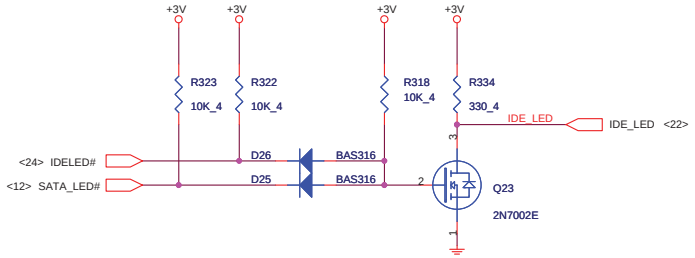


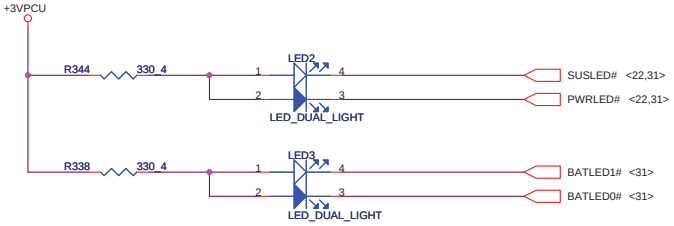

## CPU FAN

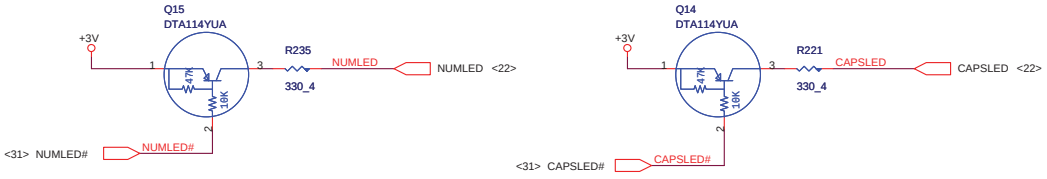



FANPWR = 1.6*VSET

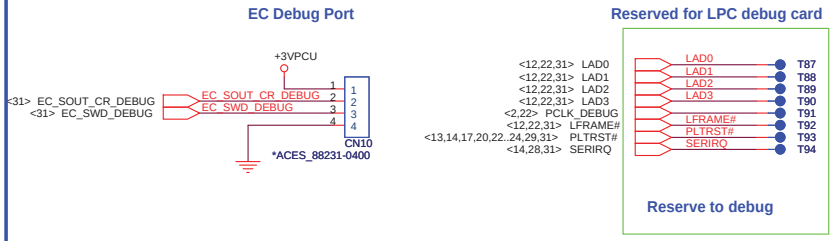
## LED



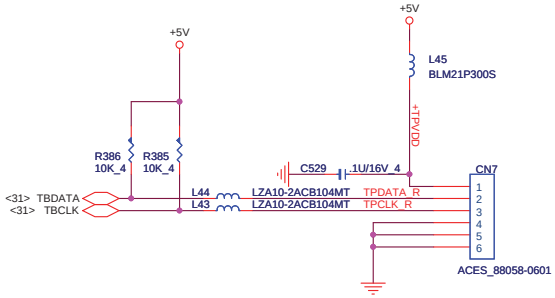



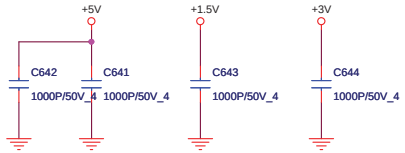

## DEBUG PORT




## T/P

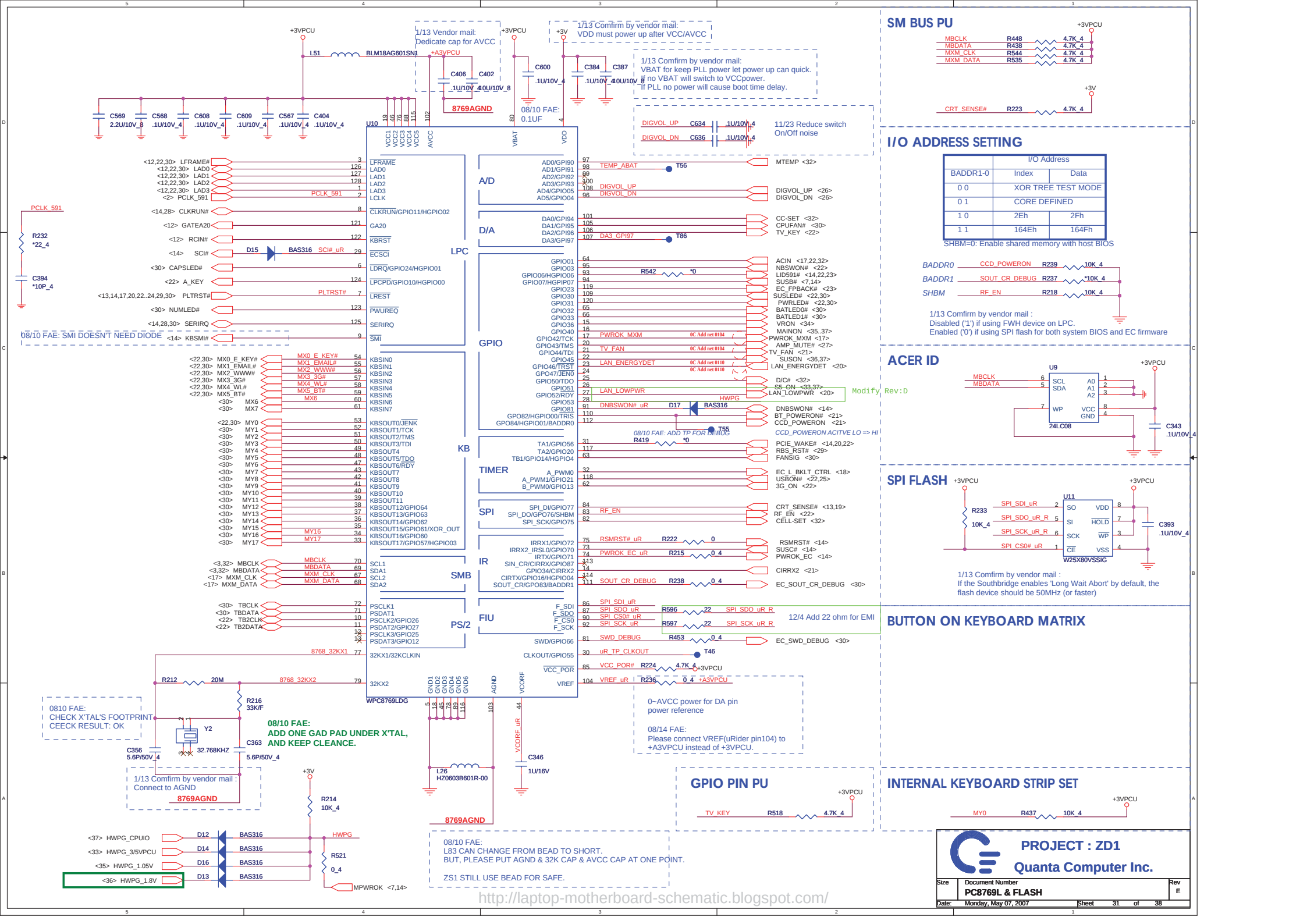


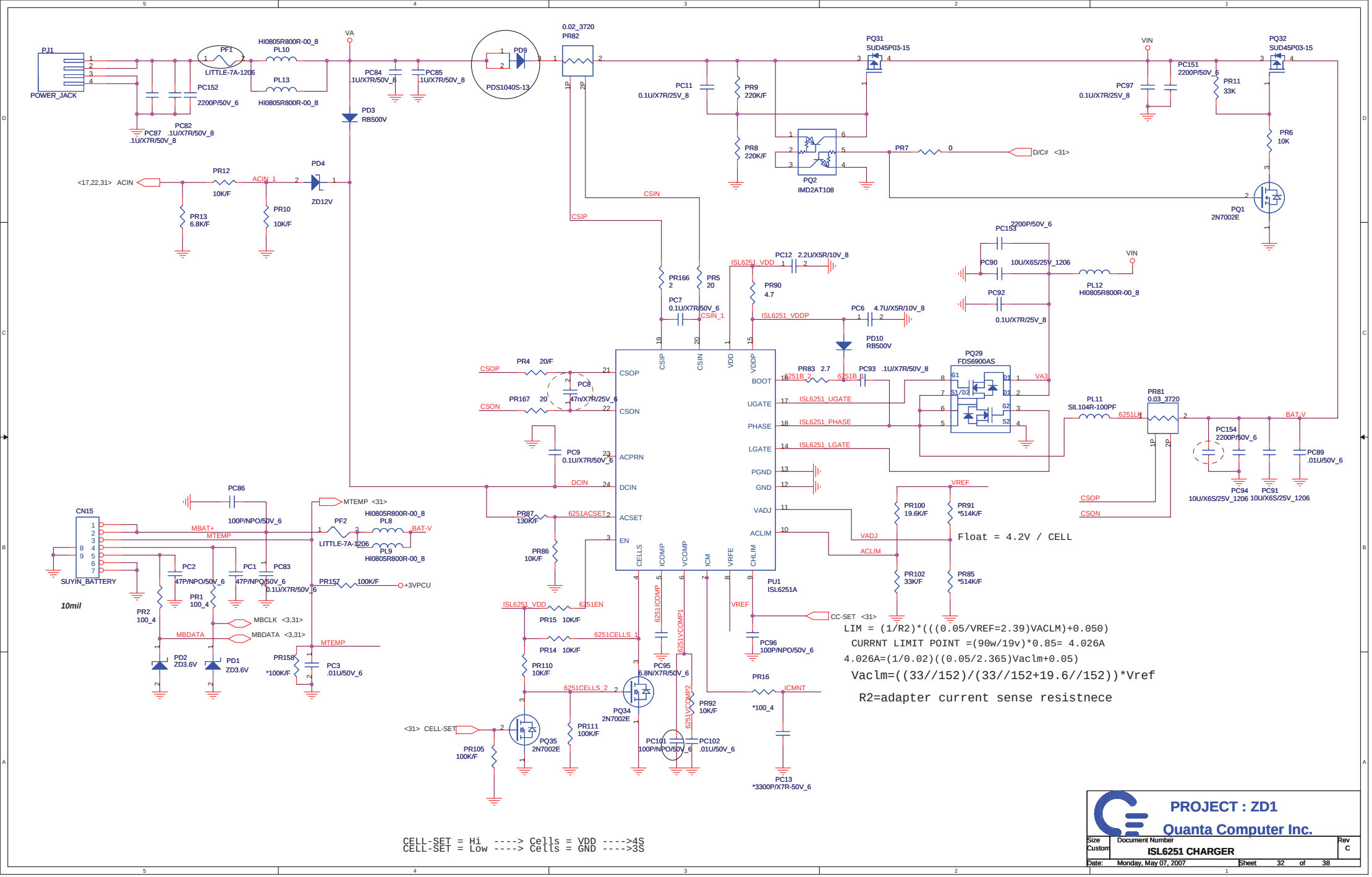

## EMI solution

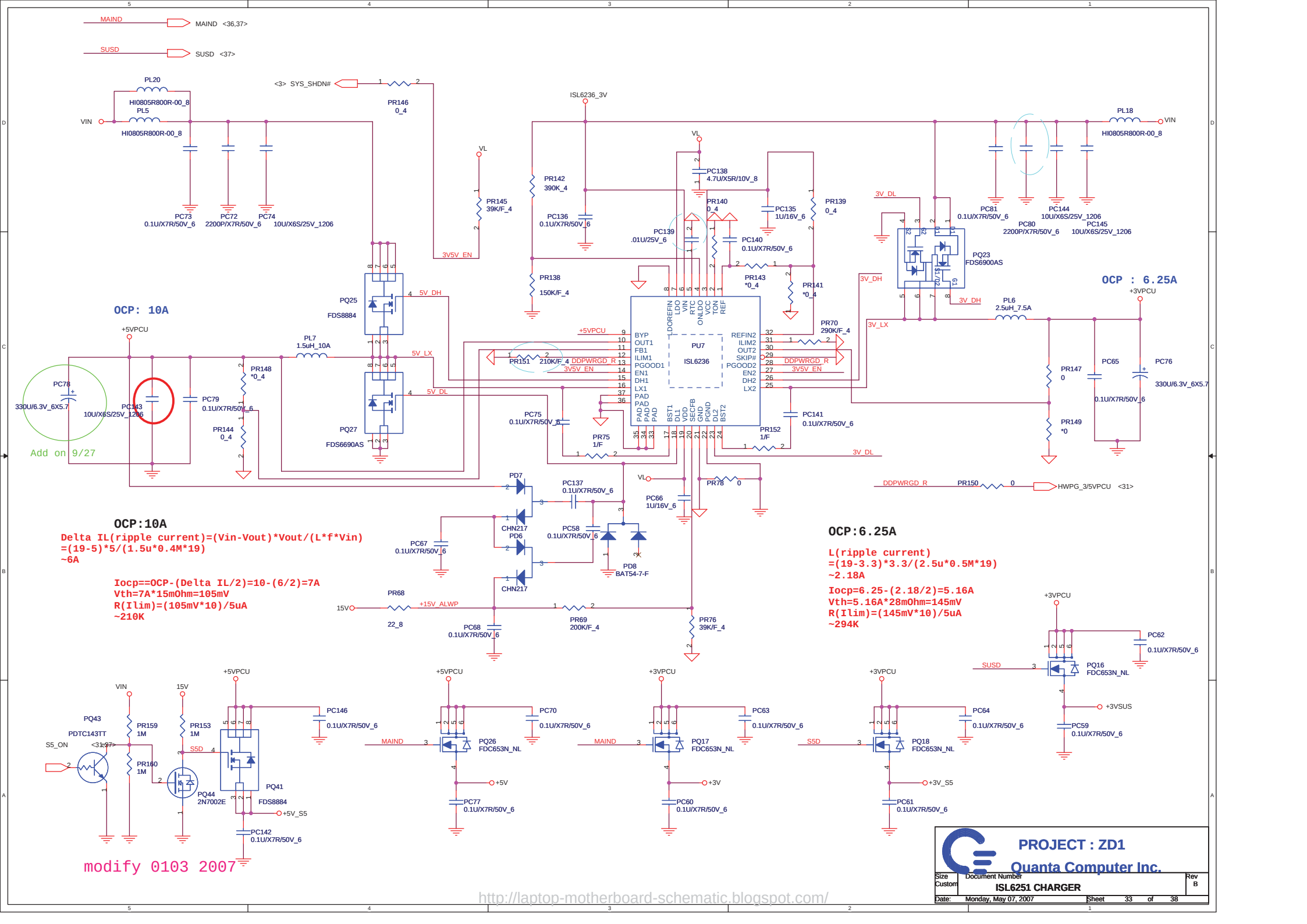


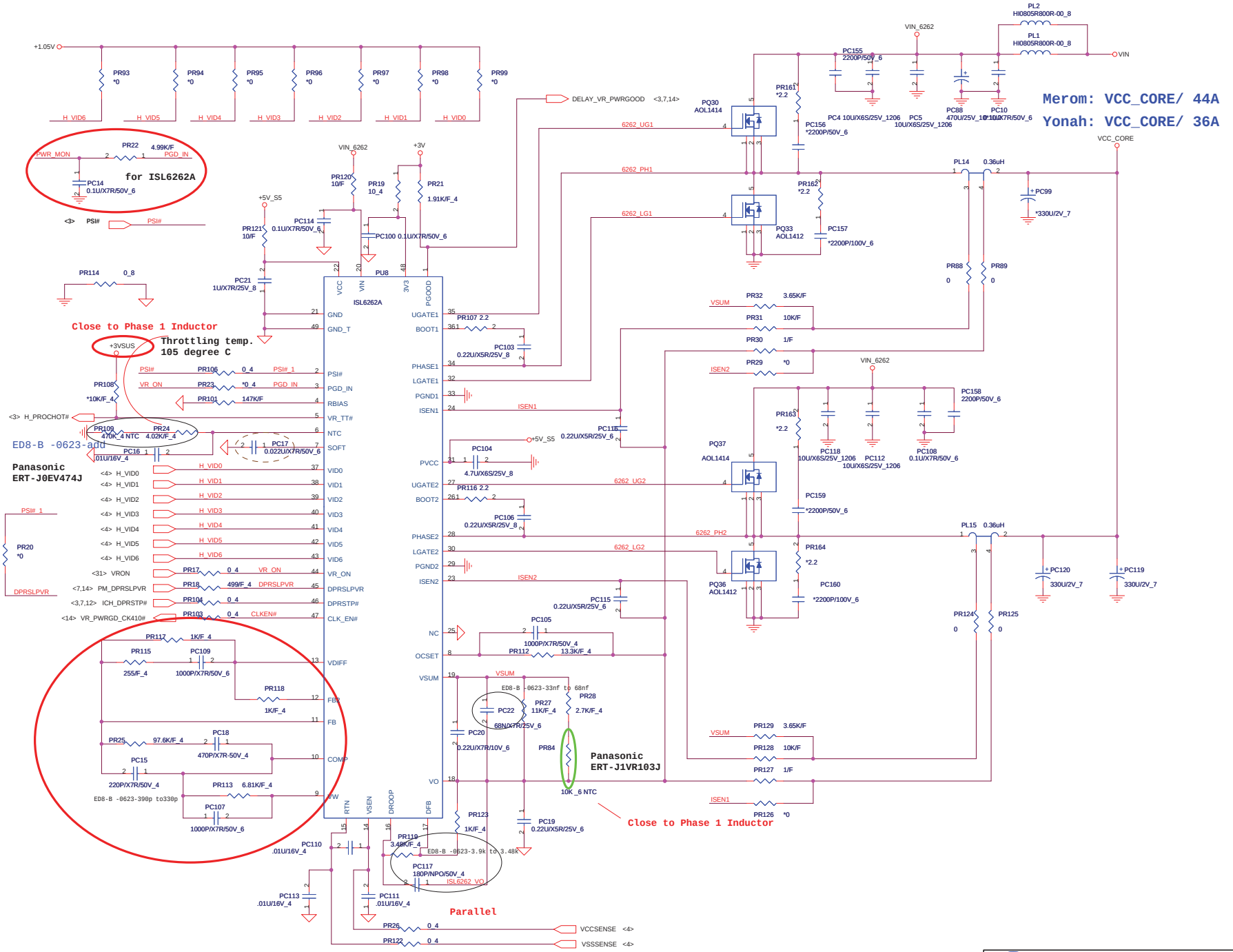

PROJECT : ZD1
Quanta Computer Inc.

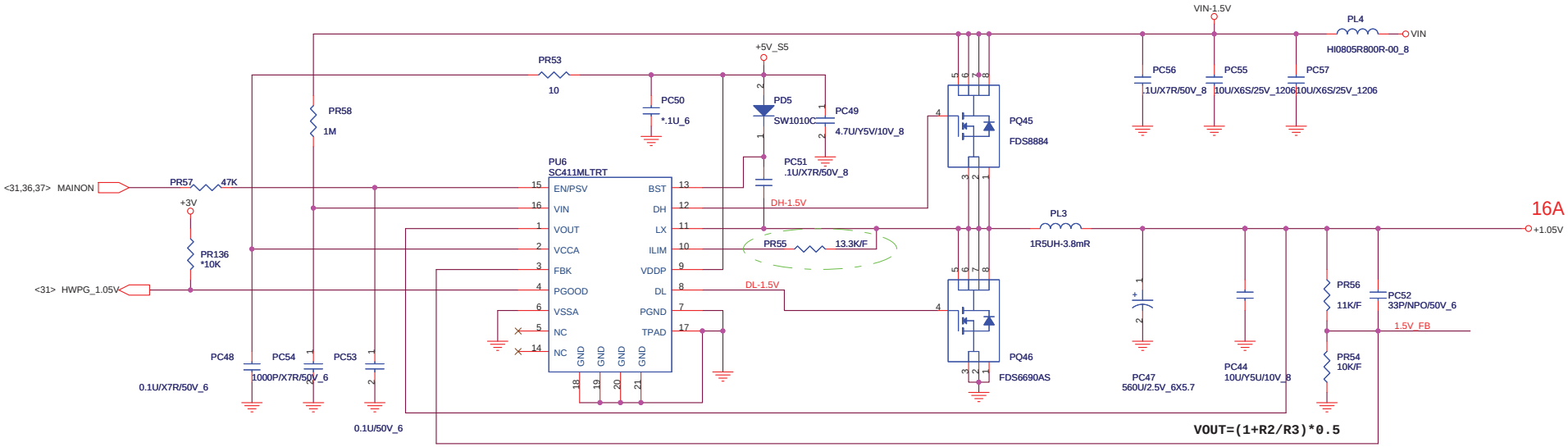
| Size | Document Number | Rev |
|---|---|---|
| | FAN,LED,KB,DEBUG PORT,TP | E |
| Date: Monday, May 07, 2007 | Sheet 30 of 38 | |


SM BUS PU
MBCLK R448 4.7K_4
MBDATA R438 4.7K_4
MXM_CLK R544 4.7K_4
MXM_DATA R535 4.7K_4
CRT_SENSE# R223 4.7K_4
I/O ADDRESS SETTING
I/O Address
BADDR1-0 Index Data
0 0 XOR TREE TEST MODE
0 1 CORE DEFINED
1 0 2Eh 2Fh
1 1 164Eh 164Fh
SHBM=0: Enable shared memory with host BIOS
BADDR0 CCD_POWERON R239 10K_4
BADDR1 SOUT_CR_DEBUG R237 *10K_4
SHBM RF_EN R218 10K_4
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
ACER ID
U9
MBCLK
MBDATA
SCL
SDA
WP
A0
A1
A2
VCC
GND
24LC08
C343 .1U/10V_4
SPI FLASH
U11
SPI_SDI_uR
SPI_SDO_uR_R
SPI_SCK_uR_R
SPI_CS0#_uR
SO
SI
SCK
CE
VDD
HOLD
WP
VSS
W25X80VSSIG
R233 10K_4
C393 .1U/10V_4
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)
BUTTON ON KEYBOARD MATRIX
INTERNAL KEYBOARD STRIP SET
MY0 R437 10K_4
GPIO PIN PU
TV_KEY R518 4.7K_4
1/13 Vendor mail:
Dedicate cap for AVCC
1/13 Comfirm by vendor mail:
VDD must power up after VCC/AVCC
1/13 Comfirm by vendor mail:
VBAT for keep PLL power let power up can quick.
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.
08/10 FAE:
0.1UF
11/23 Reduce switch
On/Off noise
08/10 FAE: SMI DOESN'T NEED DIODE
08/10 FAE: ADD TP FOR DEBUG
CCD_POWERON ACITVE LO => HI
Modify Rev:D
12/4 Add 22 ohm for EMI
0~AVCC power for DA pin
power reference
08/14 FAE:
Please connect VREF(uRider pin104) to
+A3VPCU instead of +3VPCU.
0810 FAE:
CHECK X'TAL'S FOOTPRINT
CEECK RESULT: OK
08/10 FAE:
ADD ONE GAD PAD UNDER X'TAL,
AND KEEP CLEANCE.
1/13 Comfirm by vendor mail :
Connect to AGND
8769AGND
08/10 FAE:
L83 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.
WPC8769LDG
LPC
A/D
D/A
GPIO
KB
TIMER
SPI
IR
SMB
PS/2
FIU
PROJECT : ZD1
Quanta Computer Inc.
PC8769L & FLASH
Rev E
Monday, May 07, 2007
Sheet 31 of 38
http://laptop-motherboard-schematic.blogspot.com/




MAIND
MAIND <36,37>
SUSD
SUSD <37>
<3> SYS_SHDN#
PL20
HI0805R800R-00_8
PL5
HI0805R800R-00_8
VIN
PC73 0.1U/X7R/50V_6
PC72 2200P/X7R/50V_6
PC74 10U/X6S/25V_1206
PR146 0_4
ISL6236_3V
VL
PR145 39K/F_4
3V5V_EN
PR142 390K_4
PC136 0.1U/X7R/50V_6
PR138 150K/F_4
PC138 4.7U/X5R/10V_8
PR140 0_4
PC135 1U/16V_6
PR139 0_4
PC139 .01U/25V_6
PC140 0.1U/X7R/50V_6
PR143 *0_4
PR141 *0_4
PL18
HI0805R800R-00_8
PC81 0.1U/X7R/50V_6
PC80 2200P/X7R/50V_6
PC144 10U/X6S/25V_1206
PC145 10U/X6S/25V_1206
3V_DL
PQ23 FDS6900AS
3V_DH
3V_LX
PL6 2.5uH_7.5A
+3VPCU
OCP : 6.25A
OCP: 10A
+5VPCU
PL7 1.5uH_10A
PQ25 FDS8884
5V_DH
5V_LX
5V_DL
PQ27 FDS6690AS
PR148 *0_4
PR144 0_4
PC78 330U/6.3V_6X5.7
PC143 10U/X6S/25V_1206
PC79 0.1U/X7R/50V_6
Add on 9/27
PU7 ISL6236
LDOREFIN LDO VIN RTC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DLL VDD SGND SGFB PGND DL2 BST2
+5VPCU
PR151 210K/F_4
DDPWRGD_R
3V5V_EN
PR70 290K/F_4
PC75 0.1U/X7R/50V_6
PR75 1/F
PC141 0.1U/X7R/50V_6
PR152 1/F
PR147 0
PR149 *0
PC65
PC76 330U/6.3V_6X5.7
0.1U/X7R/50V_6
PD7
CHN217
PD6
CHN217
PC137 0.1U/X7R/50V_6
PC58 0.1U/X7R/50V_6
PD8 BAT54-7-F
PC67 0.1U/X7R/50V_6
PC66 1U/16V_6
PR78 0
DDPWRGD_R
PR150 0
HWPG_3/5VPCU <31>
OCP:10A
Delta IL(ripple current)=(Vin-Vout)*Vout/(L*f*Vin)
=(19-5)*5/(1.5u*0.4M*19)
~6A
Iocp==OCP-(Delta IL/2)=10-(6/2)=7A
Vth=7A*15mOhm=105mV
R(Ilim)=(105mV*10)/5uA
~210K
OCP:6.25A
L(ripple current)
=(19-3.3)*3.3/(2.5u*0.5M*19)
~2.18A
Iocp=6.25-(2.18/2)=5.16A
Vth=5.16A*28mOhm=145mV
R(Ilim)=(145mV*10)/5uA
~294K
PR68
15V
+15V_ALWP
22_8
PC68 0.1U/X7R/50V_6
PR69 200K/F_4
PR76 39K/F_4
+3VPCU
PC62 0.1U/X7R/50V_6
SUSD
PQ16 FDC653N_NL
+3VSUS
PC59 0.1U/X7R/50V_6
VIN
15V
PQ43 PDTC143TT
S5_ON
<31,37>
PR159 1M
PR160 1M
PR153 1M
S5D
PQ44 2N7002E
PQ41 FDS8884
+5V_S5
PC142 0.1U/X7R/50V_6
PC146 0.1U/X7R/50V_6
PQ26 FDC653N_NL
PC70 0.1U/X7R/50V_6
+5V
PC77 0.1U/X7R/50V_6
PQ17 FDC653N_NL
PC63 0.1U/X7R/50V_6
+3V
PC60 0.1U/X7R/50V_6
PQ18 FDC653N_NL
PC64 0.1U/X7R/50V_6
+3V_S5
PC61 0.1U/X7R/50V_6
modify 0103 2007
PROJECT : ZD1
Quanta Computer Inc.
Size Custom
Document Number
ISL6251 CHARGER
Rev B
Date: Monday, May 07, 2007
Sheet 33 of 38
http://laptop-motherboard-schematic.blogspot.com/



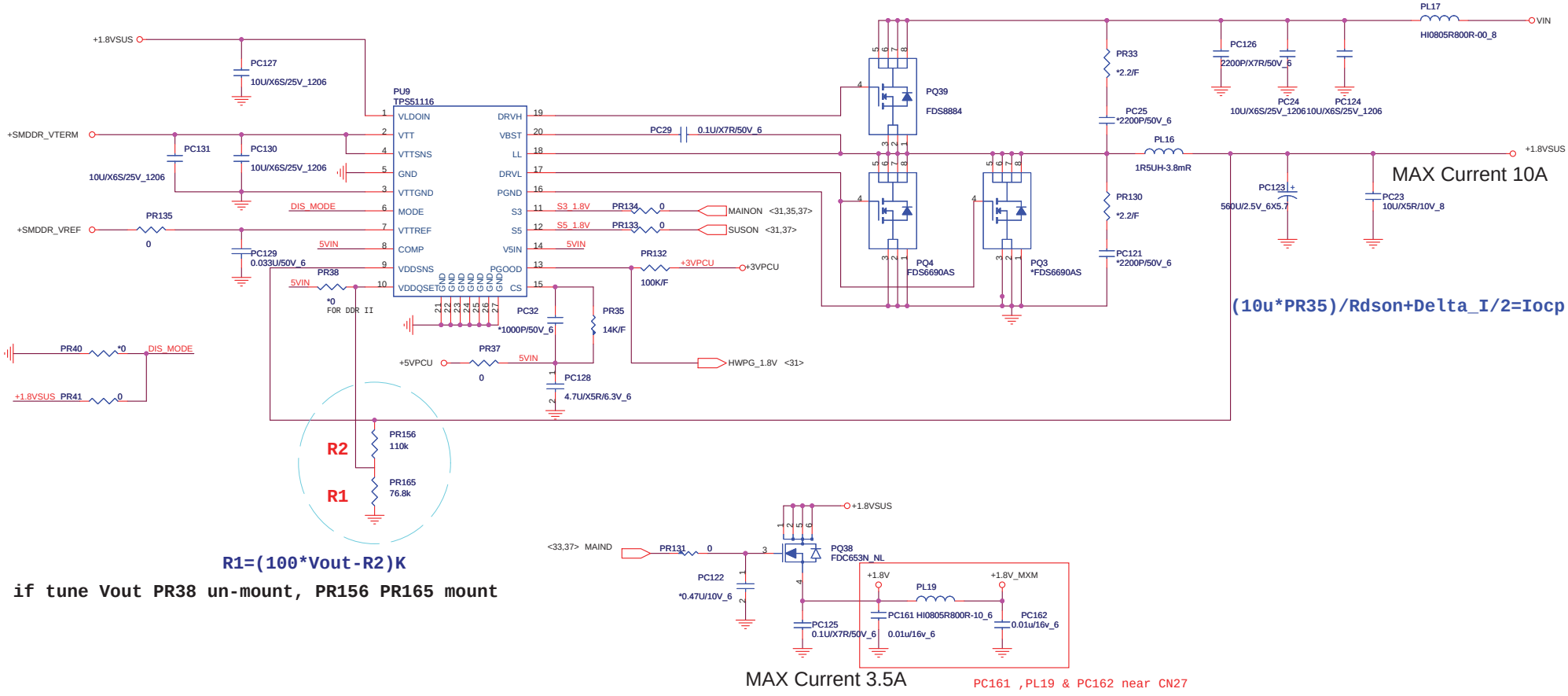



**Rdson*Iocp=PR55*10u  Rdson=15m ohm**

**PROJECT : ZD1**

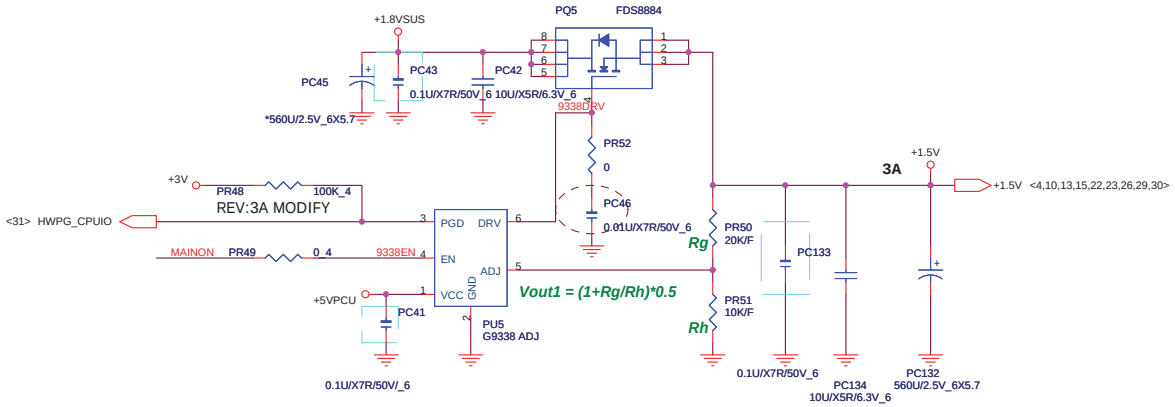
**Quanta Computer Inc.**

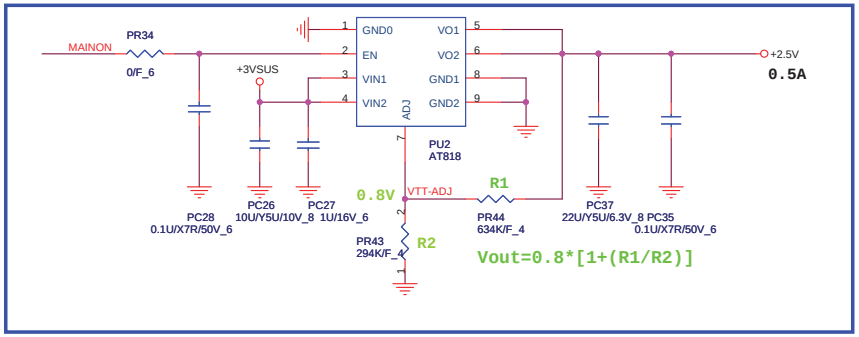
| Size | Document Number | Rev |
|---|---|---|
| | VTT +1.05V | C |
| Date: Monday, May 07, 2007 | Sheet 35 of 38 | |

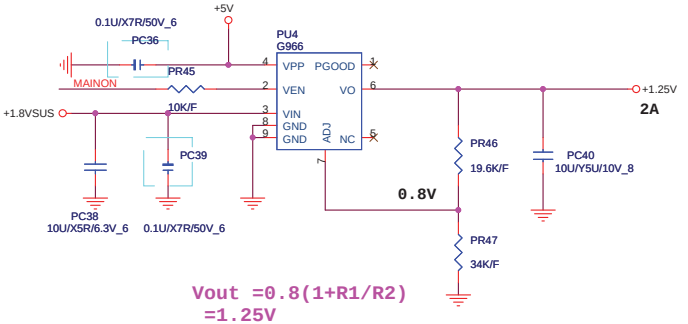


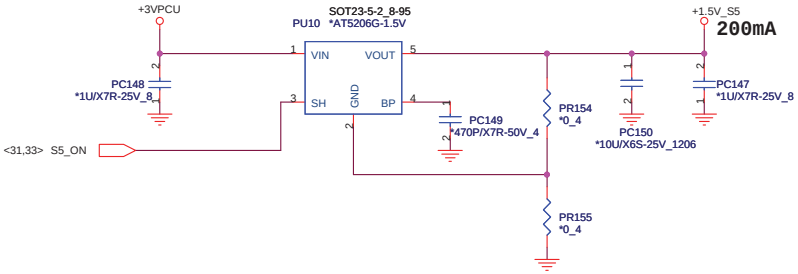


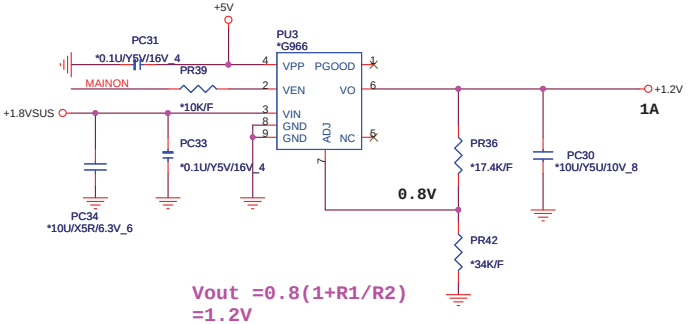

| | | |
|---|---|---|
| PROJECT : ZD1 | | |
| Quanta Computer Inc. | | |
| Size | Document Number: DDR 1.8V(TPS51116) | Rev: B |
| Date: Monday, May 07, 2007 | Sheet 36 of 38 | |

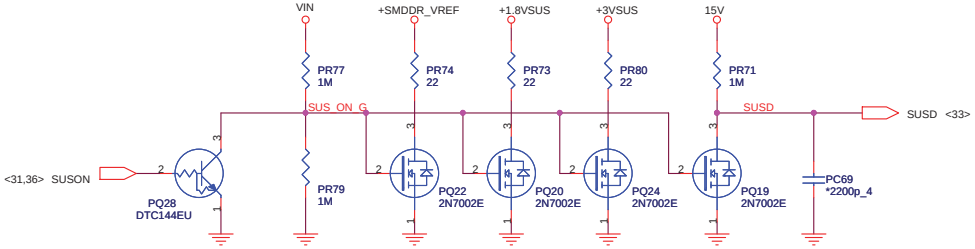


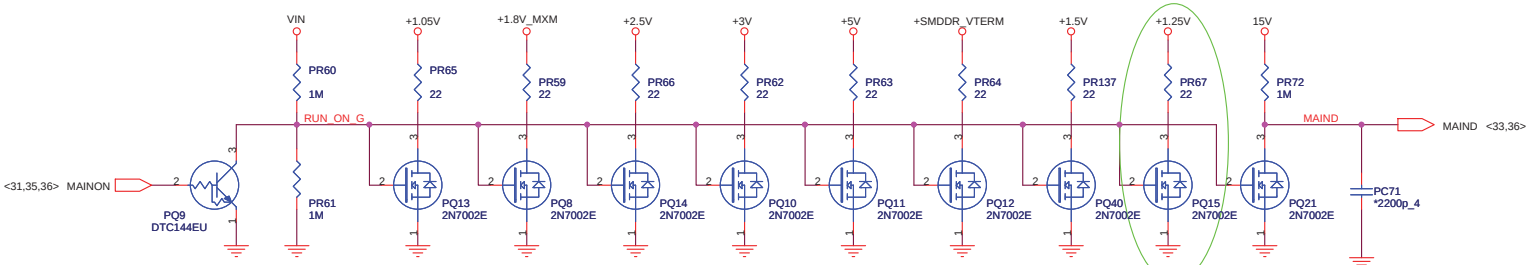




Add by power on 10/19






PROJECT : ZD1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | Discharge (1.5V/2.5V) | C |
| Date: Monday, May 07, 2007 | Sheet 37 of 38 | |

# CHANGE LIST

| Model | REV | |
|---|---|---|
| ZD1 MB | 1A | FIRST RELEASED: E200610-3793 (PCB: DA0ZD1MB6A0) |
| | 2A | Page10 : Depop R153 & pop L23 for system can not boot<br>Page14 : U36 package didn't math footprint, change P/N.<br>Page26 : Remove R275, install R276; remove R4, install R16; Change R245, R247 power source from +1.5V_S5/+1.5V to +3V_S5/+3V , Follow customer request modem change support to +3VSUS.<br>Page22 : MMB(CN8) PIN define error.<br>Page22 : TV card change support to +1.5V.<br>Page18 : Install R5, depop R7,: Follow customer request use EC to control backlight ON/OFF function.<br>Page14 : GPIO10: Reserve PU, 10K +> It is GPO and OD;<br>GPIO14: Reserve PD, 10K => It is GPI as AC present and active high;<br>Page6 : TV_DCONSEL[0:1], UMA =>NC, External VGA tie to GND.<br>Page31 : 2nd FAN change design<br>Page23 : New card power SW (location: U33) change same as ZO1<br>Page31 : add 2 capacity 0.1uF(C634,C636) in DIGVOL_UP / DIGVOL_DN pins<br>Page26 : Co-layout ALC268 and 888S<br>Page28 : SD card can not be detected , U32(ES2) sample will fix this issue.<br>Page28 : MMC card can not be detected , U32(ES2) sample will fix this issue.<br>Page14 : The CLPWROK pin of ICH8 connect with HWPG signal<br>Page22 : change CN7 pin definition for T/P no function.<br>Page24 : change CN8 pin definition MMB no function.<br>Page14 : The signal of KBSMI#_ICH add diode , and it PU to +3V_S5<br>The signal of LID591#_ICH add diode , and it PU to +3V_S5 for ICH8 electric leakage issue.<br>Page26 : Change subwoofer from 4pin to 5pin connector. |
| | 2B | Page 2 : Add C645 for EMI solution<br>Page31 : Follow customer request 2nd FAN is controlled by EC<br>Page19 : Floating CN13.16 & CN13.17 ,CN14.15 & CN14.16 for ESD test<br>Page07 : DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK and DPLL_REF_SSCLK#. To GND<br>Page36 : Add PI filter to reduce the power ripple of +1.8V.<br>Page16 : Modify SMbus address A2 , The signal of B_SA1 need to PU and B_SA0 need to PD<br>Page26 : add 2 capacity 1uF(C639,C640) for subwoofer<br>Page30 : add capacity 2.2uF(C638) |
| | 2C | Page17 : Adding (Q52 & R541 & Q53) extra circuitry to prevent power leakage from system into MXM<br>Page21 : Change power of CIR from +3VPCU and +5VPCU.<br>Page31 : AEC pin24 is multi function pin, when EC power up, pin17 will change to JTAG/TCK function not GPIO. So,need to change from pin24 (GPIO47) to pin27 (GPIO52).<br>Page22: Power/B connector add two LED control signal and change to 16 pin from 14-pin for meet ACER LED spec .<br>Page22: Q35 change to AO3413 form DTA114 for increase LED driving power.<br>Page23: BL_ON pull up resistor from 10kohm to 100Khom(R194 ).+3V pull up will cause power on leakage on BL_ON signal due to our VGA have 10kohm pull low. |
| | 2D | Page19 : Connect CRT of CN13.16 & 17 to GND for ESD<br>Page17 : Add capacity 330uF(C647) & Remove R541<br>Page22 & 25: Combine USB/B (CN17) and TV/B(CN30) connector, Connector change to 16 pin. and +5_S5 from 1pin to 2pin.<br>Page25 : Connect HOLE 28 & 29 to GND for ESD<br>Page32~37 : Update power circuit<br>Page37 : Remove 1.2V circuit<br>Page26 : Add 1000pF and 10pF total 4 PCS Location: C648 , C649, C650, C652 (between +5V_ADOand AGND).<br>Page22 : CN8.8 remove +5V & R540 & connect to +3V (K)<br>Page27 : Modify and ADD. AGND bridge (R337,R284,C459 and C472 = 0 Ohm).<br>Page34 : Remove PR161, PR163, PC156, PC159<br>Page22 : Add D45~D51 for ESD<br>Page28 : Change CN36.37 & 38 ,CN37.37 & 38 ,CN38.42 & 43 from ADOGND and GND. |
| | 3A | Page32 : PD9 Change footprint<br>Page25 : Add EMI Spring<br>Page27 : Add GND & AGND bridge (R546,R540,R408)<br>Page22 : Modify pin define (TV/B(CN30) connector) |
| | F | Page23 & 17 : HDMI circuits modify: Add level-shifter for MXM_HDMI_DDCCLK and MXM_HDMI_DDCDATA.( Location: Q54 ,Q55 , R75, R63, R297, R410 & R602) . |

| MODEL | ZY3 FROM | ZY3 To |
|---|---|---|
| | X | 1A |
| | X | 1A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 1A | 2A |
| | 2A | 2B |
| | 2A | 2B |
| | 2A | 2B |
| | 2A | 2B |
| | 2A | 2B |
| | 2A | 2B |
| | 2A | 2B |
| | 2A | 2B |
| | 2A | 2B |
| | 2B | 3A |
| | 2B | 3A |
| | 2B | 3A |
| | 2B | 3A |
| | 2B | 3A |
| | 2B | 3A |
| | 2B | 3A |

PROJECT : ZD1
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | Change list | 1A |

Date: Monday, May 07, 2007 Sheet 38 of 38

| DOC NO. | PROJECT MODEL : | ZD1 | APPROVED BY: | | DATE: | 2007/ 2/15 |
|---|---|---|---|---|---|---|
| | PART NUMBER: | | DRAWING BY: | | REVISON: | 3A |