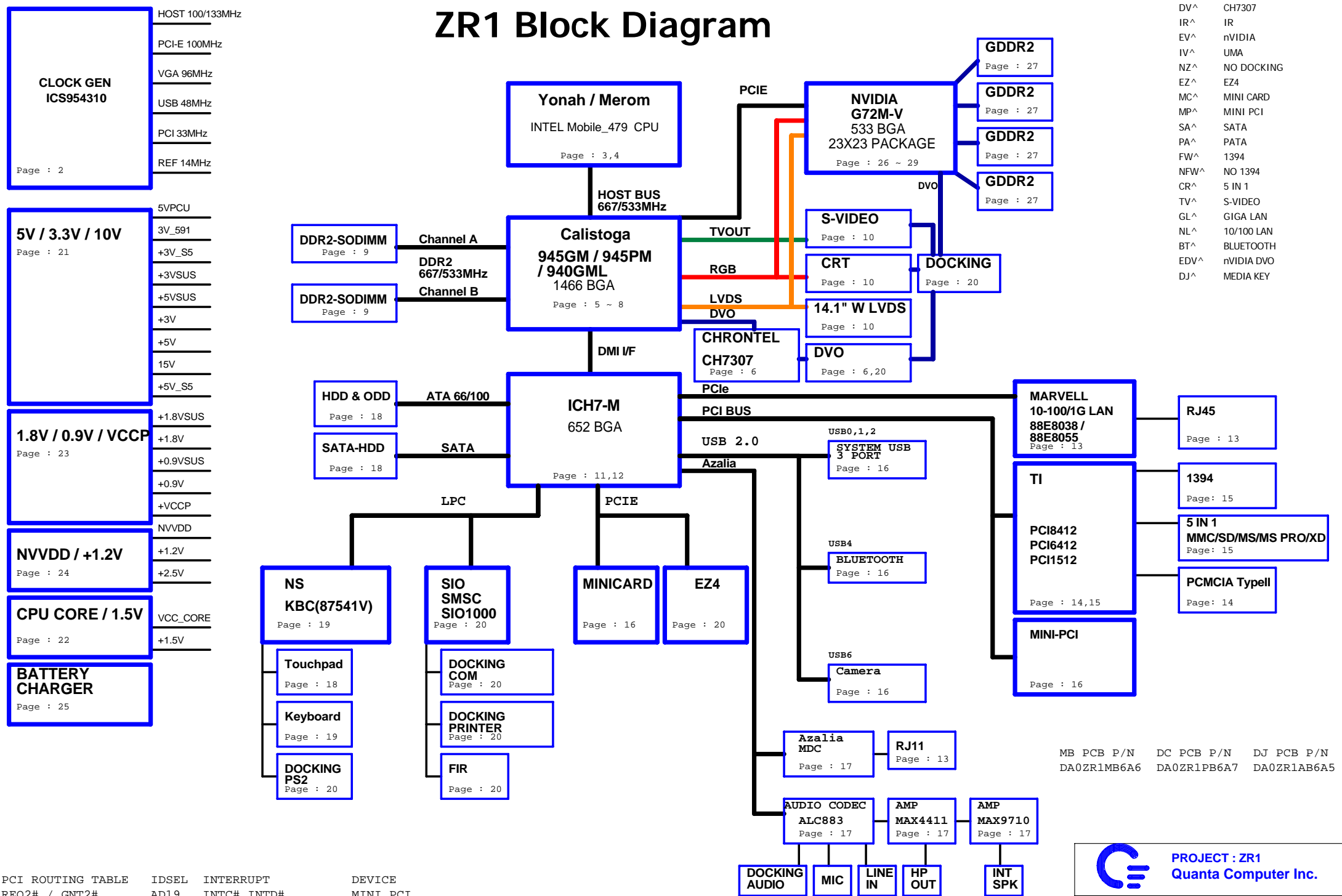



ZR1 Block Diagram



DV^ CH7307
 IR^ IR
 EV^ nVIDIA
 IV^ UMA
 NZ^ NO DOCKING
 EZ^ EZ4
 MC^ MINI CARD
 MP^ MINI PCI
 SA^ SATA
 PA^ PATA
 FW^ 1394
 NFW^ NO 1394
 CR^ 5 IN 1
 TV^ S-VIDEO
 GL^ GIGA LAN
 NL^ 10/100 LAN
 BT^ BLUETOOTH
 EDV^ nVIDIA DVO
 DJ^ MEDIA KEY

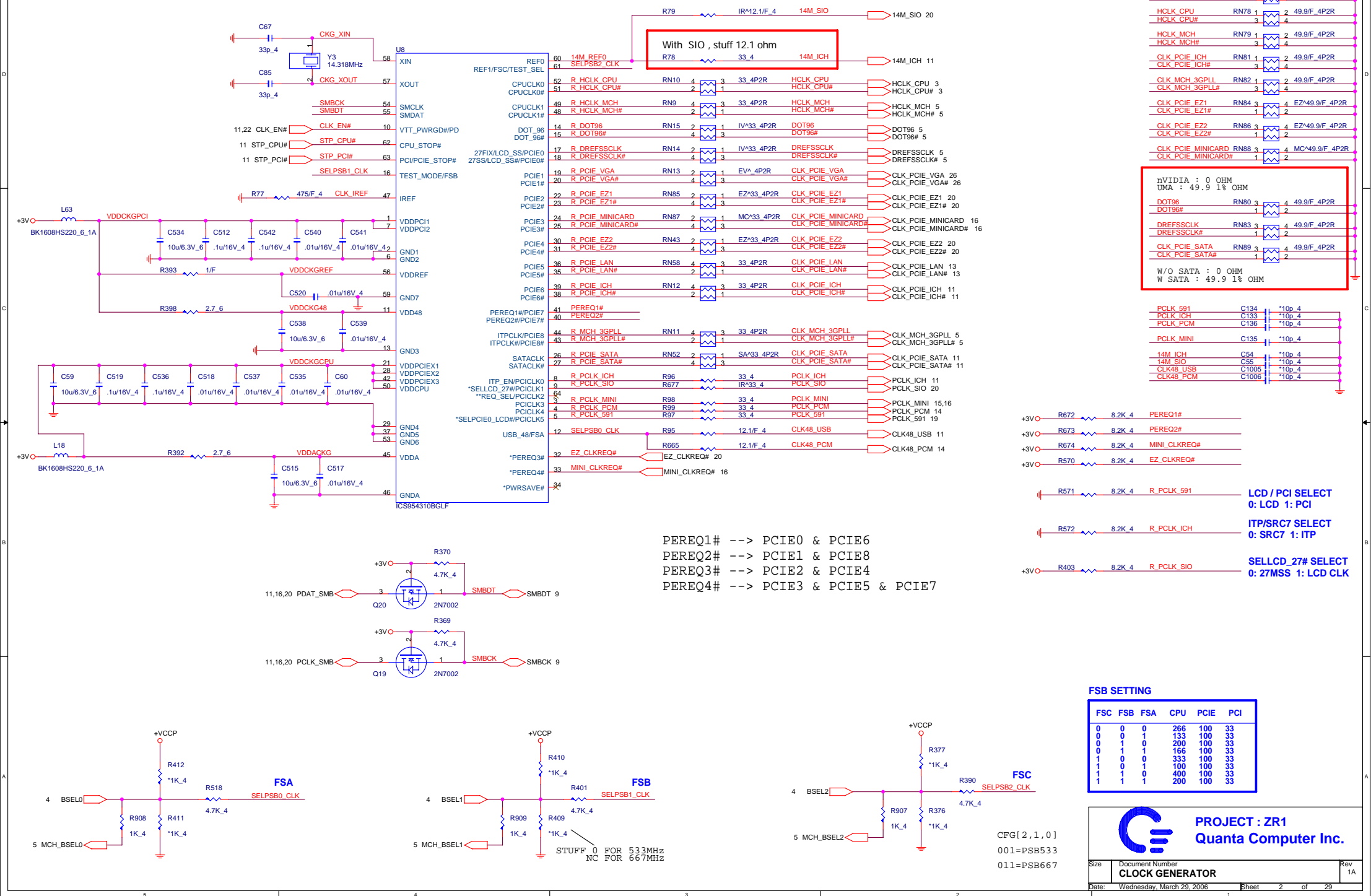
PCI ROUTING TABLE	IDSEL	INTERRUPT	DEVICE
REQ2# / GNT2#	AD19	INTC#,INTD#	MINI PCI
REQ0# / GNT0#	AD25	INTE#,INTF#,INTG#	TI XX12

MB PCB P/N DA0ZR1MB6A6 DC PCB P/N DA0ZR1PB6A7 DJ PCB P/N DA0ZR1AB6A5


PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Wednesday, March 29, 2006	Sheet 1 of 29	

CLOCK GENERATOR



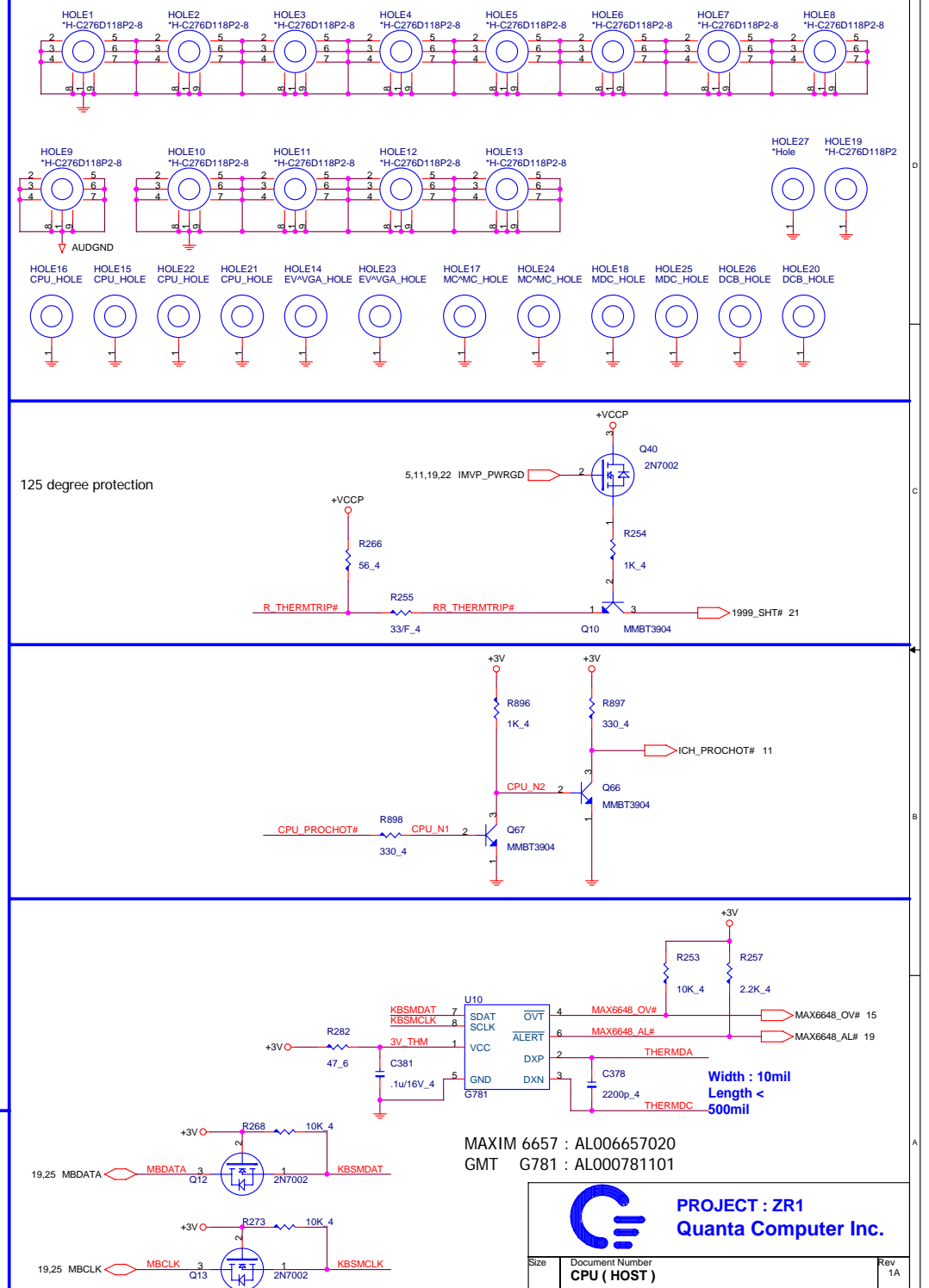
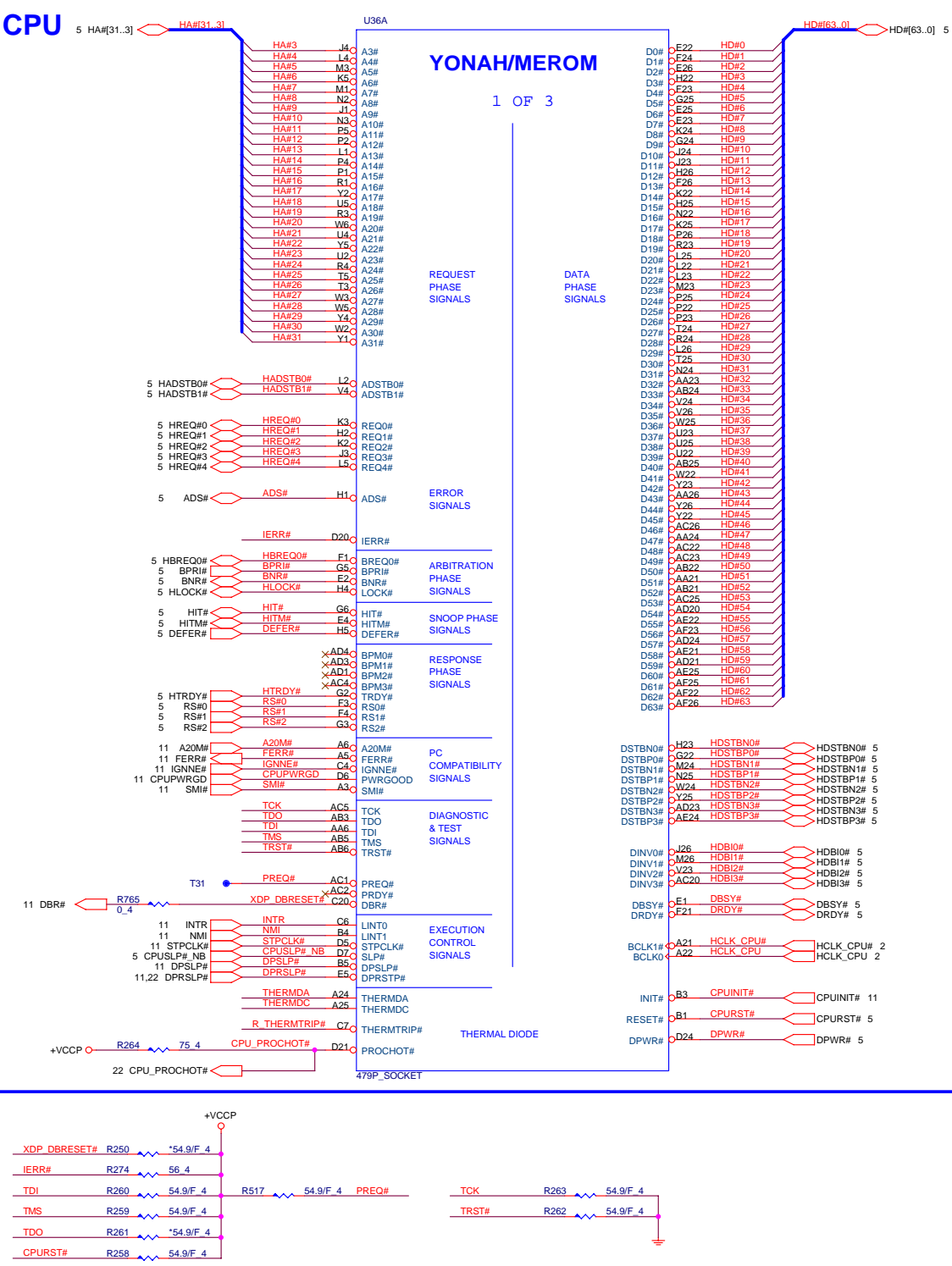
FSB SETTING

	FSC	FSB	FSA	CPU	PCIE	PCI
0	0	0	0	266	100	33
0	0	0	1	133	100	33
0	1	0	0	200	100	33
0	1	1	0	166	100	33
1	0	0	0	333	100	33
1	0	1	0	100	100	33
1	1	0	0	400	100	33
1	1	1	1	200	100	33

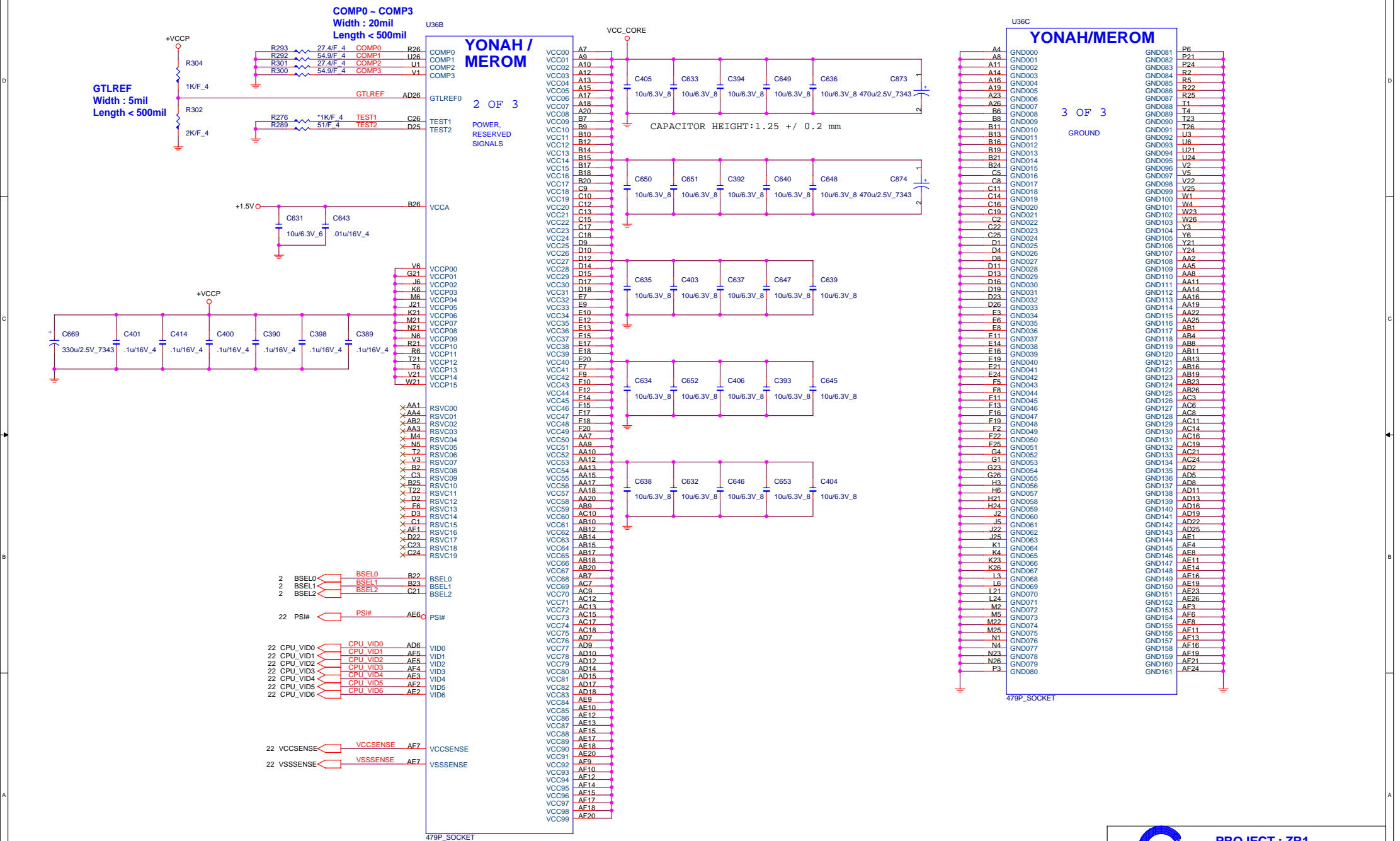



PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number CLOCK GENERATOR	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 2 of 29

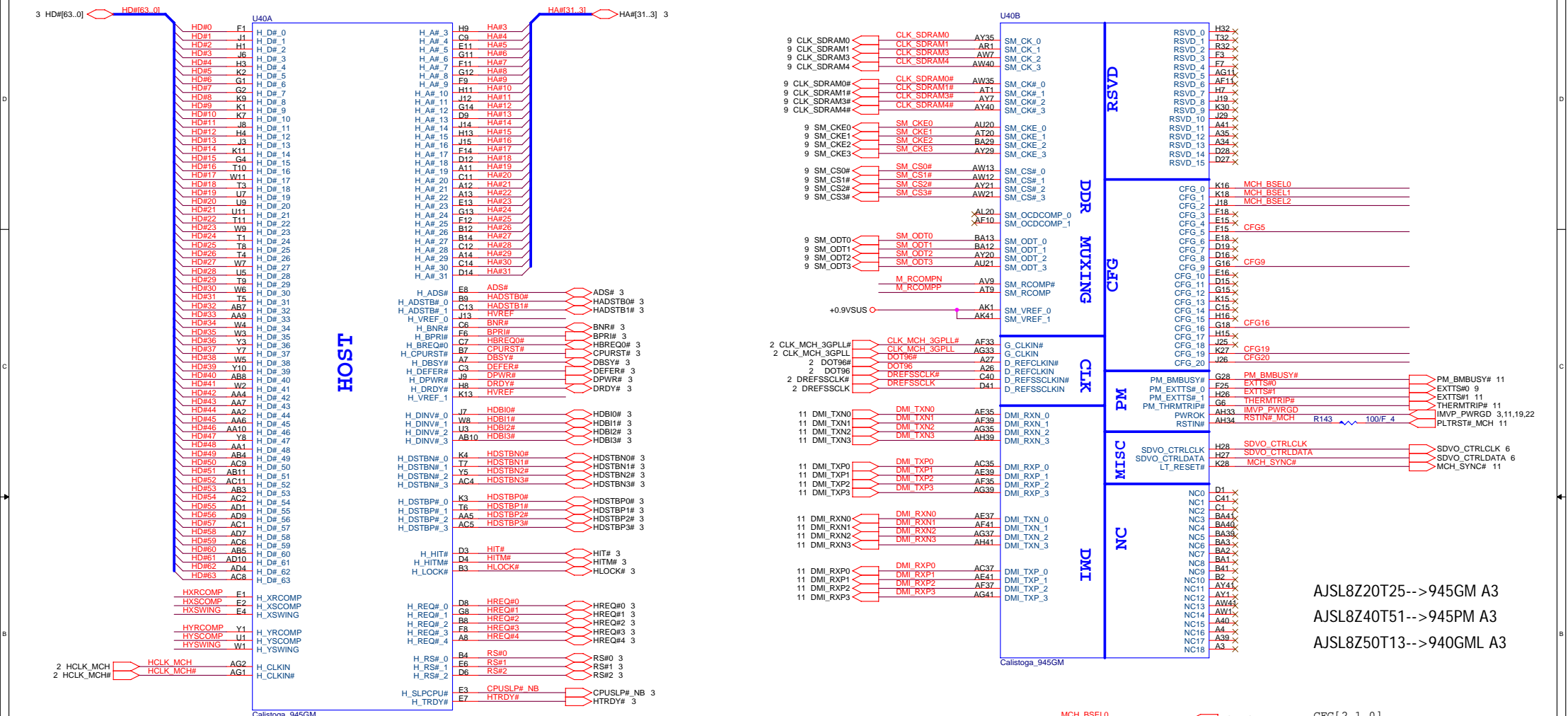


CPU

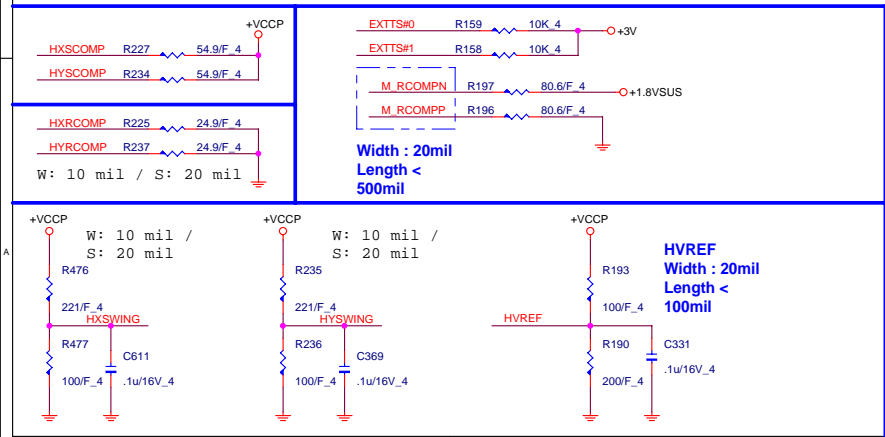


		PROJECT : ZR1 Quanta Computer Inc.	
Size	Document Number	Rev	
	CPU (POWER)	1A	
Date:	Wednesday, March 29, 2006	Sheet	4 of 29

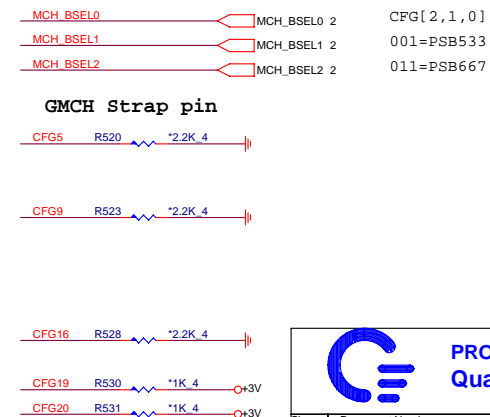
NB_945GM/PM/940GML



AJSL8Z20T25-->945GM A3
AJSL8Z40T51-->945PM A3
AJSL8Z50T13-->940GML A3

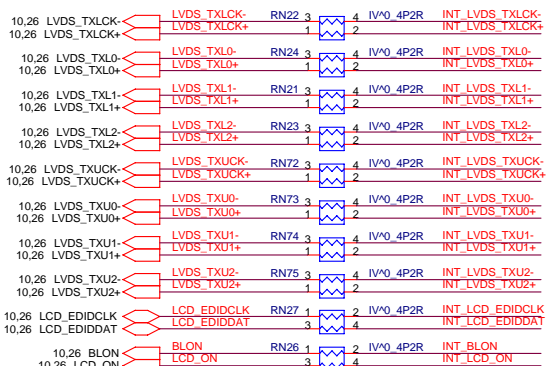
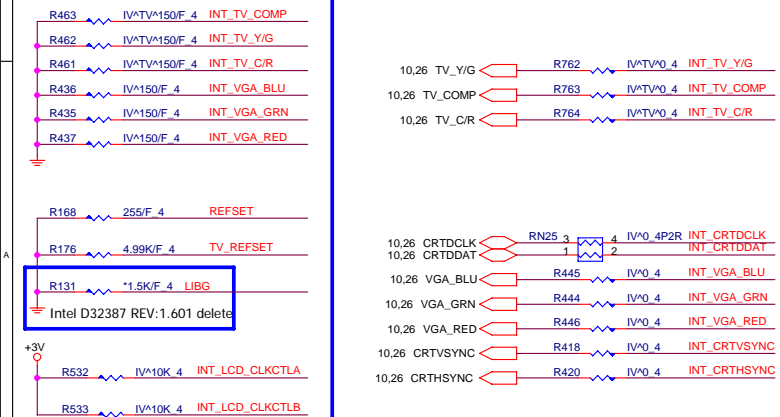
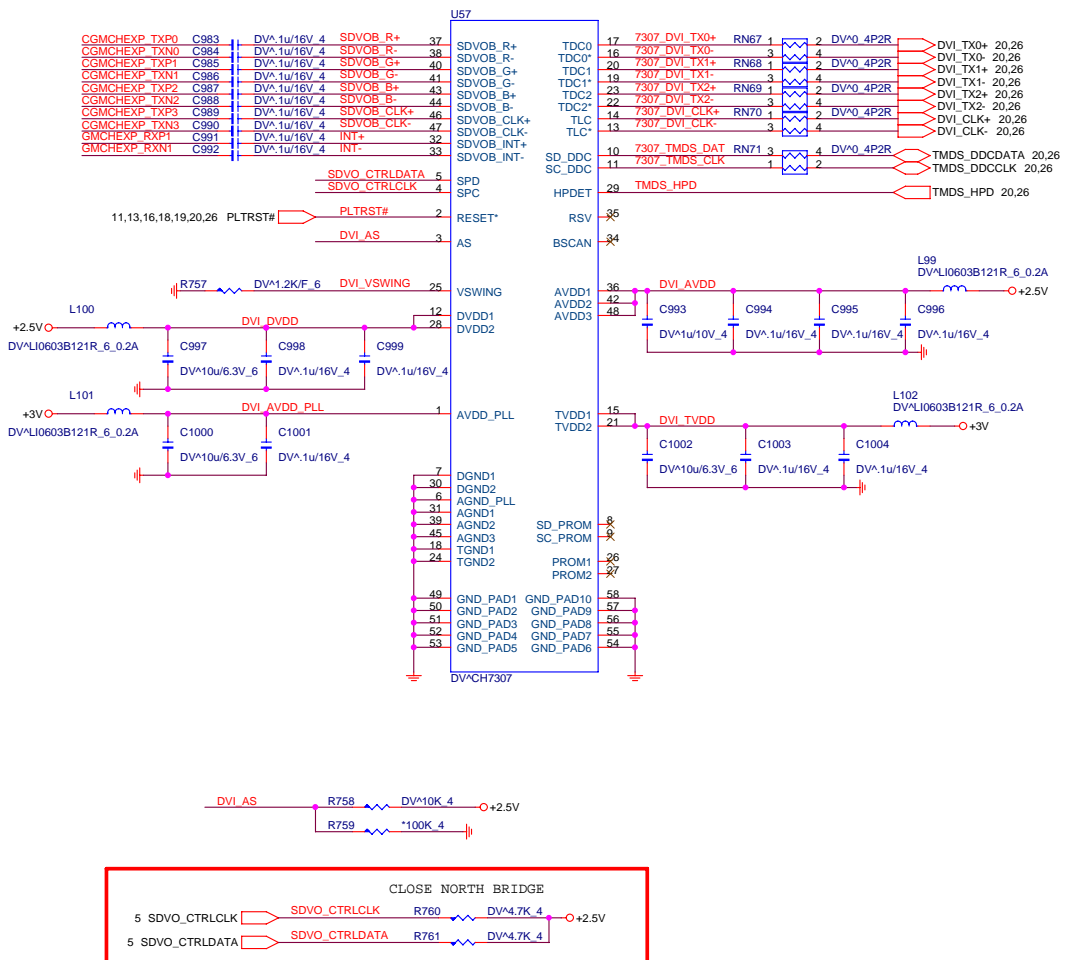
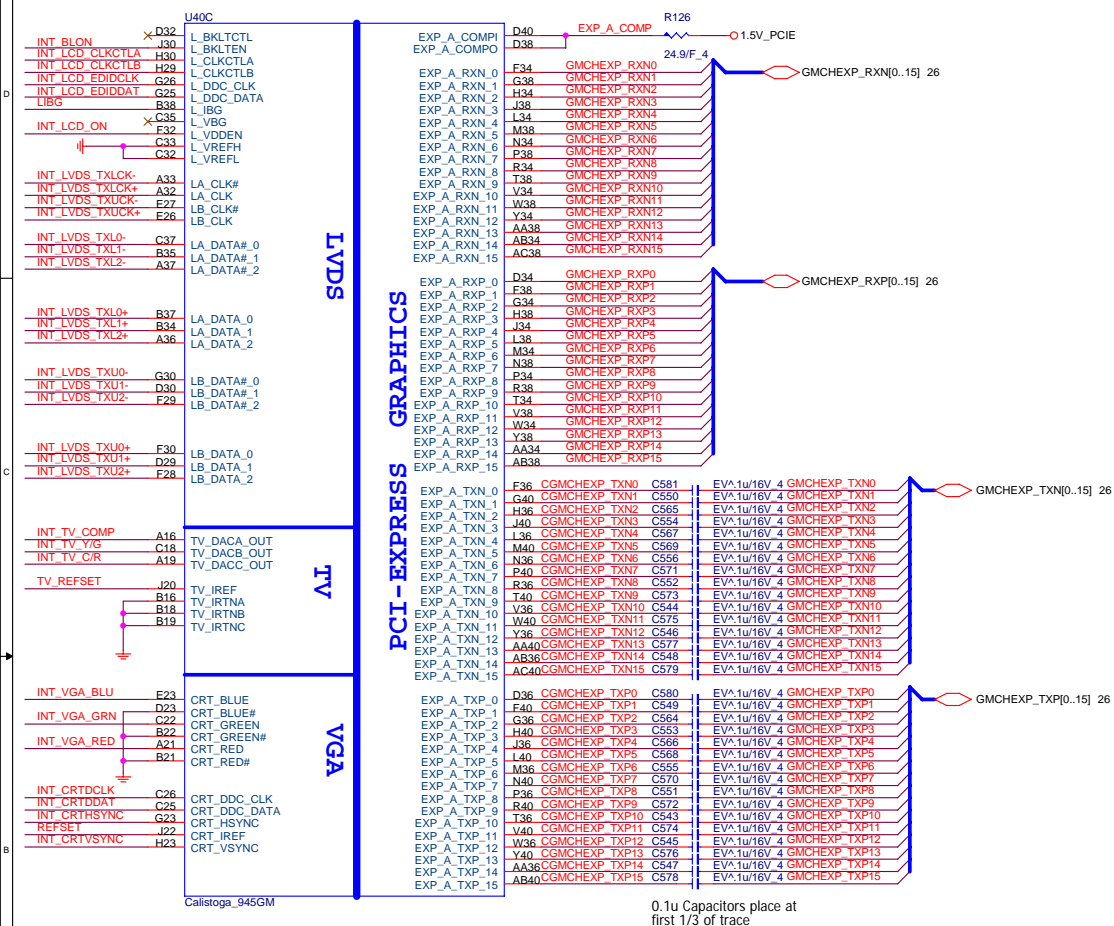


- 1.MCH_CFG_5 : Low = DMI X2, High=DMIX4
- 2.MCH_CFG_6 : Low = Moby Dick, High = Calistoga (Default)
- 3.MCH_CFG_7 : Low = RSVD, High = Mobile CPU
- 4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reverse lane ,High=Normal
- 5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
- 6.MCH_CFG_11: PSB 4x Enable : Low=Rsvd, High=Calistoga.
- 7.MCH_CFG_16 FSB Dymnic ODT: Low = Dynamic ODT Disabled,
High= Dynamic ODT Enabled.
- 8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
- 9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
- 10.MCH_CFG_20 PCIE Backward interoperability mode: Low=
only SDVO or PCIE x1 is operational (defaults) ,
High=SDVO and PCIE x1 are operation
simultaneously via the PEG port.

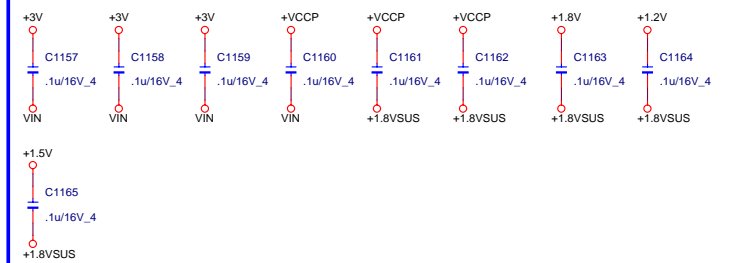


PROJECT : ZR1
Quanta Computer Inc.

DVO_CH7307



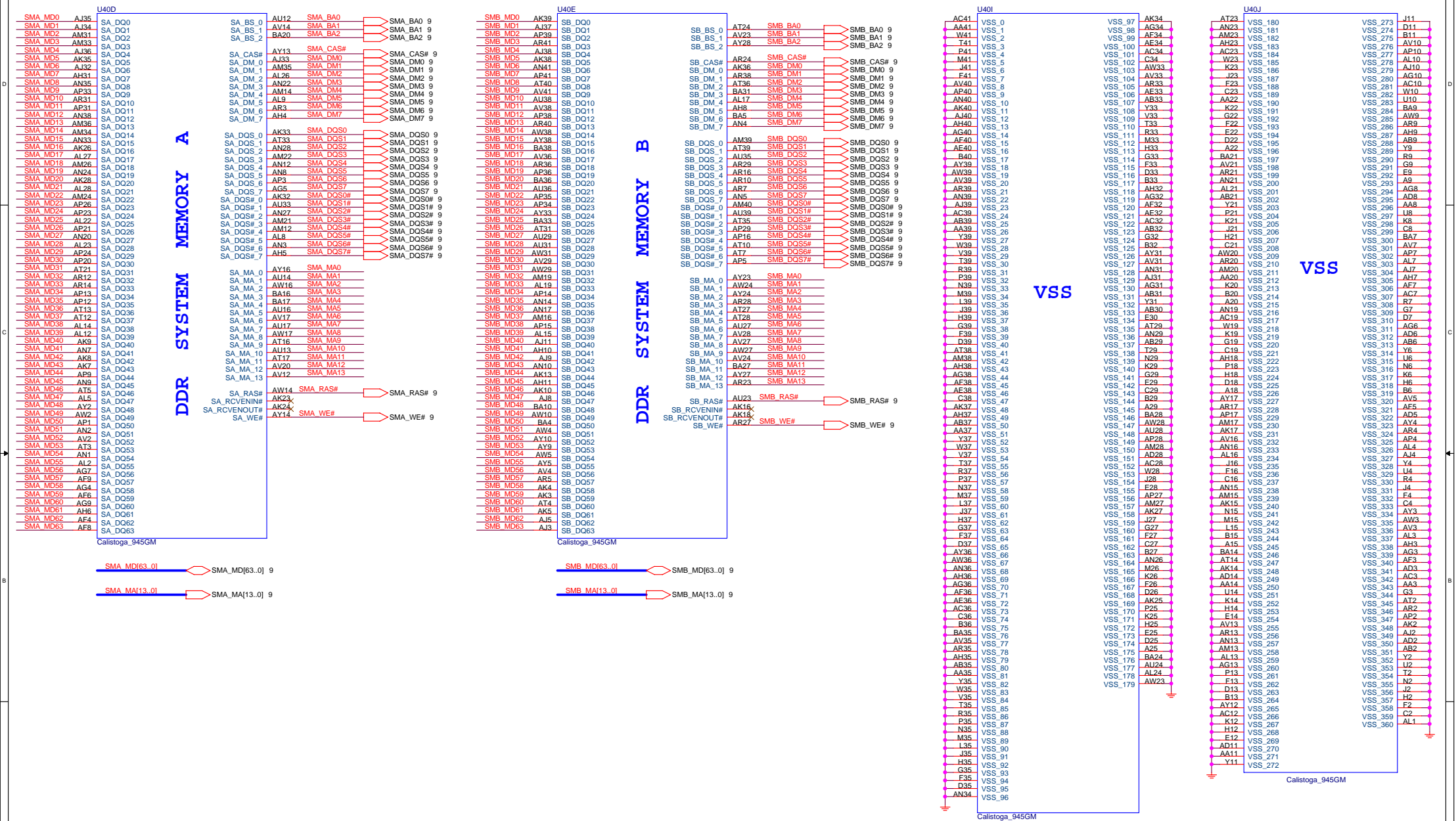
Signal Cross Moat



PROJECT : ZR1
Quanta Computer Inc.

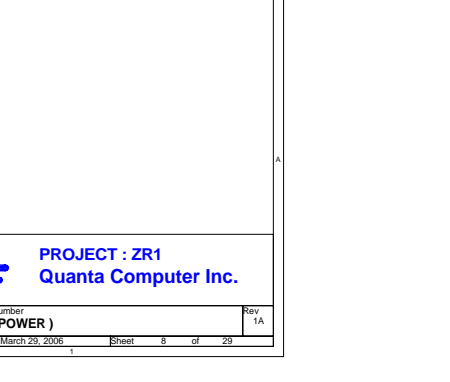
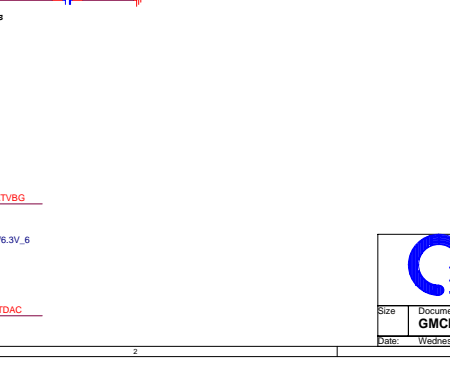
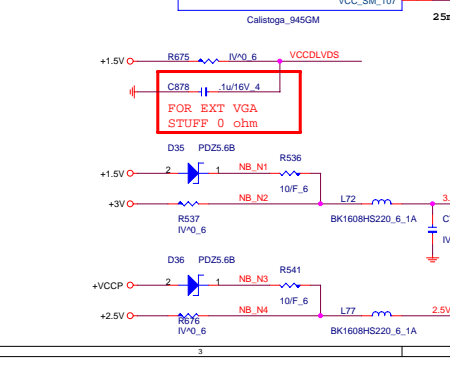
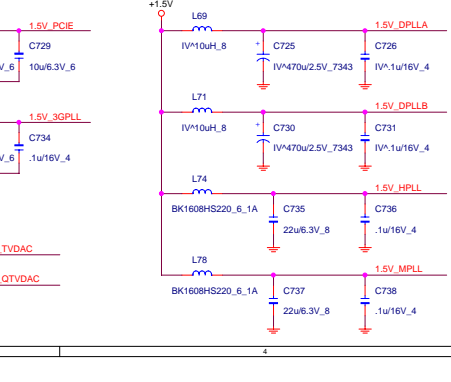
Size	Document Number GMCH (VGA)	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 6 of 29

NB_945GM/PM/940GML

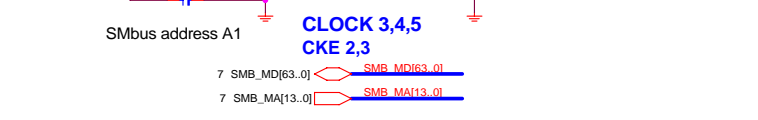
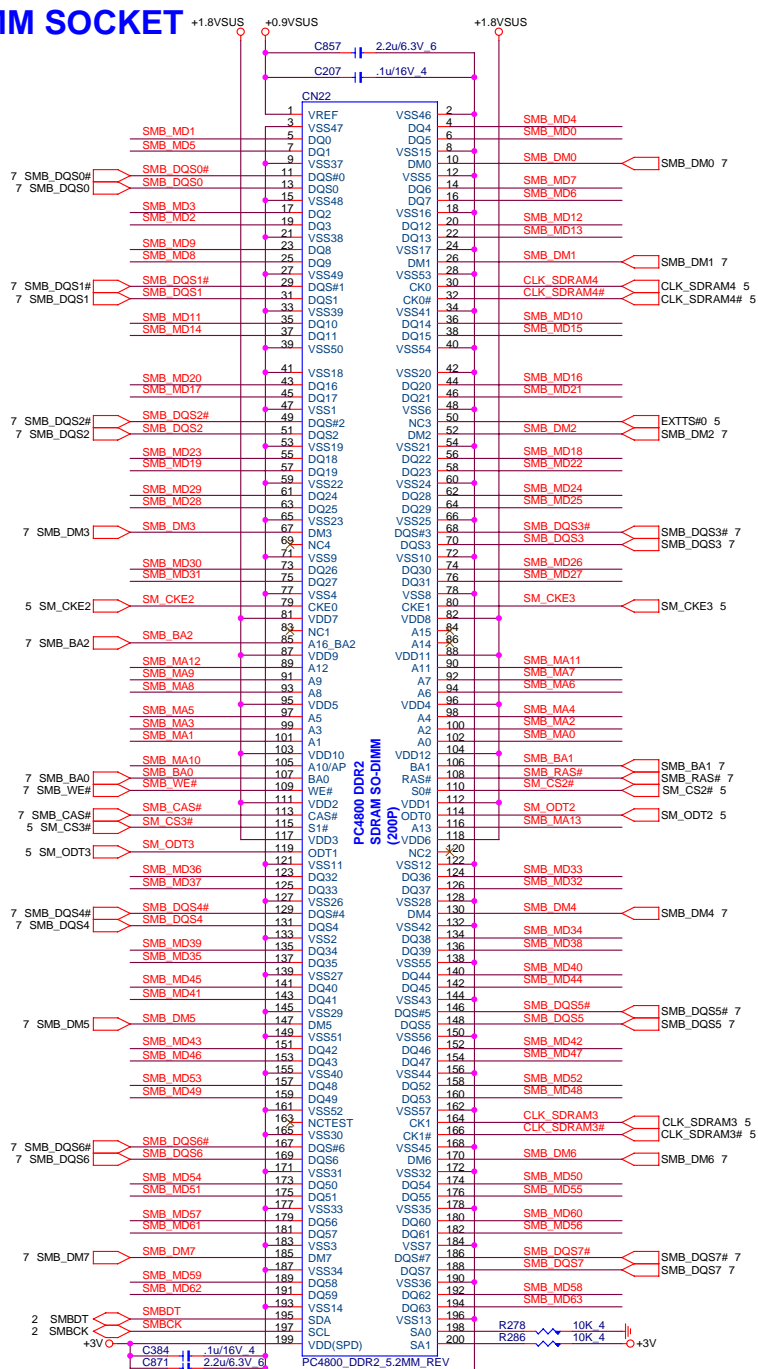
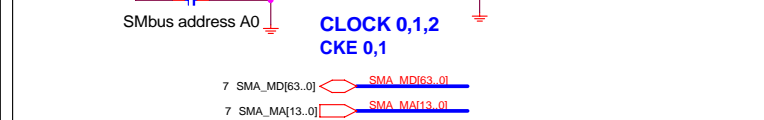
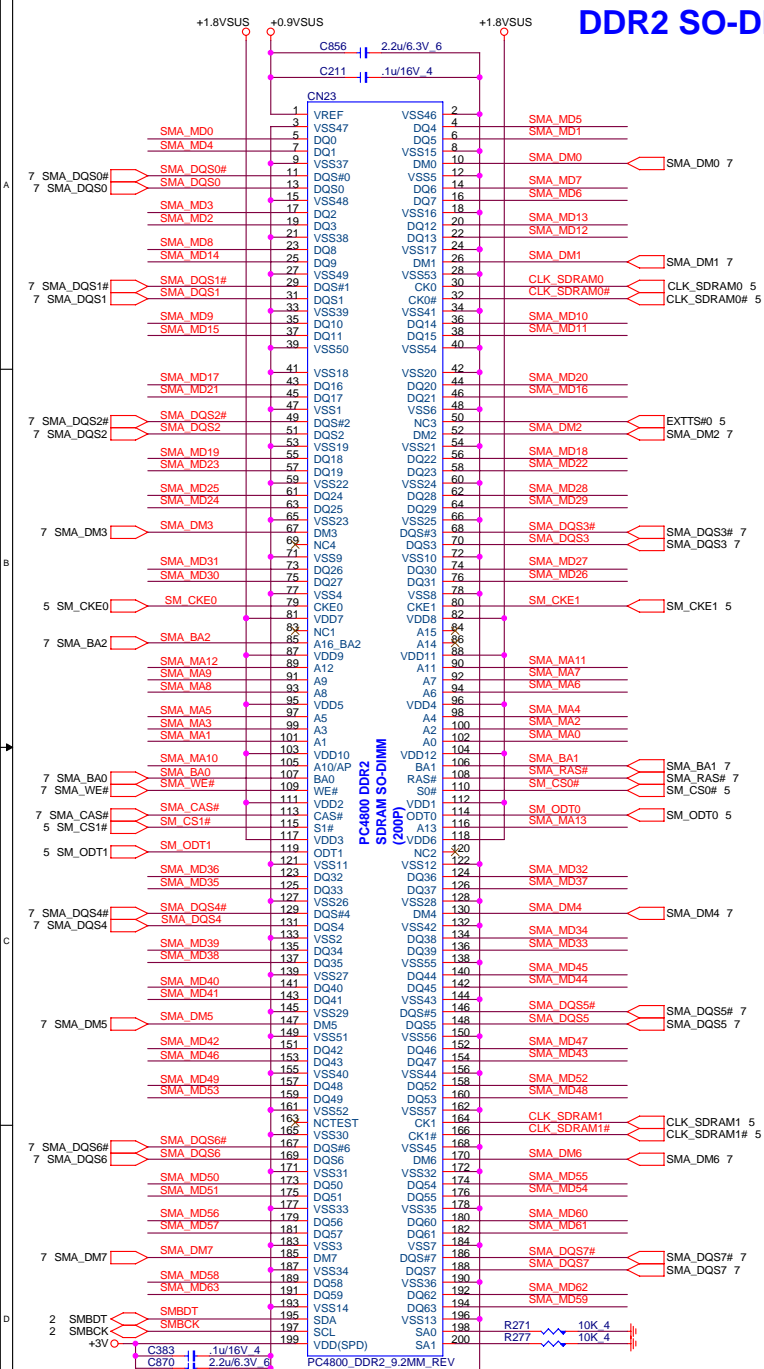


PROJECT : ZR1
Quanta Computer Inc.

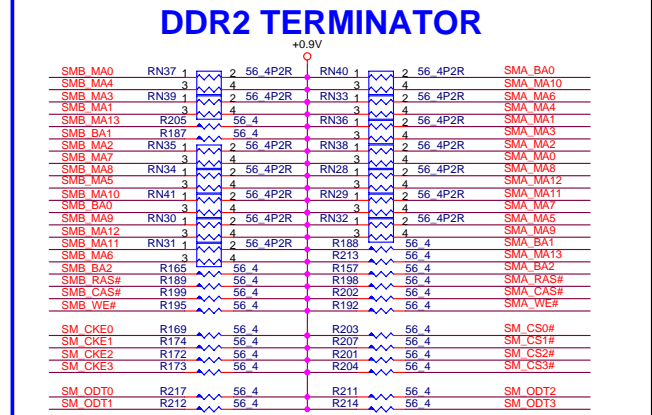
Size	Document Number GMCH (MEMORY)	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 7 of 29



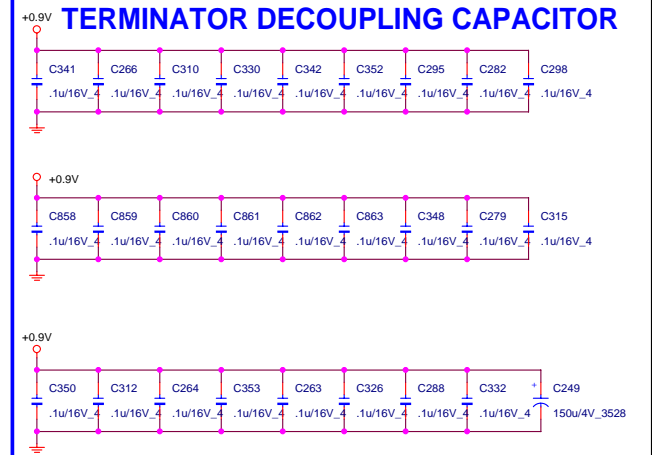
DDR2 SO-DIMM SOCKET



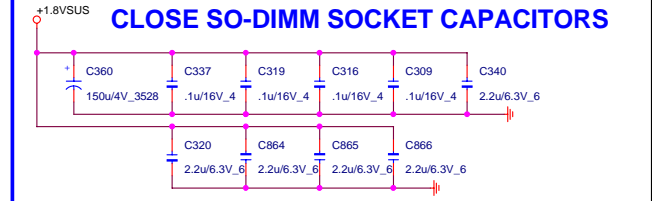
DDR2 TERMINATOR



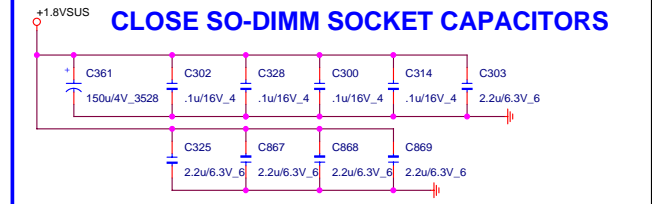
TERMINATOR DECOUPLING CAPACITOR



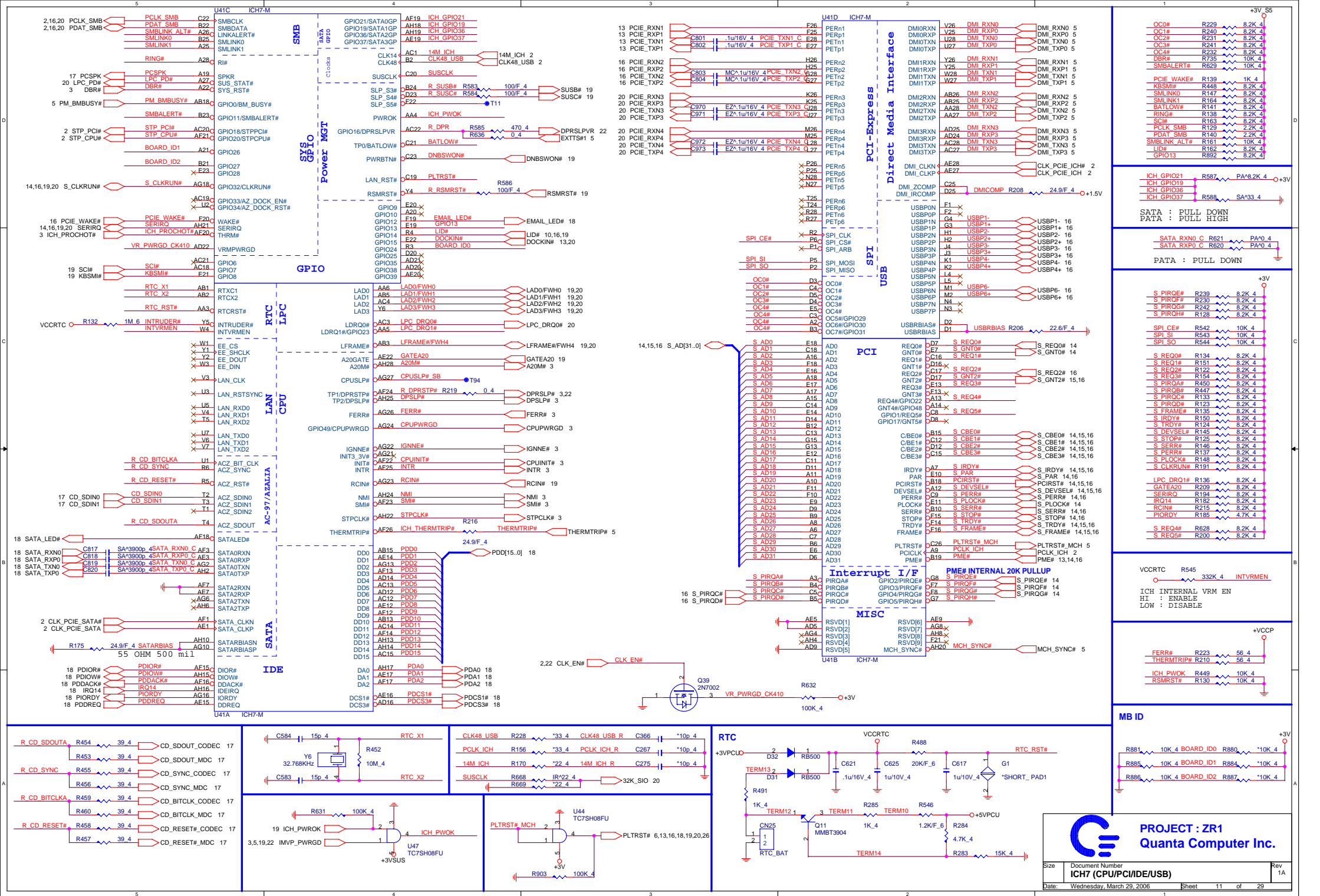
CLOSE SO-DIMM SOCKET CAPACITORS

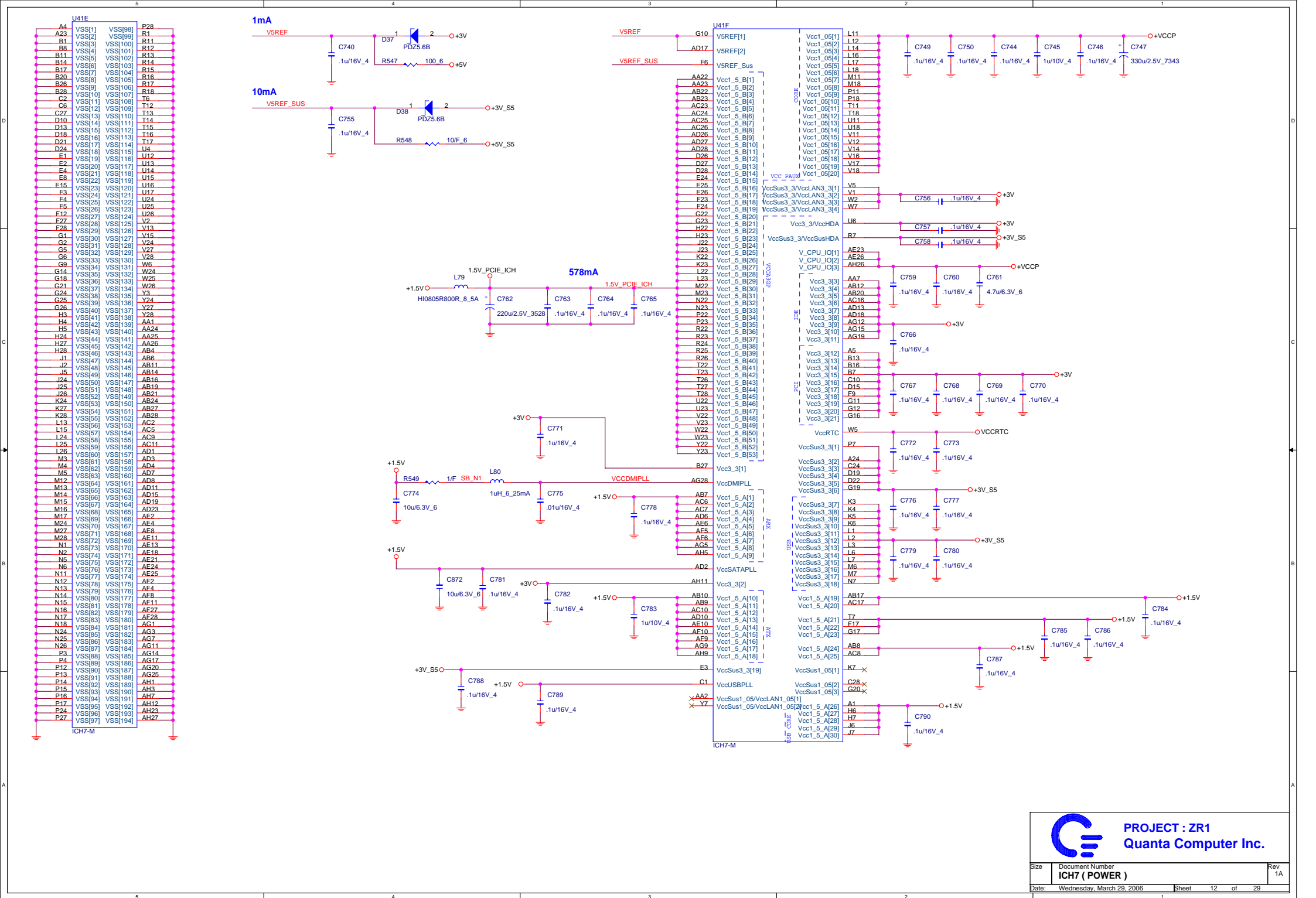


CLOSE SO-DIMM SOCKET CAPACITORS



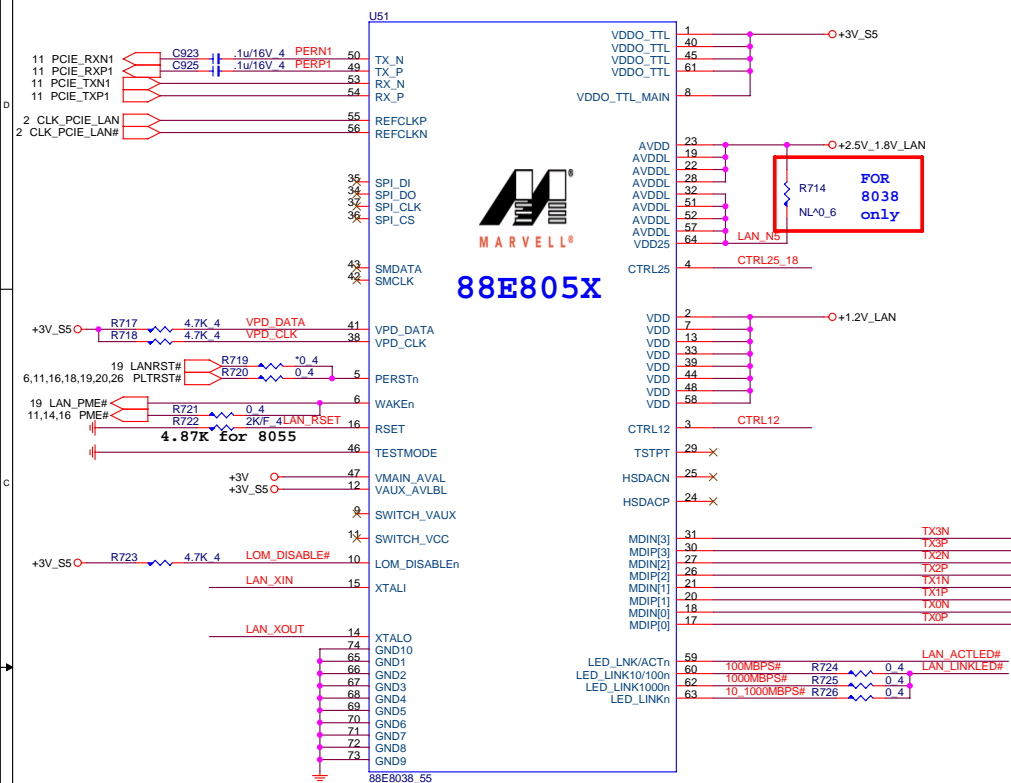
PROJECT : ZR1
Quanta Computer Inc.



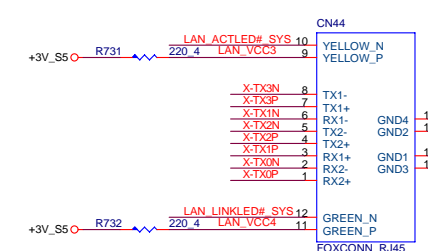
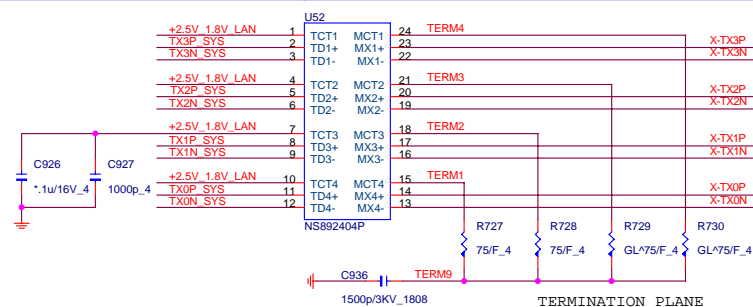
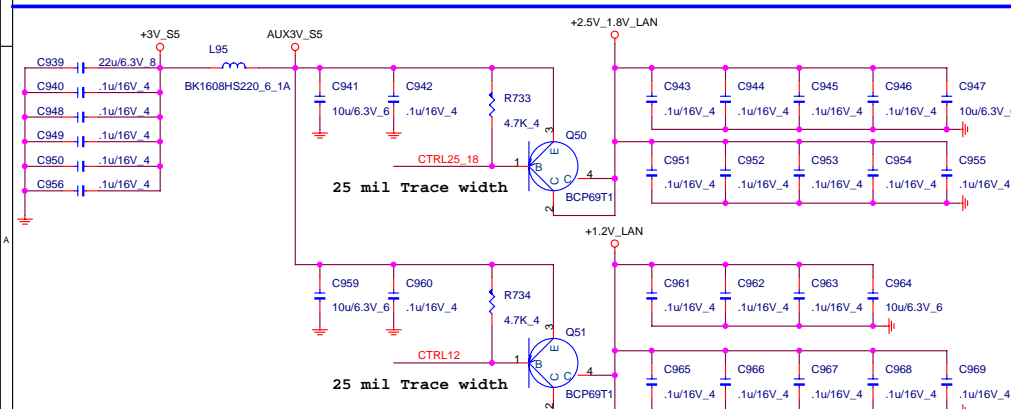
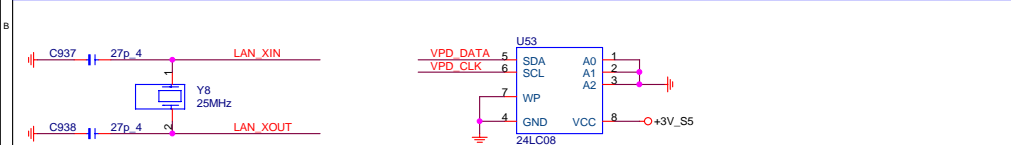
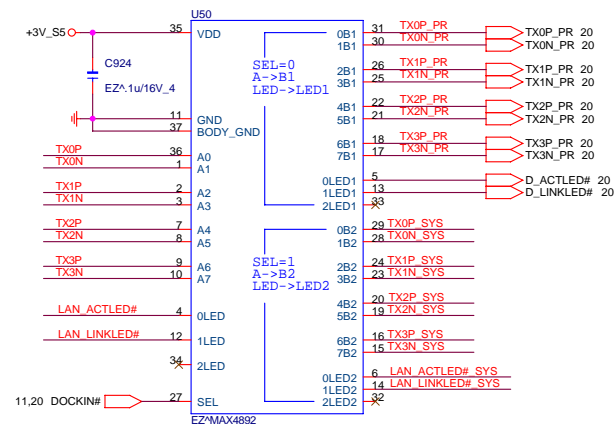
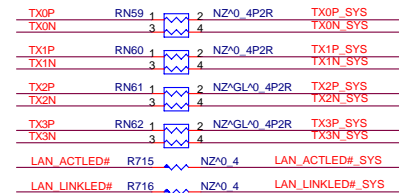
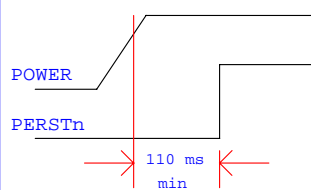


AJ080380000

AJ080550011 A2



RESET TIMING



	BOTHHAND	FCE
10/100	DB0KN7LAN24	DBED2LLAN05
GiGa	DBKN1NLAN03	DB0ZH1LAN06



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Quanta Computer Inc.

Size	Document Number			Rev
	LAN (MARVELL 8038/8055)			1.
Date:	Wednesday, March 29, 2006	Sheet	13	of 29

PCIXX12 PCMCIA

REQ0# AD25
GNT0# PIRQ(E,F,G)#

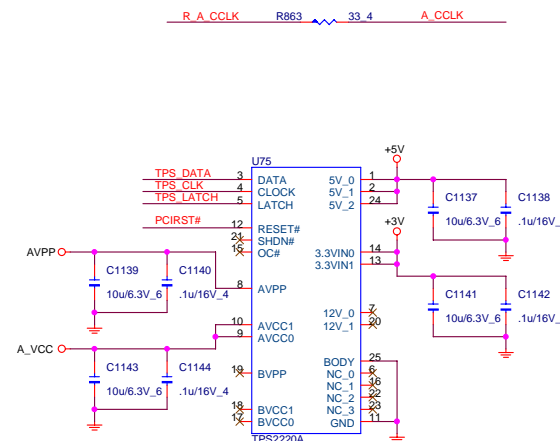
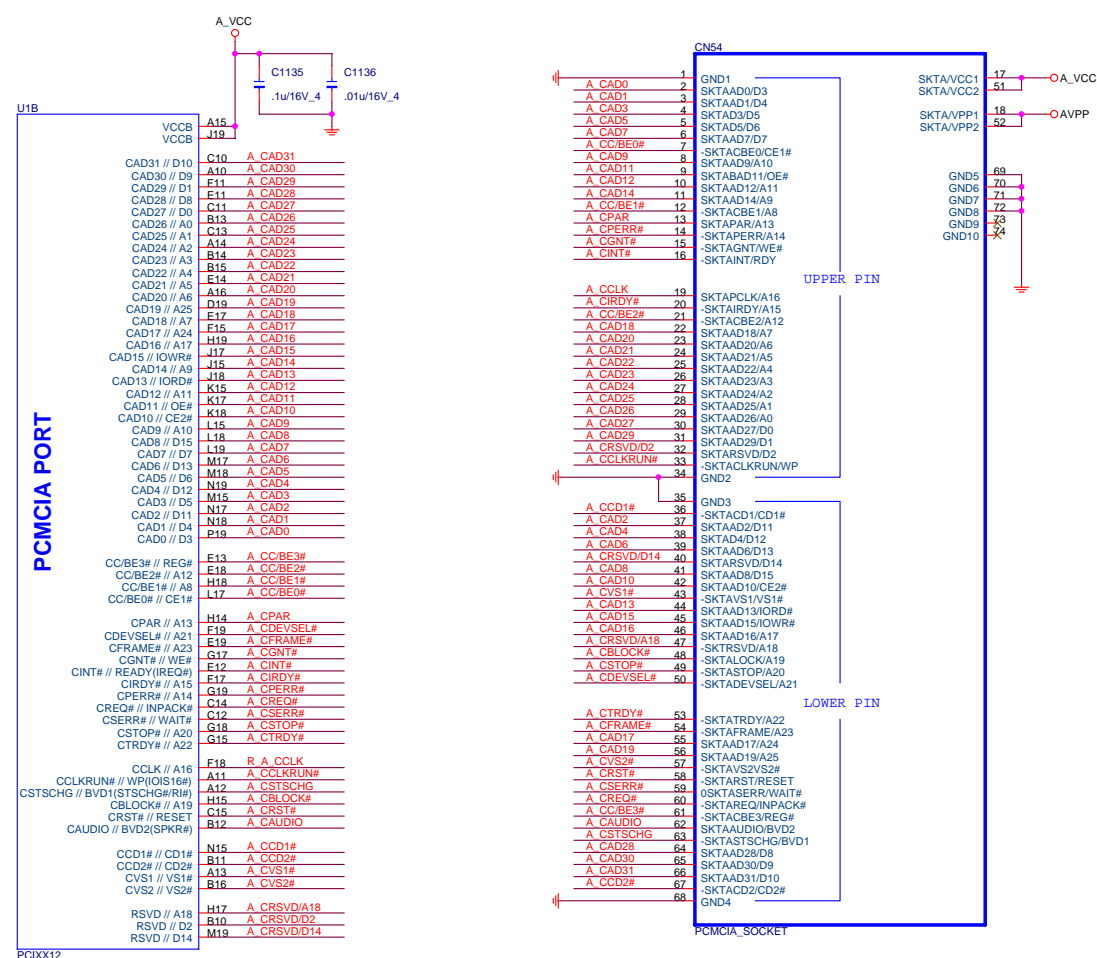
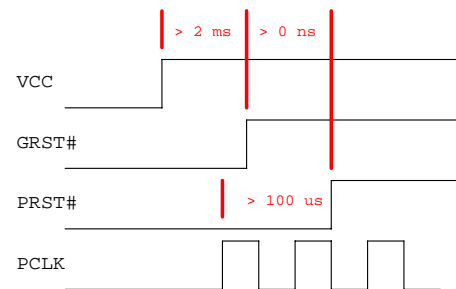
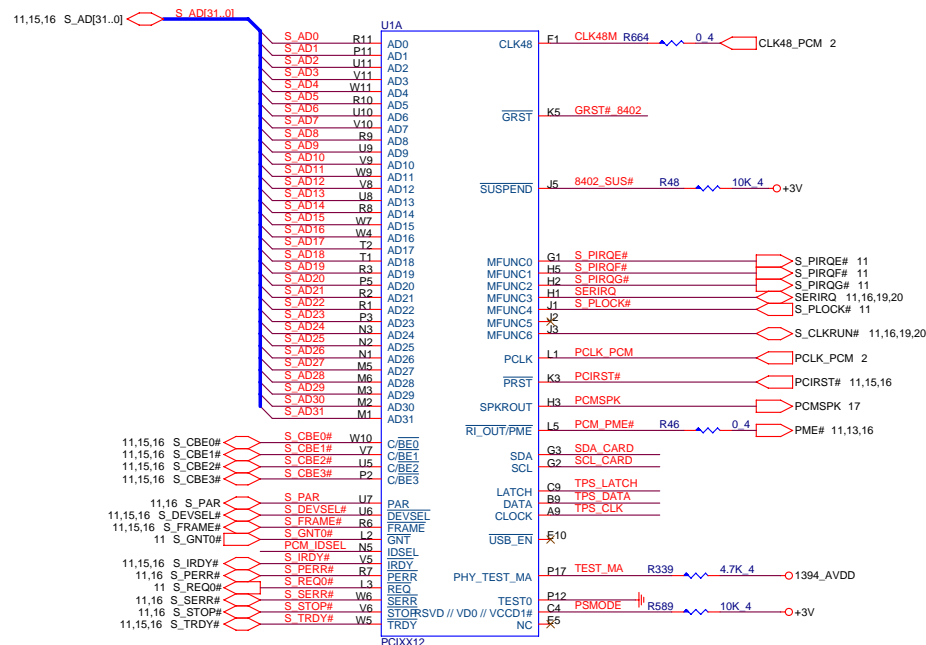
S_AD25 R346 150/F_4 PCM_IDSEL

PCI8412 : AJ084120T08 PCMCIA / 1394 / 5 IN 1

PCI6412 : AL064120T04 PCMCIA / 5 IN 1

PCI1512 : AJ015120T02

PCMCIA

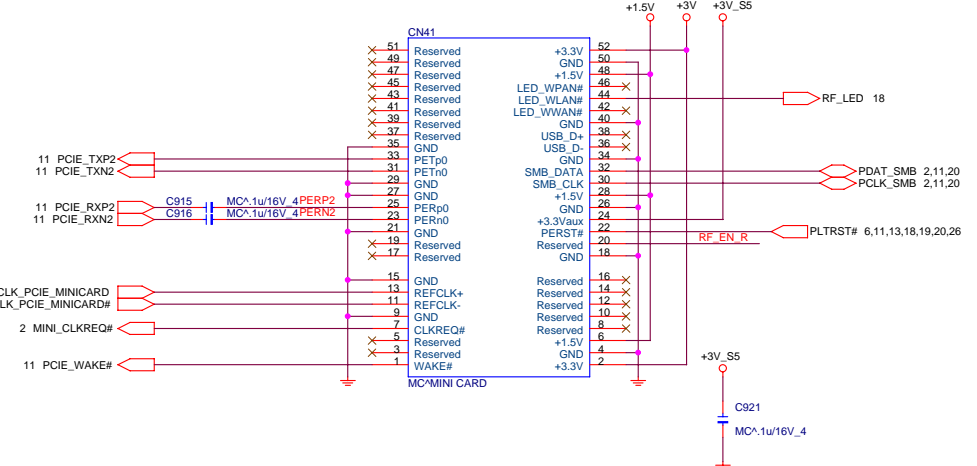


PROJECT : ZR1
Quanta Computer Inc.

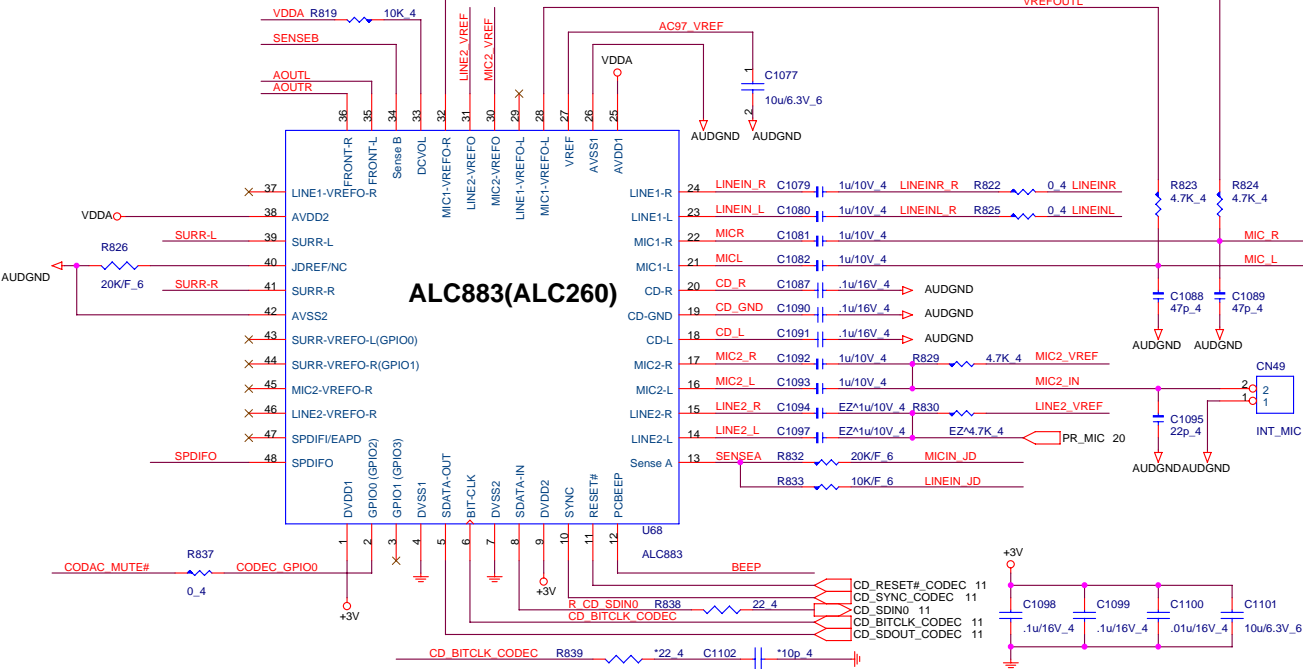
Size	Document Number PCIXX12 (PCMCIA)	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 14 of 29

REQ2# AD19
GNT2# PIRQ(C,D)#

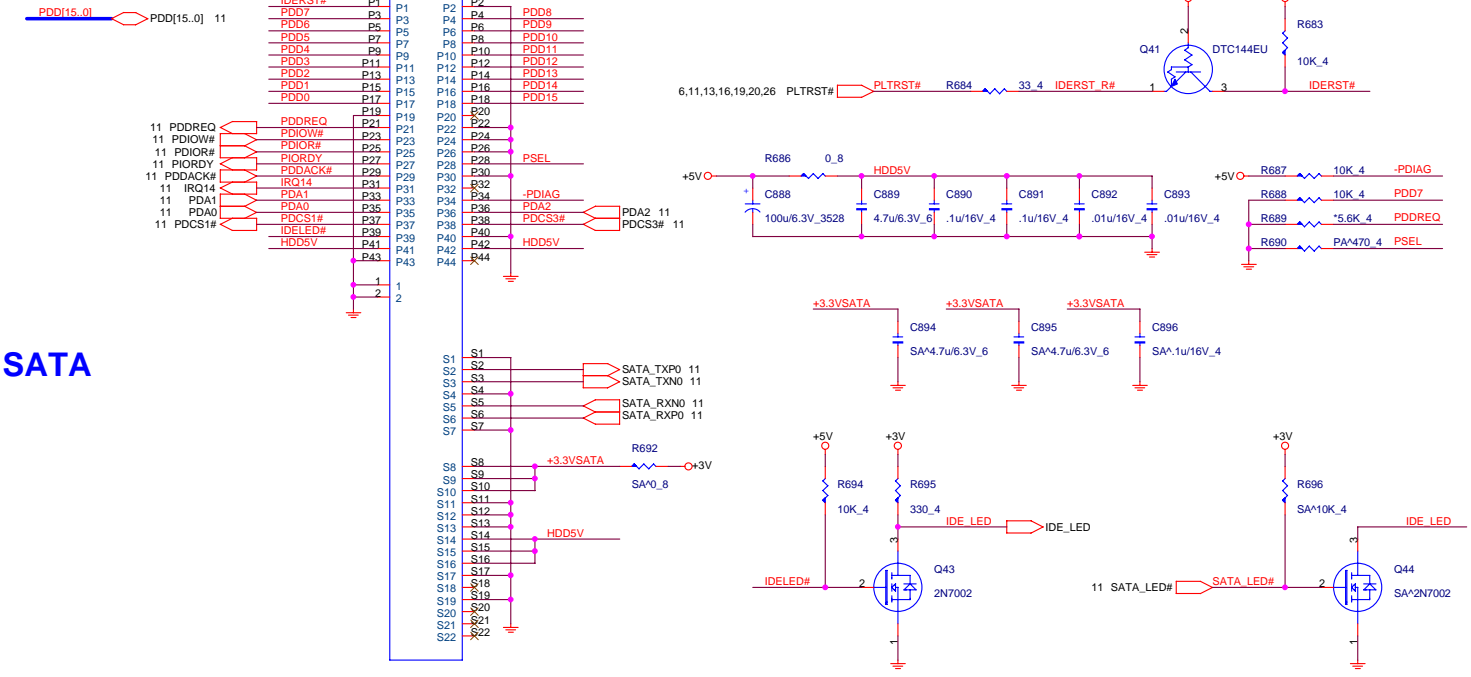
S_AD19_R705 MP150/F_4 MINI_IDSEL

[illegible]

Audio Codec_ALC883

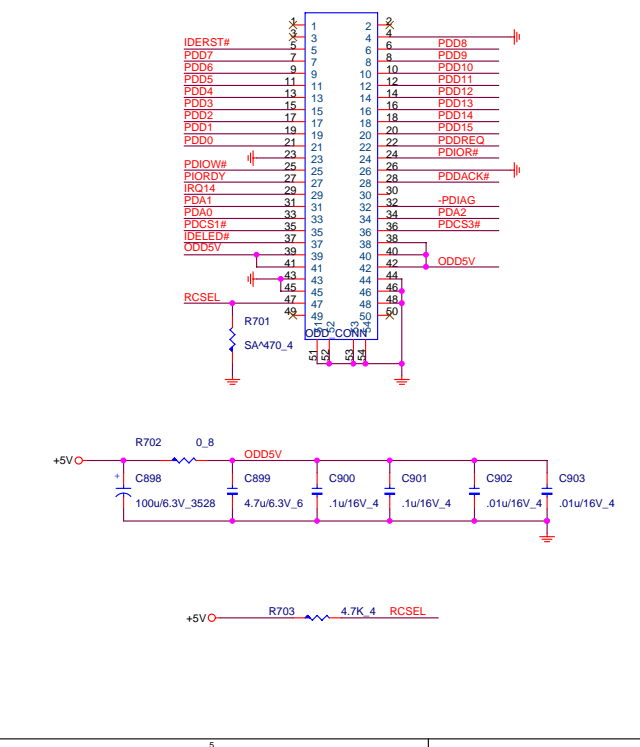


HDD

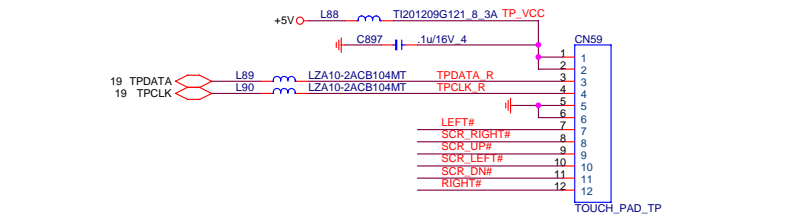


SATA

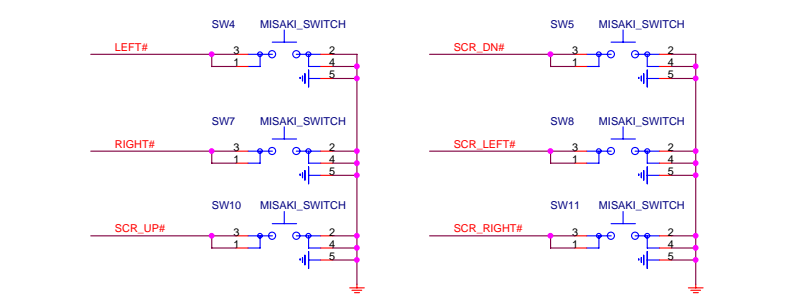
ODD



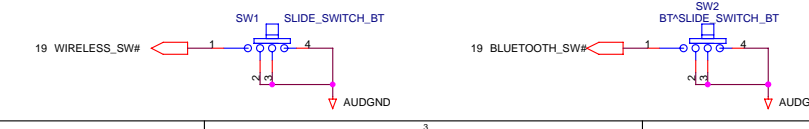
TP CONN



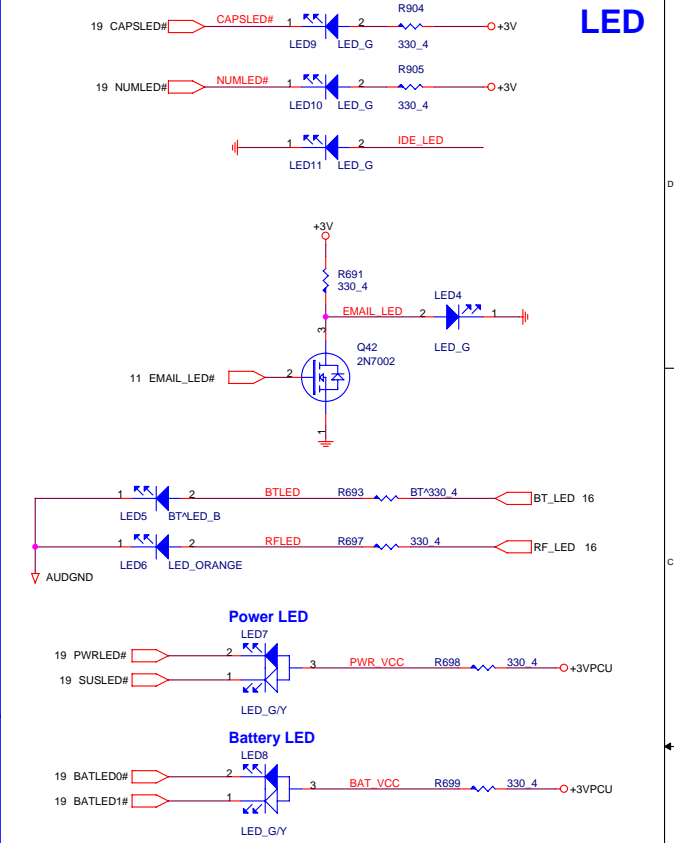
TP SWITCH



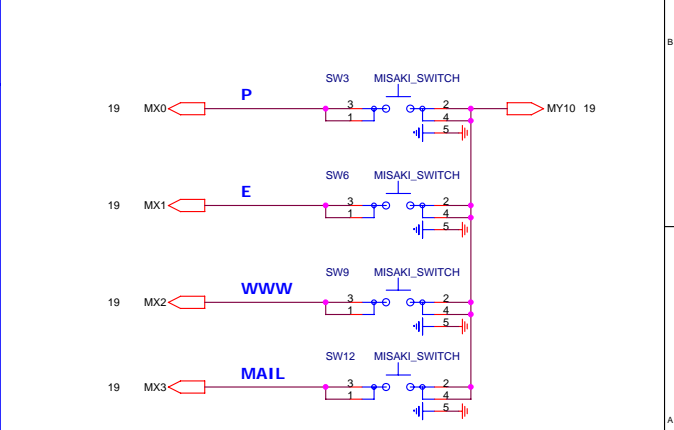
WL & BT SWITCH



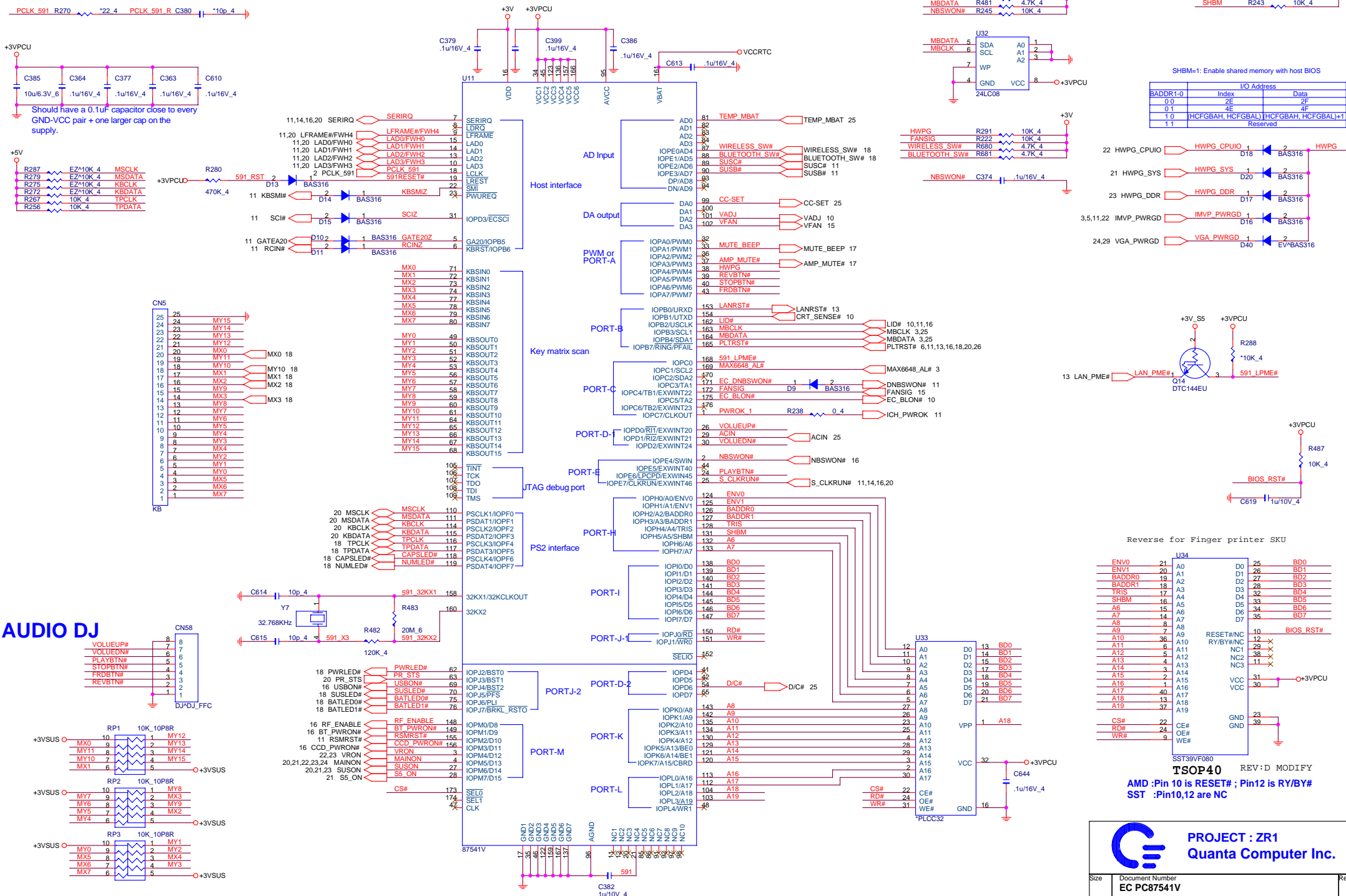
LED



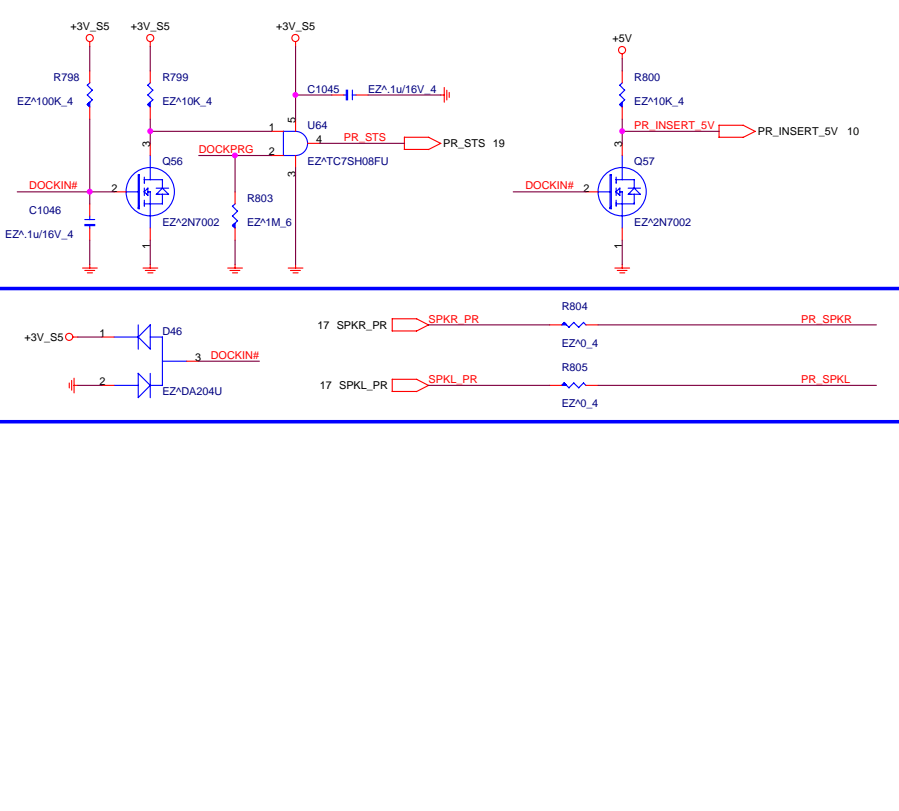
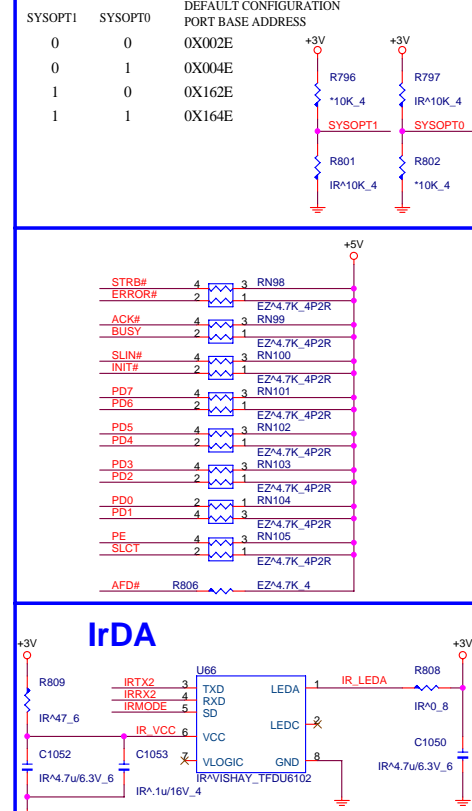
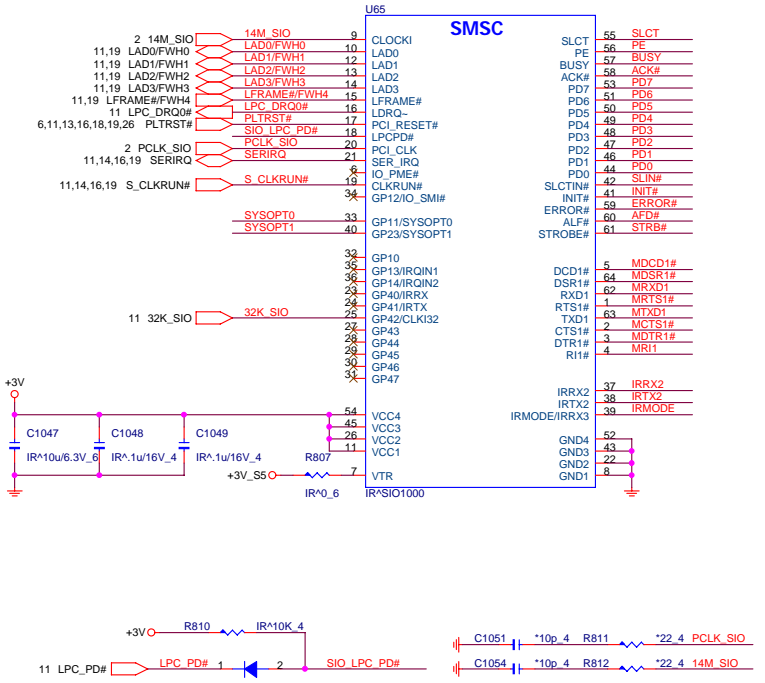
QUICK KEY SWITCH



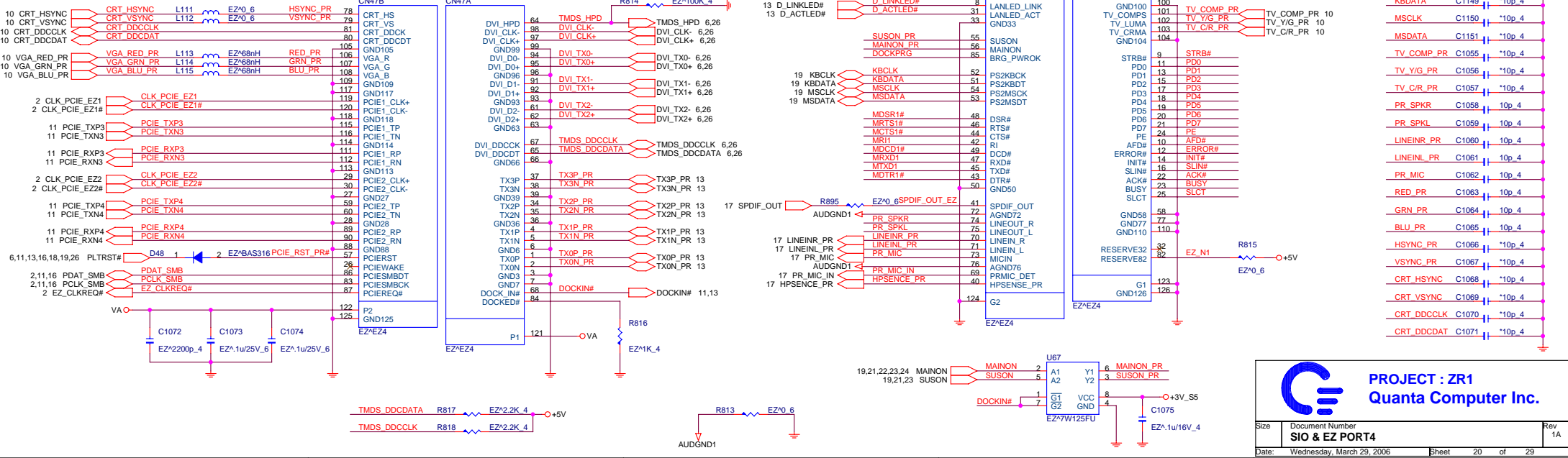
K/B CONTROLLER

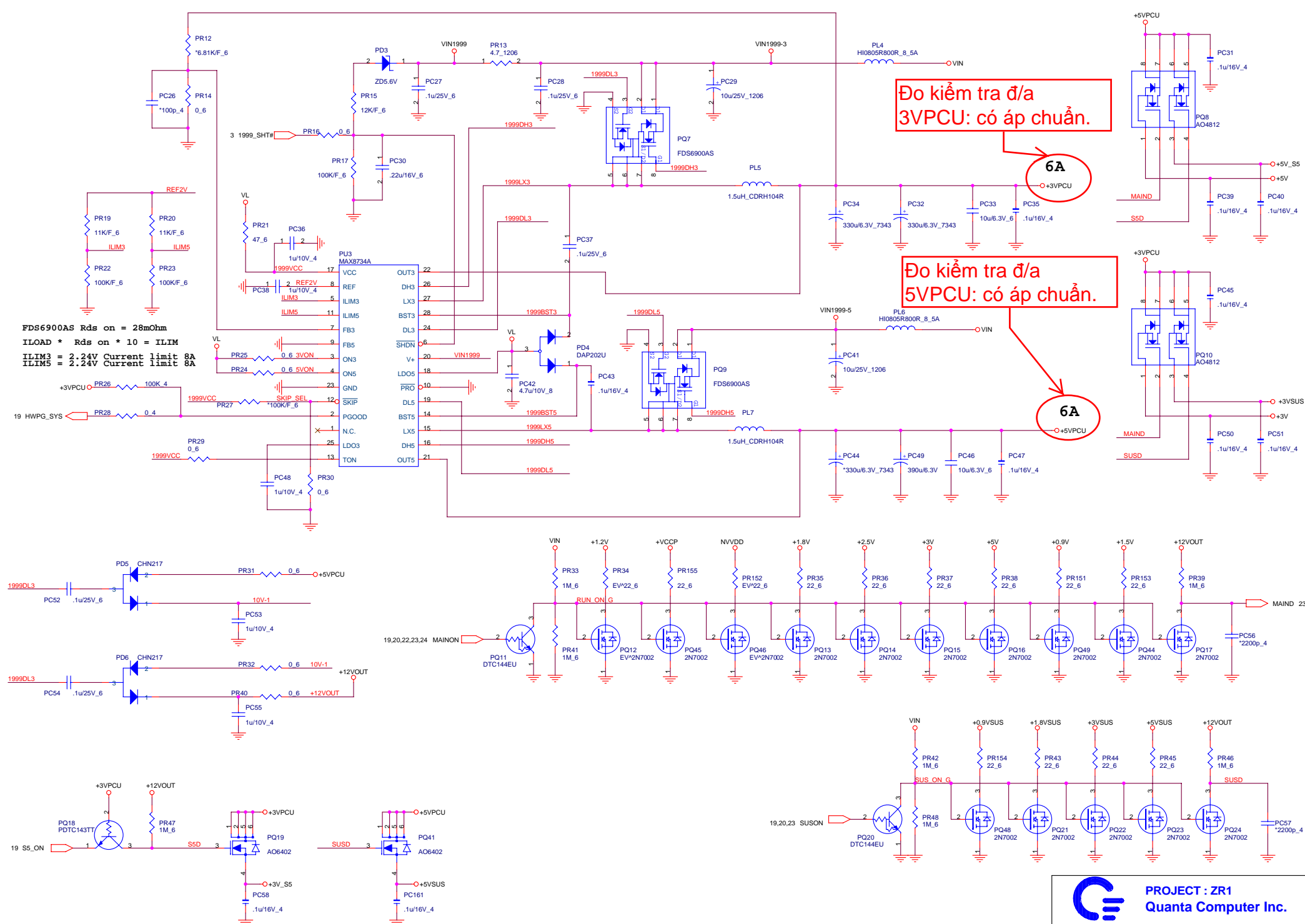


SMSC SIO1000

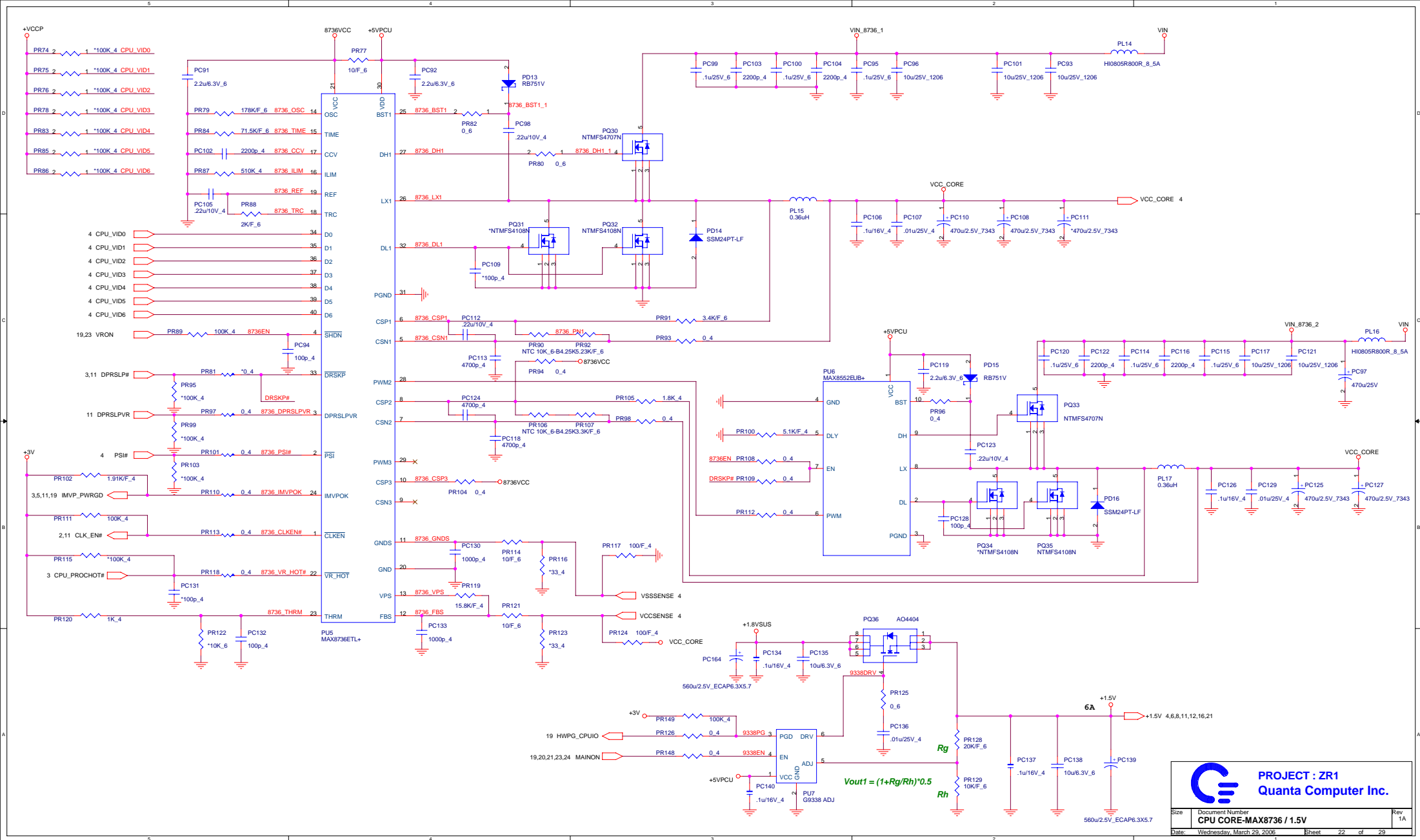


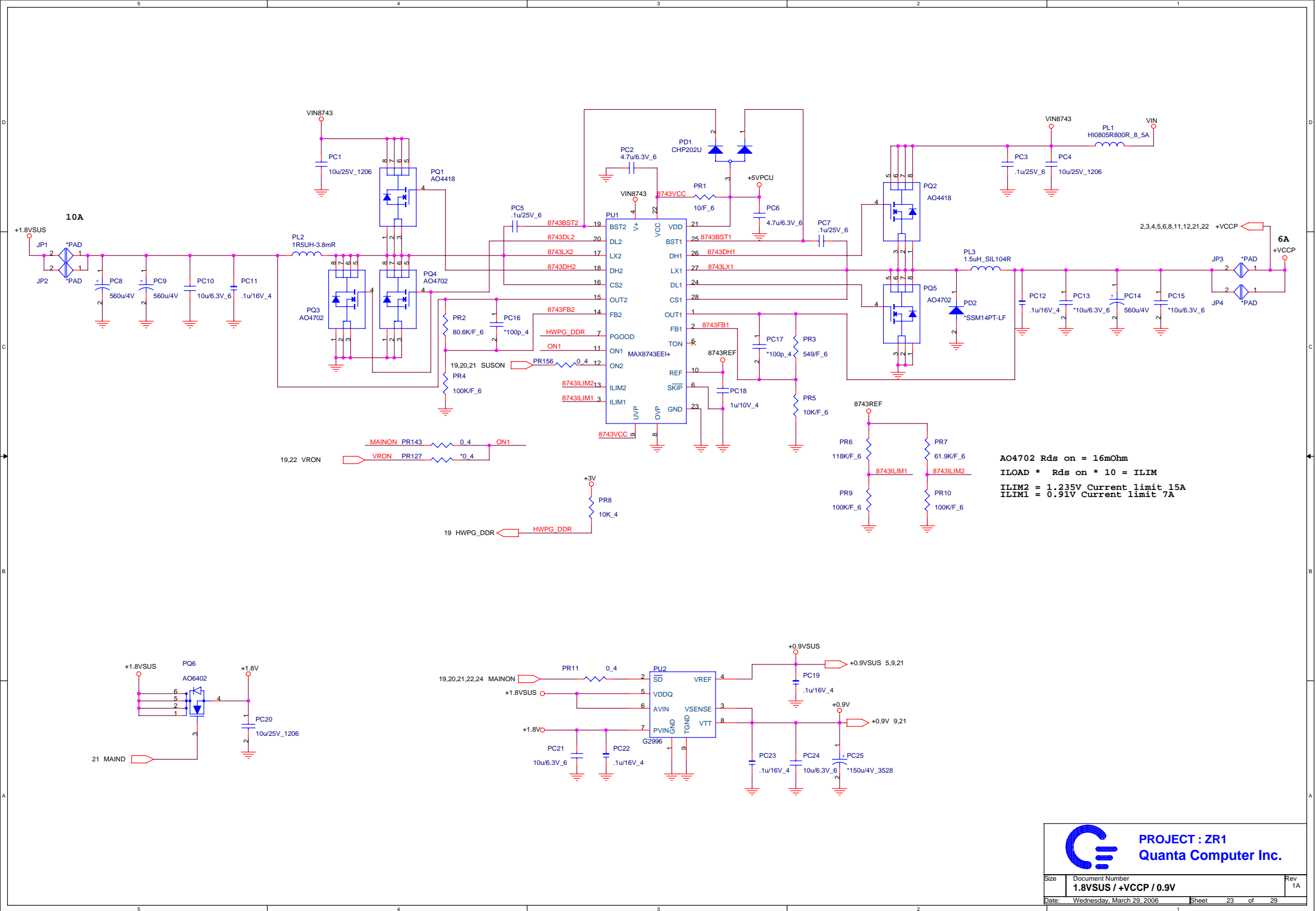
EZ4



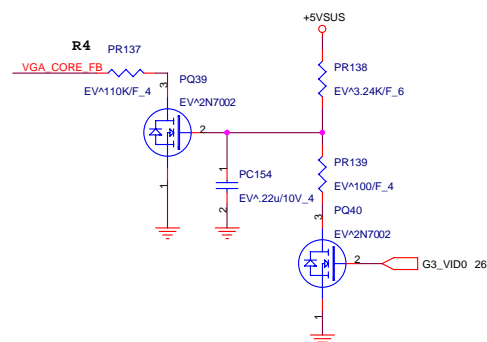
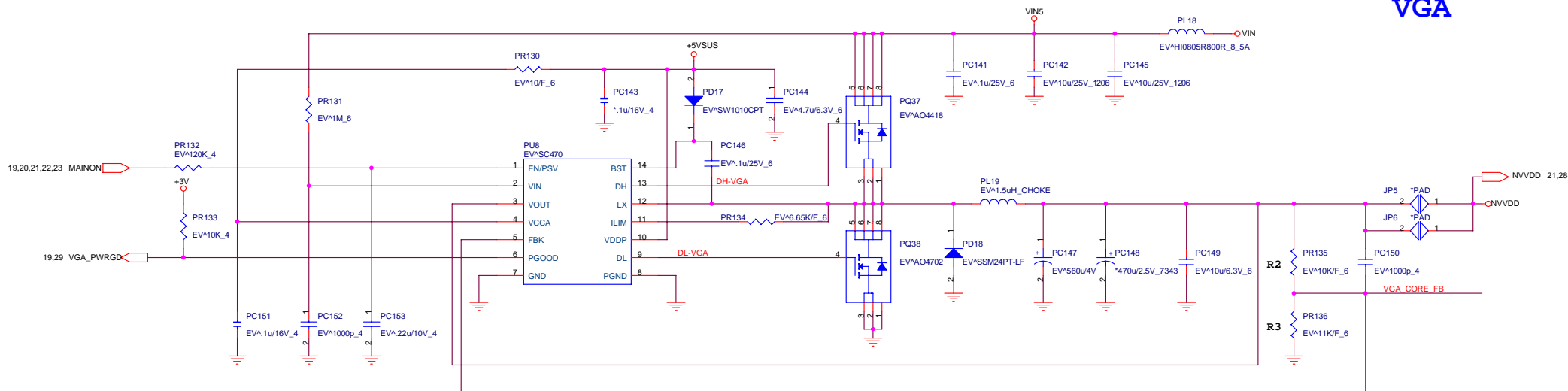


PDS6900AS Rds on = 28mOhm
ILOAD * Rds on * 10 = ILIM
ILIM3 = 2.24V Current limit 8A
ILIM5 = 2.24V Current limit 8A





VGA



$$HI \rightarrow VOUT = (1 + R2/R3) * 0.5$$

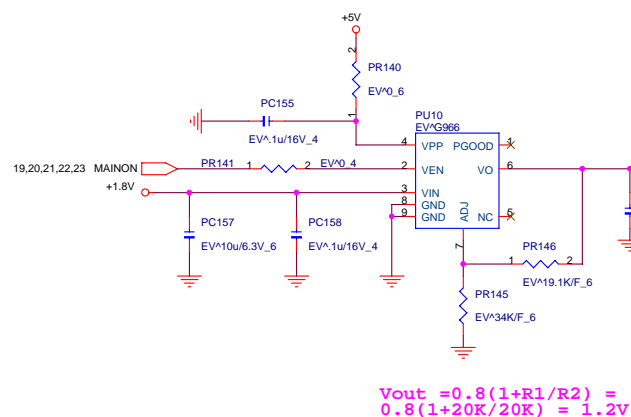
$$LO \rightarrow VOUT = (1 + R2/(R3//R4)) * 0.5$$

M52P(G)
 PR1 : 10K
 PR4 : 11K
 PR2 : 110K

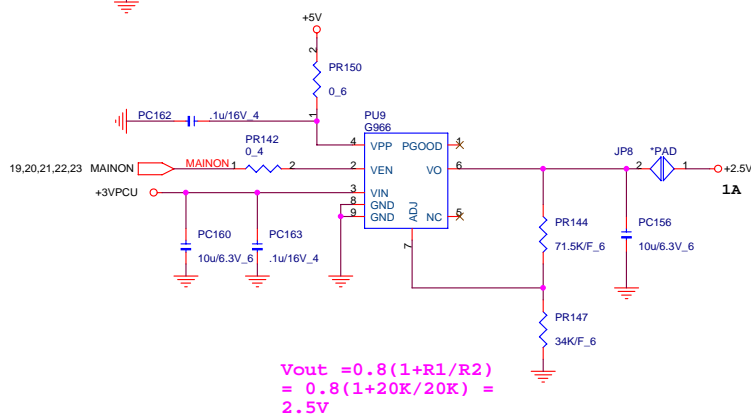
M54P
 PR1 : 12K
 PR4 : 12K
 PR2 : 60.4K

Power Play Mode

VGA_PWR_SW	VGA_CORE
HI	0.95V--M52P(G) 1.0V --M54P
Default LO	1.0V--M52P(G) 1.1V--M54P



$$Vout = 0.8(1 + R1/R2) = 0.8(1 + 20K/20K) = 1.2V$$

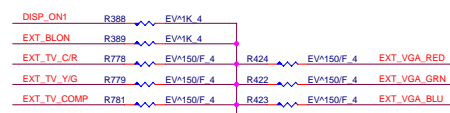
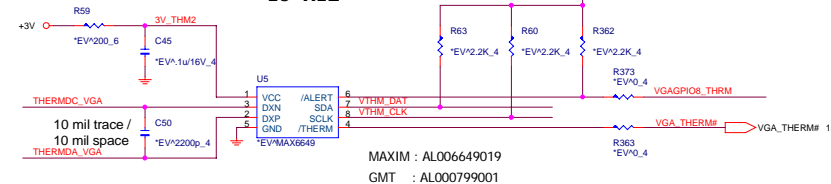
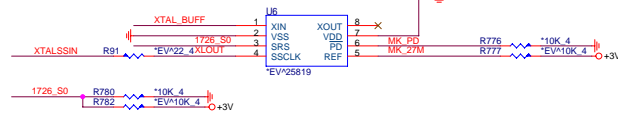
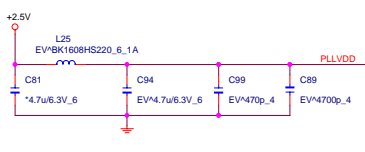
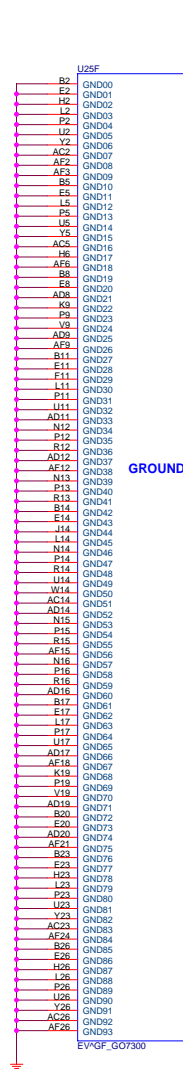
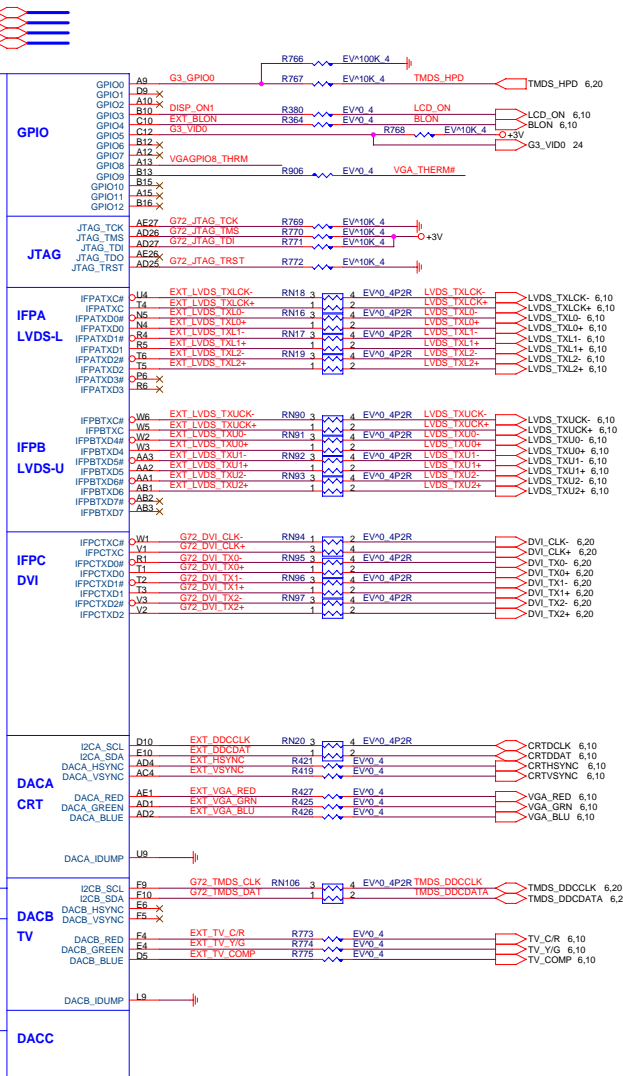
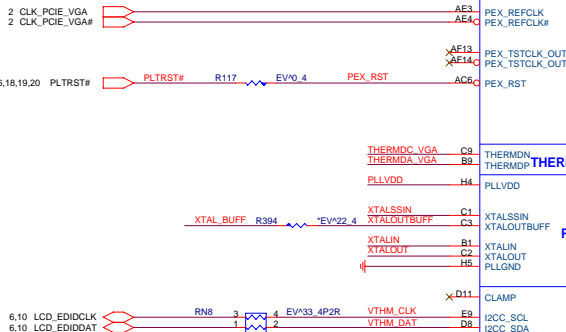


$$Vout = 0.8(1 + R1/R2) = 0.8(1 + 20K/20K) = 2.5V$$



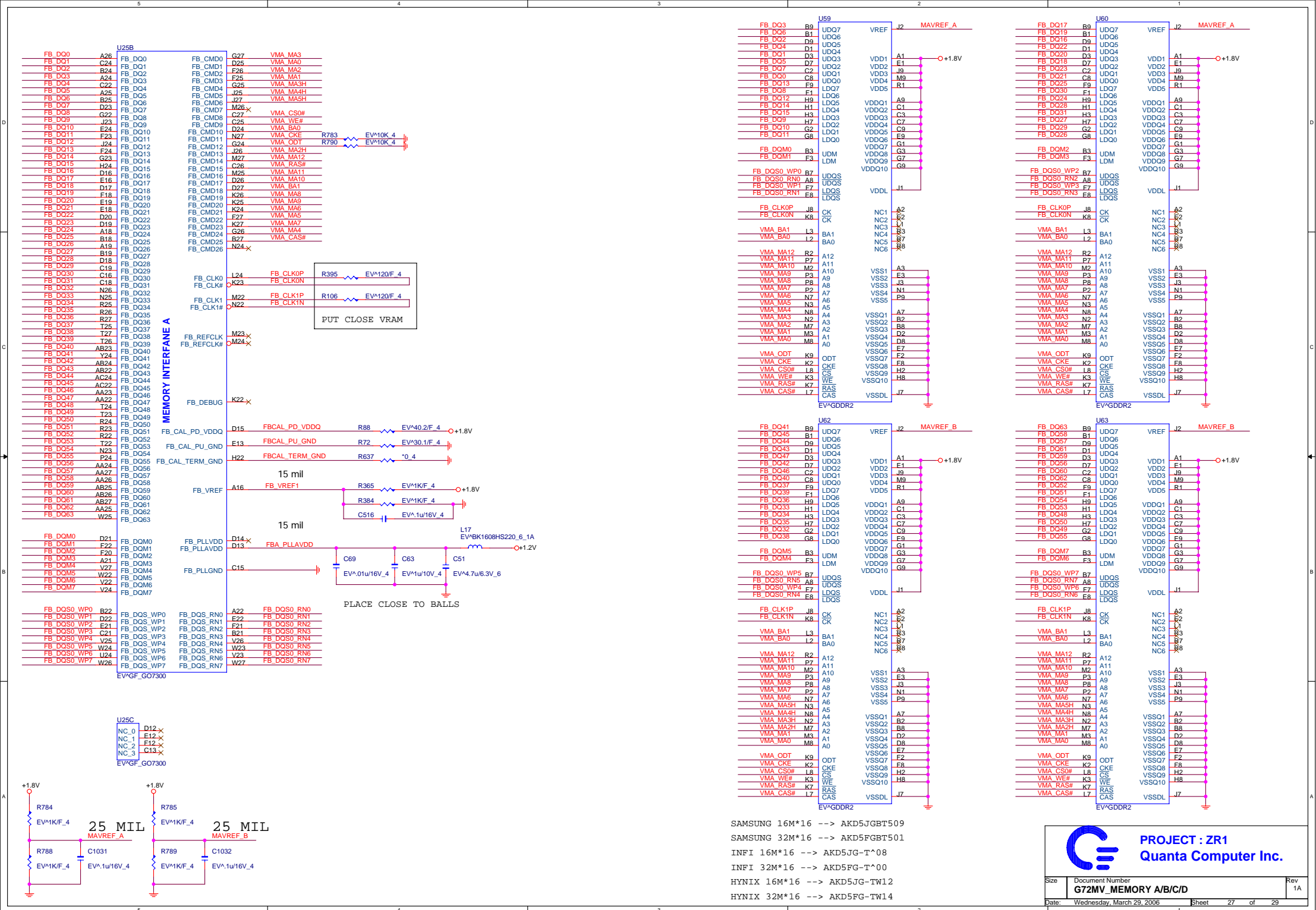
PROJECT : ZR1
 Quanta Computer Inc.

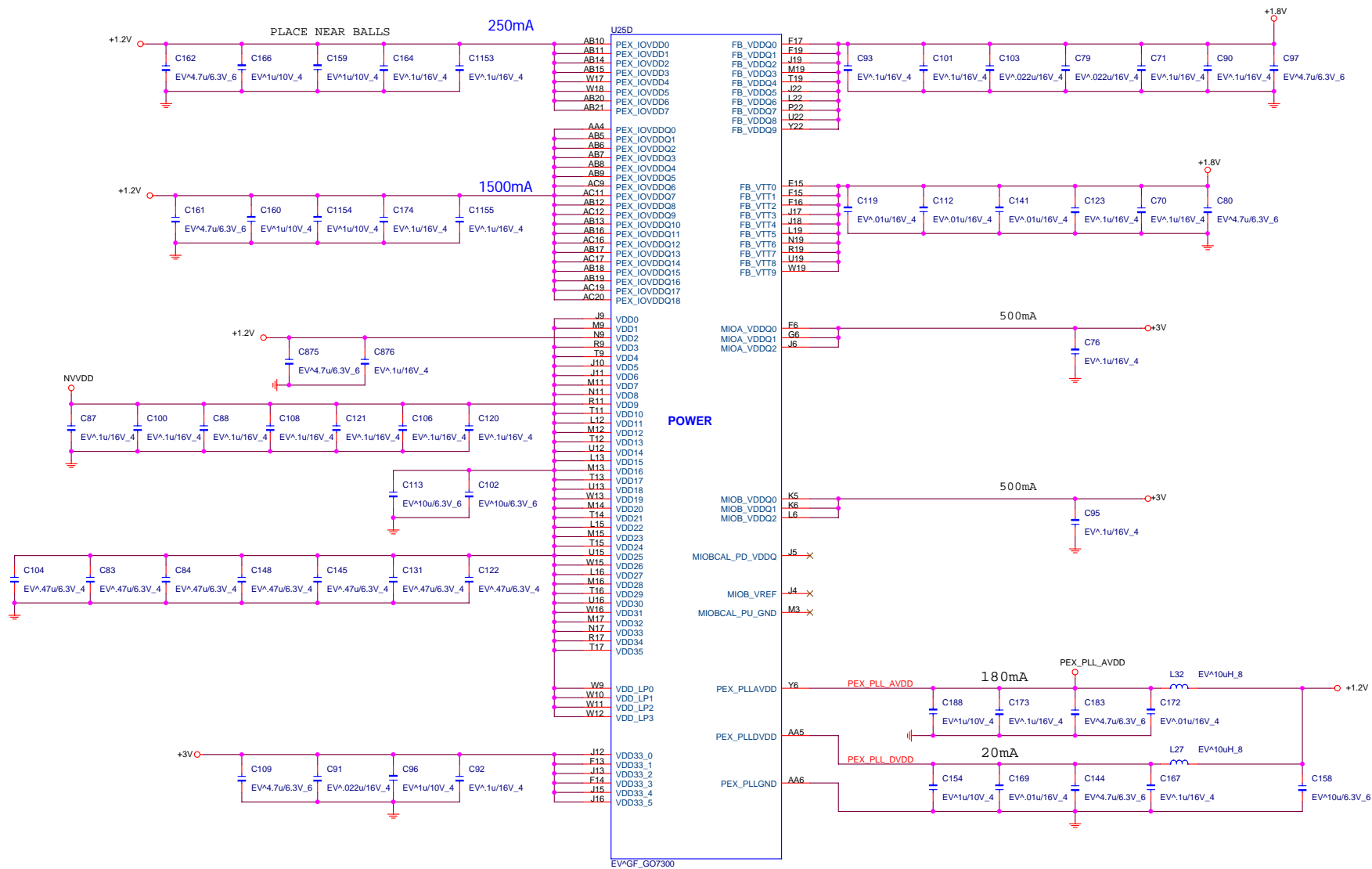
0.1u Capacitors place at
last 1/3 of trace



PROJECT : ZR1
Quanta Computer Inc.

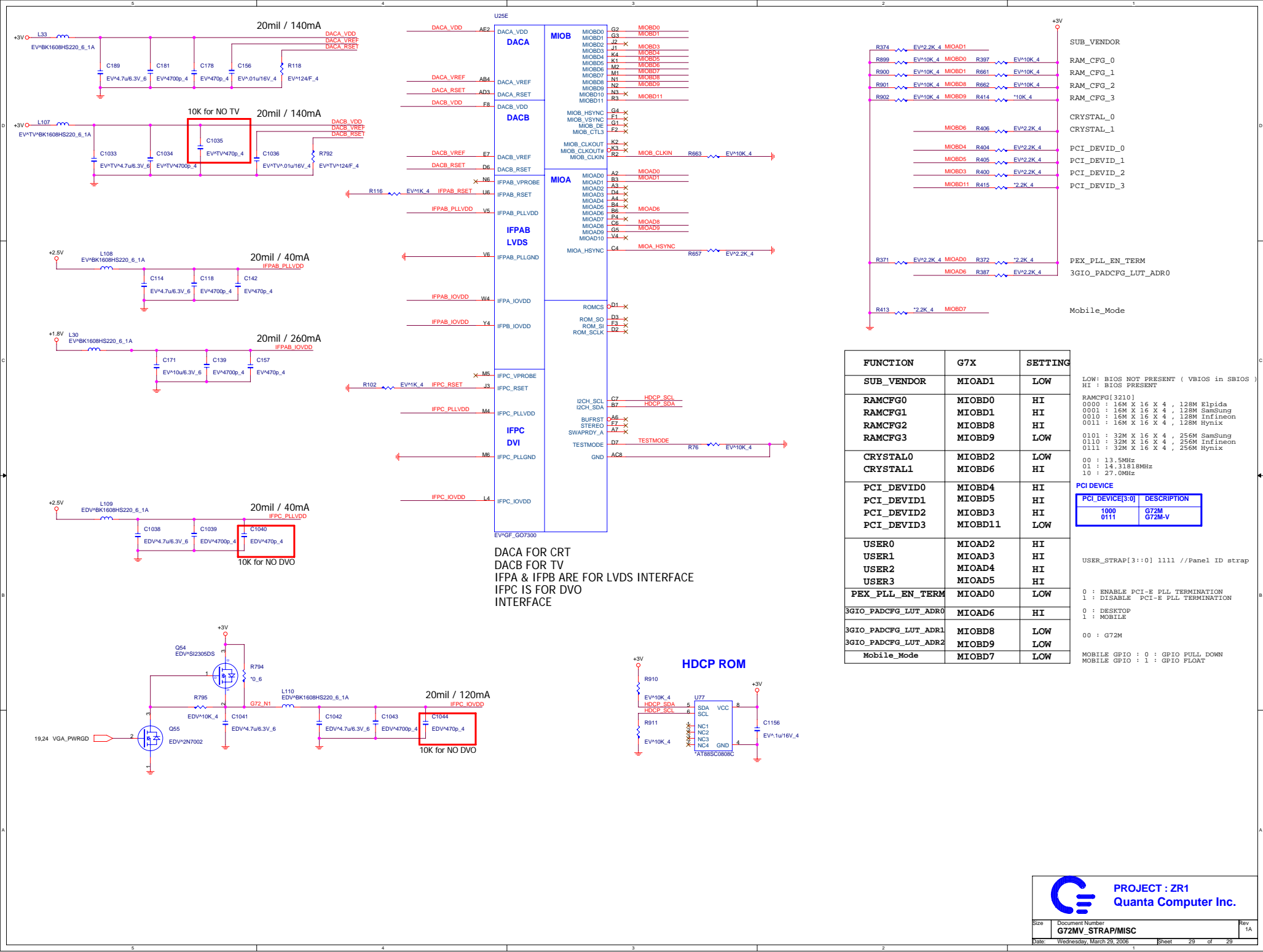
Size	Document Number G72MV_PCIE/DAC/GND	Rev 1A
Date:	Wednesday, March 29, 2006	Sheet 26 of 29





PROJECT : ZR1
Quanta Computer Inc.

Size	Document Number	Rev
	G72MV_POWER	1A
Date:	Wednesday, March 29, 2006	Sheet 28 of 29



FUNCTION	G7X	SETTING
SUB_VENDOR	MIOAD1	LOW
RAMCFG0	MIOBD0	HI
RAMCFG1	MIOBD1	HI
RAMCFG2	MIOBD8	HI
RAMCFG3	MIOBD9	LOW
CRYSTAL0	MIOBD2	LOW
CRYSTAL1	MIOBD6	HI
PCI_DEVID0	MIOBD4	HI
PCI_DEVID1	MIOBD5	HI
PCI_DEVID2	MIOBD3	HI
PCI_DEVID3	MIOBD11	LOW
USER0	MIOAD2	HI
USER1	MIOAD3	HI
USER2	MIOAD4	HI
USER3	MIOAD5	HI
PEX_PLL_EN_TERM	MIOAD0	LOW
3GIO_PADCFG_LUT_ADR0	MIOAD6	HI
3GIO_PADCFG_LUT_ADR1	MIOBD8	LOW
3GIO_PADCFG_LUT_ADR2	MIOBD9	LOW
Mobile_Mode	MIOBD7	LOW

LOW: BIOS NOT PRESENT (VBIOS in SBIOS)
HI : BIOS PRESENT

RAMCFG[3210]
0000 : 16M X 16 X 4 , 128M Elpida
0001 : 16M X 16 X 4 , 128M Samsung
0010 : 16M X 16 X 4 , 128M Infineon
0011 : 16M X 16 X 4 , 128M Hynix
0101 : 32M X 16 X 4 , 256M Samsung
0110 : 32M X 16 X 4 , 256M Infineon
0111 : 32M X 16 X 4 , 256M Hynix

PCI DEVICE

PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M
0111	G72M-V

USER_STRAP[31:0] 1111 //Panel ID strap

0 : ENABLE PCI-E PLL TERMINATION
1 : DISABLE PCI-E PLL TERMINATION

0 : DESKTOP
1 : MOBILE

00 : G72M

MOBILE GPIO : 0 : GPIO PULL DOWN
MOBILE GPIO : 1 : GPIO FLOAT