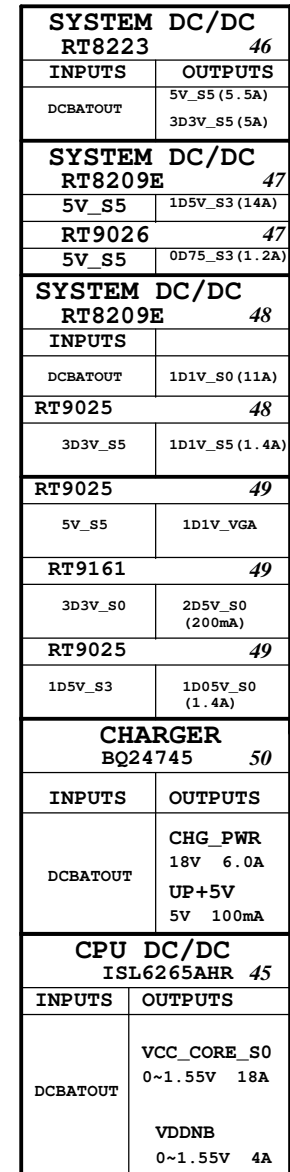


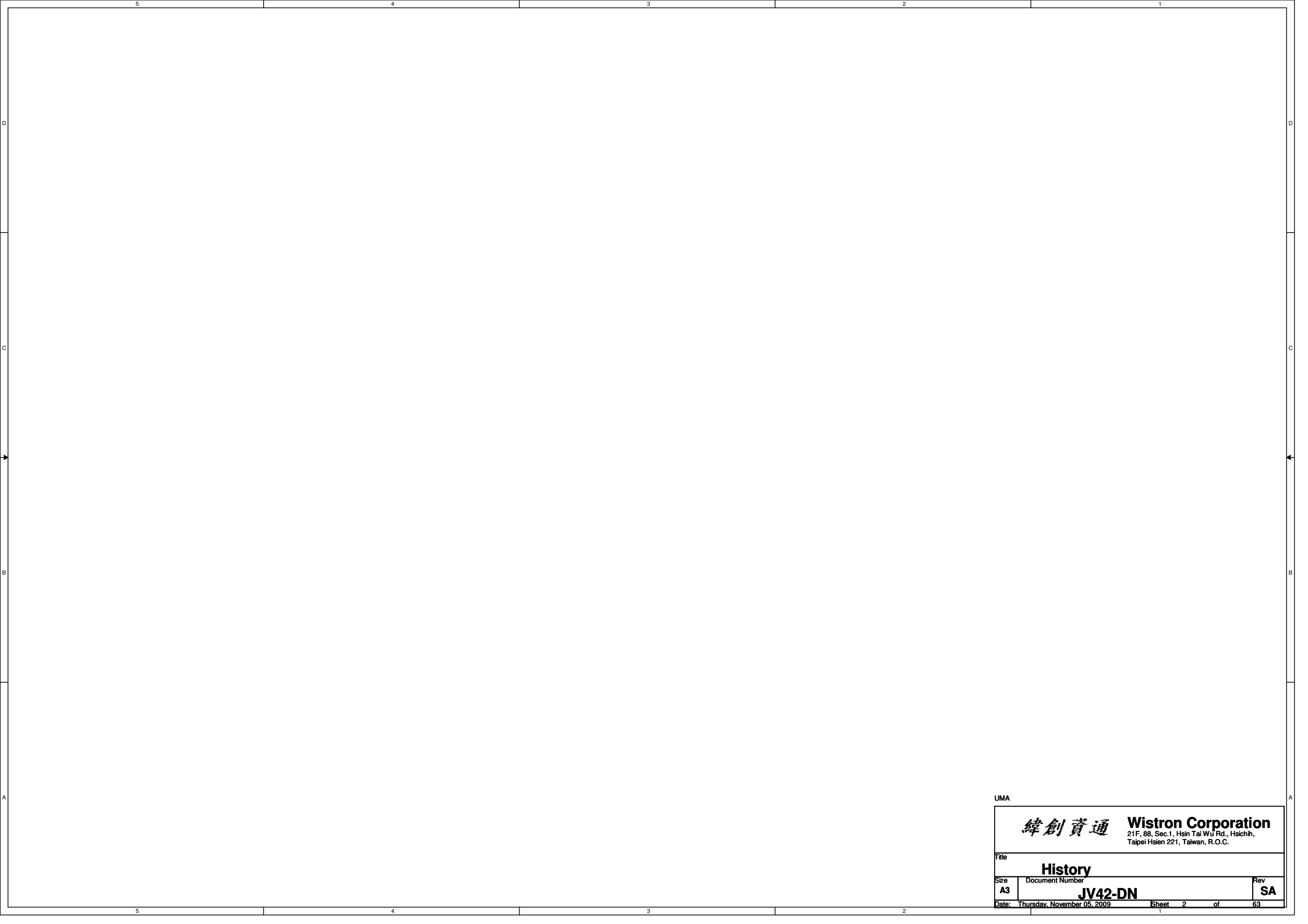
Diagram illustrating the layout of a PCB (Printed Circuit Board) showing the connection of a component to the power planes (VCC and GND) and signal planes (S).

The layout shows the following connections:

- TOP** layer: A large **VCC** pad and two **S** pads.
- VCC** layer: A large **VCC** pad.
- S** layer: Two **S** pads.
- GND** layer: A large **GND** pad.
- BOTTOM** layer: Two **S** pads.

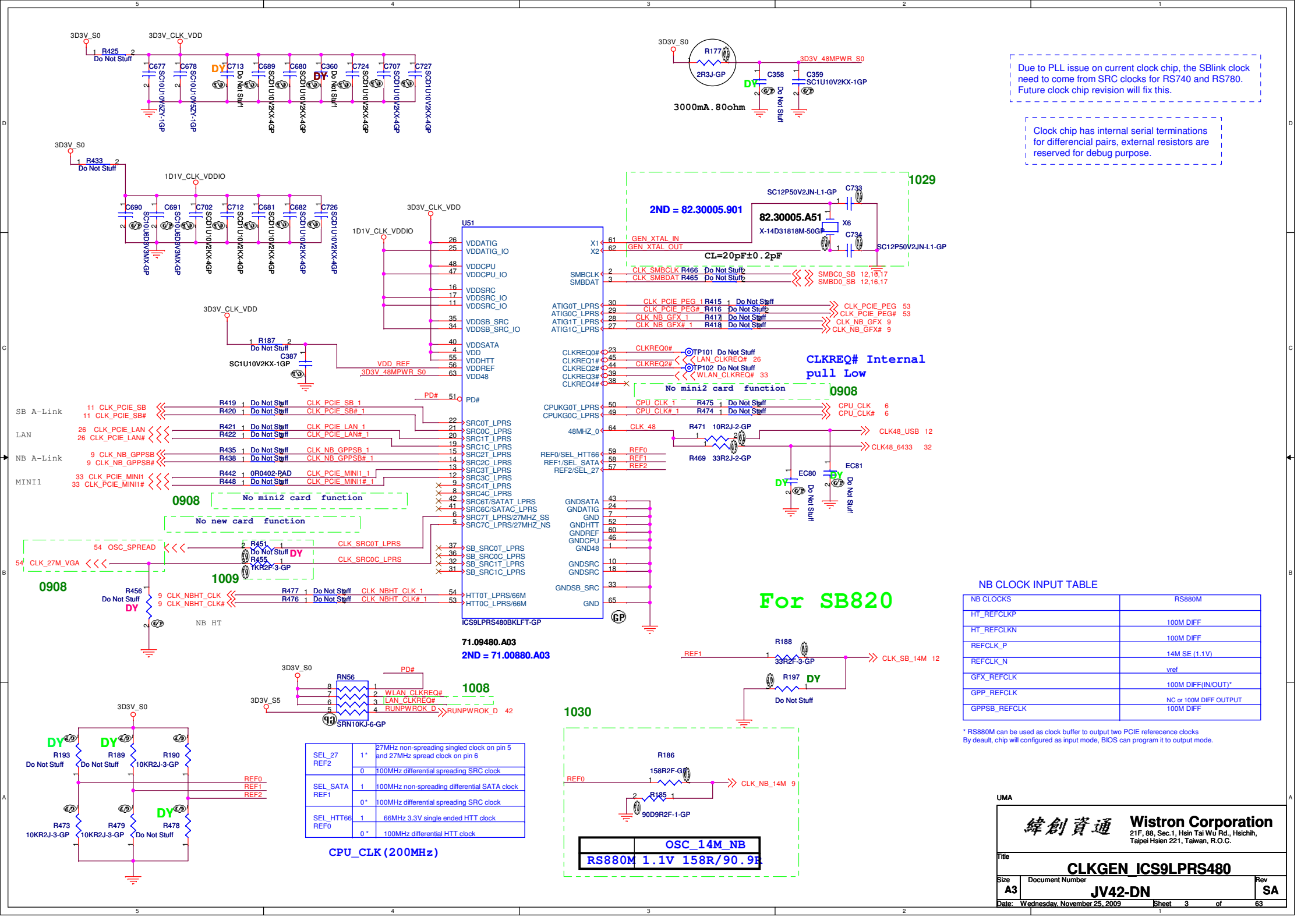
The pads are connected by a central vertical line, indicating the signal path through the layers.

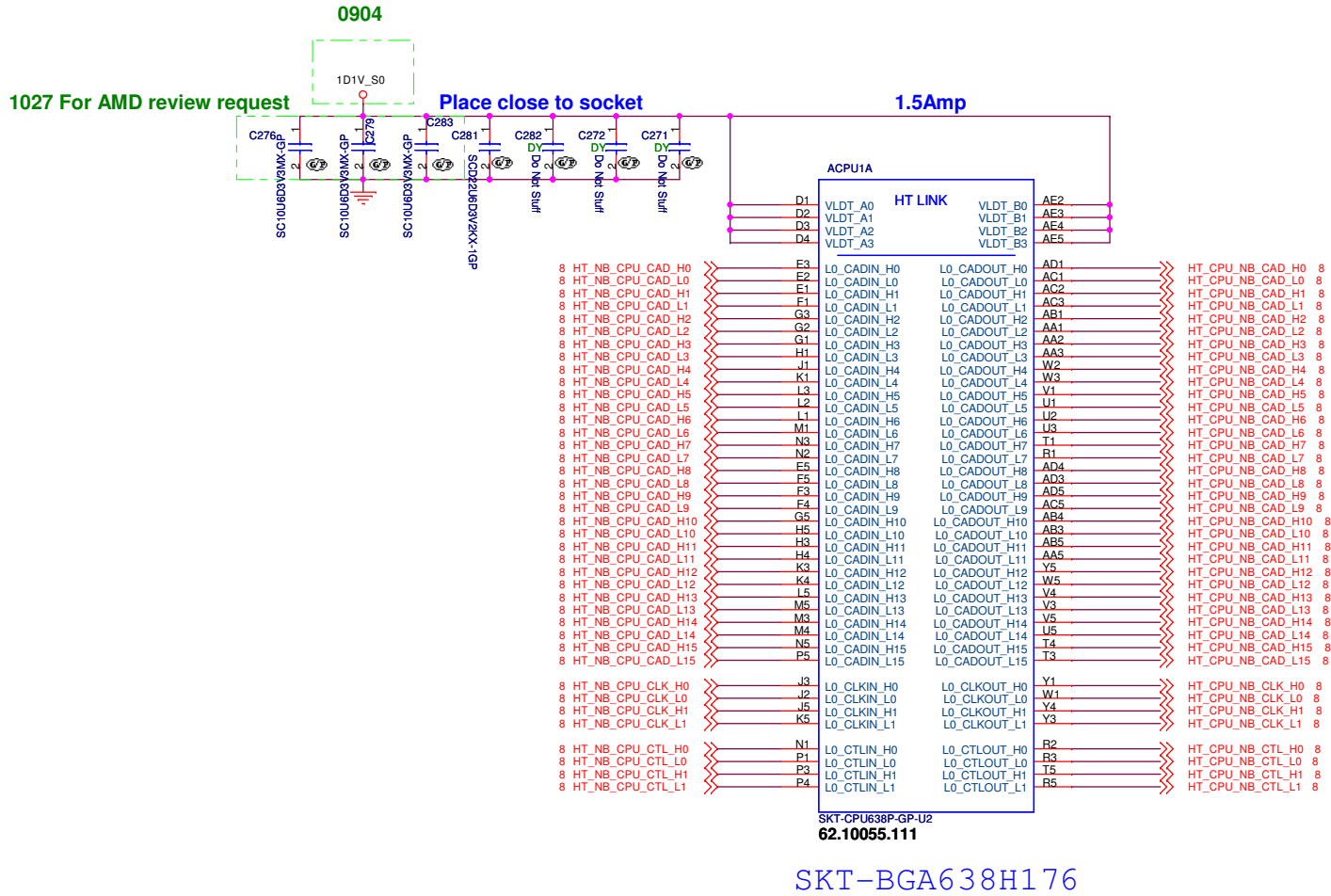




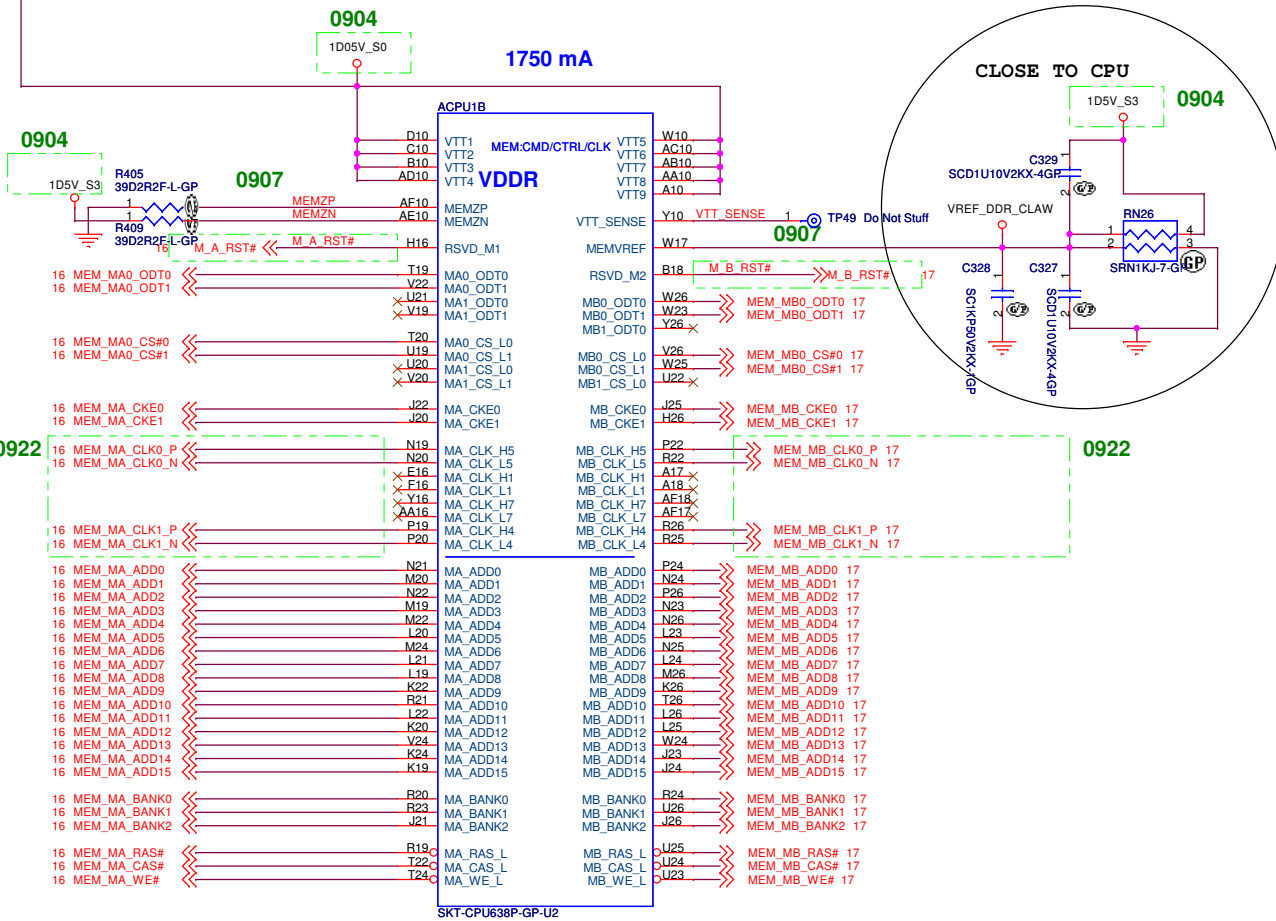
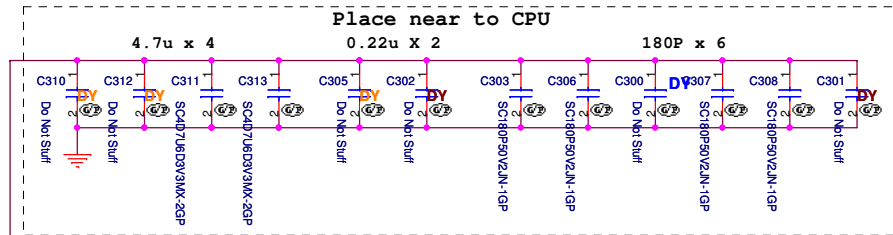
UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
History			
Size	Document Number		Rev
A3	JV42-DN		SA
Date:	Thursday, November 05, 2009	Sheet	2 of 63

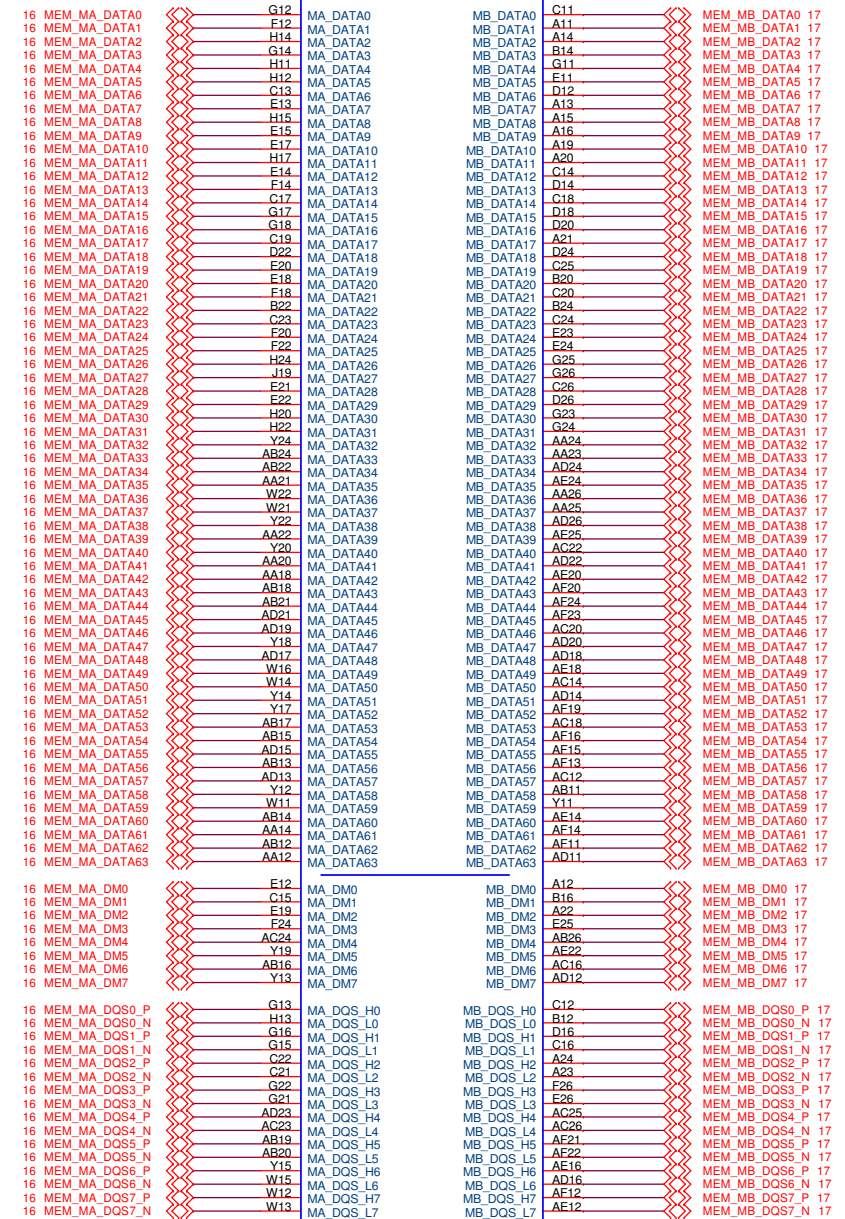




UMA



62.10055.111

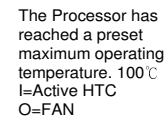


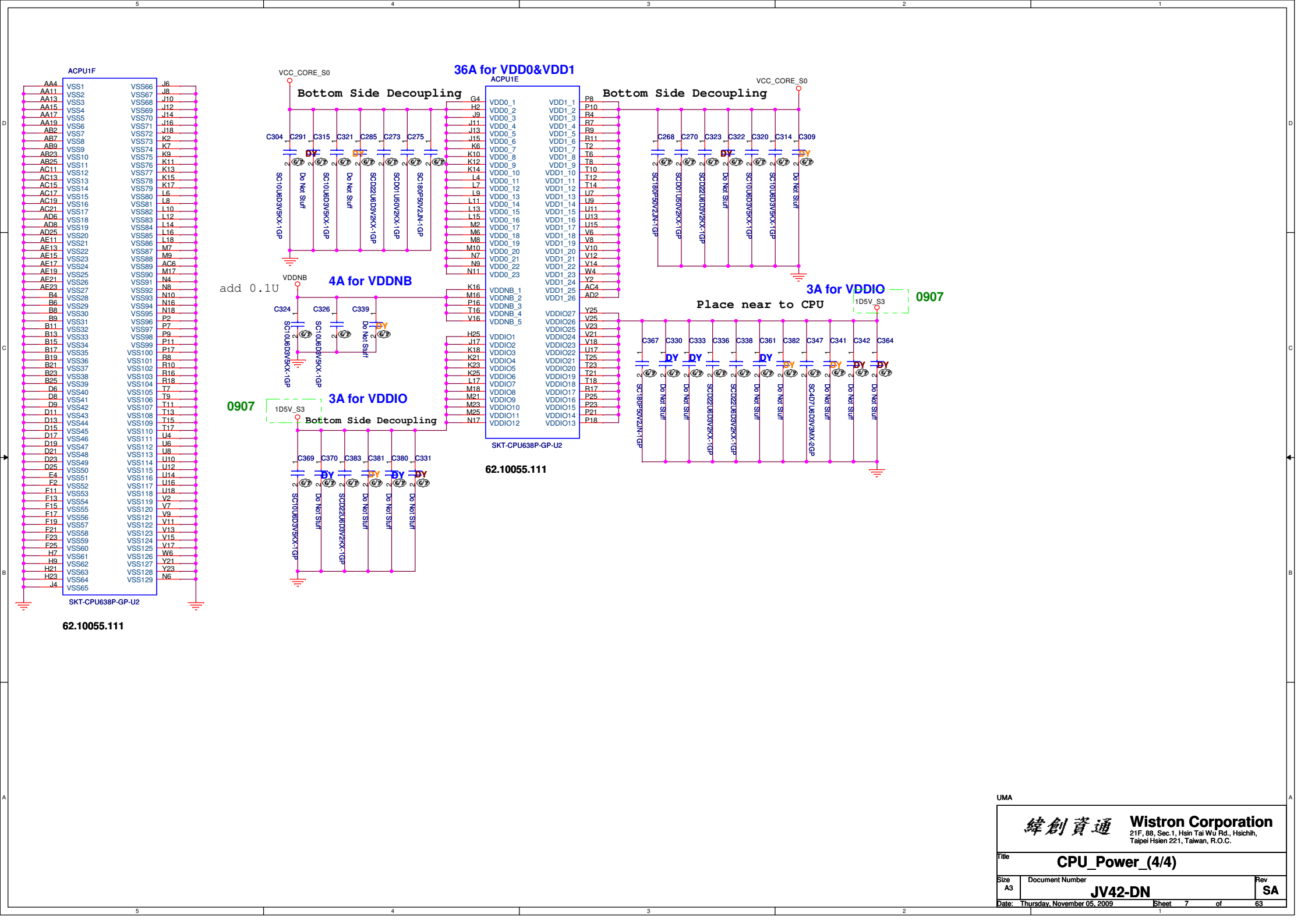
62.10055.111

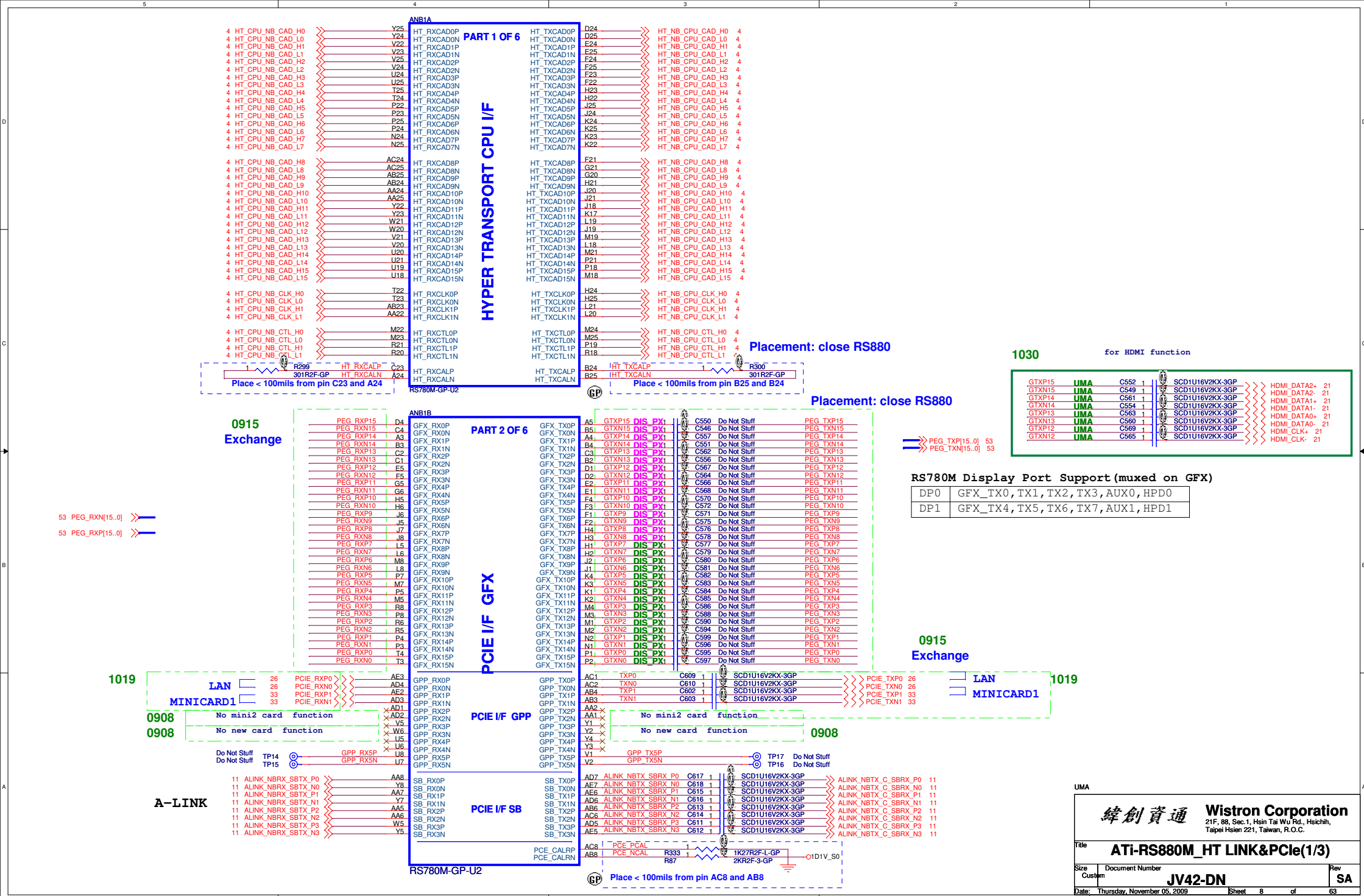
UMA

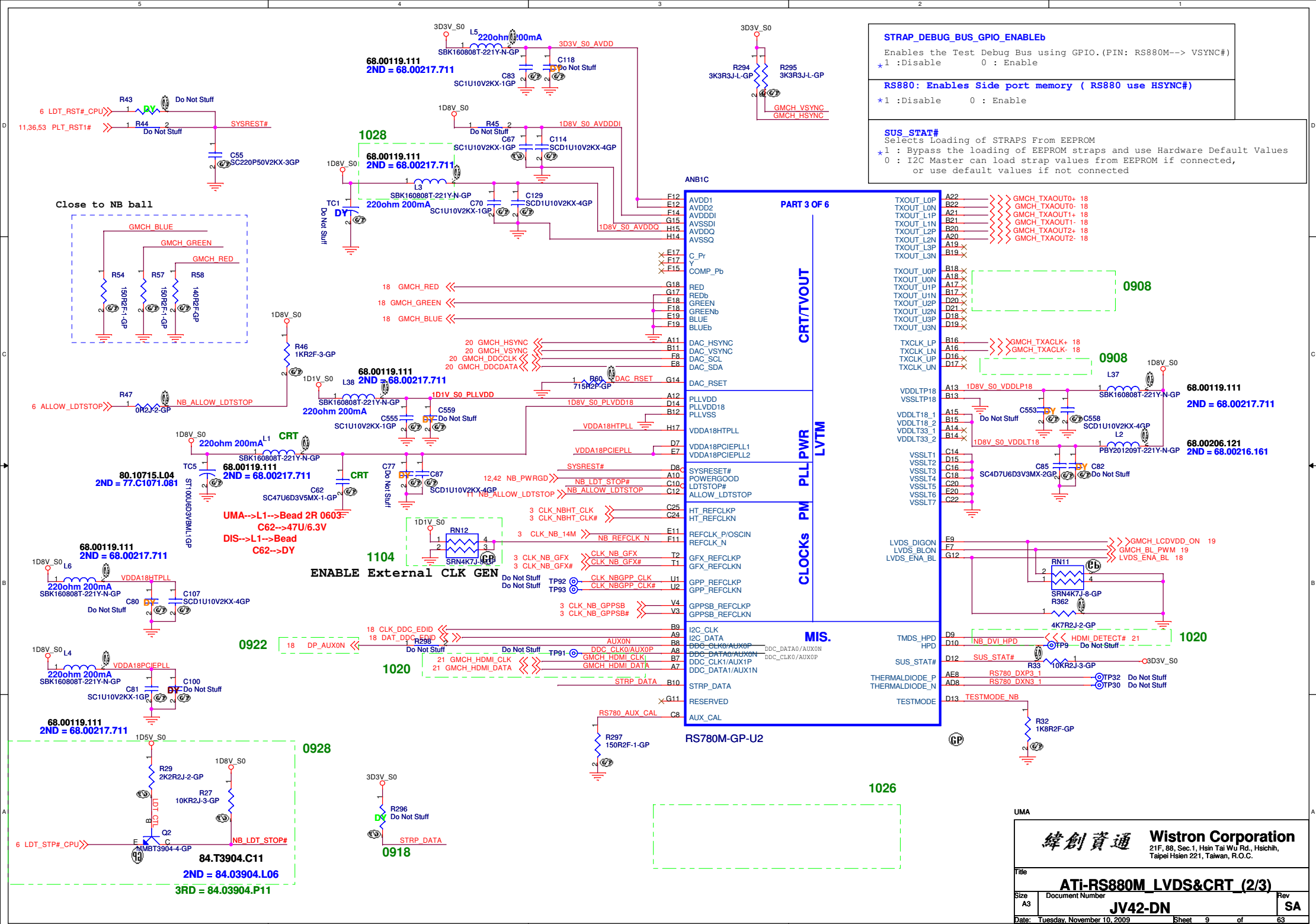
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU DDR (2/4)		
Size	Document Number	Rev
A3	JV42-DN	SA
Date: Thursday, November 05, 2009	Sheet 5 of 63	









1027 For AMD review request

0.6A per ANT Rev1.1, Page3

0.45A per ANT Rev1.1, Page3

80mil Width

1027 For AMD review request

PART 5/6

POWER

1103
10A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team

PART 6/6

GROUND

MEM_COMP_P and MEM_COMP_N trace
width >=10mils and 10mils spacing from
other Signals in X,Y,Z directions

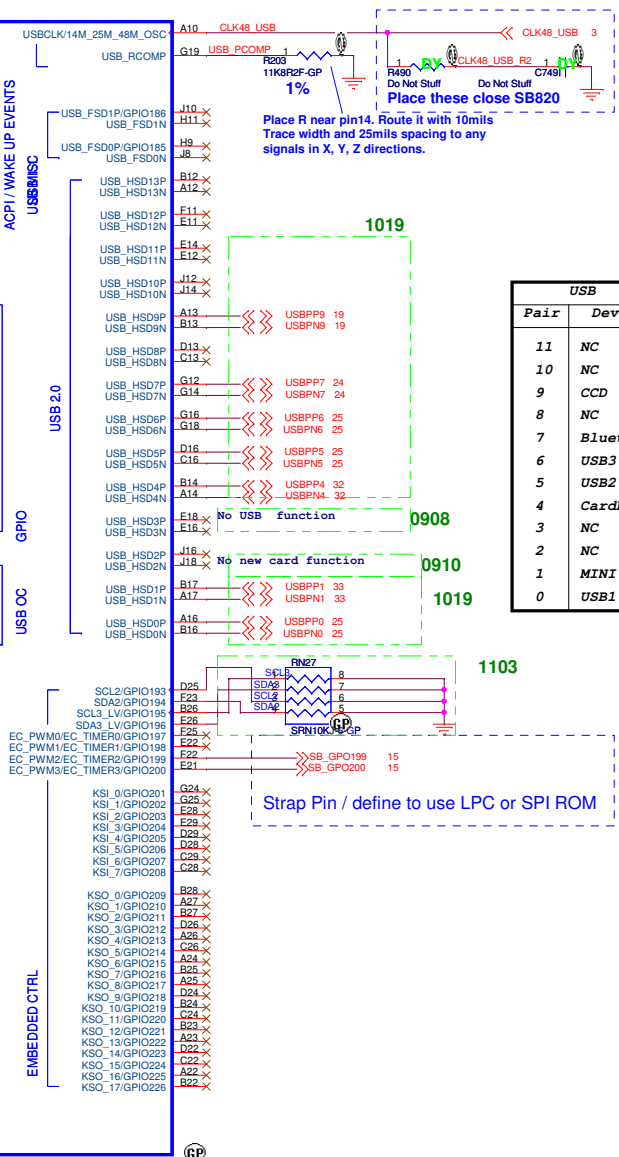
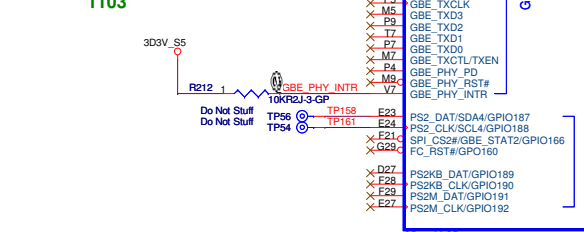
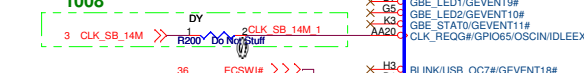
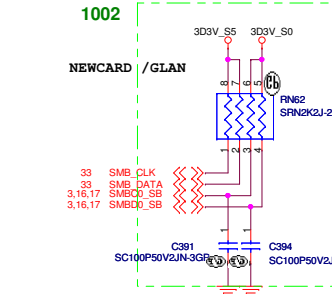
UMA

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

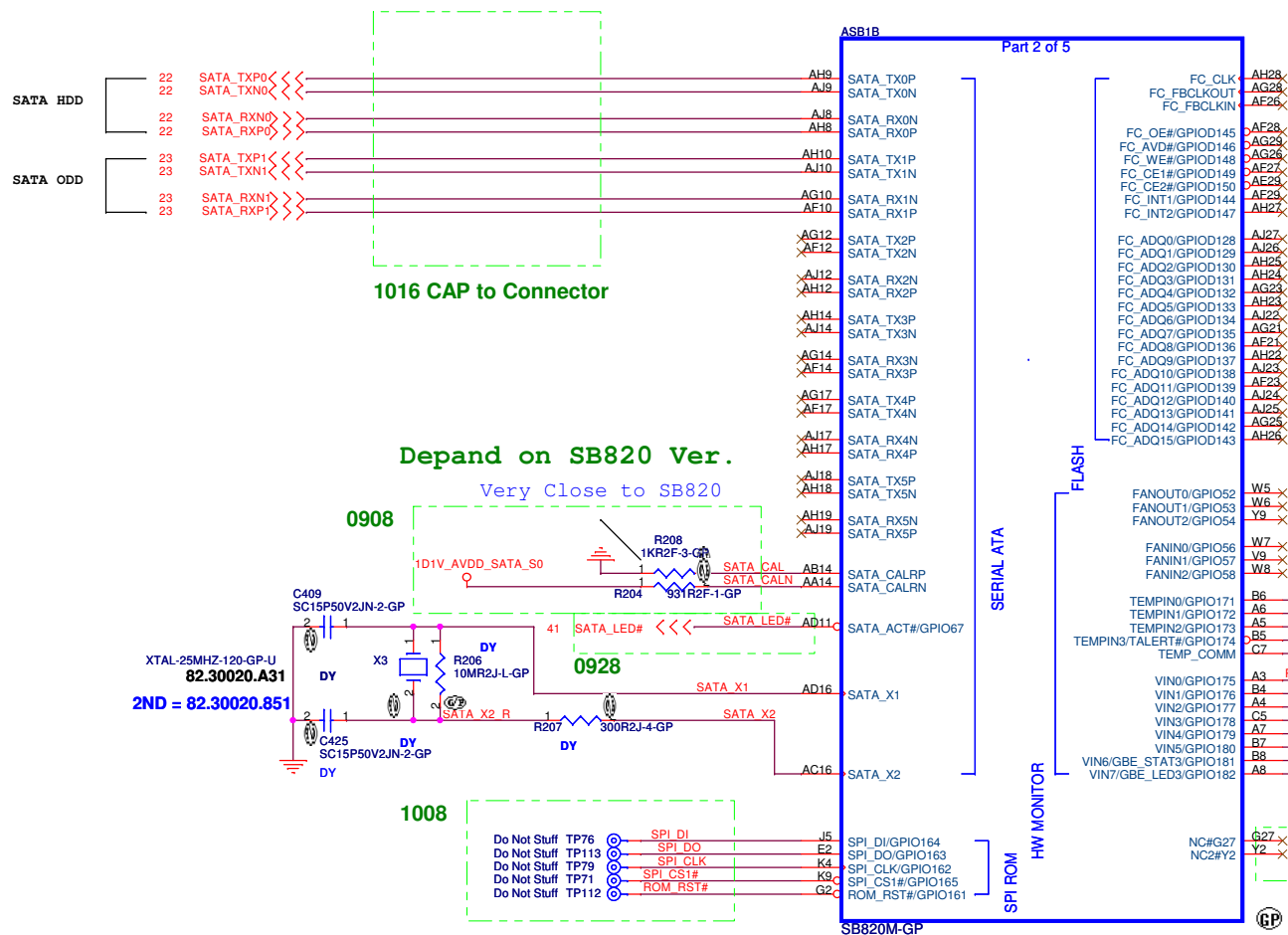
ATI-RS880M Side Port&PWR&GND(3/3)

JV42-DN

Date: Thursday, November 05, 2009 Sheet 10 of 63



USB	
Pair	Device
11	NC
10	NC
9	CCD
8	NC
7	Bluetooth
6	USB3
5	USB2
4	CardReader
3	NC
2	NC
1	MINI CARD
0	USB1



UMA

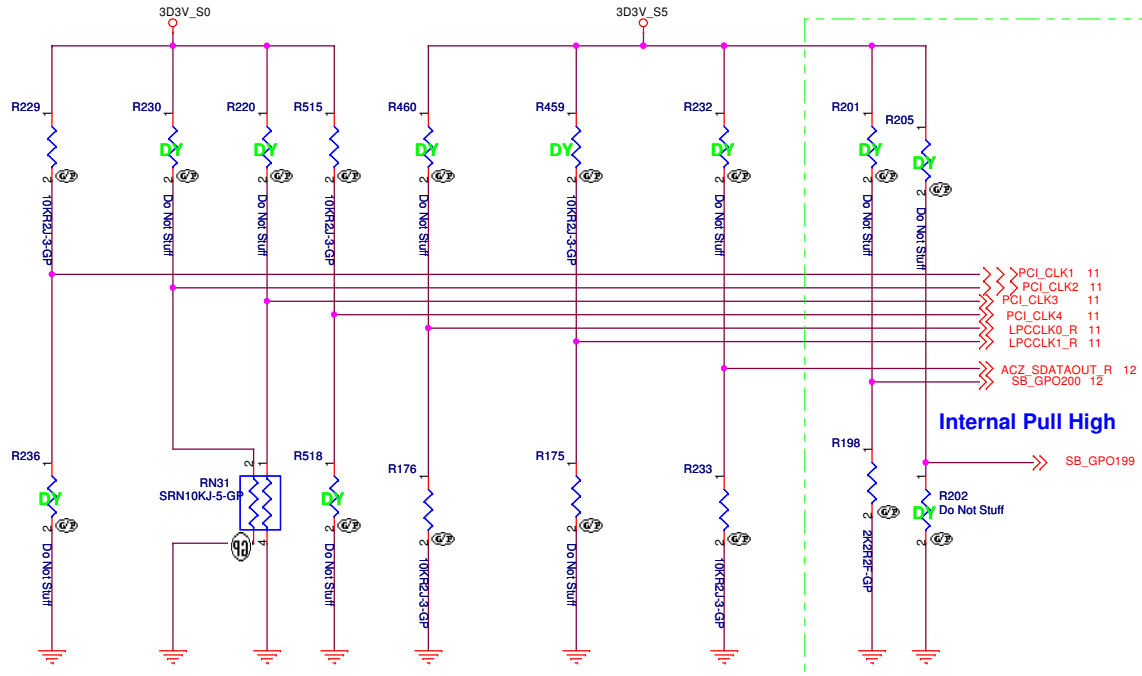
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			ATI-SB820 SATA-IDE (3/5)
Size	Document Number	Rev	SA
A3	JV42-DN		
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REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



1002

DEBUG STRAPS

Do Not Stuff	TP67	PCI_AD23	11
Do Not Stuff	TP70	PCI_AD24	11
Do Not Stuff	TP66	PCI_AD25	11
Do Not Stuff	TP77	PCI_AD26	11
Do Not Stuff	TP80	PCI_AD27	11
Do Not Stuff	TP110	PCI_AD28	11
Do Not Stuff	TP108	PCI_AD29	11
Do Not Stuff	TP111	PCI_AD30	11

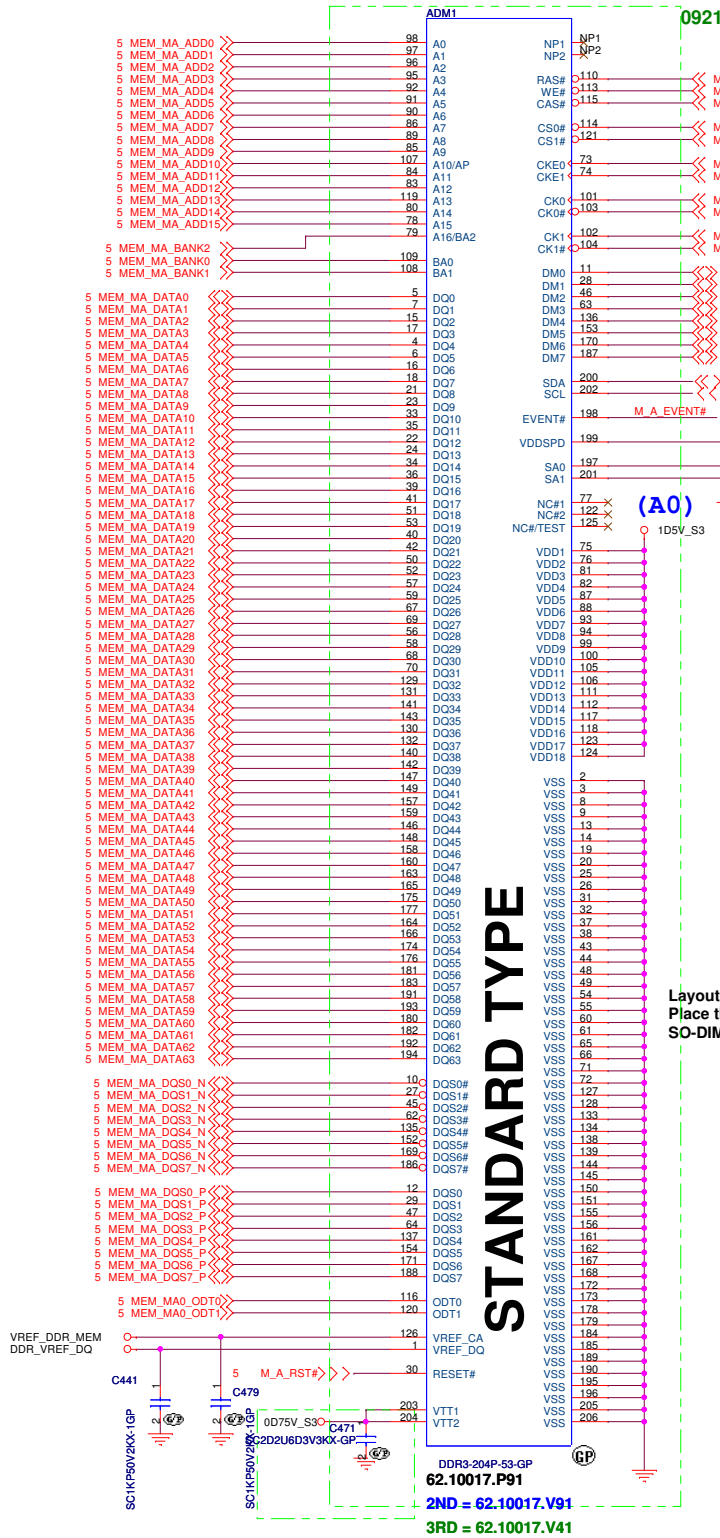
	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
PULL HIGH	ALLOW PCIe Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED DEFAULT	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM	
PULL LOW	FORCE PCIe Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM	

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

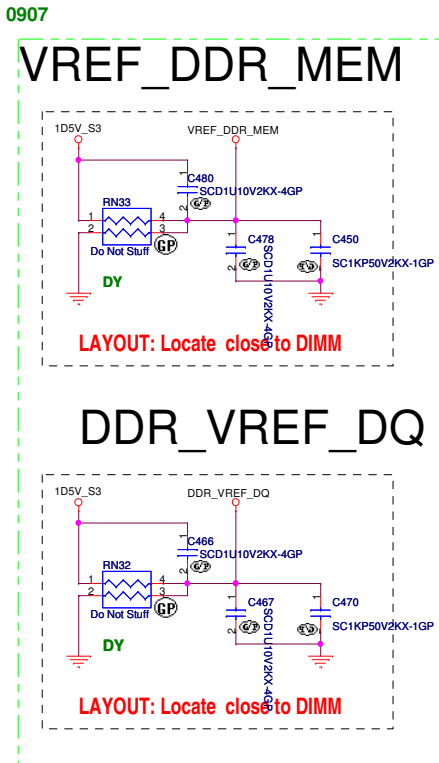
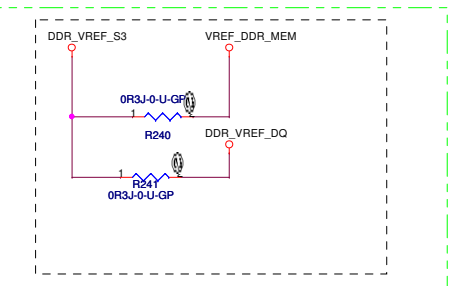
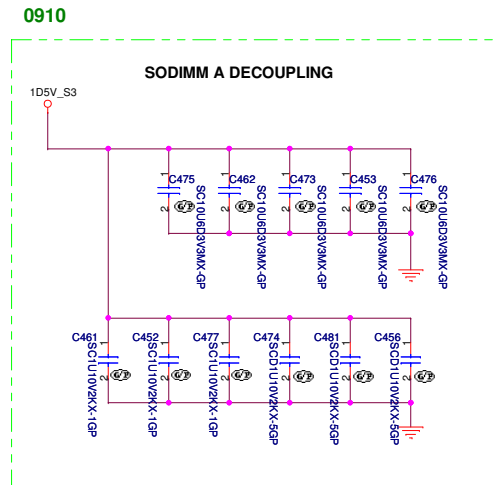
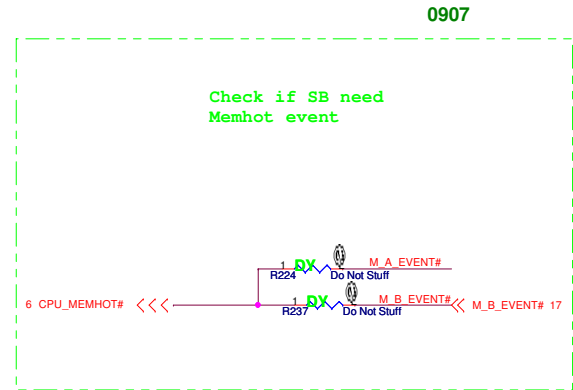
UMA

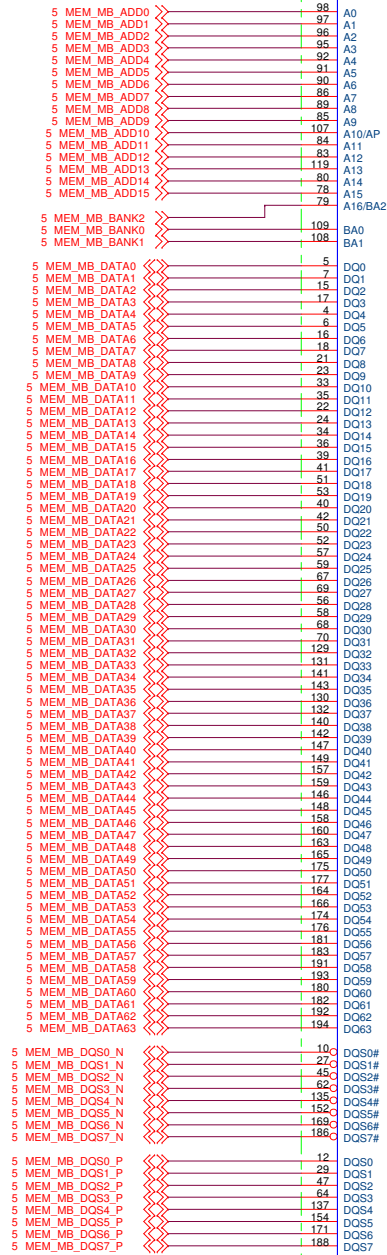
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ATI-SB820 STRAPPING (5/5)		
Size	Document Number	Rev	SA
A3	JV42-DN		
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Layout Note:
Place these Caps near
SO-DIMMA.





REVERSE TYPE

DDR3-204P-99-GP
62.10017.V01
2ND = 62.10017.V31
3RD = 62.10017.M41

0921

1029

0910

SODIMM B DECOUPLING

VREF_DDR_MEM
DDR_VREF_DQ

C437
SC1K50V20X-1GP

0924

C449
SC1K50V20X-1GP

0D75V_S3
C448
2D2U6D3V3KX-GP

VREF_CA
VREF_DQ

RESET#

VTT1
VTT2

GP

GP

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UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

DDRIII SO-DIMM SKT 2

Size

Custom

Document Number

JV42-DN

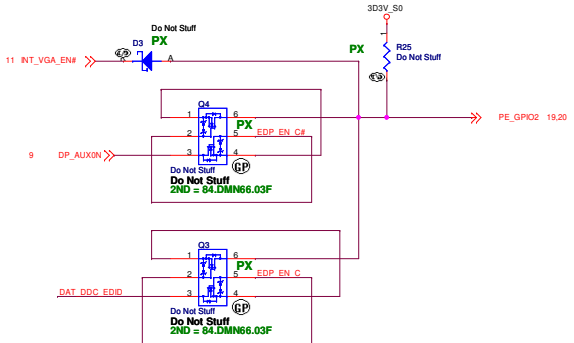
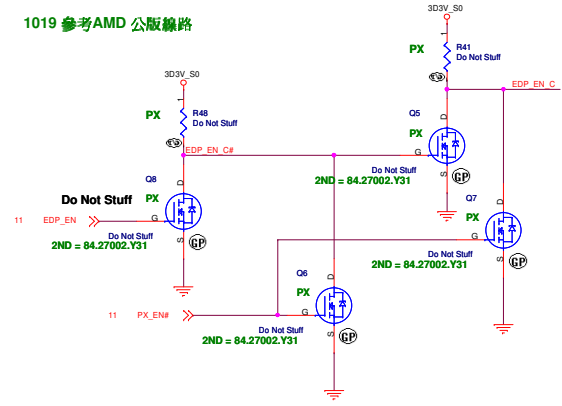
Rev

SA

Date: Thursday, November 05, 2009

Sheet 17 of 63

1019 參考AMD 公版線路



Truth Table

Function	SEL
A _N to N _B 1	L
A _N to N _B 2	H

CRT

$\bar{E}$	S	YA	YB	YC	YD	Function
H	X	H _i -Z	H _i -Z	H _i -Z	H _i -Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

EDID

Function Table

Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

H = HIGH Logic Level L = LOW Logic Level

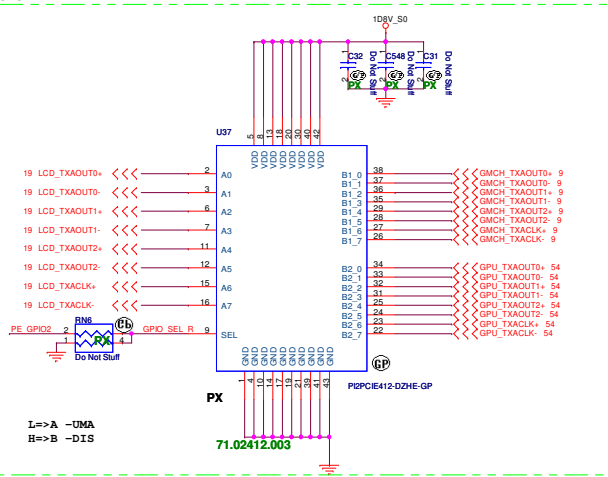
BLON_IN

Function Table

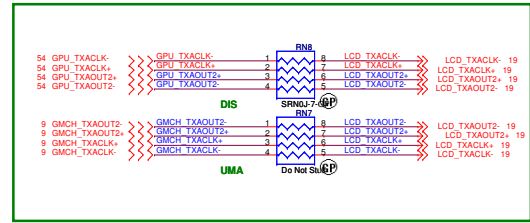
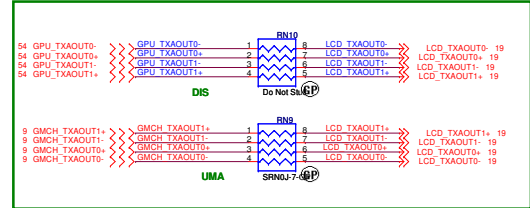
Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

H = HIGH Logic Level L = LOW Logic Level

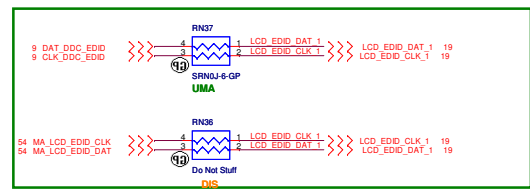
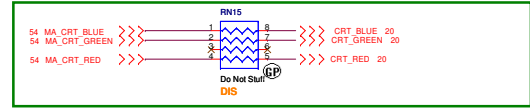
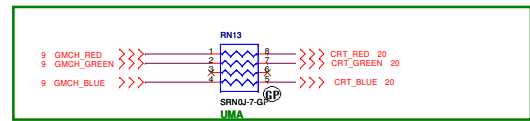
1023



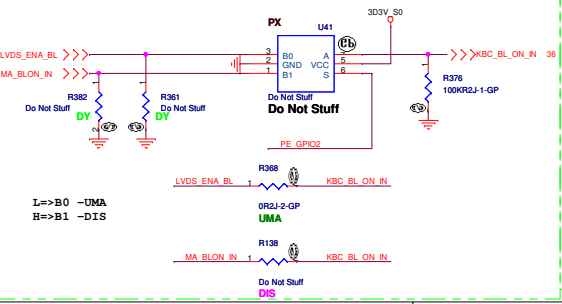
0924



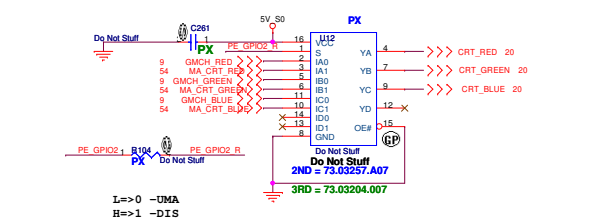
0924



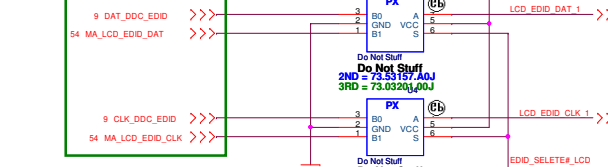
1026



0924



1023



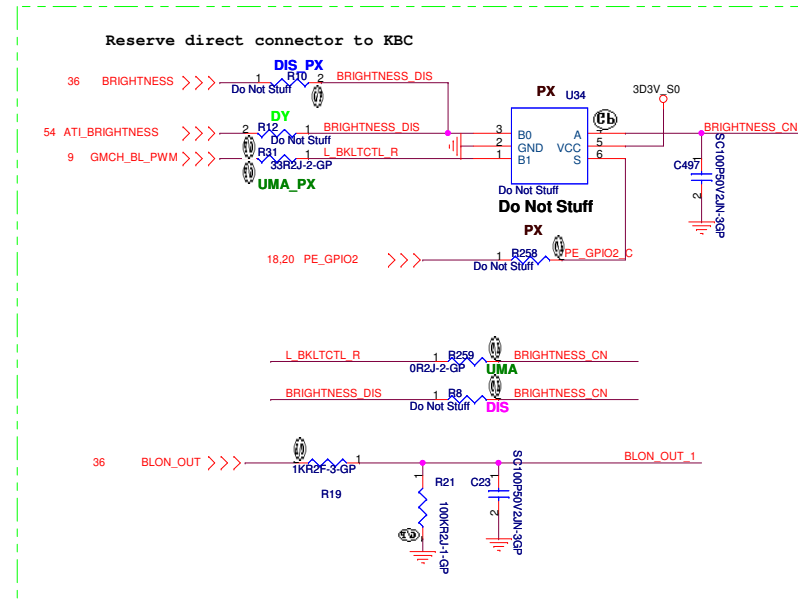
1016



0923

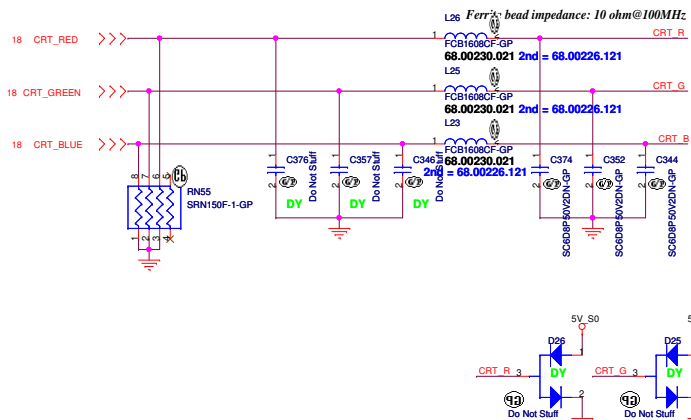


CCD Pin	
Pin	Symbol
1	CCD_PWD
2	USB-
3	USB+
4	GND
5	GND



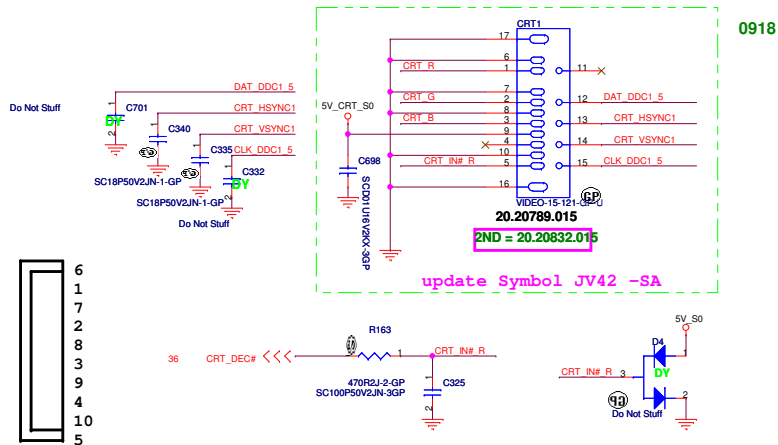
UMA			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.	
Title			
LCD CONN			
Size	Document Number		Rev
Custom	JV42-DN		SA
Date:	Thursday, November 05, 2009	Sheet	19 of 63

Layout Note:
Place these resistors
close to the CRT-out
connector



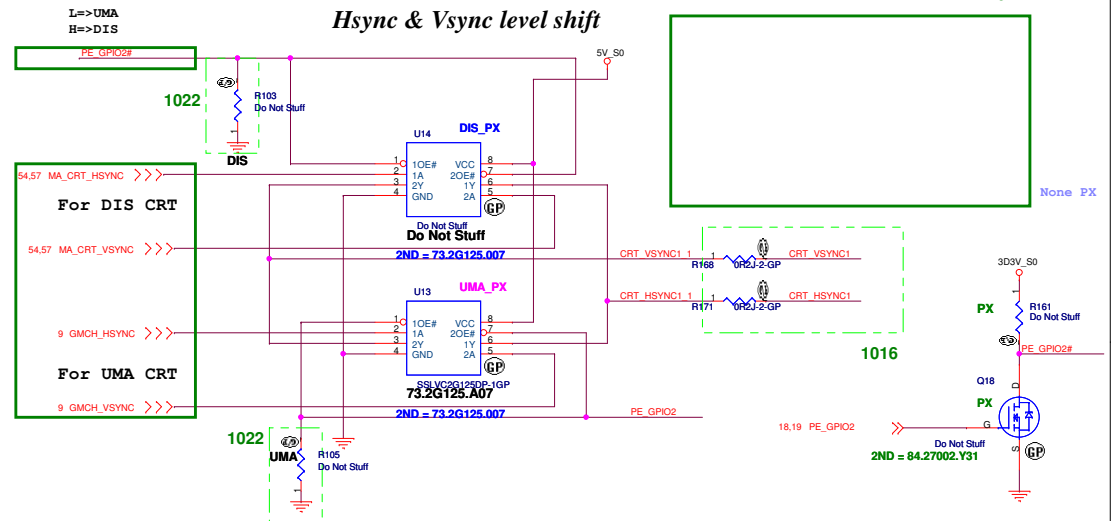
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR



update Symbol JV42 -SA

1012



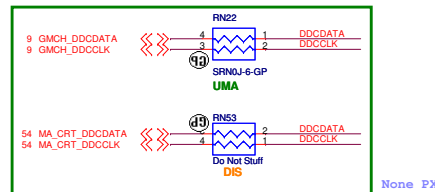
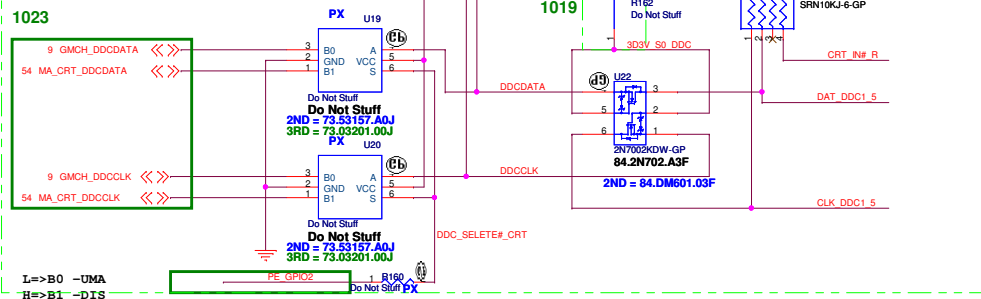
0924

DDC_CLK & DATA level shift

Function Table

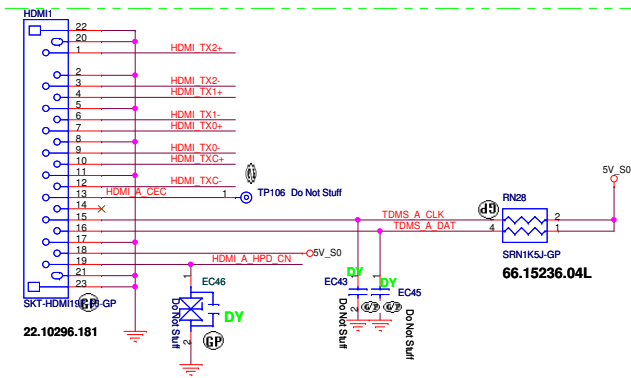
Input (S)	Function
L	B ₀ Connected to A
H	B ₁ Connected to A

H = HIGH Logic Level
L = LOW Logic Level



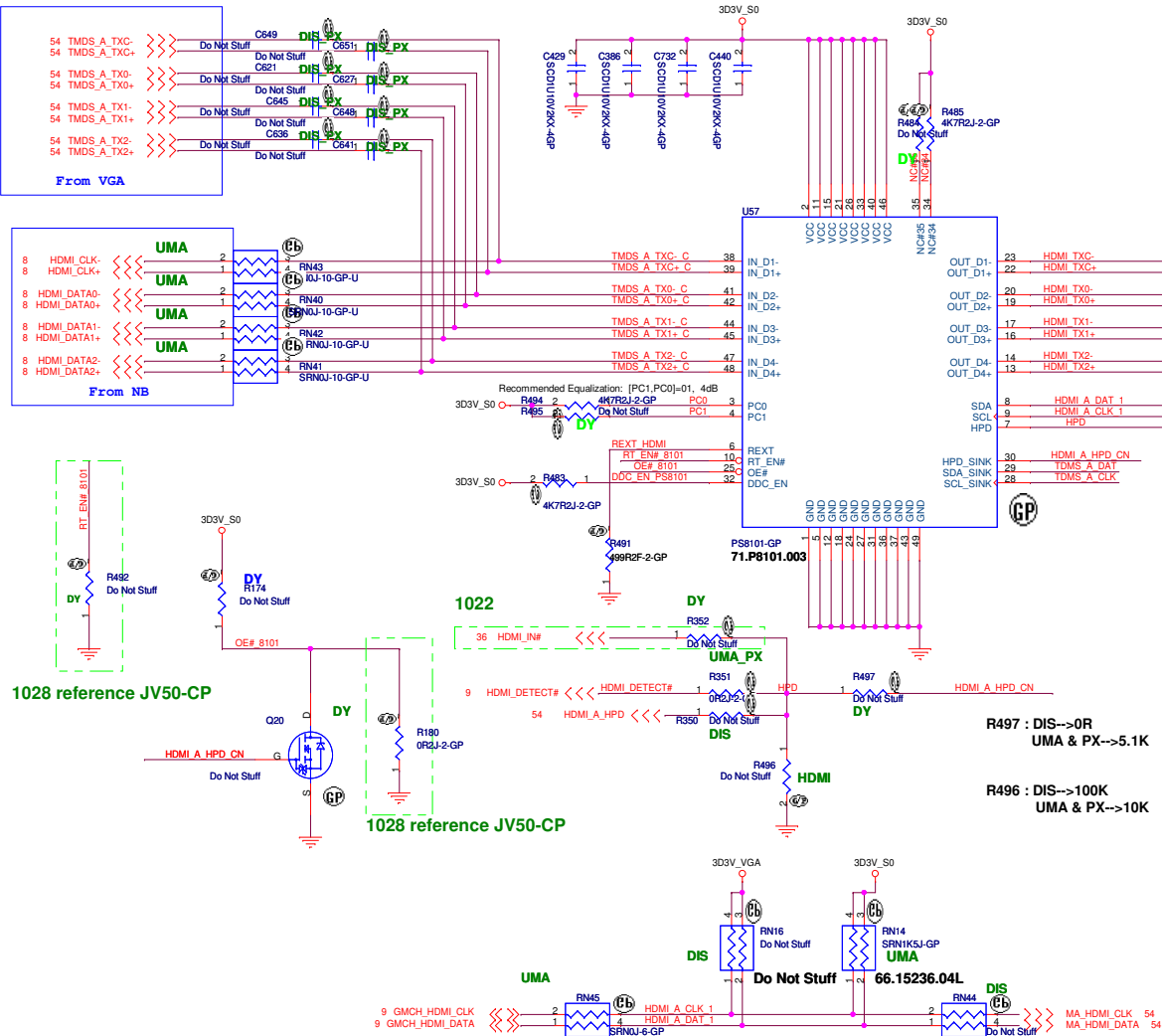
1026 for Layout request

1012



1026 for Layout request

1026 for Layout request

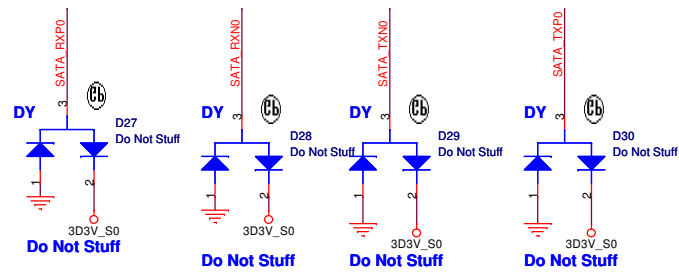
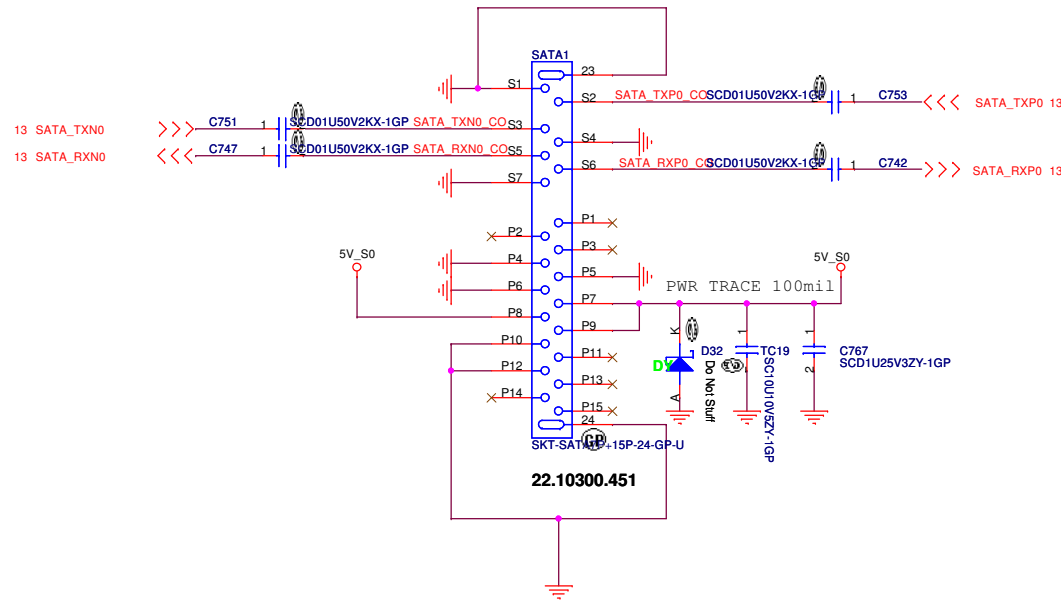


1028 reference JV50-CP

1028 reference JV50-CP

SATA Connector

0923



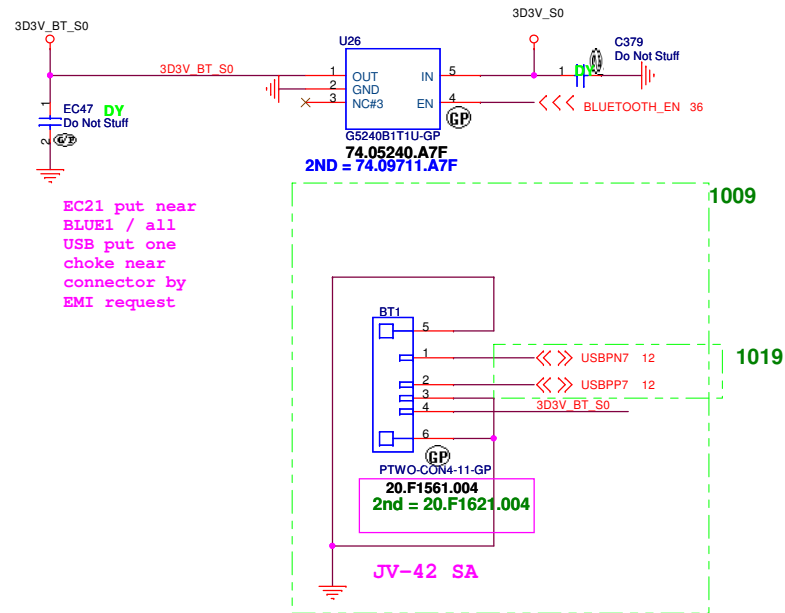
UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title HDD	
Size JV42-DN	Rev SA
Date: Thursday, November 05, 2009 Sheet 22 of 63	

######

BLUETOOTH MODULE

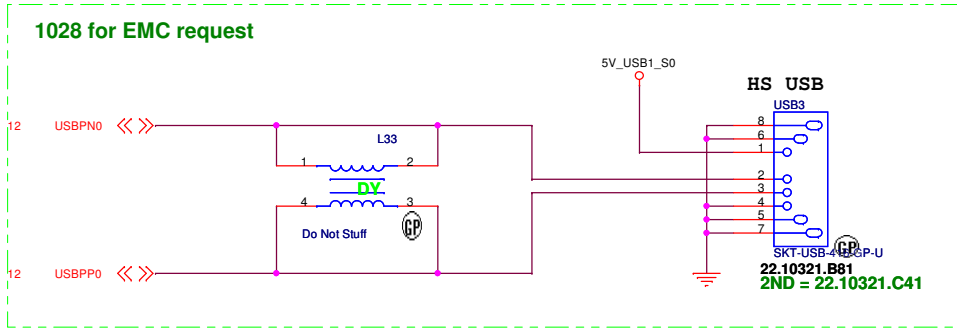
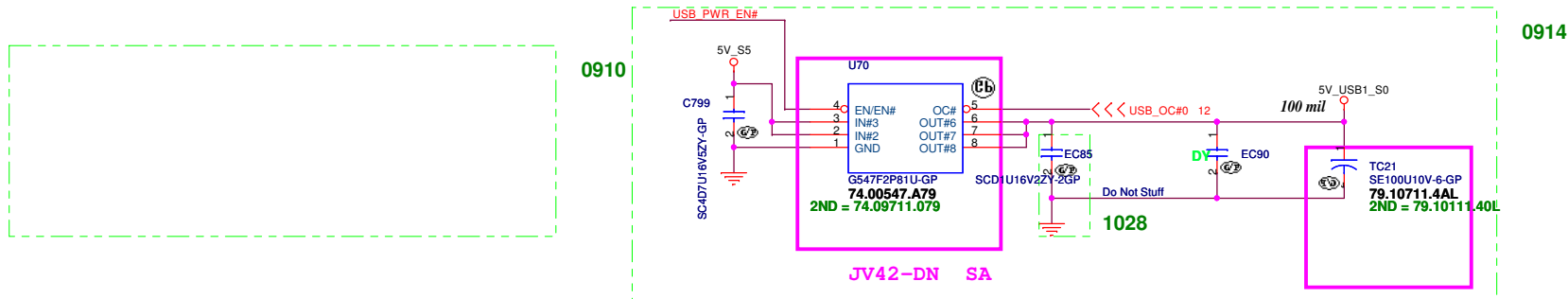
1.5A / High Active Voltage 2V



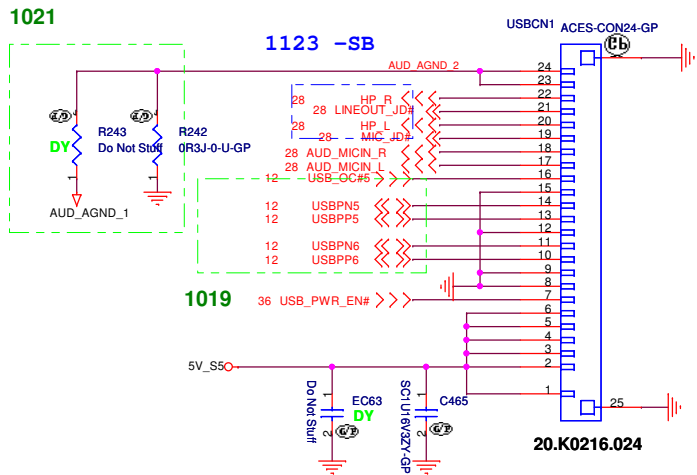
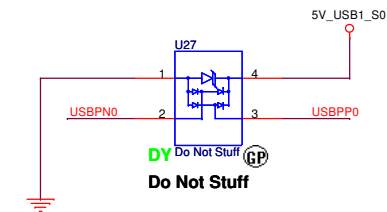
Pin 1 ->right side
20.D0197.104 Pin1 -> left side
change net sequence
can us JV50-CP Cable

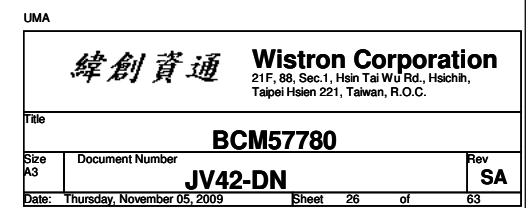
UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
BLUETOOTH			
Size	Document Number	Rev	SA
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Pin1 -> right side
 22.10218.T51 Pin1 -> left side (JV42-DN)
 change Net sequence





- 1

C



E

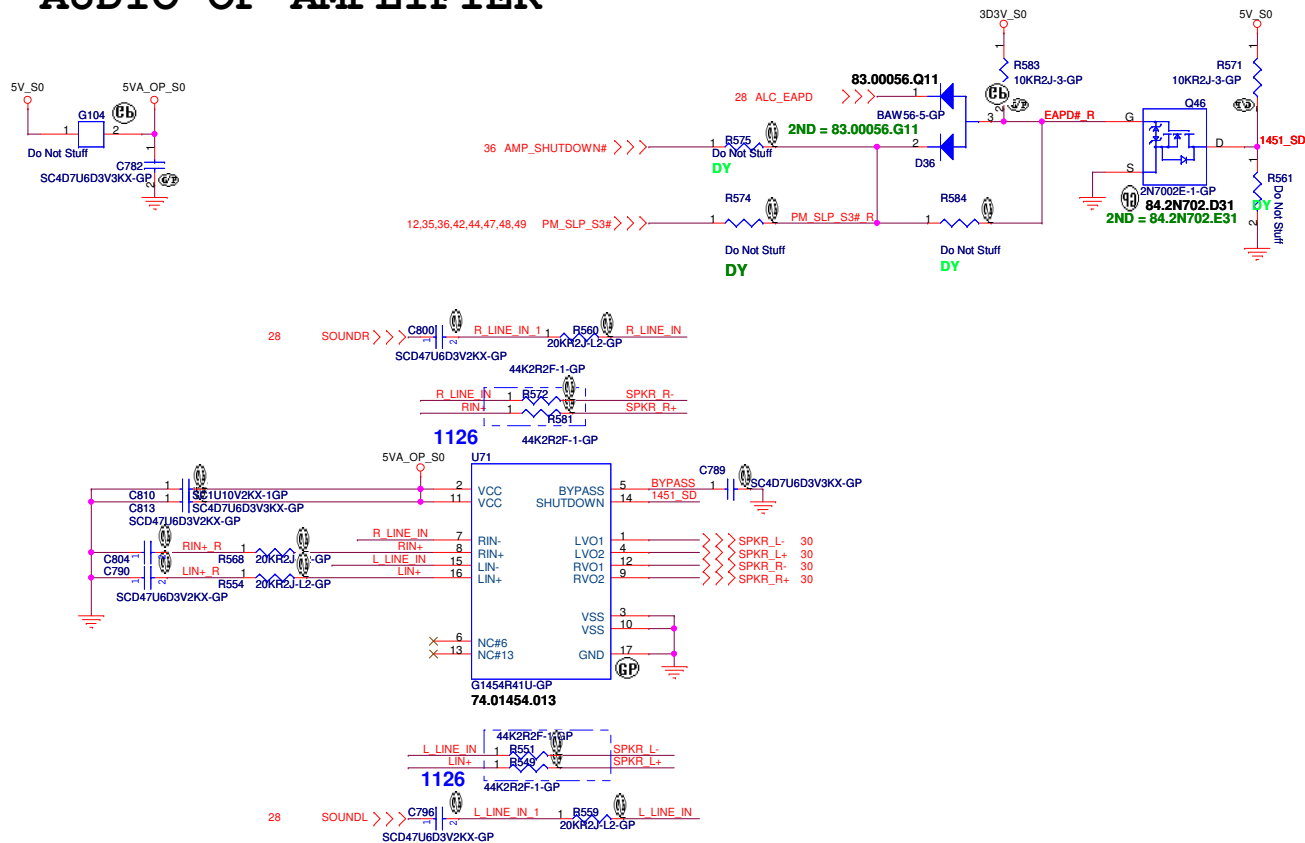
2ND = 22.10177.B51

4TH = 22.10177.B81



Rev	
S	

AUDIO OP AMPLIFIER



UMA

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

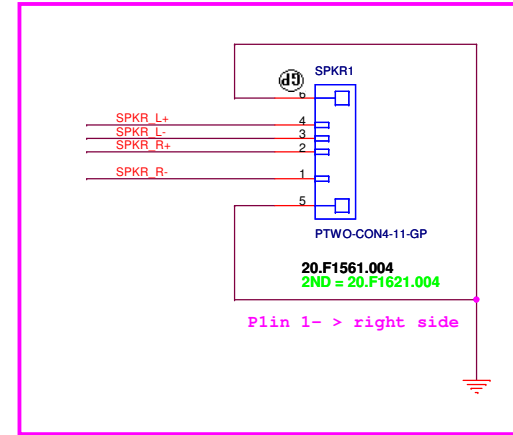
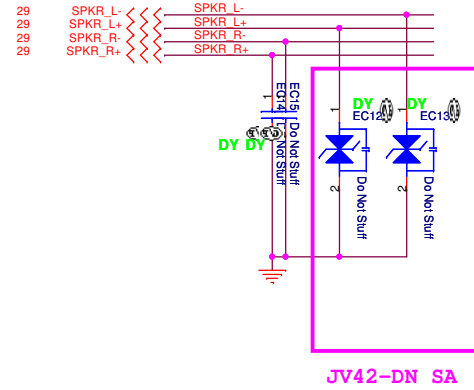
Title		
AUDIO AMP		
Size	Document Number	Rev
	JV42-DN	SA
Date:	Thursday, November 26, 2009	Sheet 29 of 63

Internal Speaker

0914



0910



JV42-DN SA

0910

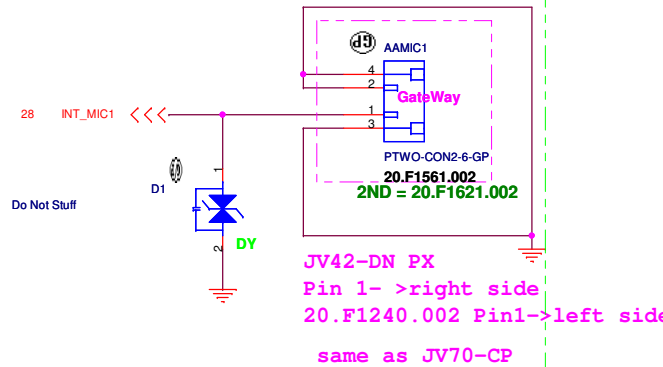
LINE OUT

0911



1016

Internal Mic



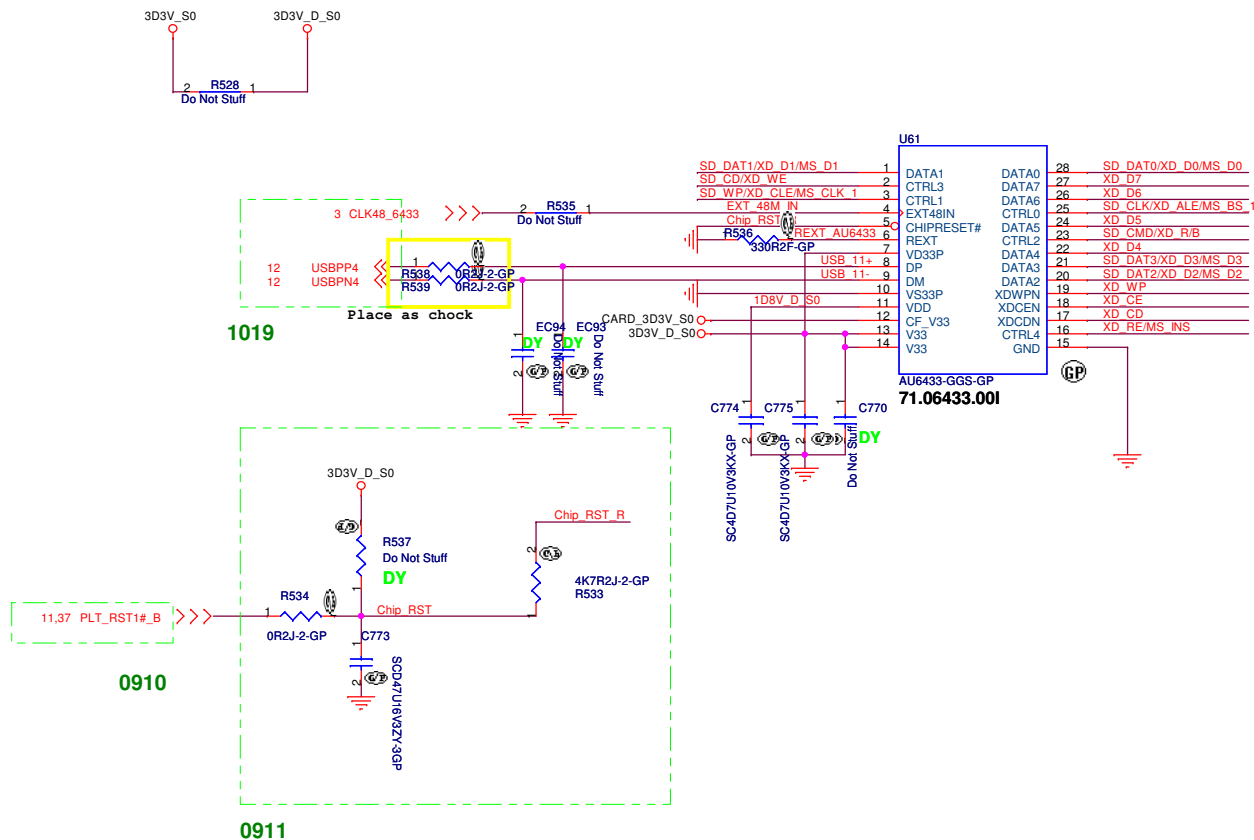
UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
AUDIO JACK			
Size	Document Number		Rev
	JV42-DN		SA
Date:	Thursday, November 05, 2009	Sheet 30 of	63

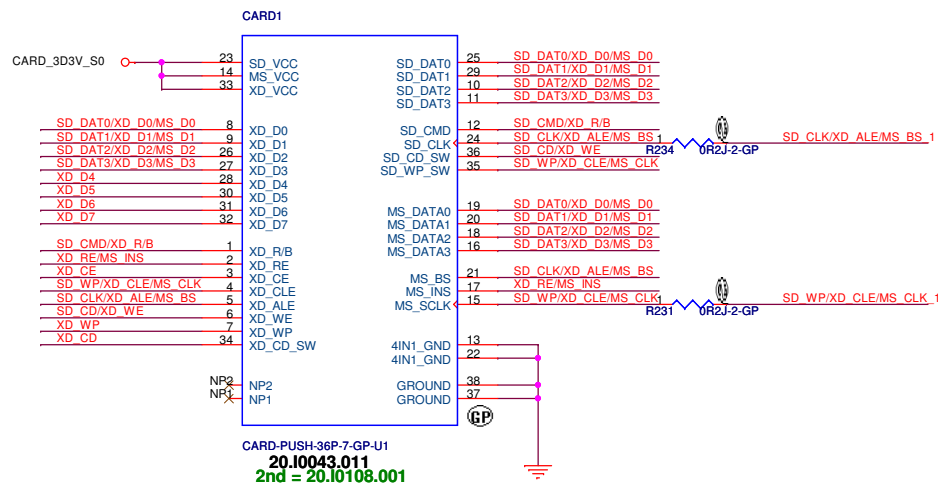
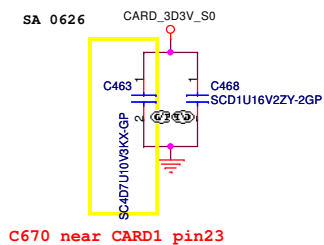
No Modem Function

UMA

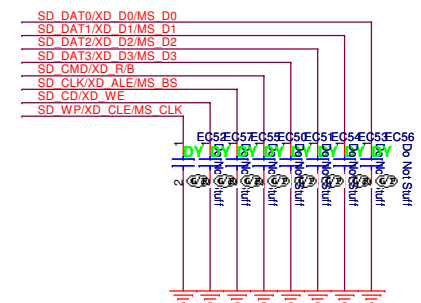
緯創資通Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
MDC		
Size	Document Number	Rev
	JV42-DN	SA
Date: Thursday, November 05, 2009		
Sheet 31 of 63		



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



EMI capacitor



UMA

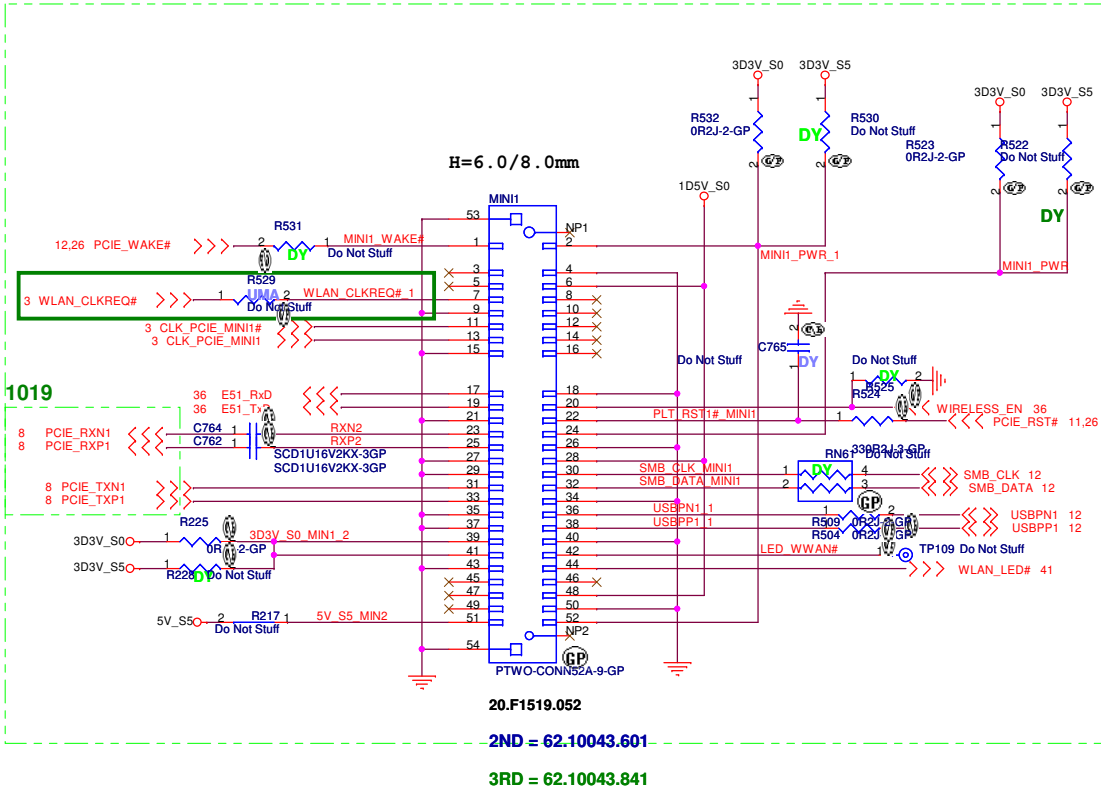
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

CARDREADER			
Size	Document Number	Rev	SA
	JV42-DN		
Date: Thursday, November 05, 2009	Sheet	32 of	63

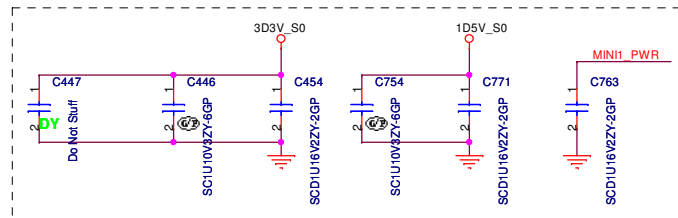
Mini Card Connector(WLAN)

No Mini Card Function (Robson2 and 3G)

0923



Place near MINI1



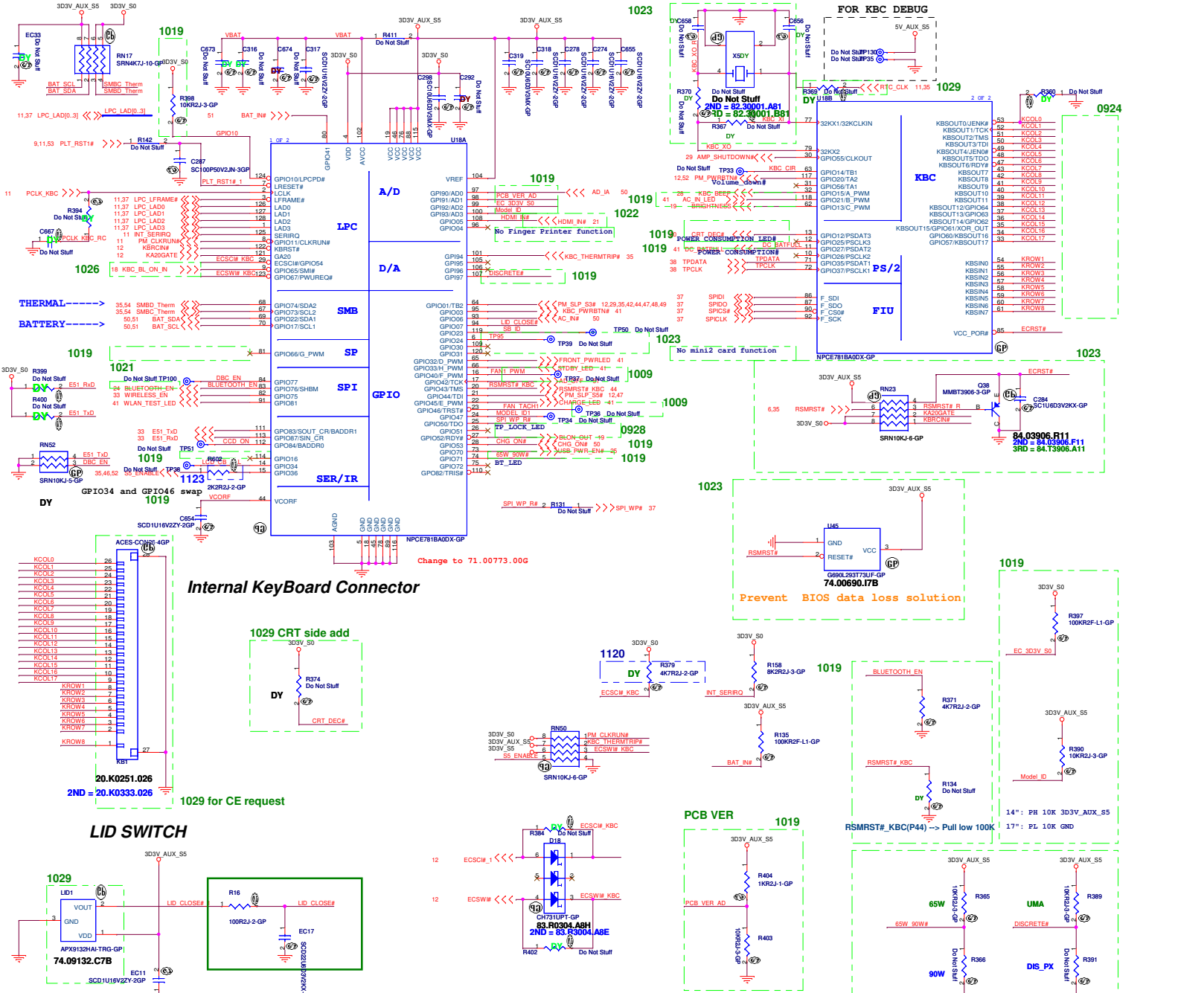
UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
MINI CARD			
Size	Document Number	Rev	
	JV42-DN	SA	
Date: Wednesday, November 18, 2009	Sheet	33	of 63

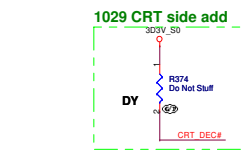
No NEWCARD Function

UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,		Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NEW CARD			
Size	Document Number		Rev
	JV42-DN		SA
Date: Thursday, November 05, 2009		Sheet	34 of 63

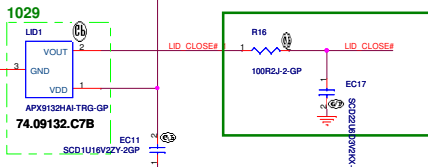


Internal KeyBoard Connector

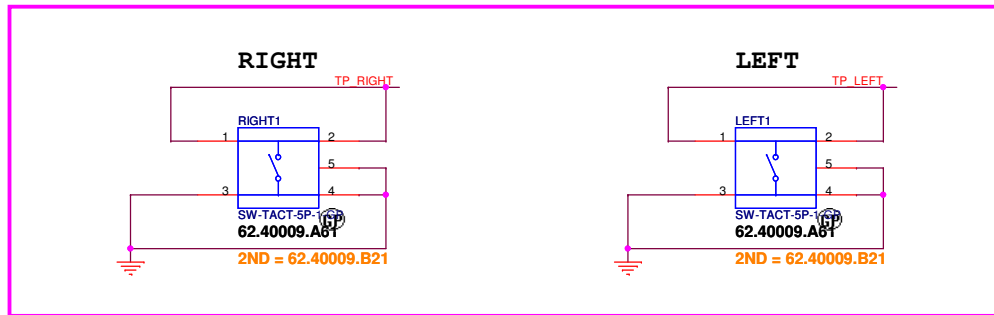
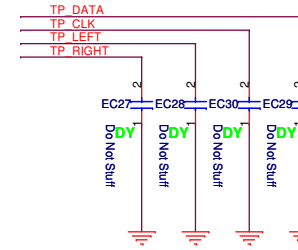
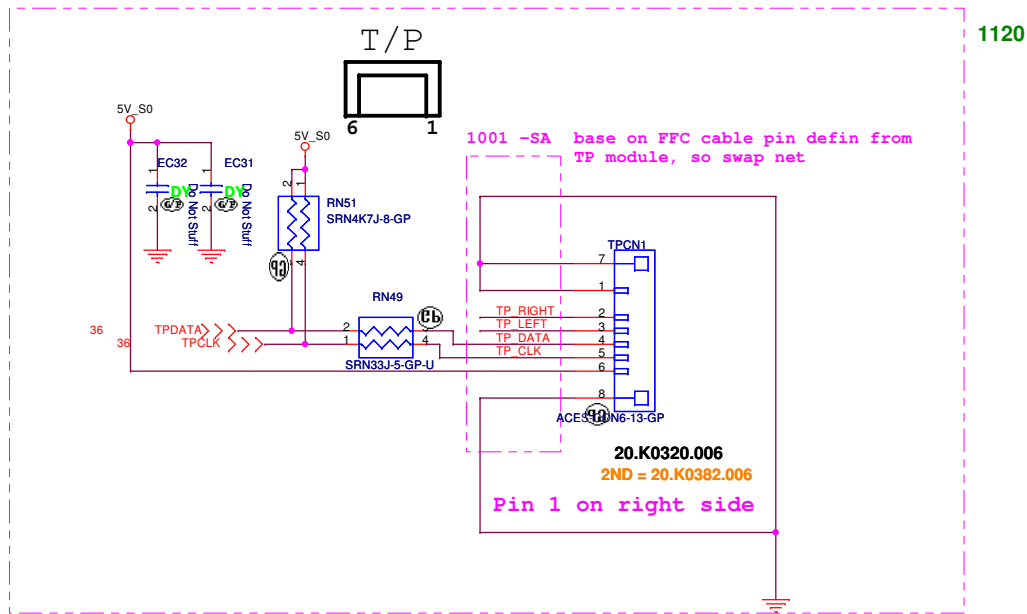


1029 for CE request

LID SWITCH



Pull-High Resistor (303V_AUX_55)	Voltage
1.0 K	3.0 V
2.0 K	2.75 V
3.0 K	2.54 V
4.7 K	2.24 V
6.98 K	1.94 V
8.2 K	1.81 V
10.0 K	1.65 V

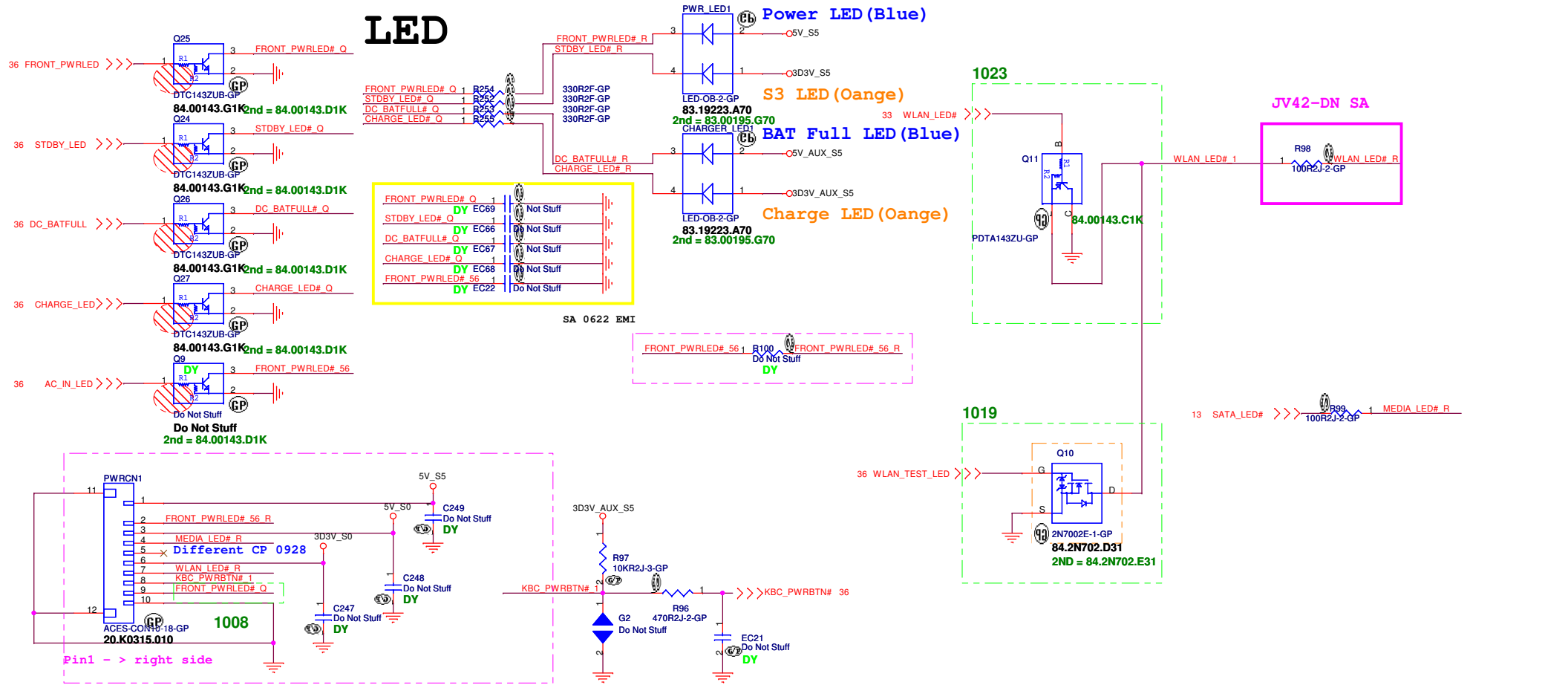


No Finger printer Function

UMA

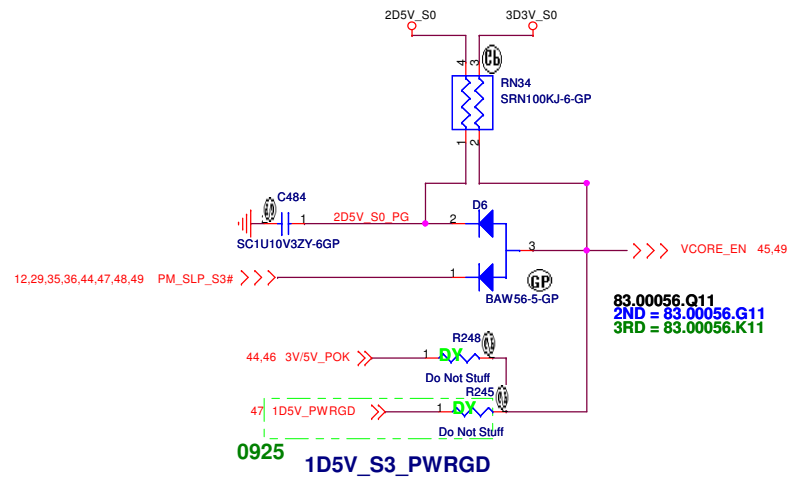
NONE BOARD

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
NONE BOARD			
Size	Document Number		Rev
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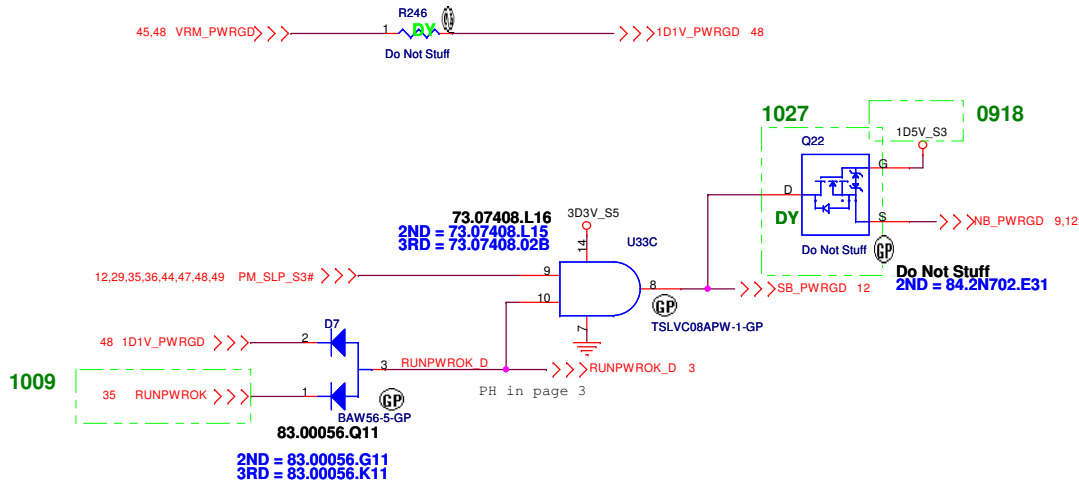


JV42-DN SA 0928

Pin 1	5V_S5	
Pin 2	(DY) FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	NC	
Pin 10	GND	

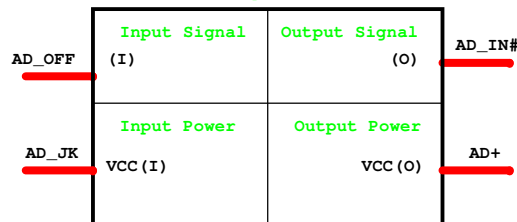


P/H @ 1D8V_S3 PAGE

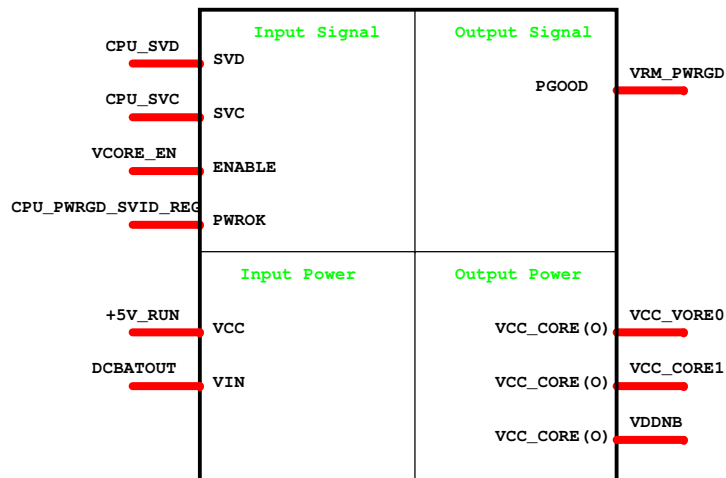


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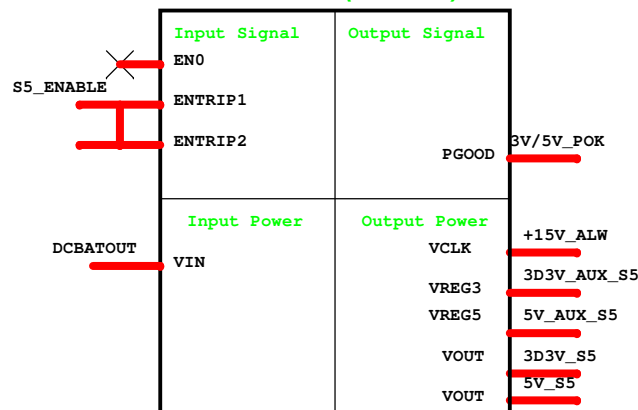
Adapter



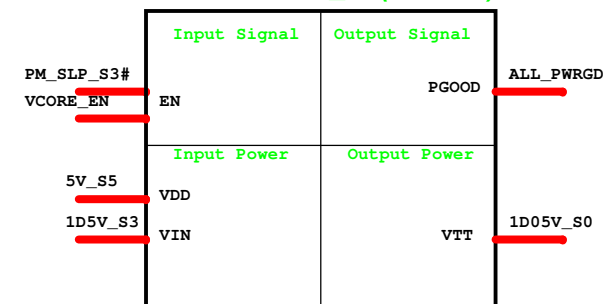
CPU_CORE ISL6265HRTZ



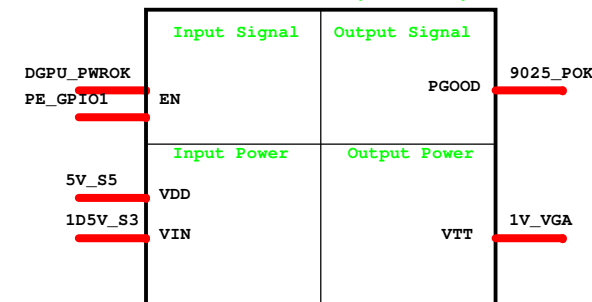
DCDC 5V/3D3V(RT8223)



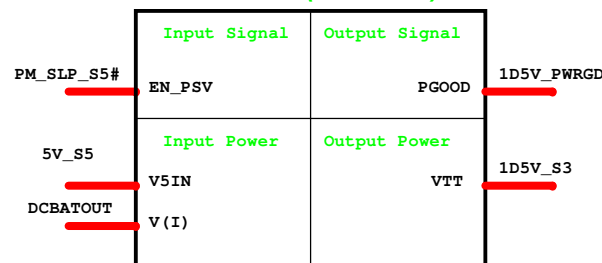
DCDC 1D05V_S0(RT9025)



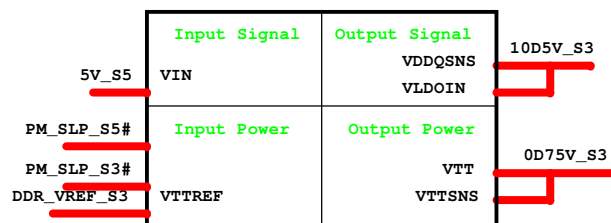
DCDC 1V_VGA(RT9025)



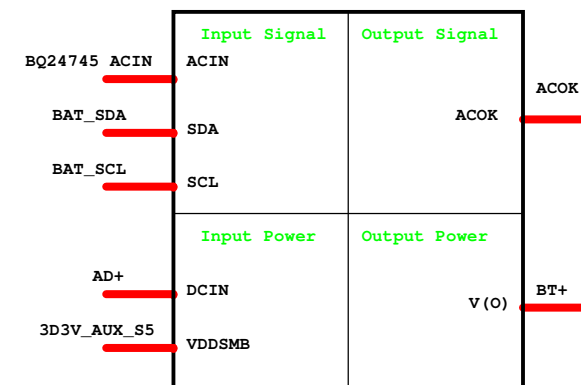
DCDC 1D5V(RT8209E)



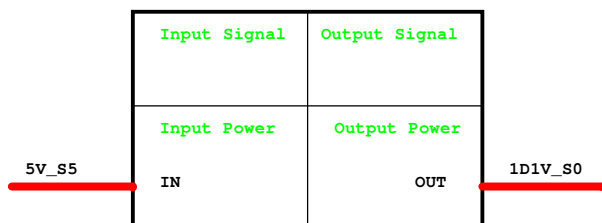
0D75V LDO RT9026



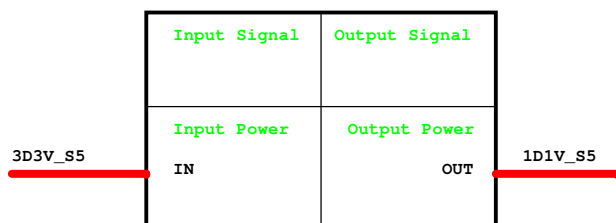
CHARGER BQ24745



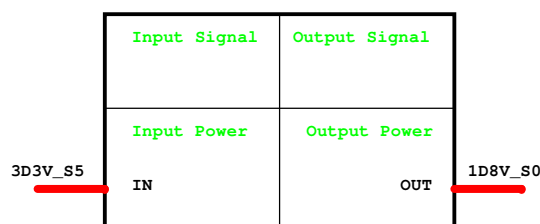
1D1V LDO RT8209E



1D1V LDO RT9025



1D8V LDO RT8015A



UMA

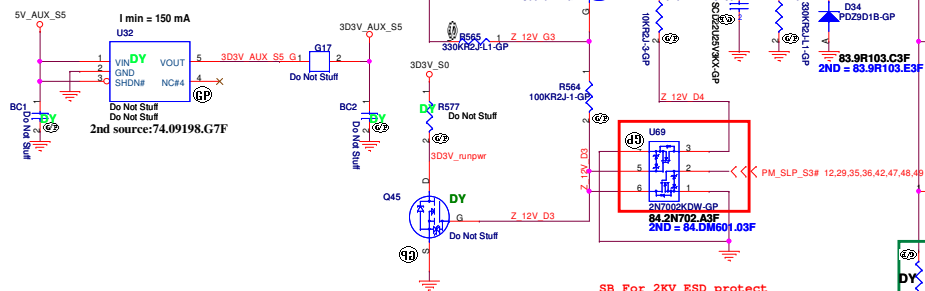
緯創資通 Wistron Corporation
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Title			Power Block Diagram	
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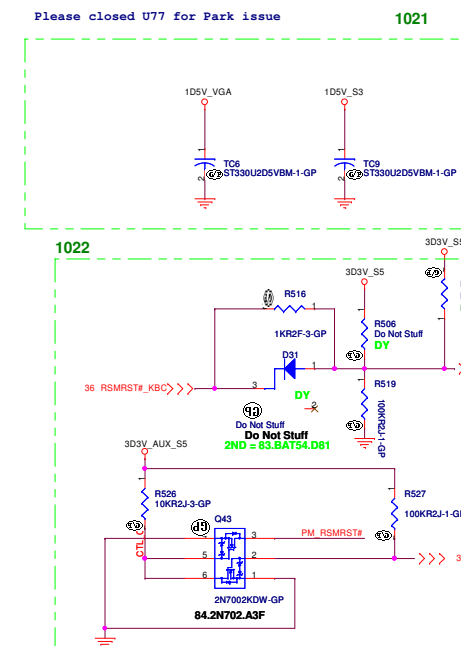
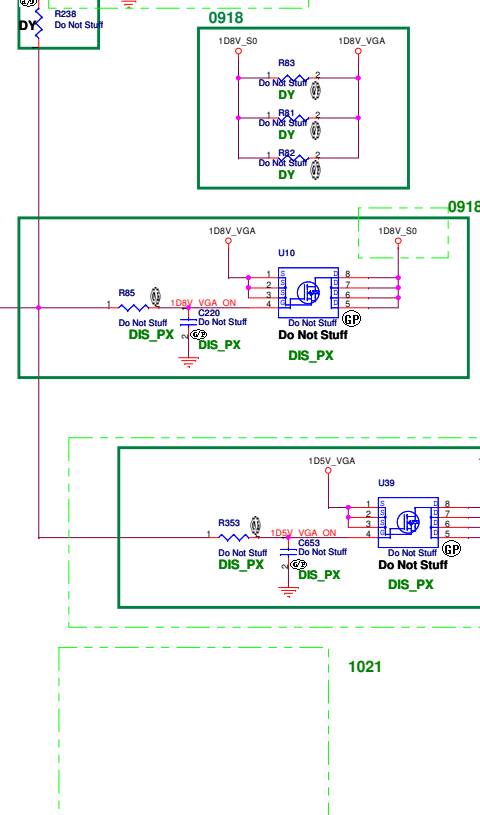
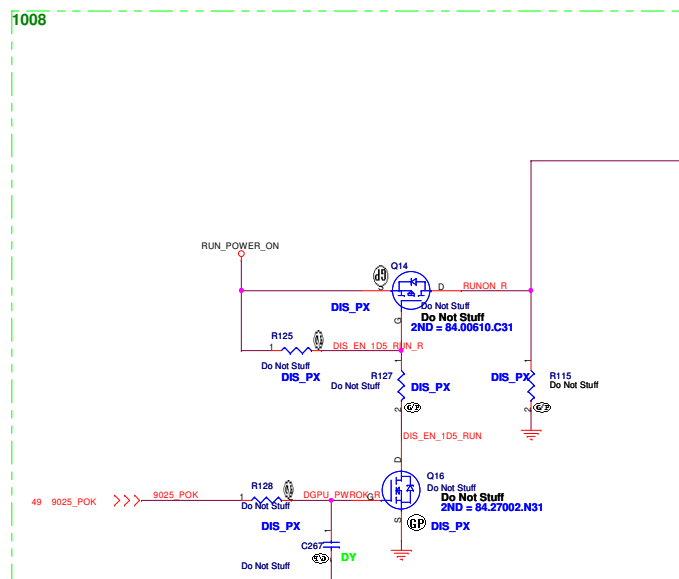
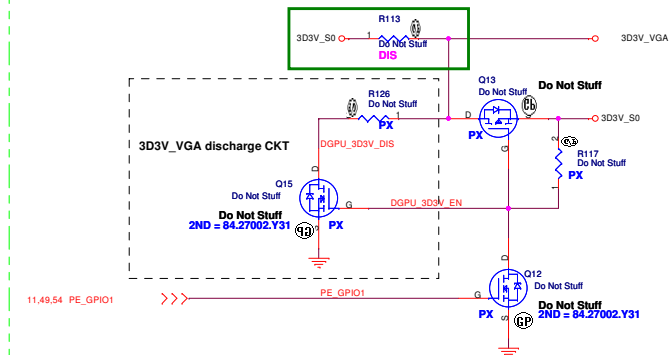
Run Power

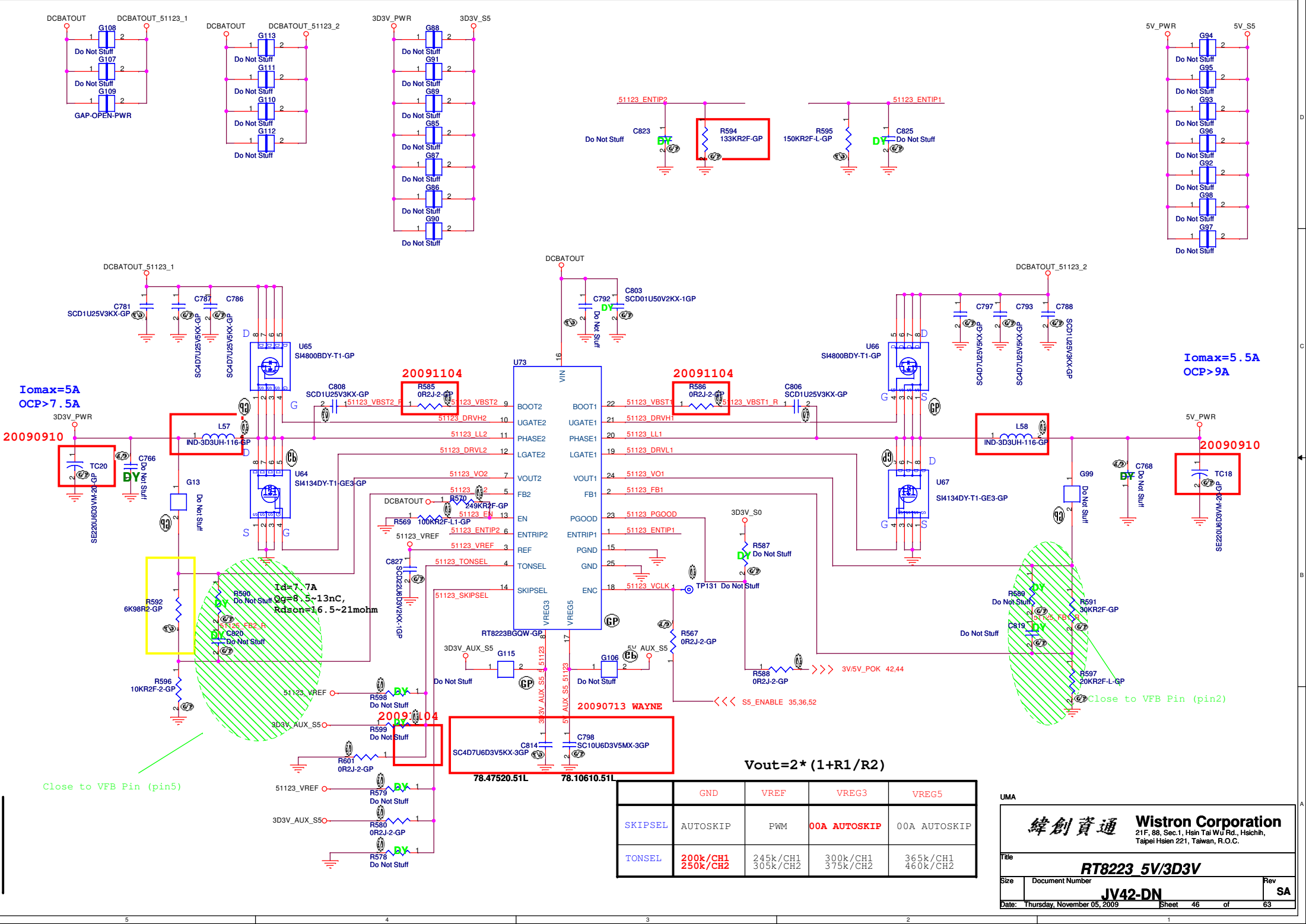
Aux Power

3D3V_AUX_S5



+3VS to 3.3V_DELAY Transfer





	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

UMA

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

RT8223 5V/3D3V

Size

Document Number

Rev

JV42-DN

SA

Date: Thursday, November 05, 2009

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[illegible]

Title			
RT8209E 1D5V			
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[illegible]

RT9025 for 1D1V_S5

Iomax=1.4A
OCP>2A

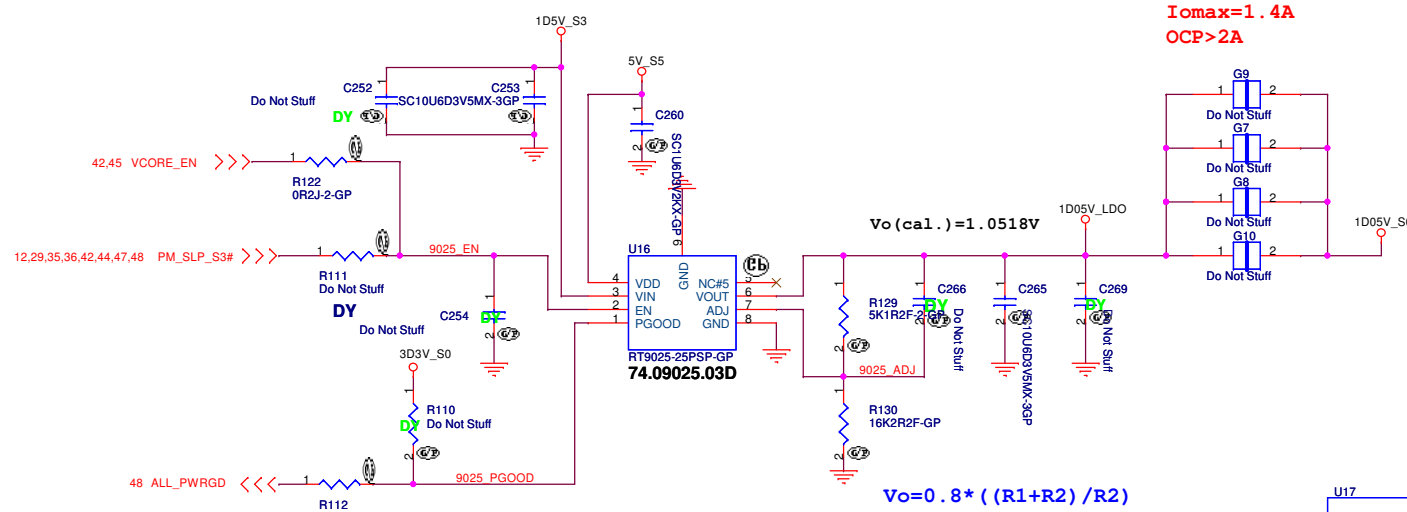
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OCP>2A

Vo(cal.)=1.0518V

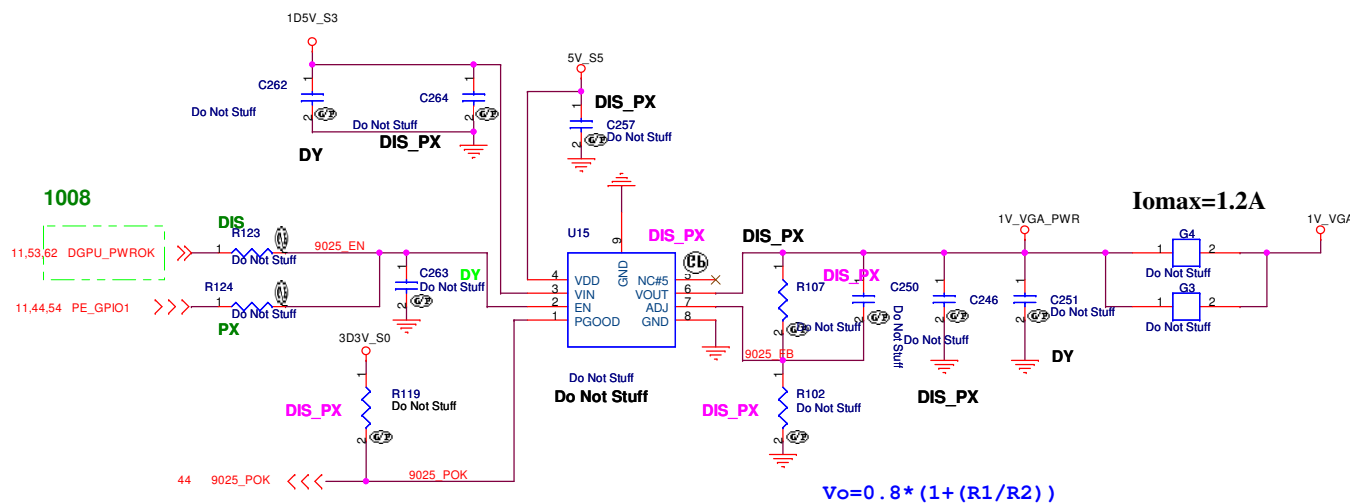
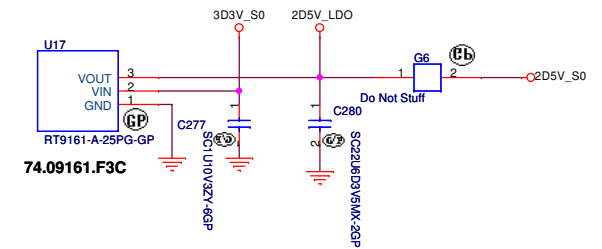
$$V_o = 0.8 * ((R_1 + R_2) / R_2)$$

$$= 0.8 * ((6.2K + 16.2K) / 16.2K) = 1.106V$$
[illegible]

RT9025 for 1D05V_S0



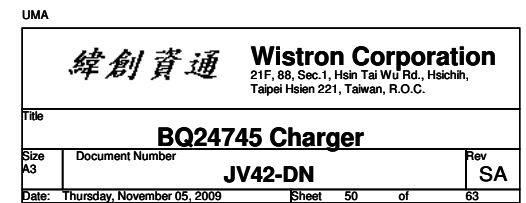
2D5V
I_{max}=0.2A

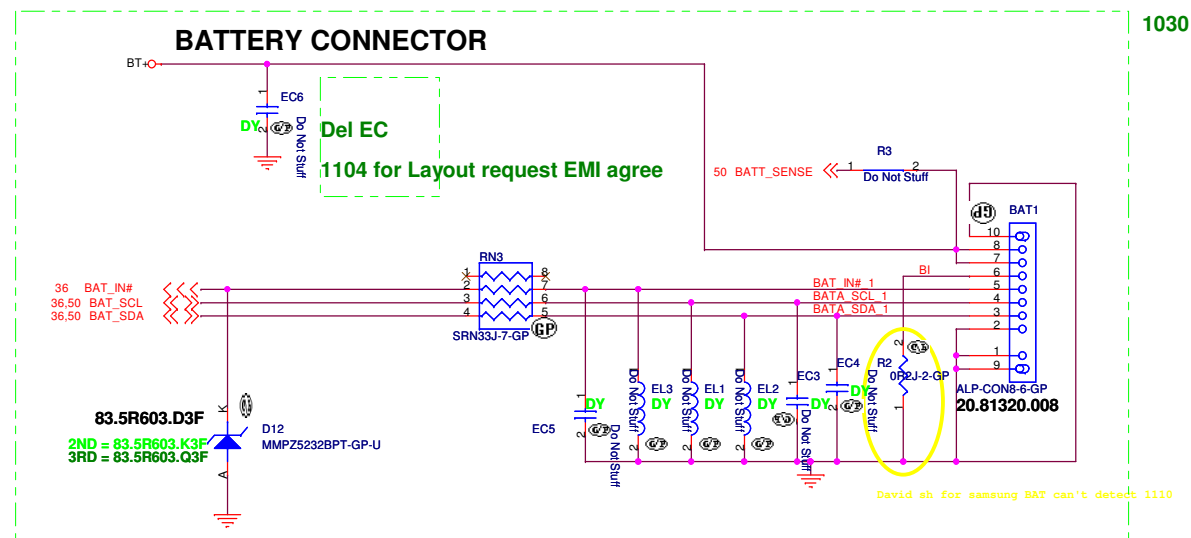
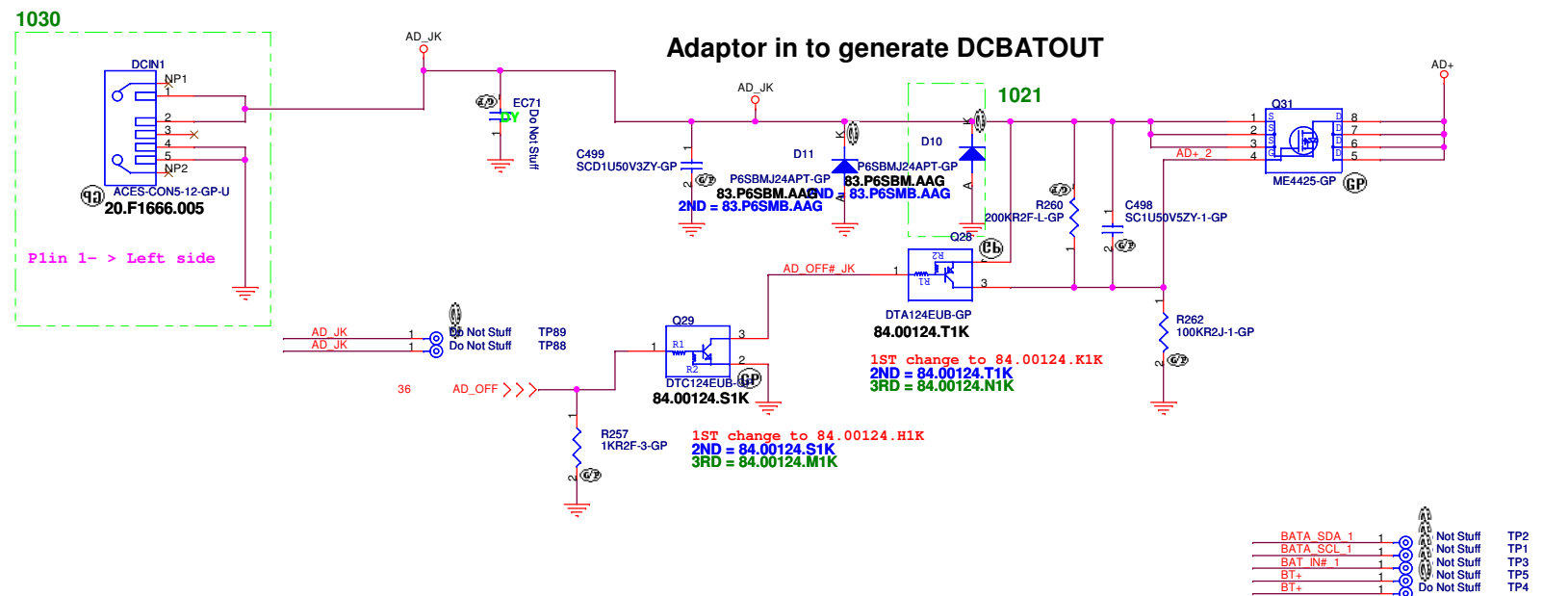


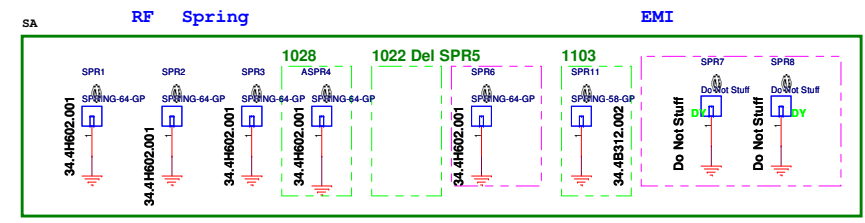
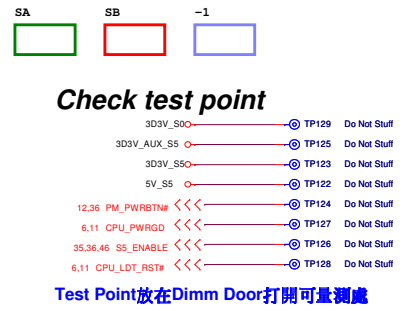
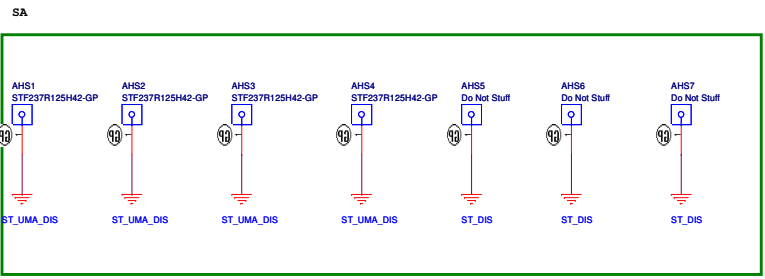
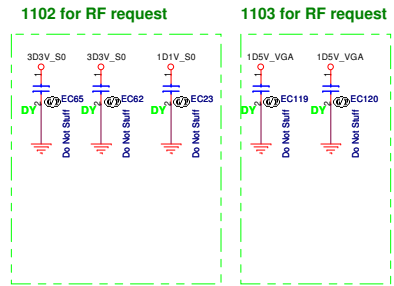
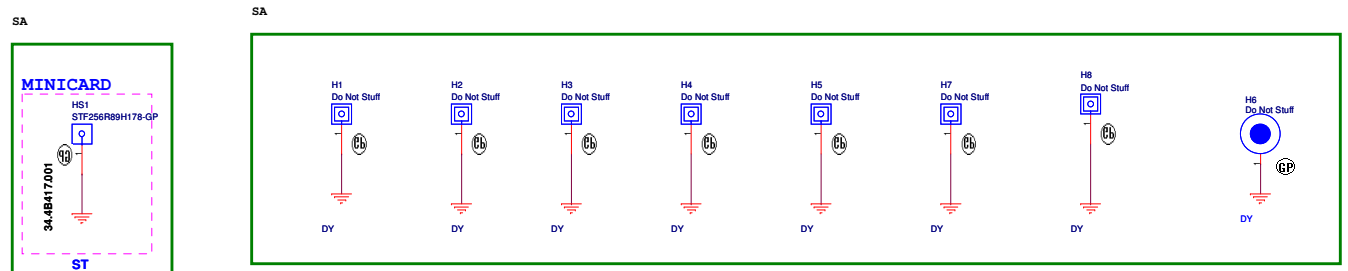
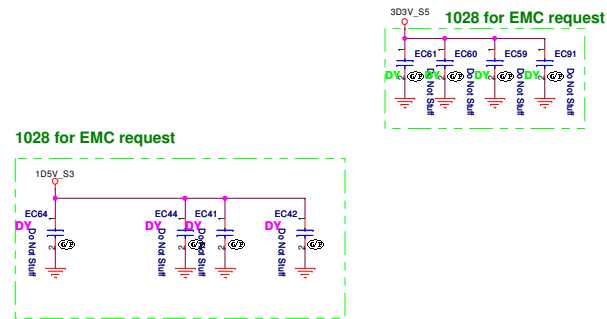
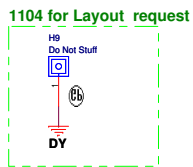
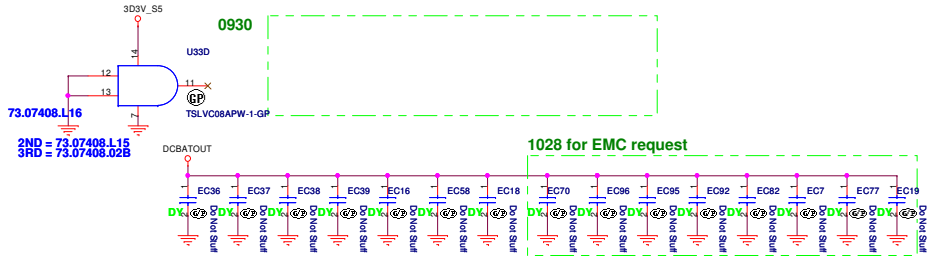
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

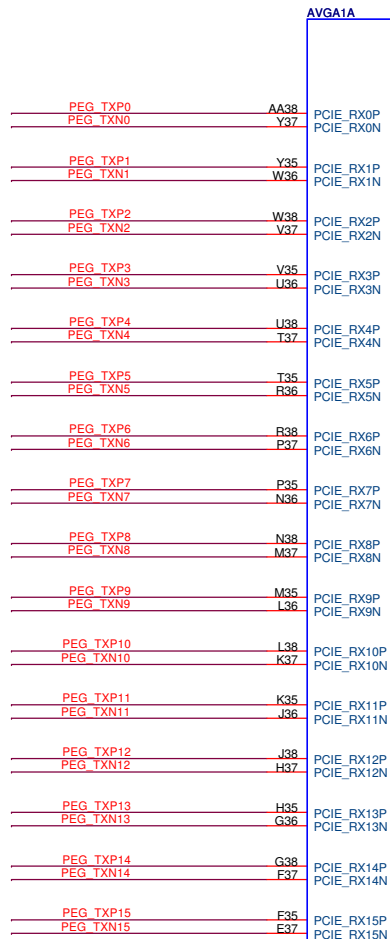
Title		
LDO 1D05V/2D5V/1V		
Size	Document Number	Rev
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Date:	Thursday, November 05, 2009	Sheet 49 of 63



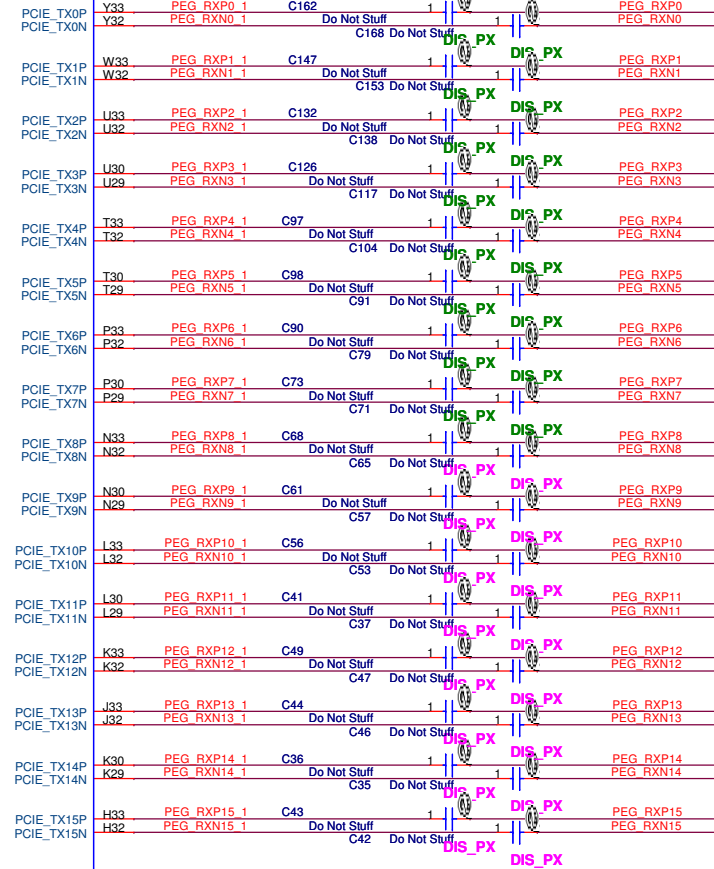




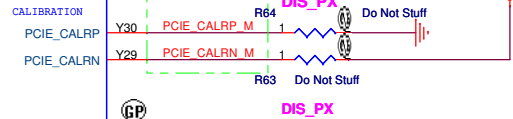
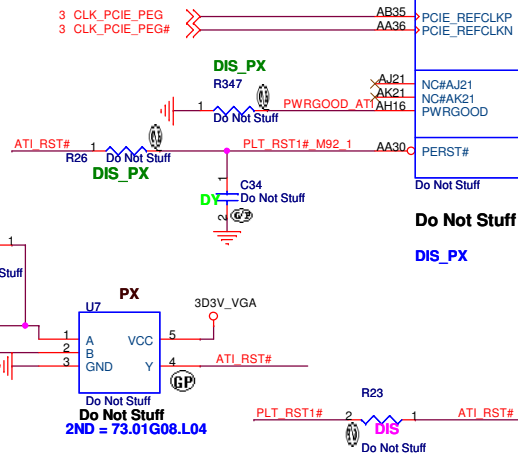
8 PEG_TXP[15..0] << PEG_TXP[15..0]
8 PEG_TXN[15..0] << PEG_TXN[15..0]



PCI EXPRESS INTERFACE



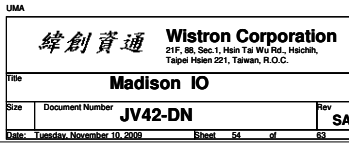
8 PEG_RXP[15..0] << PEG_RXP[15..0]
8 PEG_RXN[15..0] << PEG_RXN[15..0]

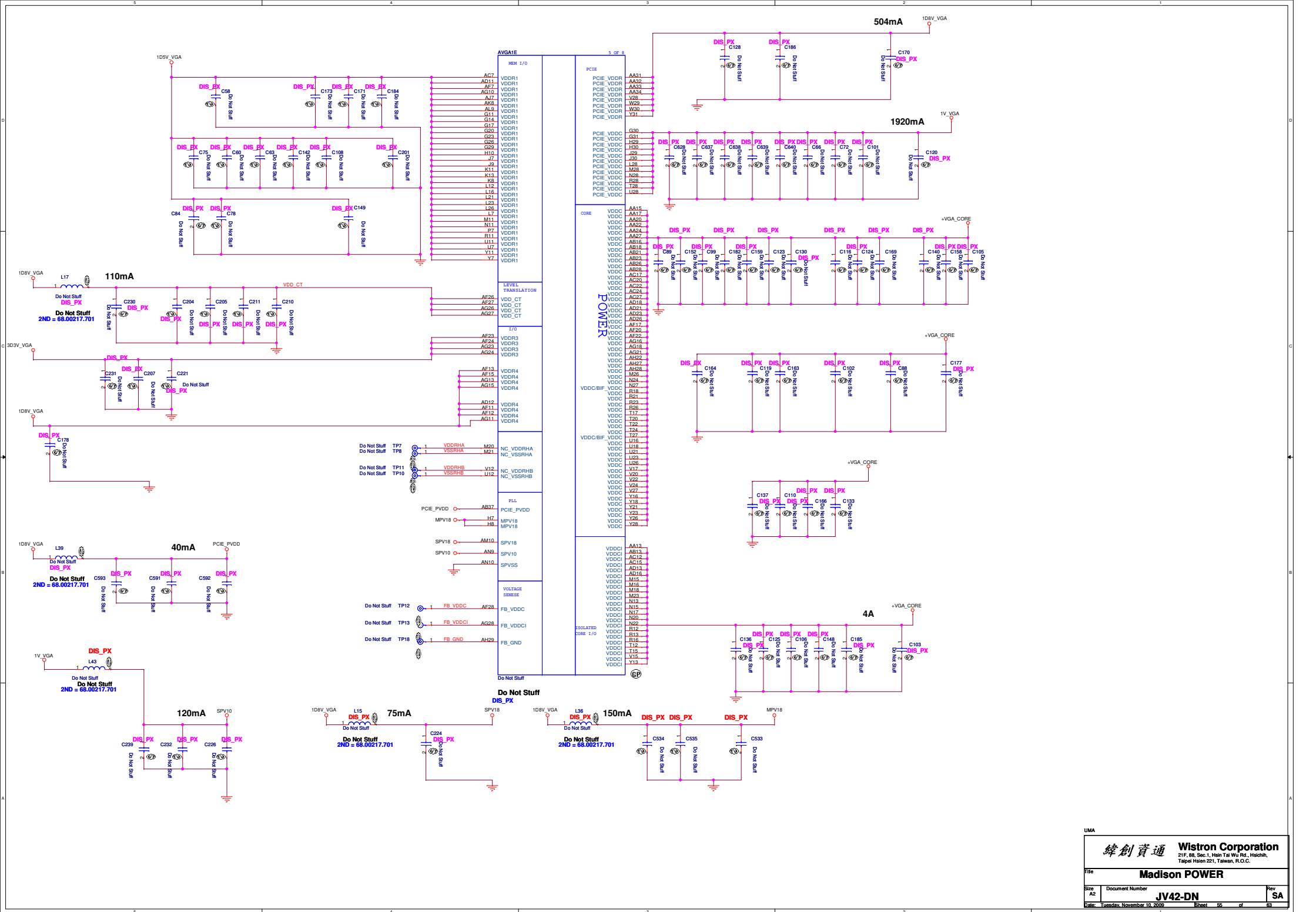


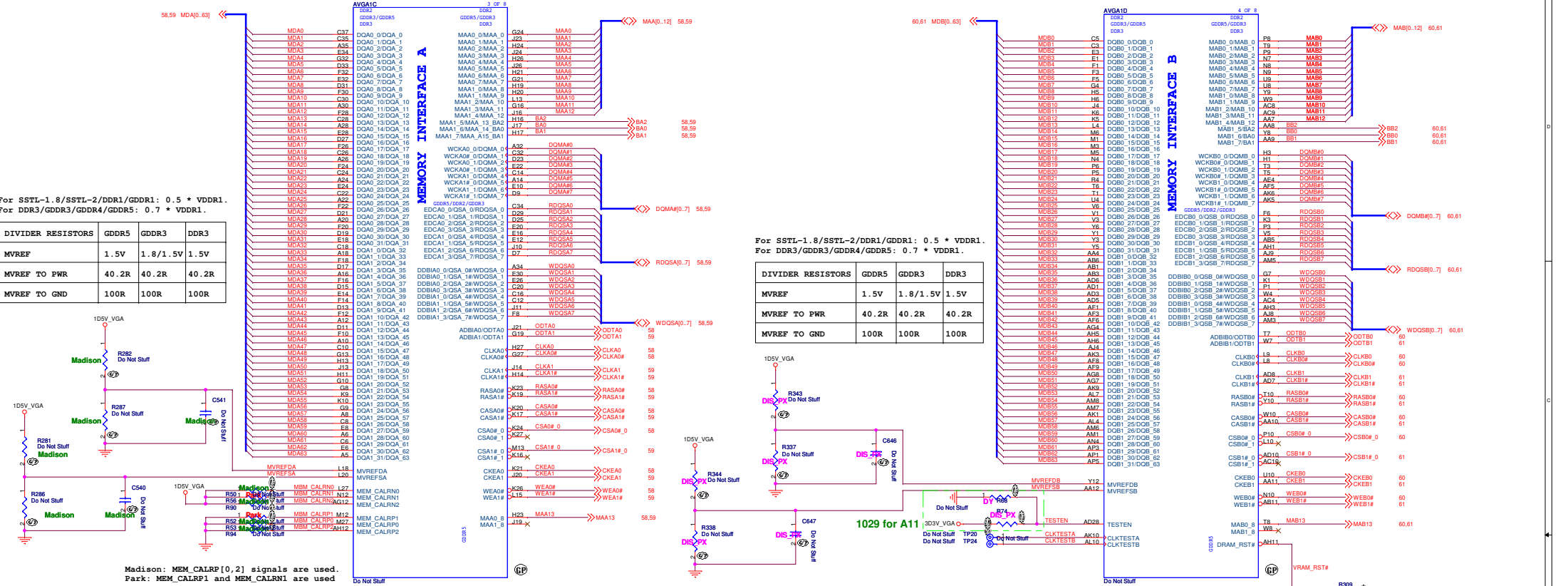
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Madison PCIE
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For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDRI.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDRI.

DIVIDER RESISTORS	GDDR5	GDDR3	DDR3
MVBREF	1.5V	1.8/1.5V	1.5V
MVBREF TO PWR	40.2R	40.2R	40.2R
MVBREF TO GND	100R	100R	100R

105V_VGA
R282 Do Not Stuff
Madison
R287 Do Not Stuff
Madison
C541
105V_VGA
R281 Do Not Stuff
Madison
R286 Do Not Stuff
Madison
C540
105V_VGA
R285 Do Not Stuff
Madison
R284 Do Not Stuff
Madison
R283 Do Not Stuff
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R282 Do Not Stuff
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R281 Do Not Stuff
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R2 Do Not Stuff
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R1 Do Not Stuff
Madison
R0 Do Not Stuff
Madison

Madison: MEM_CALRP[0,2] signals are used.
Park: MEM_CALRP1 and MEM_CALRN1 are used

Do Not Stuff
DIS_FX

Madison->71.MDS0N.M01,Park->71.0PARK.M04

AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,
THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1	
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number
128MB	x000	ST Microelectronics	M25P05A
256MB	x001		M25P10A
512MB	x010		M25P20
1GB	x		M25P40
2GB	x	Chinglis (formerly PMC)	M25P80
4GB	x		Pm25LV512A
			Pm25LV010A

1029 for A11

1026

1009 for A11

Designator	For M97-M2	For Mannheim
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

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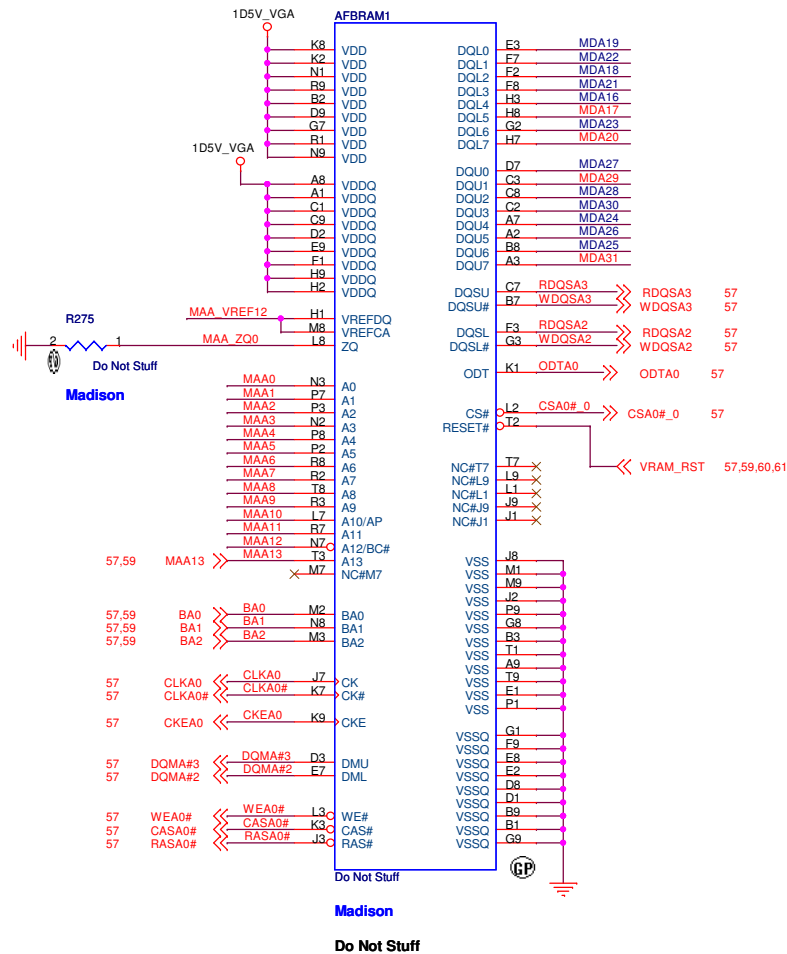
Madison Memory / Straps

Rev SA

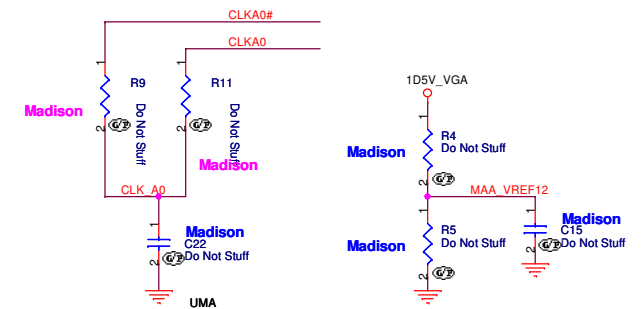
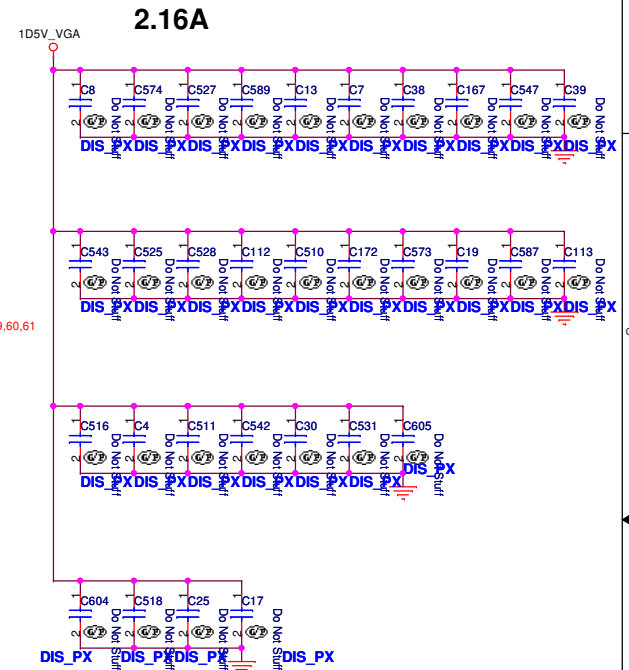
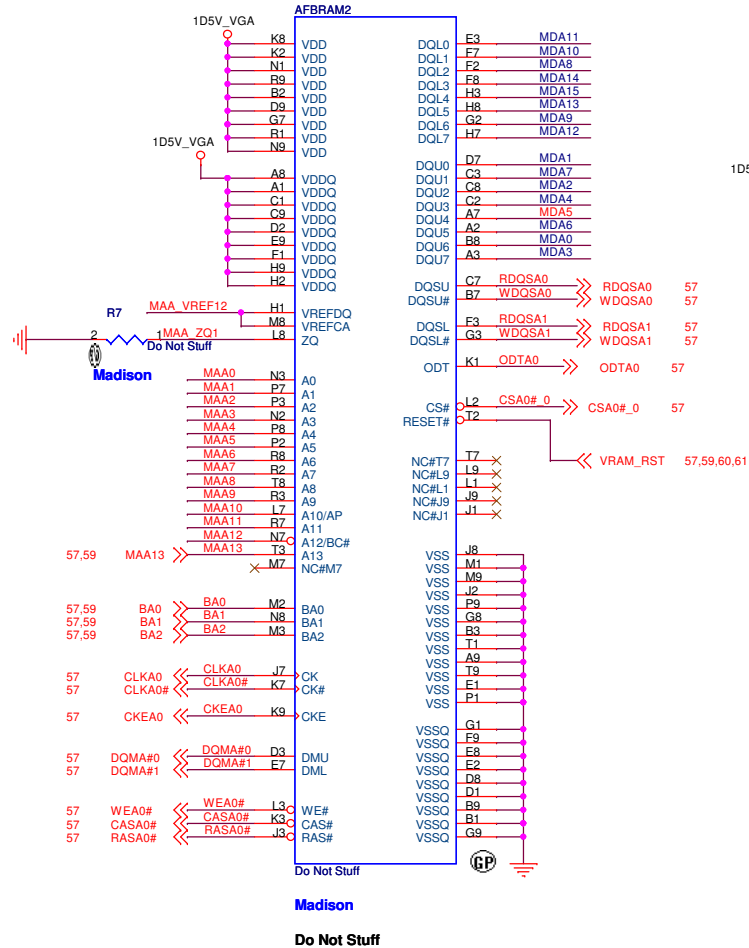
JV42-DN

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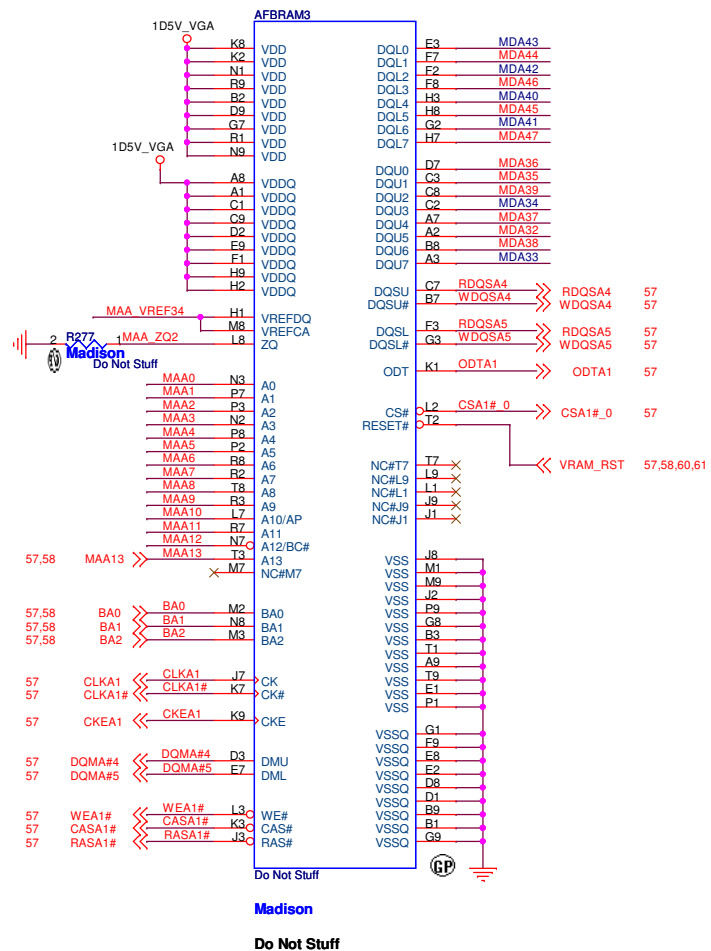
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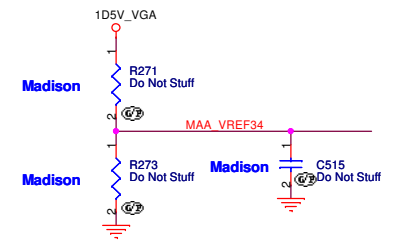
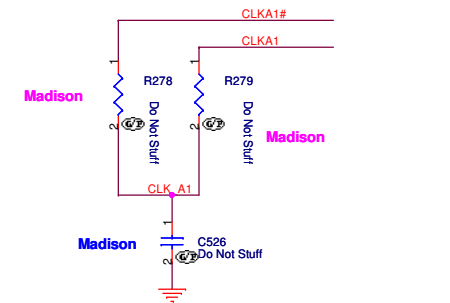
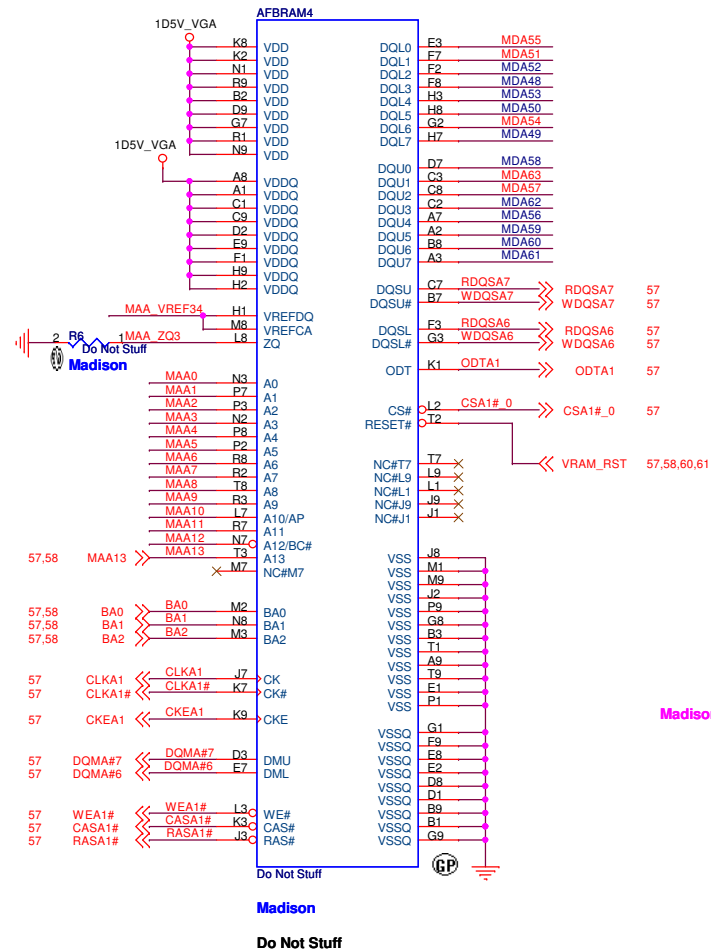
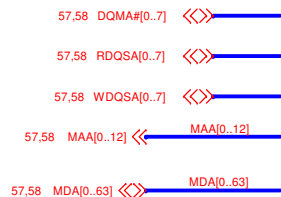
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HYNIX:   72.51G63.C0U
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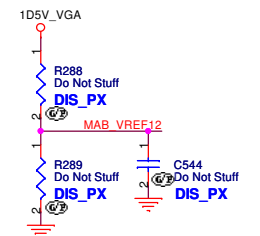
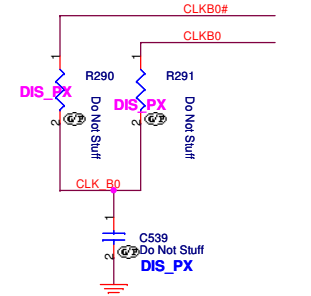
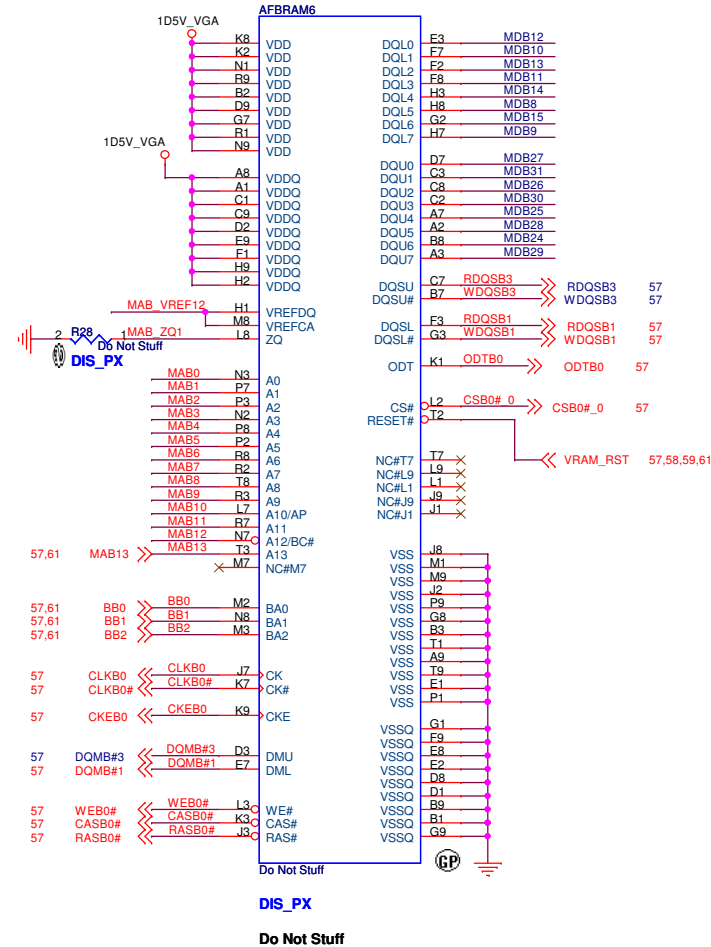
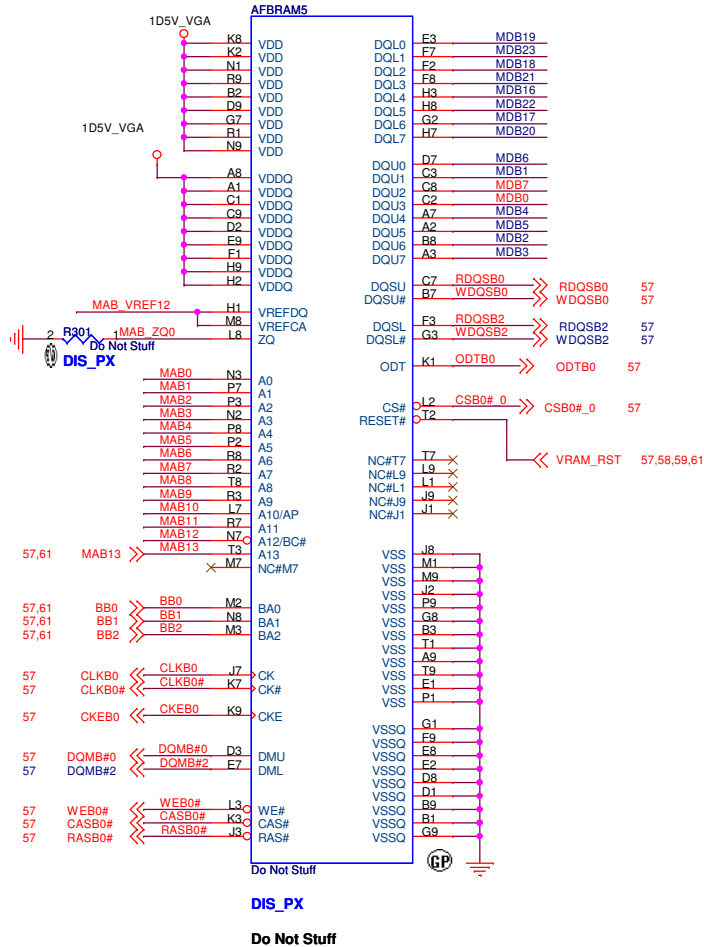
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SAMSUNG: 72.41164.H0U
HYNIX:   72.51G63.C0U
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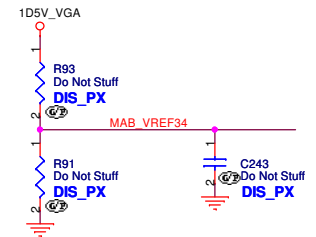
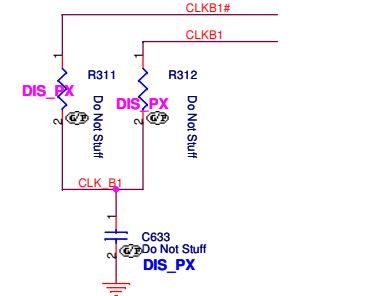
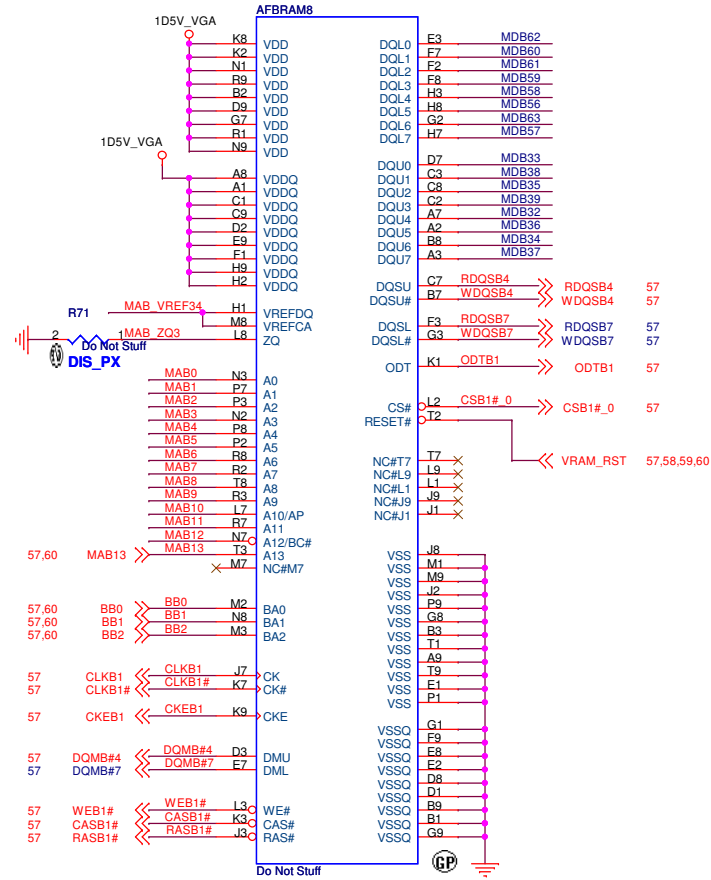
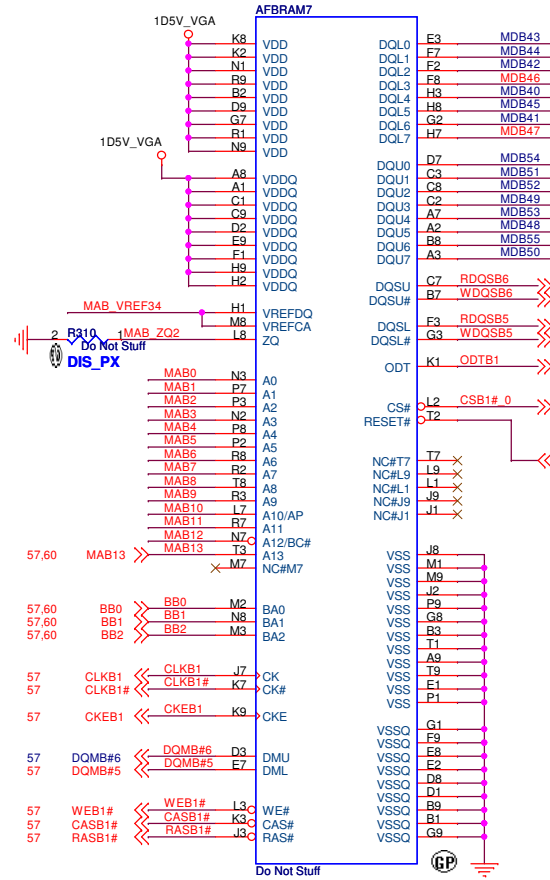
DDR3



UMA

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DDR3



SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

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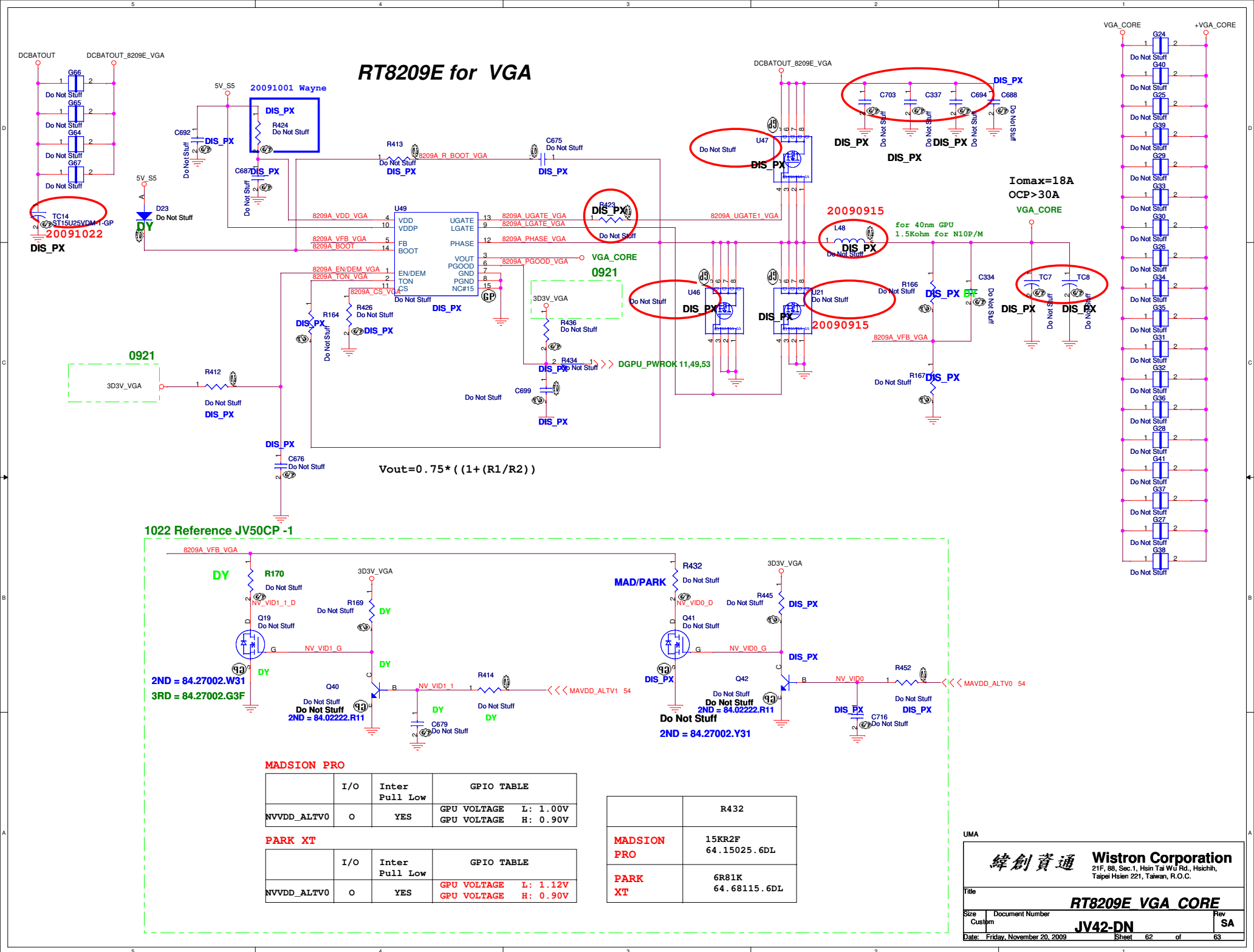
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UMA

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	A	B	C	D	E
	NB RS780-->RS880M 71.RS780.M02-->71.RS880.M02			BOM 1st -> Diserete Madison Hynix(S02G) 2nd -> UMA (S01G) 1st +3rd -> Diserete Park Hynix(S03G) 1st +3rd -> Diserete Park Samsung(S04G) 1st -> Diserete Madison Samsung (S05G) PX=PARK+Hynix(1st +3rd)	
4	SB SB820M-1-GP 71.SB820.00U-->71.SB820.M03				
	SATA_CALRP A11: 80歐姆 1% resistor to GND A12: TBD歐姆 1% resistor to GND				
	SATA_CALRN A11:A11: 931歐姆 1% resistor to VDDAN_11_SATA A12: TBD歐姆 1% resistor to VDDAN_11_SATA.				
3	VGA Madison--> PN:71.MDSON.M01 Park--> PN:71.0PARK.M04				
	VRAM Samsung-->VRAM FBRAM1~8 PN:VR.1GB0B.006 Hynix--> VRAM FBRAM1~8 PN:VR.1GB0G.004				
2	CRT UMA-->L1-->2R 0603 C62-->47U/6.3V DIS-->L1-->Bead(L1 68.00217.711 L1608-UH38 SBK160808T-221Y-N-GP) C62-->DY				
	HDMI R497 : DIS-->0R UMA & PX-->5.1K (R497 63.51234.1DL R402H16 5K1R2J-4-GP) R496 : DIS-->100K UMA & PX-->10K(R496 63.10334.1DL R402H16 10KR2J-3-GP)				
1	R432(MAD/PARK) Madison-->V15KR2F 64.15025.6DL Park-->R432 64.68115.6DL				

UMA

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NOTE

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