

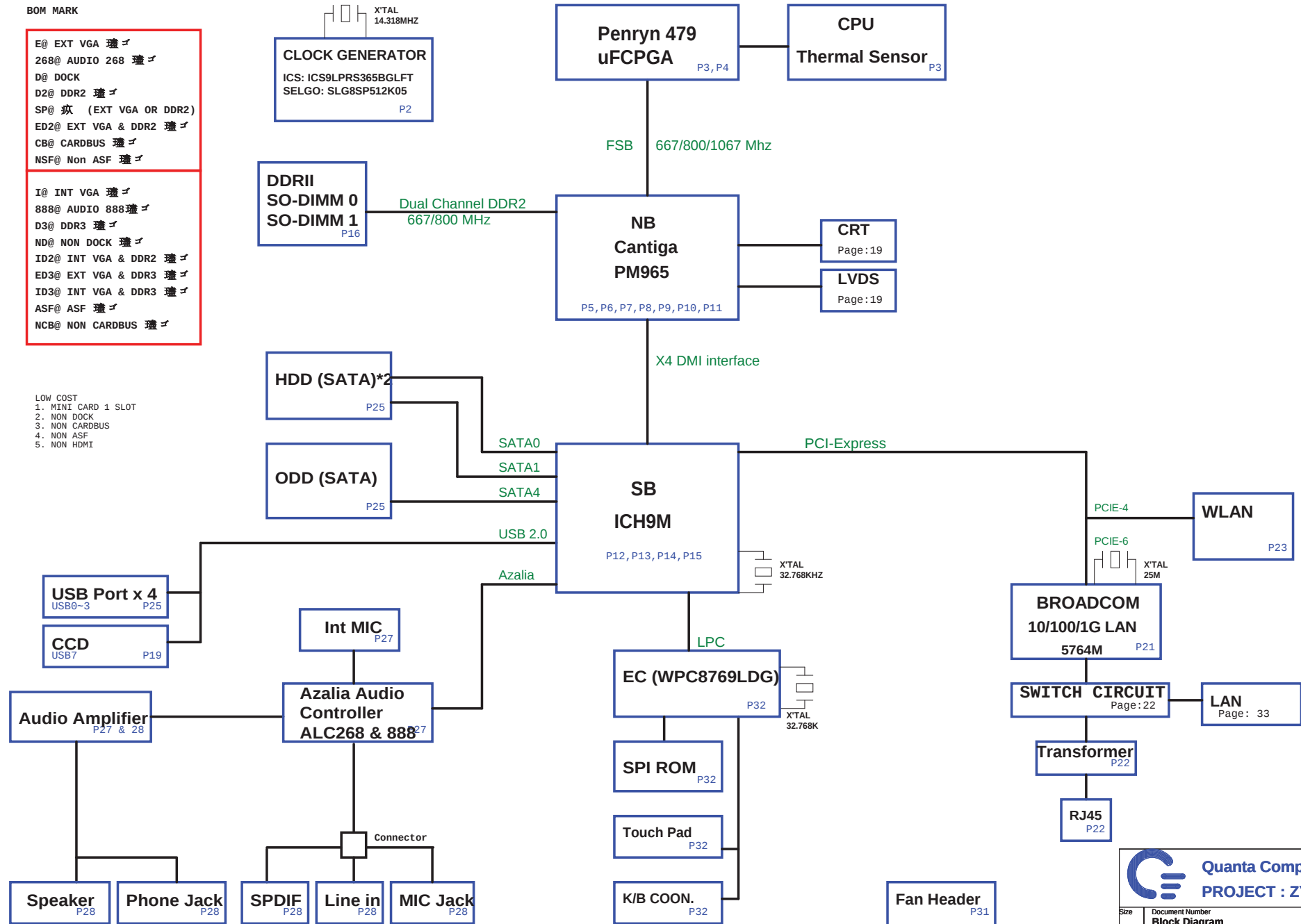
ZY6D SYSTEM BLOCK DIAGRAM

BOM MARK

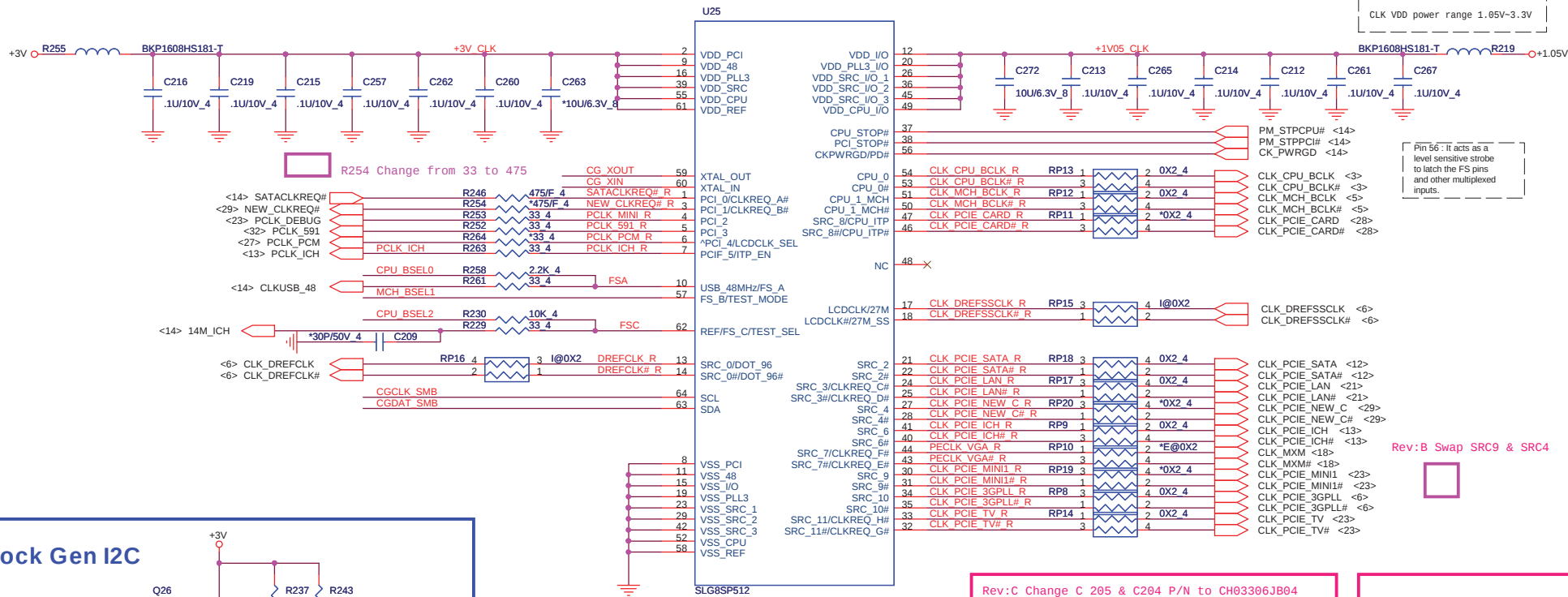
E@ EXT VGA 瓊
268@ AUDIO 268 瓊
D@ DOCK
D2@ DDR2 瓊
SP@ 瓊 (EXT VGA OR DDR2)
ED2@ EXT VGA & DDR2 瓊
CB@ CARDBUS 瓊
NSF@ Non ASF 瓊

I@ INT VGA 瓊
888@ AUDIO 888 瓊
D3@ DDR3 瓊
ND@ NON DOCK 瓊
ID2@ INT VGA & DDR2 瓊
ED3@ EXT VGA & DDR3 瓊
ID3@ INT VGA & DDR3 瓊
ASF@ ASF 瓊
NCB@ NON CARDBUS 瓊

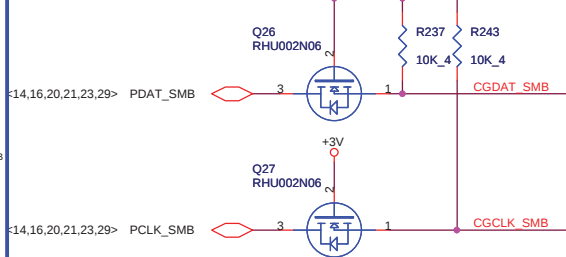
LOW COST
1. MINI CARD 1 SLOT
2. NON DOCK
3. NON CARDBUS
4. NON ASF
5. NON HDMI



Clock Generator



Clock Gen I2C

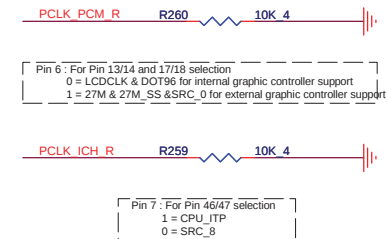


CPU Clock select

BSEL Frequency Select Table

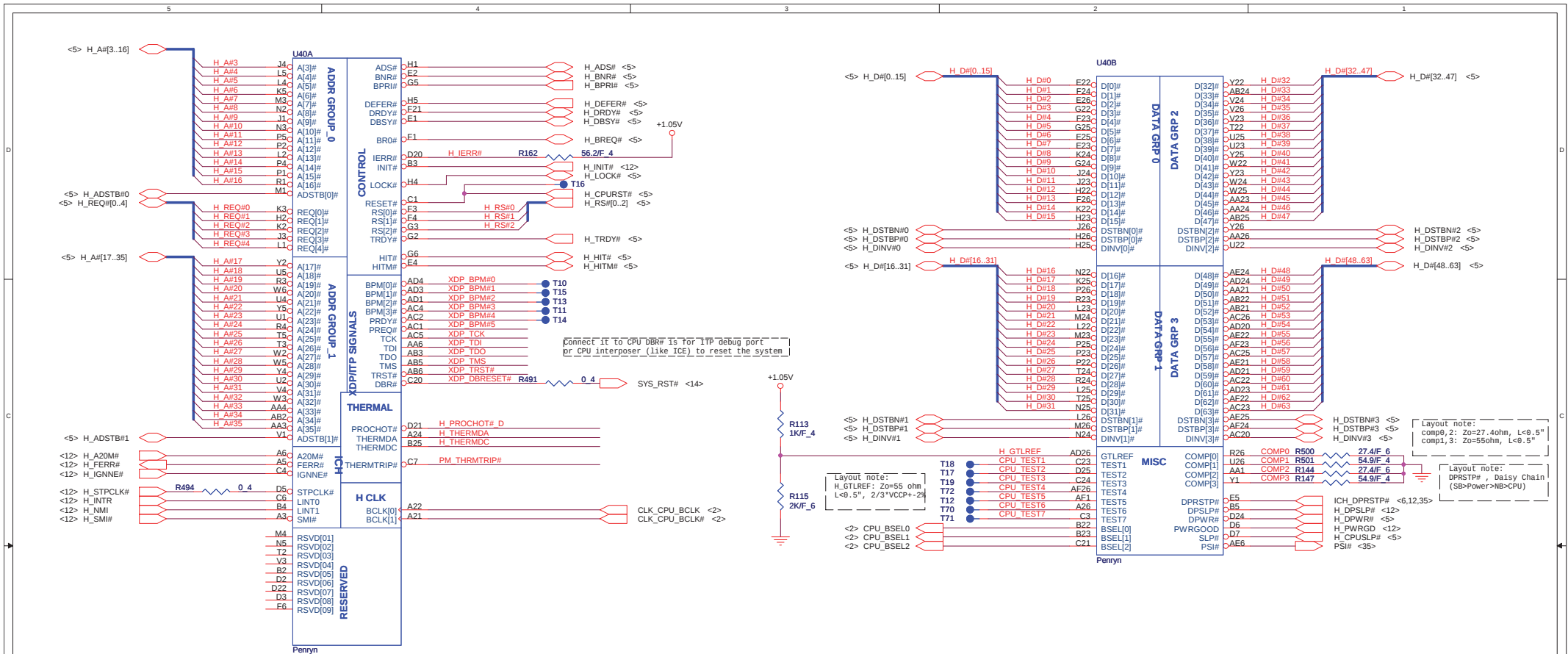
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table



Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	CLOCK GENERATOR CK505 W/REGULATOR	1A
Date:	Thursday, August 28, 2008	Sheet 2 of 40

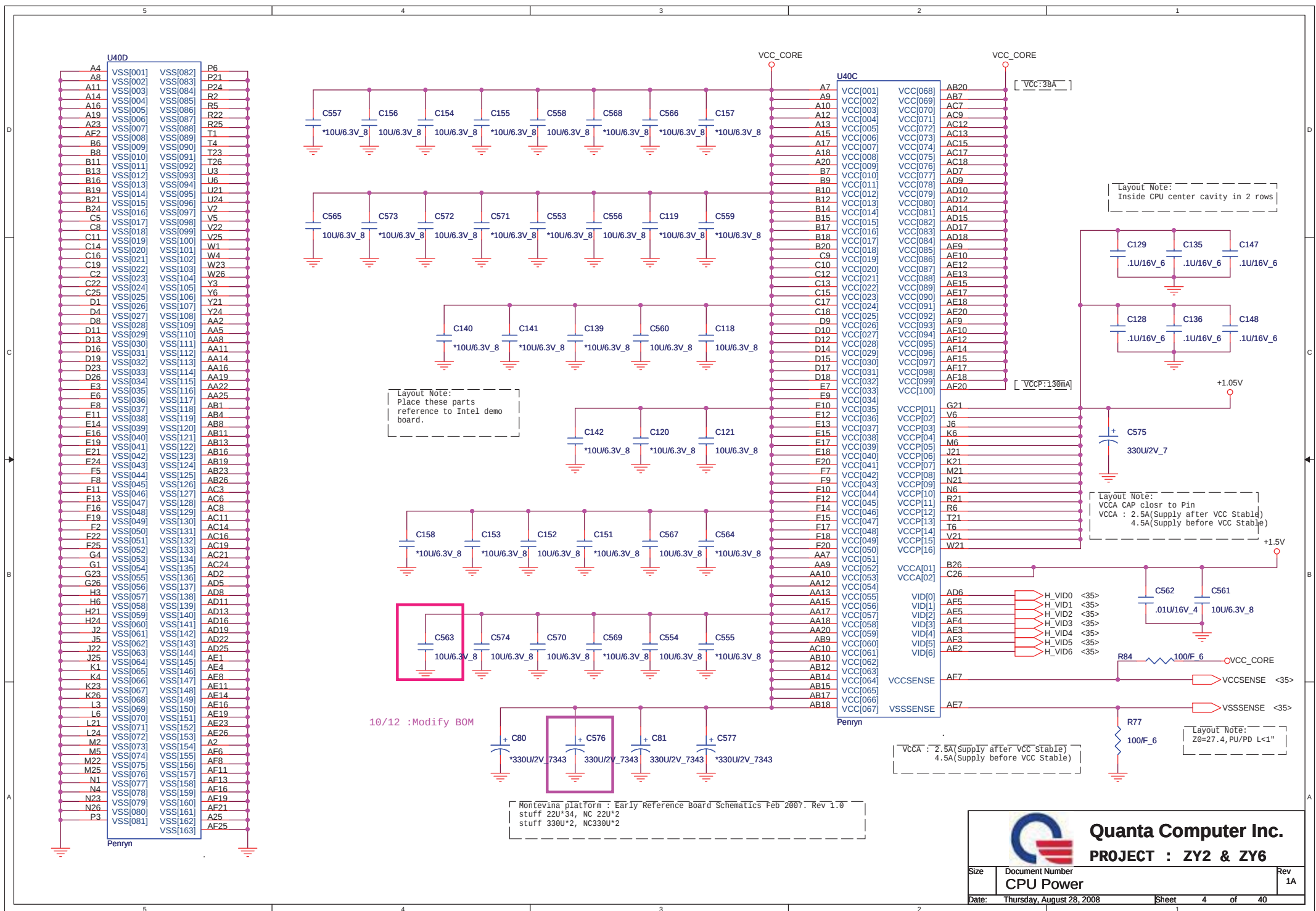


Thermal Trip

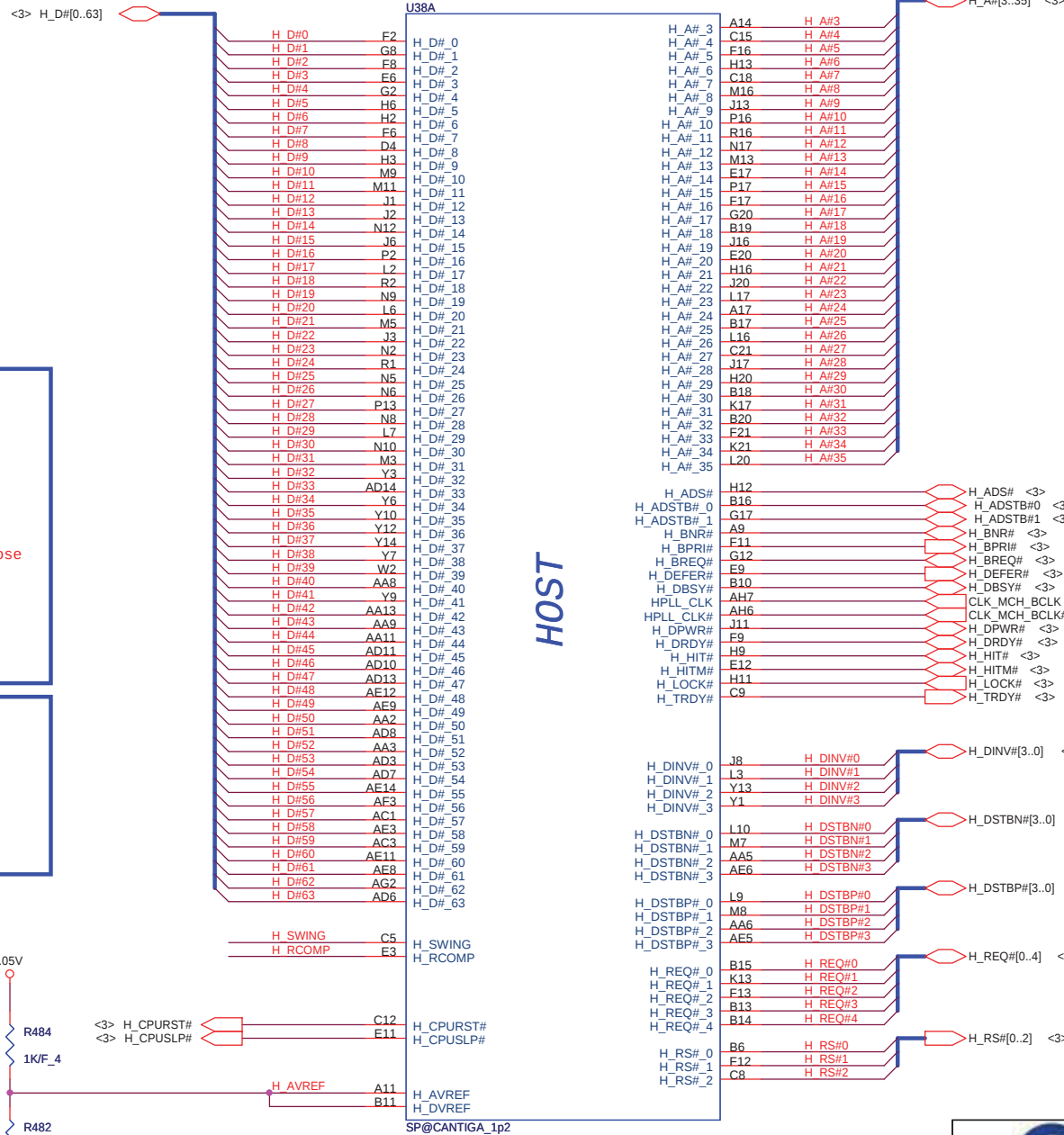
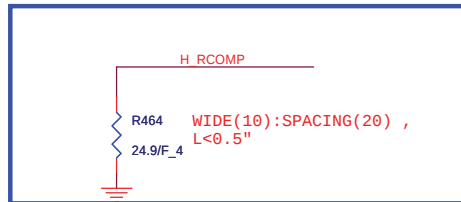
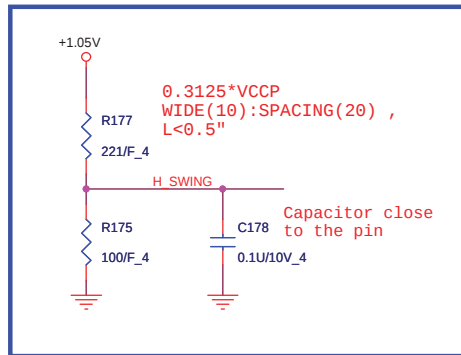
CPU Thermal monitor

XDP PU/PD

Processor hot



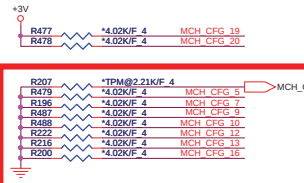
	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06



Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) or PCIe is operational (Default) and Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin



HB Thermal trip pin
No use Thermal trip NB side can NC (NB has ODT)

TPMUPSTP
The Daisy chain topology should be routed from ICHM to IMP, then to (S)MCH and CPU, in that order.

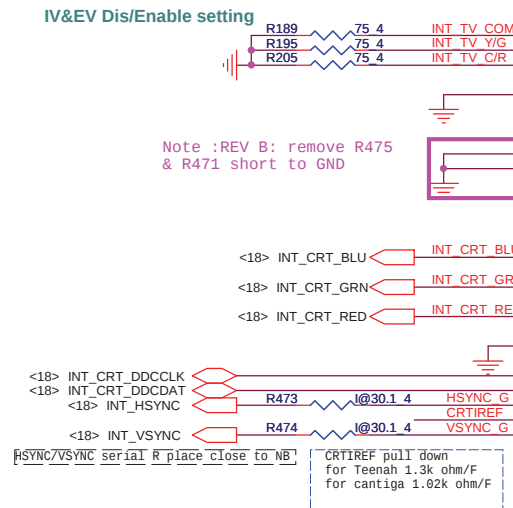
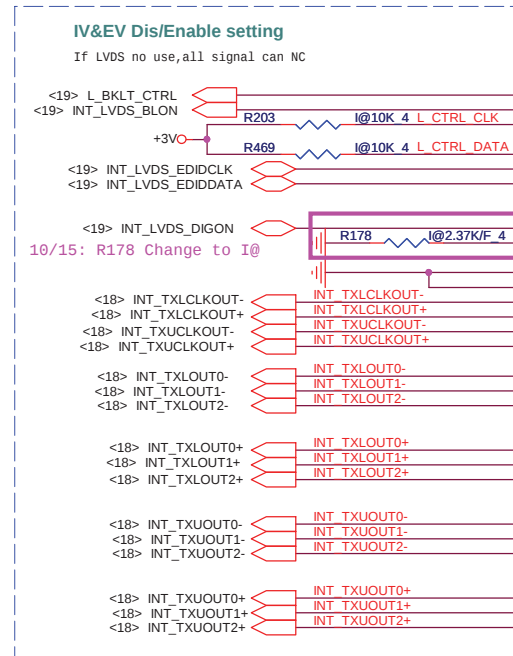
<2> MCH_BSEL0
<2> MCH_BSEL1
<2> MCH_BSEL2
<13> MCH_CFG_6

<14> PM_SYNC#
<3,12,35> ICH DPRSTP#
<16,17> PM_EXTTS#0
<16,17> PM_EXTTS#1
<3,14,32,35> DELAY_VR_PVRGOOD
<13> PLY_RST#
<3,12> PM_THRMTRIP#
<14,35> PM_DPRSLPVR

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U38C

L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA

L_VDD_EN
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSB_CLK#
LVDSB_CLK

LVDSA_DATA#_0
LVDSA_DATA#_1
LVDSA_DATA#_2
LVDSA_DATA#_3

LVDSA_DATA_0
LVDSA_DATA_1
LVDSA_DATA_2
LVDSA_DATA_3

LVDSB_DATA#_0
LVDSB_DATA#_1
LVDSB_DATA#_2
LVDSB_DATA#_3

LVDSB_DATA_0
LVDSB_DATA_1
LVDSB_DATA_2
LVDSB_DATA_3

TVA_DAC
TVB_DAC
TVC_DAC

TV_RTIN

TV_DCONSEL_0
TV_DCONSEL_1

CRT_BLUE
CRT_GREEN
CRT_RED
CRT_JRTN

CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_TVO_IREF
CRT_VSYNC

SP@CANTIGA_1p2

SDA7
PCI-EXPRESS
VGA

PEG_COMPI
PEG_COMPO

PEG_RX#_0
PEG_RX#_1
PEG_RX#_2
PEG_RX#_3
PEG_RX#_4
PEG_RX#_5
PEG_RX#_6
PEG_RX#_7
PEG_RX#_8
PEG_RX#_9
PEG_RX#_10
PEG_RX#_11
PEG_RX#_12
PEG_RX#_13
PEG_RX#_14
PEG_RX#_15

PEG_RX_0
PEG_RX_1
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PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15

PEG_TX#_0
PEG_TX#_1
PEG_TX#_2
PEG_TX#_3
PEG_TX#_4
PEG_TX#_5
PEG_TX#_6
PEG_TX#_7
PEG_TX#_8
PEG_TX#_9
PEG_TX#_10
PEG_TX#_11
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PEG_TX#_14
PEG_TX#_15

PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
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PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15

L<0.5", If PCIe not support still connect to +VCC_PEG

Rev: B Change P/N

Can support reversal routing. If CF69=1, PCI Express is normal operation. If CF69=0, then PEG_TXP8 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

EXP A COMPX
R215
49.9/F
+1.05V

PEG_RXN[15:0] <18>

PEG_RXP[15:0] <18>

PEG_TXN[15:0] <18>

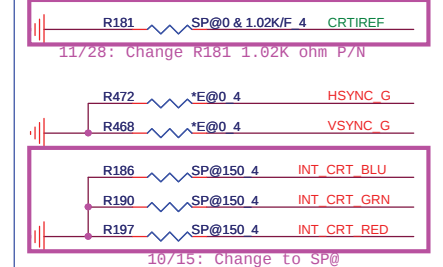
PEG_TXP[15:0] <18>

IV&EV Dis/Enable setting

<5/31>Montevina Schematics Checklist_Rev0.8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC. What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA, CRT_HSYNC, CRT_VSYNC these signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow design guide.

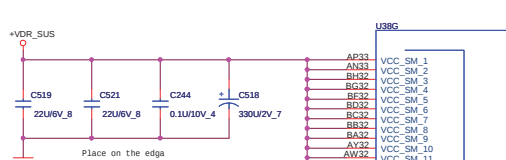
<check list>
For EV@
Connect to GND
CRT R/G/B
HSYNC/VSYNC
CRTIREF

<check list>
For IV@
Connect to 150ohm
CRT R/G/B
Connect to 1.02k ohm
CRTIREF

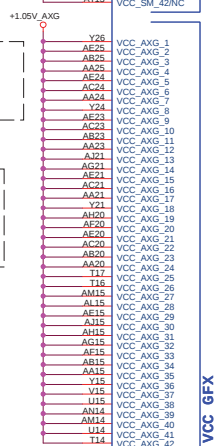


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

GM	TDP	10.5~12W
GS	TDP	7~8W
PM	TDP	7W

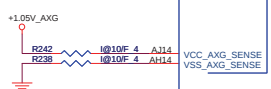


```
VCC_SM(1.8V)
DDR2(800M)
3000mA_S0 , 1mA_S3
DDR2(667M) : 2600mA_S0
DDR3(1067M) : 4140mA_S0
```



```
1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA
```

Voltage regulator is shared between the Graphics Core Rail, VCCA_HPLL, VCCA_MPLL, VCCA_PEG_PLLVCD_PEG_PLL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLb, VCCD_HPLL, VCCA_SM, VCC_AXF

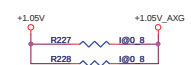
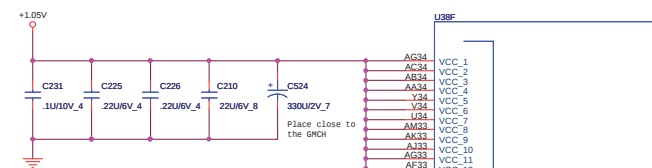


1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFY_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

```
Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB
```

```
Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm
```

```
VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA
```

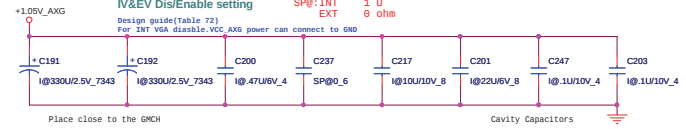


+1.05V_AXG

M&EV Dis/Enable setting

SP0:INT 1
EXT 0

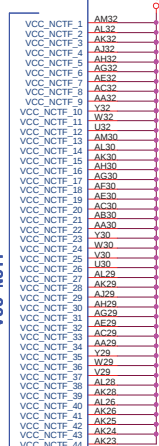
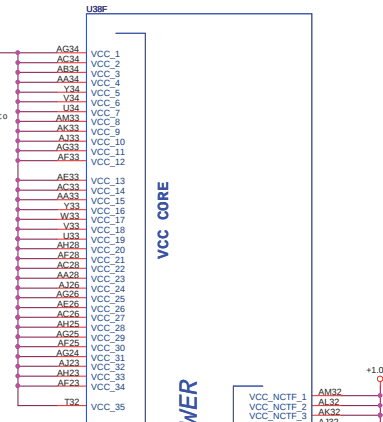
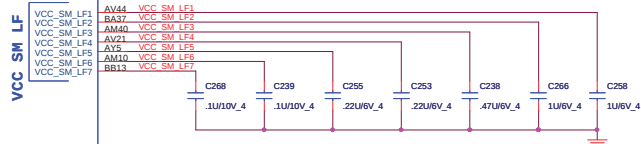
Design guide (Table 72)
For INT VGA disable, VCC_AXG power can connect to GND

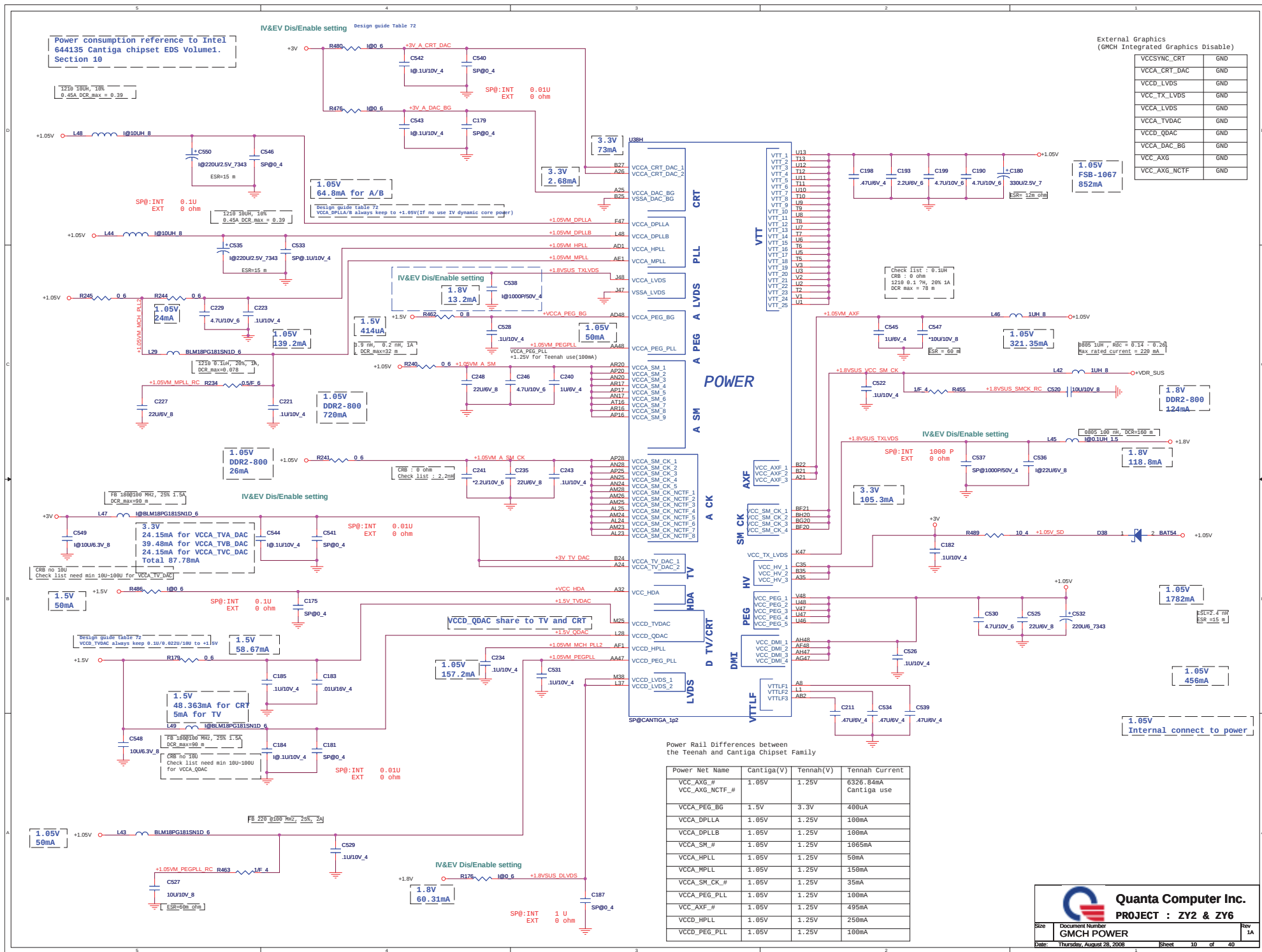


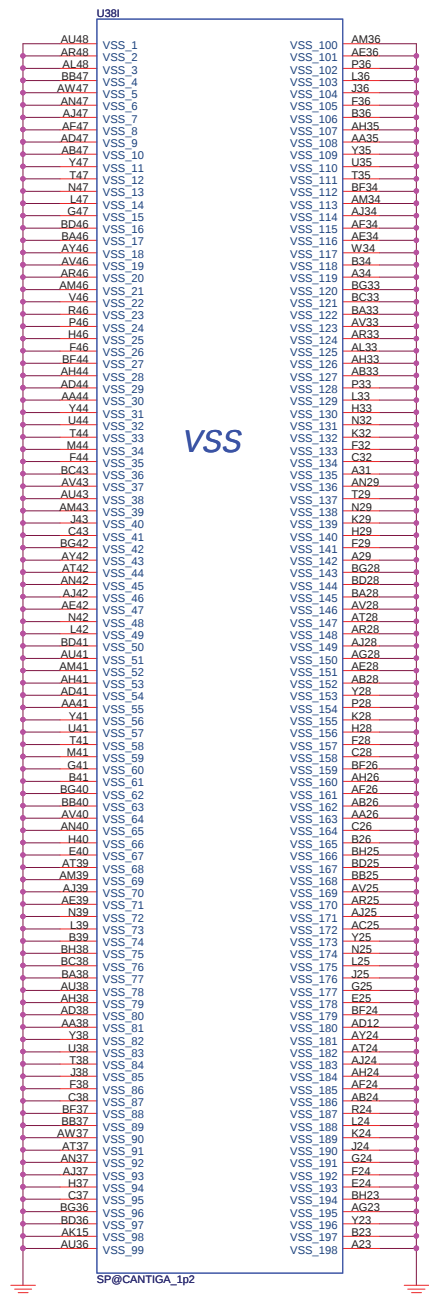
Place close to the GMCH

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

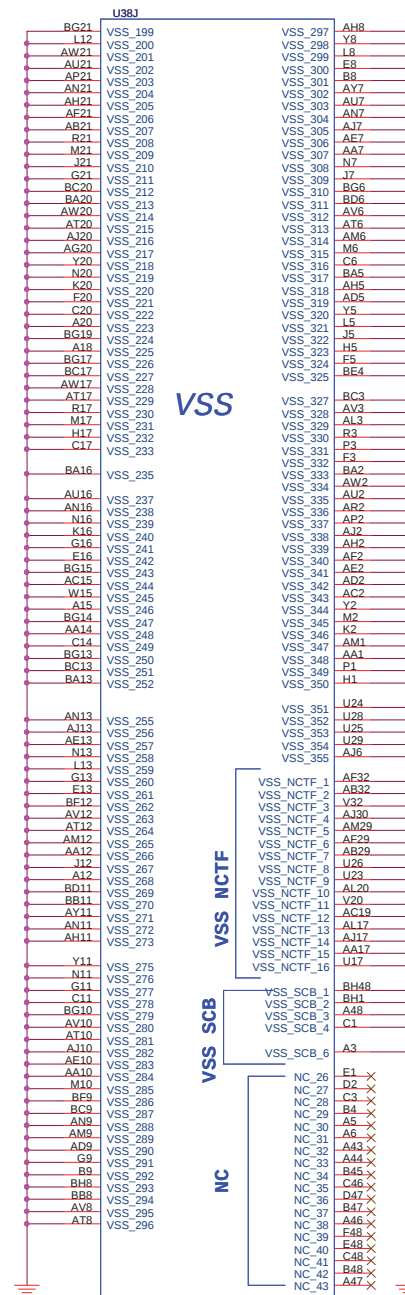
1.8V
Internal connect to power







SP@CANTIGA_1p2

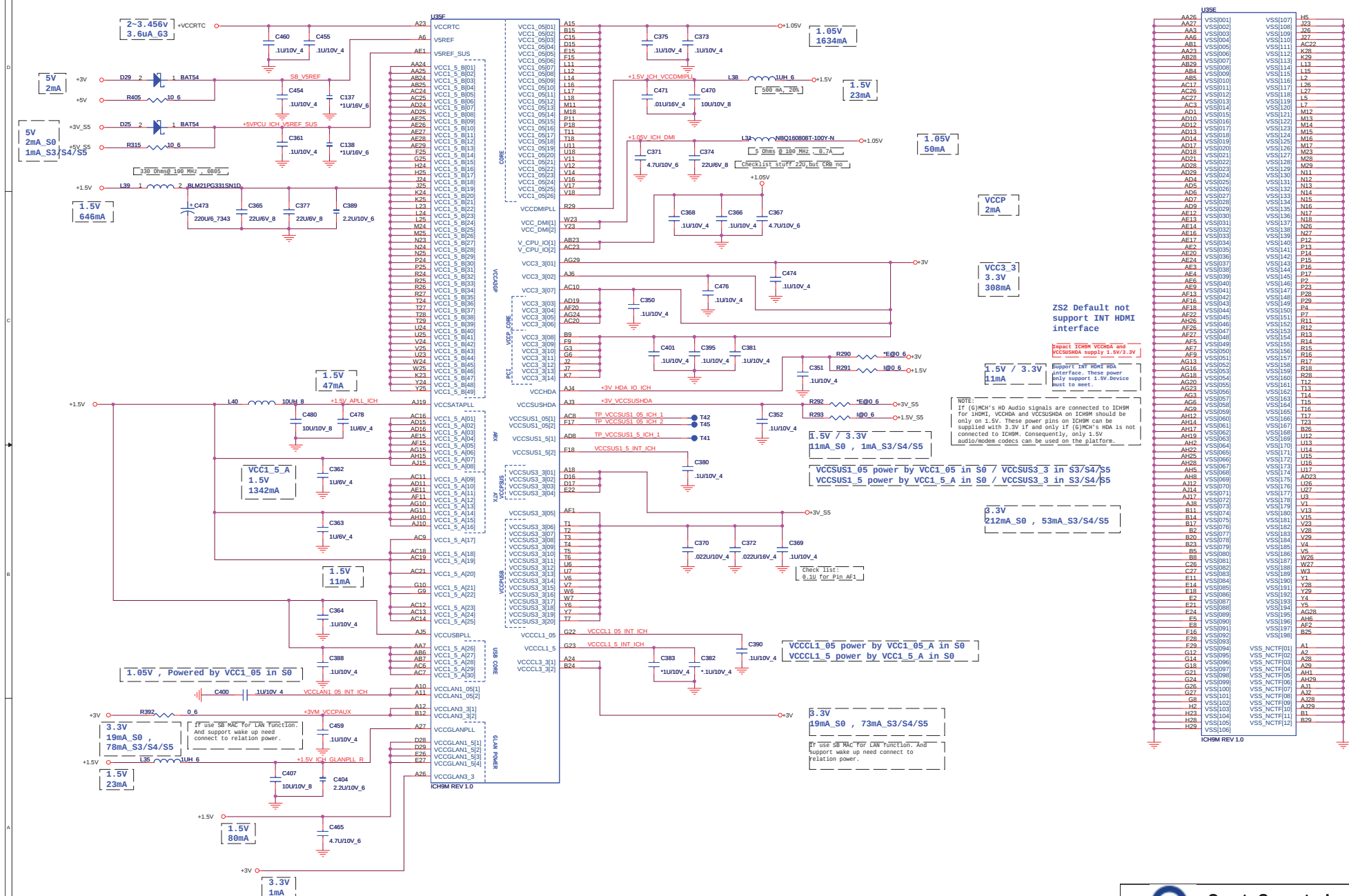


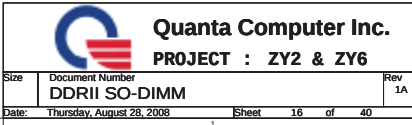
SP@CANTIGA_1p2

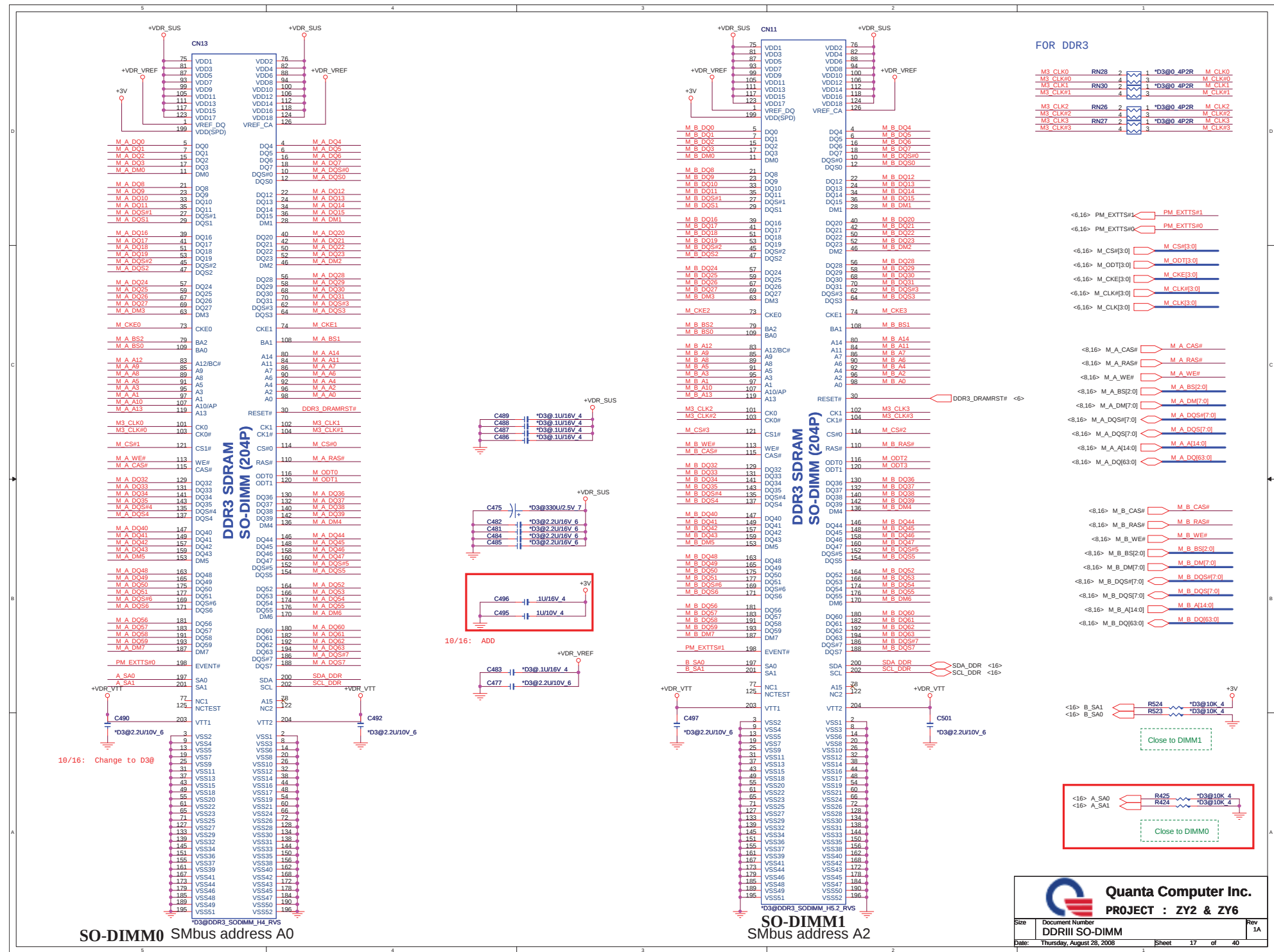


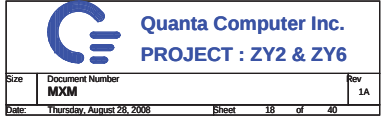
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	GMCH VSS	1A
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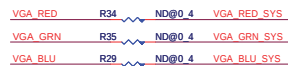
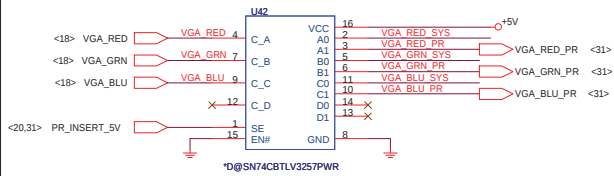




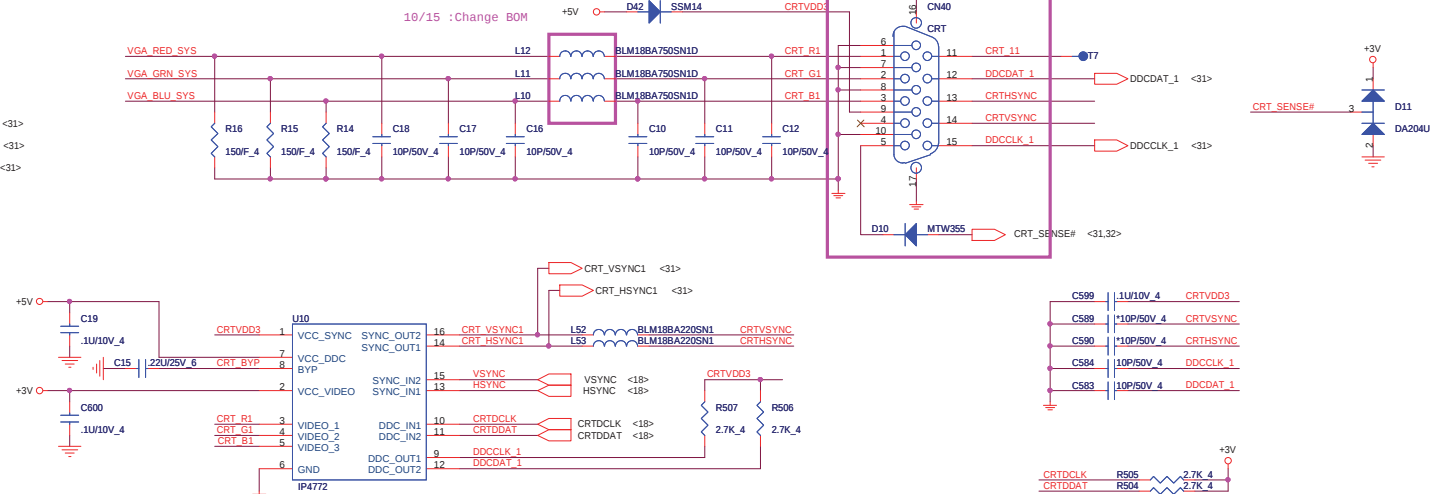


CRT Select

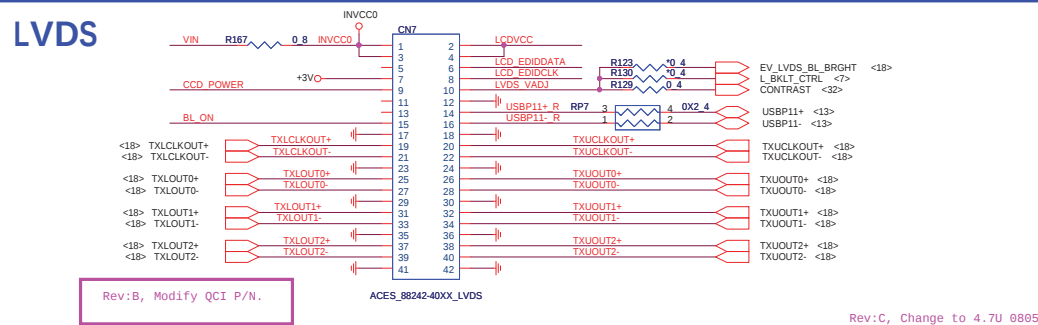
CRT SWITCH



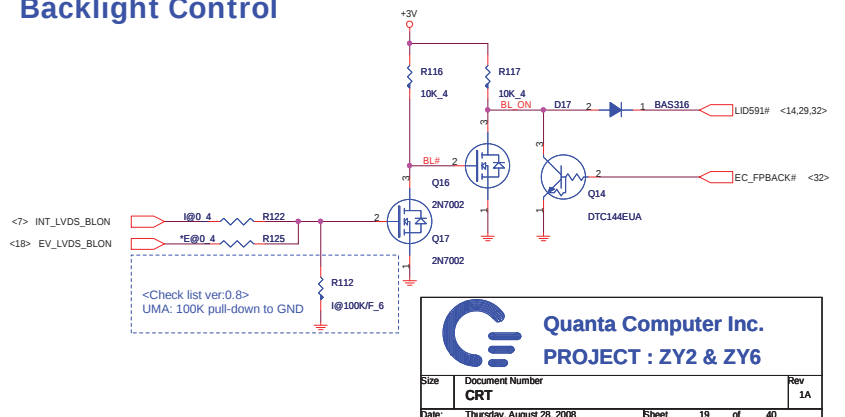
CRT CONNECTOR AND ESD



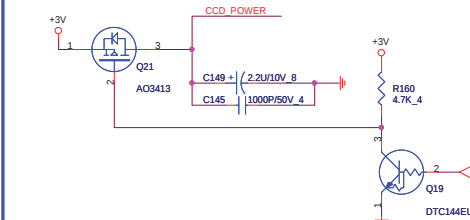
LVDS



Backlight Control

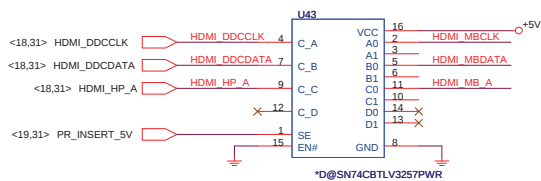
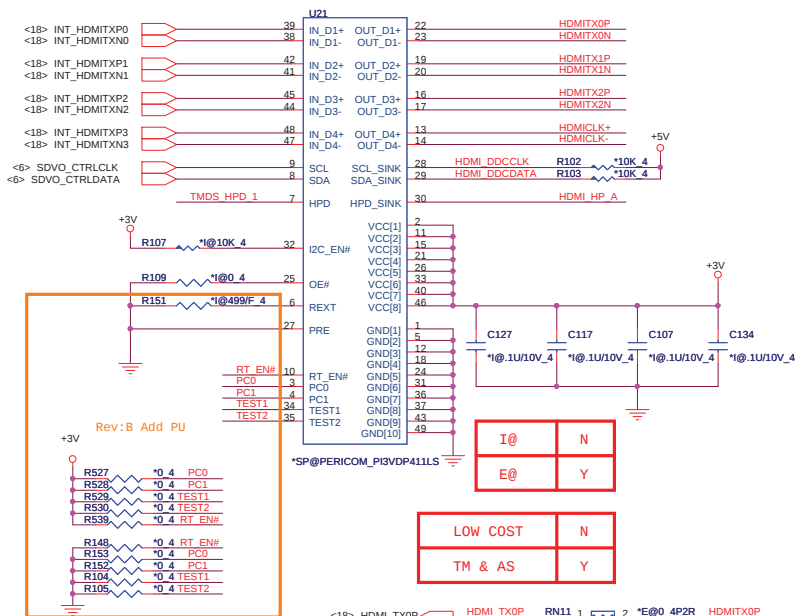


CAMERA MODULE CONNECTOR

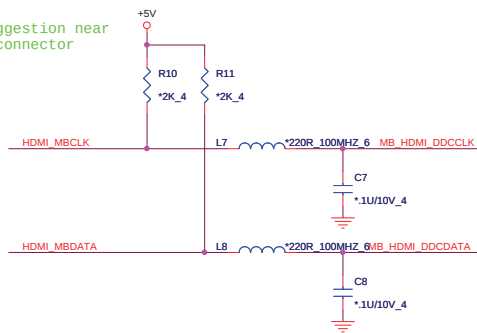


DVI-I CONNECTOR (DVI-D)

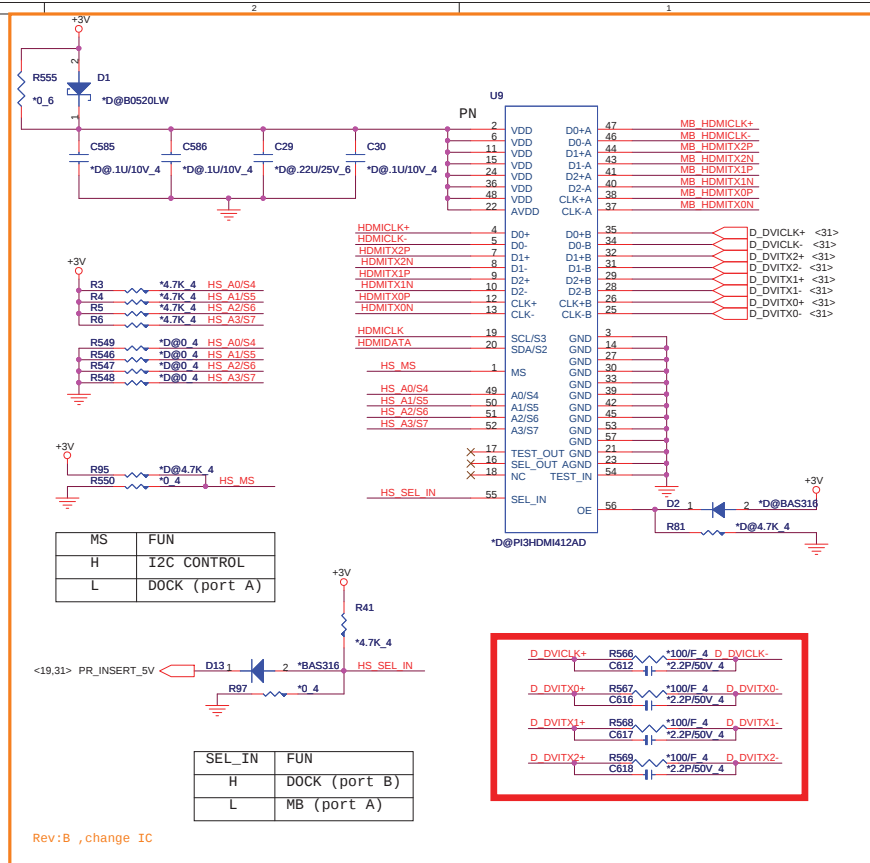
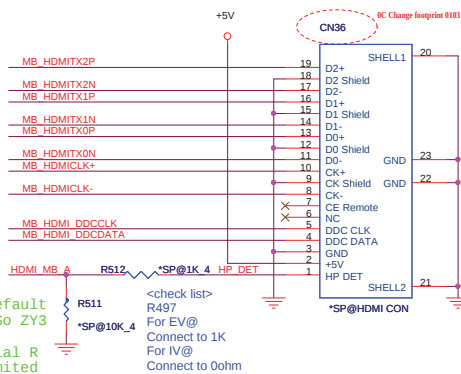
	QCI P/N
PI3VDP411LS	ALP411LS000
Ch7318A	AL007318000
PS8101	



NV suggestion near HDMI connector



HDMI monitor default have PU to 5V. So ZY3 PD for level change. And serial R for current limited



Rev:B ,change IC

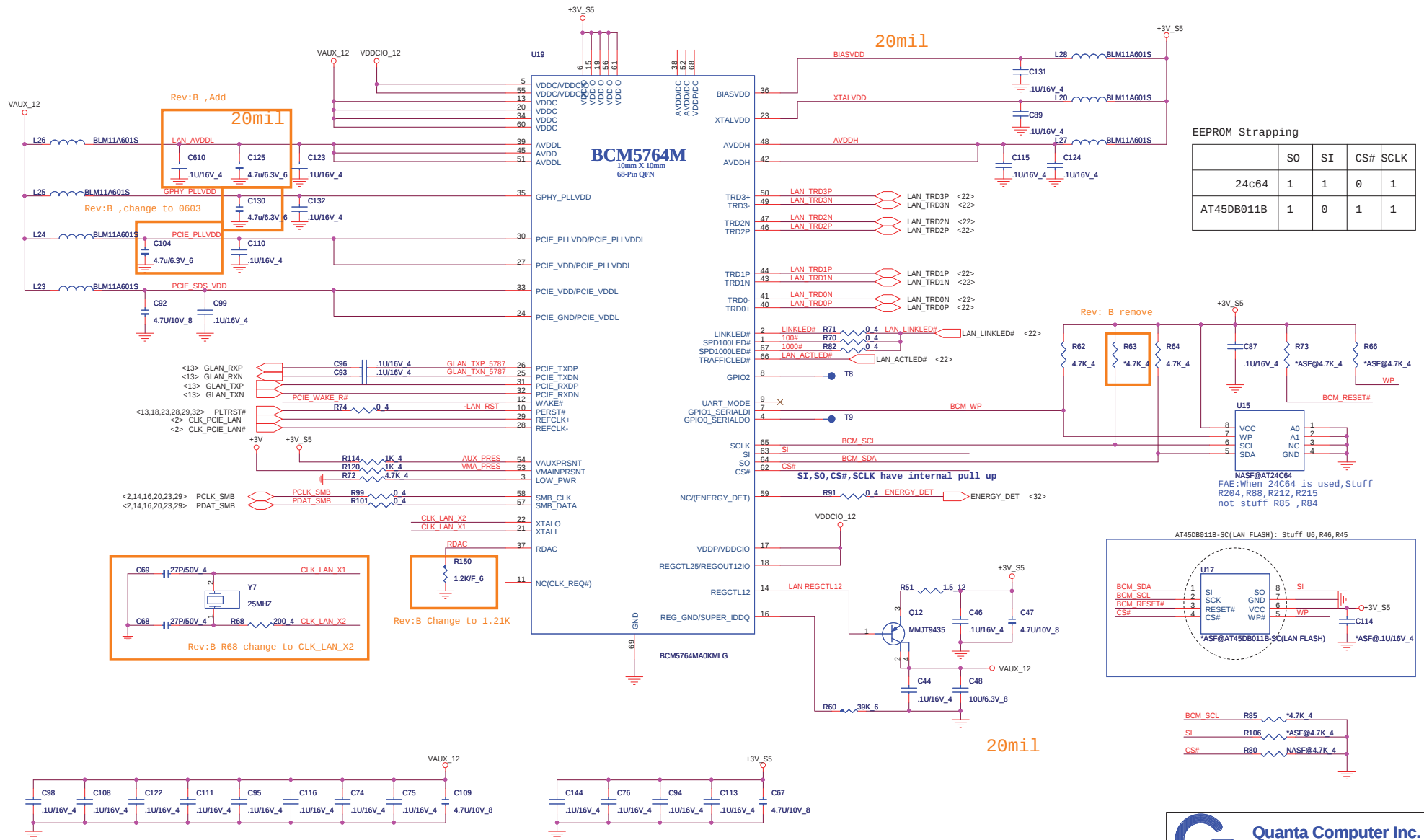
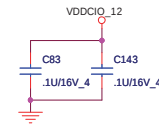
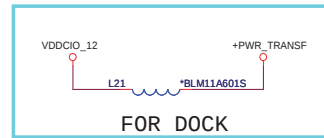
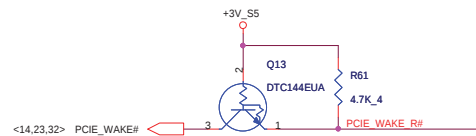
SEL_IN	FUN
H	DOCK (port B)
L	MB (port A)

LOW COST	N
TM & AS	Y

Quanta Computer Inc.
PROJECT : ZY2 & ZY6

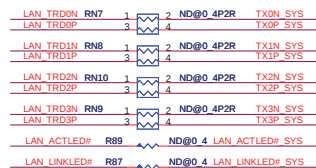
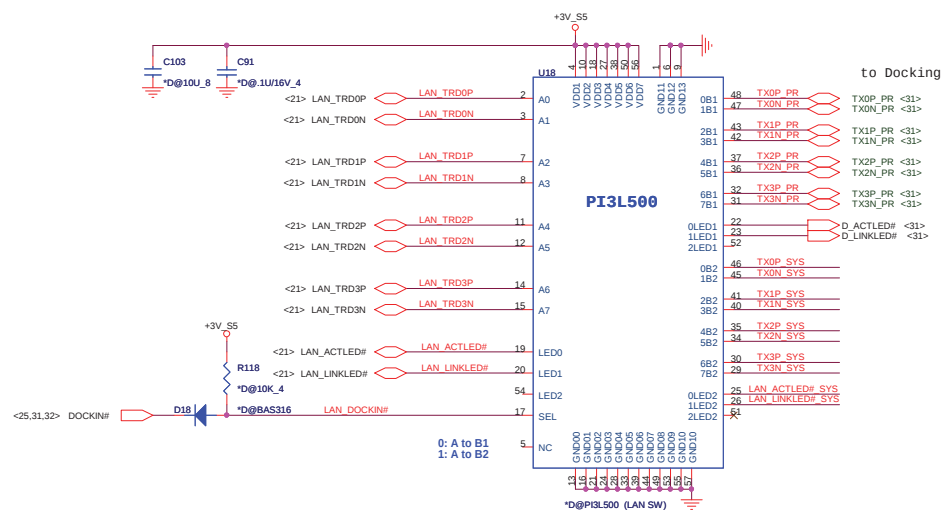
Size	Document Number	Rev
	LVDS/CAMERA/LID	1A
Date:	Tuesday, August 12, 2008	Sheet 20 of 40

LAN



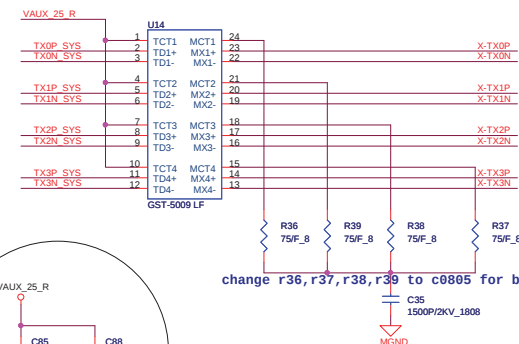
Low is normal, H->Turn Off 1.2V,
H(>0.7V <2.5V)->L will internal
reset

LAN SWITCH

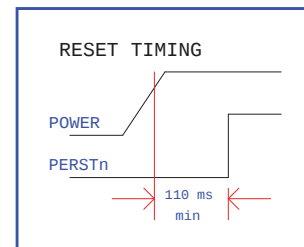
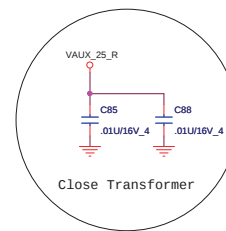


Transformer

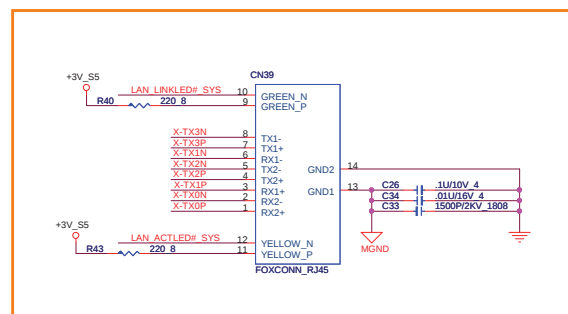
Source 1:	DELTA	LFE9249	DB0ZR1LAN11
Source 2:	Bothand	GST5009	DBKN1NLAN03



change r36,r37,r38,r39 to c0805 for burn out issue July 12th

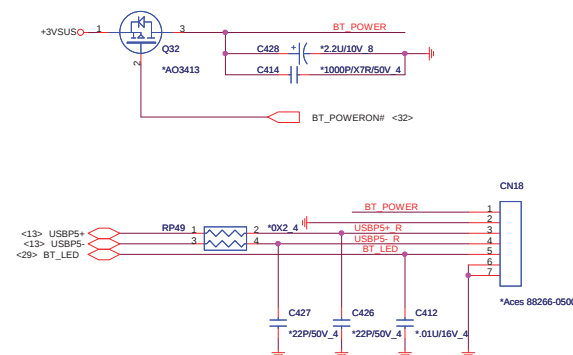


RJ45-11



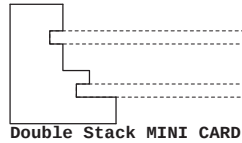
9/29: change footprint
11/27 :change footprint
11/28 : R43 & R40 Change to 0805
1/31 :Rev: C change PIN define about 9,10,11 & 12

BLUETOOTH MODULE CONNECTOR



Size	Document Number	Rev
	BT/CCD/RJ45-11/CIR/2nd FAN	1A
Date:	Thursday, August 28, 2008	Sheet 22 of 40

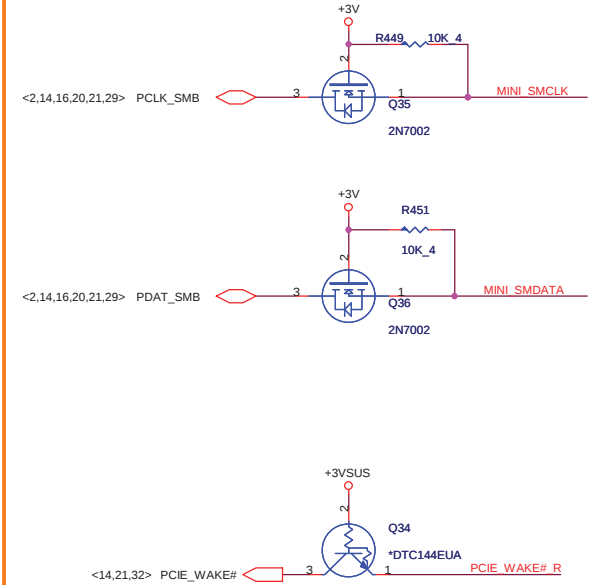
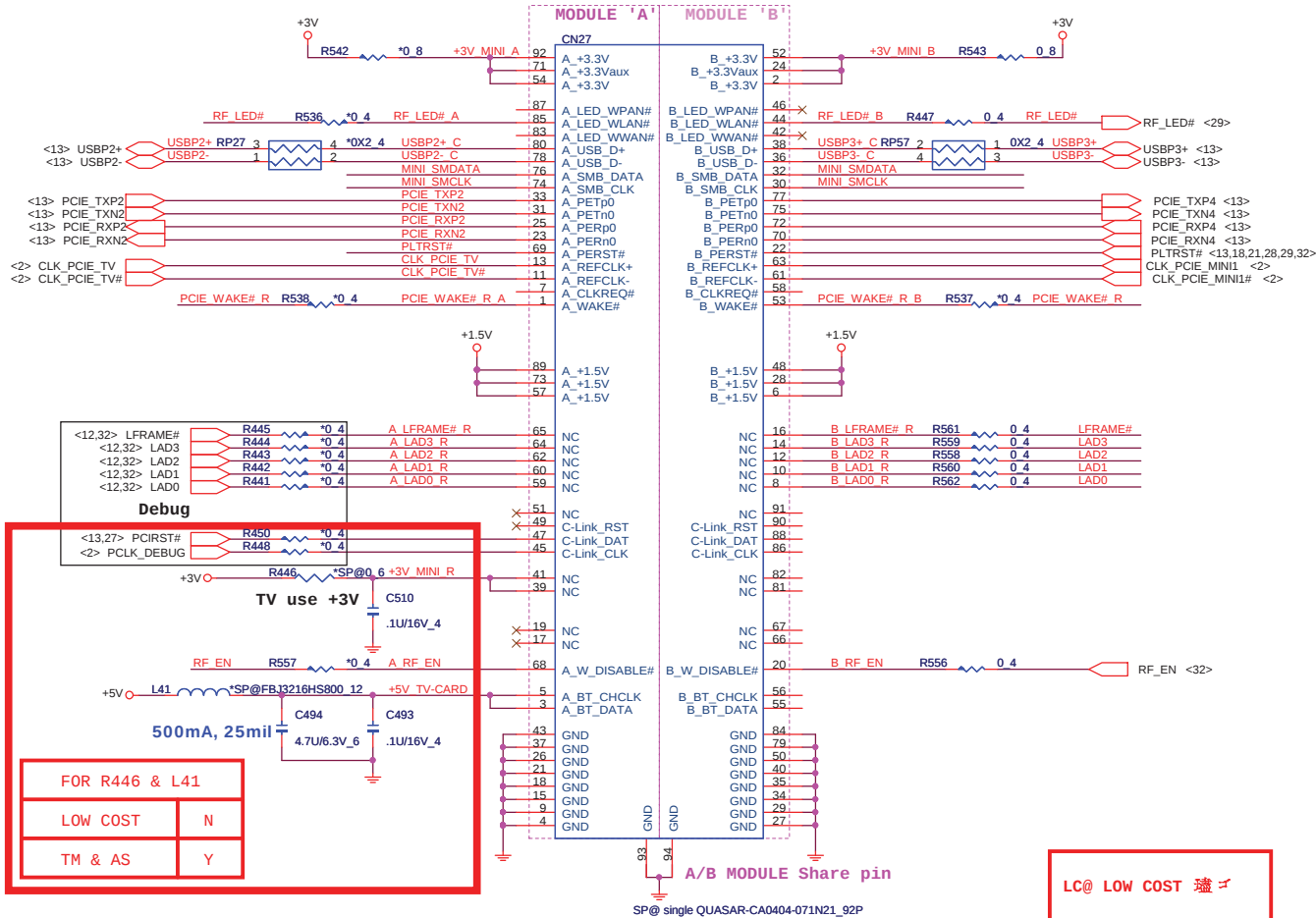
MINI-CARD



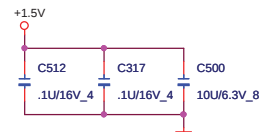
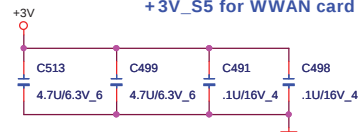
MODULE 'A' TV card

MODULE 'B' Wireless card

Rev:B PIN36,38 Add USB3
PIN69 Add R536
PIN1, 53 Add R537 & R538

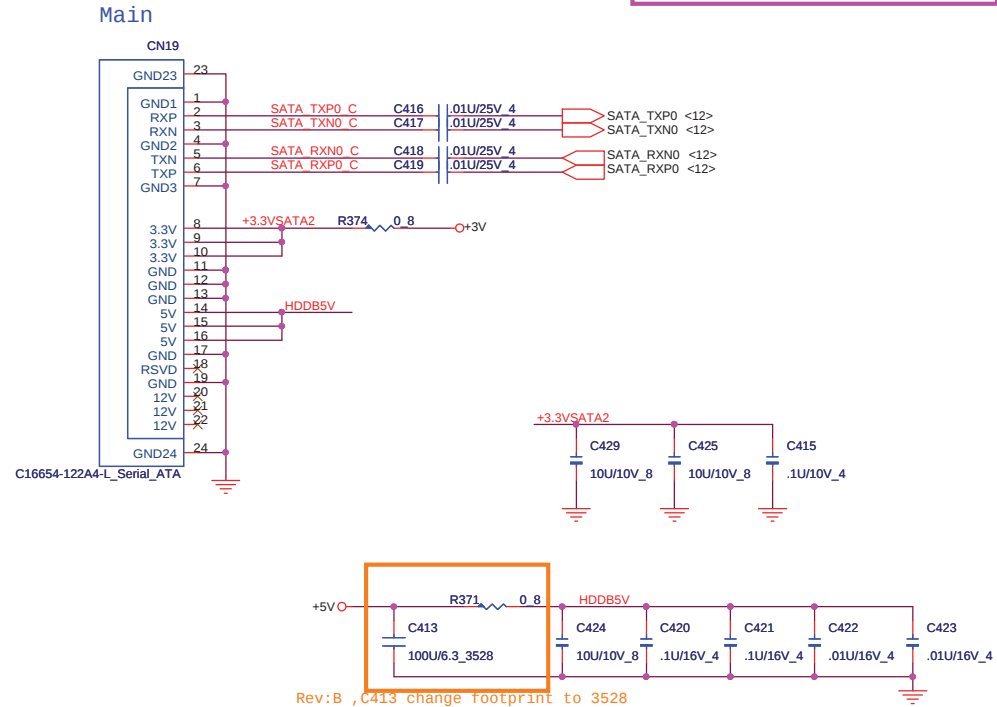


+3V_S5 for WWAN card is 2.75A

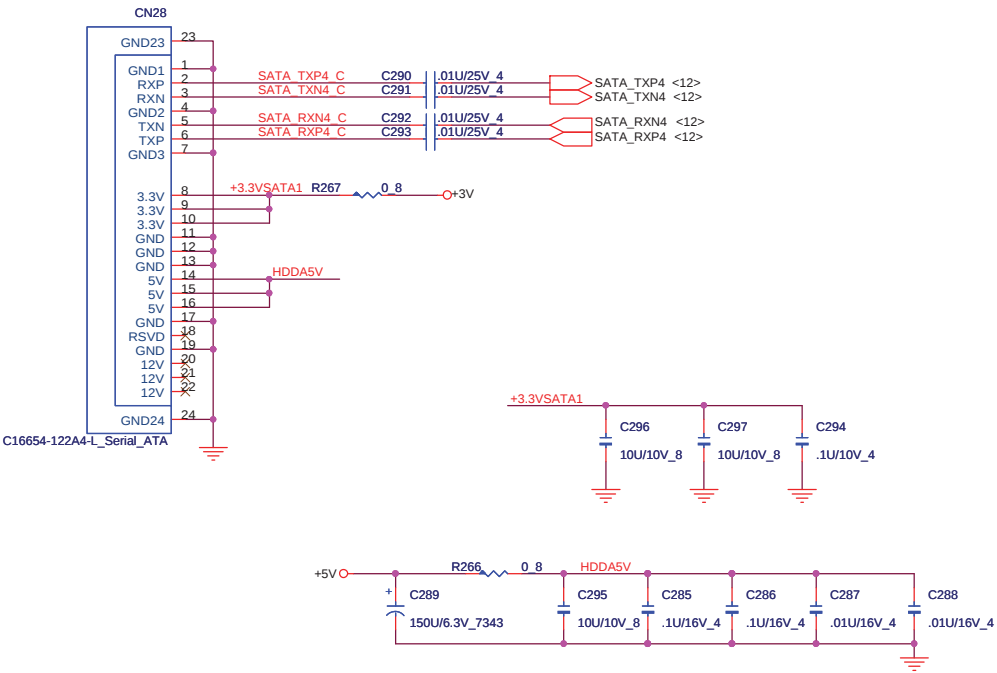


SATA HDD

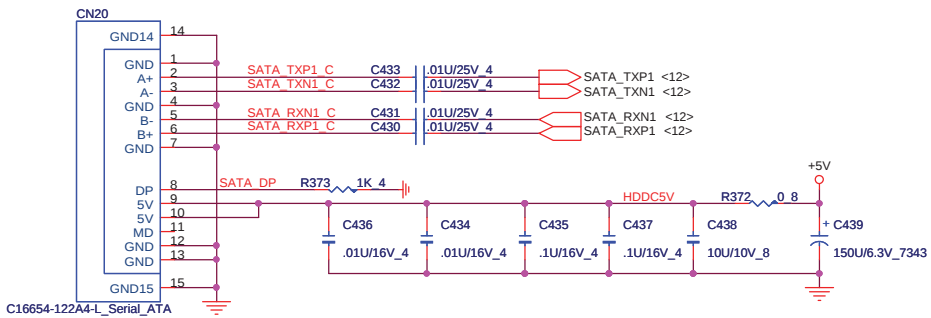
11/8 REV:B Conn. 奔癸粘 CN28 & CN19



2ND SATA HDD

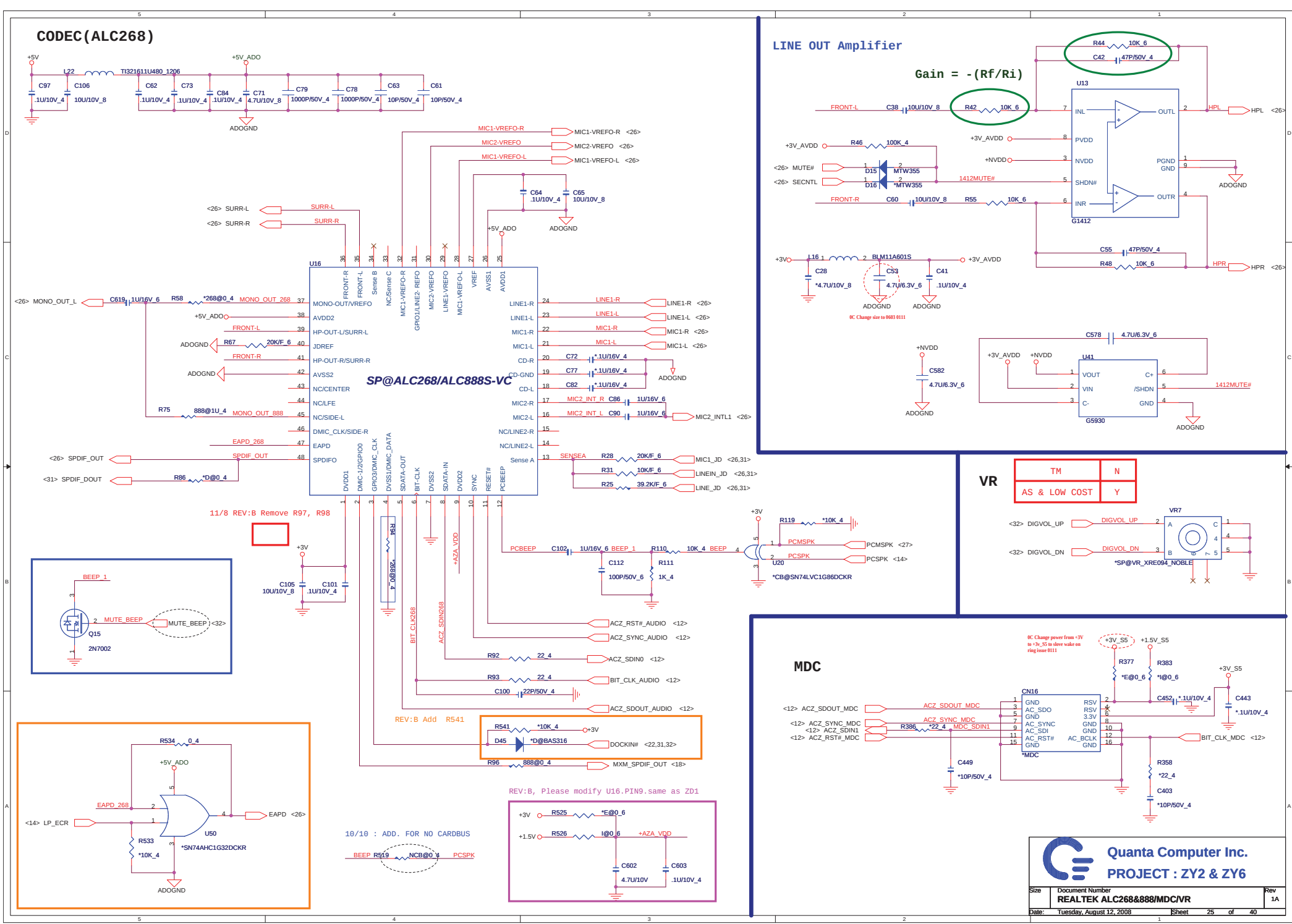
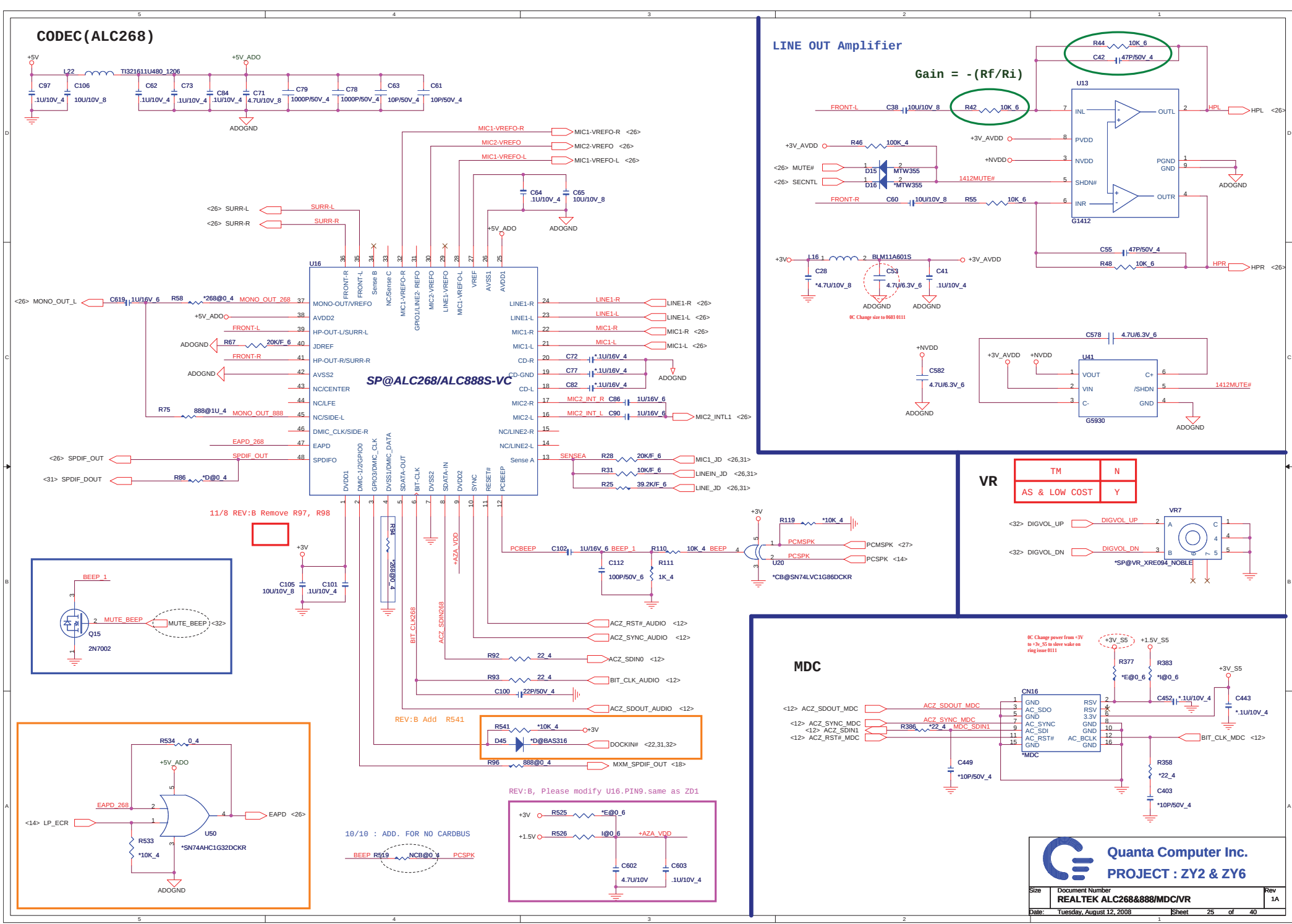
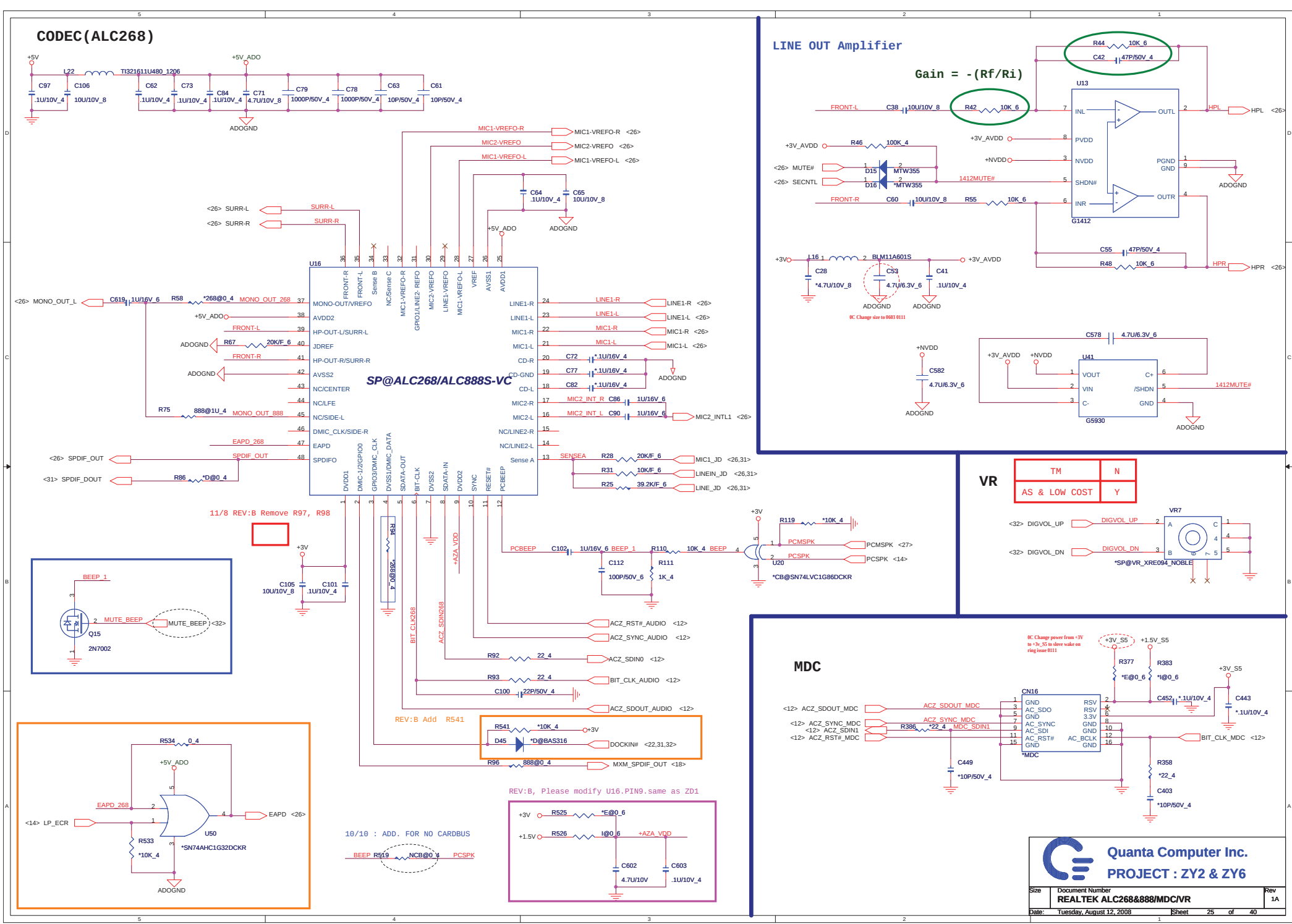
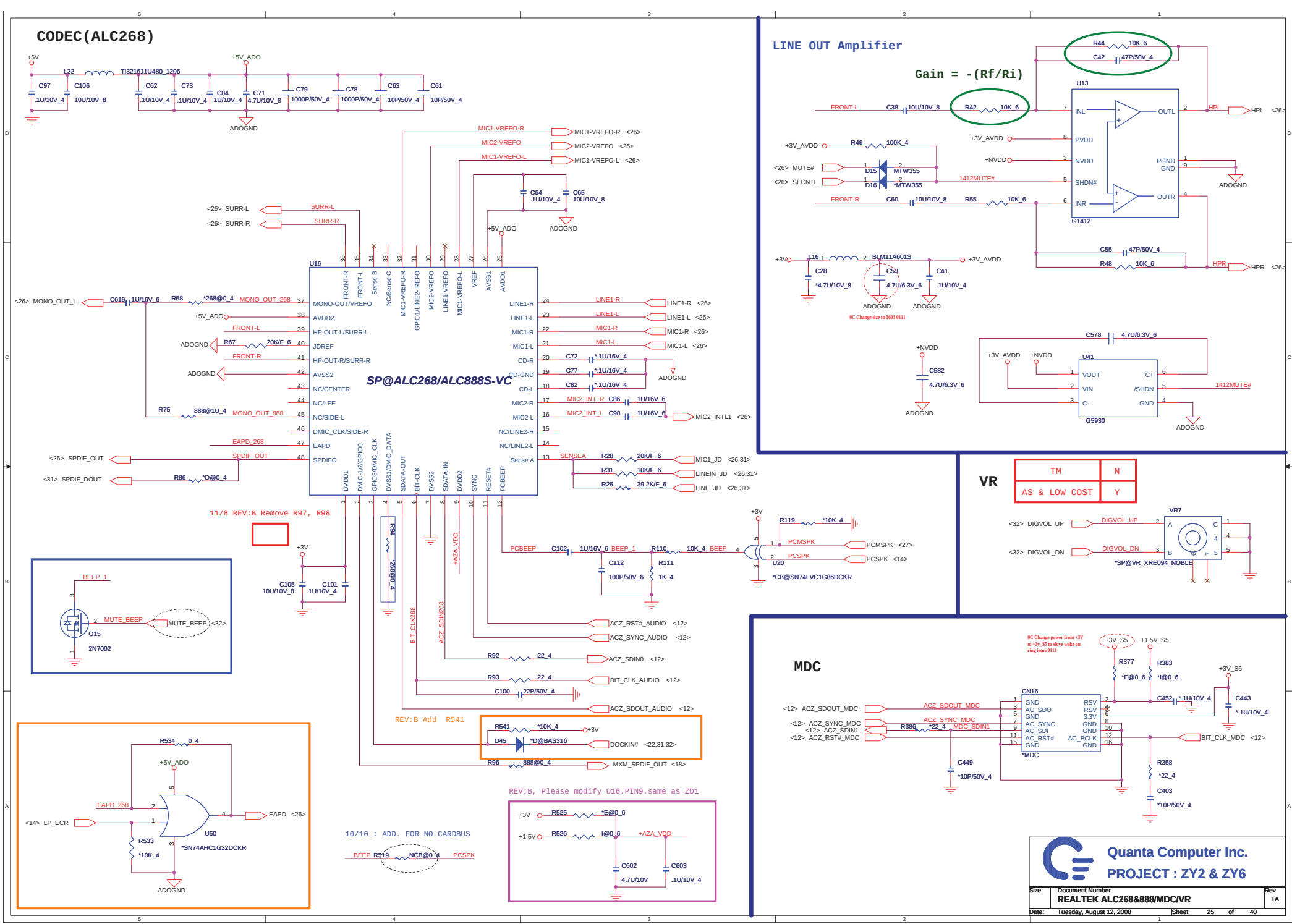
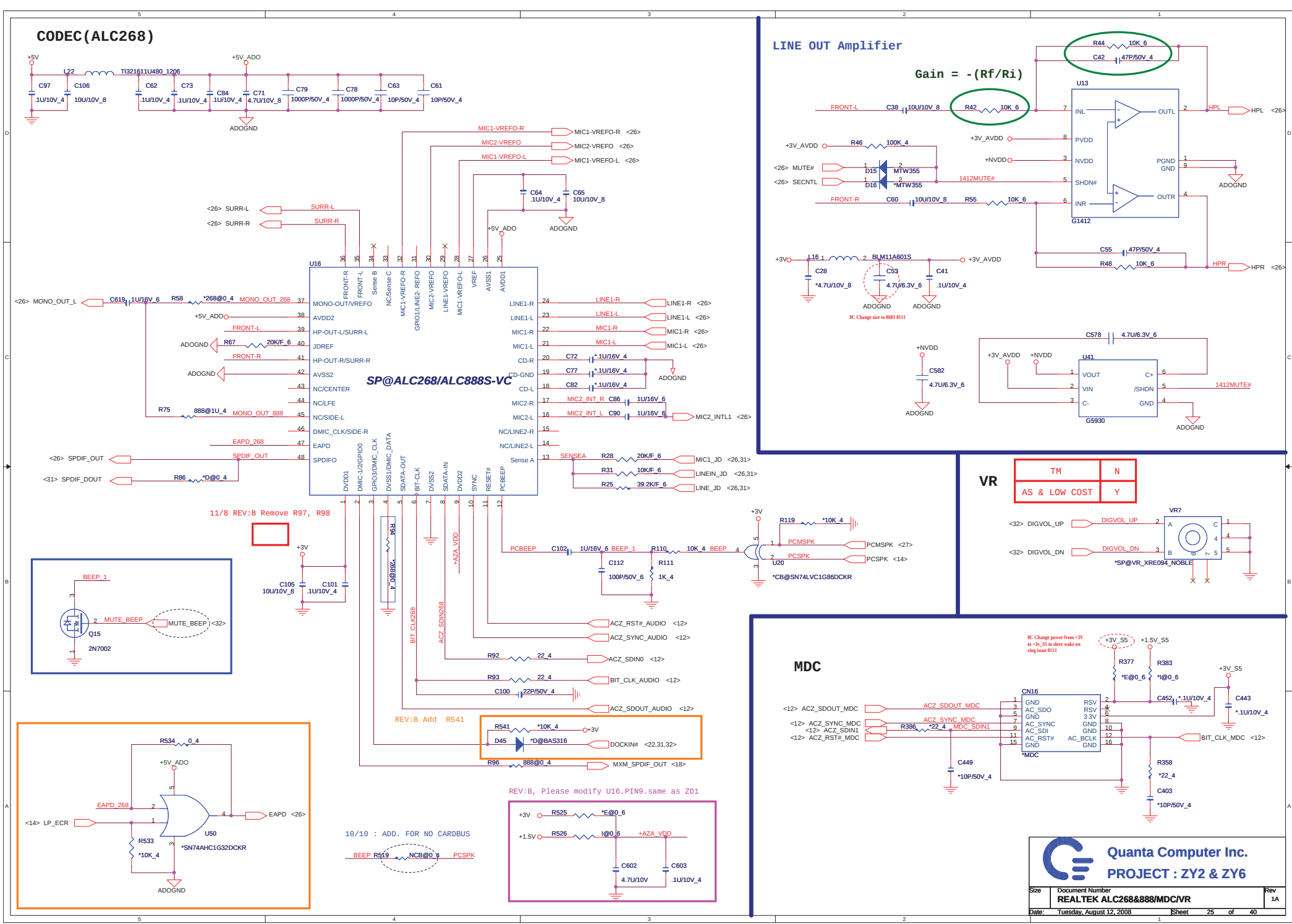


ODD (SATA)

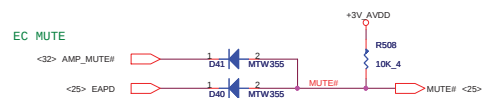
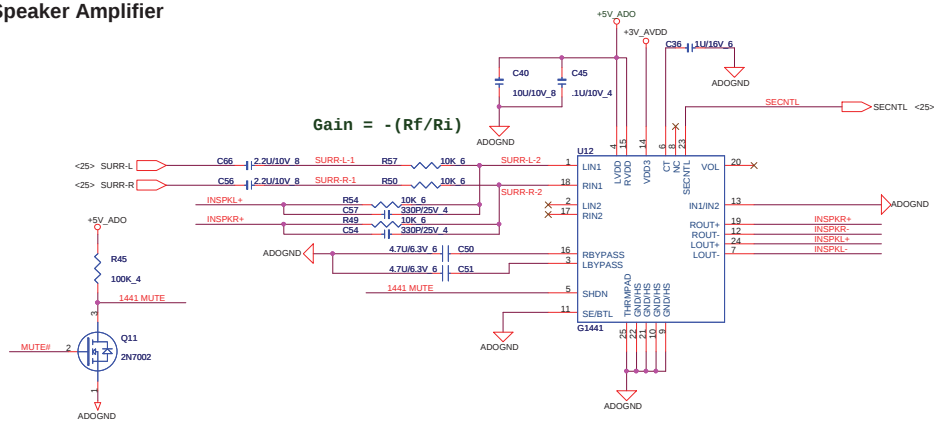


Quanta Computer Inc.
PROJECT : ZY2 & ZY6

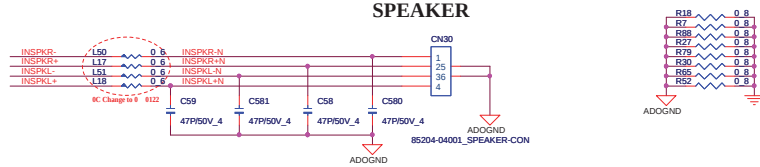
Size	Document Number	Rev
	SATA-HDD & ODD	1A
Date:	Wednesday, August 13, 2008	Sheet 24 of 40



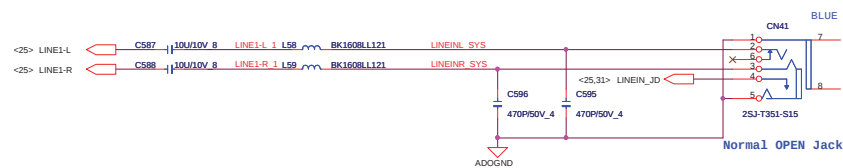
Speaker Amplifier



SPEAKER



SYSTEM LINE IN/SUBWOOFER



D2C: NEW ADD FOR ESD

LINEIN_JD

D8

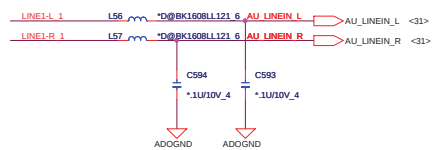
DA204U

For ESD close to audio out connector

ADOGND

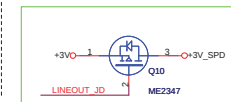
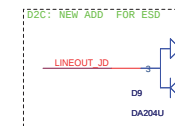
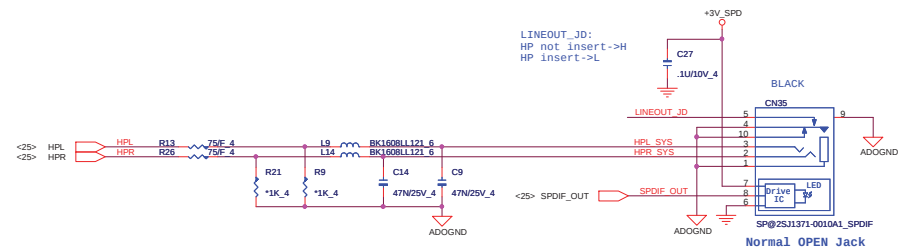
Singatron DFTJ06FR732 2SJ-T351-S15
Foxconn DFTJ06FRA21 JA6233L-U3T4-7F
Alltop DFTJ06FR902 C12107-906A9-L

Docking LINE IN

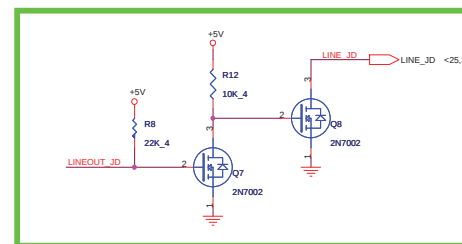


TM & LOW COST	N
AS	Y

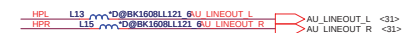
SYSTEM LINE OUT/SPDIF



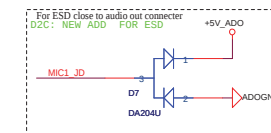
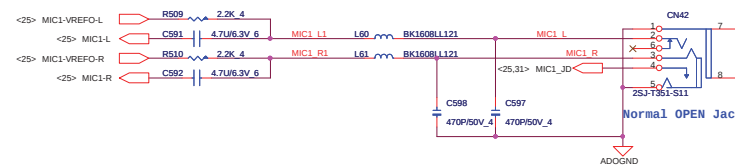
Foxconn DFTJ10FR470 2FB5441-BKMC-7F
Singatron DFTJ10FR437 2SJ1371-0010A1



Docking LINE OUT/SPDIF

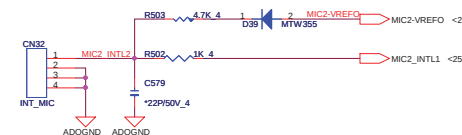


MIC



Singatron DFTJ06FR741 2SJ-T351-S11
Foxconn DFTJ06FRA39 JA6233L-P3T4-7F
Alltop DFTJ06FR899 C12107-D06A9-L

INT MIC array



THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

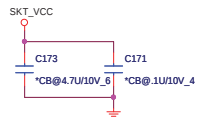
THIS DEVICE UTILIZES A "SELECTABLE IODEL" SCHEME. IODEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IODEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IODEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS

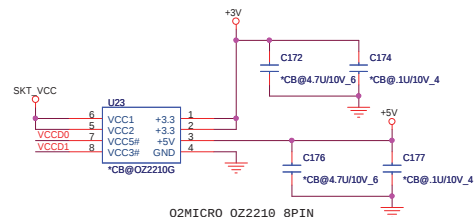
CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCCS# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

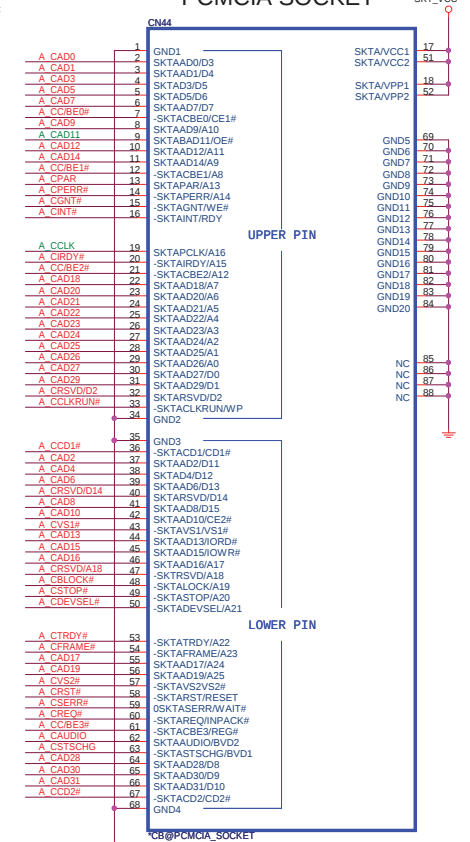
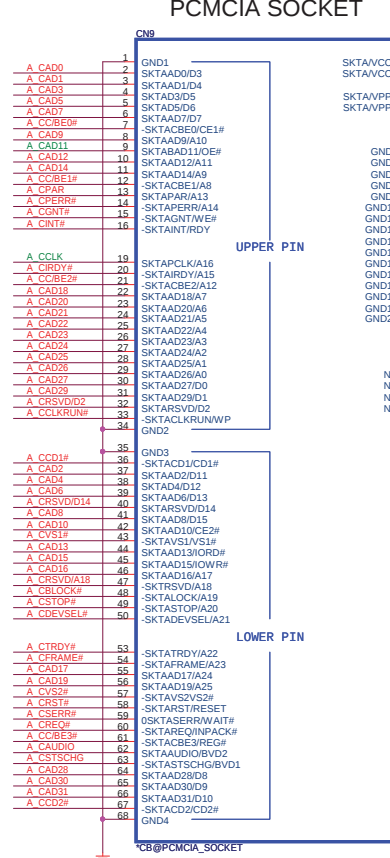
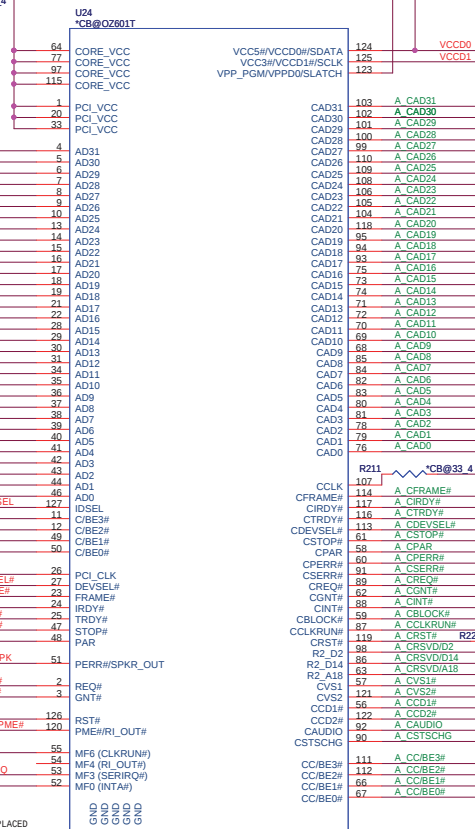
ID Select : AD20
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#



22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.

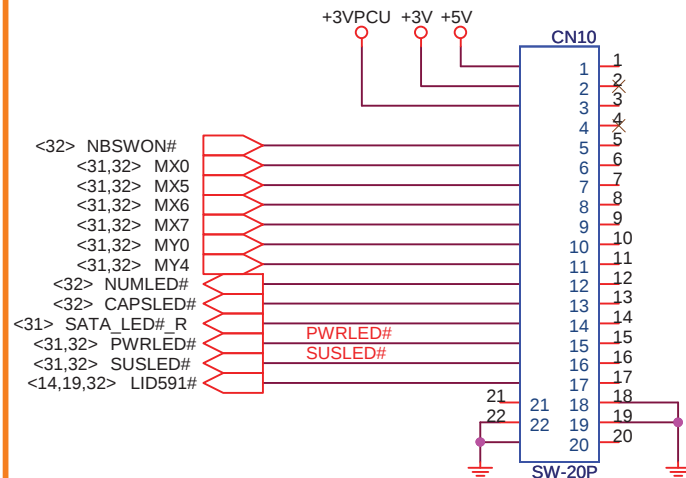


02MICRO 0Z2210 8PIN
SINGLE SLOT PARALLEL
POWER SWITCH

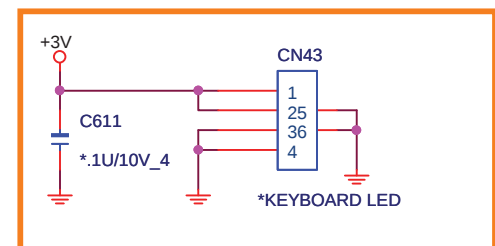
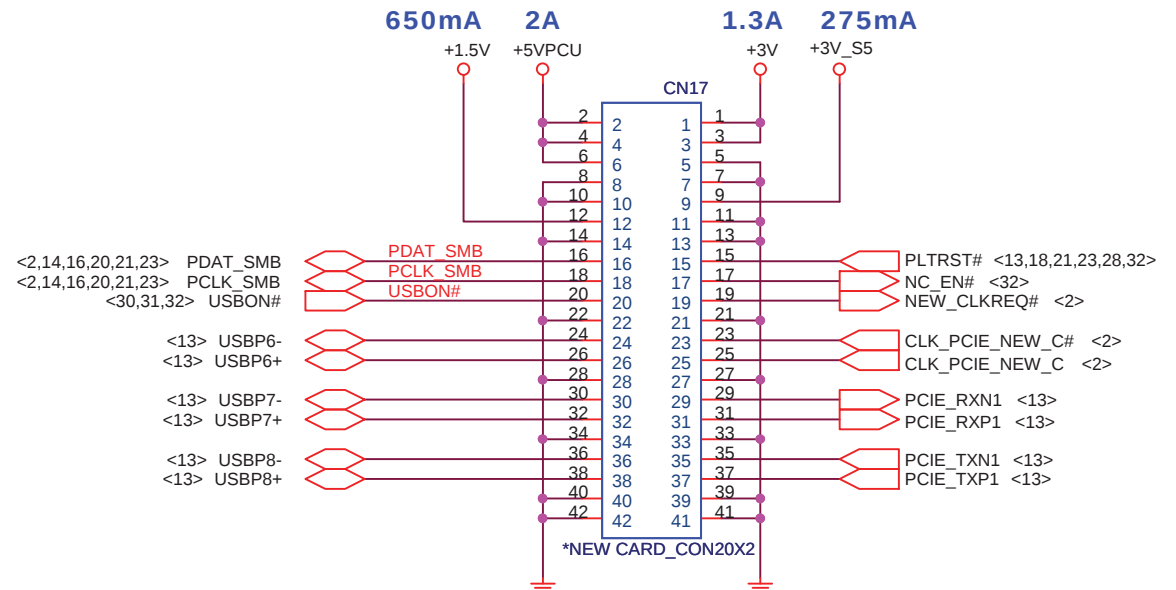
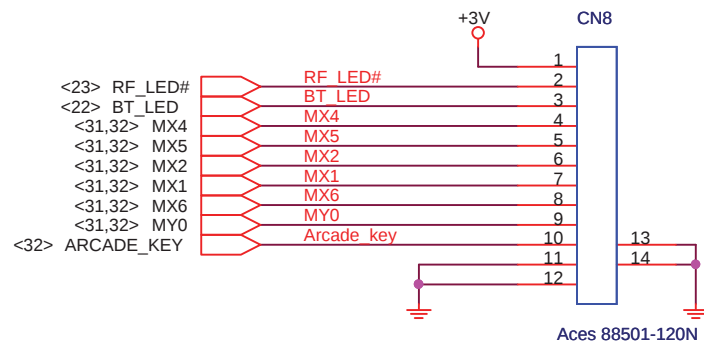


To NEW-CARD & EXT. USB

REV:B, CN10 change footprint



REV:B, Please change PIN define.same as ZY5
CN8 change footprint



Rev:B Add CN43 For backlight KB

Rev:B Change to 蛾 to 丩PAD
C255, C234, C221, C199, R217, C198, R183,
R182, R174, R257, R324, R335, R334, R349, C395

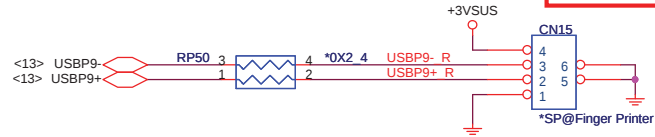
Fncion	Keyboard Matrix
E-KEY	MX0/ MY0
E-Mail	MX1/ MY0
E-WWW	MX2/ MY0
3G/TV	MX3/ MY0
Wireless	MX4/ MY0
BlueTooth	MX5/ MY0
P-KEY	MX6/ MY0
Presentation	MX5/ MY4
Lock	MX6/ MY4
Sync	MX7/ MY4



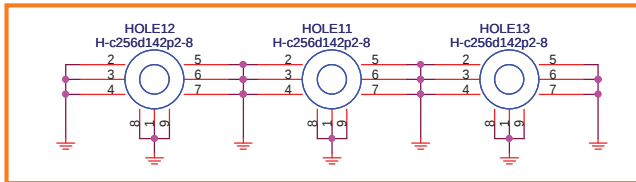
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Finger Printer

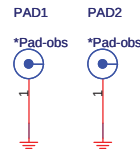
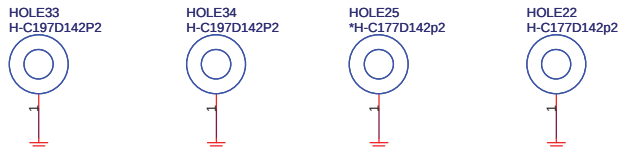
TM & AS	Y
LOW COST	N



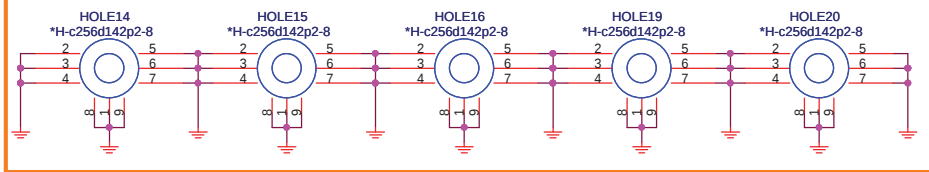
HOLES CPU NUT (BOT)



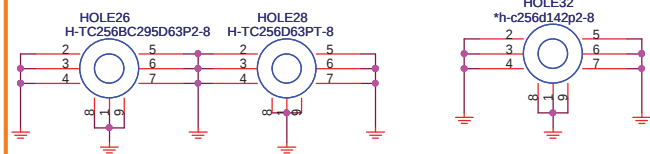
Rev : B Add MINI NUT



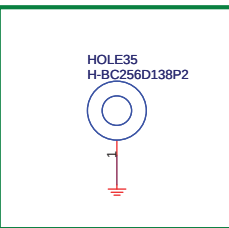
MXM NUT (BOT)



MDC NUT (TOP)

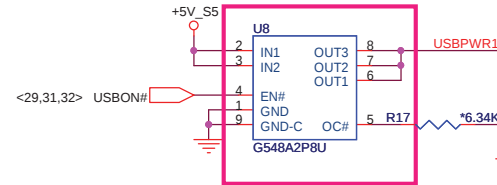


Rev:B New add HOLE32
HOLE26 & 28 Change footprint

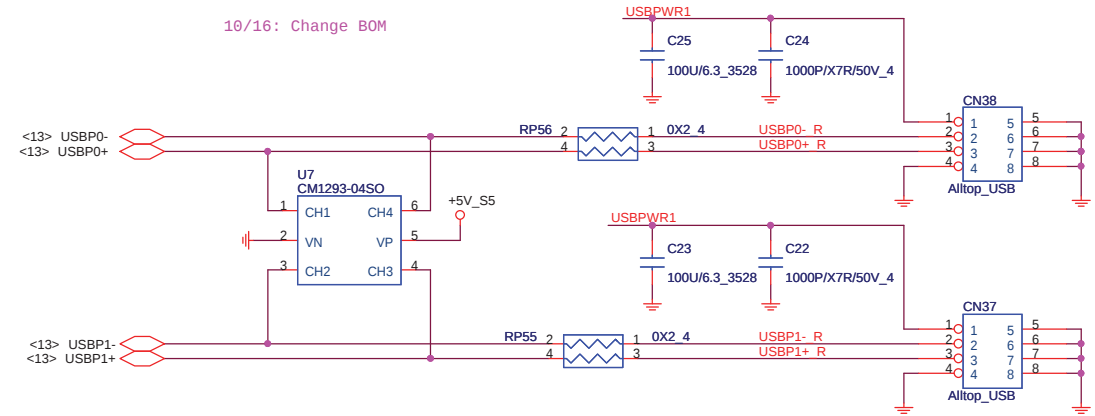


HOLE35 璫槐 BOT

USB

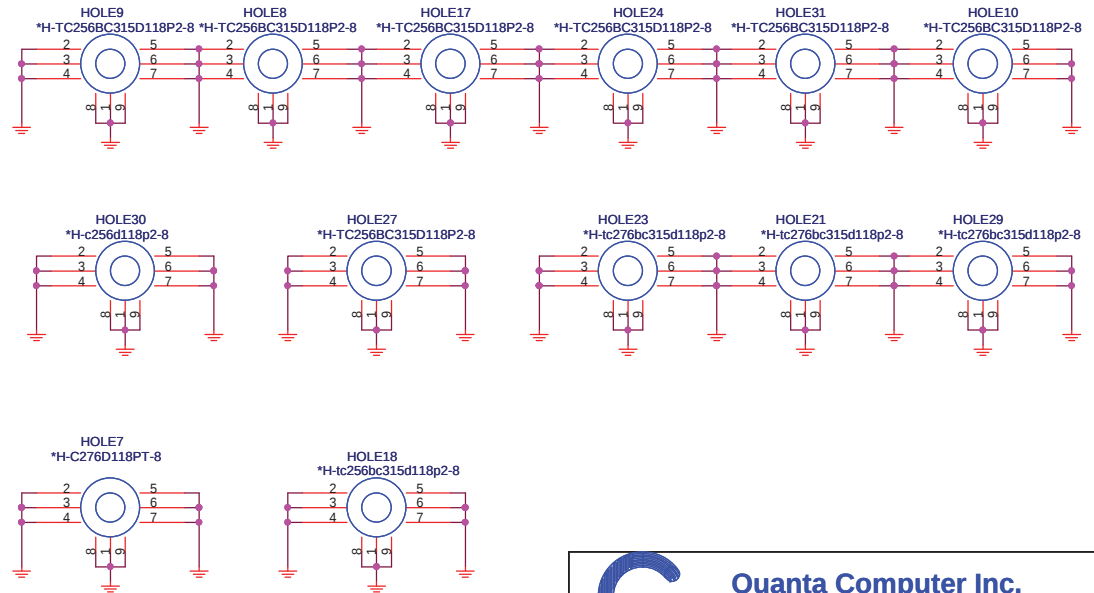


10/16: Change BOM



USBP0- R	D47	2	1	MLVG06031R
USBP0+ R	D48	2	1	MLVG06031R
USBP1- R	D49	2	1	MLVG06031R
USBP1+ R	D50	2	1	MLVG06031R

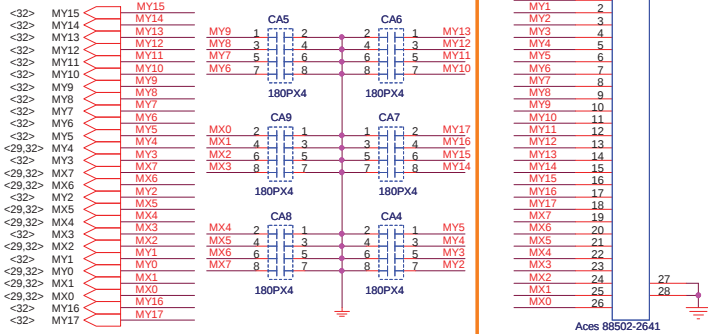
REV:C Modify



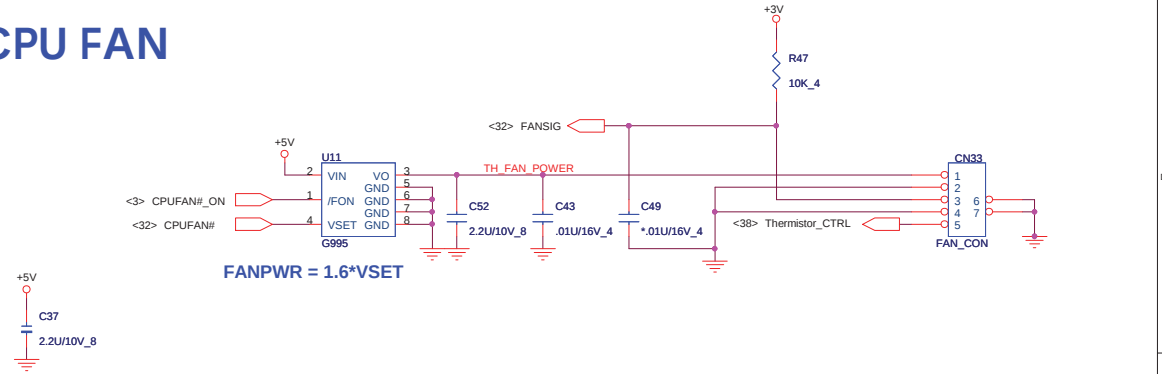
Quanta Computer Inc.
PROJECT : ZY2 & ZY6

Size	Document Number	Rev
	USB/FINGER PRINTER	1A
Date:	Tuesday, August 12, 2008	Sheet 30 of 40

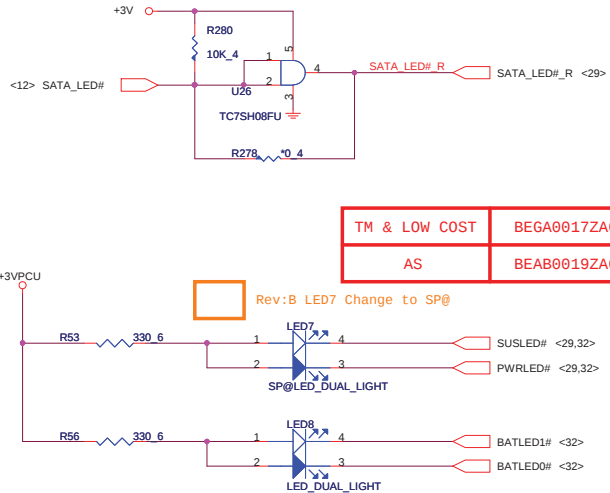
INT K/B



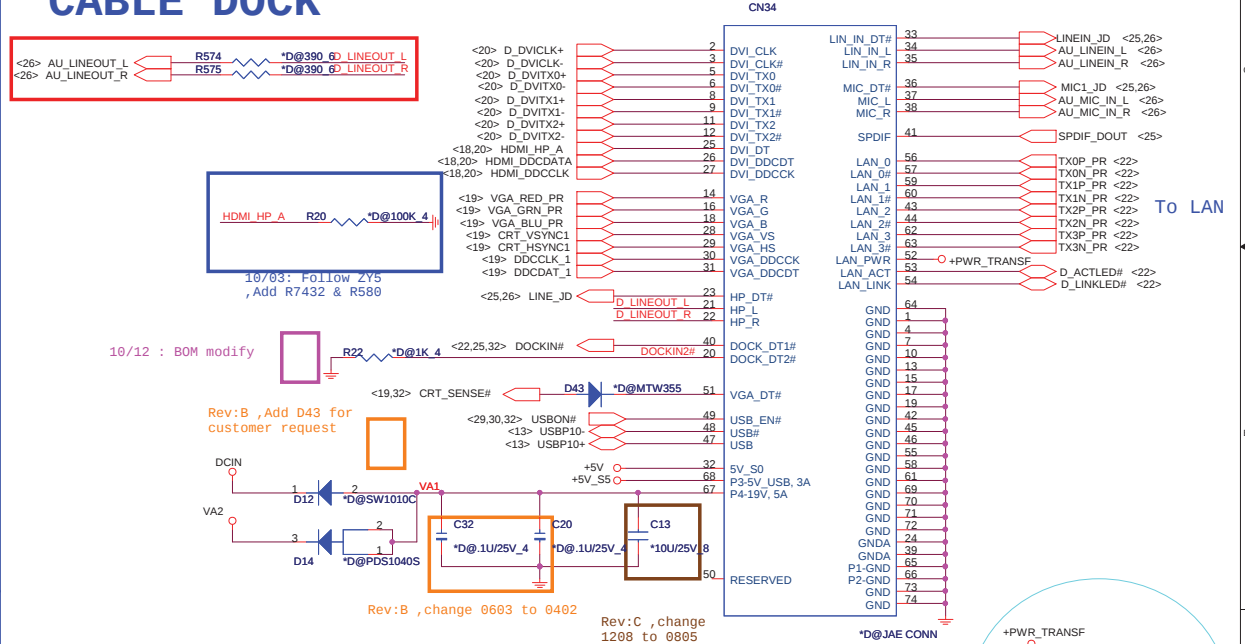
CPU FAN



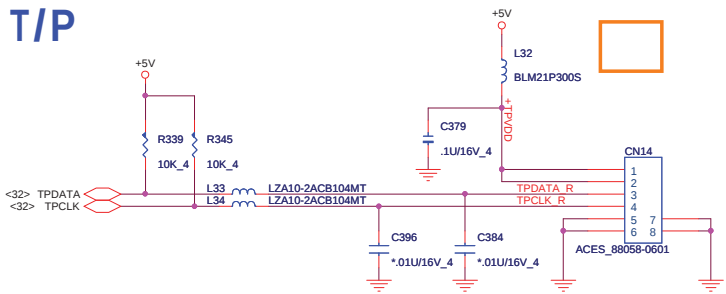
LED



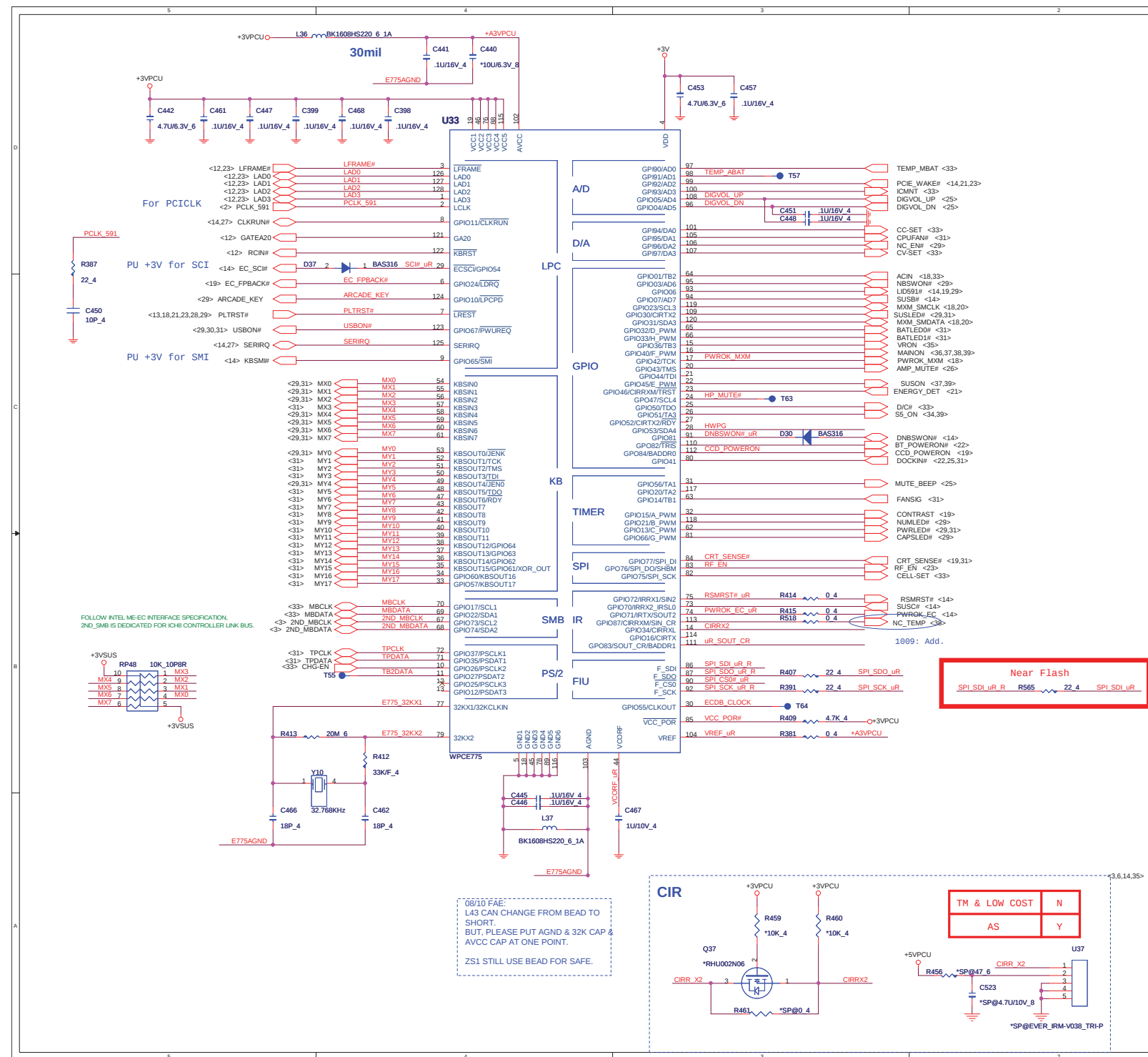
CABLE DOCK



T/P



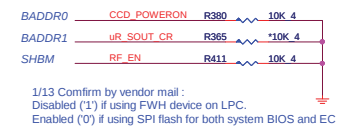
Quanta Computer Inc.
PROJECT : ZY2 & ZY6



I/O ADDRESS SETTING

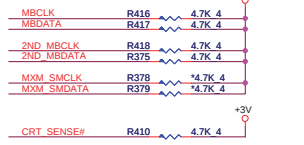
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

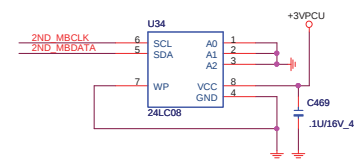


1/13 Confirm by vendor mail :
Disabled (*) if using FW/H device on LPC.
Enabled (0) if using SPI flash for both system BIOS and EC firmware

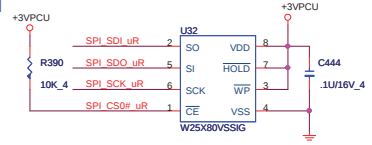
SM BUS PU



ACER ID

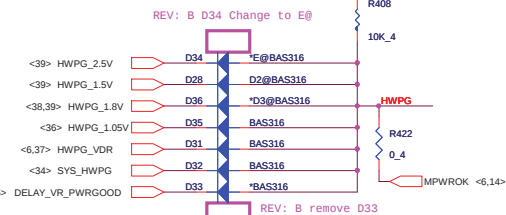


SPI FLASH



1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

H/W POWER GOOD



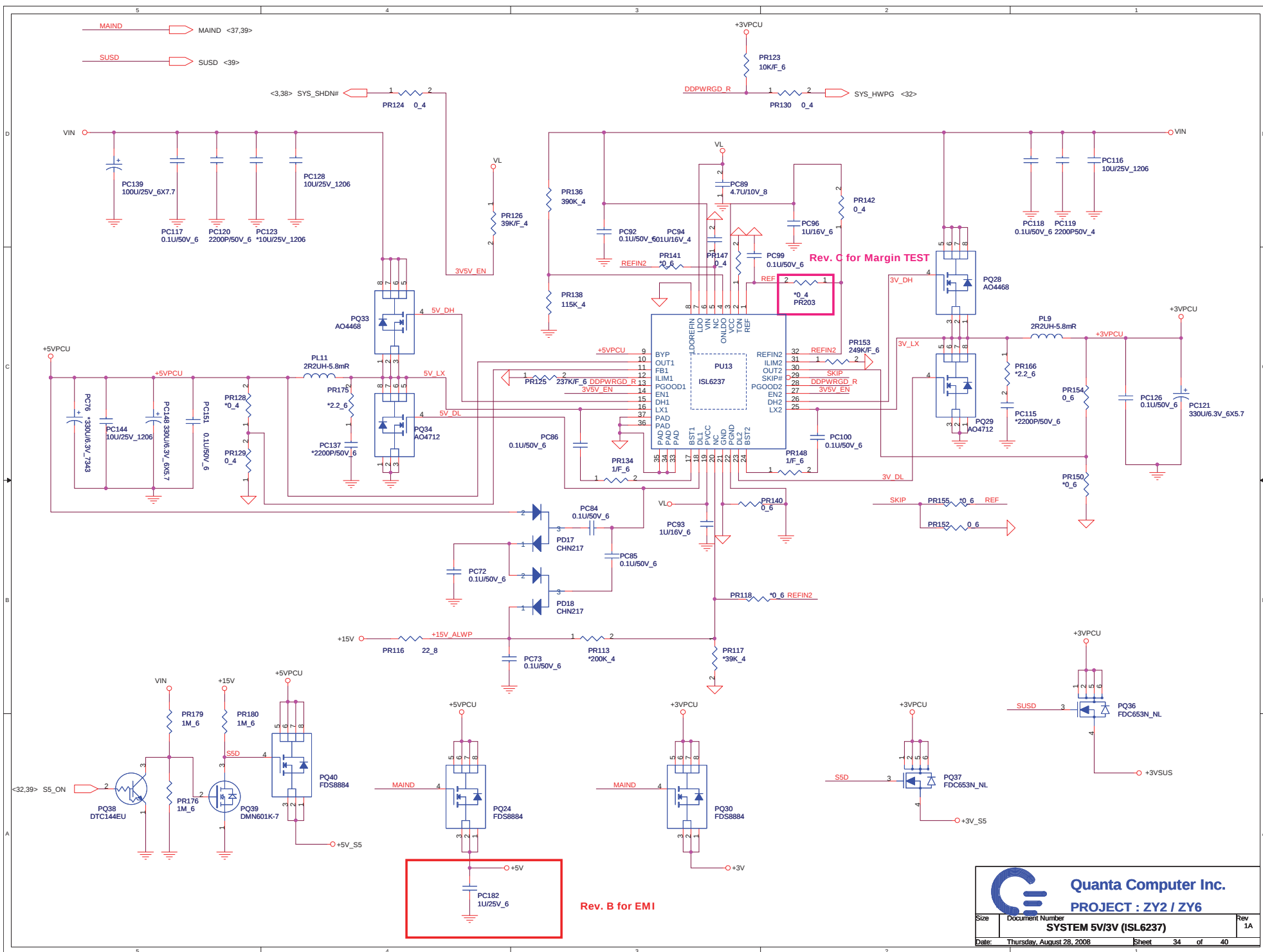
INTERNAL KEYBOARD STRIP SET

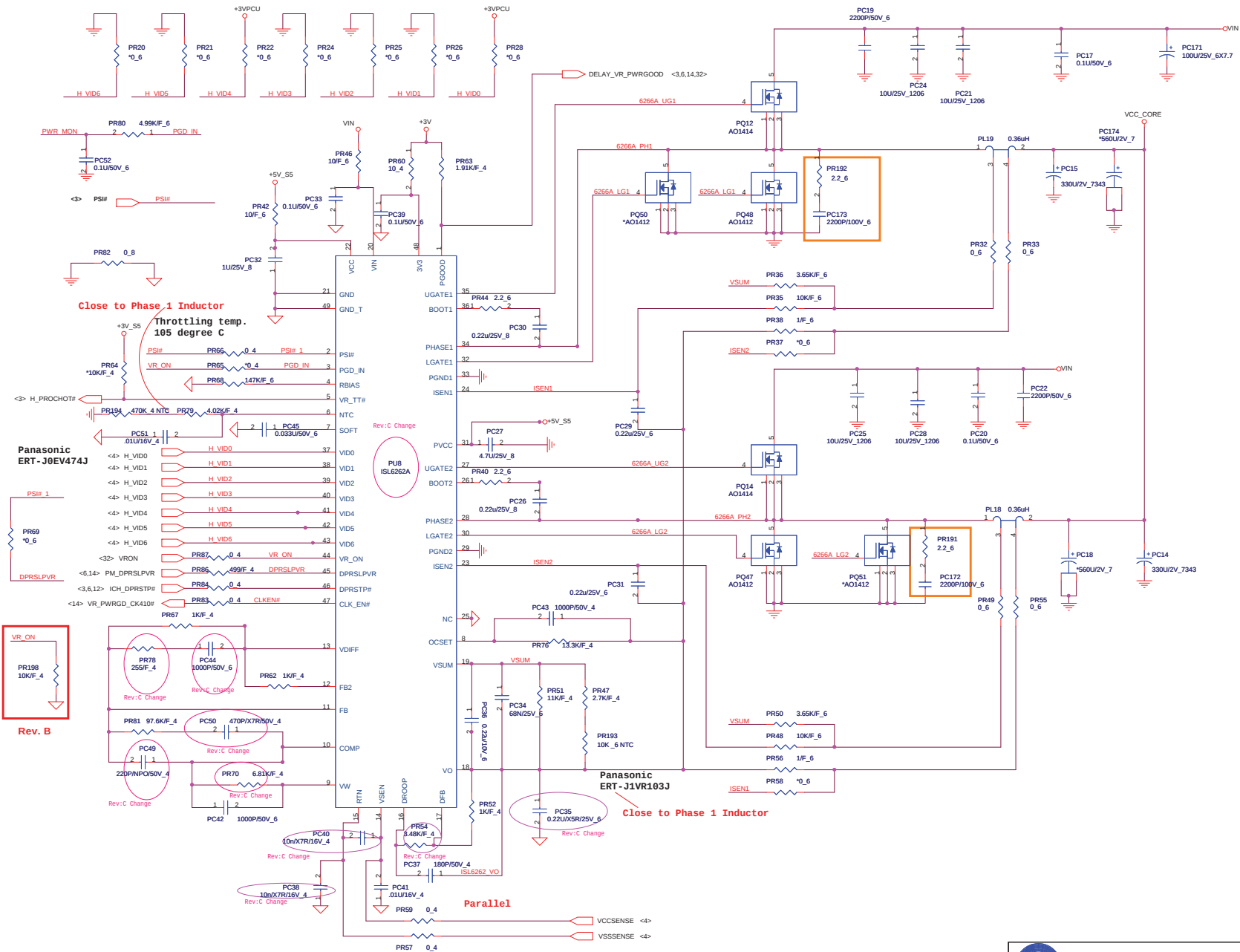


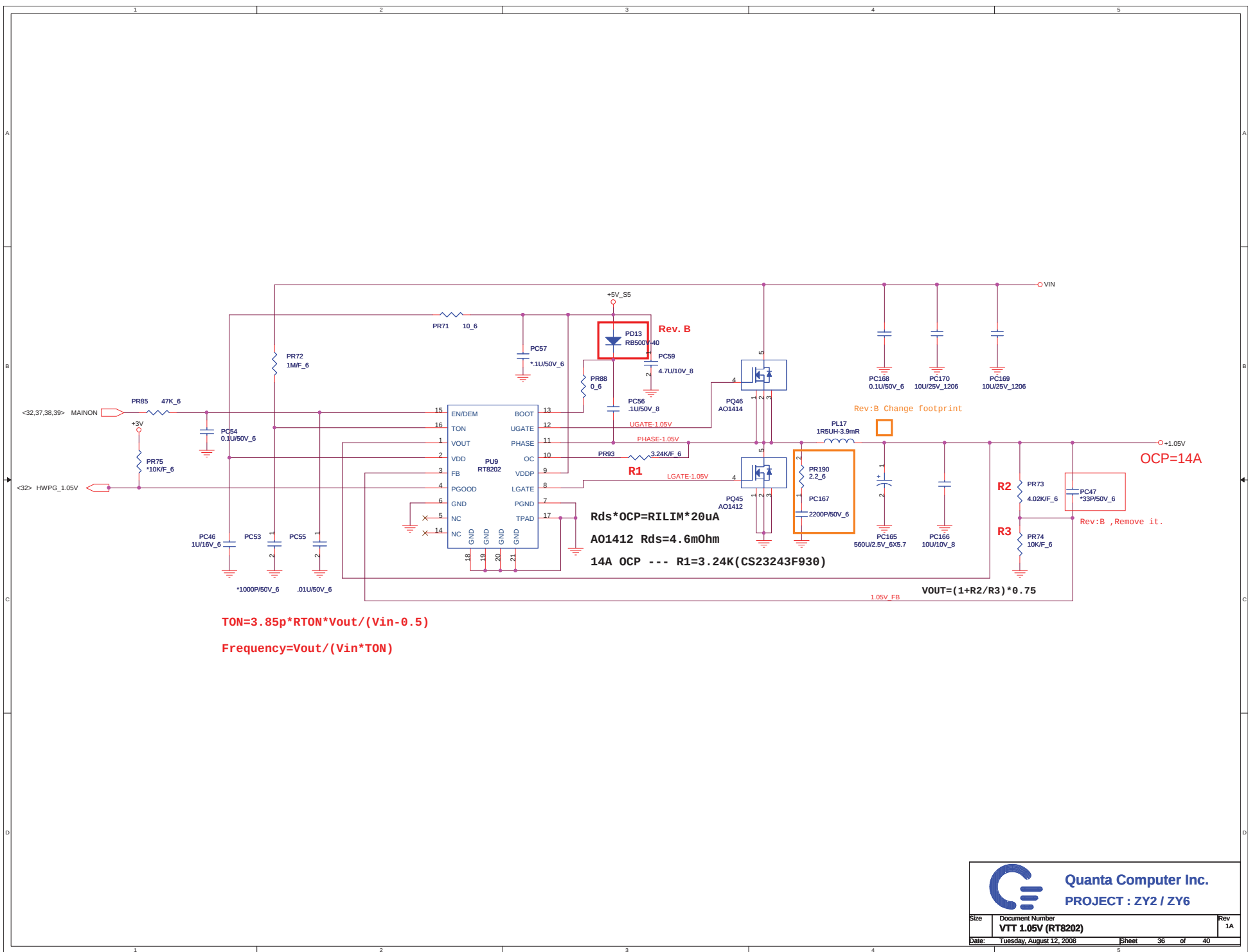
Quanta Computer Inc.
PROJECT : ZY2 & ZY6
WPC75C_0DG & FLASH

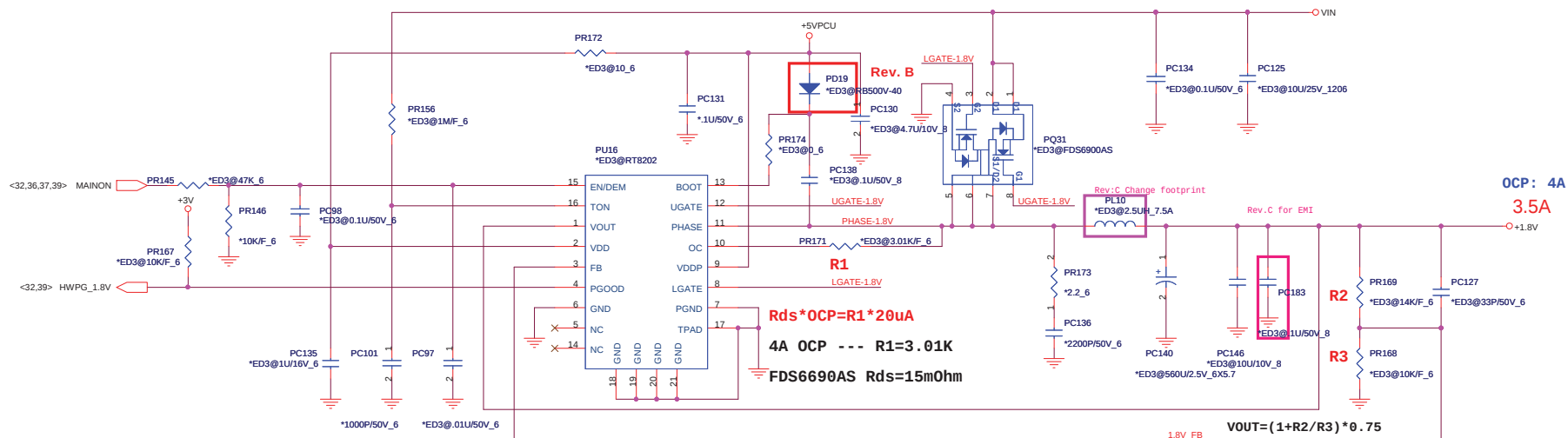
Size	Document Number	Rev
		1A

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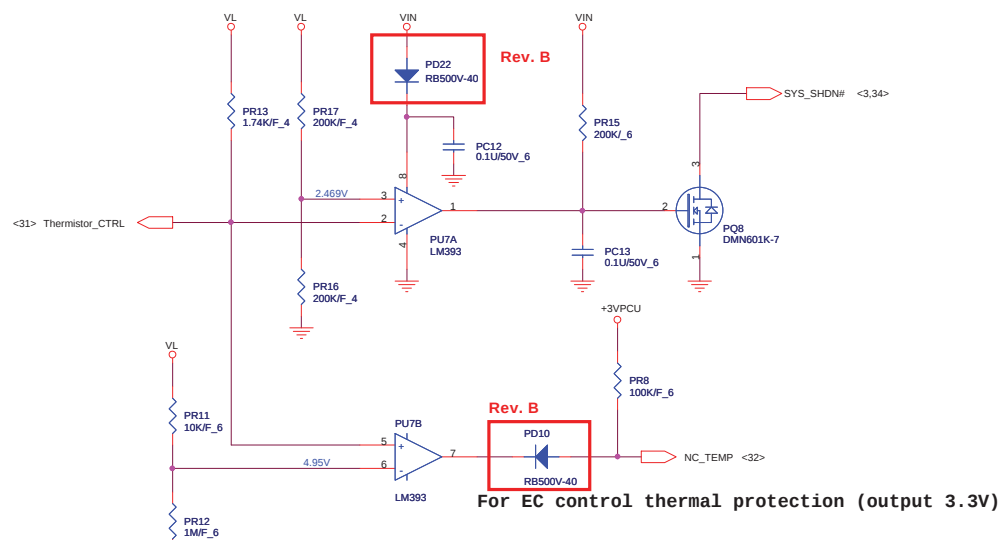




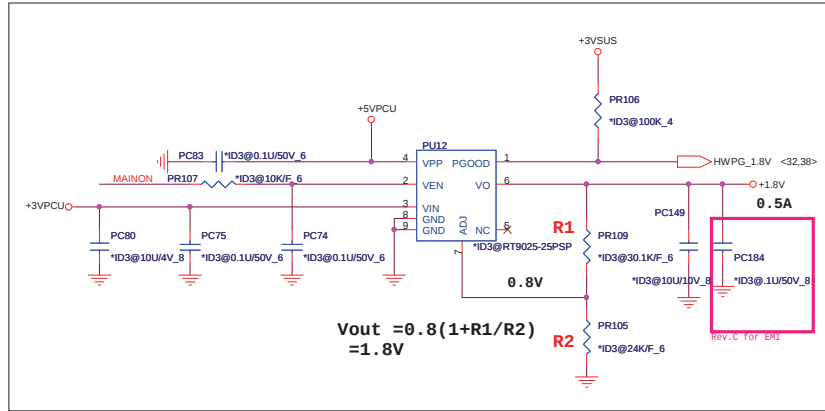




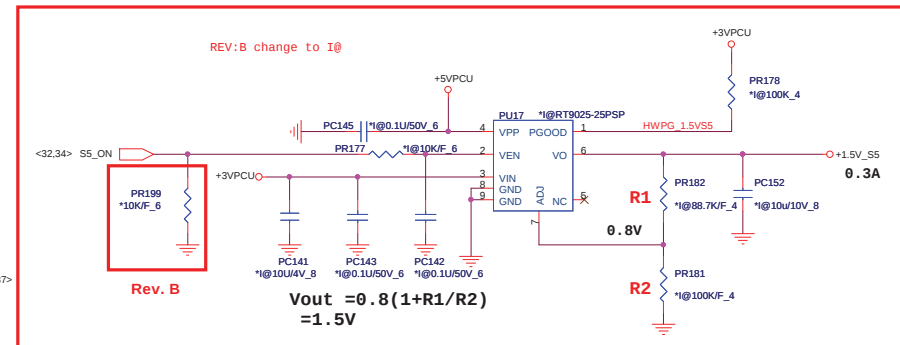
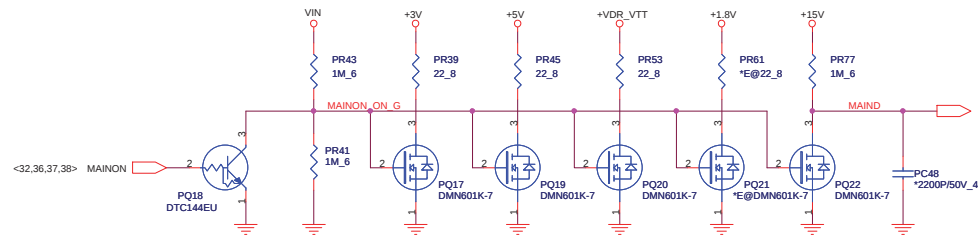
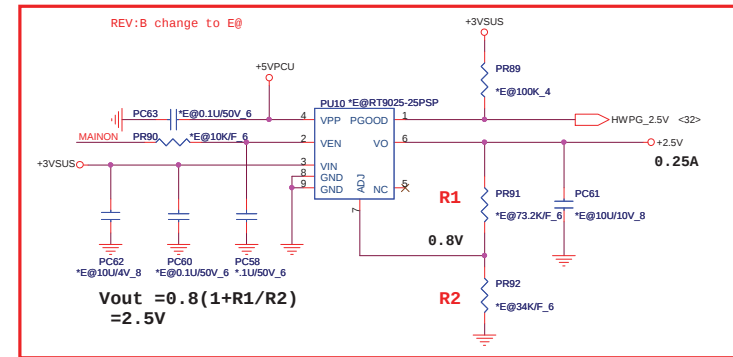
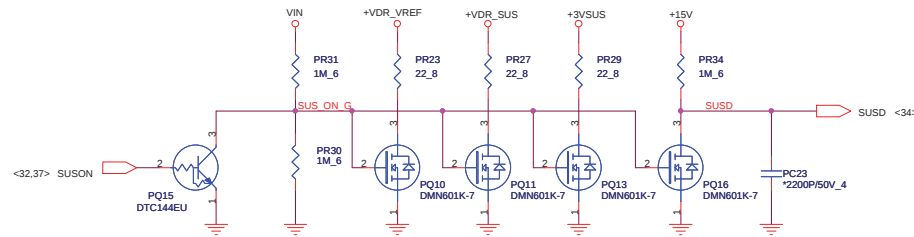
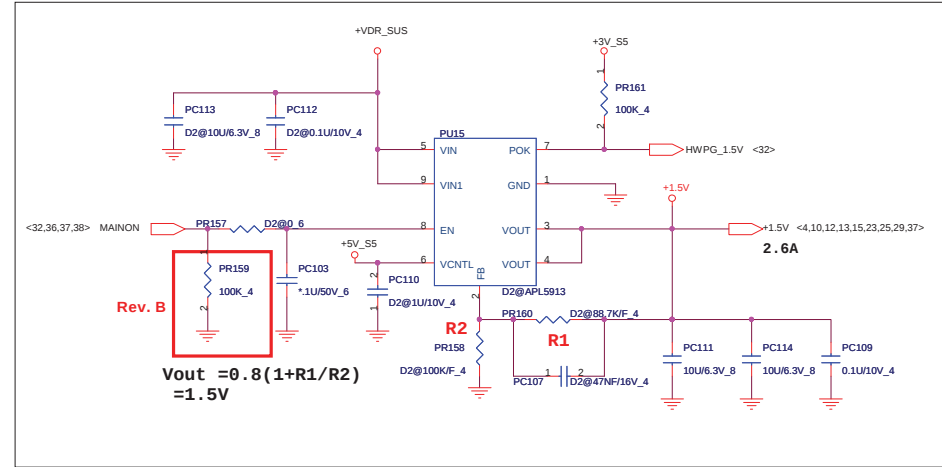
thermal protection --0928



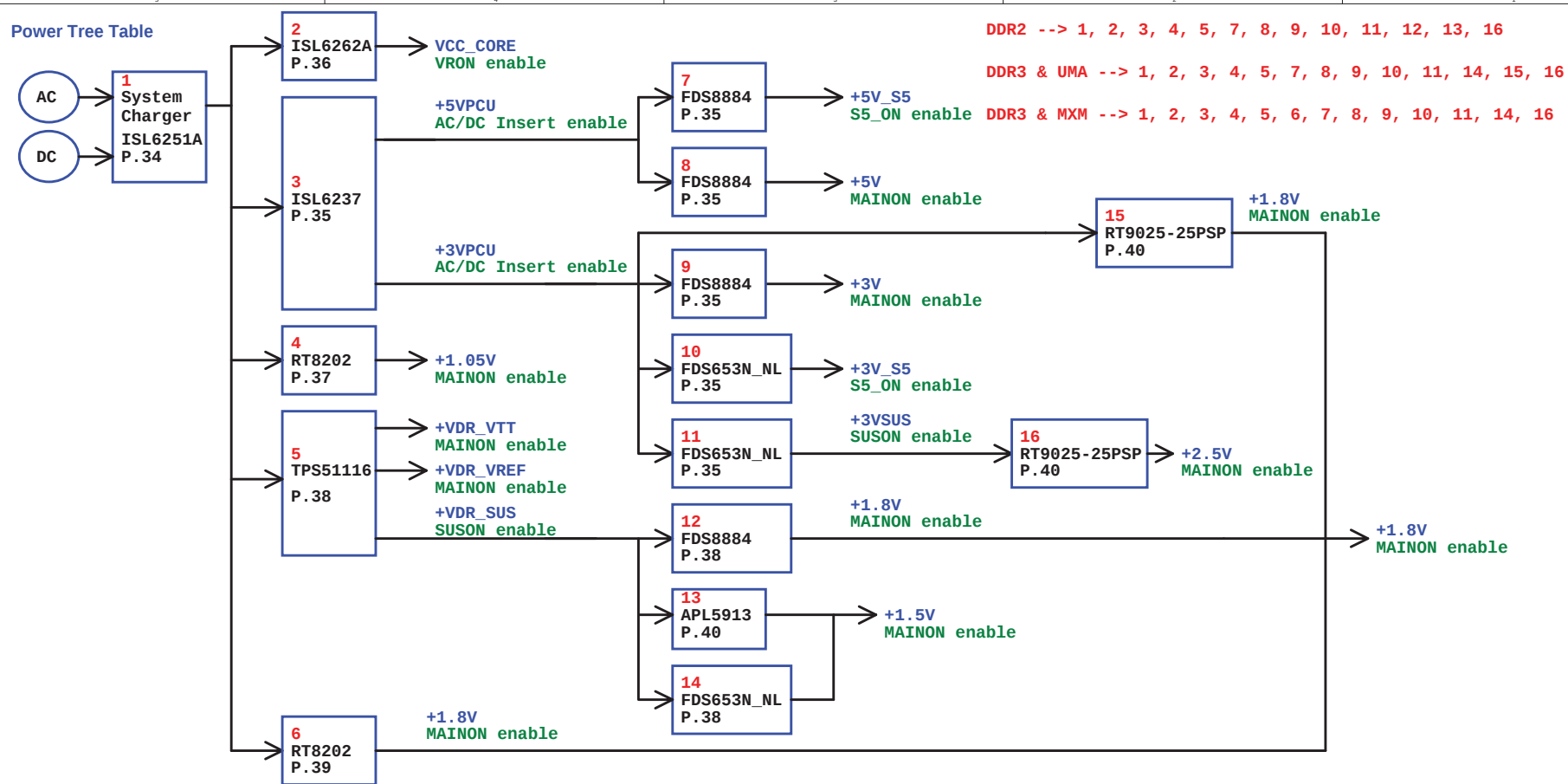
for DDR3 and UMA



DDR3 -- NC



REV:B change to E@



Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH8M, RJ45/USB /B, USB/eSATA, Satellite LED, CIR
+3VPCU	RTC, HALL SENSOR, KB, TP/FP/LED /B, Power /B, Kill SW, EC, ID, SPI Flash, CIR
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+VDR_SUS	GMCH, DDR
+VDR_VREF	GMCH, DDR
+VDR_VTT	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH8M
+5V_S5	ICH8M, G-SENSOR, Felica, USB/eSATA
+5V	CPU, ICH8M, VGA, Camera, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, TP/FP/LED /B, EC, Speaker, Headphone
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH8M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PATA ODD, PCMCIA, Cardreader (0Z129F) Mini Card, KB, TP/FP/LED /B, RJ45/USB /B, Bluetooth, MMB, New Card, PC BEEP, EC, Codec (CX20561), VR, Headphone, MDC
+3V_S5	ICH8M, Mini Card, RJ45/USB /B, New Card
+3VSUS	ICH8M, FP
+1.8V	Cardreader
+2.5V	MXM

Model		REV	CHANGE LIST	MODEL	ZY2	
					FROM	To
ZY2 MB	1A	FIRST RELEASED: E200610-3793 (PCB:)			X	1A
	1B	Page2 : Add R475 ,531 & R532 to avoid active error. (follow CK505 design guideline) Page2 : Swap SRC4 & SRC9, because NEW_CLKREQ# is only to control SRC1 or 4 Page3 : Add R540 to avoid active error. (CPU Thermal monitor) Page6 : Follow DDR3 spec R251 change to 10K. Page18 : POP C282 &C284 and RSVD. C604 for DDR3 PCB boot issue. Page18 : HDA_RST# PIN change from 151 to 134 for customer request. Page18 : Swap Net:TX0 &TX2 (RN15 & RN17) For HDMI no function issue. Page20 : Add R527 ,R528 ,R529 ,R530 ,R539 ,R148 ,R153 ,R152 ,R104 & R105 for vendor request.(HDMI level shifter) Page20 : Change HDMI SW IC (U9) & schematic Page23 : Add R536 ,R542 ,R538 ,RP57 ,R537 customer request.(MINI PCI-E card function) Page25 : Add Intel Low Power ECR Solution(Audio) Page28 : Add part for D3 Enhanced (D3E).(cerd reader) Page29 : Add Keyboard LED function for customer request. Page30 : Location :C25 & C23 change to 100U & POP it for customer request.(USB) Page31 : Add D43 for customer request(FOR Dock :CRT _SENSE#) Page31 : CN12 & CN14 change footprint.(K/B & T/P CONN.) Page31 : Add C609 ,C606 & C608.(FOR DOCK : +5V & +5V_S5)		X	1A	
				1A	2A	
					1A	2A
					1A	2A
					1A	2A
					1A	2A
					1A	2A
					1A	2A
					1A	2A
					1A	2A
					1A	2A
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PROJECT : ZY2

Quanta Computer Inc.

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