

Compal Confidential

HBL51 Schematics Document

Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M

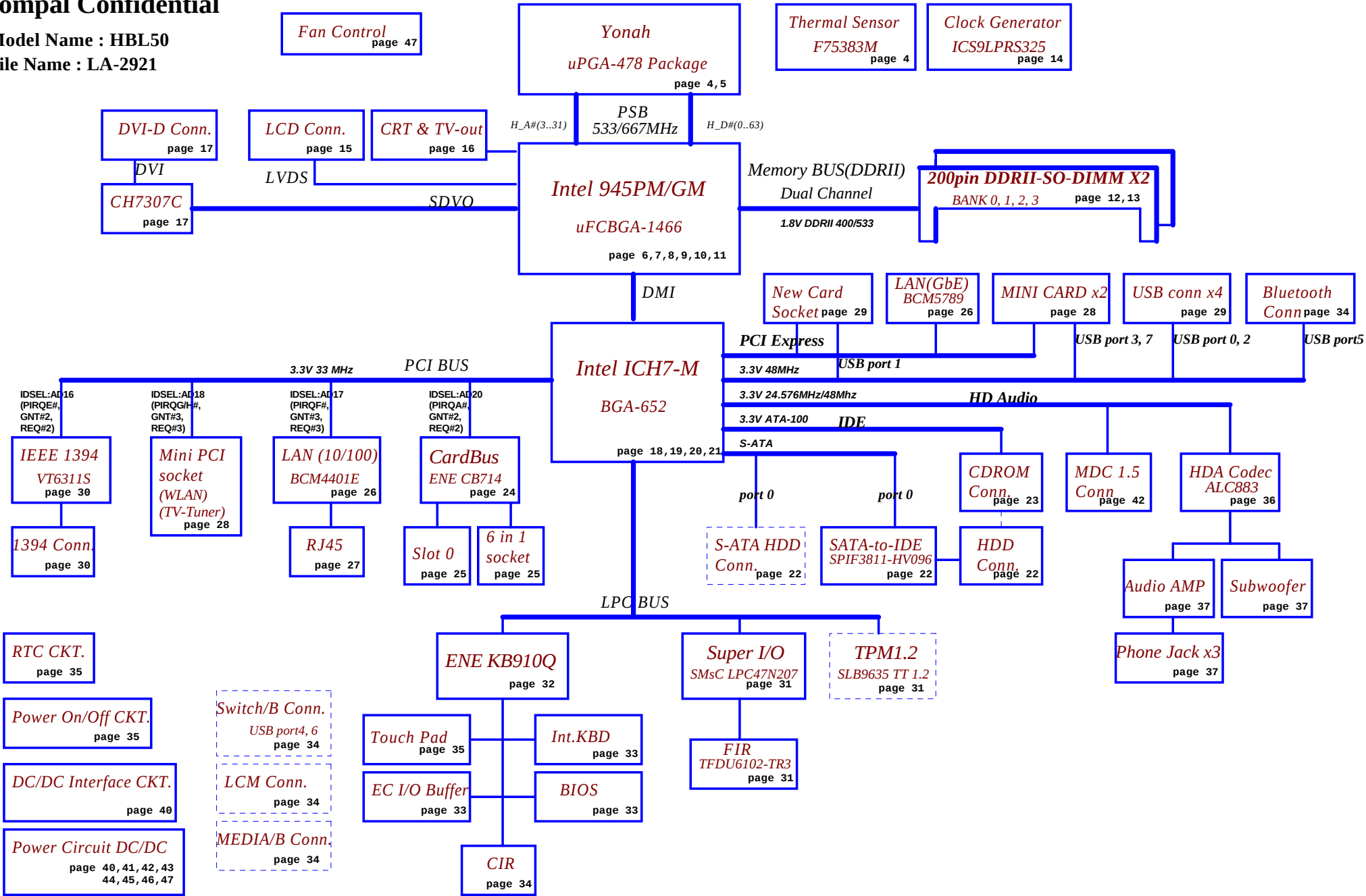
2005-11-03

REV: 0.2

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Model Name : HBL50
File Name : LA-2921



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

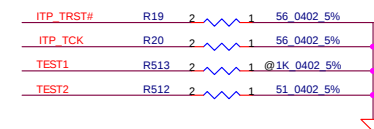
Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI CARD1	MINI1@
MINI CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
LCM	LCM@
TVOUT	TVOUT@
1394	6311S@
CARDREADER	4IN1@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@

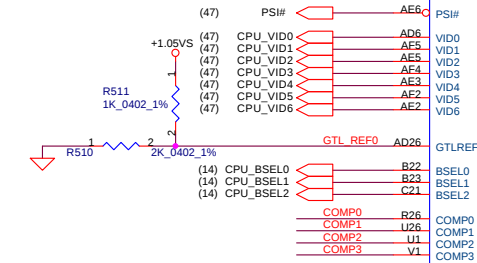
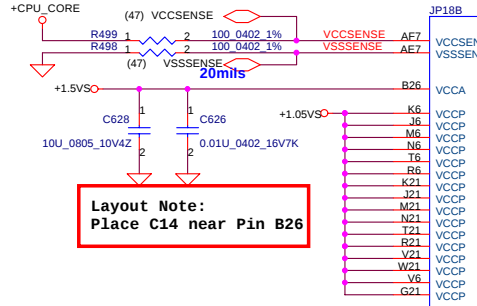
SKU ID Table

SKU ID	SKU
0	
1	GM
2	
3	
4	
5	
6	
7	

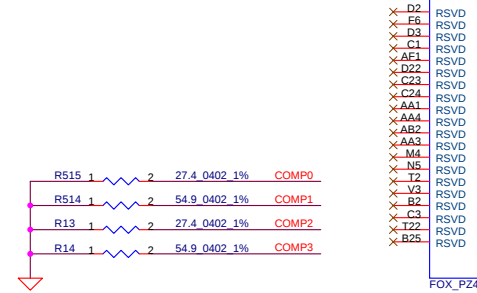


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Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.40hms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.



BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133
0	1	1	166

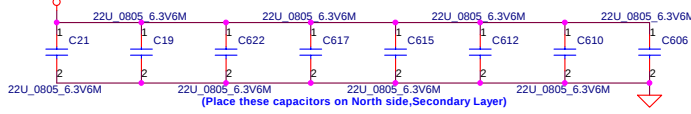
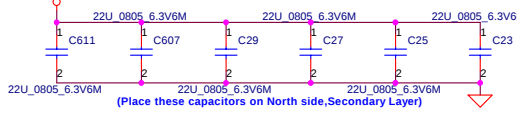
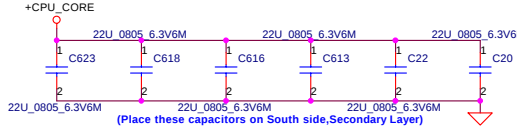
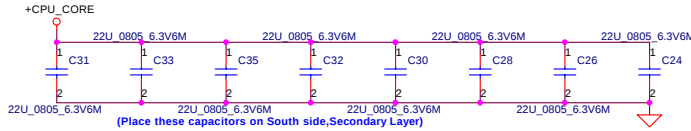
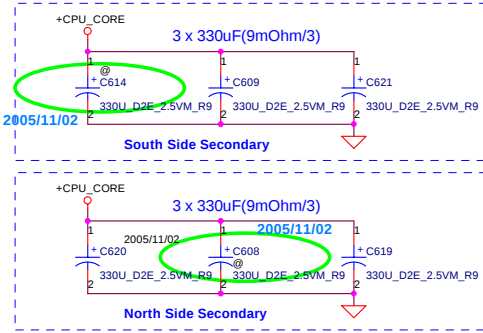


TRACE CLOSELY CPU < 0.5'
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.40hms)
COMP1, COMP3 layout : Space 25mils (550hms)

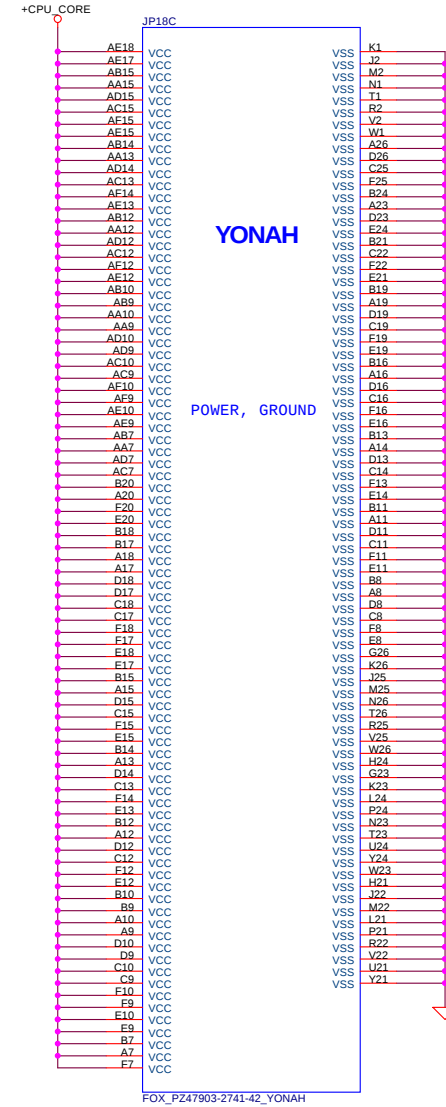
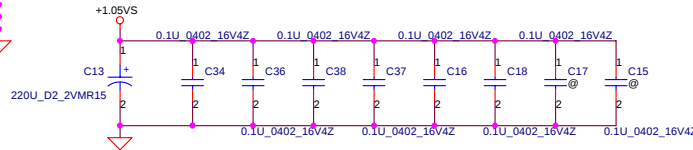
YONAH

POWER, GROUND, RESERVED SIGNALS AND NC

FOX_PZ47903-2741-42_YONAH



+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32



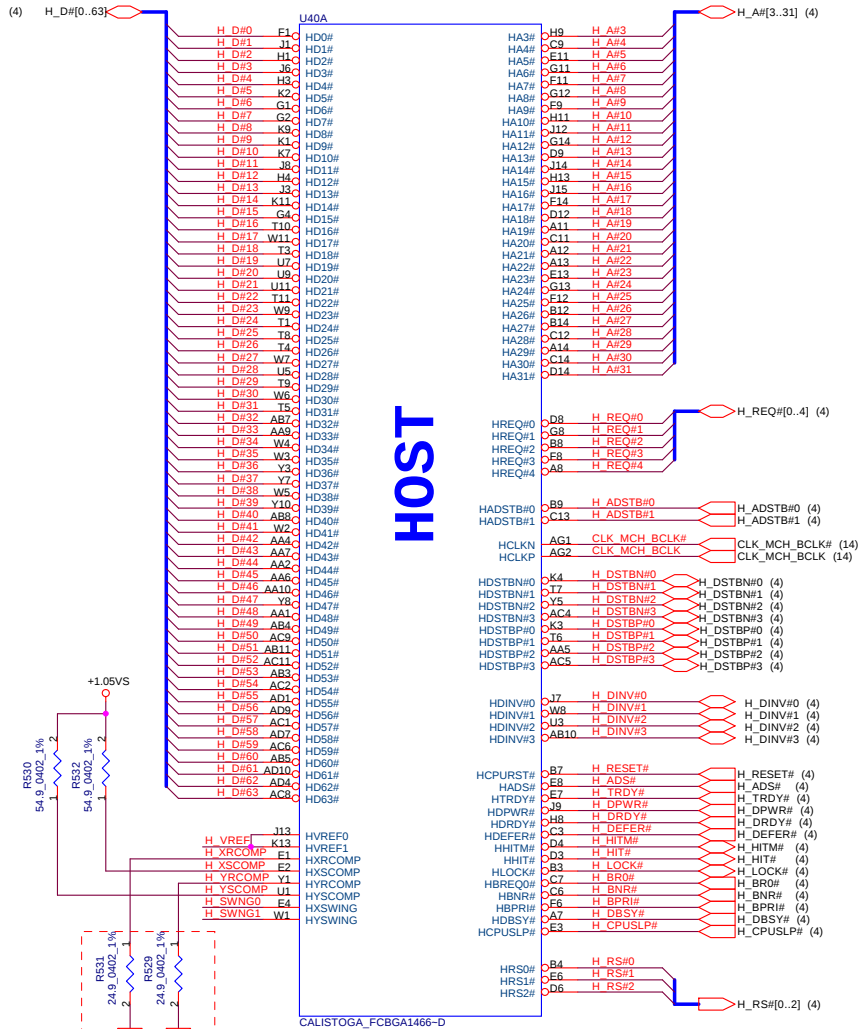
YONAH

POWER, GROUND

FOX_PZ47903-2741-42_YONAH

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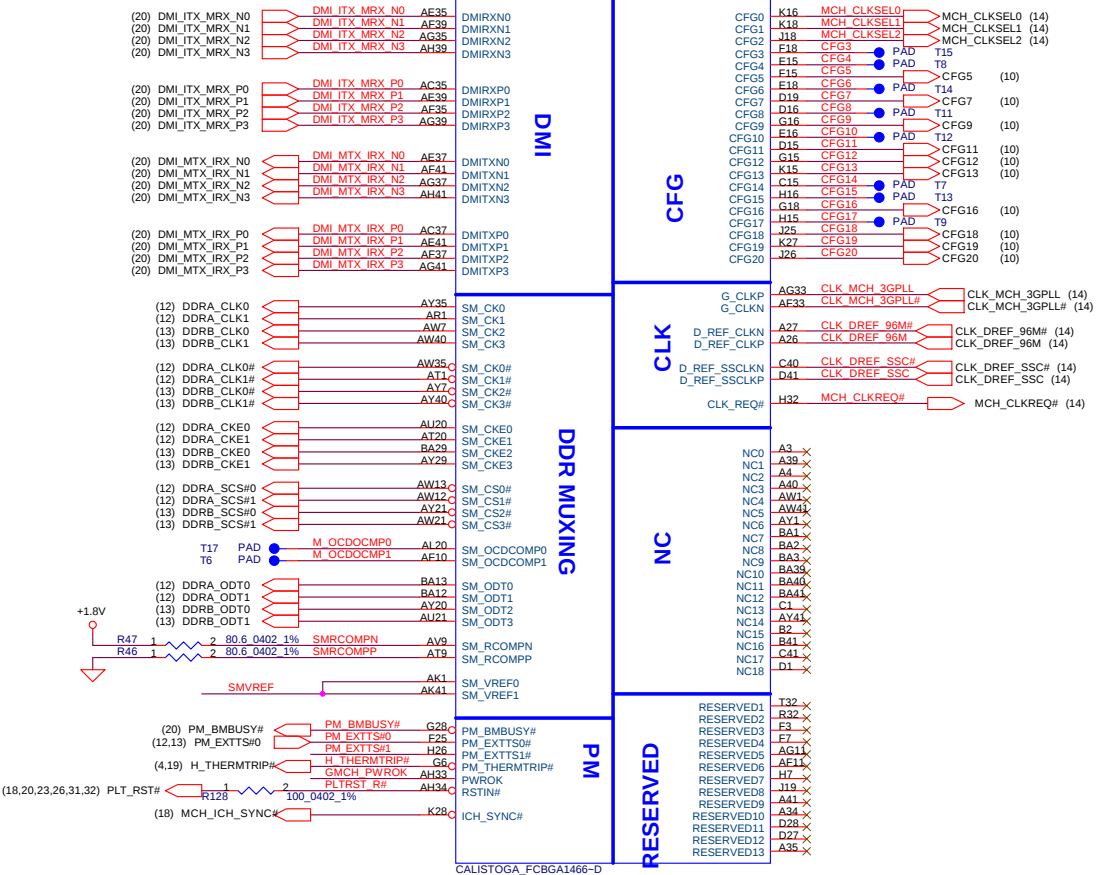
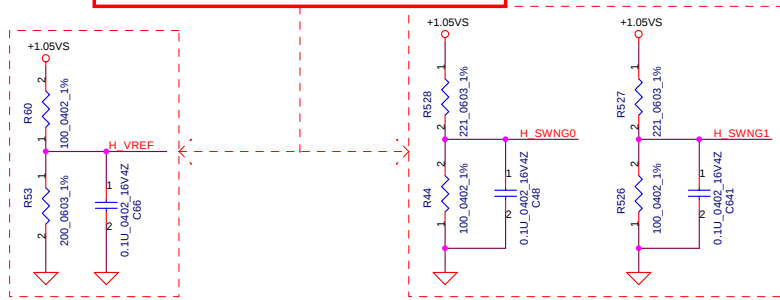
945GM(A-1)(QJ15)[ES2]: SA000005970
945GM(A-2)(QK44)[ES3]: SA000005980
945PM(A-2)(QK46)[ES3]: SA00000UV10



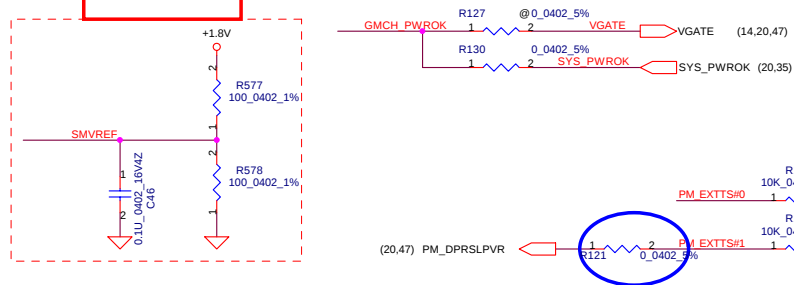
HOST

CALISTOGA_FCBGA1466-D

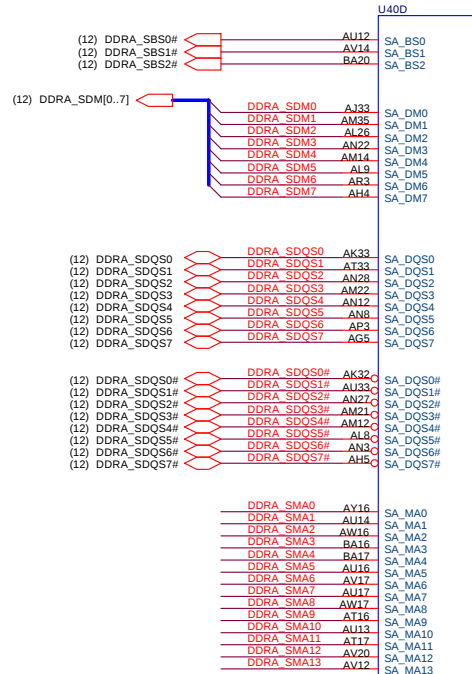
Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 10/20.



Layout Note:
SMVREF trace width and spacing is 20/20.



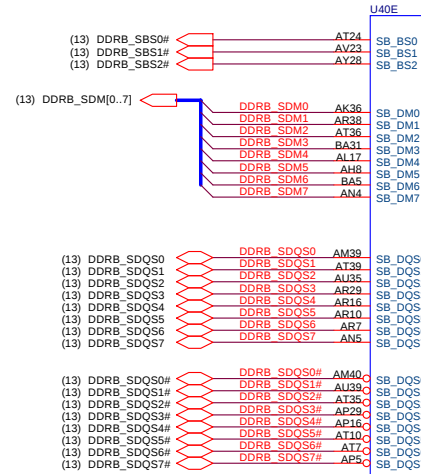
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DDR SYS MEMORY A

CALISTOGA_FCBGA1466-D

check layout

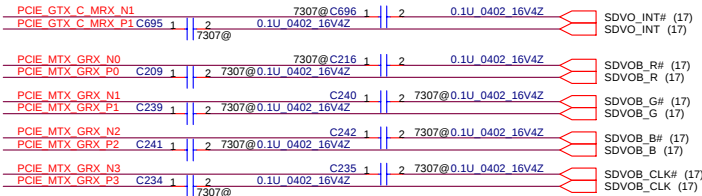
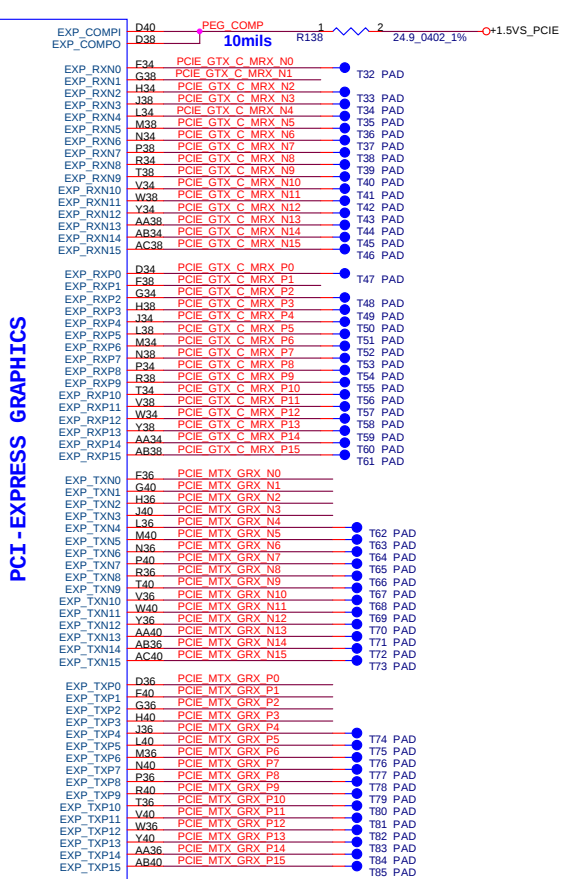
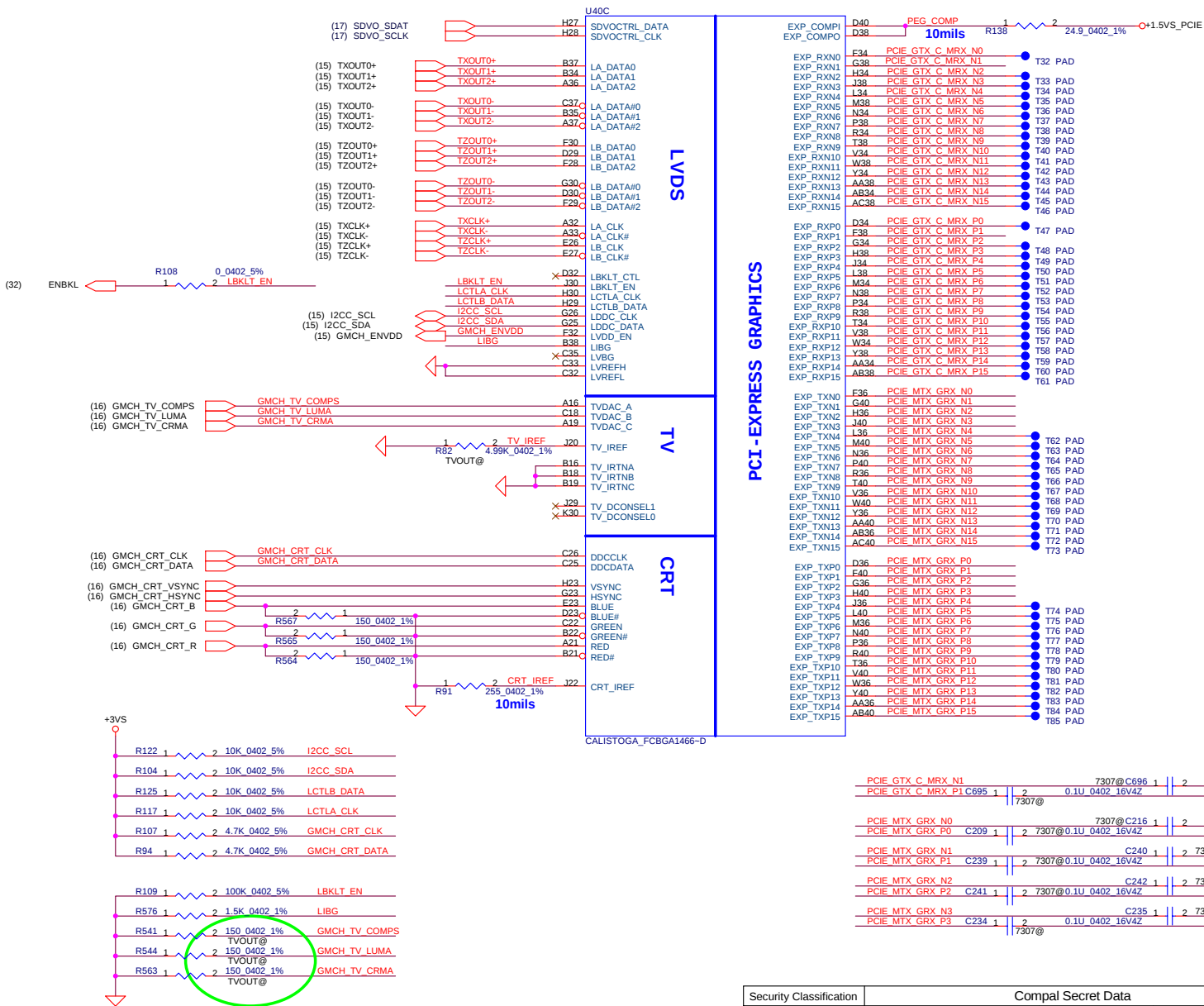


DDR SYS MEMORY B

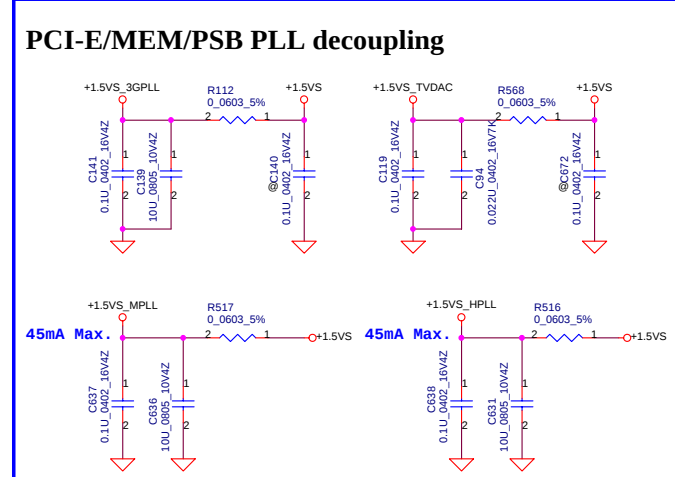
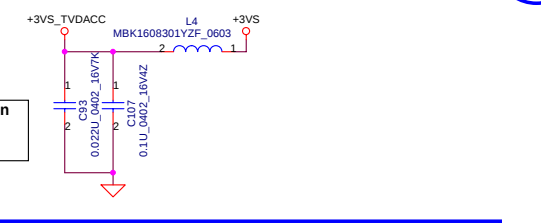
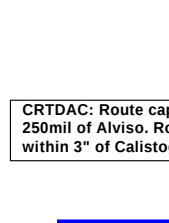
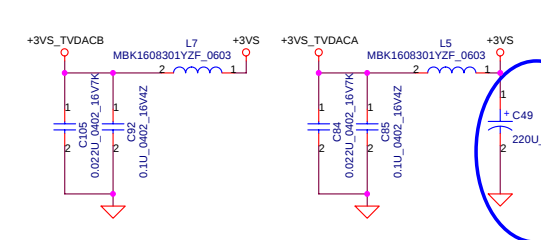
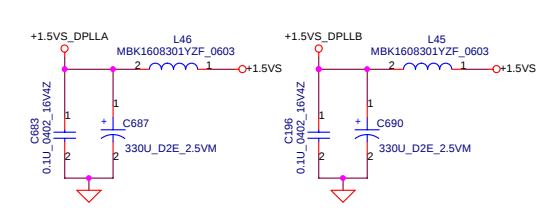
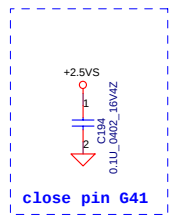
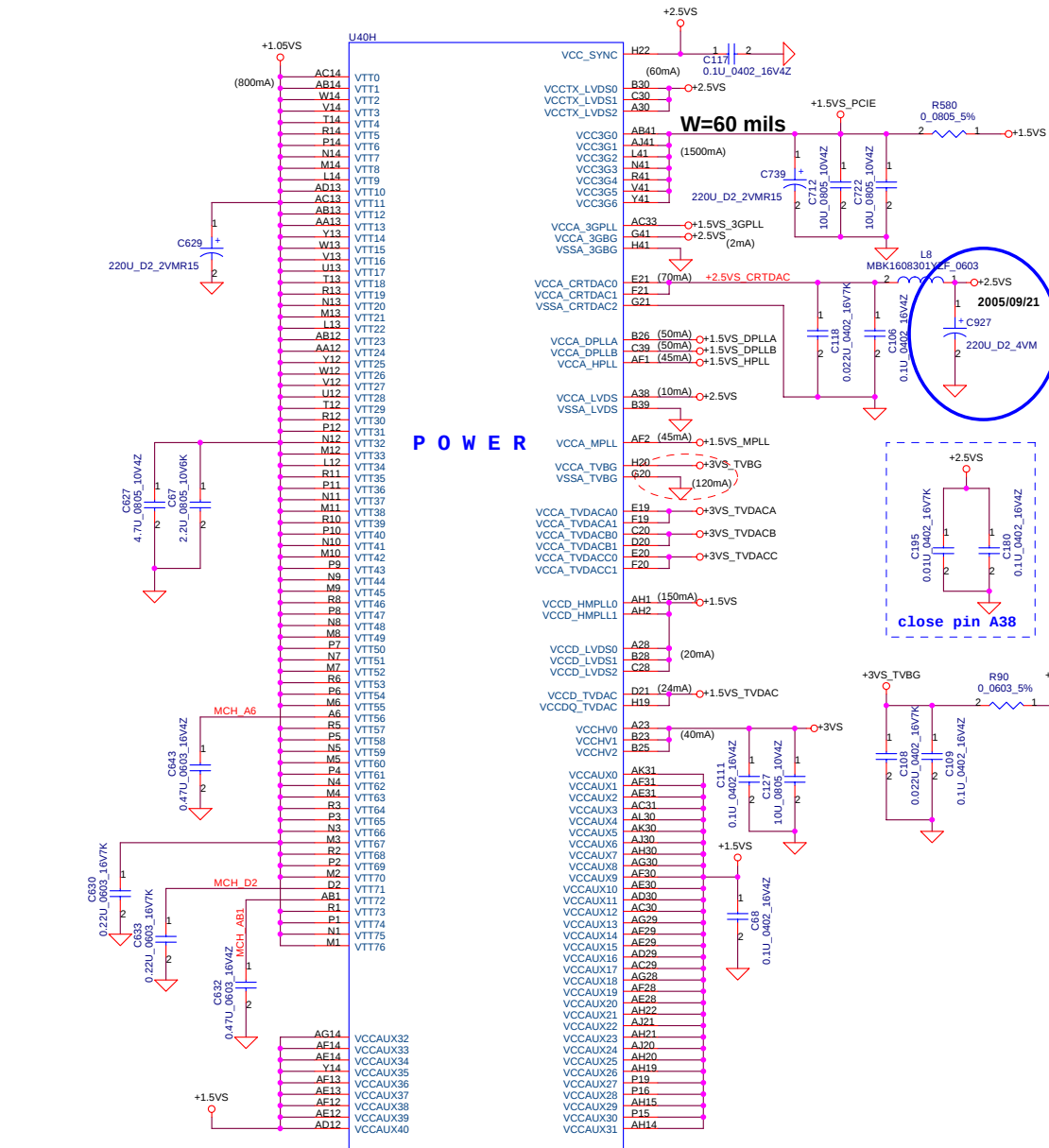
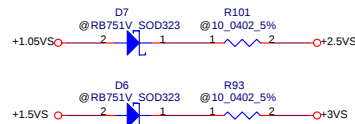
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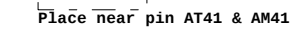


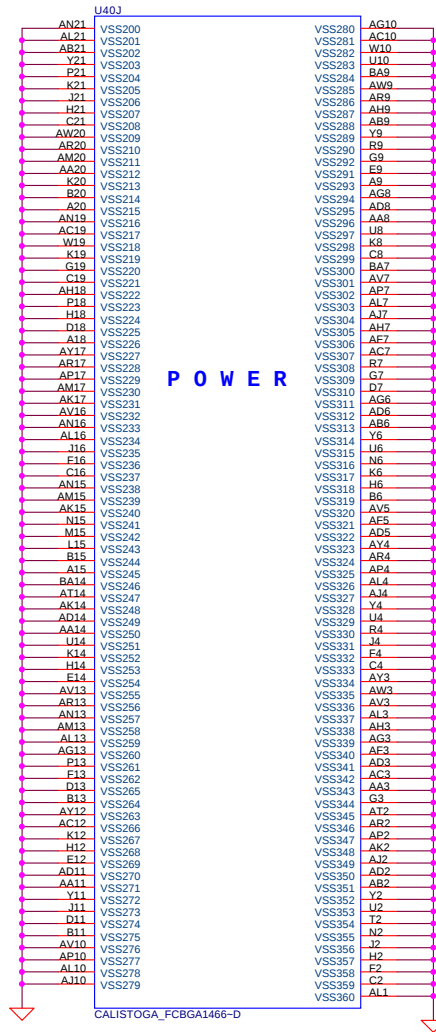
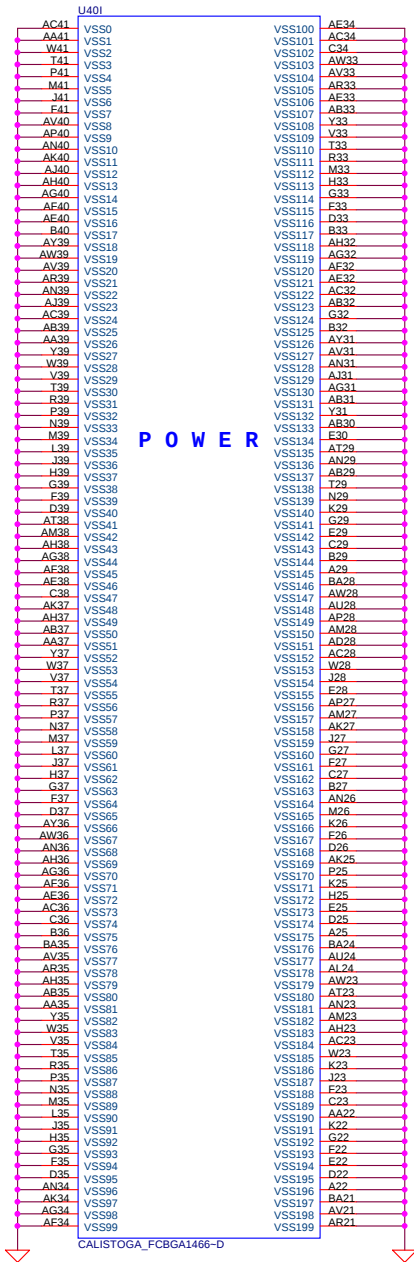
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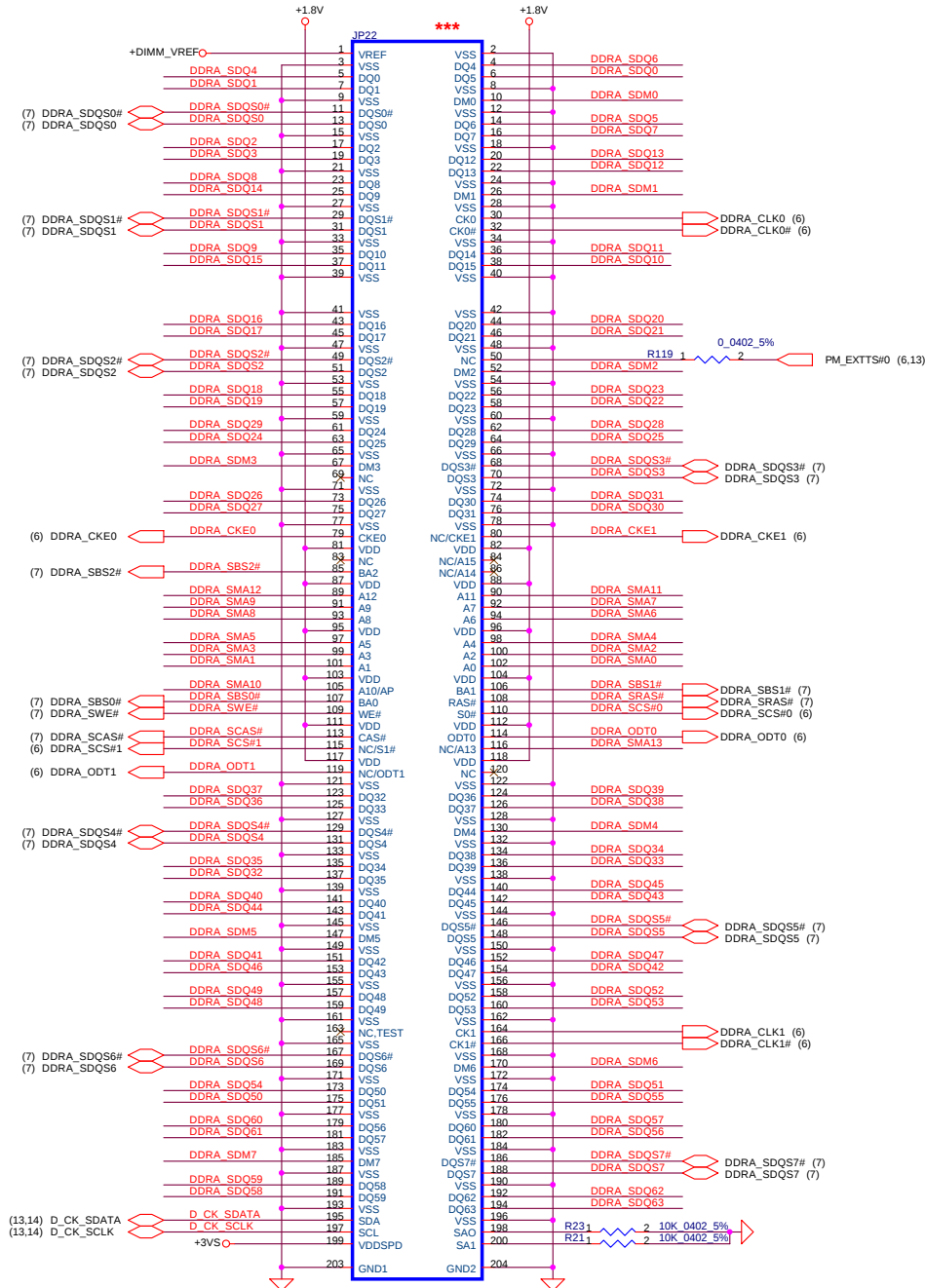
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CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

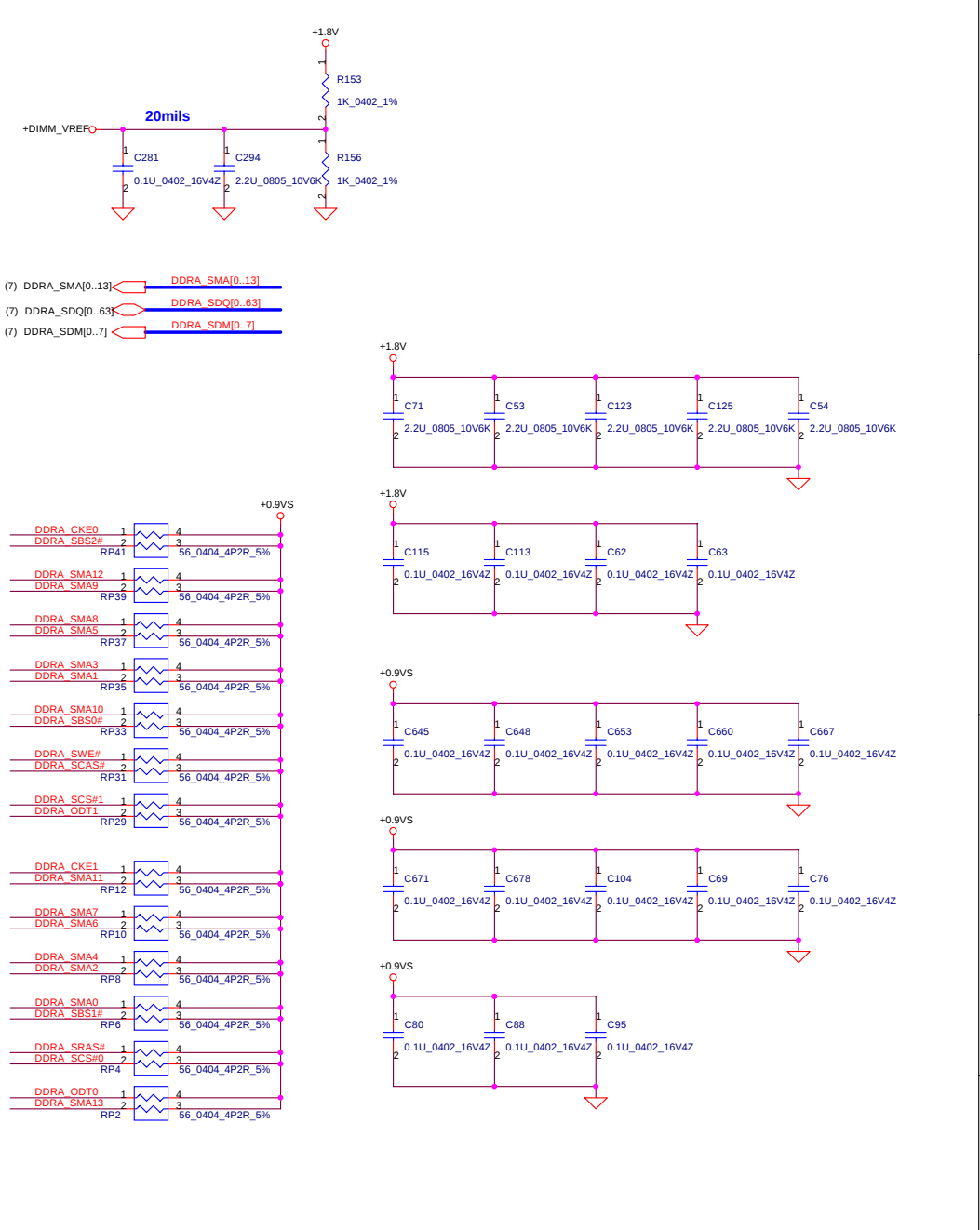
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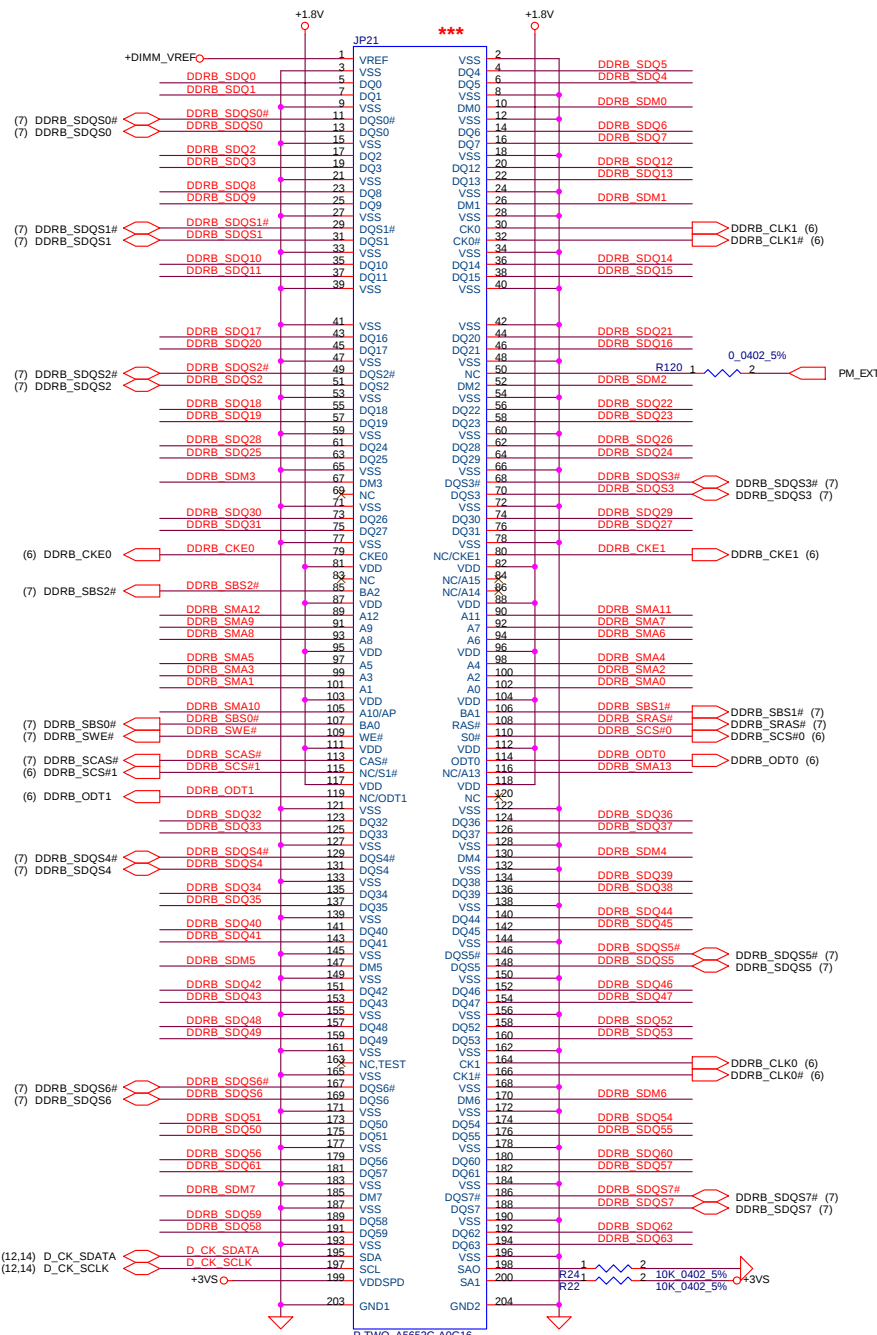


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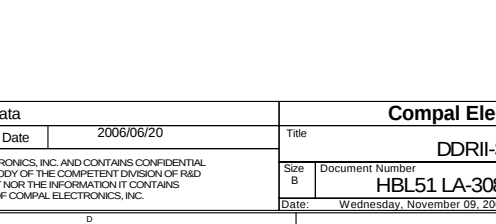
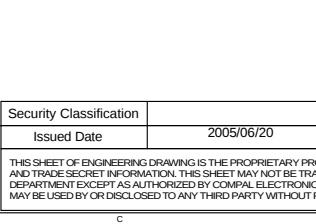
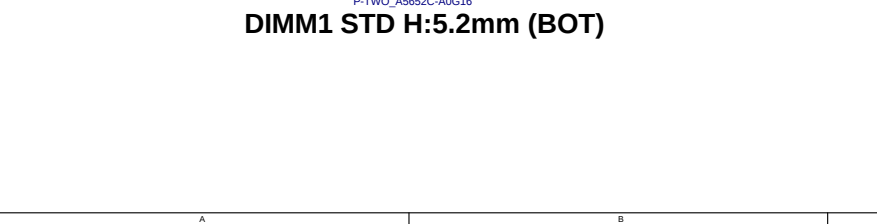
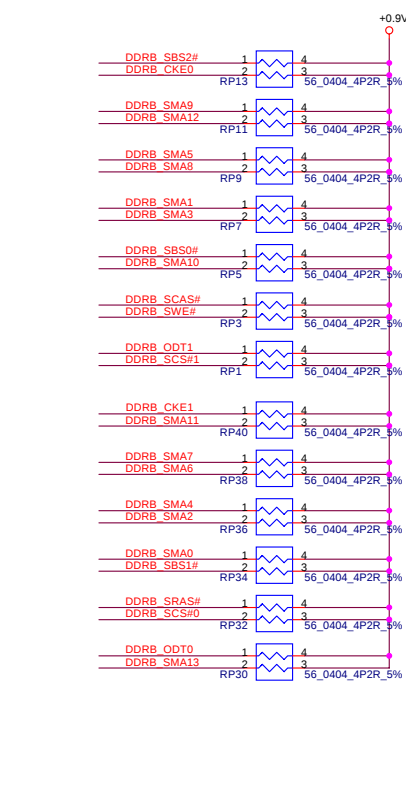
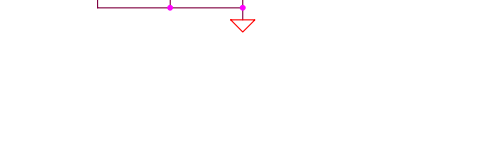
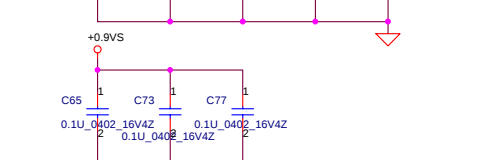
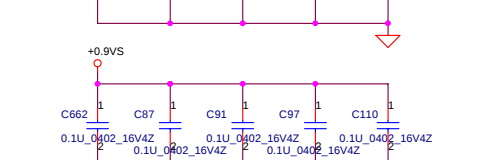
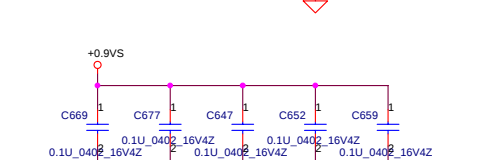
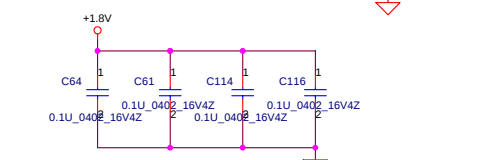
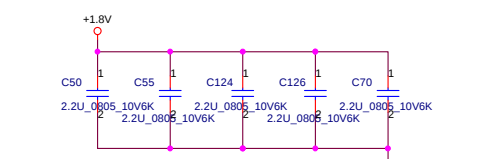
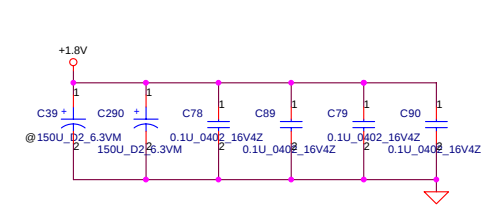
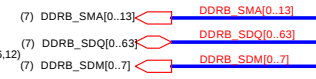
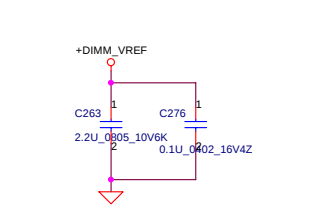


DIMM0 STD H:9.2mm (BOT)





DIMM1 STD H:5.2mm (BOT)



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						C	D	E					

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz 1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

**SEL_24M/PCICLK2=0=TESTMODE
**SEL_PCI6/PCICLK1=0=CLKREQ5#

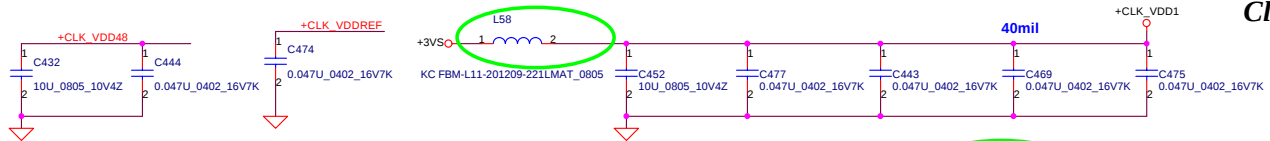
+3VS
R712
CLK REF
10K_0402_5%
R619
CLK PCIO
10K_0402_5%
ITP_EN/PCICLK_F0=0=SRC pair

R713
CLK PC14
10K_0402_5%
08/29 add

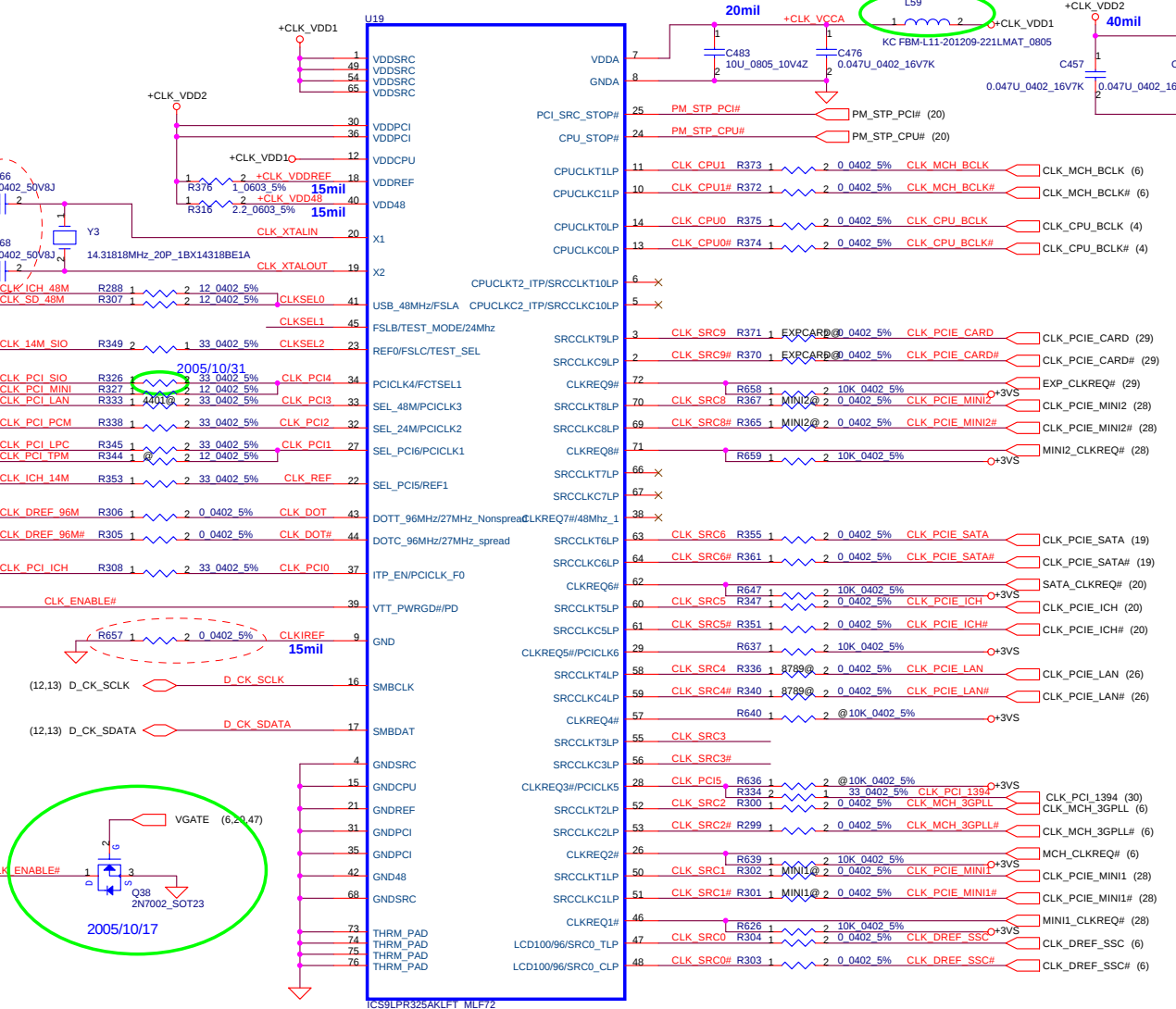
+3VS
R620
CLK ENABLE#
10K_0402_5%
2005/10/17

+3VS
R387
4.7K_0402_5%
Q15
2N7002_SOT23
D CK SDATA
+3VS
R386
4.7K_0402_5%
Q14
2N7002_SOT23
D CK SCLK
+3VS

+1.05VS
R623
@56_0402_5%
R621
8.2K_0402_5%
R622
1K_0402_5%
MCH_CLKSEL0 (6)
R616
@1K_0402_5%
R615
0_0402_5%
CPU_BSEL0 (5)
CLKSEL0
+1.05VS
R624
@1K_0402_5%
R625
1K_0402_5%
MCH_CLKSEL1 (6)
R617
@0_0402_5%
R618
0_0402_5%
CPU_BSEL1 (5)
CLKSEL1



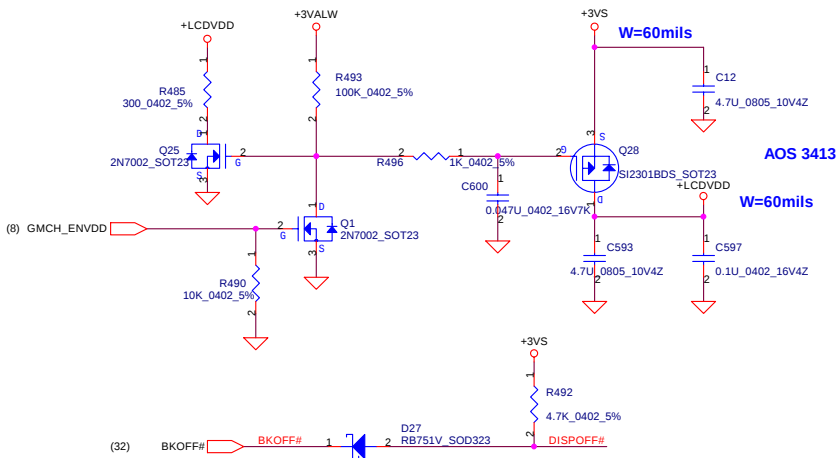
Clock Generator



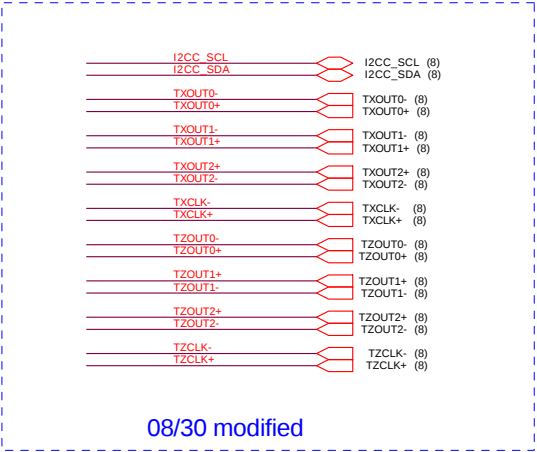
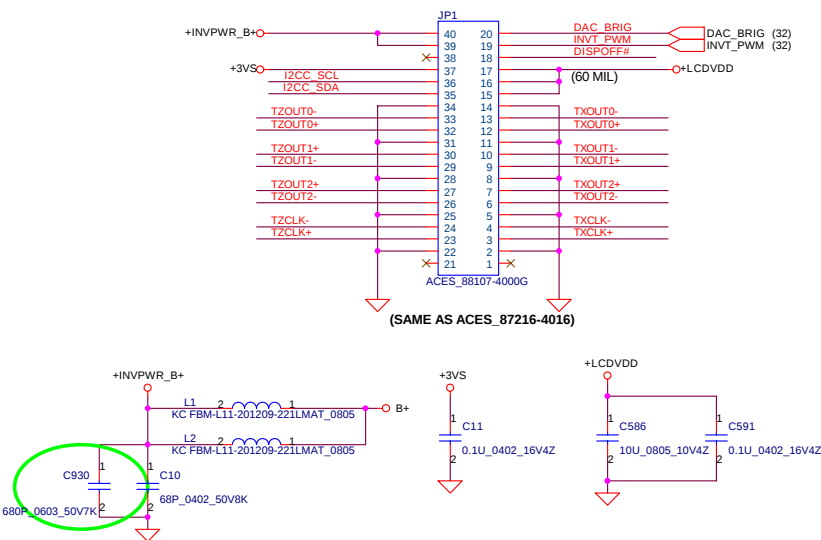
CLK MCH BCLK
CLK MCH BCLK#
CLK CPU BCLK
CLK CPU BCLK#
CLK PCIE CARD
CLK PCIE CARD#
CLK PCIE MINI2
CLK PCIE MINI2#
CLK PCIE SATA
CLK PCIE SATA#
CLK PCIE ICH
CLK PCIE ICH#
CLK PCIE MINI1
CLK PCIE MINI1#
CLK PCIE SATA
CLK PCIE SATA#
CLK DREF SSC
CLK DREF SSC#
CLK PCIE CARD
CLK PCIE CARD#
CLK MCH 3GPLL
CLK MCH 3GPLL#
CLK PCIE LAN
CLK PCIE LAN#
CLK DREF SSC
CLK DREF SSC#

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Size B	Document Number	HBL51 LA-3081P		Rev 0.2	
Date:		Thursday, November 10, 2005	Sheet 14 of 47		

LCD POWER CIRCUIT

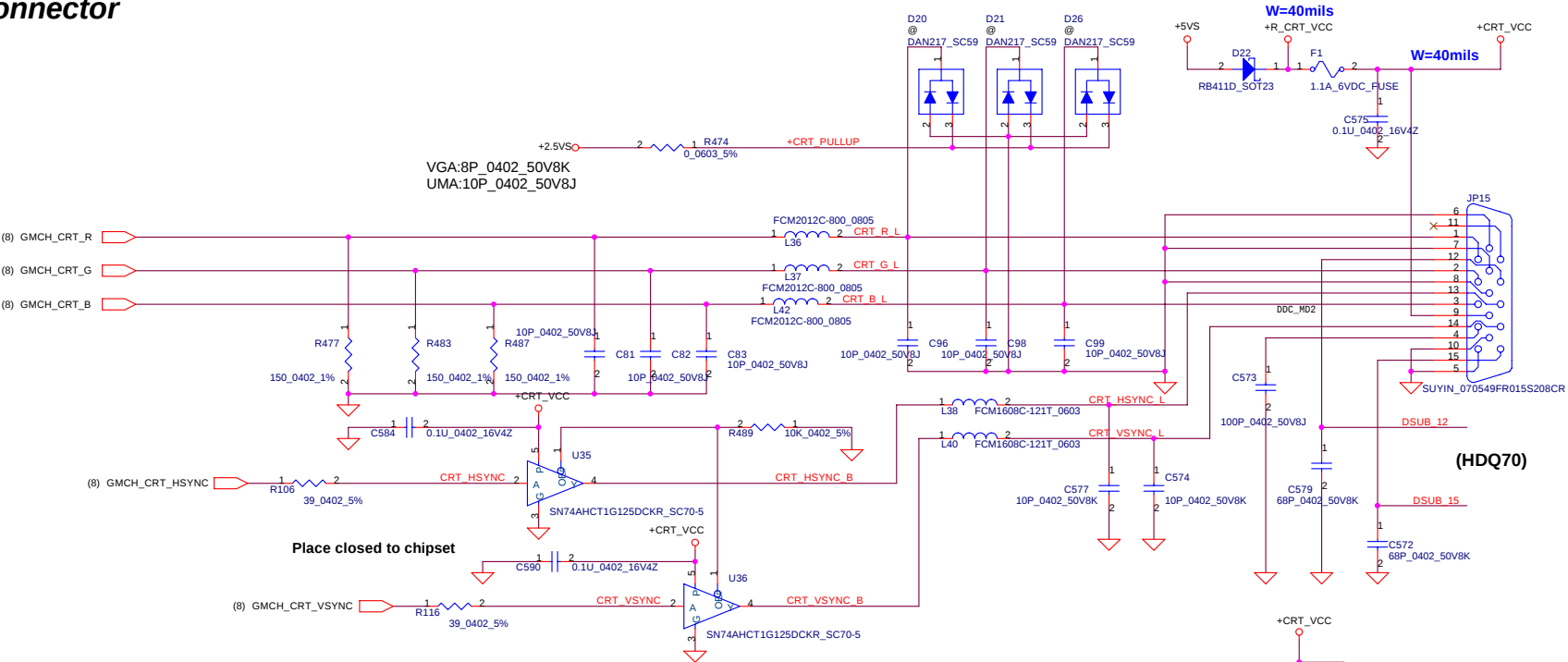


LCD/PANEL BD. Conn.

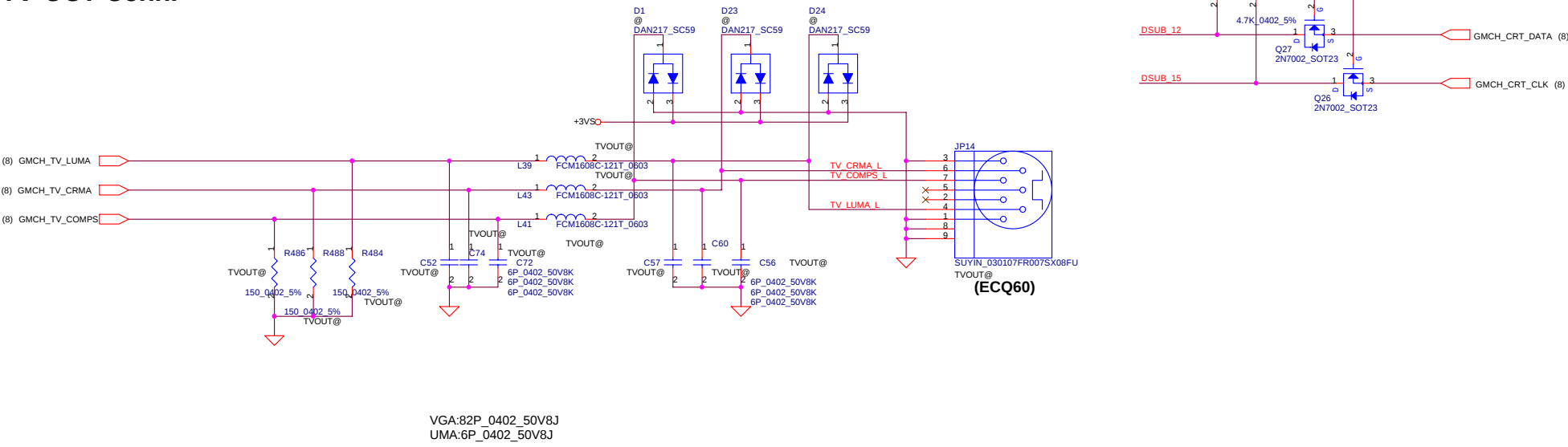


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CRT Connector

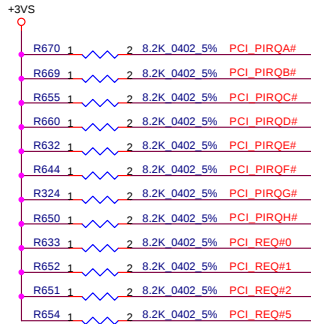
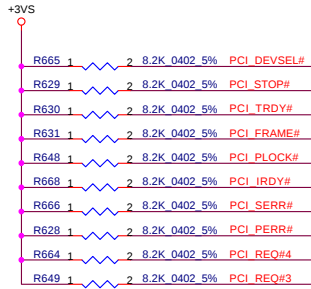


TV-OUT Conn.

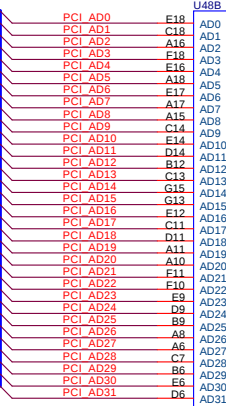


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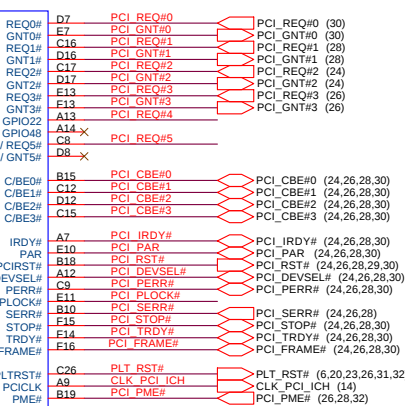
ICH7M(B-0) (QK17) [ES3] : SA00000JK30



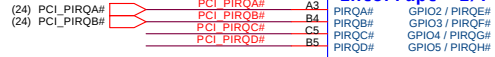
(24,26,28,30) PCI_AD[0..31]



PCI



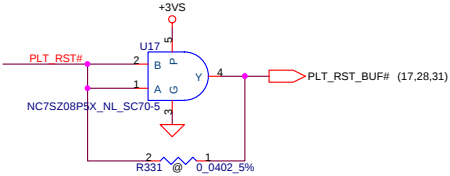
Interrupt I/F



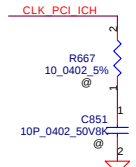
MISC



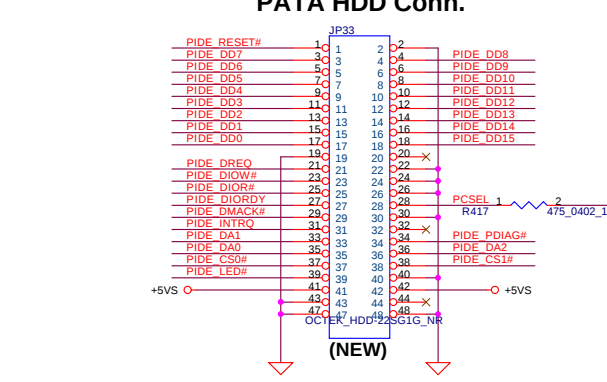
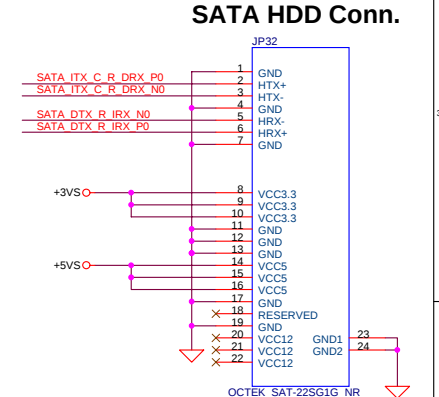
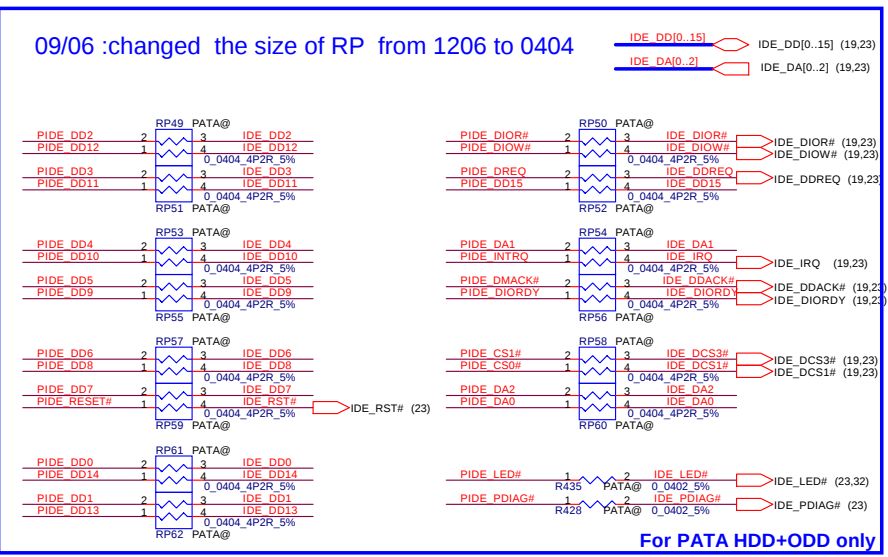
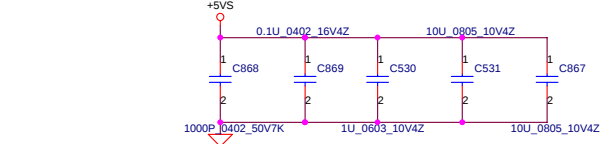
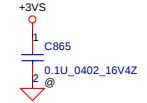
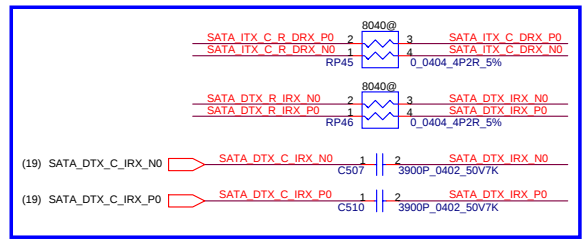
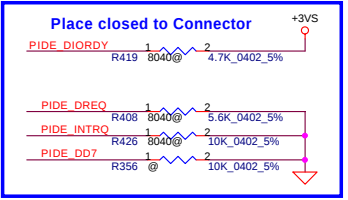
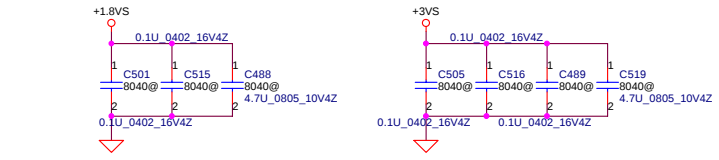
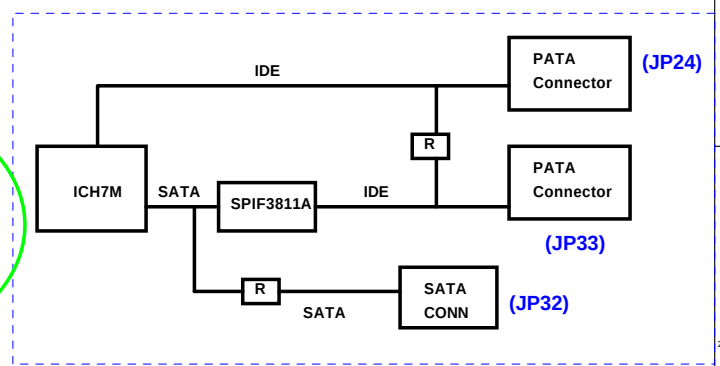
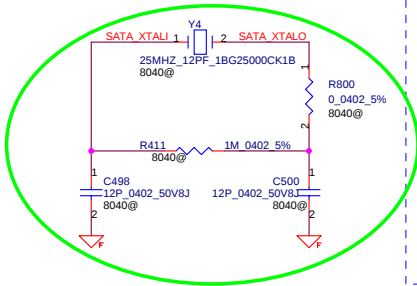
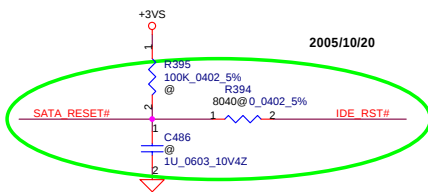
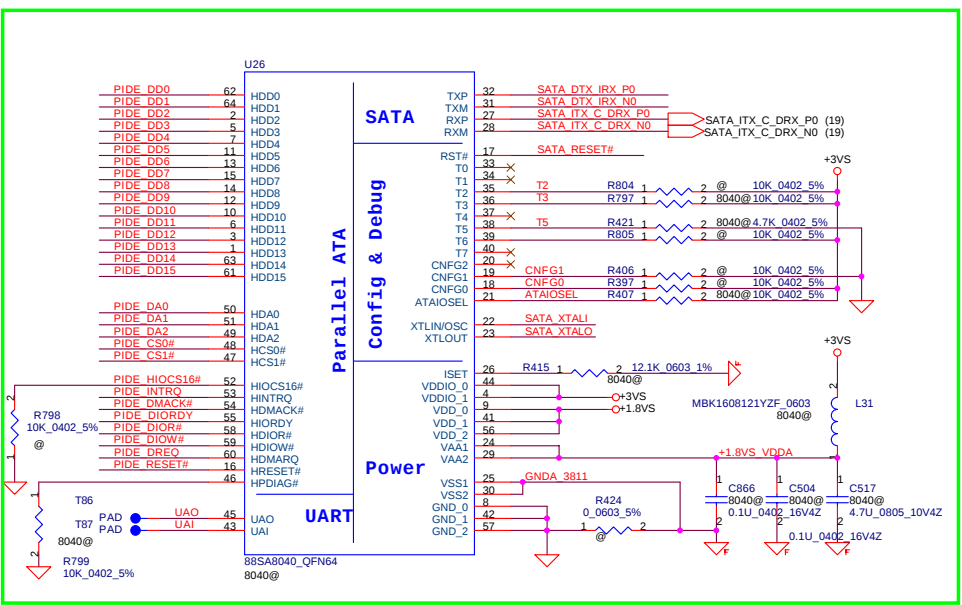
ICH7_BGA652-D



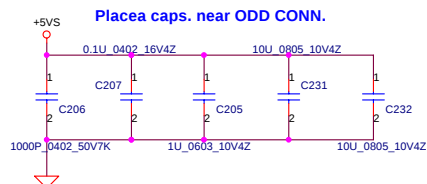
Place closely pin A9



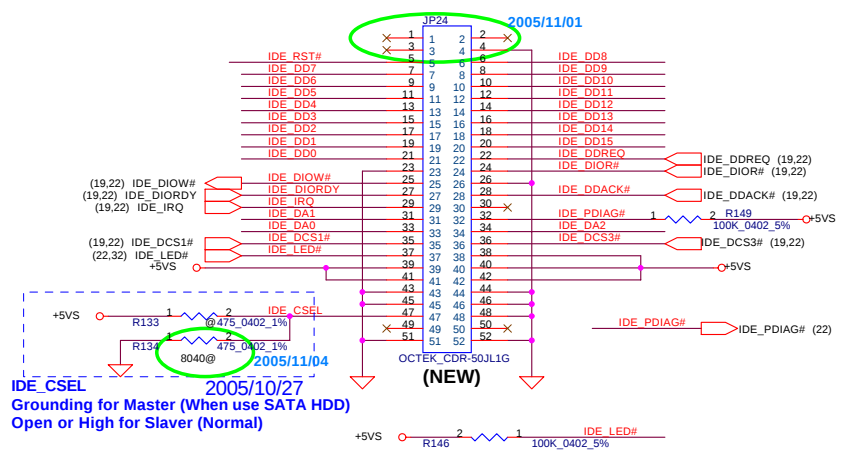
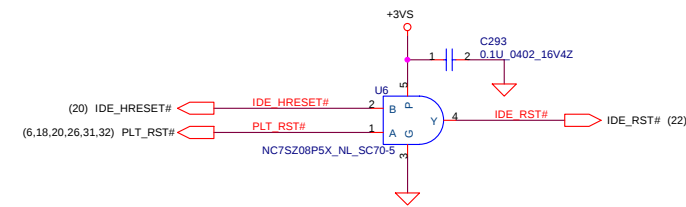
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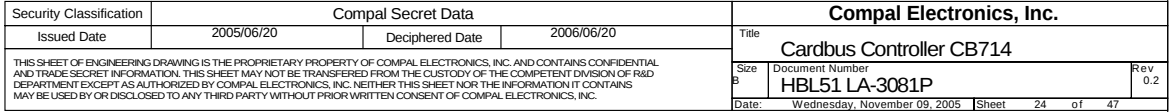
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					Size B	Document Number	Rev 0.2
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					Date:	Wednesday, November 09, 2005	Sheet 22 of 47



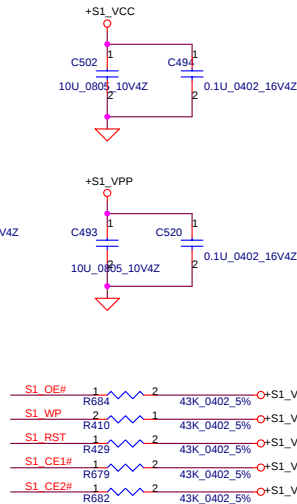
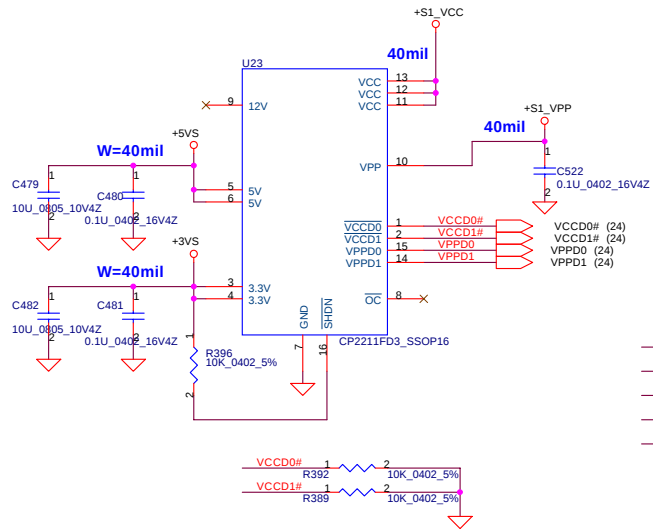
(19,22) IDE_DD[0..15] IDE_DD[0..15]
 (19,22) IDE_DA[0..2] IDE_DA[0..2]



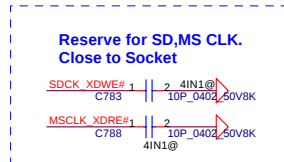
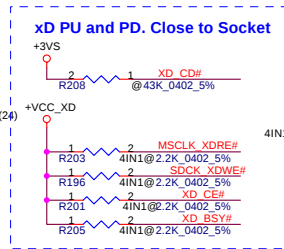
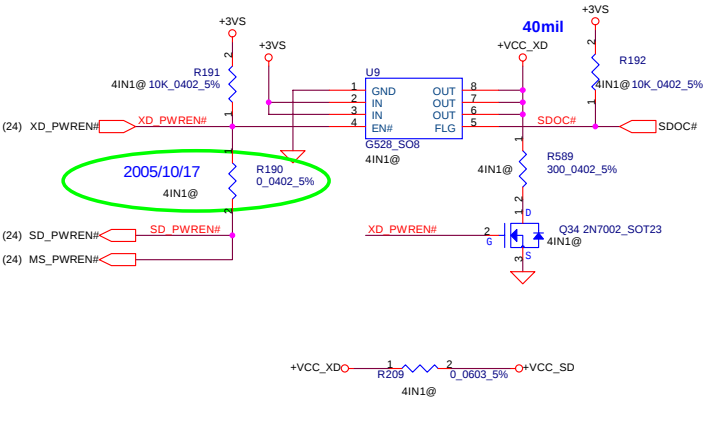
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				Size B	Document Number
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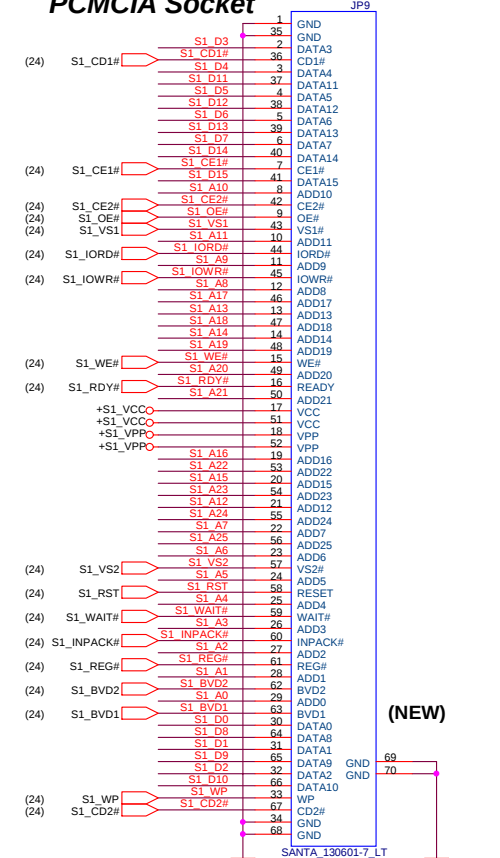
PCMCIA Power Control



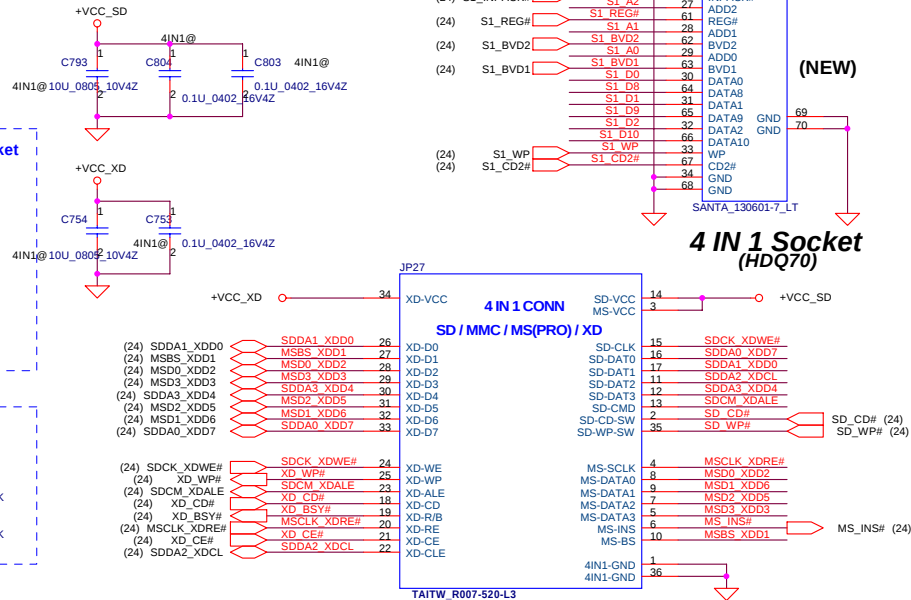
SD/MS Power Control



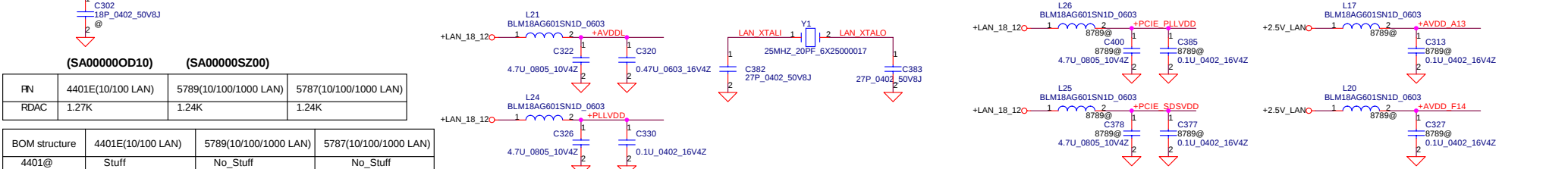
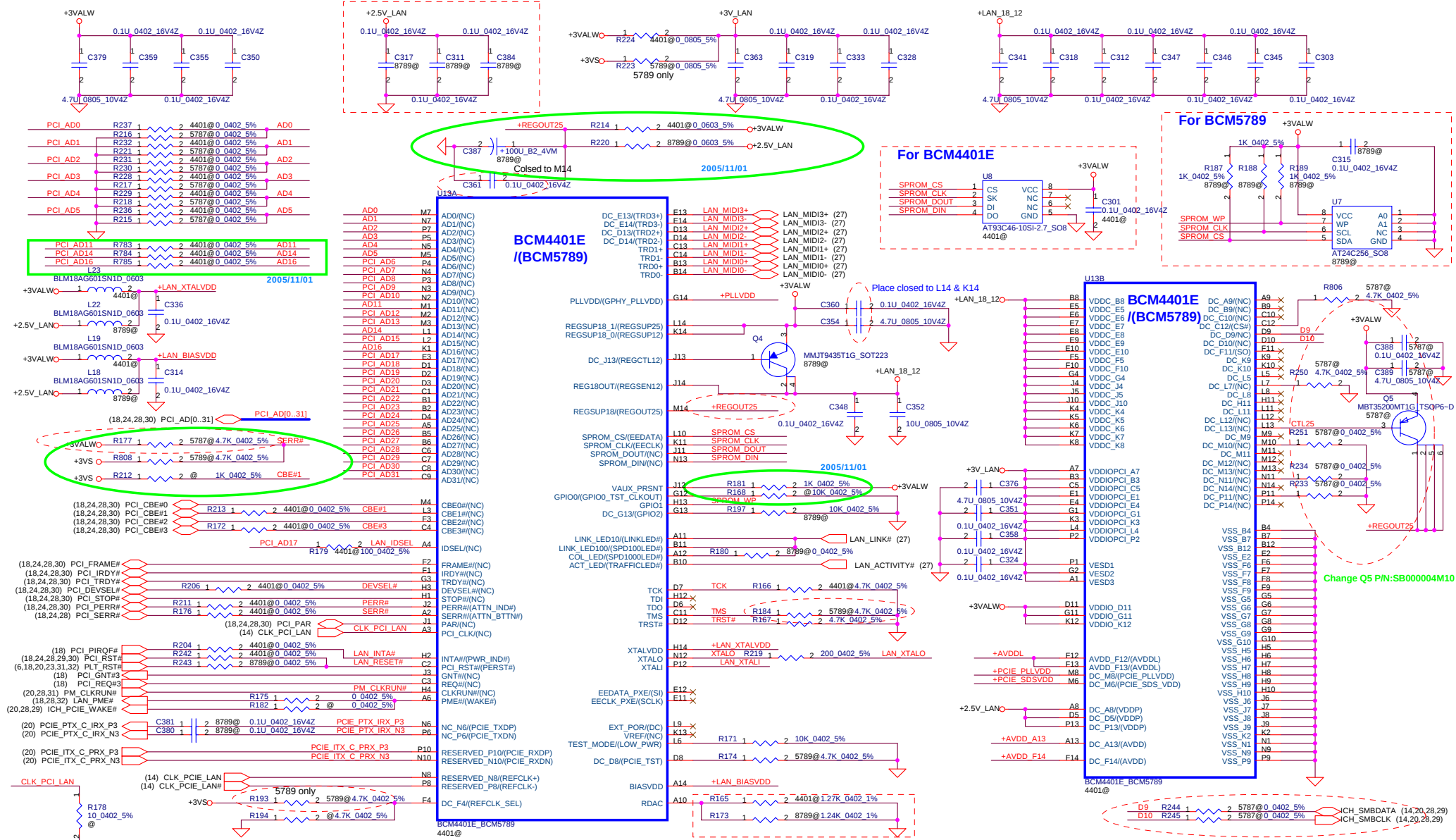
PCMCIA Socket



4 IN 1 Socket (HDQ70)



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Size B		Document Number		Rev 0.2	
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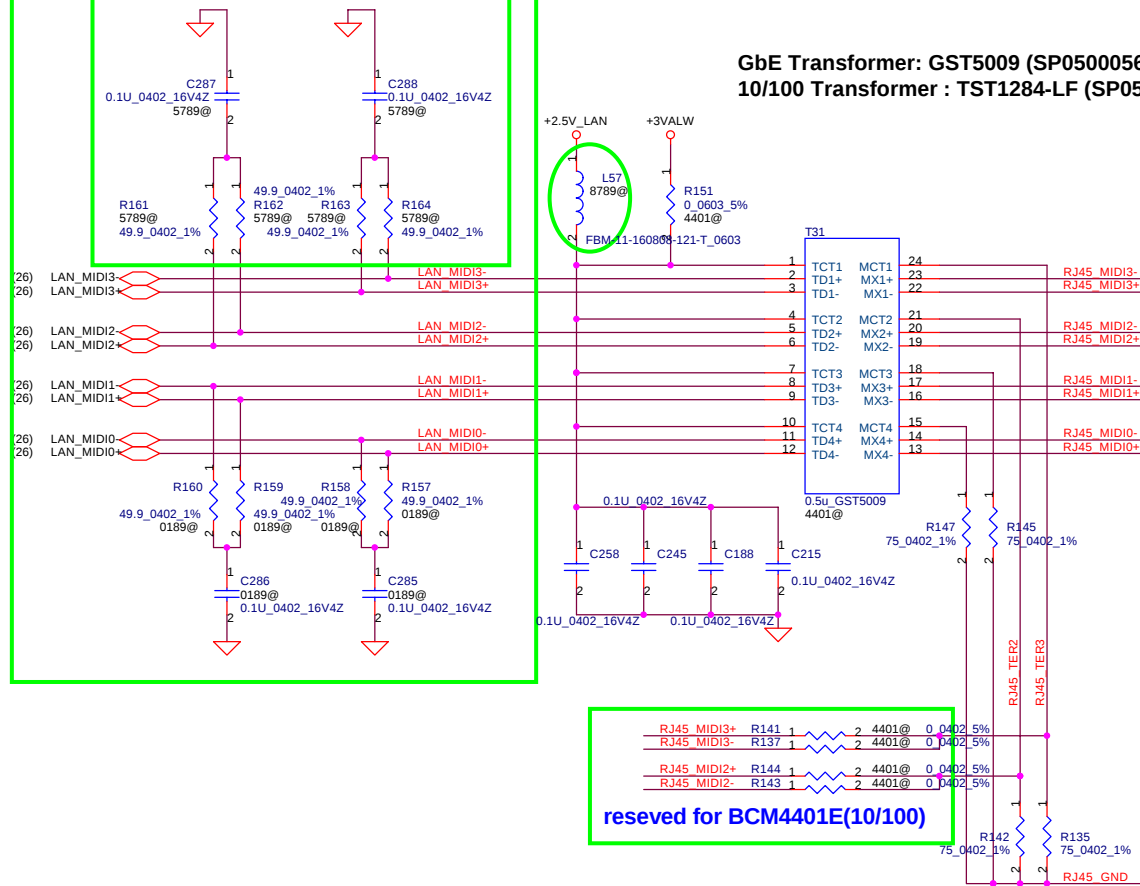


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Issued Date				Deciphered Date				LAN BCM4401E/Jade15			
2005/06/20				2006/06/20				HBL51 LA-3081P			
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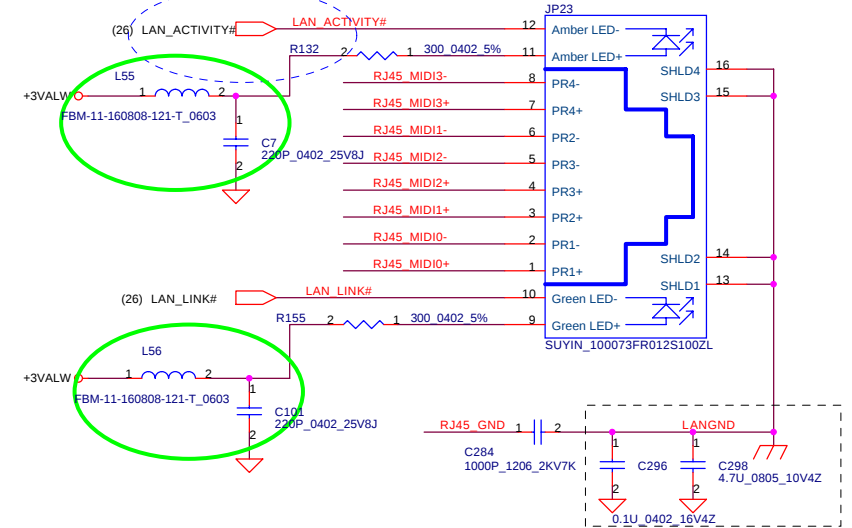
LAN BCM4401E/ BCM5789

Place these components colsed to LAN chip

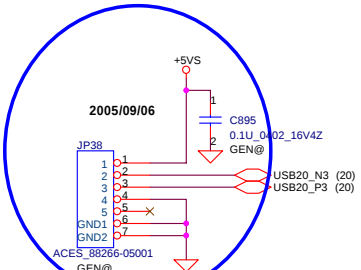
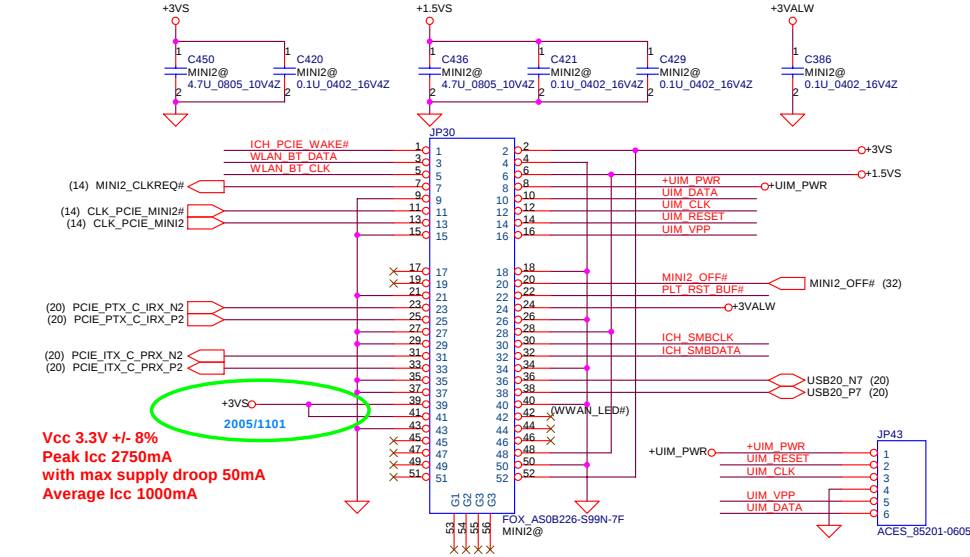
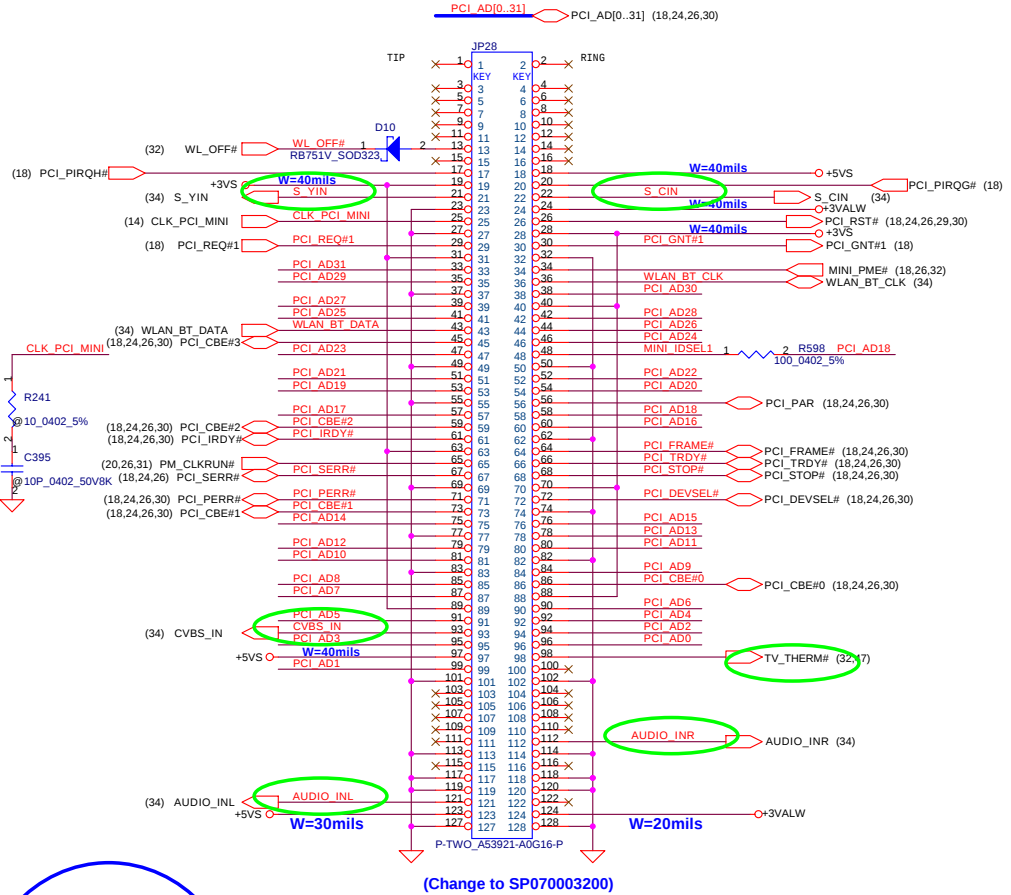
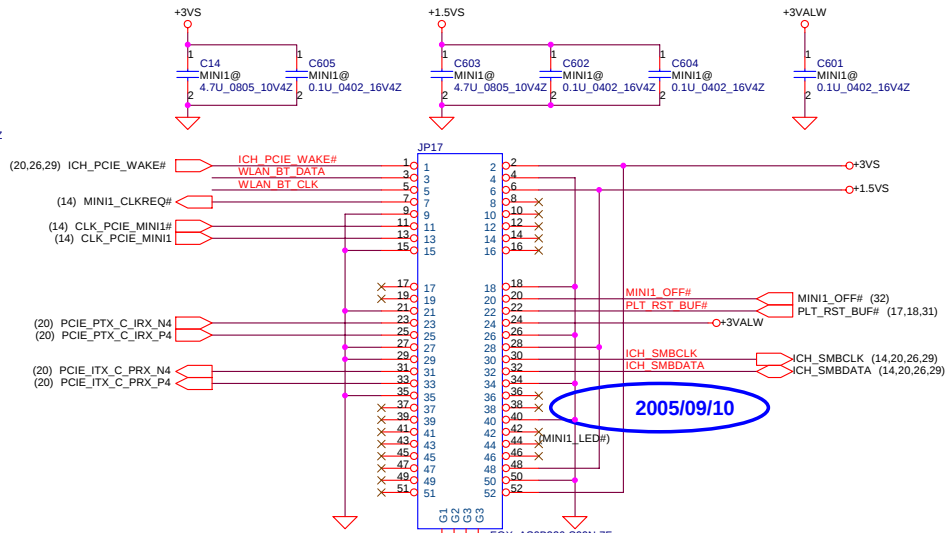
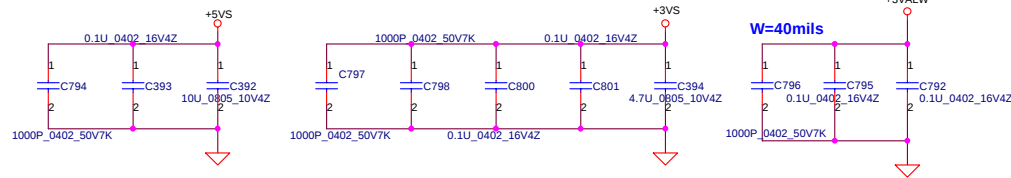
unpop when use BCM4401E(10/100)



09/06 modified (symbol must be updated)

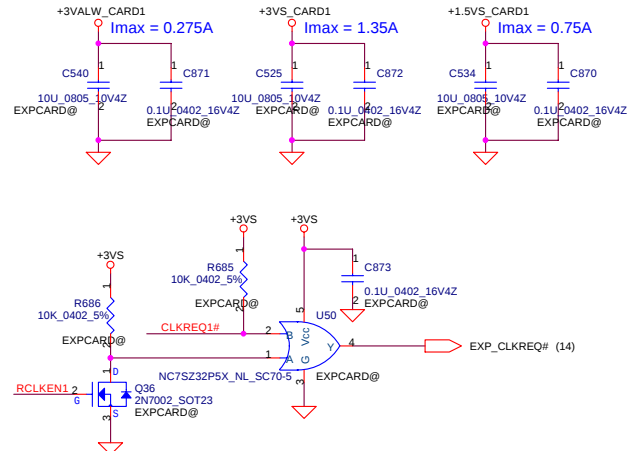
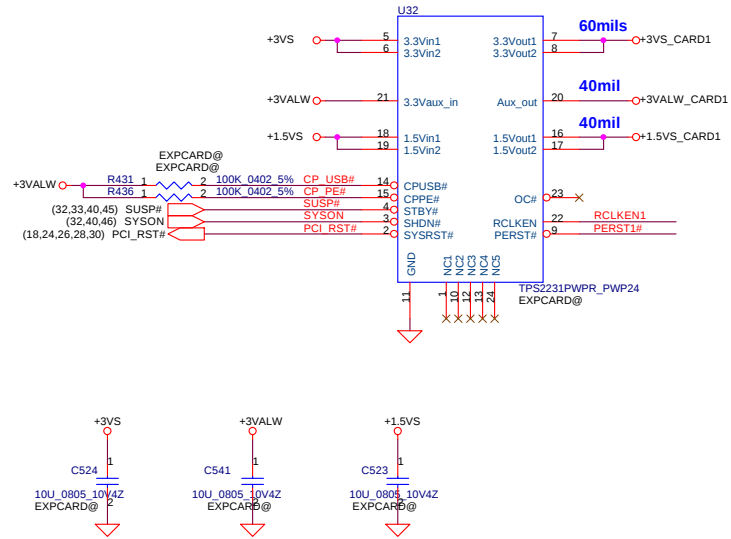


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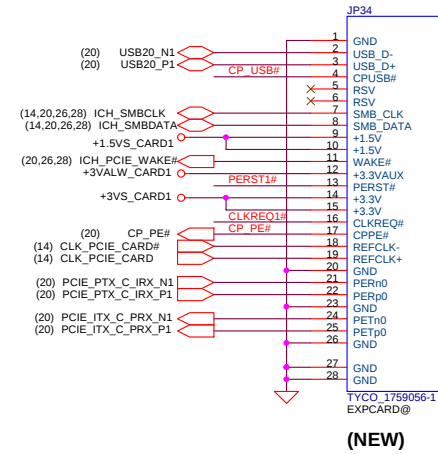


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	
+3VS	1000	750	Normal
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

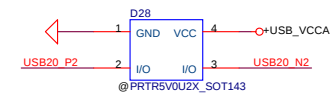
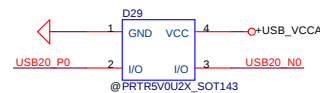
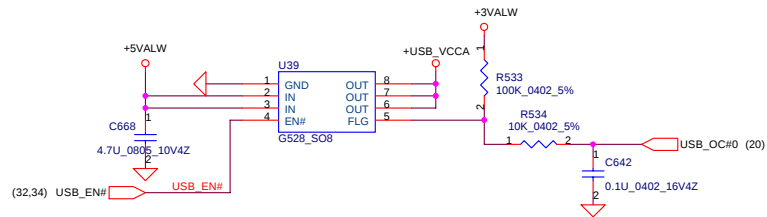
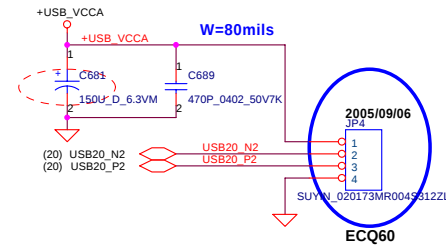
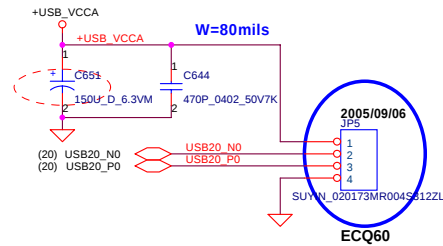
New Card Power Switch



New Card Socket (Left)



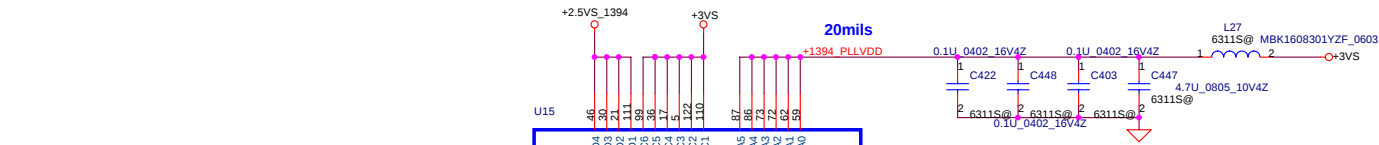
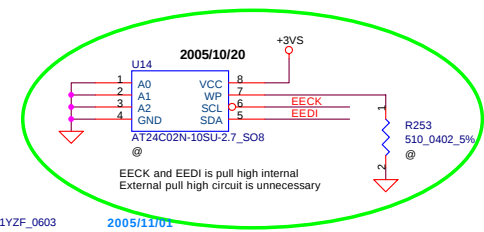
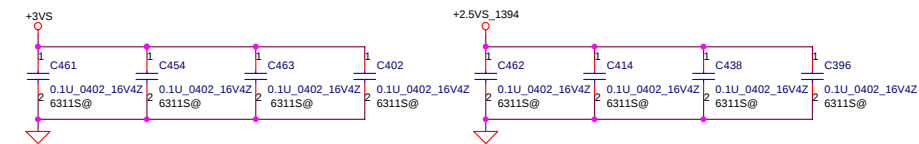
USB CONN. 1 & 2



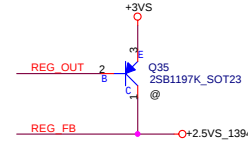
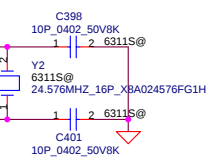
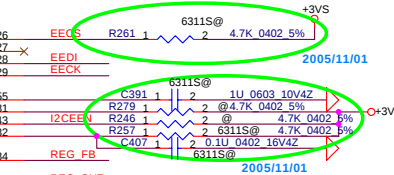
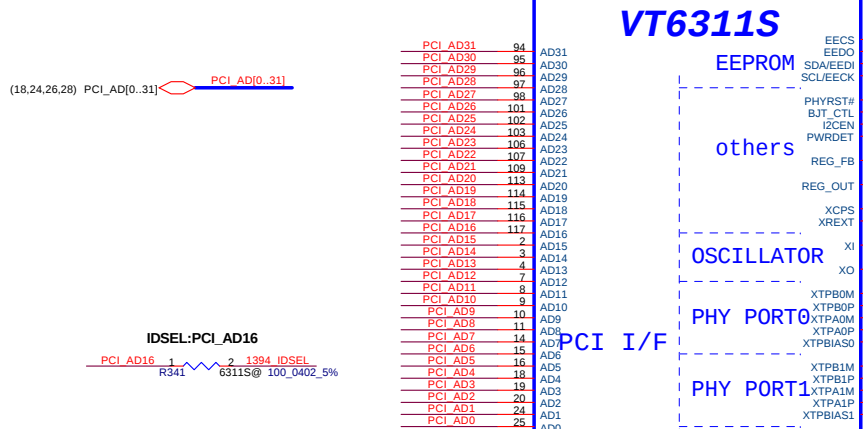
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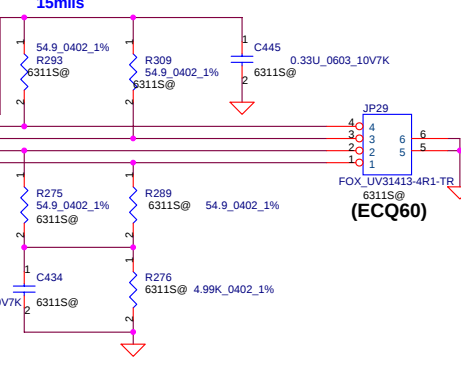
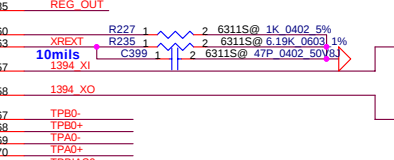
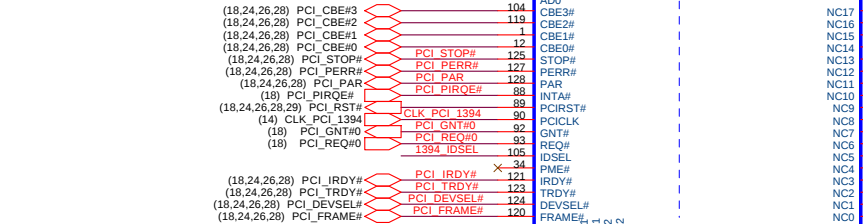
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title NEW CARD SOCKET		
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When use external EEPROM
Populate U14, R246, R253
Un-populate R261



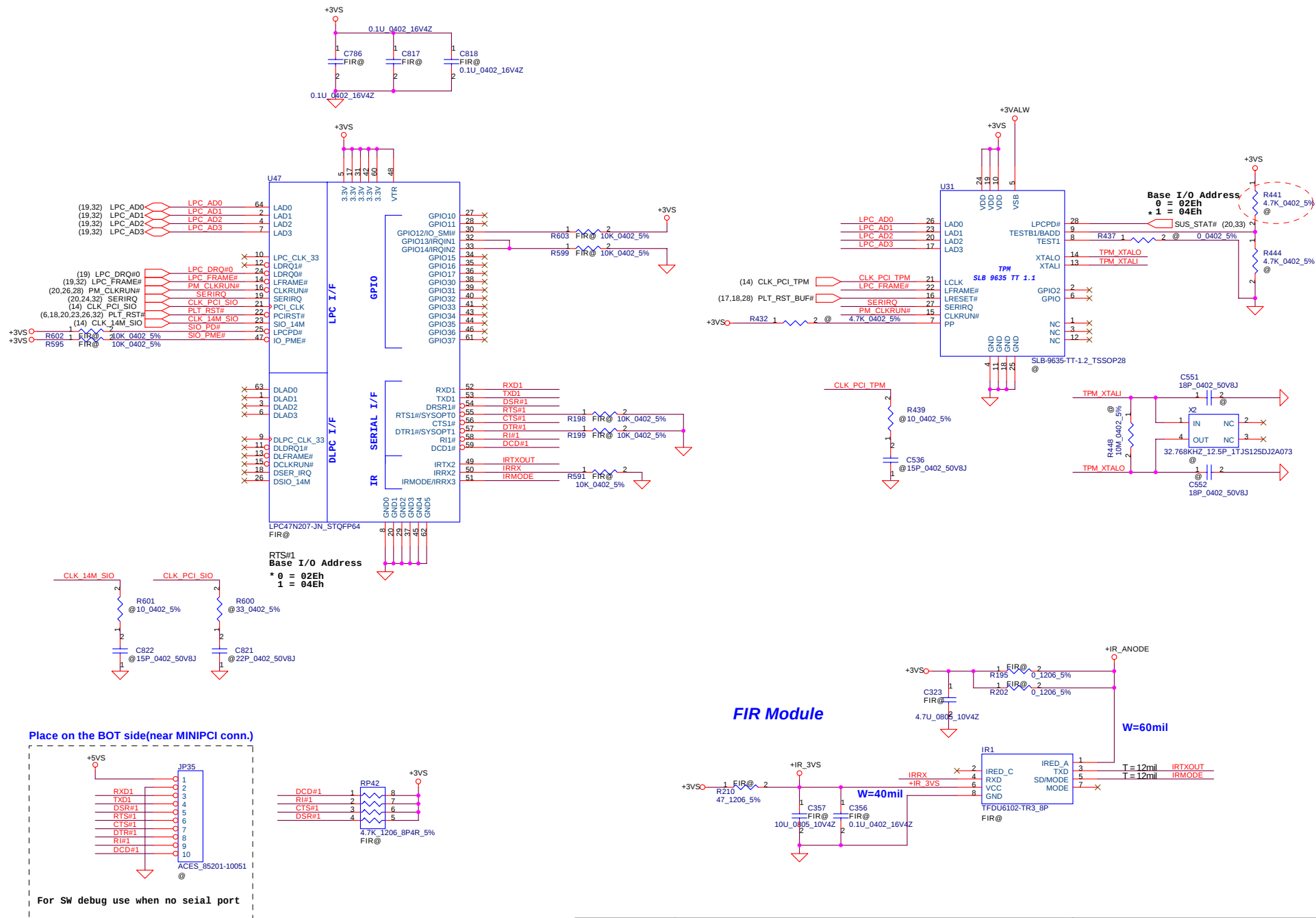
When use external BJT
Populate Q35, R279



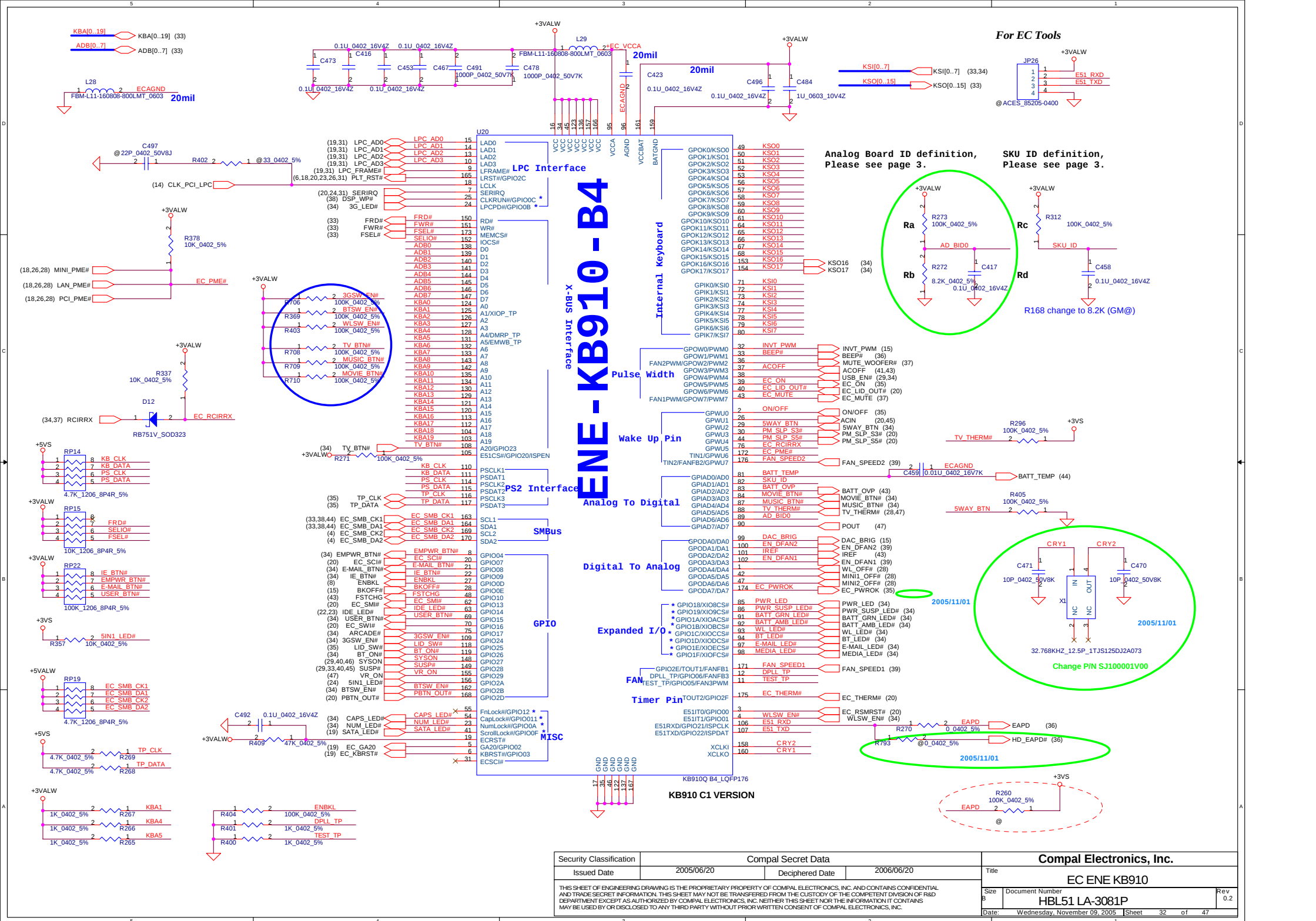
(ECQ60)

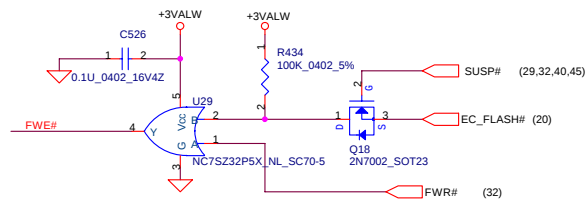
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	
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Size B	Document Number	HBL51 LA-3081P		Rev 0.2	
Date: Wednesday, November 09, 2005		Sheet 30 of 47			

SUPER I/O SMsC LPC47N207

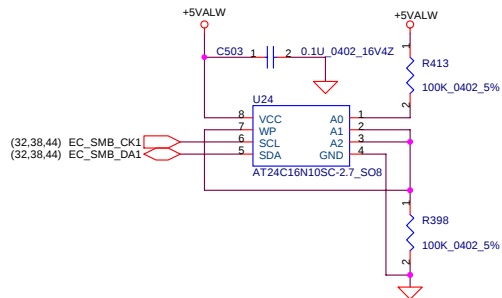


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								Size B	Document Number				Rev 0.2	
								Date:	Wednesday, November 09, 2006		ISheet	31	of	47
						HBL51 LA-3081P								

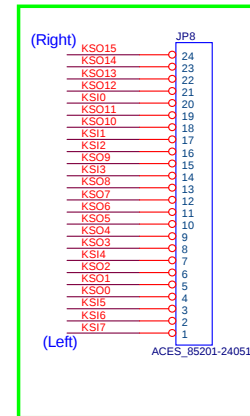
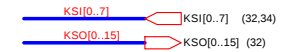




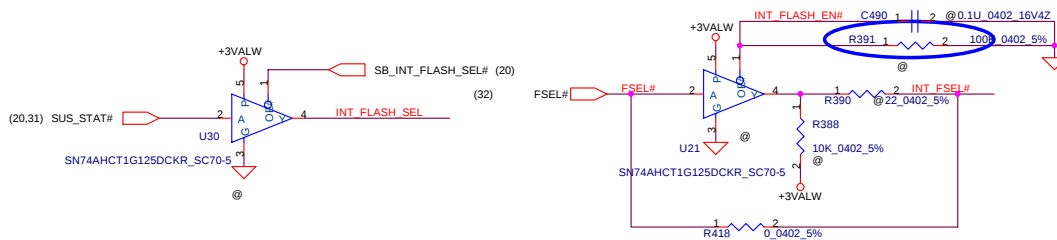
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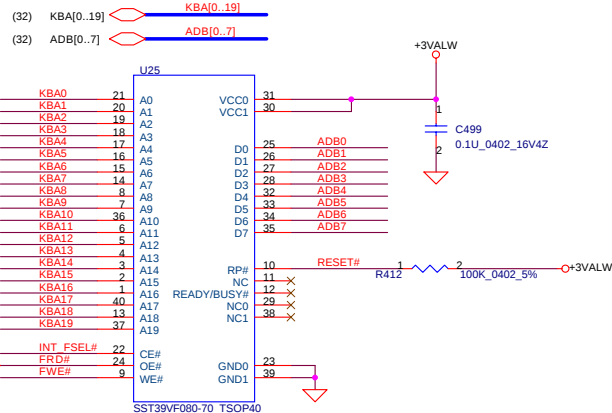
INT_KBD Conn.



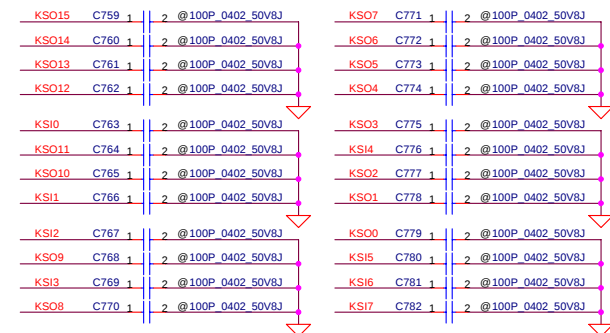
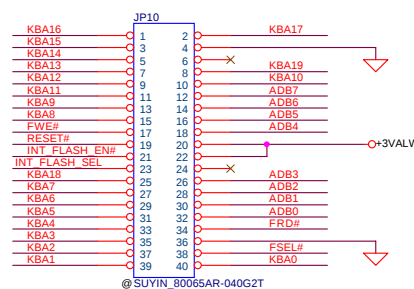
2005/11/03



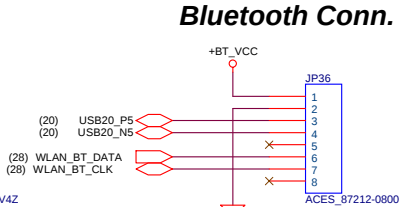
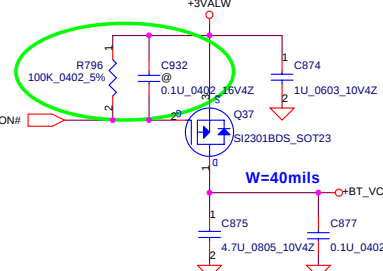
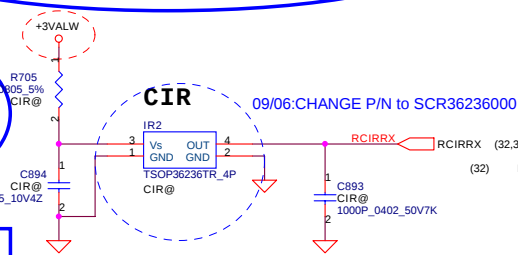
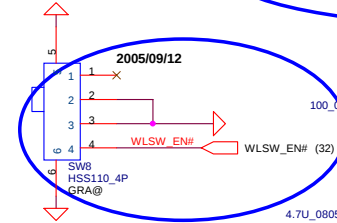
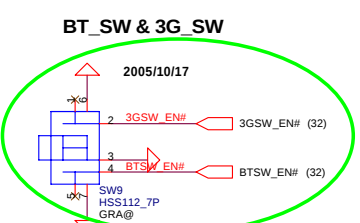
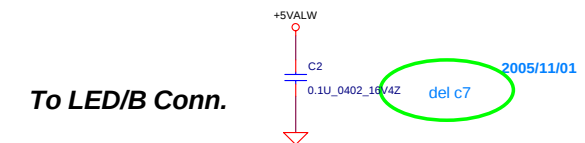
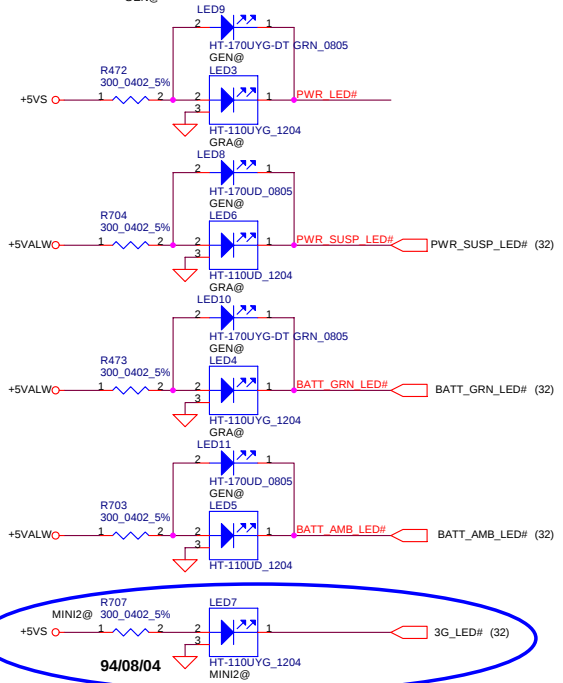
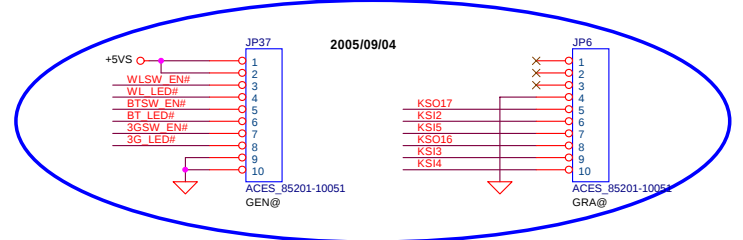
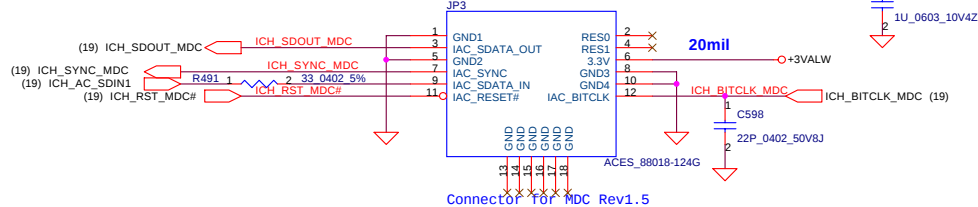
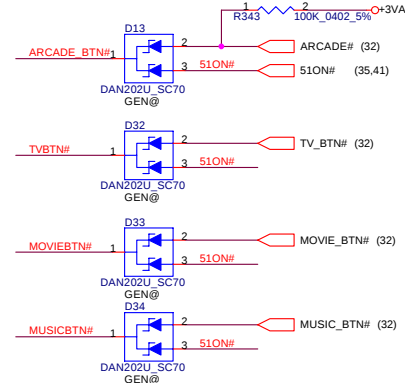
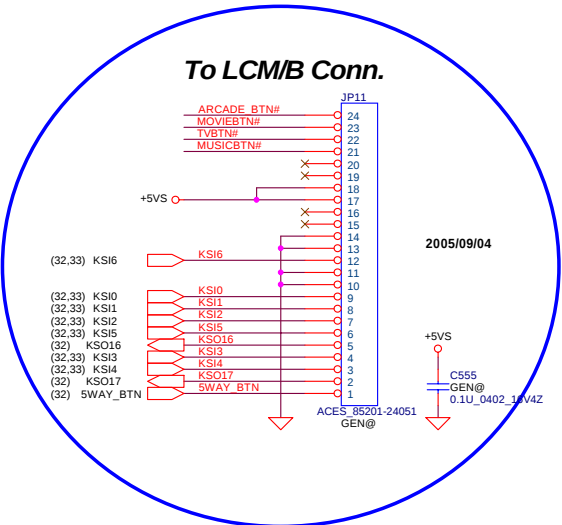
1MB Flash ROM



1MB ROM Socket



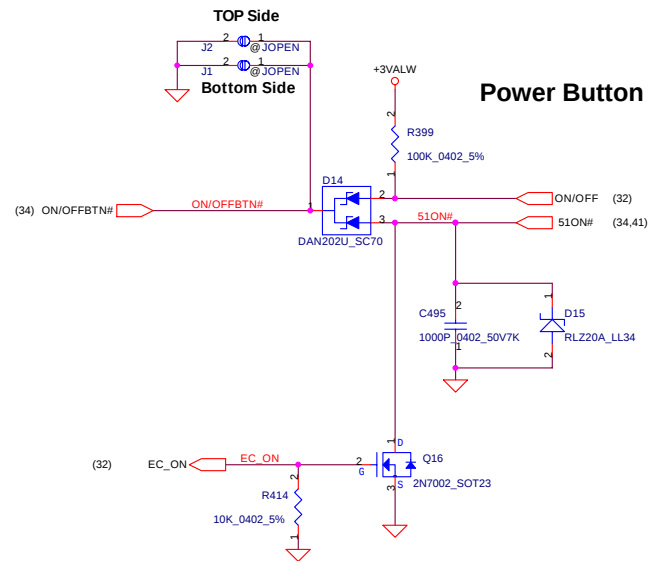
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								Size B	Document Number	HBL51 LA-3081P		Rev	0.2
								Date:	Wednesday, November 09, 2005	Sheet	33	of	47



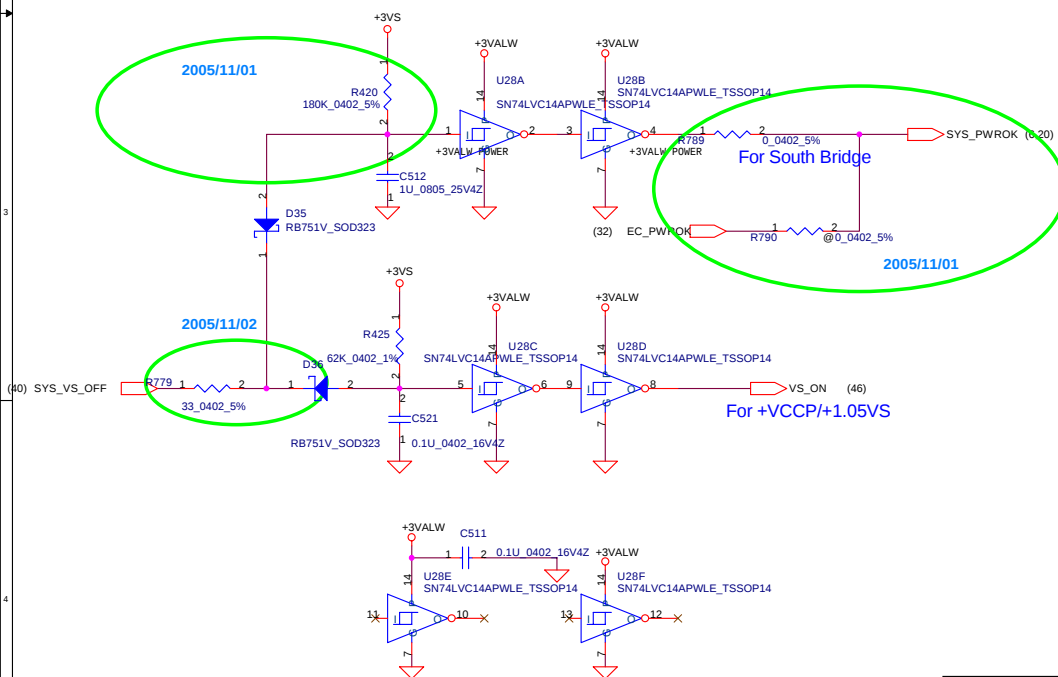
Geneva			Grapevine		
	KSO16	KSO17		KSO16	KSO17
KSI0	VOL_UP	LEFT			
KSI1	RIGHT	VOL_DOWN			
KSI2	PLAY	ENTER			
KSI3	STOP				
KSI4	NEXT				
KSI5	REV				
KSI6		RECORD			

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										LCM / MDC / BT / CIR / LED	
										Size B	
										Document Number	
										HBL51 LA-3081P	
										Rev	
										0.2	
										Date: Wednesday, November 09, 2005	
										Sheet 34 of 47	

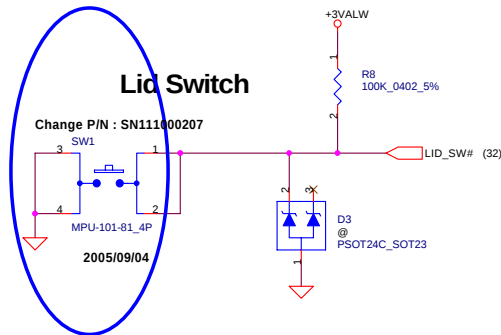
ON/OFF switch



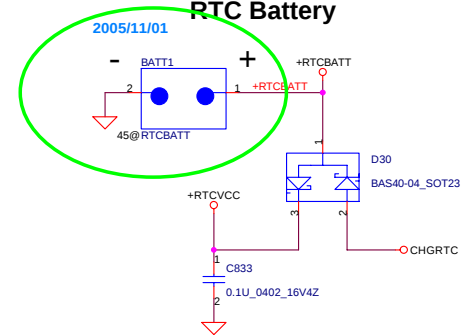
Power ON Circuit



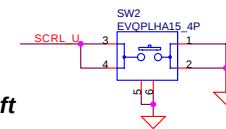
~~Lid Switch~~



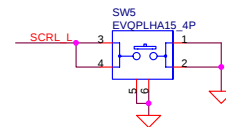
~~RTC Battery~~



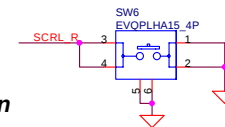
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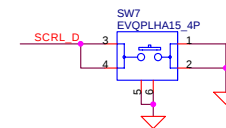
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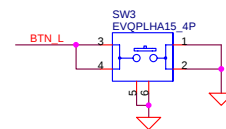
Scroll Right



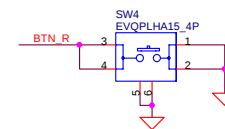
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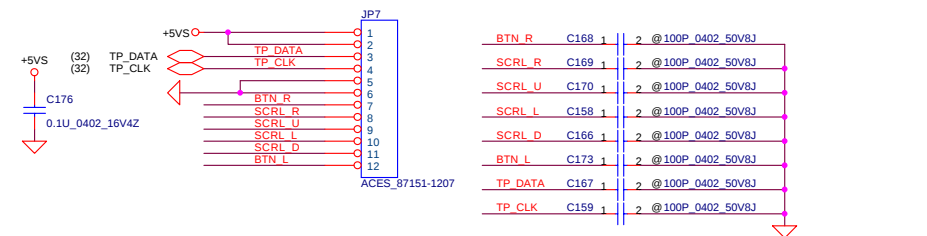
Left



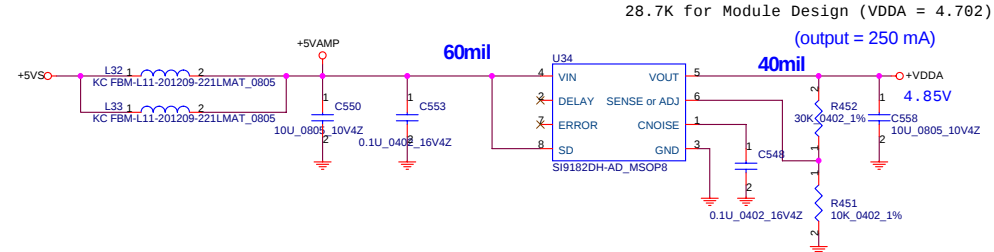
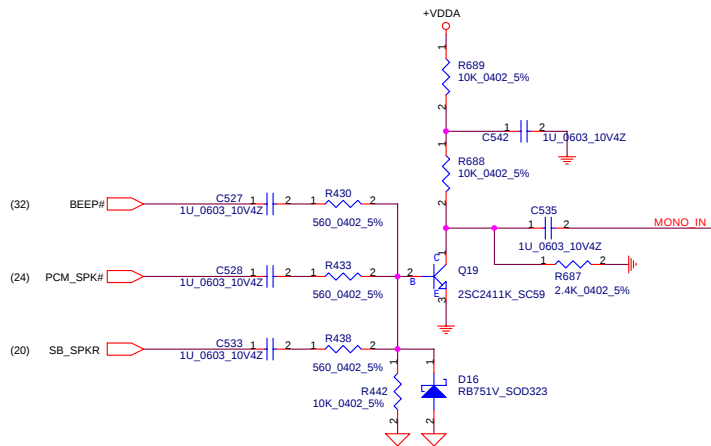
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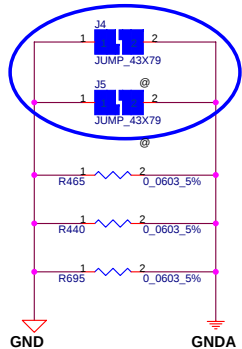
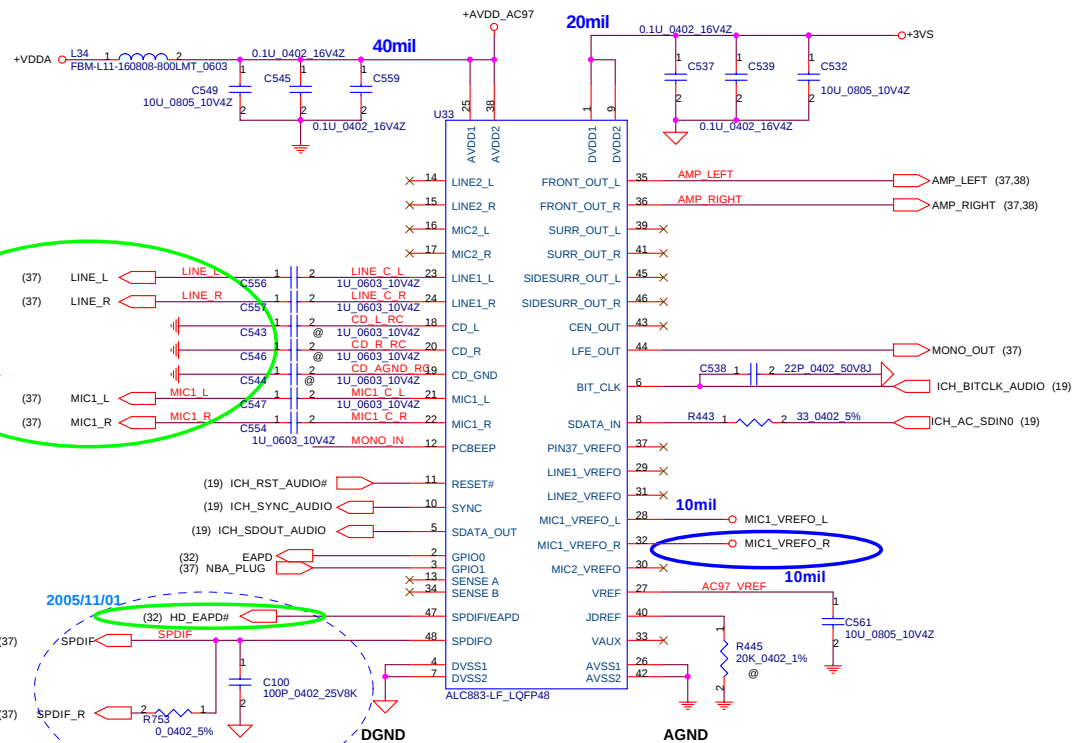
To TP/B Conn.



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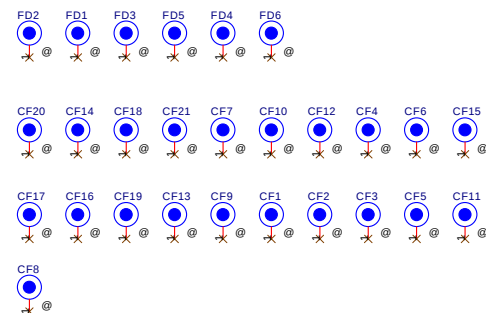
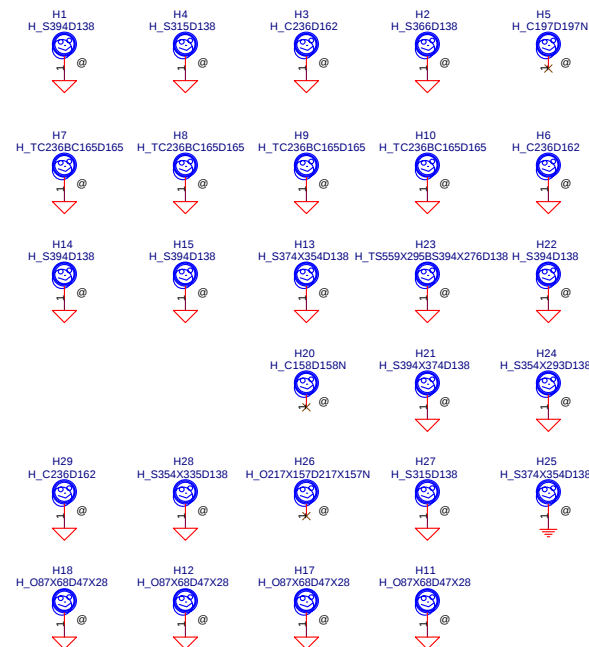
HD Audio Codec



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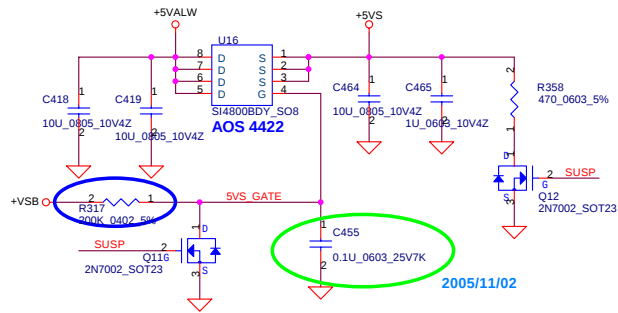
[illegible]

The schematic diagram illustrates the fan speed control circuit. It features a 5V5V supply connected to a 10U_1206_16V4Z capacitor (C338) and a 1SS355_SOD323 diode (D8). A 3V3V supply is connected to a 10K_0402_5% resistor (R207) and a 1000P_0402_50V7K capacitor (C344). The circuit also includes a 40mil trace, a 1N4148_SOT23 diode (D9), another 10U_1206_16V4Z capacitor (C339), and a 1000P_0402_50V7K capacitor (C343). The U993P1UF_SCP8 capacitor (U10) is connected to the 5V5V supply and the 3V3V supply. The circuit is connected to a 32 EN_DFN2 pin and a 32 FAN_SPEED2 pin.

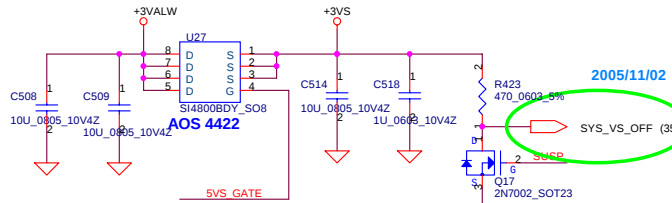


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					Size B	Document Number			HBL51 LA-3081P		Rev 0.2
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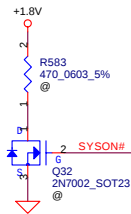
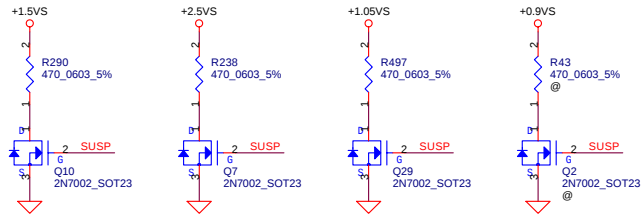
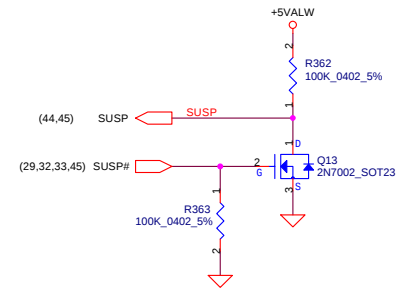
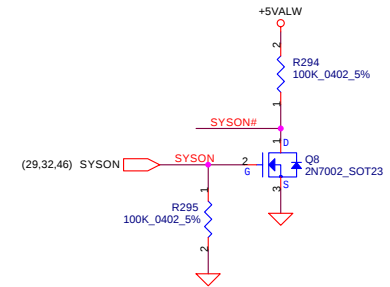
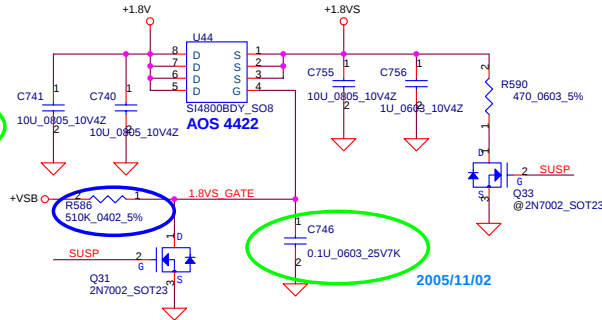
+5VALW TO +5VS



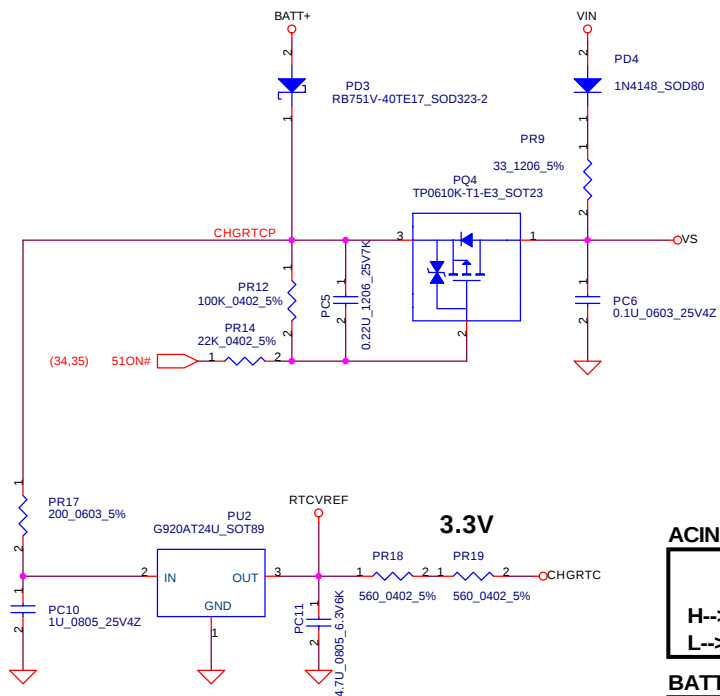
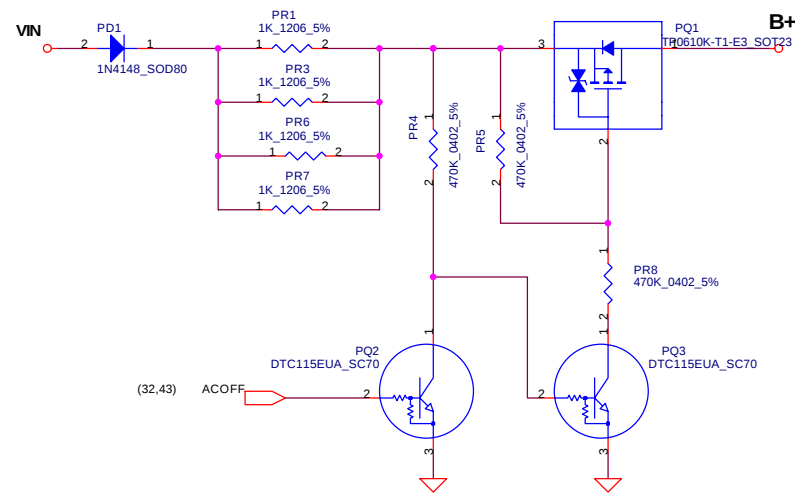
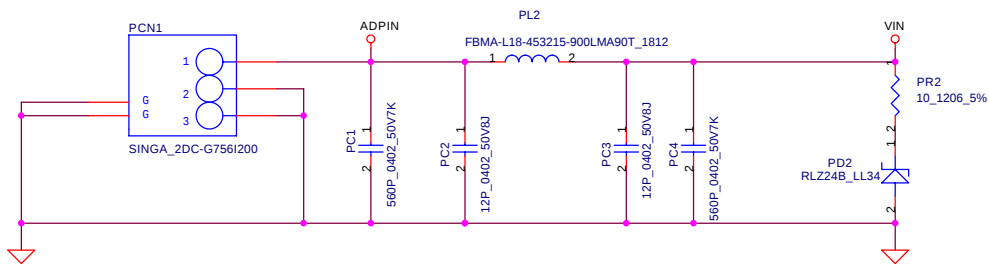
+3VALW TO +3VS



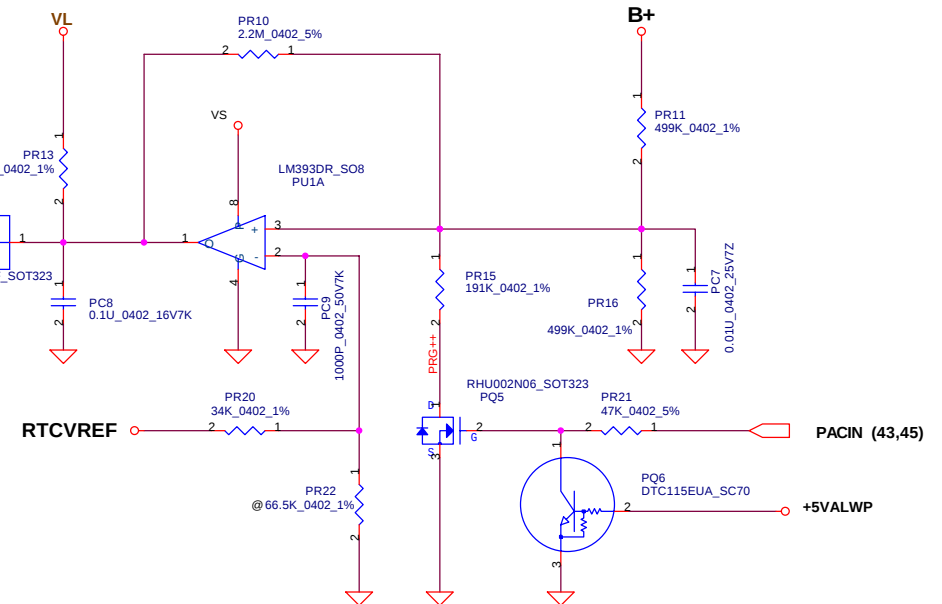
+1.8V to +1.8VS



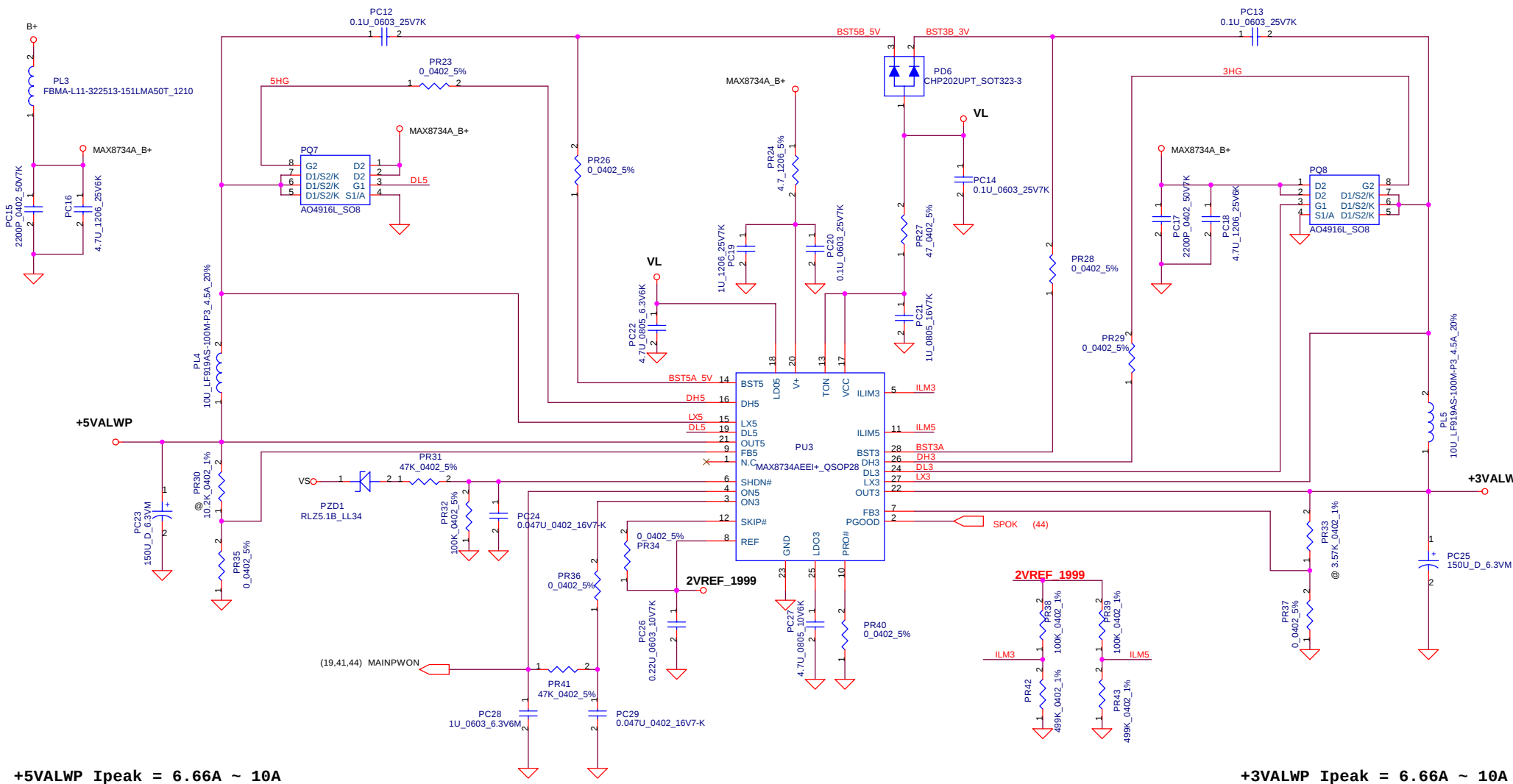
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				Size B	Document Number
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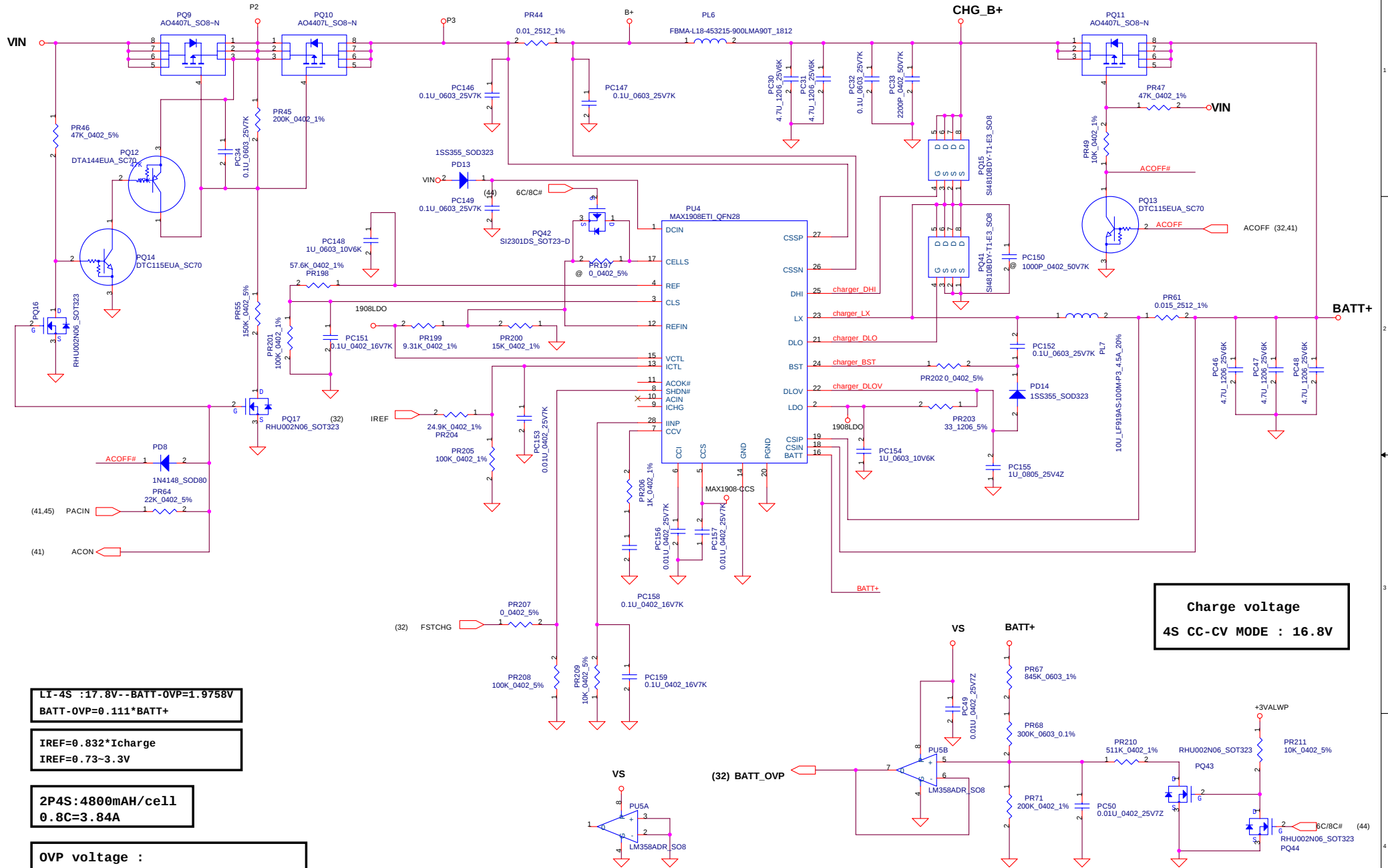
ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V
BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V



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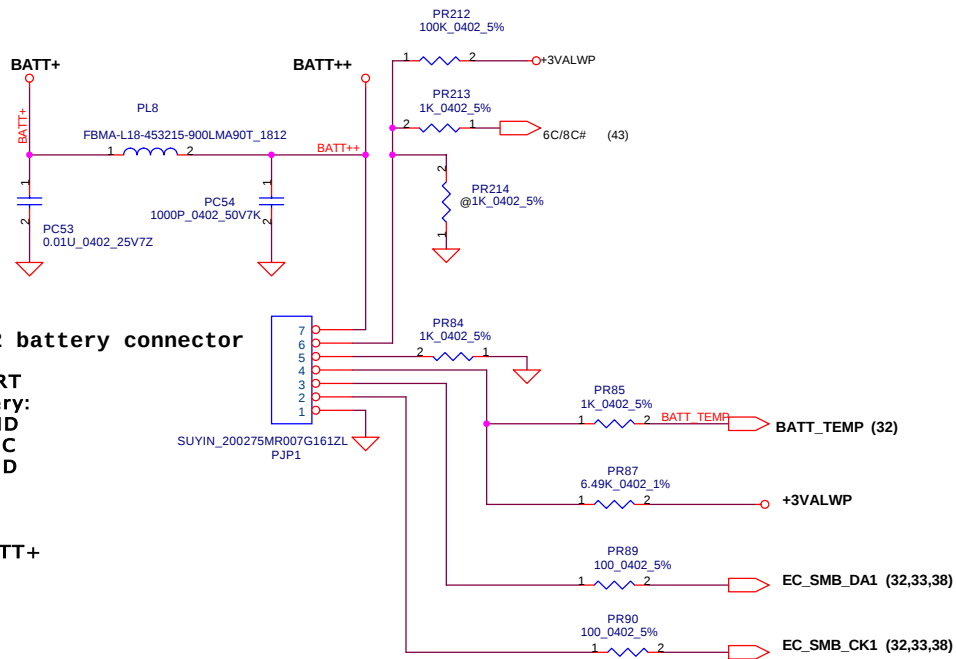
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I_{adp}=0~4.74A(90W)

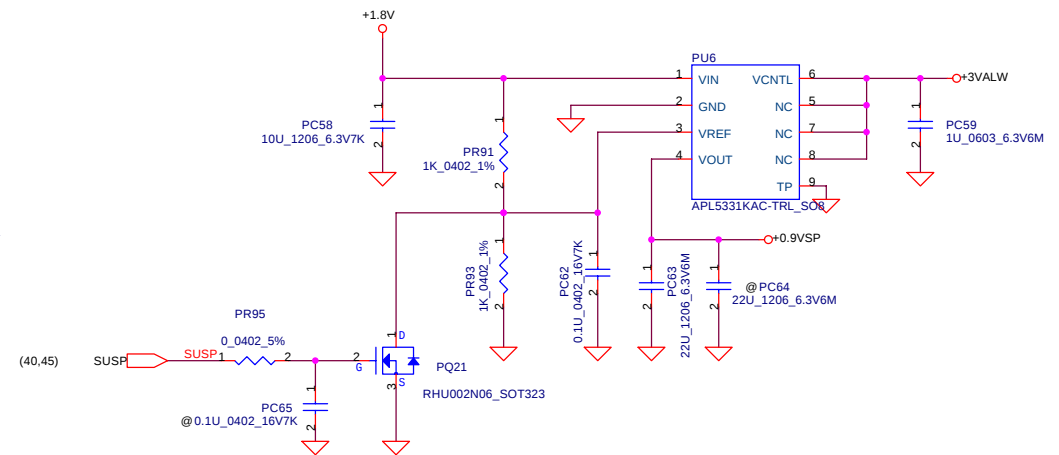
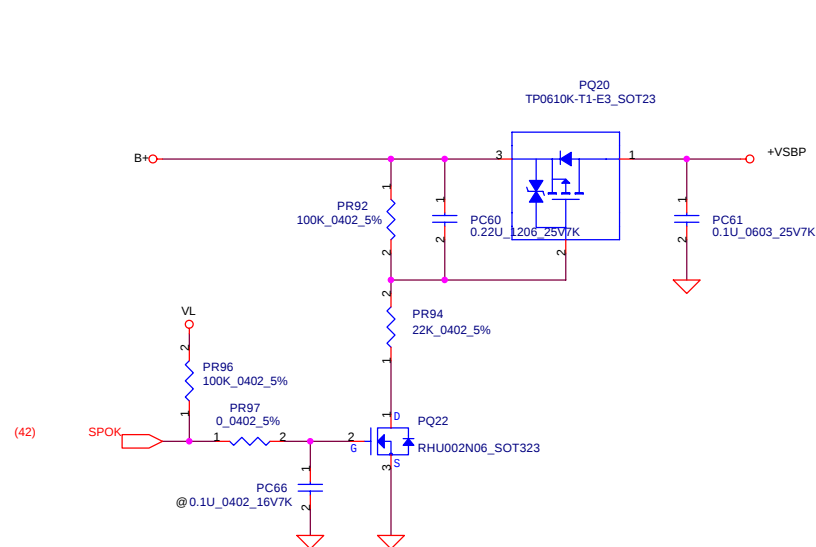
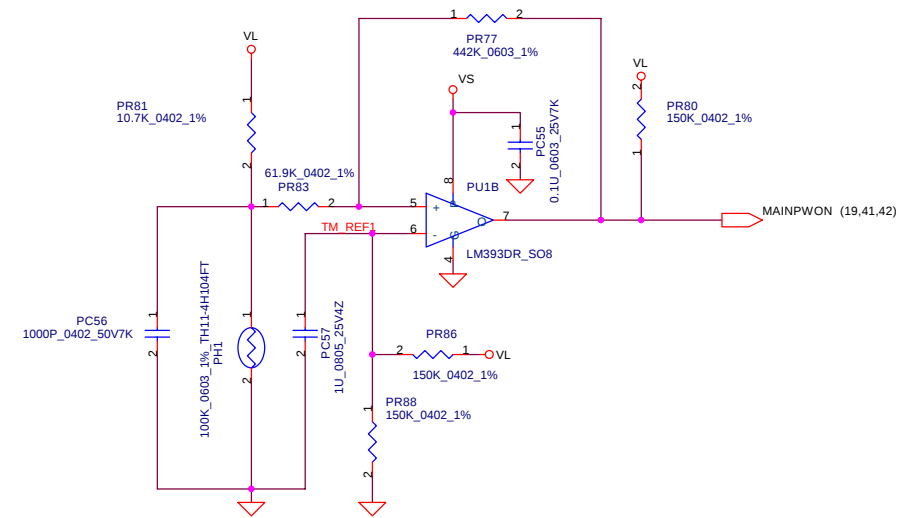
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PJP2 battery connector

SMART Battery:
 1.GND
 2.SMC
 3.SMD
 4.TS
 5.B/I
 6.ID
 7.BATT+

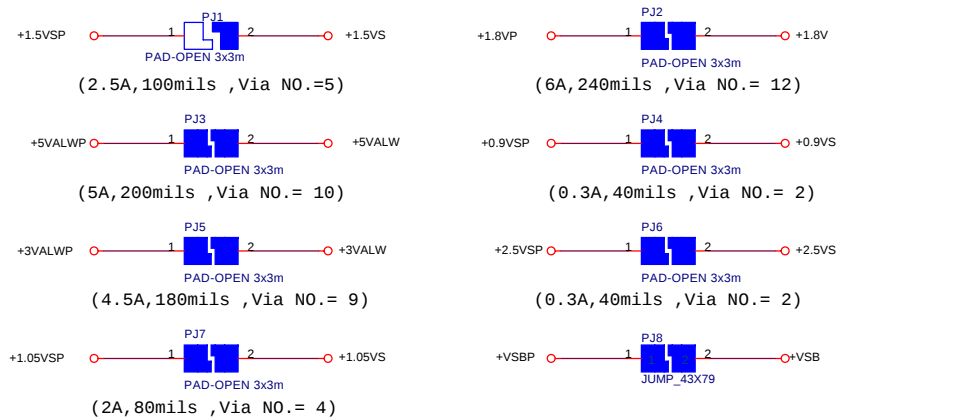


PH1 under CPU botten side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C

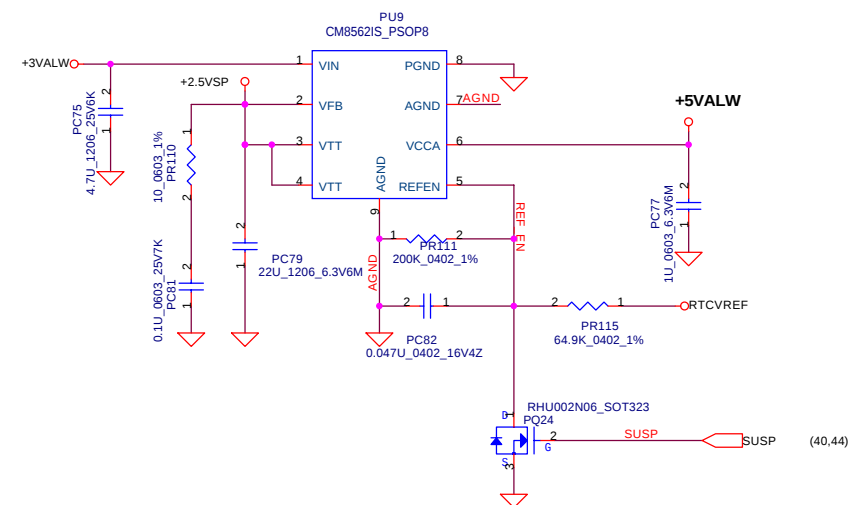
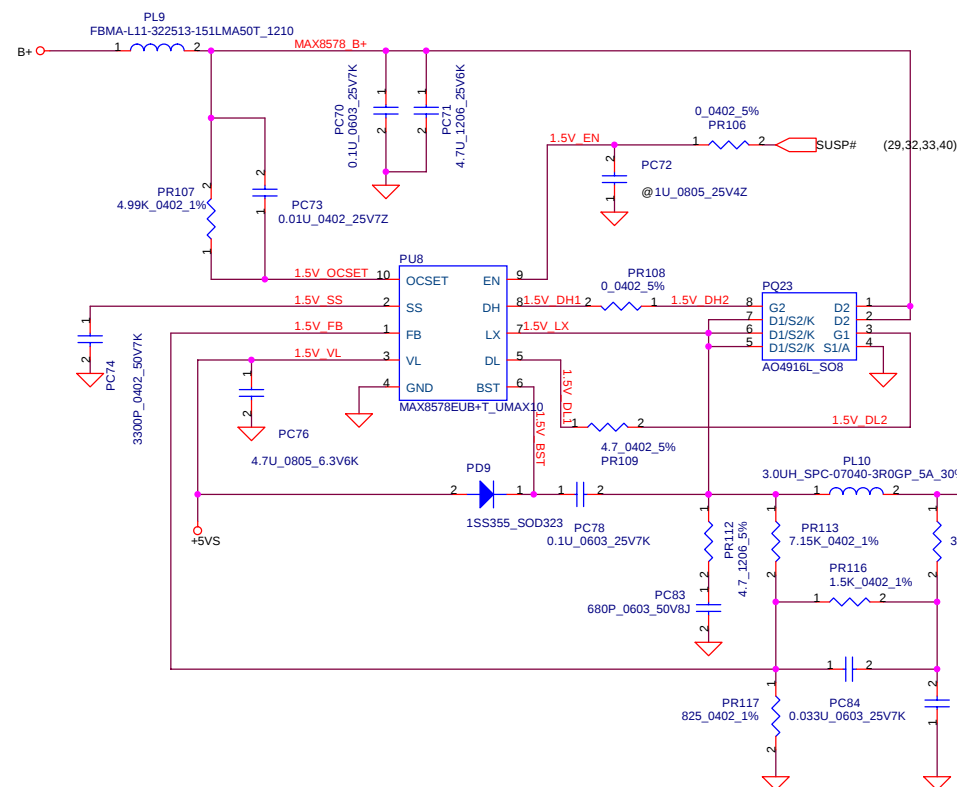
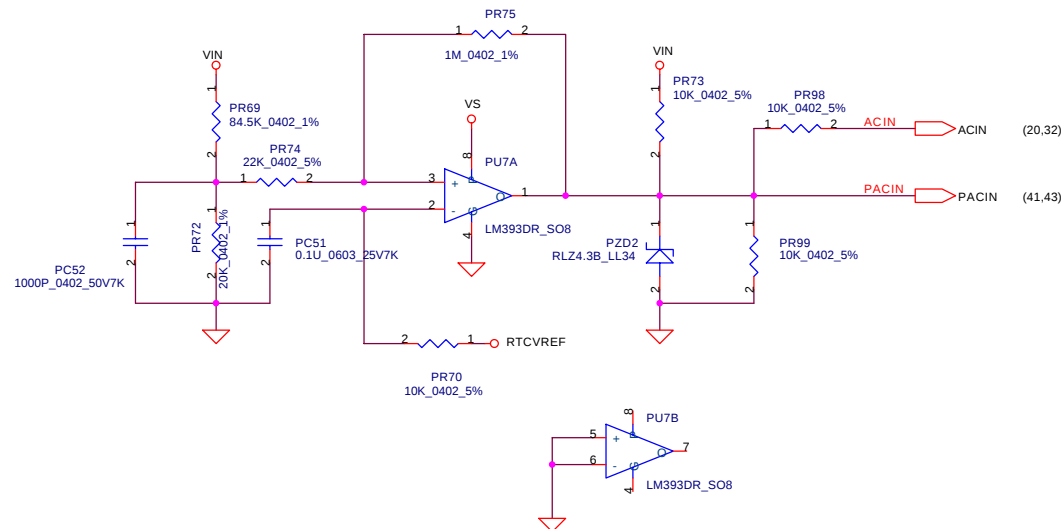


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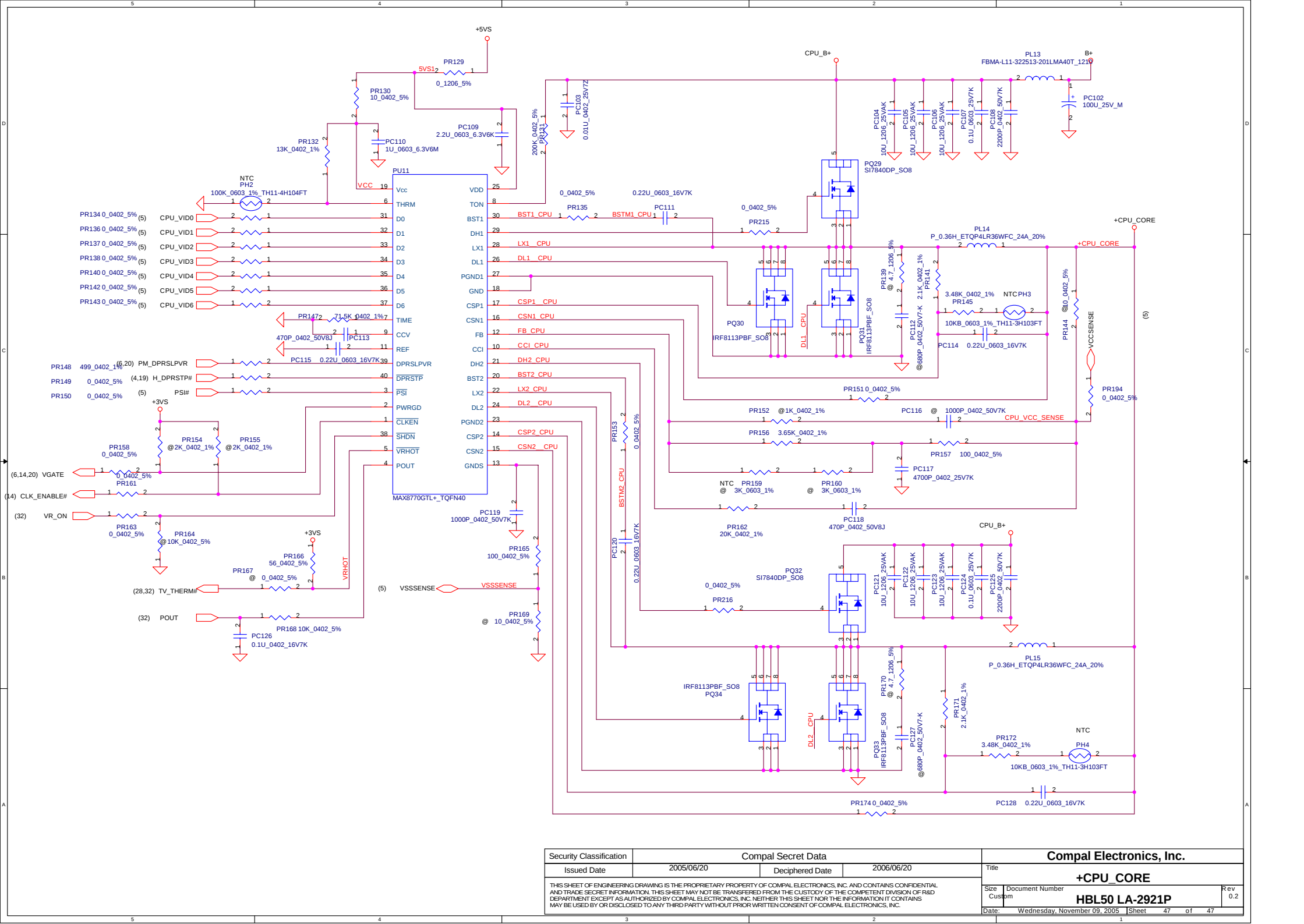
AC Adapter Detector



Vin Detector 17.90V/17.24V



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