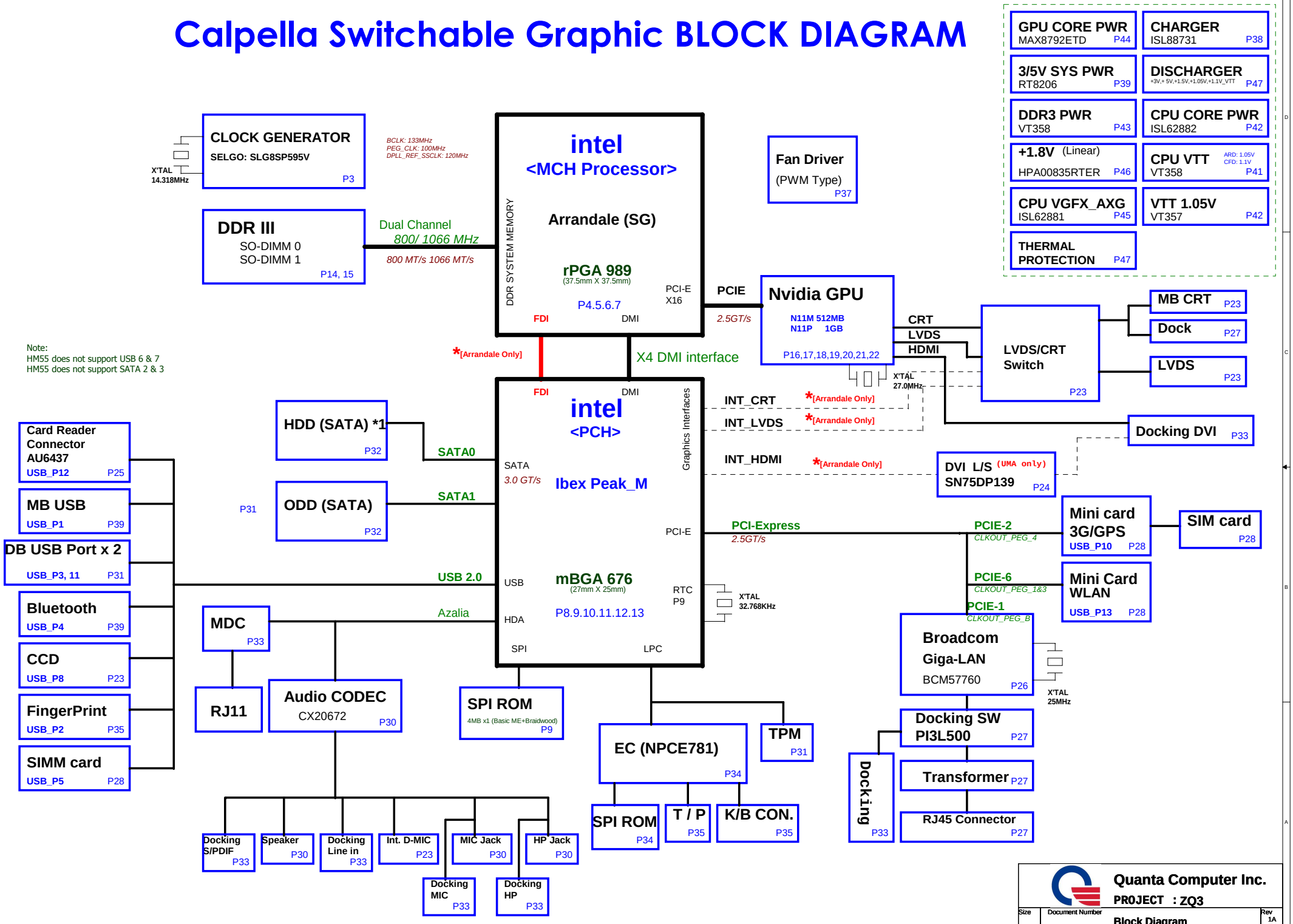
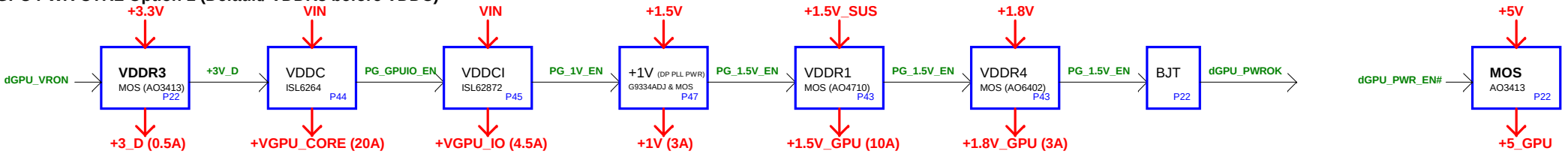
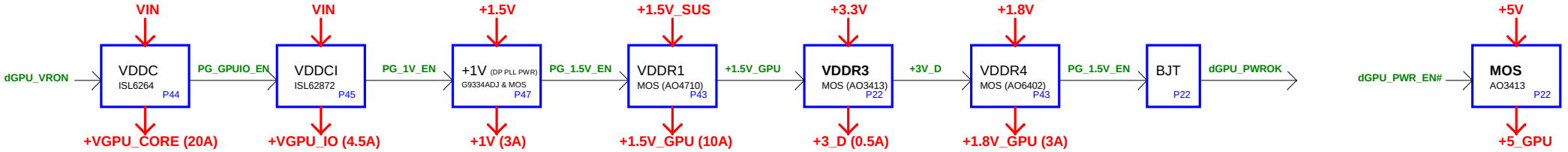
Calpella Switchable Graphic BLOCK DIAGRAM



GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



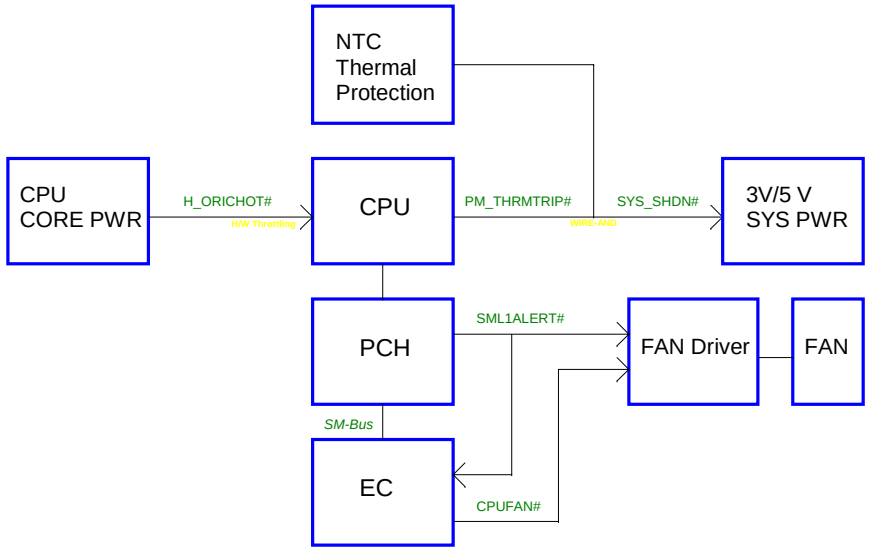
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
3V_LAN_S5	+3.3V	LAN POWER	AUX_ON	
+5VSUS	+5V		SUSD	
+3VSUS	+3.3V		SUSD	
+1.5VSUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	
+5V	+5V		MAIND	
+3V	+3.3V		MAIND	
+1.8V	+1.8V		MAINON	
+1.5V	+1.5V	PCH POWER	MAIND	
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	
+1.05V	+1.05V	PCH POWER	MAINON	
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	
MBAT+	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V		S5_ON	
+3V_S5	+3.3V		S5D	

Thermal Follow Chart



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PROJECT : ZQ3

Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

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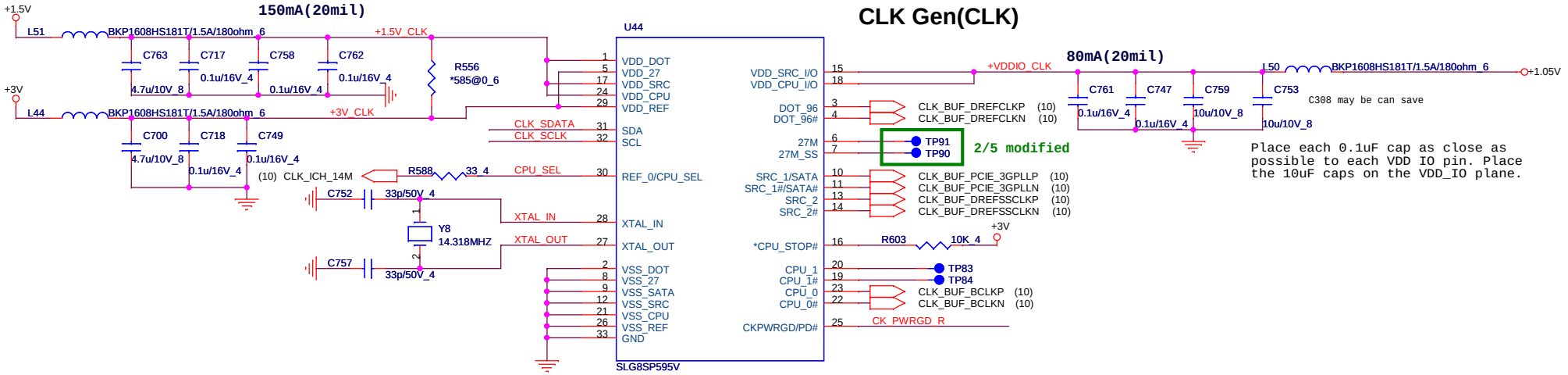
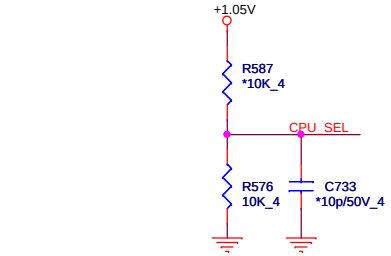
CLK Gen(CLK)

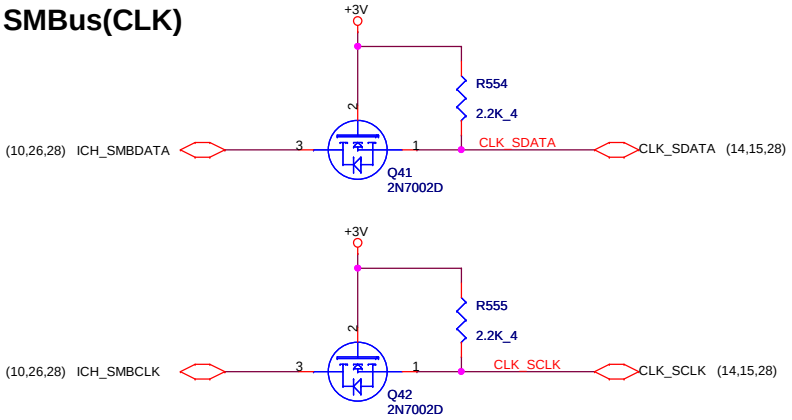


CPU_CLK select(CLK)

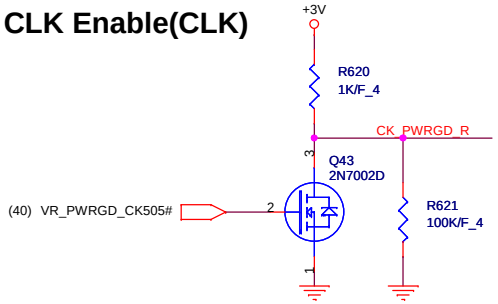


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus(CLK)



CLK Enable(CLK)



Quanta Computer Inc.

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Size	Document Number	Rev
	Clock Generator	1A

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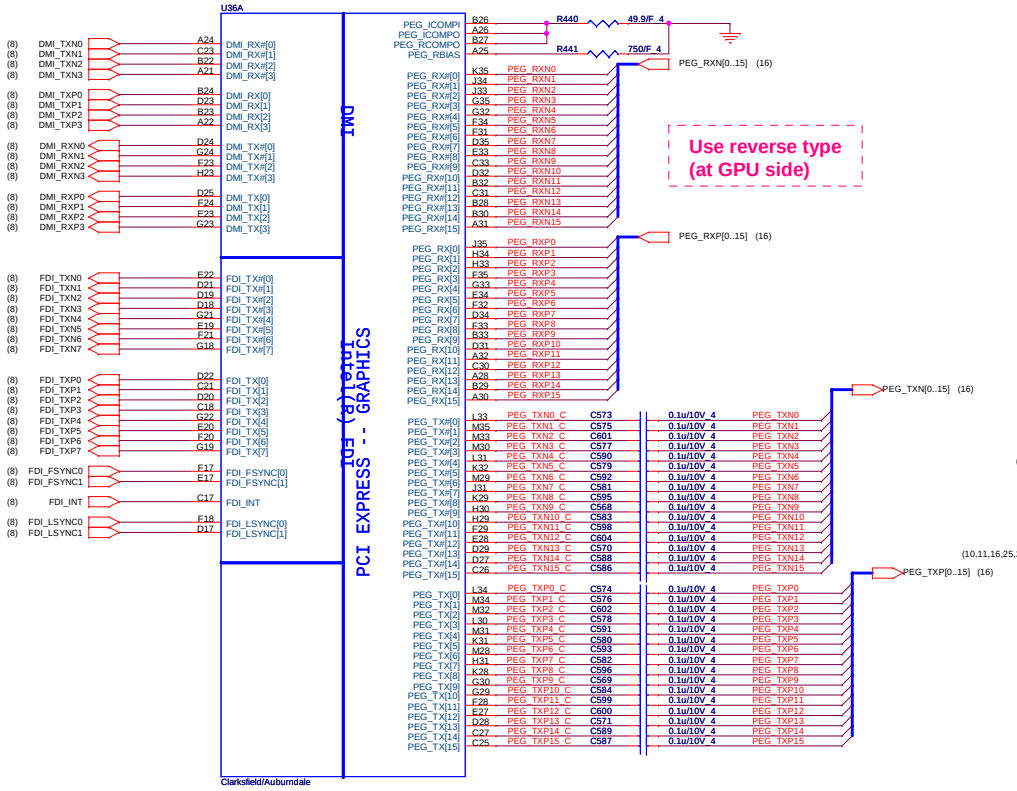
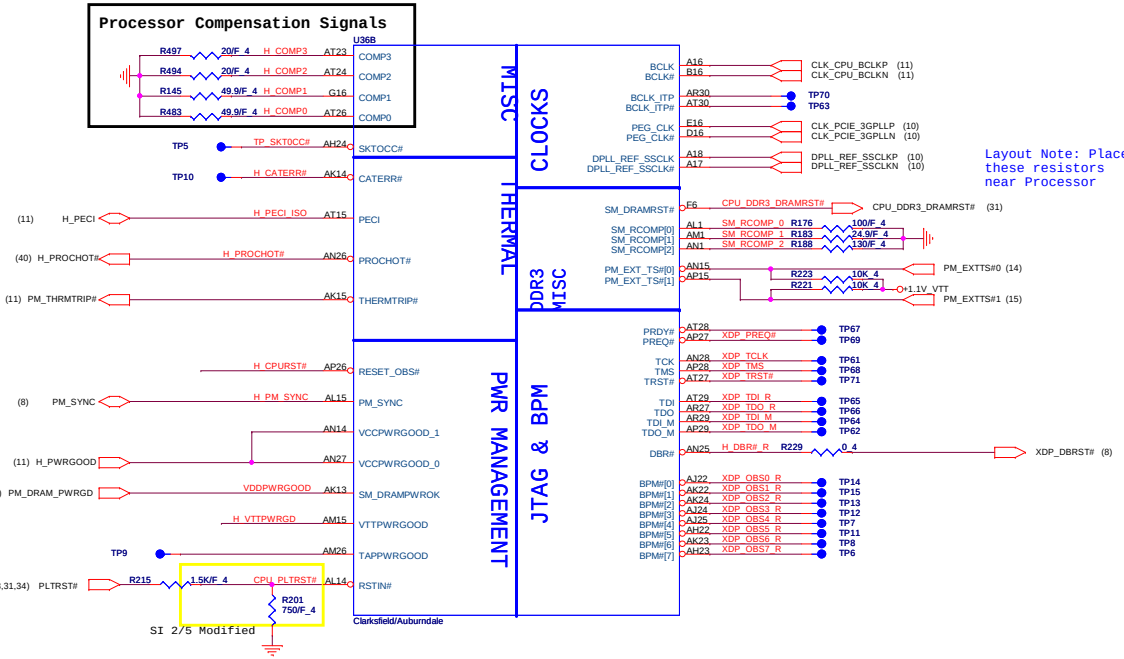
Arrandale_1(CPU)

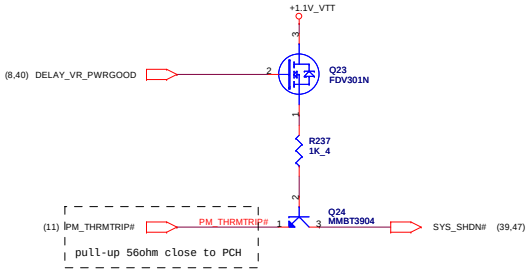
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



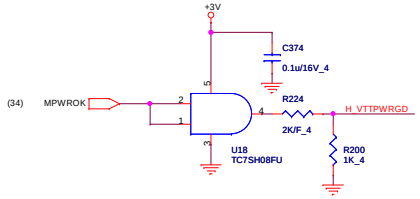
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



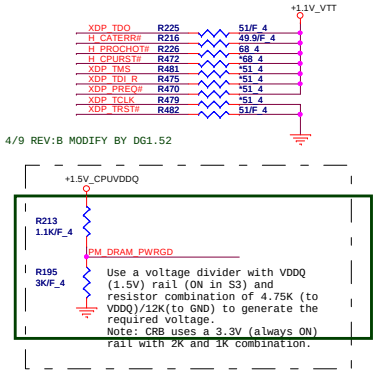
Thermaltrip protect



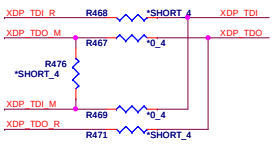
VTT PWR_Good



Processor pull-up



JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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	AUBURNDA 1/4	1A

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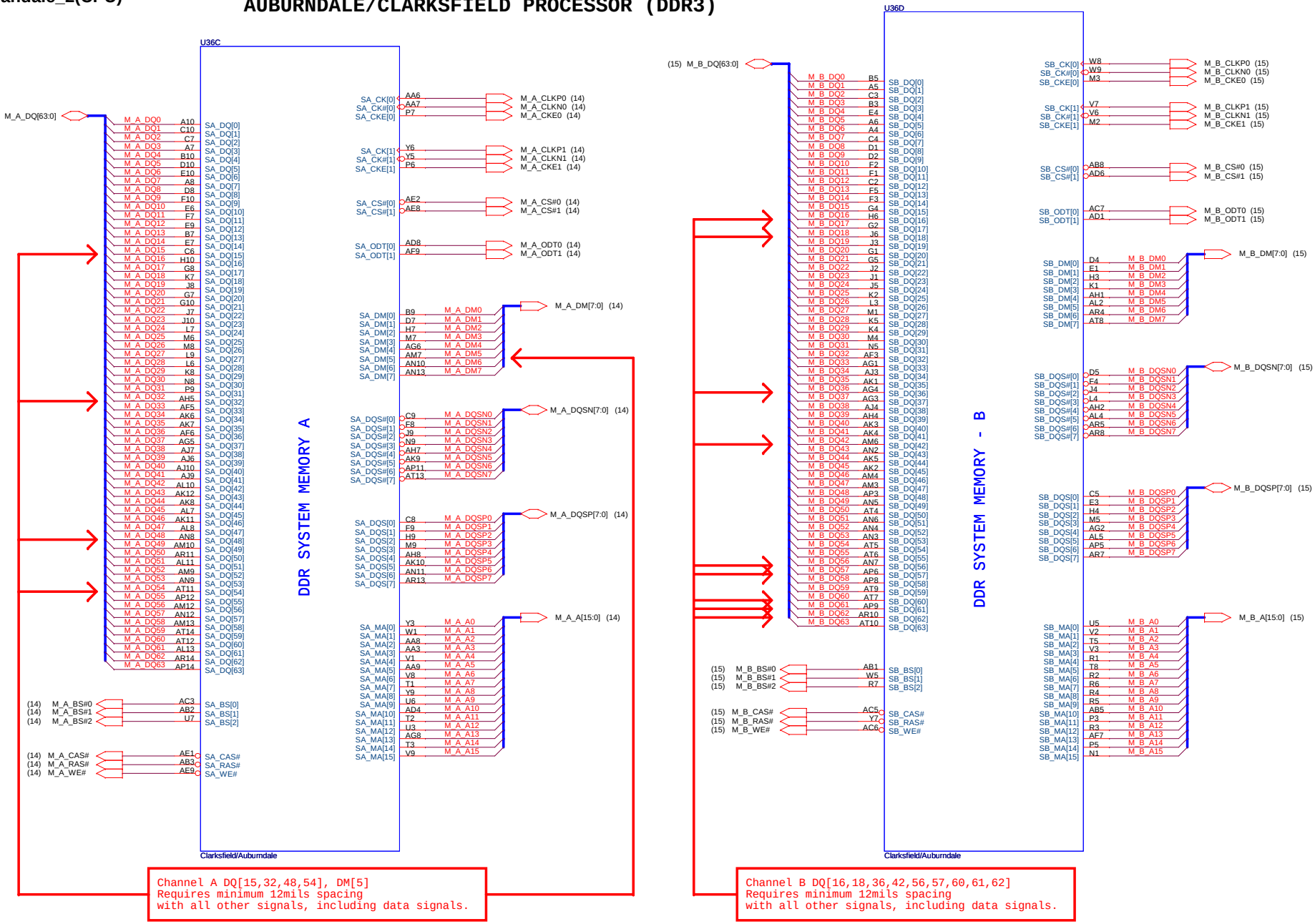
Arrandale_2(CPU)

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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	AUBURNDA 2/4	1A
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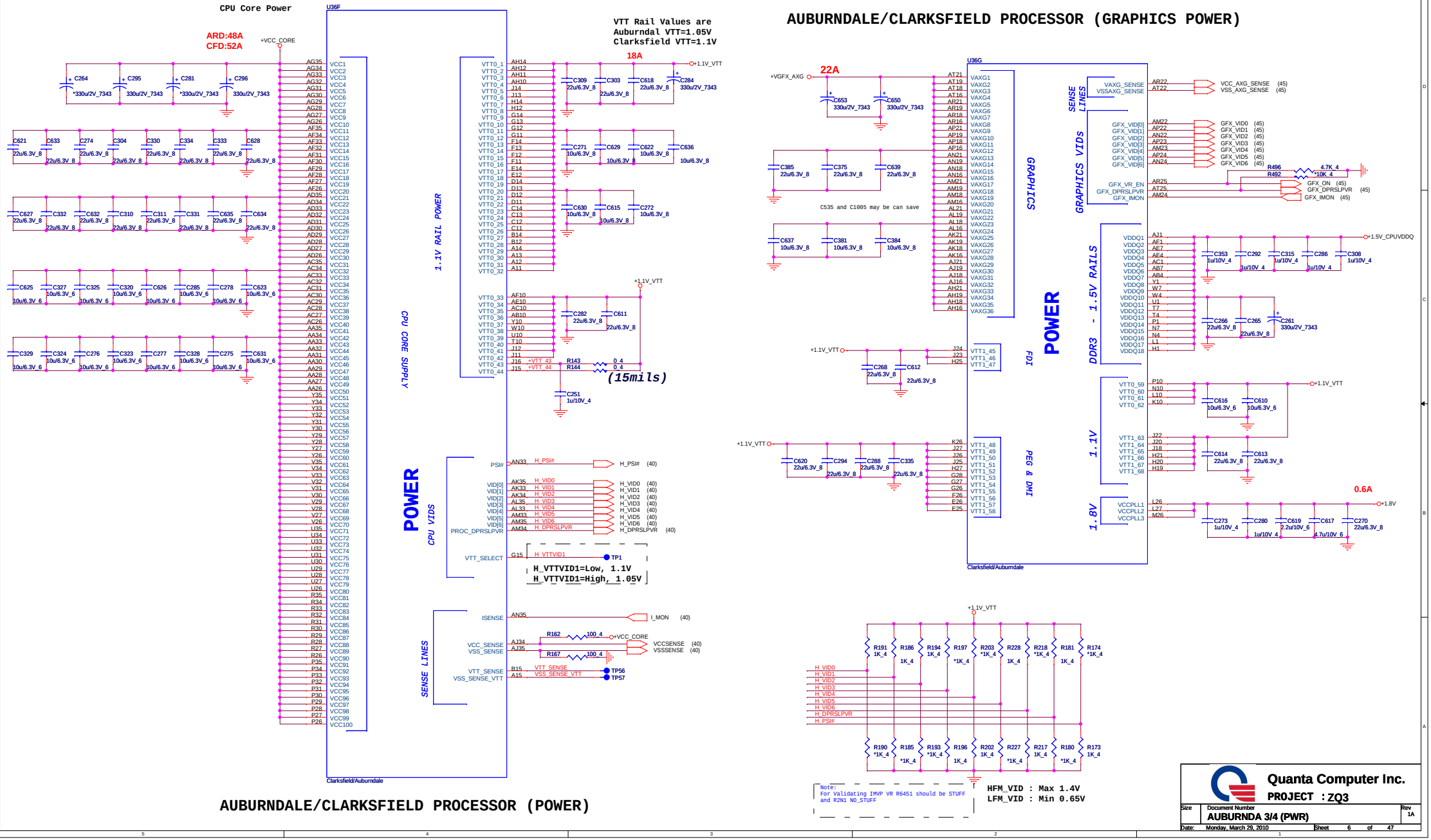
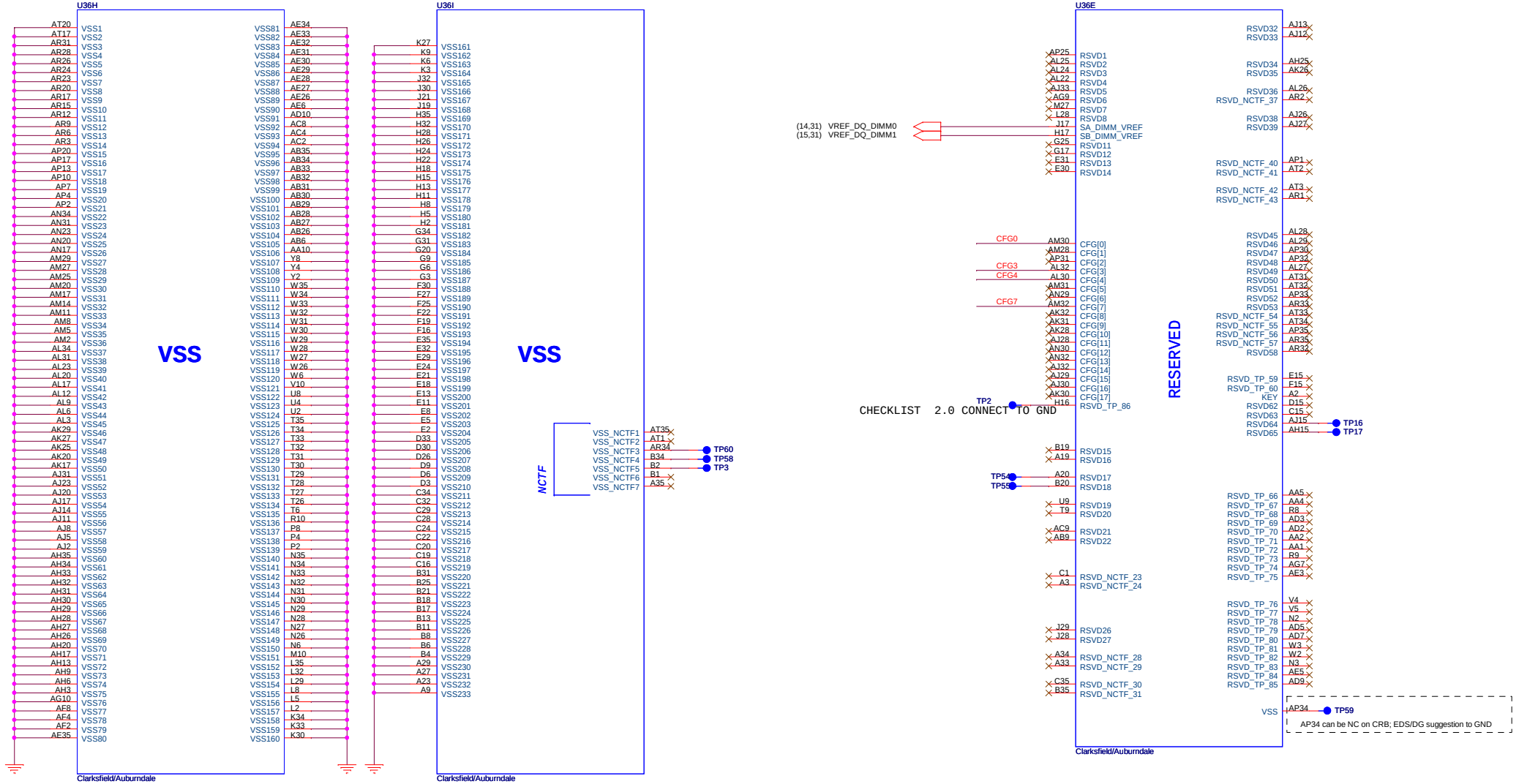
Arrandale_3(CPU)



Arrandale_4(CPU)

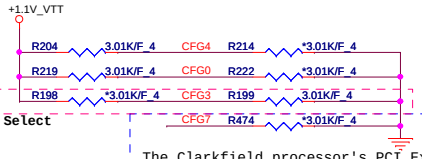
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

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	AUBURNDA 4/4	1A

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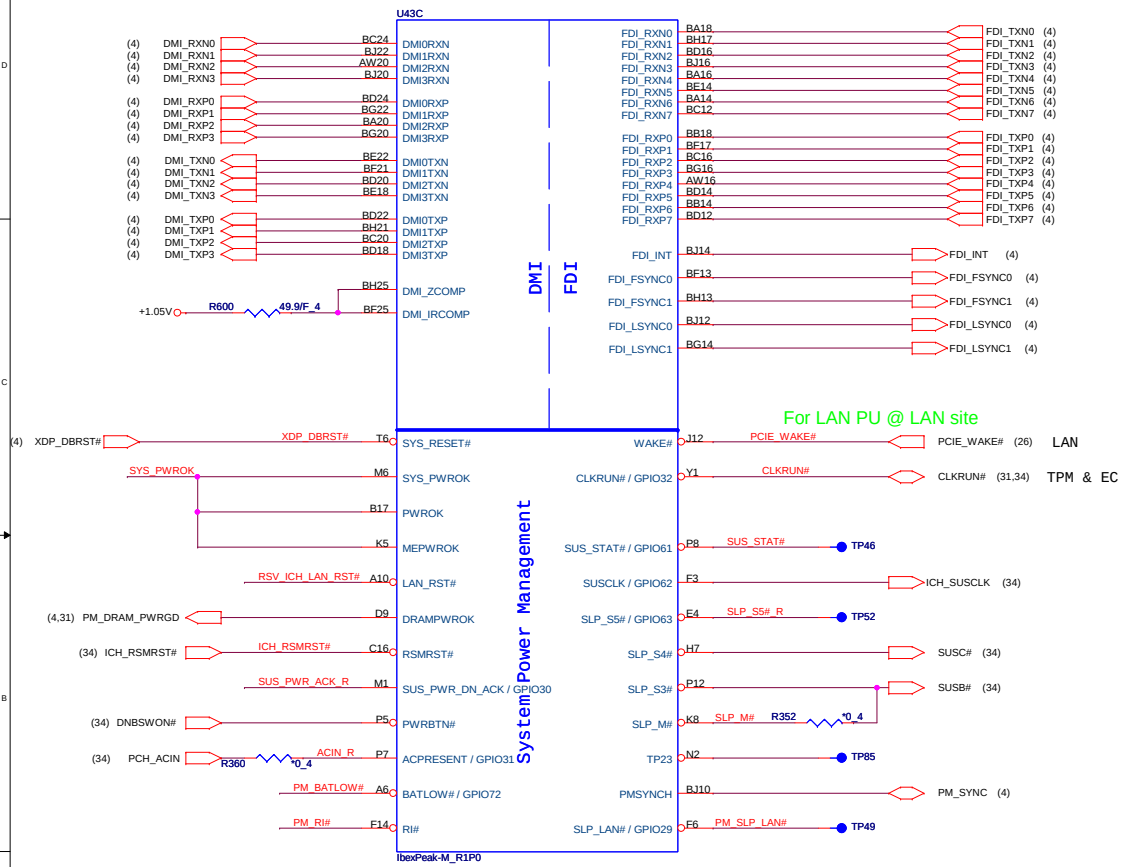
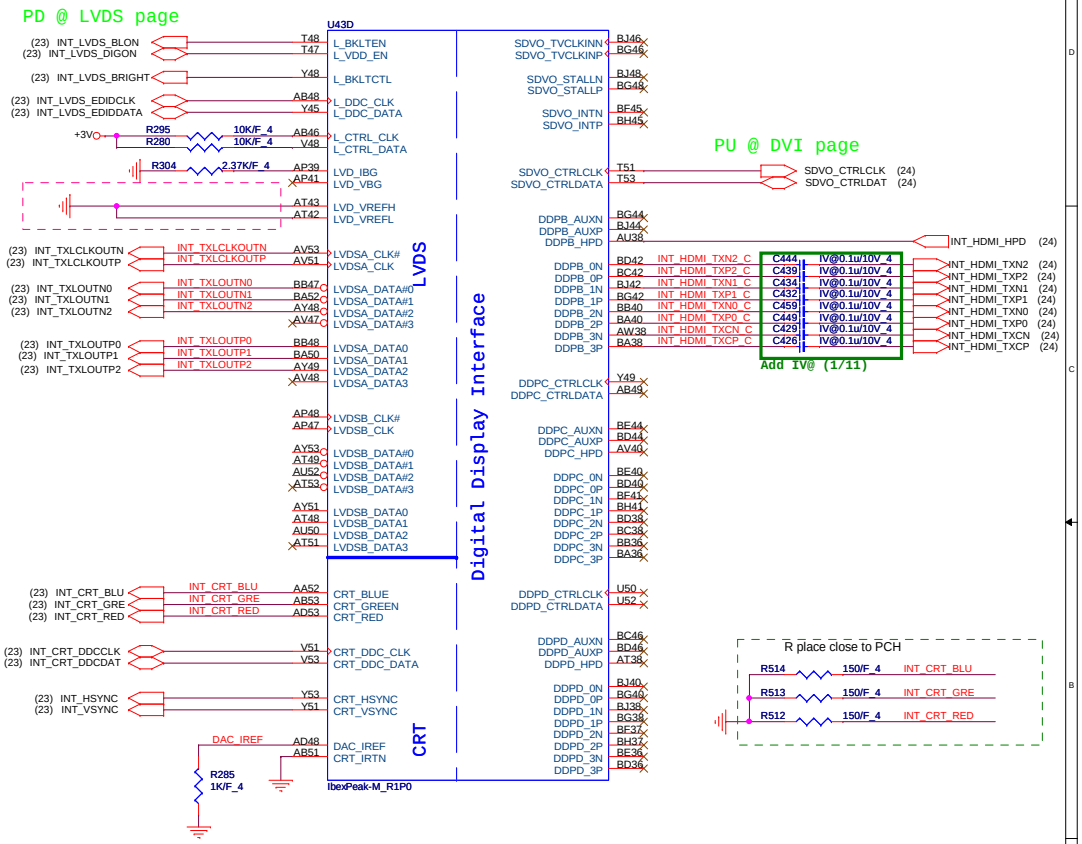
PCH1(CLG)

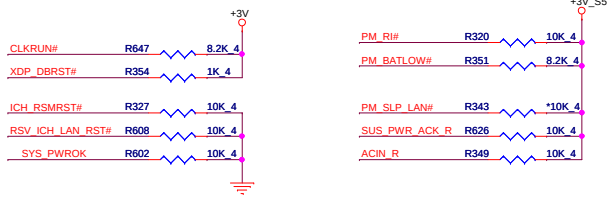
IBEX PEAK-M (DMI,FDI,GPIO)



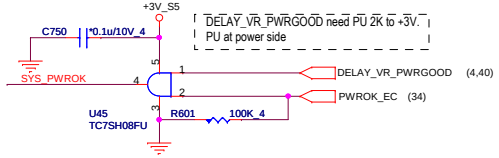
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low(CLG)



System PWR_OK(CLG)



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	IBEX PEAK-M 1/6	1A
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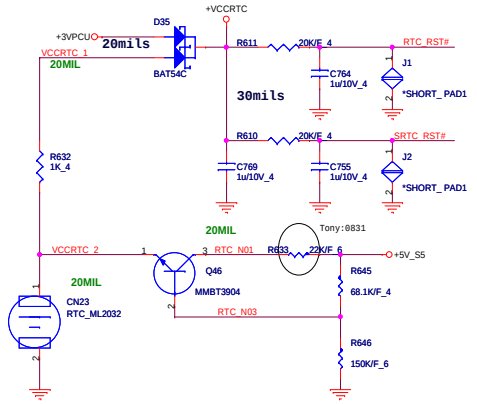
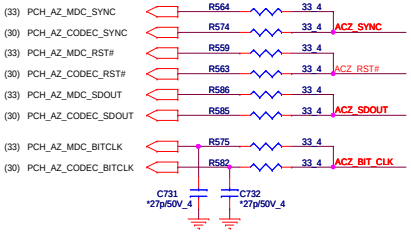
RTC Circuitry(RTC)

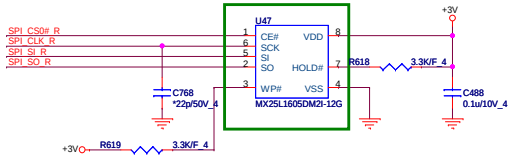


HDA Bus(CLG)

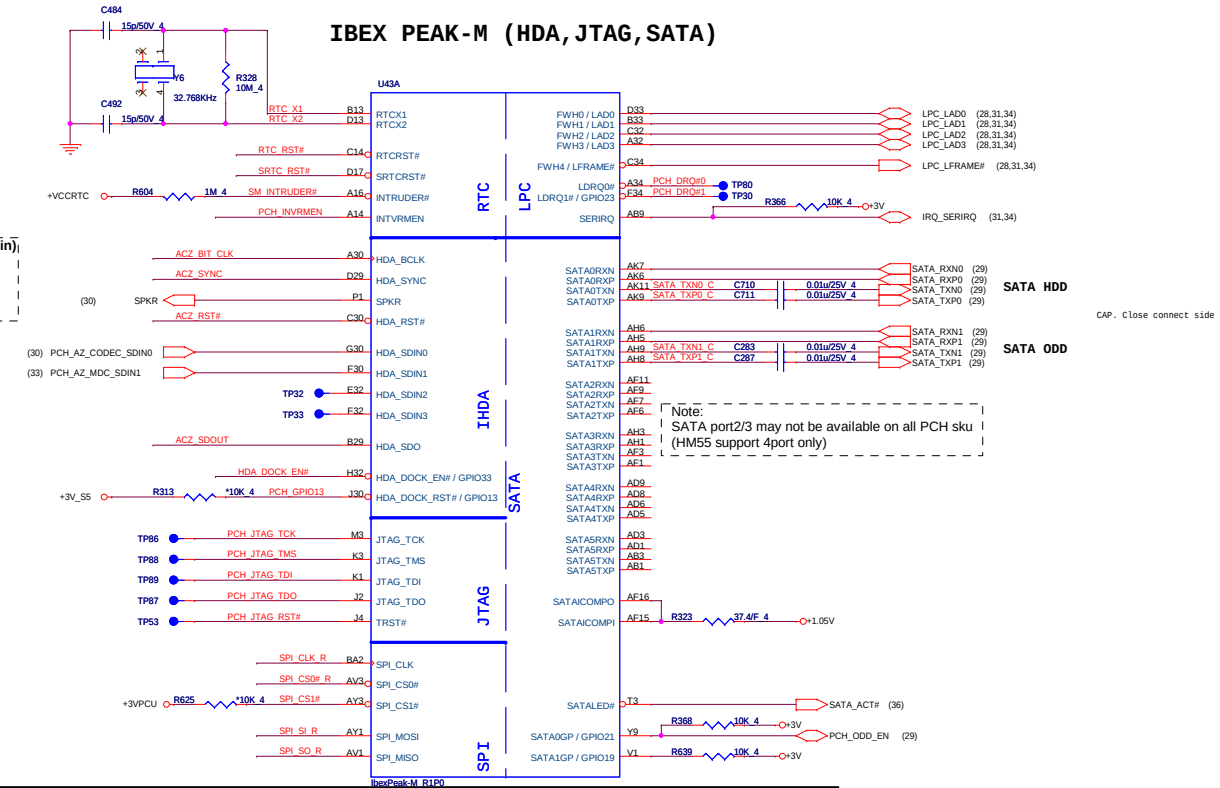


Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI(CLG)



PCH2(CLG)



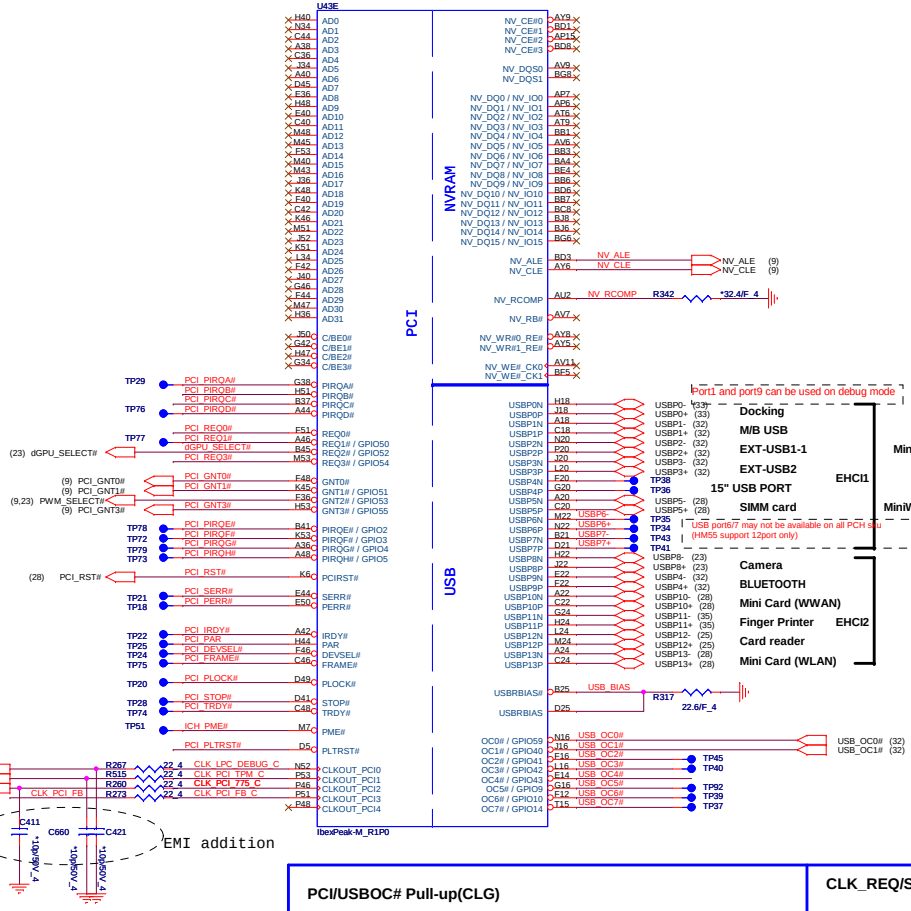
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZY9B note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R642 *10K_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R519 *4.7K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+VCCRTC R606 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / **LPC**	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]** +3V R284 *1K_4 R269 *1K_4 R292 1K_4 R268 1K_4 PCI_GNT0# (10) PCI_GNT1# (10) 1/11 modified
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	R303 *4.7K_4 PWM_SELECT# (10,23)
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R624 *1K_4 NV_ALE NV_ALE (10)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R341 *1K_4 NV_CLE NV_CLE (10)
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R592 *1K_4 R594 *10K_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R623 *8.2K_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R336 10K_4 RSV_GPIO8 (11)
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	R324 *10K_4 RSV_GPIO27 (11)
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 R346 1K_4 CR_WAKE# (11)

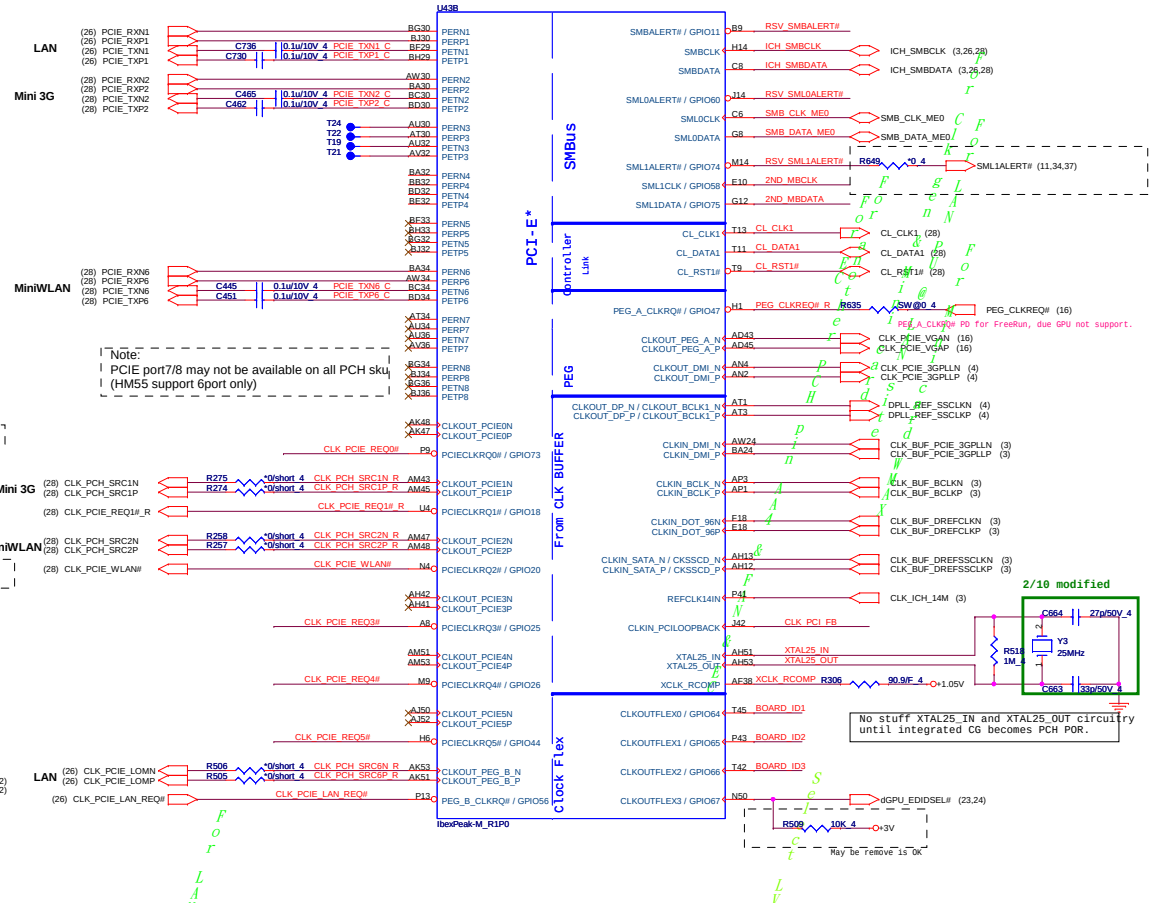
from PCH and to control SW (EC or PCH control Brightness switch)

PCH3(CLG)

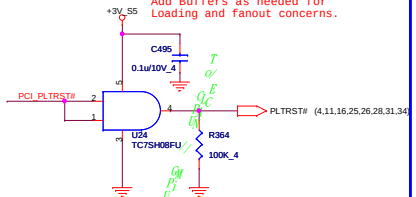
IBEX PEAK-M (PCI,USB,NVRAM)



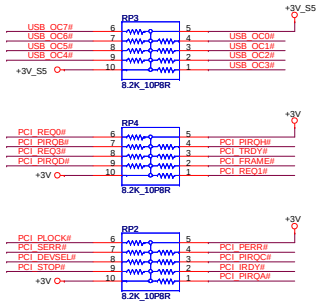
IBEX PEAK-M (PCI-E,SMBUS,CLK)



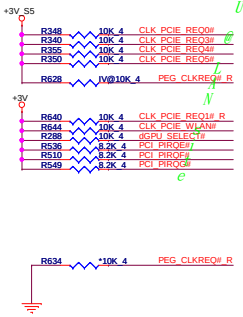
PLTRST#(CLG)



PCI/USBOC# Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)



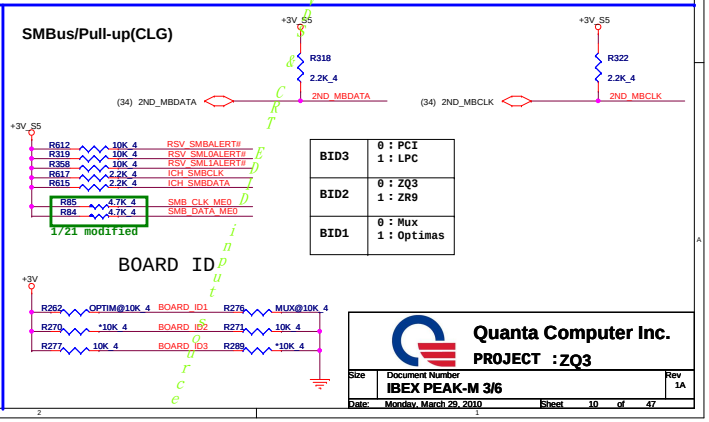
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

SMBus/Pull-up(CLG)



BID3	0 : PCI 1 : LPC
BID2	0 : ZQ3 1 : ZR9
BID1	0 : Mux 1 : Optimas

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	IBEX PEAK-M 3/6	1A
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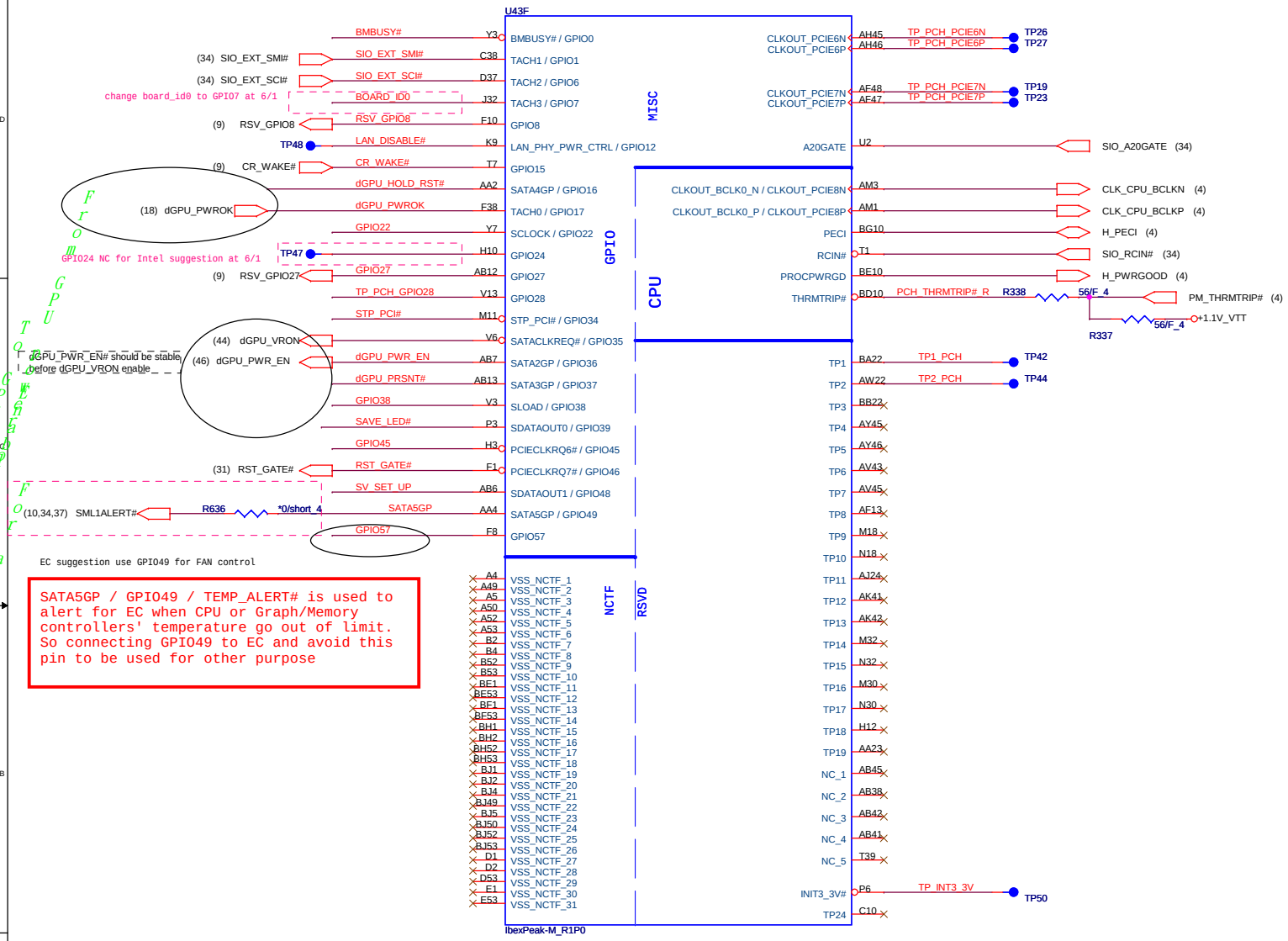
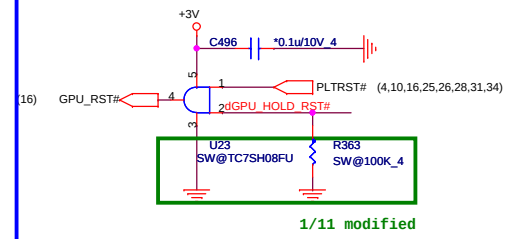
PCH4(CLG)

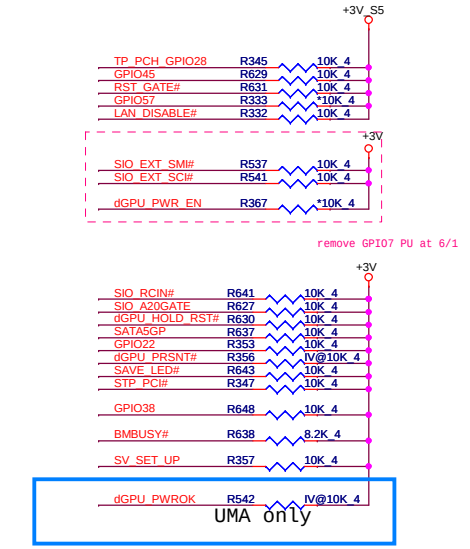
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



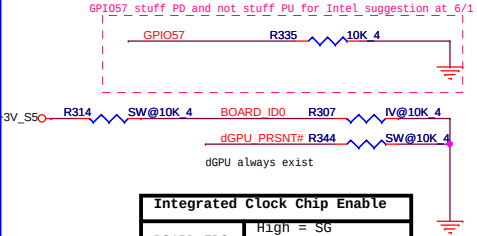
GPU RST#(CLG)



GPIO Pull-up/Pull-down(CLG)



SV_SET_UP	1-X High = Strong (Default)



Integrated Clock Chip Enable	
BOARD_ID0	High = SG Low = UMA
RSV_GPIO8	High = Disable Low = Enable

Quanta Computer Inc.

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	IBEX PEAK-M 4/6	1A
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PCH5(CLG)

IBEX PEAK-M (POWER)

VRM enable by strap pin GPIO27
which supply clean 1.05V for
[VCCACLK,VCCAPLLEXP,VCCFDIPLL,VCCSATAPLL]

HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

B test move 1u cap at check list

B test move 1u cap at check list

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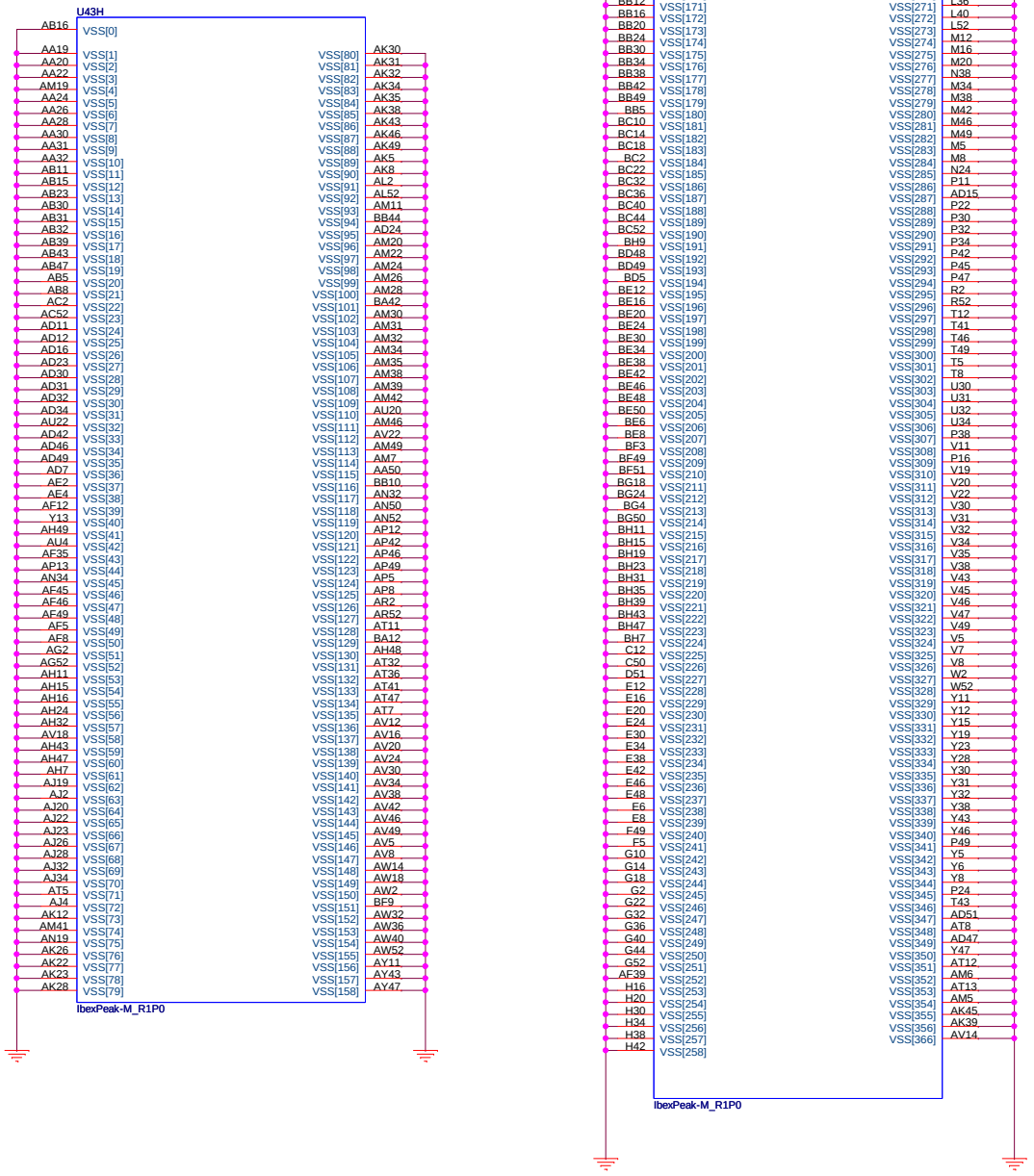
IBEX PEAK-M (GND)



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	IBEX PEAK-M 6/6	1A
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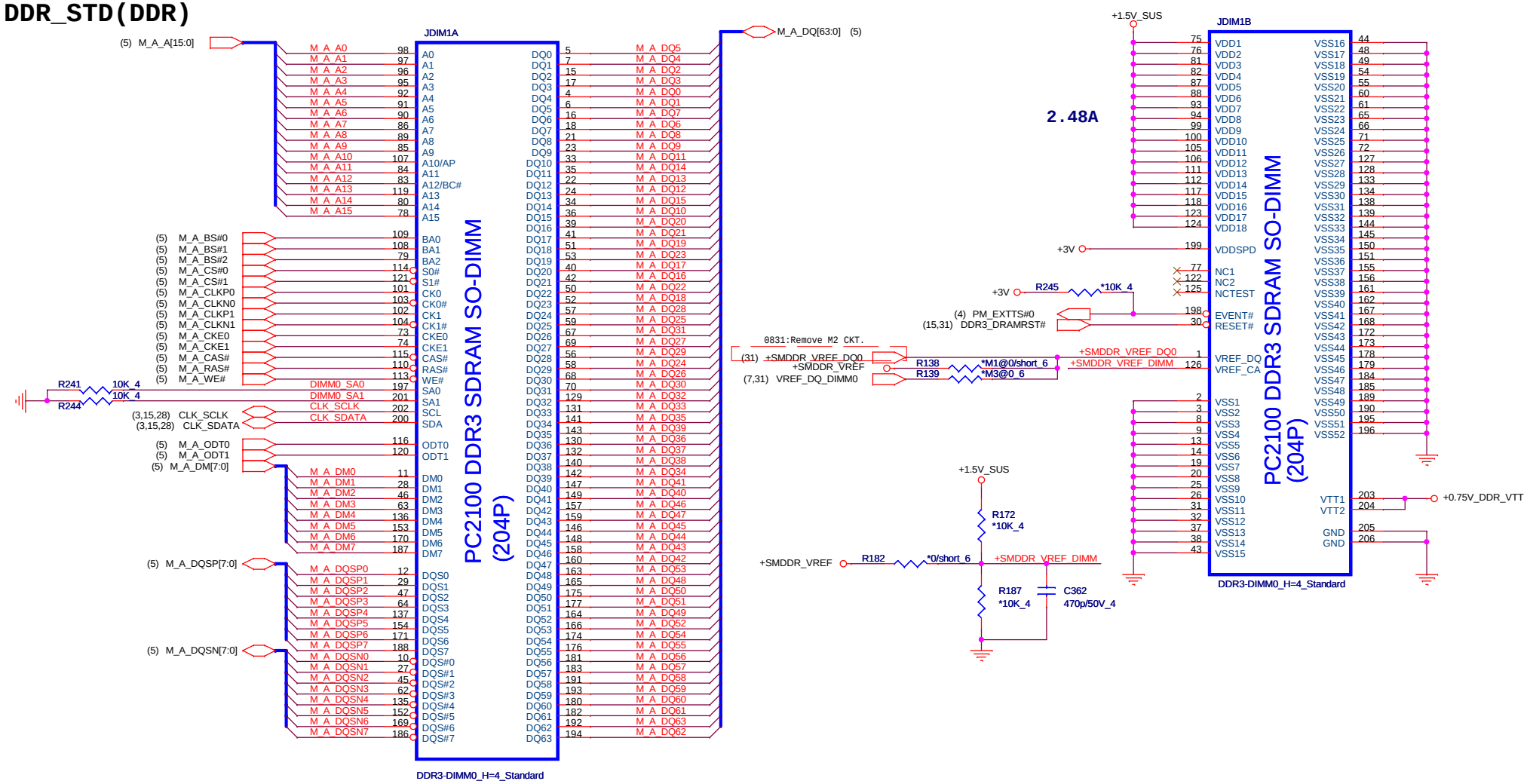
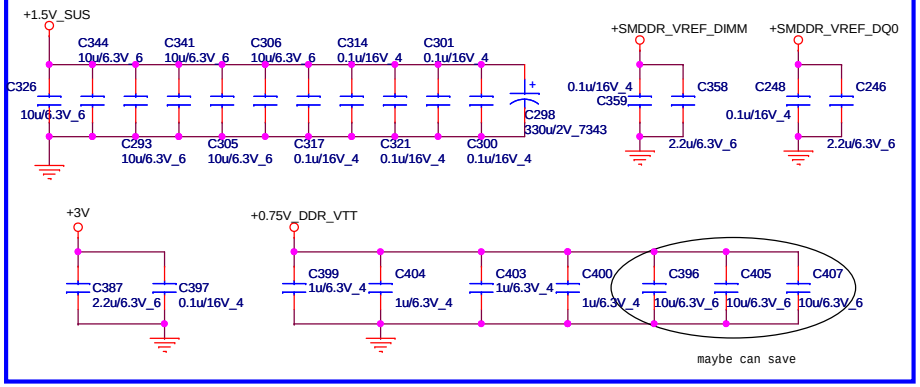
DDR_STD(DDR)

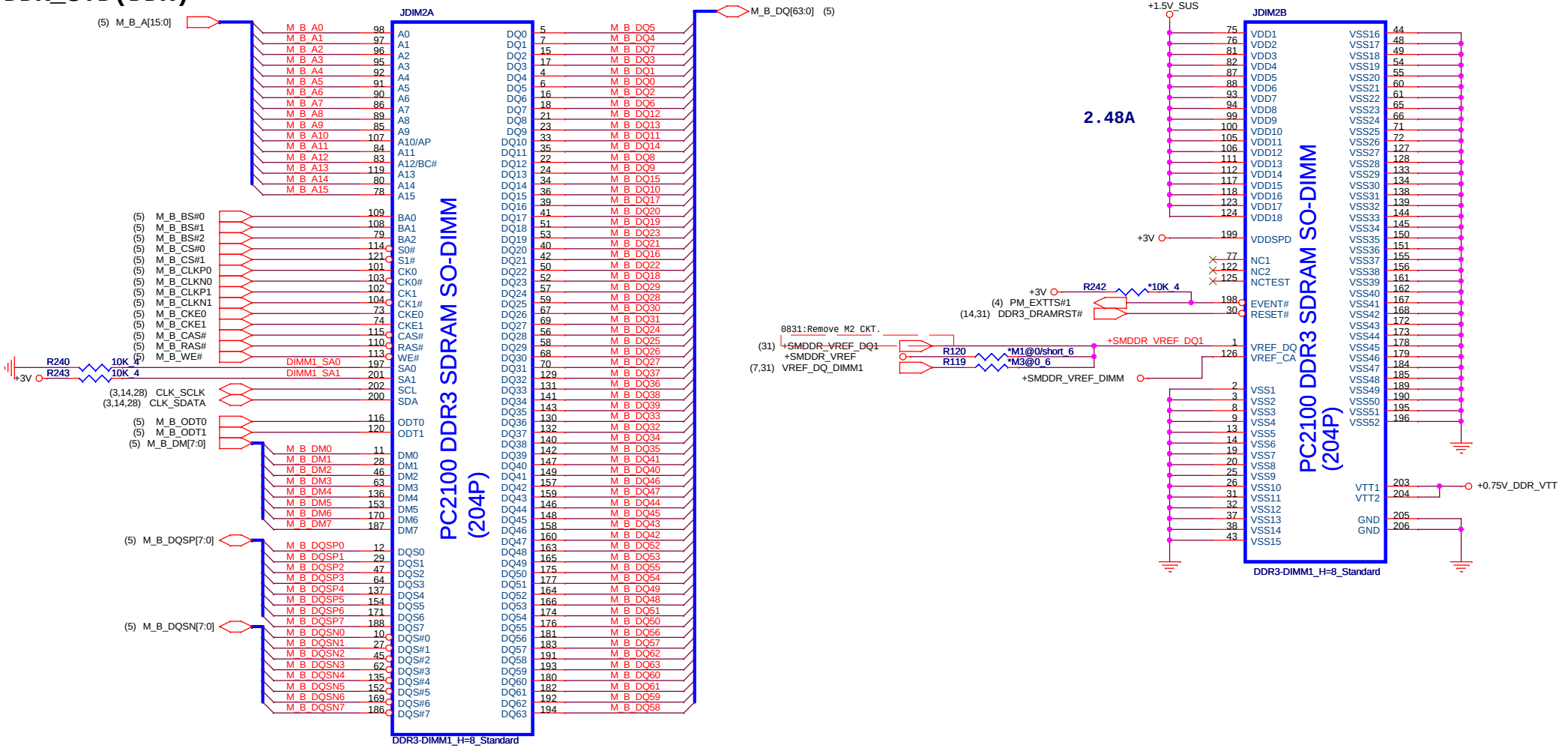


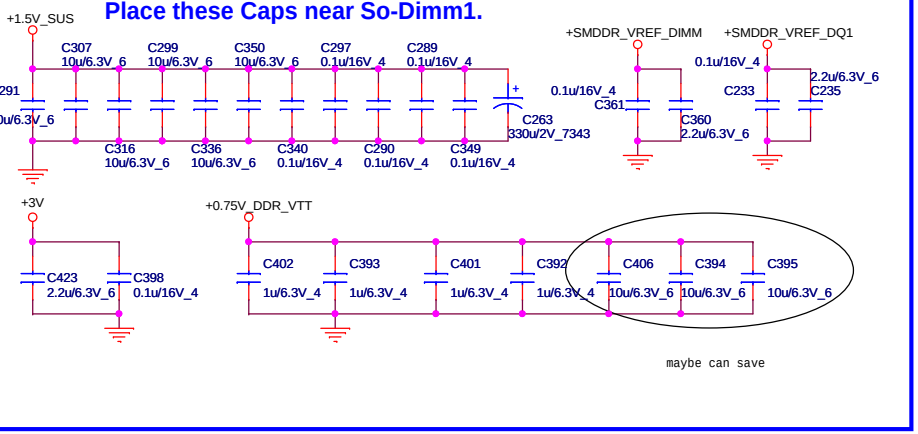
Place these Caps near So-Dimm0.



Quanta Computer Inc.		
PROJECT : ZQ3		
Size	Document Number: DDRIII SO-DIMM-0	Rev: 1A
Date: Monday, March 29, 2010	Sheet 14 of 47	

DDR_STD(DDR)





Quanta Computer Inc.

PROJECT : ZQ3

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date: Monday, March 29, 2010	Sheet 15 of 47	

GPU_1(VGA)

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

N11P GPU : AJ0N11P0T05

N11M GPU : AJ0N11M0T07

N11P_A2 GPU : AJ0N11P0T20

N11M_B1 GPU : AJ0N11M0T22

~ 500mA

1600mA

Near BGA

12~16 mils width 110mA

12~16 mils width

10/20 add

10/20 del C3553,C3554

10/20 Modify to 1uF

U32A COMMON

PCI EXPRESS

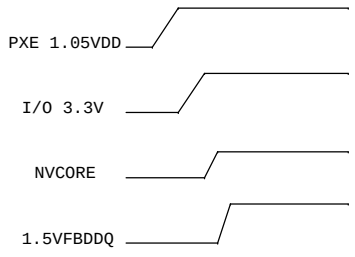
CSP@N11P-GE1-A3

1211 for Nvidia request add transition cap

R450 un-mount for switchable function

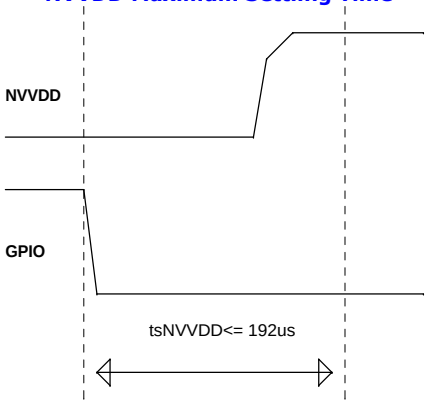
Only for Hybrid

power up sequence

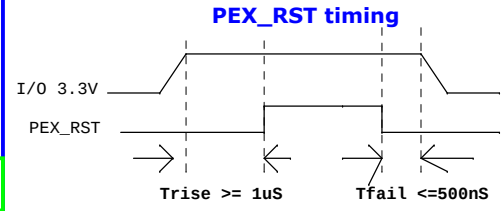


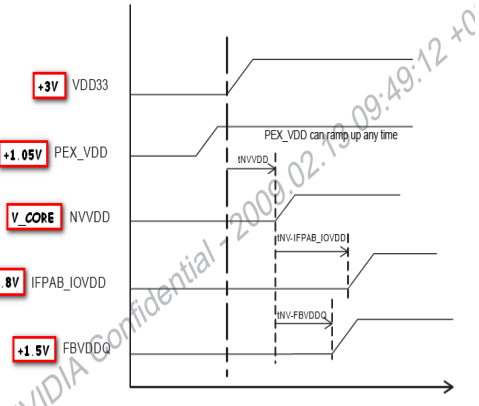
NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



PEX_RST timing





Quanta Computer Inc.	
PROJECT : ZQ3	
Size	Document Number: N11P-GE (PCIE I/F) 1/5 — Rev: 1A
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GPU_2(VGA)

U32B
fcbga973-nvidia-n11p-es-a1
COMMON

U32C
fcbga973-nvidia-n11p-es-a1
COMMON

12/02 modify package for N10

12/02 modify package for N10

12/02 modify package for N10

12/02 modify package for N10

12/02 modify package for N10

(21) VMA_DQ[63..0]
(21) VMA_DM[7..0]
(21) VMA_WDQS[7..0]
(21) VMA_RDQS[7..0]
(22) VMC_DQ[63..0]
(22) VMC_DM[7..0]
(22) VMC_WDQS[7..0]
(22) VMC_RDQS[7..0]

Un-stuff for N11M

Stuff for N11P ,N11S

MEMORY I/F A

MEMORY I/F C

15mils width

15mils width

For Debug only

SW@PBY160808T-301Y-N/2A/30ohm_6

2/16

All need stuff for N10P

N11P-GE1 Stuff 40.2 ohm

N11M-GE1 Stuff 60.2 ohm

CSP@N11P-GE1-A3

CSP@N11P-GE1-A3

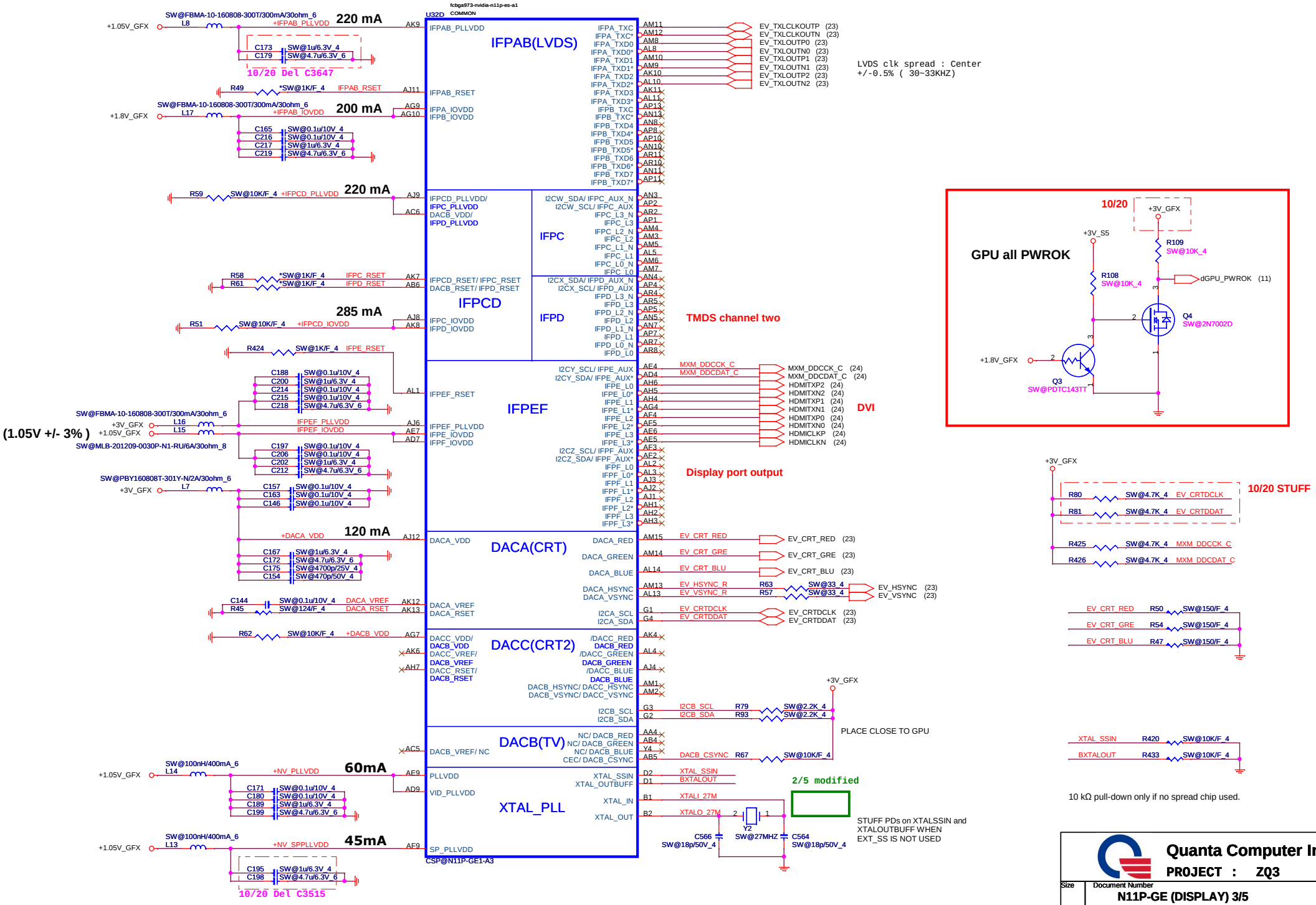
Quanta Computer Inc.

PROJECT : ZQ3

Size	Document Number	Rev
	N11P-GE (MEMORY I/F) 2/5	1A

Date: Monday, March 29, 2010 Sheet 17 of 47

GPU_3(VGA)


fcbga973-nvidia-n11p-es-a1
U32D COMMON
IFPAB(LVDS)
IFPC
IFPD
IFPCD
IFPEF
DACA(CRT)
DACC(CRT2)
DACB(TV)
XTAL_PLL
CSP@N11P-GE1-A3
220 mA
200 mA
220 mA
285 mA
120 mA
60mA
45mA
SW@FBMA-10-160808-300T/300mA/30ohm_6
SW@FBMA-10-160808-300T/300mA/30ohm_8
SW@MLB-201209-0030P-N1-RU/6A/30ohm_8
SW@PBY160808T-301Y-N/2A/30ohm_6
SW@100nH/400mA_6
10/20 Del C3647
10/20 Del C3515
(1.05V +/- 3%)
LVDS clk spread : Center
+/-0.5% (30~33KHZ)
TMDS channel two
DVI
Display port output
PLACE CLOSE TO GPU
2/5 modified
STUFF PDs on XTALSSIN and
XTALOUTBUFF WHEN
EXT_SS IS NOT USED
GPU all PWROK
10/20
10/20 STUFF
10 kΩ pull-down only if no spread chip used.
Quanta Computer Inc.
PROJECT : ZQ3
N11P-GE (DISPLAY) 3/5
Monday, March 29, 2010
Sheet 18 of 47

PIN STRAPS(VGA)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

(Ra)

AKD58GGT^01
AKD5LZGTW00
AKD5LGGT502

(Ra)

Default: Hynix VRAM

Hynix =15K pull down(64Mx16)
Samsung =20k pull down(64Mx16)

CHIP	ROM_SCLK	STRAP2	PCI_DEVID
N11M-GE1	PU 15K	PD 30K	0x0A75
N11P-GE1	PD 15K	PU 10K	0x0A29

Logical Strap Bit Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

HDCP ROM (VGA)

Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

HDCP ROM reserve , Due to N11x had support internal HDCP function.

A5 N.C due to N11X HAD function is through PCI-E interface

VGA Thermal(VGA)

Quanta Computer Inc.
PROJECT : ZQ3
Size | Document Number: N11P-GE (GPIO&STRAPS) 4/5 | Rev 1A
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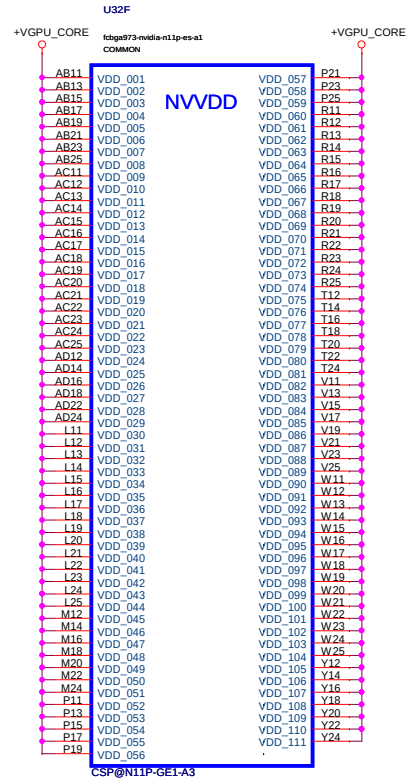
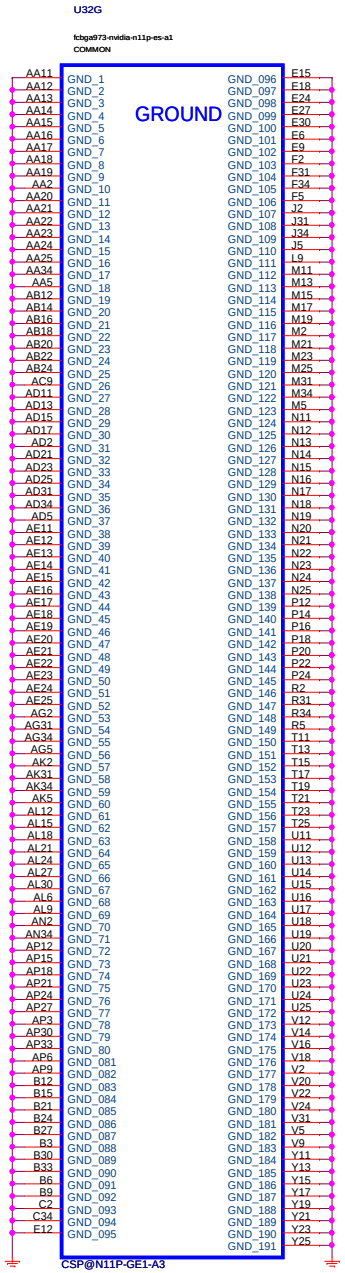
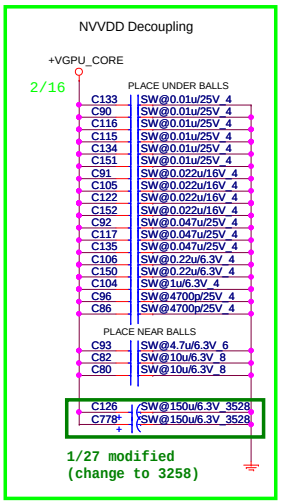
GPU_4(VGA)

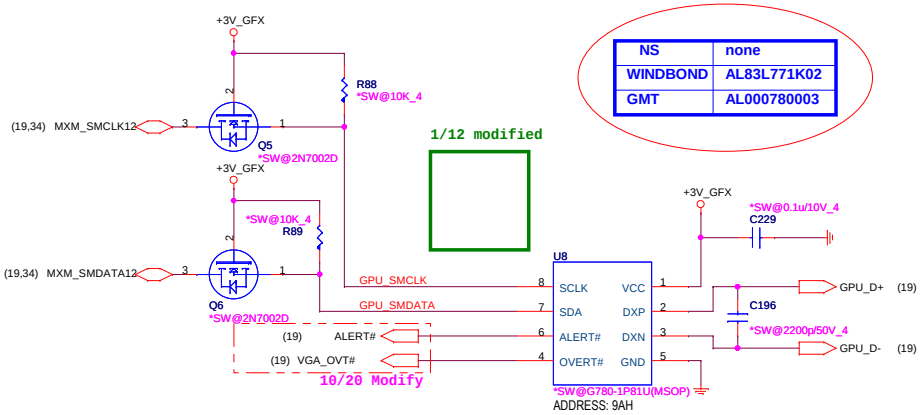




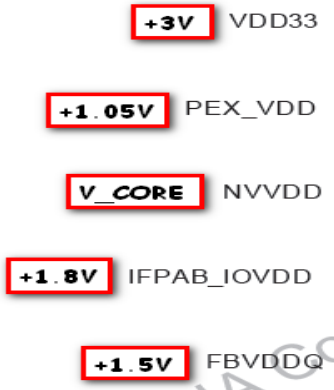


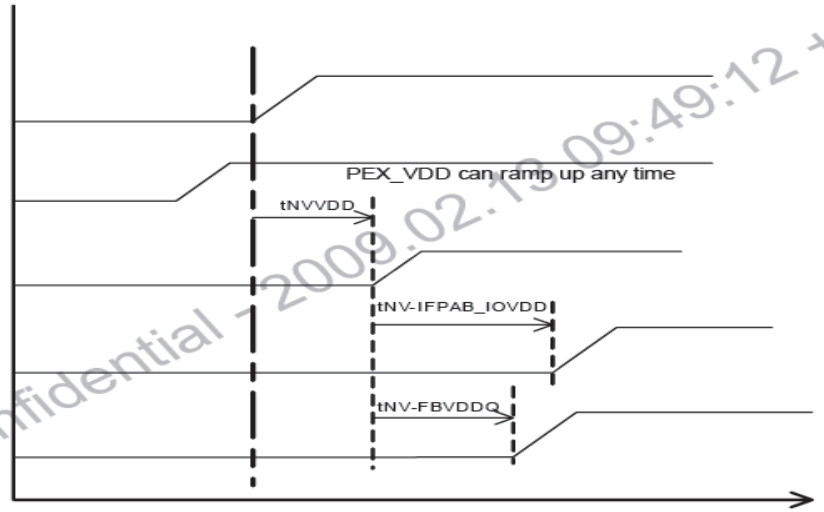
12/9 ADD TWO 4700PF

Thermal Sensor(VGA)



NS	none
WINDBOND	AL83L771K02
GMT	AL000780003





Quanta Computer Inc.
PROJECT : ZQ3

Size	Document Number	Rev
	N11P-GE (POWER & GND&THM) 5/5	1A

Date: Monday, March 29, 2010 Sheet 20 of 47

VRAM_A(VGA)

CHANNEL A: 256MB/512MB DDR3

(17) VMA_DQ[63..0]
(17) VMA_DM[7..0]
(17) VMA_WDQS[7..0]
(17) VMA_RDQS[7..0]

(17,22,46) +1.5V_GFX

U4 / U30 / U29 / U3 — 96-BALL SDRAM DDR3 — CSP@VRAM_DDR3

Should be 240 Ohms +-1%

R24 SW@243/F_4
R394 SW@243/F_4
R403 SW@243/F_4
R17 SW@243/F_4

Samsung 1Gb : AKD5LGGT506
Hynix 1Gb : AKD5LZGTW04

R398 SW@243/F_4
R21 SW@243/F_4

R397 SW@1.33K/F_4
R23 SW@1.33K/F_4
R22 SW@1.33K/F_4
R396 SW@1.33K/F_4

R393 SW@1.33K/F_4
R20 SW@1.33K/F_4
R18 SW@1.33K/F_4
R392 SW@1.33K/F_4

C526 SW@0.1u/10V_4
C29 SW@0.1u/10V_4
C20 SW@0.1u/10V_4
C516 SW@0.1u/10V_4

12/9 NV recommend 0.1uf x 5, 1uf x 4 per DDR3

DEL C3627,C3684,C3681,C3662 ,C3678,C3692
C3690,C3695,C3685 FOR NV suggestion

10/21 Add for NV Request

10/21 Add for NV Request

C514 SW@4.7u/6.3V_6
C26 SW@0.1u/10V_4
C519 SW@0.1u/10V_4
C545 SW@0.1u/10V_4
C28 SW@0.1u/10V_4

C520 SW@0.1u/10V_4
C521 SW@0.1u/10V_4
C548 SW@0.1u/10V_4
C517 SW@0.1u/10V_4
C549 SW@0.1u/10V_4
C546 SW@0.1u/10V_4
C37 SW@0.1u/10V_4
C527 SW@0.1u/10V_4

C515 SW@0.1u/10V_4
C518 SW@0.1u/10V_4
C550 SW@0.1u/10V_4
C523 SW@0.1u/10V_4
C25 SW@0.1u/10V_4
C40 SW@0.1u/10V_4
C35 SW@0.1u/10V_4
C522 SW@0.1u/10V_4

C24 SW@1u/6.3V_4
C31 SW@1u/6.3V_4
C38 SW@1u/6.3V_4
C27 SW@1u/6.3V_4
C19 SW@1u/6.3V_4
C39 SW@1u/6.3V_4
C547 SW@1u/6.3V_4
C17 SW@1u/6.3V_4

C524 SW@1u/6.3V_4
C16 SW@1u/6.3V_4
C18 SW@1u/6.3V_4
C77 SW@1u/6.3V_4
C22 SW@1u/6.3V_4
C41 SW@1u/6.3V_4
C23 SW@1u/6.3V_4
C21 SW@1u/6.3V_4

Quanta Computer Inc.
PROJECT : ZQ3

Size	Document Number	Rev
	N11P-GE VRAM-1(DDR3 BGA96)	1A
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VRAM_C(VGA)

CHANNEL B: 256MB/512MB DDR3

(17) VMC_DQ[63..0]
(17) VMC_DM[7..0]
(17) VMC_WDQS[7..0]
(17) VMC_RDQS[7..0]

(17,21,46) +1.5V_GFX

U33 — 96-BALL SDRAM DDR3 — SNP@CSP@VRAM _DDR3

U7 — 96-BALL SDRAM DDR3 — SNP@CSP@VRAM _DDR3

U5 — 96-BALL SDRAM DDR3 — SNP@CSP@VRAM _DDR3

U31 — 96-BALL SDRAM DDR3 — SNP@CSP@VRAM _DDR3

Should be 240 Ohms +-1%

R413 SNP@243/F_4
R48 SNP@243/F_4
R37 SNP@243/F_4
R409 SNP@243/F_4

R414 SNP@243/F_4
R411 SNP@1.33K/F_4
R412 SNP@1.33K/F_4
C558 SNP@0.1u/10V_4
R42 SNP@1.33K/F_4
R46 SNP@1.33K/F_4
C153 SNP@0.1u/10V_4
R31 SNP@243/F_4
R405 SNP@1.33K/F_4
R406 SNP@1.33K/F_4
C555 SNP@0.1u/10V_4
R27 SNP@1.33K/F_4
R29 SNP@1.33K/F_4
C45 SNP@0.1u/10V_4

12/9 NV recommend 0.1uf x 5, 1uf x 4 per DDR3
DEL C3585,C3637,C3653,C3655,C3665 FOR NV recommend

10/21 Add for NV Request

10/21 Add for NV Request

+1.5V_GFX
C537 SNP@4.7u/6.3V_6
C32 SNP@0.1u/10V_4
C46 SNP@0.1u/10V_4
C557 SNP@0.1u/10V_4
C554 SNP@0.1u/10V_4

C544 SNP@0.1u/10V_4
C561 SNP@0.1u/10V_4
C541 SNP@0.1u/10V_4
C36 SNP@0.1u/10V_4
C553 SNP@0.1u/10V_4
C540 SNP@0.1u/10V_4
C107 SNP@0.1u/10V_4
C140 SNP@0.1u/10V_4

C543 SNP@0.1u/10V_4
C132 SNP@0.1u/10V_4
C169 SNP@0.1u/10V_4
C556 SNP@0.1u/10V_4
C34 SNP@0.1u/10V_4
C539 SNP@0.1u/10V_4
C542 SNP@0.1u/10V_4
C538 SNP@0.1u/10V_4

C69 SNP@1u/6.3V_4
C158 SNP@1u/6.3V_4
C51 SNP@1u/6.3V_4
C525 SNP@1u/6.3V_4
C166 SNP@1u/6.3V_4
C164 SNP@1u/6.3V_4
C128 SNP@1u/6.3V_4
C33 SNP@1u/6.3V_4

C552 SNP@1u/6.3V_4
C97 SNP@1u/6.3V_4
C42 SNP@1u/6.3V_4
C63 SNP@1u/6.3V_4
C551 SNP@1u/6.3V_4
C30 SNP@1u/6.3V_4
C60 SNP@1u/6.3V_4
C112 SNP@1u/6.3V_4

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Size	Document Number	Rev
	N11P-GE VRAM-2(DDR3 BGA96)	1A
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CRT Switch(CRT)

IV@

SW@

S	Yn
0	EV
1	IV

dGPU_SELECT# dGPU_EDIDSEL#	Output
L	EV_LVDS/CRT
H	INT_LVDS/CRT

U12 SW@SN74CBT3257CPWR

U10 SW@SN74CBT3257CPWR

3.3V or 5V level?

UMA only

10/20 Del

10/20 Modify

U9 SW@SN74CBT3257CPWR

10/16

1/22 add for EMI

CRT SWITCH (DOK)

U35 SN74CBT3257CPWR

(CRT)

1/27 change R443 to fuse

2/03 modify footprint

CN14 CRT

U15 CM2009-02QR

LVDS Switch (LDS)

S	Yn
0	EV
1	IV

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

U13 SW@TS3DV421DGVR

10/16

10/16

10/16

UMA only

For EMI (12/22)

U2 SW@74LVC1G3157GW

10/18

1/22 add for EMI

LVDS

CN1 LVD-A305YG+

0.8A

1/22 add for EMI

CAMERA Module(CCD)

CCD&MIC CONN

EMI addition

For EMI. (3/26)

RFCMF1632100M3T/200mA/90ohm

LCD Power(LDS)

10/20 Modify

U26 AAT4280-4

10/16

U28 *SW@NL17SZ32DFT2G

Backlight Control (LDS)

10/20 Modify

LID591#,EC intrnal PU

10/16

10/16

U27 *SW@NL17SZ32DFT2G

Quanta Computer Inc.

PROJECT : ZQ3

Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A

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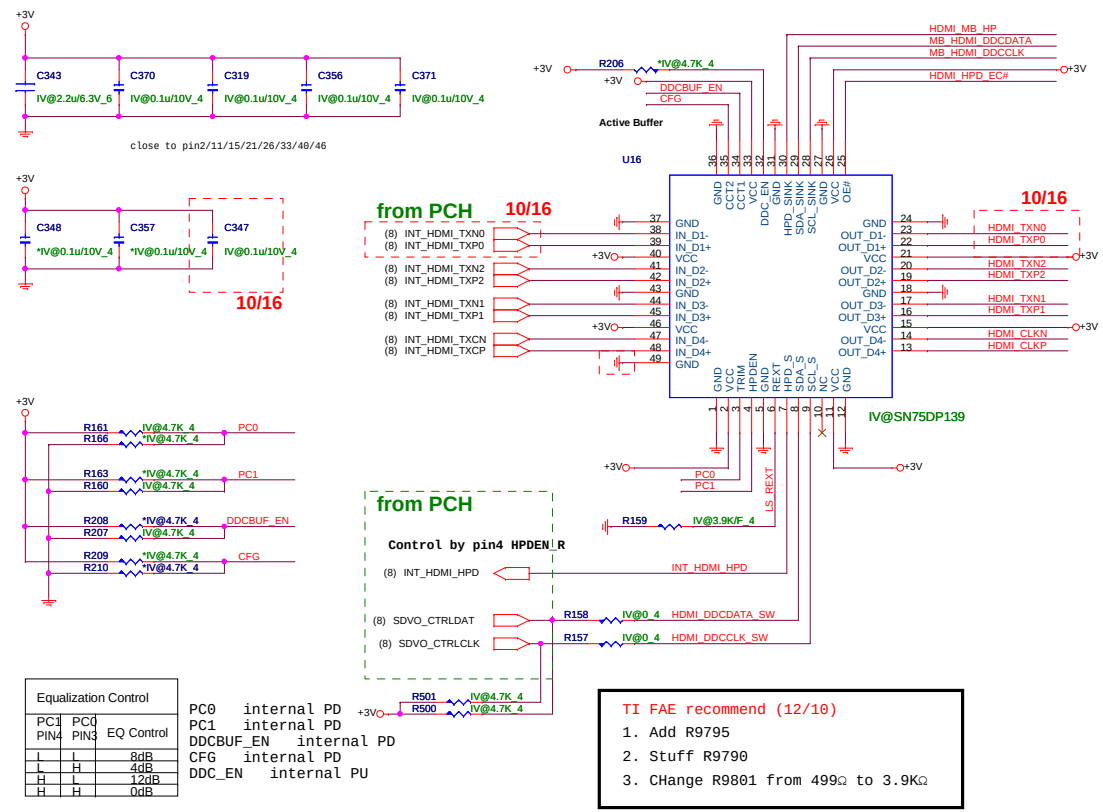
I@ HDMI LEVEL SHIFTER(DOK)

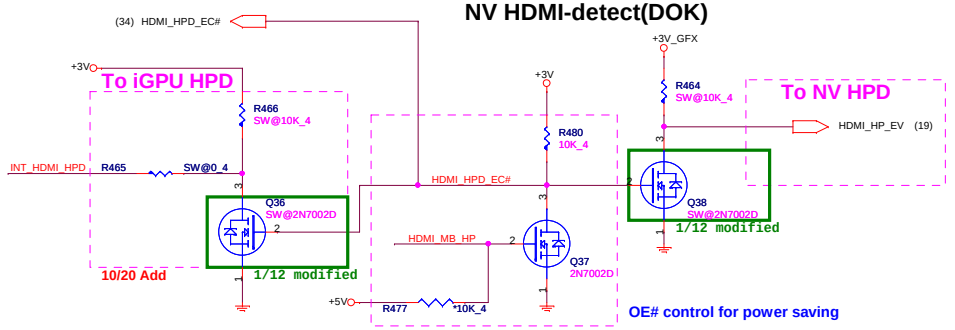


Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

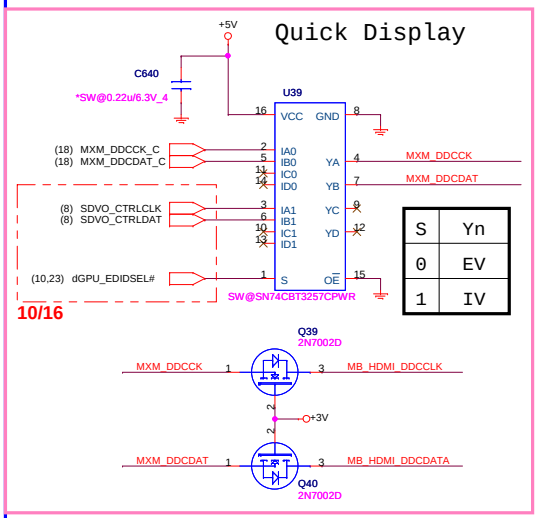
PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

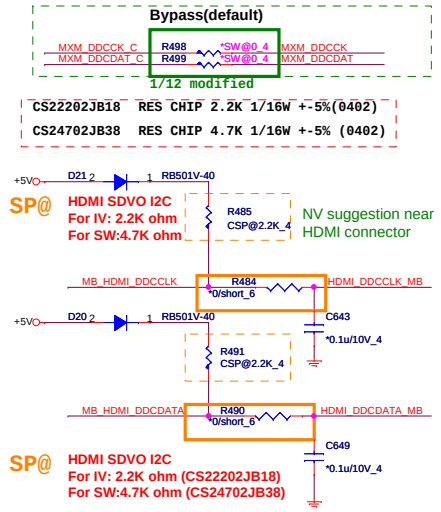
TI FAE recommend (12/10)
1. Add R9795
2. Stuff R9790
3. CHange R9801 from 499Ω to 3.9KΩ

NV HDMI-detect(DOK)

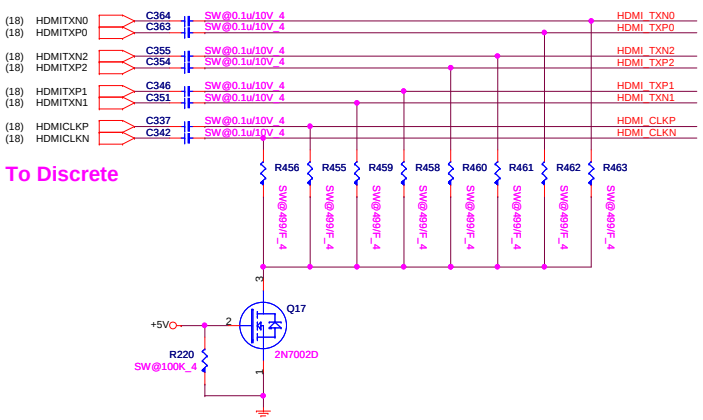


SDVO I2C Control(DOK)

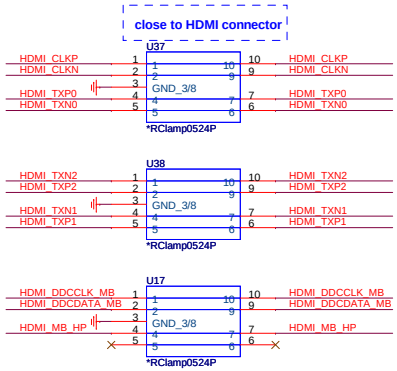


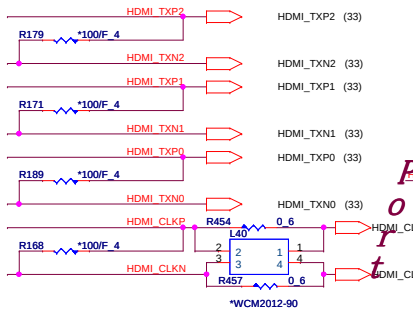


Switchable Graphic HDMI source(DOK)



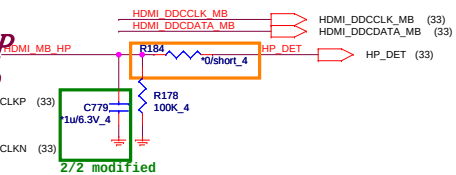
ESD Protect(DOK)





IV@
SW@
SP@

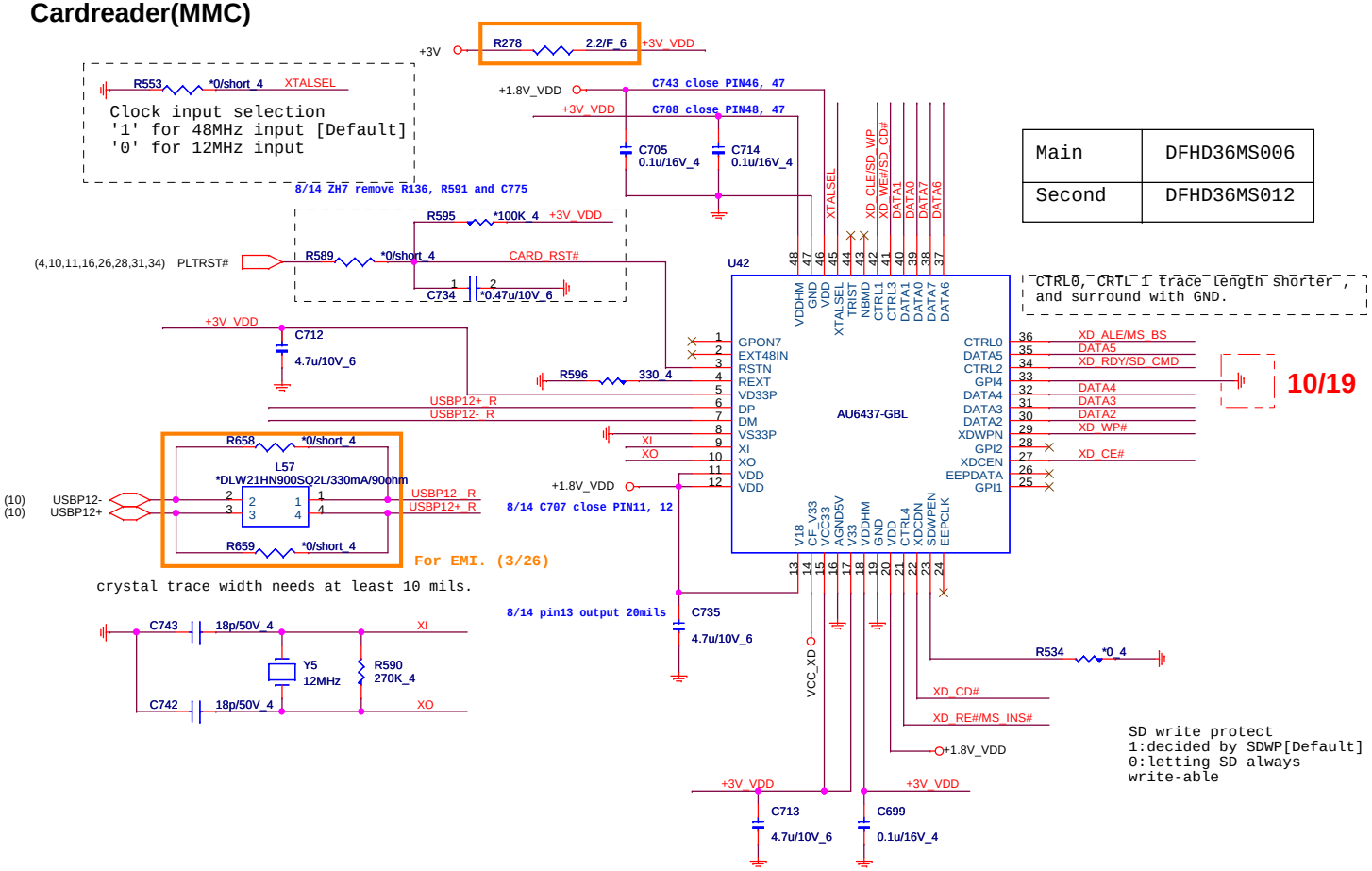
TO Port



Replicate

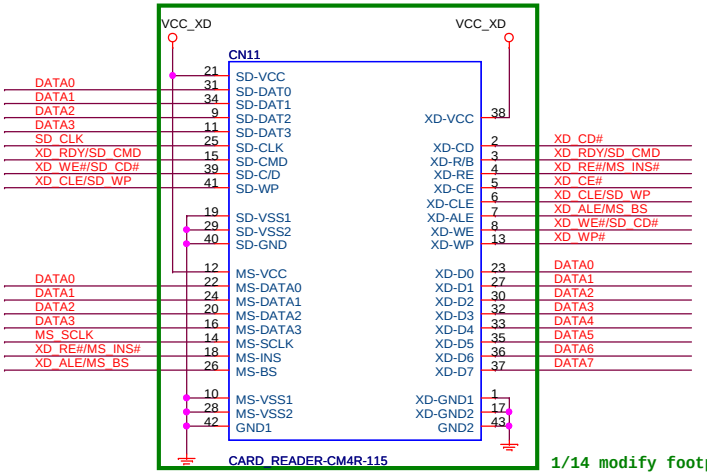
Quanta Computer Inc.		
PROJECT : ZQ3		
Size	Document Number	Rev
	DVI (PS8101)	1A
Date: Monday, March 29, 2010	Sheet 24 of 47	

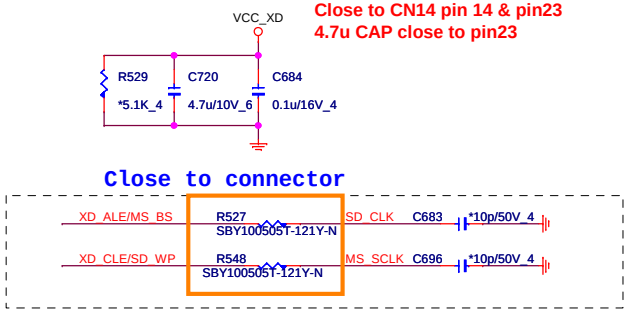
Cardreader(MMC)



Main	DFHD36MS006
Second	DFHD36MS012

4 IN 1 CARD READER (MMC)





Quanta Computer Inc.
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Size	Document Number	Rev
	AU6437 CardReader	1A
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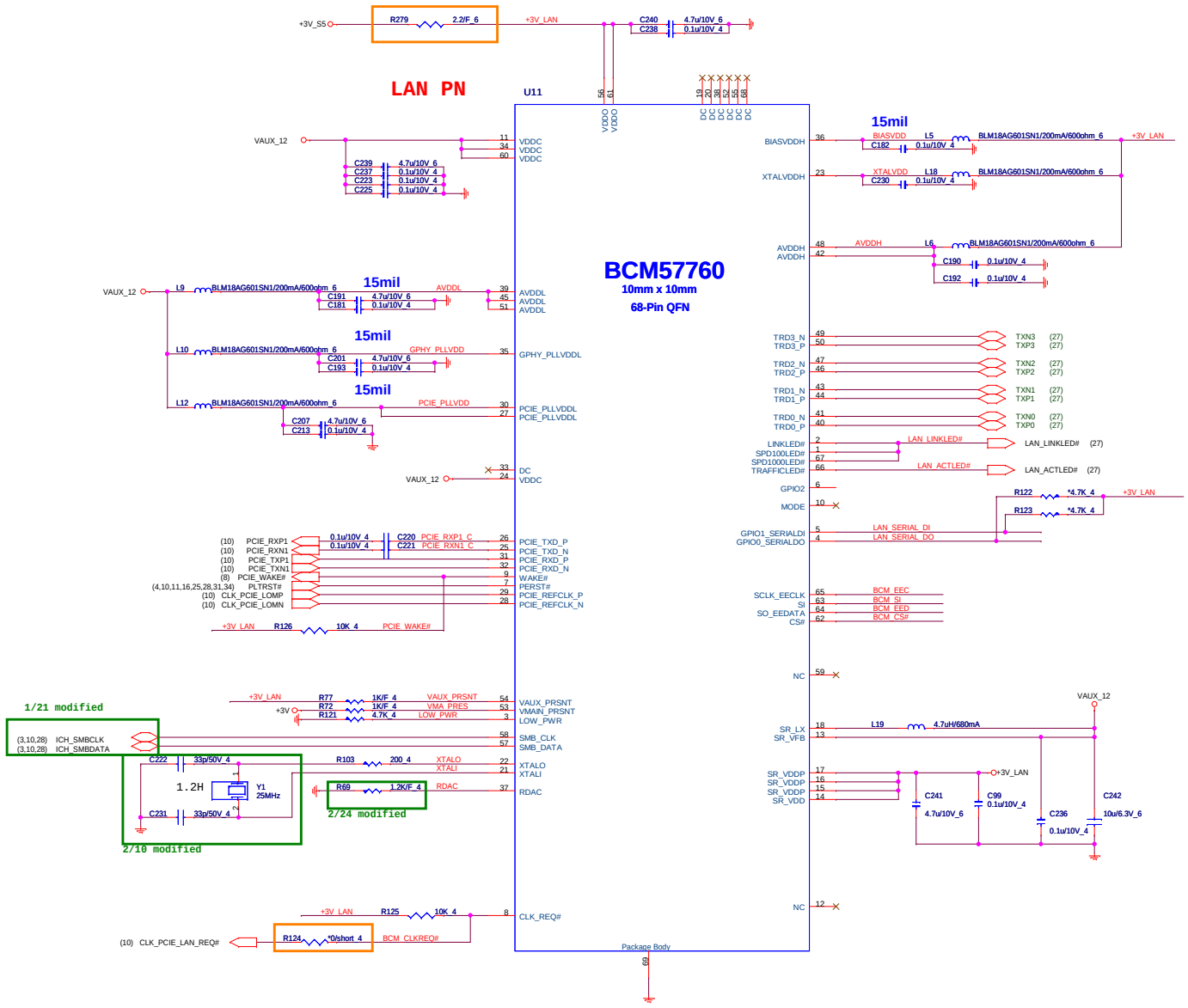
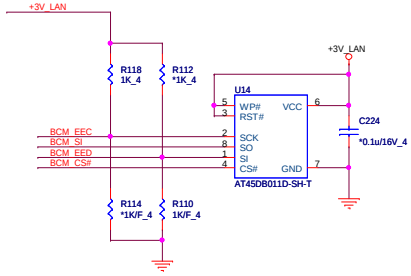
Giga-LAN BCM57760(LAN)



Flash (1M) for ASF2.0



Quanta Computer Inc.			
PROJECT : ZQ3			
Size	Document Number		Rev
	LAN (AR8151)		1A
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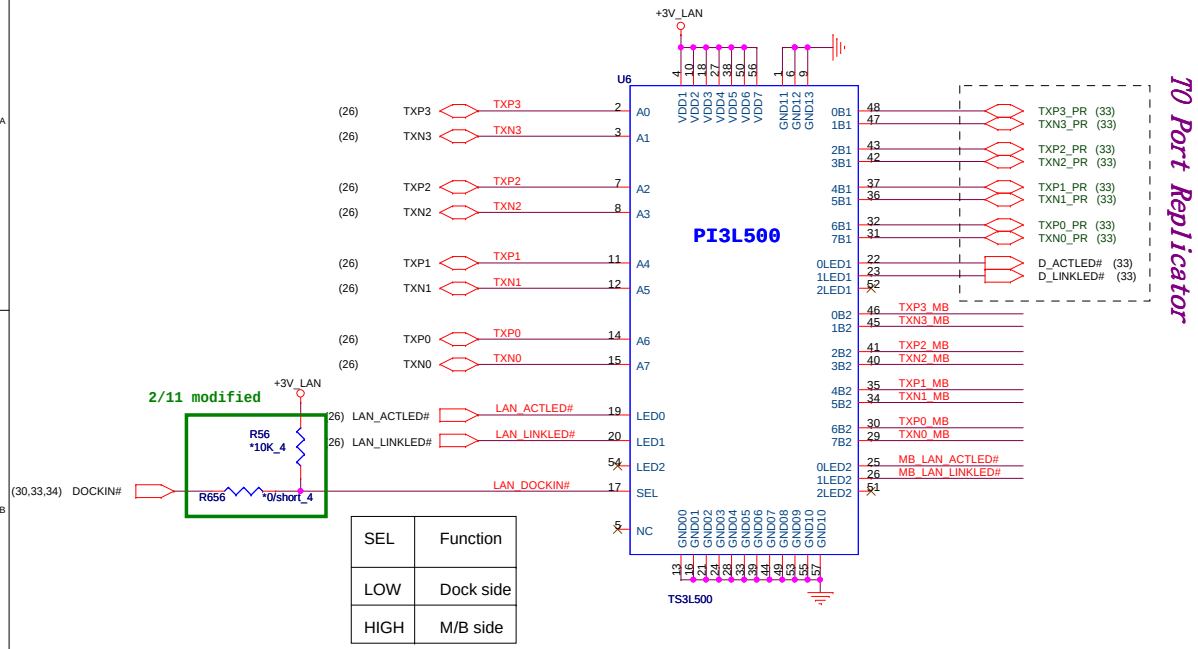
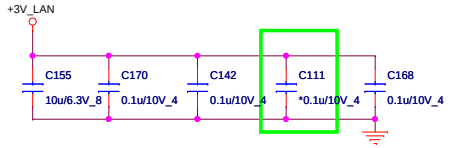
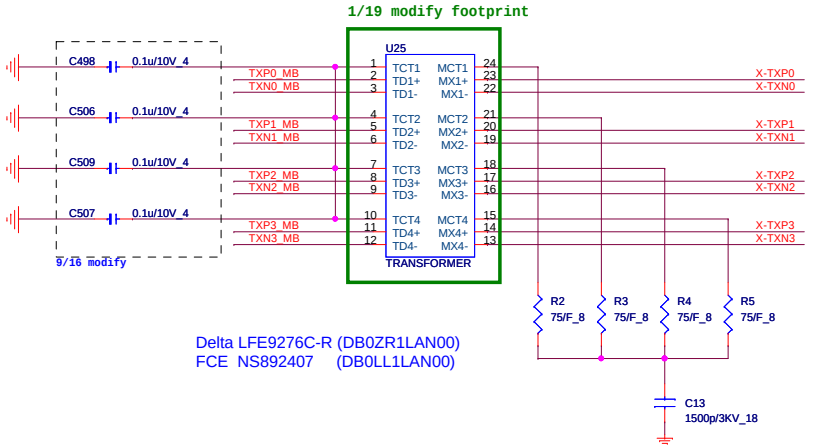
LAN SWITCH (DOK)



SEL	Function
LOW	Dock side
HIGH	M/B side

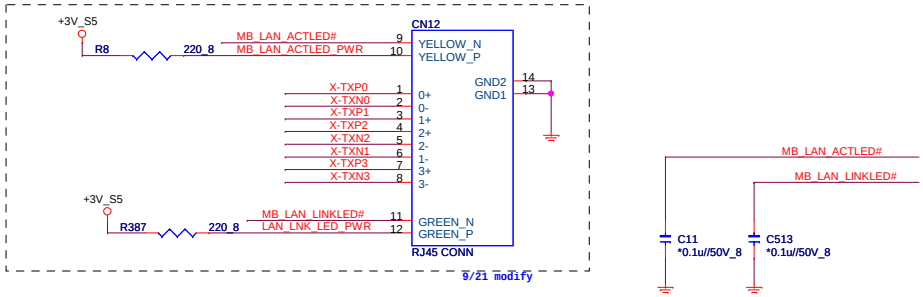


TRANSFORMER (LAN)



Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)

RJ45(LAN)



Quanta Computer Inc.
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Size	Document Number	Rev
	LAN SWITCH/TRANSFORMER/RJ45/BT	1A
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+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

MINI-CARD WLAN/WMAX(MPC)

1/21 modify (R281,R291 no stuff)

H=5.6mm

CN20

(10) PCI_RST# R291 *0_4 CL_DATA1_WLAN
(10) CLK_LPC_DEBUG R281 *0_4 CL_CLK1_WLAN

(10) CL_RST1# R283 *0_4 CL_RST1#_WLAN
(10) CL_DATA1 R282 *0_4 CL_DATA1_WLAN
(10) CL_CLK1 R290 *0_4 CL_CLK1_WLAN

+WL_VDD

(10) PCIE_TXP6
(10) PCIE_TXN6

(10) PCIE_RXP6
(10) PCIE_RXN6

8/12 modify
(10) CLK_PCH_SRC2P
(10) CLK_PCH_SRC2N
(10) CLK_PCIE_WLAN#
9/2 modify

T60 WLAN_WAKE#
9/4 modify
9/22 modify

51	Reserved	+3.3V	52
49	Reserved	GND	50
47	Reserved	+1.5V	48
45	Reserved	LED_WPAN#	46
43	Reserved	LED_WLAN#	44
41	Reserved	LED_WWAN#	42
39	Reserved	GND	40
37	Reserved	USB_D+	38
35	GND	USB_D-	36
33	PETp0	GND	34
31	PETn0	SMB_DATA	32
29	GND	SMB_CLK	30
27	GND	+1.5V	28
25	PERp0	GND	26
23	PERn0	+3.3Vaux	24
21	GND	PERST#	22
19	UIM_C4	W_DISABLE#	20
17	UIM_C8	GND	18
15	GND	UIM_VPP	16
13	REFCLK+	UIM_RST	14
11	REFCLK-	UIM_CLK	12
9	GND	UIM_DATA	10
7	CLKREQ#	UIM_PWR	8
5	Reserved	+1.5V	6
3	Reserved	GND	4
1	WAKE#	+3.3V	2

MINI-CARD 5.6H CONN

+WL_VDD
+1.5V
RF_LED#_R
USBP13+ (10)
USBP13- (10)
CLK_SDATA (3,14,15)
CLK_SCLK (3,14,15)
PLTRST# (4,10,11,16,25,26,31,34)
RF_EN (34)
LPC_LFRAME# (9,31,34)
LPC_LAD3 (9,31,34)
LPC_LAD2 (9,31,34)
LPC_LAD1 (9,31,34)
LPC_LAD0 (9,31,34)

A_LFRAME#_R R566 *0/short_4
A_LAD3_R R567 *0/short_4
A_LAD2_R R568 *0/short_4
A_LAD1_R R569 *0/short_4
A_LAD0_R R570 *0/short_4

R572 *0_4
R571 *0_4

+WL_VDD
R540 *10K_4
Active Low
1/21 modify to NMOS
Q26 2N7002D
9/10 modify
R573 *0_4
R657 0_4 3G_LED#
RF_LED_EN# (34)
RF_LED# (34,36)

+3V
R286 *0/short_8
C424 10u/10V_8
C716 0.1u/10V_4
C723 *0.1u/10V_4
C721 *0.1u/10V_4

+1.5V
C724 1000p/50V_4
C722 0.1u/10V_4
C437 10u/6.3V_8

MINI-CARD 3G(MNC)Reserve for JV41-CP

H=7.0mm

CN17

T59 9/4 modify
T58 9/4 modify
9/22 modify

(10) PCIE_TXP2
(10) PCIE_TXN2

(10) PCIE_RXP2
(10) PCIE_RXN2

(10) CLK_PCH_SRC1P
(10) CLK_PCH_SRC1N

(10) CLK_PCIE_REQ1#_R

51	Reserved	+3.3V	52
49	Reserved	GND	50
47	Reserved	+1.5V	48
45	Reserved	LED_WPAN#	46
43	Reserved	LED_WLAN#	44
41	Reserved	LED_WWAN#	42
39	Reserved	GND	40
37	Reserved	USB_D+	38
35	GND	USB_D-	36
33	PETp0	GND	34
31	PETn0	SMB_DATA	32
29	GND	SMB_CLK	30
27	GND	+1.5V	28
25	PERp0	GND	26
23	PERn0	+3.3Vaux	24
21	GND	PERST#	22
19	UIM_C4	W_DISABLE#	20
17	UIM_C8	GND	18
15	GND	UIM_VPP	16
13	REFCLK+	UIM_RST	14
11	REFCLK-	UIM_CLK	12
9	GND	UIM_DATA	10
7	CLKREQ#	UIM_PWR	8
5	Reserved	+1.5V	6
3	Reserved	GND	4
1	WAKE#	+3.3V	2

MINI-CARD 7.0H CONN

RF_LED#
3G_LED#_R
3G_LED# (36)
USBP10+ (10)
USBP10- (10)
9/10 modify
3G_SMDATA
3G_SMCLK
PLTRST#_3G
UIM_VPP
UIM_RST
UIM_CLK
UIM_DATA
UIM_PWR
3G_EN (34)
RF_EN

R489 10K_4
Active Low
R486 *0/short_4
R487 *0_4
1/13 modified

C645 *0.1u/10V_4
C647 *0.47u/10V_6
C380 *10u/6.3V_8
C373 0.1u/10V_4
C382 *10u/6.3V_8

Q19 *2N7002D
Q20 *2N7002D
R488 *4.7K_4P2R
R234 *0_4
R235 *0_4
(3,10,26) ICH_SMBDATA
(3,10,26) ICH_SMBCLK
3G_SMDATA
3G_SMCLK

L25 0_8
L24 *0_8
100mil
C379 10u/6.3V_8
C646 0.1u/10V_4
C372 0.1u/10V_4
C642 0.1u/10V_4
C383 0.47u/10V_6
C644 10p/50V_4

A:(10/17)FAE confirm:
3G module need +3VSUS and no need +1.5V and no need SMBUS

SIM CARD FFC connector(RFM)

CN4

(10) USBP5-
(10) USBP5+
R44 *3G@0_4 USBP5-_R
R43 *3G@0_4 USBP5+_R

UIM_PWR
UIM_VPP
UIM_RST
UIM_CLK
UIM_DATA

3G@SIM_CARD FFC CONN

C141 *3G@10u/6.3V_8
C123 3G@27p/50V_4
C110 3G@10p/50V_4
C136 3G@27p/50V_4
C147 *3G@10u/6.3V_8
C137 3G@33p/50V_4
C120 3G@10p/50V_4

U20 *3G@SN74AHC1G32DCKR
PLTRST#_3G
3G_RESET (34)
PLTRST# (4,10,11,16,25,26,31,34)
R233 3G@0_4

Quanta Computer Inc.
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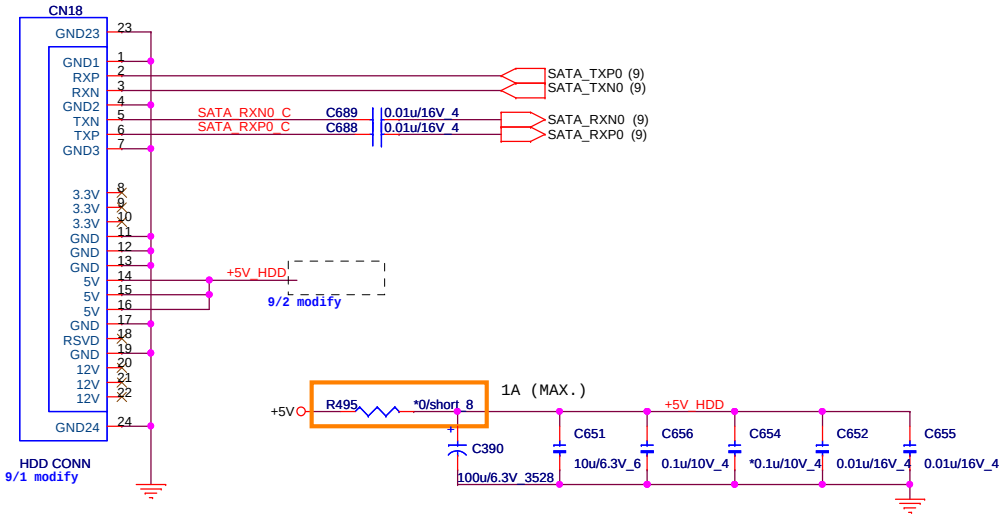
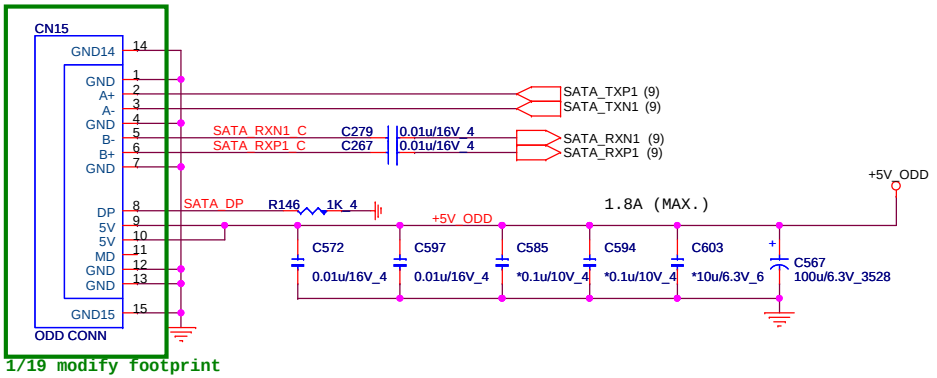
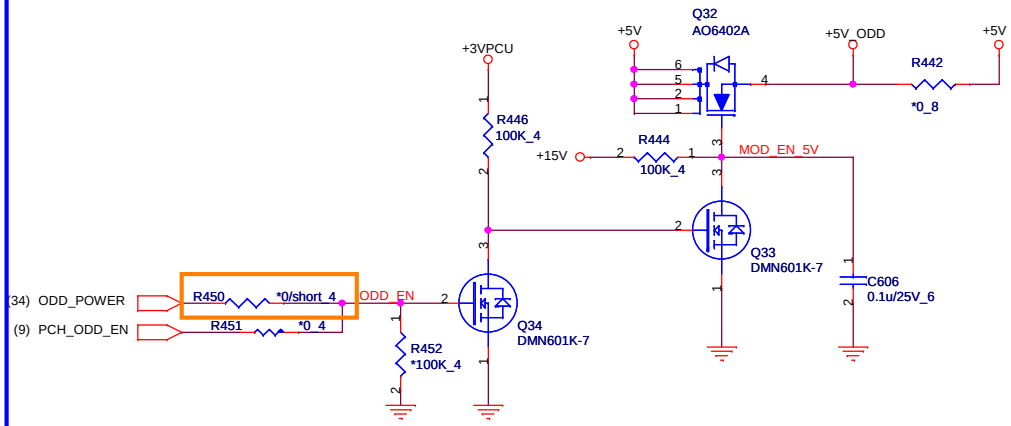
SATA HDD(HDD)



SATA ODD (ODD)



ODD POWER(ODD)



Connect to PCH(GPIO21) pin Y9
and EC pin28(GPIO53)

Quanta Computer Inc.		
PROJECT : ZQ3		
Size	Document Number: SATA-HDD/ODD/HOLE	Rev: 1A
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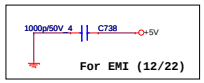
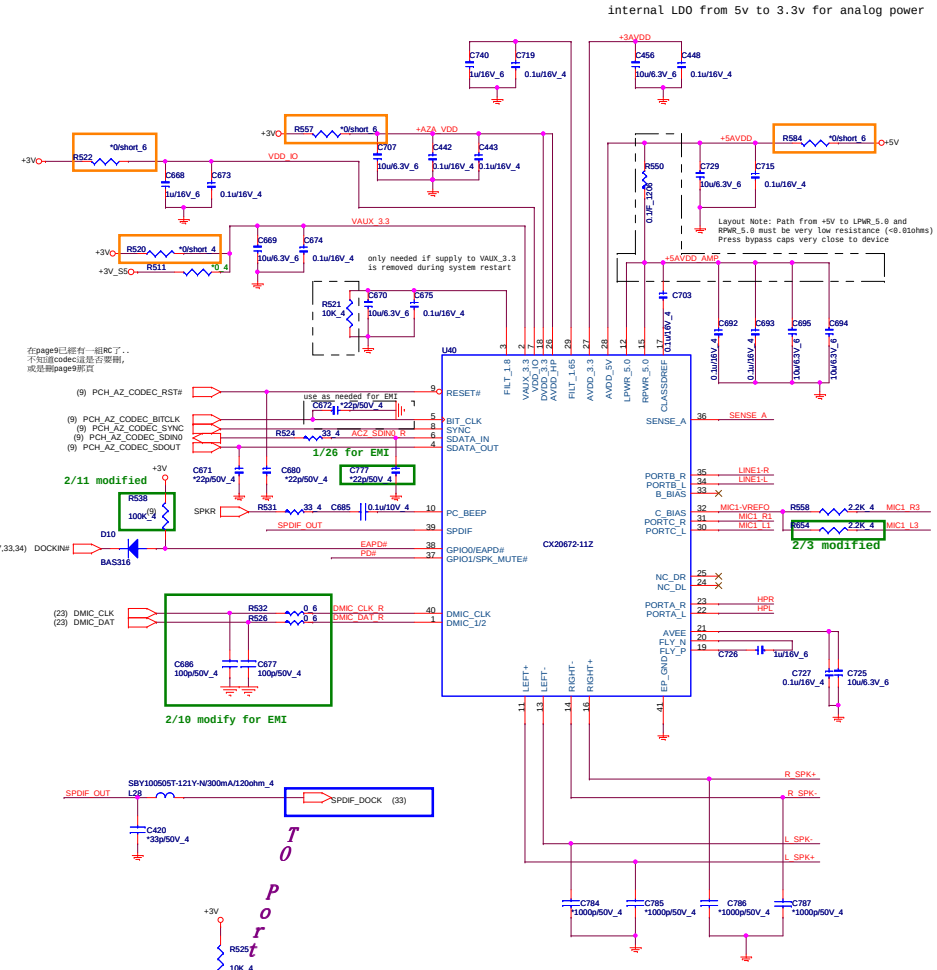
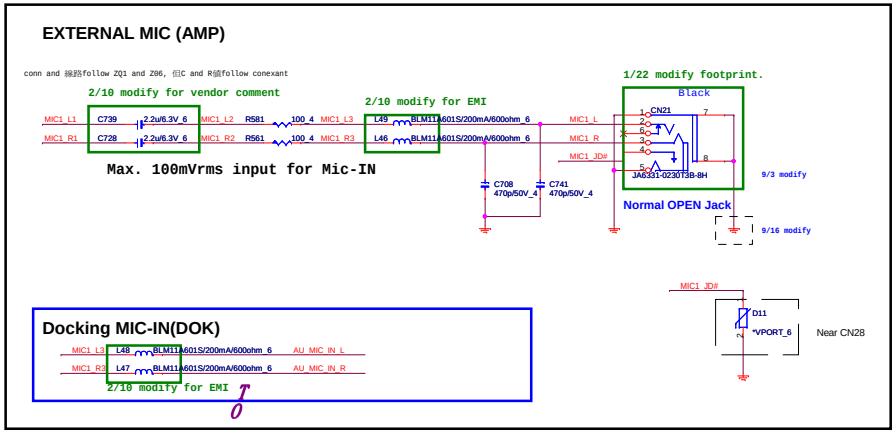
Codec(ADO)

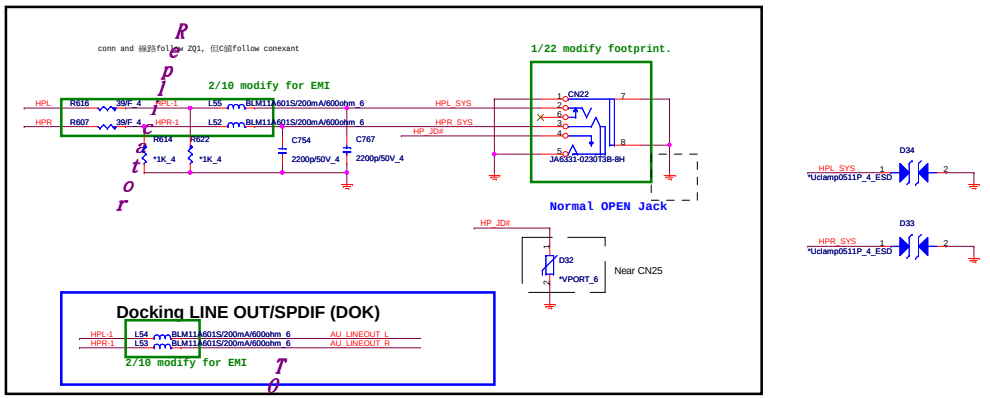




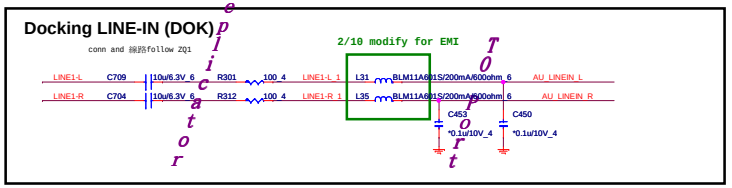
EXTERNAL MIC (AMP)



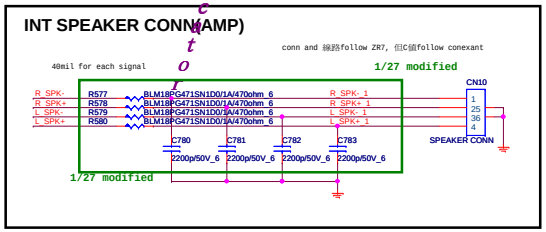
LINE-OUT/SPDIFO(AMP)



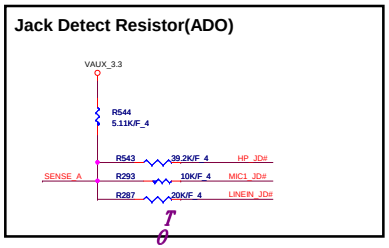
Docking LINE-IN (DOK)

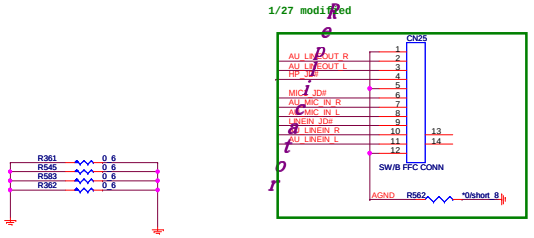


INT SPEAKER CONN(AMP)



Jack Detect Resistor(ADO)





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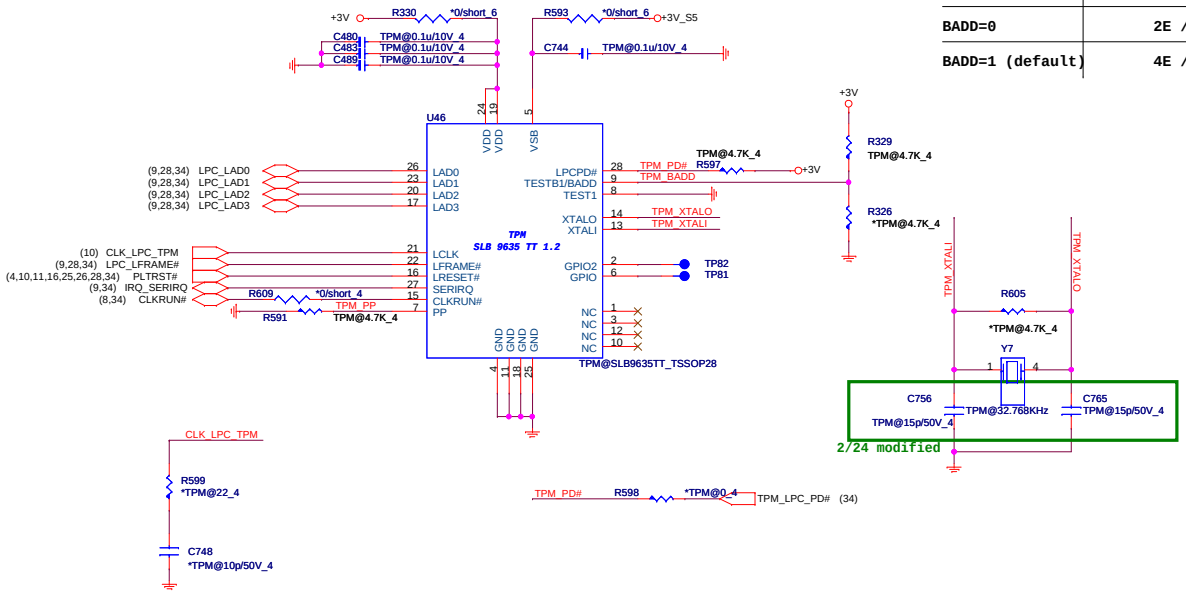
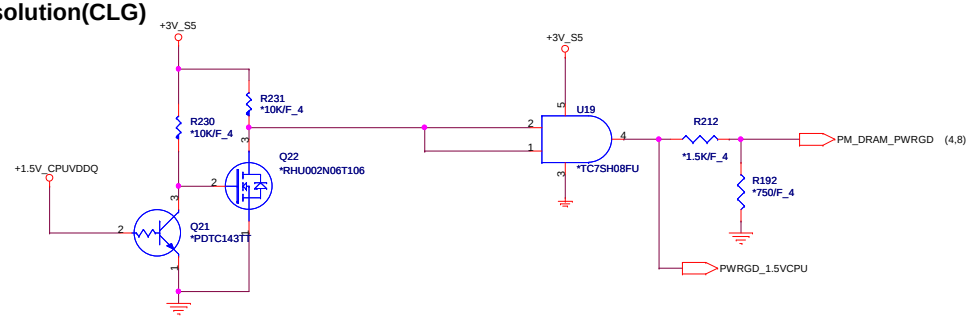
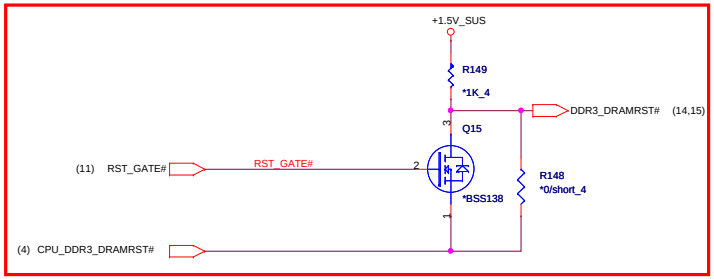
(TPM)

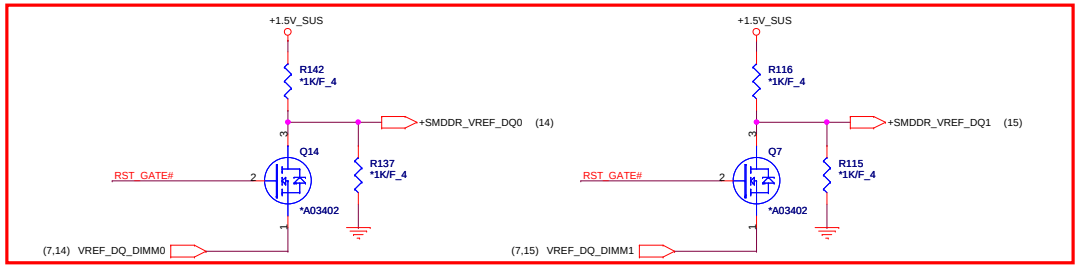
	Resiger Base Address
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F



S3 leakage solution(CLG)







Quanta Computer Inc.
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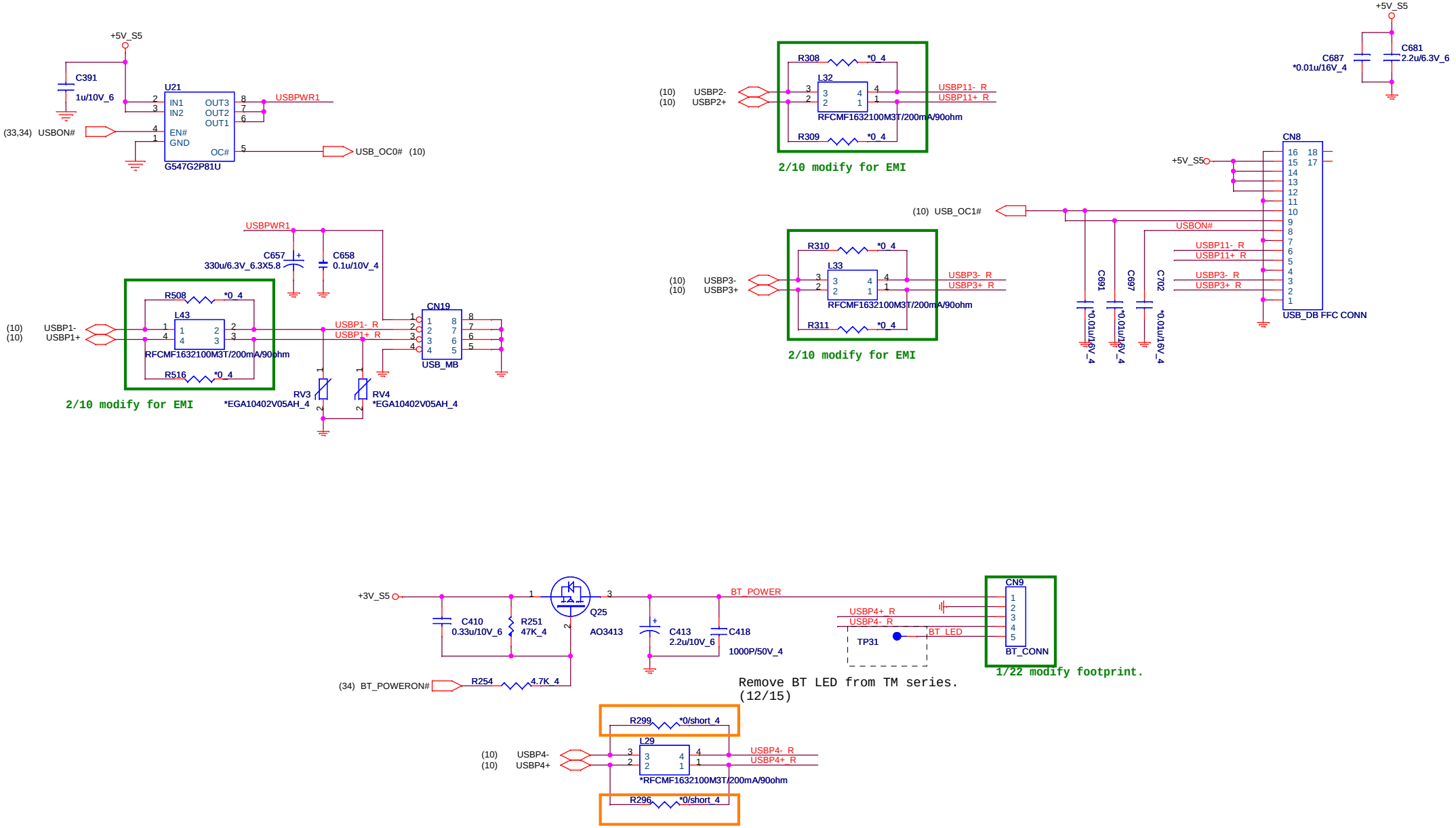

Quanta Computer Inc.		
PROJECT : ZQ3		
Size	Document Number	Rev
	eSATA/USB	1A
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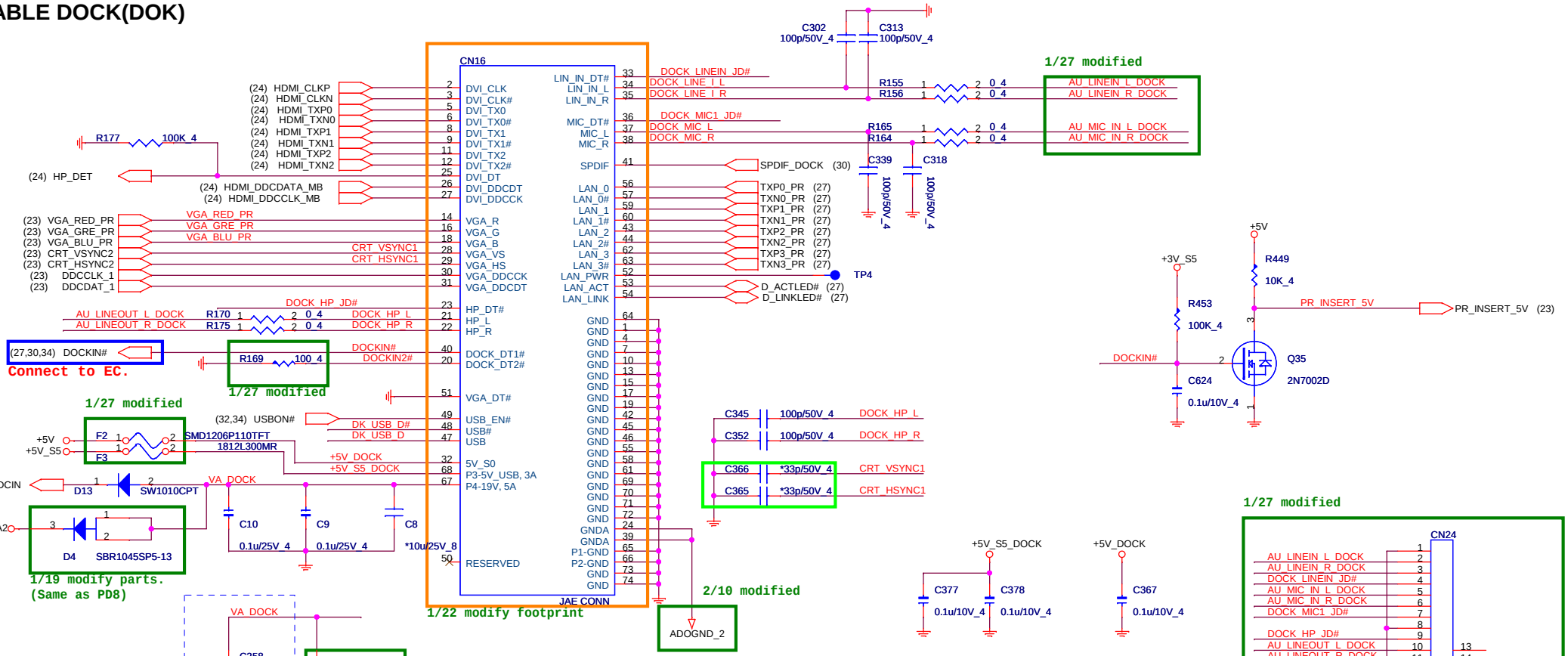
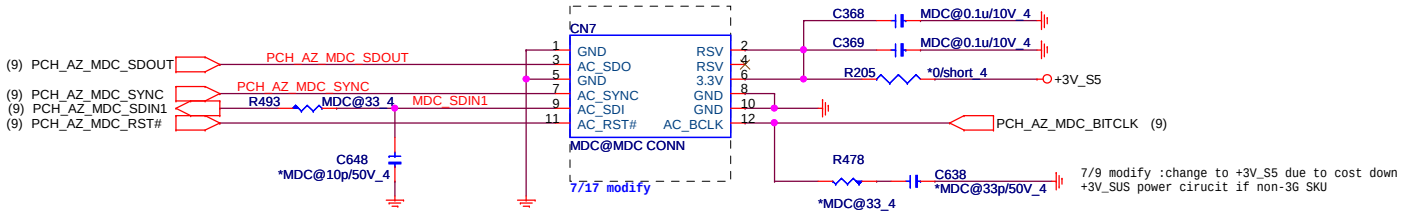
CABLE DOCK(DOK)



MDC(MDM)



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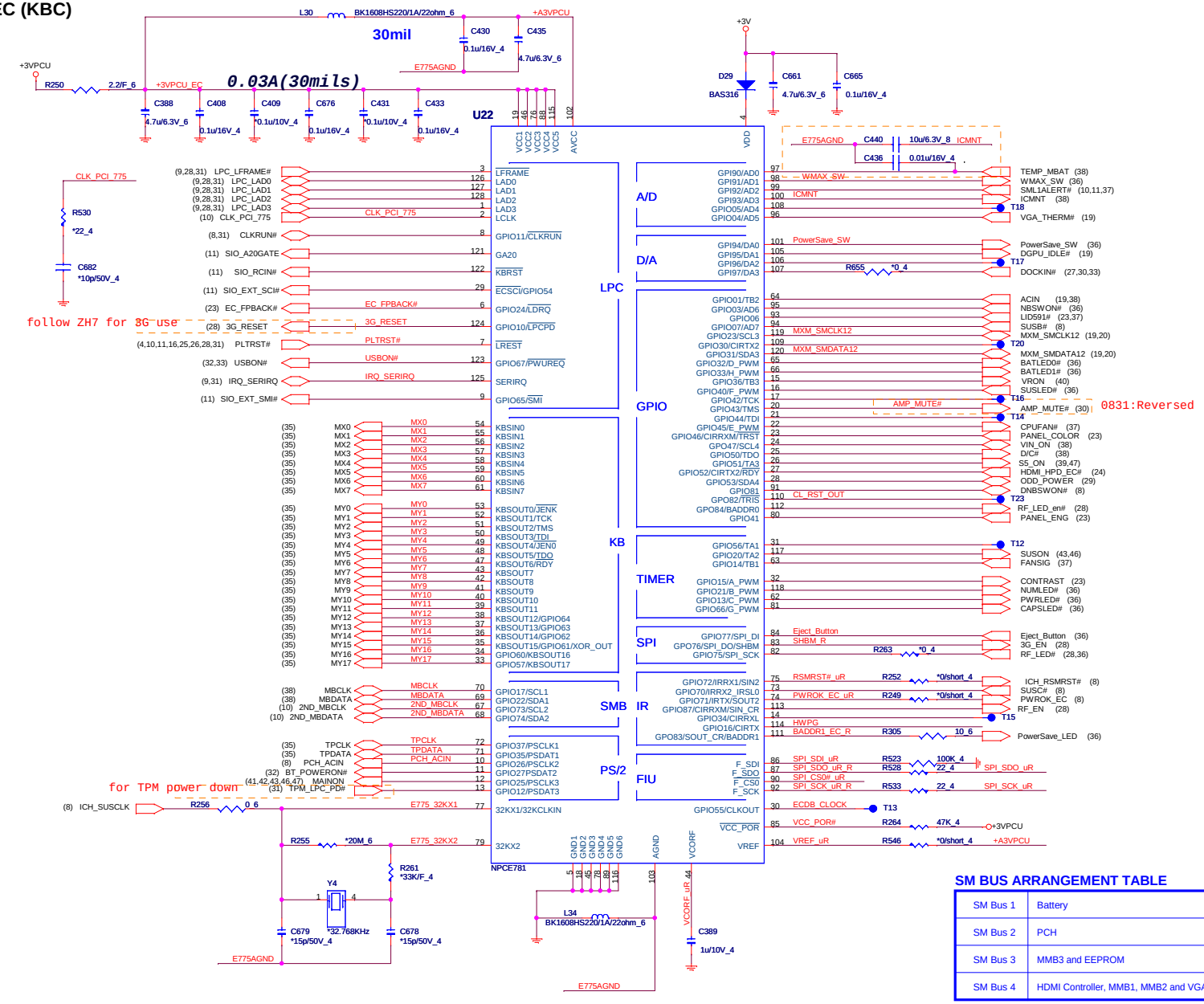
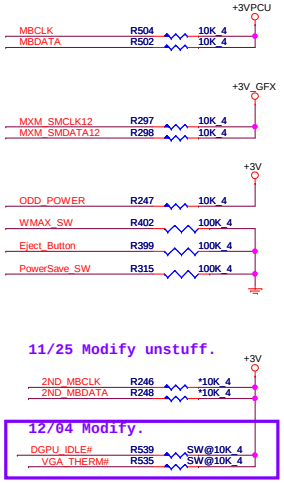
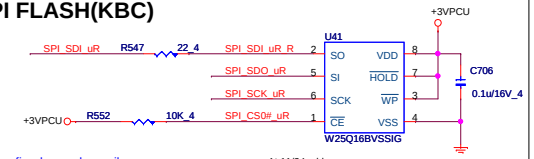
EC (KBC)



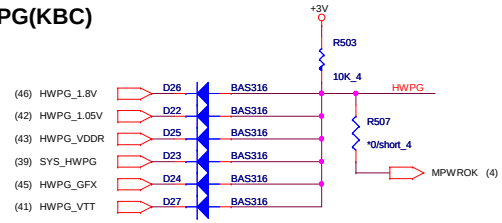
SM BUS PU(KBC)



SPI FLASH(KBC)



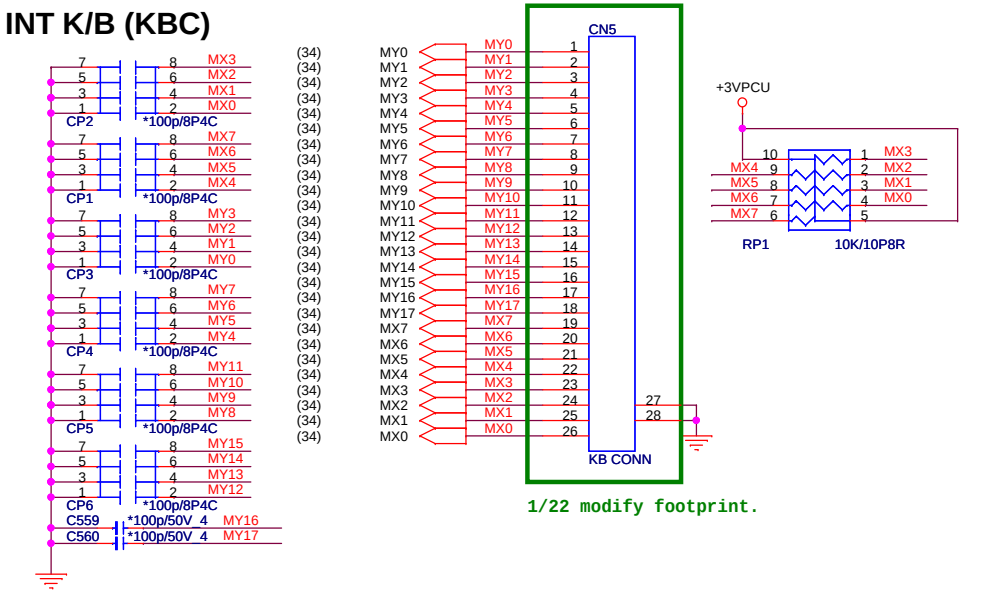
HWPG(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

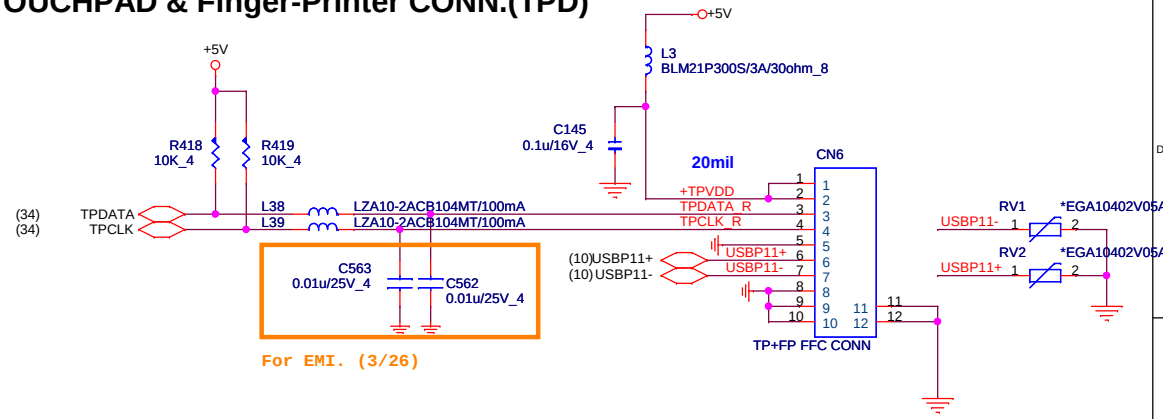
Quanta Computer Inc.	PROJECT : ZQ3
Size	Document Number: WPCE775C_0DG & FLASH — Rev: 1A
Date: Monday, March 29, 2010	Sheet 34 of 47

INT K/B (KBC)



1/22 modify footprint.

TOUCHPAD & Finger-Printer CONN.(TPD)



For EMI. (3/26)

HOLE1 *HG-C276D118P2
HOLE2 *HG-C315D118P2
HOLE28 *HG-C276D118P2
HOLE7 *HG-C276D118P2
HOLE5 *HG-TC276BC315D118P2
HOLE12 *HG-C197D118P2
HOLE10 *HG-TC315BC276D118P2

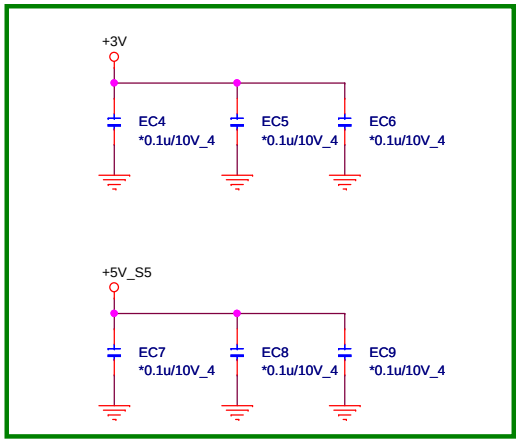
HOLE16 *HG-C276D118P2
HOLE23 *HG-C276D118P2
HOLE21 *HG-C236D118P2
HOLE24 *HG-C236D118P2
HOLE22 *HG-C315D118P2
HOLE14 *HG-C315D118P2

HOLE3 *H-C276D142P2
HOLE4 *H-C217D146P2
HOLE9 *H-C217D146P2
HOLE11 *H-TC276BC256D146P2
HOLE15 * H-C197D59P2
HOLE18 * H-C197D59P2
HOLE17 *H-TC276BC217D146P2
HOLE20 *H-TC276BC217D146P2

HOLE25 *H-C197D87P2
HOLE26 *H-C197D87P2
HOLE27 * H-C197D51P1

HOLE6 *H-C94D94N
HOLE8 *O-ZQ3-2
HOLE19 *O-ZQ3-1

ZQ3_BKT
*Intel_CPU_BKT



2/8 modified for EMI

Quanta Computer Inc.		
PROJECT : ZQ3		
Size	Document Number: KB/TP+FP/CIR/BT/TPScreen	Rev: 1A
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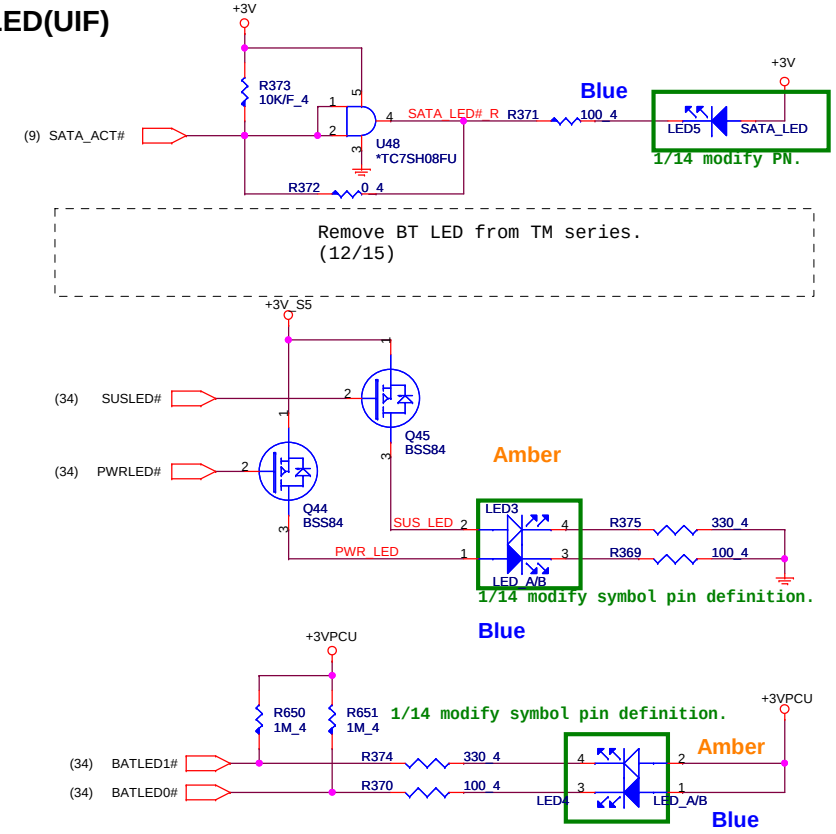
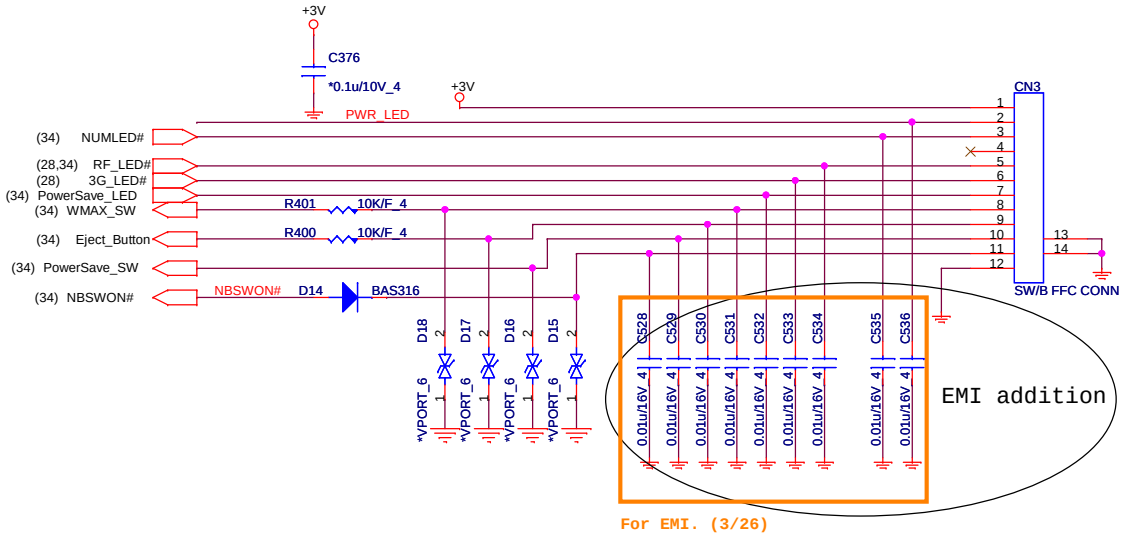
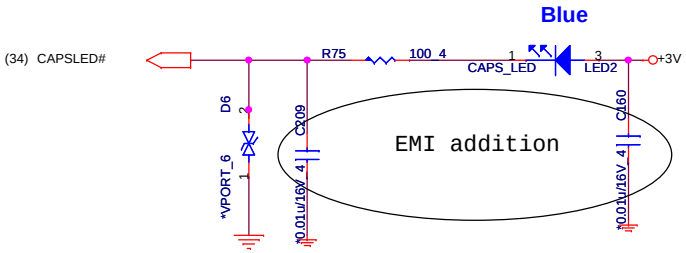
M/B LED(UIF)

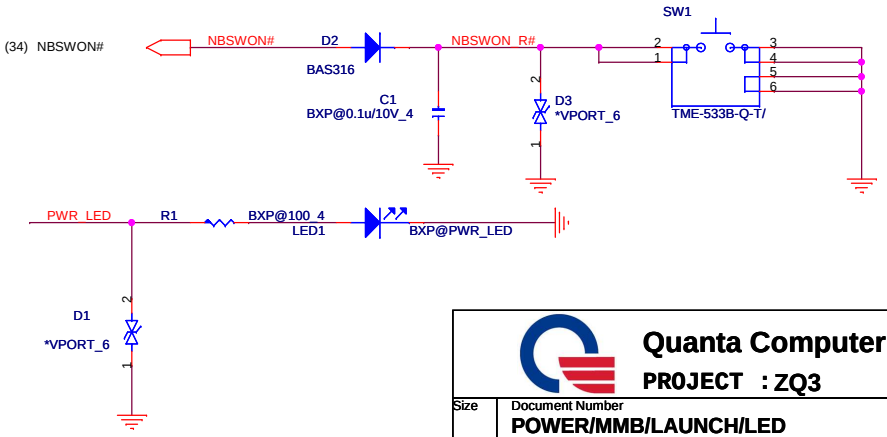


SW BOARD CONNECTOR(UIF)



M/B LED(UIF)





Quanta Computer Inc.

PROJECT : ZQ3

Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A

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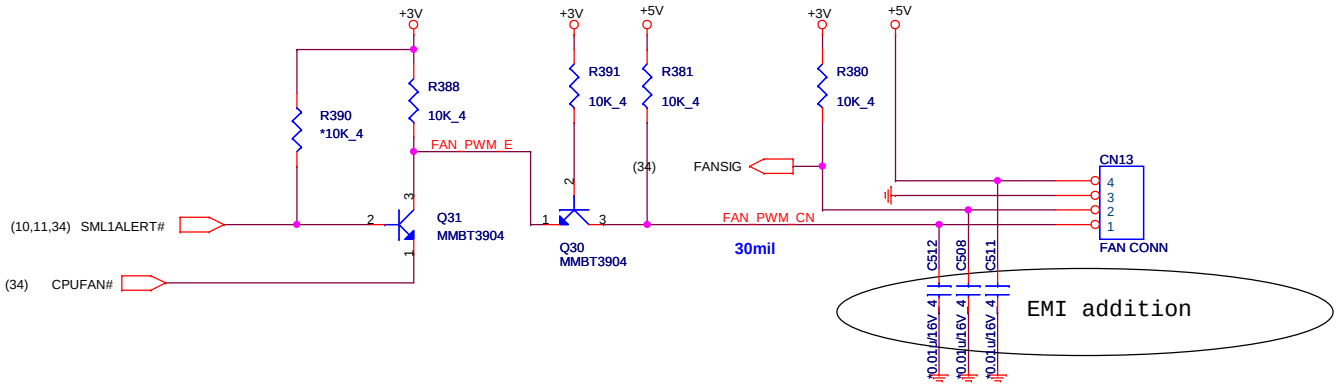
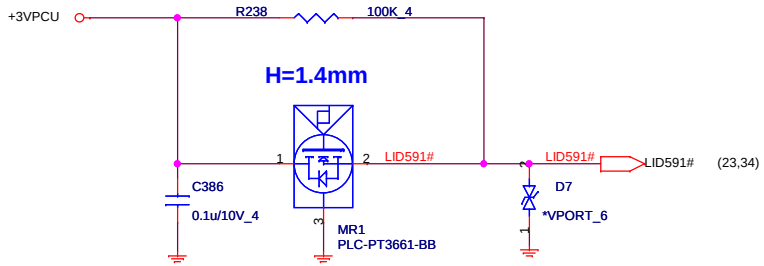
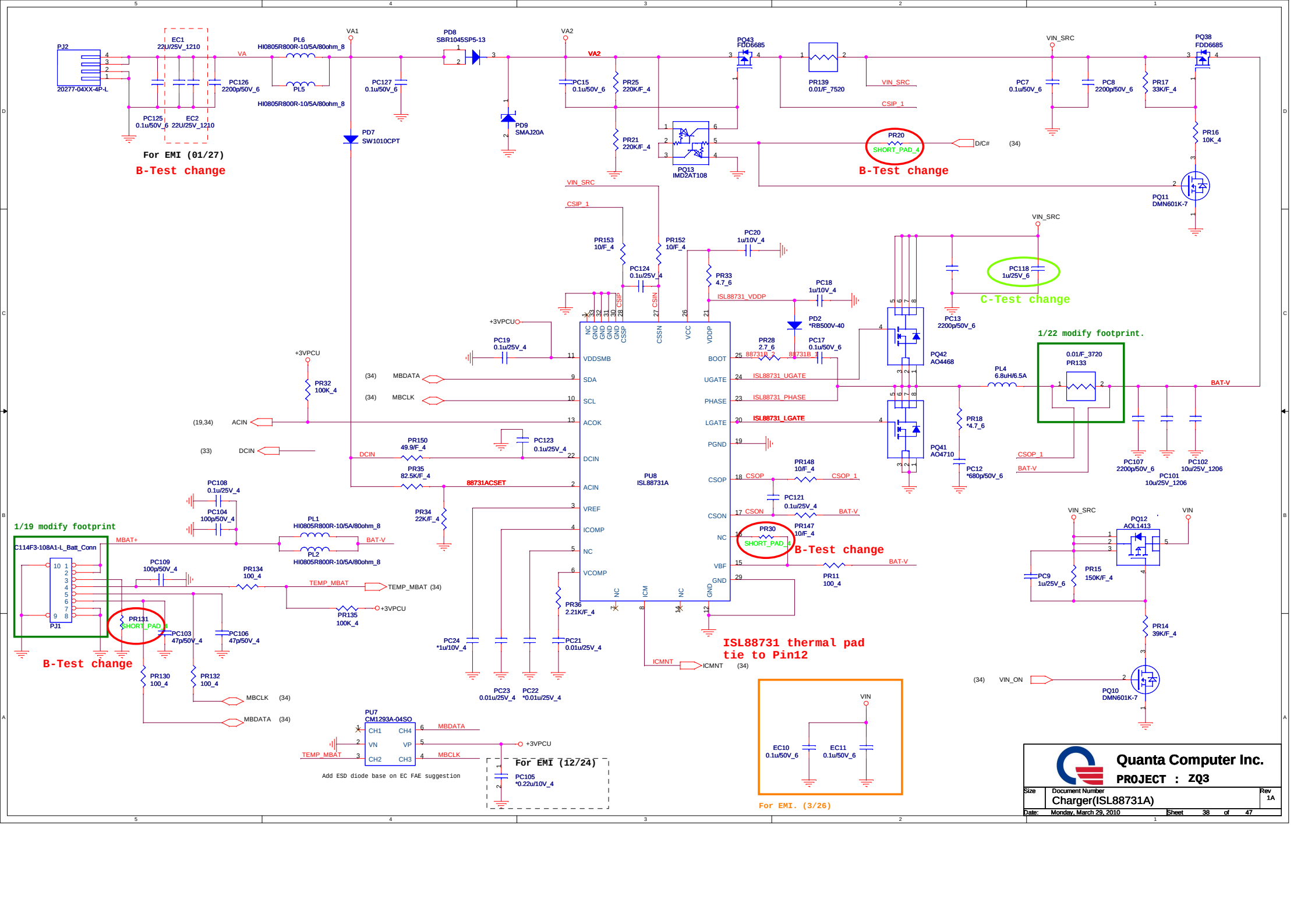
CPU FAN(THM)

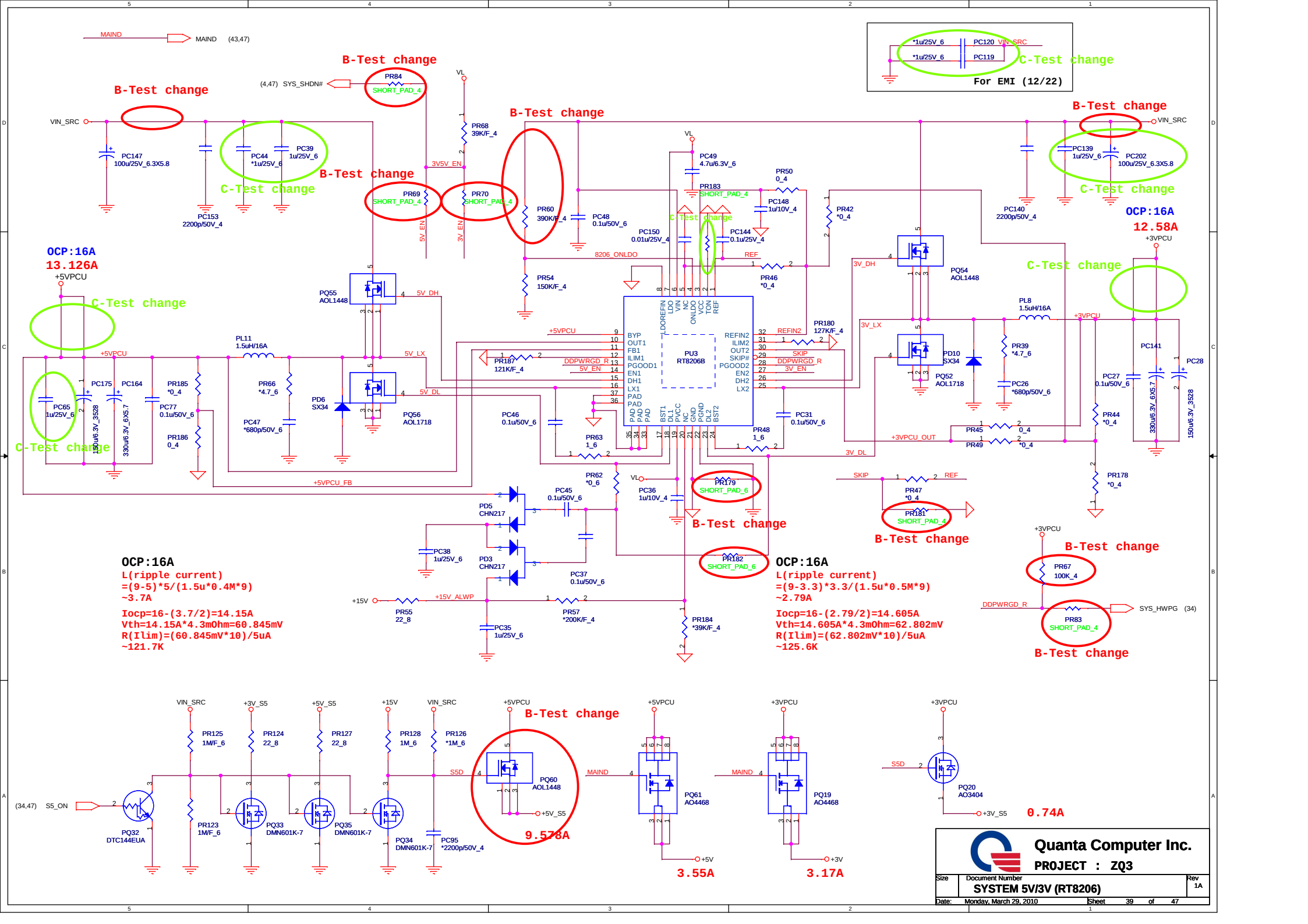


HALL SENSOR(HSR)



Quanta Computer Inc.		
PROJECT : ZQ3		
Size	Document Number: FAN/Thermal Protection	Rev: 1A
Date: Monday, March 29, 2010	Sheet 37 of 47	


PJ2
20277-04XX-4P-L
EC1
22U/25V_1210
EC2
22U/25V_1210
PC125
0.1u/50V_6
PC126
2200p/50V_6
VA
PL6
HI0805R800R-10/5A/80ohm_8
PL5
HI0805R800R-10/5A/80ohm_8
VA1
PC127
0.1u/50V_6
PD7
SW1010CPT
PD8
SBR1045SP5-13
PD9
SMAJ20A
VA2
PC15
0.1u/50V_6
PR25
220K/F_4
PR21
220K/F_4
PQ43
FDD6685
PQ13
IMD2AT108
PR139
0.01/F_7520
VIN_SRC
CSIP_1
PR20
SHORT_PAD_4
D/C#
(34)
B-Test change
For EMI (01/27)
B-Test change
PQ38
FDD6685
PC7
0.1u/50V_6
PC8
2200p/50V_6
PR17
33K/F_4
PR16
10K_4
PQ11
DMN601K-7
PR153
10/F_4
PR152
10/F_4
PC124
0.1u/25V_4
PC20
1u/10V_4
PR33
4.7_6
ISL88731_VDDP
PC18
1u/10V_4
PD2
*RB500V-40
PC118
1u/25V_6
C-Test change
PC13
2200p/50V_6
1/22 modify footprint.
0.01/F_3720
PR133
PQ42
AO4468
PQ41
AO4710
PL4
6.8uH/6.5A
BAT-V
PR18
*4.7_6
PC12
*680p/50V_6
PC107
2200p/50V_6
PC102
10u/25V_1206
PC101
10u/25V_1206
+3VPCU
PC19
0.1u/25V_4
PR32
100K_4
(34) MBDATA
(34) MBCLK
(19,34) ACIN
(33) DCIN
PR150
49.9/F_4
PC123
0.1u/25V_4
PR35
82.5K/F_4
88731ACSET
PR34
22K/F_4
PU8
ISL88731A
NC
GND
GND
GND
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
PR28
2.7_6
88731B_2
88731B_1
PC17
0.1u/50V_6
PR148
10/F_4
CSOP_1
PC121
0.1u/25V_4
PR147
10/F_4
PR30
SHORT_PAD_4
PR11
100_4
PR36
2.21K/F_4
PC24
*1u/10V_4
PC23
0.01u/25V_4
PC22
*0.01u/25V_4
PC21
0.01u/25V_4
ICMNT
ICMNT (34)
ISL88731 thermal pad
tie to Pin12
B-Test change
1/19 modify footprint
C114F3-108A1-L_Batt_Conn
PJ1
MBAT+
PC108
0.1u/25V_4
PC104
100p/50V_4
PL1
HI0805R800R-10/5A/80ohm_8
PL2
HI0805R800R-10/5A/80ohm_8
BAT-V
PC109
100p/50V_4
PR134
100_4
TEMP_MBAT
TEMP_MBAT (34)
PR135
100K_4
+3VPCU
PR131
SHORT_PAD_4
PC103
47p/50V_4
PC106
47p/50V_4
PR130
100_4
PR132
100_4
MBCLK (34)
MBDATA (34)
B-Test change
PU7
CM1293A-04SO
CH1
VN
CH2
CH4
VP
CH3
MBDATA
MBCLK
+3VPCU
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
For EMI (12/24)
PC105
*0.22u/10V_4
VIN
EC10
0.1u/50V_6
EC11
0.1u/50V_6
For EMI. (3/26)
PQ12
AOL1413
VIN
PC9
1u/25V_6
PR15
150K/F_4
PR14
39K/F_4
(34) VIN_ON
PQ10
DMN601K-7
Quanta Computer Inc.
PROJECT : ZQ3
Size
Document Number
Charger(ISL88731A)
Rev
1A
Date: Monday, March 29, 2010
Sheet 38 of 47


MAIND
MAIND (43,47)
B-Test change
(4,47) SYS_SHDN#
PR84
SHORT_PAD_4
VL
VIN_SRC
PC147
100u/25V_6.3X5.8
PC44
*1u/25V_6
PC39
1u/25V_6
C-Test change
PC153
2200p/50V_4
PR68
39K/F_4
3V5V_EN
PR69
SHORT_PAD_4
PR70
SHORT_PAD_4
5V_EN
3V_EN
PR60
390K/F_4
PR54
150K/F_4
PC48
0.1u/50V_6
PC150
0.01u/25V_4
8206_ONLDO
REF
PC49
4.7u/6.3V_6
PR183
SHORT_PAD_4
PR50
0_4
PC148
1u/10V_4
PC144
0.1u/25V_4
PR42
*0_4
PR46
*0_4
PC140
2200p/50V_4
PC139
1u/25V_6
PC202
100u/25V_6.3X5.8
OCP:16A
12.58A
OCP:16A
13.126A
+5VPCU
+3VPCU
PQ55
AOL1448
5V_DH
3V_DH
PQ54
AOL1448
PL11
1.5uH/16A
5V_LX
3V_LX
PL8
1.5uH/16A
PU3
RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DL1
PVCC
NC
GND
PGND
DL2
BST2
PR187
121K/F_4
DDPWRGD_R
5V_EN
PR180
127K/F_4
REFIN2
SKIP
DDPWRGD_R
3V_EN
PC65
1u/25V_6
PC175
150u/6.3V_3528
PC164
330u/6.3V_6X5.7
PR185
*0_4
PR186
0_4
PC77
0.1u/50V_6
PR66
*4.7_6
PC47
*680p/50V_6
PD6
SX34
PQ56
AOL1718
PC46
0.1u/50V_6
PR63
1_6
PR48
1_6
PC31
0.1u/50V_6
PD10
SX34
PQ52
AOL1718
PR39
*4.7_6
PC26
*680p/50V_6
PC27
0.1u/50V_6
PC141
330u/6.3V_6X5.7
PC28
150u/6.3V_3528
PR44
*0_4
PR45
0_4
PR49
*0_4
PR178
*0_4
+3VPCU_OUT
PR62
*0_6
PC45
0.1u/50V_6
PC36
1u/10V_4
PR179
SHORT_PAD_6
PR47
*0_4
PR181
SHORT_PAD_4
SKIP
REF
PD5
CHN217
PD3
CHN217
PC38
1u/25V_6
PC37
0.1u/50V_6
PR182
SHORT_PAD_6
+15V
+15V_ALWP
PR55
22_8
PR57
*200K/F_4
PC35
1u/25V_6
PR184
*39K/F_4
PR67
100K_4
DDPWRGD_R
SYS_HWPG (34)
PR83
SHORT_PAD_4
B-Test change
C-Test change
For EMI (12/22)
*1u/25V_6
PC120
VIN_SRC
*1u/25V_6
PC119
OCP:16A
L(ripple current)
=(9-5)*5/(1.5u*0.4M*9)
~3.7A
Iocp=16-(3.7/2)=14.15A
Vth=14.15A*4.3mOhm=60.845mV
R(Ilim)=(60.845mV*10)/5uA
~121.7K
OCP:16A
L(ripple current)
=(9-3.3)*3.3/(1.5u*0.5M*9)
~2.79A
Iocp=16-(2.79/2)=14.605A
Vth=14.605A*4.3mOhm=62.802mV
R(Ilim)=(62.802mV*10)/5uA
~125.6K
(34,47) S5_ON
PQ32
DTC144EUA
PR125
1M/F_6
PR123
1M/F_6
PR124
22_8
PQ33
DMN601K-7
PR127
22_8
PQ35
DMN601K-7
PR128
1M_6
PR126
*1M_6
S5D
PQ34
DMN601K-7
PC95
*2200p/50V_4
PQ60
AOL1448
+5V_S5
9.578A
PQ61
AO4468
+5V
3.55A
PQ19
AO4468
+3V
3.17A
PQ20
AO3404
+3V_S5
0.74A
Quanta Computer Inc.
PROJECT : ZQ3
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev
1A
Date: Monday, March 29, 2010
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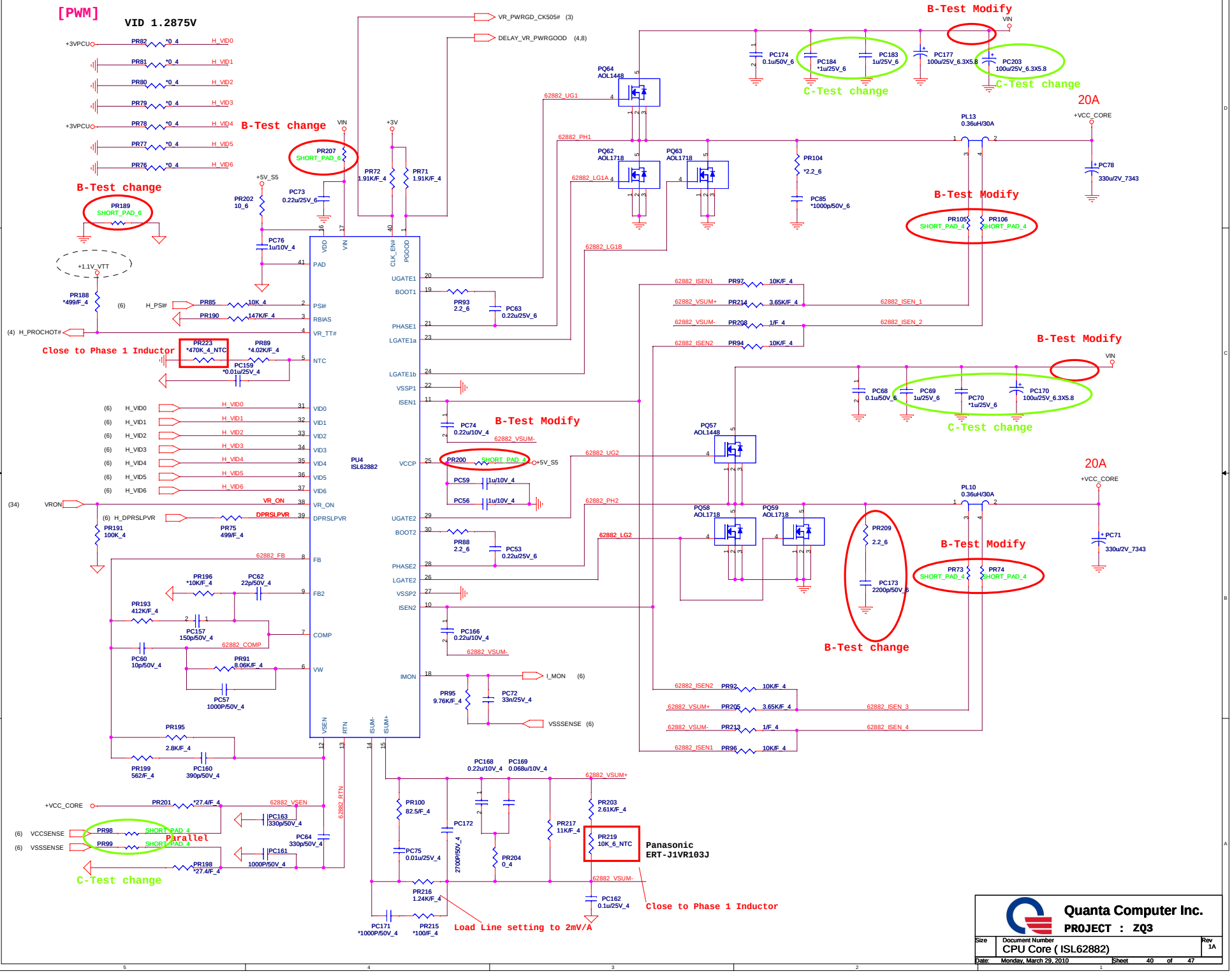
[PWM]
VID 1.2875V
B-Test Modify
C-Test change
B-Test change
20A
Close to Phase 1 Inductor
Parallel
Panasonic
ERT-J1VR103J
Load Line setting to 2mV/A
Quanta Computer Inc.
PROJECT : ZQ3
CPU Core (ISL62882)
Monday, March 29, 2010
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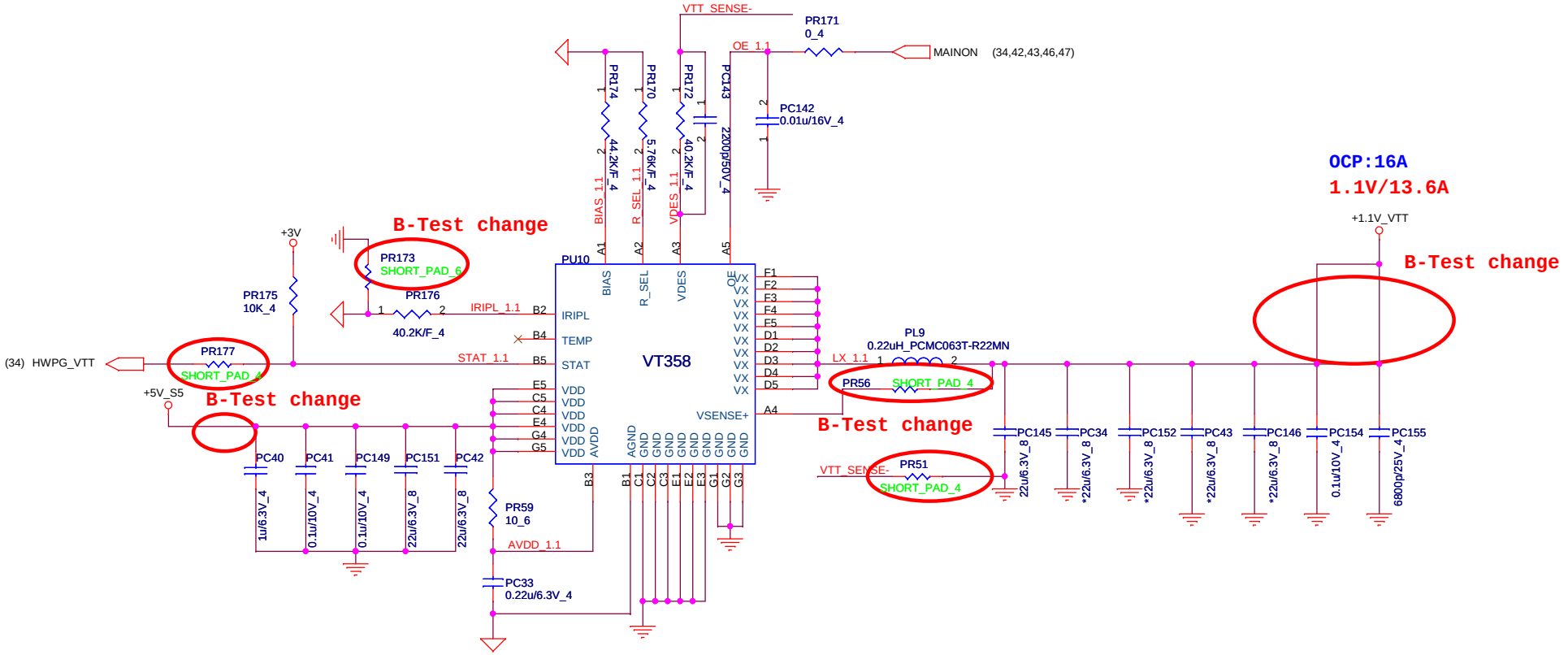
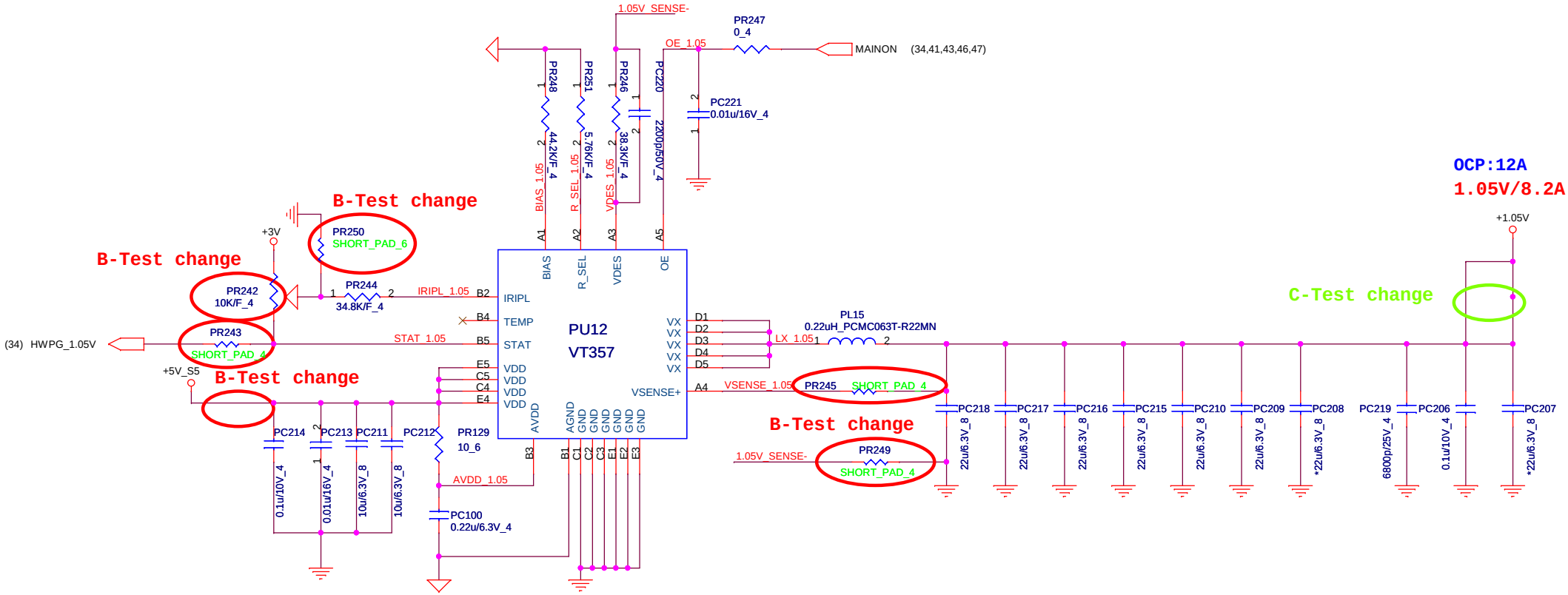
[PWM]

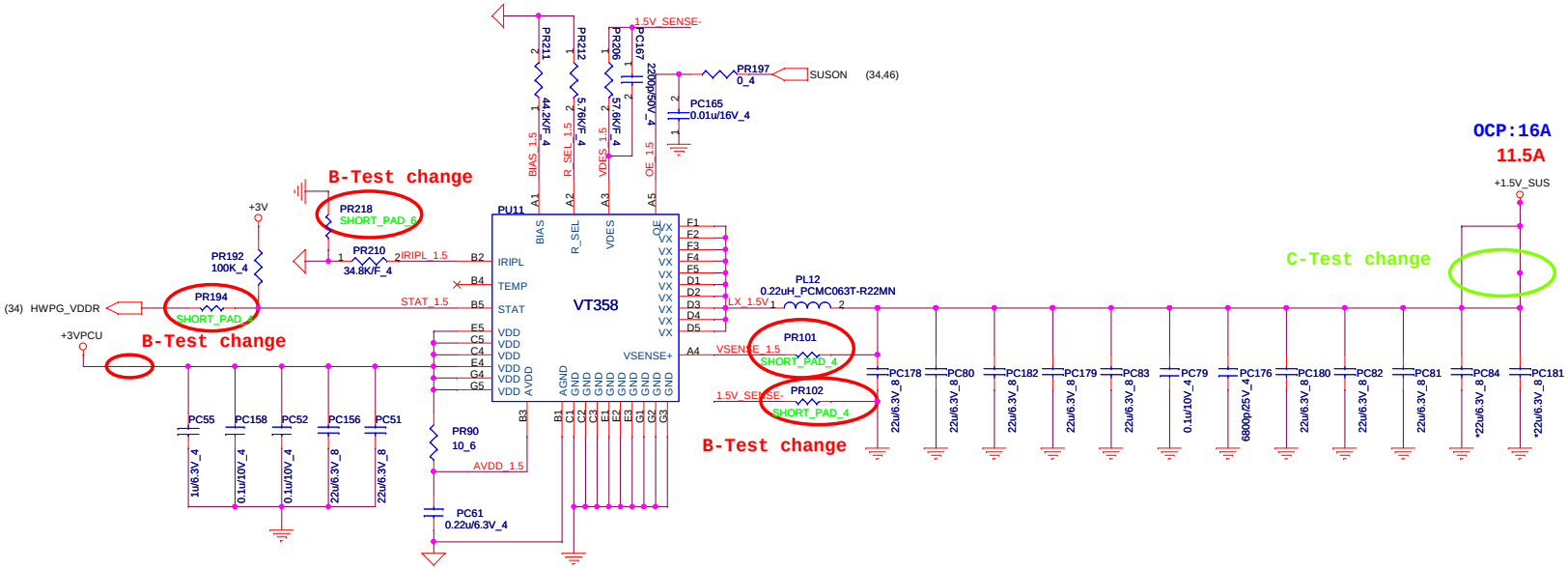


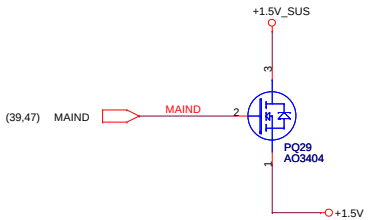
Quanta Computer Inc.		
PROJECT : ZQ3		
Size	Document Number: +VTT (UP6111A)	Rev: 1A
Date: Monday, March 29, 2010	Sheet 41 of 47	

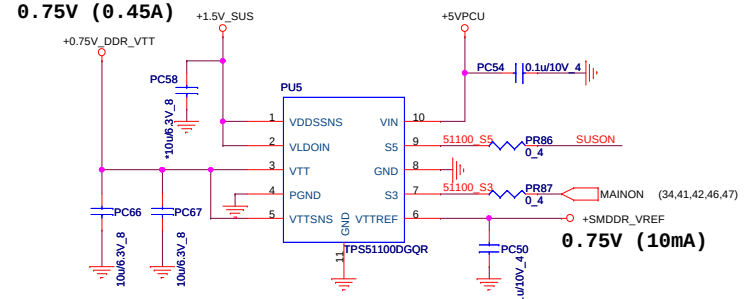


Quanta Computer Inc.		
PROJECT : ZQ3		
Size	Document Number: VCCP 1.05V(UP6111A)	Rev: 1A
Date: Monday, March 29, 2010	Sheet 42 of 47	

[PWM]







	S3	S5	VTT	REF	+1.5VSUS
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.

PROJECT : ZQ3

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

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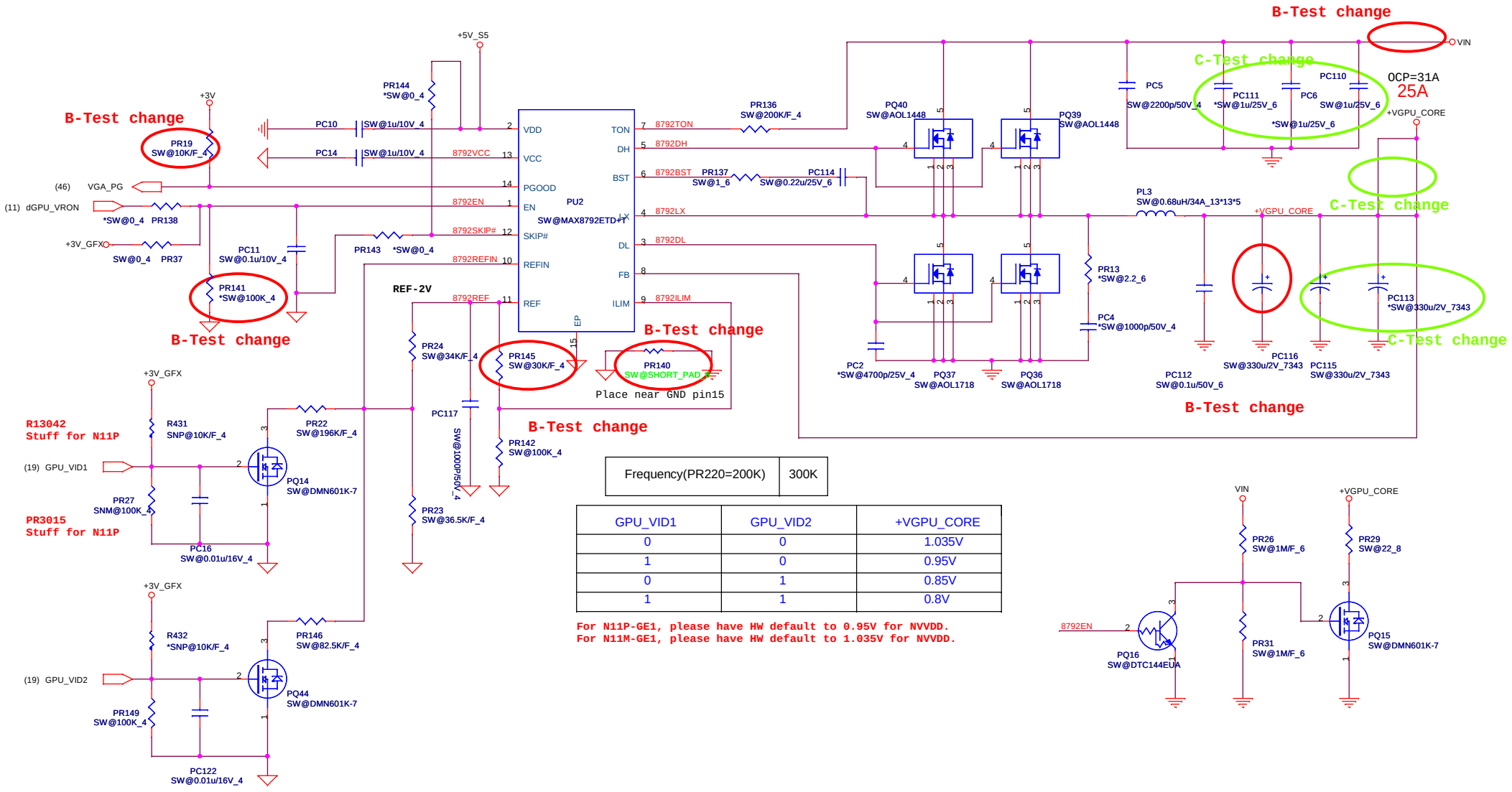
B-Test change
C-Test change
+5V_S5
+3V
VIN
PU2
SW@MAX8792ETD+T
VDD
VCC
PGOOD
EN
SKIP#
REFIN
REF
TON
DH
BST
LX
DL
FB
ILIM
EP
8792VCC
8792EN
8792SKIP#
8792REFIN
8792REF
8792TON
8792DH
8792BST
8792LX
8792DL
8792ILIM
PR144 *SW@0_4
PC10 SW@1u/10V_4
PC14 SW@1u/10V_4
PR19 SW@10K/F_4
(46) VGA_PG
(11) dGPU_VRON
*SW@0_4 PR138
+3V_GFX
SW@0_4 PR37
PC11 SW@0.1u/10V_4
PR143 *SW@0_4
PR141 *SW@100K_4
REF-2V
PR24 SW@34K/F_4
PR145 SW@30K/F_4
PR140 SW@SHORT_PAD
Place near GND pin15
PC117 SW@1000P/50V_4
PR142 SW@100K_4
PR23 SW@36.5K/F_4
PR136 SW@200K/F_4
PR137 SW@1_6
PC114 SW@0.22u/25V_6
PQ40 SW@AOL1448
PQ39 SW@AOL1448
PC5 SW@2200p/50V_4
PC111 *SW@1u/25V_6
PC6 SW@1u/25V_6
PC110 *SW@1u/25V_6
OCP=31A
25A
+VGPU_CORE
PL3 SW@0.68uH/34A_13*13*5
PR13 *SW@2.2_6
PC4 *SW@1000p/50V_4
PC2 *SW@4700p/25V_4
PQ37 SW@AOL1718
PQ36 SW@AOL1718
PC112 SW@0.1u/50V_6
PC116 SW@330u/2V_7343
PC115 SW@330u/2V_7343
PC113 *SW@330u/2V_7343
R13042
Stuff for N11P
PR3015
Stuff for N11P
+3V_GFX
R431 SNP@10K/F_4
PR22 SW@196K/F_4
(19) GPU_VID1
PR27 SNM@100K_4
PQ14 SW@DMN601K-7
PC16 SW@0.01u/16V_4
R432 *SNP@10K/F_4
PR146 SW@82.5K/F_4
(19) GPU_VID2
PR149 SW@100K_4
PQ44 SW@DMN601K-7
PC122 SW@0.01u/16V_4
Frequency(PR220=200K) 300K
GPU_VID1 GPU_VID2 +VGPU_CORE
0 0 1.035V
1 0 0.95V
0 1 0.85V
1 1 0.8V
For N11P-GE1, please have HW default to 0.95V for NVVDD.
For N11M-GE1, please have HW default to 1.035V for NVVDD.
8792EN
PQ16 SW@DTC144EUA
PR26 SW@1M/F_6
PR31 SW@1M/F_6
PR29 SW@22_8
PQ15 SW@DMN601K-7
12/9 R13042,R13043 move to PWM IC circut page
Quanta Computer Inc.
PROJECT : ZQ3
Size
Document Number
GPU CORE(MAX8792)
Rev 1A
Date: Monday, March 29, 2010
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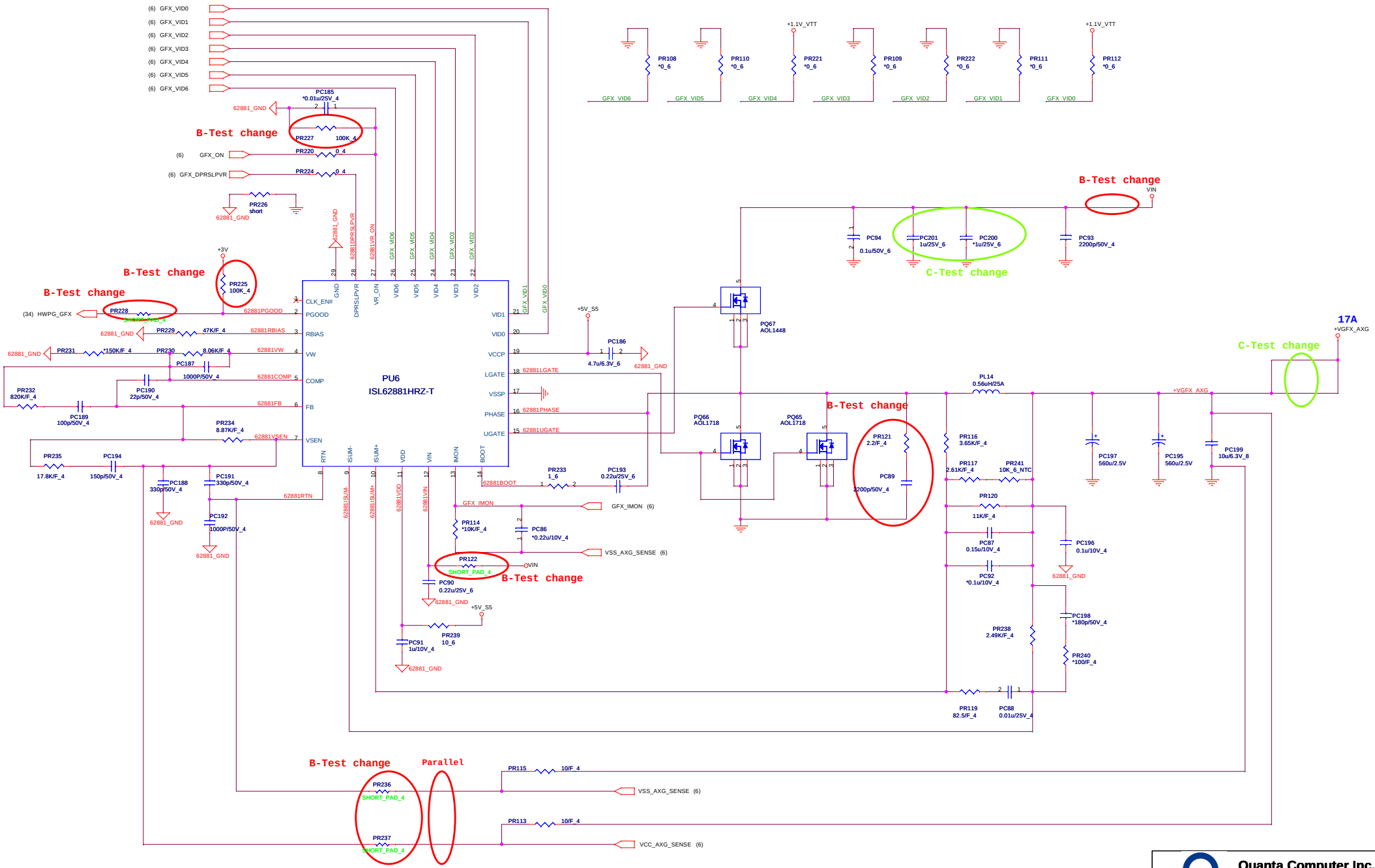
Int_VGA [PWM]



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

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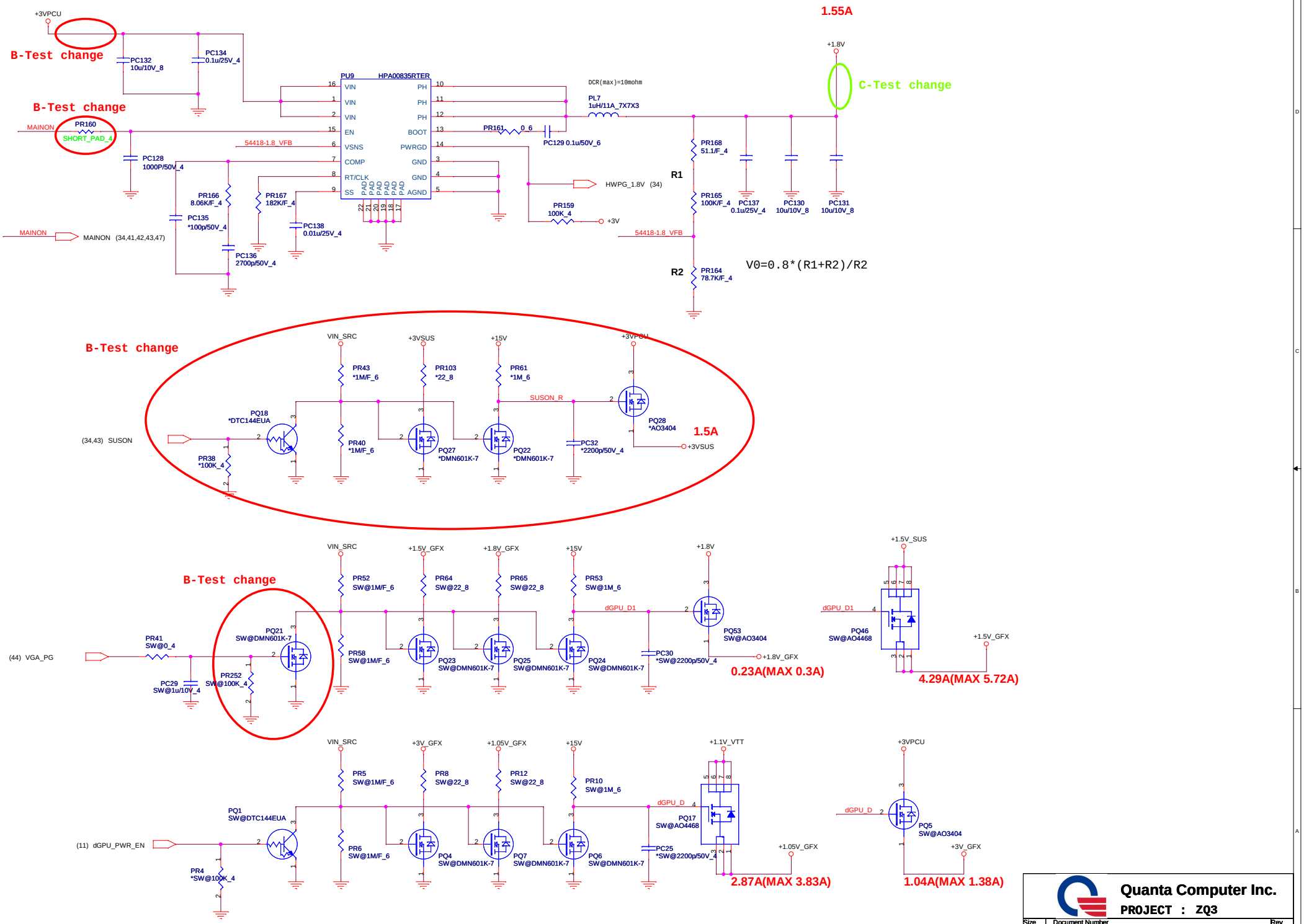
1.55A
B-Test change
C-Test change
+3VPCU
+1.8V
PC132 10u/10V_8
PC134 0.1u/25V_4
PU9 HPA00835RTER
VIN
PH
EN
BOOT
VSNS
PWRGD
COMP
GND
RT/CLK
SS
AGND
PAD
DCR(max)=10mohm
PL7 1uH/11A_7X7X3
PR160 SHORT_PAD_4
MAINON
54418-1.8_VFB
PR161 0_6
PC129 0.1u/50V_6
PC128 1000P/50V_4
PR166 8.06K/F_4
PR167 182K/F_4
PC135 *100p/50V_4
PC136 2700p/50V_4
PC138 0.01u/25V_4
HWPG_1.8V (34)
PR159 100K_4
+3V
R1
R2
PR168 51.1/F_4
PR165 100K/F_4
PR164 78.7K/F_4
PC137 0.1u/25V_4
PC130 10u/10V_8
PC131 10u/10V_8
MAINON (34,41,42,43,47)
V0=0.8*(R1+R2)/R2
B-Test change
VIN_SRC
+3VSUS
+15V
PR43 *1M/F_6
PR103 *22_8
PR61 *1M_6
SUSON_R
PQ18 *DTC144EUA
PQ27 *DMN601K-7
PQ22 *DMN601K-7
PQ28 *AO3404
PR40 *1M/F_6
PR38 *100K_4
PC32 *2200p/50V_4
(34,43) SUSON
1.5A
+3VSUS
B-Test change
VIN_SRC
+1.5V_GFX
+1.8V_GFX
+15V
+1.8V
PR52 SW@1M/F_6
PR64 SW@22_8
PR65 SW@22_8
PR53 SW@1M_6
dGPU_D1
PQ21 SW@DMN601K-7
PQ23 SW@DMN601K-7
PQ25 SW@DMN601K-7
PQ24 SW@DMN601K-7
PQ53 SW@AO3404
PR41 SW@0_4
PR58 SW@1M/F_6
PR252 SW@100K_4
PC29 SW@1u/10V_4
PC30 *SW@2200p/50V_4
(44) VGA_PG
+1.8V_GFX
0.23A(MAX 0.3A)
+1.5V_SUS
dGPU_D1
PQ46 SW@AO4468
+1.5V_GFX
4.29A(MAX 5.72A)
VIN_SRC
+3V_GFX
+1.05V_GFX
+15V
+1.1V_VTT
PR5 SW@1M/F_6
PR8 SW@22_8
PR12 SW@22_8
PR10 SW@1M_6
dGPU_D
PQ1 SW@DTC144EUA
PQ4 SW@DMN601K-7
PQ7 SW@DMN601K-7
PQ6 SW@DMN601K-7
PQ17 SW@AO4468
PR6 SW@1M/F_6
PR4 *SW@100K_4
PC25 *SW@2200p/50V_4
(11) dGPU_PWR_EN
+1.05V_GFX
2.87A(MAX 3.83A)
+3VPCU
dGPU_D
PQ5 SW@AO3404
+3V_GFX
1.04A(MAX 1.38A)
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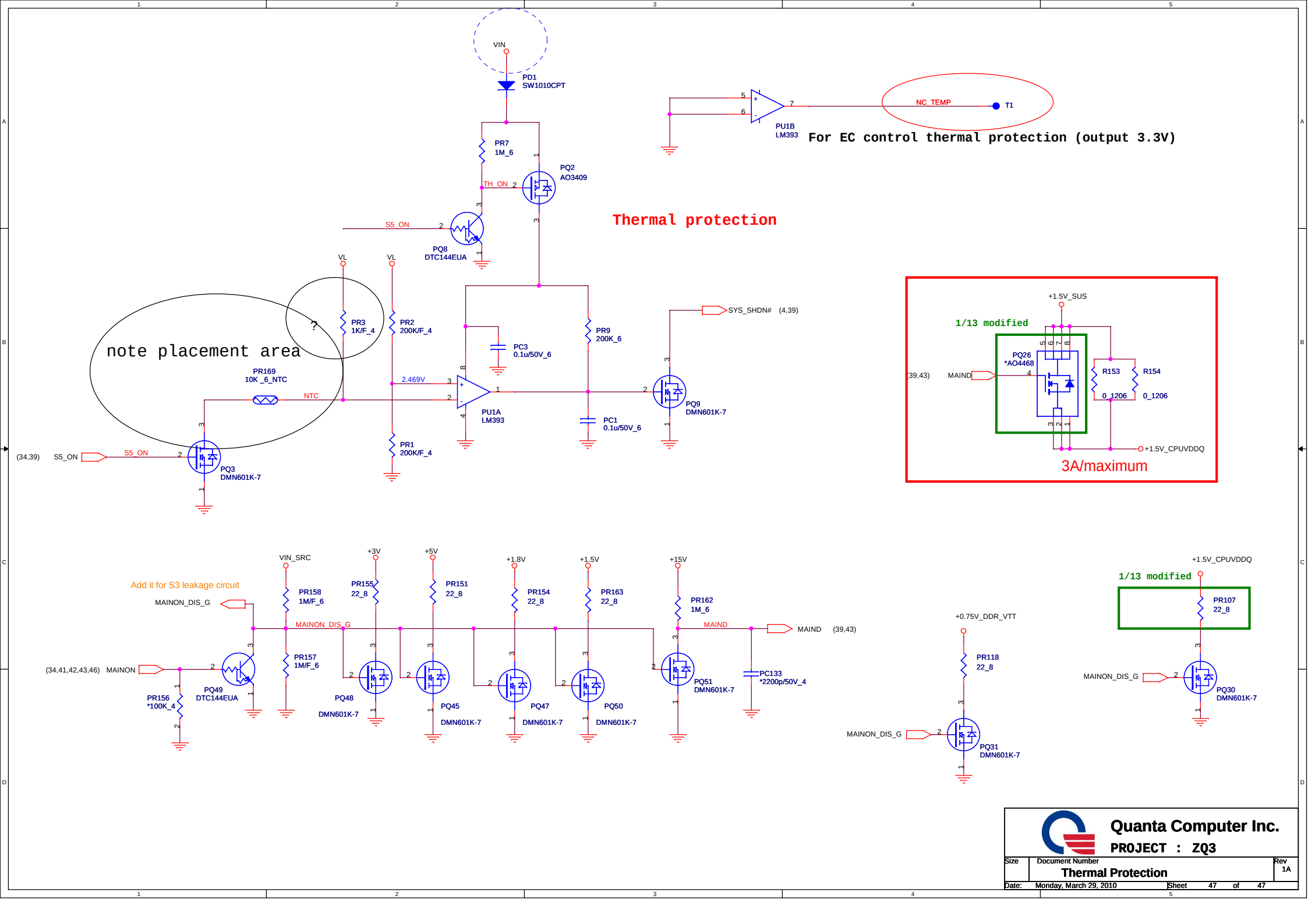

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