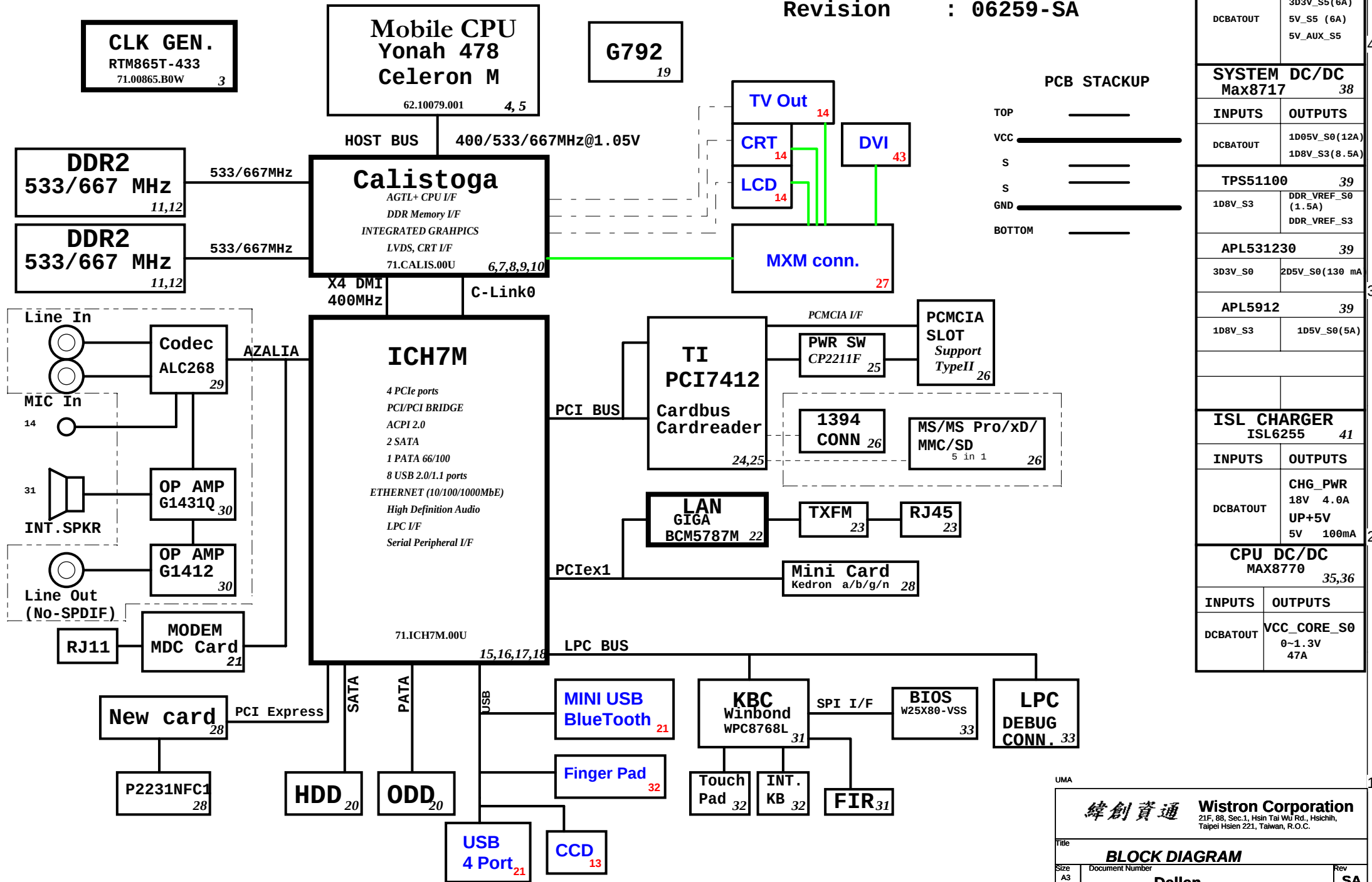


Dellen Block Diagram

Project code: 91.4V401.001
PCB P/N : 48.4T307.0SA
Revision : 06259-SA



ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN,EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS,SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], D10W#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSusi_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSusi_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	FingerPad
5	BlueTooth
6	CCD
7	NewCard

Calistoga Strapping Signals and Configuration

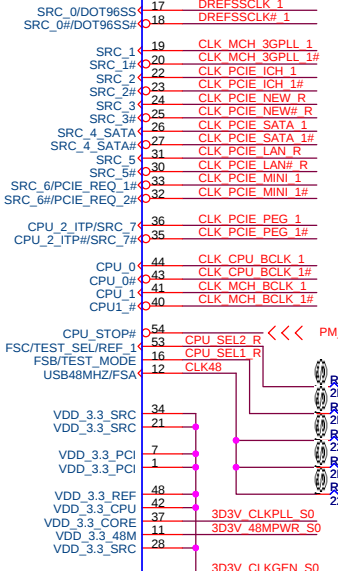
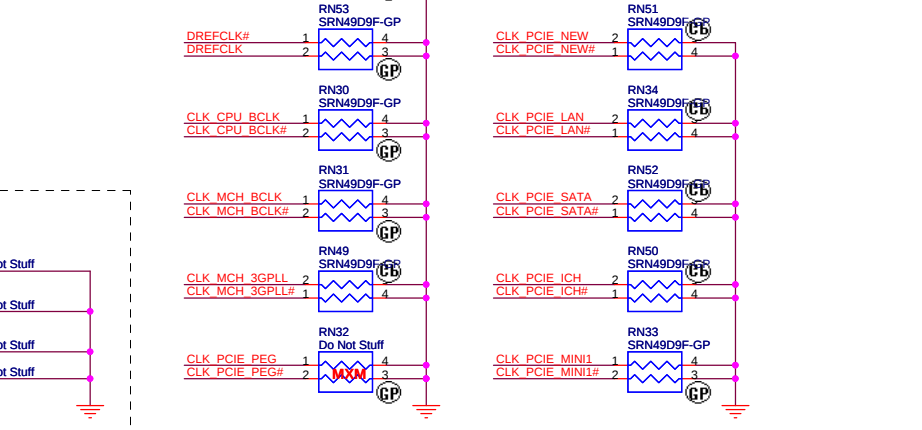
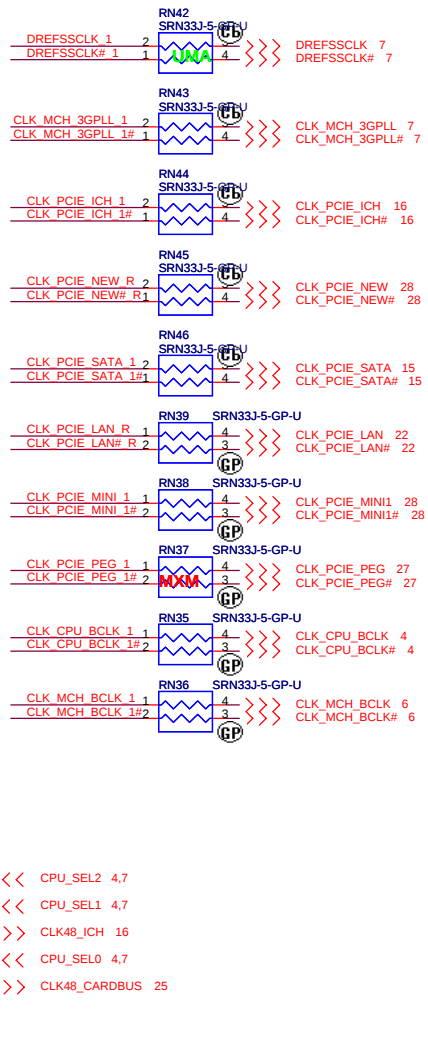
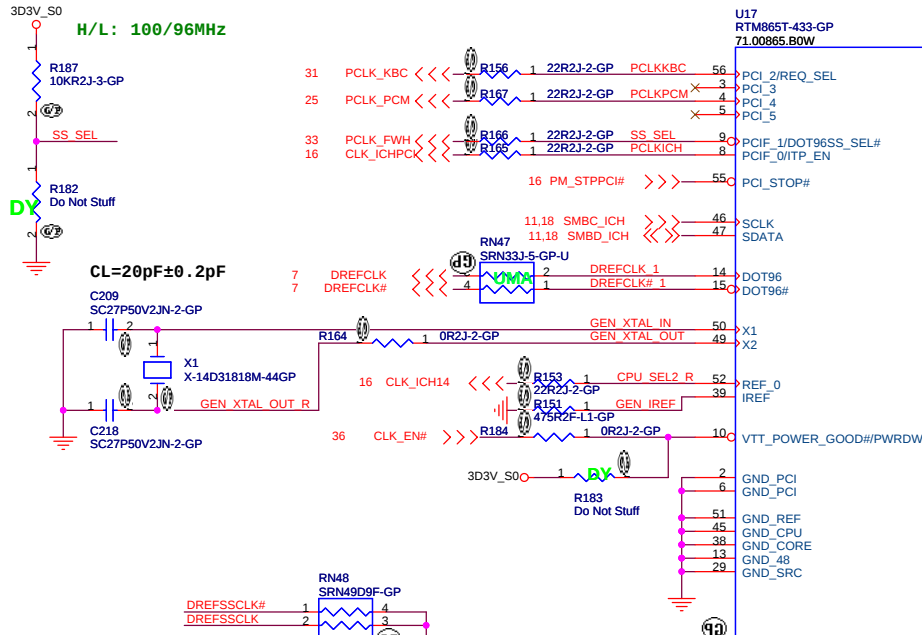
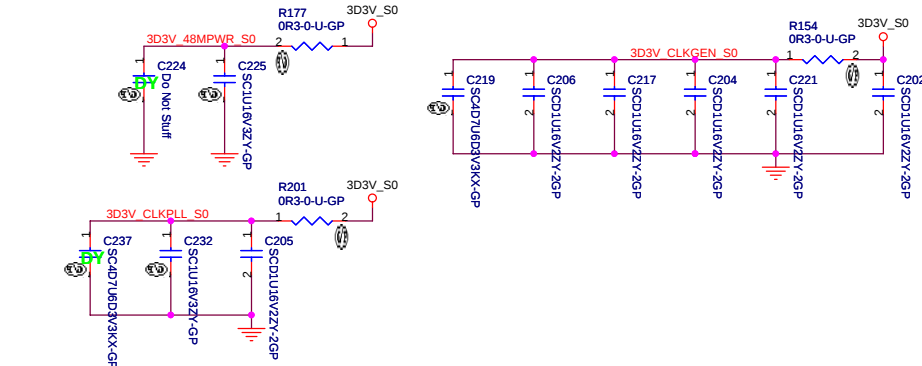
EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

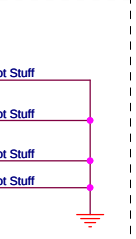
NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORX in signal.

UMA

緯創資通		Wistron Corporation		
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title				
Reference				
Size A3	Document Number		Rev	
	Dellen		SA	
Date: Tuesday, January 16, 2007				
Sheet 2 of 43				



FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	333M	X
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

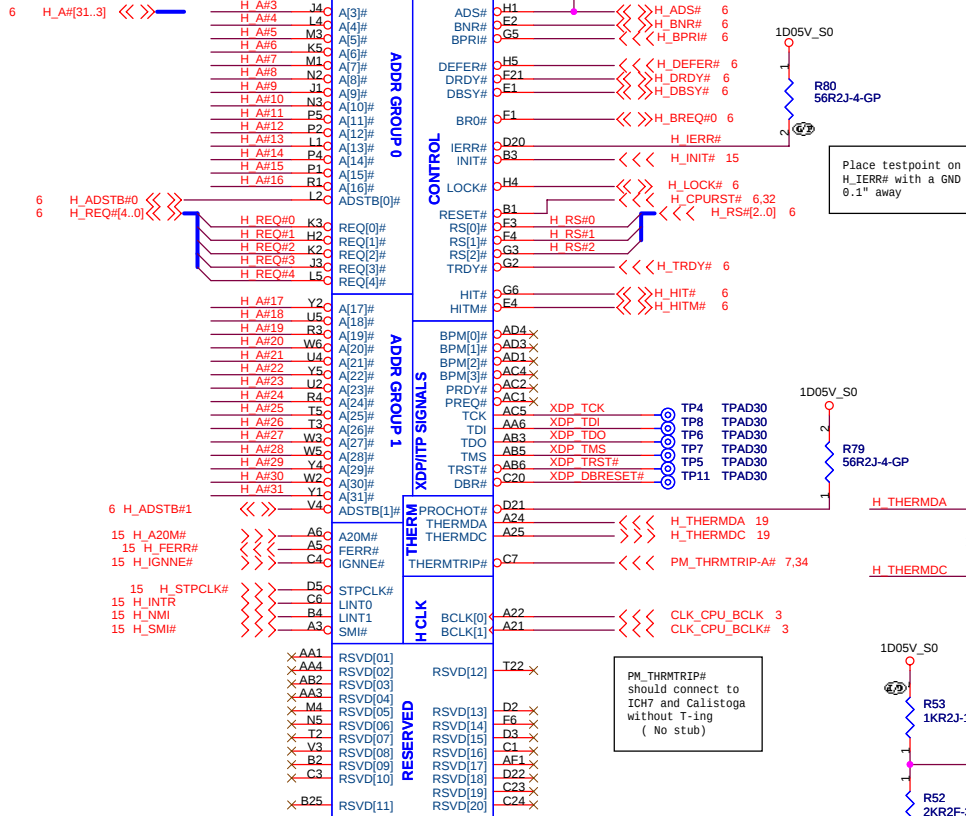
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Size A3 Document Number **Dellen** Rev SA

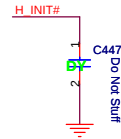
Date: Tuesday, January 16, 2007 Sheet 3 of 43

2nd source: 62.10053.401

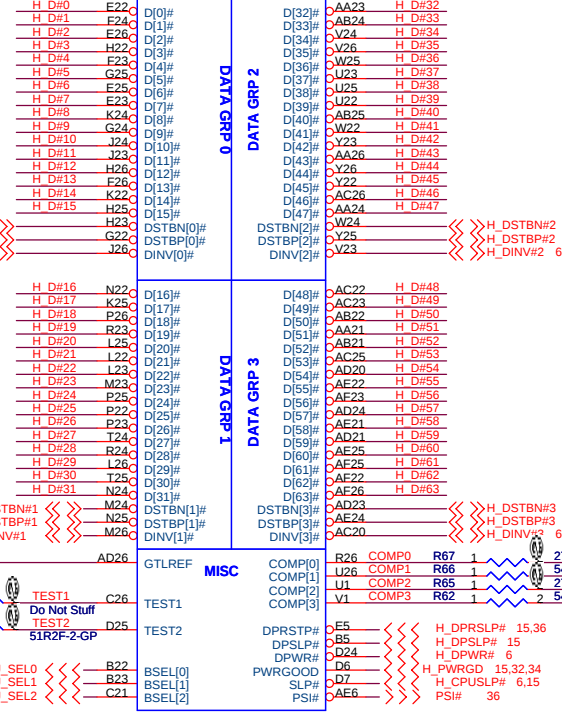
U41A
BGA479-SKT6-GPU3
62.10079.001



Layout Note:
0.5" max length.



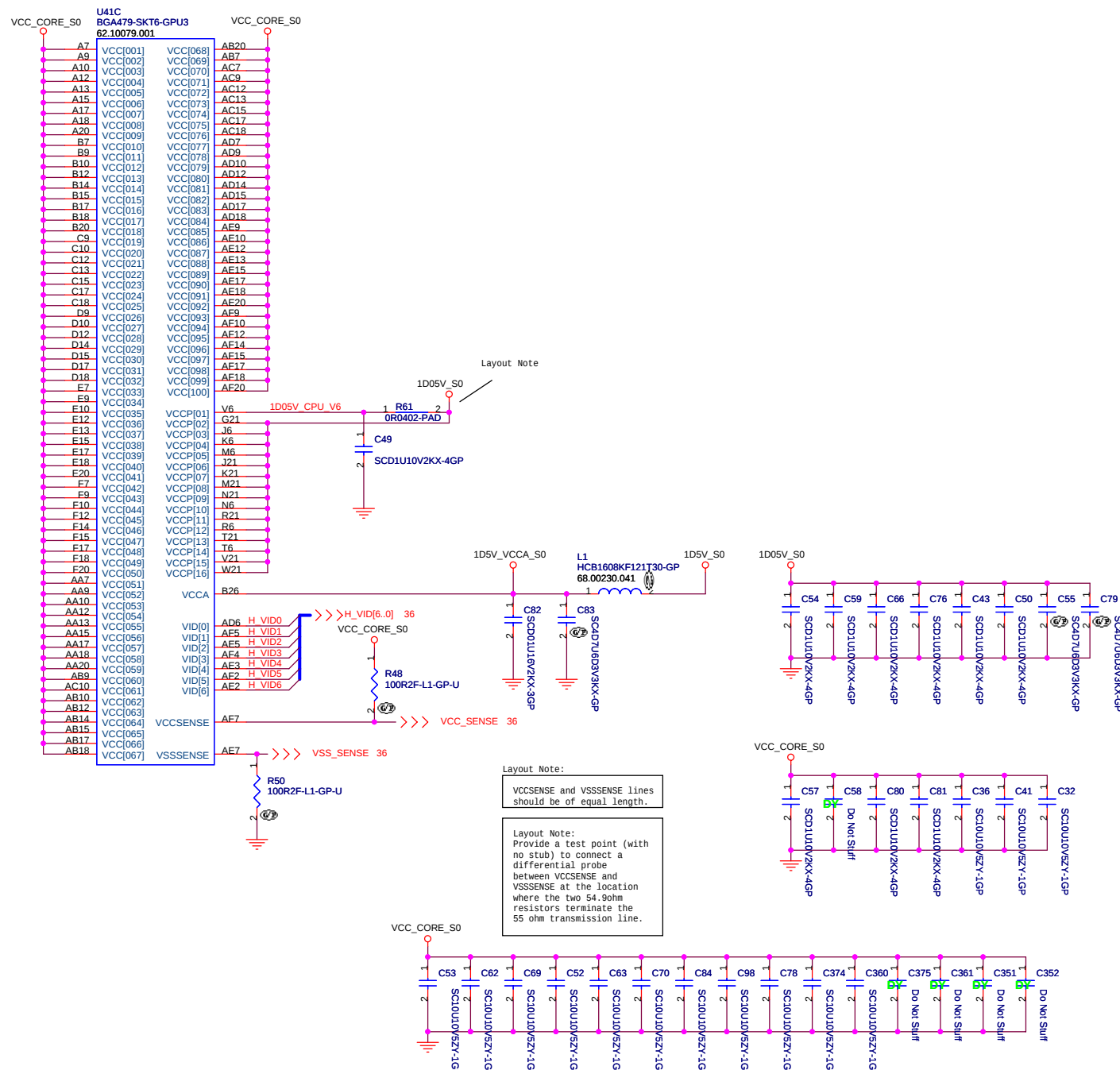
U41B
BGA479-SKT6-GPU3
62.10079.001



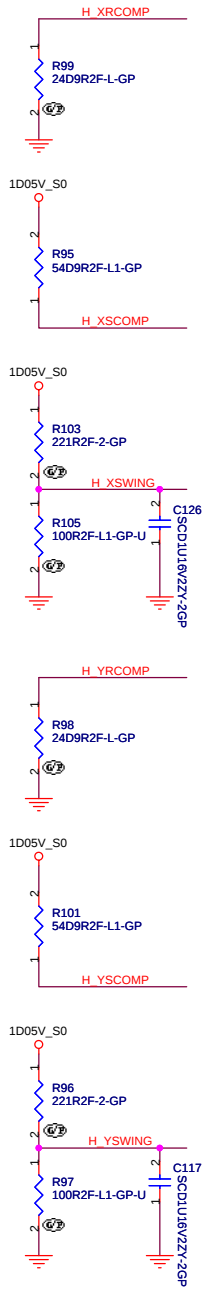
Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make
trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make
trace length shorter than 0.5" .

UMA

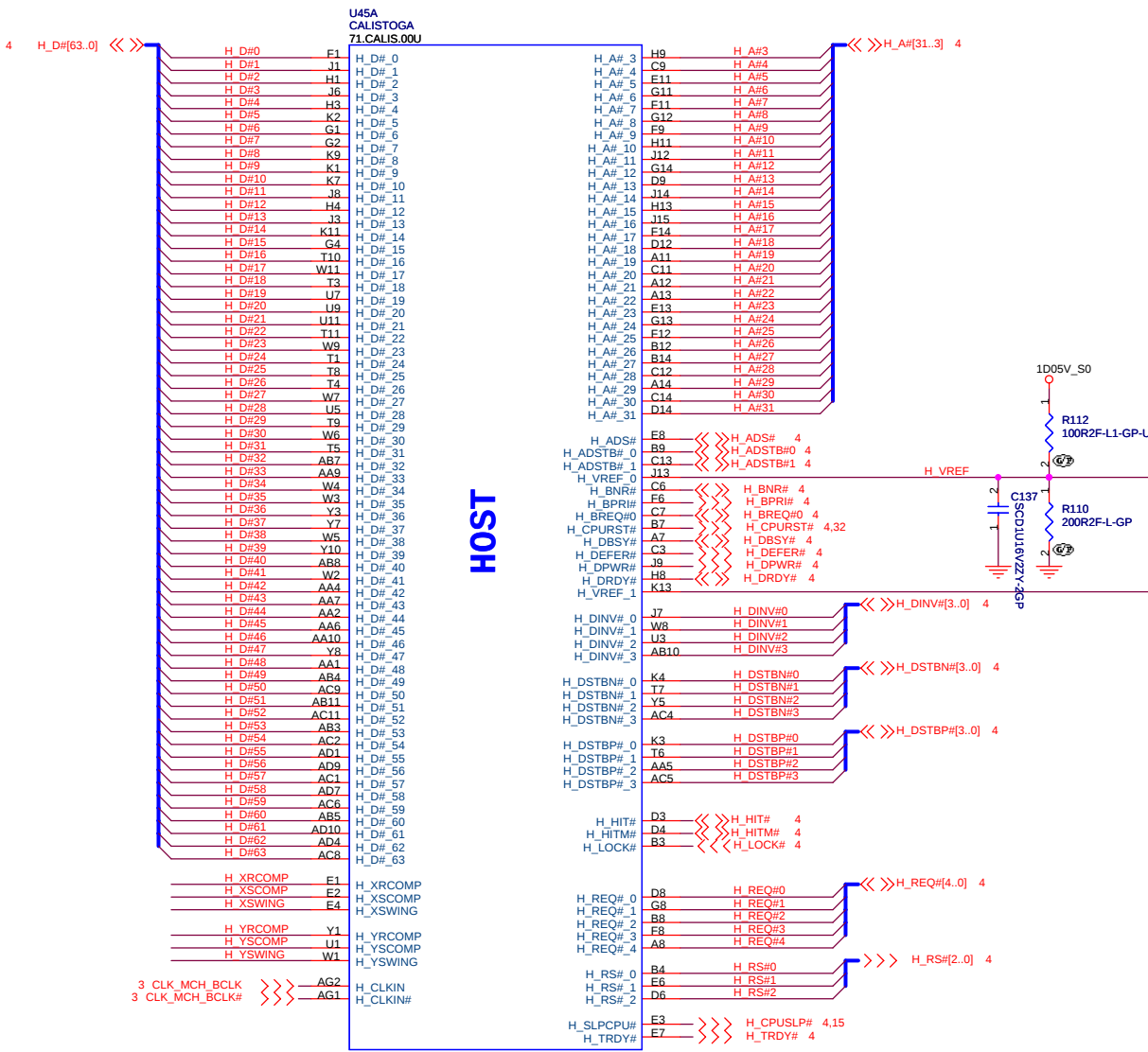
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.



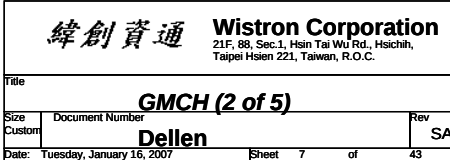
U1D1 BG4A7-SKT6-GP-U3 62.10079.001		
A4	VSS[001]	VSS[082]
A8	VSS[002]	VSS[083]
A11	VSS[003]	VSS[084]
A14	VSS[004]	VSS[085]
A16	VSS[005]	VSS[086]
A23	VSS[006]	VSS[087]
A26	VSS[007]	VSS[088]
A26	VSS[008]	VSS[089]
B6	VSS[009]	VSS[090]
B8	VSS[010]	VSS[091]
B11	VSS[011]	VSS[092]
B13	VSS[012]	VSS[093]
B16	VSS[013]	VSS[094]
B19	VSS[014]	VSS[095]
B21	VSS[015]	VSS[096]
B24	VSS[016]	VSS[097]
C5	VSS[017]	VSS[098]
C8	VSS[018]	VSS[099]
C11	VSS[019]	VSS[100]
C14	VSS[020]	VSS[101]
C16	VSS[021]	VSS[102]
C19	VSS[022]	VSS[103]
C22	VSS[023]	VSS[104]
C25	VSS[024]	VSS[105]
D1	VSS[025]	VSS[106]
D4	VSS[026]	VSS[107]
D8	VSS[027]	VSS[108]
D8	VSS[028]	VSS[109]
D11	VSS[029]	VSS[110]
D16	VSS[030]	VSS[111]
D19	VSS[031]	VSS[112]
D19	VSS[032]	VSS[113]
D23	VSS[033]	VSS[114]
D26	VSS[034]	VSS[115]
E3	VSS[035]	VSS[116]
E6	VSS[036]	VSS[117]
E8	VSS[037]	VSS[118]
E11	VSS[038]	VSS[119]
E14	VSS[039]	VSS[120]
E16	VSS[040]	VSS[121]
E19	VSS[041]	VSS[122]
E21	VSS[042]	VSS[123]
E24	VSS[043]	VSS[124]
F8	VSS[044]	VSS[125]
F11	VSS[045]	VSS[126]
F13	VSS[046]	VSS[127]
F16	VSS[047]	VSS[128]
F19	VSS[048]	VSS[129]
F22	VSS[049]	VSS[130]
F22	VSS[050]	VSS[131]
F25	VSS[051]	VSS[132]
G4	VSS[052]	VSS[133]
G5	VSS[053]	VSS[134]
G1	VSS[054]	VSS[135]
G23	VSS[055]	VSS[136]
H3	VSS[056]	VSS[137]
H6	VSS[057]	VSS[138]
H21	VSS[058]	VSS[139]
H24	VSS[059]	VSS[140]
H24	VSS[060]	VSS[141]
J2	VSS[061]	VSS[142]
J22	VSS[062]	VSS[143]
J25	VSS[063]	VSS[144]
K1	VSS[064]	VSS[145]
K4	VSS[065]	VSS[146]
K4	VSS[066]	VSS[147]
K23	VSS[067]	VSS[148]
K26	VSS[068]	VSS[149]
L1	VSS[069]	VSS[150]
L21	VSS[070]	VSS[151]
L24	VSS[071]	VSS[152]
M2	VSS[072]	VSS[153]
M2	VSS[073]	VSS[154]
M5	VSS[074]	VSS[155]
M22	VSS[075]	VSS[156]
M25	VSS[076]	VSS[157]
N1	VSS[077]	VSS[158]
N4	VSS[078]	VSS[159]
N23	VSS[079]	VSS[160]
N26	VSS[080]	VSS[161]
P3	VSS[081]	VSS[162]



Place them near to the chip (< 0.5")



DIS : KI.94501.006
UMA : 943GML P/N is 71.00943.M01



11 M_A_DQ[63.0] << >>

U45D
CALISTOGA
71.CALIS.00U

M A DQ0	AJ35	SA DQ0
M A DQ1	AJ34	SA DQ1
M A DQ2	AM31	SA DQ2
M A DQ3	AM33	SA DQ3
M A DQ4	AJ36	SA DQ4
M A DQ5	AK35	SA DQ5
M A DQ6	AJ32	SA DQ6
M A DQ7	AH31	SA DQ7
M A DQ8	AN35	SA DQ8
M A DQ9	AP33	SA DQ9
M A DQ10	AR31	SA DQ10
M A DQ11	AP31	SA DQ11
M A DQ12	AN38	SA DQ12
M A DQ13	AM36	SA DQ13
M A DQ14	AM34	SA DQ14
M A DQ15	AN33	SA DQ15
M A DQ16	AK26	SA DQ16
M A DQ17	AL27	SA DQ17
M A DQ18	AM26	SA DQ18
M A DQ19	AN24	SA DQ19
M A DQ20	AK23	SA DQ20
M A DQ21	AL28	SA DQ21
M A DQ22	AM24	SA DQ22
M A DQ23	AP26	SA DQ23
M A DQ24	AP23	SA DQ24
M A DQ25	AL22	SA DQ25
M A DQ26	AP21	SA DQ26
M A DQ27	AN20	SA DQ27
M A DQ28	AL23	SA DQ28
M A DQ29	AP24	SA DQ29
M A DQ30	AP20	SA DQ30
M A DQ31	AT21	SA DQ31
M A DQ32	AR12	SA DQ32
M A DQ33	AR14	SA DQ33
M A DQ34	AP13	SA DQ34
M A DQ35	AP12	SA DQ35
M A DQ36	AT13	SA DQ36
M A DQ37	AT12	SA DQ37
M A DQ38	AL14	SA DQ38
M A DQ39	AL12	SA DQ39
M A DQ40	AK9	SA DQ40
M A DQ41	AN7	SA DQ41
M A DQ42	AK8	SA DQ42
M A DQ43	AK7	SA DQ43
M A DQ44	AP9	SA DQ44
M A DQ45	AT5	SA DQ45
M A DQ46	AL5	SA DQ46
M A DQ47	AY2	SA DQ47
M A DQ48	AW2	SA DQ48
M A DQ49	AP1	SA DQ49
M A DQ50	AN2	SA DQ50
M A DQ51	AV2	SA DQ51
M A DQ52	AT3	SA DQ52
M A DQ53	AN1	SA DQ53
M A DQ54	AL2	SA DQ54
M A DQ55	AG7	SA DQ55
M A DQ56	AF9	SA DQ56
M A DQ57	AG4	SA DQ57
M A DQ58	AF6	SA DQ58
M A DQ59	AG9	SA DQ59
M A DQ60	AH6	SA DQ60
M A DQ61	AF4	SA DQ61
M A DQ62	AF4	SA DQ62
M A DQ63	AF8	SA DQ63

DDR SYSTEM MEMORY A

SA_BS_0	AU12	M A BS#0 11.12
SA_BS_1	AV14	M A BS#1 11.12
SA_BS_2	BA20	M A BS#2 11.12
SA_BS_2		M A CAS# 11.12
SA_BS_2		M A_DM[7.0] 11
SA_CAS#	AY13	
SA_DM_0	AJ33	M A DM0
SA_DM_1	AM35	M A DM1
SA_DM_2	AL26	M A DM2
SA_DM_3	AN22	M A DM3
SA_DM_4	AM14	M A DM4
SA_DM_5	AL9	M A DM5
SA_DM_6	AR3	M A DM6
SA_DM_7	AH4	M A DM7
SA_DQS_0	AK33	M A DQS0
SA_DQS_1	AT33	M A DQS1
SA_DQS_2	AN28	M A DQS2
SA_DQS_3	AM22	M A DQS3
SA_DQS_4	AN12	M A DQS4
SA_DQS_5	AN8	M A DQS5
SA_DQS_6	AP3	M A DQS6
SA_DQS_7	AG5	M A DQS7
SA_DQS#_0	AK32	M A DQS#0
SA_DQS#_1	AU33	M A DQS#1
SA_DQS#_2	AN27	M A DQS#2
SA_DQS#_3	AM21	M A DQS#3
SA_DQS#_4	AM12	M A DQS#4
SA_DQS#_5	AL8	M A DQS#5
SA_DQS#_6	AN3	M A DQS#6
SA_DQS#_7	AH5	M A DQS#7
SA_MA_0	AY16	M A A0
SA_MA_1	AU14	M A A1
SA_MA_2	AW16	M A A2
SA_MA_3	BA16	M A A3
SA_MA_4	BA17	M A A4
SA_MA_5	AU16	M A A5
SA_MA_6	AV17	M A A6
SA_MA_7	AU17	M A A7
SA_MA_8	AT16	M A A8
SA_MA_9	AU13	M A A9
SA_MA_10	AT17	M A A10
SA_MA_11	AV20	M A A11
SA_MA_12	AV12	M A A12
SA_MA_13	AV12	M A A13
SA_RAS#	AW14	M A_RAS# 11.12
SA_RCVENIN#	AK23	SA RCVENIN#
SA_RCVENOUT#	AK24	SA RCVENOUT#
SA_WE#	AY14	M A_WE# 11.12

Place Test PAD Near to Chip
as could as possible

11 M_B_DQ[63.0] << >>

U45E
CALISTOGA
71.CALIS.00U

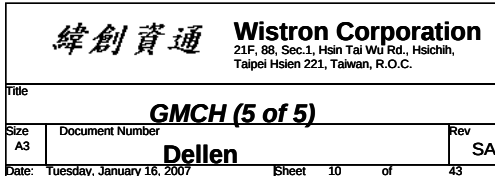
M B DQ0	AK39	SB DQ0
M B DQ1	AJ37	SB DQ1
M B DQ2	AP39	SB DQ2
M B DQ3	AR41	SB DQ3
M B DQ4	AJ38	SB DQ4
M B DQ5	AK38	SB DQ5
M B DQ6	AN41	SB DQ6
M B DQ7	AP41	SB DQ7
M B DQ8	AT40	SB DQ8
M B DQ9	AV41	SB DQ9
M B DQ10	AU38	SB DQ10
M B DQ11	AV38	SB DQ11
M B DQ12	AP38	SB DQ12
M B DQ13	AR40	SB DQ13
M B DQ14	AW38	SB DQ14
M B DQ15	AY38	SB DQ15
M B DQ16	BA38	SB DQ16
M B DQ17	AV36	SB DQ17
M B DQ18	AR36	SB DQ18
M B DQ19	AP36	SB DQ19
M B DQ20	BA36	SB DQ20
M B DQ21	AU36	SB DQ21
M B DQ22	AP34	SB DQ22
M B DQ23	AP34	SB DQ23
M B DQ24	AY33	SB DQ24
M B DQ25	BA33	SB DQ25
M B DQ26	AT31	SB DQ26
M B DQ27	AU29	SB DQ27
M B DQ28	AU31	SB DQ28
M B DQ29	AW31	SB DQ29
M B DQ30	AV29	SB DQ30
M B DQ31	AW29	SB DQ31
M B DQ32	AM19	SB DQ32
M B DQ33	AL19	SB DQ33
M B DQ34	AP14	SB DQ34
M B DQ35	AN14	SB DQ35
M B DQ36	AN17	SB DQ36
M B DQ37	AM16	SB DQ37
M B DQ38	AP15	SB DQ38
M B DQ39	AL15	SB DQ39
M B DQ40	AJ11	SB DQ40
M B DQ41	AH10	SB DQ41
M B DQ42	AJ9	SB DQ42
M B DQ43	AN10	SB DQ43
M B DQ44	AK13	SB DQ44
M B DQ45	AH11	SB DQ45
M B DQ46	AK10	SB DQ46
M B DQ47	AJ8	SB DQ47
M B DQ48	BA10	SB DQ48
M B DQ49	AW10	SB DQ49
M B DQ50	BA4	SB DQ50
M B DQ51	AW4	SB DQ51
M B DQ52	AY10	SB DQ52
M B DQ53	AY9	SB DQ53
M B DQ54	AY5	SB DQ54
M B DQ55	AV4	SB DQ55
M B DQ56	AR5	SB DQ56
M B DQ57	AK4	SB DQ57
M B DQ58	AK3	SB DQ58
M B DQ59	AT4	SB DQ59
M B DQ60	AK5	SB DQ60
M B DQ61	AJ5	SB DQ61
M B DQ62	AJ3	SB DQ62
M B DQ63	AJ3	SB DQ63

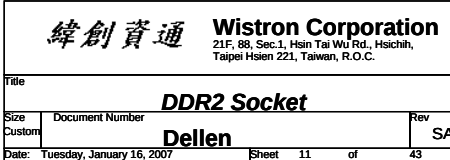
DDR SYSTEM MEMORY B

SB_BS_0	AT24	M B BS#0 11.12
SB_BS_1	AV23	M B BS#1 11.12
SB_BS_2	AY28	M B BS#2 11.12
SB_BS_2		M B CAS# 11.12
SB_BS_2		M B_DM[7.0] 11
SB_CAS#	AR24	
SB_DM_0	AK36	M B DM0
SB_DM_1	AR38	M B DM1
SB_DM_2	AT36	M B DM2
SB_DM_3	BA31	M B DM3
SB_DM_4	AL17	M B DM4
SB_DM_5	AH8	M B DM5
SB_DM_6	BA5	M B DM6
SB_DM_7	AN4	M B DM7
SB_DQS_0	AM39	M B DQS0
SB_DQS_1	AT39	M B DQS1
SB_DQS_2	AU35	M B DQS2
SB_DQS_3	AR29	M B DQS3
SB_DQS_4	AR16	M B DQS4
SB_DQS_5	AR10	M B DQS5
SB_DQS_6	AR7	M B DQS6
SB_DQS_7	AN5	M B DQS7
SB_DQS#_0	AM40	M B DQS#0
SB_DQS#_1	AU39	M B DQS#1
SB_DQS#_2	AT35	M B DQS#2
SB_DQS#_3	AP29	M B DQS#3
SB_DQS#_4	AP16	M B DQS#4
SB_DQS#_5	AT10	M B DQS#5
SB_DQS#_6	AT7	M B DQS#6
SB_DQS#_7	AP5	M B DQS#7
SB_MA_0	AY23	M B A0
SB_MA_1	AW24	M B A1
SB_MA_2	AY24	M B A2
SB_MA_3	AR28	M B A3
SB_MA_4	AT27	M B A4
SB_MA_5	AT28	M B A5
SB_MA_6	AU27	M B A6
SB_MA_7	AV28	M B A7
SB_MA_8	AV27	M B A8
SB_MA_9	AW27	M B A9
SB_MA_10	AV24	M B A10
SB_MA_11	BA27	M B A11
SB_MA_12	AY27	M B A12
SB_MA_13	AR23	M B A13
SB_RAS#	AU23	M_B_RAS# 11.12
SB_RCVENIN#	AK18	SB RCVENIN#
SB_RCVENOUT#	AK18	SB RCVENOUT#
SB_WE#	AR27	M_B_WE# 11.12

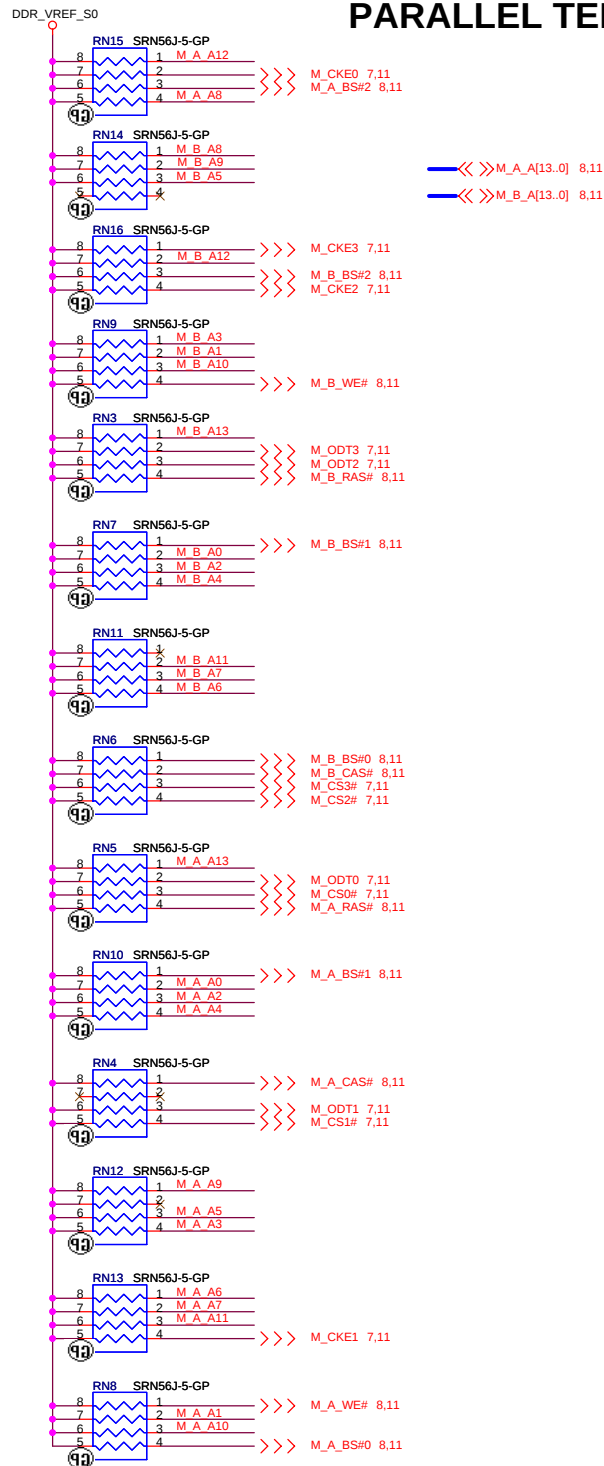
Place Test PAD Near to Chip
as could as possible

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Taipei Hsien 221, Taiwan, R.O.C.

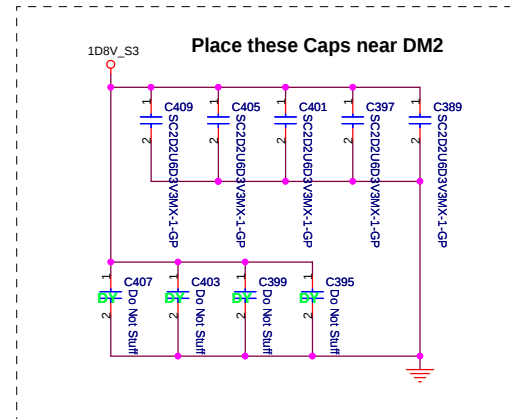
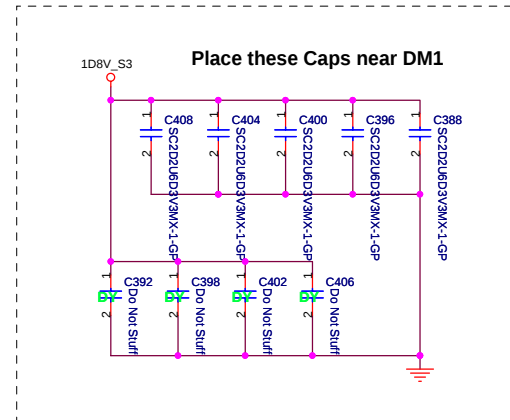
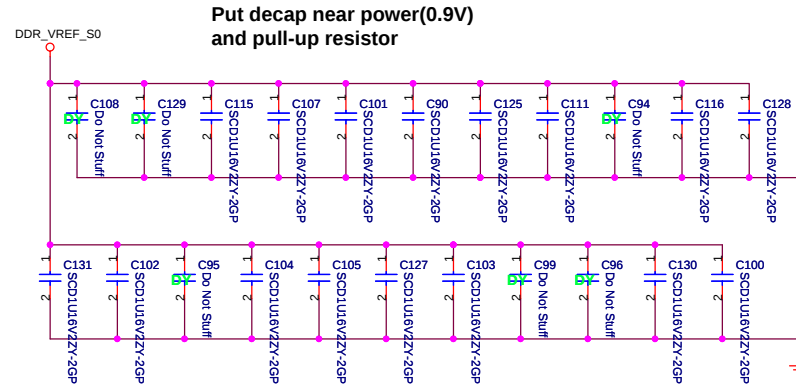


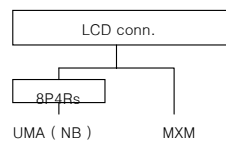
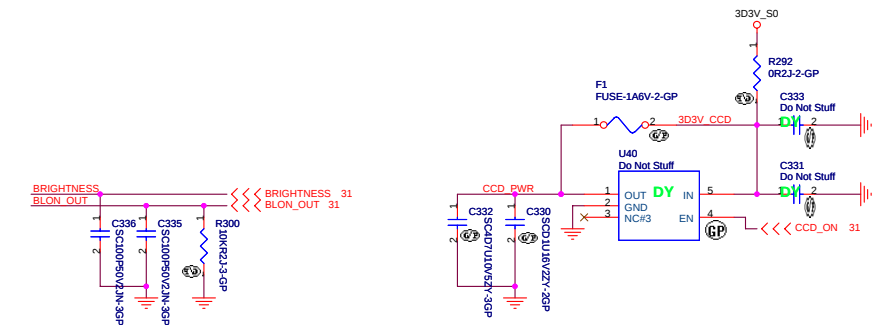
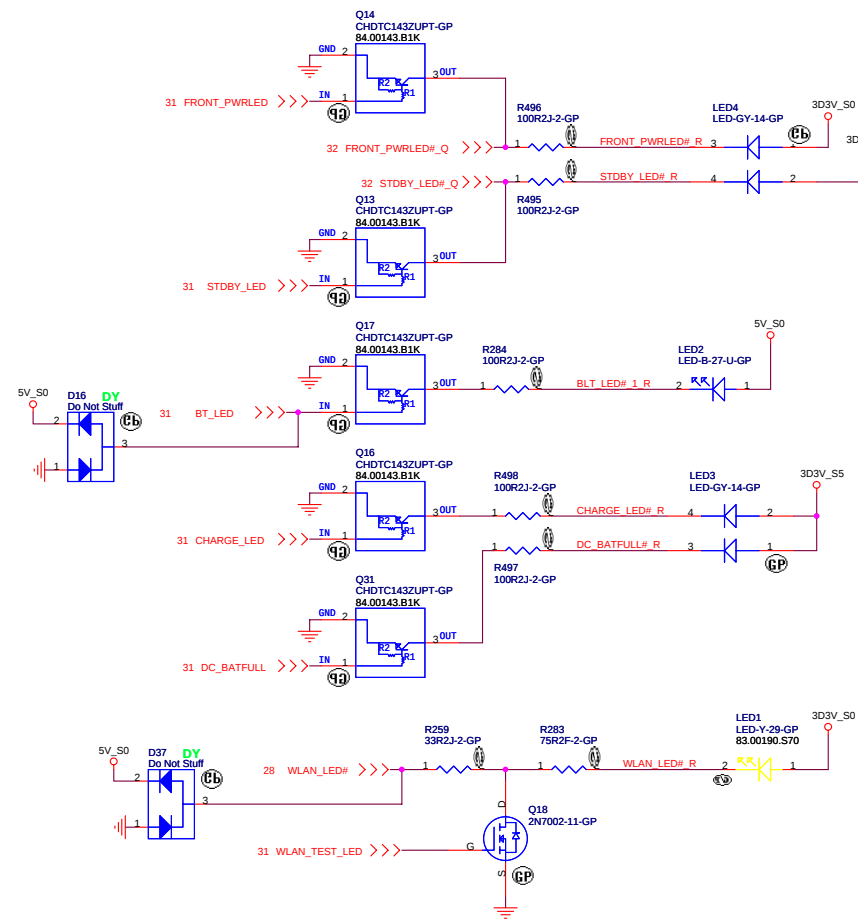
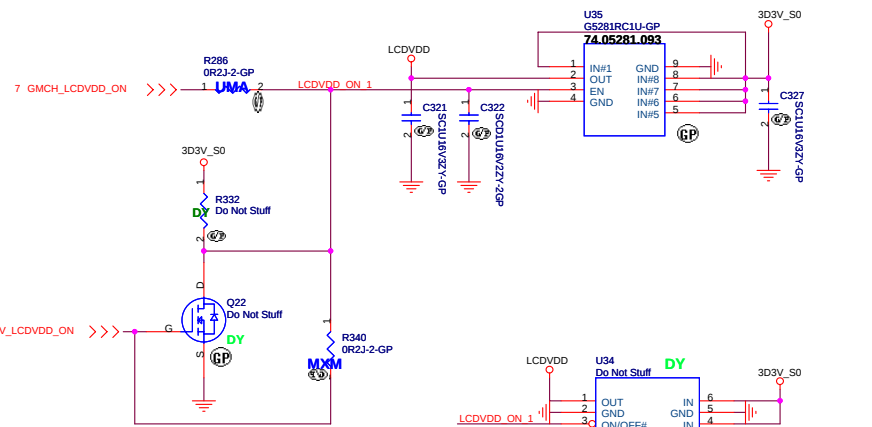


PARALLEL TERMINATION

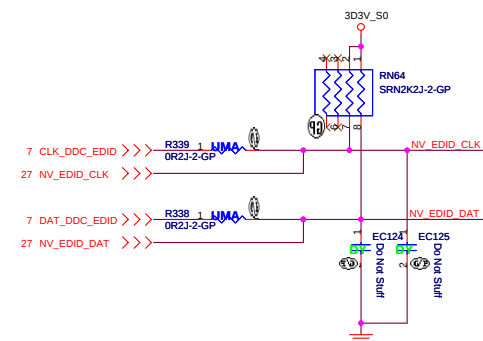
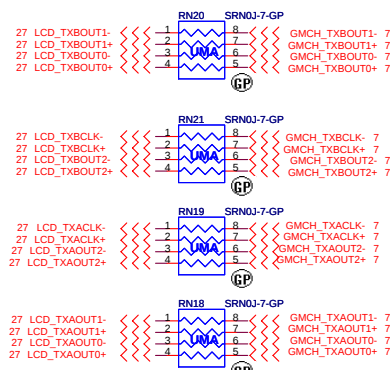
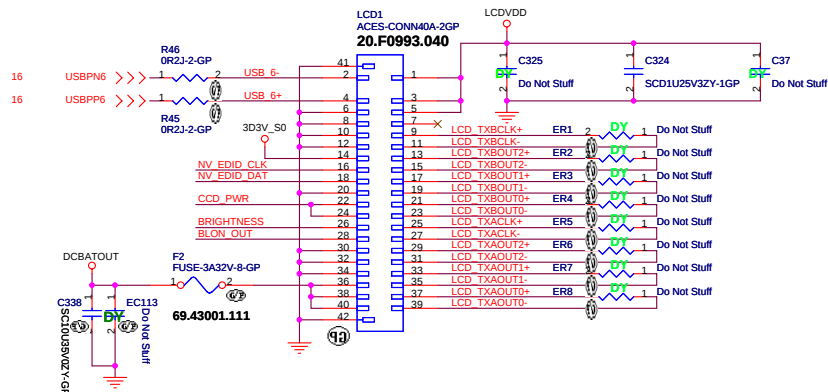


Decoupling Capacitor





LCD / Inverter conn.

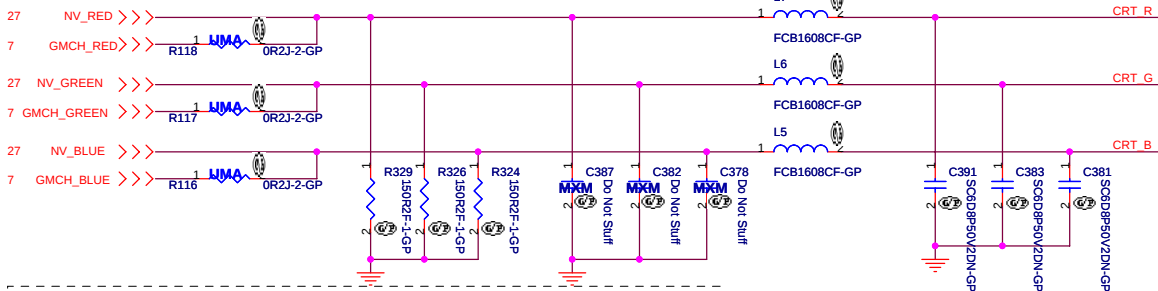


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Title LCD CONN & LED	
Size Custom	Document Number Dellen
Date Tuesday, January 16, 2007	Sheet 13 of 43

Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 10 ohm@100MHz

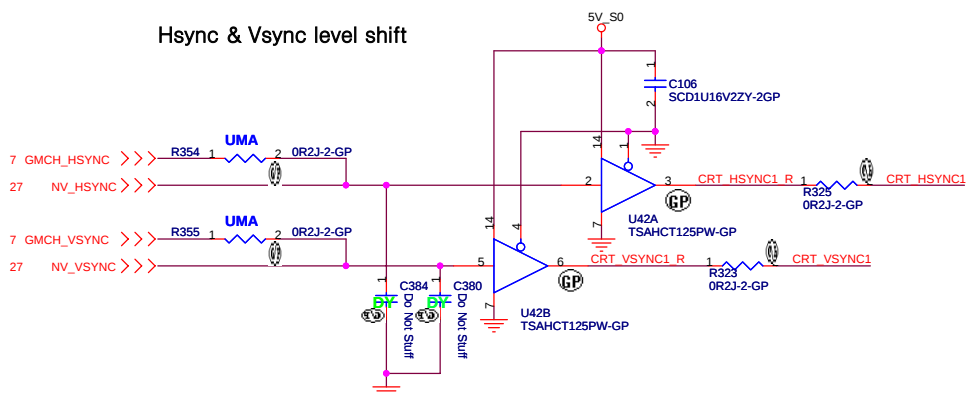
CRT I/F & connector



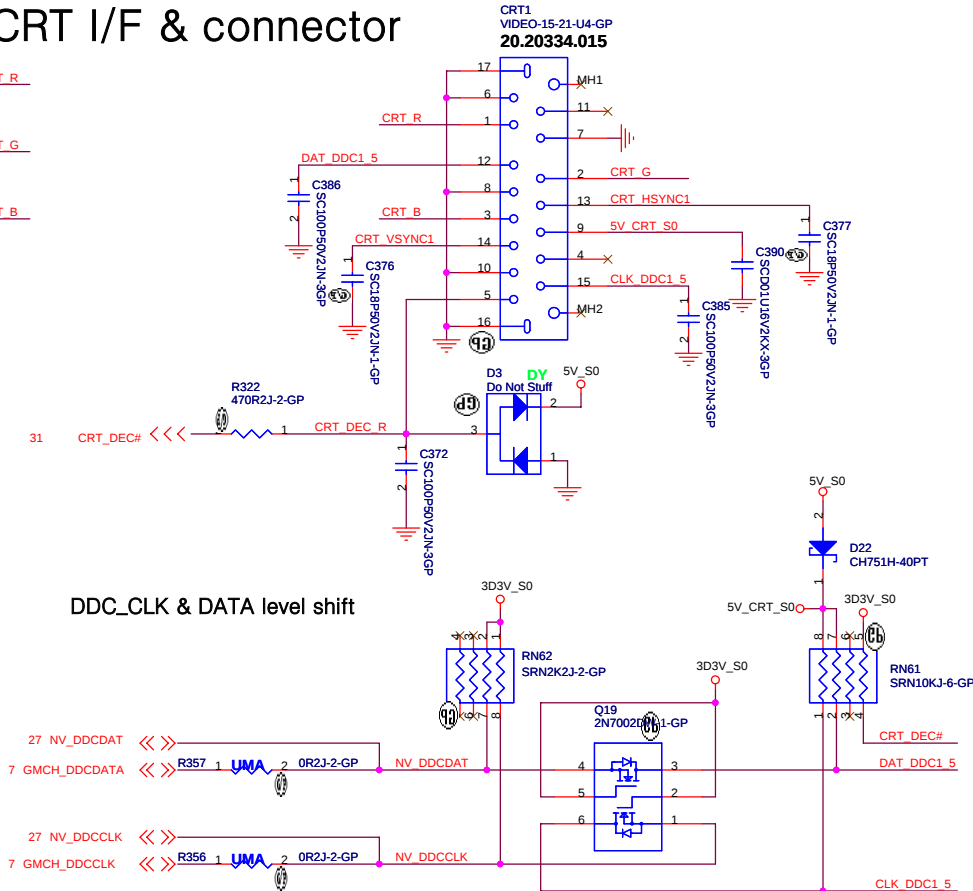
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

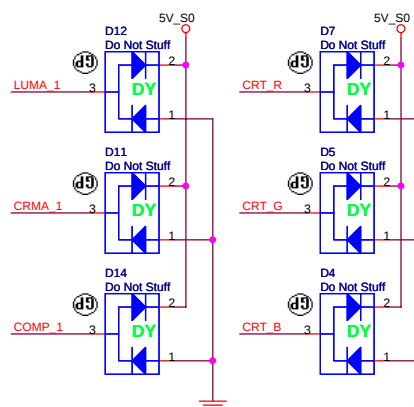
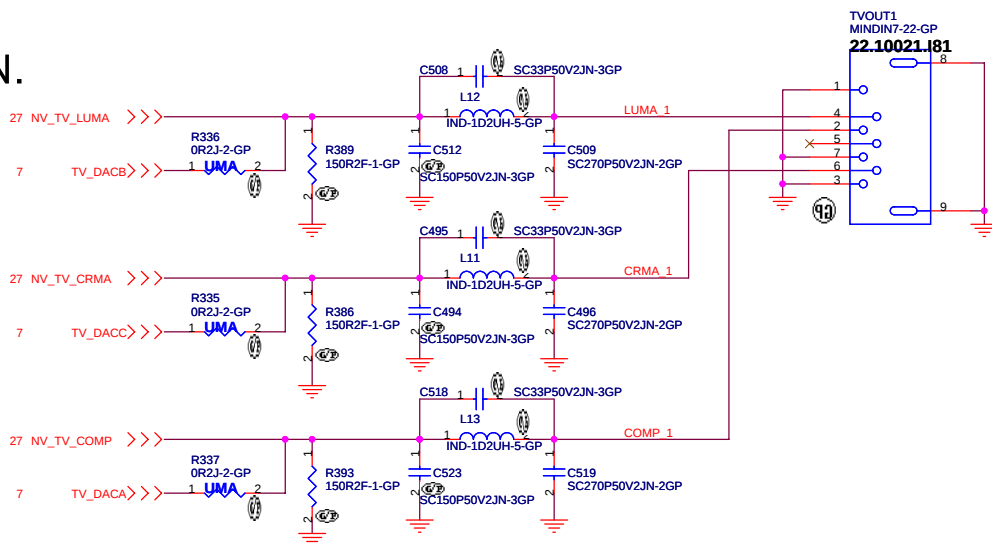
Hsync & Vsync level shift



DDC_CLK & DATA level shift



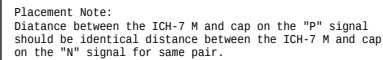
TV CONN.



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Title			CRT/TV Connector	
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Date:	Tuesday, January 16, 2007	Sheet	14	of 43

RTC1
BAT-CON2-1-GP
62.70001.011



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ICH7-M (1 of 4)

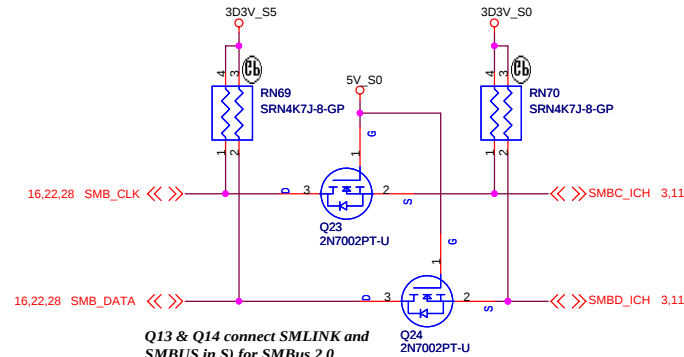
Dellen

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SA

U15E ICH7-M-GP 71.ICH7M.00U		
A4	VSS[1]	VSS[98]
A23	VSS[2]	VSS[99]
B1	VSS[3]	VSS[100]
B8	VSS[4]	VSS[101]
B11	VSS[5]	VSS[102]
B14	VSS[6]	VSS[103]
B17	VSS[7]	VSS[104]
B20	VSS[8]	VSS[105]
B26	VSS[9]	VSS[106]
B28	VSS[10]	VSS[107]
C2	VSS[11]	VSS[108]
C6	VSS[12]	VSS[109]
C27	VSS[13]	VSS[110]
D10	VSS[14]	VSS[111]
D13	VSS[15]	VSS[112]
D18	VSS[16]	VSS[113]
D21	VSS[17]	VSS[114]
D24	VSS[18]	VSS[115]
E1	VSS[19]	VSS[116]
E2	VSS[20]	VSS[117]
E4	VSS[21]	VSS[118]
E8	VSS[22]	VSS[119]
E15	VSS[23]	VSS[120]
F3	VSS[24]	VSS[121]
F4	VSS[25]	VSS[122]
F5	VSS[26]	VSS[123]
F12	VSS[27]	VSS[124]
F27	VSS[28]	VSS[125]
F28	VSS[29]	VSS[126]
G1	VSS[30]	VSS[127]
G2	VSS[31]	VSS[128]
G5	VSS[32]	VSS[129]
G6	VSS[33]	VSS[130]
G9	VSS[34]	VSS[131]
G14	VSS[35]	VSS[132]
G18	VSS[36]	VSS[133]
G21	VSS[37]	VSS[134]
G24	VSS[38]	VSS[135]
G25	VSS[39]	VSS[136]
G26	VSS[40]	VSS[137]
H3	VSS[41]	VSS[138]
H4	VSS[42]	VSS[139]
H5	VSS[43]	VSS[140]
H24	VSS[44]	VSS[141]
H27	VSS[45]	VSS[142]
H28	VSS[46]	VSS[143]
J1	VSS[47]	VSS[144]
J2	VSS[48]	VSS[145]
J5	VSS[49]	VSS[146]
J24	VSS[50]	VSS[147]
J25	VSS[51]	VSS[148]
J26	VSS[52]	VSS[149]
K24	VSS[53]	VSS[150]
K27	VSS[54]	VSS[151]
K28	VSS[55]	VSS[152]
L13	VSS[56]	VSS[153]
L15	VSS[57]	VSS[154]
L24	VSS[58]	VSS[155]
L25	VSS[59]	VSS[156]
L26	VSS[60]	VSS[157]
M3	VSS[61]	VSS[158]
M4	VSS[62]	VSS[159]
M5	VSS[63]	VSS[160]
M12	VSS[64]	VSS[161]
M13	VSS[65]	VSS[162]
M14	VSS[66]	VSS[163]
M15	VSS[67]	VSS[164]
M16	VSS[68]	VSS[165]
M17	VSS[69]	VSS[166]
M24	VSS[70]	VSS[167]
M27	VSS[71]	VSS[168]
M28	VSS[72]	VSS[169]
N1	VSS[73]	VSS[170]
N2	VSS[74]	VSS[171]
N5	VSS[75]	VSS[172]
N6	VSS[76]	VSS[173]
N11	VSS[77]	VSS[174]
N12	VSS[78]	VSS[175]
N13	VSS[79]	VSS[176]
N14	VSS[80]	VSS[177]
N15	VSS[81]	VSS[178]
N16	VSS[82]	VSS[179]
N17	VSS[83]	VSS[180]
N18	VSS[84]	VSS[181]
N24	VSS[85]	VSS[182]
N25	VSS[86]	VSS[183]
N26	VSS[87]	VSS[184]
P3	VSS[88]	VSS[185]
P4	VSS[89]	VSS[186]
P12	VSS[90]	VSS[187]
P13	VSS[91]	VSS[188]
P14	VSS[92]	VSS[189]
P15	VSS[93]	VSS[190]
P16	VSS[94]	VSS[191]
P17	VSS[95]	VSS[192]
P24	VSS[96]	VSS[193]
P27	VSS[97]	VSS[194]

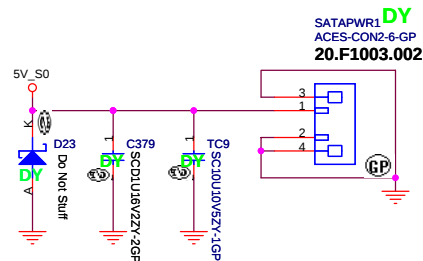
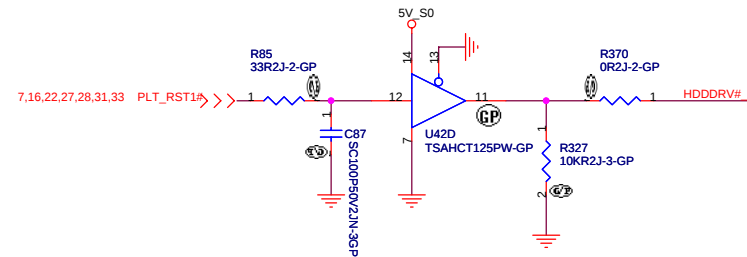
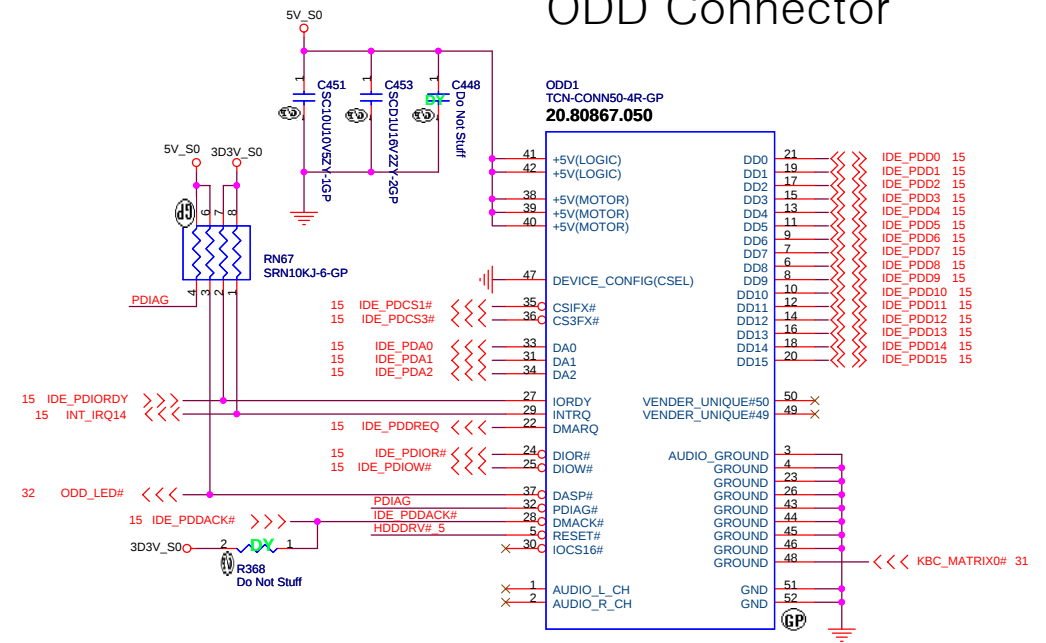
SMBUS

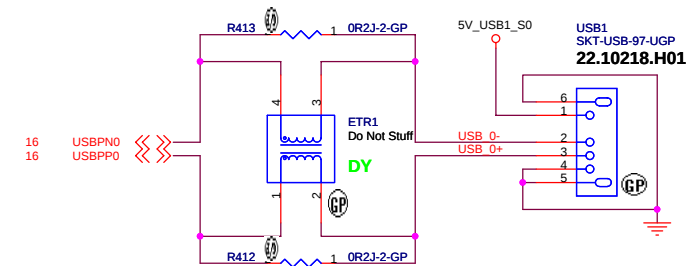
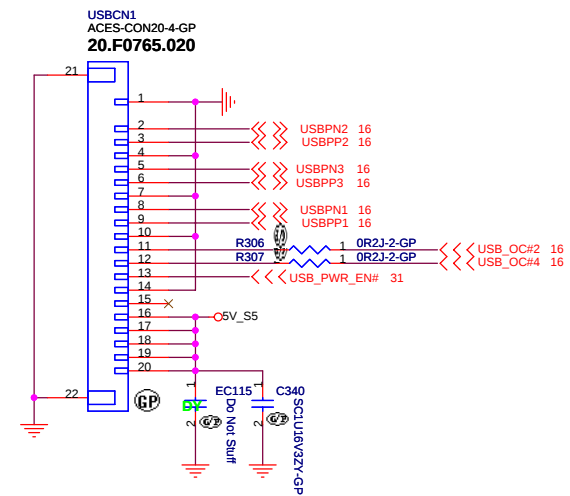
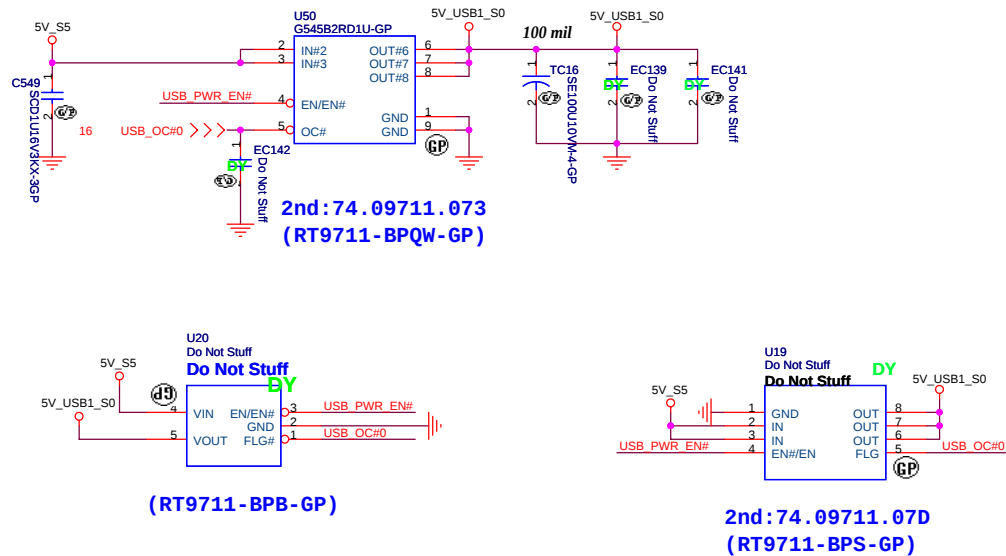


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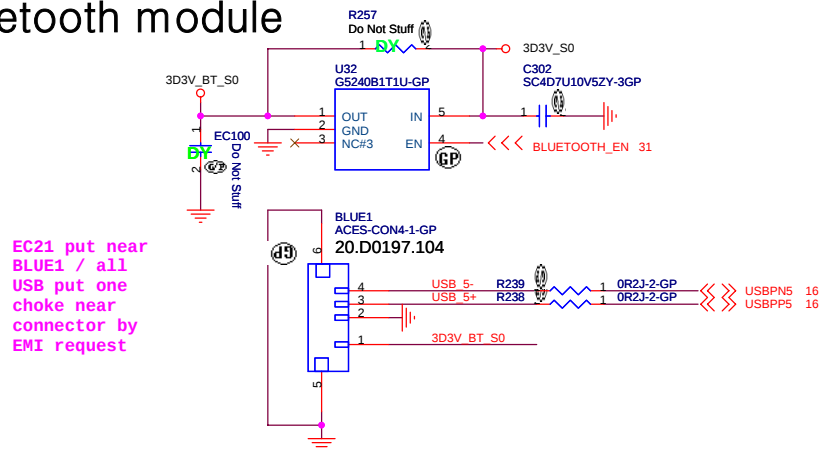
Title		
ICH7-M (4 of 4)		
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ODD Connector

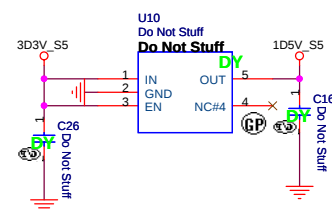
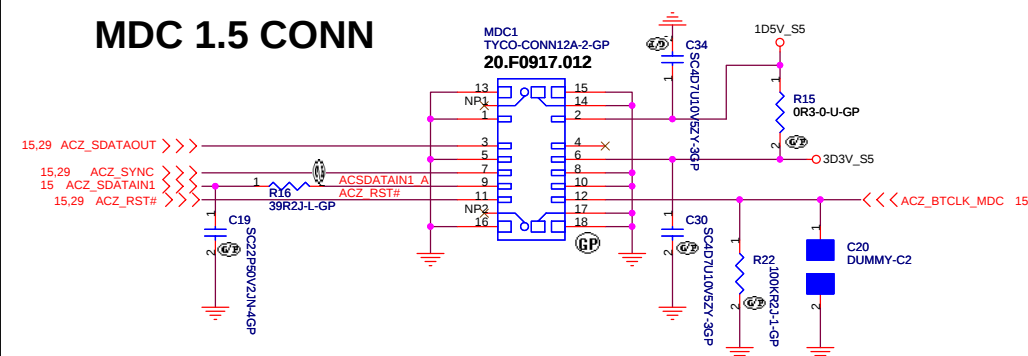




Bluetooth module



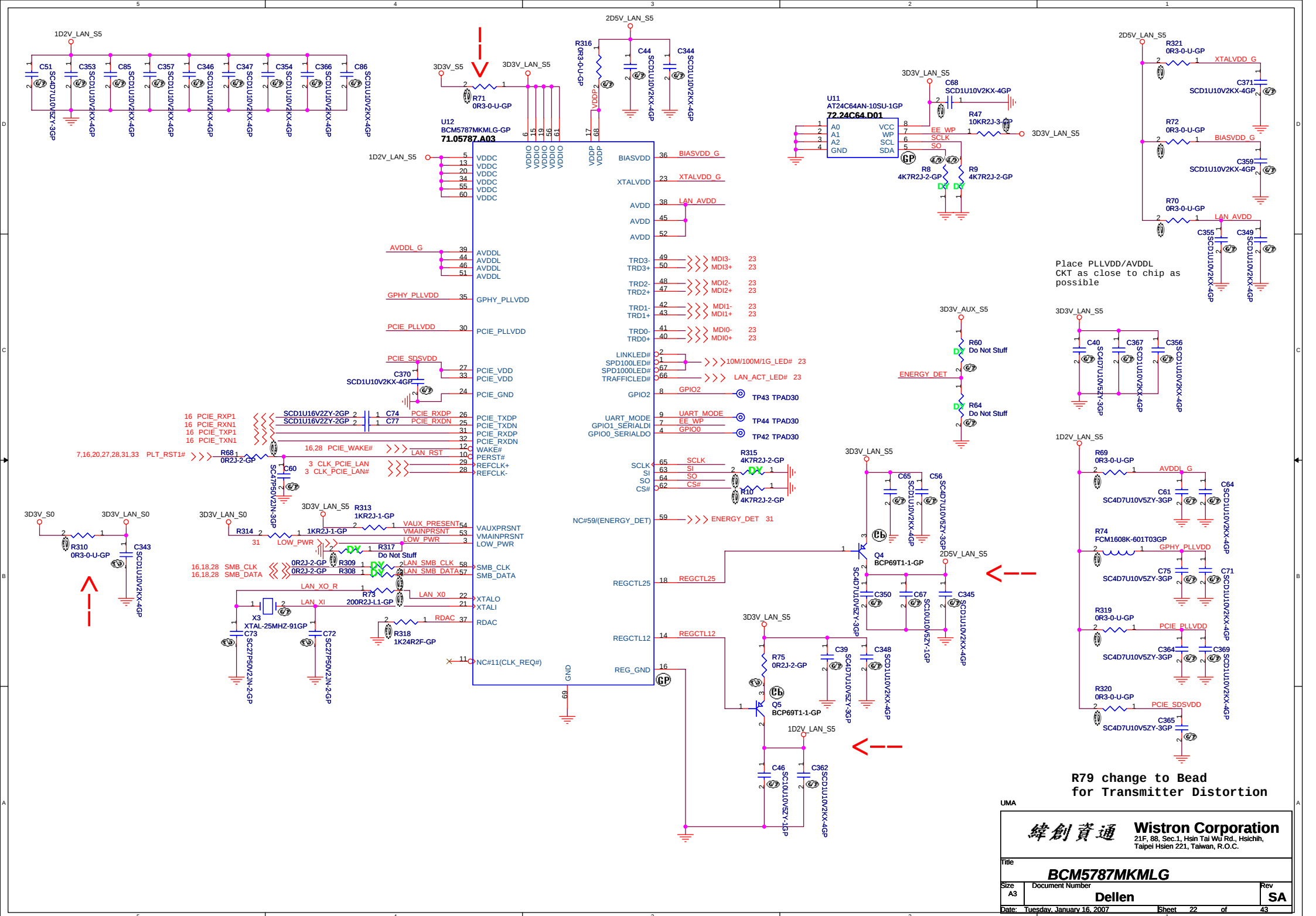
MDC 1.5 CONN



UMA

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Title			
USB / MDC / BLUETOOTH			
Size A3	Document Number	SA	
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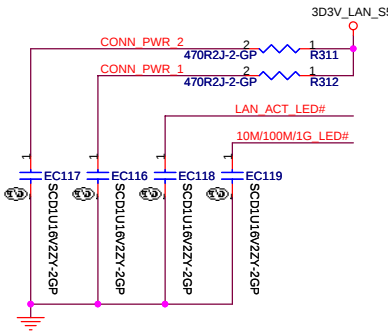


Place PLLVDD/AVDDL
CKT as close to chip as
possible

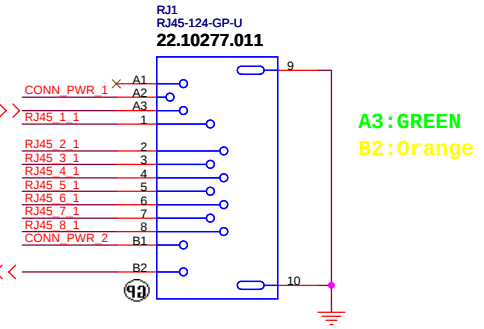
R79 change to Bead
for Transmitter Distortion

LAN Connector

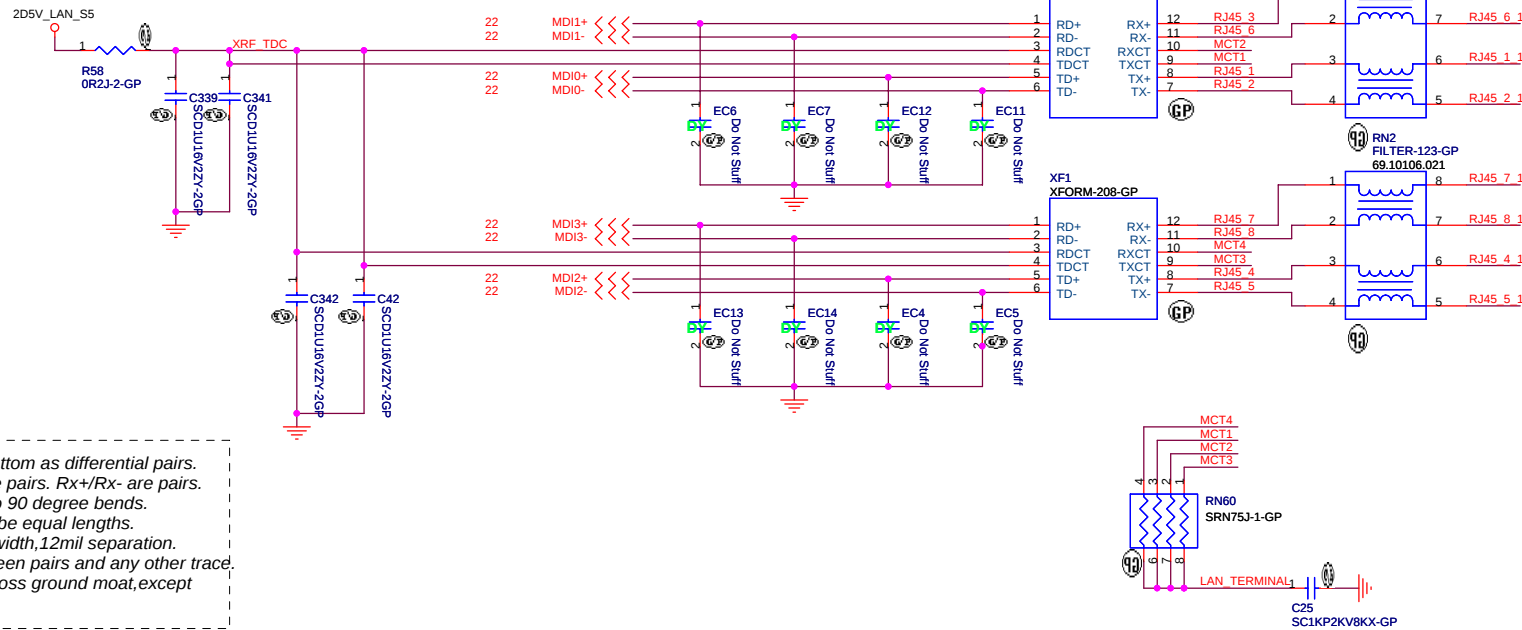
Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



22 10M/100M/1G_LED# >>>
22 LAN_ACT_LED# <<<



GIGA Lan Transformer



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

UMA

緯創資通

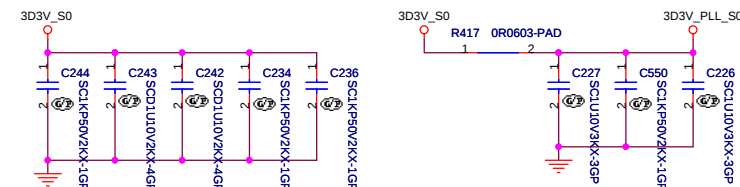
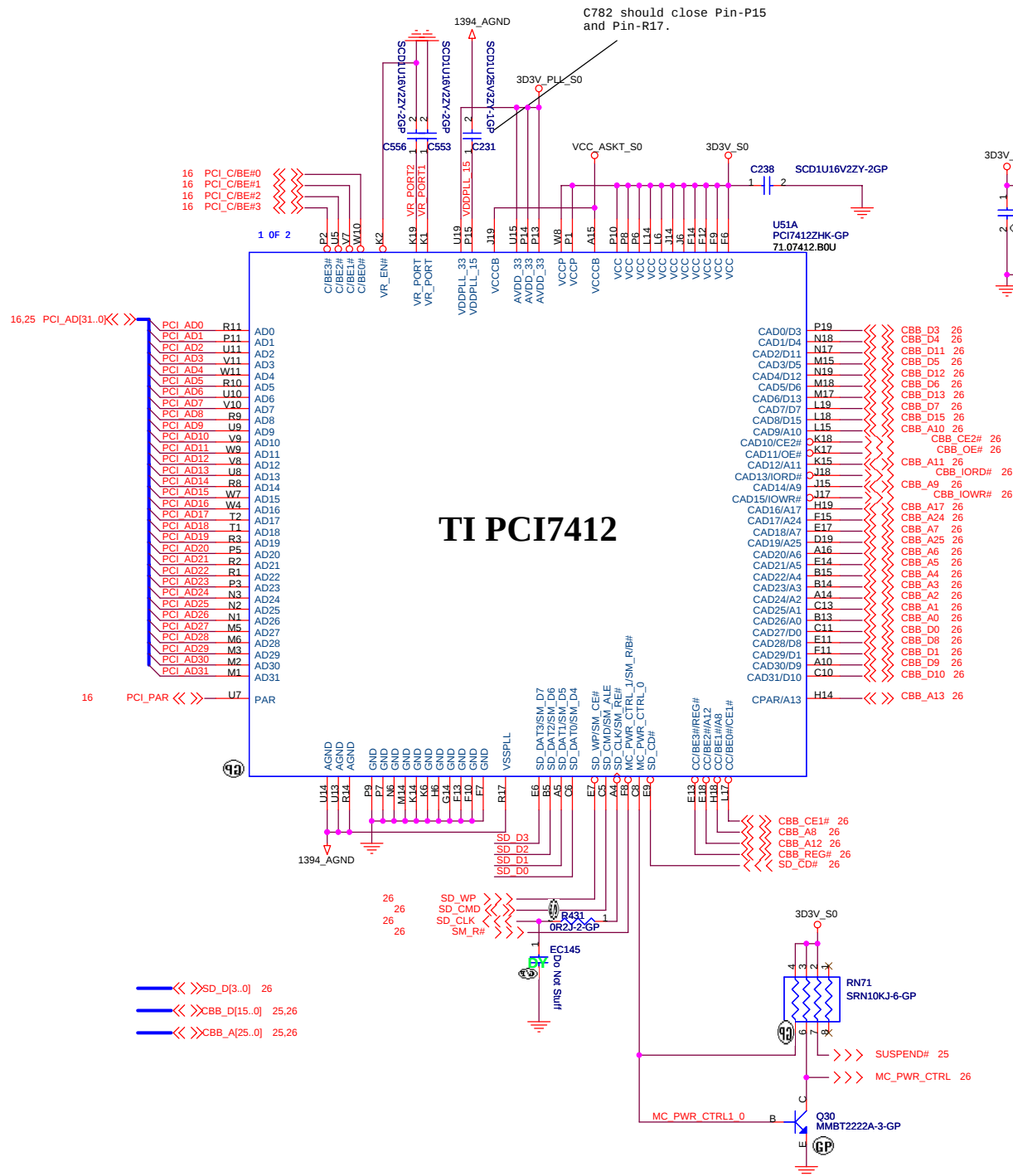
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Title

LAN Connector

Size A3 Document Number Dellen Rev SA

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Bypass/Decoupling Capacitors
Should be places as close to
PCI7412 as possible

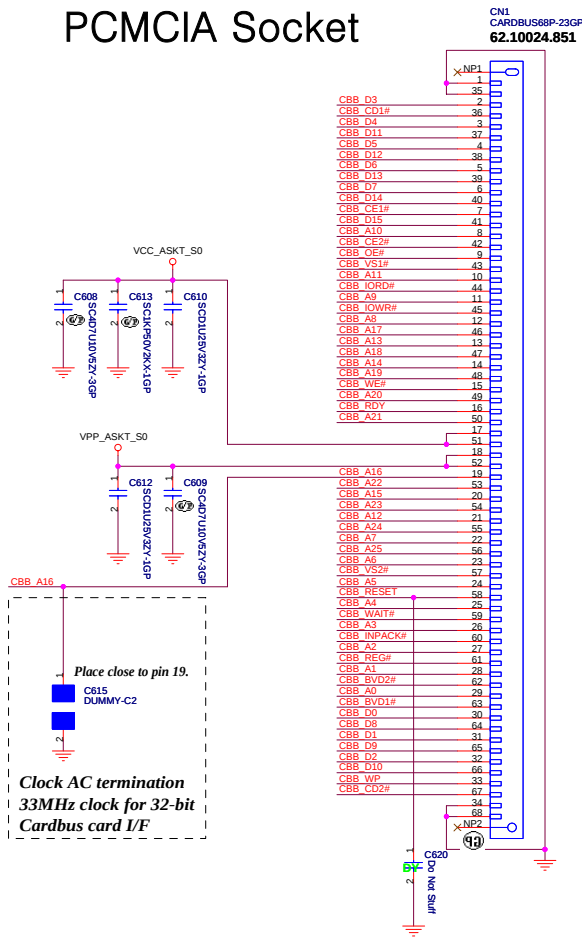
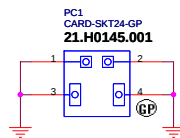
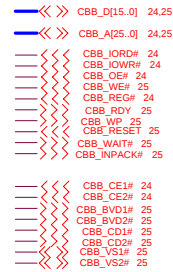
- * All 1394 signals must be routed on top side only
- * Differential pairs of each ports should have equal trace length
- * Stubs must be keep as short as possible

UMA

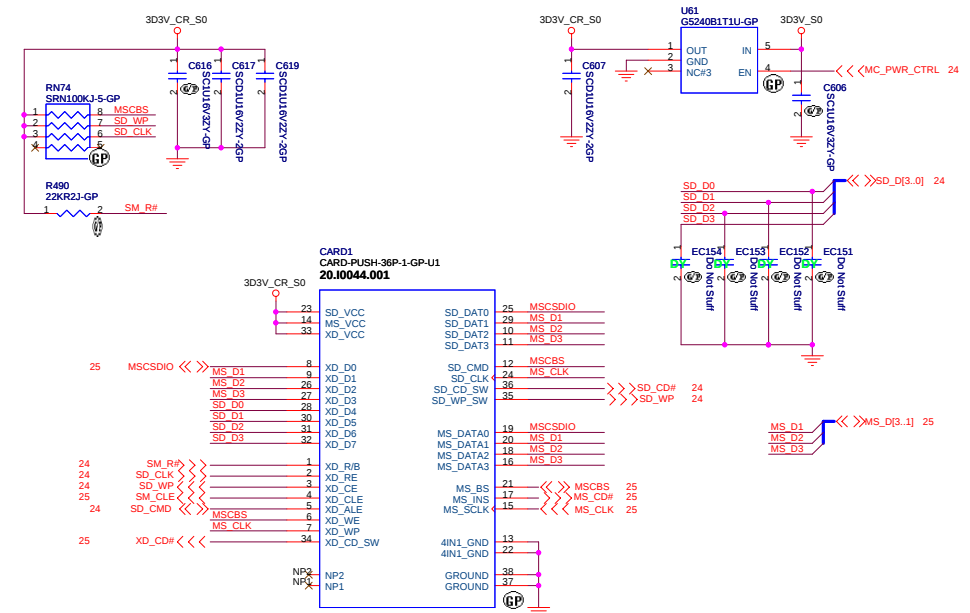
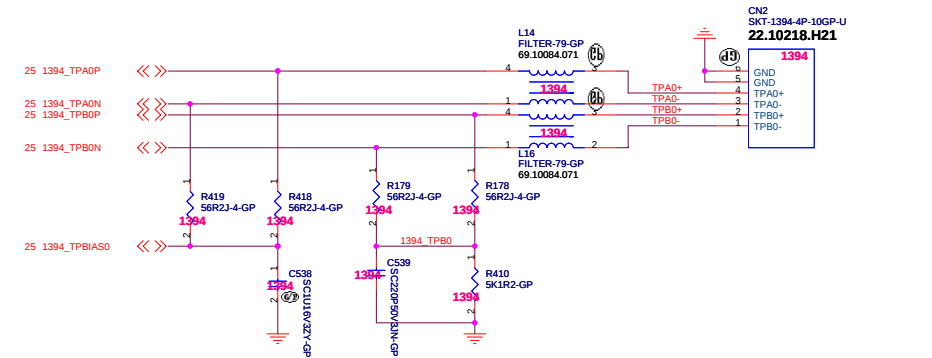
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title			TI PCI7412 (1 of 2)	
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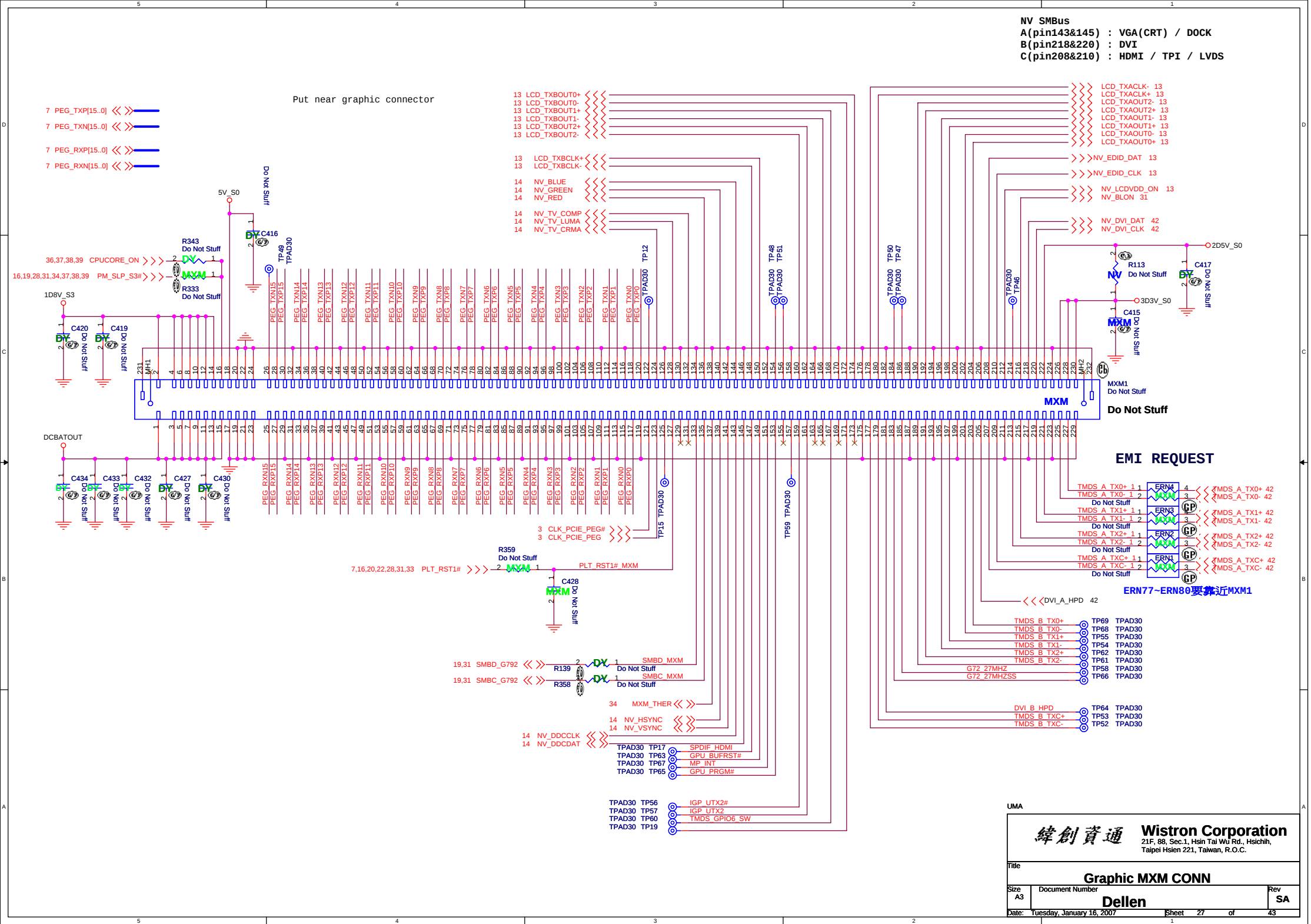
PCMCIA Socket

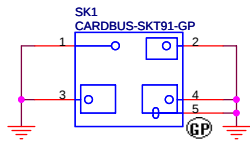
**Cardbus I/F**

1394 Connector



XD
MS / MS PRO
SD / SD IO / MMC

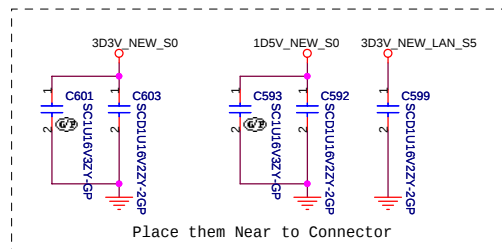
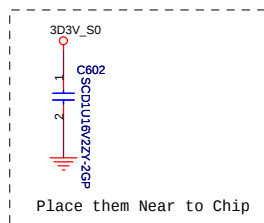
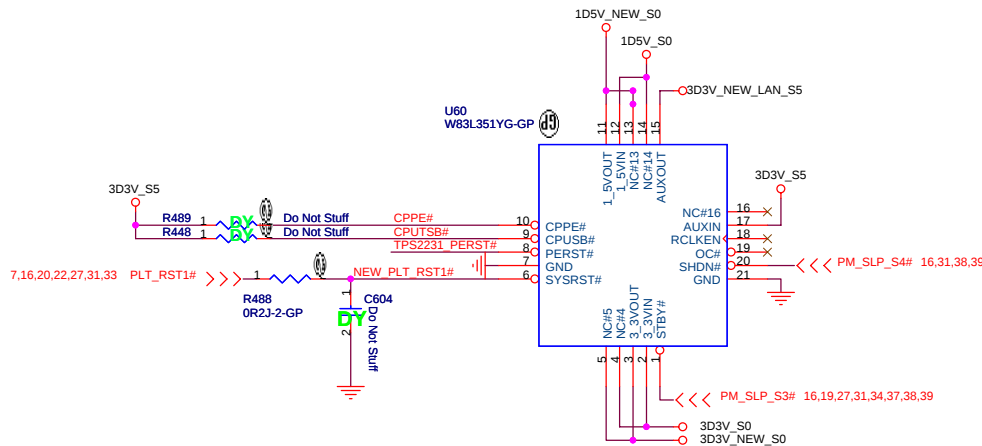
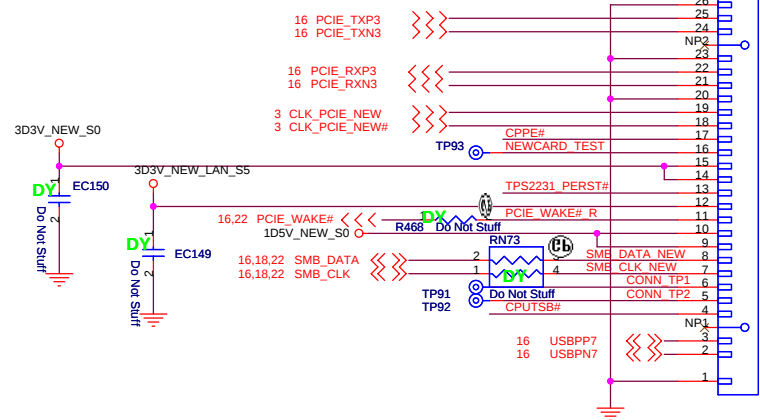




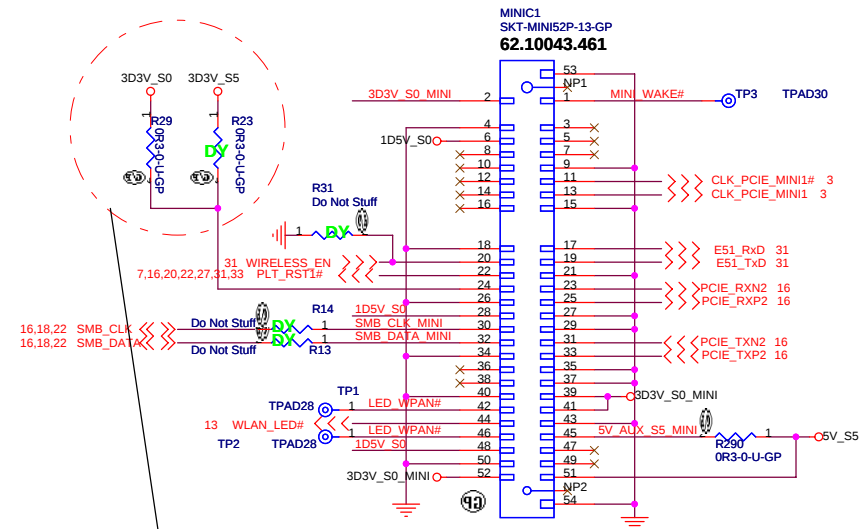
NEWCARD Connector

Reserve the symbol
for bottom side
connector

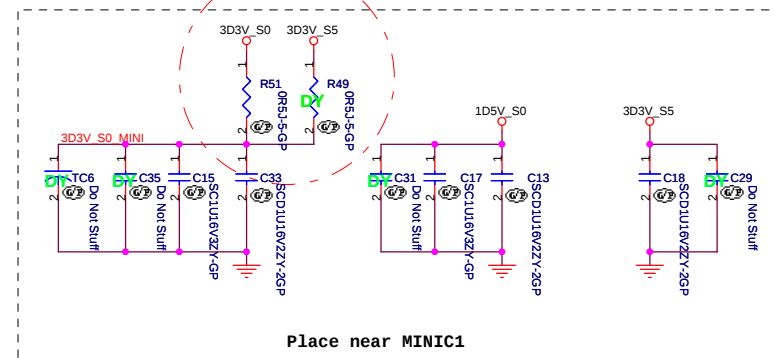
NEW1
CARDBUS26P-8GP
62.10024.881



Mini Card Connector



PCIE Mini Card For WLA W/O iAMT, TV or 3G

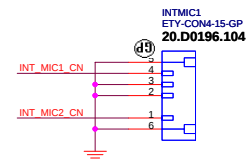
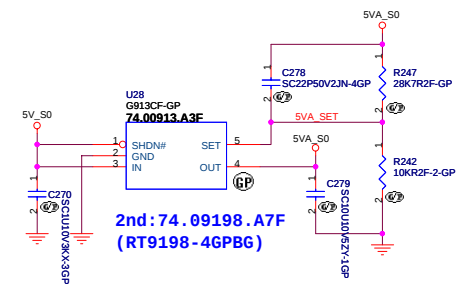


UMA

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Title			
MINI CARD / NEW CARD			
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AUDIO OP AMPLIFIER

R, L 1.5W Speaker

mount R274, R281
R269->63.36334.1DL
R268->63.33334.1DL

R, L 1W Speaker

mount R280, R281
R269->63.15334.1DL
R268->63.12334.1DL

R, L 1.2W Speaker

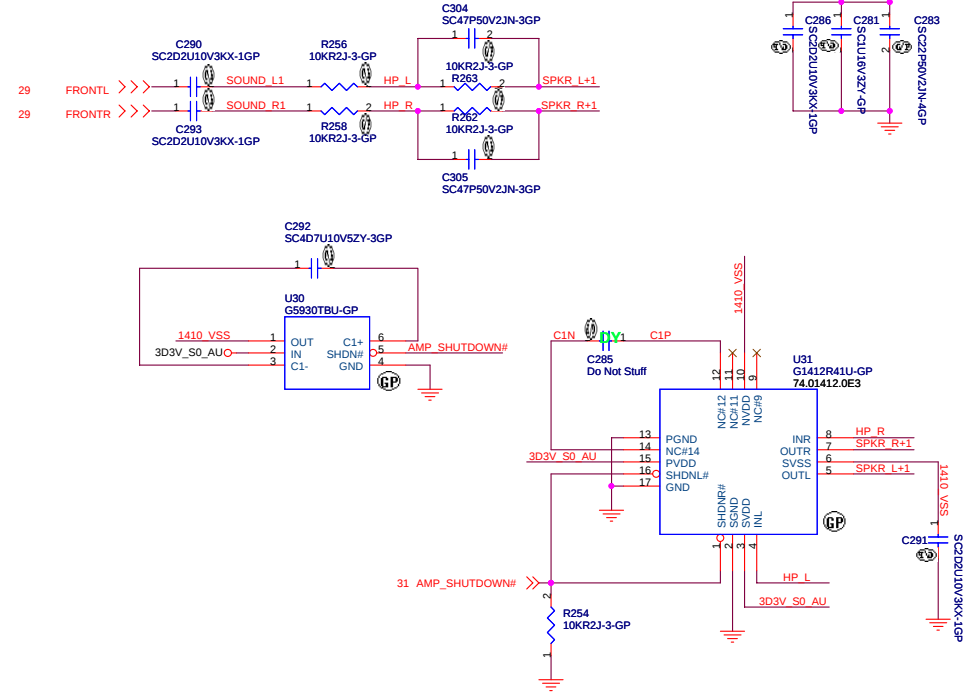
mount R280, R281
R269->63.10334.1DL
R268->63.68234.1DL

Internal Speaker

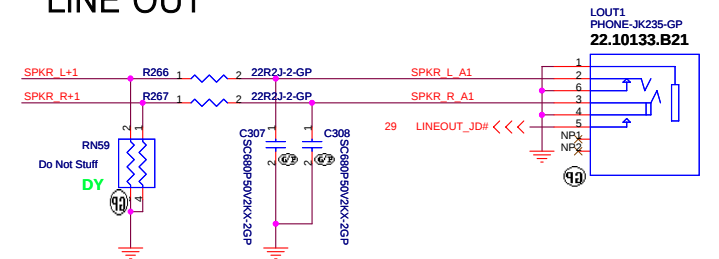
SPKR1
ETY-CON4-15-GP
20.D0196.104

ERC4
Do Not Stuff
DY

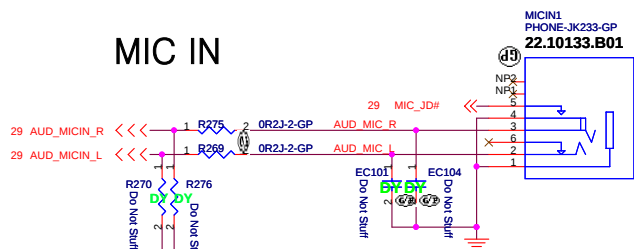
KBC_MUTE_GPI08



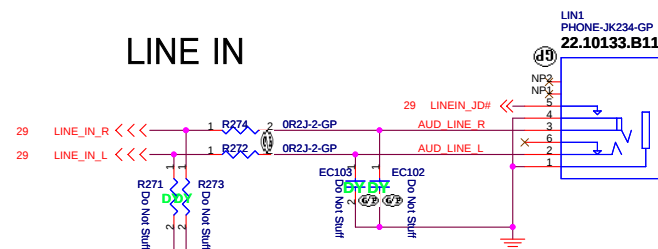
LINE OUT

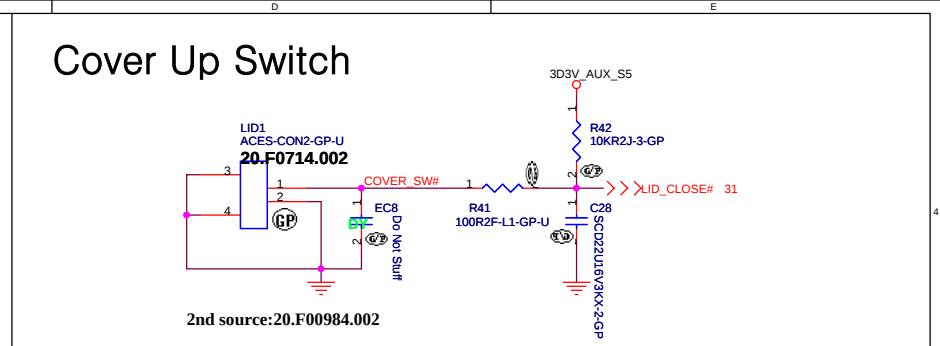


MIC IN



LINE IN





Signal	TP	TPAD30
3D3V_S5	TP90	TPAD30
5V_S5	TP89	TPAD30
16.31 PM_PWRBTN#	TP88	TPAD30
4.15.34 H_PWRGD	TP9	TPAD30
31.37 SS_ENABLE	TP87	TPAD30
4.6 H_CPURST#	TP45	TPAD30

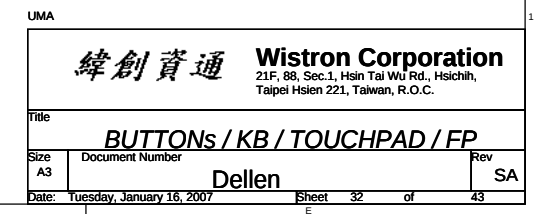
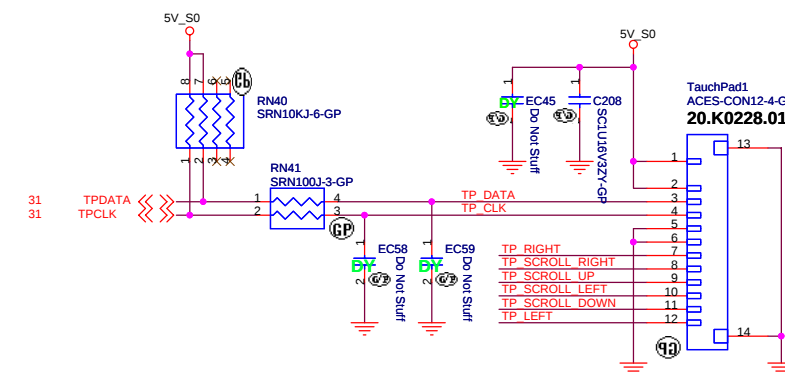
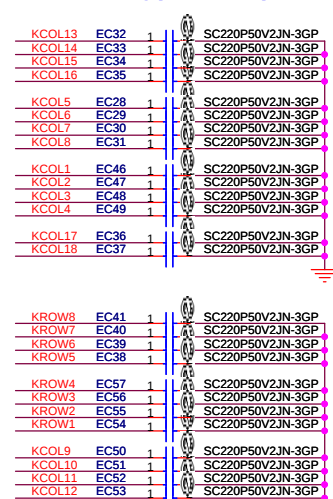
20 ODD_LED# >> 2

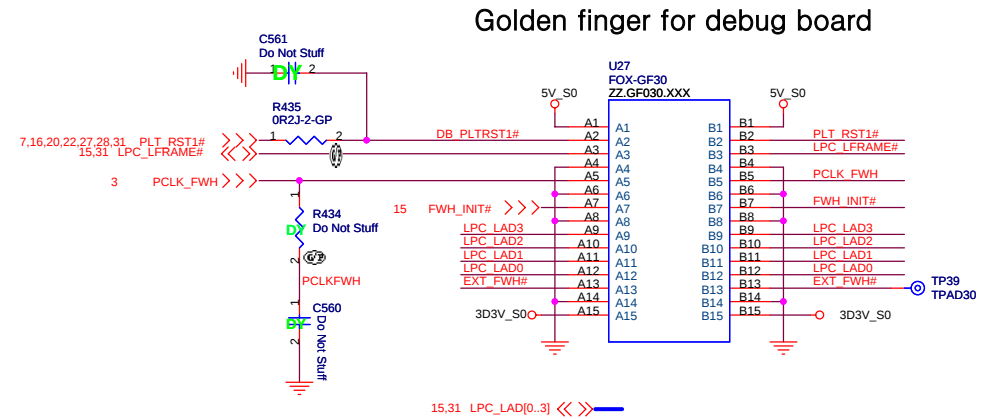
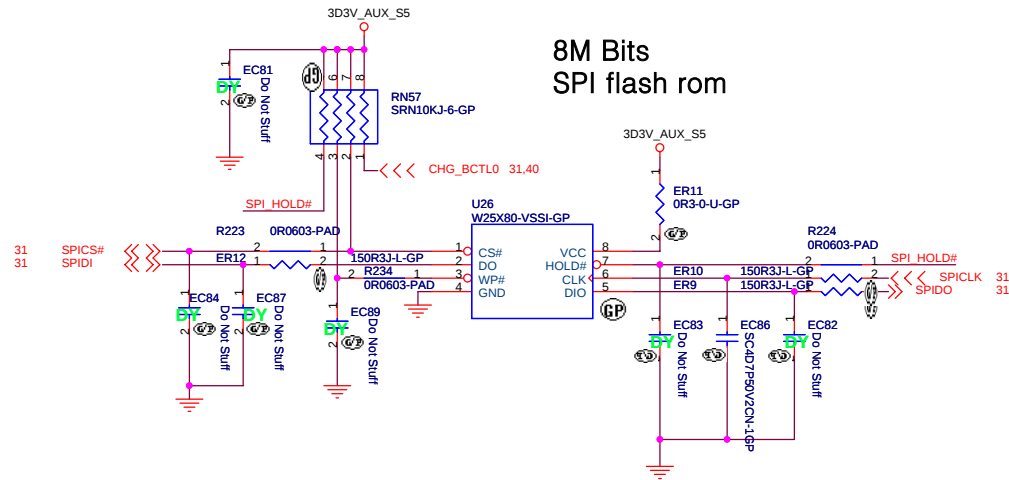
15 SATA_LED# >> 1

3 MEDIA_LED#

D27
BAW56PT-U
83.00056.E11

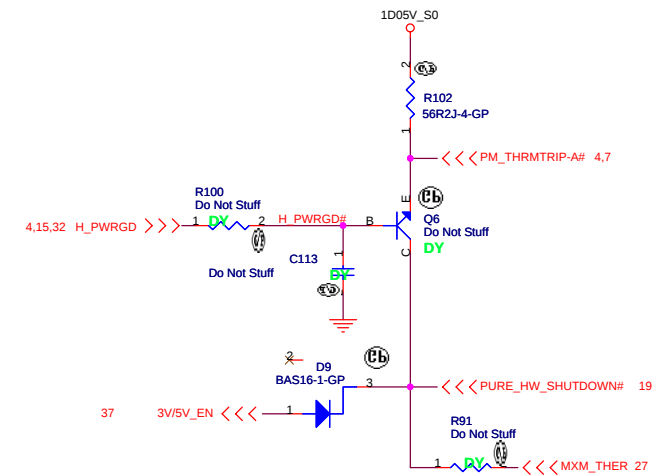
The schematic diagram illustrates the electrical connections for the ACES-CON12-4-GP connector. It shows the internal wiring between the 12 pins of the connector and the 16 pins of the FPCN1 ACES-CON15-GP connector. Key components include capacitors EC45, EC60, EC59, EC61, C208, C210, and C211, and resistors R155 and R156. The diagram also shows the connection to a 3D3V_S0 power source and a 5V_S0 power source. The connector is labeled 'TauchPad1 ACES-CON12-4-GP 20.K0228.012'.





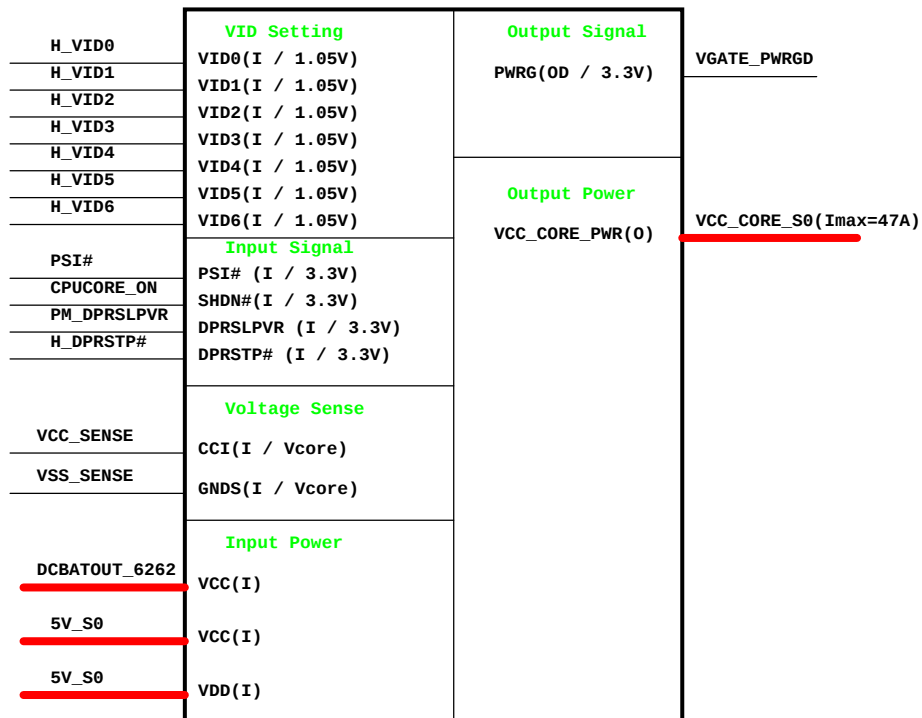
UMA

3D3V_AUX_S5

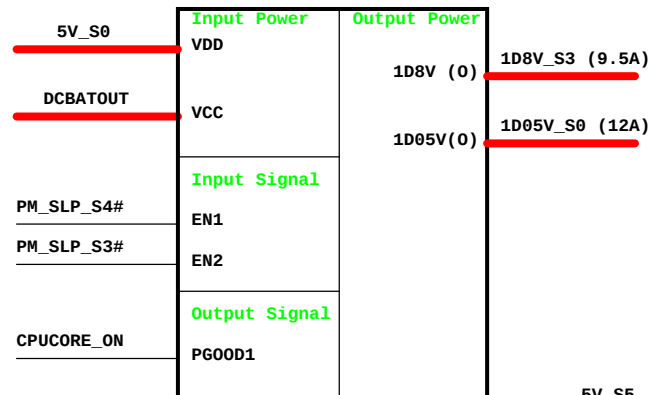


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Title 3D3V_AUX_S5 / 3D3V_S0 / 5V_S0			
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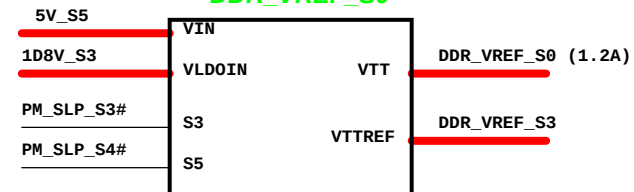
CPU_CORE
MAX8770



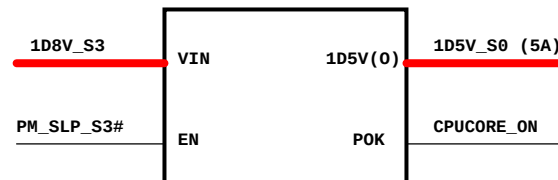
MAX8717
1D8V_S3 / 1D05V_S0



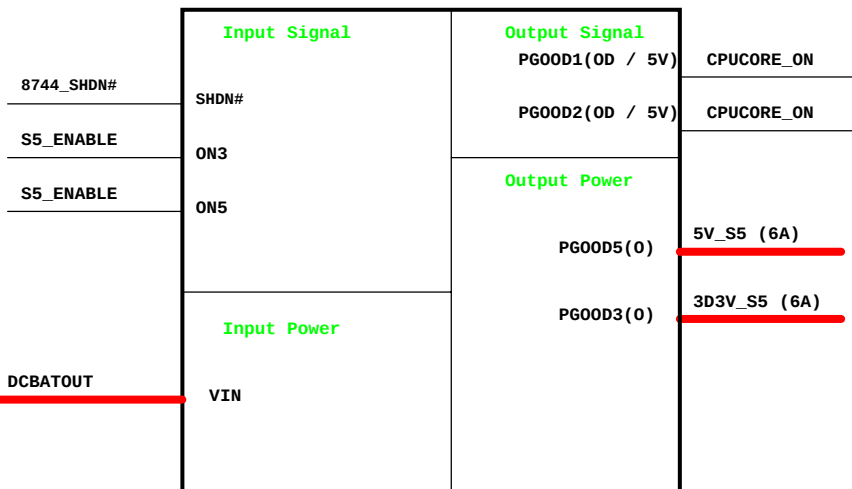
TPS51100
DDR_VREF_S0



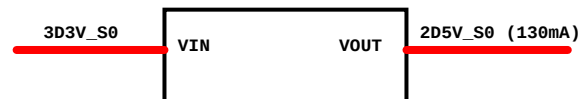
APL5912
1D5V_S0



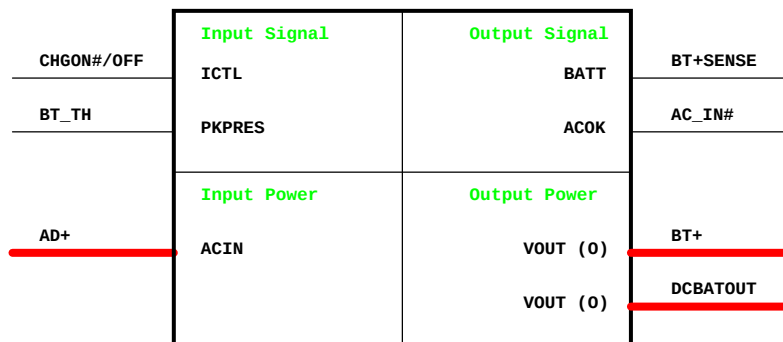
MAX8744
5V_S5 / 3D3V_S5



APL5312
2D5V_S0

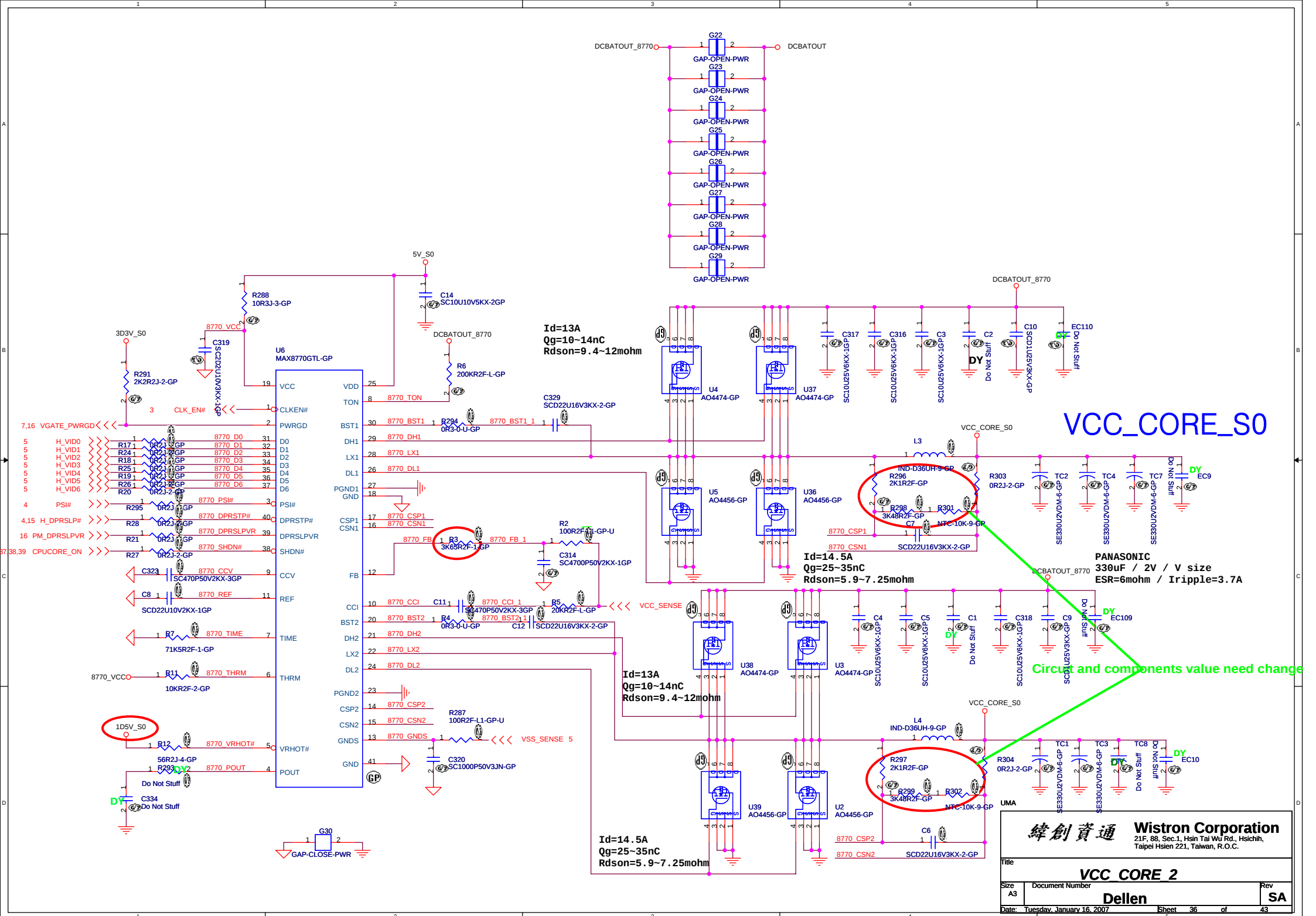


Charger ISL6255



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Id=13A
Qg=10~14nC
Rdson=9.4~12mohm

Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm

Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm

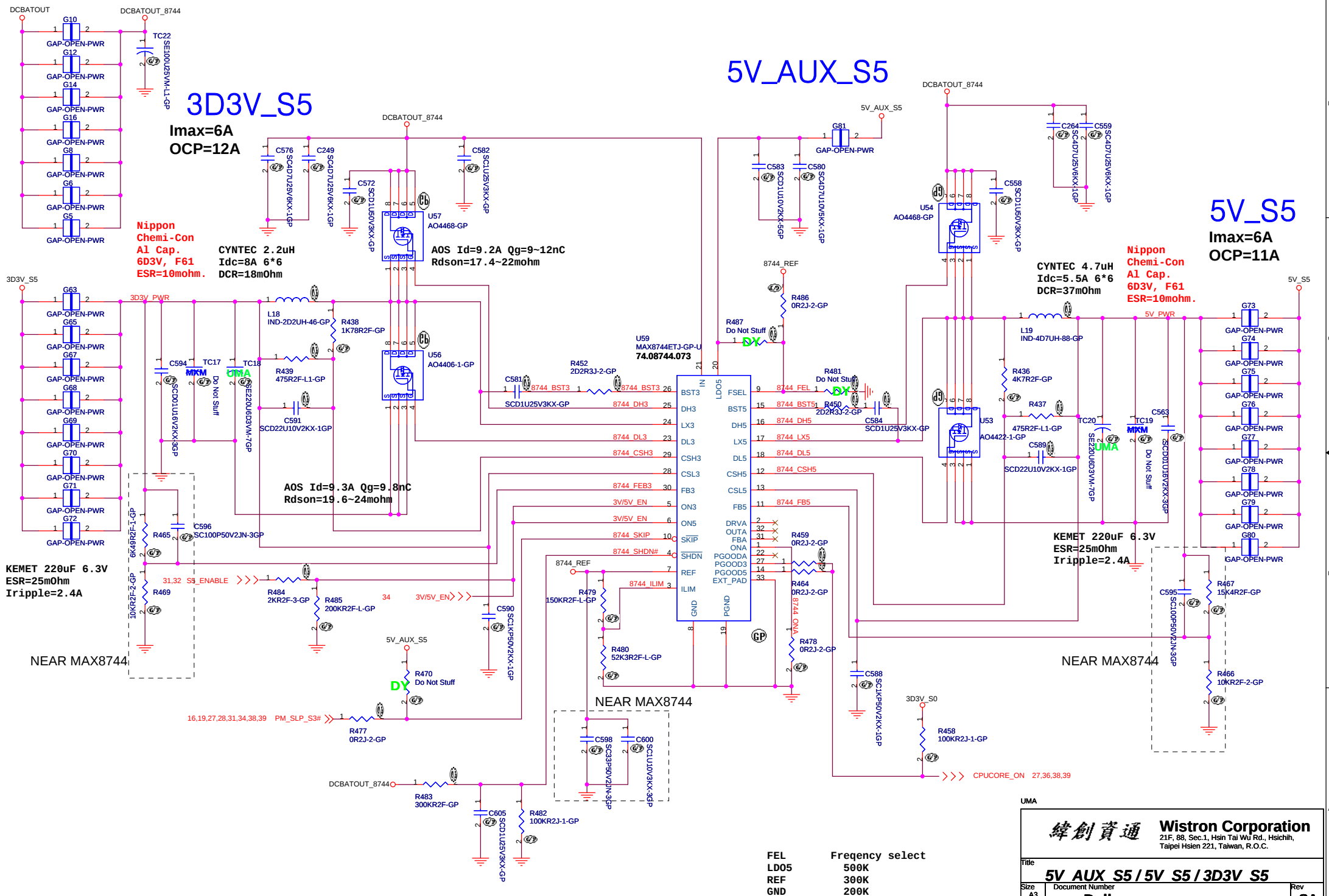
VCC_CORE_S0

PANASONIC
330uF / 2V / V size
ESR=6mohm / Irripple=3.7A

Circuit and components value need change

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Taipei Hsien 221, Taiwan, R.O.C.

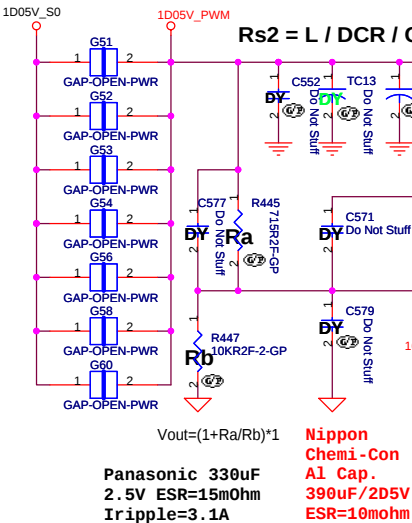
Title			VCC CORE 2	
Size	Document Number			Rev
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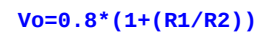
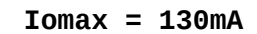
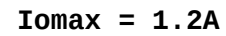


1D05V_S0

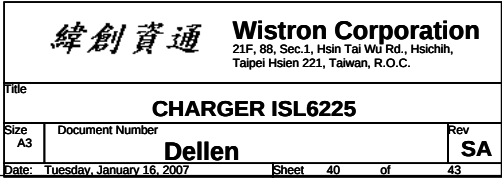
1D05V I_{max}=12A
OCP>19A

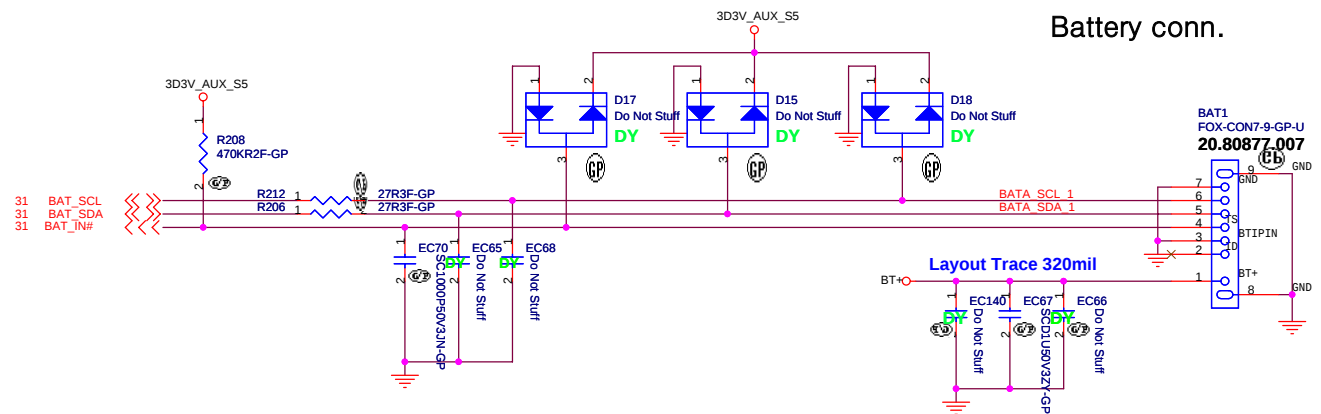
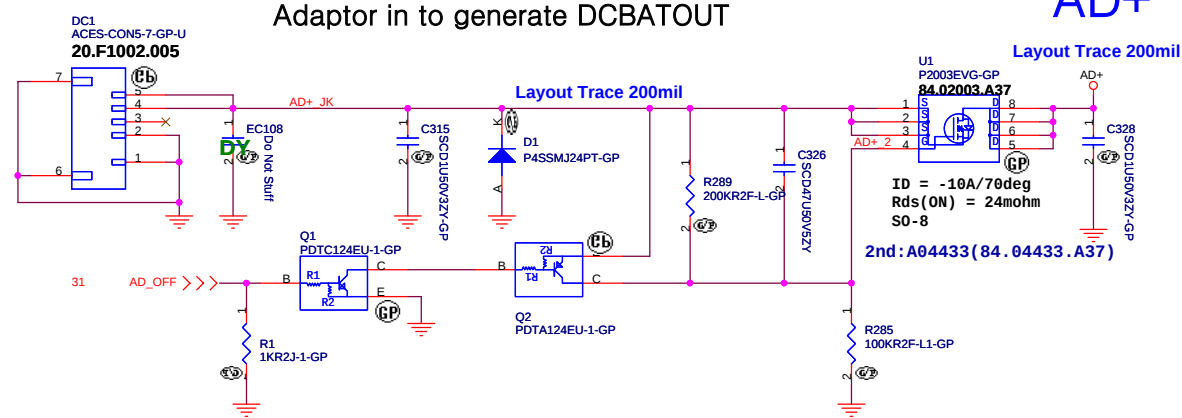
V_{cal}=1.0511V





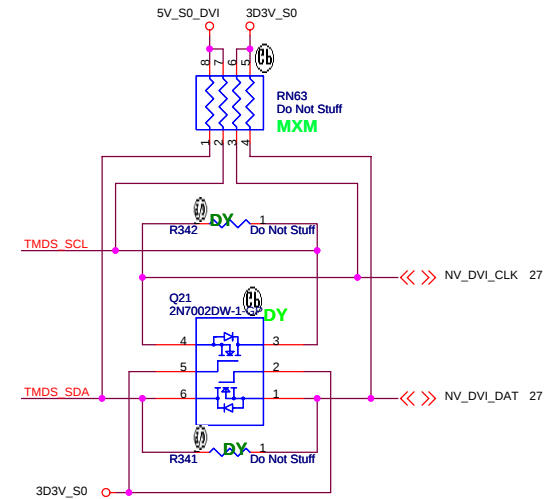
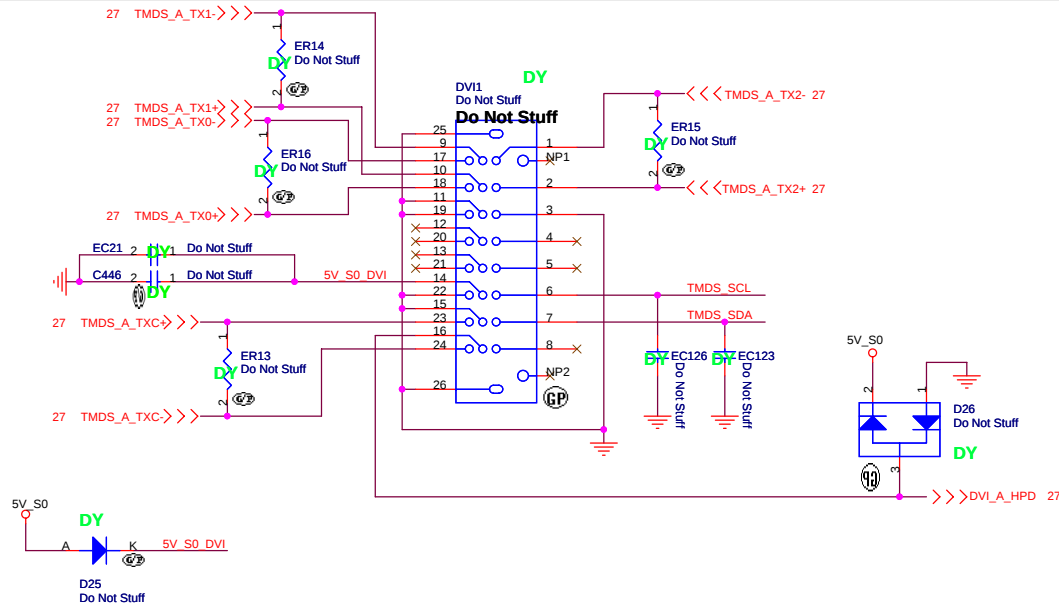
SANYO
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm





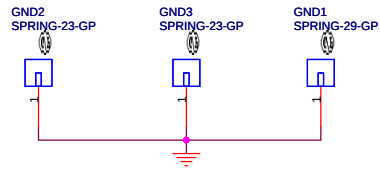
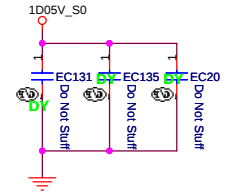
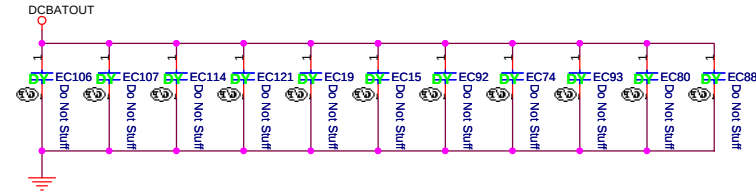
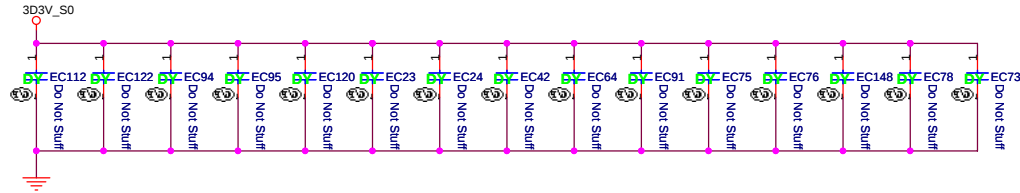
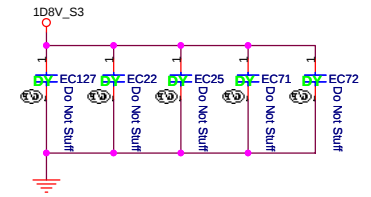
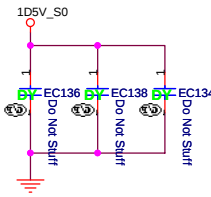
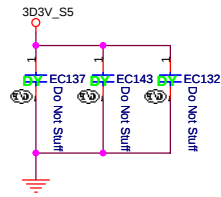
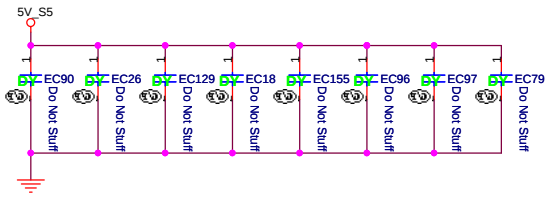
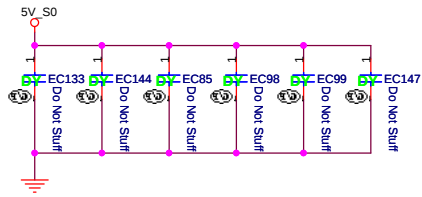
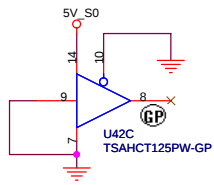
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Title	
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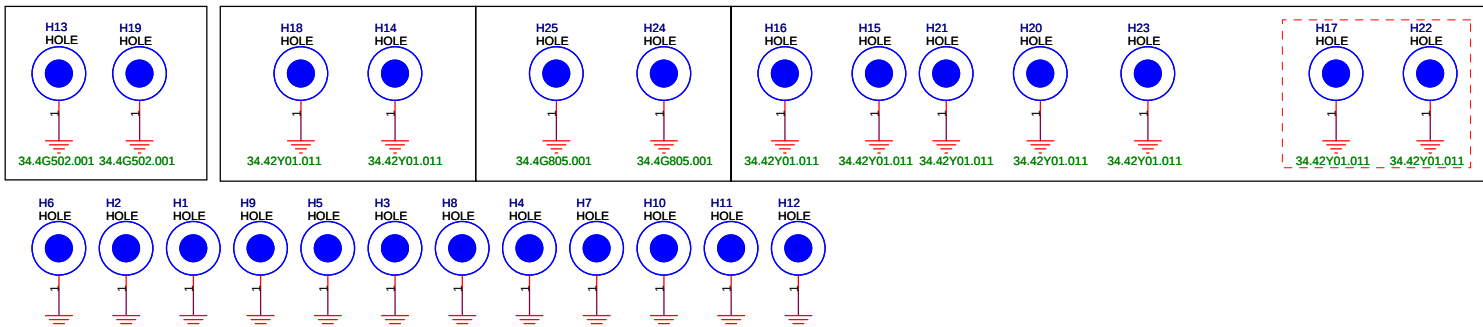
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: DVI CONNECTOR			
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Spring

GND 1 : 34.42T14.001
GND 2/3 : 34.39S07.003

MINI CARD



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Title EMI / Spring / Boss	
Size A3	Document Number
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