

CPU DC/DC
Switching Power
MAX1718/MAX1714

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 VCCT_S0 PAGE : 27, 28

DC/DC&CHARGER
Switching Power
MAX1632/OZT05J02

INPUTS	OUTPUTS
DCBATOUT	3D3V_S5AC 3D3V1_S5AC 3D3V_S3 3D3V_S0 5V_S0 12V_S0 BT+ PAGE : 29, 30, 31 /32, 33
AD+	

OTHER DC/DC
MAX1792/G913

INPUTS	OUTPUTS
3D3V_S0	2D5V_S0
2D5V_S0	1D5V_S0 1D8V_S0
3D3V_S3	2D5V_S3 PAGE : 28

TM100

Project Code : 91.48R01.001
PCB P/N : 01201-1
PCB : 48.48R01.001

CLOCK
Genertor
3D3V_S0/2D5V_S0
ICS9248-61 Page:3

CPU
PIII TUALATIN
ULV 700MHZ~
FCBGA Page:3,4

HOST BUS
100MHZ

SDRAM
SDRAM*2
3D3V_S3
Page:8

HDD
5V_S0
Page:13

IDE BUS
Ultra 33

CORE LOGIC
Intel 82443MX
+3.3V/M+3V/+2.5V/M+2.5V/+5V
Page:7

2D5V_S3/3D3V_S3
/2D5VRD_S3
VGA
SMI SM722
Page:9

5V_S0
CRT
Page:10

3D3V_S0
LCD
Page:11

PCB LAYER
L1: COMPONENT
L2: GND
L3: SIGNAL
L4: SIGNAL
L5: GND
L6: VCC
L7: SIGNAL
L8: SIGNAL
L9: GND
L10: COMPONENT

+3.3V/+5V/+12V
CARDBUS
02 0Z711
TARZEN
Page:14

SMART Card
SLOT *1
Page:15

CARDBUS
SLOT *1
Page:15

PCI BUS

LAN_3D3V_S5AC/
LAN_2D5V_S5AC/
LAN
RTL8100BL
Page:17,18

3D3V_S5AC
MINIPCI
802.11
Page:19

3D3V_S0
IEEE 1394
TI TSB43AB21
Page:16

XD BUS

5V_S0
SIO
NS 97338
Page:25

5V_S3
KBC
M38869
Page:23

5V_S0
BIOS
ROM
Page:24

5V_S0
DEBUG
PORT
Page:27

AC-LINK

3D3V_S0
FIR
IRMS6452
Page:26

5V_S0
DIGITIZER
Page:11

5V_S0
Touch
Pad
Page:23

5V_S3
INTKB
Page:23

5V_S0
USB
PORT
0,1 Page:26

3D3V_S0/5V_S0
MODEM
Daughter
Card
Page:19

5VA_S0
AC 97
Codec
CS4299-XQ
Page:20,21,22

緯創資通

Wistron Corporation
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Title System Block Diagram		
Size A4	Document Number TM100	Rev -1
Date: Thursday, April 04, 2002	Sheet 1 of 35	

1. Support S3 State (Suspend To RAM):

No	Wake Up Event	Chip Controller	Description
1	PME#_RSM(WOL)	LAN Controller RTL8100L	Magic Packet/ Wake Up Frame
2	PWRBTN#_SRSM	Banister	Wake Event from User
3	LID	KBC	
4	Ring IN	MDC	
5	Any Key	KBC	
6	BL2#	KBC	

2. Change notice :

* Before SMT of SA::

1>0R3-0-U (63.R0004.151) DEL: R260, R211, R214 ADD: R261, R209, R216, R263

2>Charger firmware U48 from P/N:71.12509.00A(PIC) to P/N:71.00012.00A(ATMEL)

* SA -> SB:

1>Swap smart card connector and use this one. P/N: 20.K0090.012

2>Dummy the 5 resistors of VGA: R46, R238, R240, R241, R242 - P/N:63.47234.151

3>Modify the U4-4 from 2D5V_S0 to 2D5V_S3

4>Change the Q6 from 2N7002 - P/N:84.27002.031 to TP0610 -P/N: 84.00610.031 , then swap D and S

5>Change R6 from 10K - 63.10334.151 to 1K - 63.10234.151

6>Connect R49 and R52 LVDSVDD to 2D5V_S3

7>Modify core voltage setting: (1)R313:100K->Dummy (2)R311:Dummy->1K (3)R325, R326:1K->Dummy (4)R328, R329:Dummy->100K

8>Modify GPIO of KBC: (1)P20:HOTKEY->CH6_FLASH (2)P66:PCB_VER_SET2->EN_FLASH

9>R403:33R(63.33034.1D1)->0R(63.R0034.1D1)

10>Add U08 to modify the driving voltage from 3.3V to 5V

11>VGAU34: 71.00722.00U->71.00722.A0U

* SB -> SC:

Page 3:

1> Reserve test pads for 48MSEL100/66# and DIV4#

2> Change R418 to 0R and BC351 to dummy to tune 48M signal quality

Page 7:

3> Change

GPIO2 to MP_COMMAND, GPIO3 to MP_ACK, GPIO6 to OBLAN-80211#, GPIO20 to AD_OFF, GPIO29 to PCI_REQ#3, GPIO30 to PCI_GNT#3

Page 11:

4> Modify the logic of STD_LED and PWR_LED

5> Add R521 to pull 3D3V_S0 for SUSB#

Page 12:

6> Change R269 pull H plane from 5V_S0 to 3D3V_S0

Page 13:

7> Change HDD connector for ME request

8> Add pull H for PCI_REQ#3, PCI_GNT#3. and PCI_PERR#

Page 14:

9> Change PCI_REQ# from 1 to 3 , PCI_GNT# from 1 to 3

10> Add R546 between BAN_PME# and CARDBUS_PME#

Page 15:

11> Change the cardbus socket SKT3 for ME request

Page 16:

12> Change PLLVDD(Pin 1) to 3D3V_S0

13> Dummy Pin121-125 for 43AB21, but reserve resistors for 43AB22

Page 17/18:

14> Mount the components for RTL8100BL

15> Add R524 and Q32 for preventing leakage current

16> Modify JK2(RJ11-45) for ME request

17> Add circuit for BIOS setting between LAN and 802.11

Page 19:

18> Add BC486 and BC488 for EMI request

Page 20/21/22:

19> Add BEEP from uP to control BEEP sound

20> Codec Pin 27: NC

21> Add BC487 between AUD_GND and DIG_GND for EMI

22> Change U75 and U80 to GMT 1211

23> Change U77 to APA2020

24> Performance tuning:

(1) BC308 to 0.01uF (2)BC466, BC467, and BC469 to 3.3V (3)R491 to 470R (4)DUMMY:BC424, BC448, BC451, R506, R381, R303, BC475, BC476, BC434, BC432 (5)Change R513, R516, R497, R495 to 12K(6)Change R514, R496 to 15K (7)R498, R515 to 27K (8)R382, R380 to 0R3

Page 23:

25> Modify KBC P27 to NC, P40 to EMAIL_LED#, P65 to BACKLIGHT_OFF#

Page 24:

26> Change button_interrupt from IRQ7 to PCI_INTB#

Page 28:

27> Reserve R532 for EMI request

28> Add R531to pull L(Reduce_on)

Page 29:

29> Change U3 and U36 to FDS6982S, then dummy D3 and D17

30> Change D13 and D14 to 83.1R003.A8F

Page 32:

U9 -pin 13: NC

Page 33:

31> Modify the U48 circuit for preventing U48(5V) drive 82440MX(3V)

32> Use U48 to replace U9(uP) to control charge_LED

Page 34:

33> Reserve test pads for cLock-down circuit

* SC -> SD

Page 6:

1.>Change Q26 from BSS138 to MMBT3904

Page 7:

2.>GPIO9 : Replace 802.11LED# with OBLAN-80211#

3.>Add smith trigger and debounce RC to solve 100uS drop of SUSB#

Page 10:

4.>Change VGA connector for ME request

Page 11:

5.>Change U88-1 control pin from U50-2 to BL2#

6.>Replace digitizer reset signal from SUSB# to PCIRST2#

7.>Add R564 to limit the current

Page 12:

8.>U51-1control signal changed from 3D3V_S0 to PRE_SUSC#

Page 13:

9.>Add D34 to prevent park voltage of HDD under -0.3V

Page 14:

10.>Add DTC124EKA and dummy R546 to be the gate of PME# of OZ711.

Page 16:

11.>Change 1394 connector for ME request

Page 17:

12.>Use U90 as the gate to control PCIRST2# to OBLAN and PL 10K to PCIRST2#_LAN

13.>Replace the L15 to R563(0R3) for vendor request.

14.>Add 100K to PL the U70-74 to solve the wake on LAN.

Page 18:

15.>Dummy BC38, R526, R527, R528 for vendor request.

Page 19:

16.>Modify the 802.11L_ACT from CN18 pin12 to pin11.

17.>Use U91 as the gate to control PCIRST2# to 802.11 and PL 10K to PCIRST2#_80211

18.>Add 10K to pull up BAN_PME# to 3D3V_S5

Page 20:

19.>Add 3 open-gapes for EMI request.

Page 21:

20.>Add DC bias PH 4.7K to internal MIC

Page 22:

21.>Update Audio Jack for ME request

Page 23:

22.>Modify the email-led control method because there is no GND on KB for KB matrix to PL.

23.>Use 7474 to keep the reset of KBC while in S3.

24.>Use the DTC124EKA and RB731U to prevent the leakage between KBC and Banister while in S3.

Page 24:

25.>Add helf smith-trigger to 5 button.

Page 26:

26.>Delet F2 and change it to 0.75A

27.>Add Beads between USB conn. and bypass C for EMI request

Page 27:

28.>Use CC.CPUSTP to drive CC.DPSLP#

29.>Change R93 from 0R to 4.7R for EMI request

Page 28:

30.>Change R532 from 0R to 4.7R

Page 29:

31.>Parallel 47KR to BC55

32.>For SKIP mode , modify the BC5 and BC140 to 47PF and add 100PF to replace R24 and R37.

33.>Change R26,R27,R13 and R36 from 0R to 4.7R for EMI request.

Page 30:

34.>Add smith trigger and debounce RC to solve 100uS drop of SUSC#

Page 31:

35.>Add bypass 0.1uF between AC Jack and bead for EMI request .

36.>Change R3 from 10K to 2.2K

Page 32:

37.>Change R07 from 15mR to 10mR for current limit of adaptor.

38.>Change R258 and R96 from 0R to 4.7R for EMI request

Page 33:

39.>Add 10KR to Pull BL2# to 3D3V_S3

40.>Change R261 from 10K to 2.2K

41.>Change U44 from MAX1615 to LP2951 for cost down

Page 35:

42.>DEL: K8, K9, K10, and K11

43.>Add: K15

SD -> SE

Page 10:

1.>Add F2 for safety request.

Page 13:

2.>Remove R335 for the driving high is not enough.

Page 27:

3.>DeL R567

Page 32:

4.>Change R97 from 64.R0185.A71 to 64.R0185781 because it might generate shortage due to the pad of compoment is too large

SE => -1

Page 7:

1.>Change VCC of 82440MX from 3D3V_S0 to 3D3V_S3.

2.>Change power plane of R139 from 5V_S0 to 5V_S3

3.>Change power plane of D9 from 3D3V_S0 to 3D3V_S3

Page 20:

4.>Reserve R569 and R570 to use different Codec.

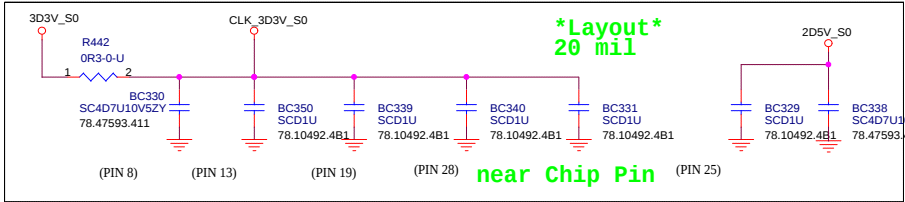
Page 22:

5.>Tune R380, R381, R383, and R383 for audio performance.

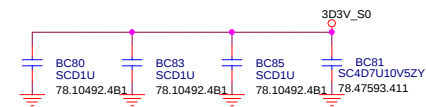
Page 30:

6.>Add U21D between U35 and U60C.

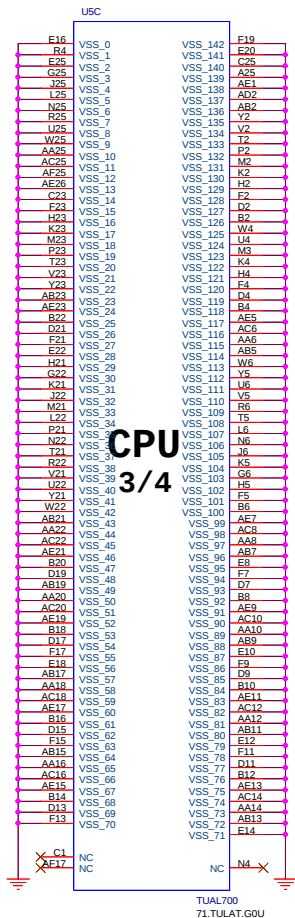
CPU CLOCK = 440BX CLOCK + 877 MILS
440BX CLOCK = 1.25 ~ 1.35 inches



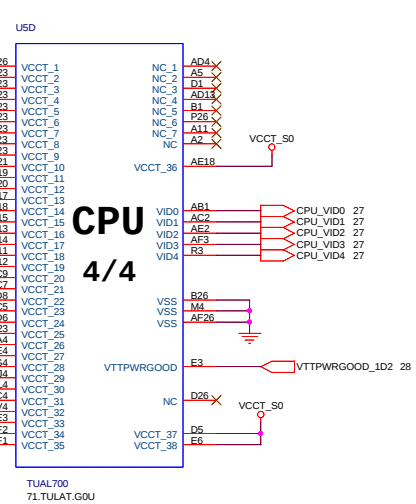
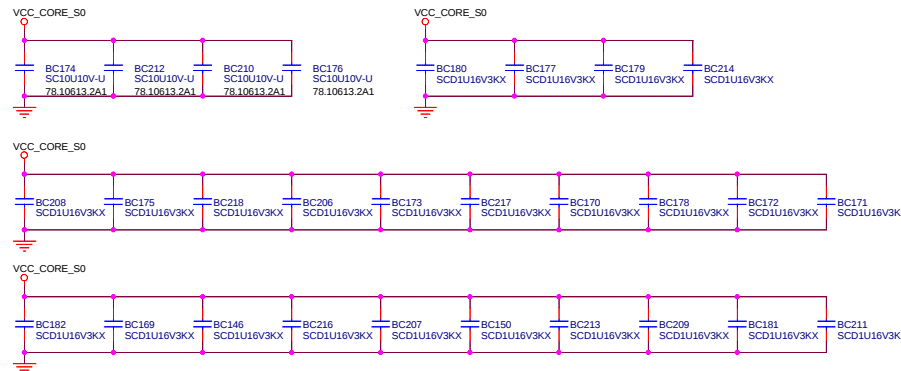
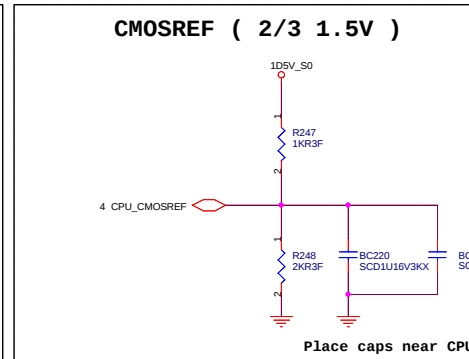
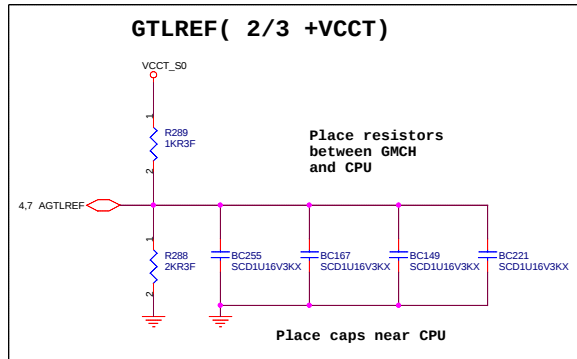
SDRAM Clock Buffer



FS2	FS1	CLKA[1..4]	CLKB[1..4]	CLKOUT	OUTPUT SOURCE	PLL SHUTDOWN
0	0	TRISTATE	TRISTATE	DRIVEN	PLL	N
0	1	DRIVEN	TRISTATE	DRIVEN	PLL	N
*1	0	DRIVEN	DRIVEN	DRIVEN	REF	Y
1	1	DRIVEN	DRIVEN	DRIVEN	PLL	N



CPU 3/4



CPU 4/4

Decoupling Recommendation

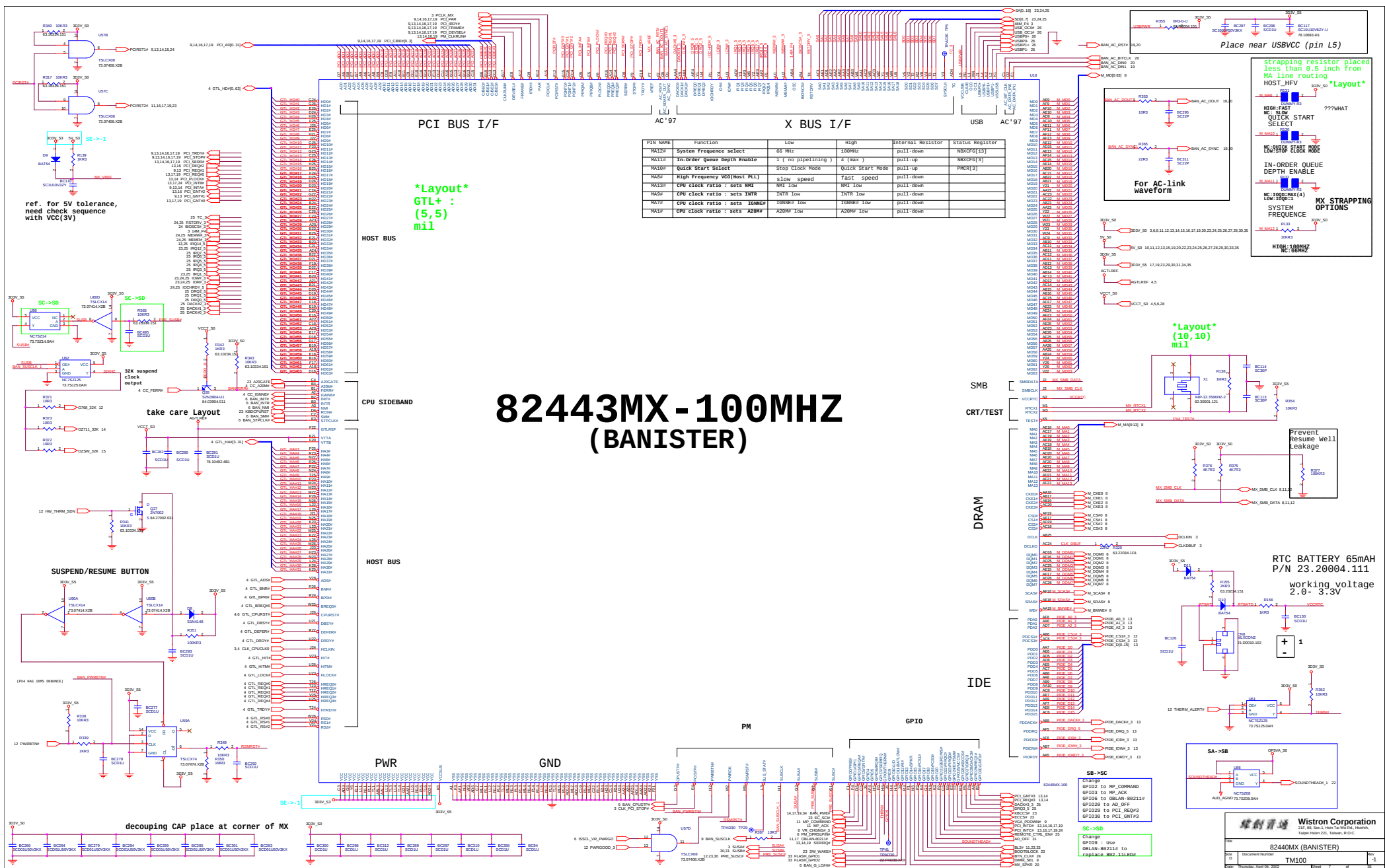
TM100

Ver. 0.1

VCC_CORE	Underneath balls on solder side	0.47uF * 24	Use 2-3 vias per pad for reduced inductance during layout	0.1uF * 24	10uF / 6.3V * 12
	On the peripheral near balls	10uF / 6.3V * 10	Placement should be near processor for all	10uF / 10V * 10	10uF / 6.3V * 10 + 6 * NS
	Bulk Caps			220uF / 2.5V * 8	150uF / 4V * 12 + 2 * NS
VCCT	Place close to processor for all Bulk Caps	1uF * 10	Use 2 vias per pad for reduced inductance during layout	1uF * 10	1uF * 10 + 2 * NS
				220uF / 2.5V * 2	150uF / 4V * 5 + 1 * NS

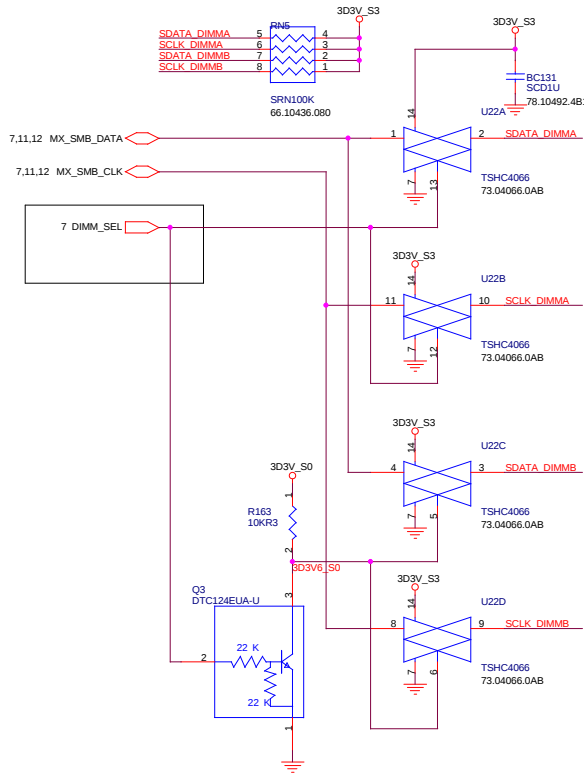
Almador-M Checklist Ver. 0.5 8/28

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
CPU 2/2 CONFIGURATION	
Size	Document Number
Custom	TM100
Date	Thursday, April 04, 2002
Sheet	5 of 95
Rev	-1

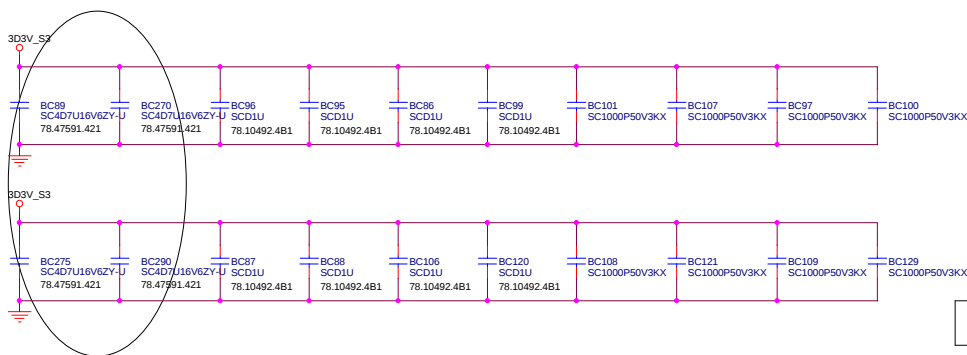


7 M_MA[0..13]
7 M_MD[0..63]
7 M_CS[0..3]
7 M_DQM[0..7]
7 M_CKE[0..3]

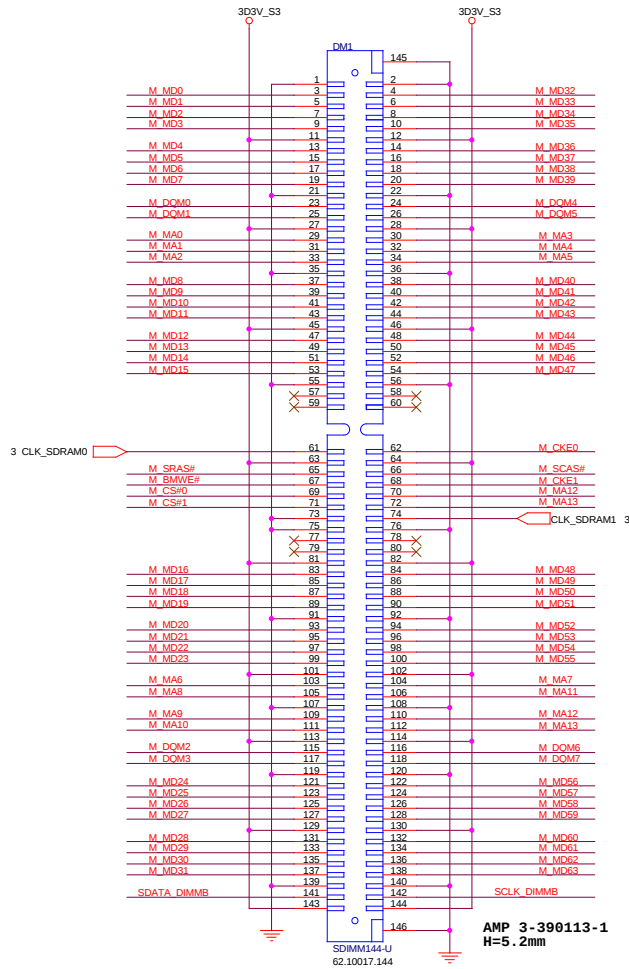
7 M_SCAS#
7 M_SRAS#
7 M_BMWE#



Cap. Height is too high

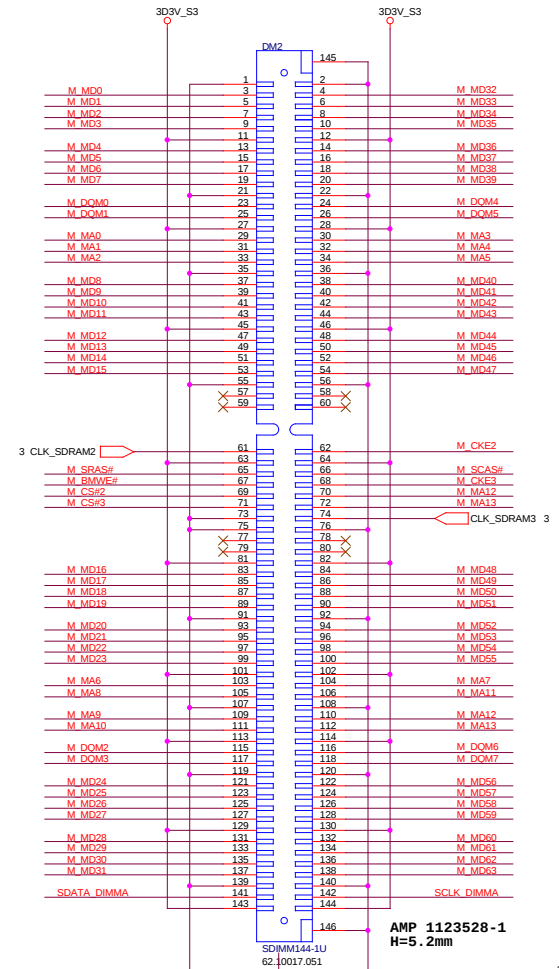


(Normal Type)



AMP 3-390113-1
H=5.2mm

(Reverse Type)

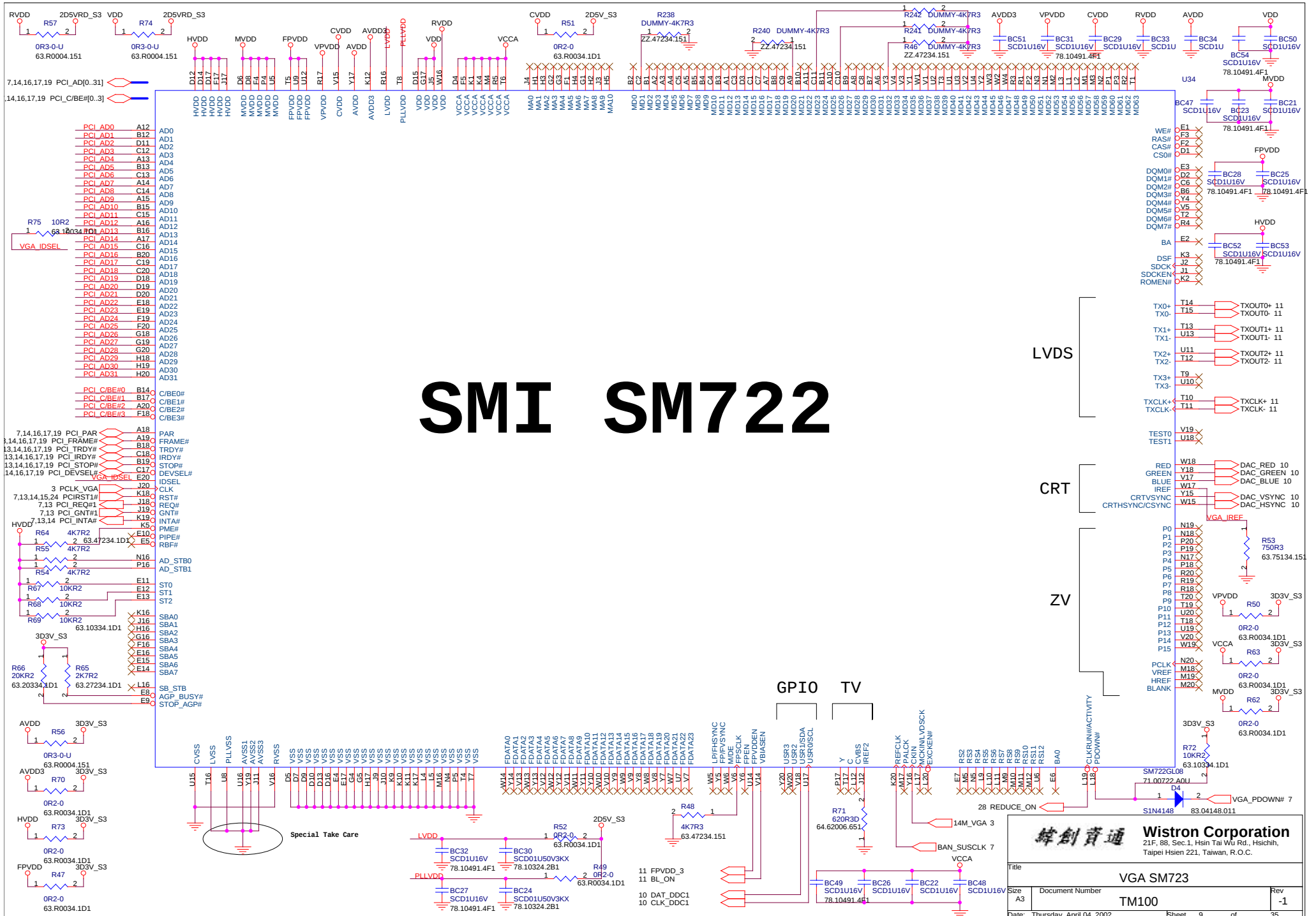


AMP 1123528-1
H=5.2mm

NOTE: NETWORK RESISTOR NEAR GMCH < 1.5 inch.

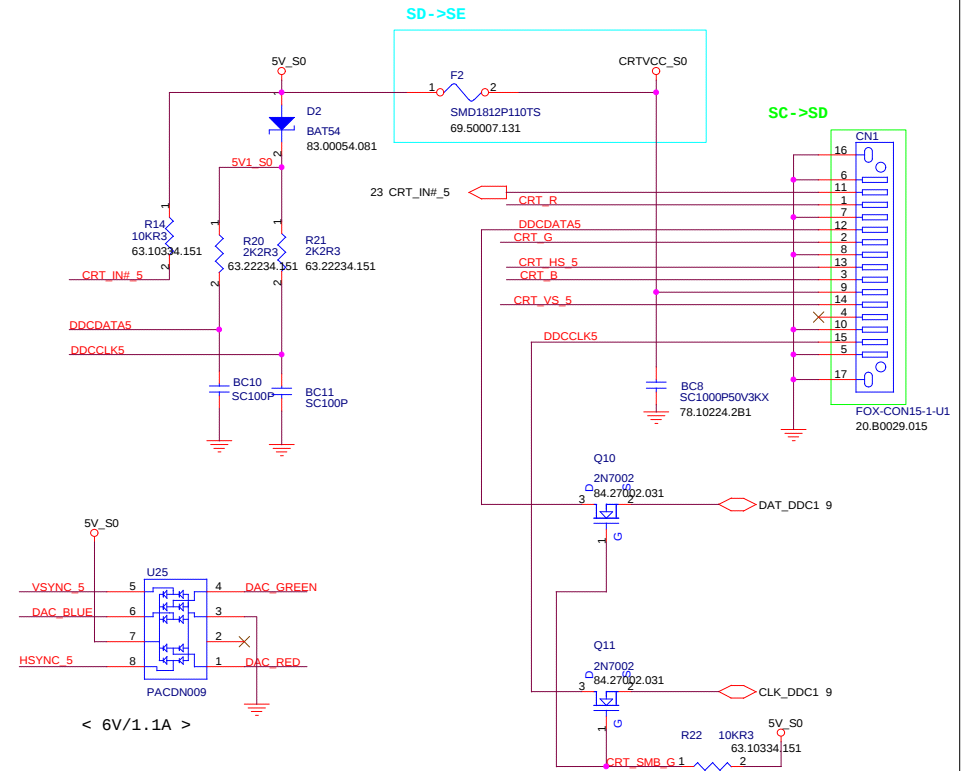
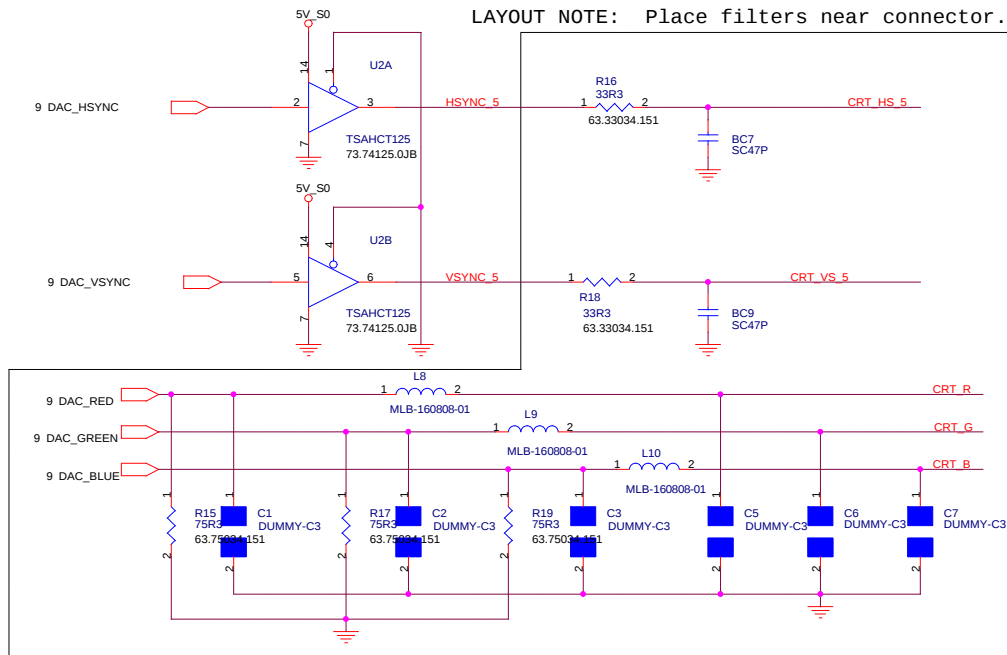
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
SO-DIMM		
Size	Document Number	Rev
Custom	TM100	-1
Date: Thursday, April 04, 2002	Sheet 8	of 95

SMI SM722



CRT

LAYOUT NOTE: Place filters near connector.



LVDS & DIGITIZER Connector

The diagram illustrates the electrical connections for the LVDS & DIGITIZER Connector. Key components and connections include:

- Connector (CN2 AMP-CONN30A-1):** A 33-pin connector with pins numbered 1 through 33.
- Power and Ground:**
 - 3D3V_S0:** Connected to pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, and 33.
 - LCDPWR_S0:** Connected to pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, and 32.
- Signal Lines:**
 - TXCLK- and TXCLK+:** Pins 1 and 3.
 - TXOUT2- and TXOUT2+:** Pins 9 and 11.
 - TXOUT1- and TXOUT1+:** Pins 2 and 4.
 - TXOUT0- and TXOUT0+:** Pins 10 and 12.
 - D_RX, D_DTR, and D_CTS:** Pins 25, 27, and 29.
 - D_TX and D_RTS:** Pins 23 and 25.
- Capacitors:**
 - BC43, BC42, BC41:** SC680P capacitors connected to ground.
 - BC44:** SC1000P50V3KX capacitor connected to ground.
 - BC162:** SC4D7U10V5ZY capacitor connected to ground.
 - BC161:** SCD1U capacitor connected to ground.
 - BC194:** SC680P capacitor connected to ground.
 - BC195:** SC680P capacitor connected to ground.
- Resistors:**
 - R522:** OR3-0-U 63.R0004.151 resistor connected between pins 1 and 2.
 - R223:** 10KR3 resistor connected between pins 7 and 8.
- Integrated Circuits:**
 - U32:** TPS2013D IC connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, and 33.
 - U58A:** TS1C14 IC connected to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, and 33.

INVERTER & LED & BUTTOM Connector

33 CHARGE_LED#
7,8,12 MX_SMB_DATA
7,8,12 MX_SMB_CLK
23 CAPS_LED#

24 PAGE_UP
24 PAGE_DN
24 TAKE_NOTE

CHARGE_LED#
MX_SMB_DATA
MX_SMB_CLK
CAPS_LED#

D_BRIGHTNESS#
PWR_LED#
INVERTER_3D3V_S0

5V_S5
3D3V_S0
3D3V_S3

ENTER_24
ALT_ESC_24

DCBATOUT

ENABLE
HDD_LED#
NUM_LED#
M+3V_LED

HDD_LED# 13
NUM_LED# 23

R02_I1_LED#
S1D0Y_LED#
BRIGHTNESS

BRIGHTNESS 23

BC236 DUMMY-C3
BC242 DUMMY-C3
BC233 DUMMY-C3
BC235 DUMMY-C3
BC239 DUMMY-C3
BC240 DUMMY-C3
BC231 DUMMY-C3
BC234 DUMMY-C3
BC241 DUMMY-C3
BC237 DUMMY-C3
BC239 ZZ.DUMMY.XC3
DUMMY-C3

SB->SC
R545
10K R3
63.10334.151

9 BL_ON
23 BACKLIGHT_OFF#

57A
TSLCX08
73.07408.X2B

SC->SD
R564
33R3
63.33034.151

3D3V_S0
R318
10K R3

SC->SD

Micro Processor for Bat. Low LED

The diagram shows the internal circuitry of the Micro Processor for Bat. Low LED, including the PIC12C508-1 microcontroller, various capacitors, and power supply connections. The circuit is divided into two main sections: SB->SC and SC->SD.

SB->SC: This section includes the PIC12C508-1 microcontroller, a 7.23.33 capacitor, and a 23 1HZ capacitor. It also shows the connection to the 3D3V_S3 power supply and the 5V_S0 power supply. The microcontroller is connected to the 3D3V_S3 power supply via a 7.23.33 capacitor and to the 5V_S0 power supply via a 23 1HZ capacitor. The microcontroller is also connected to the 3D3V_S3 power supply via a 7.23.33 capacitor and to the 5V_S0 power supply via a 23 1HZ capacitor.

SC->SD: This section includes the PIC12C508-1 microcontroller, a 7.23.33 capacitor, and a 23 1HZ capacitor. It also shows the connection to the 3D3V_S3 power supply and the 5V_S0 power supply. The microcontroller is connected to the 3D3V_S3 power supply via a 7.23.33 capacitor and to the 5V_S0 power supply via a 23 1HZ capacitor. The microcontroller is also connected to the 3D3V_S3 power supply via a 7.23.33 capacitor and to the 5V_S0 power supply via a 23 1HZ capacitor.

Power Table:

	(GP036) E_MAIL	(GP107) STDBY	(GP1015) ENSTDBY#_S	SPLD	Standby_LED	E_mail_LED
POWER ON DEFAULT	H	H	H	L	OFF	OFF
S0 without E_mail LED	L	H	H	Flash	OFF	OFF
S0 with E_mail LED	H	H	H	Flash	OFF	Flash
S1 without E_mail LED	L	L	L	Flash	ON	OFF
S1 with E_mail LED	L/H	L	L	Flash	ON	OFF/Flash (Decide by BIOS)
Enter/Leave S3 without E_mail LED	L	H	L	Flash	Flash	OFF
Enter/Leave S3 with E_mail LED	L	H	L	Flash	Flash	OFF
S3	L	L	L	L	ON	OFF
Enter/Leave S4 without E_mail LED	L	H	L	Flash	Flash	Flash
Enter/Leave S4 with E_mail LED	L	H	L	Flash	Flash	OFF
S4	L	L	NO POWER	L	OFF	OFF

* Standby_LED is made by OFF_Pwr1, GP1015, SPLD
* E_mail_LED is made by OFF_Pwr1, SPLD

	(GP036) E_MAIL	(GP107) STDBY	(GP1015) ENSTDY#_5	SPLED	Standby_LED	E_mail_LED
POWER ON DEFAULT	H	H	H	L	OFF	OFF
S0 without E_mail LED	L	H	H	Flash	OFF	OFF
S0 with E_mail LED	H	H	H	Flash	ON	Flash
S1 without E_mail LED	L	L	L	Flash	ON	OFF
S1 with E_mail LED	L/H	L	L	Flash	ON	OFF/Flash
Enter/Leave S3 without E_mail LED	L	H	L	Flash	Flash	OFF (Decide by BIOS)
Enter/Leave S3 with E_mail LED	L	H	L	Flash	Flash	OFF
S3	L	L	L	L	ON	OFF
Enter/Leave S4 without E_mail LED	L	H	L	Flash	Flash	
Enter/Leave S4 with E_mail LED	L	H	L	Flash	Flash	OFF
S4	L	L	NO POWER	L	OFF	OFF

```
* Standby_LED is made by OFF_Pwr1,GPI015,SPLED
* E_mail_LED is made by OFF_Pwr1,SPLED
```

**Change To
G913C(Fixed Mode)**

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,

Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD POWER,INVERTER
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Size	Document Number
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A3	TM100
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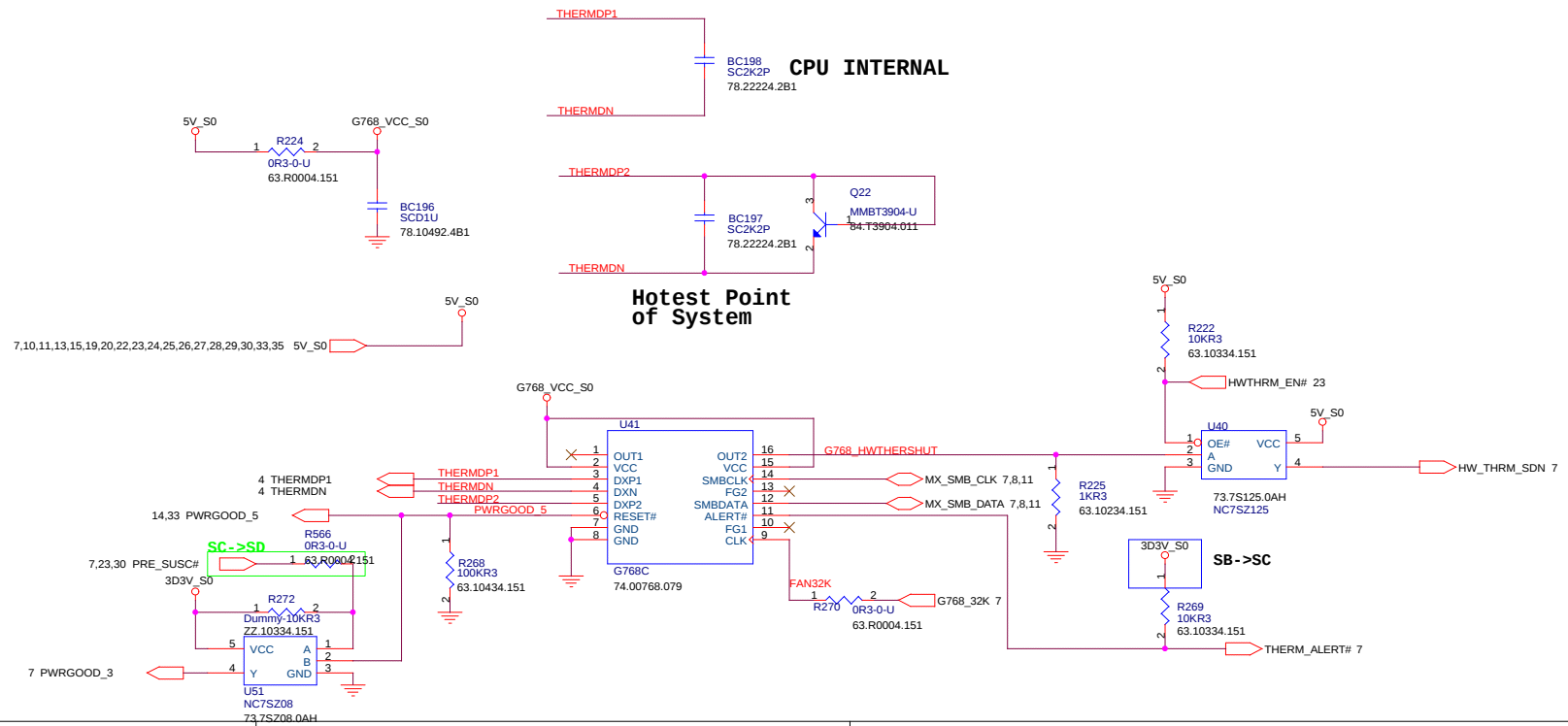
Date: Thursday, April 04, 2002

Date: Thursday, April 04, 2002

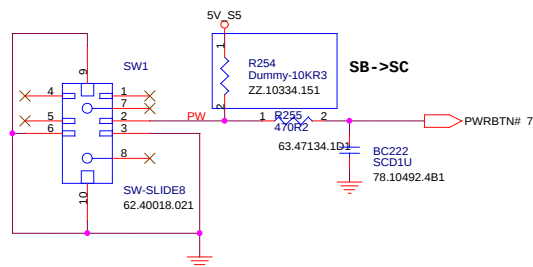
Sheet 11 of 25

Sheet 11 of 35

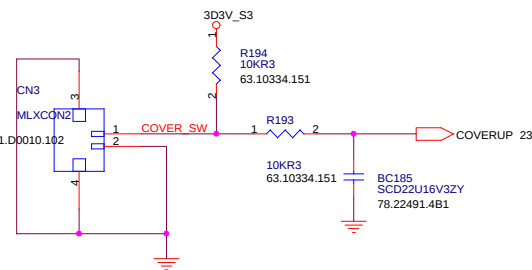
THERMAL SENSOR & FAN CONTROLLER



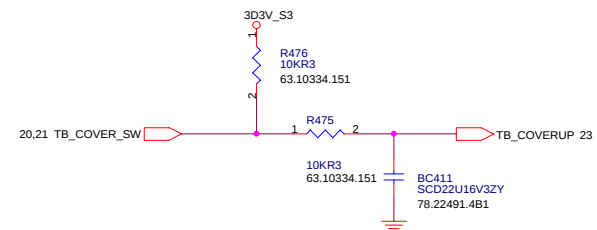
POWER SWITCH



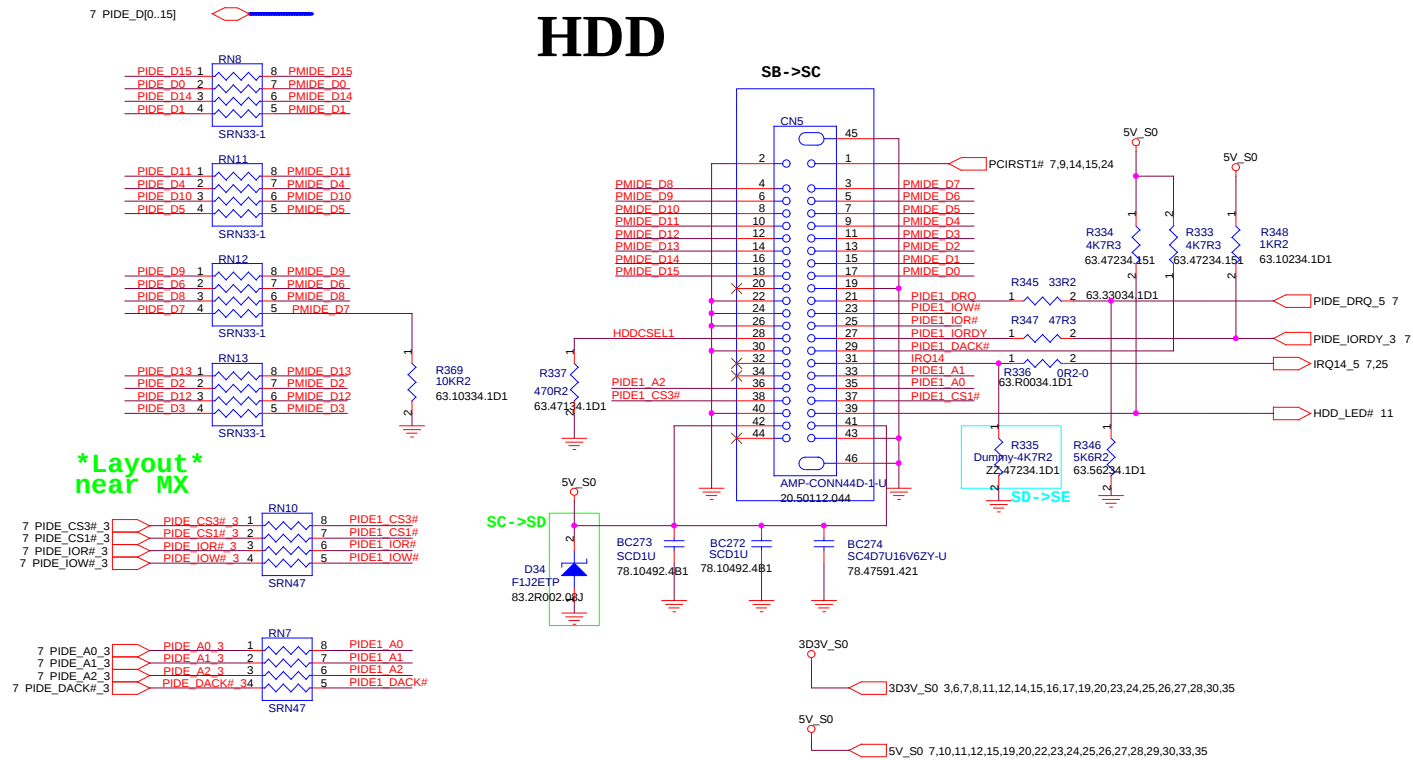
COVER SWITCH



TABLET COVER SWITCH

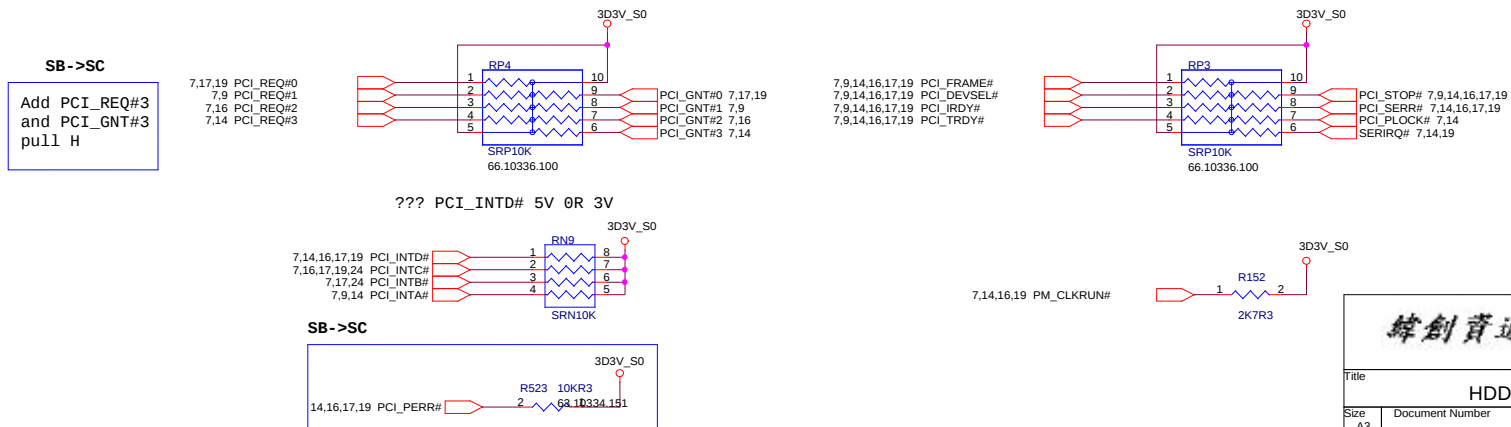


緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title THERMALSENSOR		
Size A3	Document Number TM100	Rev -1
Date: Thursday, April 04, 2002 Sheet 12 of 35		

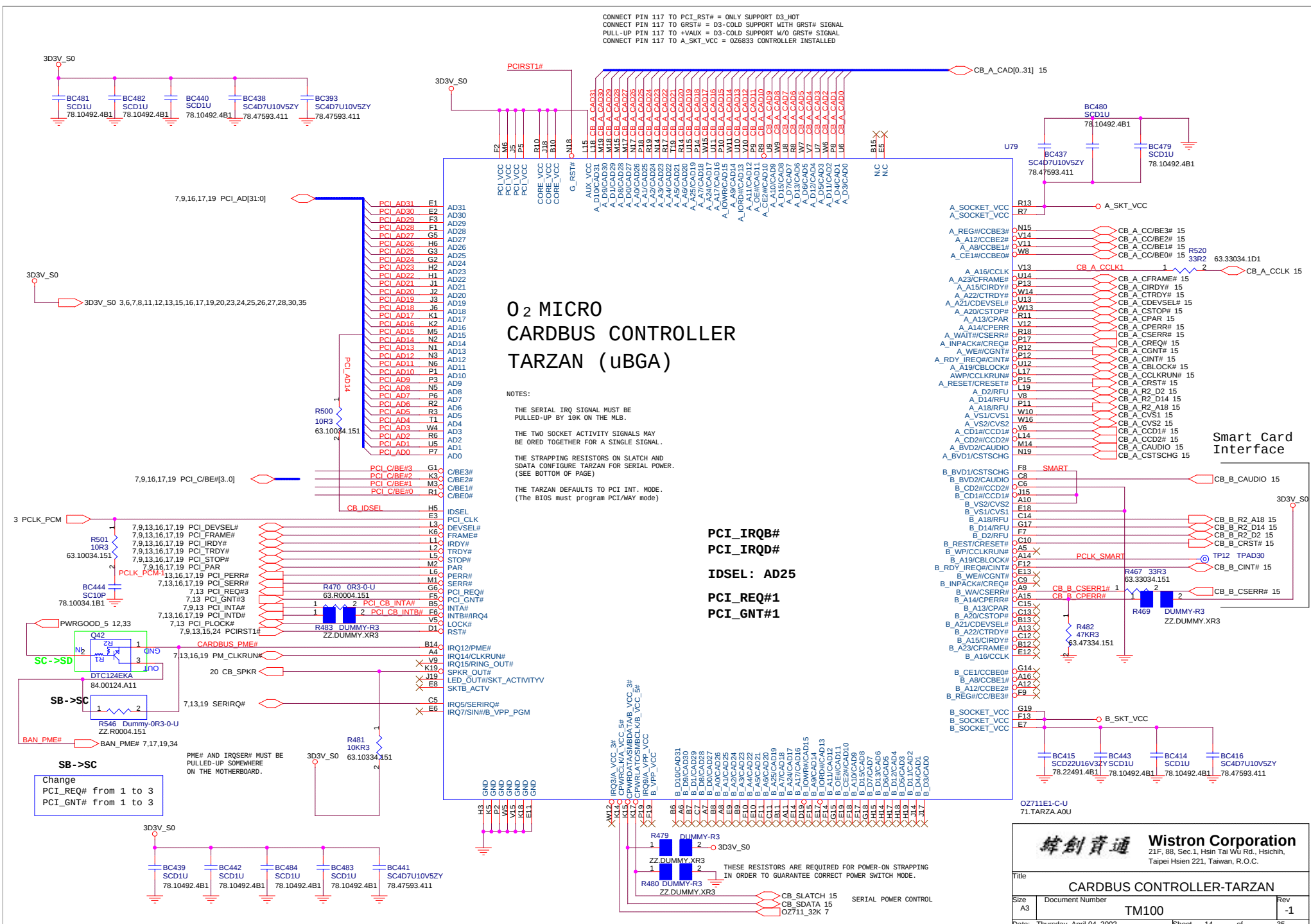


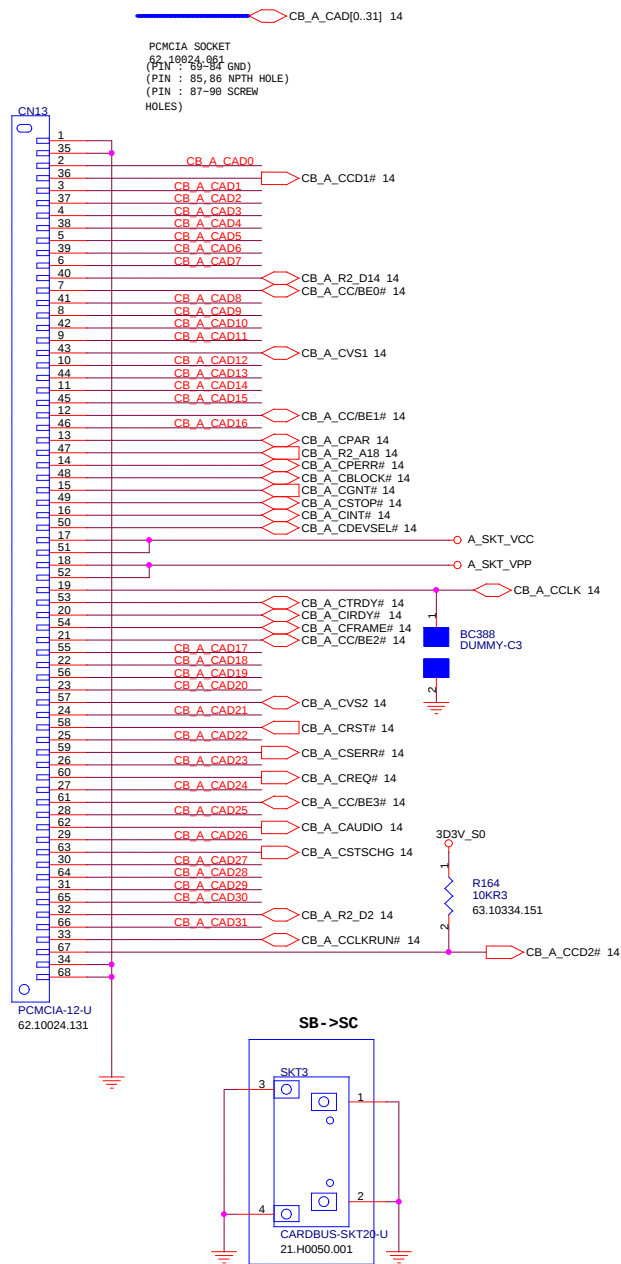
PCI Pull High Resister

REQ3/ GNT3 used as GPIO29/30

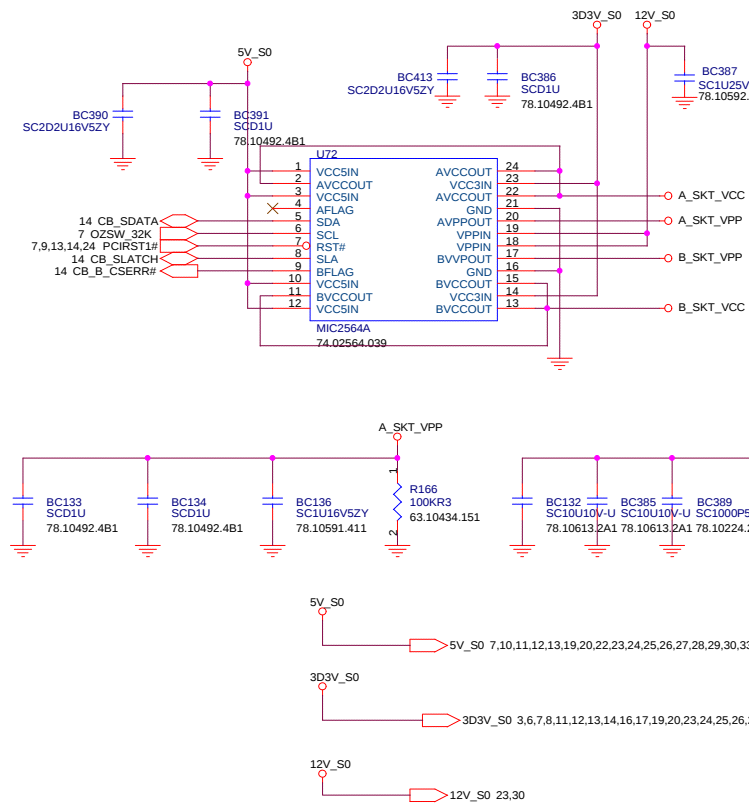
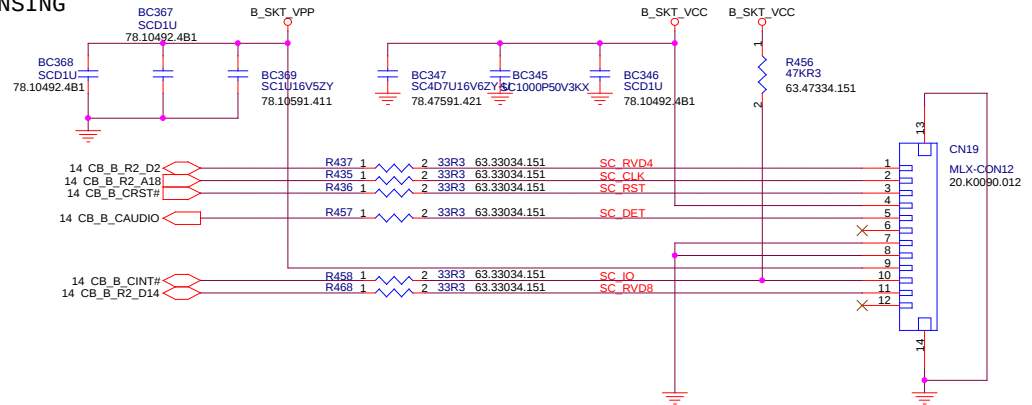


緯創資通		Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
HDD & PCI PH Resistors			
Size A3	Document Number TM100	Rev -1	
Date: Thursday, April 04, 2002		Sheet 13	of 35





SMART CARD INTERFACE SMARTSENSING

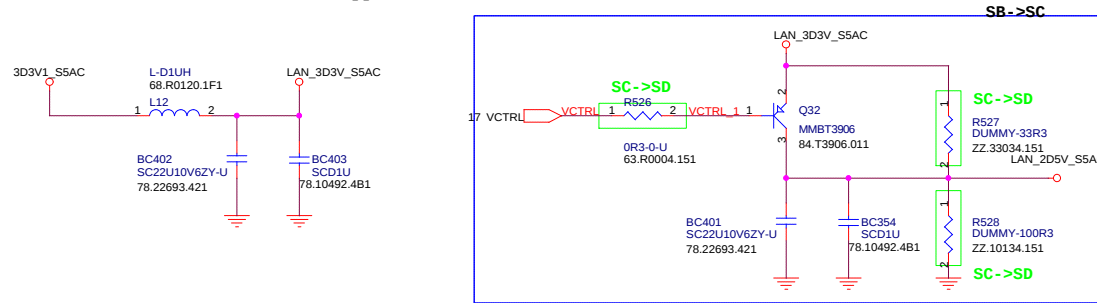


Take Care Cap. Voltage Rating
VCC for 3.3V/5V
VPP for 12V

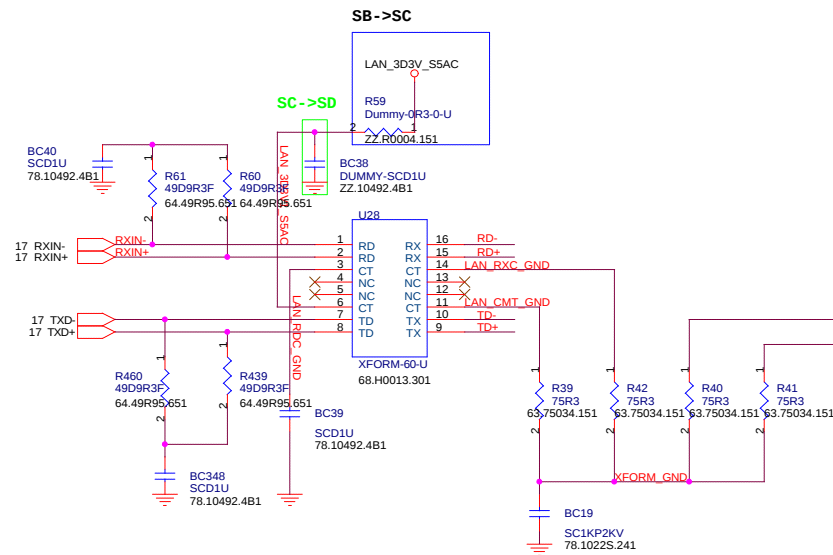
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
SOCKET/Smart Card Interface			
Size	Document Number		Rev
A3	TM100		-1
Date:	Thursday, April 04, 2002	Sheet 15 of	35

*For RTL8100 application, all bead must be rated 300mA/100ohm@100MHz



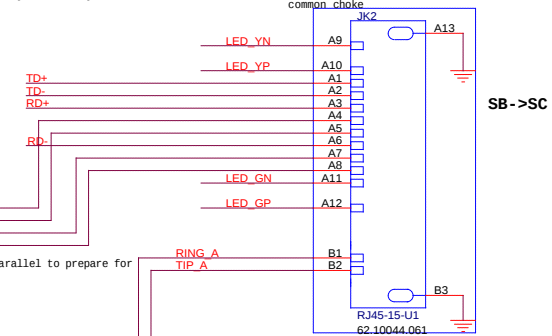
The components of this region are reserved for future use. Please reserve the component space and pads in your layout for future extension.



The components of this region are reserved for future use. Please reserve the component space and pads in your layout for future extension.

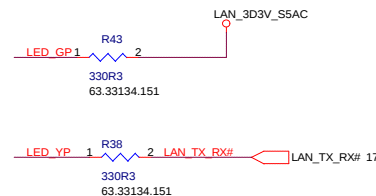
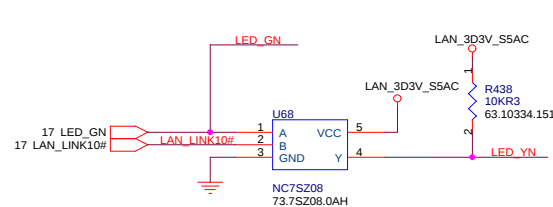
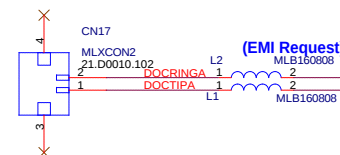
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

put two resistor in parallel to prepare for common choke



SB->SC

RJ11 signal must leave the other signal or power plane 100mil.



LEDS1-0	00	01	10	11
LED0	TX/RX	TX/RX	TX	TX
LED1	LINK100	LINK10/100	LINK10/100	LINK100
LED2	LINK10	FULL	RX	LINK10

Green LED:Speed 100: ON/Speed 10:OFF
Yellow LED:Link : ON, TX/RX: Flash(10Hz)

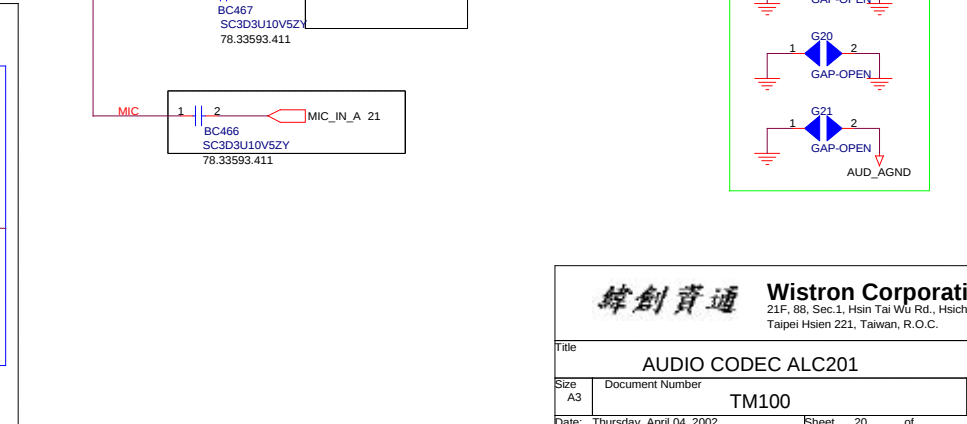
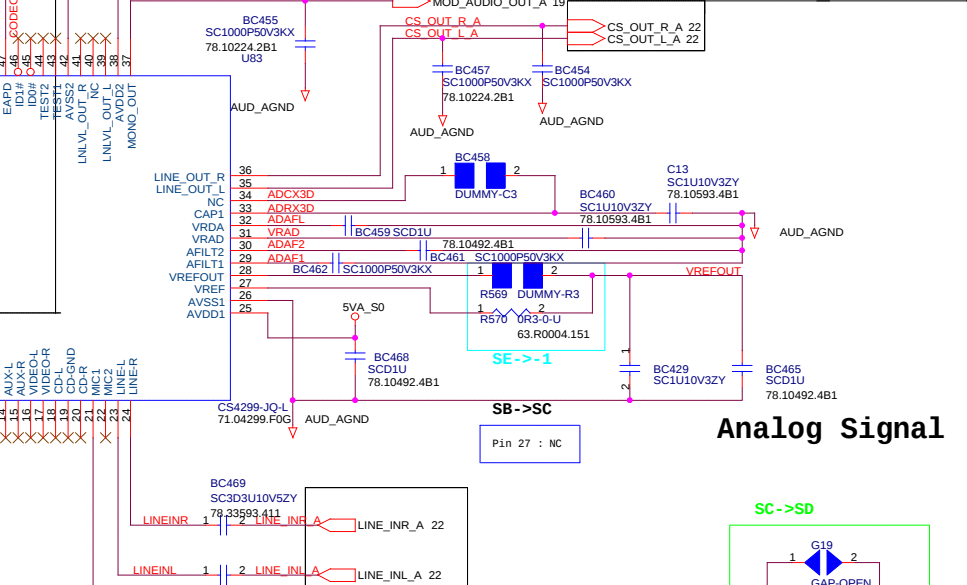
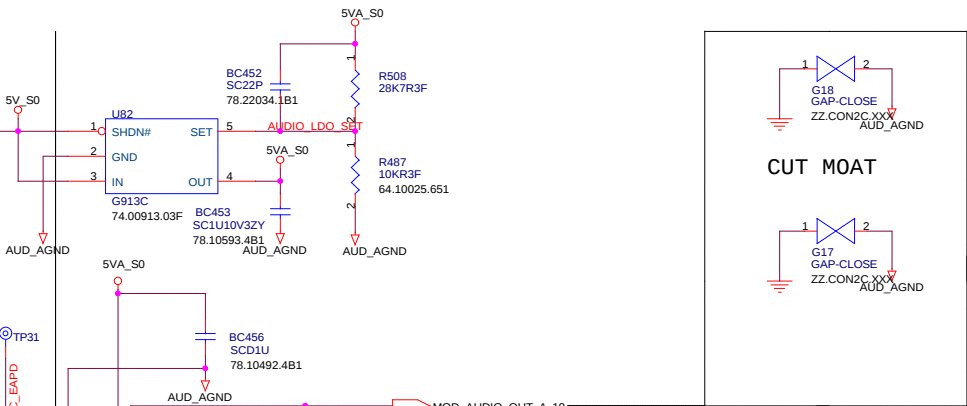
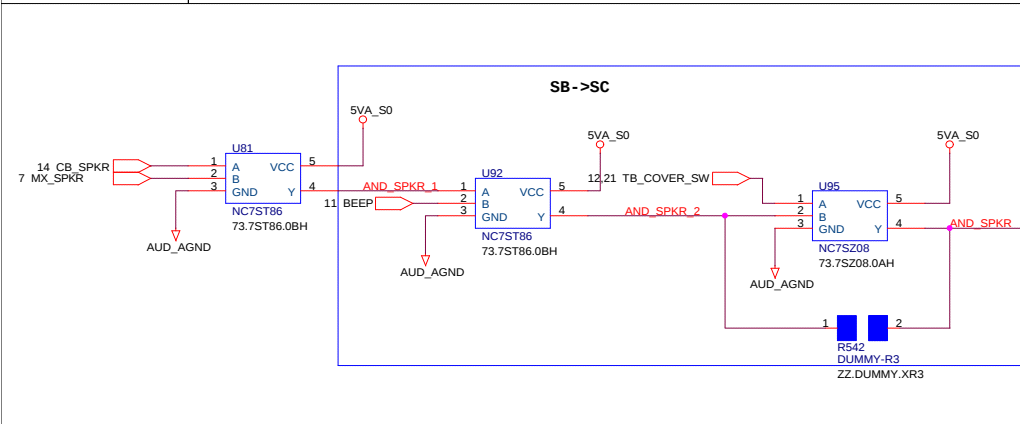
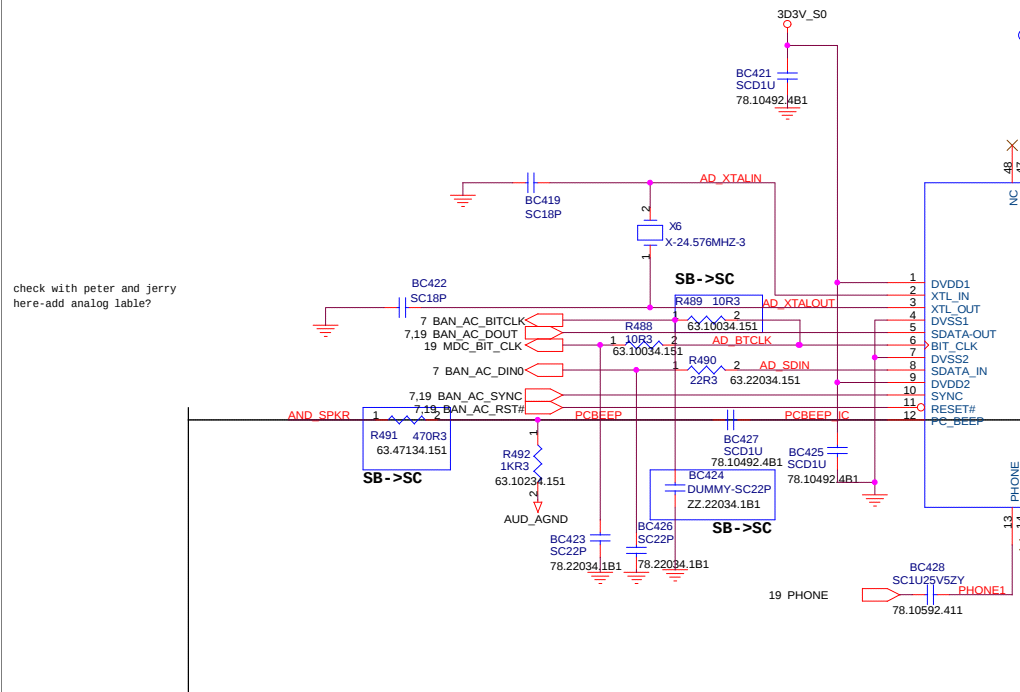
MODEM BOARD CONNECTOR

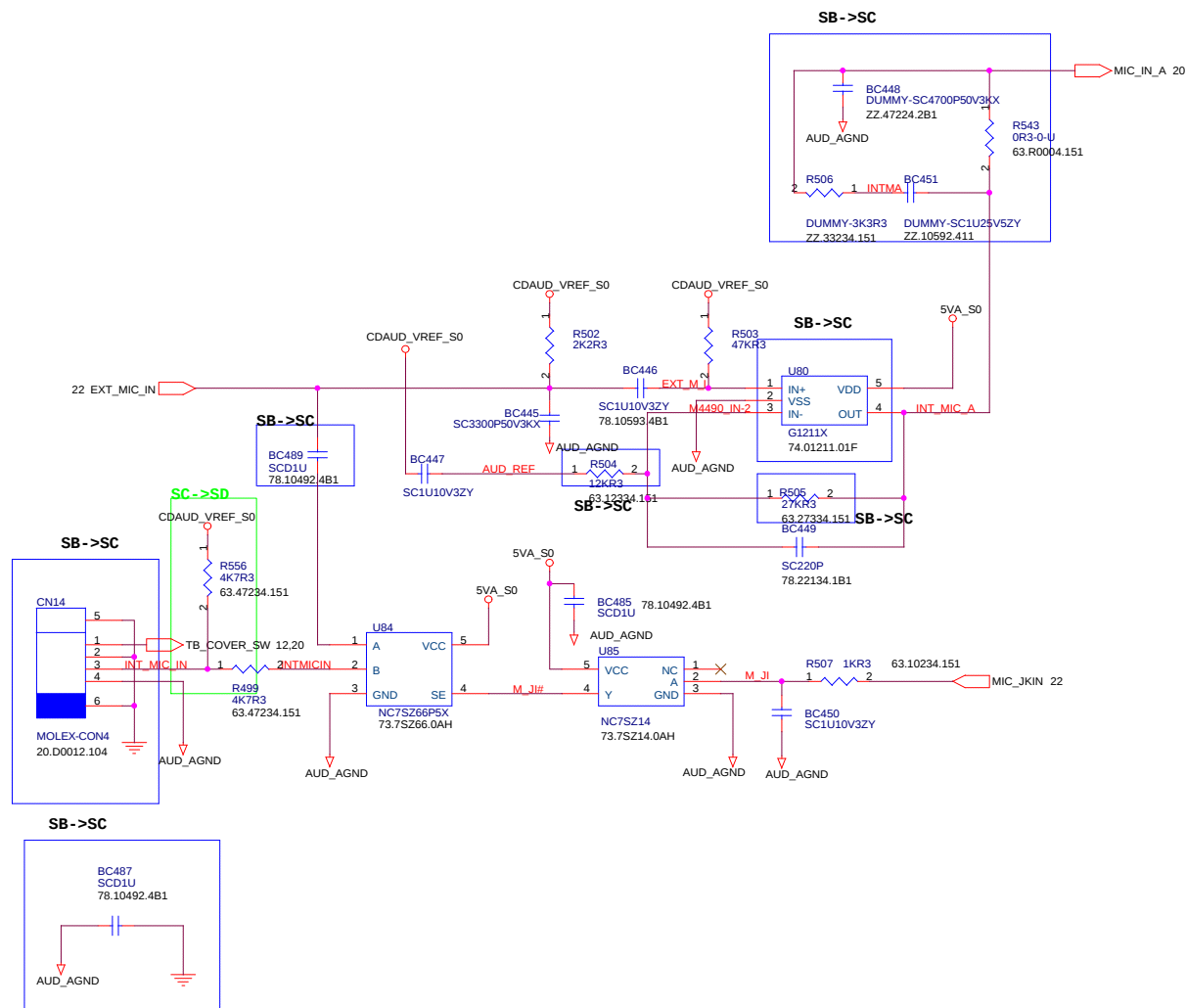
The diagram illustrates the electrical connections for a modem board. Key components and connections include:

- Power and Grounding:**
 - 3D3V_S5AC and AC97_3V are connected to the board.
 - 3D3V_S0 is connected to the board.
 - AC97_5V is connected to the board.
 - 5V_S0 is connected to the board.
 - MDC_GND is connected to the board.
 - SB->SC is connected to the board.
- Connectors:**
 - CN6: A multi-pin connector with pins 1-34.
 - CN9: A 2-pin connector.
 - CN10: A 2-pin connector.
 - CN11: A 2-pin connector.
 - CN12: A 2-pin connector.
 - CN13: A 2-pin connector.
 - CN14: A 2-pin connector.
 - CN15: A 2-pin connector.
 - CN16: A 2-pin connector.
 - CN17: A 2-pin connector.
 - CN18: A 2-pin connector.
 - CN19: A 2-pin connector.
 - CN20: A 2-pin connector.
 - CN21: A 2-pin connector.
 - CN22: A 2-pin connector.
 - CN23: A 2-pin connector.
 - CN24: A 2-pin connector.
 - CN25: A 2-pin connector.
 - CN26: A 2-pin connector.
 - CN27: A 2-pin connector.
 - CN28: A 2-pin connector.
 - CN29: A 2-pin connector.
 - CN30: A 2-pin connector.
 - CN31: A 2-pin connector.
 - CN32: A 2-pin connector.
 - CN33: A 2-pin connector.
 - CN34: A 2-pin connector.
 - CN35: A 2-pin connector.
 - CN36: A 2-pin connector.
 - CN37: A 2-pin connector.
 - CN38: A 2-pin connector.
 - CN39: A 2-pin connector.
 - CN40: A 2-pin connector.
 - CN41: A 2-pin connector.
 - CN42: A 2-pin connector.
 - CN43: A 2-pin connector.
 - CN44: A 2-pin connector.
 - CN45: A 2-pin connector.
 - CN46: A 2-pin connector.
 - CN47: A 2-pin connector.
 - CN48: A 2-pin connector.
 - CN49: A 2-pin connector.
 - CN50: A 2-pin connector.
 - CN51: A 2-pin connector.
 - CN52: A 2-pin connector.
 - CN53: A 2-pin connector.
 - CN54: A 2-pin connector.
 - CN55: A 2-pin connector.
 - CN56: A 2-pin connector.
 - CN57: A 2-pin connector.
 - CN58: A 2-pin connector.
 - CN59: A 2-pin connector.
 - CN60: A 2-pin connector.
 - CN61: A 2-pin connector.
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 - CN66: A 2-pin connector.
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 - CN73: A 2-pin connector.
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 - CN79: A 2-pin connector.
 - CN80: A 2-pin connector.
 - CN81: A 2-pin connector.
 - CN82: A 2-pin connector.
 - CN83: A 2-pin connector.
 - CN84: A 2-pin connector.
 - CN85: A 2-pin connector.
 - CN86: A 2-pin connector.
 - CN87: A 2-pin connector.
 - CN88: A 2-pin connector.
 - CN89: A 2-pin connector.
 - CN90: A 2-pin connector.
 - CN91: A 2-pin connector.
 - CN92: A 2-pin connector.
 - CN93: A 2-pin connector.
 - CN94: A 2-pin connector.
 - CN95: A 2-pin connector.
 - CN96: A 2-pin connector.
 - CN97: A 2-pin connector.
 - CN98: A 2-pin connector.
 - CN99: A 2-pin connector.
 - CN100: A 2-pin connector.
- Resistors:**
 - R361: 10k
 - R362: 10k
 - R363: 10k
 - R364: 10k
 - R365: 10k
 - R366: 10k
 - R367: 10k
 - R368: 10k
 - R369: 10k
 - R370: 10k
 - R371: 10k
 - R372: 10k
 - R373: 10k
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 - R488: 10k
 - R489: 10k
 - R490: 10k
 - R491: 10k
 - R492: 10k
 - R493: 10k
 - R494: 10k
 - R495: 10k
 - R496: 10k
 - R497: 10k
 - R498: 10k
 - R499: 10k
 - R500: 10k
- Capacitors:**
 - C9: SC4D7U10V5ZY
 - C10: SCD1U
 - C11: SCD1U
 - C12: SCD1U
 - C13: SCD1U
 - C14: SCD1U
 - C15: SCD1U
 - C16: SCD1U
 - C17: SCD1U
 - C18: SCD1U
 - C19: SCD1U
 - C20: SCD1U
 - C21: SCD1U
 - C22: SCD1U
 - C23: SCD1U
 - C24: SCD1U
 - C25: SCD1U
 - C26: SCD1U
 - C27: SCD1U
 - C28: SCD1U
 - C29: SCD1U
 - C30: SCD1U
 - C31: SCD1U
 - C32: SCD1U
 - C33: SCD1U
 - C34: SCD1U
 - C35: SCD1U
 - C36: SCD1U
 - C37: SCD1U
 - C38: SCD1U
 - C39: SCD1U
 - C40: SCD1U
 - C41: SCD1U
 - C42: SCD1U
 - C43: SCD1U
 - C44: SCD1U
 - C45: SCD1U
 - C46

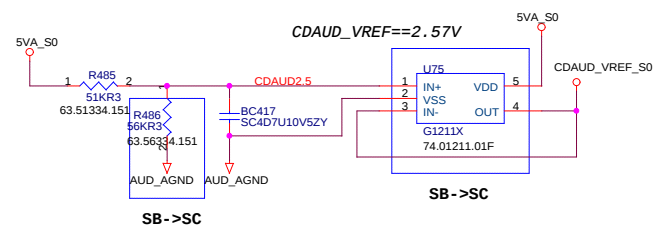
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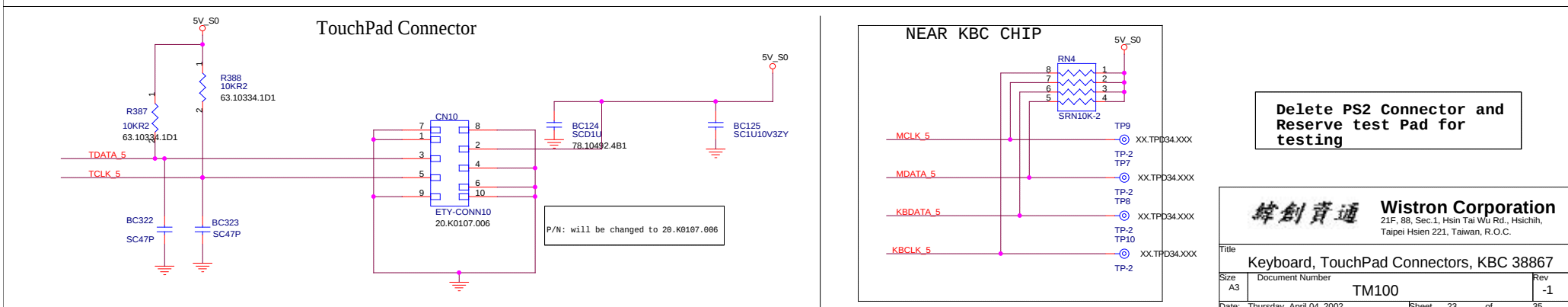
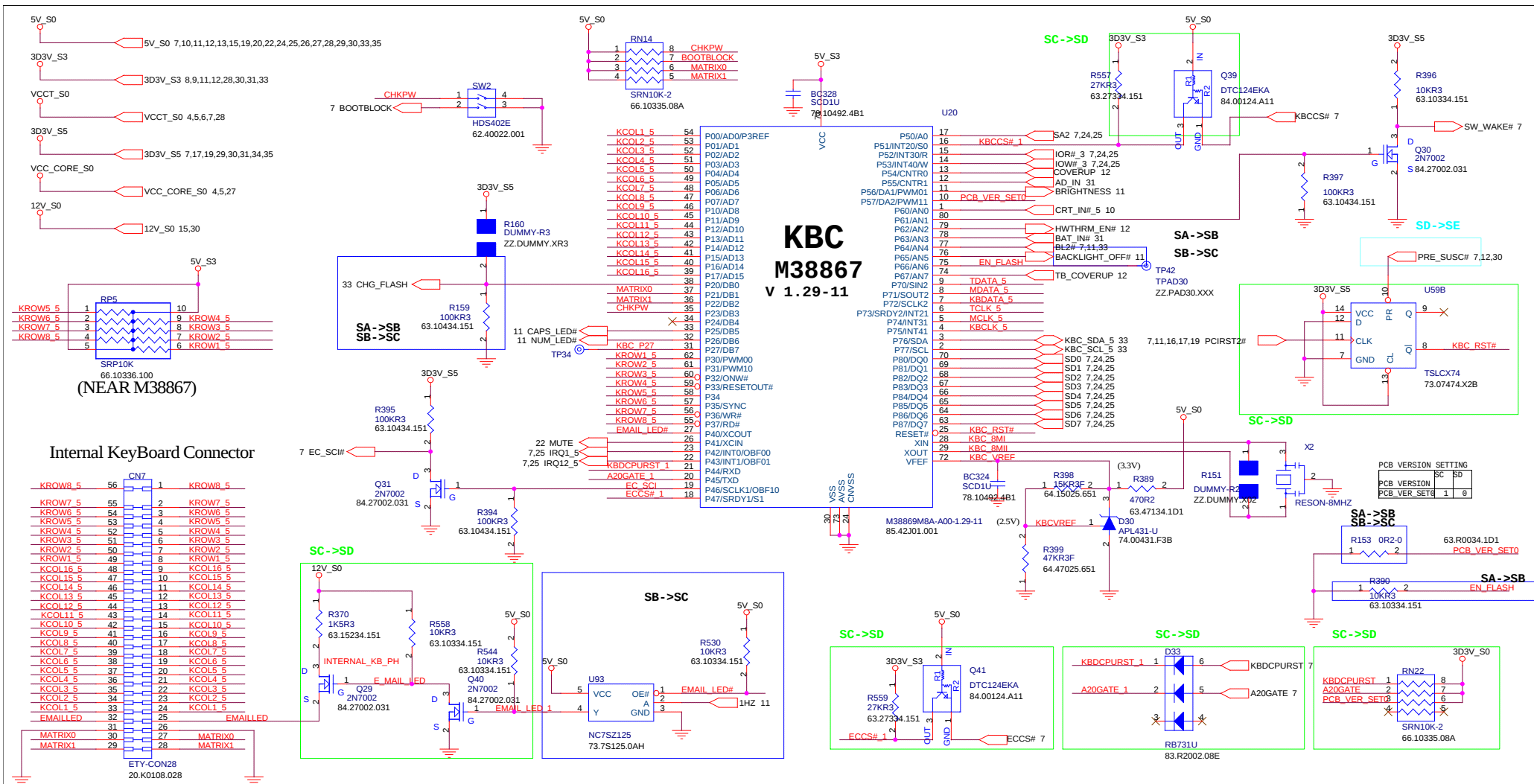
Digital Signal

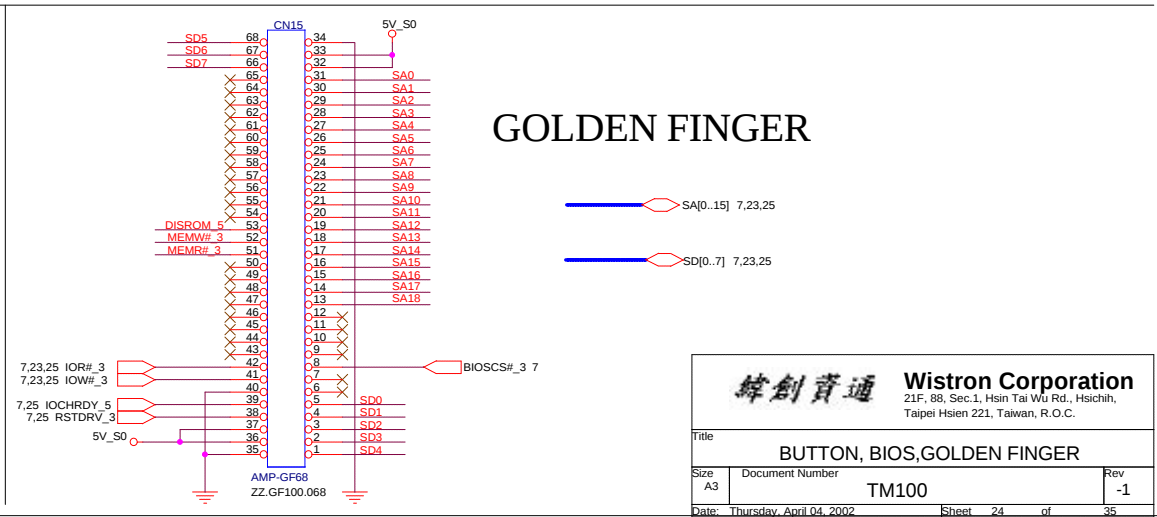
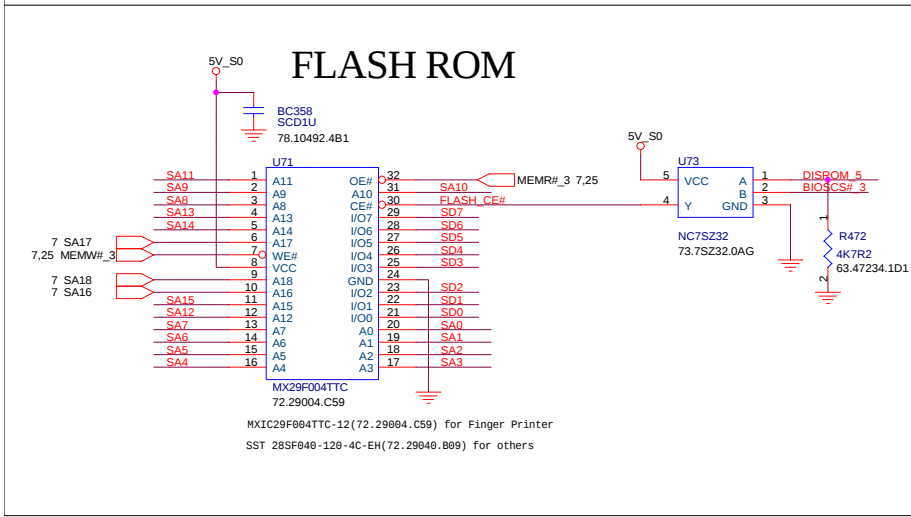
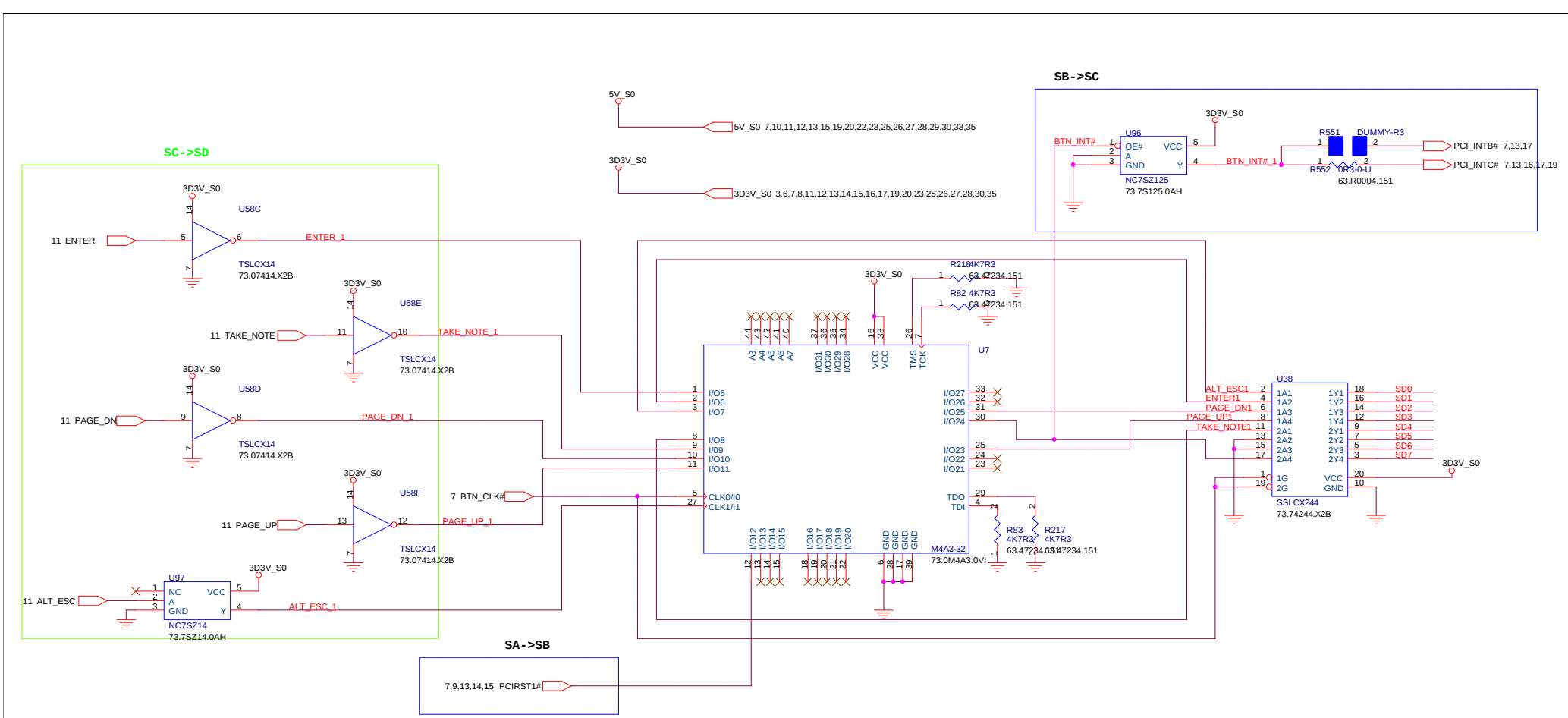




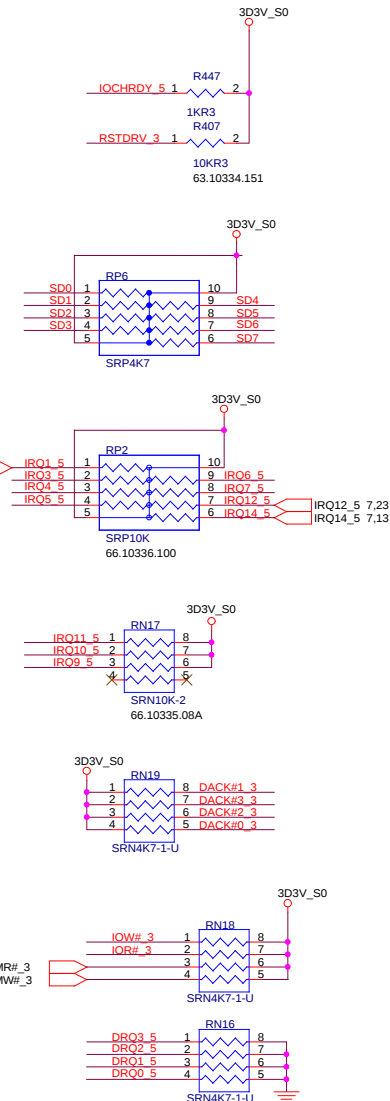
Internal System Microphone Pre_Amp /near CN4

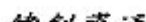


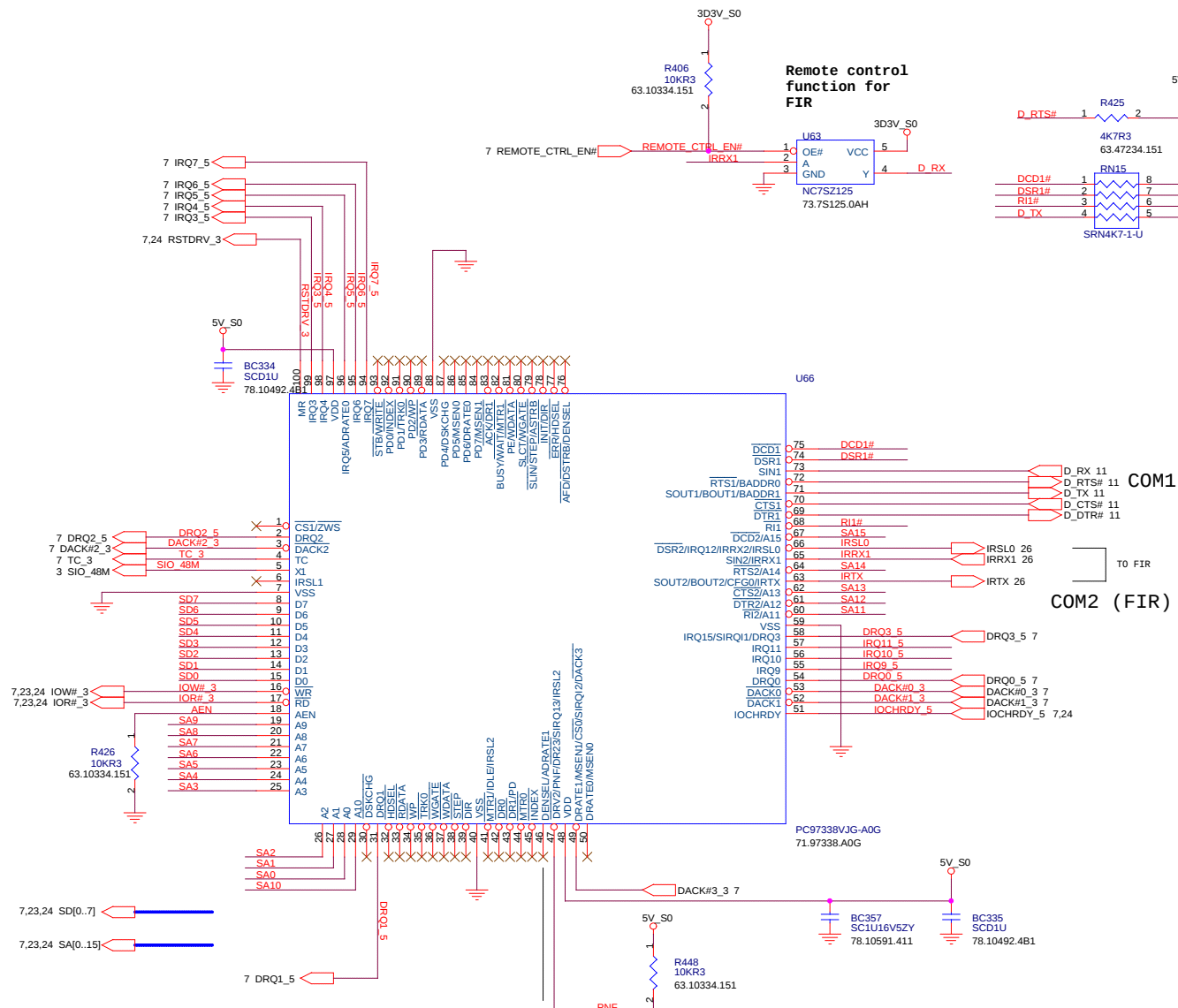




ISA Pull High/Low



		Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
SUPER IO 97338 & ISA PH/PL			
Size A3	Document Number TM100	Rev -1	
Date: Thursday, April 04, 2002		Sheet 25 of 35	



USB PORT



Mode	Tualitin	Copermine-T	Celeron-T	Tualitin-UTL
PERFORMANCE	1.4V	1.70V	1.70V	1.1V
BATTERY	1.15V	1.35V	1.35V	0.95V
Deeper Sleep	0.85V	Non	Non	0.85V

Input	Output
Low	ON
High	OFF

D4	D3	D2	D1	D0	Vout (V)
0	0	0	0	0	1.75
0	0	0	0	1	1.70
0	0	0	1	0	1.65
0	0	0	1	1	1.60
0	0	1	0	0	1.55
0	0	1	0	1	1.50
0	0	1	1	0	1.45
0	0	1	1	1	1.40
0	1	0	0	0	1.35
0	1	0	0	1	1.30
0	1	0	1	0	1.25
0	1	0	1	1	1.20
0	1	1	0	0	1.15
0	1	1	0	1	1.10
0	1	1	1	0	1.05
0	1	1	1	1	1.00

S1	S0	Vout (V)
GND	GND	0.975
GND	REF	0.950
GND	Float	0.925
GND	VCC	0.900
REF	GND	0.875
REF	REF	0.850
REF	Float	0.825
REF	VCC	0.800
Float	GND	0.775
Float	REF	0.750
Float	Float	0.725
Float	VCC	0.700
VCC	GND	0.675
VCC	REF	0.650
VCC	Float	0.625
VCC	VCC	0.600

ZMODE	SUS	Vout Determined by:
GND	GND	Logic Level of D0 - D4
VCC	GND	Impedance of D0 - D4
X	VCC	Logic Level of S0, S1

For ZMODE=High
Set CPU Voltage 1.1V
D[4:0]=[01101]

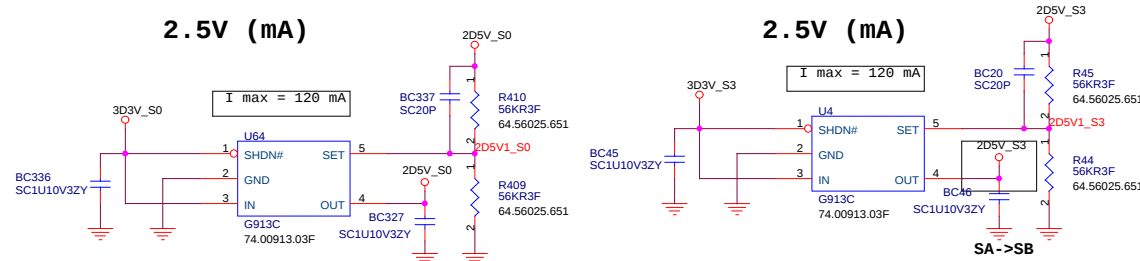
For ZMODE=Low
Set CPU Voltage 0.95V
D[4:0]=[10001]

ZMODE Defined Level-Judge Method
If ZMODE=Low, Set D[4..0] by Voltage-Level in wire
If ZMODE=High, Set D[4..0] by R (resistor)
R=100kOhm, High
R=10kOhm, Low

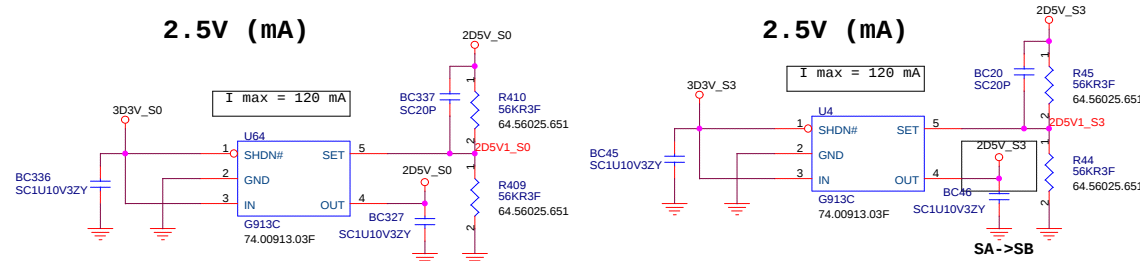
Offset Truth Table

PM_DPRSLPVR	CC_DPSLP#	CORE_ZMODE	Voffset
1	X	X	0mV
0	0	0	-59mV
0	0	1	-52mV
0	1	0	-29mV
0	1	1	-3mV

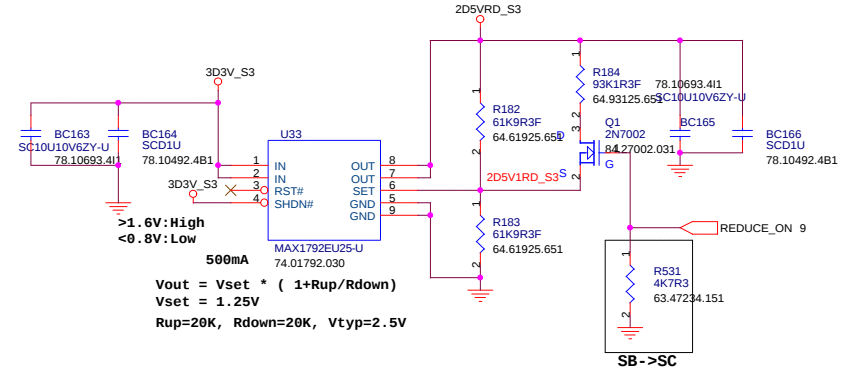
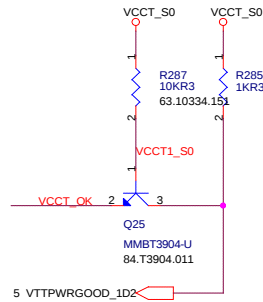
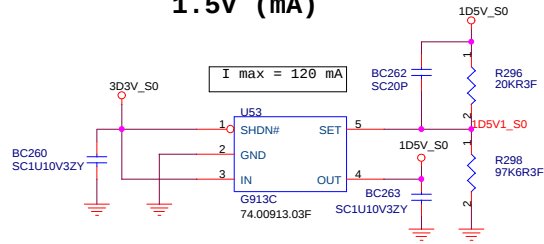
2.5V (mA)



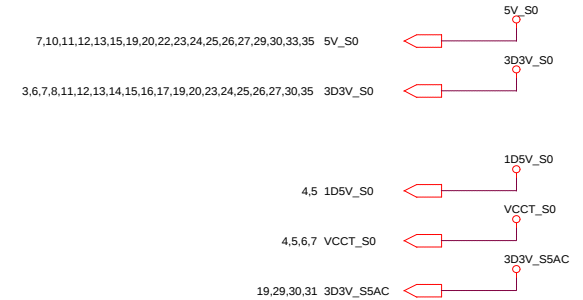
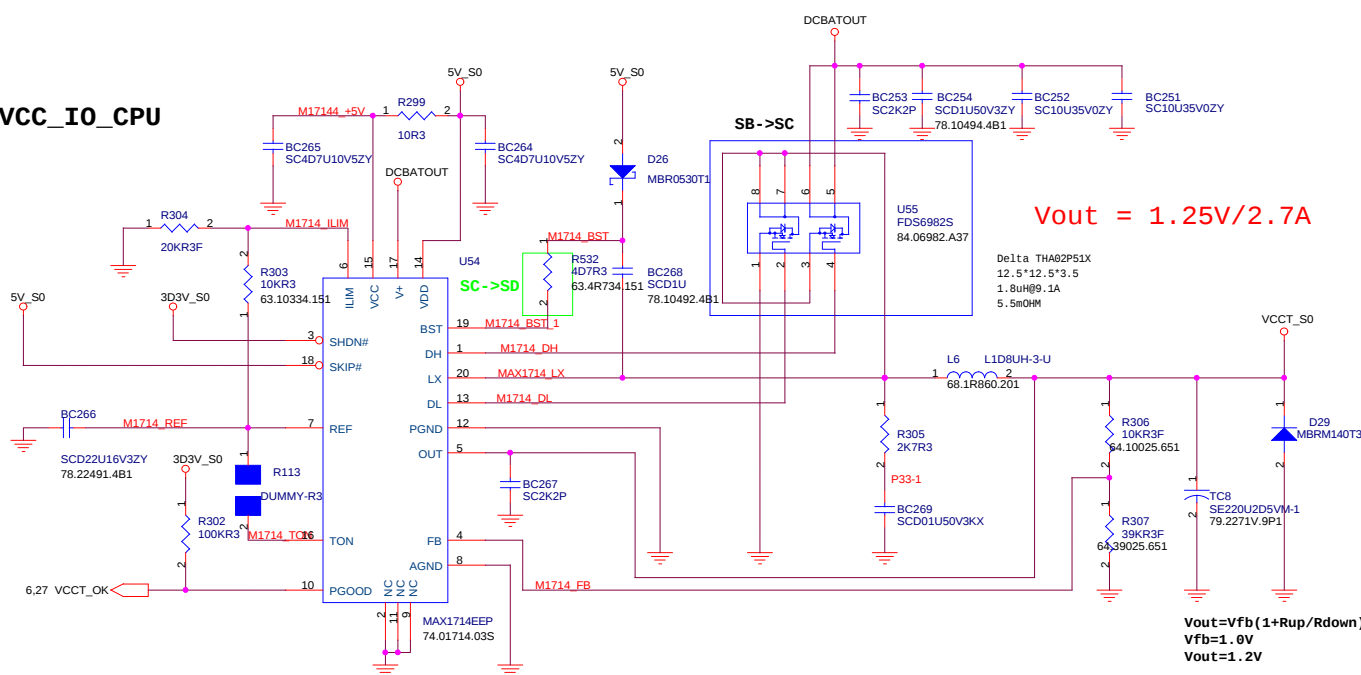
2.5V (mA)



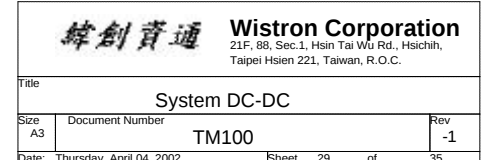
1.5V (mA)

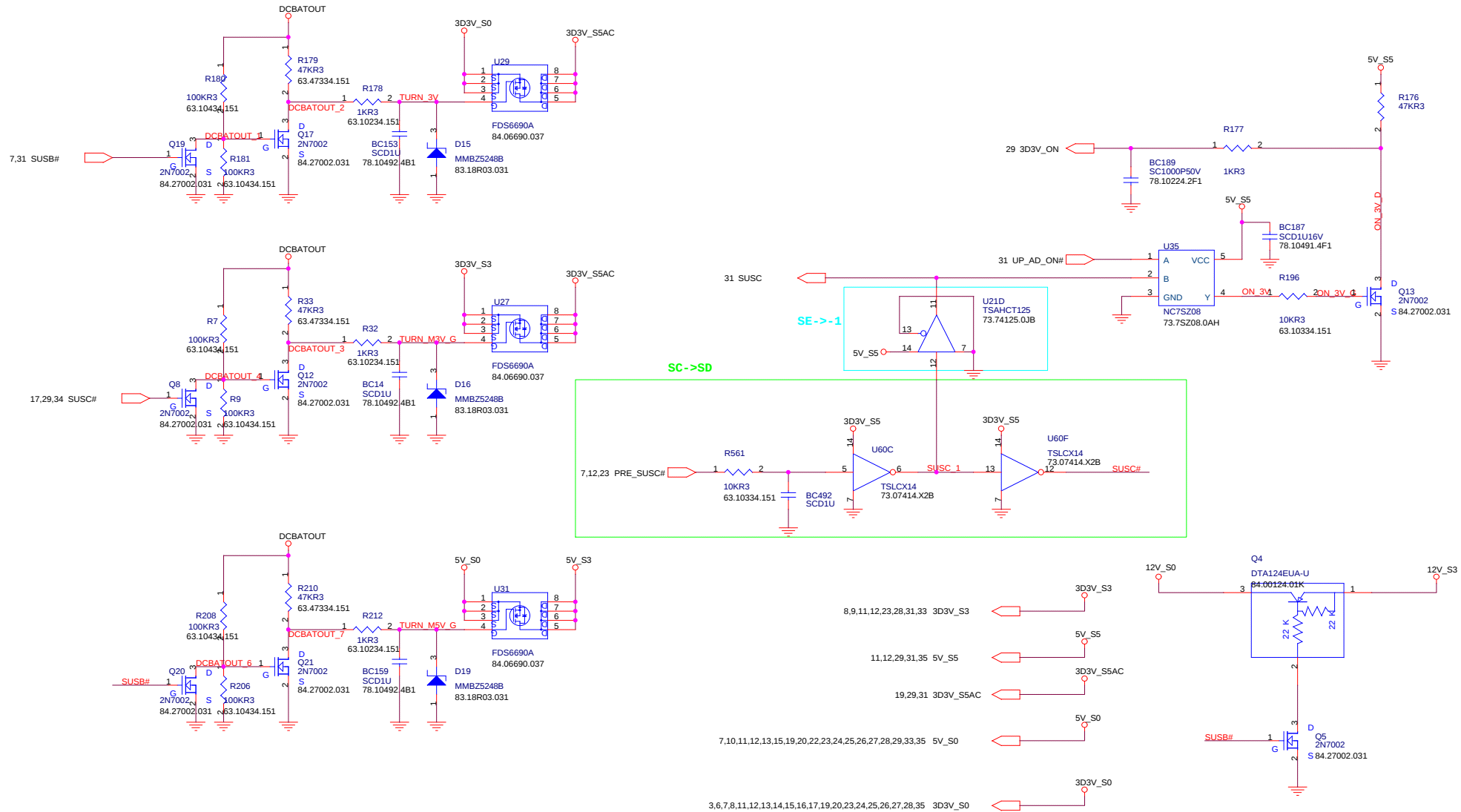


VCC_IO_CPU



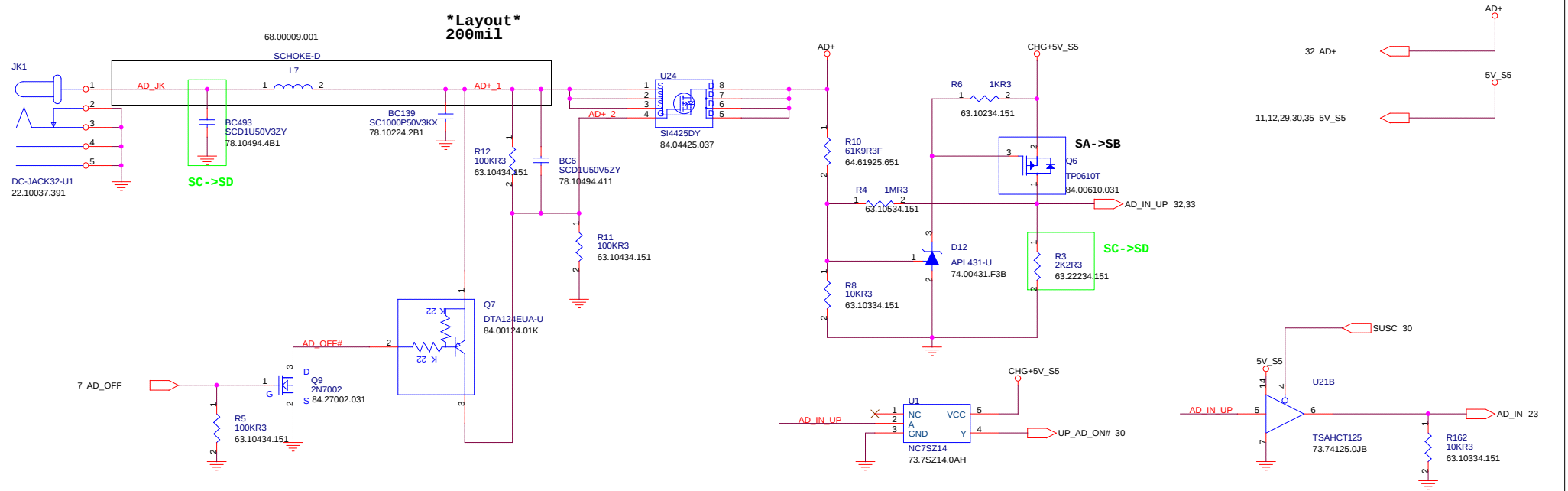
緯創資通		Wistron Corporation 21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU10,1.5V,1.8V,1.2V			
Size A3	Document Number	Rev -1	
TM100			
Date:	Thursday, April 04, 2002	Sheet 28 of 35	



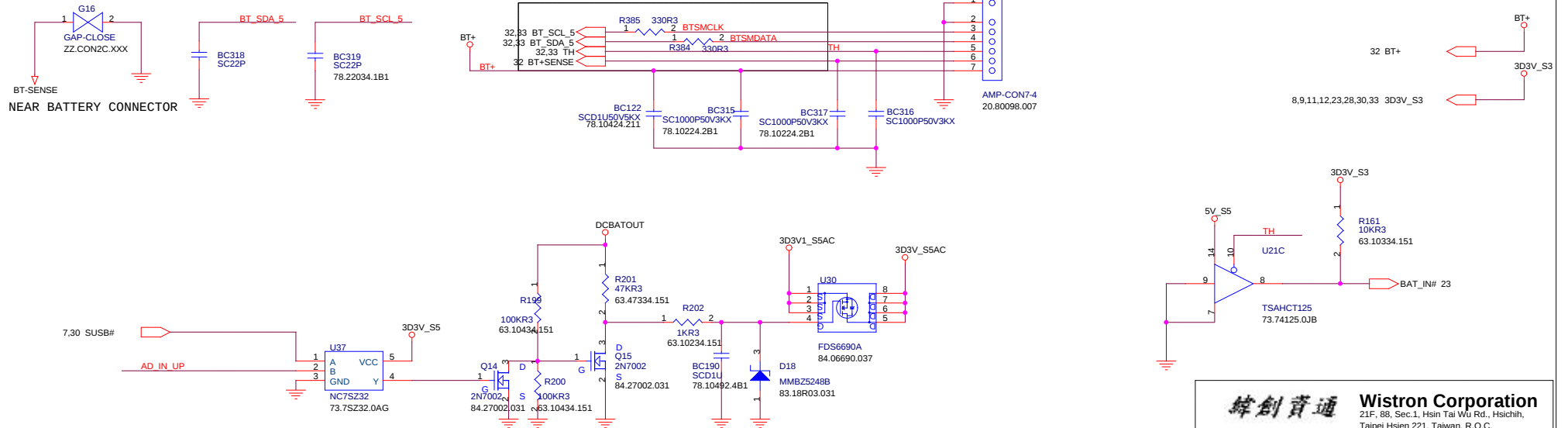


Adaptor in to generate DCBATOUT

Layout
200mil



BATTERY CONNECTOR



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Taipei Hsien 221, Taiwan, R.O.C.

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Charger Max
Current Sensor
Scaling 20mV/A

R98 MUST BE AS CLOSS TO
U9 PIN6 AS POSSIBLE

THE TRACE LENGTH FOR U9
PIN 6 & PIN 7 MUST BE THE
SAME

R97 MUST BE AS CLOSS TO
U9 PIN4 AS POSSIBLE

THE TRACE LENGTH FOR U9
PIN 4 & PIN 5 MUST BE THE
SAME

Adapter Max
Current Sensor
40mv/18m ohm=2.2 A

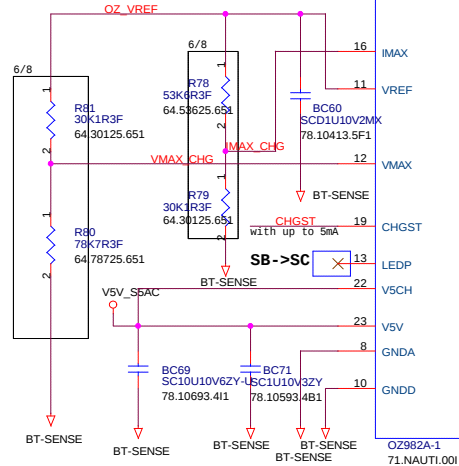
6/8

$$I_{max} = R79 / (R78 + R79) * V_{ref}(2.5V) * 2$$

$$(2A/V) = 1.65A$$

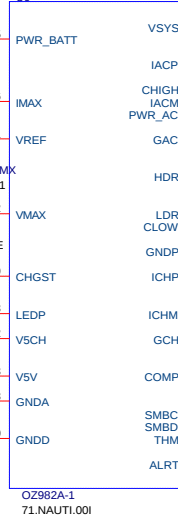
$$V_{max} = R80 / (R80 + R81) * V_{ref}(2.5V) * 10$$

$$= 18V$$



BT-SENSE 31

0 ohm, payolute with OZT05005 only



AD+ 31

CHG+5V_S5 31,33,35

DCBATOUT 11,27,28,29,30,31

BT+ 31

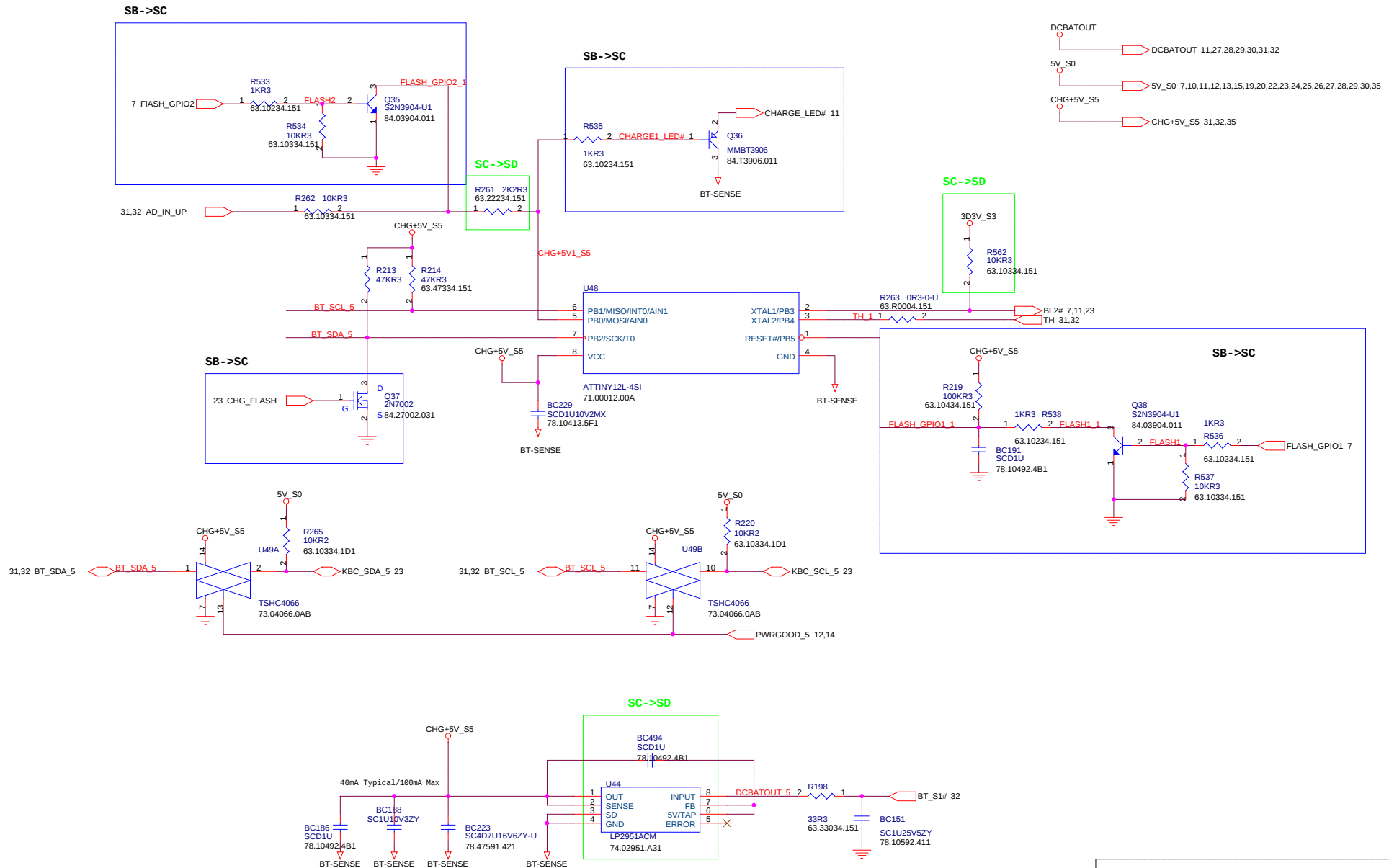
5V_S0 7,10,11,12,13,15,19,20,22,23,24,25,26,27,28,29,30,33,35

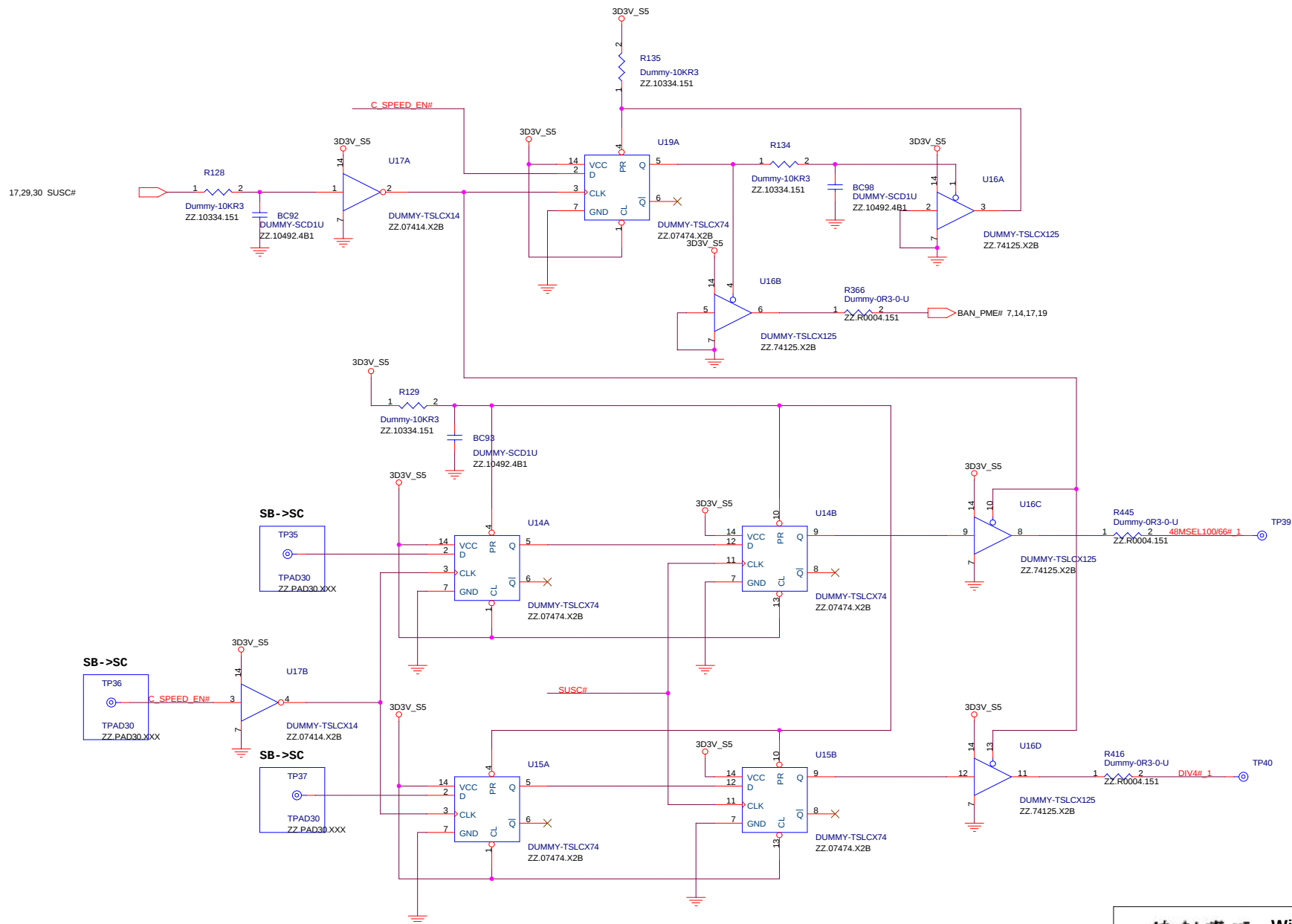
Layout
200mil

Layout
100mil

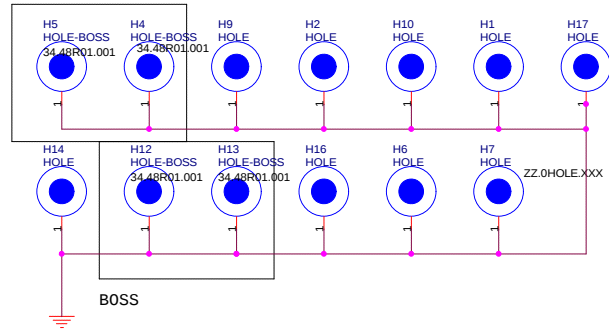
Layout
200mil

Layout
200mil

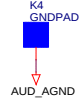
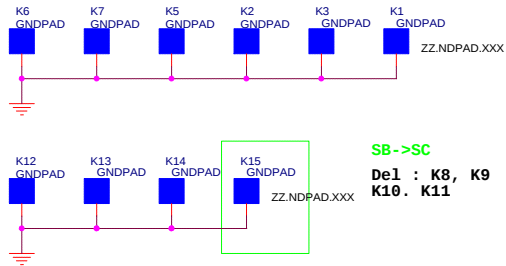




BOSS



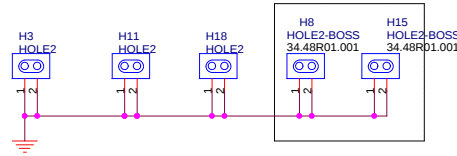
BOSS



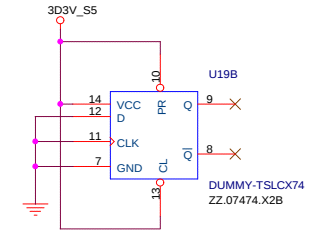
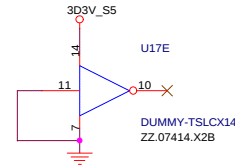
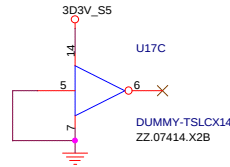
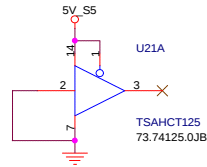
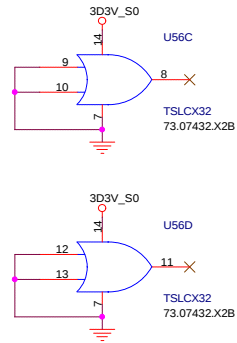
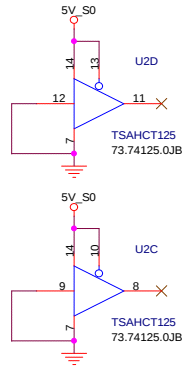
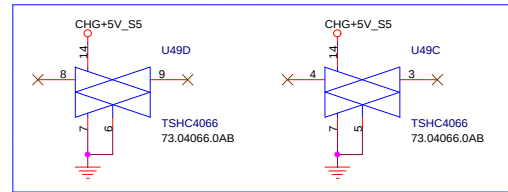
SB->SC

Del : K8, K9
K10. K11

BOSS



SA->SB



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Title		
SPARE GATES & HOLES		
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