ZR9 BLOCK DIAGRAM

SW@ --> iGPU & GPU Switch
IV@ --> iGPU only
EV@ --> GPU only
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only
CSP@ --> Operation P/N

GPU CORE PWR ISL6264 P44	CHARGER ISL88731 P50
GPU IO PWR ISL62827 P45	3/5V SYS PWR ISL6237 P49
DISCHARGER +3V,+ 5V,+1.5V,+1.05V,+1.1V_VTT P51	CPU CORE PWR ISL62882 P42
+1.0V/+1.5V G93334 + Linear P51	CPU VTT ARD: 1.05V CFD: 1.1V UP61111AQDD P46
CPU VGFX_AXG ISL62881 P43	VTT 1.05V UP61111AQDD P47
THERMAL PROTECTION P41	DDR3 PWR TPS5116 P48

Optional DOCKING

DVI
VGA
RJ45
USBX4
AC JACK
AUDIO/SPDIF MIC / LINE-IN

Note:
HM55 does not support USB 6 & 7
HM55 does not support SATA 2 & 3

CLOCK GENERATOR
SELGO: SLG8SP585V
P3
X'TAL 14.318MHz

BCLK: 133MHz
PEG_CLK: 100MHz
DPLL_REF_SSCLK: 120MHz

DDR III
SO-DIMM 0
SO-DIMM 1
P14, 15

Dual Channel
800/ 1066 MHz
800 MT/s 1066 MT/s

DDR SYSTEM MEMORY

intel
<MCH Processor>
Arrandale (SG)*
rPGA 989
(37.5mm X 37.5mm)
P4.5.6.7
PCI-E X16
FDI
DMI

*[Arrandale Only]

X4 DMI interface

Fan Driver
(PWM Type)
P34

PCIE
2.5GT/s

Nvidia GPU
N11M 512M
(64Mb x 32 IO x 8 pcs)
P16,17,18,19,20,21,22,23

CRT
LVDS
HDMI

LVDS_CRT_Switch
Grapgics
P23

CRT P27
LVDS P24
Docking DVI P25

X'TAL 27.0MHz

INT_CRT *[Arrandale Only]
INT_LVDS *[Arrandale Only]
INT_HDMI *[Arrandale Only]

HDMI/DVI PS8101 P24, 25

intel
<PCH>
Ibex Peak_M
mBGA 676
(27mm X 25mm)
P8.9.10.11.12.13

FDI
DMI
Graphics Interfaces
SATA
3.0 GT/s
PCI-E
USB
HDA
SPI
LPC
RTC
P9

X'TAL 32.768KHz

HDD (SATA) *1
P29
SATA0

ODD (SATA)
P29
SATA1

USB0

Card Reader Connector AU6437 P25
USB Port x 4
USB 1, 3, 11, 12 P31
Bluetooth
USB 4 P32
CCD
USB 8 P23
FingerPrint
USB 2 P34
SIMM card
USB 0 P28

USB 2.0

Azalia

MDC P33

Audio CODEC
CX20672
P30

SPI ROM
4MB x1 (Basic ME+Braidwood)
P9

EC (WPC781)
P38

X'TAL 32.768KHz

TPM
SLB 9635
P31

SPI ROM P38

Touch Pad P34

K/B COON. P34

AUDIO Jack P30
Speaker P30
Docking S/PDIF P33
Docking Line in P33
MIC Jack P30
Int. D-MIC P23

PCI-Express
2.5GT/s

PCIE-2
CLKOUT_PEG_4
Mini card 3G/GPS
USB 10 P28

PCIE-6
CLKOUT_PEG_1&3
Mini Card WLAN
USB 13 P28

PCIE-1
CLKOUT_PEG_B
Broadcom Giga-LAN
BCM57760
P26

X'TAL 25MHz

Docking SW PI3L500 P27
Transformer P27
RJ45 Connector P27

Docking

Quanta Computer Inc.
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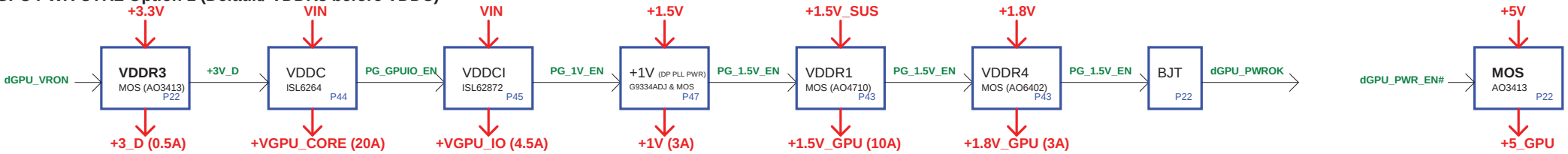
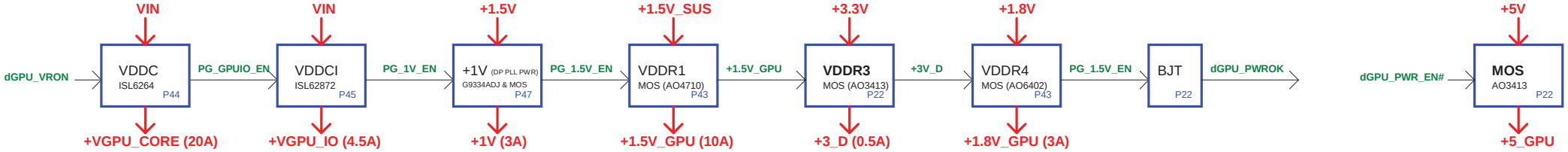
Size | Document Number | Rev 1A
Block Diagram
Date: Thursday, April 29, 2010 | Sheet 1 of 47

GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



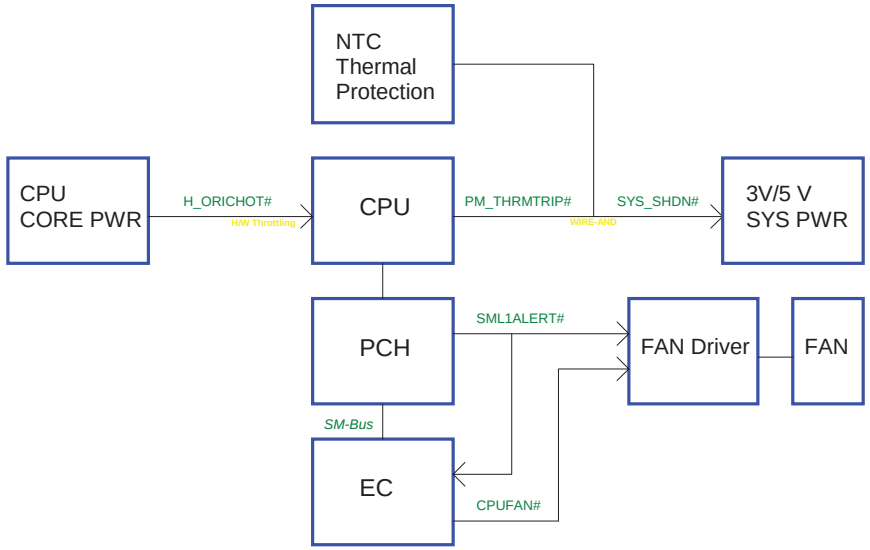
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER		S0~S5
+RTC_CELL	+3V~+3.3V	RTC		S0~S5
+3VPCU	+3.3V	8051 POWER	ALWON	S0~S5
+5VPCU	+5V	CHARGE POWER	ALWON	S0~S5
+15V	+15V	LARGE POWER	+15V_ALWP	S0~S5
3V_LAN_S5	+3.3V	LAN POWER	AUX_ON	
+5VSUS	+5V		SUSD	
+3VSUS	+3.3V		SUSD	
+1.5VSUS	+1.5V	SODIMM POWER	SUSON	
+0.75V_DDR_VTT	+0.9V	SODIMM POWER	MAINON	
+5V	+5V		MAIND	
+3V	+3.3V		MAIND	
+1.8V	+1.8V		MAINON	
+1.5V	+1.5V	PCH POWER	MAIND	
+1.1V_VTT	+1.05V~+1.1V	CPU POWER	MAINON	
+1.05V	+1.05V	PCH POWER	MAINON	
+VCC_CORE	0V~+1.5V	CPU CORE POWER	VRON	
LCDVCC	+3.3V	LCD Power	LVDS_VDDEN	
MBAT+	+10V~+17V	MAIN BATTERY		
+5V_S5	+5V		S5_ON	
+3V_S5	+3.3V		S5D	

Thermal Follow Chart



Quanta Computer Inc.
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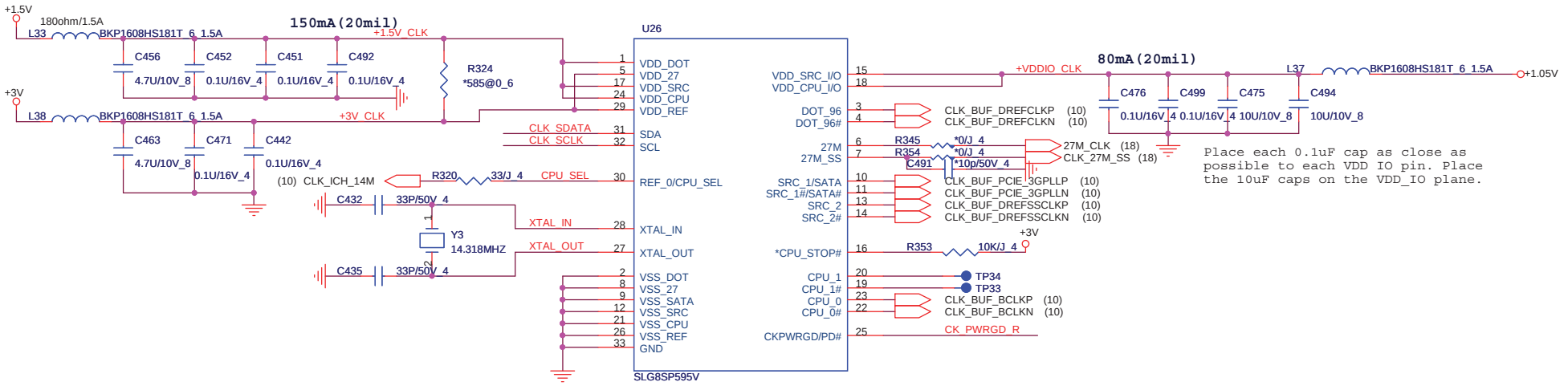
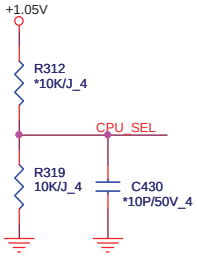
Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

Date: Thursday, April 29, 2010 Sheet 2 of 47

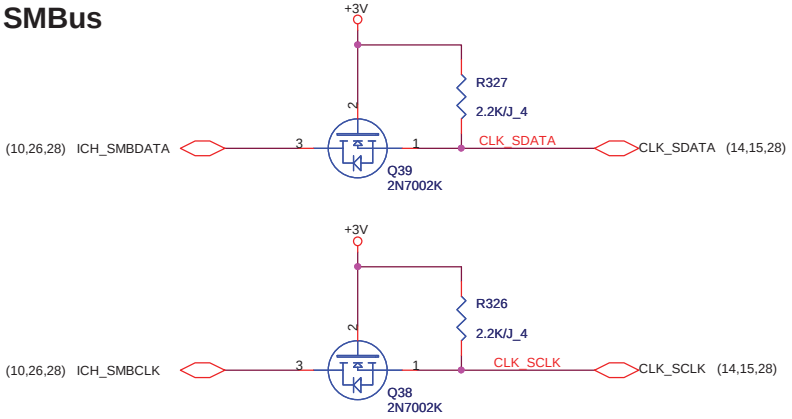


CPU_CLK select

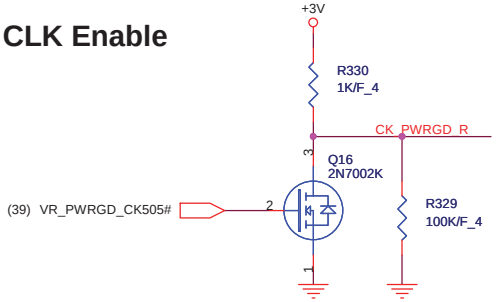


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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Size	Document Number	Rev
	Clock Generator	1A

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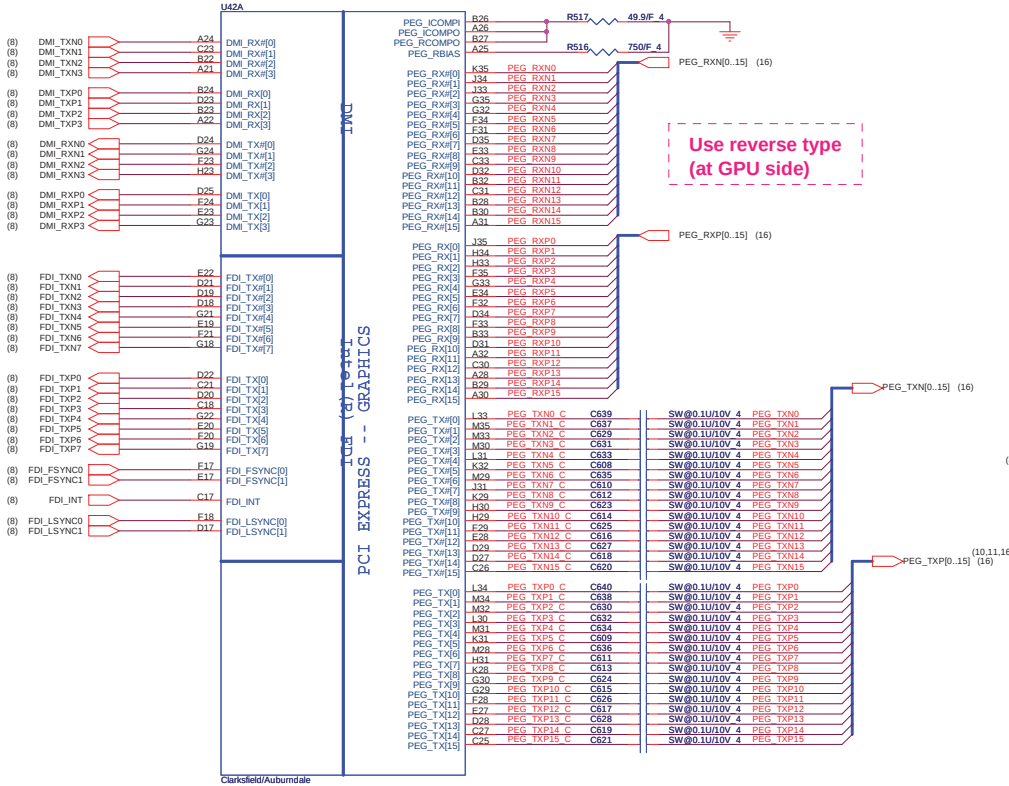
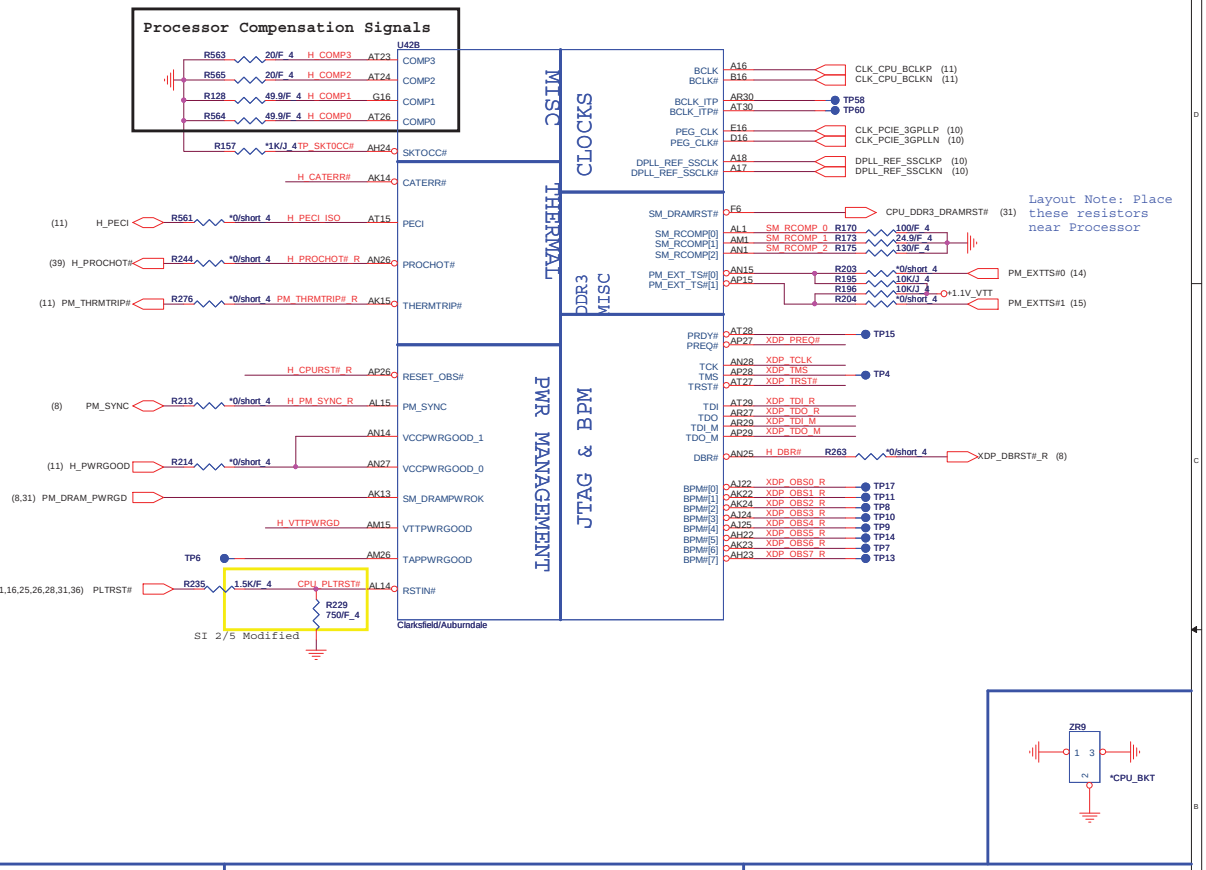
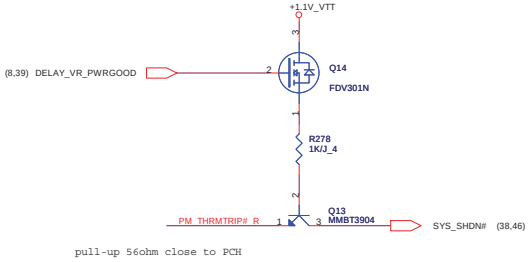
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



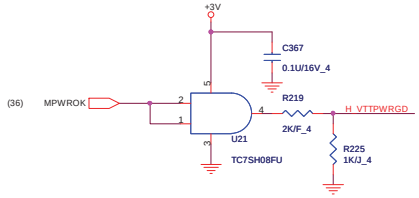
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



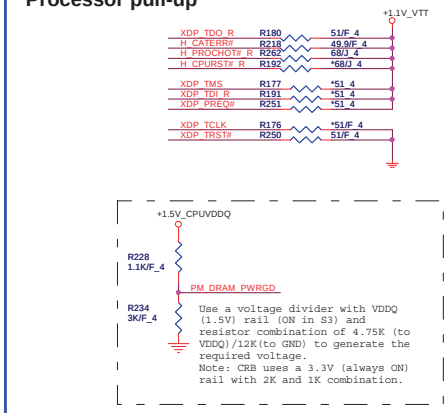
Thermaltrip protect



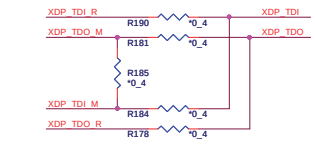
VTT PWR_Good



Processor pull-up



JTAG MAPPING



Scan Chain (Default)	STUFF -> R535, R538, R528 NO STUFF -> R536, R534
CPU Only	STUFF -> R536, R534 NO STUFF -> R535, R538, R528
GMCH Only	STUFF -> R534, R528 NO STUFF -> R538, R536, R535

Quanta Computer Inc.

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Size	Document Number	Rev
	AUBURNDA 1/4	1A

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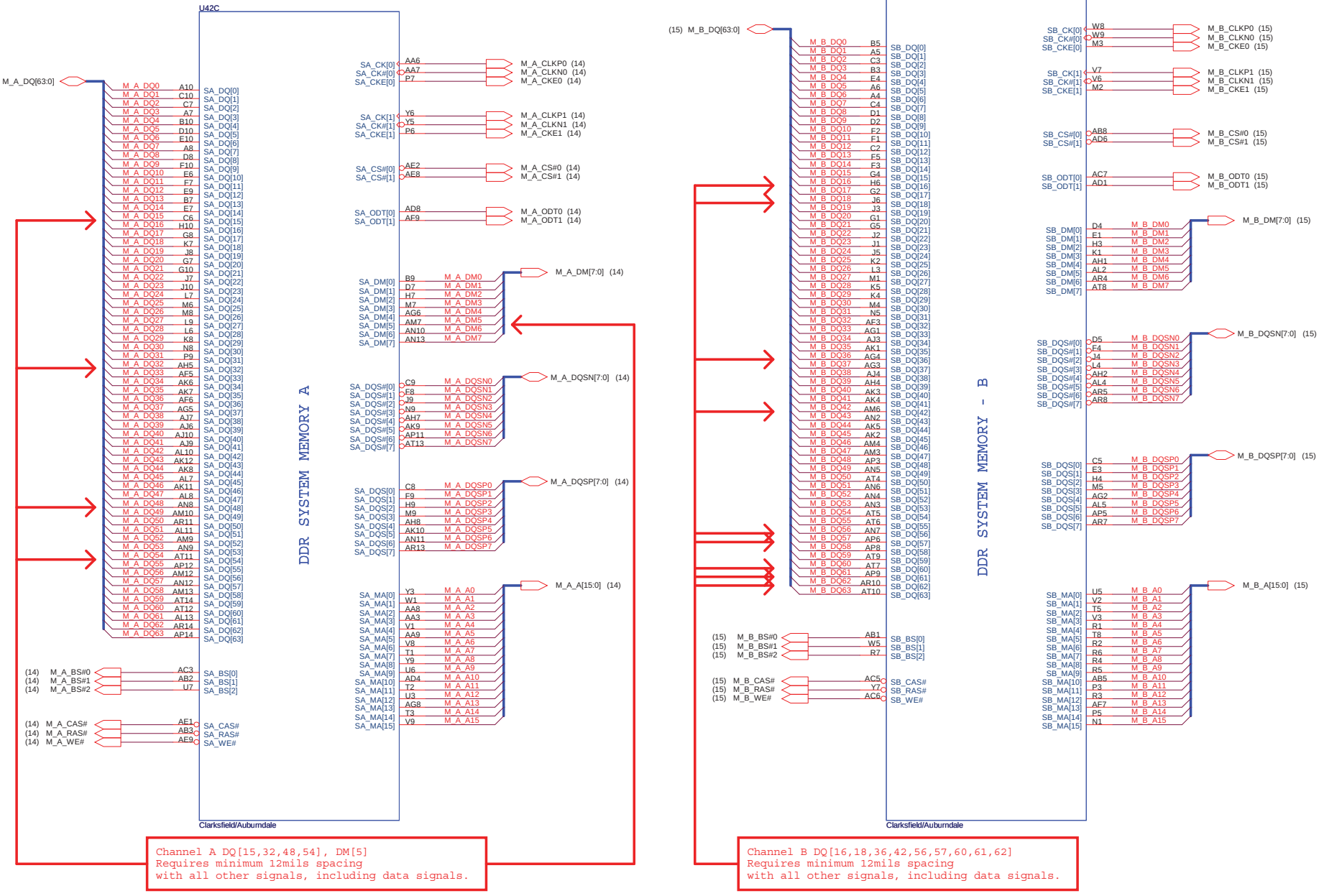
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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Size	Document Number	Rev
	AUBURNDA 2/4	1A
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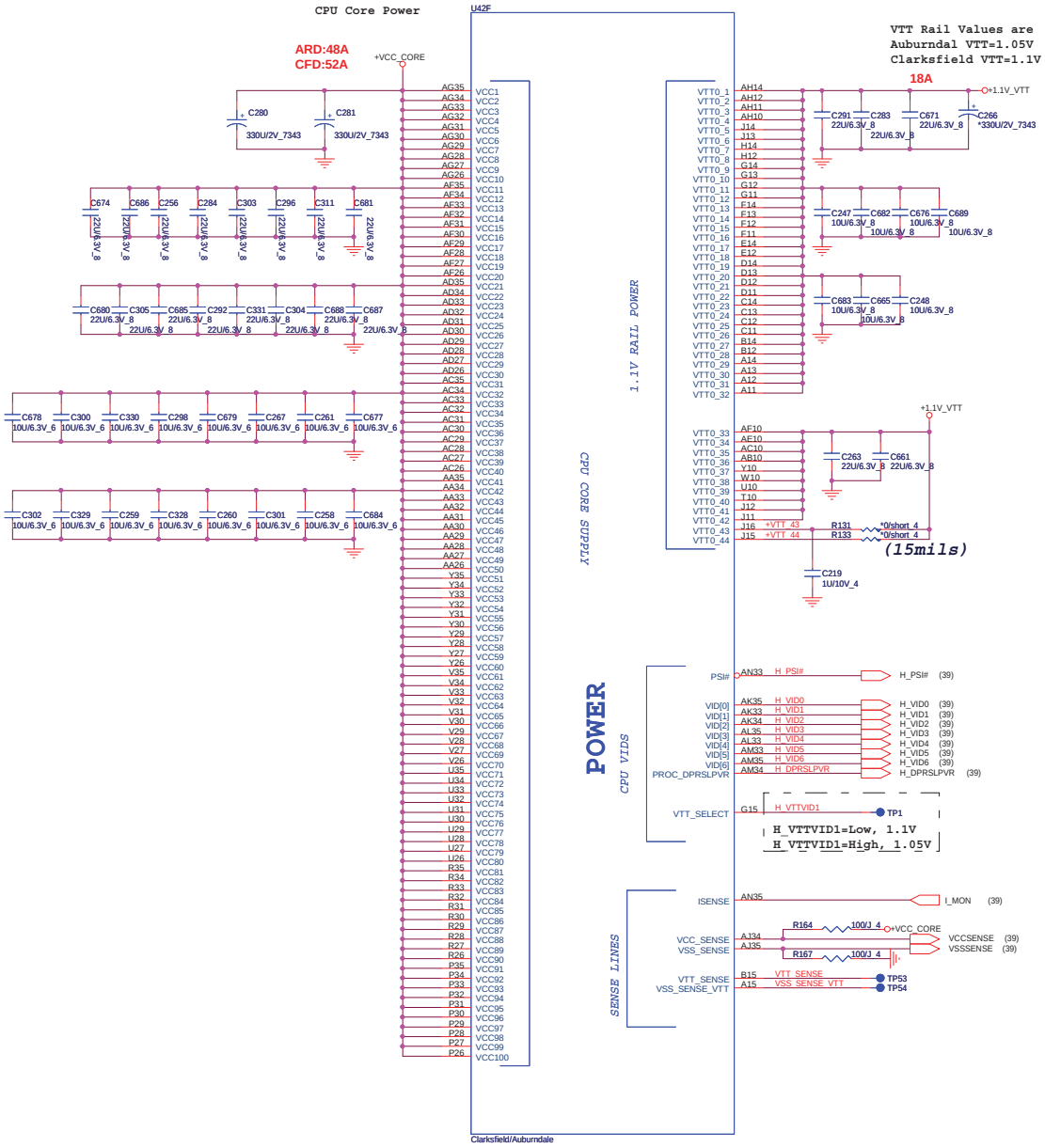
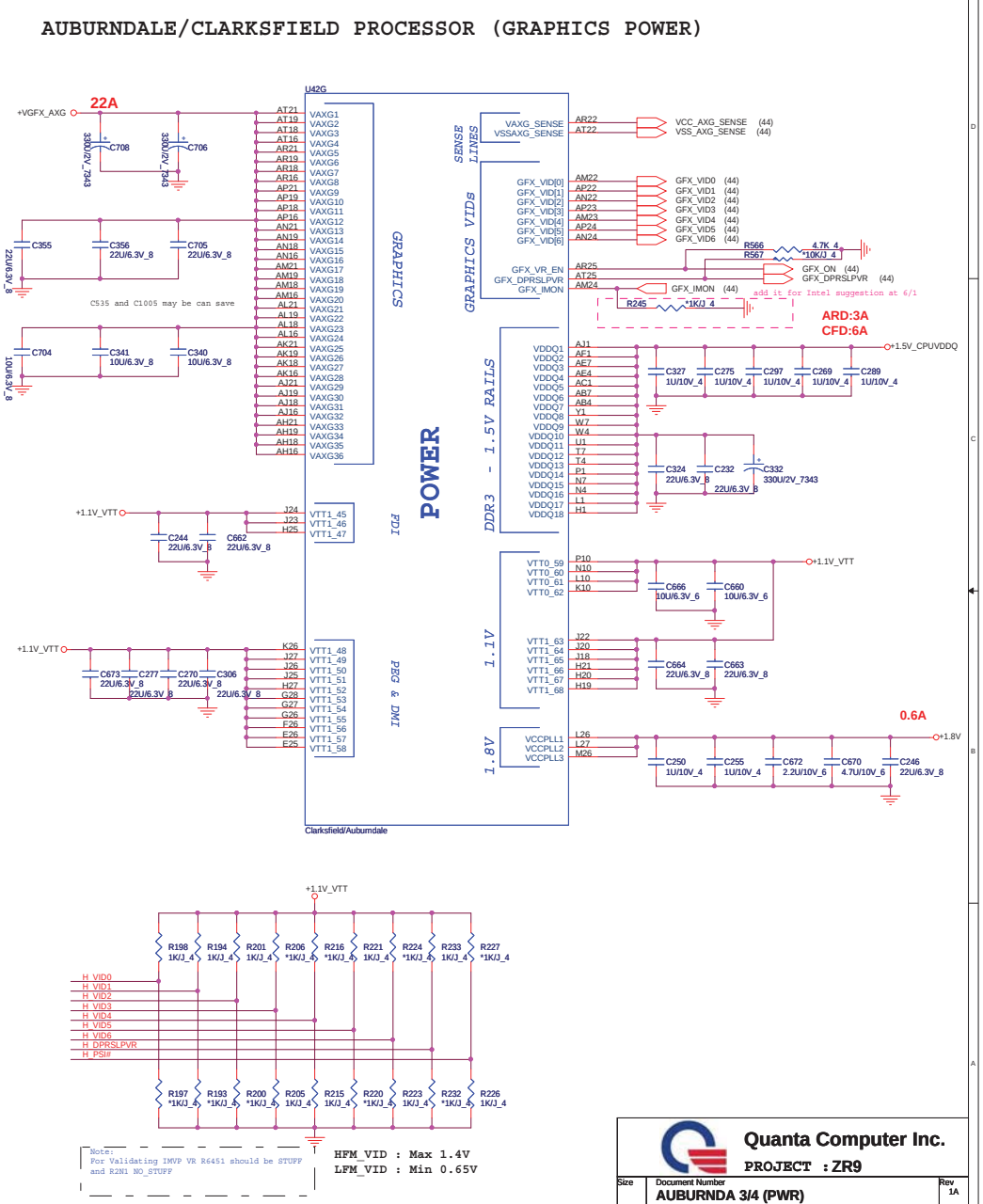


AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)



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Size	Document Number	Rev
	AUBURNDA 3/4 (PWR)	1A

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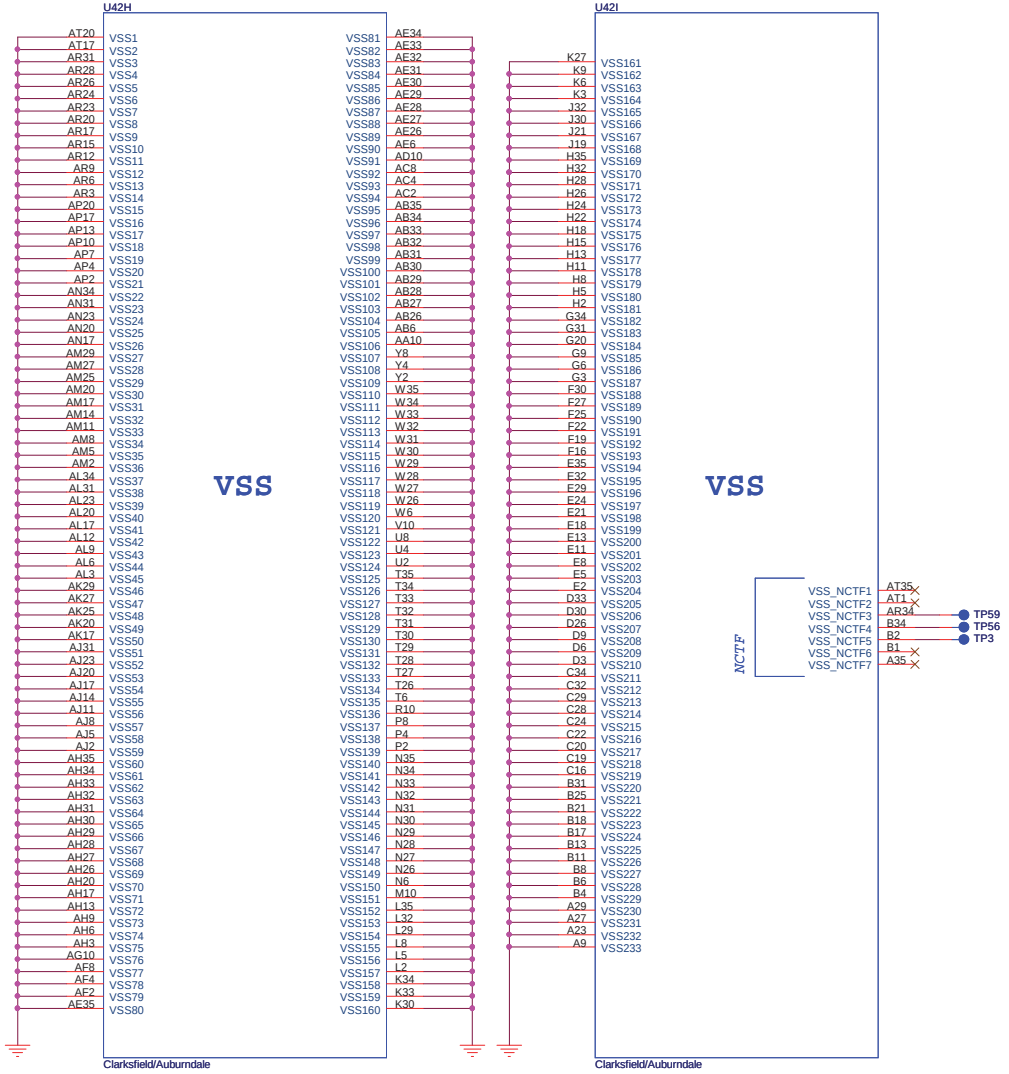
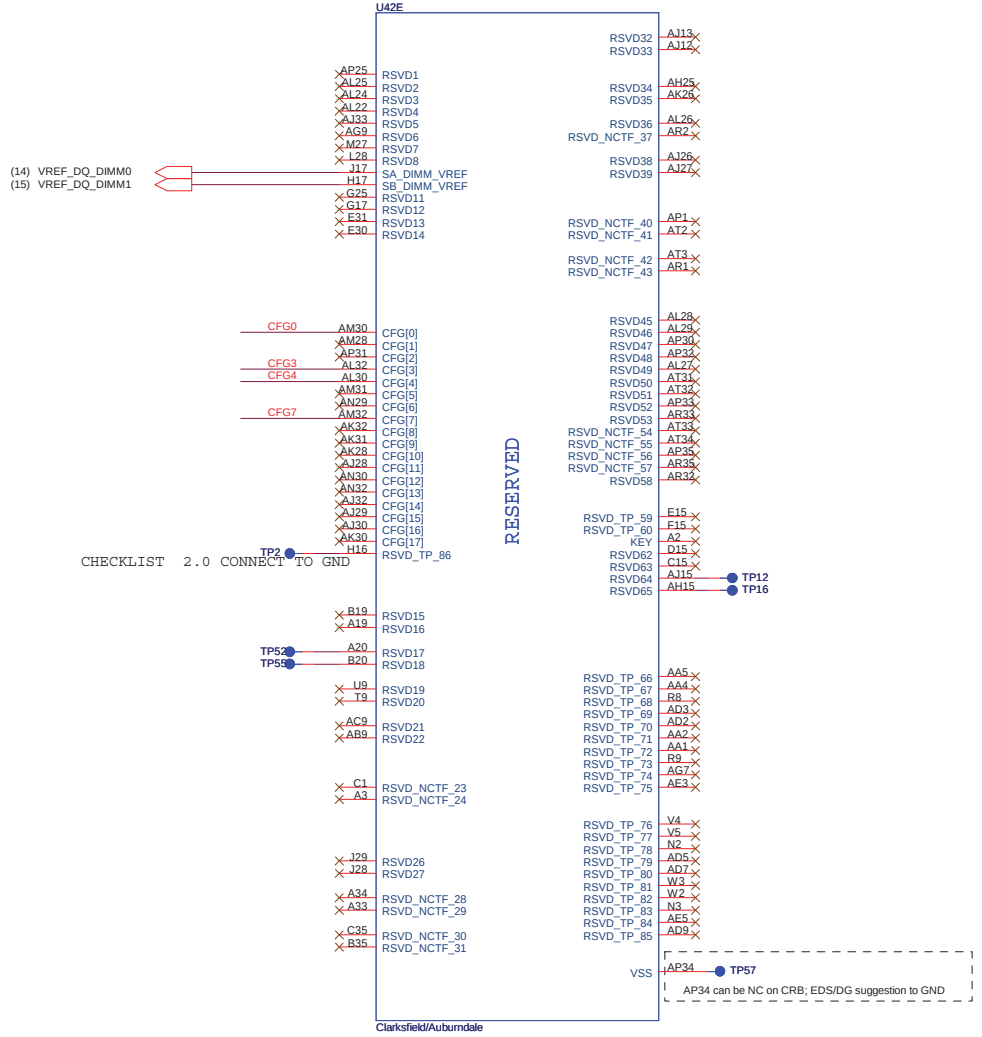
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

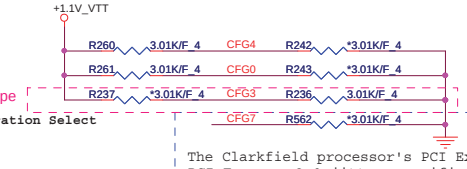


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

Quanta Computer Inc.
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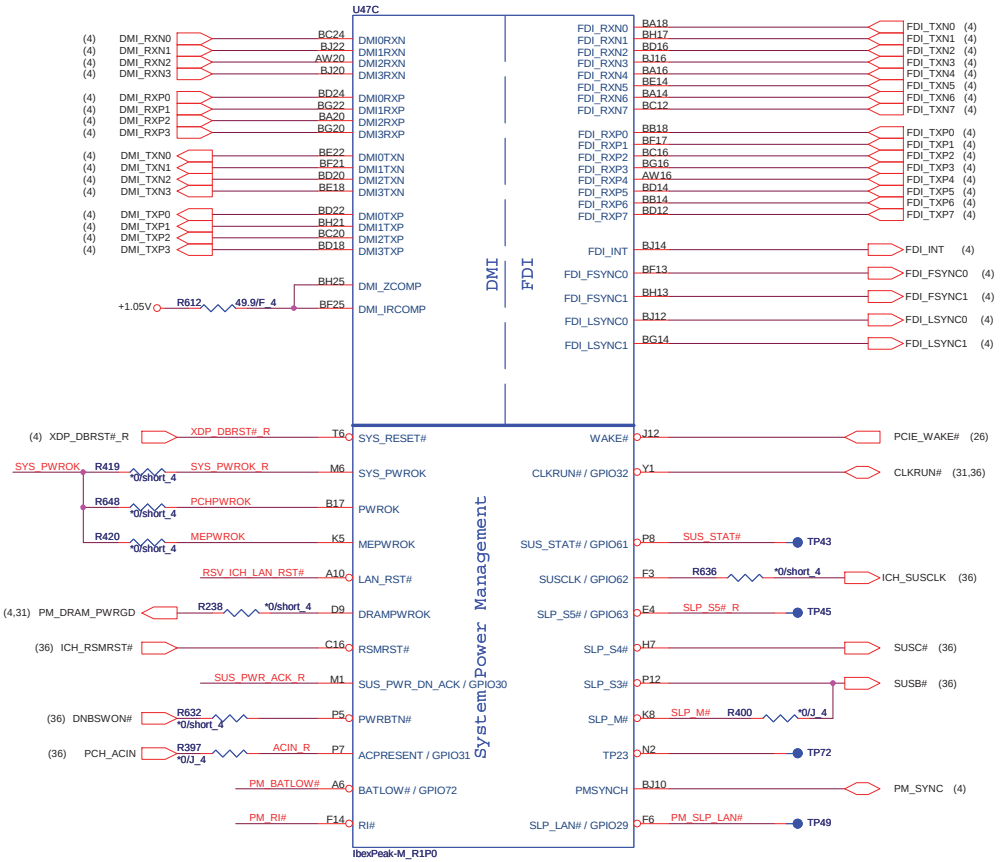
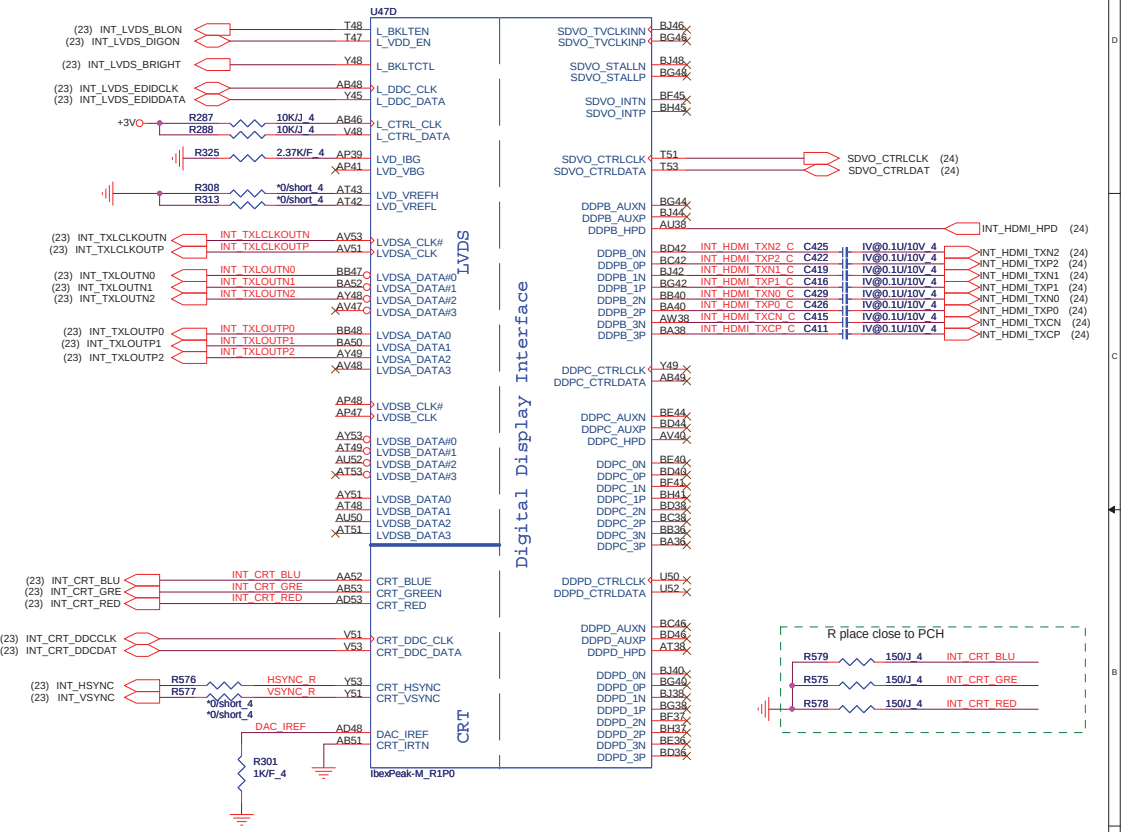
Size	Document Number	Rev
	AUBURNDA 4/4	1A
Date: Wednesday, May 05, 2010	Sheet 7 of 47	

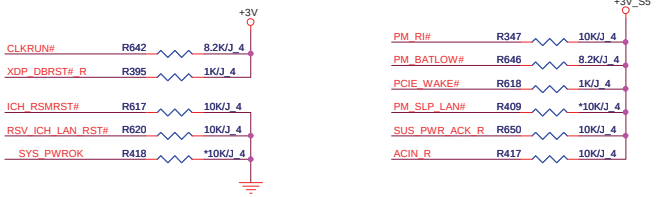
IBEX PEAK-M (DMI,FDI,GPIO)



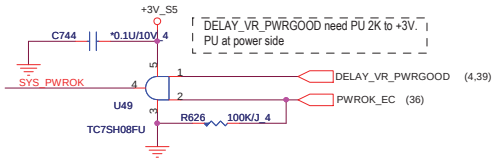
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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Size	Document Number	Rev
	IBEX PEAK-M 1/6	1A

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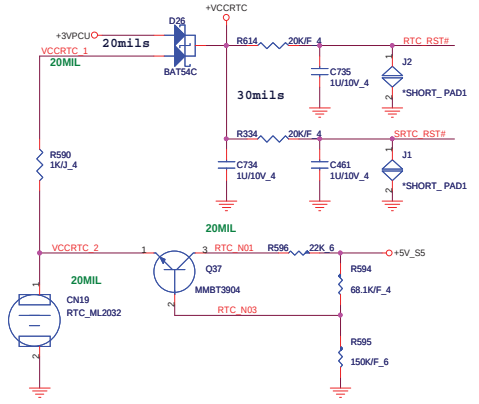
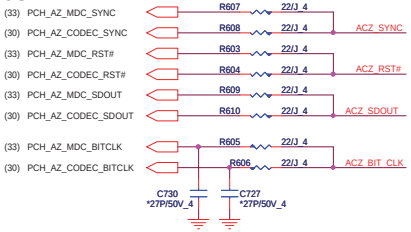
RTC Circuitry

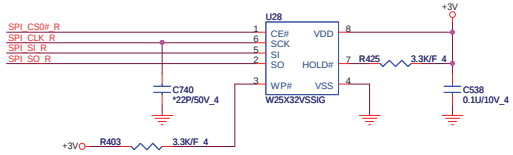


HDA Bus

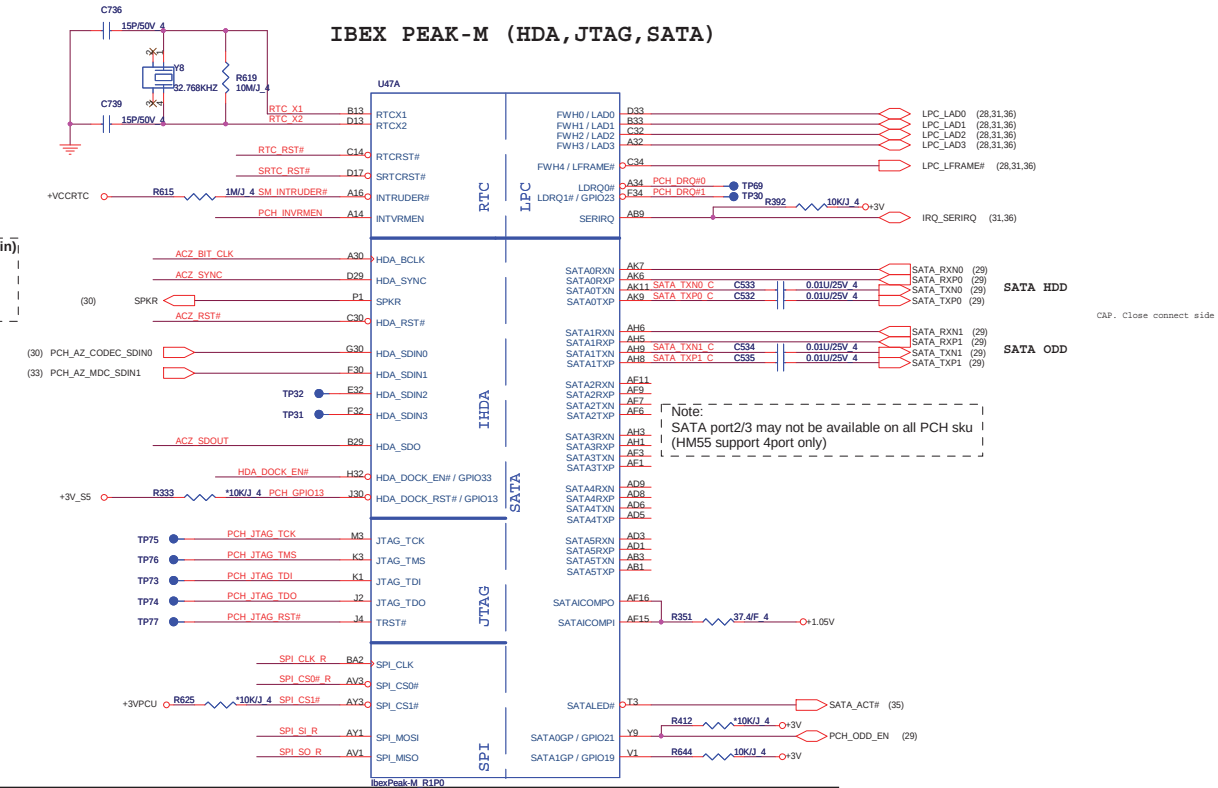


Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI



IBEX PEAK-M (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZY9B note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R633 *10K/J_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R583 *4.7K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+VCCRTC R616 330K/J_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / LPC	Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS] +3V R286 *1K/J_4, R282 *1K/J_4 R285 1K/J_4, R306 1K/J_4 PCI_GNT0# (10) PCI_GNT1# (10)
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	R307 *4.7K_4 PWM_SELECT# (10,23
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R623 *1K/J_4 NV_ALE NV_ALE (10)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R622 *1K/J_4 NV_CLE NV_CLE (10)
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R310 *1K/J_4, R309 *10K/J_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R624 *1K/J_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R383 10K/J_4 RSV_GPIO8 (11)
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	R364 *10K/J_4 RSV_GPIO27 (11)
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 R414 1K/J_4 CR_WAKE# (11)

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Size	Document Number	Rev
	IBEX PEAK-M 2/6	1A

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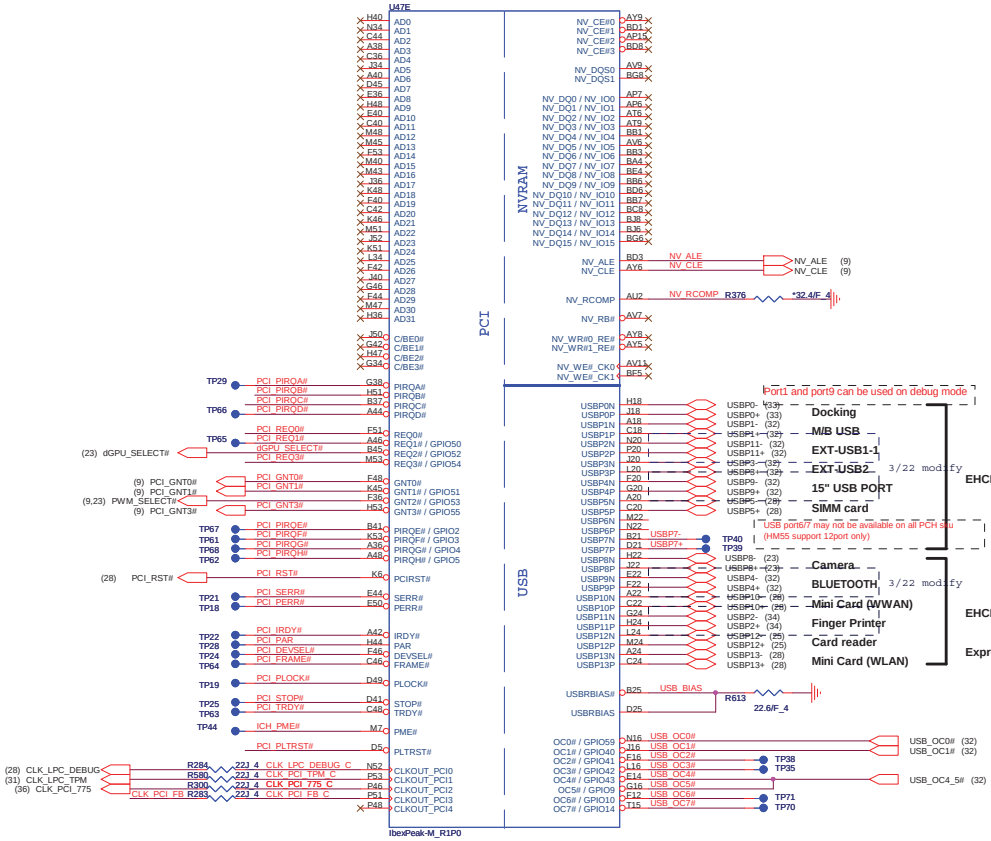
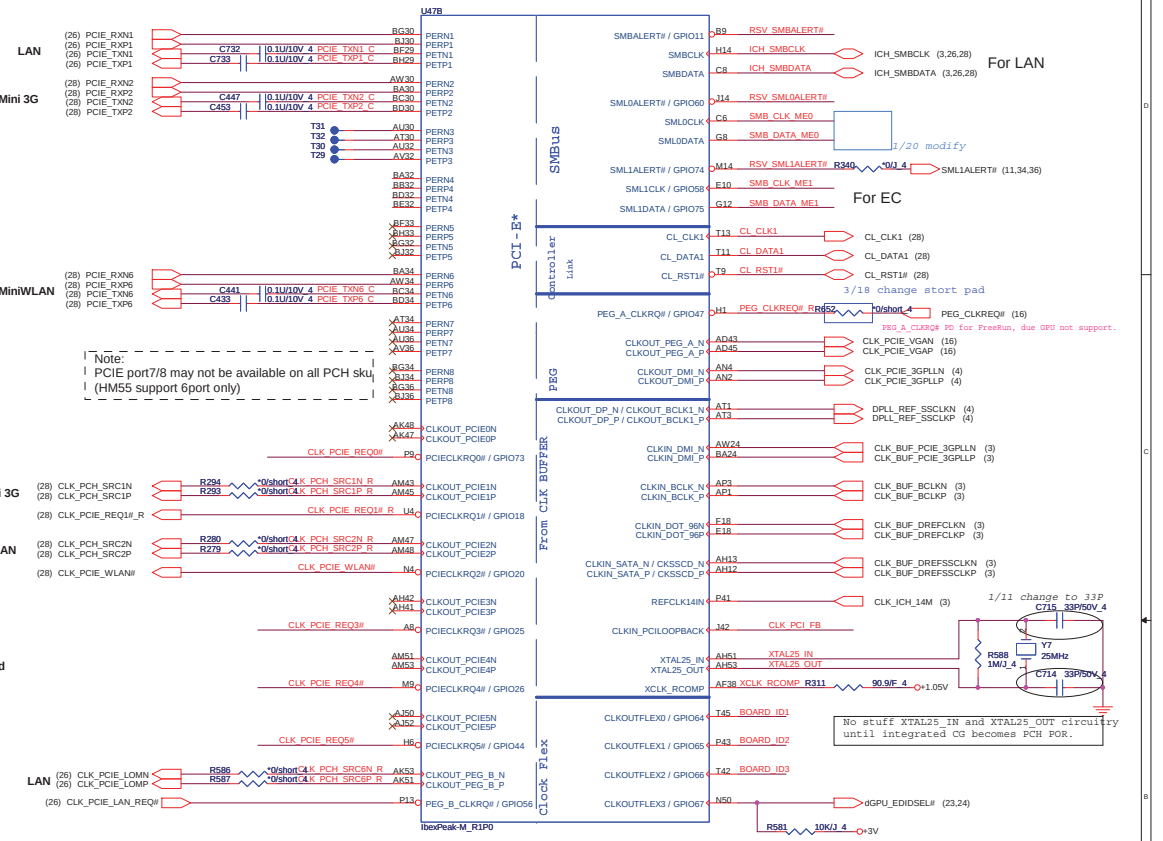
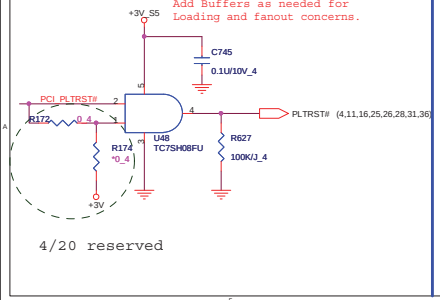
IBEX PEAK-M (PCI,USB,NVRAM)



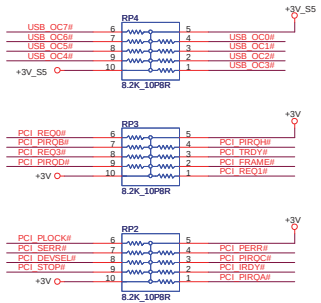
IBEX PEAK-M (PCI-E,SMBUS,CLK)



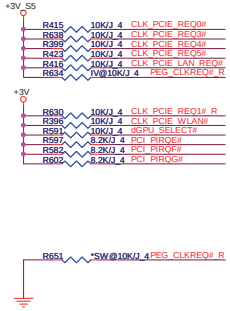
PLTRST#



PCI/USBOC# Pull-up



CLK_REQ/Strap Pin



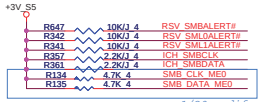
PEG_A_CLKRQ# PD for FreeRun, due GPU not support.

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

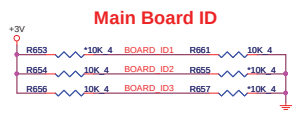
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

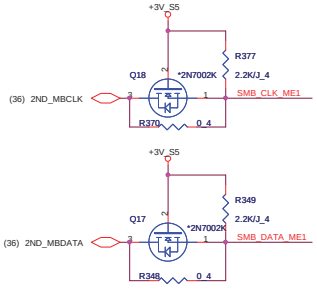
SMBus/Pull-up



Board ID3	Board ID2	Board ID1	Board ID0
Debug port 0:PCI 1:LPC(default)	0:ZQ3 series 1:ZR9 series	0:non- optimas 1:NV optimas	0:UMA 1:Discrete
1	1	NC	NC
1	1	0	0
1	1	0	1
1	1	NC	NC
1	1	1	1

Main Board ID





Quanta Computer Inc.
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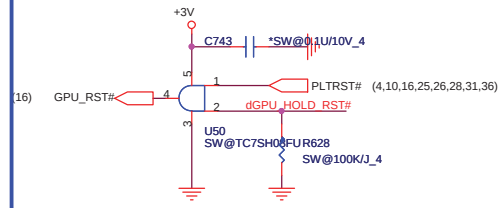
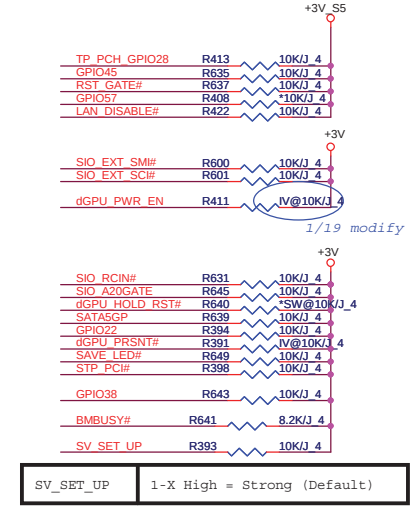
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

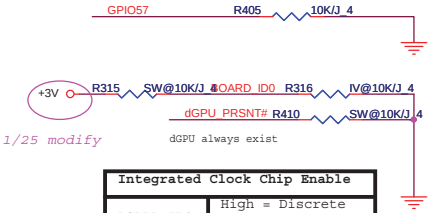
GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)



Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

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	IBEX PEAK-M 4/6	1A

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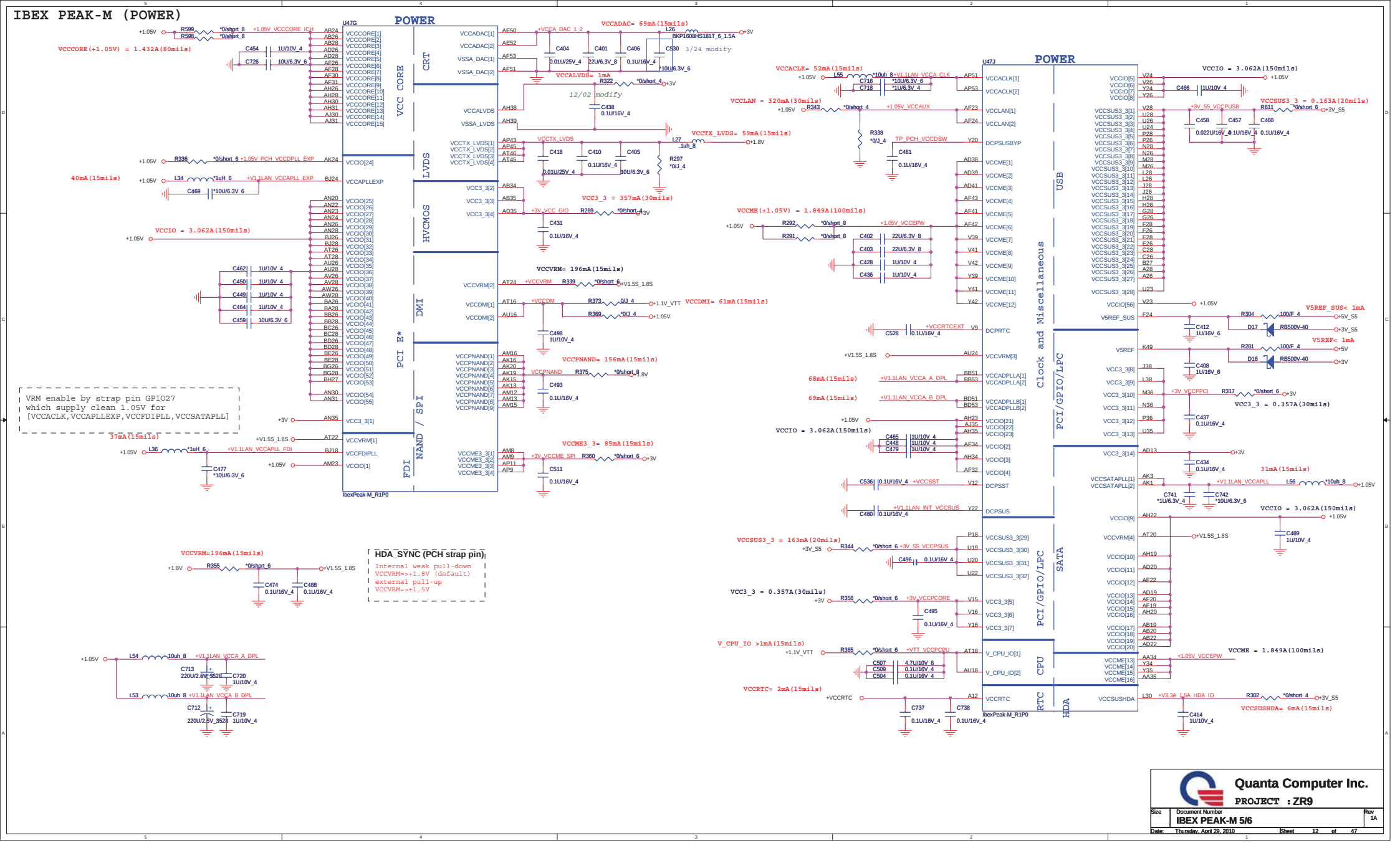
IBEX PEAK-M (POWER)



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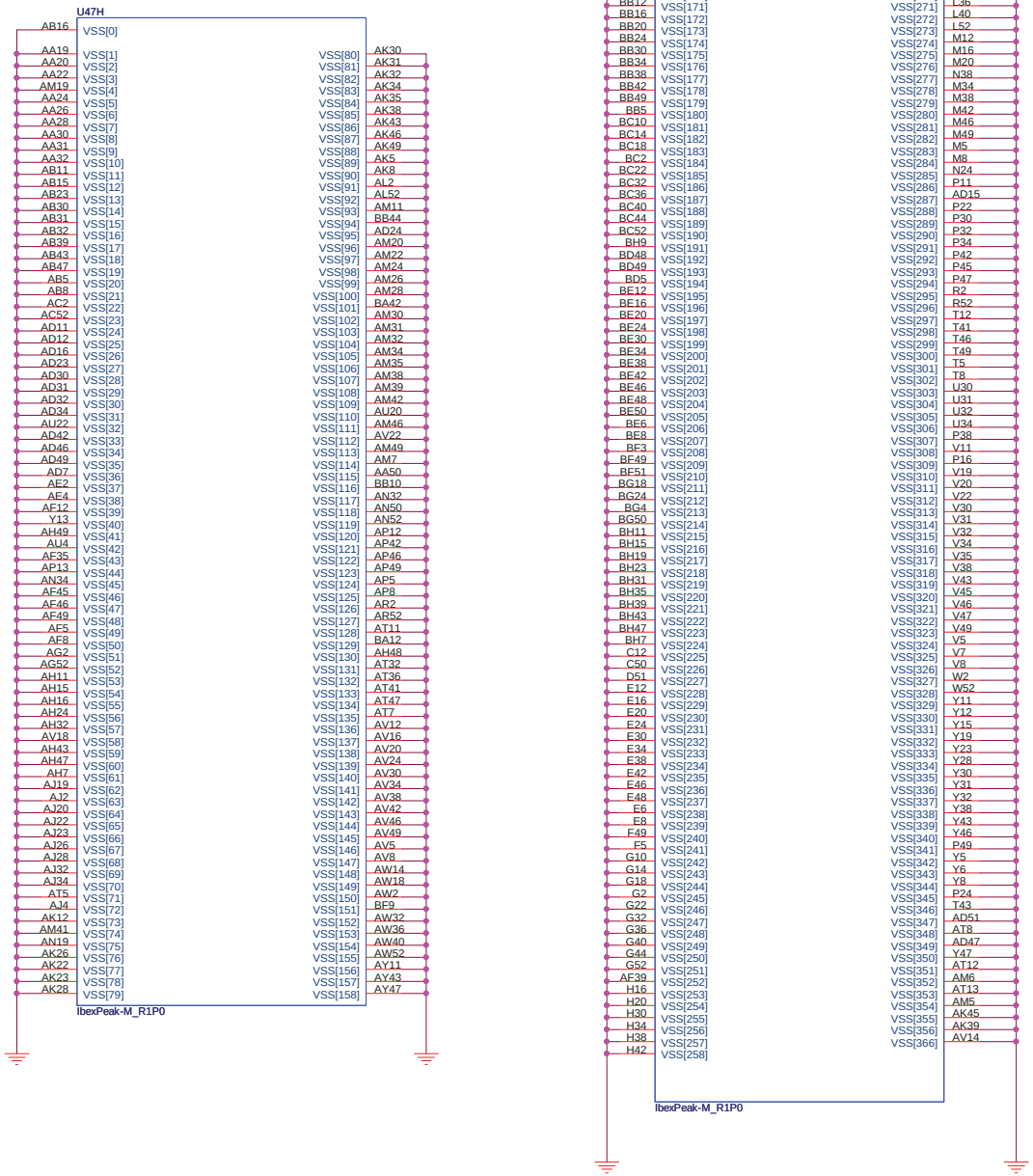
IBEX PEAK-M (GND)



Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

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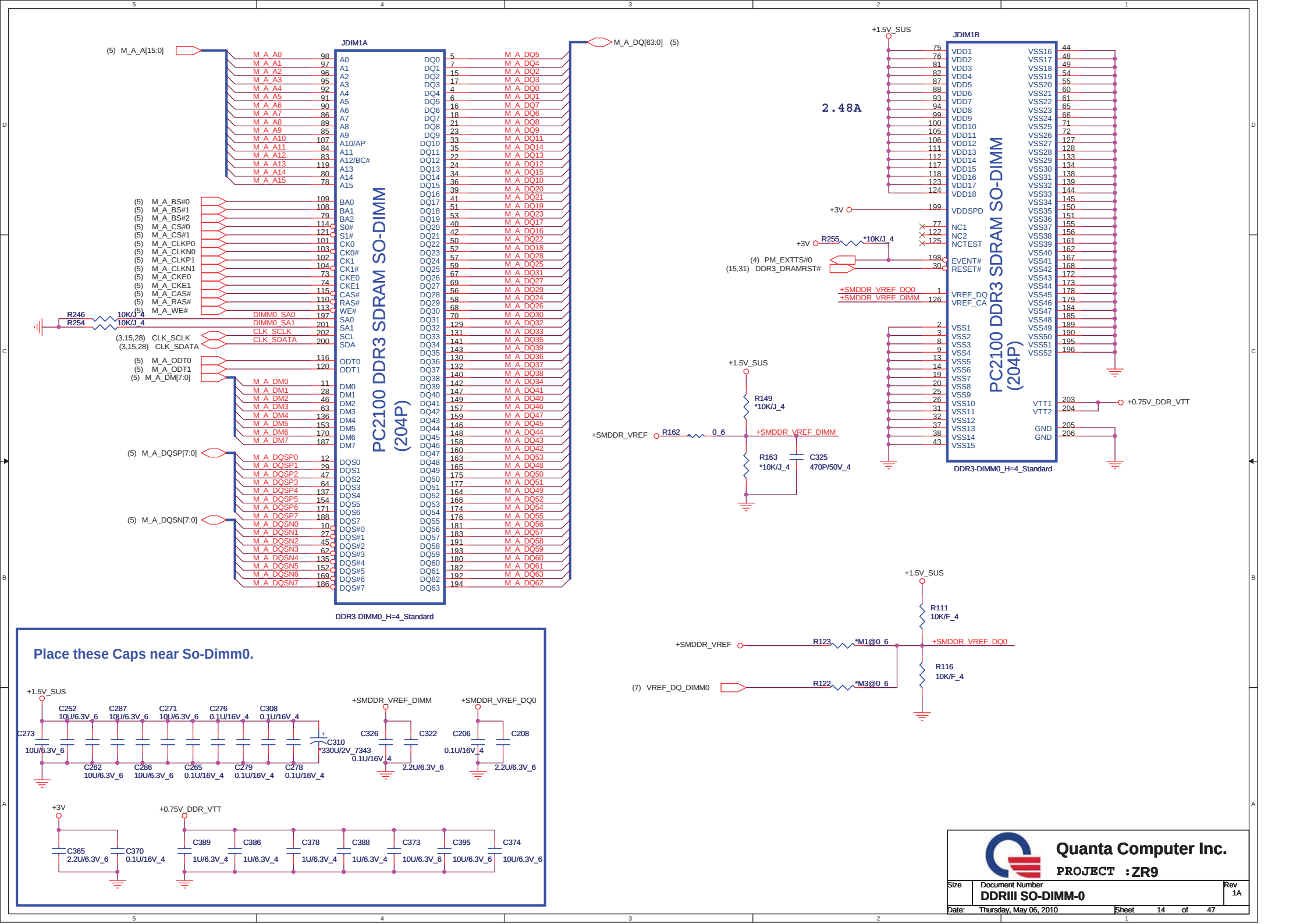
JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0_H=4_Standard
(5) M_A_A[15:0]
M_A_DQ[63:0] (5)
(5) M_A_BS#0
(5) M_A_BS#1
(5) M_A_BS#2
(5) M_A_CS#0
(5) M_A_CS#1
(5) M_A_CLKP0
(5) M_A_CLKN0
(5) M_A_CLKP1
(5) M_A_CLKN1
(5) M_A_CKE0
(5) M_A_CKE1
(5) M_A_CAS#
(5) M_A_RAS#
(5) M_A_WE#
R246 10K/J_4
R254 10K/J_4
DIMM0_SA0
DIMM0_SA1
(3,15,28) CLK_SCLK
(3,15,28) CLK_SDATA
CLK_SCLK
CLK_SDATA
(5) M_A_ODT0
(5) M_A_ODT1
(5) M_A_DM[7:0]
(5) M_A_DQSP[7:0]
(5) M_A_DQSN[7:0]
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0_H=4_Standard
+1.5V_SUS
2.48A
+3V
R255 *10K/J_4
(4) PM_EXTTS#0
(15,31) DDR3_DRAMRST#
+SMDDR_VREF_DQ0
+SMDDR_VREF_DIMM
+0.75V_DDR_VTT
R149 *10K/J_4
R162 0_6
R163 *10K/J_4
C325 470P/50V_4
+SMDDR_VREF
+SMDDR_VREF_DIMM
R111 10K/F_4
R116 10K/F_4
R123 *M1@0_6
R122 *M3@0_6
(7) VREF_DQ_DIMM0
Place these Caps near So-Dimm0.
C252 10U/6.3V_6
C287 10U/6.3V_6
C271 10U/6.3V_6
C276 0.1U/16V_4
C308 0.1U/16V_4
C273 10U/6.3V_6
C262 10U/6.3V_6
C286 10U/6.3V_6
C265 0.1U/16V_4
C279 0.1U/16V_4
C278 0.1U/16V_4
C310 *330U/2V_7343
C326 0.1U/16V_4
C322 2.2U/6.3V_6
C206 0.1U/16V_4
C208 2.2U/6.3V_6
C365 2.2U/6.3V_6
C370 0.1U/16V_4
C389 1U/6.3V_4
C386 1U/6.3V_4
C378 1U/6.3V_4
C388 1U/6.3V_4
C373 10U/6.3V_6
C395 10U/6.3V_6
C374 10U/6.3V_6
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Size
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DDRIII SO-DIMM-0
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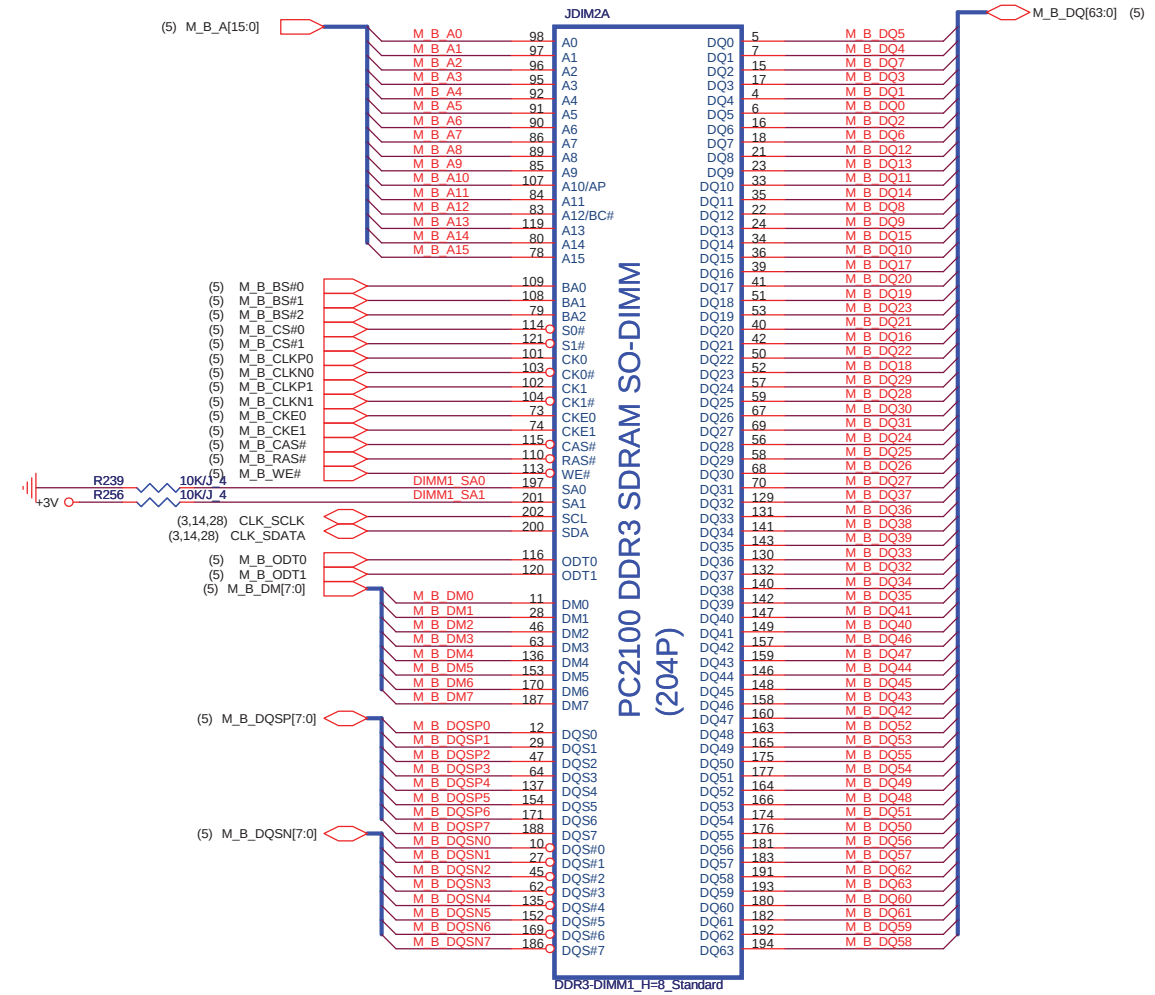

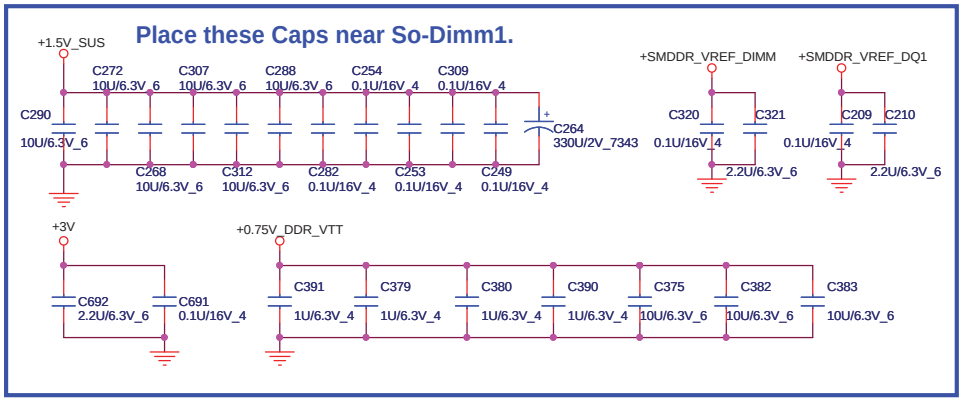

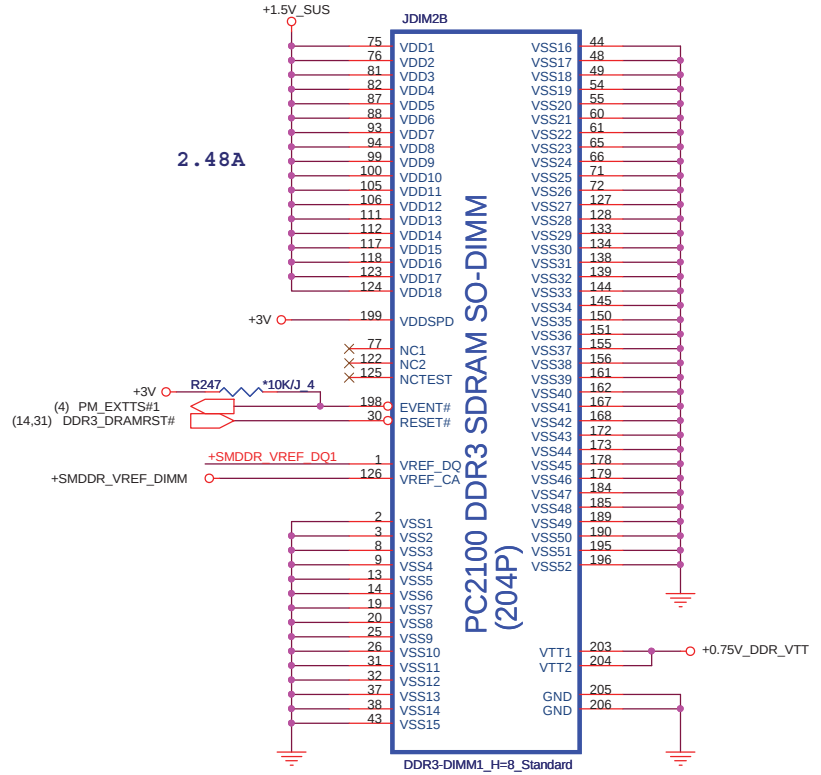

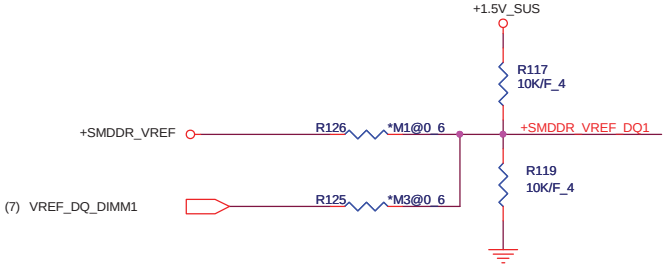

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Size	Document Number: DDRIII SO-DIMM-1	Rev: 1A
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N11P	AJ0N11P0T19
N11M	AJ0N11M0T20

SW@ --> iGPU & GPU Switch
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only
CSP@ --> Operation P/N

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

U35A
fcbga973-nvidia-n11p-es-a1
COMMON

+1.05V_GFX
~ 500mA
C109 SW@0.1U/10V_4
C98 SW@0.1U/10V_4
C118 SW@1U/6.3V_4
C128 SW@1U/6.3V_4
C201 SW@4.7U/6.3V_6
C176 SW@4.7U/6.3V_6
C185 SW@10U/6.3V_8
AK16 AK17 AK21 AK24 AK27

+1.05V_GFX
1600mA
C127 SW@0.1U/10V_4
C97 SW@0.1U/10V_4
C96 SW@1U/6.3V_4
C138 SW@1U/6.3V_4
C171 SW@4.7U/6.3V_6
C167 SW@4.7U/6.3V_6
C202 SW@10U/6.3V_8
Near BGA
AG11 AG12 AG13 AG15 AG16 AG17 AG18 AG22 AG23 AG24 AG25 AG26 AJ14 AJ15 AJ19 AJ21 AJ22 AJ24 AJ25 AJ27 AK18 AK20 AK23 AK26 AL16

PEX_IOVDD_1 PEX_IOVDD_2 PEX_IOVDD_3 PEX_IOVDD_4 PEX_IOVDD_5
PEX_IOVDDQ_1 PEX_IOVDDQ_2 PEX_IOVDDQ_3 PEX_IOVDDQ_4 PEX_IOVDDQ_5 PEX_IOVDDQ_6 PEX_IOVDDQ_7 PEX_IOVDDQ_8 PEX_IOVDDQ_9 PEX_IOVDDQ_10 PEX_IOVDDQ_11 PEX_IOVDDQ_12 PEX_IOVDDQ_13 PEX_IOVDDQ_14 PEX_IOVDDQ_15 PEX_IOVDDQ_16 PEX_IOVDDQ_17 PEX_IOVDDQ_18 PEX_IOVDDQ_19 PEX_IOVDDQ_20 PEX_IOVDDQ_21 PEX_IOVDDQ_22 PEX_IOVDDQ_23 PEX_IOVDDQ_24 PEX_IOVDDQ_25

PCI EXPRESS

PEX_RX0 PEX_RX0* PEX_RX1 PEX_RX1* PEX_RX2 PEX_RX2* PEX_RX3 PEX_RX3* PEX_RX4 PEX_RX4* PEX_RX5 PEX_RX5* PEX_RX6 PEX_RX6* PEX_RX7 PEX_RX7* PEX_RX8 PEX_RX8* PEX_RX9 PEX_RX9* PEX_RX10 PEX_RX10* PEX_RX11 PEX_RX11* PEX_RX12 PEX_RX12* PEX_RX13 PEX_RX13* PEX_RX14 PEX_RX14* PEX_RX15 PEX_RX15*
AP17 AN17 AN19 AP19 AR19 AR20 AP20 AN20 AN22 AP22 AR22 AR23 AP23 AN23 AN25 AP25 AR25 AR26 AP26 AN26 AN28 AP28 AR28 AR29 AP29 AN29 AN31 AP31 AR31 AR32 AR34 AP34
PEG_TXP15 PEG_TXN15 PEG_TXP14 PEG_TXN14 PEG_TXP13 PEG_TXN13 PEG_TXP12 PEG_TXN12 PEG_TXP11 PEG_TXN11 PEG_TXP10 PEG_TXN10 PEG_TXP9 PEG_TXN9 PEG_TXP8 PEG_TXN8 PEG_TXP7 PEG_TXN7 PEG_TXP6 PEG_TXN6 PEG_TXP5 PEG_TXN5 PEG_TXP4 PEG_TXN4 PEG_TXP3 PEG_TXN3 PEG_TXP2 PEG_TXN2 PEG_TXP1 PEG_TXN1 PEG_TXP0 PEG_TXN0
PEG_TXP15 (4) PEG_TXN15 (4) PEG_TXP14 (4) PEG_TXN14 (4) PEG_TXP13 (4) PEG_TXN13 (4) PEG_TXP12 (4) PEG_TXN12 (4) PEG_TXP11 (4) PEG_TXN11 (4) PEG_TXP10 (4) PEG_TXN10 (4) PEG_TXP9 (4) PEG_TXN9 (4) PEG_TXP8 (4) PEG_TXN8 (4) PEG_TXP7 (4) PEG_TXN7 (4) PEG_TXP6 (4) PEG_TXN6 (4) PEG_TXP5 (4) PEG_TXN5 (4) PEG_TXP4 (4) PEG_TXN4 (4) PEG_TXP3 (4) PEG_TXN3 (4) PEG_TXP2 (4) PEG_TXN2 (4) PEG_TXP1 (4) PEG_TXN1 (4) PEG_TXP0 (4) PEG_TXN0 (4)

PEX_TX0 PEX_TX0* PEX_TX1 PEX_TX1* PEX_TX2 PEX_TX2* PEX_TX3 PEX_TX3* PEX_TX4 PEX_TX4* PEX_TX5 PEX_TX5* PEX_TX6 PEX_TX6* PEX_TX7 PEX_TX7* PEX_TX8 PEX_TX8* PEX_TX9 PEX_TX9* PEX_TX10 PEX_TX10* PEX_TX11 PEX_TX11* PEX_TX12 PEX_TX12* PEX_TX13 PEX_TX13* PEX_TX14 PEX_TX14* PEX_TX15 PEX_TX15*
AL17 AM17 AM18 AM19 AL19 AK19 AL20 AM20 AM21 AM22 AL22 AK22 AL23 AM23 AM24 AM25 AL25 AK25 AL26 AM26 AM27 AM28 AL28 AK28 AK29 AL29 AM29 AM30 AM31 AM32 AM32 AN32 AP32
PEG_RXP15_C PEG_RXN15_C PEG_RXP14_C PEG_RXN14_C PEG_RXP13_C PEG_RXN13_C PEG_RXP12_C PEG_RXN12_C PEG_RXP11_C PEG_RXN11_C PEG_RXP10_C PEG_RXN10_C PEG_RXP9_C PEG_RXN9_C PEG_RXP8_C PEG_RXN8_C PEG_RXP7_C PEG_RXN7_C PEG_RXP6_C PEG_RXN6_C PEG_RXP5_C PEG_RXN5_C PEG_RXP4_C PEG_RXN4_C PEG_RXP3_C PEG_RXN3_C PEG_RXP2_C PEG_RXN2_C PEG_RXP1_C PEG_RXN1_C PEG_RXP0_C PEG_RXN0_C
C130 C137 C126 C120 C119 C115 C114 C110 C107 C104 C103 C95 C88 C93 C84 C86 C81 C75 C71 C65 C63 C64 C62 C61 C58 C59 C57 C54 C48 C47 C50 C52
SW@0.1U/10V_4
PEG_RXP15 (4) PEG_RXN15 (4) PEG_RXP14 (4) PEG_RXN14 (4) PEG_RXP13 (4) PEG_RXN13 (4) PEG_RXP12 (4) PEG_RXN12 (4) PEG_RXP11 (4) PEG_RXN11 (4) PEG_RXP10 (4) PEG_RXN10 (4) PEG_RXP9 (4) PEG_RXN9 (4) PEG_RXP8 (4) PEG_RXN8 (4) PEG_RXP7 (4) PEG_RXN7 (4) PEG_RXP6 (4) PEG_RXN6 (4) PEG_RXP5 (4) PEG_RXN5 (4) PEG_RXP4 (4) PEG_RXN4 (4) PEG_RXP3 (4) PEG_RXN3 (4) PEG_RXP2 (4) PEG_RXN2 (4) PEG_RXP1 (4) PEG_RXN1 (4) PEG_RXP0 (4) PEG_RXN0 (4)

+3V_GFX
C132 SW@4.7U/6.3V_6
C142 SW@1U/6.3V_4
C152 SW@0.1U/10V_4
C149 SW@0.1U/10V_4
C141 SW@0.1U/10V_4
J10 J11 J12 J13 J9
VDD33_1 VDD33_2 VDD33_3 VDD33_4 VDD33_5

T6 T1 T8
AD20 D35 P7
VDD_SENSE NC_9/ VDD_SENSE NC_16/ VDD_SENSE

12~16 mils width 110mA
+1.05V_GFX
C161 SW@1U/6.3V_4
C108 SW@1U/6.3V_4
L3 SW@100nH_6
C133 SW@1U/6.3V_4
C144 SW@4.7U/6.3V_6
+PEX_PLLVDD
AD19 E35 R7 AG14
GND_SENSE NC_10/ GND_SENSE NC_17/ GND_SENSE
PEX_PLLVDD

12~16 mils width
+3V_GFX
L6 SW@0_6 +PEX_SVDD_3V3
AG19 F7
C117 SW@1U/6.3V_4
C162 SW@0.1U/10V_4
C164 SW@4.7U/6.3V_6
AG20 A2 AB7 AD6 AF6 AG6 AJ5 AK15 AL7 E7 H32 M7 P6 U7 V6
PEX_CAL_PD_VDDQ/ PEX_SVDD_3V3 NC_12/ PEX_SVDD_3V3
PEX_CAL_PU_GND/ NC NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_11 NC_13 NC_14 NC_15 NC_18 NC_19

PEX_REFCLK AR16
PEX_REFCLK* AR17
CLK_PCIE_VGAP (10)
CLK_PCIE_VGAN (10)

PEX_TSTCLK_OUT AJ17 PEX_TSTCLK R51 *SW@200/J_4
PEX_TSTCLK_OUT* AJ18 PEX_TSTCLK#
R458 SW@100K_4
R457 SW@0_4
GPU_RST# (11)

PEX_RST* AM16 VGA_RST# R456 *SW@0_4
PLTRST# (4,10,11,25,26,28,31,36)

PEX_CLKREQ* AR13 PEX_CLKREQ# R467 SW@10K/F_4
+3V_GFX

PEX_TERMP AG21 PEX_TERMP R49 SW@2.49K/F_4

TESTMODE AP35 TESTMODE R449 SW@10K/F_4
R448 *SW@10K/F_4
+3V_GFX

R3589 un-mount for switchable function

Only for Hybrid
+3V_GFX
R80 SW@10K/F_4
Q20 SW@DTC144EUA
R489 SW@10K/F_4
+3V_S5
PEG_CLKREQ# (10)
PEX_CLKREQ#
Q6 SW@DTC144EUA

+3V VDD33
+1.05V PEX_VDD
V_CORE NVVDD
+1.8V IFPAB_IOVDD
+1.5V FBVDDQ
PEX_VDD can ramp up any time
tNVVDD
tNV-IFPAB_IOVDD
tNV-FBVDDQ

power up sequence

PXE 1.05VDD
I/O 3.3V
NVCORE
1.5VFBDDQ

NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time

NVVDD
GPIO
tsNVVDD<= 192us

PEX_RST timing

I/O 3.3V
PEX_RST
Trise >= 1uS
Tfail <=500nS

Quanta Computer Inc.
PROJECT : ZR9

Size	Document Number	Rev
	N11P-GE (PCIE I/F) 1/5	1A
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SW@ --> iGPU & GPU Switch
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only

N11P	AJ0N11P0T19
N11M	AJ0N11M0T20

U35B
fcbga973-nvidia-n11p-es-a1
COMMON

U35C
fcbga973-nvidia-n11p-es-a1
COMMON

(21) VMA_DQ[63..0]
(21) VMA_DM[7..0]
(21) VMA_WDQS[7..0]
(21) VMA_RDQS[7..0]
(22) VMC_DQ[63..0]
(22) VMC_DM[7..0]
(22) VMC_WDQS[7..0]
(22) VMC_RDQS[7..0]

VMA_CMD25 R27 SW@10K/F_4
VMA_CMD16 R447 SW@10K/F_4
VMA_CMD0 R444 SW@10K/F_4
VMA_CMD27 R23 SW@10K/F_4
VMA_CMD28 R38 SW@10K/F_4

VMC_CMD25 R56 SNP@10K/F_4
VMC_CMD16 R453 SNP@10K/F_4
VMC_CMD0 R455 SNP@10K/F_4
VMC_CMD27 R40 SNP@10K/F_4
VMC_CMD28 R454 SNP@10K/F_4

Un-stuff for N11M
Stuff for N11P ,N11S

+1.5V_GFX

FB_VREF J27 +FB_VREF1 T4
15mils width

MEMORY I/F A

For Debug only
FBA_DEBUG T30 FBA_DEBUG R42 *SW@10K/F_4 +1.5V_GFX
15mils width
SW@PBY160808T-301Y-N_6
FB_DLLAVDD0 AG27 +FB_PLLAVDD L2 +1.05V_GFX
FB_PLLAVDD0 AF27 C83 SW@4.7U/6.3V_6
C82 SW@1U/6.3V_4
C85 SW@0.1U/10V_4

4/20 reserved for long run
+1.5V_GFX C755 *SW@10U/6.3V_6 C756 *SW@10U/6.3V_6
+1.05V_GFX C757 *SW@10U/6.3V_6 C758 *SW@10U/6.3V_6

+1.5V_GFX
C72 SW@0.01U/25V_4
C73 SW@0.01U/25V_4
C78 SW@0.01U/25V_4
C77 SW@0.01U/25V_4
C106 SW@0.1U/10V_4
C92 SW@0.1U/10V_4
C74 SW@0.1U/10V_4
C69 SW@0.047U/10V_4
C67 SW@0.047U/10V_4
C79 SW@0.047U/10V_4
C124 SW@4.7U/6.3V_6
C53 SW@4.7U/6.3V_6
All need stuff for N10P

MEMORY I/F C

FB_CAL_PD_VDDQ K27 FB_CAL_PD_VDDQ R43 SW@40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND L27 FB_CAL_PU_GND R48 SW@40.2/F_4
FB_CAL_TERM_GND M27 FB_CAL_TERM_GND R46 SNP@40.2/F_4
R47 SNM@60.4/F_4
FBC_DEBUG G19 FBC_DEBUG R50 *SW@10K/F_4 +1.5V_GFX
NC/ FB_DLLAVDD1 J19
NC/ FB_PLLAVDD1 J18

N11P-GE1 Stuff 40.2 ohm
N11M-GE1 Stuff 60.4 ohm

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PROJECT : ZR9

Size	Document Number	Rev
	N11P-GE (MEMORY I/F) 2/5	1A
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SW@ --> iGPU & GPU Switch
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only

N11P	AJ0N11P0T19
N11M	AJ0N11M0T20

fcbga973-nvidia-n11p-es-a1
U35D COMMON

IFPAB(LVDS)
IFPAB_PLLVDD
IFPAB_RSET
IFPA_IOVDD
IFPB_IOVDD
IFPA_TXC AM11
IFPA_TXC* AM12
IFPA_TXD0 AM8
IFPA_TXD0* AL8
IFPA_TXD1 AM10
IFPA_TXD1* AM9
IFPA_TXD2 AK10
IFPA_TXD2* AL10
IFPA_TXD3 AK11
IFPA_TXD3* AL11
IFPB_TXC AP13
IFPB_TXC* AN13
IFPB_TXD4 AN8
IFPB_TXD4* AP8
IFPB_TXD5 AP10
IFPB_TXD5* AN10
IFPB_TXD6 AR11
IFPB_TXD6* AR10
IFPB_TXD7 AN11
IFPB_TXD7* AP11

EV_TXLCLKOUTP (23)
EV_TXLCLKOUTN (23)
EV_TXLOUTP0 (23)
EV_TXLOUTN0 (23)
EV_TXLOUTP1 (23)
EV_TXLOUTN1 (23)
EV_TXLOUTP2 (23)
EV_TXLOUTN2 (23)

LVDS clk spread : Center
+/-0.5% (30~33KHZ)

IFPCD
IFPCD_PLLVDD/ IFPC_PLLVDD/ DACB_VDD/ IFPD_PLLVDD
IFPCD_RSET/ IFPC_RSET
DACB_RSET/ IFPD_RSET
IFPC_IOVDD
IFPD_IOVDD

IFPC
I2CW_SDA/ IFPC_AUX_N AN3
I2CW_SCL/ IFPC_AUX AP2
IFPC_L3_N AR2
IFPC_L3 AP1
IFPC_L2_N AM4
IFPC_L2 AM3
IFPC_L1_N AM5
IFPC_L1 AL5
IFPC_L0_N AM6
IFPC_L0 AM7

IFPD
I2CX_SDA/ IFPD_AUX_N AN4
I2CX_SCL/ IFPD_AUX AP4
IFPD_L3_N AR4
IFPD_L3 AR5
IFPD_L2_N AP5
IFPD_L2 AN5
IFPD_L1_N AN7
IFPD_L1 AP7
IFPD_L0_N AR7
IFPD_L0 AR8

TMDS channel two

IFPEF
IFPEF_RSET
IFPEF_PLLVDD
IFPE_IOVDD
IFPF_IOVDD

I2CY_SCL/ IFPE_AUX AE4
I2CY_SDA/ IFPE_AUX* AD4
IFPE_L0 AH6
IFPE_L0* AH5
IFPE_L1 AH4
IFPE_L1* AG4
IFPE_L2 AF4
IFPE_L2* AF5
IFPE_L3 AE6
IFPE_L3* AE5
I2CZ_SCL/ IFPF_AUX AF3
I2CZ_SDA/ IFPF_AUX* AF2
IFPF_L0 AL2
IFPF_L0* AL3
IFPF_L1 AJ3
IFPF_L1* AJ2
IFPF_L2 AJ1
IFPF_L2* AH1
IFPF_L3 AH2
IFPF_L3* AH3

MXM_DDCCK_C
MXM_DDCDAT_C
MXM_DDCCK_C (24)
MXM_DDCDAT_C (24)
HDMITXP2 (24)
HDMITXN2 (24)
HDMITXP1 (24)
HDMITXN1 (24)
HDMITXP0 (24)
HDMITXN0 (24)
HDMICLKP (24)
HDMICLKN (24)

Display port output

DACA(CRT)
DACA_VDD
DACA_VREF
DACA_RSET
DACA_RED AM15
DACA_GREEN AM14
DACA_BLUE AL14
DACA_HSYNC AM13
DACA_VSYNC AL13
I2CA_SCL G1
I2CA_SDA G4

EV_CRT_RED
EV_CRT_GRE
EV_CRT_BLU
EV_CRT_RED (23)
EV_CRT_GRE (23)
EV_CRT_BLU (23)
EV_HSYNC_R R469 SW@33_4
EV_VSYNC_R R470 SW@33_4
EV_HSYNC (23)
EV_VSYNC (23)
EV_CRTDCLK
EV_CRTDDAT
EV_CRTDCLK (23)
EV_CRTDDAT (23)

DACC(CRT2)
DACC_VDD/ DACB_VDD
DACC_VREF/ DACB_VREF
DACC_RSET/ DACB_RSET
/DACC_RED DACB_RED AK4
/DACC_GREEN DACB_GREEN AL4
/DACC_BLUE DACB_BLUE AJ4
DACB_HSYNC/ DACC_HSYNC AM1
DACB_VSYNC/ DACC_VSYNC AM2
I2CB_SCL G3
I2CB_SDA G2

I2CB_SCL R85 SW@2.2K_4
I2CB_SDA R86 SW@2.2K_4
+3V_GFX
PLACE CLOSE TO GPU

DACB(TV)
DACB_VREF/ NC AC5
NC/ DACB_RED AA4
NC/ DACB_GREEN AB4
NC/ DACB_BLUE Y4
CEC/ DACB_CSYNC AB5
DACB_CSYNC R74 SW@10K/F_4

XTAL_PLL
PLLVDD
VID_PLLVDD
SP_PLLVDD
XTAL_SSIN AE9
XTAL_OUTBUFF AD9
XTAL_IN B1
XTAL_OUT B2
XTALI_27M
XTALO_27M
Y5
C596 SW@33P/50V_4
SW@27MHZ
C595 SW@33P/50V_4

D2 XTAL_SSIN R497 *SW@22_4 CLK_27M_SS (3)
D1 BXTALOUT
XTALI_27M R487 *SW@0_4 27M_CLK (3)

STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

+1.05V_GFX L4 SW@FBMA-10-160808-300T_6 +IFPAB_PLLVDD 220 mA AK9
C160 SW@1U/6.3V_4
C168 SW@4.7U/6.3V_6
R52 IFPAB_RSET AJ11 *SW@1K/F_4
+1.8V_GFX L11 SW@FBMA-10-160808-300T_6 +IFPAB_IOVDD 200 mA AG9 AG10
C155 SW@0.1U/10V_4
C192 SW@0.1U/10V_4
C195 SW@1U/6.3V_4
C197 SW@4.7U/6.3V_6

R66 SW@10K/F_4 +IFPCD_PLLVDD AJ9 AC6
R63 IFPC_RSET AK7
R68 IFPD_RSET AB6 *SW@1K/F_4 *SW@1K/F_4
+3V_GFX L10 SW@FBMA-10-160808-300T_6 220 mA IFPEF_PLLVDD
C172 SW@0.1U/10V_4
C182 SW@1U/6.3V_4
C194 SW@0.1U/10V_4
C196 SW@0.1U/10V_4
C200 SW@4.7U/6.3V_6
R55 SW@10K/F_4 +IFPCD_IOVDD AJ8 AK8
R476 SW@1K/F_4 IFPE_RSET AL1

(1.05V +/- 3%)
+1.05V_GFX L9 SW@MLB-201209-0030P-N1-RU_8 285 mA IFPEF_PLLVDD AJ6 IFPEF_IOVDD AE7 AD7
C179 SW@0.1U/10V_4
C187 SW@0.1U/10V_4
C184 SW@1U/6.3V_4
C193 SW@4.7U/6.3V_6
11/19 modify
+3V_GFX L5 SW@PBY160808T-301Y-N_6
C151 SW@0.1U/10V_4
C156 SW@0.1U/10V_4
C166 SW@0.1U/10V_4
+DACA_VDD 120 mA AJ12
C159 SW@1U/6.3V_4
C175 SW@4.7U/6.3V_6
C170 SW@4700P/25V_4
C143 SW@470P/50V_4
4/17
Add a 1UF for monitor test
C315 SW@1U/6.3V_4
C165 SW@0.1U/10V_4 DACA_VREF AK12
R65 SW@124/F_4 DACA_RSET AK13
R69 SW@10K/F_4 +DACB_VDD AG7 AK6 AH7

SW@CS0603-R10J-S_6
+1.05V_GFX L8 +NV_PLLVDD 60mA AE9 AD9
C158 SW@0.1U/10V_4
C169 SW@0.1U/10V_4
C173 SW@1U/6.3V_4
C181 SW@4.7U/6.3V_6
SW@CS0603-R10J-S_6
+1.05V_GFX L7 +NV_SPPLLVDD 45mA AF9
C174 SW@1U/6.3V_4
C180 SW@4.7U/6.3V_6

GPU all PWROK
+3V_GFX
+3V_S5
R506 SW@100K_4
R496 SW@10K_4
dGPU_PWROK (11)
Q25 SW@2N7002E
+1.8V_GFX
Q7 SW@PDTC143TT

+3V_GFX
R87 SW@4.7K_4 EV_CRTDCLK
R88 SW@4.7K_4 EV_CRTDDAT
R474 SW@4.7K_4 MXM_DDCCK_C
R473 SW@4.7K_4 MXM_DDCDAT_C

EV_CRT_RED R54 SW@150/F_4
EV_CRT_GRE R61 SW@150/F_4
EV_CRT_BLU R53 SW@150/F_4

XTAL_SSIN R485 SW@10K/F_4
BXTALOUT R486 SW@10K/F_4

10 kΩ pull-down only if no spread chip used.

Quanta Computer Inc.
PROJECT : ZR9

Size	Document Number	Rev
	N11P-GE (DISPLAY) 3/5	1A
Date: Thursday, May 06, 2010	Sheet 18 of 47	

SW@ --> iGPU & GPU Switch
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only
CSP@ --> Operation P/N

N11P	AJ0N11P0T19
N11M	AJ0N11M0T20

U35E fcbga973-nvidia-n11p-es-a1 COMMON

MIOA
MIOA_VDDQ_1 P9
MIOA_VDDQ_2 R9
MIOA_VDDQ_3 T9
MIOA_VDDQ_4 U9
MIOA_CAL_PD_VDDQ U5
MIOA_CAL_PU_GND T5
MIOA_VREF N5
MIOA_CTL3 P5
MIOA_HSYNC N3
MIOA_VSYNC L3
MIOA_DE N2
MIOA_CLKOUT R4
MIOA_CLKOUT* T4
MIOA_CLKIN N4
MIOA_D0 N1 T59
MIOA_D1 P4 T66
MIOA_D2 P1 T58
MIOA_D3 P2 T65
MIOA_D4 P3 T43
MIOA_D5 T3 T62
MIOA_D6 T2 T45
MIOA_D7 T1 T52
MIOA_D8 U4 T48
MIOA_D9 U1 T40
MIOA_D10 U2 T60
MIOA_D11 U3 T55
MIOA_D12 R6
MIOA_D13 T6
MIOA_D14 N6

MIOB
MIOB_VDDQ_1 AA9
MIOB_VDDQ_2 AB9
MIOB_VDDQ_3 W9
MIOB_VDDQ_4 Y9
MIOB_CAL_PD_VDDQ AA7
MIOB_CAL_PU_GND AA6
MIOB_VREF AF1
MIOB_CTL3 W3
MIOB_HSYNC W1
MIOB_VSYNC W2
MIOB_DE Y5
MIOB_CLKOUT V4
MIOB_CLKOUT* W4
MIOB_CLKIN AE1
MIOB_D0 Y1 T54
MIOB_D1 Y2 T47
MIOB_D2 Y3 T61
MIOB_D3 AB3 T51
MIOB_D4 AB2 T44
MIOB_D5 AB1 T64
MIOB_D6 AC4 T56
MIOB_D7 AC1 T49
MIOB_D8 AC2 T42
MIOB_D9 AC3 T63
MIOB_D10 AE3 T57
MIOB_D11 AE2 T50
MIOB_D12 U6
MIOB_D13 W6
MIOB_D14 Y6
STRAP0 W5
STRAP1 W7
STRAP2 V7

THERMDN B4
THERMDP B5

MISC1 (GPIOS,JTAG,THERM,I2C)
JTAG_TCK AP14
JTAG_TMS AR14
JTAG_TDI AN14
JTAG_TDO AN16
JTAG_TRST* AP16
I2CS_SCL E2
I2CS_SDA E1
I2CC_SCL E3
I2CC_SDA E4
I2CD_SCL/ NC F4
I2CD_SDA/ NC G5
I2CE_SCL/ NC D5
I2CE_SDA/ NC E5
GPIO0 K1 T41
GPIO1 K2
GPIO2 H3 EV_LVDS_BRIGHT
GPIO3 H2 EV_LVDS_VDDEN
GPIO4 H1 EV_LVDS_BLON
GPIO5 H4 GPU_VID1
GPIO6 H5 GPU_VID2
GPIO7 H6 VGA_OVT# T9
GPIO8 J7 ALERT#
GPIO9 K4
GPIO10 K5 T46
GPIO11 H7 T53 VGA_ACIN
GPIO12 J4
GPIO13 J6
GPIO14 L1 HDMI_HP_EV
GPIO15 L2
GPIO16 L4
GPIO17 M4 DGPU_IDLE_INT#
GPIO18 L7
GPIO19 L5
GPIO20 K6
GPIO21 L6
GPIO22 M6
GPIO23

MISC2(ROM)
BBIASN_NC J26
BBIASP_NC J25
HDA_BCLK/ NC D7
HDA_RST*/ NC D6
HDA_SDI/ NC C7
HDA_SDO/ NC B7
HDA_SYNC/ NC A7
STRAP_REF_3V3/ MULTI_STRAP_REF0_GND N9
STRAP_REF_MIOB/ MULTI_STRAP_REF1_GND M9
ROM_CS* C3
ROM_SI D3
ROM_SO C4
ROM_SCLK D4
I2CH_SCL F6
I2CH_SDA G6
SPDIF A5 T39
BUFRST* A4
NC C5
GND AK14
GND/ NC K9

SW@
N11P/M : Stuff 0 ohm
N11X-FERMI : UnStuff 0 ohm

SW@
N11P/M: Stuff 0.1uF
N11X-FERMI : Stuff 10K ohm

SW@
N11PX : Stuff 10 Kohm
N11X-FERMI : UnStuff 10 Kohm

SW@
N11P/M: Stuff 10 Kohm
N11X-FERMI : UnStuff 10 Kohm

A5 N.C due to N11X HAD function is through PCI-E interface

11/25 NV request add 10K PU

10/20

VGA Thermal
ADDRESS: 9AH

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
0000		Reserved		
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
0101		Reserved		
0110				
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

(Ra)

AKD58GGT^01
AKD5LZGTW00
AKD5LGGT502

Logical Strap Bit Mapping

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

(Ra)
Default: Hynix VRAM
Hynix =15K pull down(64Mx16)
Samsung =20k pull down(64Mx16)

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)
30K/F_4: CS33002JB23 [RES CHIP 30K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

CHIP	ROM_SCLK	STRAP2	PCI_DEVID
N11M-GE1	PU 15K	PD 30K	0x0A75
N11P-GE1	PU 15K	PU 10K	0x0A29

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

HDCP ROM

U37 AT88SC0808C-SU
Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

HDCP ROM reserve , Due to N11x had support internal HDCP function.

Quanta Computer Inc.
PROJECT : ZR9

Size	Document Number	Rev
	N11P-GE (GPIO&STRAPS) 4/5	1A
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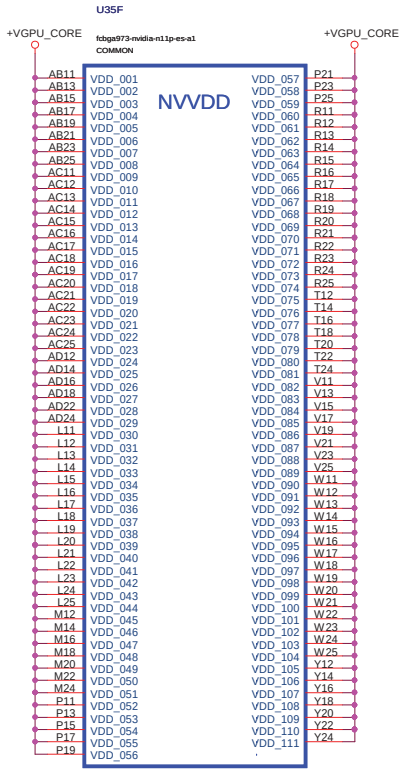
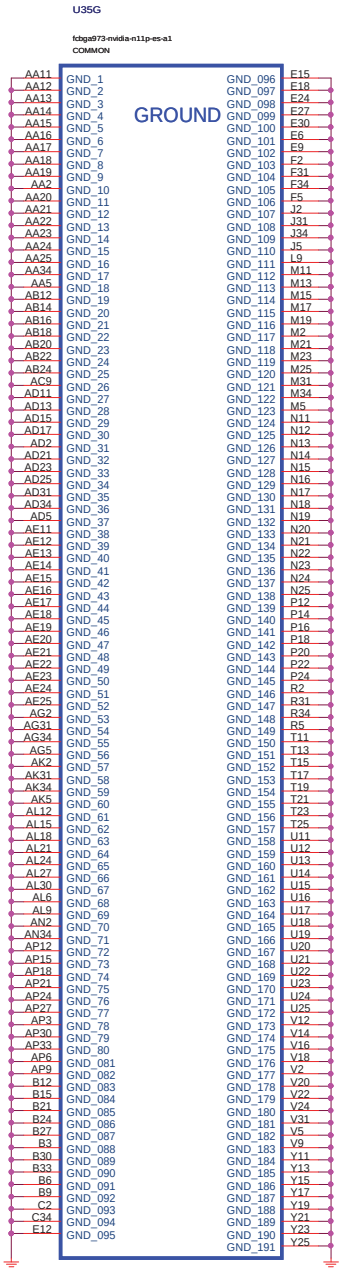
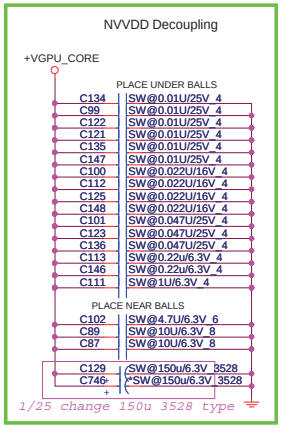
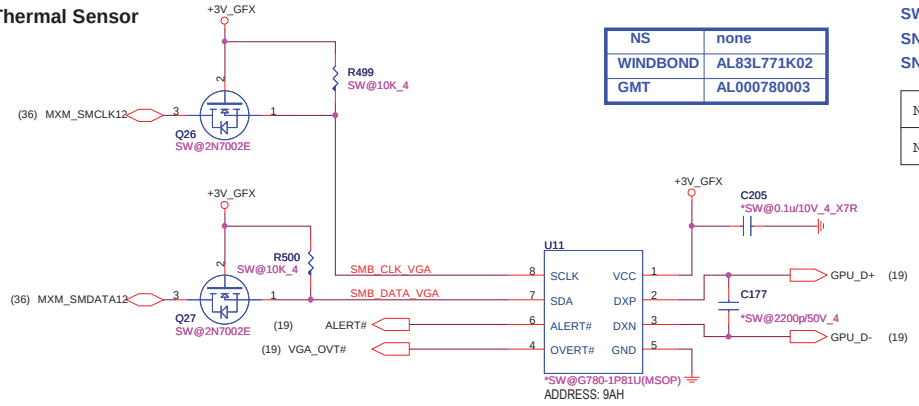






Thermal Sensor



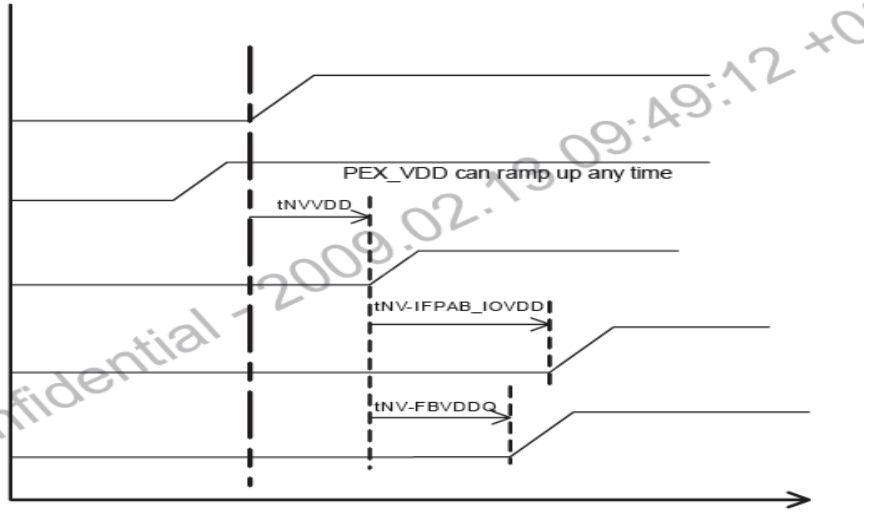
NS	none
WINDBOND	AL83L771K02
GMT	AL000780003

SW@ --> iGPU & GPU Switch
SNP@ --> GPU N11P only
SNM@ --> GPU N11M only

N11P	AJ0N11P0T19
N11M	AJ0N11M0T20

(19) SMB_CLK_VGA — SMB_CLK_VGA
(19) SMB_DATA_VGA — SMB_DATA_VGA

+3V VDD33
+1.05V PEX_VDD
V_CORE NVVDD
+1.8V IFPAB_IOVDD
+1.5V FBVDDQ



Quanta Computer Inc.
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Size	Document Number	Rev
	N11P-GE (POWER & GND&THM) 5/5	1A

Date: Thursday, May 06, 2010 Sheet 20 of 47

SNP@ --> GPU N11P only
SNM@ --> GPU N11M only

HYU	AKD5LZGTW04
SAM	AKD5LGGT506

(17) VMA_DQ[63..0]
(17) VMA_DM[7..0]
(17) VMA_WDQS[7..0]
(17) VMA_RDQS[7..0]

CHANNEL A: 256MB/512MB DDR3

(17,22,45) +1.5V_GFX

U7 / U32 / U6 / U31 — 96-BALL SDRAM DDR3 — SW@VRAM _DDR3

Should be 240 Ohms +-1%

R37 SW@243/F_4
R443 SW@243/F_4
R24 SW@243/F_4
R446 SW@243/F_4

VMA_ZQ1
VMA_ZQ2
VMA_ZQ3
VMA_ZQ4

R445 SW@243/F_4
R30 SW@243/F_4

R441 SW@1.33K/F_4
R29 SW@1.33K/F_4
R26 SW@1.33K/F_4
R439 SW@1.33K/F_4

R442 SW@1.33K/F_4
R28 SW@1.33K/F_4
R25 SW@1.33K/F_4
R440 SW@1.33K/F_4

C553 SW@.1U/10V_4
C28 SW@.1U/10V_4
C22 SW@.1U/10V_4
C548 SW@.1U/10V_4

C105 C31 C131 C157 C80 C20 C91 C51 SW@1U/6.3V_4
C44 C546 C26 C45 SW@1U/6.3V_4
C186 C30 C25 C566 C35 C43 SW@10U/6.3V_6 / SW@1.1U/10V_4
C564 C549 C552 C27 C563 C565 C24 C551 SW@1.1U/10V_4
C559 C547 C40 C562 C38 C42 C39 C561 SW@1.1U/10V_4
C70 C49 C94 C116 SW@1U/6.3V_4
C23 C33 C545 C560 SW@1.1U/10V_4

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PROJECT : ZR9

Size	Document Number	Rev
	N11P-GE VRAM-1(DDR3 BGA96)	1A
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SNP@ --> GPU N11P only
SNM@ --> GPU N11M only

HYU	AKD5LZGTW04
SAM	AKD5LGGT506

CHANNEL B: 256MB/512MB DDR3

(17) VMC_DQ[63..0]
(17) VMC_DM[7..0]
(17) VMC_WDQS[7..0]
(17) VMC_RDQS[7..0]

(17,21,45) +1.5V_GFX

U36 — SNP@VRAM _DDR3

U10 — SNP@VRAM _DDR3

U9 — SNP@VRAM _DDR3

U33 — SNP@VRAM _DDR3

96-BALL SDRAM DDR3

Should be 240 Ohms +-1%

R463 SNP@243/F_4
R60 SNP@243/F_4
R41 SNP@243/F_4
R452 SNP@243/F_4

R72 SNP@243/F_4
R39 SNP@243/F_4

R461 SNP@1.33K/F_4
R460 SNP@1.33K/F_4
R62 SNP@1.33K/F_4
R64 SNP@1.33K/F_4
R45 SNP@1.33K/F_4
R44 SNP@1.33K/F_4
R450 SNP@1.33K/F_4
R451 SNP@1.33K/F_4

C586 SNP@.1U/10V_4
C163 SNP@.1U/10V_4
C68 SNP@.1U/10V_4
C572 SNP@.1U/10V_4

C570 SNP@1U/6.3V_4
C556 SNP@1U/6.3V_4
C594 SNP@1U/6.3V_4
C29 SNP@1U/6.3V_4
C550 SNP@1U/6.3V_4
C557 SNP@1U/6.3V_4
C593 SNP@1U/6.3V_4
C21 SNP@1U/6.3V_4

C36 SNP@1U/6.3V_4
C139 SNP@1U/6.3V_4
C584 SNP@1U/6.3V_4
C582 SNP@1U/6.3V_4

C568 SNP@10U/6.3V_6S
C66 SNP@.1U/10V_4
C575 SNP@.1U/10V_4
C579 SNP@.1U/10V_4
C580 SNP@.1U/10V_4
C558 SNP@.1U/10V_4

C583 SNP@.1U/10V_4
C588 SNP@.1U/10V_4
C555 SNP@.1U/10V_4
C76 SNP@.1U/10V_4
C581 SNP@.1U/10V_4
C585 SNP@.1U/10V_4
C571 SNP@.1U/10V_4
C150 SNP@.1U/10V_4

C554 SNP@.1U/10V_4
C140 SNP@.1U/10V_4
C145 SNP@.1U/10V_4
C590 SNP@.1U/10V_4
C90 SNP@.1U/10V_4
C592 SNP@.1U/10V_4
C587 SNP@.1U/10V_4
C569 SNP@.1U/10V_4

C178 SNP@1U/6.3V_4
C183 SNP@1U/6.3V_4
C60 SNP@1U/6.3V_4
C567 SNP@1U/6.3V_4

Quanta Computer Inc.
PROJECT : ZR9

Size	Document Number	Rev
	N11P-GE VRAM-2(DDR3 BGA96)	1A

Date: Thursday, May 06, 2010 Sheet 22 of 47

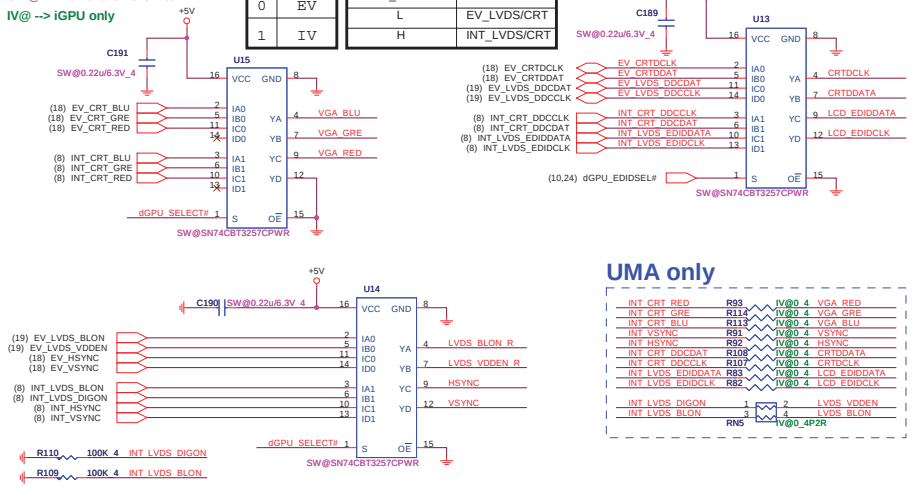
CRT Switch

SW@ --> iGPU & GPU Switch

IV@ --> iGPU only

S	Yn
0	EV
1	IV

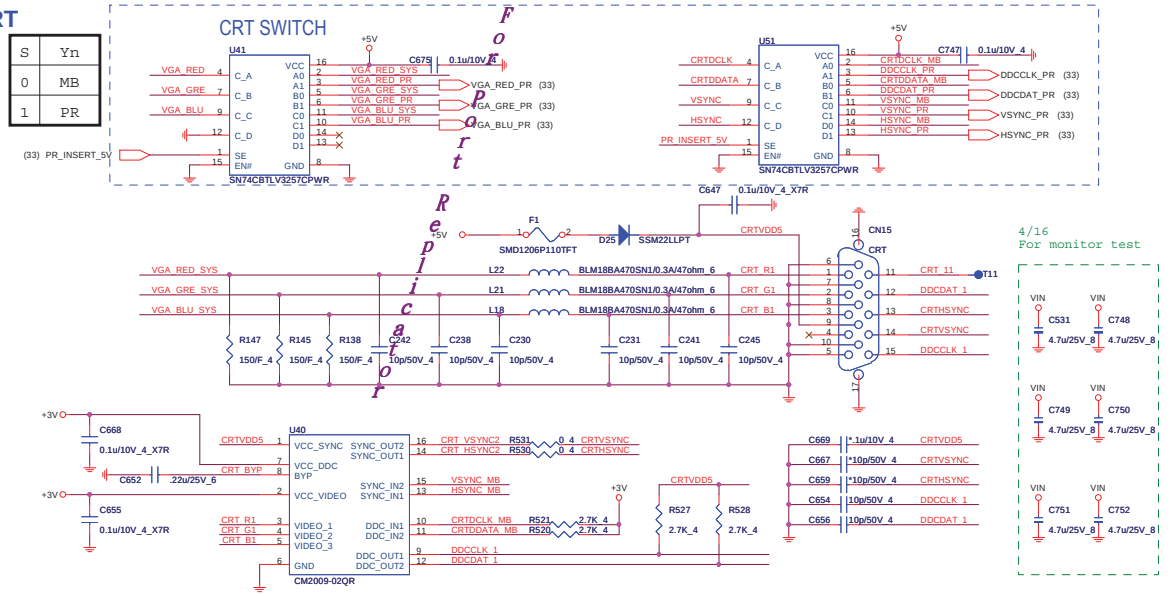
dGPU_SELECT# / dGPU_EDIDSEL#	Output
L	EV_LVDS/CRT
H	INT_LVDS/CRT



UMA only

CRT

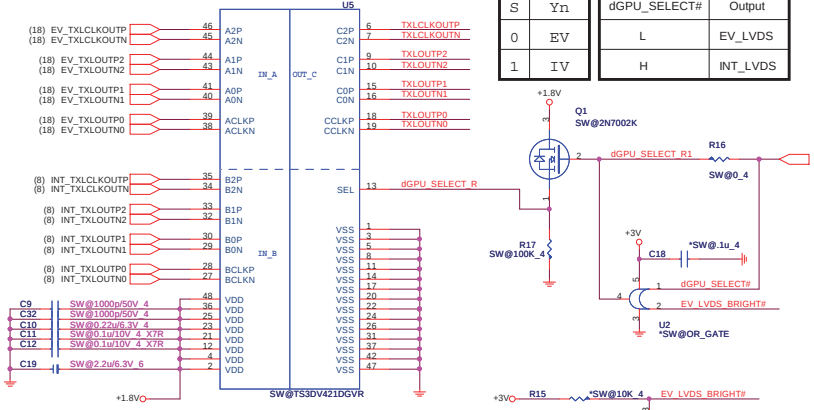
S	Yn
0	MB
1	PR



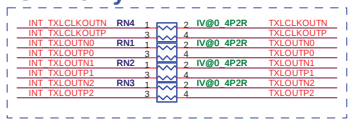
LVDS Switch

S	Yn
0	EV
1	IV

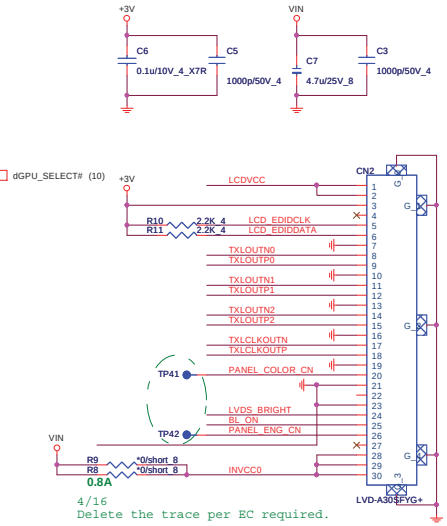
dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

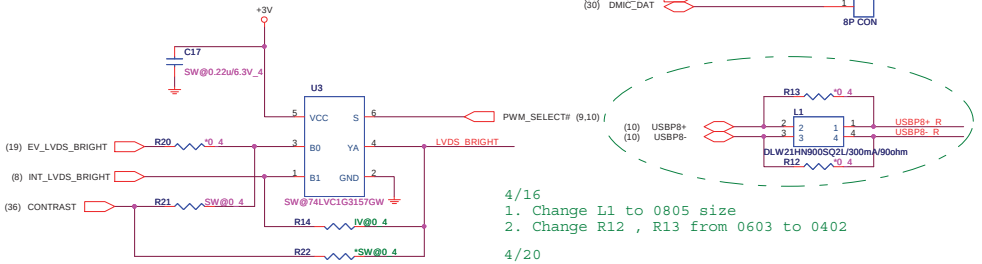


UMA only

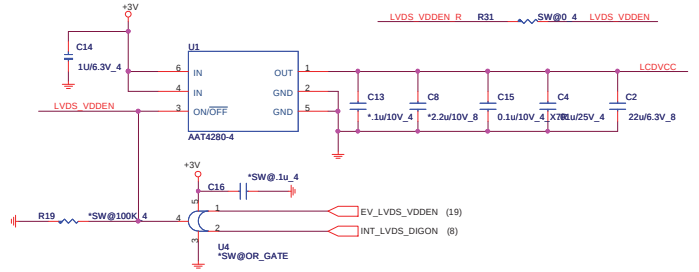


LVDS

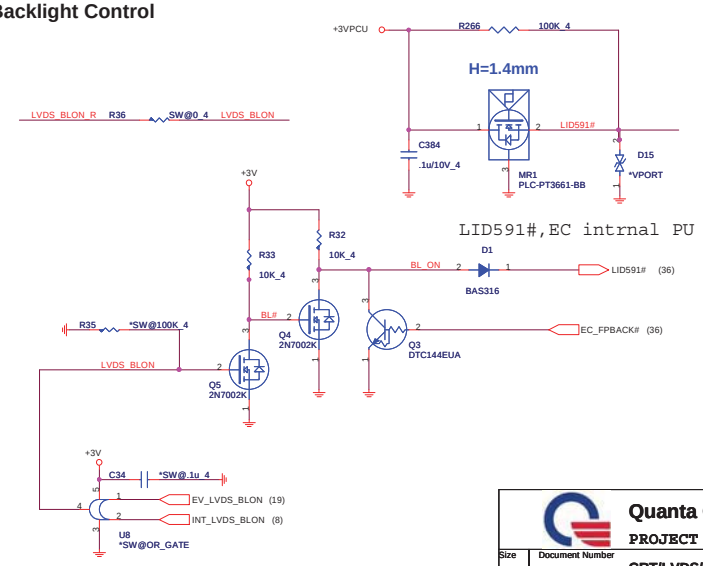




LCD Power



Backlight Control



Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	CRT/LVDS/CCD/HALL	1A

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I@ HDMI LEVEL SHIFTER

IV@ --> iGPU only
SW@ --> iGPU & GPU Switch
CSP@ --> Operation P/N

12/02 modify

from PCH

U22 — Active Buffer

Parade	AL008101000
TI	AL000139000

IV@DP139

from PCH

Control by pin4 HPDEN_R

TI 3.9K	CS23902JB00
PS 499	CS14992FB24

Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

close to pin2/11/15/21/26/33/40/46

NV HDMI-detect

To iGPU HPD
To NV HPD
OE# control for power saving

SDVO I2C Control

Quick Display

U18 — SW@SN74CBT3257CPWR

S	Yn
0	EV
1	IV

UMA	CS22202JB18
SW	CS24702JB38

CSP@ HDMI SDVO I2C For IV: 2.2K ohm For SW:4.7K ohm

NV suggestion near HDMI connector

Switchable Graphic HDMI source

To Discrete

ESD Protect

close to HDMI connector

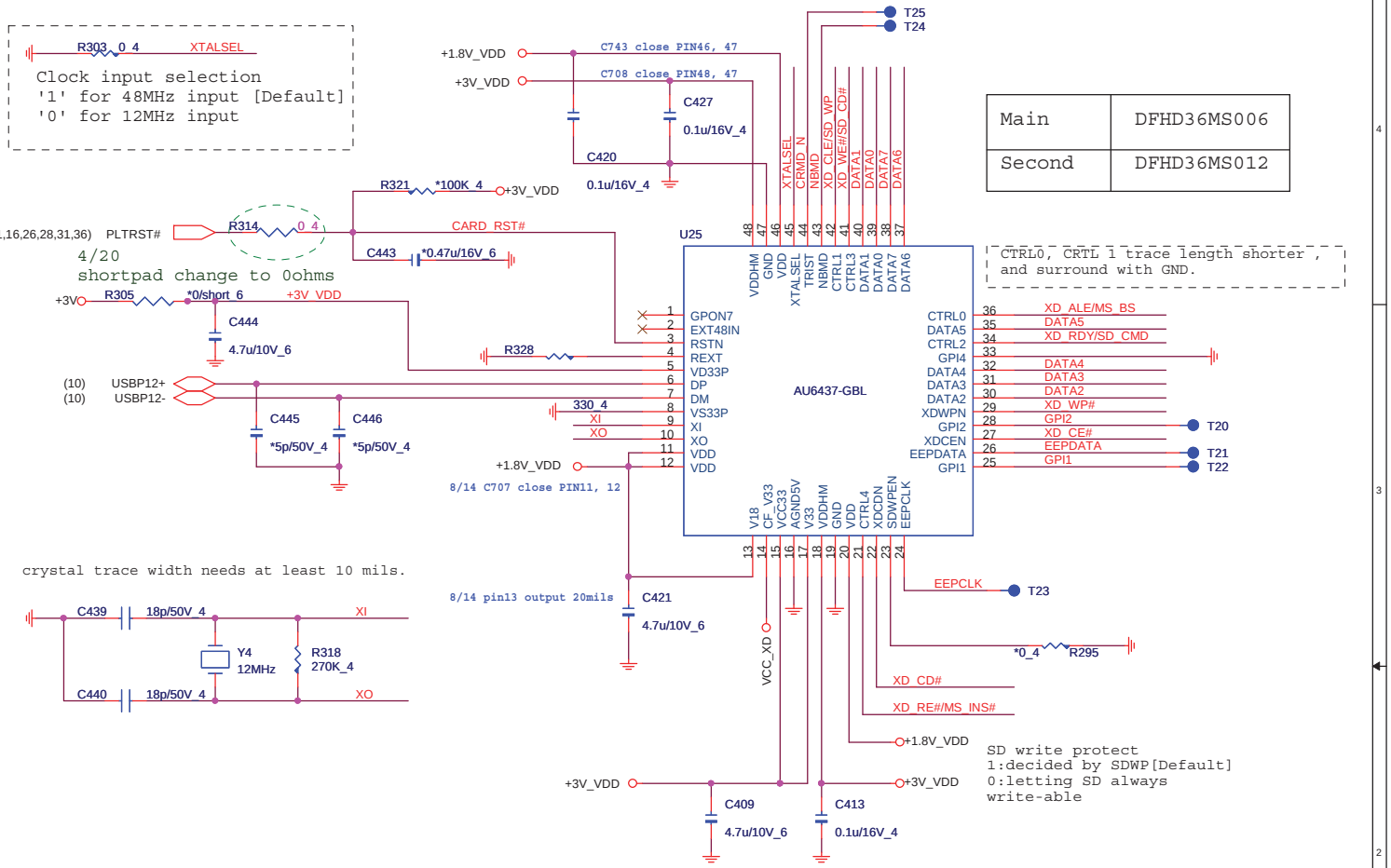
U44, U45, U19 — *RClamp0524P

To Port

Quanta Computer Inc.			
PROJECT : ZR9			
Size	Document Number		Rev
	DVI (PS8101)		1A
Date: Thursday, May 06, 2010		Sheet 24 of 47	

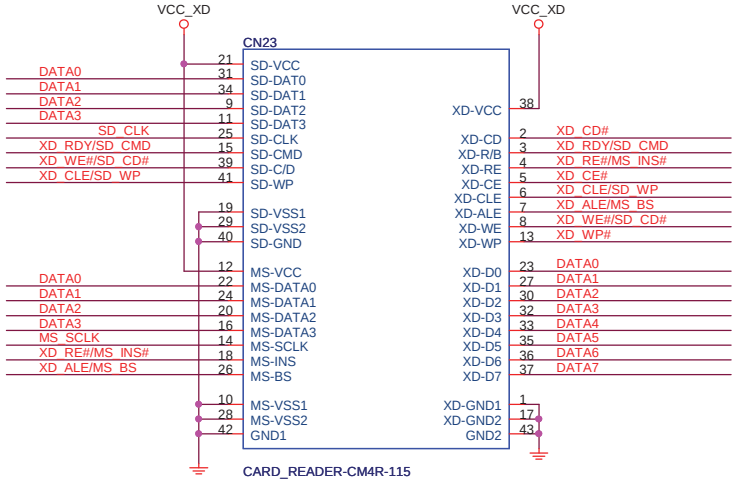
Replicat

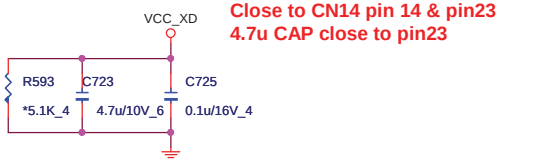
CARD READER Controller



Main	DFHD36MS006
Second	DFHD36MS012

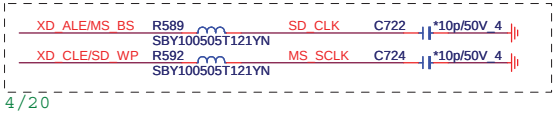
4 IN 1 CARD READER (MMC)





Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

Close to connector



4/20
R589,R592 need to mount the bead SBY100505T121YN (CX05T121000) for EMI .

Quanta Computer Inc.
PROJECT : ZR9

Size	Document Number	Rev
	AU6437 CardReader	1A
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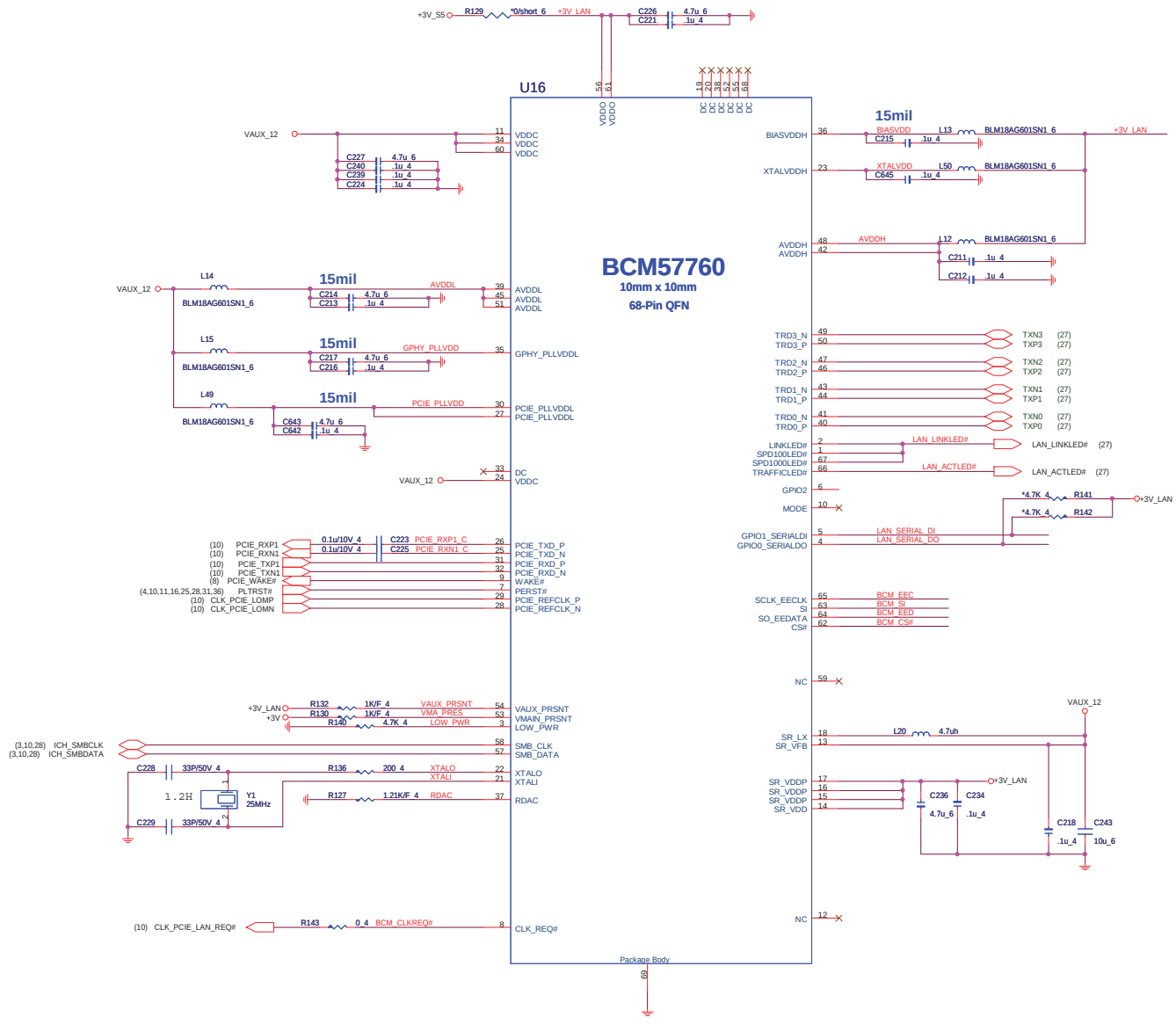
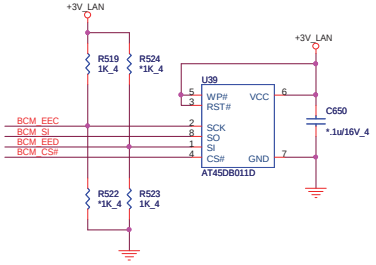
Giga-LAN BCM57760(LAN)



Flash (1M) for ASF2.0



Quanta Computer Inc.			
PROJECT : ZR9			
Size	Document Number		Rev
	LAN (BCM577760)		1A
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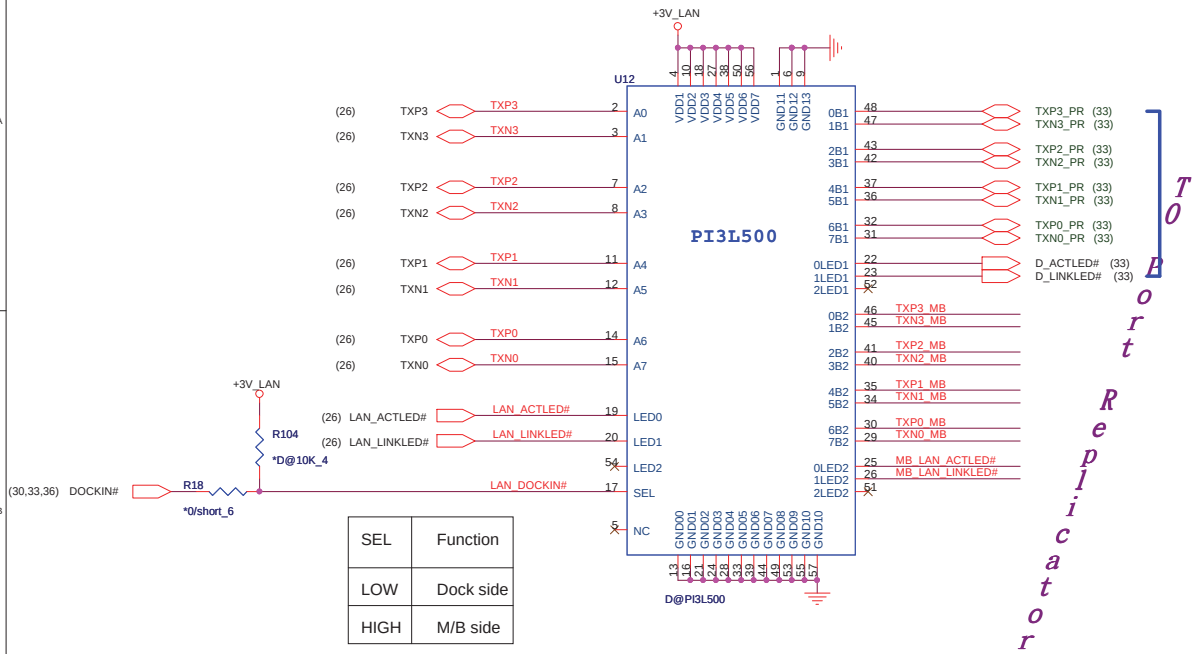
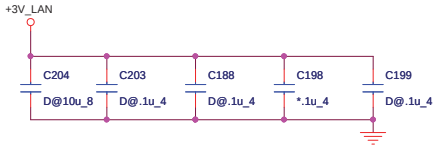
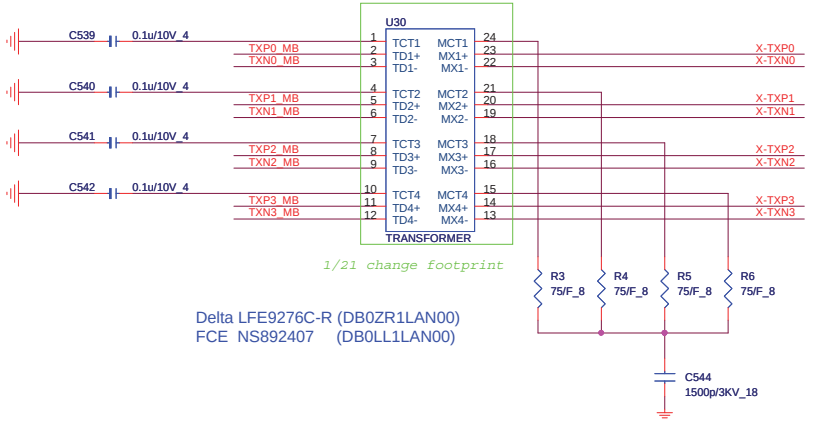
LAN SWITCH



SEL	Function
LOW	Dock side
HIGH	M/B side

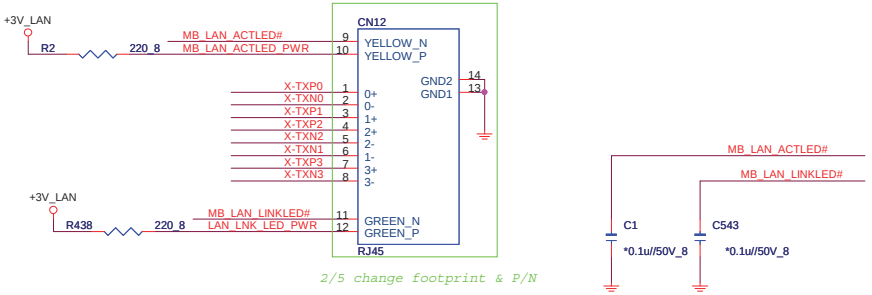


TRANSFORMER



Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)

RJ45(LAN)



Quanta Computer Inc.
PROJECT : ZR9

Size	Document Number	Rev
	LAN SWITCH/TRANSFORMER/RJ45	1A
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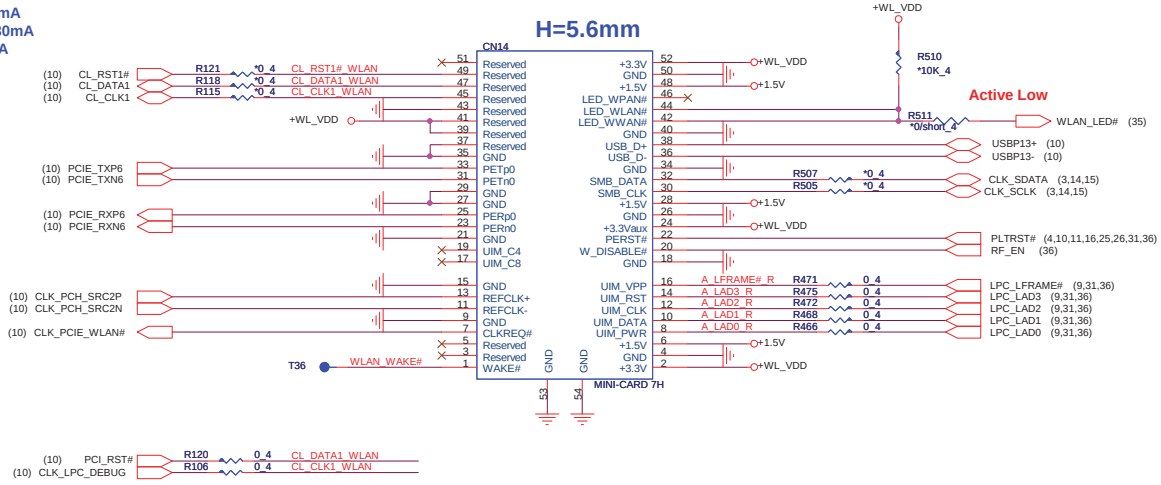
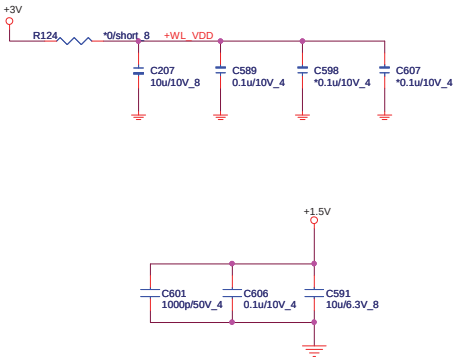
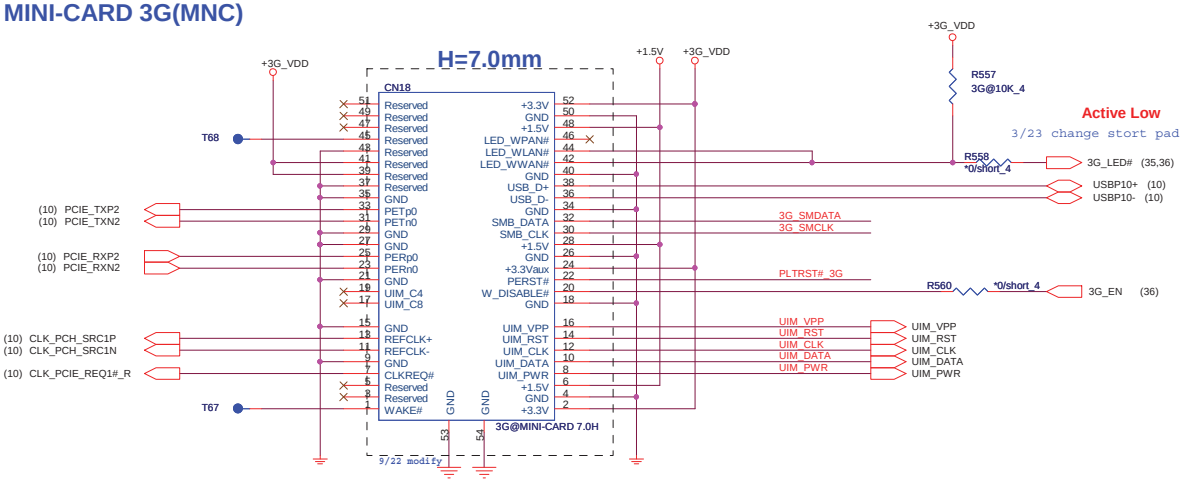
MINI-CARD WLAN(MPC)

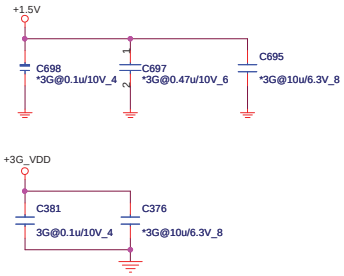
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

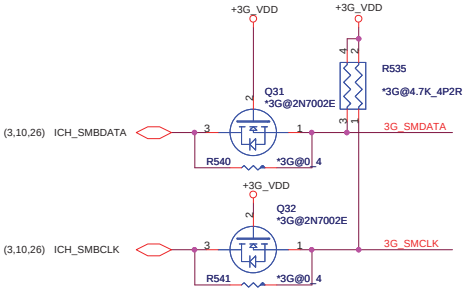


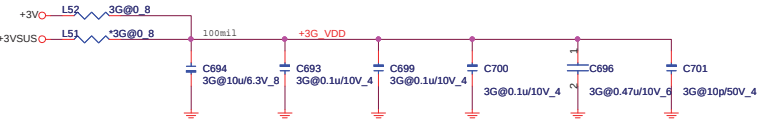


MINI-CARD 3G(MNC)



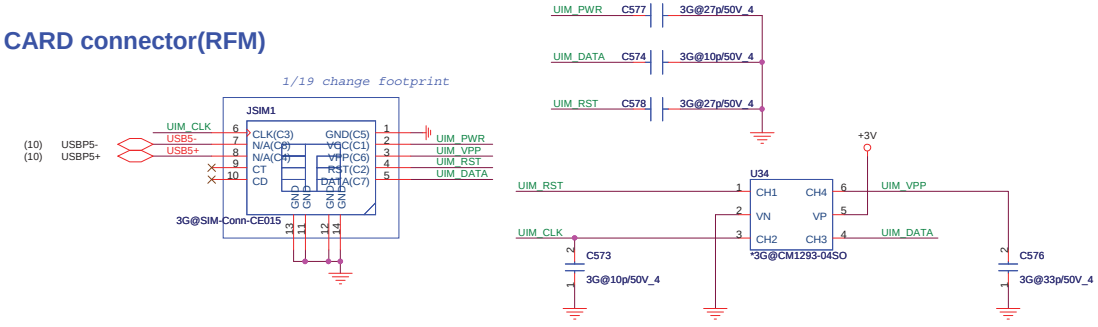


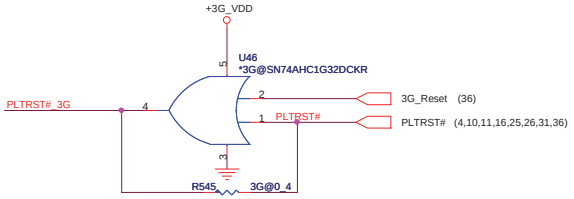




A:(10/17)FAE confirm:
3G module need +3VSUS and no need +1.5V and no need SMBUS

SIM CARD connector(RFM)

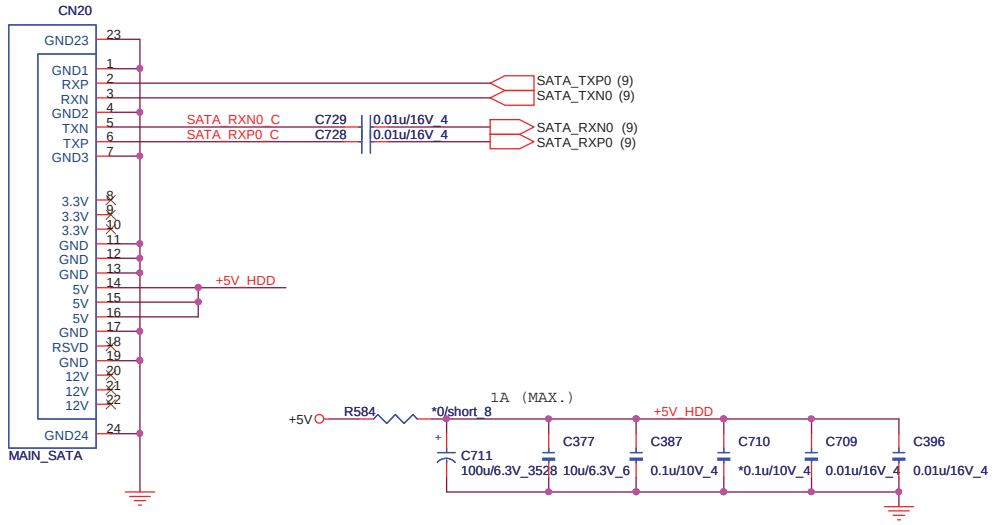




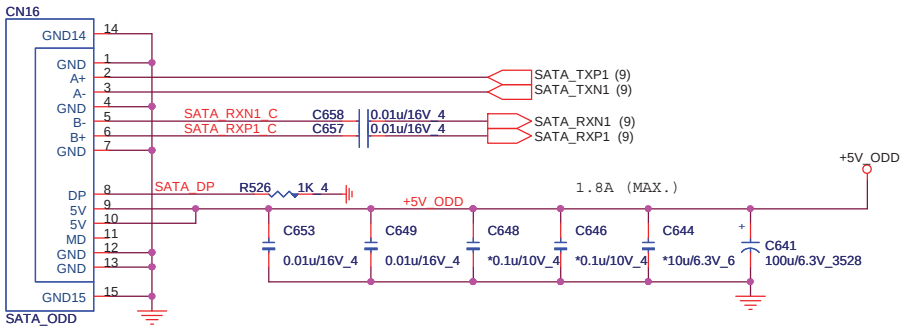
Quanta Computer Inc.
PROJECT : ZR9

Size	Document Number	Rev
	Mini-Card/WL/3G/SIM	1A
Date: Thursday, May 06, 2010	Sheet 28 of 47	

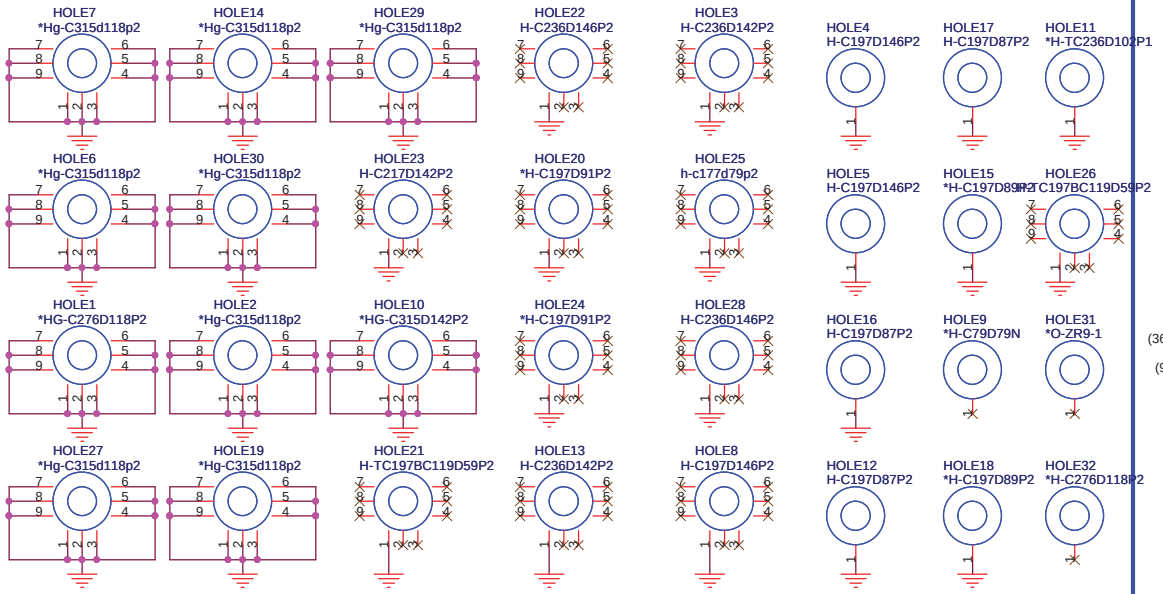
SATA HDD(HDD)



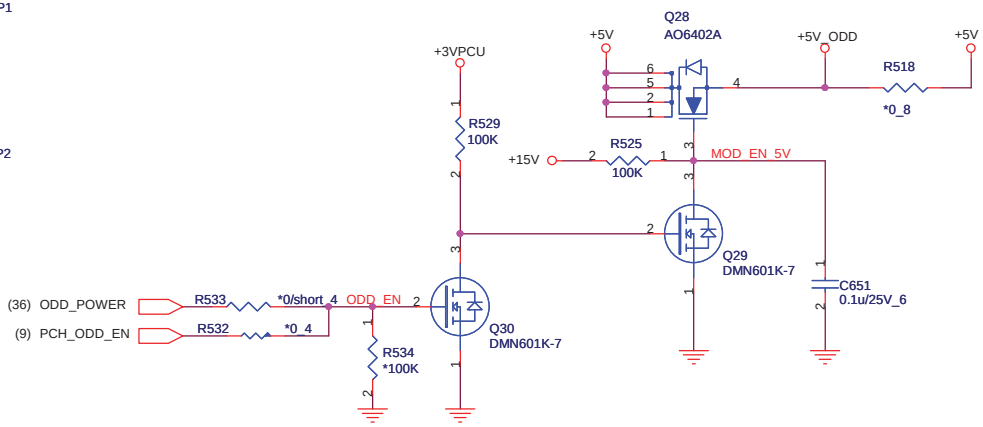
SATA ODD (ODD)



HOLE(OTH)



ODD POWER(ODD)

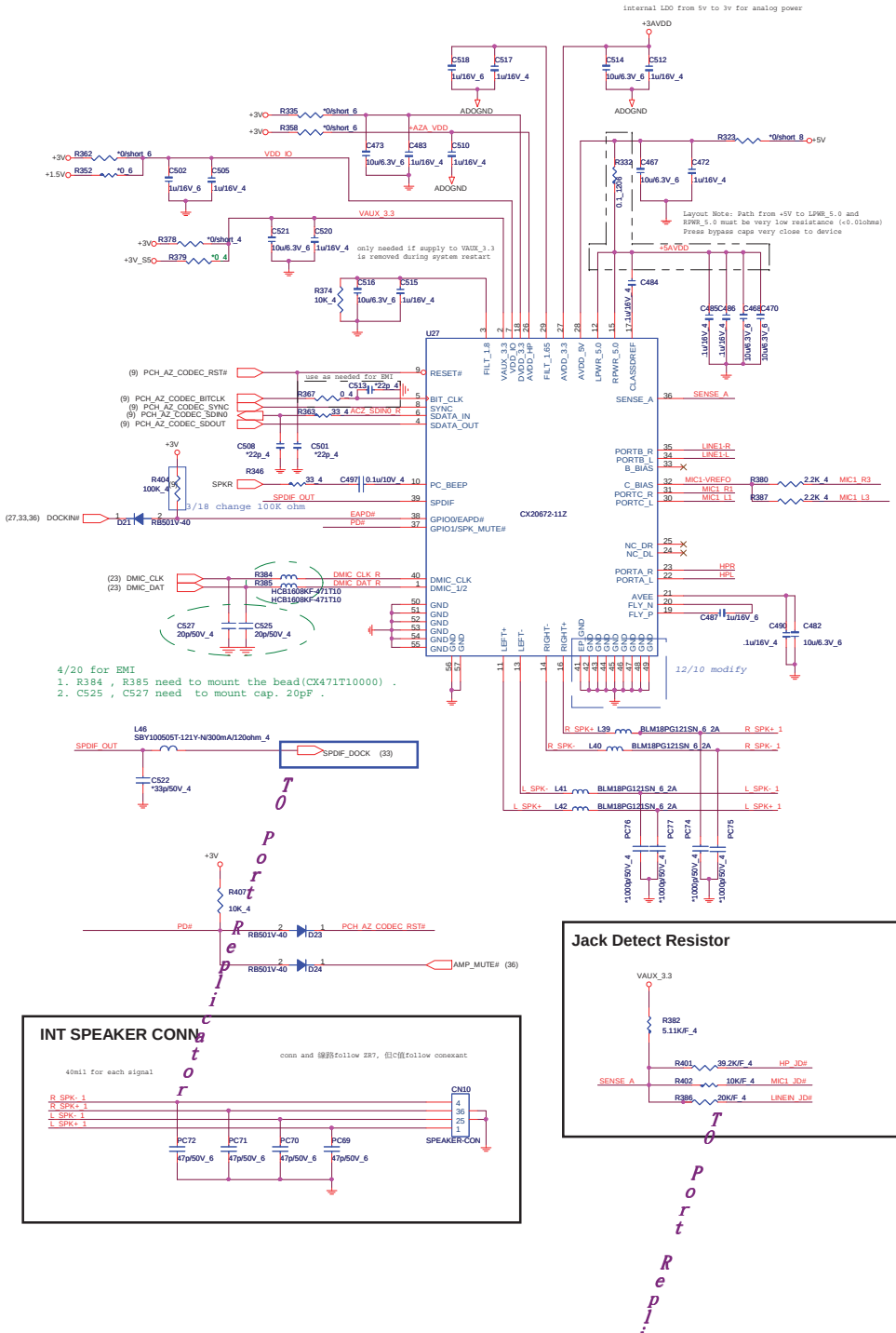


Connect to PCH(GPIO21) pin Y9
and EC pin28(GPIO53)

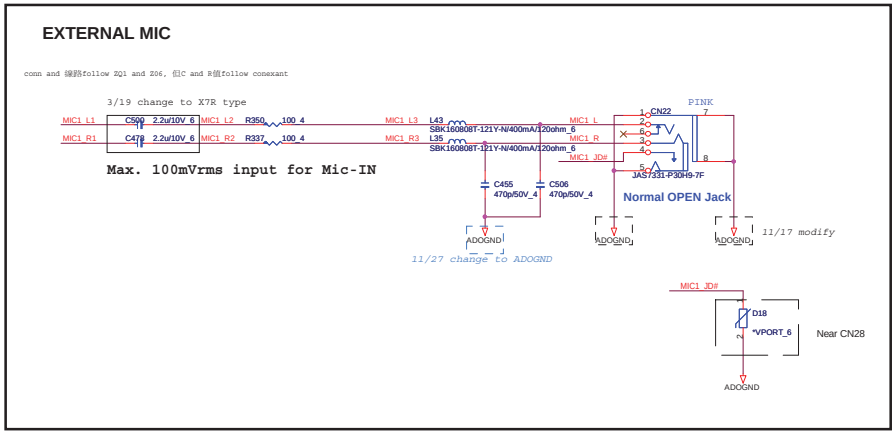
Quanta Computer Inc.

PROJECT : ZR9

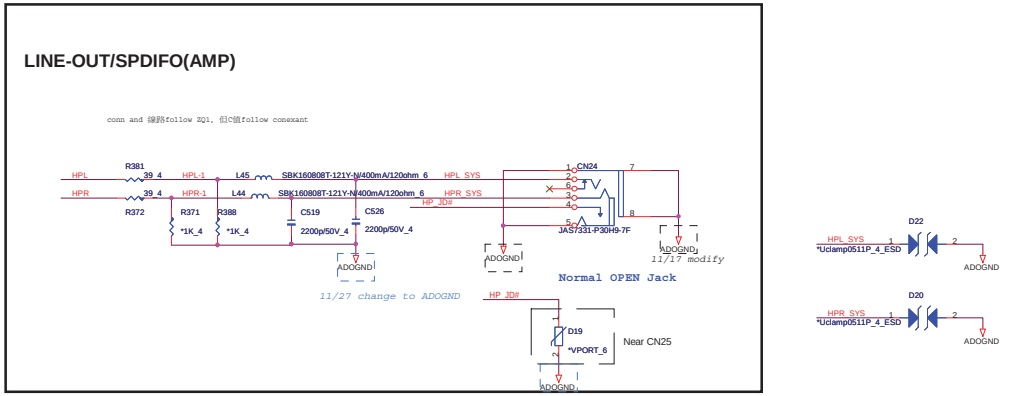
Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A
Date: Thursday, May 06, 2010	Sheet 29 of 47	



EXTERNAL MIC

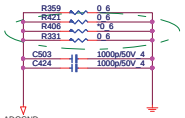


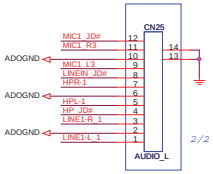
LINE-OUT/SPDIFO(AMP)



INT SPEAKER CONN

Jack Detect Resistor





4/20 EMI suggested that R421 , R331 need to be mounted .

Quanta Computer Inc.			
PROJECT : ZR9			
Size	Document Number	CX20672-11Z/MIC/HP/SPK	Rev 1A
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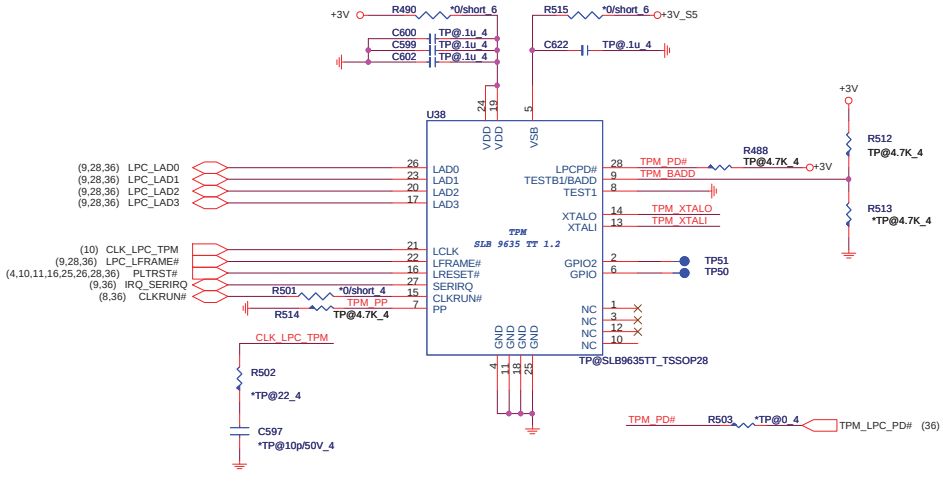
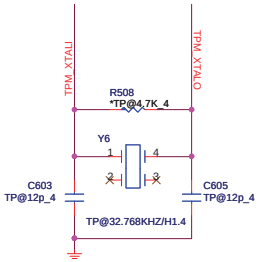
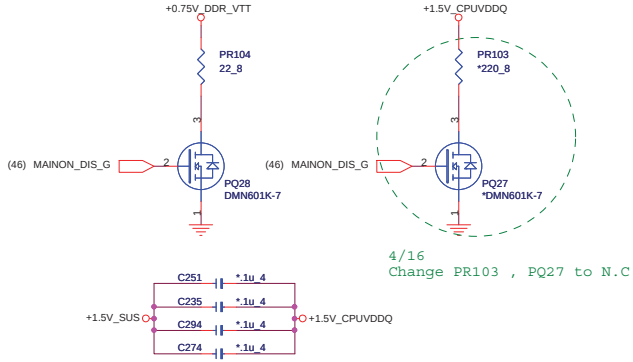
Trust Platform Module(Reserved)

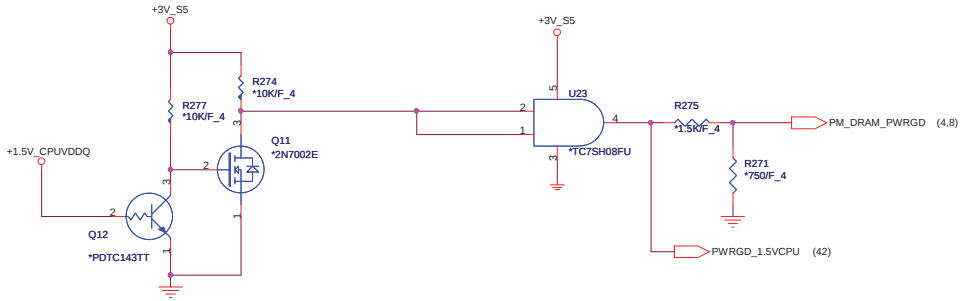
	Resiger Base Address
BADD=0	2E / 2F
BADD=1 (default)	4E / 4F

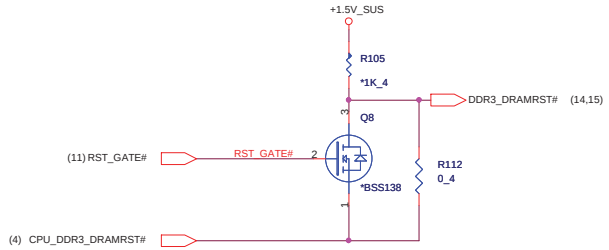


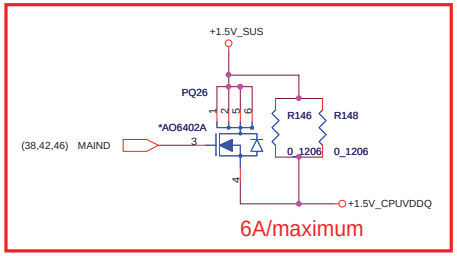




4/16
Change PR103 , PQ27 to N.C



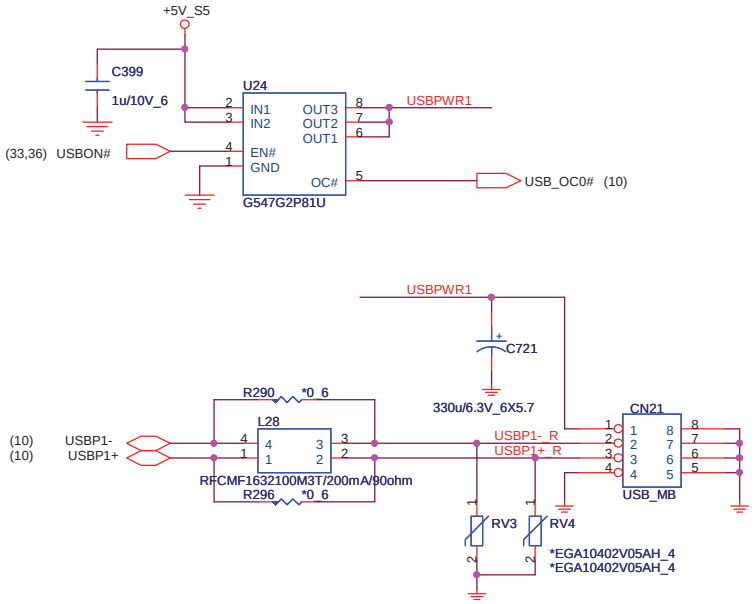




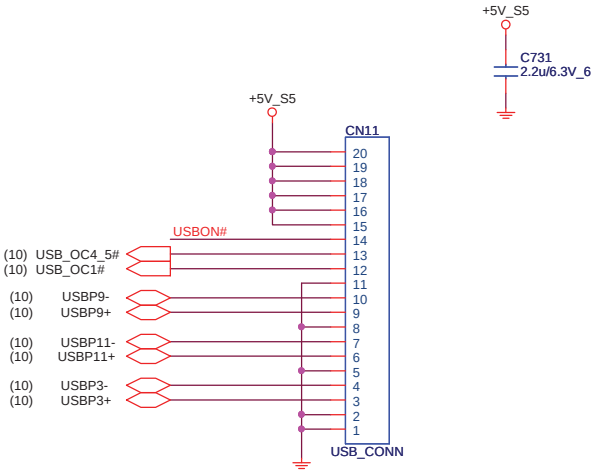
Quanta Computer Inc.
PROJECT : ZR9

Size	Document Number	Rev
	TPM/ S3 POWER SAVING	1A
Date: Thursday, May 06, 2010	Sheet 31 of 47	

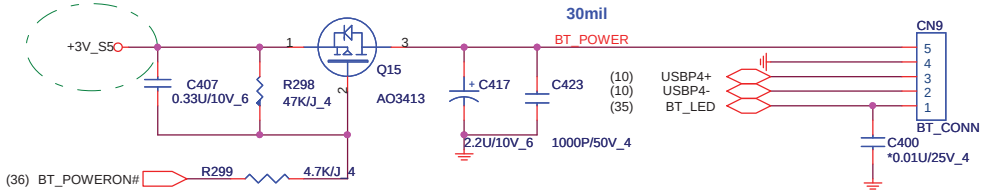
USB PORT(USB)



USB BOARD CONN(USB)



BLUETOOTH CONNECTOR



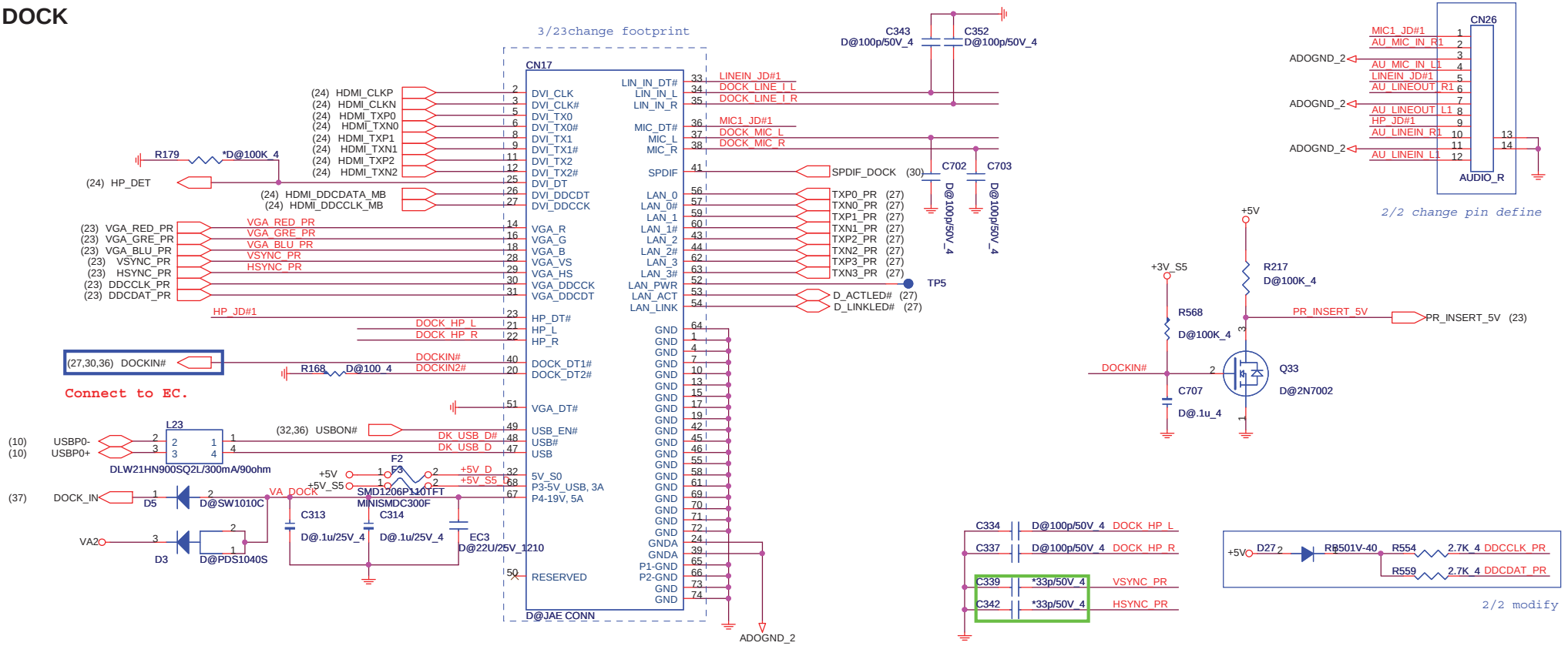
4/16 modify power from +3V to +3V_S5

Quanta Computer Inc.

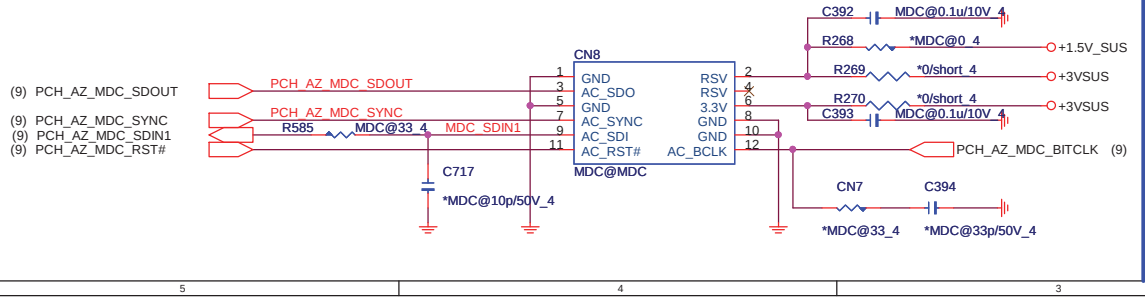
PROJECT : ZR9

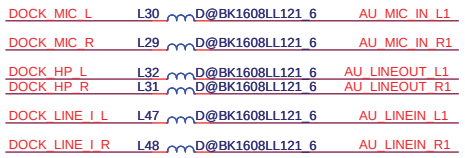
Size	Document Number	Rev
	BT/USB/USB DB	1A
Date: Wednesday, May 05, 2010	Sheet 32 of 47	

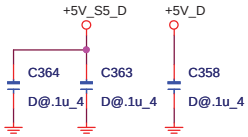
CABLE DOCK



MDC(MDM)







Quanta Computer Inc.		
PROJECT : ZR9		
Size	Document Number: Docking / MDC	Rev 1A
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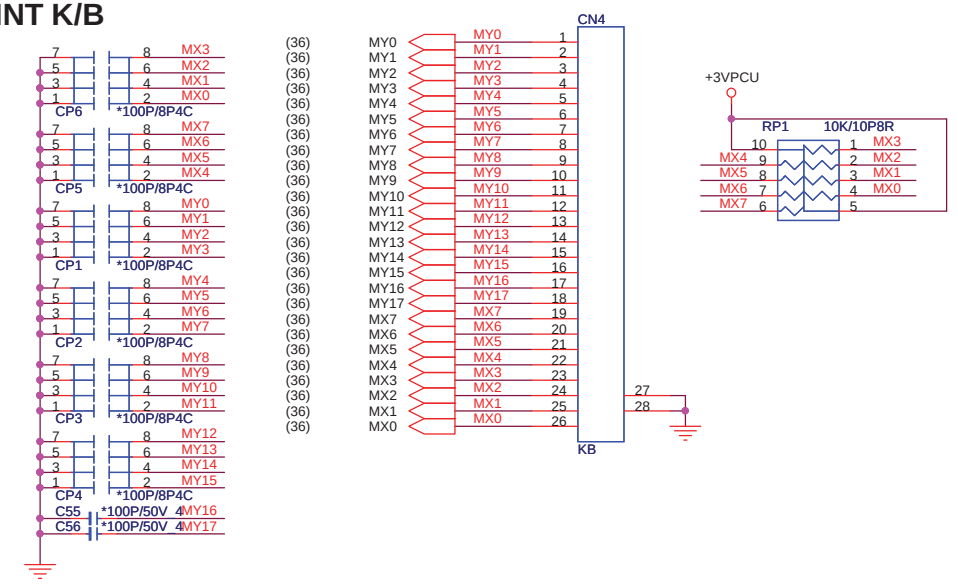
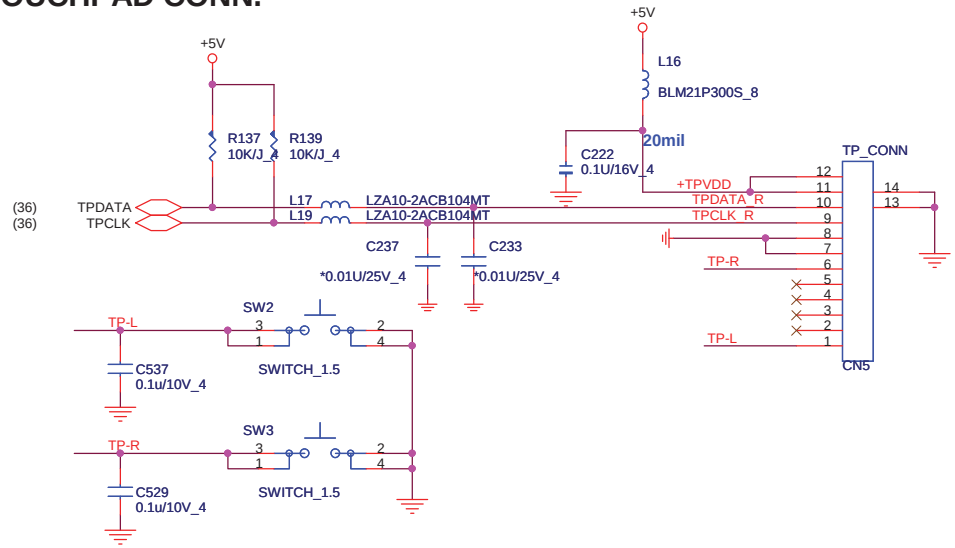
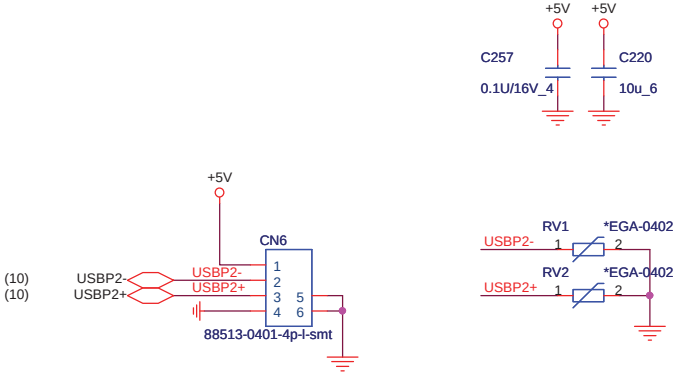
INT K/B



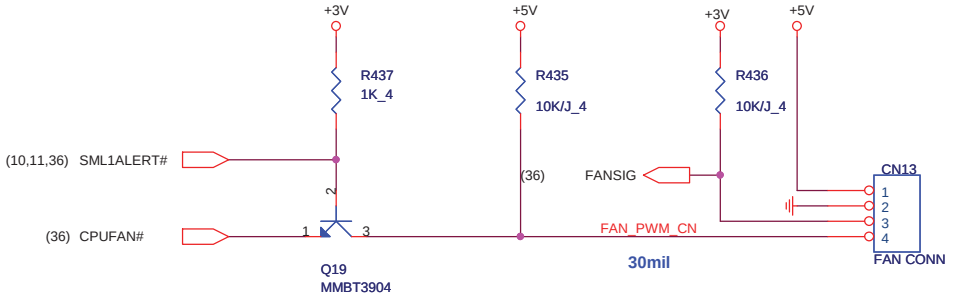
TOUCHPAD CONN.



Finger-Printer CONN.

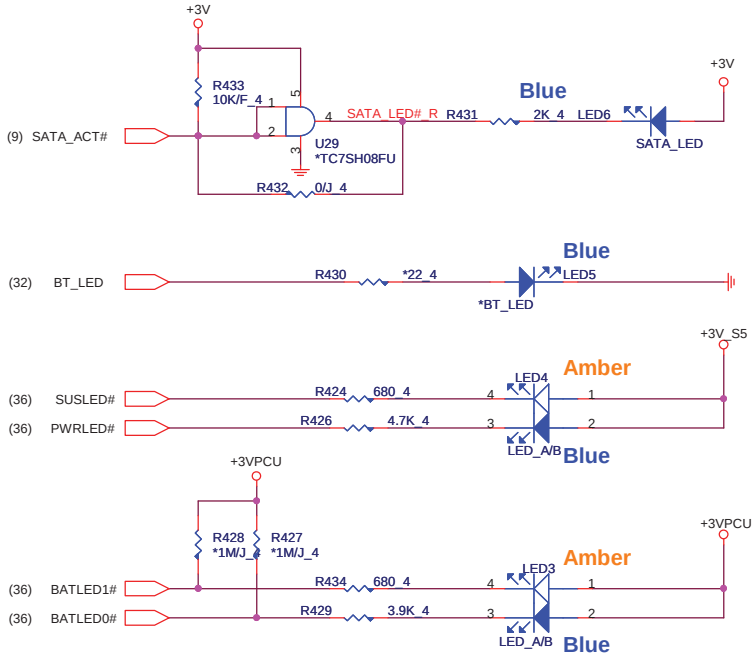


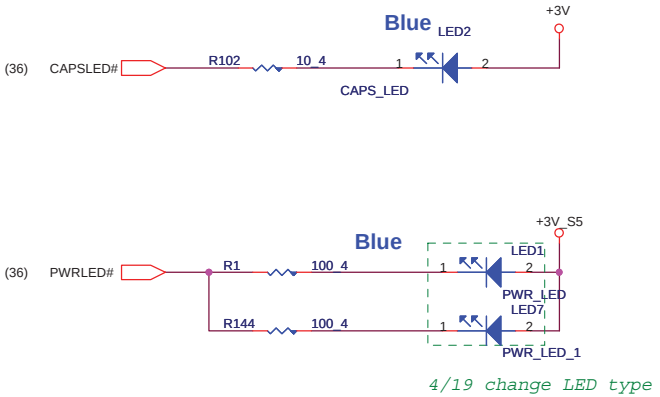
CPU FAN



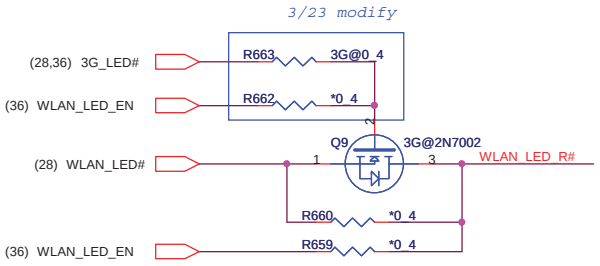
Quanta Computer Inc.		
PROJECT : ZR9		
Size	Document Number: KB/TP+FP/FAN	Rev: 1A
Date: Thursday, May 06, 2010	Sheet 34 of 47	

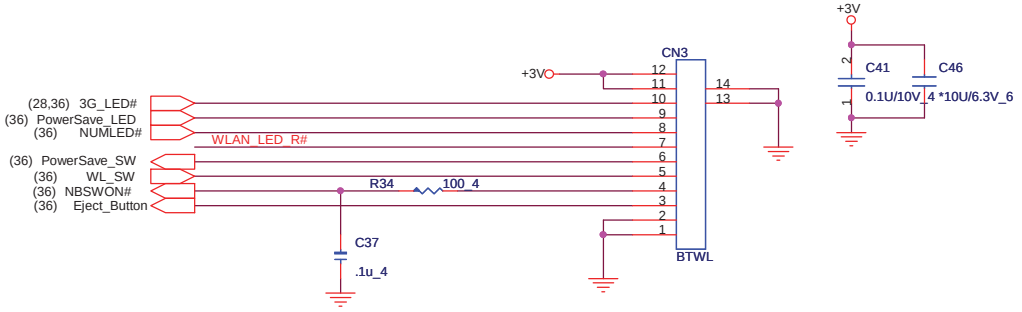
M/B LED





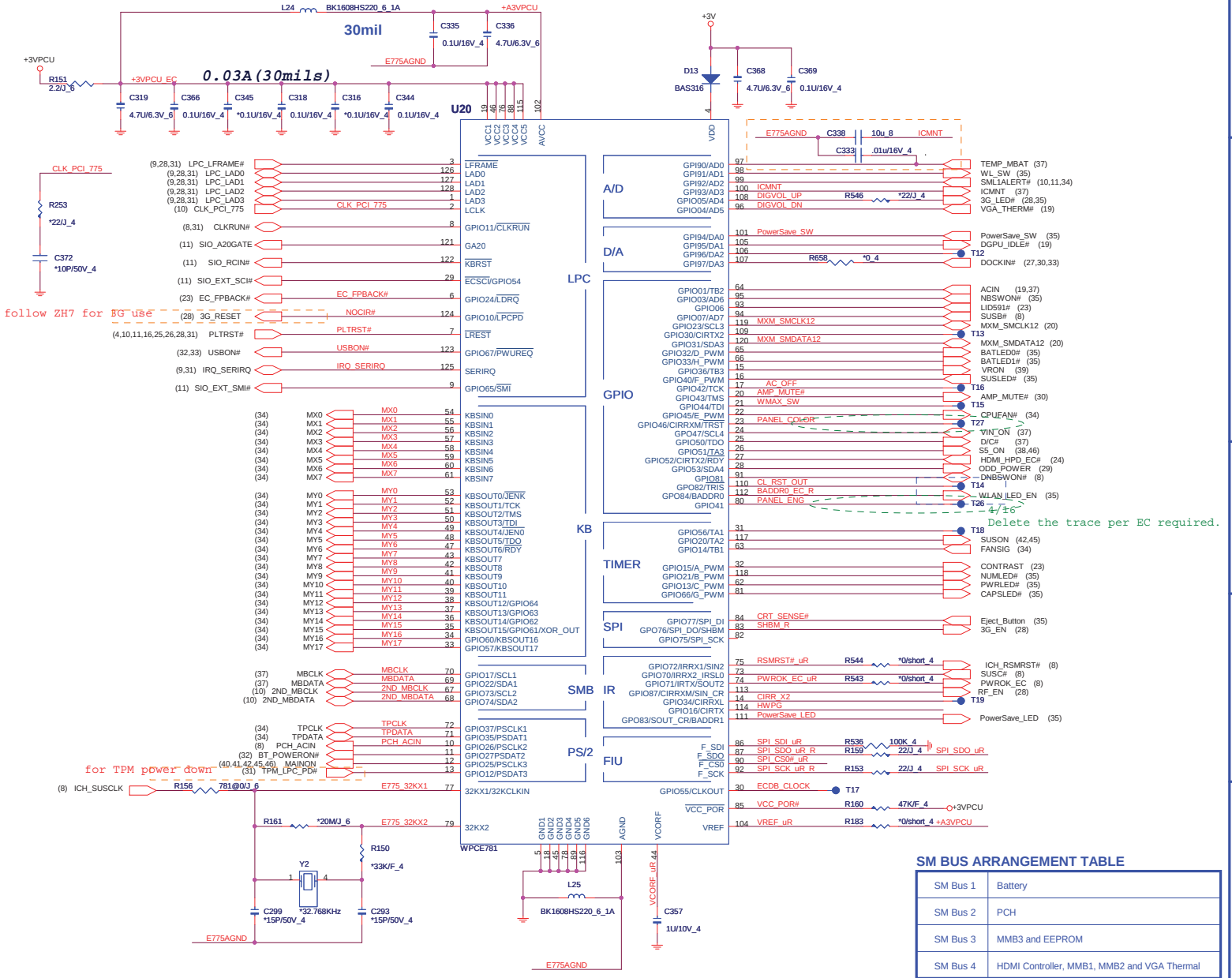
POWER D/B CONNECTOR





Quanta Computer Inc.		
PROJECT : ZR9		
Size	Document Number: POWER/DB/LED	Rev: 1A
Date: Thursday, May 06, 2010	Sheet 35 of 47	

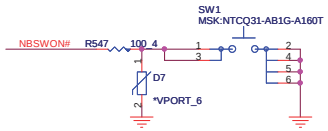
EC



SM BUS ARRANGEMENT TABLE

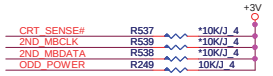
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Thermal

POWER-ON Switch

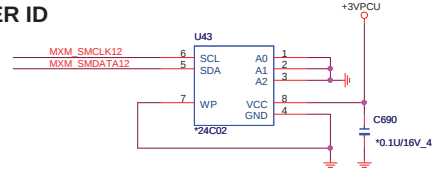


3G_EN

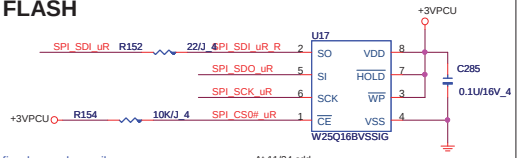
SM BUS PU



ACER ID



SPI FLASH

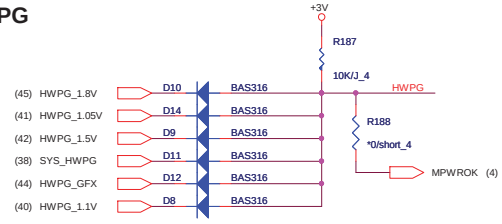


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add

Winbond	W25X16AVSSIG	AKE38ZP0N01
MXIC	MX25L1605AM2C-15G	AKE37FP0Z13
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

HWPG



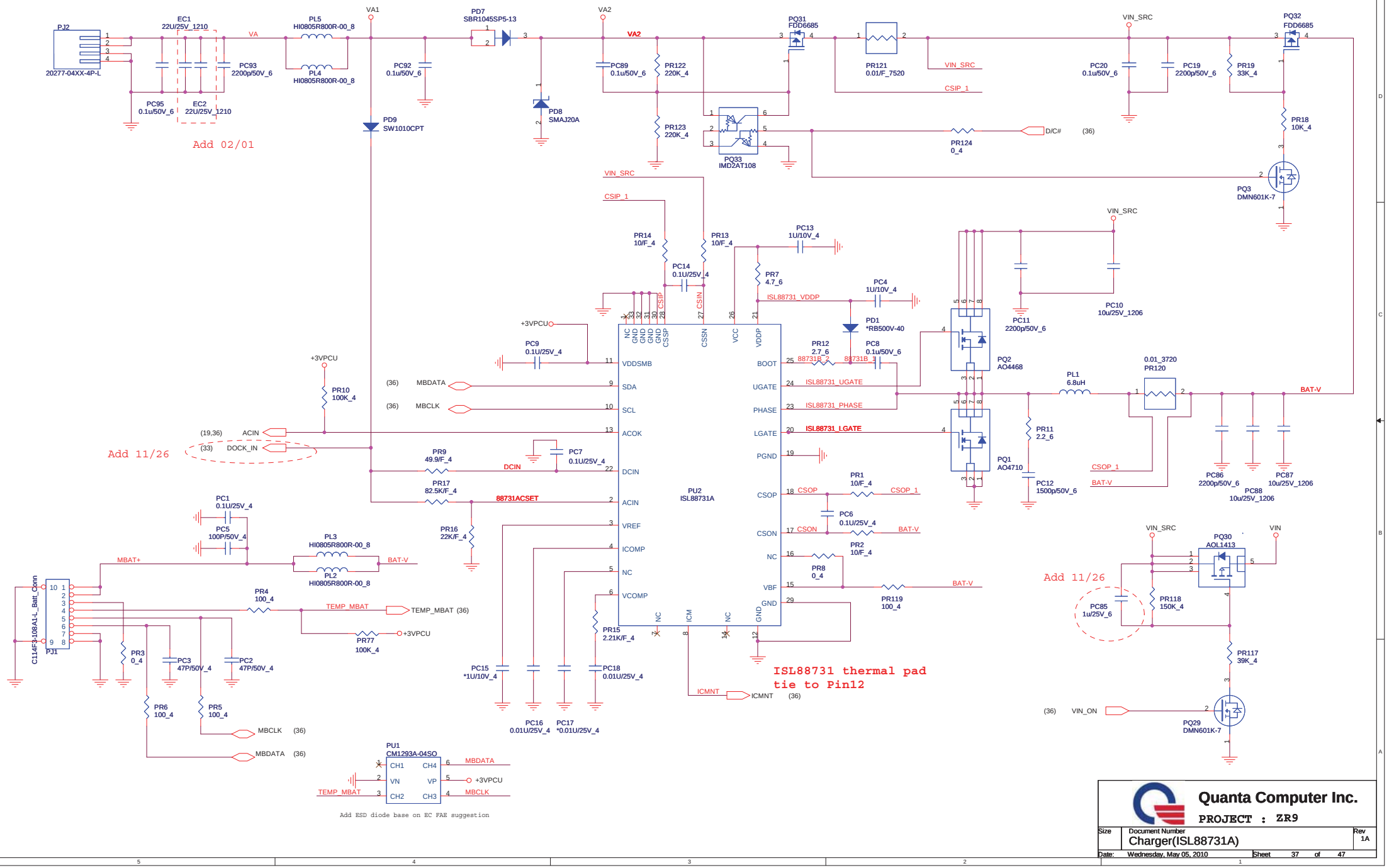
INTERNAL KEYBOARD STRIP SET

Quanta Computer Inc.

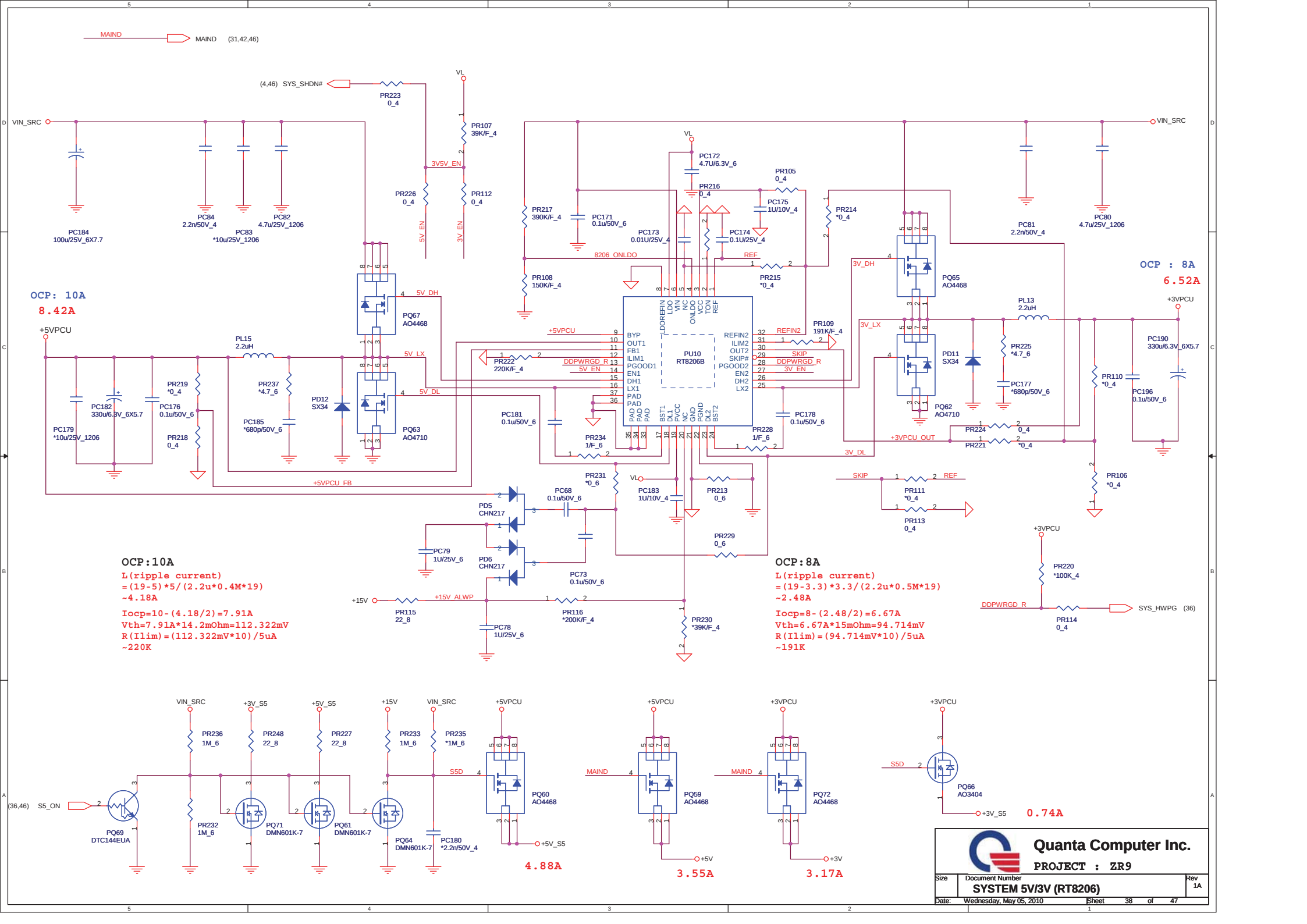
PROJECT : ZR9

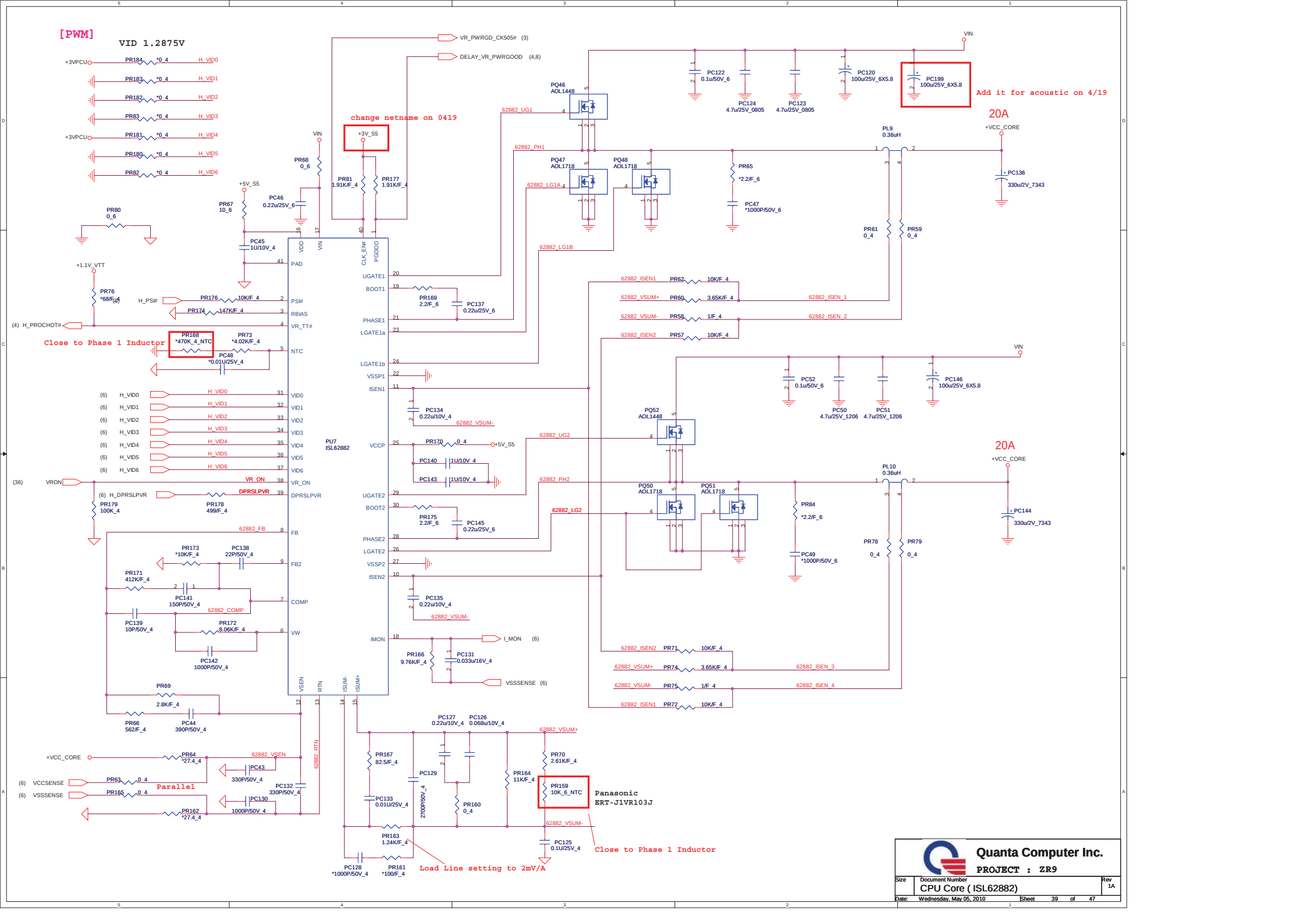
Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

Date: Thursday, May 06, 2010 Sheet 36 of 47

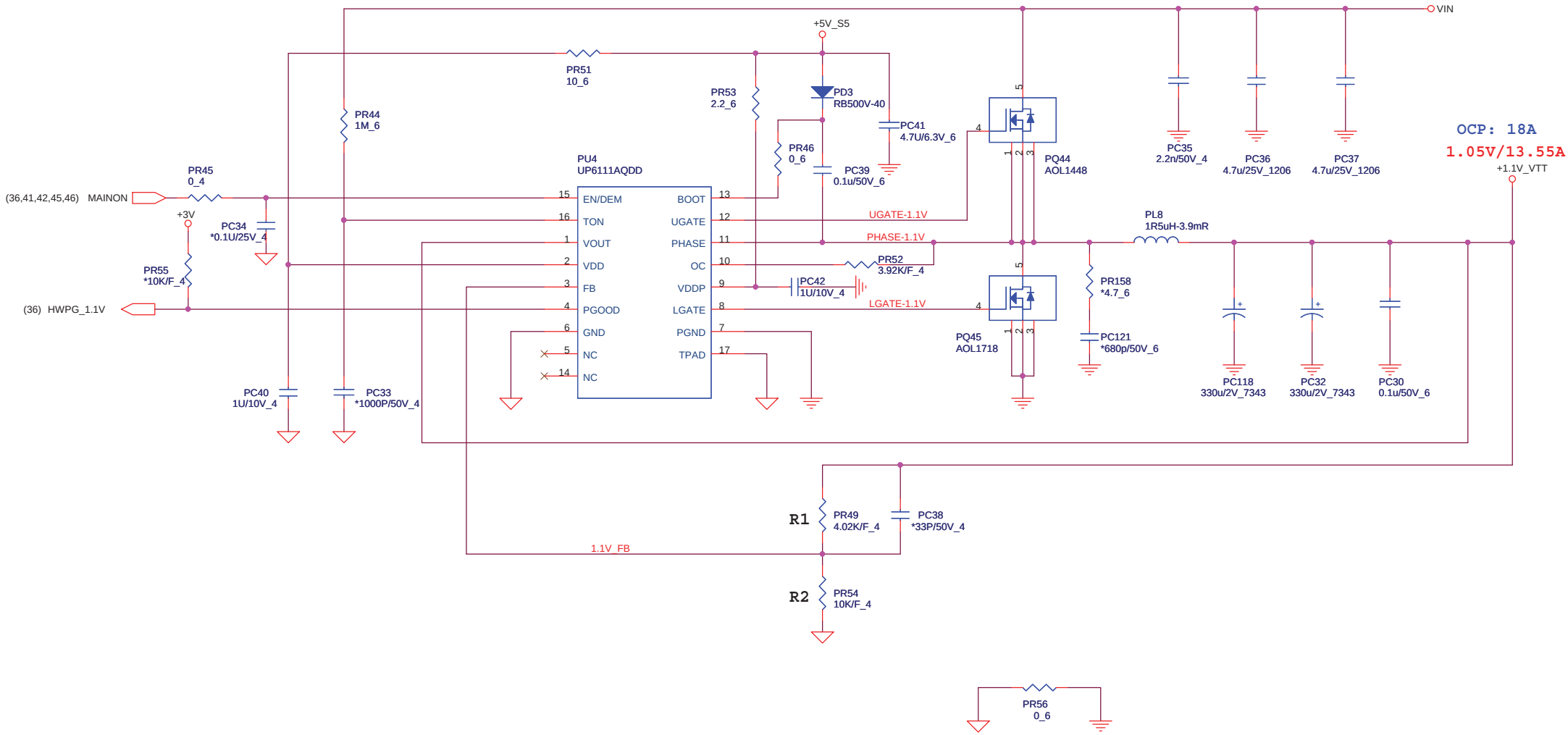


Quanta Computer Inc.		
PROJECT : ZR9		
Size	Document Number: Charger(ISL88731A)	Rev: 1A
Date: Wednesday, May 05, 2010	Sheet 37 of 47	


MAIND
MAIND (31,42,46)
(4,46) SYS_SHDN#
PR223 0_4
VL
VIN_SRC
PR107 39K/F_4
3V5V_EN
PR226 0_4
PR112 0_4
5V_EN
3V_EN
PC184 100u/25V_6X7.7
PC84 2.2n/50V_4
PC83 *10u/25V_1206
PC82 4.7u/25V_1206
PC81 2.2n/50V_4
PC80 4.7u/25V_1206
PR217 390K/F_4
PC171 0.1u/50V_6
PC172 4.7U/6.3V_6
PR216 0_4
PR105 0_4
PC175 1U/10V_4
PC173 0.01U/25V_4
PC174 0.1U/25V_4
8206_ONLDO
REF
PR108 150K/F_4
PR215 *0_4
PR214 *0_4
OCP : 8A
6.52A
OCP: 10A
8.42A
PQ67 AO4468
5V_DH
5V_LX
5V_DL
PQ63 AO4710
PQ65 AO4468
3V_DH
3V_LX
3V_DL
PQ62 AO4710
PD11 SX34
PD12 SX34
+5VPCU
PL15 2.2uH
PL13 2.2uH
+3VPCU
PR222 220K/F_4
DDPWRGD_R
5V_EN
PU10 RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
DL1
PVCC
NC
GND
PSV
DL2
BST2
PR109 191K/F_4
SKIP
3V_EN
PR219 *0_4
PR218 0_4
PR237 *4.7_6
PR225 *4.7_6
PC177 *680p/50V_6
PC182 330u/6.3V_6X5.7
PC176 0.1u/50V_6
PC179 *10u/25V_1206
PC185 *680p/50V_6
PC181 0.1u/50V_6
PC178 0.1u/50V_6
PC190 330u/6.3V_6X5.7
PC196 0.1u/50V_6
PR110 *0_4
PR106 *0_4
PR234 1/F_6
PR228 1/F_6
PR224 0_4
PR221 *0_4
+3VPCU_OUT
+5VPCU_FB
PR231 *0_6
PC68 0.1u/50V_6
PC183 1U/10V_4
PR213 0_6
PR111 *0_4
PR113 0_4
PD5 CHN217
PD6 CHN217
PC79 1U/25V_6
PC73 0.1u/50V_6
PR229 0_6
PR220 *100K_4
PR114 0_4
SYS_HWPG (36)
+15V
+15V_ALWP
PR115 22_8
PR116 *200K/F_4
PC78 1U/25V_6
PR230 *39K/F_4
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
VIN_SRC
+3V_S5
+5V_S5
+15V
PR236 1M_6
PR248 22_8
PR227 22_8
PR233 1M_6
PR235 *1M_6
S5D
(36,46) S5_ON
PQ69 DTC144EUA
PR232 1M_6
PQ71 DMN601K-7
PQ61 DMN601K-7
PQ64 DMN601K-7
PC180 *2.2n/50V_4
PQ60 AO4468
+5V_S5
4.88A
MAIND
PQ59 AO4468
+5V
3.55A
PQ72 AO4468
+3V
3.17A
PQ66 AO3404
+3V_S5
0.74A
Quanta Computer Inc.
PROJECT : ZR9
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
Date: Wednesday, May 05, 2010
Sheet 38 of 47


[PWM]
VID 1.2875V
change netname on 0419
Add it for acoustic on 4/19
20A
Close to Phase 1 Inductor
Parallel
Panasonic
ERT-J1VR103J
Load Line setting to 2mV/A
Close to Phase 1 Inductor
PU7
ISL62882
Quanta Computer Inc.
PROJECT : ZR9
CPU Core (ISL62882)
Wednesday, May 05, 2010

[PWM]



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

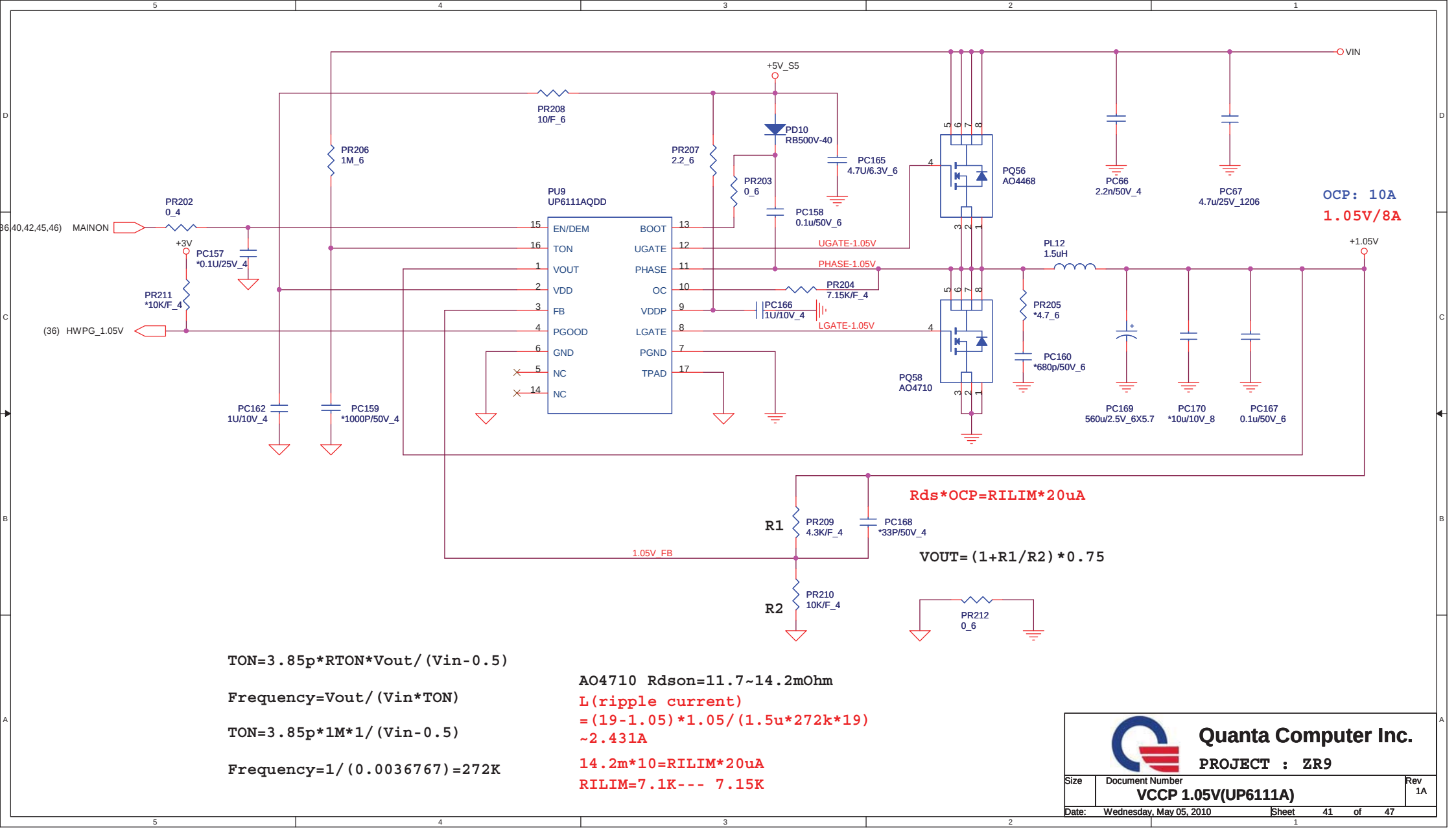
Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K

Quanta Computer Inc.		
PROJECT : ZR9		
Size	Document Number: +VTT (UP6111A)	Rev: 1A
Date: Wednesday, May 05, 2010	Sheet 40 of 47	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

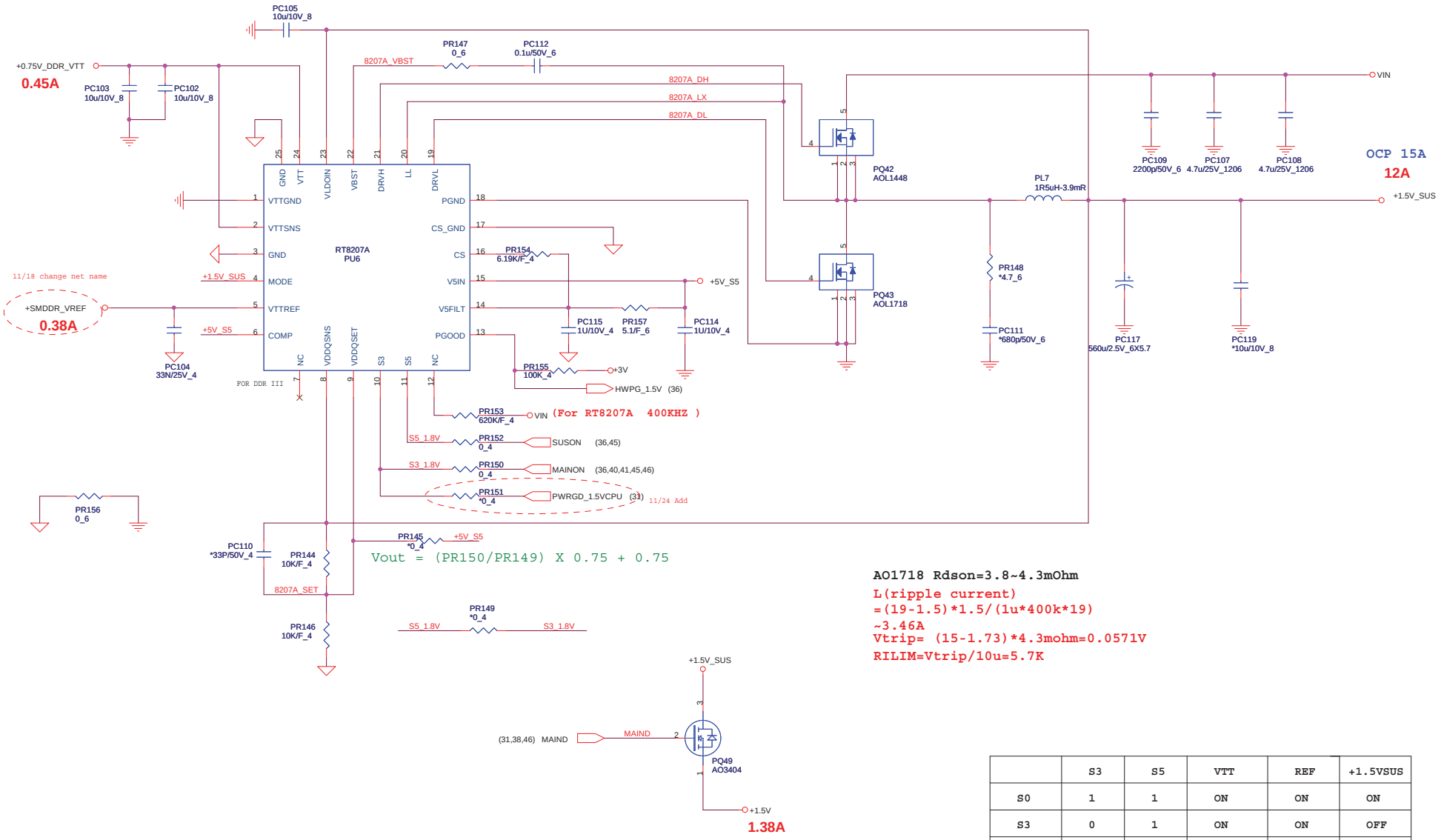
L(ripple current)
=(19-1.05)*1.05/(1.5u*272k*19)
~2.431A

14.2m*10=RILIM*20uA

RILIM=7.1K--- 7.15K

Quanta Computer Inc.		
PROJECT : ZR9		
Size	Document Number: VCCP 1.05V(UP6111A)	Rev: 1A
Date: Wednesday, May 05, 2010	Sheet 41 of 47	

[PWM]



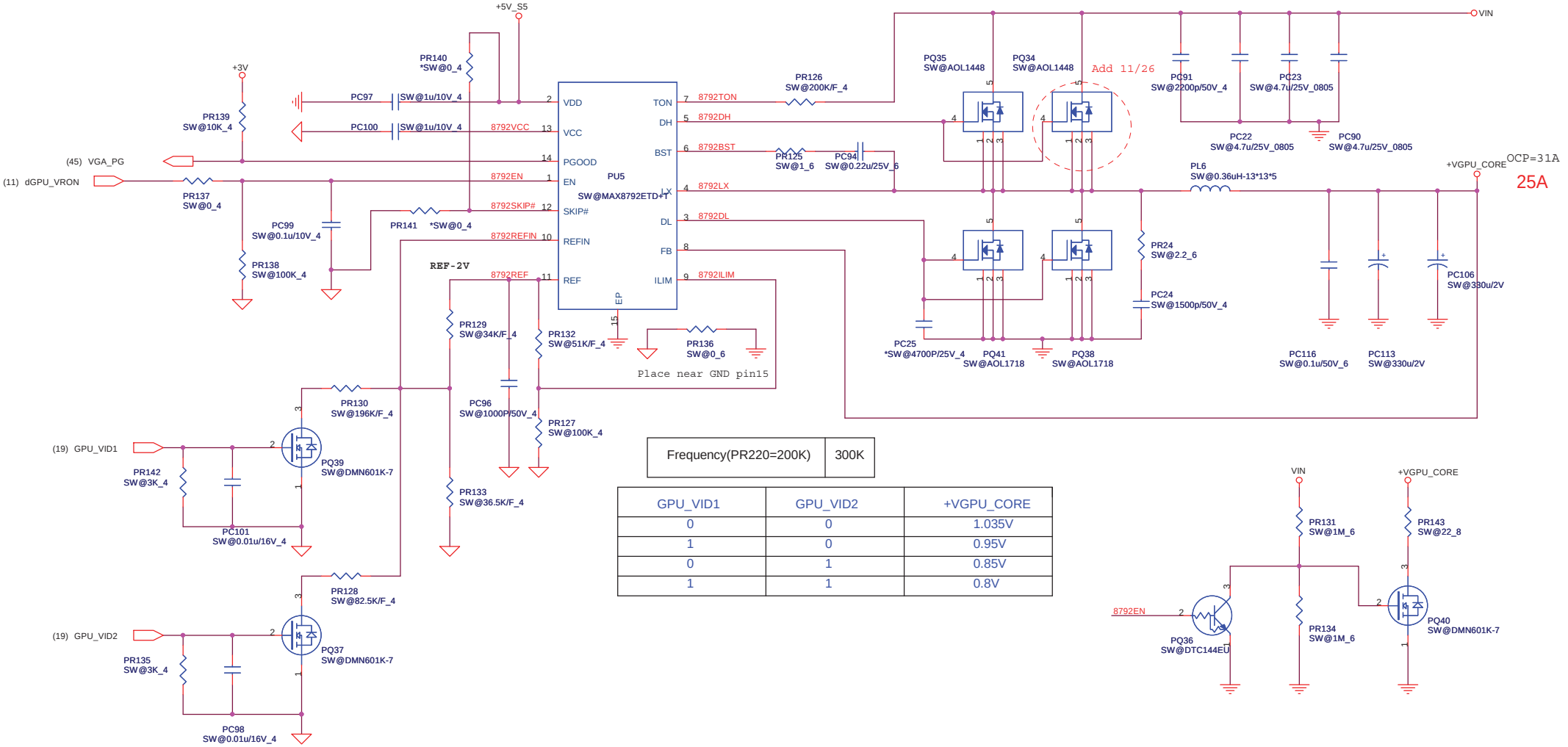
AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.46A
Vtrip= (15-1.73)*4.3mohm=0.0571V
RILIM=Vtrip/10u=5.7K

	S3	S5	VTT	REF	+1.5VSUS
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZR9

Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

Date: Wednesday, May 05, 2010 Sheet 42 of 47



Frequency(PR220=200K)	300K

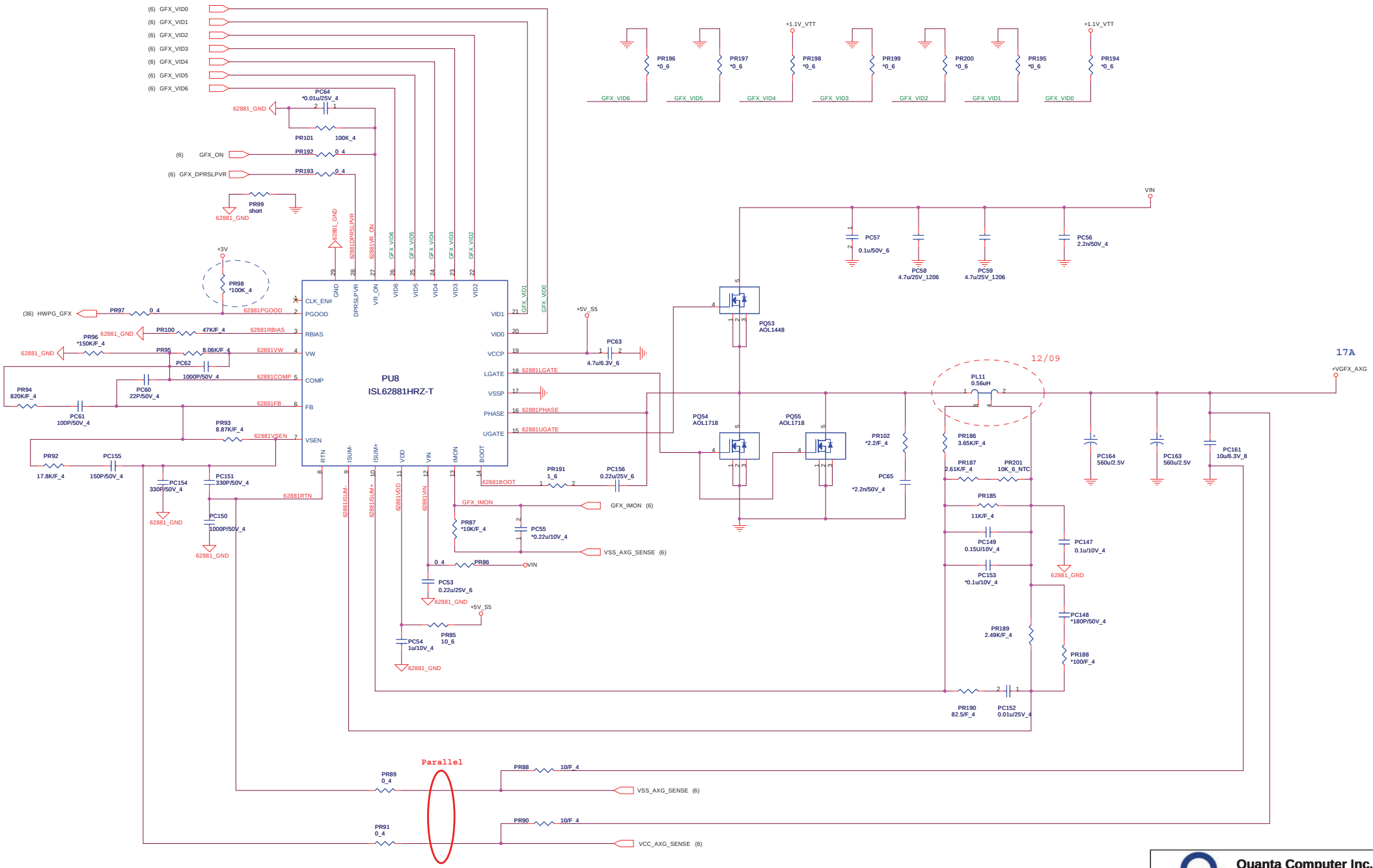
GPU_VID1	GPU_VID2	+VGPU_CORE
0	0	1.035V
1	0	0.95V
0	1	0.85V
1	1	0.8V

Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	GPU CORE(MAX8792)	1A
Date: Thursday, April 29, 2010	Sheet 43 of 47	

Int_VGA [PWM]

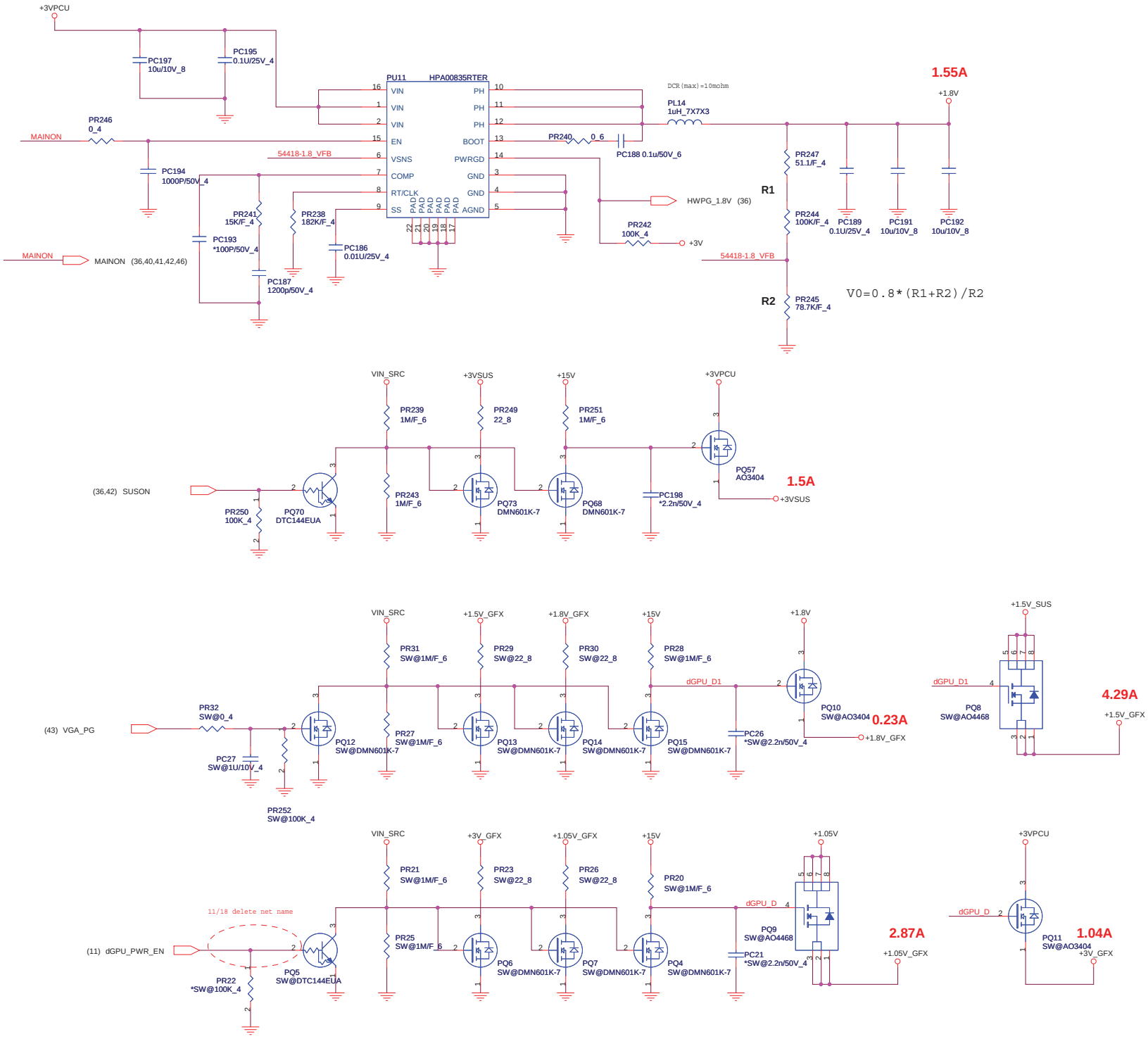


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZR9

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	1A

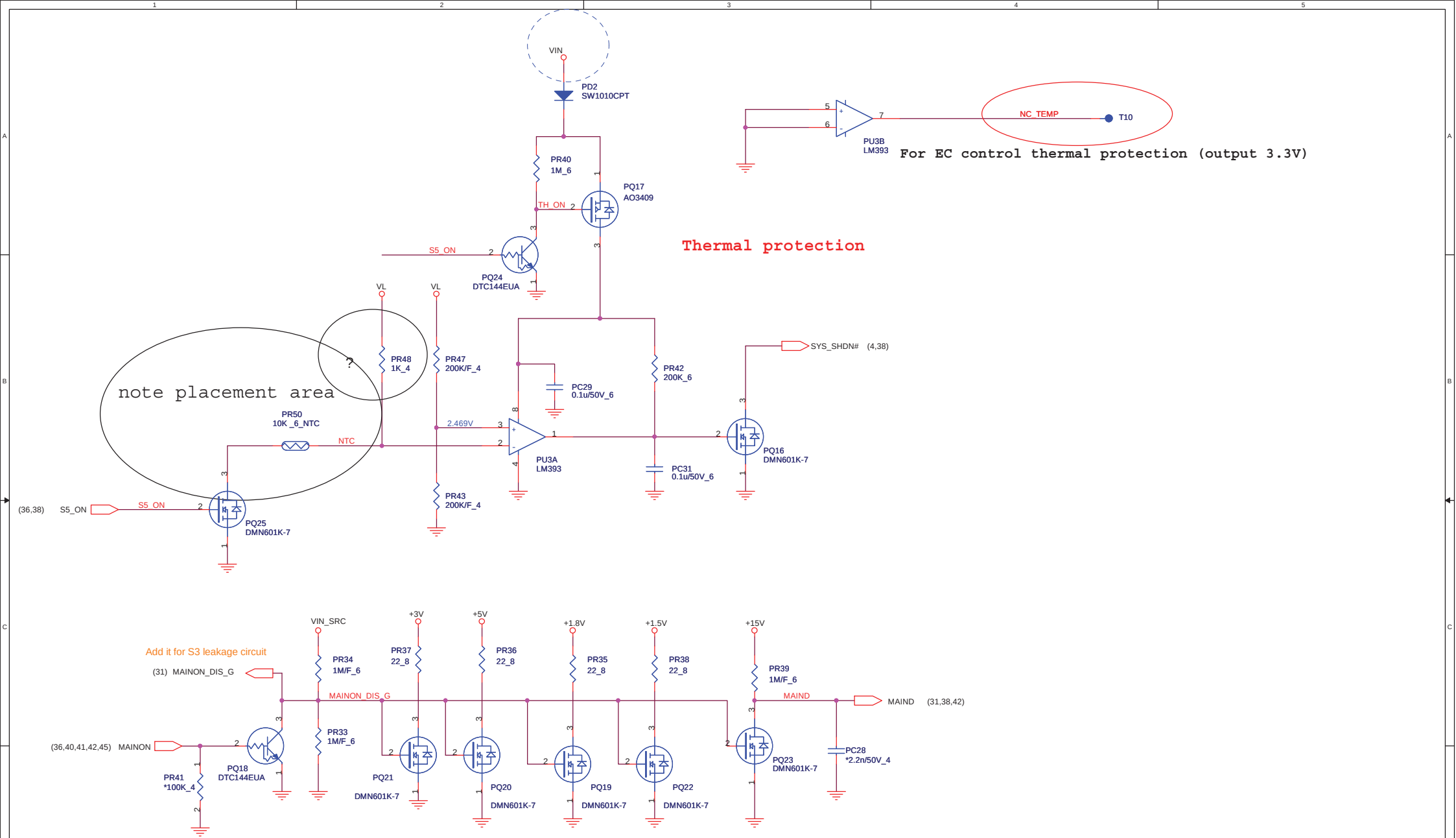
Date: Wednesday, May 05, 2010 Sheet 44 of 47



Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	(GPU_Power/1.8V)	1A
Date: Wednesday, May 05, 2010	Sheet 45 of 47	



Quanta Computer Inc.

PROJECT : ZR9

Size	Document Number	Rev
	Thermal Protection	1A
Date: Wednesday, May 05, 2010	Sheet 46 of 47	

Model	REV	DATE	CHANGE LIST
ZR9	A	20091117	page 10:delete R8345 & add C8407 & modify usb port define --> sim card to port 5 ,docking to port 0
			page 34:modify CN7009 pin define
			page 30:modify speaker out circuit
			Evan Wang update Power circuit
		20091119	page 33 :cn9055 pin.67 change net name DCIN to DOCK_IN
			page 18 Base on Design Guide , DVI should change to port E.
			Evan Wang update Power circuit
			page 4 :add R529,R232,R537,R527,R213,R524,R538,R536,R534,R528,R230
		20091124	page 19 :delete R3515,R3514,Q3500,Q3501
			page 24 :change net name MB_HDMI_DDCDATA ,MB_HDMI_DDCCLK to SDVO_CTRL_DAT, DVO_CTRL_CLK
			page 34 :delete R7451 & change R7442 to 1K , add C8031,C9053
			page 30 :U9001 Pin.26 C12021change PD to AGND & add R13069,R228,R233
		20091125	page 24 :delete R9798,R9810
			page 35 :add LED7005,R7402,R7408 & modify CN7008 Pin define
			page 19 :add R3590 to PU +3V_GPX
		20091126	Evan Wang update Power circuit 1. Add PC9020(1u/25V_6),2. PR9028 changes to 150K_4,3. PR9025 changes to 39K_4,4. Add PQ3008(SW@AOL1448),5.GPU_CORE solution change to MAX8732.
			page 35 :del LED7005,R7402,R7408
			page 14 :JDIM8000 SWAP PIN
			page 15 :JDIM8999 SWAP PIN
			page 21 :U3502,U3509,U3503,U3508 SWAP PIN
		20091127	page 22 :U3504,U3500,U3501,U3507 SWAP PIN
			page 24 :U15 SWAP PIN
			page 27 :U45 SWAP PIN
			page 32 :delete R295,R296,R297,R298,R363,R346,L28,L29,L32
			page 16 :delete C3513,C3500,C3643,C3644,C3501
		20091130	page 21 :delete C557,C559,C7,C560
			page 22 :delete C565,C563,C20,C564
			page 35 :add LED2,R7402 & modify CN7008 Pin define
			page 23 :CN9049 modify pin define & change 6 pin
		20091201	page 32 :CN7008 modify pin define
			page 36 :U7020.14 net name WLN_LED# change to U7020.112 & add net name WL_LED# on U7020.98
			Evan Wang update Power circuit
		20091202	page 6 :del R8237
			page 12:del R8268 & add R8432,R8433
			page 30:del R228
		20091203	page 32:CN11 change Pin define
			page 35:del D13,D7022 & add R13093,R12101
		20091207	page 35:add R7406,LED7001
			page 23:CN9049 change to 8 pin
		20091210	page 35:R7398,R7399,R7400R7402,R7403,R7404,R7405,R7406 chnage to 150 ohm
			page 35:add Q7027
		20091214	page 24:add R9802,R9795
	B	20100106	page 4: change R185 to NC
			page 8: change R395 to un-mount
			page 10: change C715,C714 to 33pf & add R508,R653,R654,R655,R656,R657 & for LAN SMBus form SMB_CLK_ME0,SMB_DATA_ME0 to ICH_SMBCLK,ICH_SMBDATA & change high resistor 4.7k ohm R134,R135 close to chip side
			page 11: chnage dGPU_PWR_EN pin high resistor 1V@ un-mount
			page 18: change C595,C596 to 33pf
			page 23: VGA power add poly switch
		20100125	page 26: LAN SMBus change net name to ICH_SMBCLK,ICH_SMBDATA & C228,C229 to 33pf
			page 28: del net name RF_EN & R559 & R511 un-mount
			page 31: change R508 to NC
			page 33: DOCK power add poly switch & R269,C392 un-mount
			page 35: change Q9 to N type & add R660,R659
			page 36: add R658
			Evan Wang update Power circuit
			page 30: add connector CN25 & change L29 , L30 , L31 , L32 , L47, L48 , C531 , C530 to docking side
		20100127	page 33: add connector CN26
			page 33: CN17 ADOGND change to ADOGND_2
		20100201	Evan Wang update Power circuit
			page 23: add U51
			page 33: CN26 ADOGND change to ADOGND_2
		20100202	page 36: add R547
			page 33: add R554,R559 & D27
			page 33: Docking power add f2,f3
		20100205	page 27: CN12 chnage footprint
	C	20100325	page 12: Add C530 to decrease CRT DAC ripple noise
			page 25: Change R589, R592 to bead for EMI require
			page 30: C478, C500 change from Y5V to X7R for MIC THD+N quality
			page 30: R404 pull hgh R to 100k for docking insert detect
			page 35: Change POWLED# power to +3V_S5 to prevent when EC go into power saving, Power LED will turn on in battery only.
			page 35: Modify 3G/WIFI LED turn on behavior.
	Ramp	20100416	page 32 : Modify B/T power from +3V to +3V_S5
			page 23 , 1. Change L1 to 0805 size 2. Change R12 , R13 from 0603 to 0402
			page 31 : Change PR103 , PQ27 to N.C
			page 23 , 36 : Delete PANEL_COLOR and PANEL_ENG per EC required.
			page 41 : PR209 changes to 4.3K/F_4(CS243022PB07)
			page 37 : Mount PR11 and changes to 2.2_6(CS-2203F911)
			page 37 : Mount PC12 and changes to 1500p/50V_6(CH21506K915)
			page 43 : PR24 changes to SW@2.2_6(CS-2203F911)
			page 43 : PC24 changes to SW@1500p/50V_4(CH21506KB14)
			page 35 : Change BXP power LED size from 0805 to 0603 and the quantity increase to two
			page 23 : Add cap. C531 , C748-C752 for monitor test
		20100420	page 23 : Remove R12 , R13 and mount common mode choke L1 for EMI requirement
			page 25 : R589,R592 need to mount the bead SBY100505T121YN(CX05TI2100) for EMI requirement
			page 30 : EMI suggested that R421 , R331 need to be mounted
			page 30 : R384 , R385 need to mount the bead(CX471T10000) for EMI
			page 30 : C525 , C527 need to mount cap. 20pF for EMI

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Size | Document Number: Change List01 | Rev: 1A
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