

BAP/BXP30

A02 Build

2010.05.22

INVENTEC

TITLE
BAP/BXP30

SIZE Custom	CODE CS	DOC NUMBER CS-131	REV X01
SHEET		1	of 41

CHANGE by	IEC	DATE	Saturday, May 22, 2010
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1. Schematic Page Description :

BAP30/BXP30 Schematic Ver : X01

01. Title	16. Processor(2/3)	31. EASY PORT
02. Schematic Page DESCR	17. Processor(3/3)	32. Hybrid Switch (1/2)
03. Block Diagram	18. PCH_RTC,SATA,PCI-E,CLK	33. Hybrid Switch (2/2)
04. Power Block Diagram	19. PCH_DMI,MISC,LVDS,CRT	34. N10x PCIE/ I/O(1/6)
05. Annotations	20. PCH_USB, PCI,NVRAM,XDP	35. N10x Memory(2/6)
06. Schematic Modify	21. PCH Power 1	36. N10x Power(3/6)
07. Timing Diagram	22. PCH Power 2	37 1.8V/1.05V/NVDD(4/6)
08. PWR_Adaptor in/Charge	23. Clock Generator	38. DDR3 VRAM
09. PWR_CPU Core Power	24. DDR3 SDRAM SO-DIMM 0/1	39. CX20672-11Z
10. PWR_Graphics Core	25. LCD/CAM/DVI PLUG/CRT	40. Card reader/ Audio
11. PWR_DDR PWR	26. USB/LID/LED	41. POWER SEQUENCE
12. PWR_1.1VS_VTT/1.1VS	27. BCM57760	
13. PWR_5VA/5VLA/3VA/3VLA	28. 3G/USIM	
14. PWR_3VS/5VS/1.8VS/5VUSB	29. HDD/ODD/DAUGHTER CONN	
15. Processor(1/3)	30. KBC ITE8502E*	

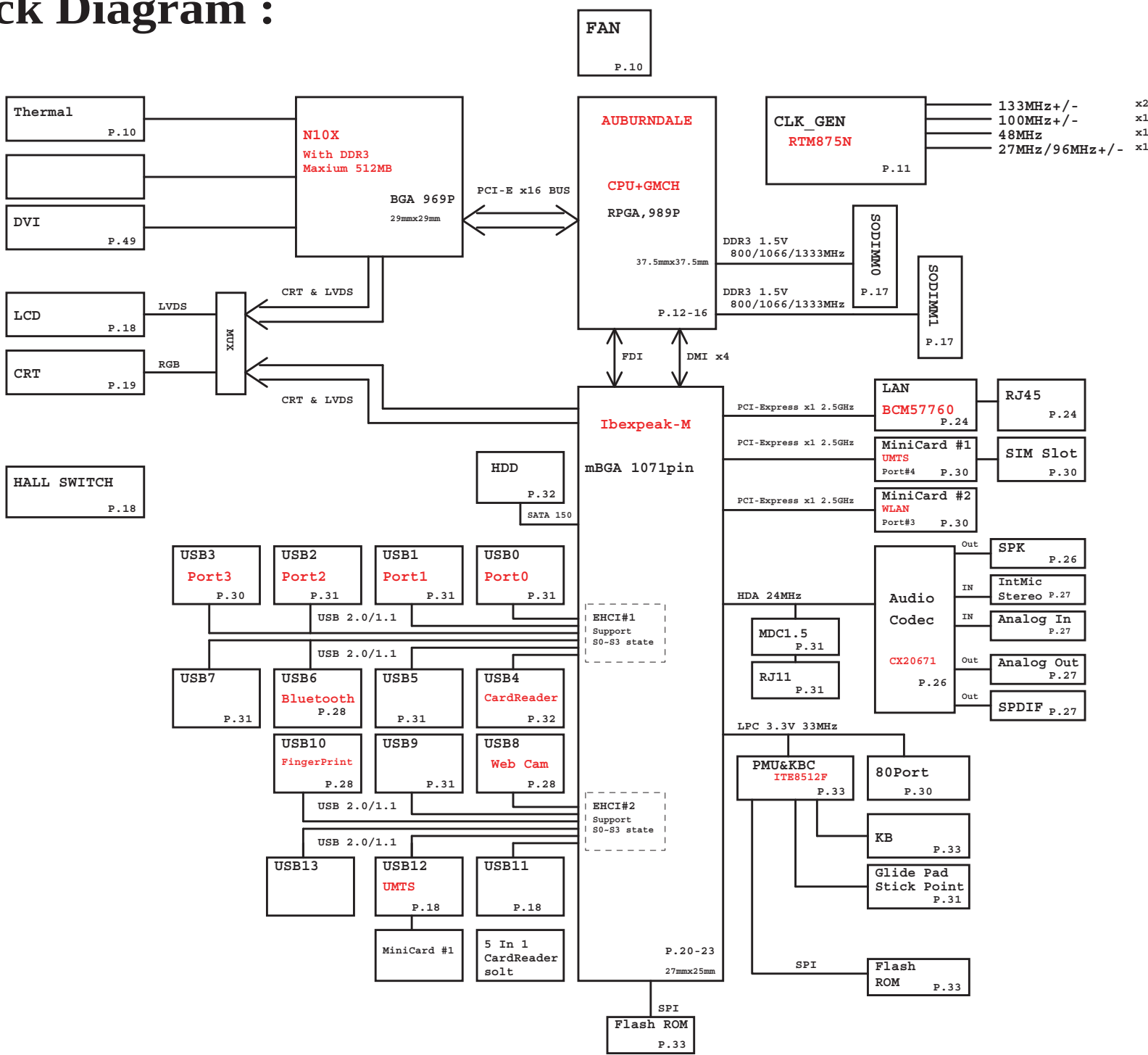
2. PCI & IRQ & DMA Description :

IDSEL	CHIP	PCIINT	CHIP	Interface	REQ	CHIP
None		None			None	

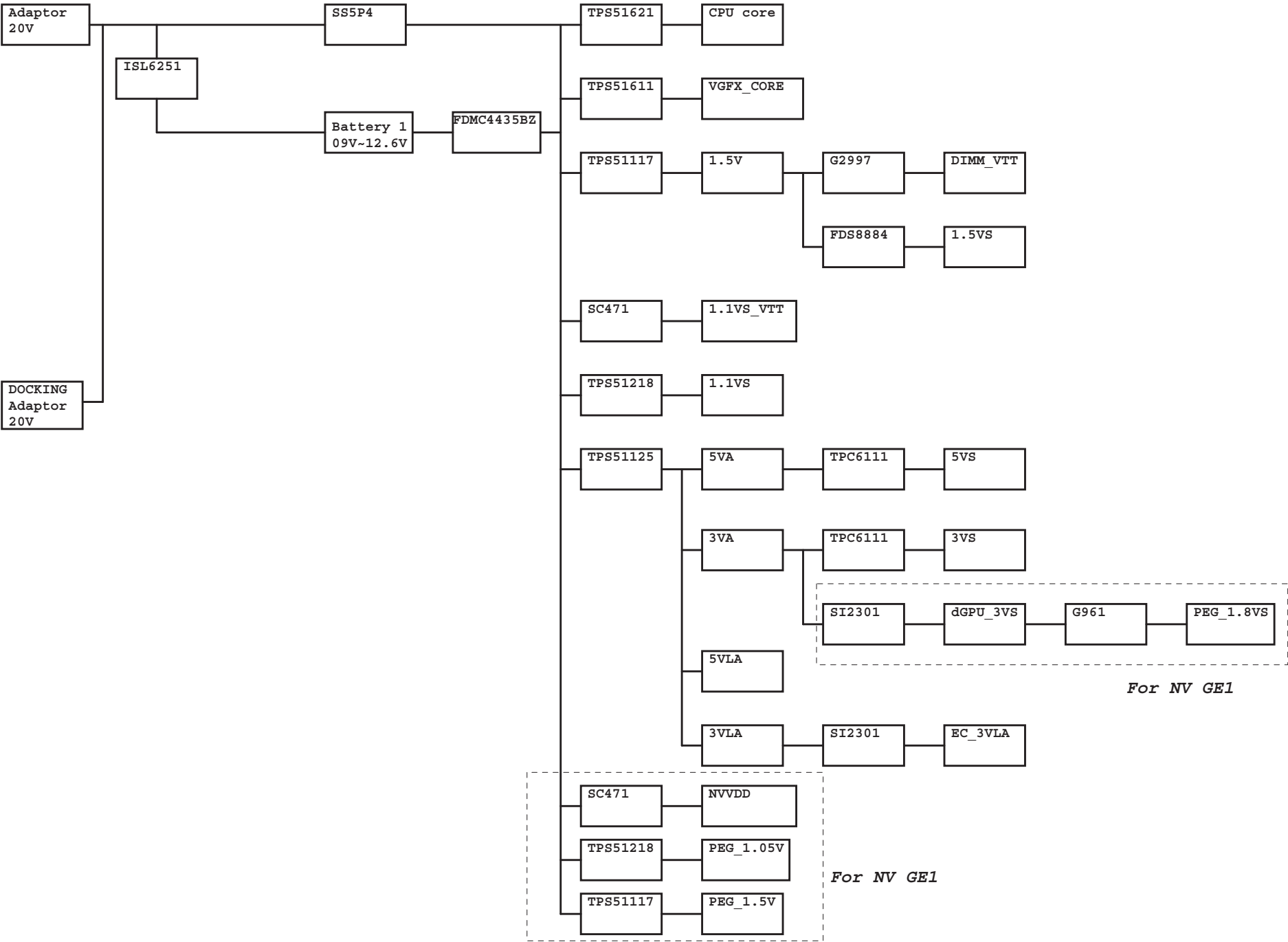
3. USB & PCI-Express & SATA Description :

USB Port	DEVICE	USB Port	DEVICE	PCI-E	DEVICE	SATA	DEVICE
Port 0	System (ESATA)	Port 7	Bluetooth	Port 1	New Card	Port 1	HDD
Port 1	System	Port 8		Port 2	Docking	Port 2	E-SATA
Port 2	System	Port 9	Web Cam	Port 3	Mini Card(WLAN)	Port 4	BAY
Port 3	System	Port 10		Port 4	Mini Card(3G)	Port 5	None
Port 4	CardReader	Port 11	FingerPrint	Port 5	Mini Card(ROBSON)		
Port 5		Port 12		Port 6	Giga-LAN		
Port 6		Port 13	3G				

3. Block Diagram :



Power Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
3VLA	3.3V always on power rail by DCIN
5VLA	5.0V always on power rail by DCIN
EC 3VLA	3.3V always on power rail by 5VAUXON
3VA	3.3V always on power rail by LATCH_ON
5VA	5.0V always on power rail by LATCH_ON
3VM	3.3V power rail by SUSM#
1.05VM	1.05V switched power rail by SUSM#
1.5V	1.5V switched power rail by SUSC#
1.8V	1.8V power rail by SUSC#
3VS	3.3V power rail by SUSB#
5VS	5.0V power rail by SUSB#
1.5VS	1.5V power rail by SUSB#
1.05VS	1.05V power rail by SUSB#
PWR_DIMM_VTT	0.75V DDR Termination Voltage by SUSB#
VGFX_CORE	1.05V power rail for UMA by SUSB#
PEG 1.8VS	1.8V switched power rail for NB9x by SUSB#
PEG_PEX_1.1VS	1.1V switched power rail for NB9x by SUSB#
PEG_NVDD	Variable switched power rail for NB9x by SUSB#
Vcore_CPU	Core switched power rail for CPU

Part Naming Conventions

C	=	Capacitor	Q	=	Transistor
CN	=	Connector	R	=	Resistor
D	=	Diode	RP	=	Resistor Pack
F	=	Fuse	U	=	Arbitrary Logic Device
L	=	Inductor	Y	=	Crystal and Osc

Name Suffix

#	=	Active Low signal
NU	=	No Stuff

5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip(5-mils)	Differential Impedance for Stripline(4-mils)
Host Clock	95 ohm +/- 20%	100 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	100 ohm +/- 20%
DDR2 CLK	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	85 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	100 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	100 ohm +/- 20%
SDVO	95 ohm +/- 20%	100 ohm +/- 20%
SATA	95 ohm +/- 20%	100 ohm +/- 20%
USB	90 ohm +/- 20%	95 ohm +/- 20%
LVDS		100 ohm +/- 20%
Lan	95 ohm +/- 20%	100 ohm +/- 20%

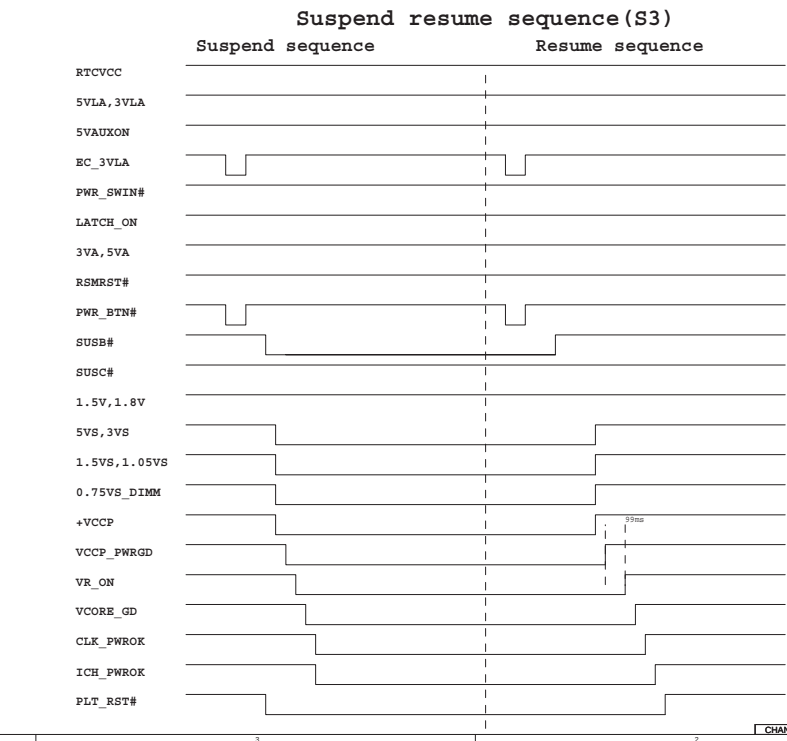
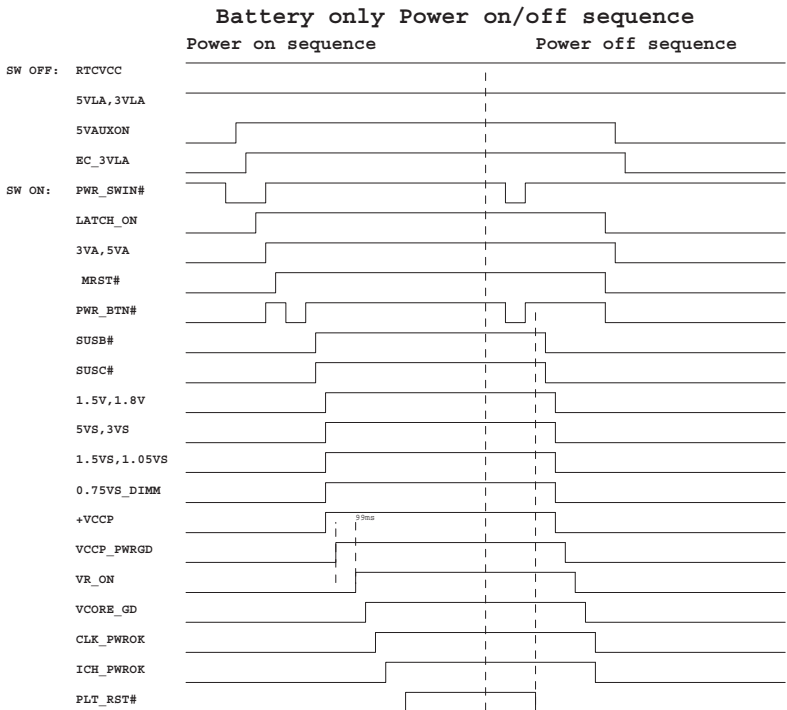
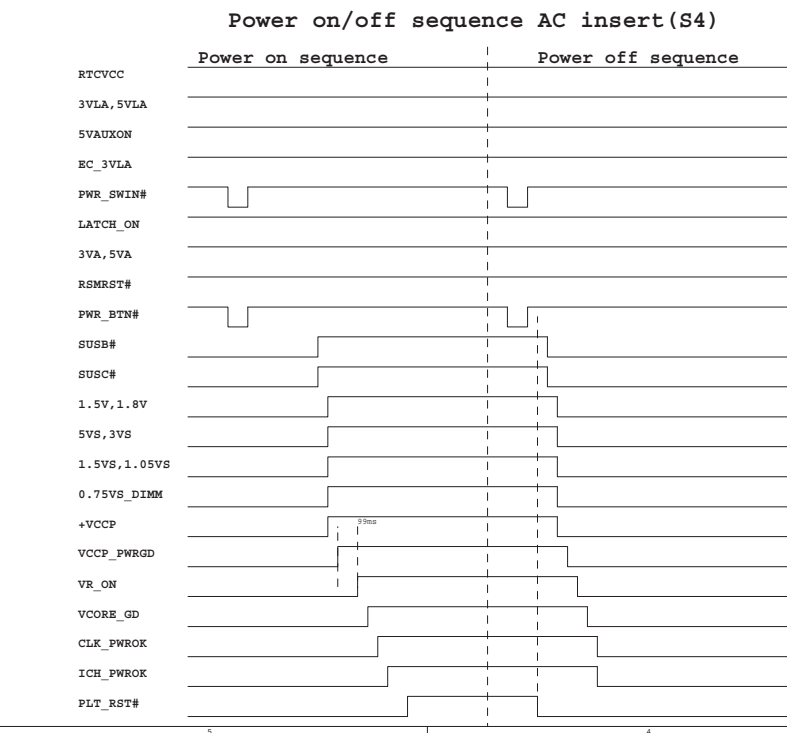
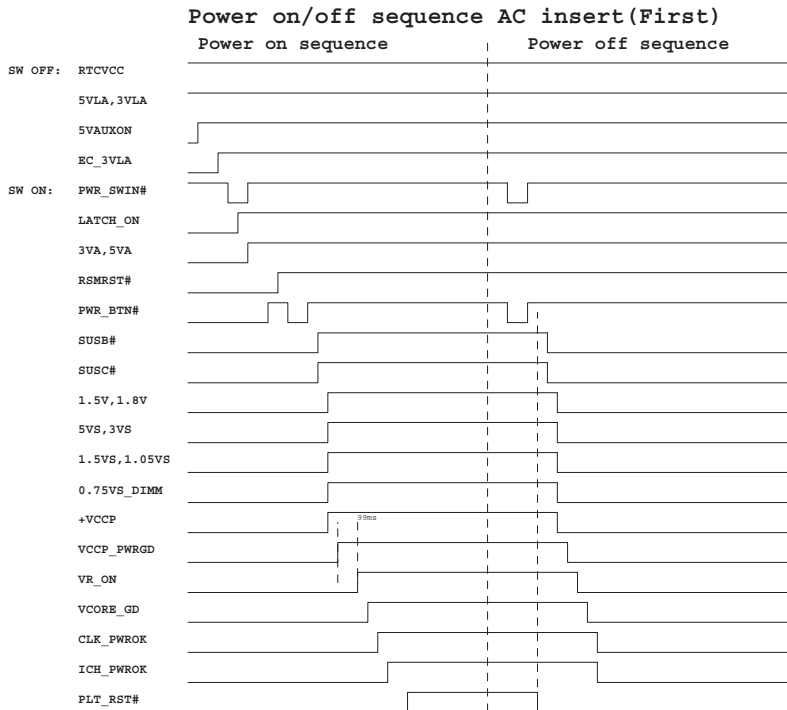
Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	36A
1.05VS	Penryn: AGTL+ termination Cantiga GM: Core Cantiga GM: PCIE Cantiga GM:Core+IMEL+HSIO Cantiga GM:VCC_GMCH Cantiga GM:VCCA_SM_CK and NCTF Cantiga GM:VCC_DMI Cantiga GM:VCCA_SM Cantiga GM:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn PLL Cantiga GM: QDAC Cantiga GM: LVDS Cantiga GM: TVDAC Cantiga GM: Various PLLS analog supply Cantiga GM: VCC_SM_CK Cantiga GM: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GM: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GM: HV CMOS Cantiga GM: VCCS_TV DAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS397BKLF Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:82567LM Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 1.0V and 1.8V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A Each 1A
5VS	Cardreader: GL827 Azalia Codec: ALC262 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB and ESATA	5VA 5VA	1.5A 2A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

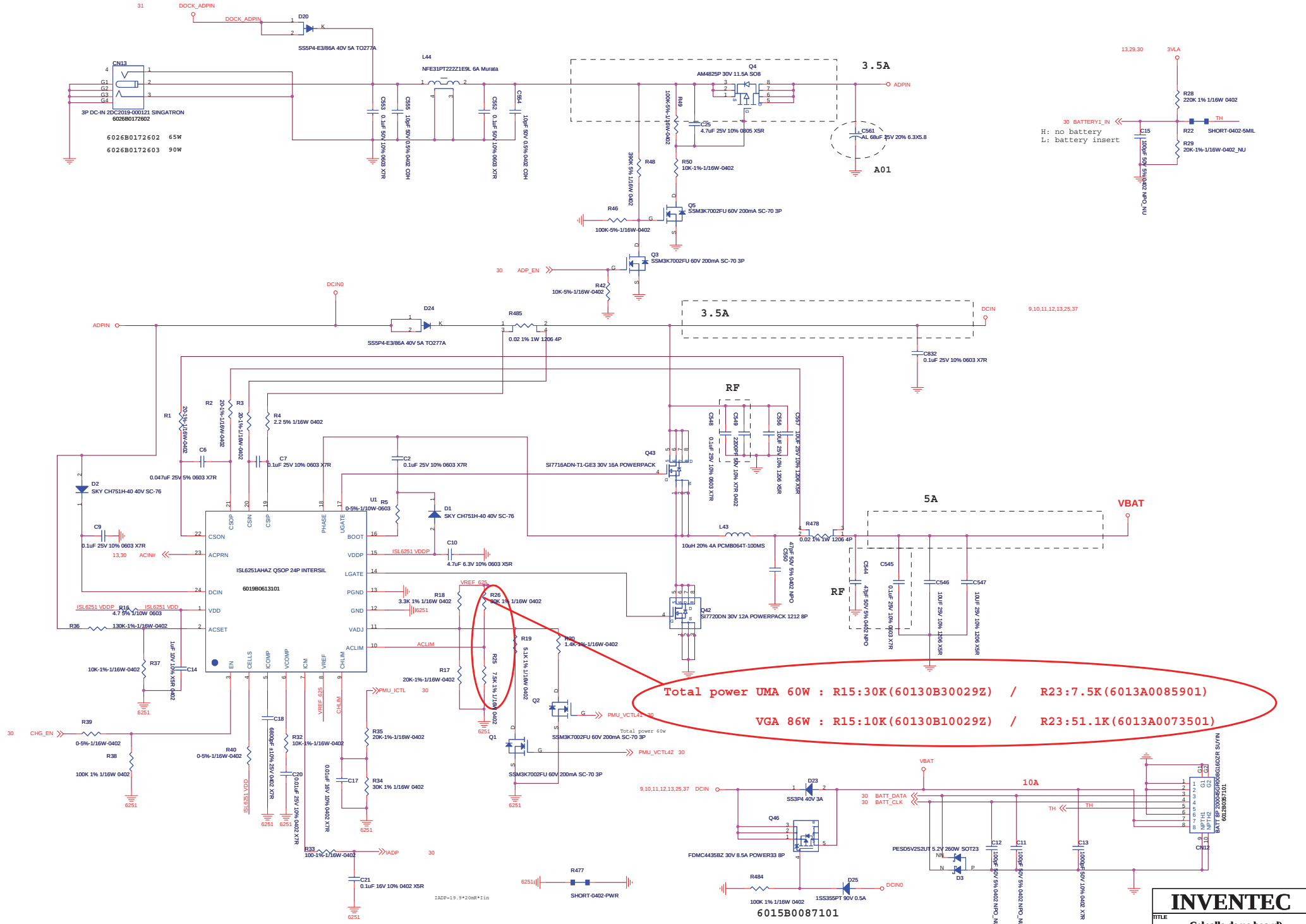
INVENTEC				
BAP/BXP30				
Annotations				
SIZE	CODE	DOC NUMBER	REV	
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6.Schematic modify Item and History :

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TITLE			
BAP/BXP30			
schematics modify			
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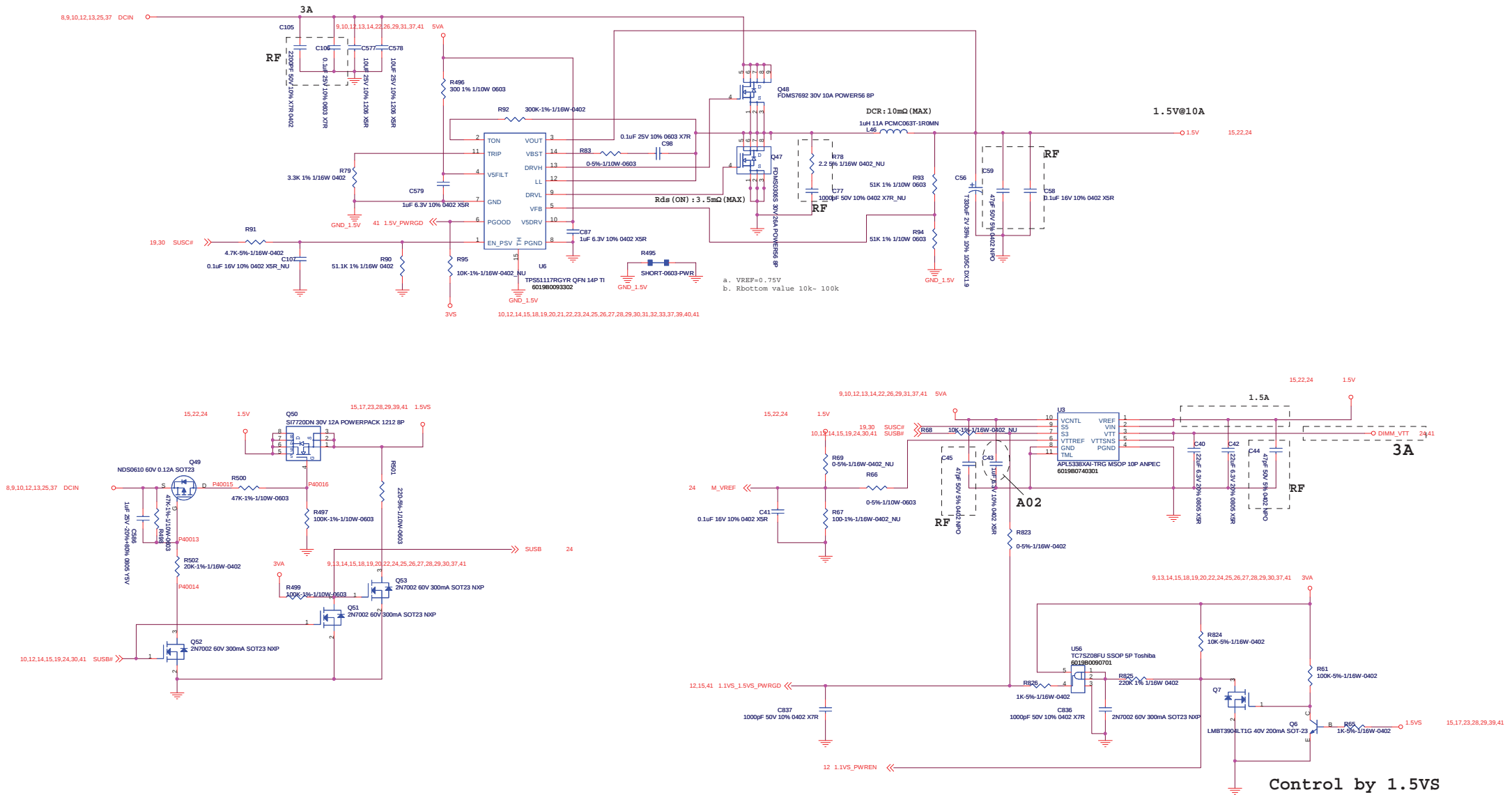
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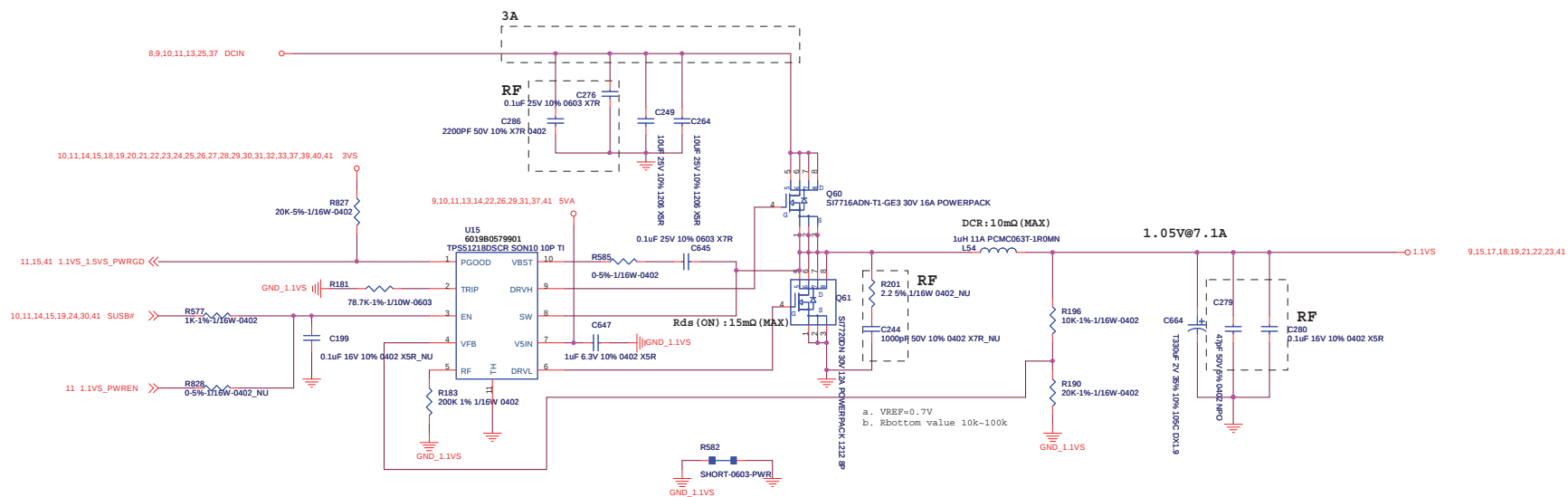
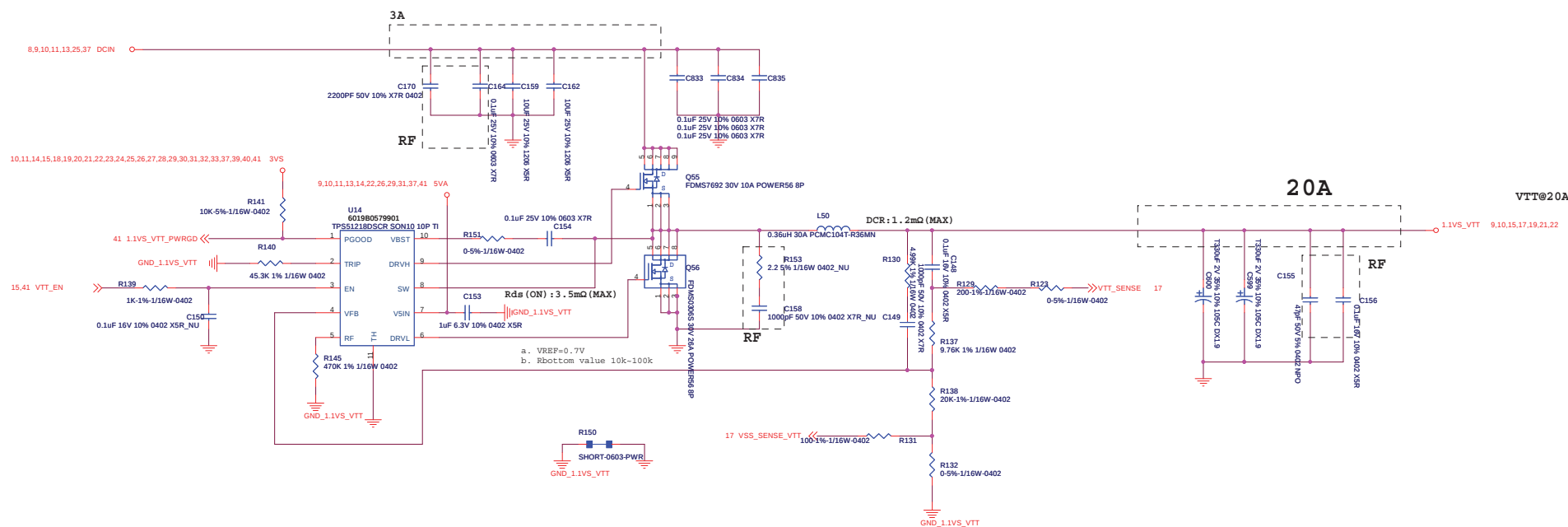


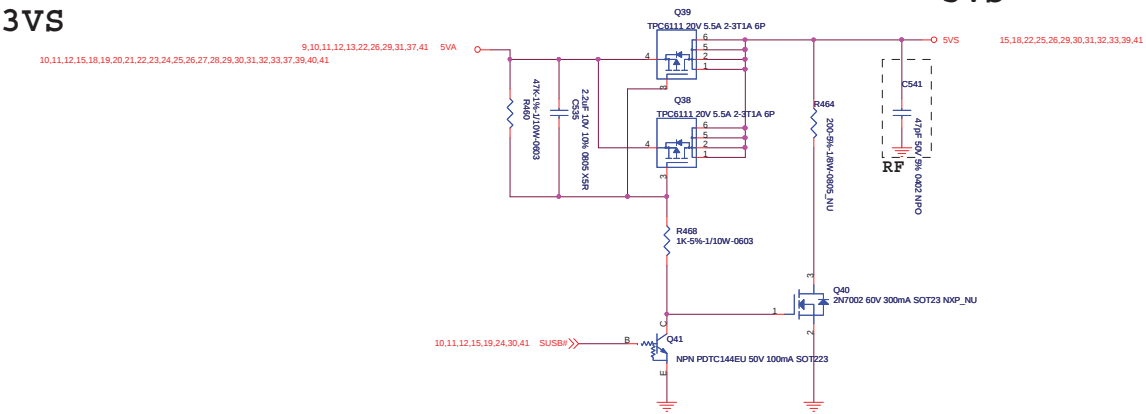
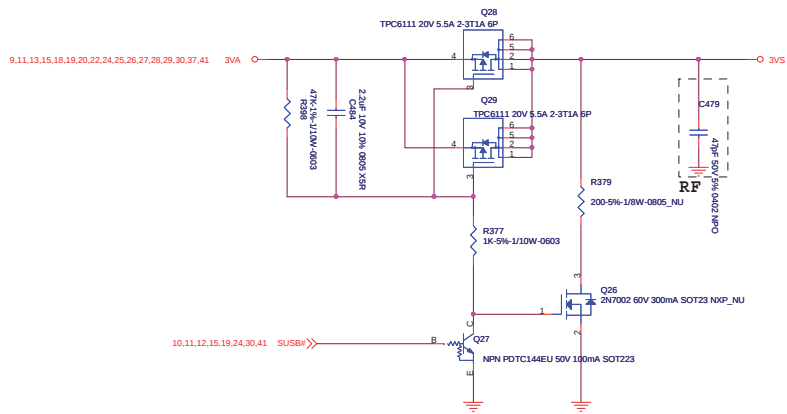
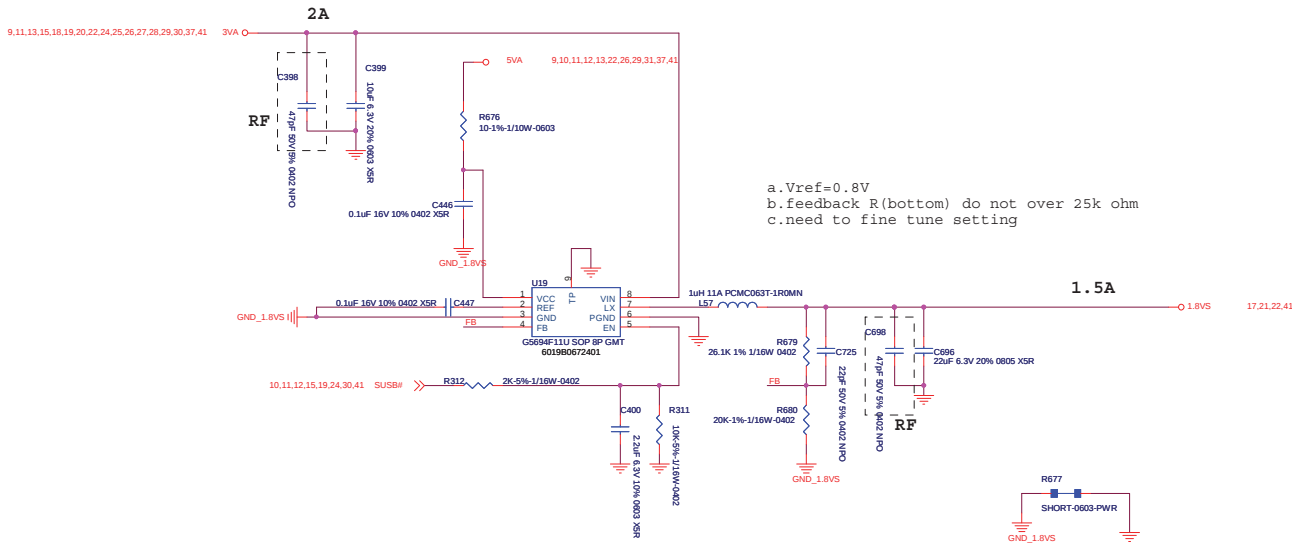
CPU core Power			
SIZE Custom	CODE CS	DOC.NUMBER CS-131	
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DDR POWER



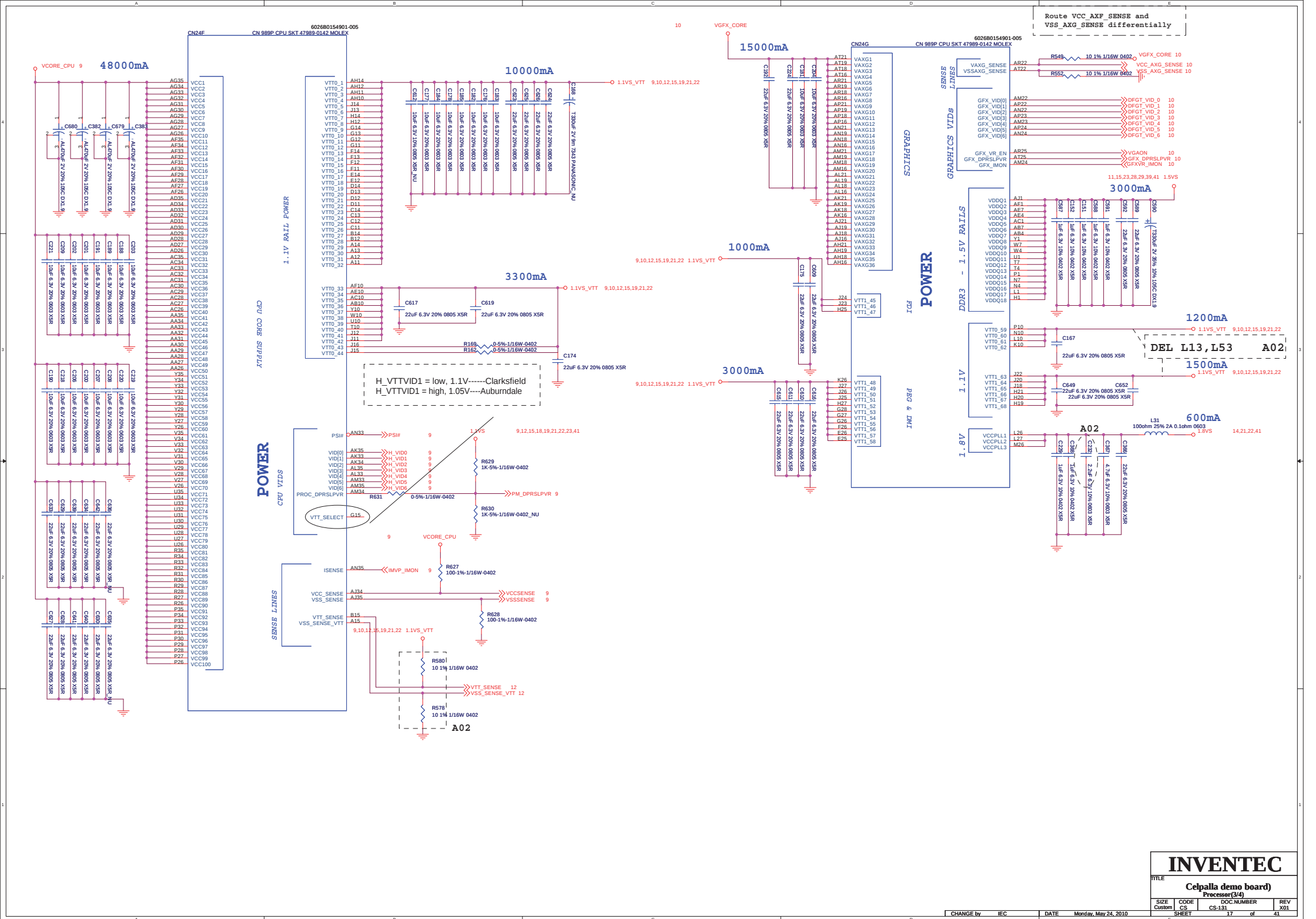
Control by 1.5VS





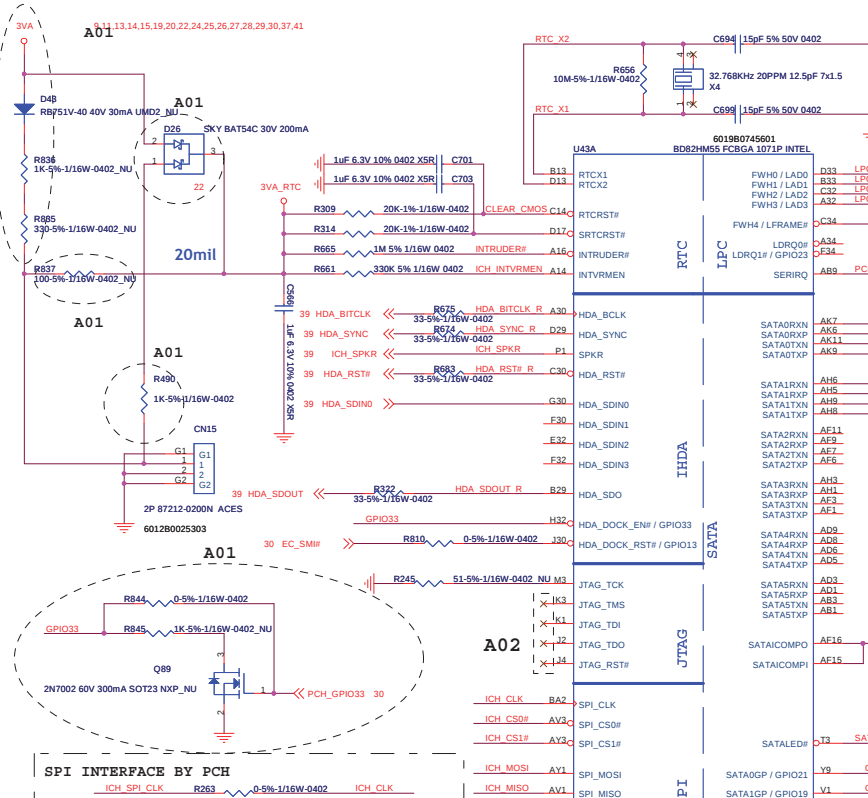






RTC Circuit

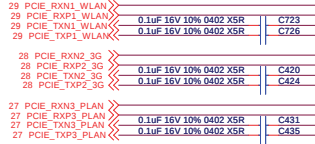
A01



WLAN

3G CARD

PCIE LAN



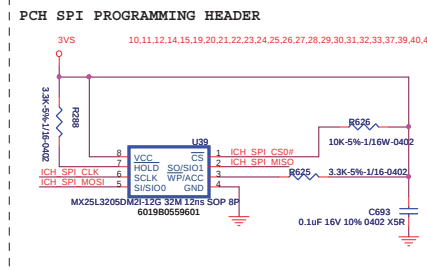
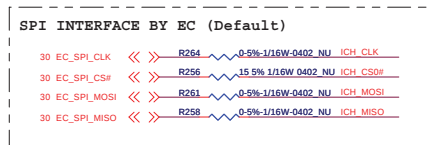
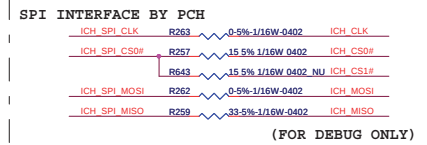
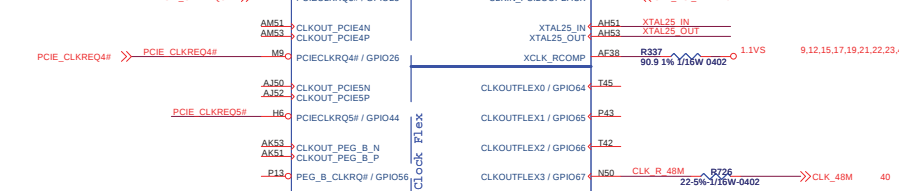
HDD I/F

ODD I/F

WLAN

3G CARD

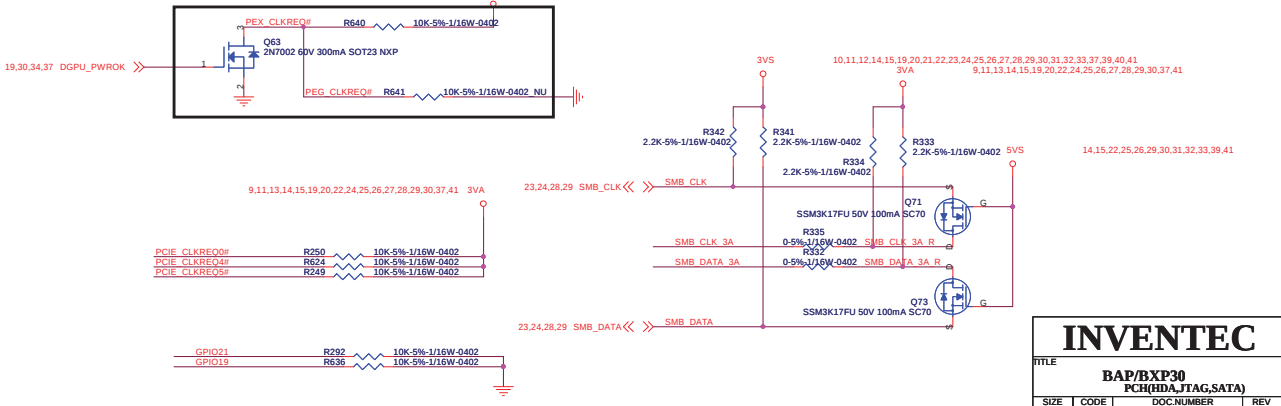
PCIE LAN



Flash Descriptor Security Override	
PCH_GPIO33	Low : Enable
	High : Disable

STUFF for iTPM enable

PCIECLKREQ# 0,3,4,5,6,7 --- 3VA plane
PCIECLKREQ# 1,2 --- 3VS plane



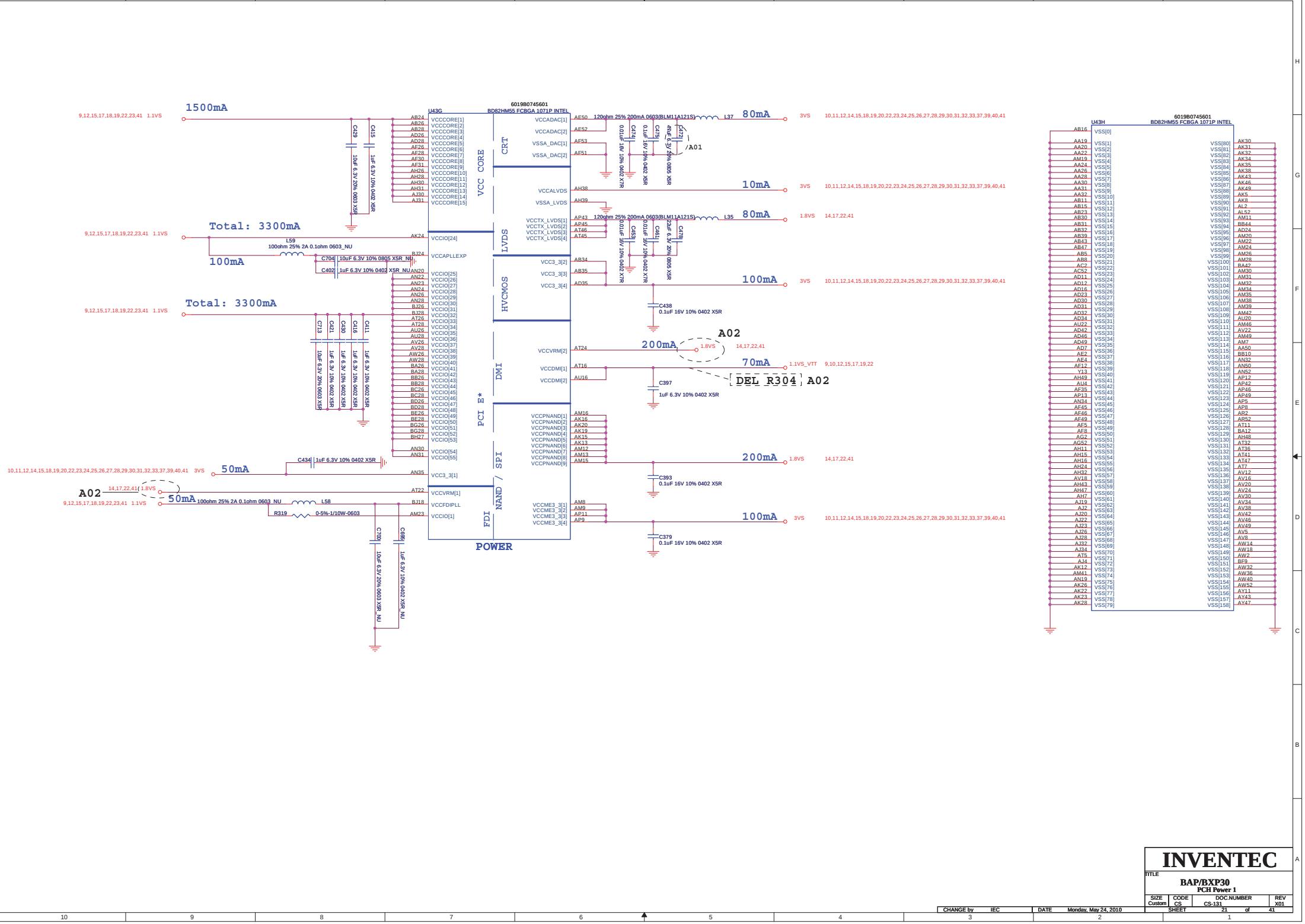
INVENTEC				
TITLE				
BAP/BXP30				
PCH(HDA, JTAG, SATA)				
SIZE	CODE	DOC NUMBER	REV	
Custom	CS	CS-131	1.0	41
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CHANGE by	IEC	DATE	Monday, May 24, 2010
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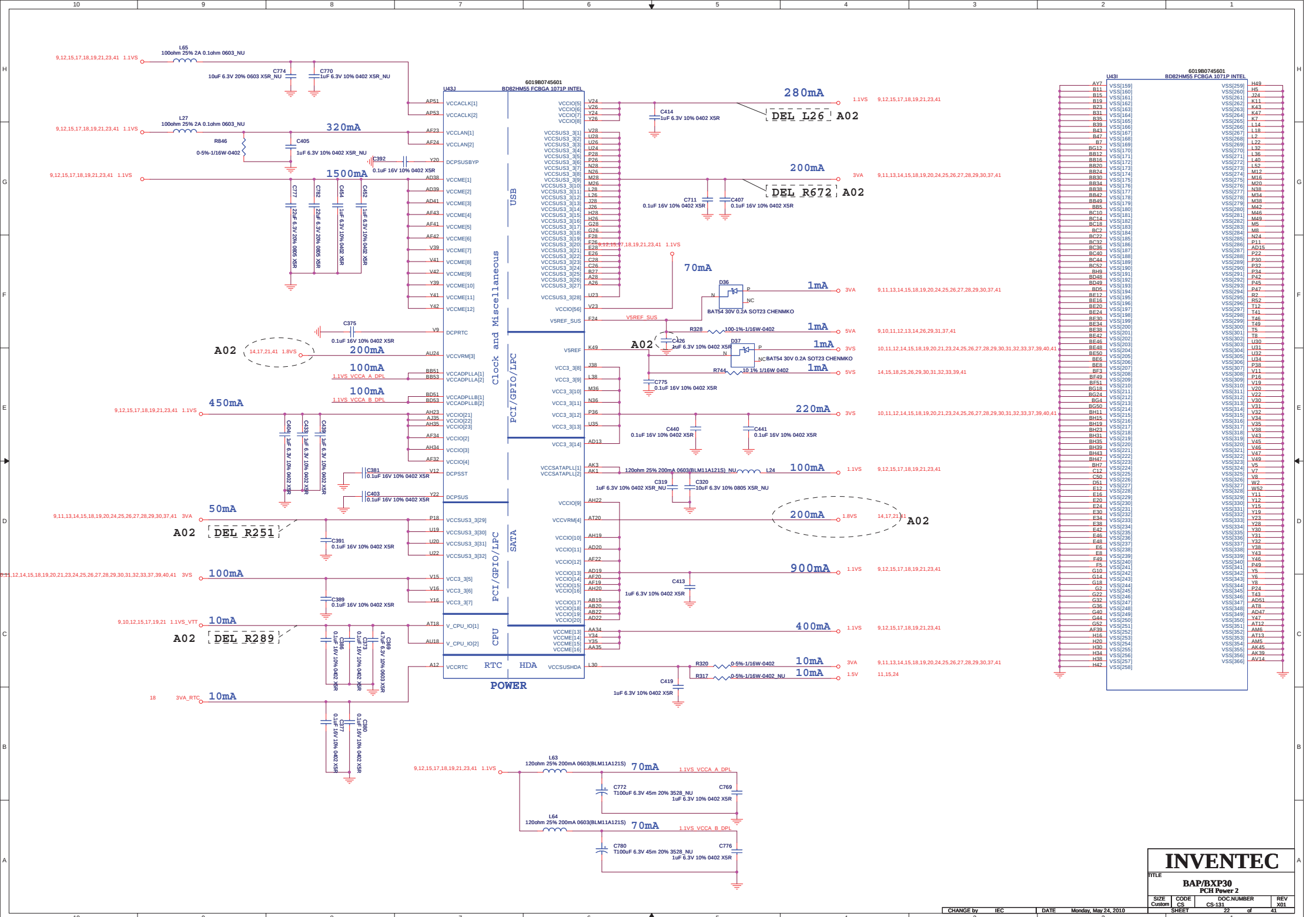


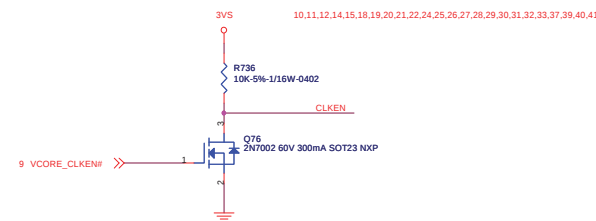
INVENTEC

TITLE				
BAP/BXP30				
PCH(FDI,DMI,SPM)				
SIZE	CODE	DOC NUMBER	REV	
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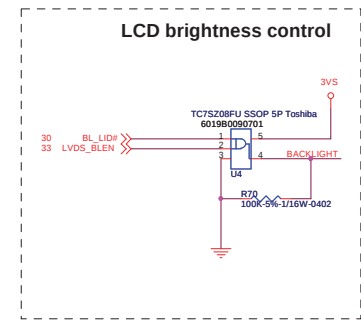
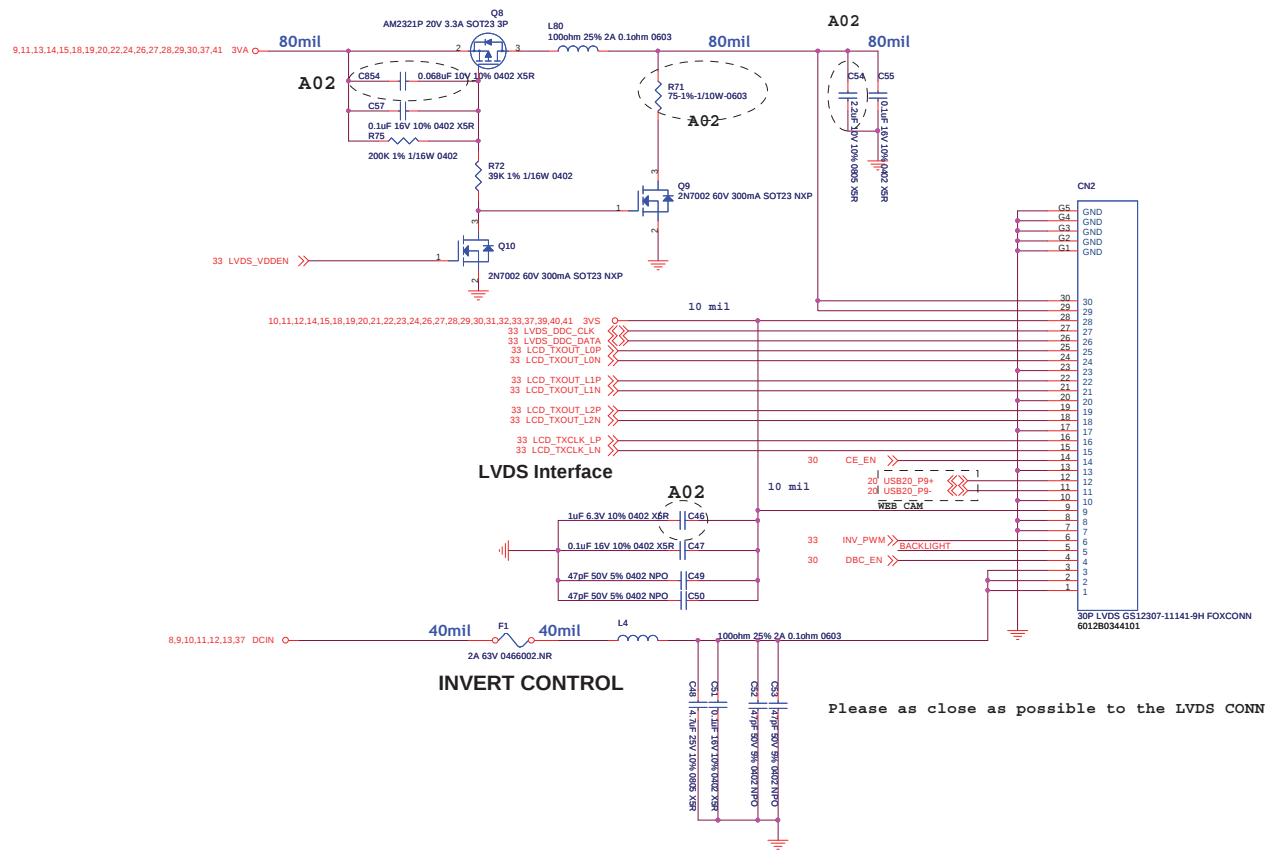
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BAP/BXP30				
PCH Power 1				
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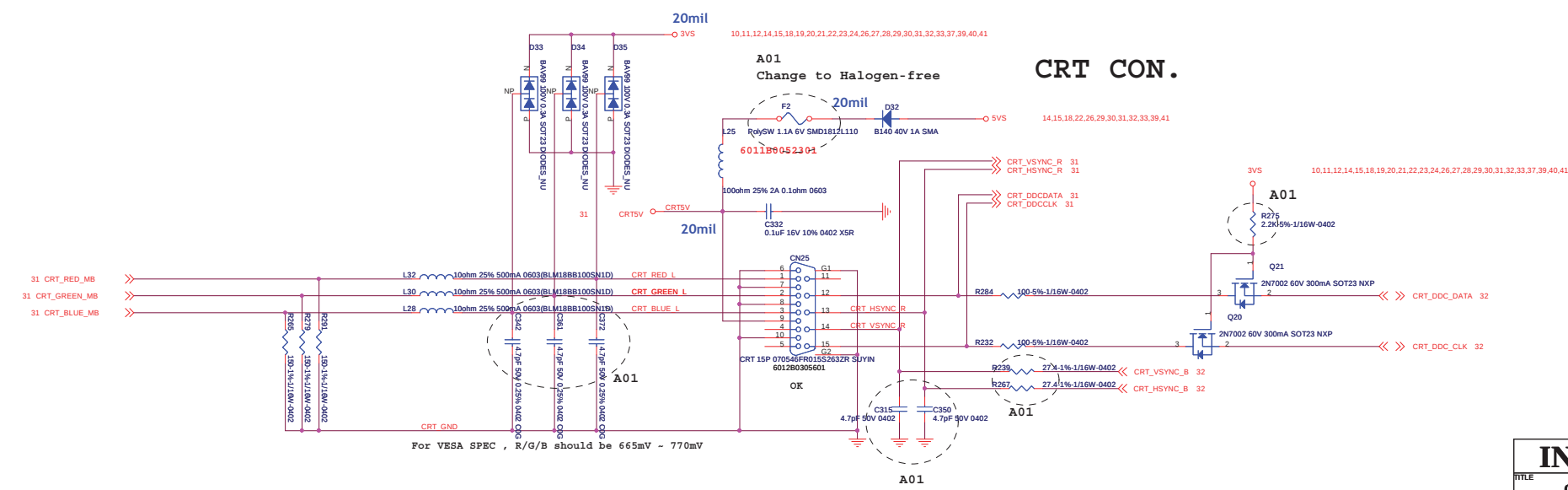
SO-DIMM1





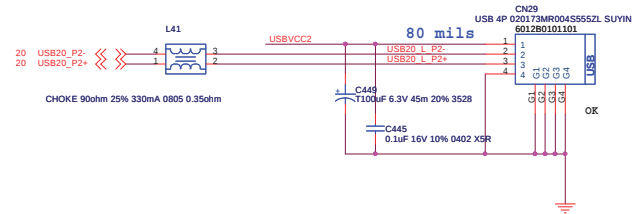
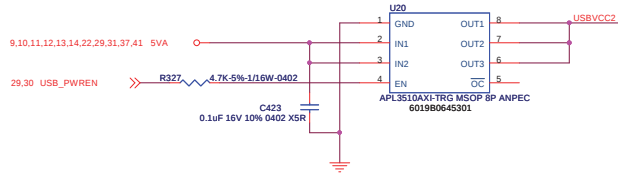
10,11,12,14,15,18,19,20,21,22,23,24,26,27,28,29,30,31,32,33,37,39,40,41

Please as close as possible to the LVDS CONN

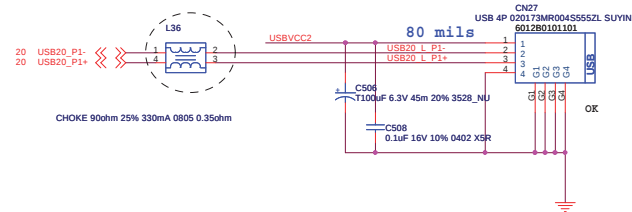


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TITLE			
Celpalla demo board)			
LCD/LID/NVRAM			
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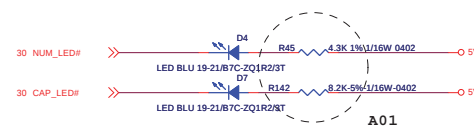
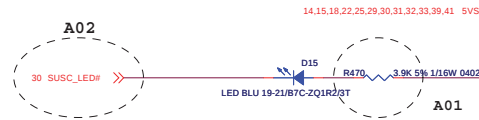
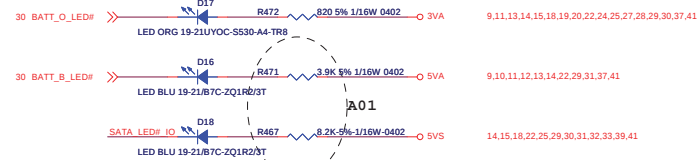
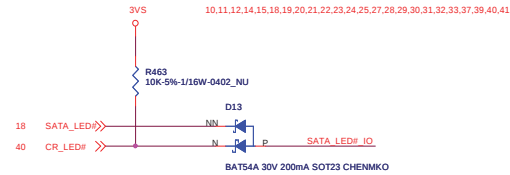
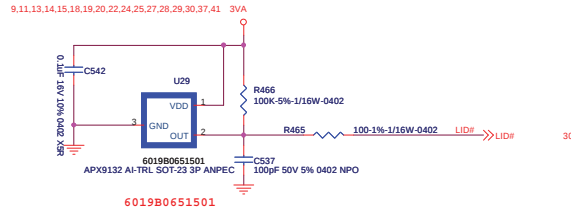
USB



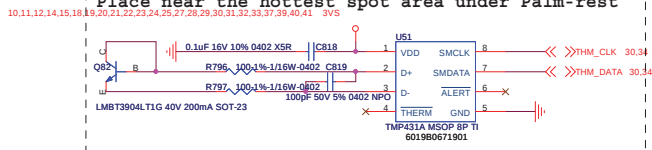
move to bottom side



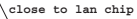
HALL Switch



REMOTE thermal sensor
Place near the hottest spot area under Palm-rest

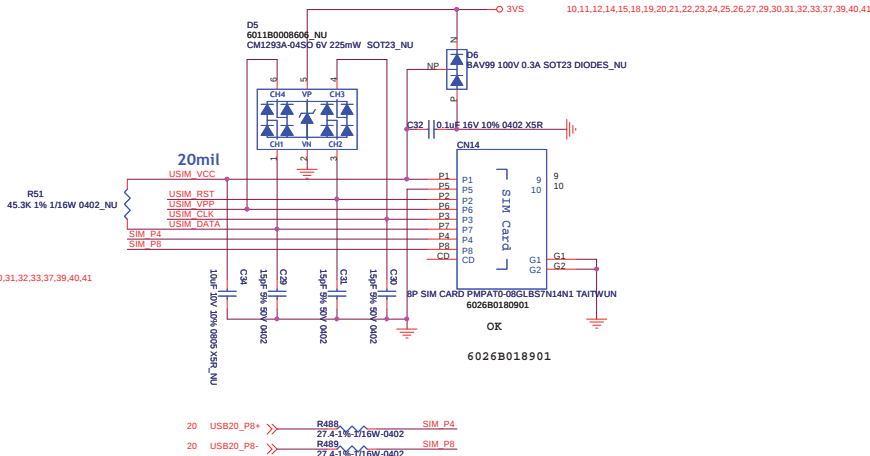
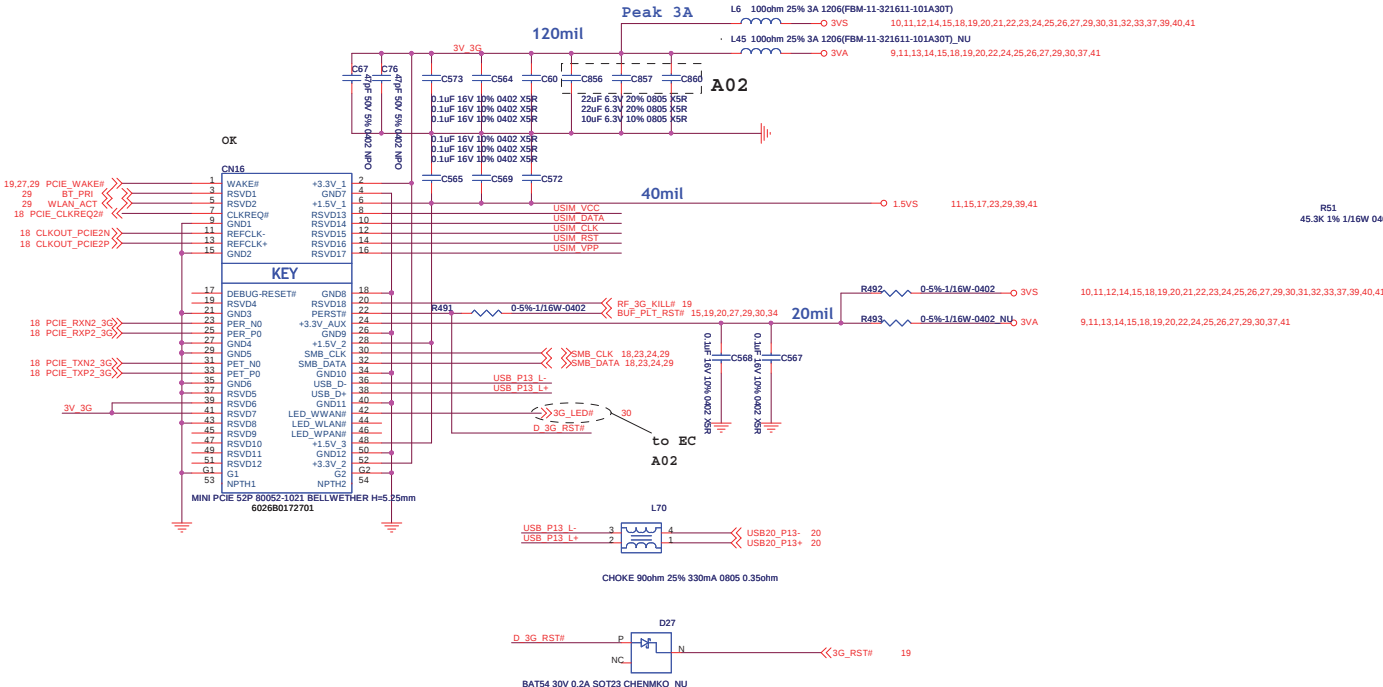


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TITLE BAP/BXP30			
HDD/DAUGHTER CONNECTOR			
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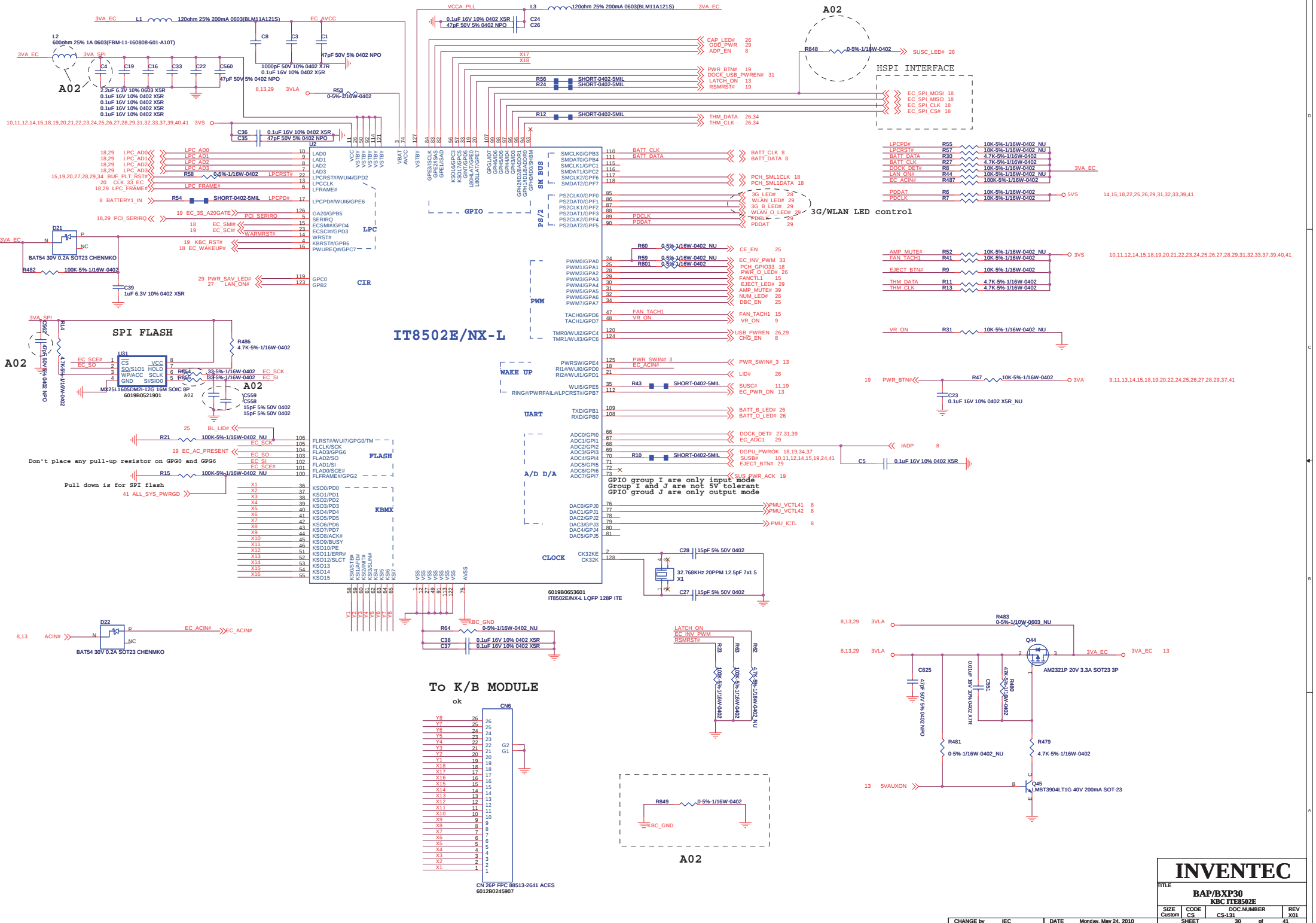
PCIE Mini Card for 3G

On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.



INVENTEC

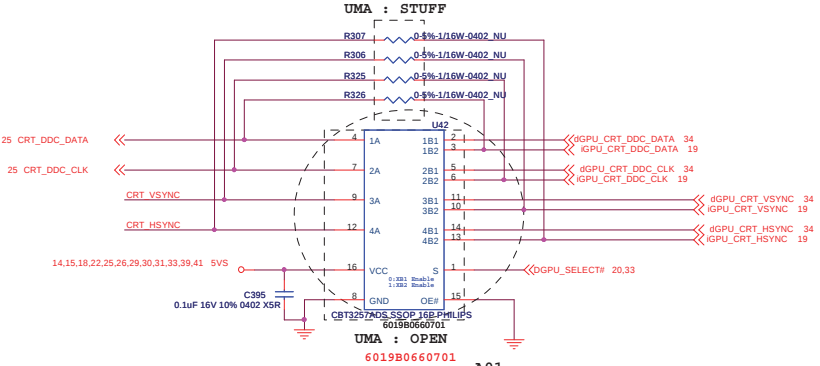
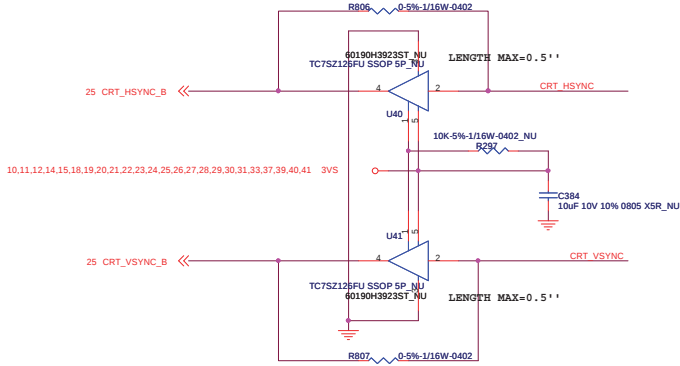
TITLE			
BAP/BXP30 WLAN/3G			
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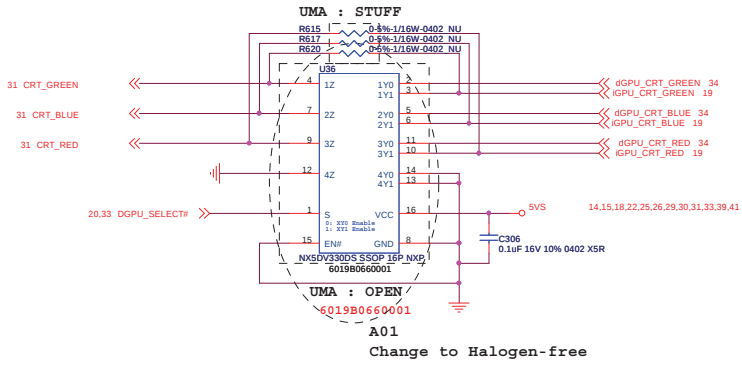
INVENTEC			
TITLE			
BAP/BXP30			
KBC ITERS02E			
SIZE	CODE	DOC NUMBER	REV
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CRT HSYNC/VSYNC SW For Dock



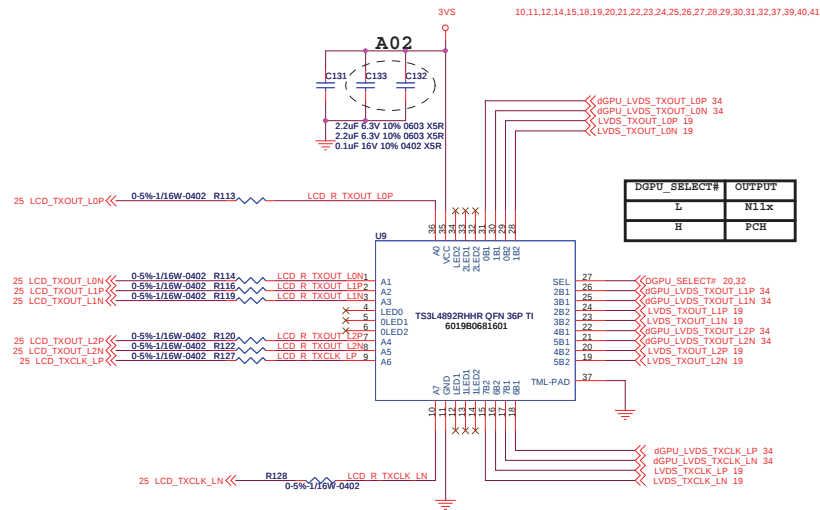
CRT HSYNC/VSYNC/DDC SW



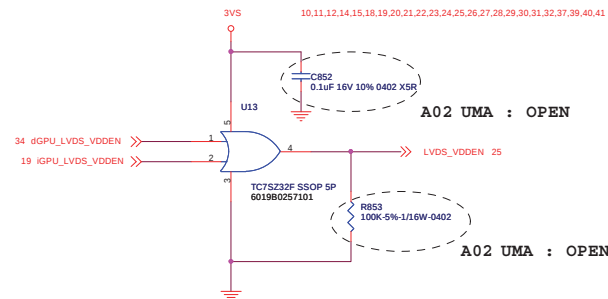
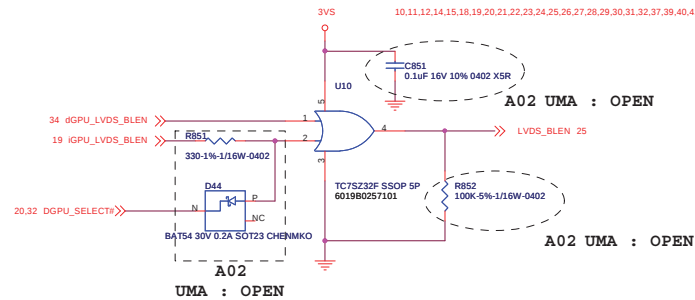
CRT R/G/B SW

Signal	During Reset	After Reset	Description
DGPU_PWR_EN#	High	High	0 : dGPU power switch turned on 1 : power switch turned off
DGPU_PWROK			0 : dGPU power is not stable 1 : dGPU power is stable
DGPU_HOLD_RST#	Low	Low	0 : Keep dGPU in reset 1 : Reset is released
DGPU_SELECT#	High	High	0 : Display switch enabled for dGPU 1 : Display switch enabled for iGPU
HPD_INT#			0 : DVI insertion 1 : No DVI insertion
DGPU_PWM_SELECT#		High	0 : PWM switch enabled for dGPU 1 : PWM switch enabled for iGPU
GPU_EDID_SEL#		High	0 : EDID/DDC switch enabled for dGPU 1 : EDID/DDC switch enabled for iGPU

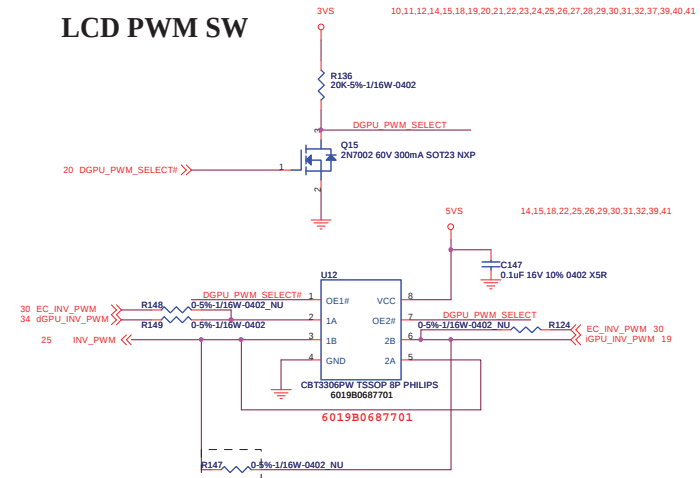
LVDS SW



DGPU_SELECT#	OUTPUT
L	N11x
H	PCH

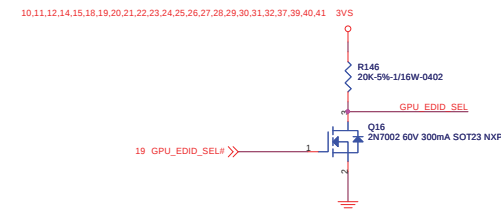
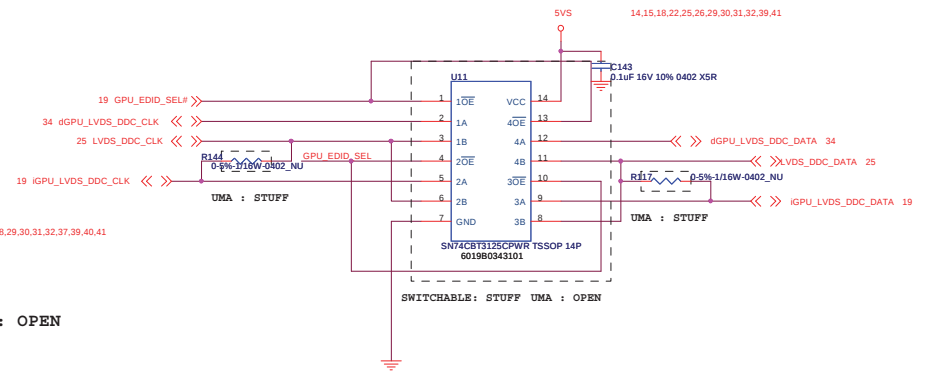


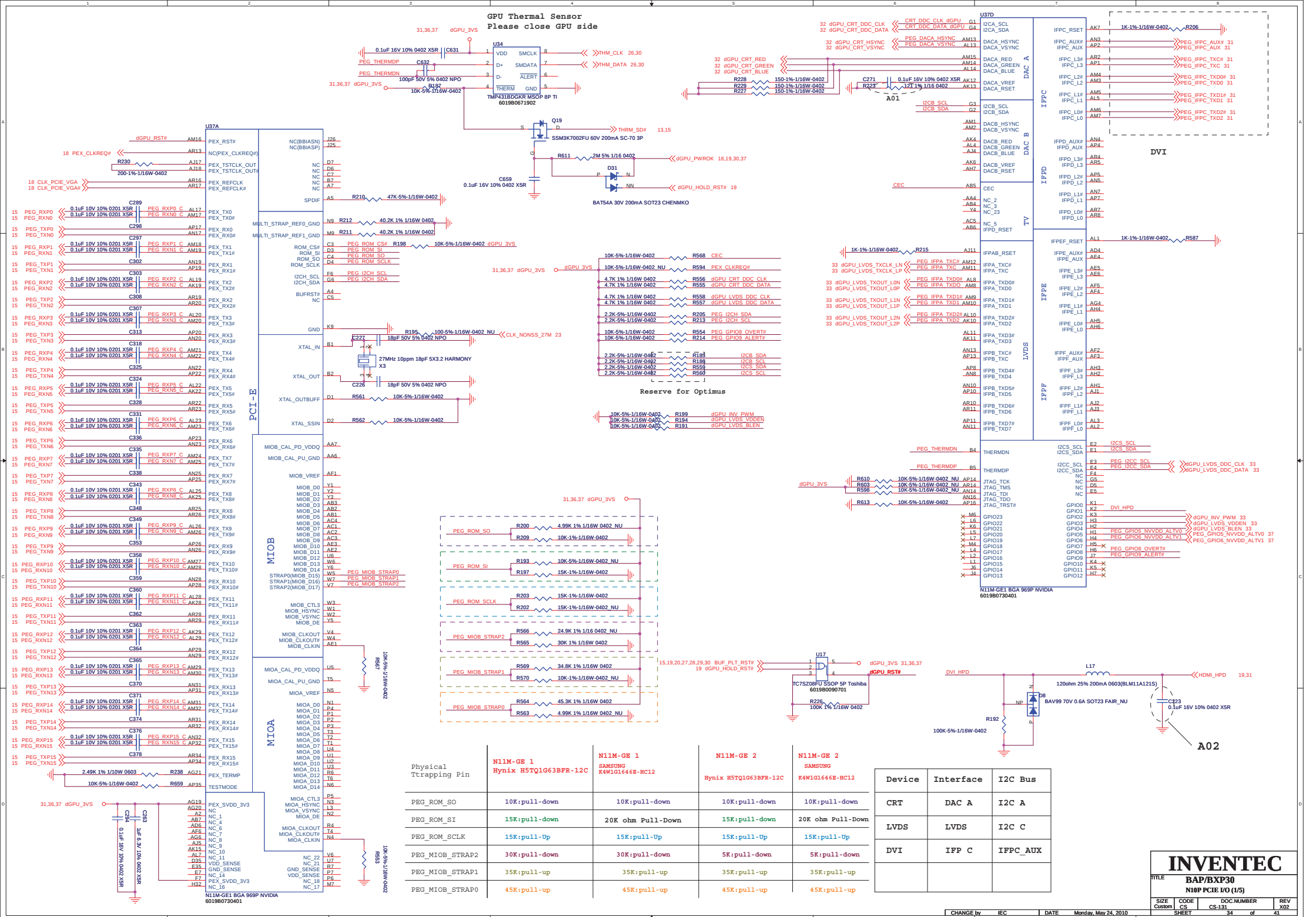
LCD PWM SW

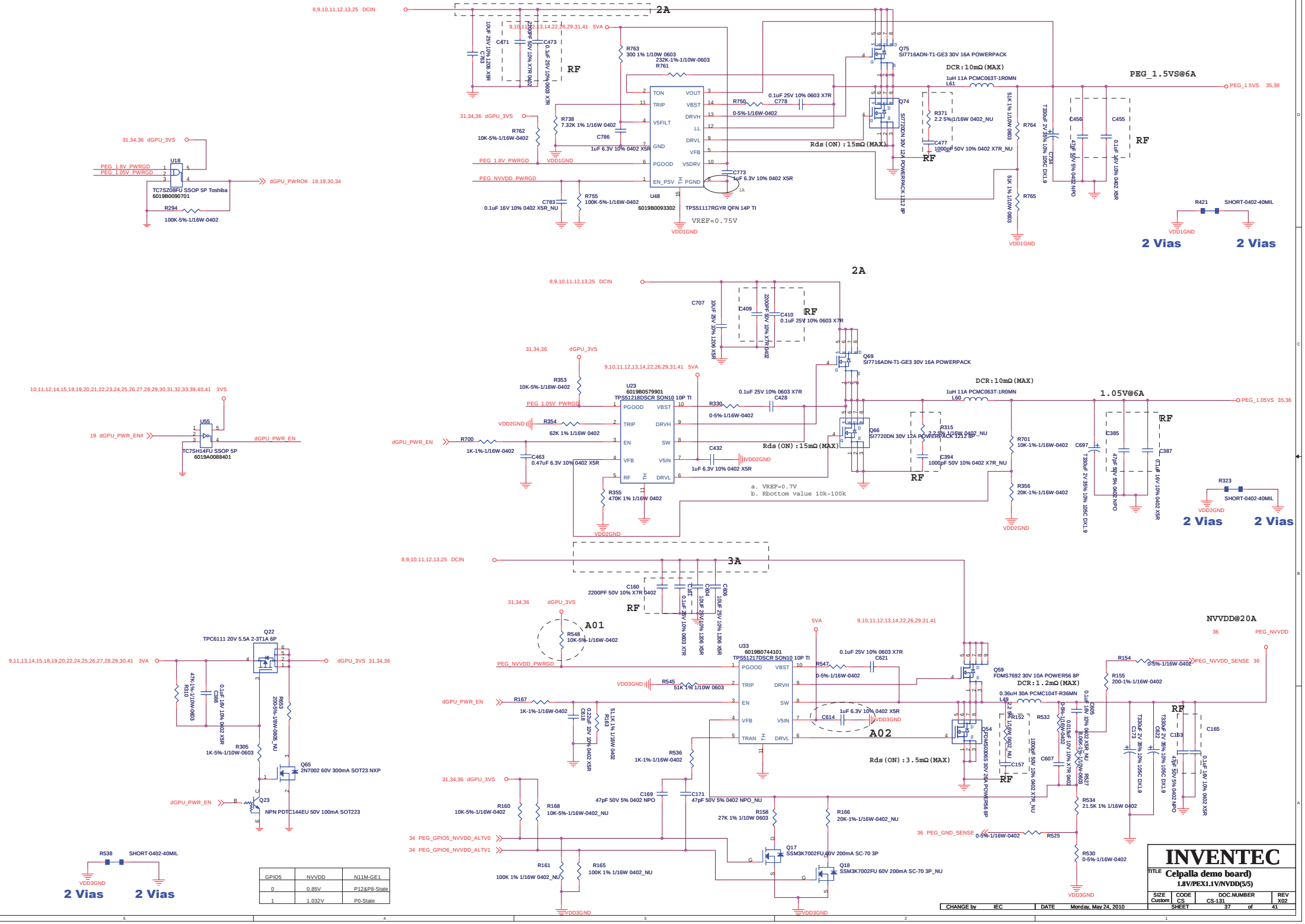


```
SW Gfx:OPEN
UMA:Stuff
```

LCD DDC SW

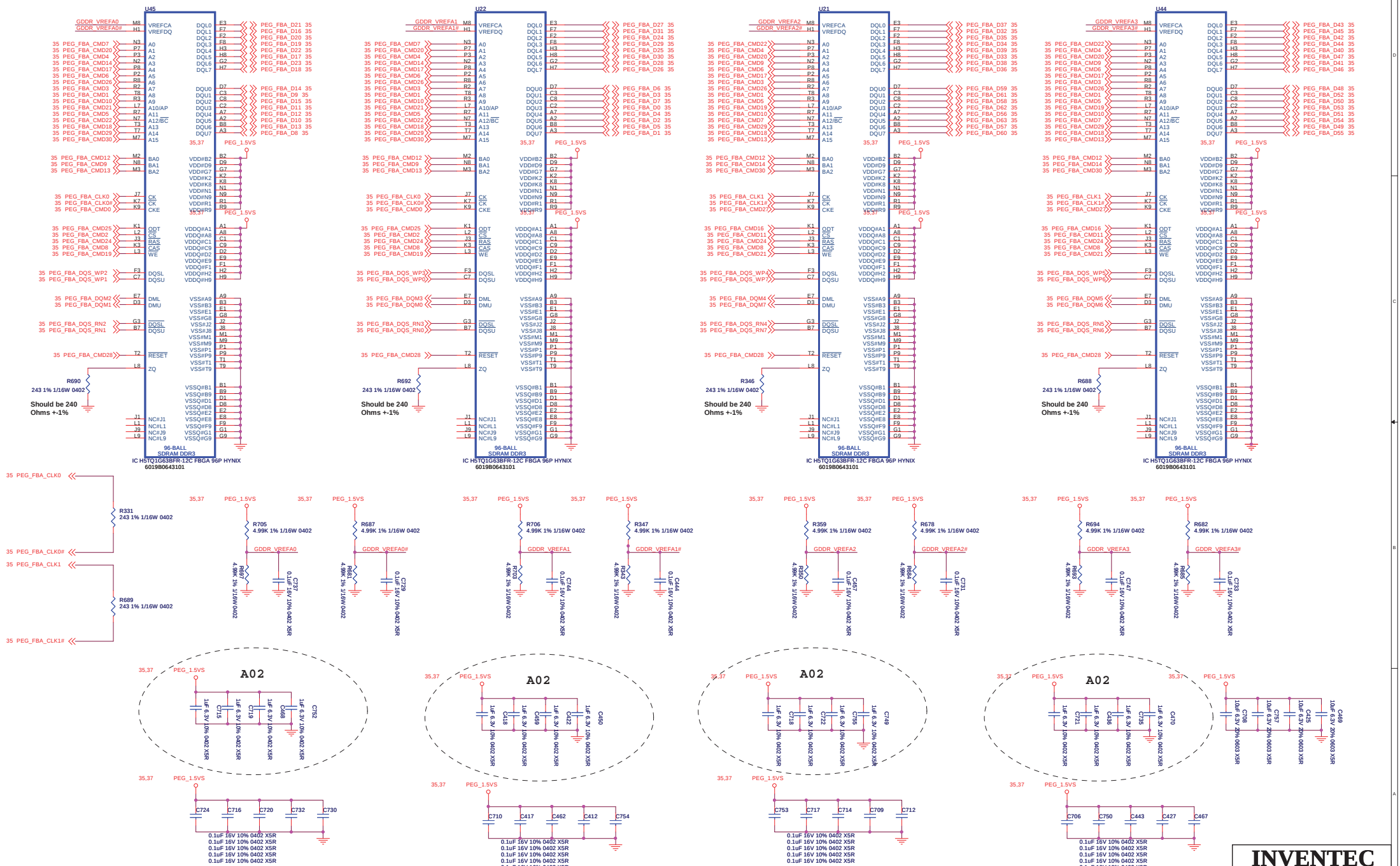






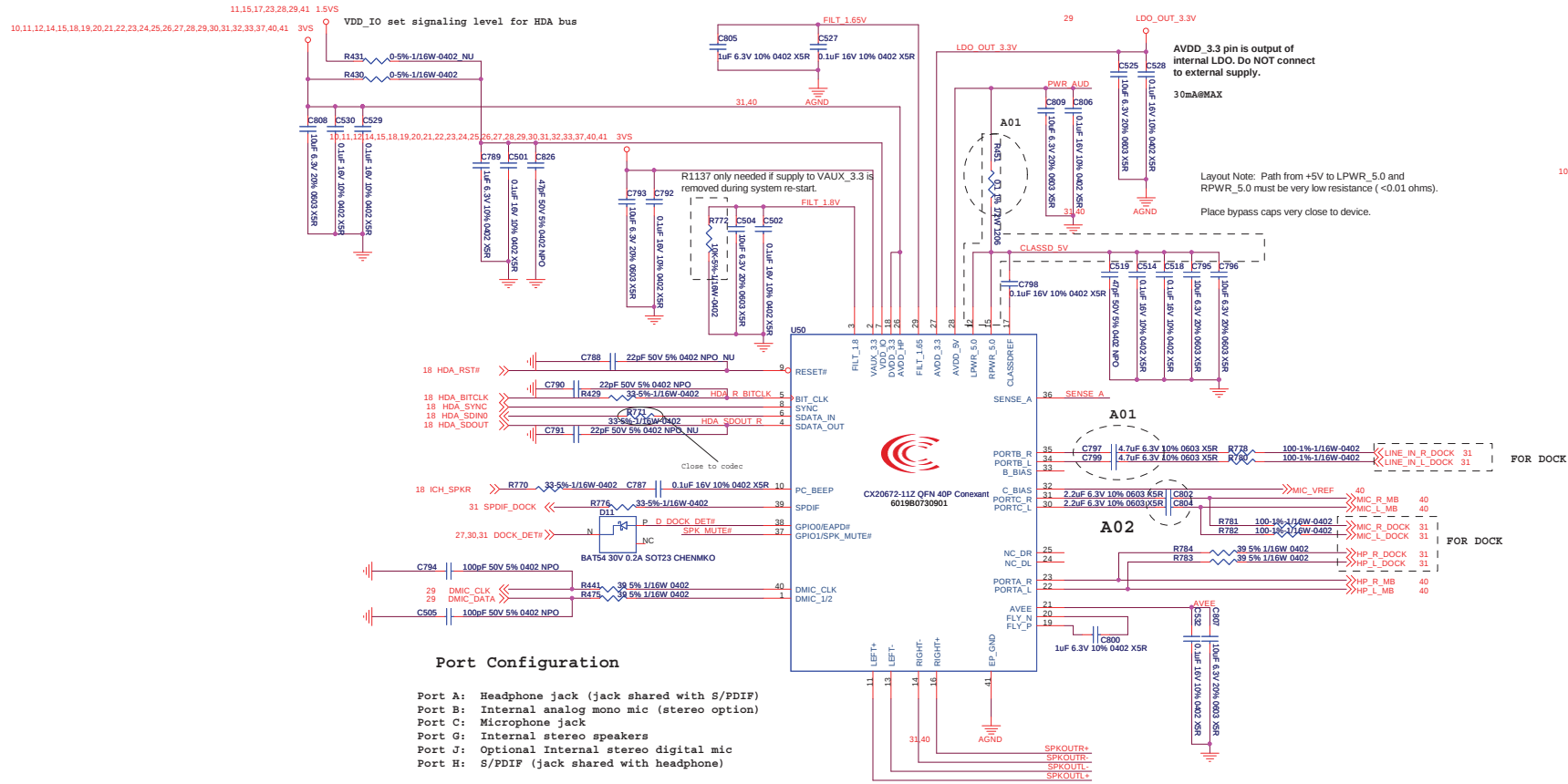
GPIO5	NVVDD	N11M-GE1
0	0.85V	P12APB-State
1	1.032V	PD-State

INVENTEC
TITLE Celpalla demo board)
1.8V/PEX1.1V/NVVDD(5/5)
SIZE CODE DOC NUMBER REV
Custom CS CS-131 of 41
CHANGE by IEC DATE Monday, May 24, 2010 SHEET 37 of 41



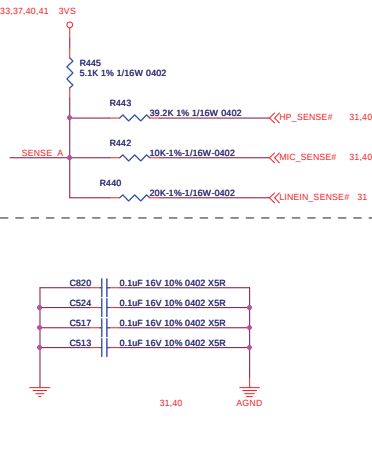
Note:
To support Wake-on-Jack, the CODEC VAUX_3.3 pins must be powered by a Standby supply.

AUDIO CODEC

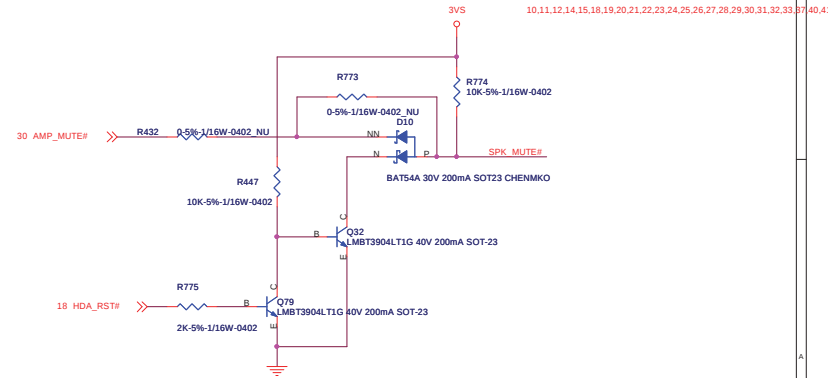
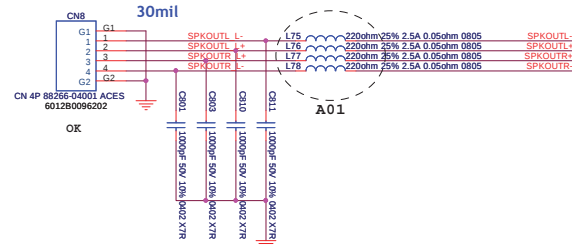


Port Configuration

Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal analog mono mic (stereo option)
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Optional Internal stereo digital mic
Port H: S/PDIF (jack shared with headphone)



SPEAKER



INVENTEC			
TITLE			
Celpalla demo board)			
Audio Codec /AMP			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	CS-131	X01
SHEET	39	of	41

CHANGE by	<CHANGE by>	DATE	Monday, May 24, 2010
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