ZC1 SYSTEM BLOCK DIAGRAM

EV@: Stuff when external VGA used
SH@: Stuff when SATA HDD used
PH@: Stuff when PATA HDD used

X'TAL 14.318MHZ
Clock Generator
ICS954310BGLF P2

Yonah/Merom 479
uFCPGA P3,P4

CPU Thermal Sensor P5

533/667 MHZ FSB

DVI P25
TVOUT P25
TFT LCD Panel 15.4" WSXGA+ P25
CRT P26

VRAM X 4(GDDR3) 256MB/500MHZ P23

DVI
TVout
LVDS
VGA

VGA ATI M56P
P18,P19,P20,P21,P22,P24

X'TAL 27M

PCI-Express 16X Lan

CALISTOGA-945PM
1466
FCBGA
P6,P7,P8,P9,P10,P11

Dual Channel DDR2
533/667 Mhz

DDR II SODIMM0
DDR II SODIMM1
P12,P13

EZ4 Docking Connector
PCIE1~2 , Lan
Ser & Par Port
PS2 , VGA, DVI
SPDIF,SM BUS
P32

PCI-Express X 2
TV out / CRT → Switch P25,26
Audio → Switch P37
DVI
10/100/1G → Switch MAX4892 P25,P28

DMI X4 interface

HDD P35
SATA

MiniCard / WLAN P29
USB5
New Card P33

ICH7-M Digital Home
652 BGA
P14,P15,P16,P17

PCI-Express

Bluetooth USB6 P29
Media-Bay ODD/2nd HDD/2nd Battery P35
Camera Module(1.3M) USB7 P25
6 in 1 Cardreader (SMSC 2228) USB4 P31
USB Port x 4 USB0~3 P29
X'TAL 6M

USB 2.0

PCI Bus interface

X'TAL24.576MHZ
X'TAL 25M

PCMCIA+1394 +Cardreader Controller
O2 711MP1
P30,P31
OSC 48MHZ

Intel Tekoa GigaLAN
82573E P27

SPI FLASH P27
Transformer P28
RJ45 P28

SMBUS
G-SENSOR P35
X'TAL 32.768KHZ

Int MIC P37
Azalia Audio Controller Realtek ALC883 P36
Azalia
Audio Amplifier Maxim Max 9750 P37

LPC
X'TAL 32.768K
KBC PC97551 P39

IEEE 1394 Port P31
Smart card P30
PCMCIA Slot P30
Fan Header P5

Primary Battery
Secod Battery
P45,P46

MIC Jack P37
Line in P37

BIOS P39
G sensor P35

Speaker P37
Phone Jack P37
Azalia MDC P36
RJ11 P28

Touch Pad (Dual-Point) P40

Super I/O NS PC87383 P38
FIR P38
TPM 1.2 P38 (Option)

PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A
Date: Monday, November 07, 2005	Sheet 1 of 46	

FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	
0	0	1	133	100	33	Default
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	200	100	33	

A1A-change X1,X2 capacitor from 27pf to 33pf(CL=20pf)

Close to IC <500mils

Place these termination to close CK410M.

CK-410M

U46

ICS954310BGLF

A1A:Remove PCIE clock

A1A:Change pin 3 PCLK_LAN to PCLK_TPM

25 mils

25 mils

PREQ3(PCIE) Latched Select
"0" : CLK Enable
"1" : CLK Disable Control : PCIE 2,4,6,8

PREQ4(PCIE) Latched Select
"0" : CLK Enable
"1" : CLK Disable Control : PCIE 1,3,5,7

A1A-FSB Frequency Select:by CPU driven

swap

ITP/SRC7 SELECT
0: SRC7 1: ITP

Latched Select. (Pin 17,18)
"0" : LCD CLK(UMA)
"1" : PCIEX CLK(M56)

Latched Select. (Pin 40,41)
"0" : PCIEX CLK
"1" : PEREQ#

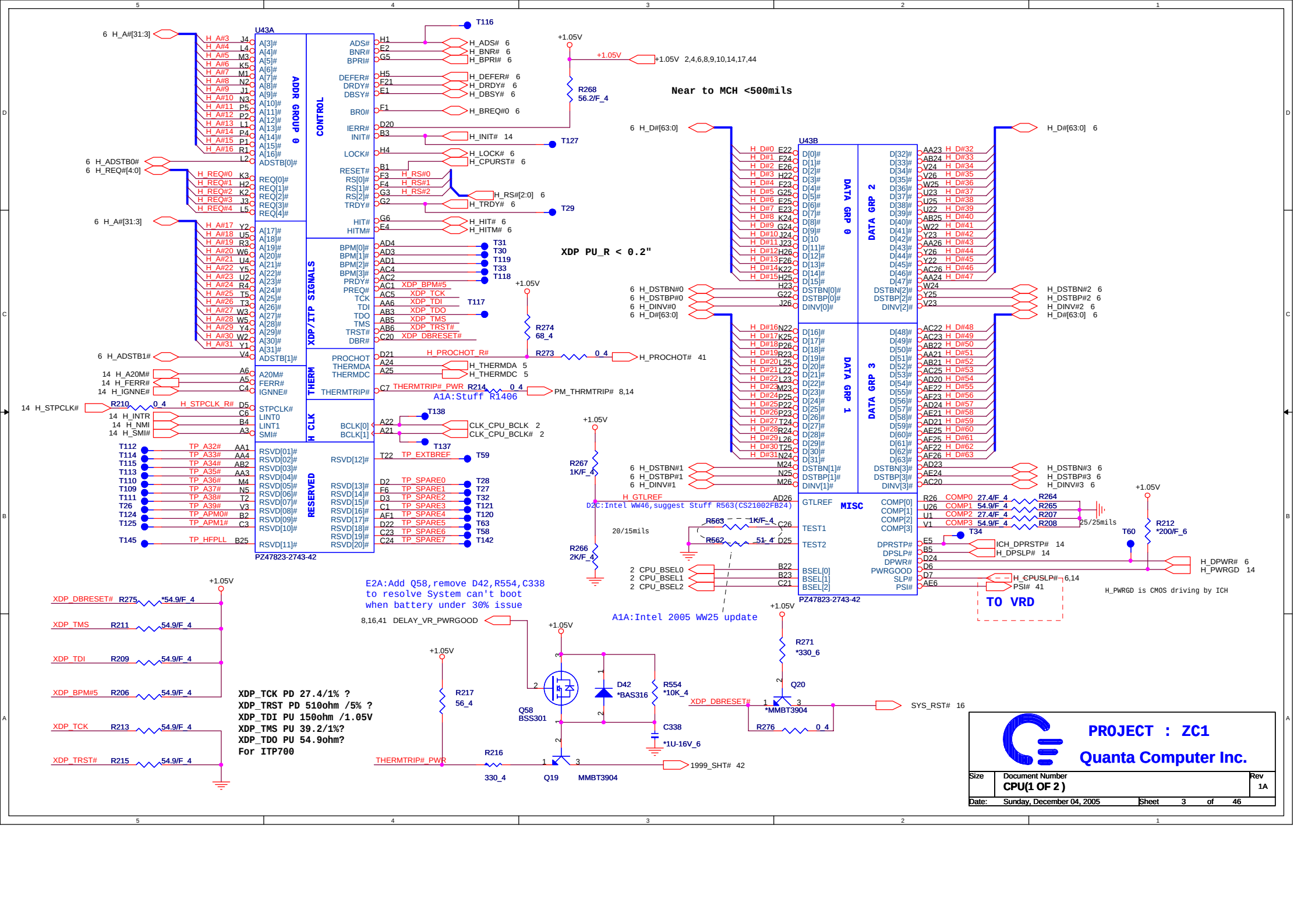
SELLCD_27# Select. (Pin 17,18)
"0" : 27MHzSS/27MHzSS# pair
"1" : LCD CLK pair

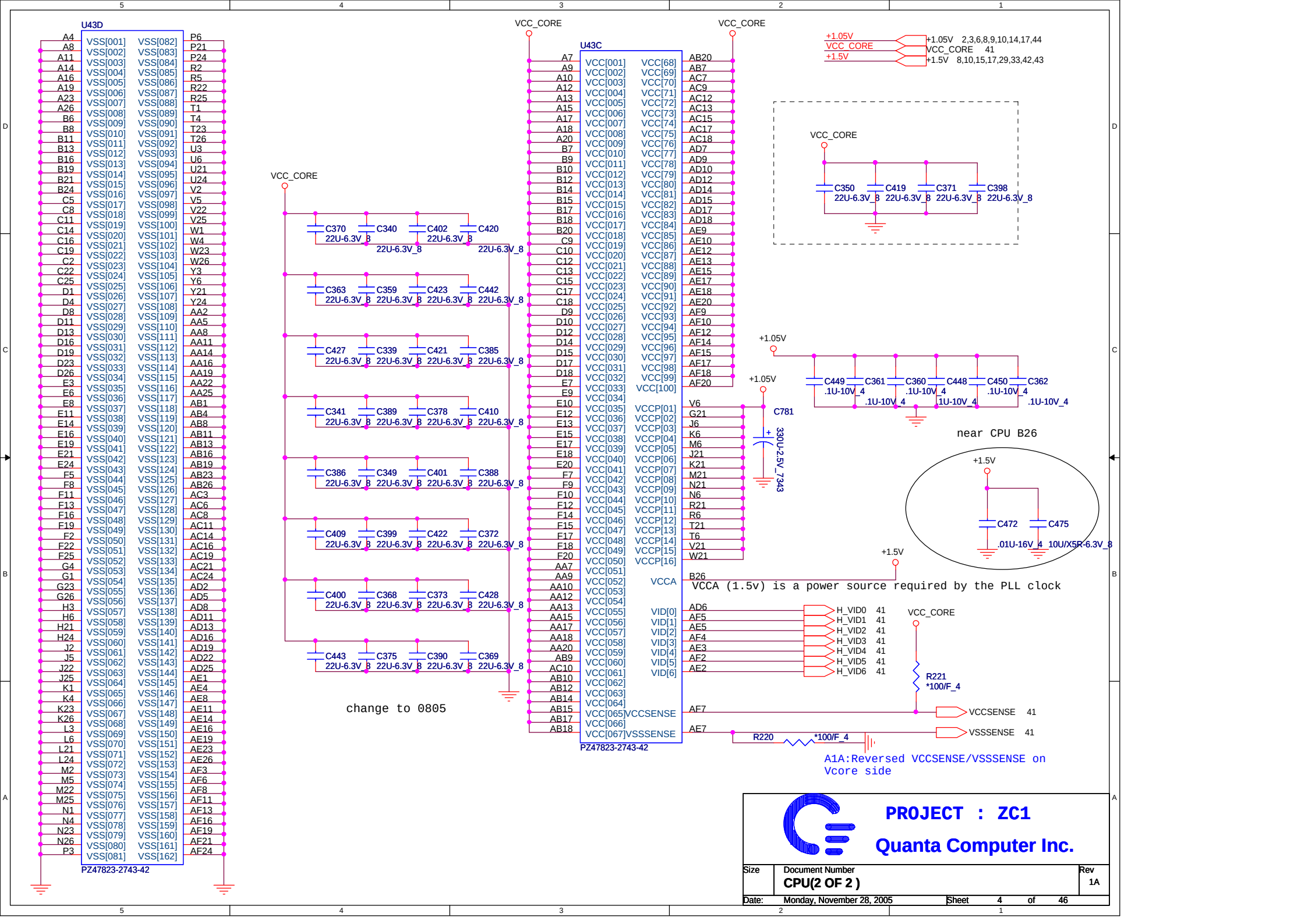
Stuff 0 ohm for 533MHz, NC for 667MHz

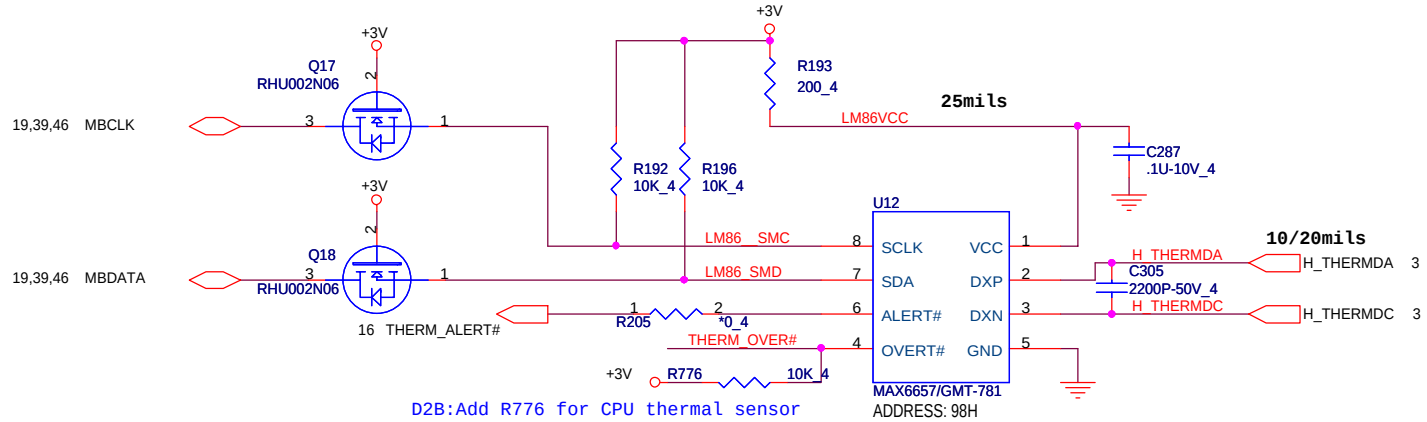
PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date: Friday, December 09, 2005	Sheet 2 of 46	

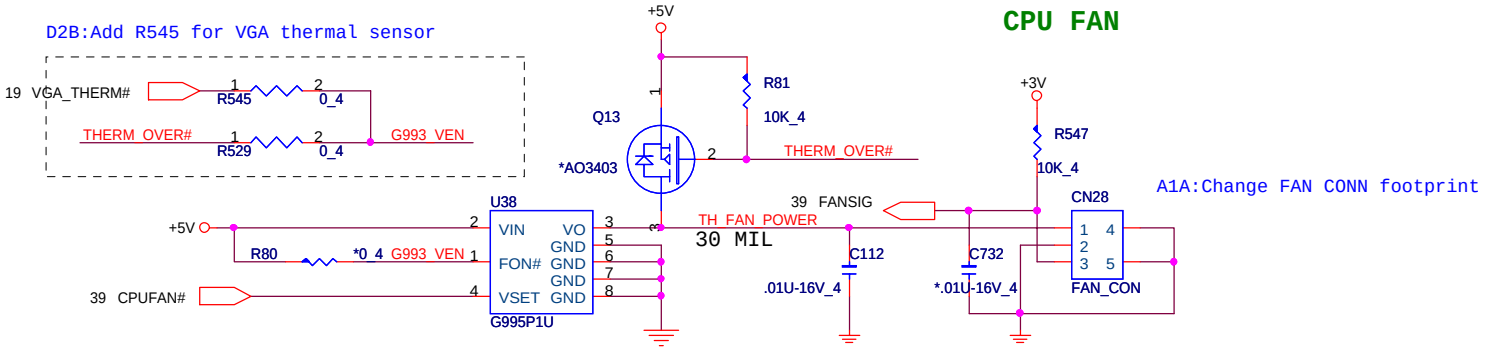

U43A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
PZ47823-2743-42
U43B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
PZ47823-2743-42
Near to MCH <500mils
XDP PU_R < 0.2"
A1A:Stuff R1406
D2C:Intel WW46,suggest Stuff R563(CS21002FB24)
A1A:Intel 2005 WW25 update
E2A:Add Q58,remove D42,R554,C338
to resolve System can't boot
when battery under 30% issue
TO VRD
H_PWRGD is CMOS driving by ICH
XDP_TCK PD 27.4/1% ?
XDP_TRST PD 510ohm /5% ?
XDP_TDI PU 150ohm /1.05V
XDP_TMS PU 39.2/1%?
XDP_TDO PU 54.9ohm?
For ITP700
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
CPU(1 OF 2)
Rev
1A
Date: Sunday, December 04, 2005
Sheet 3 of 46


U43D
PZ47823-2743-42
U43C
PZ47823-2743-42
VCC_CORE
+1.05V
+1.5V
+1.05V 2,3,6,8,9,10,14,17,44
VCC_CORE 41
+1.5V 8,10,15,17,29,33,42,43
C350 C419 C371 C398
22U-6.3V_8
C370 C340 C402 C420
C363 C359 C423 C442
C427 C339 C421 C385
C341 C389 C378 C410
C386 C349 C401 C388
C409 C399 C422 C372
C400 C368 C373 C428
C443 C375 C390 C369
change to 0805
C449 C361 C360 C448 C450 C362
.1U-10V_4
near CPU B26
C781
330U-2.5V_7343
C472 C475
.01U-16V_4 10U/X5R-6.3V_8
VCCA (1.5v) is a power source required by the PLL clock
H_VID0 41
H_VID1 41
H_VID2 41
H_VID3 41
H_VID4 41
H_VID5 41
H_VID6 41
R221
*100/F_4
VCCSENSE 41
VSSSENSE 41
R220
*100/F_4
A1A:Reversed VCCSENSE/VSSSENSE on Vcore side
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
CPU(2 OF 2)
Rev
1A
Date: Monday, November 28, 2005
Sheet 4 of 46



D2B:Add R776 for CPU thermal sensor

D2B:Add R545 for VGA thermal sensor



CPU FAN

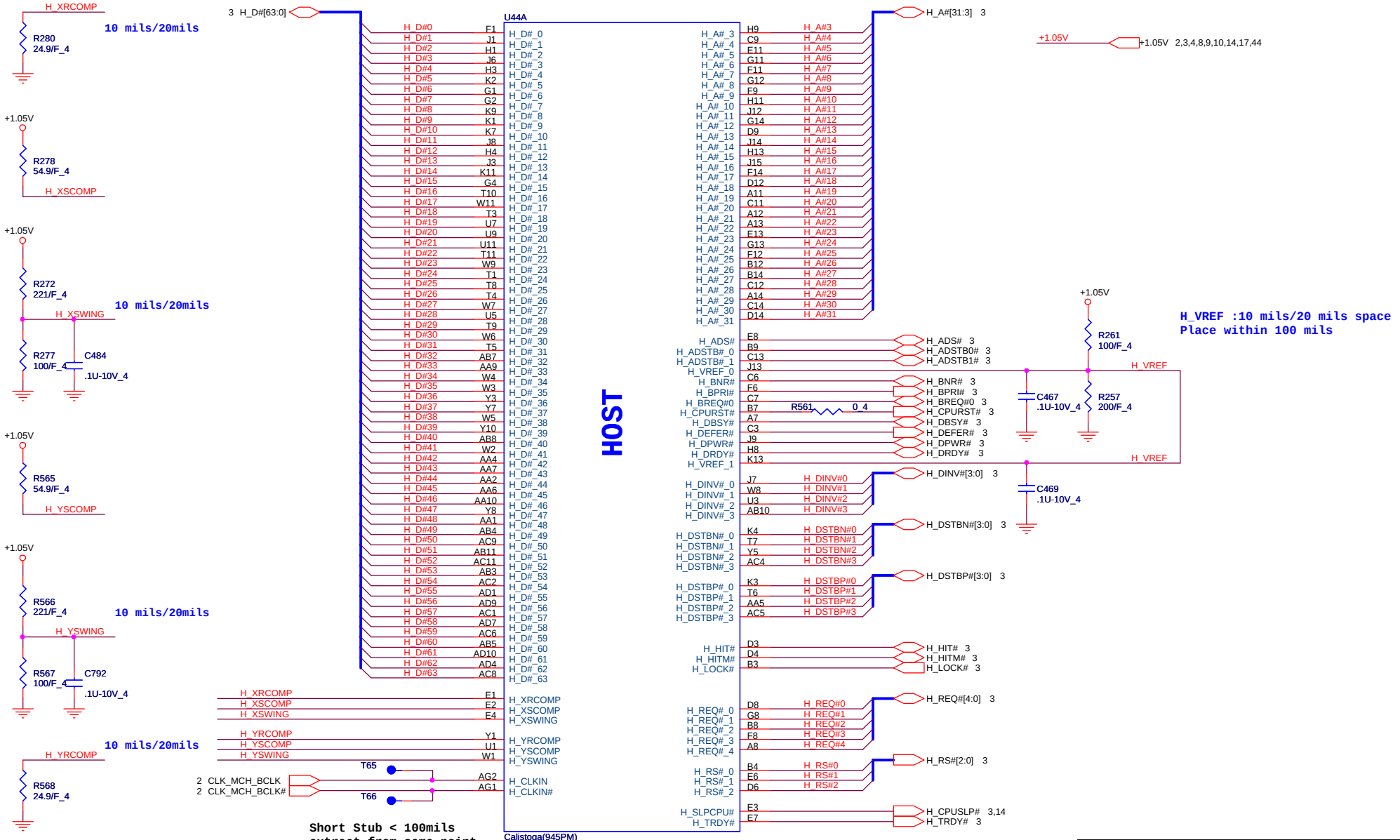
A1A:Change FAN CONN footprint

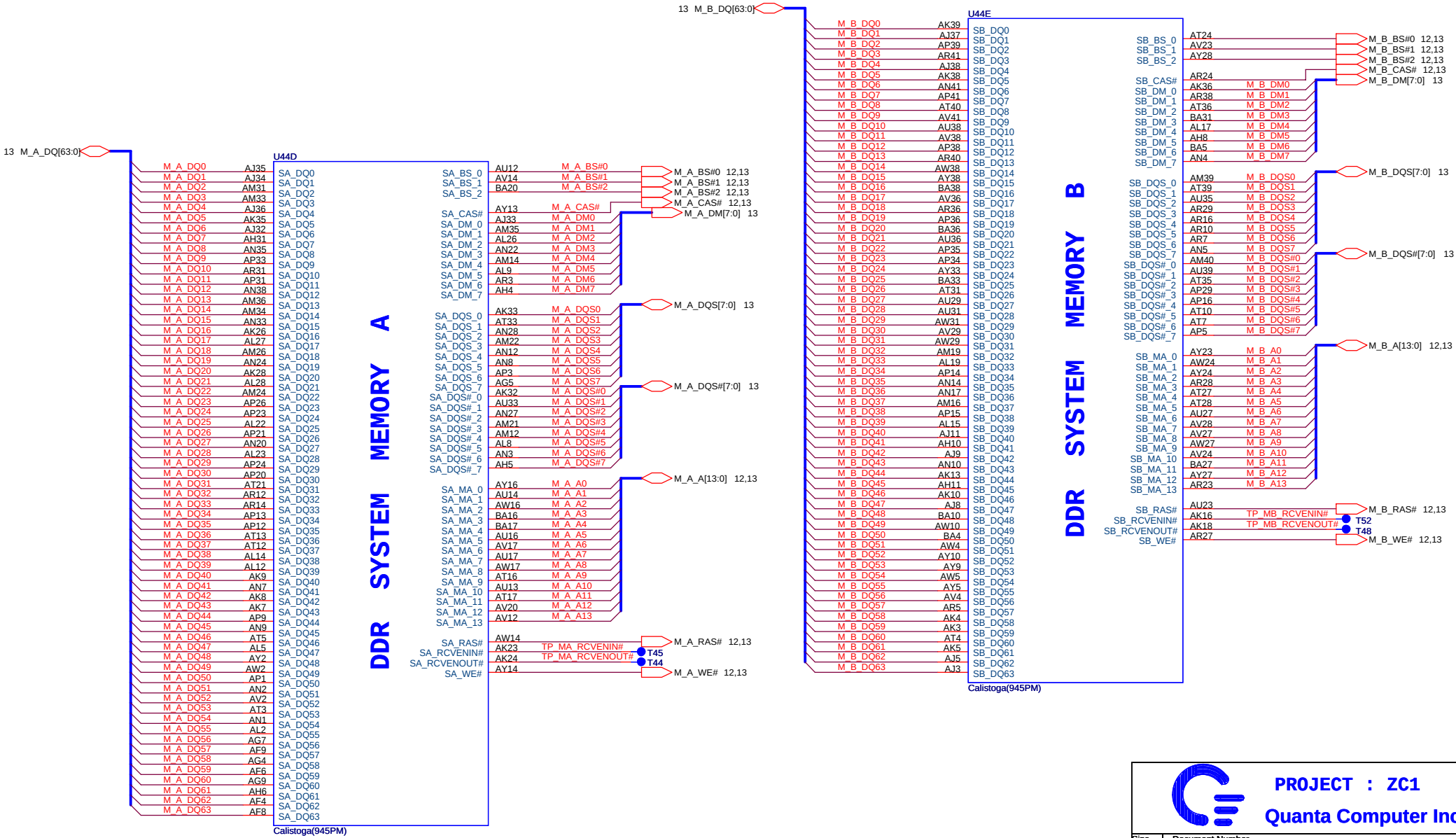
A1A:Change FAN driver to G995

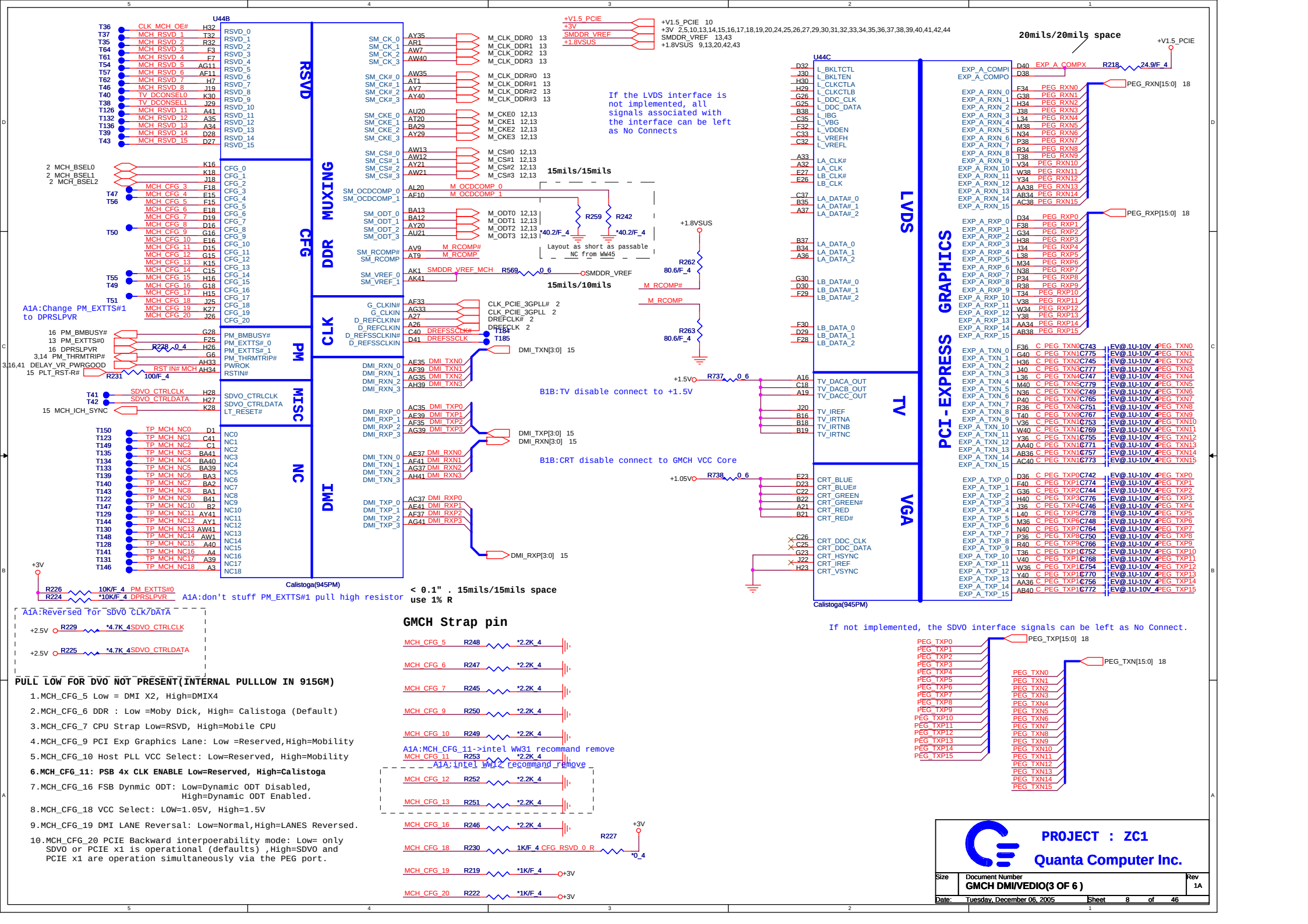
F3B:Add R793,C974 to prevent FAN noise

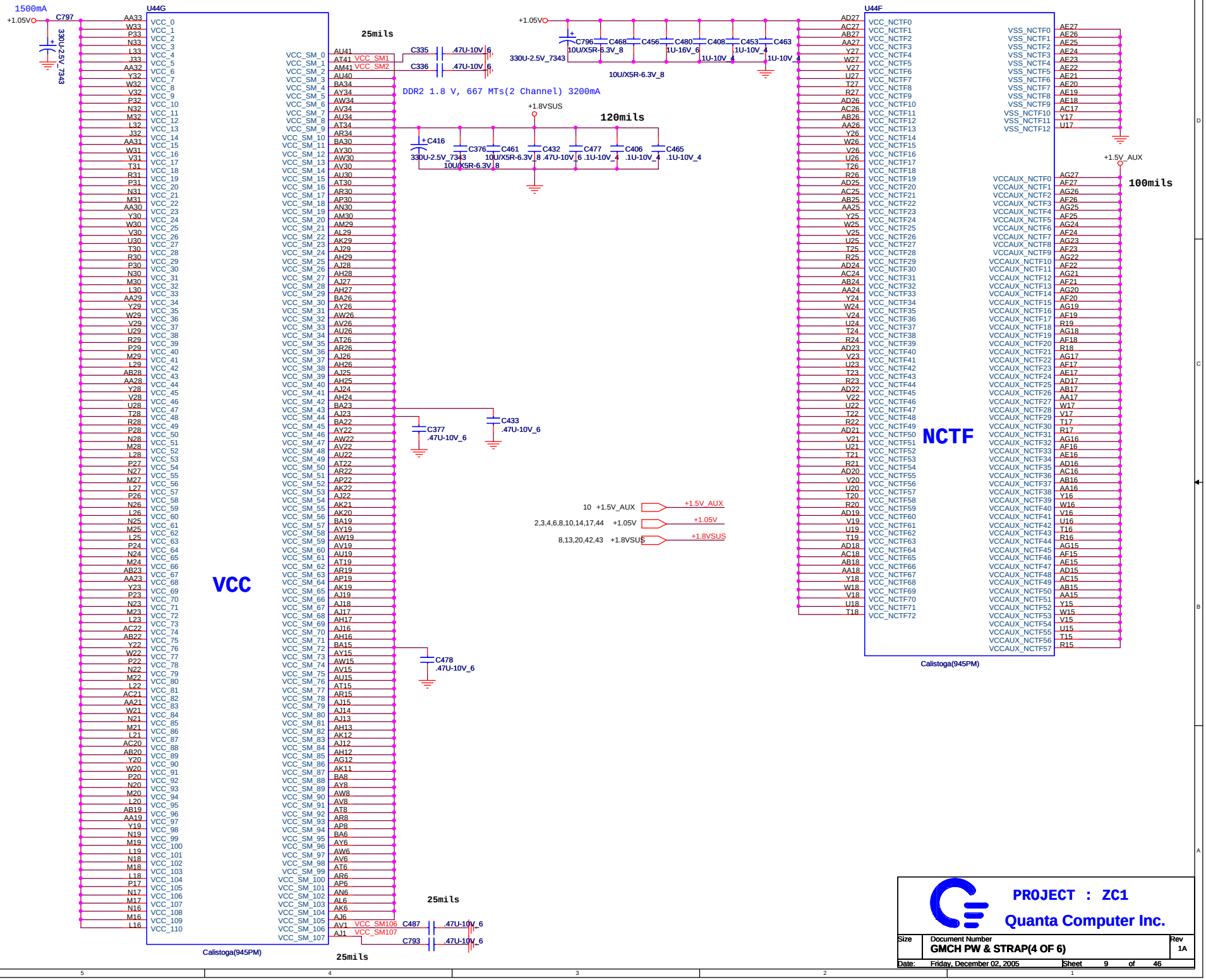
A1A:Remove FANSIG capacitor

PROJECT : ZC1		
Quanta Computer Inc.		
Size	Document Number: Thermal Sensor,FAN	Rev: 1A
Date: Friday, December 02, 2005	Sheet 5 of 46	


H_XRCOMP
10 mils/20mils
R280
24.9/F_4
+1.05V
R278
54.9/F_4
H_XSCOMP
+1.05V
R272
221/F_4
10 mils/20mils
H_XSWING
R277
100/F_4
C484
.1U-10V_4
+1.05V
R565
54.9/F_4
H_YSCOMP
+1.05V
R566
221/F_4
10 mils/20mils
H_YSWING
R567
100/F_4
C792
.1U-10V_4
10 mils/20mils
H_YRCOMP
R568
24.9/F_4
3 H_D#[63:0]
U44A
HOST
H_D#0 F1
H_D#1 J1
H_D#2 H1
H_D#3 J6
H_D#4 H3
H_D#5 K2
H_D#6 G1
H_D#7 G2
H_D#8 K9
H_D#9 K1
H_D#10 K7
H_D#11 J8
H_D#12 H4
H_D#13 J3
H_D#14 K11
H_D#15 G4
H_D#16 T10
H_D#17 W11
H_D#18 T3
H_D#19 U7
H_D#20 U9
H_D#21 U11
H_D#22 T11
H_D#23 W9
H_D#24 T1
H_D#25 T8
H_D#26 T4
H_D#27 W7
H_D#28 U5
H_D#29 T9
H_D#30 W6
H_D#31 T5
H_D#32 AB7
H_D#33 AA9
H_D#34 W4
H_D#35 W3
H_D#36 Y3
H_D#37 Y7
H_D#38 W5
H_D#39 Y10
H_D#40 AB8
H_D#41 W2
H_D#42 AA4
H_D#43 AA7
H_D#44 AA2
H_D#45 AA6
H_D#46 AA10
H_D#47 Y8
H_D#48 AA1
H_D#49 AB4
H_D#50 AC9
H_D#51 AB11
H_D#52 AC11
H_D#53 AB3
H_D#54 AC2
H_D#55 AD1
H_D#56 AD9
H_D#57 AC1
H_D#58 AD7
H_D#59 AC6
H_D#60 AB5
H_D#61 AD10
H_D#62 AD4
H_D#63 AC8
H_XRCOMP E1
H_XSCOMP E2
H_XSWING E4
H_YRCOMP Y1
H_YSCOMP U1
H_YSWING W1
T65
T66
2 CLK_MCH_BCLK
2 CLK_MCH_BCLK#
AG2
AG1
H_CLKIN
H_CLKIN#
Short Stub < 100mils
extract from same point
H_A#_3 H9
H_A#_4 C9
H_A#_5 E11
H_A#_6 G11
H_A#_7 F11
H_A#_8 G12
H_A#_9 F9
H_A#_10 H11
H_A#_11 J12
H_A#_12 G14
H_A#_13 D9
H_A#_14 J14
H_A#_15 H13
H_A#_16 J15
H_A#_17 F14
H_A#_18 D12
H_A#_19 A11
H_A#_20 C11
H_A#_21 A12
H_A#_22 A13
H_A#_23 E13
H_A#_24 G13
H_A#_25 F12
H_A#_26 B12
H_A#_27 B14
H_A#_28 C12
H_A#_29 A14
H_A#_30 C14
H_A#_31 D14
H_A#3
H_A#4
H_A#5
H_A#6
H_A#7
H_A#8
H_A#9
H_A#10
H_A#11
H_A#12
H_A#13
H_A#14
H_A#15
H_A#16
H_A#17
H_A#18
H_A#19
H_A#20
H_A#21
H_A#22
H_A#23
H_A#24
H_A#25
H_A#26
H_A#27
H_A#28
H_A#29
H_A#30
H_A#31
H_A#[31:3] 3
+1.05V
+1.05V 2,3,4,8,9,10,14,17,44
H_ADS# E8
H_ADSTB#_0 B9
H_ADSTB#_1 C13
H_VREF_0 J13
H_BNR# C6
H_BPRI# F6
H_BREQ#0 C7
H_CPURST# B7
H_DBSY# A7
H_DEFER# C3
H_DPWR# J9
H_DRDY# H8
H_VREF_1 K13
H_ADS# 3
H_ADSTB0# 3
H_ADSTB1# 3
H_BNR# 3
H_BPRI# 3
H_BREQ#0 3
H_CPURST# 3
H_DBSY# 3
H_DEFER# 3
H_DPWR# 3
H_DRDY# 3
R561 0_4
+1.05V
R261
100/F_4
H_VREF
C467
.1U-10V_4
R257
200/F_4
H_VREF
C469
.1U-10V_4
H_VREF :10 mils/20 mils space
Place within 100 mils
H_DINV#_0 J7
H_DINV#_1 W8
H_DINV#_2 U3
H_DINV#_3 AB10
H_DINV#0
H_DINV#1
H_DINV#2
H_DINV#3
H_DINV#[3:0] 3
H_DSTBN#_0 K4
H_DSTBN#_1 T7
H_DSTBN#_2 Y5
H_DSTBN#_3 AC4
H_DSTBN#0
H_DSTBN#1
H_DSTBN#2
H_DSTBN#3
H_DSTBN#[3:0] 3
H_DSTBP#_0 K3
H_DSTBP#_1 T6
H_DSTBP#_2 AA5
H_DSTBP#_3 AC5
H_DSTBP#0
H_DSTBP#1
H_DSTBP#2
H_DSTBP#3
H_DSTBP#[3:0] 3
H_HIT# D3
H_HITM# D4
H_LOCK# B3
H_HIT# 3
H_HITM# 3
H_LOCK# 3
H_REQ#_0 D8
H_REQ#_1 G8
H_REQ#_2 B8
H_REQ#_3 F8
H_REQ#_4 A8
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
H_REQ#[4:0] 3
H_RS#_0 B4
H_RS#_1 E6
H_RS#_2 D6
H_RS#0
H_RS#1
H_RS#2
H_RS#[2:0] 3
H_SLPCPU# E3
H_TRDY# E7
H_CPUSLP# 3,14
H_TRDY# 3
Calistoga(945PM)
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
GMCH HOST(1 OF 6)
Rev
1A
Date: Friday, December 02, 2005
Sheet 6 of 46


13 M_A_DQ[63:0]
U44D
DDR SYSTEM MEMORY A
Calistoga(945PM)
M_A_DQ0 AJ35
M_A_DQ1 AJ34
M_A_DQ2 AM31
M_A_DQ3 AM33
M_A_DQ4 AJ36
M_A_DQ5 AK35
M_A_DQ6 AJ32
M_A_DQ7 AH31
M_A_DQ8 AN35
M_A_DQ9 AP33
M_A_DQ10 AR31
M_A_DQ11 AP31
M_A_DQ12 AN38
M_A_DQ13 AM36
M_A_DQ14 AM34
M_A_DQ15 AN33
M_A_DQ16 AK26
M_A_DQ17 AL27
M_A_DQ18 AM26
M_A_DQ19 AN24
M_A_DQ20 AK28
M_A_DQ21 AL28
M_A_DQ22 AM24
M_A_DQ23 AP26
M_A_DQ24 AP23
M_A_DQ25 AL22
M_A_DQ26 AP21
M_A_DQ27 AN20
M_A_DQ28 AL23
M_A_DQ29 AP24
M_A_DQ30 AP20
M_A_DQ31 AT21
M_A_DQ32 AR12
M_A_DQ33 AR14
M_A_DQ34 AP13
M_A_DQ35 AP12
M_A_DQ36 AT13
M_A_DQ37 AT12
M_A_DQ38 AL14
M_A_DQ39 AL12
M_A_DQ40 AK9
M_A_DQ41 AN7
M_A_DQ42 AK8
M_A_DQ43 AK7
M_A_DQ44 AP9
M_A_DQ45 AN9
M_A_DQ46 AT5
M_A_DQ47 AL5
M_A_DQ48 AY2
M_A_DQ49 AW2
M_A_DQ50 AP1
M_A_DQ51 AN2
M_A_DQ52 AV2
M_A_DQ53 AT3
M_A_DQ54 AN1
M_A_DQ55 AL2
M_A_DQ56 AG7
M_A_DQ57 AF9
M_A_DQ58 AG4
M_A_DQ59 AF6
M_A_DQ60 AG9
M_A_DQ61 AH6
M_A_DQ62 AF4
M_A_DQ63 AF8
SA_DQ0 SA_DQ1 SA_DQ2 SA_DQ3 SA_DQ4 SA_DQ5 SA_DQ6 SA_DQ7 SA_DQ8 SA_DQ9 SA_DQ10 SA_DQ11 SA_DQ12 SA_DQ13 SA_DQ14 SA_DQ15 SA_DQ16 SA_DQ17 SA_DQ18 SA_DQ19 SA_DQ20 SA_DQ21 SA_DQ22 SA_DQ23 SA_DQ24 SA_DQ25 SA_DQ26 SA_DQ27 SA_DQ28 SA_DQ29 SA_DQ30 SA_DQ31 SA_DQ32 SA_DQ33 SA_DQ34 SA_DQ35 SA_DQ36 SA_DQ37 SA_DQ38 SA_DQ39 SA_DQ40 SA_DQ41 SA_DQ42 SA_DQ43 SA_DQ44 SA_DQ45 SA_DQ46 SA_DQ47 SA_DQ48 SA_DQ49 SA_DQ50 SA_DQ51 SA_DQ52 SA_DQ53 SA_DQ54 SA_DQ55 SA_DQ56 SA_DQ57 SA_DQ58 SA_DQ59 SA_DQ60 SA_DQ61 SA_DQ62 SA_DQ63
SA_BS_0 AU12 M_A_BS#0
SA_BS_1 AV14 M_A_BS#1
SA_BS_2 BA20 M_A_BS#2
SA_CAS# AY13 M_A_CAS#
SA_DM_0 AJ33 M_A_DM0
SA_DM_1 AM35 M_A_DM1
SA_DM_2 AL26 M_A_DM2
SA_DM_3 AN22 M_A_DM3
SA_DM_4 AM14 M_A_DM4
SA_DM_5 AL9 M_A_DM5
SA_DM_6 AR3 M_A_DM6
SA_DM_7 AH4 M_A_DM7
SA_DQS_0 AK33 M_A_DQS0
SA_DQS_1 AT33 M_A_DQS1
SA_DQS_2 AN28 M_A_DQS2
SA_DQS_3 AM22 M_A_DQS3
SA_DQS_4 AN12 M_A_DQS4
SA_DQS_5 AN8 M_A_DQS5
SA_DQS_6 AP3 M_A_DQS6
SA_DQS_7 AG5 M_A_DQS7
SA_DQS#_0 AK32 M_A_DQS#0
SA_DQS#_1 AU33 M_A_DQS#1
SA_DQS#_2 AN27 M_A_DQS#2
SA_DQS#_3 AM21 M_A_DQS#3
SA_DQS#_4 AM12 M_A_DQS#4
SA_DQS#_5 AL8 M_A_DQS#5
SA_DQS#_6 AN3 M_A_DQS#6
SA_DQS#_7 AH5 M_A_DQS#7
SA_MA_0 AY16 M_A_A0
SA_MA_1 AU14 M_A_A1
SA_MA_2 AW16 M_A_A2
SA_MA_3 BA16 M_A_A3
SA_MA_4 BA17 M_A_A4
SA_MA_5 AU16 M_A_A5
SA_MA_6 AV17 M_A_A6
SA_MA_7 AU17 M_A_A7
SA_MA_8 AW17 M_A_A8
SA_MA_9 AT16 M_A_A9
SA_MA_10 AU13 M_A_A10
SA_MA_11 AT17 M_A_A11
SA_MA_12 AV20 M_A_A12
SA_MA_13 AV12 M_A_A13
SA_RAS# AW14
SA_RCVENIN# AK23 TP_MA_RCVENIN#
SA_RCVENOUT# AK24 TP_MA_RCVENOUT#
SA_WE# AY14
T45
T44
M_A_BS#0 12,13
M_A_BS#1 12,13
M_A_BS#2 12,13
M_A_CAS# 12,13
M_A_DM[7:0] 13
M_A_DQS[7:0] 13
M_A_DQS#[7:0] 13
M_A_A[13:0] 12,13
M_A_RAS# 12,13
M_A_WE# 12,13
13 M_B_DQ[63:0]
U44E
DDR SYSTEM MEMORY B
Calistoga(945PM)
M_B_DQ0 AK39
M_B_DQ1 AJ37
M_B_DQ2 AP39
M_B_DQ3 AR41
M_B_DQ4 AJ38
M_B_DQ5 AK38
M_B_DQ6 AN41
M_B_DQ7 AP41
M_B_DQ8 AT40
M_B_DQ9 AV41
M_B_DQ10 AU38
M_B_DQ11 AV38
M_B_DQ12 AP38
M_B_DQ13 AR40
M_B_DQ14 AW38
M_B_DQ15 AY38
M_B_DQ16 BA38
M_B_DQ17 AV36
M_B_DQ18 AR36
M_B_DQ19 AP36
M_B_DQ20 BA36
M_B_DQ21 AU36
M_B_DQ22 AP35
M_B_DQ23 AP34
M_B_DQ24 AY33
M_B_DQ25 BA33
M_B_DQ26 AT31
M_B_DQ27 AU29
M_B_DQ28 AU31
M_B_DQ29 AW31
M_B_DQ30 AV29
M_B_DQ31 AW29
M_B_DQ32 AM19
M_B_DQ33 AL19
M_B_DQ34 AP14
M_B_DQ35 AN14
M_B_DQ36 AN17
M_B_DQ37 AM16
M_B_DQ38 AP15
M_B_DQ39 AL15
M_B_DQ40 AJ11
M_B_DQ41 AH10
M_B_DQ42 AJ9
M_B_DQ43 AN10
M_B_DQ44 AK13
M_B_DQ45 AH11
M_B_DQ46 AK10
M_B_DQ47 AJ8
M_B_DQ48 BA10
M_B_DQ49 AW10
M_B_DQ50 BA4
M_B_DQ51 AW4
M_B_DQ52 AY10
M_B_DQ53 AY9
M_B_DQ54 AW5
M_B_DQ55 AY5
M_B_DQ56 AV4
M_B_DQ57 AR5
M_B_DQ58 AK4
M_B_DQ59 AK3
M_B_DQ60 AT4
M_B_DQ61 AK5
M_B_DQ62 AJ5
M_B_DQ63 AJ3
SB_DQ0 SB_DQ1 SB_DQ2 SB_DQ3 SB_DQ4 SB_DQ5 SB_DQ6 SB_DQ7 SB_DQ8 SB_DQ9 SB_DQ10 SB_DQ11 SB_DQ12 SB_DQ13 SB_DQ14 SB_DQ15 SB_DQ16 SB_DQ17 SB_DQ18 SB_DQ19 SB_DQ20 SB_DQ21 SB_DQ22 SB_DQ23 SB_DQ24 SB_DQ25 SB_DQ26 SB_DQ27 SB_DQ28 SB_DQ29 SB_DQ30 SB_DQ31 SB_DQ32 SB_DQ33 SB_DQ34 SB_DQ35 SB_DQ36 SB_DQ37 SB_DQ38 SB_DQ39 SB_DQ40 SB_DQ41 SB_DQ42 SB_DQ43 SB_DQ44 SB_DQ45 SB_DQ46 SB_DQ47 SB_DQ48 SB_DQ49 SB_DQ50 SB_DQ51 SB_DQ52 SB_DQ53 SB_DQ54 SB_DQ55 SB_DQ56 SB_DQ57 SB_DQ58 SB_DQ59 SB_DQ60 SB_DQ61 SB_DQ62 SB_DQ63
SB_BS_0 AT24 M_B_BS#0
SB_BS_1 AV23 M_B_BS#1
SB_BS_2 AY28 M_B_BS#2
SB_CAS# AR24 M_B_CAS#
SB_DM_0 AK36 M_B_DM0
SB_DM_1 AR38 M_B_DM1
SB_DM_2 AT36 M_B_DM2
SB_DM_3 BA31 M_B_DM3
SB_DM_4 AL17 M_B_DM4
SB_DM_5 AH8 M_B_DM5
SB_DM_6 BA5 M_B_DM6
SB_DM_7 AN4 M_B_DM7
SB_DQS_0 AM39 M_B_DQS0
SB_DQS_1 AT39 M_B_DQS1
SB_DQS_2 AU35 M_B_DQS2
SB_DQS_3 AR29 M_B_DQS3
SB_DQS_4 AR16 M_B_DQS4
SB_DQS_5 AR10 M_B_DQS5
SB_DQS_6 AR7 M_B_DQS6
SB_DQS_7 AN5 M_B_DQS7
SB_DQS#_0 AM40 M_B_DQS#0
SB_DQS#_1 AU39 M_B_DQS#1
SB_DQS#_2 AT35 M_B_DQS#2
SB_DQS#_3 AP29 M_B_DQS#3
SB_DQS#_4 AP16 M_B_DQS#4
SB_DQS#_5 AT10 M_B_DQS#5
SB_DQS#_6 AT7 M_B_DQS#6
SB_DQS#_7 AP5 M_B_DQS#7
SB_MA_0 AY23 M_B_A0
SB_MA_1 AW24 M_B_A1
SB_MA_2 AY24 M_B_A2
SB_MA_3 AR28 M_B_A3
SB_MA_4 AT27 M_B_A4
SB_MA_5 AT28 M_B_A5
SB_MA_6 AU27 M_B_A6
SB_MA_7 AV28 M_B_A7
SB_MA_8 AY27 M_B_A8
SB_MA_9 AW27 M_B_A9
SB_MA_10 AY24 M_B_A10
SB_MA_11 BA27 M_B_A11
SB_MA_12 AY27 M_B_A12
SB_MA_13 AR23 M_B_A13
SB_RAS# AU23
SB_RCVENIN# AK16 TP_MB_RCVENIN#
SB_RCVENOUT# AK18 TP_MB_RCVENOUT#
SB_WE# AR27
T52
T48
M_B_DM[7:0] 13
M_B_DQS[7:0] 13
M_B_DQS#[7:0] 13
M_B_A[13:0] 12,13
M_B_RAS# 12,13
M_B_WE# 12,13
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
GMCH DDR(2 OF 6)
Rev
1A
Date: Friday, December 02, 2005
Sheet 7 of 46


U44B
RSVD
CFG
DDR MUXING
CLK
PM
MISC
NC
DMI
Calistoga(945PM)
U44C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
Calistoga(945PM)
20mils/20mils space
15mils/15mils
15mils/10mils
If the LVDS interface is not implemented, all signals associated with the interface can be left as No Connects
A1A:Change PM_EXTTS#1 to DPRSLPVR
A1A:don't stuff PM_EXTTS#1 pull high resistor
B1B:TV disable connect to +1.5V
B1B:CRT disable connect to GMCH VCC Core
< 0.1" . 15mils/15mils space use 1% R
A1A:Reversed for SDVO CLK/DATA
If not implemented, the SDVO interface signals can be left as No Connect.
GMCH Strap pin
A1A:MCH_CFG_11->intel WW31 recommand remove
A1A:intel WW12 recommand remove
PULL LOW FOR DVO NOT PRESENT(INTERNAL PULLLOW IN 915GM)
1.MCH_CFG_5 Low = DMI X2, High=DMIX4
2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6.MCH_CFG_11: PSB 4x CLK ENABLE Low=Reserved, High=Calistoga
7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
9.MCH_CFG_19 DMI LANE Reversal: Low=Normal,High=LANES Reversed.
10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.
PROJECT : ZC1
Quanta Computer Inc.
GMCH DMI/VEDIO(3 OF 6)
Size
Document Number
Rev 1A
Date: Tuesday, December 06, 2005
Sheet 8 of 46


1500mA
+1.05V
C797
330U-2.5V_7343
U44G
VCC
Calistoga(945PM)
25mils
C335 .47U-10V_6
C336 .47U-10V_6
DDR2 1.8 V, 667 MTs(2 Channel) 3200mA
+1.8VSUS
120mils
C416 330U-2.5V_7343
C376 10U/X5R-6.3V_8
C461 10U/X5R-6.3V_8
C432 .47U-10V_6
C477 .1U-10V_4
C406 .1U-10V_4
C465 .1U-10V_4
C377 .47U-10V_6
C433 .47U-10V_6
C478 .47U-10V_6
25mils
C487 .47U-10V_6
C793 .47U-10V_6
25mils
+1.05V
C796 330U-2.5V_7343
C468 10U/X5R-6.3V_8
C456 10U/X5R-6.3V_8
C480 .1U-16V_6
C408 .1U-10V_4
C453 .1U-10V_4
C463 .1U-10V_4
10U/X5R-6.3V_8
10 +1.5V_AUX
2,3,4,6,8,10,14,17,44 +1.05V
8,13,20,42,43 +1.8VSUS
+1.5V_AUX
+1.05V
+1.8VSUS
U44F
NCTF
Calistoga(945PM)
+1.5V_AUX
100mils
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
GMCH PW & STRAP(4 OF 6)
Rev
1A
Date: Friday, December 02, 2005
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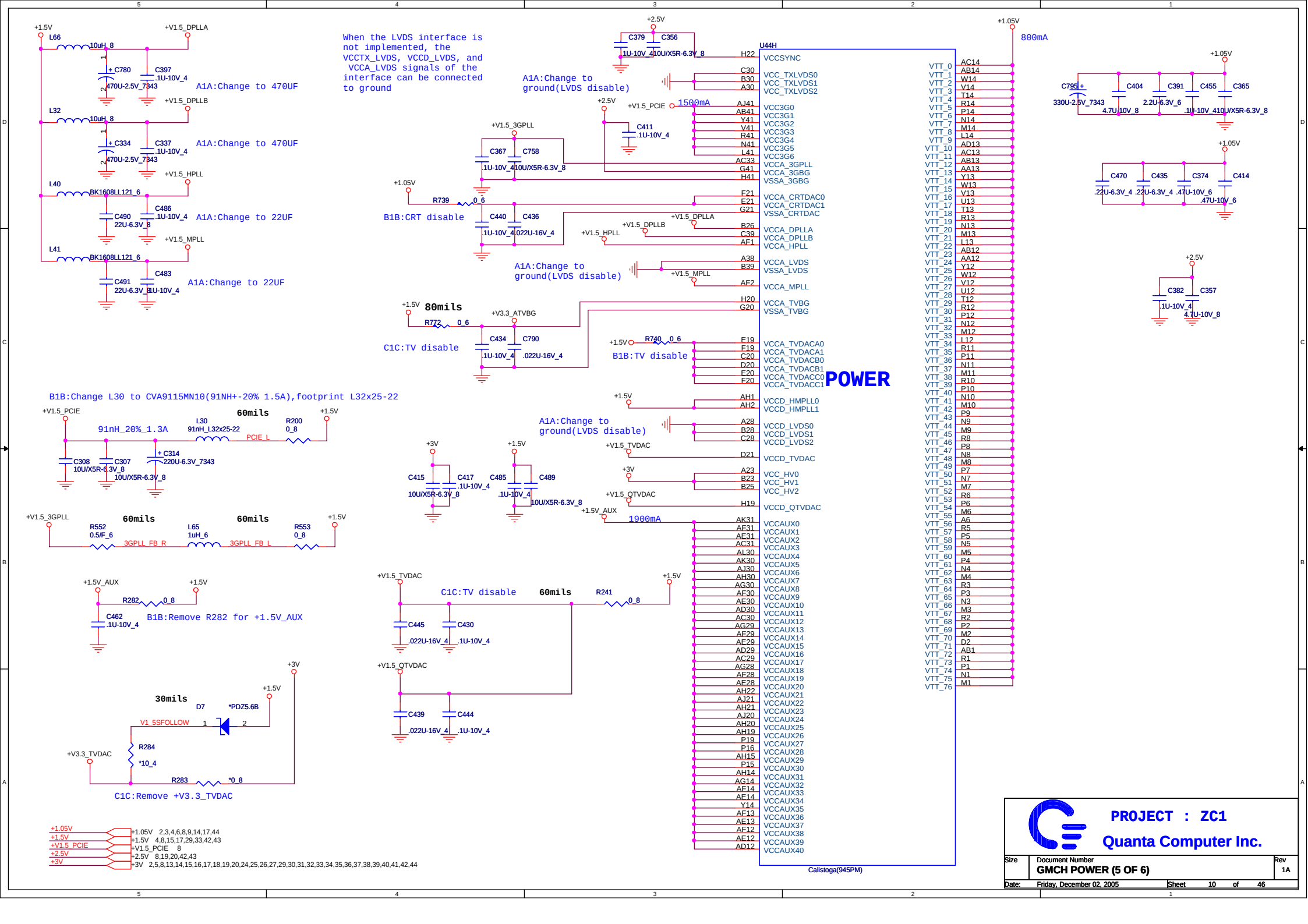
When the LVDS interface is not implemented, the VCCTX_LVDS, VCCD_LVDS, and VCCA_LVDS signals of the interface can be connected to ground
A1A:Change to 470UF
A1A:Change to 470UF
A1A:Change to 22UF
A1A:Change to 22UF
A1A:Change to ground(LVDS disable)
A1A:Change to ground(LVDS disable)
A1A:Change to ground(LVDS disable)
B1B:CRT disable
B1B:TV disable
C1C:TV disable
B1B:Change L30 to CVA9115MN10(91NH+-20% 1.5A),footprint L32x25-22
B1B:Remove R282 for +1.5V_AUX
C1C:TV disable
C1C:Remove +V3.3_TVDAC
U44H
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
VCCA_3GPLL
VCCA_3GBG
VSSA_3GBG
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_LVDS
VSSA_LVDS
VCCA_MPLL
VCCA_TVBG
VSSA_TVBG
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
VCCD_TVDAC
VCC_HV0
VCC_HV1
VCC_HV2
VCCD_QTVDAC
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
Calistoga(945PM)
POWER
800mA
1500mA
1900mA
80mils
60mils
30mils
+1.05V 2,3,4,6,8,9,14,17,44
+1.5V 4,8,15,17,29,33,42,43
+V1.5_PCIE 8
+2.5V 8,19,20,42,43
+3V 2,5,8,13,14,15,16,17,18,19,20,24,25,26,27,29,30,31,32,33,34,35,36,37,38,39,40,41,42,44
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
GMCH POWER (5 OF 6)
Rev
1A
Date: Friday, December 02, 2005
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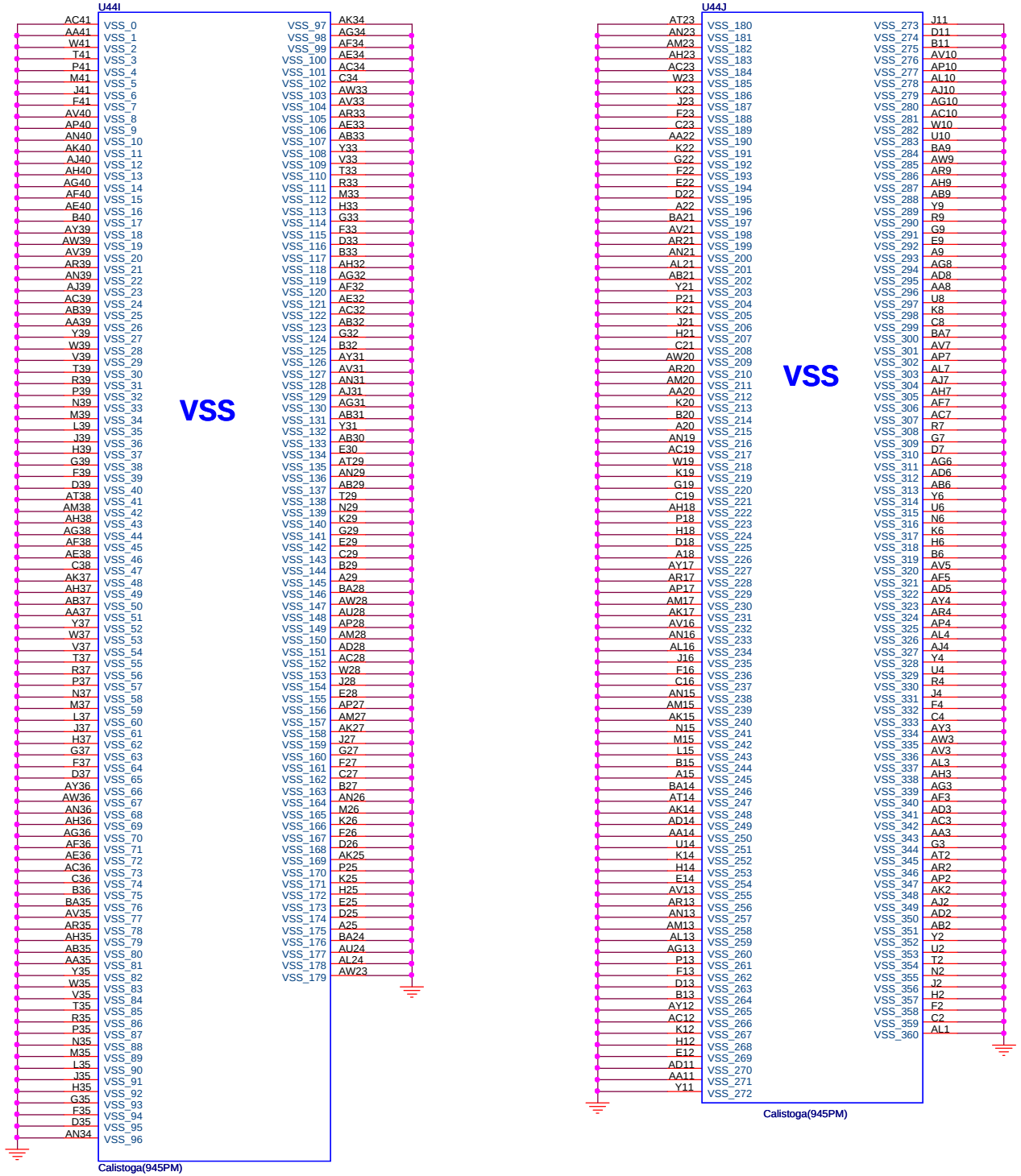


PROJECT : ZC1

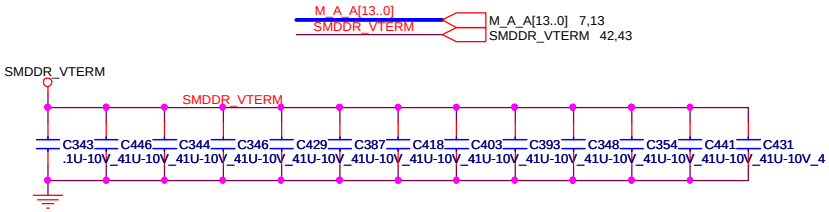
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH GND(6 OF 6)	1A

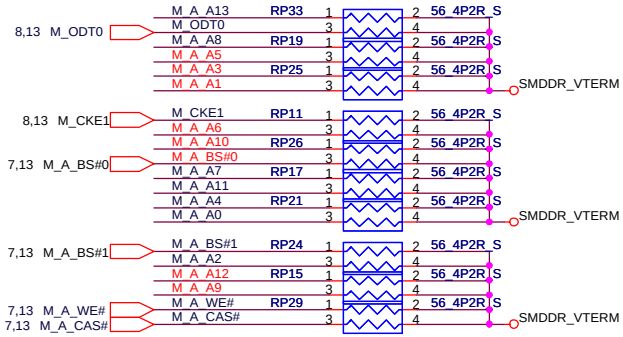
Date: Friday, December 02, 2005 Sheet 11 of 46

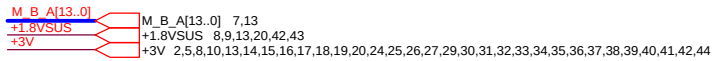
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

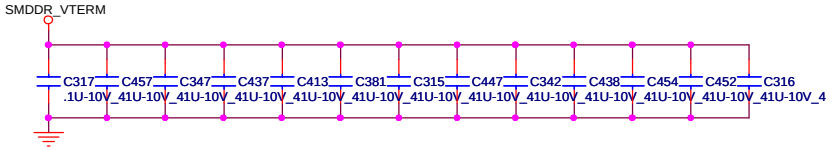


A1A:Swap net



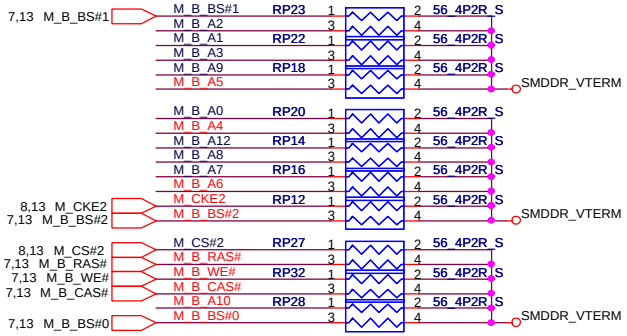


DDRII B CHANNEL

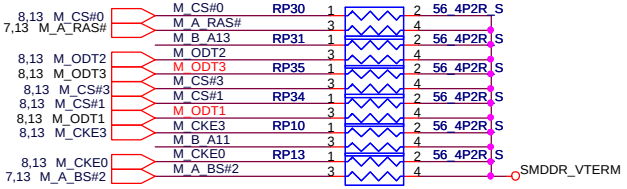


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

A1A:Swap net



A1A:Swap net



PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	DDR RES. ARRAY	1A

Date: Monday, November 28, 2005 Sheet 12 of 46

+3V
+1.8VSUS
+3V 2,5,8,10,14,15,16,17,18,19,20,24,25,26,27,29,30,31,32,33,34,35,36,37,38,39,40,41,42,44
+1.8VSUS 8,9,20,42,43

SMDDR_VREF_DIMM
A1A:Swap net

A1A:Change DDRII footprint to same as CT6

M_A_DM[0..7] 7
M_A_DQ[0..63] 7
M_A_DQS[0..7] 7
M_A_DQS#[0..7] 7
M_A_A[0..13] 7,12

CN31

DDR2_SODIMM(1-1734074-1)

PC4800 DDR2 SDRAM SO-DIMM (200P)

	1	VREF	VSS46	2			
	3	VSS47	DQ4	4	M_A_DQ4		
M_A_DQ1	5	DQ0	DQ5	6	M_A_DQ0		
M_A_DQ5	7	DQ1	VSS15	8			
	9	VSS37	DM0	10	M_A_DM0		
M_A_DQS#0	11	DQS#0	VSS5	12			
M_A_DQS0	13	DQS0	DQ6	14	M_A_DQ7		
	15	VSS48	DQ7	16	M_A_DQ6		
M_A_DQ2	17	DQ2	VSS16	18			
M_A_DQ3	19	DQ3	DQ12	20	M_A_DQ13		
	21	VSS38	DQ13	22	M_A_DQ12		
M_A_DQ14	23	DQ8	VSS17	24			
M_A_DQ8	25	DQ9	DM1	26	M_A_DM1		
	27	VSS49	VSS53	28			
M_A_DQS#1	29	DQS#1	CK0	30	M_CLK_DDR0	M_CLK_DDR0	8
M_A_DQS1	31	DQS1	CK0#	32	M_CLK_DDR#0	M_CLK_DDR#0	8
	33	VSS39	VSS41	34			
M_A_DQ9	35	DQ10	DQ14	36	M_A_DQ11		
M_A_DQ15	37	DQ11	DQ15	38	M_A_DQ10		
	39	VSS50	VSS54	40			
	41	VSS18	VSS20	42			
M_A_DQ21	43	DQ16	DQ20	44	M_A_DQ20		
M_A_DQ17	45	DQ17	DQ21	46	M_A_DQ16		
	47	VSS1	VSS6	48			
M_A_DQS#2	49	DQS#2	NC3	50	PM_EXTTS#0	PM_EXTTS#0	8
M_A_DQS2	51	DQS2	DM2	52	M_A_DM2		
	53	VSS19	VSS21	54			
M_A_DQ23	55	DQ18	DQ22	56	M_A_DQ18		
M_A_DQ19	57	DQ19	DQ23	58	M_A_DQ22		
	59	VSS22	VSS24	60			
M_A_DQ24	61	DQ24	DQ28	62	M_A_DQ28		
M_A_DQ25	63	DQ25	DQ29	64	M_A_DQ29		
	65	VSS23	VSS25	66			
M_A_DM3	67	DM3	DQS#3	68	M_A_DQS#3		
	69	NC4	DQS3	70	M_A_DQS3		
	71	VSS9	VSS10	72			
M_A_DQ30	73	DQ26	DQ30	74	M_A_DQ27		
M_A_DQ31	75	DQ27	DQ31	76	M_A_DQ26		
	77	VSS4	VSS8	78			
M_CKE0	79	CKE0	CKE1	80	M_CKE1	M_CKE1	8,12
	81	VDD7	VDD8	82			
	83	NC1	A15	84			
M_A_BS#2	85	A16_BA2	A14	86			
	87	VDD9	VDD11	88			
M_A_A12	89	A12	A11	90	M_A_A11		
M_A_A9	91	A9	A7	92	M_A_A7		
M_A_A8	93	A8	A6	94	M_A_A6		
	95	VDD5	VDD4	96			
M_A_A5	97	A5	A4	98	M_A_A4		
M_A_A3	99	A3	A2	100	M_A_A2		
M_A_A1	101	A1	A0	102	M_A_A0		
	103	VDD10	VDD12	104			
M_A_A10	105	A10/AP	BA1	106	M_A_BS#1	M_A_BS#1	7,12
	107	BA0	RAS#	108	M_A_RAS#	M_A_RAS#	7,12
M_A_WE#	109	WE#	S0#	110	M_CS#0	M_CS#0	8,12
	111	VDD2	VDD1	112			
M_A_CAS#	113	CAS#	ODT0	114	M_ODT0	M_ODT0	8,12
M_CS#1	115	S1#	A13	116	M_A_A13		
	117	VDD3	VDD6	118			
M_ODT1	119	ODT1	NC2	120			
	121	VSS11	VSS12	122			
M_A_DQ37	123	DQ32	DQ36	124	M_A_DQ36		
M_A_DQ35	125	DQ33	DQ37	126	M_A_DQ32		
	127	VSS26	VSS28	128			
M_A_DQS#4	129	DQS#4	DM4	130	M_A_DM4		
M_A_DQS4	131	DQS4	VSS42	132			
	133	VSS2	DQ38	134	M_A_DQ33		
M_A_DQ38	135	DQ34	DQ39	136	M_A_DQ34		
M_A_DQ39	137	DQ35	VSS55	138			
	139	VSS27	DQ44	140	M_A_DQ45		
M_A_DQ41	141	DQ40	DQ45	142	M_A_DQ44		
M_A_DQ40	143	DQ41	VSS43	144			
	145	VSS29	DQS#5	146	M_A_DQS#5		
M_A_DM5	147	DM5	DQS5	148	M_A_DQS5		
	149	VSS51	VSS56	150			
M_A_DQ42	151	DQ42	DQ46	152	M_A_DQ46		
M_A_DQ43	153	DQ43	DQ47	154	M_A_DQ47		
	155	VSS40	VSS44	156			
M_A_DQ53	157	DQ48	DQ52	158	M_A_DQ49		
M_A_DQ52	159	DQ49	DQ53	160	M_A_DQ48		
	161	VSS52	VSS57	162			
	163	NCTEST	CK1	164	M_CLK_DDR1	M_CLK_DDR1	8
	165	VSS30	CK1#	166	M_CLK_DDR#1	M_CLK_DDR#1	8
M_A_DQS#6	167	DQS#6	VSS45	168			
M_A_DQS6	169	DQS6	DM6	170	M_A_DM6		
	171	VSS31	VSS32	172			
M_A_DQ51	173	DQ50	DQ54	174	M_A_DQ55		
M_A_DQ50	175	DQ51	DQ55	176	M_A_DQ54		
	177	VSS33	VSS35	178			
M_A_DQ61	179	DQ56	DQ60	180	M_A_DQ56		
M_A_DQ57	181	DQ57	DQ61	182	M_A_DQ60		
	183	VSS3	VSS7	184			
M_A_DM7	185	DM7	DQS#7	186	M_A_DQS#7		
	187	VSS34	DQS7	188	M_A_DQS7		
M_A_DQ63	189	DQ58	VSS36	190			
M_A_DQ59	191	DQ59	DQ62	192	M_A_DQ58		
	193	VSS14	DQ63	194	M_A_DQ62		
CGDAT_SMB	195	SDA	VSS13	196			
CGCLK_SMB	197	SCL	SA0	198	R285 10K_4		
	199	VDD(SPD)	SA1	200	R287 10K_4		

+3VO

SMBus address A0

2nd source:DGMK00000C0

CLOCK 0,1 CKE 0,1 H 5.2

SMDDR_VREF_DIMM
A1A:Swap net

M_B_DM[0..7] 7
M_B_DQ[0..63] 7
M_B_DQS[0..7] 7
M_B_DQS#[0..7] 7
M_B_A[0..13] 7,12

CN30

DDR2_SODIMM(2-1734073-2)

PC4800 DDR2 SDRAM SO-DIMM (200P)

	1	VREF	VSS46	2			
M_B_DQ1	3	VSS47	DQ4	4	M_B_DQ4		
M_B_DQ5	5	DQ0	DQ5	6	M_B_DQ0		
	7	DQ1	VSS15	8			
	9	VSS37	DM0	10	M_B_DM0		
M_B_DQS#0	11	DQS#0	VSS5	12			
M_B_DQS0	13	DQS0	DQ6	14	M_B_DQ7		
	15	VSS48	DQ7	16	M_B_DQ6		
M_B_DQ2	17	DQ2	VSS16	18			
M_B_DQ3	19	DQ3	DQ12	20	M_B_DQ12		
	21	VSS38	DQ13	22	M_B_DQ13		
M_B_DQ8	23	DQ8	VSS17	24			
M_B_DQ9	25	DQ9	DM1	26	M_B_DM1		
	27	VSS49	VSS53	28			
M_B_DQS#1	29	DQS#1	CK0	30	M_CLK_DDR3	M_CLK_DDR3	8
M_B_DQS1	31	DQS1	CK0#	32	M_CLK_DDR#3	M_CLK_DDR#3	8
	33	VSS39	VSS41	34			
M_B_DQ11	35	DQ10	DQ14	36	M_B_DQ15		
M_B_DQ10	37	DQ11	DQ15	38	M_B_DQ14		
	39	VSS50	VSS54	40			
	41	VSS18	VSS20	42			
M_B_DQ17	43	DQ16	DQ20	44	M_B_DQ16		
M_B_DQ20	45	DQ17	DQ21	46	M_B_DQ21		
	47	VSS1	VSS6	48			
M_B_DQS#2	49	DQS#2	NC3	50	PM_EXTTS#0	PM_EXTTS#0	8
M_B_DQS2	51	DQS2	DM2	52	M_B_DM2		
	53	VSS19	VSS21	54			
M_B_DQ19	55	DQ18	DQ22	56	M_B_DQ18		
M_B_DQ23	57	DQ19	DQ23	58	M_B_DQ22		
	59	VSS22	VSS24	60			
M_B_DQ28	61	DQ24	DQ28	62	M_B_DQ24		
M_B_DQ29	63	DQ25	DQ29	64	M_B_DQ25		
	65	VSS23	VSS25	66			
M_B_DM3	67	DM3	DQS3	68	M_B_DQS#3		
	69	NC4	DQS3	70	M_B_DQS3		
	71	VSS9	VSS10	72			
M_B_DQ30	73	DQ26	DQ30	74	M_B_DQ26		
M_B_DQ31	75	DQ27	DQ31	76	M_B_DQ27		
	77	VSS4	VSS8	78			
M_CKE2	79	CKE0	CKE1	80	M_CKE3	M_CKE3	8,12
	81	VDD7	VDD8	82			
	83	NC1	A15	84			
M_B_BS#2	85	A16_BA2	A14	86			
	87	VDD9	VDD11	88			
M_B_A12	89	A12	A11	90	M_B_A11		
M_B_A9	91	A9	A7	92	M_B_A7		
M_B_A8	93	A8	A6	94	M_B_A6		
	95	VDD5	VDD4	96			
M_B_A5	97	A5	A4	98	M_B_A4		
M_B_A3	99	A3	A2	100	M_B_A2		
M_B_A1	101	A1	A0	102	M_B_A0		
	103	VDD10	VDD12	104			
M_B_A10	105	A10/AP	BA1	106	M_B_BS#1	M_B_BS#1	7,12
M_B_BS#0	107	BA0	RAS#	108	M_B_RAS#	M_B_RAS#	7,12
M_B_WE#	109	WE#	S0#	110	M_CS#2	M_CS#2	8,12
	111	VDD2	VDD1	112			
M_B_CAS#	113	CAS#	ODT0	114	M_ODT2	M_ODT2	8,12
M_CS#3	115	S1#	A13	116	M_B_A13		
	117	VDD3	VDD6	118			
M_ODT3	119	ODT1	NC2	120			
	121	VSS11	VSS12	122			
M_B_DQ37	123	DQ32	DQ36	124	M_B_DQ32		
M_B_DQ36	125	DQ33	DQ37	126	M_B_DQ33		
	127	VSS26	VSS28	128			
M_B_DQS#4	129	DQS#4	DM4	130	M_B_DM4		
M_B_DQS4	131	DQS4	VSS42	132			
	133	VSS2	DQ38	134	M_B_DQ34		
M_B_DQ39	135	DQ34	DQ39	136	M_B_DQ38		
M_B_DQ35	137	DQ35	VSS55	138			
	139	VSS27	DQ44	140	M_B_DQ44		
M_B_DQ41	141	DQ40	DQ45	142	M_B_DQ45		
M_B_DQ40	143	DQ41	VSS43	144			
	145	VSS29	DQS#5	146	M_B_DQS#5		
M_B_DM5	147	DM5	DQS5	148	M_B_DQS5		
	149	VSS51	VSS56	150			
M_B_DQ47	151	DQ42	DQ46	152	M_B_DQ46		
M_B_DQ42	153	DQ43	DQ47	154	M_B_DQ43		
	155	VSS40	VSS44	156			
M_B_DQ53	157	DQ48	DQ52	158	M_B_DQ52		
M_B_DQ49	159	DQ49	DQ53	160	M_B_DQ48		
	161	VSS52	VSS57	162			
	163	NCTEST	CK1	164	M_CLK_DDR2	M_CLK_DDR2	8
	165	VSS30	CK1#	166	M_CLK_DDR#2	M_CLK_DDR#2	8
M_B_DQS#6	167	DQS#6	VSS45	168			
M_B_DQS6	169	DQS6	DM6	170	M_B_DM6		
	171	VSS31	VSS32	172			
M_B_DQ50	173	DQ50	DQ54	174	M_B_DQ54		
M_B_DQ55	175	DQ51	DQ55	176	M_B_DQ51		
	177	VSS33	VSS35	178			
M_B_DQ61	179	DQ56	DQ60	180	M_B_DQ60		
M_B_DQ57	181	DQ57	DQ61	182	M_B_DQ56		
	183	VSS3	VSS7	184			
M_B_DM7	185	DM7	DQS#7	186	M_B_DQS#7		
	187	VSS34	DQS7	188	M_B_DQS7		
M_B_DQ63	189	DQ58	VSS36	190			
M_B_DQ58	191	DQ59	DQ62	192	M_B_DQ59		
	193	VSS14	DQ63	194	M_B_DQ62		
2 CGDAT_SMB	195	SDA	VSS13	196			
2 CGCLK_SMB	197	SCL	SA0	198	R286 10K_4		
+3VO	199	VDD(SPD)	SA1	200	R288 10K_4		

+3VO

SMBus address A4

2nd source:DGMK0002610

CLOCK 3,4 CKE 2,3 H 9.2

A1A:Change SODIMM1 pin 50 from PM_EXTTS#1 to PM_EXTTS#0(Intel recommend)

+1.8VSUS
Place these Caps near So-Dimm1.
C355 2.2U-6.3V_6
C352 2.2U-6.3V_6
C451 2.2U-6.3V_6
C425 2.2U-6.3V_6
C405 2.2U-6.3V_6

+1.8VSUS
Place these Caps near So-Dimm1.
C396 .1U-10V_4
C424 .1U-10V_4
C358 .1U-10V_4
C395 .1U-10V_4

SMDDR_VREF_DIMM
+3V
C267 .1U-10V_4
C250 2.2U-6.3V_6
C493 2.2U-6.3V_6
C495 .1U-10V_4

Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

+1.8VSUS
Place these Caps near So-Dimm2.
C366 2.2U-6.3V_6
C345 2.2U-6.3V_6
C426 2.2U-6.3V_6
C351 2.2U-6.3V_6
C353 2.2U-6.3V_6

+1.8VSUS
Place these Caps near So-Dimm1.
C384 .1U-10V_4
C407 .1U-10V_4
C383 .1U-10V_4
C394 .1U-10V_4

SMDDR_VREF_DIMM
+3V
C264 .1U-10V_4
C272 2.2U-6.3V_6
C492 2.2U-6.3V_6
C494 .1U-10V_4

Place these Caps near So-Dimm2.
No Vias Between the Trace of PIN to CAP.

SMDDR_VREF
SMDDR_VREF_DIMM
R170 0_4
SMDDR_VREF 8,43
R162 *10K/F_4
R160 *10K/F_4
+1.8VSUS

PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	DDRII SO-DIMM(200P)	1A
Date: Wednesday, November 30, 2005	Sheet 13 of 46	

RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
A1A:Change RTXC1/RTXC2 from 10pf to 18pf

A1A:Change RTC Connector footprint

20MIL 20MIL

B1B:Per Intel comment,don't stuff R307 for CPUSLP#

Should be 2" close ICH7

A series termination resistor is required for the PRIMARY CODEC

B1B:Add R719 for BIT_CLK_MODEM

CKL:1n ~ 20nF

25mils/15mils

Place within 500 mils of ICH7

ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M HOST (1 OF 4)	1A

Date: Friday, December 02, 2005 Sheet 14 of 46

A1A:Change PCIE pin define to meet Acer spec

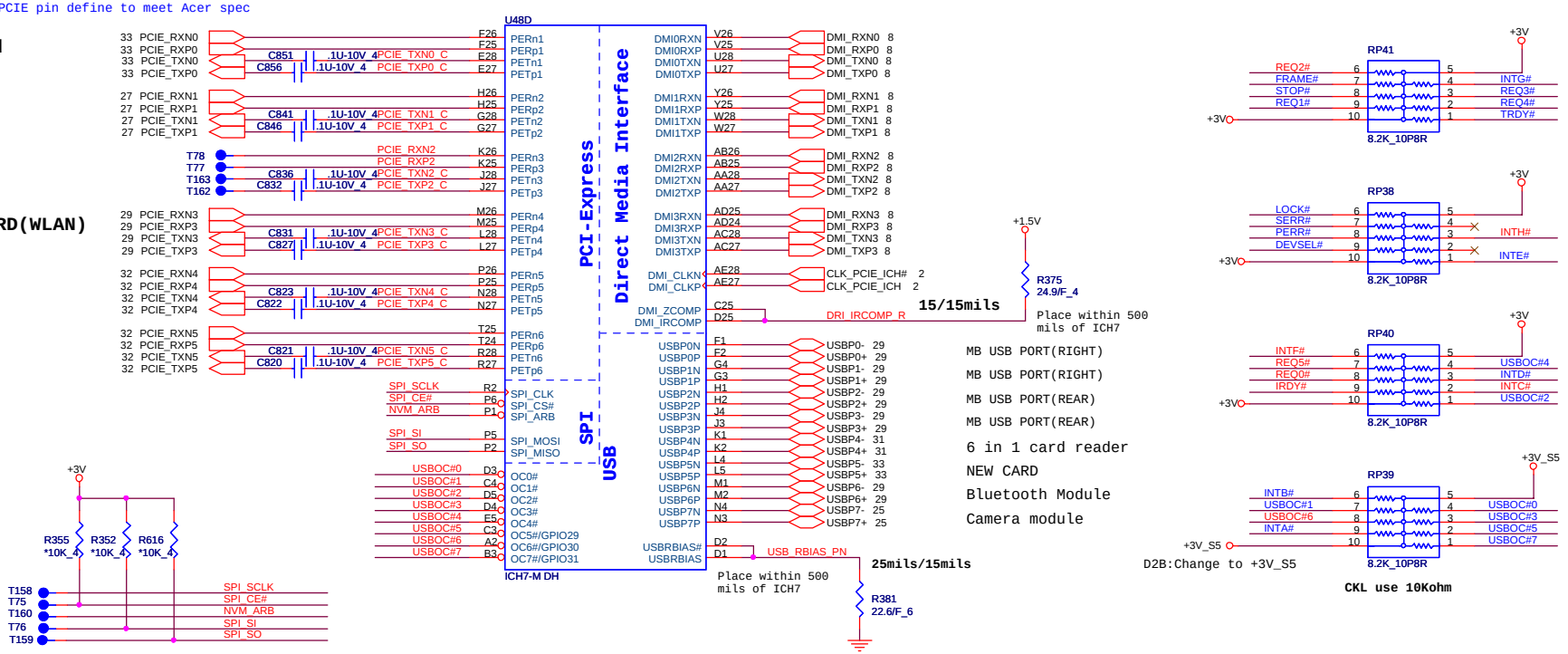
New card

GLAN

MINI CARD(WLAN)

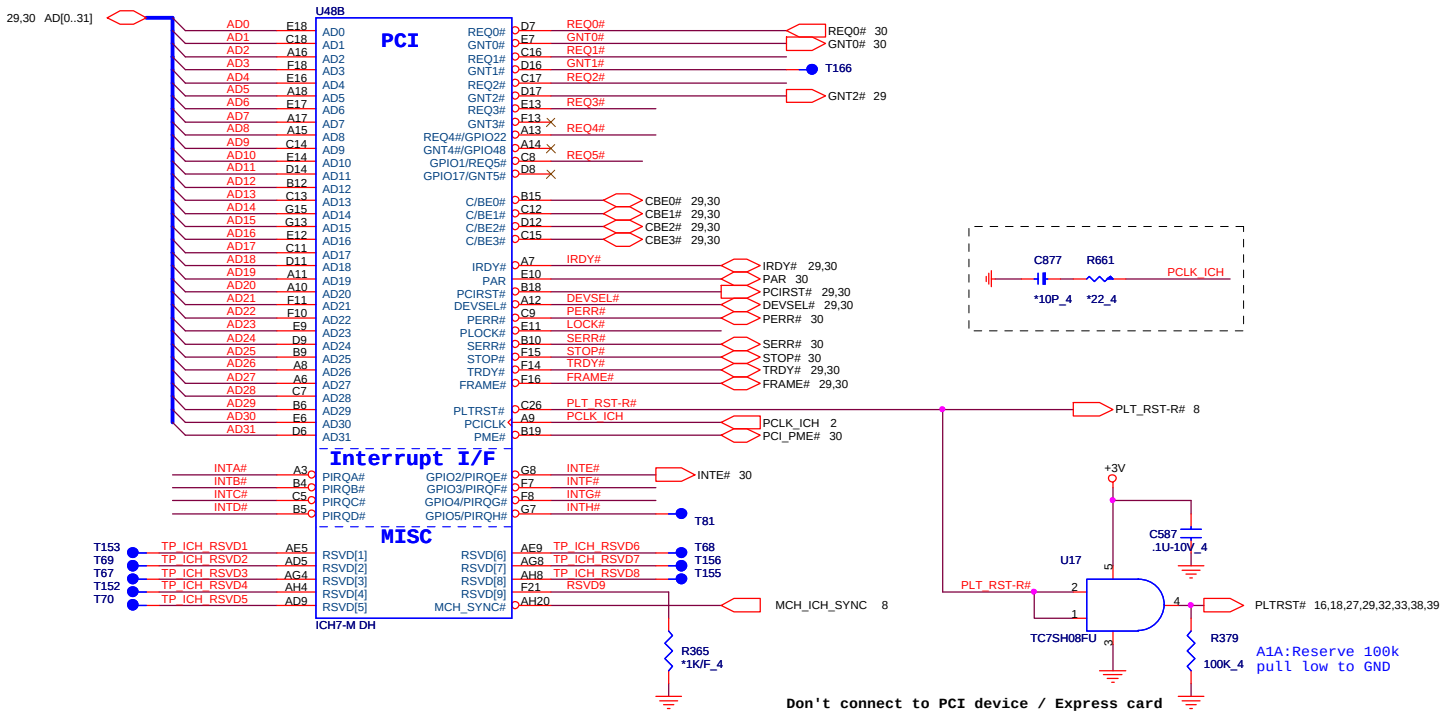
EZ4_1

EZ4_2



ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
OZ711MP1	AD25	REQ0# / GNT0#	INTE#

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M PCI E (2 OF 4)	1A

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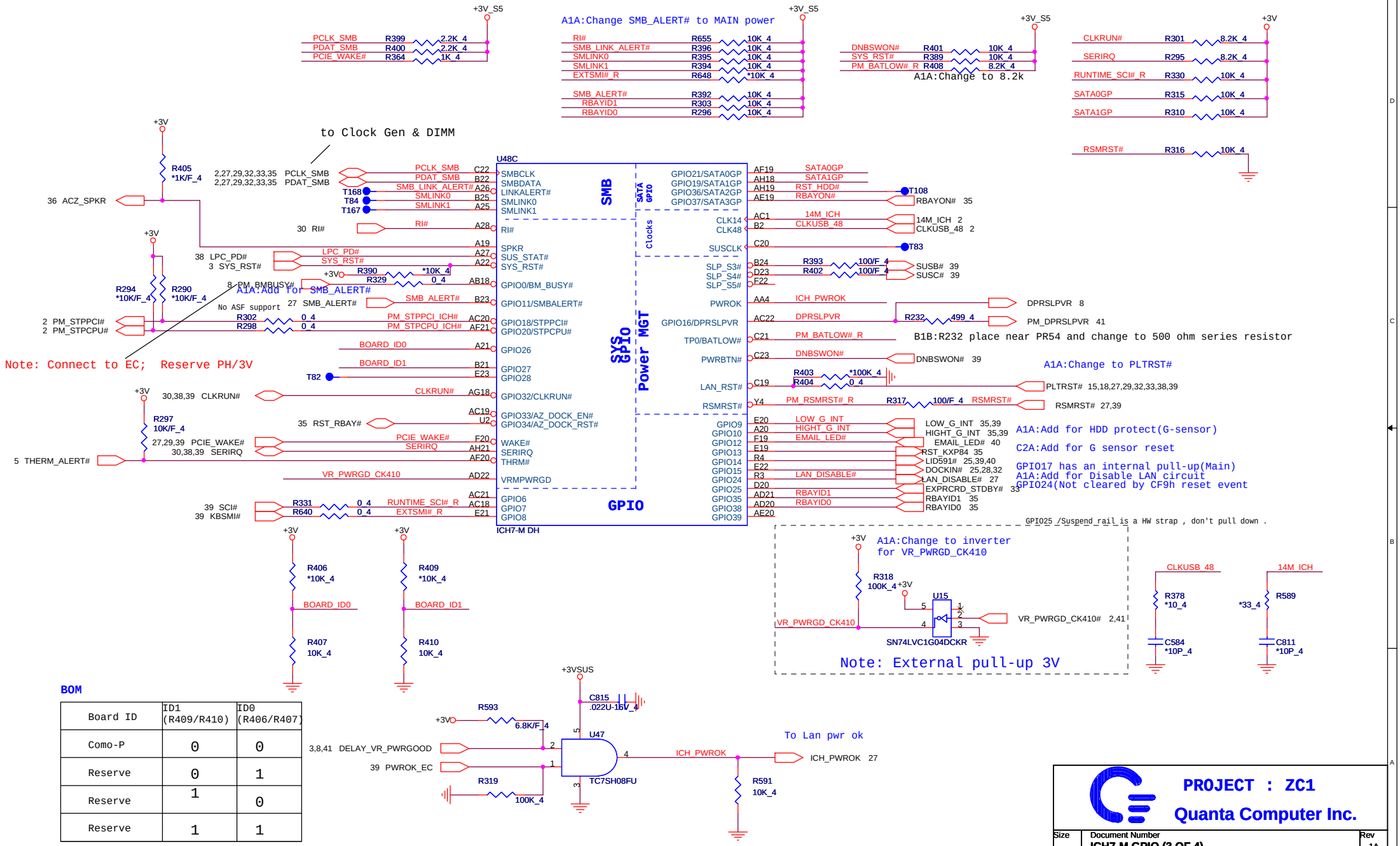

BOM

Board ID	ID1 (R409/R410)	ID0 (R406/R407)
Como-P	0	0
Reserve	0	1
Reserve	1	0
Reserve	1	1

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M GPIO (3 OF 4)	1A

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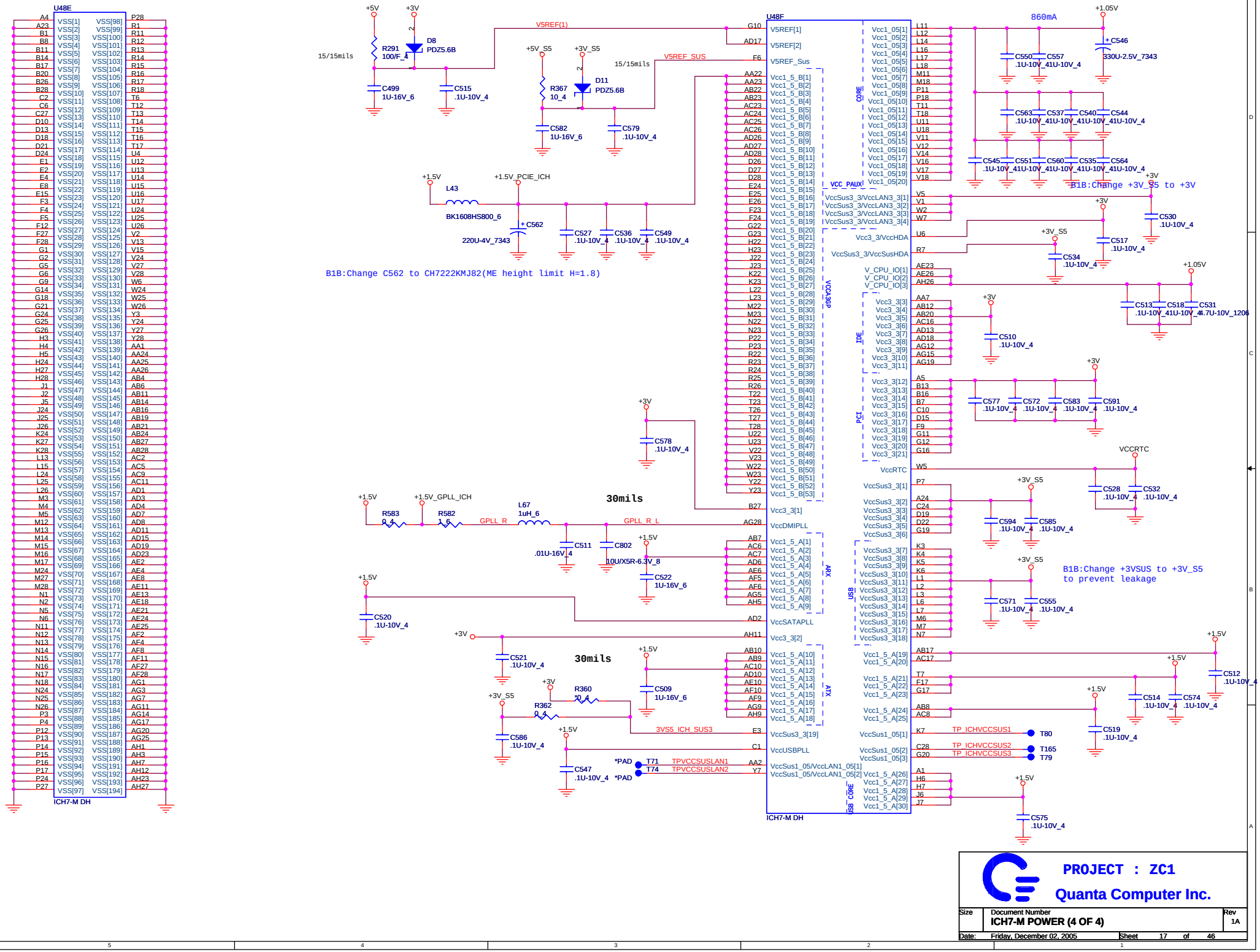
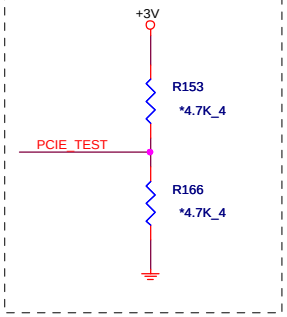

U48E
ICH7-M DH
U48F
ICH7-M DH
B1B:Change C562 to CH7222KMJ82(ME height limit H=1.8)
B1B:Change +3V_S5 to +3V
B1B:Change +3VSUS to +3V_S5
to prevent leakage
860mA
30mils
30mils
PROJECT : ZC1
Quanta Computer Inc.
ICH7-M POWER (4 OF 4)
Rev 1A
Friday, December 02, 2005
Sheet 17 of 46

PCIE TEST PADS
PCIE TEST POINTS MUST BE WITHIN 250 MILS
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE
SIGNALS THE SAME DISTANCE

8 PEG_RXP[15:0]
8 PEG_RXN[15:0]
8 PEG_TXP[15:0]
8 PEG_TXN[15:0]

ATI FEATURE NOT ENABLED (M52P,M54P,M56P)
B1B:Don't stuff R153,R166 for PCIE_TEST



U41A

PART 1 OF 7

PEG_TXP0	AJ31	PCIE_RX0P		PCIE_TX0P	AK27	V_GMCHEXP_RXP0	C304 EV@.1U-10V_4 PEG_RXP0
PEG_TXN0	AH31	PCIE_RX0N		PCIE_TX0N	AJ27	V_GMCHEXP_RXN0	C303 EV@.1U-10V_4 PEG_RXN0
PEG_TXP1	AH30	PCIE_RX1P		PCIE_TX1P	AJ25	V_GMCHEXP_RXP1	C333 EV@.1U-10V_4 PEG_RXP1
PEG_TXN1	AG30	PCIE_RX1N		PCIE_TX1N	AH25	V_GMCHEXP_RXN1	C332 EV@.1U-10V_4 PEG_RXN1
PEG_TXP2	AG32	PCIE_RX2P		PCIE_TX2P	AH28	V_GMCHEXP_RXP2	C302 EV@.1U-10V_4 PEG_RXP2
PEG_TXN2	AF32	PCIE_RX2N		PCIE_TX2N	AG28	V_GMCHEXP_RXN2	C301 EV@.1U-10V_4 PEG_RXN2
PEG_TXP3	AF31	PCIE_RX3P		PCIE_TX3P	AG27	V_GMCHEXP_RXP3	C331 EV@.1U-10V_4 PEG_RXP3
PEG_TXN3	AE31	PCIE_RX3N		PCIE_TX3N	AF27	V_GMCHEXP_RXN3	C330 EV@.1U-10V_4 PEG_RXN3
PEG_TXP4	AE30	PCIE_RX4P		PCIE_TX4P	AF25	V_GMCHEXP_RXP4	C300 EV@.1U-10V_4 PEG_RXP4
PEG_TXN4	AD30	PCIE_RX4N		PCIE_TX4N	AE25	V_GMCHEXP_RXN4	C299 EV@.1U-10V_4 PEG_RXN4
PEG_TXP5	AD32	PCIE_RX5P		PCIE_TX5P	AE28	V_GMCHEXP_RXP5	C329 EV@.1U-10V_4 PEG_RXP5
PEG_TXN5	AC32	PCIE_RX5N		PCIE_TX5N	AD28	V_GMCHEXP_RXN5	C328 EV@.1U-10V_4 PEG_RXN5
PEG_TXP6	AC31	PCIE_RX6P		PCIE_TX6P	AD27	V_GMCHEXP_RXP6	C298 EV@.1U-10V_4 PEG_RXP6
PEG_TXN6	AB31	PCIE_RX6N		PCIE_TX6N	AC27	V_GMCHEXP_RXN6	C297 EV@.1U-10V_4 PEG_RXN6
PEG_TXP7	AB30	PCIE_RX7P		PCIE_TX7P	AC25	V_GMCHEXP_RXP7	C327 EV@.1U-10V_4 PEG_RXP7
PEG_TXN7	AA30	PCIE_RX7N		PCIE_TX7N	AB25	V_GMCHEXP_RXN7	C326 EV@.1U-10V_4 PEG_RXN7
PEG_TXP8	AA32	PCIE_RX8P		PCIE_TX8P	AB28	V_GMCHEXP_RXP8	C296 EV@.1U-10V_4 PEG_RXP8
PEG_TXN8	Y32	PCIE_RX8N		PCIE_TX8N	AA28	V_GMCHEXP_RXN8	C295 EV@.1U-10V_4 PEG_RXN8
PEG_TXP9	Y31	PCIE_RX9P		PCIE_TX9P	AA27	V_GMCHEXP_RXP9	C325 EV@.1U-10V_4 PEG_RXP9
PEG_TXN9	W31	PCIE_RX9N		PCIE_TX9N	Y27	V_GMCHEXP_RXN9	C324 EV@.1U-10V_4 PEG_RXN9
PEG_TXP10	W30	PCIE_RX10P		PCIE_TX10P	Y25	V_GMCHEXP_RXP10	C294 EV@.1U-10V_4 PEG_RXP10
PEG_TXN10	V30	PCIE_RX10N		PCIE_TX10N	W25	V_GMCHEXP_RXN10	C293 EV@.1U-10V_4 PEG_RXN10
PEG_TXP11	V32	PCIE_RX11P		PCIE_TX11P	W28	V_GMCHEXP_RXP11	C323 EV@.1U-10V_4 PEG_RXP11
PEG_TXN11	U32	PCIE_RX11N		PCIE_TX11N	V28	V_GMCHEXP_RXN11	C322 EV@.1U-10V_4 PEG_RXN11
PEG_TXP12	U31	PCIE_RX12P		PCIE_TX12P	V27	V_GMCHEXP_RXP12	C292 EV@.1U-10V_4 PEG_RXP12
PEG_TXN12	T31	PCIE_RX12N		PCIE_TX12N	U27	V_GMCHEXP_RXN12	C291 EV@.1U-10V_4 PEG_RXN12
PEG_TXP13	T30	PCIE_RX13P		PCIE_TX13P	U25	V_GMCHEXP_RXP13	C321 EV@.1U-10V_4 PEG_RXP13
PEG_TXN13	R30	PCIE_RX13N		PCIE_TX13N	T25	V_GMCHEXP_RXN13	C320 EV@.1U-10V_4 PEG_RXN13
PEG_TXP14	R32	PCIE_RX14P		PCIE_TX14P	T28	V_GMCHEXP_RXP14	C290 EV@.1U-10V_4 PEG_RXP14
PEG_TXN14	P32	PCIE_RX14N		PCIE_TX14N	R28	V_GMCHEXP_RXN14	C289 EV@.1U-10V_4 PEG_RXN14
PEG_TXP15	P31	PCIE_RX15P		PCIE_TX15P	R27	V_GMCHEXP_RXP15	C319 EV@.1U-10V_4 PEG_RXP15
PEG_TXN15	N31	PCIE_RX15N		PCIE_TX15N	P27	V_GMCHEXP_RXN15	C318 EV@.1U-10V_4 PEG_RXN15

P C I - E X P R E S S I N T E R F A C E

Clock

2 CLK_PCIE_M56	AL28	PCIE_REFCLKP
2 CLK_PCIE_M56#	AK28	PCIE_REFCLKN

Calibration

PCIE_CALRN	AE24	R156	EV@2K/F_4
PCIE_CALRP	AD24	R172	EV@562/F_4
PCIE_CALI	AB24	R167	EV@1.47K/F_4

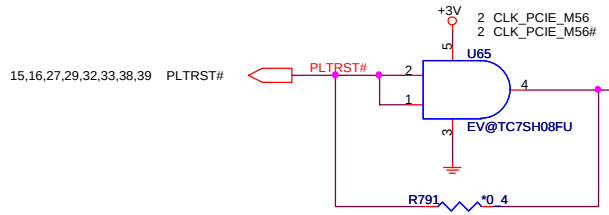
+1.2V_VPCIE

B1B:PCIE_CALRN(ball AE24) need change to +1.2V_VPCIE

FOR M52P,M54P,M56P
PCIE_CALRN = 2K
PCIE CALRP = 562R
PCIE CALI = 1.47K

PERSTB — PLTRST#_M56 — AG24
PCIE_TEST — AA24
PERSTB_MASK — AF24 — Tie To VSS

EV@M56-P B13



E3A:Add U65 for M56 PLTRST#

PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	M56P 1 OF 7	1A

Date: Friday, December 02, 2005 Sheet 18 of 46

MEMORY CLOCK SPREAD SPECTRUM

ANY UNUSED GPIO CAN OPTIONALLY BE MEMORY TYPE CONFIG STRAPS

C1C:Change GPIO27 instead of GPIO25 for MEMTYPE_1
E3A:Add R792 for MEMTYPE_1

D2B:The TMDS termination resistor values (330 ohm) are pcb layout dependent and may require final tuning

D2B:Change R123,R130,R132,R134 from 330 to 180 for TMDS

B1B:Change R177,R181 to 0 ohm for VGA 27MHZ

FOR M52P,M54P,M56P NOT CONNECTED

Voltage divider resistor values R181 and R551 to ensure XTALIN/XTALOUT voltage level matches vddc

B1B:Don't stuff C739

A1A:Reversed LVDSCLK,LVDSDATA pull high to LVDS side

A1A:Change LVDS_DAT/LVDS_CLK to DVPDATA18/DVPDATA19

A1A:Add pull low 10k
GPIO15 HI = 1.0V VDDC
GPIO15 LO = 1.1V VDDC

V_PWRCNTL DRIVEN HI SELECT 1.0V VDDC
V_PWRCNTL DRIVEN LO SELECT 1.1V VDDC

For m26x,m52p,m54p,m56p thermal interrupt is low edge and connects to gpio17

B1B:Reserved for VREFG

FOR M52P,M54P,M56P CONNECT TO +2.5V

1.2V OR 1.0V @ 20MA ASIC MPVDD
CONNECT TO VDDC

For m26x,m52p,m54p,m56p thermal interrupt is low edge and connects to gpio17

FOR M52P,M54P,M56P A2VDDQ IT IS NO CONNECT

FOR M52P,M54P,M56P CONNECT TO +2.5V

VDD_PNL_PLL25 (2.5V @ 40mA ASIC LPVDD,TPVDD)
FOR M52P,M54P,M56P CONNECT TO +2.5V

AVDD_2.5 (2.5V @ 65mA ASIC AVDD)
FOR M52P,M54P,M56P CONNECT TO +2.5V

VDDDI_2.5 (2.5V @ 40mA ASIC VDD1DI,VDD2DI)

PLACE CLOSE TO ASIC

E3B:Add R137,R143,R146,R174,R175,R176 (150 ohm) for CRT/TV can't detect issue

R_DAC1	R174	150/F_4
G_DAC1	R176	150/F_4
B_DAC1	R175	150/F_4
EXT_TV_Y/G	R146	150/F_4
EXT_TV_C/R	R137	150/F_4
EXT_TV_COMP	R143	150/F_4

The DDC2 is for DVI (TMDS) reading EDID data, which cannot be shared with other I2C devices.

A1A:Reserve for thermal sensor CLK/DATA
B1B:Stuff R125,R126 for VGA thermal sensor SMBus
D2B:Remove R125,R126 for VGA thermal sensor SMBus

FOR M52P,M54P,M56P GENERICC IT IS GPIO

15 MIL

10 mil trace / 10 mil space

Close to pin ASIC

SLAVE ADDRESS: 9A

B1B:Don't stuff R82,R95 for thermal sensor
D2B:stuff R82 for thermal sensor

D2B:Connect U7 OVERT to fan driver

A1A:Reserve for VGA thermal sensor

D2B:Change R122,R133 to 10K to resolve Battery can't learning issue

C2A:Stuff Q12,Q31 for VGA thermal sensor

B1B:Remove Q12,Q31 for VGA thermal sensor

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	M56P 2 OF 7	1A

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If memory interface has to be up to 600Mhz or above, the GPU core voltage and memory I/O voltage may need to be increased to 1.2~1.3V and 2.0V

A1A:Change to VGA_MEM_IO

1.2V ASIC PCIE_PVDD_12 @ 100mA, PCIE_VDDR_12 @ 2000mA

FOR M52P,M54P,M56P CONNECT TO +1.2V

1.2V OR 1.0V @ 18A ASIC VDDC,VDDCI

D2B:Add R778,Q56,Q57 for VGA +3V power sequence

VDD_PNL_PLL25 (2.5V @ 40mA ASIC LPVDD,TPVDD)

GENERICD : FOR M56P IT IS A BACK BIAS REGULATOR CONTROL

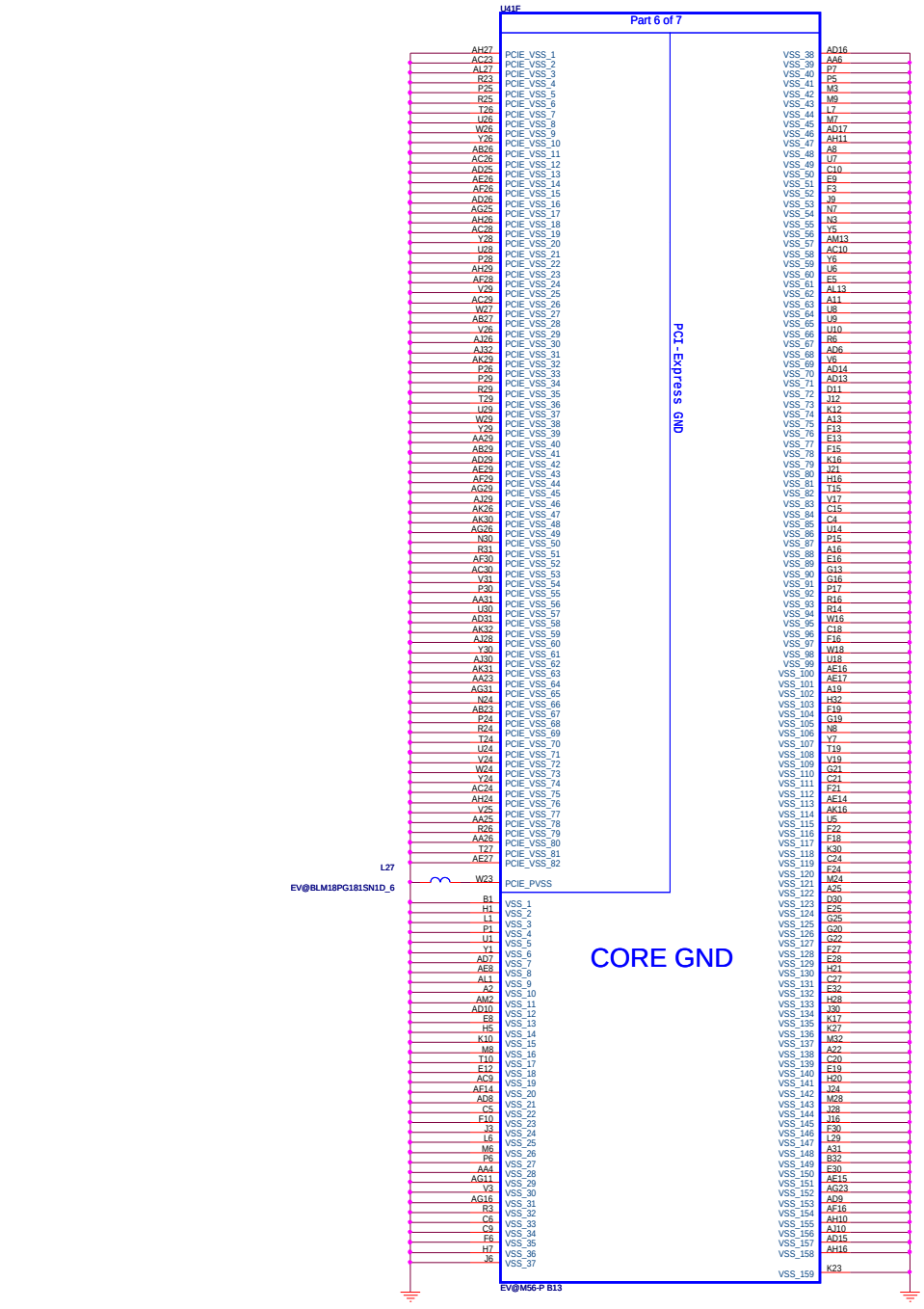
Panel power(LCDVCC) control

GENERICD->FOR M56P IT IS A BACK BIAS REGULATOR CONTROL

E3A:Add R789 for G966_VIN,change source to +1.8VSUS

D2B:Add R778,R780 for +1.2V_VPCIE

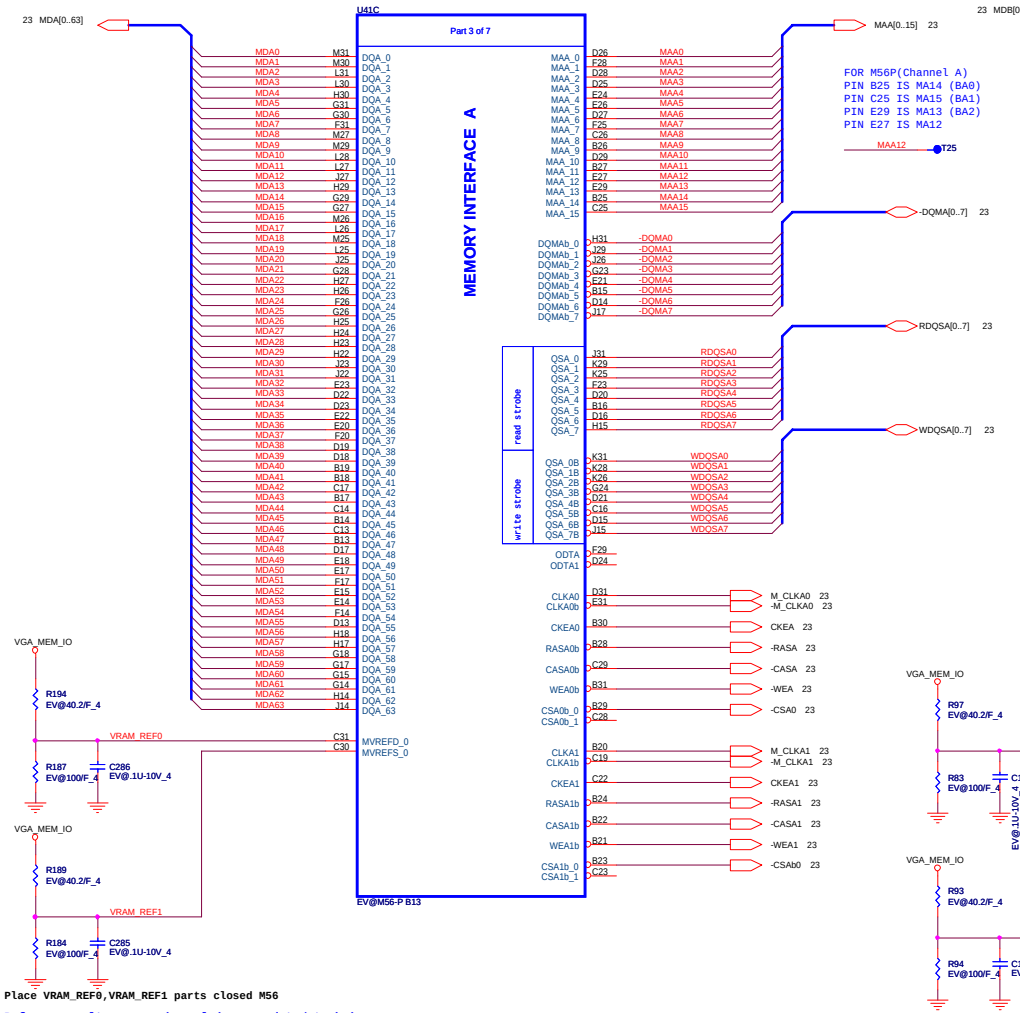
PROJECT : ZC1			
Quanta Computer Inc.			
Size	Document Number: M56P POWER		Rev: 1A
Date: Tuesday, November 29, 2005	Sheet 20 of 46		



PROJECT :	ZC1
Quanta Computer Inc.	
Size	Document Number: M56P 6 OF 7 — Rev: 1A
Date: Thursday, November 17, 2005	Sheet 21 of 46

RV410 MEMORY CHANNELS A and B

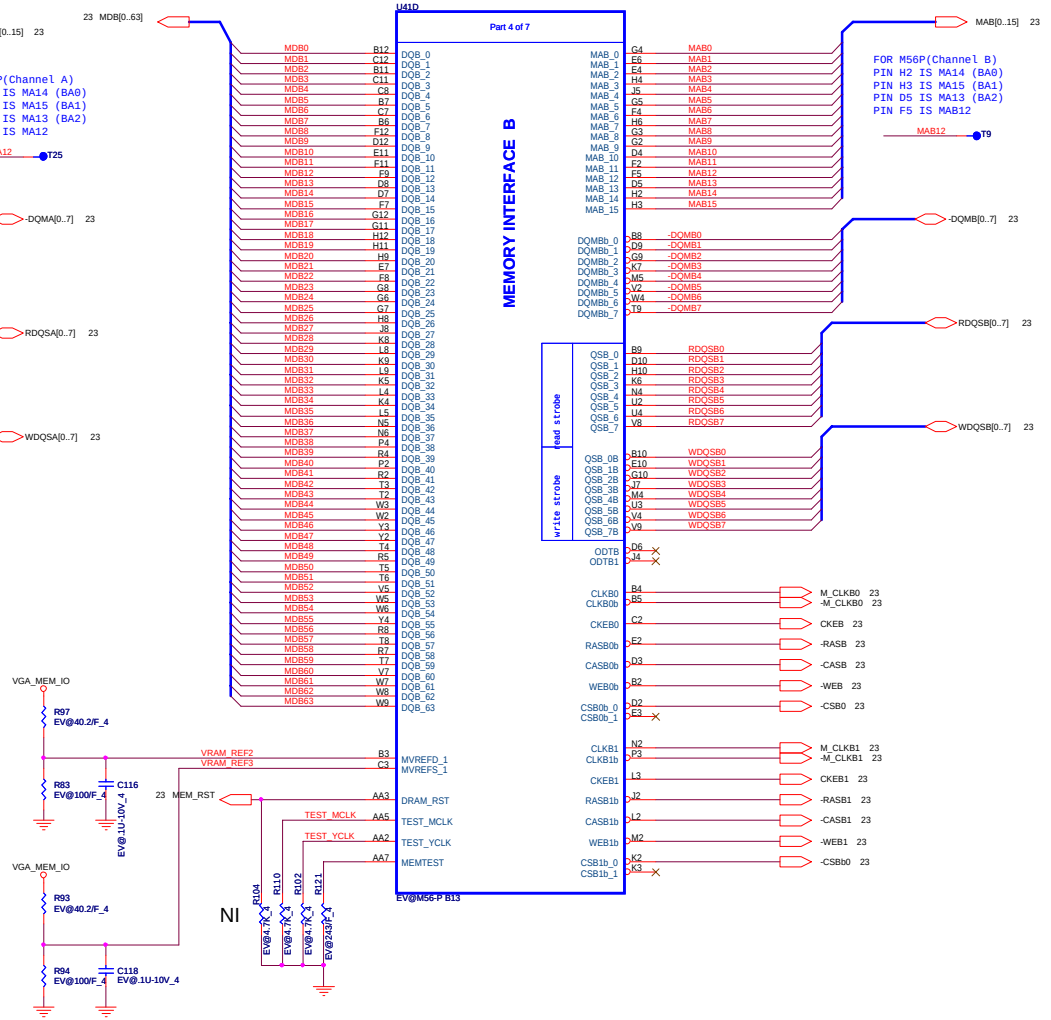
Channel A



Place VRAM_REF0,VRAM_REF1 parts closed M56

Reference voltage per channel (memory data/strobe)
MVREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVREFS_[0:1] (0.7 * VDDR1) (for GDDR3)

Channel B



Reference voltage per channel (memory data/strobe)
MVREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVREFS_[0:1] (0.7 * VDDR1) (for GDDR3)

PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	M56P 3/4 OF 7	1A
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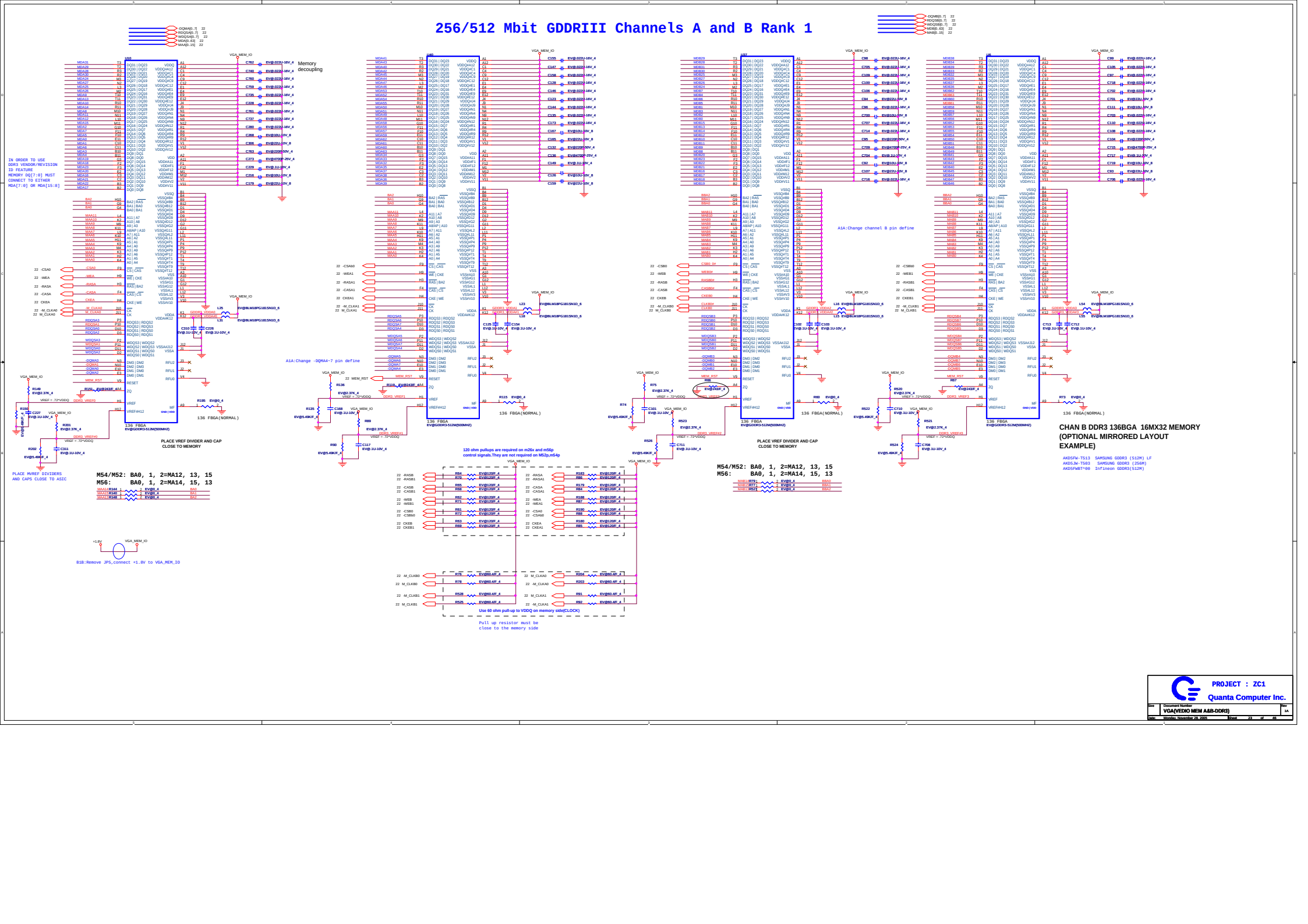
256/512 Mbit GDDRIII Channels A and B Rank 1



CHAN B DDR3 136BGA 16MX32 MEMORY (OPTIONAL MIRRORED LAYOUT EXAMPLE)

AKD5FW-TS13 SAMSUNG GDDR3 (512M) LF
AKD5JW-TS03 SAMSUNG GDDR3 (256M)
AKD5FWBT*00 Infineon GDDR3(512M)

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	VGA(VEDIO MEM A&B-DDR3)	1A
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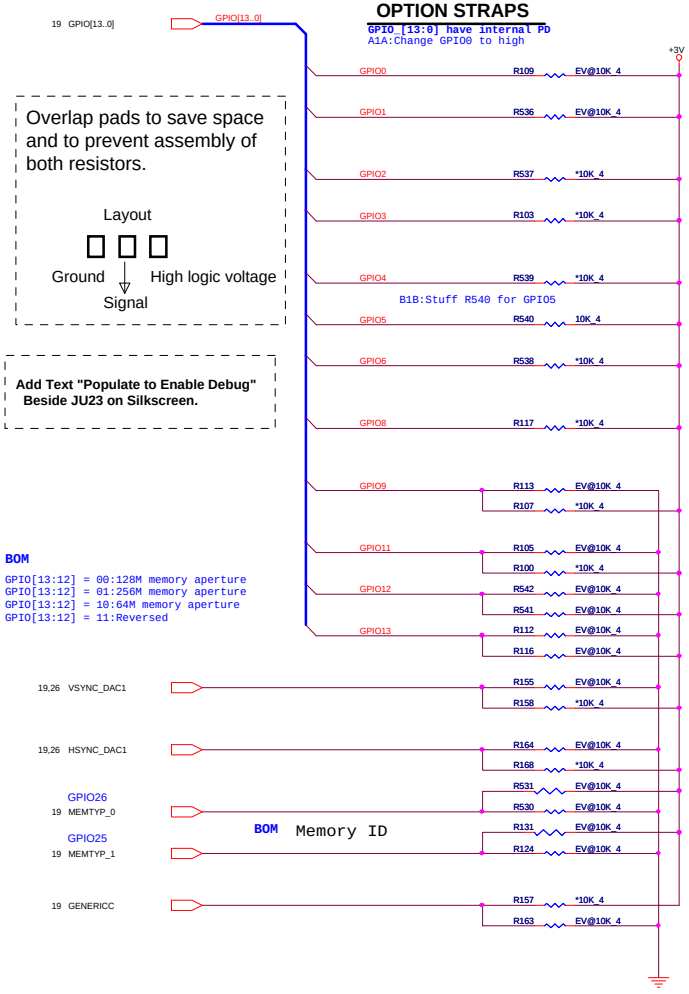
OPTION STRAPS

GPIO_[13:0] have internal Pd
A1A:Change GPIO0 to high



Overlap pads to save space and to prevent assembly of both resistors.

Layout

Ground — High logic voltage

Signal

Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.

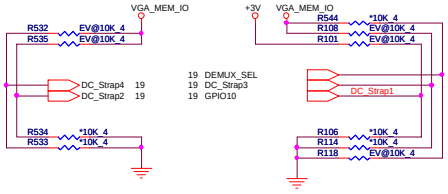
BOM

GPIO[13:12] = 00:128M memory aperture
GPIO[13:12] = 01:256M memory aperture
GPIO[13:12] = 10:64M memory aperture
GPIO[13:12] = 11:Reversed

BOM Memory ID

M56-P Strap

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE FOR M26X,M56P: INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS DO NOT INSTALL WITH INTEL 915PM CHIPSET FOR M5X - INSTALL	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE RSVD	GPIO5	sets the desired PCIE PLL bandwidth for M5x parts	DO NOT INSTALL 10K RESISTOR
COMMON MODE RANGE	GPIO6	NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO(9,13:11)	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE 000x - No ROM, MEM_AP_SIZE=00(128MB) 001x - No ROM,MEM_AP_SIZE=01(256MB) 010x - No Rom, MEM_AP_SIZE=10(64MB) 011x - No ROM,MEM_AP_SIZE=11(Reserved) 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	A1A:change ROMIDCFG(3:0) to 0010
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	No default
NO STRAP FUNCTION	H2SYNC, V2SYNC,GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	



A1A:change video capture enable setting

Board Straps REV_0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	GPIO25,26	MEMORY TYPE AND SPEED SELECT Memory connected to R420 identification for BIOS 00 - Samsung GDDR 3 memory(256Mb) 136 Ball BGA package 01 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package 10 - Infineon GDDR 3 memory(256Mb) 136 Ball BGA package 11 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package	00
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Enabled	1
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected **1 - Not detected**	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT **10 - DAC2 On as TVOUT** 11 - DAC2 On as TVOUT and CRT	10
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1

MEMORY TYPE AND SPEED SELECT

PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	M56P OPTION STRAPS	1A

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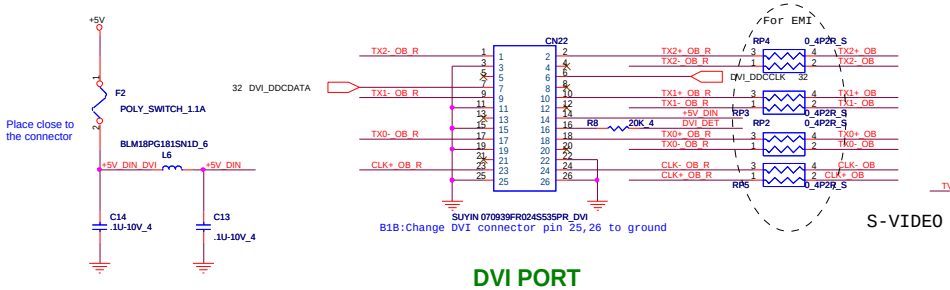
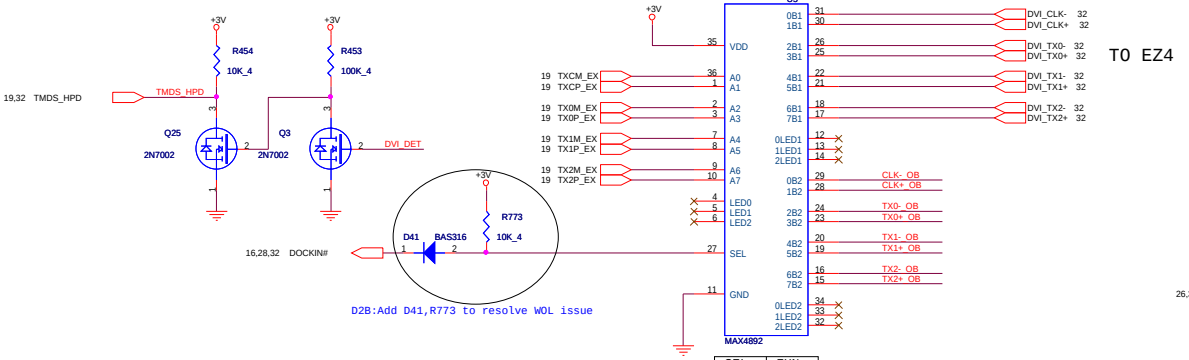
DVI-I CONNECTOR (DVI-D)



B1B:Change DVI connector pin 25,26 to ground

DVI PORT

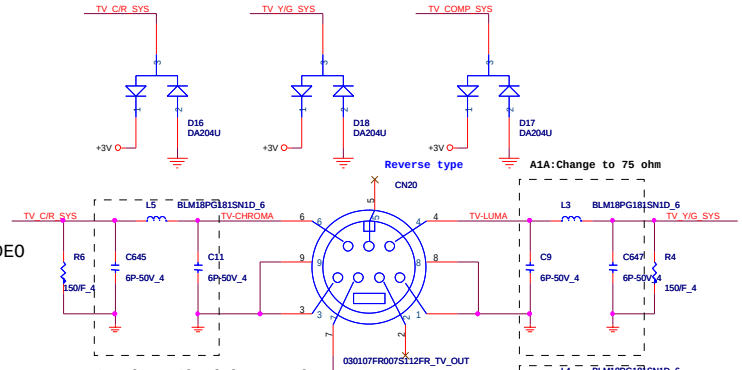


D2B:Add D41,R773 to resolve WOL issue

SEL	FUN
H	B2
L	B1

TO EZ4

S-VIDEO

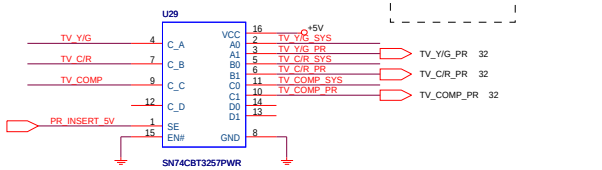


TV Out (SVHS) MiniDIN 7-pin

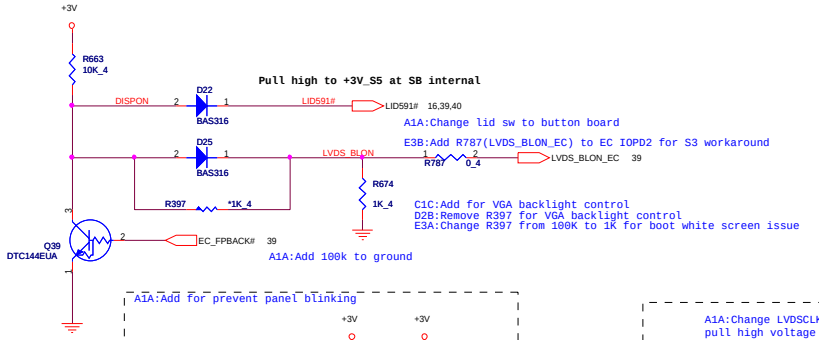
A1A:Change SVIDEO footprint to SV-030107FR007S108FU-RVS-7P

C2A:Change CN20 SVIDEO p/n to DFMD07FR206

E3B:Change R4,R5,R6 to 150 ohm for TV can't detect issue



A1A:Change to SN74CBT3257PWR(Vin 5V)

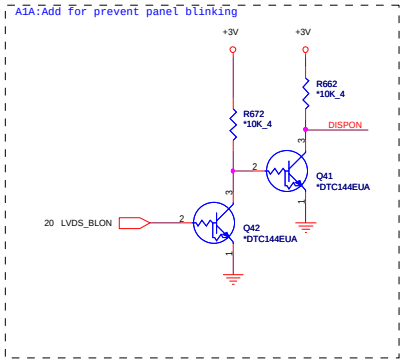


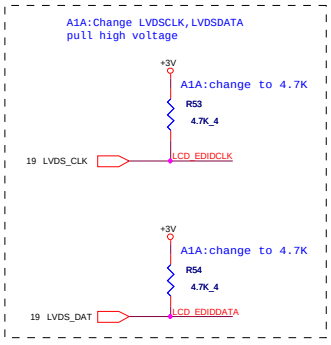
A1A:Change lid sw to button board

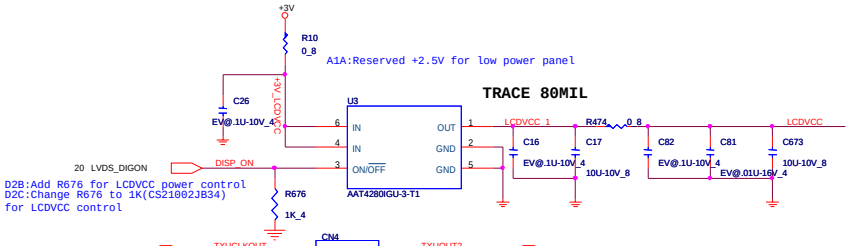
E3B:Add R787(LVDS_BLON_EC) to EC IOPD2 for S3 workaround

C1C:Add for VGA backlight control
D2B:Remove R397 for VGA backlight control
E3A:Change R397 from 100K to 1K for boot white screen issue

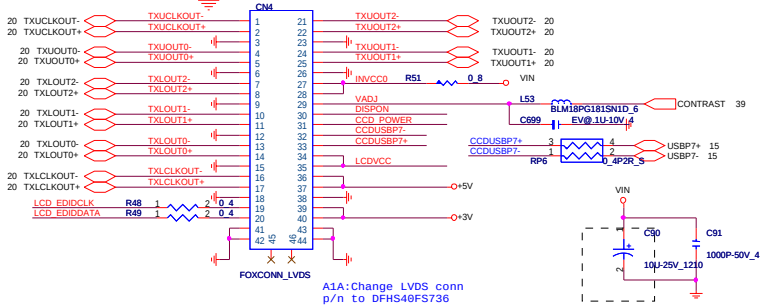
A1A:Add 100k to ground





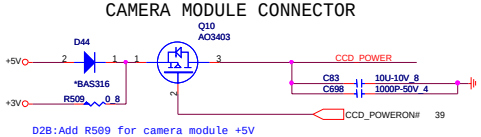


D2B:Add R676 for LCDVCC power control
D2C:Change R676 to 1K(CS21002JB34) for LCDVCC control



A1A:Change LVDS conn p/n to DFHS40FS736

CAMERA MODULE CONNECTOR



D2B:Add R509 for camera module +5V

PROJECT : ZC1			
Quanta Computer Inc.			
Size	Document Number: LVDS DVI-I TV-OUT CONNECTOR		Rev: 1A
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near switch

19 R_DAC1
19 G_DAC1
19 B_DAC1
R463 EV@0_4 VGA_RED
R462 EV@0_4 VGA_GRN
R483 EV@0_4 VGA_BLU

19,24 VSYNC_DAC1
19,24 HSYNC_DAC1
RN6 EV@0_4P2R_S VSYNC HSYNC

19 CRT1DDCDATA
19 CRT1DDCCLK
RN7 EV@0_4P2R_S CRTDDAT CRTDCLK

B1B:Remove UMA CRT support

U31
VGA_RED 4 C_A
VGA_GRN 7 C_B
VGA_BLU 9 C_C
12 C_D
25,32 PR_INSERT_5V PR_INSERT_5V 1 SE
15 EN#
VCC 16 +5V
A0 2 VGA_RED_SYS
A1 3 VGA_RED_PR
B0 5 VGA_GRN_SYS
B1 6 VGA_GRN_PR
C0 11 VGA_BLU_SYS
C1 10 VGA_BLU_PR
D0 14
D1 13
GND 8
SN74CBT3257PWR

VGA_RED_PR 32
VGA_GRN_PR 32
VGA_BLU_PR 32

+5V
C683 EV@.1U-10V_4
C51 EV@.1U-10V_4
C686 EV@.1U-10V_4

A1A:Change to SN74CBT3257PWR(Vin 5V)

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

C37 EV@.1U-10V_4

B1B:Change CRT p/n to DFHS15FR057
Reverse type

+5V F3 POLY_SWITCH_1.1A CRTVDD2 D3 SSM14 CRTVDD3
25 MIL

CN23
VGA_RED_SYS L2 BLM18BA220SN1_6 CRT_R1
VGA_GRN_SYS L13 BLM18BA220SN1_6 CRT_G1
VGA_BLU_SYS L14 BLM18BA220SN1_6 CRT_B1
T2
CRT

R2 150/F_4 C642 10P-50V_4 R18 150/F_4 C34 10P-50V_4 R24 150/F_4 C39 10P-50V_4 C677 10P-50V_4 C672 10P-50V_4 C643 10P-50V_4

A1A:delete CRT_SENSE#

A1A:Change to 75 ohm
PLACE RGB TERMINATION RESISTORS,FILTERING CLOSE TO CONNECTOR

E3B:Change R2,R18,R24 to 150 ohm for CRT can't detect issue

+3V R23 2.2K_4 R22 2.2K_4
CRTDCLK
CRTDDAT
A1A:Pull high to 3.3V

B1B:Change U30 pin1,8,9,12 to CRTVDD3

U30
CRTVDD3 1 VCC_SYNC
+5V 7 VCC_DDC
CRTVDD3 8 BYP
+3V 2 VCC_VIDEO
VGA_RED_SYS 3 VIDEO_1
VGA_GRN_SYS 4 VIDEO_2
VGA_BLU_SYS 5 VIDEO_3
6 GND
SYNC_OUT2 16
SYNC_OUT1 14
SYNC_IN2 15 VSYNC
SYNC_IN1 13 HSYNC
DDC_IN1 10 CRTDCLK
DDC_IN2 11 CRTDDAT
DDC_OUT1 9 DDCCLK_1
DDC_OUT2 12 DDCDAT_1
CM2009-02QR

VSYNC_EZ4 32
HSYNC_EZ4 32
L52 BLM18BA220SN1_6 CRTVSYNC
L51 BLM18BA220SN1_6 CRTHSYNC
C681 10P-50V_4 C679 10P-50V_4
CRTVDD3 R482 2.7K_4 R3 2.7K_4
DDCCLK_1 32
DDCDAT_1 32
C684 10P-50V_4 C644 10P-50V_4

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Quanta Computer Inc.

Size	Document Number	Rev
	CRT-PORT	1A
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B1B:Add R723,C959 for LAN_PWR_GOOD

A1A:Change GLAN from PCIE5 to PCIE1

after all power rail OK 80ms

Stuff R488 for D3_wake up

A1A:Leave ball C3, DOCK_IND, unconnected. This feature is not supported in the 82573.

Pull up to +3V_S5 on SB side

A1A:Add PCIE_WAKE# circuit

A1A:No_Stuff R391,It is for Tekoa Validation support only

A1A:Place termination resistors and caps as close to LAN controller as possible

A1A:Installed R484 when use shared mode

Install to use SPI FLASH (Tekoa only)

Install when sharing SPI Flash with the ICH7

Install R487 to disable NVM protection

add suport S5 wake up on LAN solution

Dedicated LAN Flash

A1A:add 47 ohms for SPI EEPROM program

A1A:These resistors should be placed less than 0.5" from the Shared Flash

B1B:Change U32(SST25LF080) WP# to LANVCC

A1A:These capacitors should be placed less than 0.5" from the LAN Controller

B1B:Change Q5,Q28 footprint to SOT-223(SMT issue)

M2(Fuse Supply). This should be connected to 2.5V for normal operation.

reduce the ripple

compensate for undershoot

Install to disable Internal 2.5V regulator

LAN Disable Circuit

A1A:Stuff R57 and not stuff R55 to disable LAN

GPIO24(Not cleared by CF9h reset event
Defaults to high on power up, is powered from the resume well, and retains its value during PCI reset

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	Gigalan Tekoa 82573E	1A
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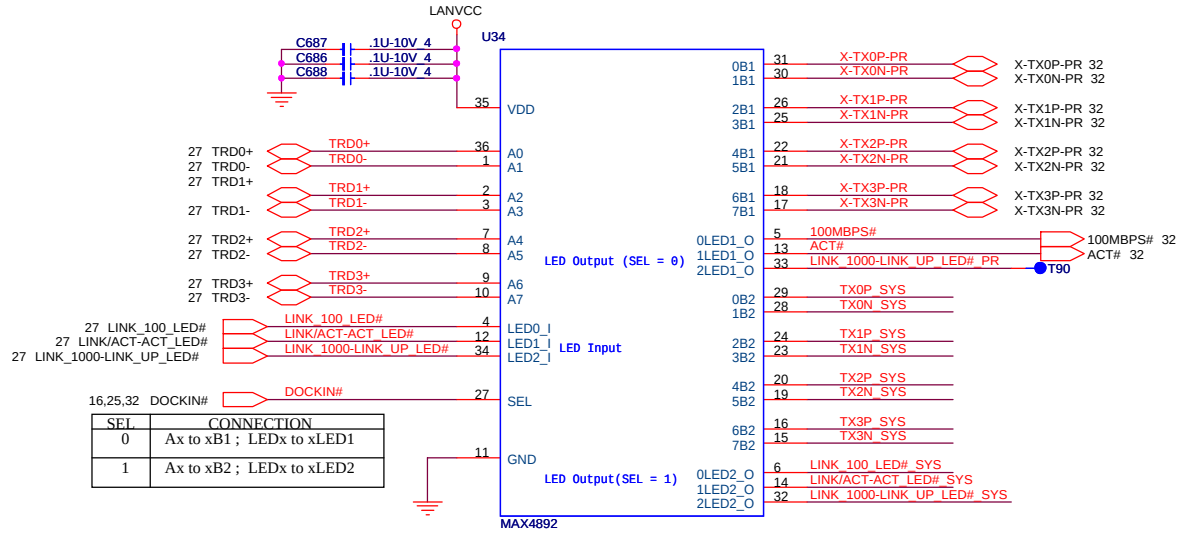
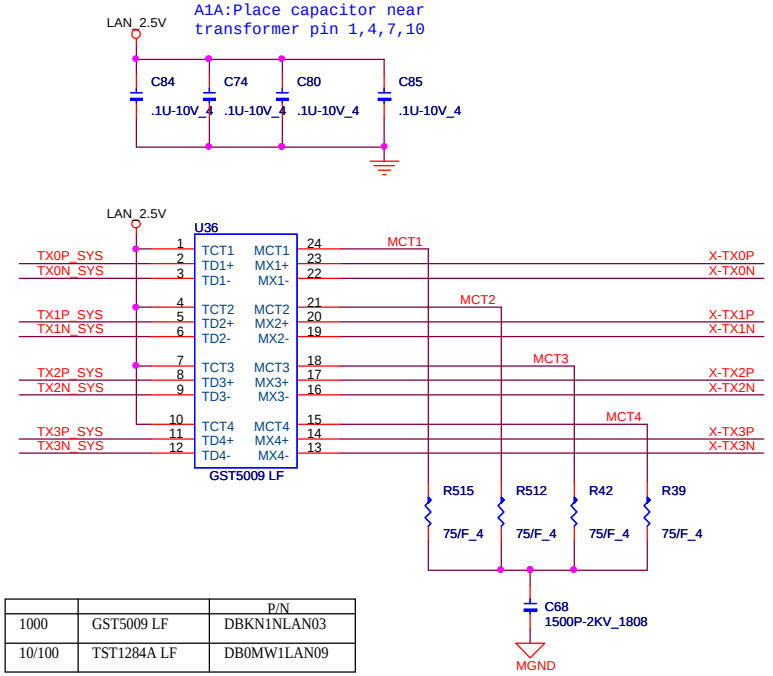


SEL	CONNECTION
0	Ax to xB1 ; LEDx to xLED1
1	Ax to xB2 ; LEDx to xLED2

LED0 Input
0LED1 Output. Connects LED0 to 0LED1 when SEL = 0.
0LED2 Output. Connects LED0 to 0LED2 when SEL = 1.

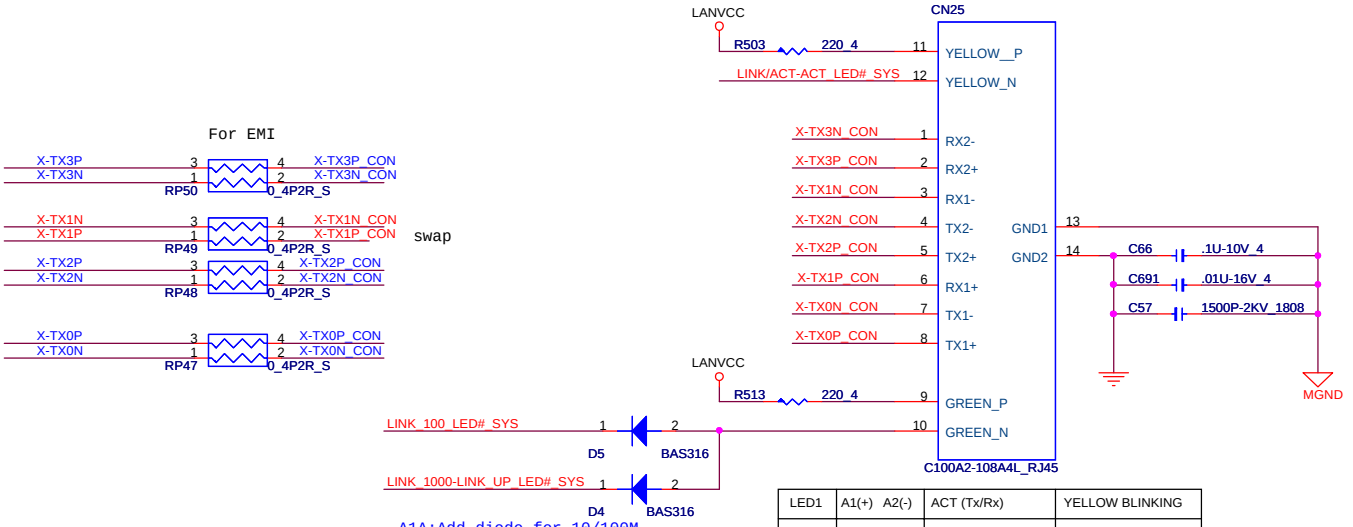
B1B:Change MAX4892 pin define

A1A:Place capacitor near transformer pin 1,4,7,10



		P/N
1000	GST5009 LF	DBKN1NLAN03
10/100	TST1284A LF	DB0MW1LAN09

A1A:Change RJ45 CONN to C100A2-108A4L
A1A:Change RJ45 TX,RX pin define



A1A:Add diode for 10/100M & 1000M led control

LED1	A1(+) A2(-)	ACT (Tx/Rx)	YELLOW BLINKING
LED2	B1(+) B2(-)	LINK 10/100/1000	GREEN

PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	TRANSFORMER/RJ45	A
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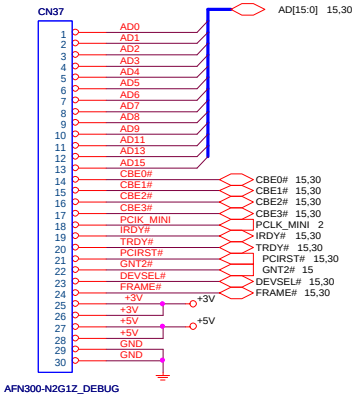
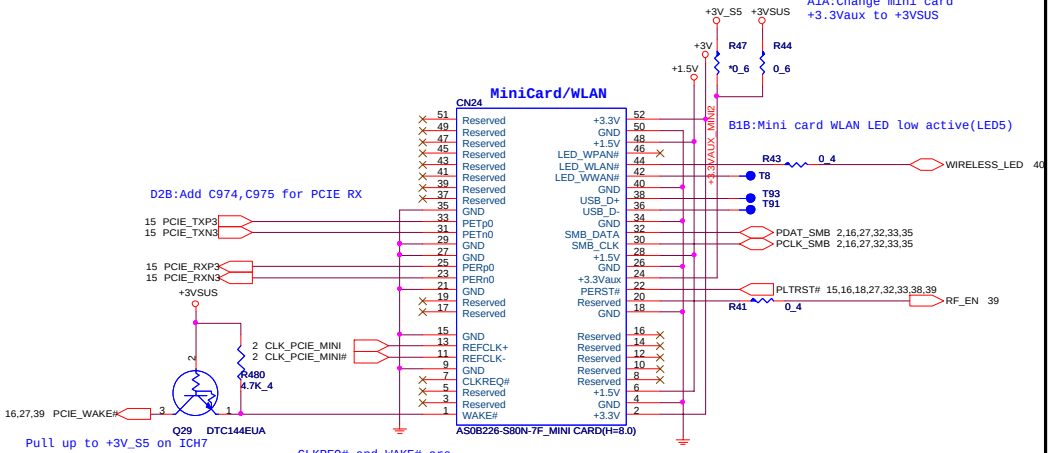
Debug card interface

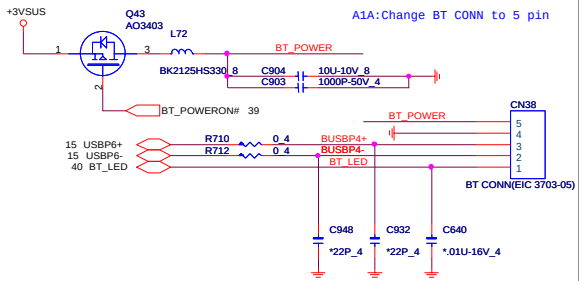
BOT contact



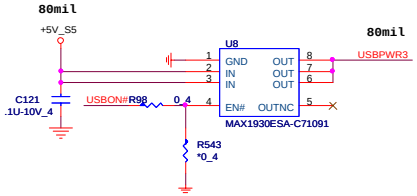
MiniCard/WLAN

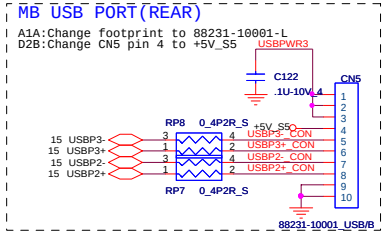


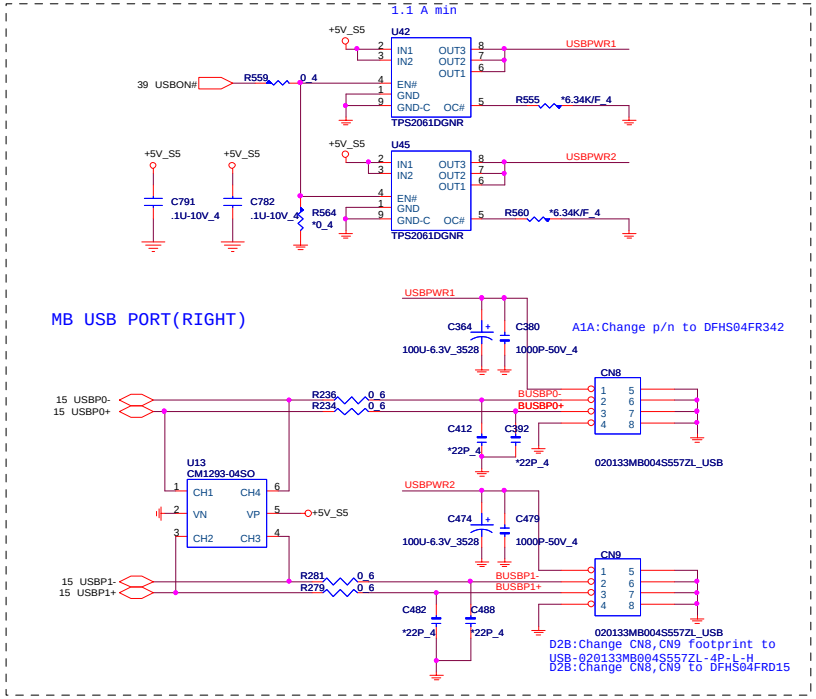
BLUETOOTH MODULE CONNECTOR



A1A:In adapter mode, should be powered during S0~S5.
In battery only mode, should be powered during S0 and S3, and not powered during S5







PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	DEBUG CARD&PCI-E card&USB	1A
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Place near U183 K4,P9,E7 ...

C833 10U-10V_8 | C860 .1U-10V_4 | C850 .1U-10V_4 | C858 .1U-10V_4 | C861 .1U-10V_4

A1A:Connect A_VPP to A_VCC since the Oz711MP1 do not control the VPP of OZ2211

O2MICRO OZ2211 16PIN SINGLE SLOT PARALLEL POWER SWITCH(THIS IMPLEMENTATION DOES NOT SUPPORT 12V VPP.

A1A:Change cardbus headr to 130601-5(H=0)
TOP MOUNT

CN12

U51A — OZ711MP1BN

Reserve for EMI

Place near U182(power switch)

OZ2211SN

CARDBUS SLOT
SANTA-130601-5-68P

C1C:Change Smart card schematic

D2B:Add D35,C965,C966 for smart card VCC

D2B:Change R759 From CS34703J901 to CS34702JB21

C2A:Ad R774 for SC_DET#

B1B:Add U63 for Cardbus detect
D2B:Remove U63 for Cardbus detect

CN10
85201-12021_SCR_CONN
R/A Top Contact

PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
	OZ711MP1-PCMCIA-SMART CARD	1A
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A1A:1394 function of OZ711MP1 do not used the EEPROM , and Oz711MP1 put the GUID in PCI register , So , 24Lc02BT can be remove

A1A:Change the C1885 filter Cap value from 270 pf to 820 pf

A1A:Change1394 footprint to 1394-020204fr004s502zx-c-4p-v

B1B:Change pin 7,8 to GND

B1B:Change 1394 p/n to DFHS04FS578

E3A:Change 1394 footprint to 1394-020204fr004s109zl-4p-v8

5pF attached to SD_D0 and GND for 48M compatibility issue

External xD resistors

Group 1 and 2 not populated:
Firmware in Internal ROM
No unique serial number

Group 2 populated:
Firmware in External FLASH
Unique serial number and configuration in FLASH

External FLASH

*SST39VF010-70-4C-WHE

C2B:Remove U49,C867,R361

Group 1 populated:
Firmware in Internal ROM
Unique serial number and configuration in EEPROM

External EEPROM

AT93C66A-10TU-2.7(TSSOP)

C2B:Stuff U16,R368

E3A:Change U16 to AR0ZC1C1009

SD/MMC

MS/MS pro

D2B:Connect CN14 pin 4,12,22,23 to GND

Check GPIO Pin & Det

SM/xD

R013-000-XX_CARD READER

6 IN1 CARD READER
(MS,MS pro,SD, MMC,xD,SDIO)

20 mil

D2B:Change C641 to 1M_4(CS51002JB21)

D2B:Change C845 to 1M_4(CS51002JB21)

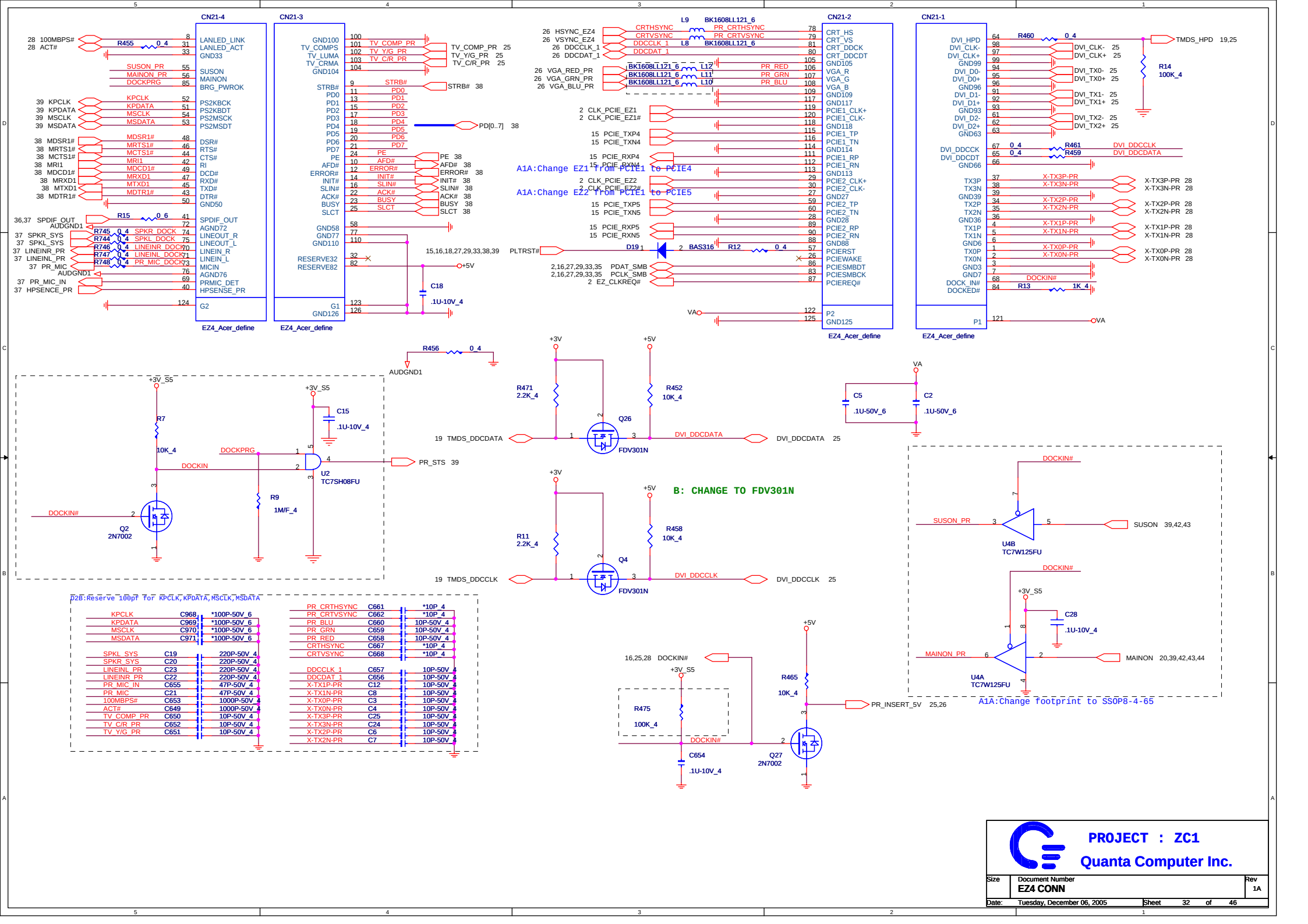
020204FR004S502ZL_1394 CONN

USB2228-NU-XX_VTQFP128

Check USB2.0 Power

Place C567 at pin 100, C542 at pin 108, and C524 at pin 89.

PROJECT : ZC1		
Quanta Computer Inc.		
Size	Document Number: OZ711MP1-IEEE1394-SMART CARD	Rev: 1A
Date: Wednesday, November 30, 2005	Sheet 31 of 46	


CN21-4
CN21-3
CN21-2
CN21-1
EZ4_Acer_define
A1A:Change EZ1 from PCIE1 to PCIE4
A1A:Change EZ2 from PCIE1 to PCIE5
B: CHANGE TO FDV301N
D2B:Reserve 100pf for KPCLK,KPDATA,MSCLK,MSDATA
A1A:Change footprint to SSOP8-4-65
PROJECT : ZC1
Quanta Computer Inc.
EZ4 CONN
Tuesday, December 06, 2005

+NEW_1.5V Max. 650mA, Average 500mA.
+NEW_3V Max. 1300mA, Average 1000mA.

A1A:Change New card power sw to Oz27c10

A1A:Change New card to small type(130832-1)

Reverse

U20

ExpressSwitch

R5538D001-TR-F/OZ27C10LN

Place near U20

Place near U20

D2B:Remove HOLE6

TPM

CPU

MDC

POWER/B

MINI CARD

Thermal module

Place near CN35

CN35

130832-1_NEW CARD

B1B:Change HOLE8,27 footprint

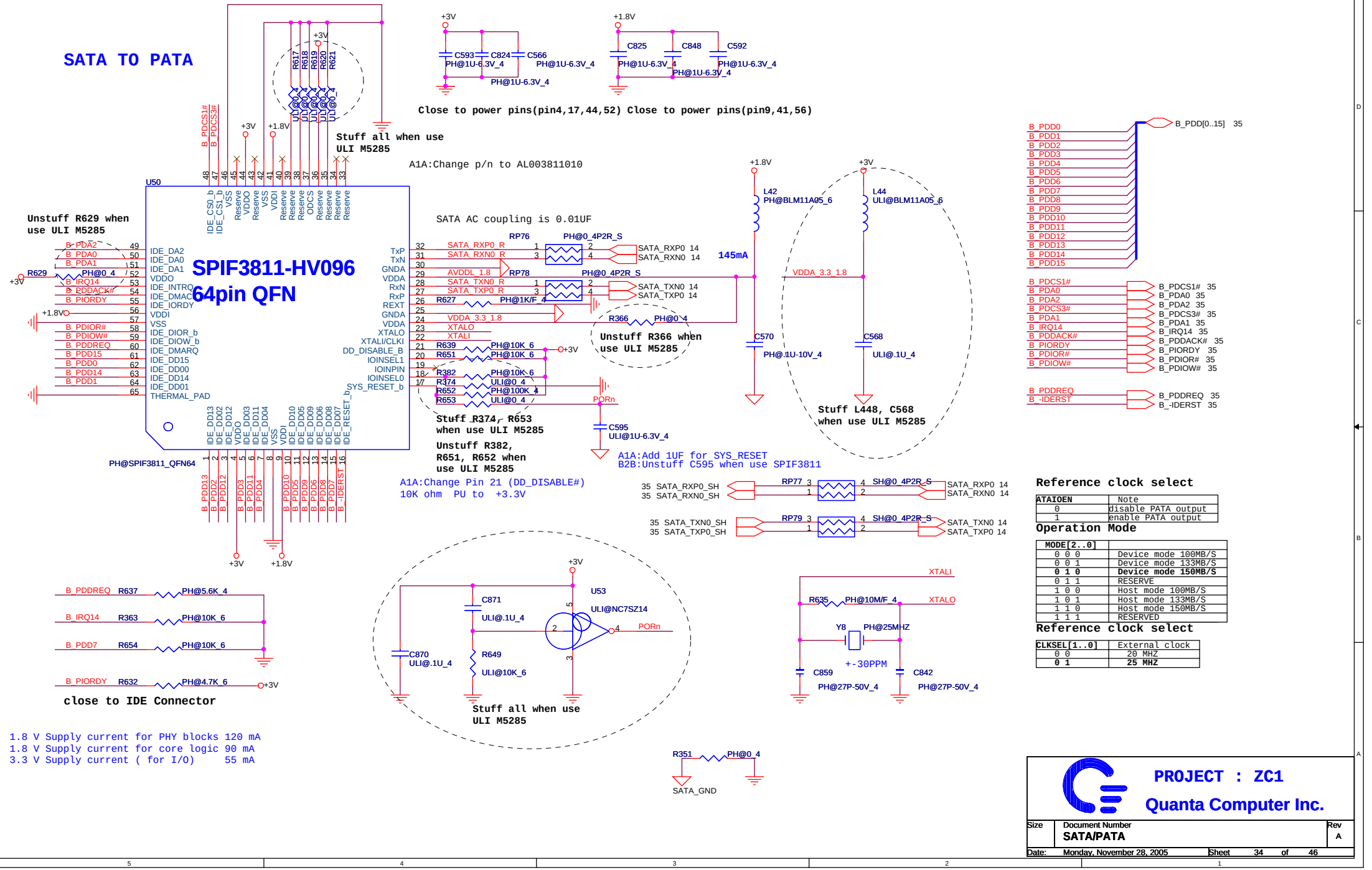
PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	NEW CARD &HOLE	C

Date: Monday, November 28, 2005 Sheet 33 of 46

SATA TO PATA



Reference clock select

ATAIOEN	Note
0	disable PATA output
1	enable PATA output

Operation Mode

MODE[2..0]	
0 0 0	Device mode 100MB/S
0 0 1	Device mode 133MB/S
0 1 0	**Device mode 150MB/S**
0 1 1	RESERVE
1 0 0	Host mode 100MB/S
1 0 1	Host mode 133MB/S
1 1 0	Host mode 150MB/S
1 1 1	RESERVED

Reference clock select

CLKSEL[1..0]	External clock
0 0	20 MHZ
0 1	**25 MHZ**

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	SATA/PATA	A

Date: Monday, November 28, 2005 Sheet 34 of 46

From SATA -> PATA bridge

BOM
SH@,PH@

A1A:Change PATA to C178D4-14401-L

CSEL:
0 DRIVE0
1 DRIVE1

A1A:Change SATA to C16654-122A4-L

B1B:Reserved +3V for security alarm cicuit

A1A:Add for HDD protect(G-sensor)

E3B:Change U14 to KXP84-2050(new version IC)

Bandwidth control(250HZ)

Slave Address = 001100XX = 0x30

I2C/SPI mode selection (1 = I2C mode, 0 = SPI mode)

From ICH7 bridge

Media Bay Connector

BAY ID STATUS

RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	0	FDD
0	1	HDD
1	0	CD/DVD

B1B:Remove R141,R545,Q32 for -IDERST

B1B:Add MOS for G sensor SMBUS
D2B:Change Q48,Q49 VCC to +3VSUS
D2B:Add R269,R434 for SMBUS PU resistor
D2B:Add R411,R433 for SMBUS

D2B:Add C967,R775,D43 for G sensor reset

A1A:change -PDIAG to B_-PDIAG
C2A:Stuff R161,set ODD to Master
C2A:Remove R173 for RBAYID

C2A:Remove R139,R145 for RBAYVCC(FDD)

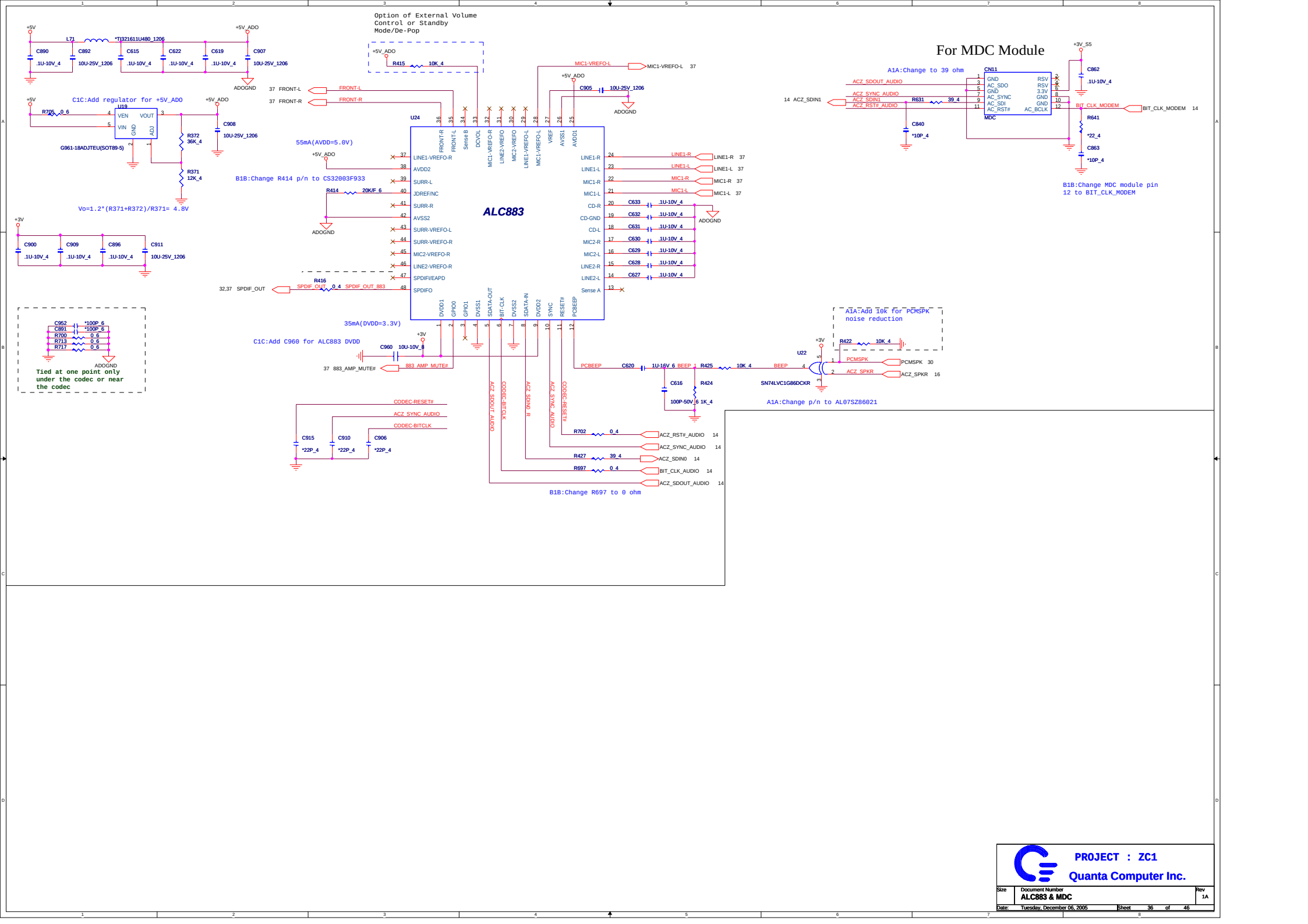
ADD DISCHARGE CIRCUIT

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM & MEDIA BAY	C

Date: Friday, December 09, 2005 Sheet 35 of 46


Option of External Volume Control or Standby Mode/De-Pop
For MDC Module
ALC883
C1C:Add regulator for +5V_ADO
Vo=1.2*(R371+R372)/R371= 4.8V
55mA(AVDD=5.0V)
B1B:Change R414 p/n to CS32003F933
35mA(DVDD=3.3V)
C1C:Add C960 for ALC883 DVDD
Tied at one point only under the codec or near the codec
A1A:Change to 39 ohm
B1B:Change MDC module pin 12 to BIT_CLK_MODEM
A1A:Add 10k for PCMSPK noise reduction
A1A:Change p/n to AL07SZ86021
B1B:Change R697 to 0 ohm
PROJECT : ZC1
Quanta Computer Inc.
ALC883 & MDC
Tuesday, December 06, 2005

Audio amplifier

A1A:Change audio amplifier to MAX9750
A1A:Change footprint to tqfn28-5x5-5-33p

D2C:Change R693,R699 from 0 to 5.1K to solve audio performance issue.

Low--->Speak Mode
Hi ---->HP

MAX : 0 V
MIN : 2.8 V (1.5K)

E3B:Remove D13 for Audio Bo Bo sound

GAIN2	GAIN1	SPKR MODE	HP MODE
0	0	6	0
0	1	7.5	
1	0	9	3
1	1	10.5	

LINE OUT/SPDIF

BLACK

HPPLG#:
HP not insert->H
HP insert->L

Pin5 connect to Pin3 on Jack

D2B:Change CN17 to DFTJ10FR356

C2A:Change Line out schematic

E3A:Remove Q45,add R790 for SPDIF can't use issue

For ESD close to audio out connecter

C2A:Change Line out schematic

LINE IN

BLUE

C2A:Change CN18 to DFTJ06MS716

MIC

PINK

D2B:Change R435 to 2.2K to meet MIC voltage reference

C2A:Change CN19 to DFTJ06MS724

D2B:Reserve R726 for EMI request

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

C1C:Reversed for ESD(MIC)

For ESD close to audio out connecter

SPEAKER CONNECTOR

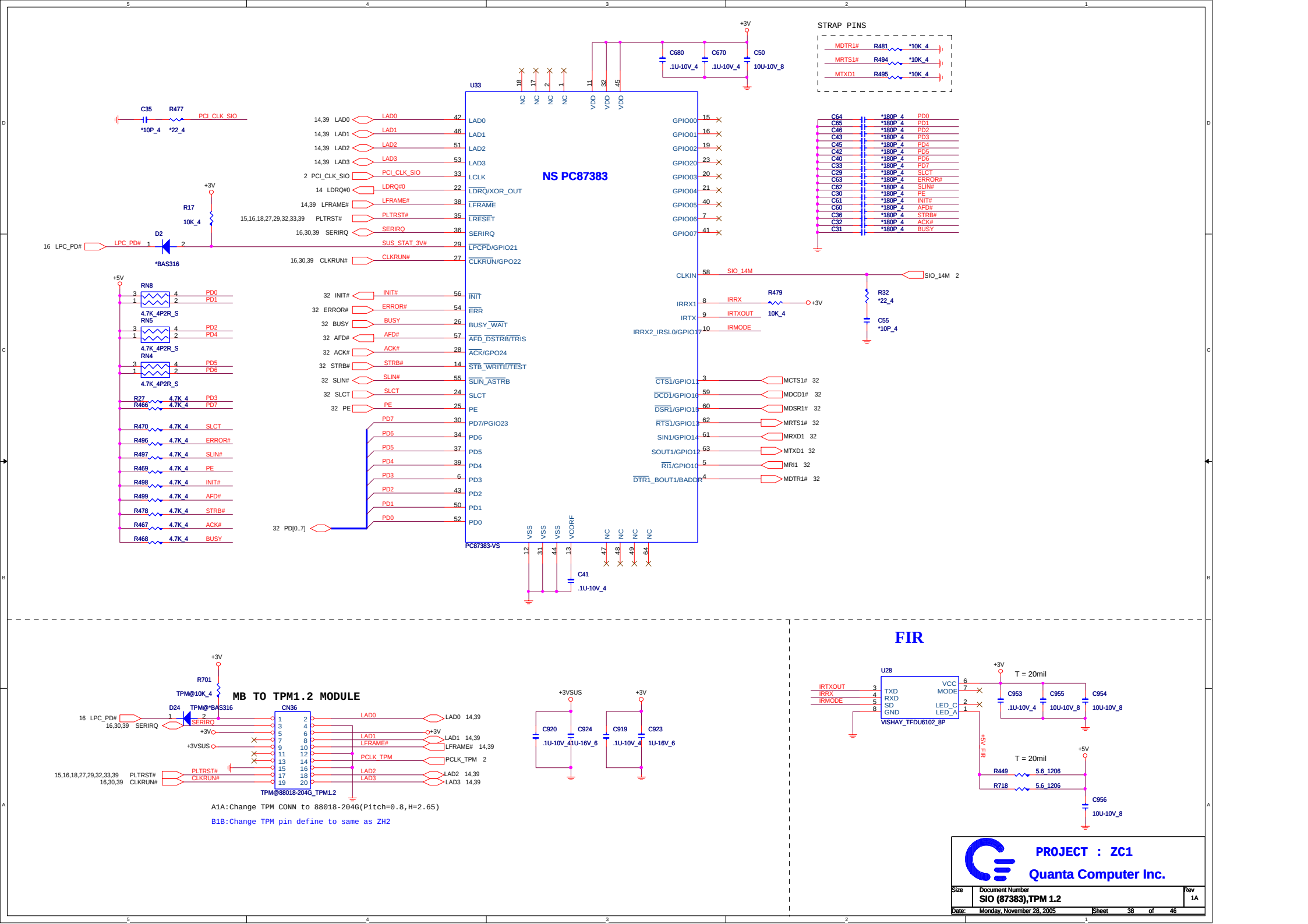
A1A:Change Speaker conn footprint

B1B:Change speaker p/n to DFHD04MR701

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP(MAX9750) / JACK	1A
Date: Saturday, December 10, 2005	Sheet 37 of 46	


STRAP PINS
MDTR1# R481 *10K_4
MRTS1# R494 *10K_4
MTXD1 R495 *10K_4
U33
NS PC87383
PC87383-VS
LAD0
LAD1
LAD2
LAD3
LCLK
LDRQ/XOR_OUT
LFRAME
LRESET
SERIRQ
LPCPD/GPIO21
CLKRUN/GPO22
INIT
ERR
BUSY_WAIT
AFD_DSTRB/TRIS
ACK/GPO24
STB_WRITE/TEST
SLIN_ASTRB
SLCT
PE
PD7/PGIO23
PD6
PD5
PD4
PD3
PD2
PD1
PD0
GPIO00
GPIO01
GPIO02
GPIO20
GPIO03
GPIO04
GPIO05
GPIO06
GPIO07
CLKIN
IRRX1
IRTX
IRRX2_IRSL0/GPIO17
IRRX
IRTXOUT
IRMODE
CTS1/GPIO11
DCD1/GPIO16
DSR1/GPIO15
RTS1/GPIO13
SIN1/GPIO14
SOUT1/GPIO12
RI1/GPIO10
DTR1_BOUT1/BADDR
MCTS1# 32
MDCD1# 32
MDSR1# 32
MRTS1# 32
MRXD1 32
MTXD1 32
MRI1 32
MDTR1# 32
SIO_14M
SIO_14M 2
R32 *22_4
C55 *10P_4
R479 10K_4
+3V
+5V
C680 .1U-10V_4
C670 .1U-10V_4
C50 10U-10V_8
C35 *10P_4
R477 *22_4
PCI_CLK_SIO
R17 10K_4
D2 *BAS316
LPC_PD#
SUS_STAT_3V#
CLKRUN#
LDRQ#0
LFRAME#
PLTRST#
SERIRQ
INIT#
ERROR#
BUSY
AFD#
ACK#
STRB#
SLIN#
SLCT
PE
PD[0..7]
RN8 4.7K_4P2R_S
RN5 4.7K_4P2R_S
RN4 4.7K_4P2R_S
R27 4.7K_4
R466 4.7K_4
R470 4.7K_4
R496 4.7K_4
R497 4.7K_4
R469 4.7K_4
R498 4.7K_4
R499 4.7K_4
R478 4.7K_4
R467 4.7K_4
R468 4.7K_4
C64 *180P_4 PD0
C65 *180P_4 PD1
C46 *180P_4 PD2
C43 *180P_4 PD3
C45 *180P_4 PD4
C42 *180P_4 PD5
C40 *180P_4 PD6
C33 *180P_4 PD7
C29 *180P_4 SLCT
C63 *180P_4 ERROR#
C62 *180P_4 SLIN#
C30 *180P_4 PE
C61 *180P_4 INIT#
C60 *180P_4 AFD#
C36 *180P_4 STRB#
C32 *180P_4 ACK#
C31 *180P_4 BUSY
C41 .1U-10V_4
MB TO TPM1.2 MODULE
R701 TPM@10K_4
D24 TPM@*BAS316
CN36
TPM@88018-204G_TPM1.2
C920 .1U-10V_4
C924 1U-16V_6
C919 .1U-10V_4
C923 1U-16V_6
A1A:Change TPM CONN to 88018-204G(Pitch=0.8,H=2.65)
B1B:Change TPM pin define to same as ZH2
FIR
U28
VISHAY_TFDU6102_8P
T = 20mil
C953 .1U-10V_4
C955 10U-10V_8
C954 10U-10V_8
C956 10U-10V_8
R449 5.6_1206
R718 5.6_1206
PROJECT : ZC1
Quanta Computer Inc.
Size
Document Number
SIO (87383),TPM 1.2
Rev 1A
Date: Monday, November 28, 2005
Sheet 38 of 46

Adapter ID	
Watt	Voltage
65W	0.66 +/- 0.1V
90W	1.32 +/- 0.1V
135W	1.98 +/- 0.1V
150W	2.64 +/- 0.1V
Un-define	3.3 +/- 0.1V

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

LDRQ#(pin 8) internal is no use

A1A:Reserved GSENSOR-X/Y/Z for security alarm cicuit

A1A:Remove REFON pin (DA3 pin 102)

D2B:Add RST_KXP84_EC for G sensor reset(IOPA6)

D2B:Add G_Sensor SMBUS to EC(SCL2,SDA2)

D2B:Change EC_FPBACK# to IOPC6

D2B:Change Cardbus detect to IOPD0

SST 1MB BIOS (AKE35ZAKK17)

ST Micro M29W008AB/AMD-29LV081B/SST39VF080

B1B:Reversed for G sensor buzzer

D2B:Change buzzer power to +5V,increase volume

SHBM=1: Enable shared memory with host BIOS

BIU configuration should match flash speed used

A1A:Reserved for debug use

B1B:Change SW4 p/n to DHP00BB1J03

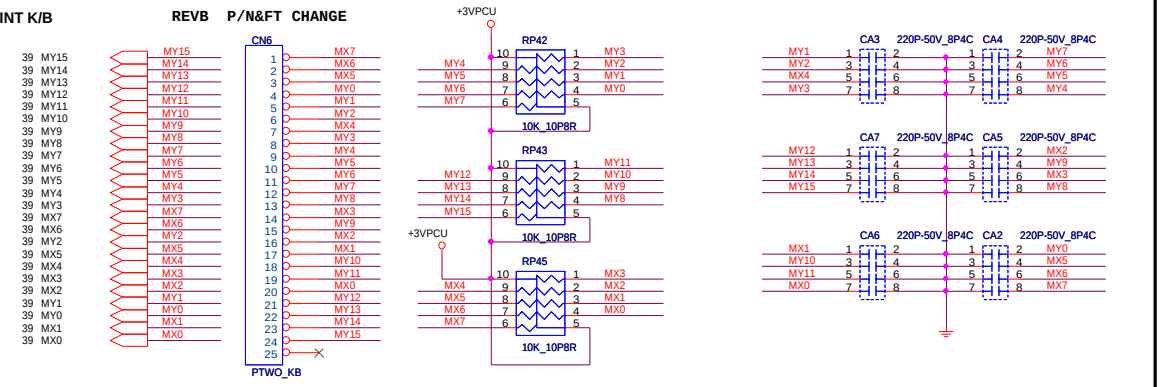
INTERNAL PULLUP IN SB

FOR 97551 ONLY

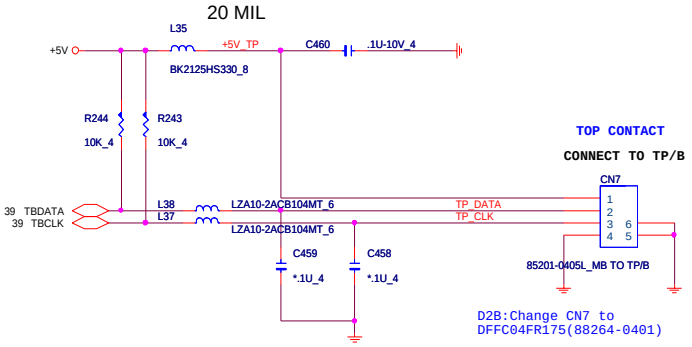
PROJECT :	ZC1
Quanta Computer Inc.	
Size	Document Number: 97551 & FLASH
Rev	1A
Date:	Friday, December 02, 2005
Sheet	39 of 46

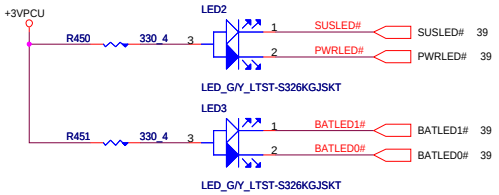
INT K/B

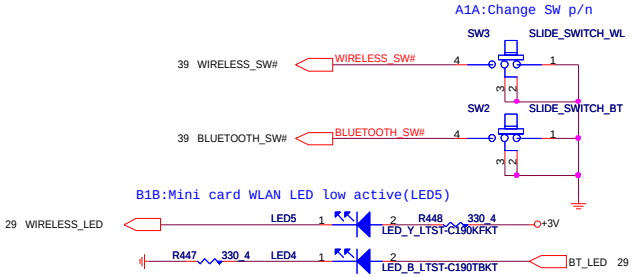
REVB P/N&FT CHANGE

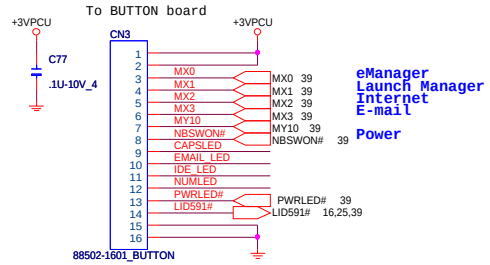


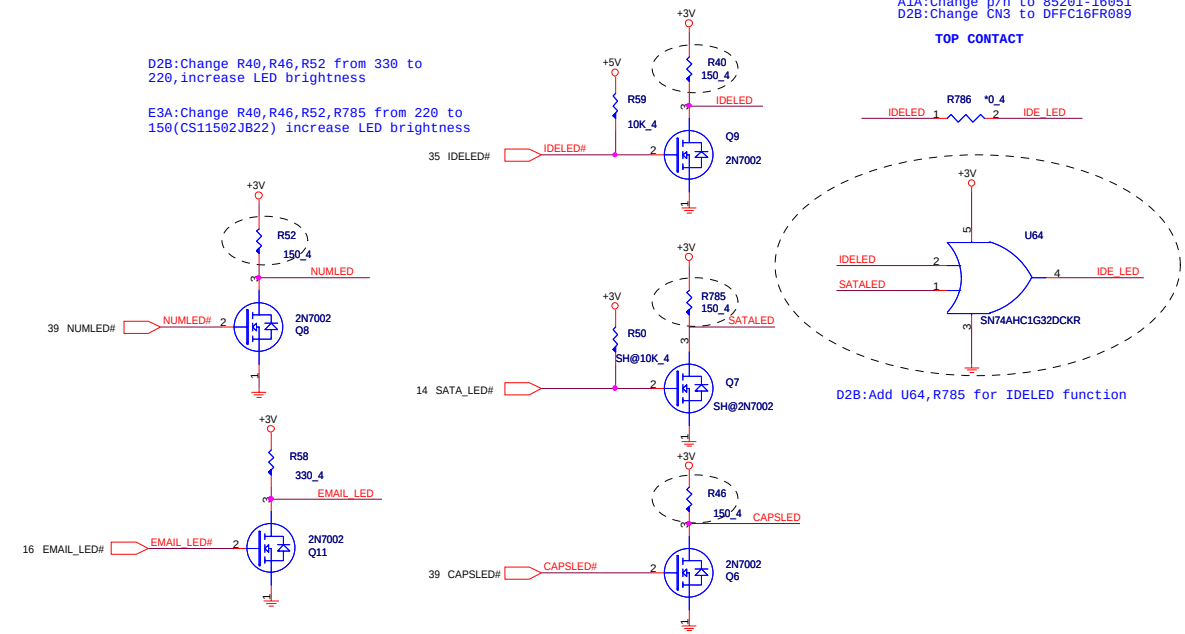
TOUCH PAD









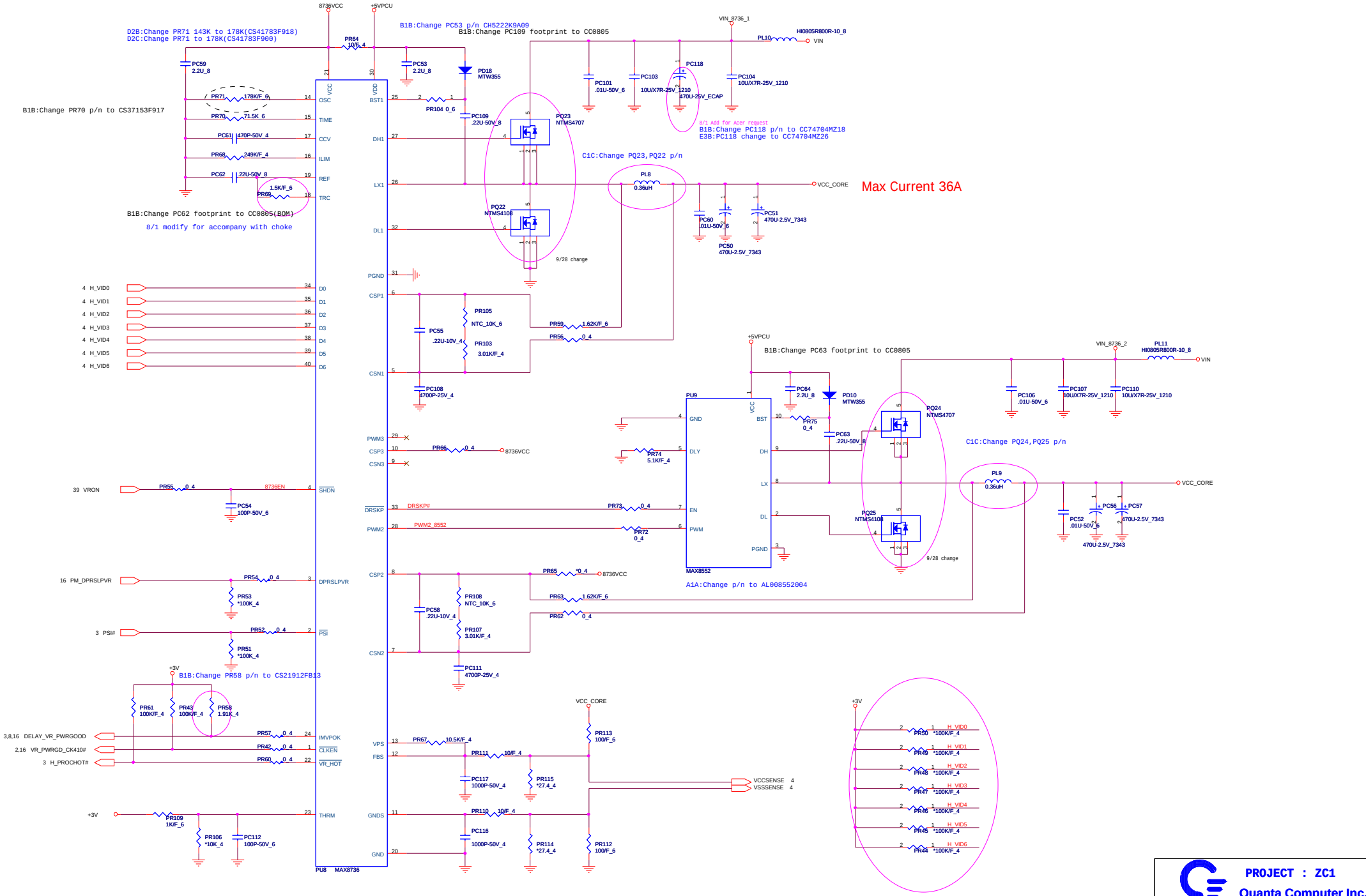


PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	SWITCH,LED,K/B,TP	1A

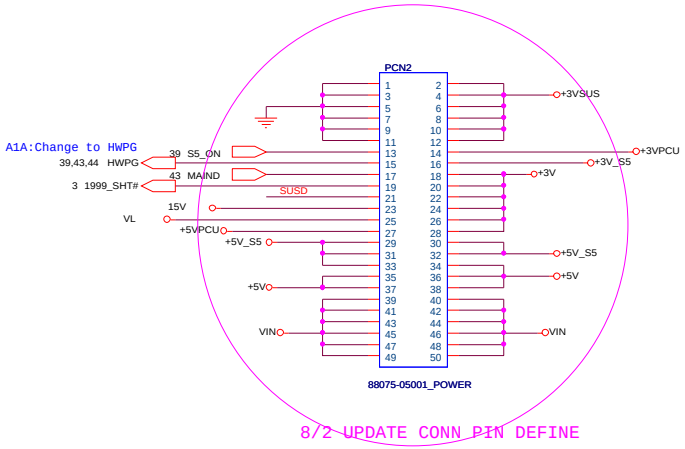
Date: Saturday, December 10, 2005 Sheet 40 of 46



PROJECT : ZC1

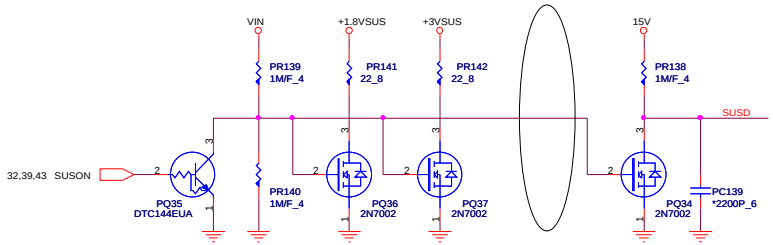
Quanta Computer Inc.

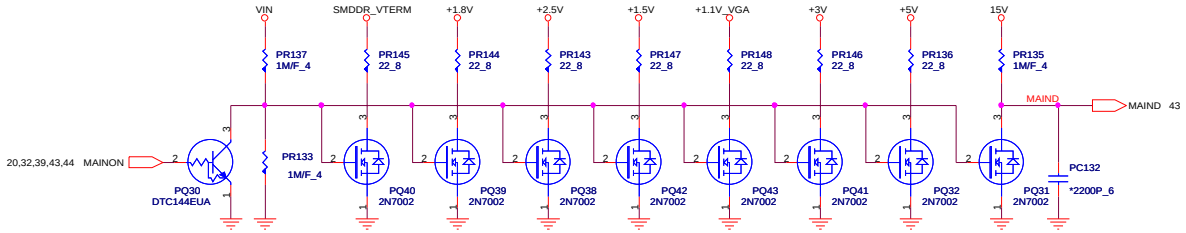
Size	Document Number	Rev
	VCORE (MAX8736)	1A
Date: Saturday, December 10, 2005	Sheet 41 of 46	



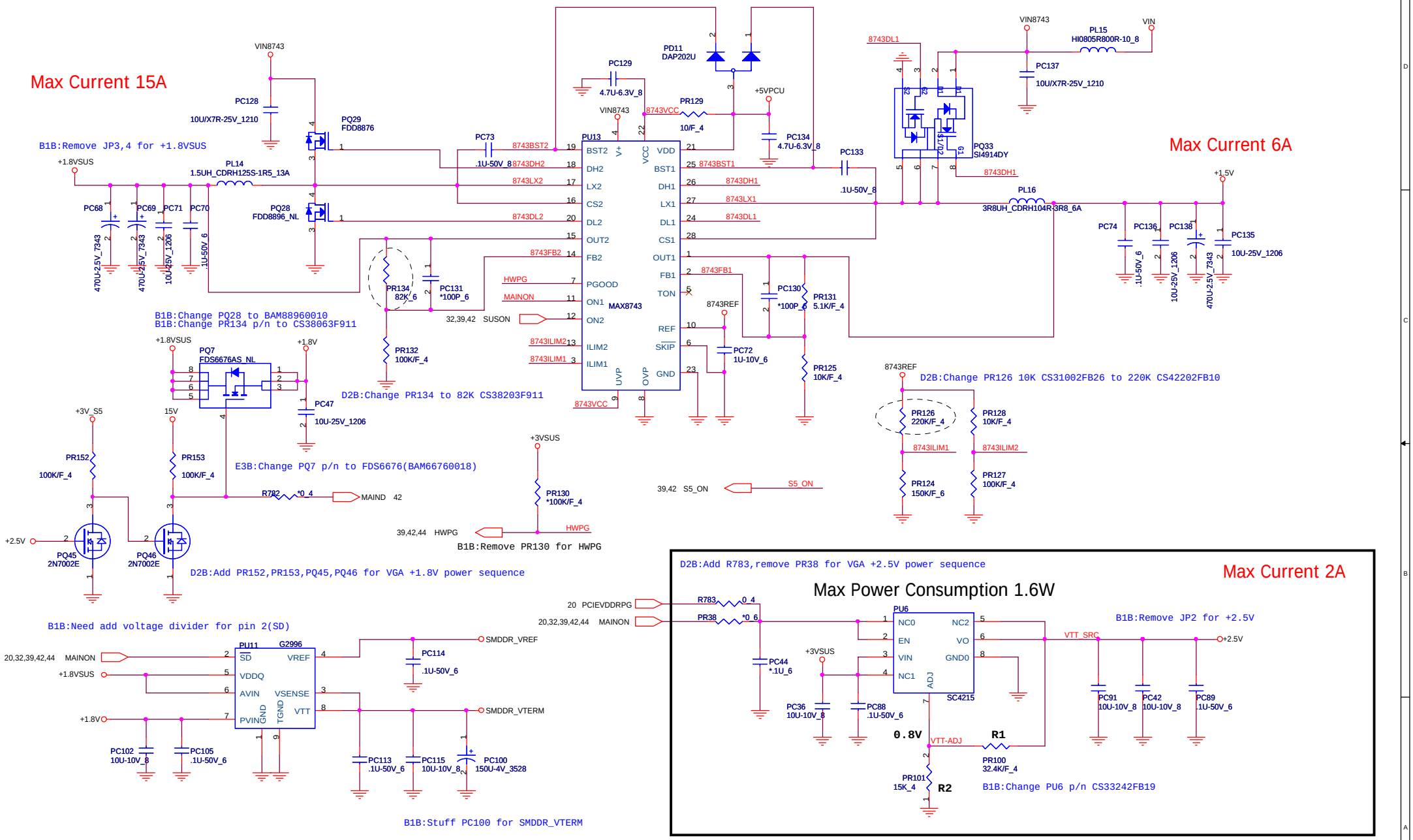
8/2 UPDATE CONN PIN DEFINE

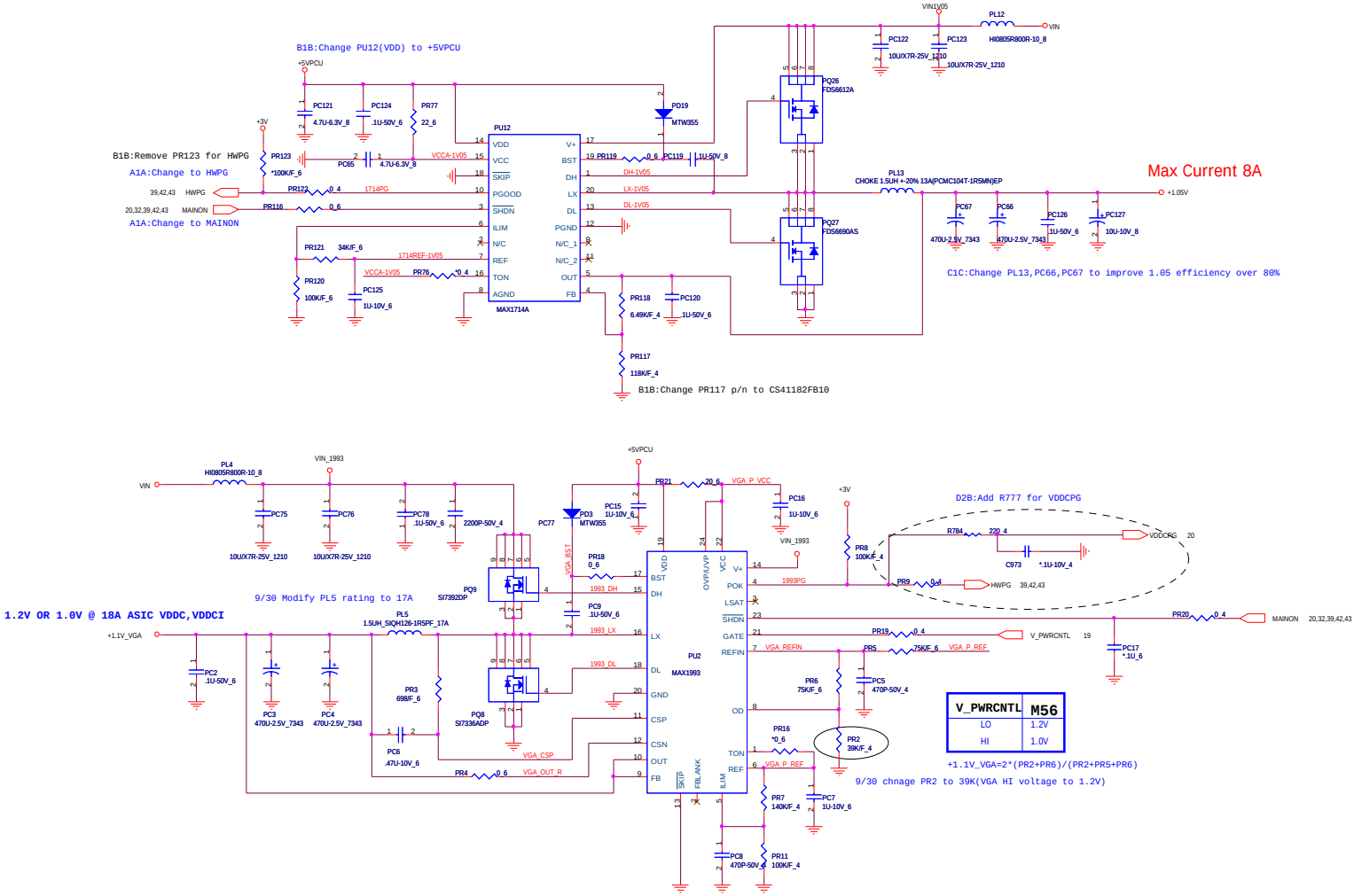
A1A:Del +5VSUS discharge





PROJECT : ZC1		
Quanta Computer Inc.		
Size	Document Number: DISCHARGE/CONNECTOR	Rev: 1A
Date: Monday, November 28, 2005	Sheet 42 of 46	


Max Current 15A
Max Current 6A
Max Current 2A
Max Power Consumption 1.6W
B1B:Remove JP3,4 for +1.8VSUS
B1B:Change PQ28 to BAM88960010
B1B:Change PR134 p/n to CS38063F911
D2B:Change PR134 to 82K CS38203F911
E3B:Change PQ7 p/n to FDS6676(BAM66760018)
D2B:Add PR152,PR153,PQ45,PQ46 for VGA +1.8V power sequence
B1B:Remove PR130 for HWPG
B1B:Need add voltage divider for pin 2(SD)
B1B:Stuff PC100 for SMDDR_VTERM
D2B:Change PR126 10K CS31002FB26 to 220K CS42202FB10
D2B:Add R783,remove PR38 for VGA +2.5V power sequence
B1B:Remove JP2 for +2.5V
B1B:Change PU6 p/n CS33242FB19
MAX8743
SC4215
PROJECT : ZC1
Quanta Computer Inc.
+2.5V/+1.8VSUS / +1.5V
Saturday, December 10, 2005
Sheet 43 of 46



PROJECT : ZC1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V/+1.2V_VGA/+1.2V	1A

Date: Monday, November 28, 2005 Sheet 44 of 46

A1A:Change footprint to 20277-05XX-5P-L

C2B:Change PJ2 to DFHD04MS988(4 PIN)
D2B:Change PJ2 footprint to 4 pin

C1C:Remove fuse,bead

B1B:Change PD17 p/n to LF

7/29 Modify for 3 cell setting

8/16 Change for 5R6 choke

Charge Current max setting = 0.8C

CURRNT LIMIT POINT = 4.5A (95% adapter power)

E3B:PR37 change from 8.25K to 6.65K(CS26653D900)
E3B:PR102 change from 14K to 10K(CS31003B919)

7/29 modife connect REFP to VIN

7/29 modife connect REF3V to +3VPCU

USE DEFAULT 4.2V/CELL

7/29 change from 4422 to 4704

7/29 delete

Size	Document Number		Rev
	BATTERY CHARGER		1A
Date:	Saturday, December 10, 2005	Sheet 45 of 46	

PROJECT : ZC1
Quanta Computer Inc.

A1A:Change p/n to DFHD07MR391
B1B:Change CN26 footprint to 20175A-07G1-7P-R

1ST_BATT_CONN

C1C:Remove fuse

D2B:Change PQ12 to FDS6679(BAM66790014)

CN26 — MAIN_BATTERY

TEMP_MBAT — TEMP_MBAT 39

MBAT+

PC12 47P-50V_4 | PC11 47P-50V_4 | PC13 1U-50V_6 | PC79 47P-50V_4 | PC19 10U/X7R-25V_1210

PR14 330_4 | PR13 330_4

MBDATA_MBAT — MBCLK 5,19,39

PD2 RLZ5.6B | PD4 ZD5.6V

CLOSE TO BATTERY CON

PQ12 FDS6679 | PQ16 AO4411

PR89 10K/F_4

PQ4 PDTC143TT — MDISCHG

ADISCHG 2 — PQ10 PDTC143TT | PQ11 IMD2

ACHG

PR86 10K/F_4

VH

PC81 .1U-50V_6

PU10A LM358ADR — PR83 1M/F_4 — MCHG

PR85 470K_6

PD13 RLZ15B

E3B:PQ19 change to FDS6676(BAM66760018)

45 BAT-V — PC83 .01U-50V_6

PQ19 AO4414-LF

PU10B LM358ADR — PR84 470K_6 — ACHG

PR82 100K/F_4

PD14 RLZ15B

C1C:Add PQ44 for charger

PQ44 AO4414-LF

REF3V — PR12 10K/F_4 — TEMP_MBAT — PC14 .01U-50V_6

PC92 10U/X7R-25V_1210

VIN

PR15 10K/F_4

PQ21 FDS6612A

PC80 .01U-50V_6

PC84 .01U-50V_6

PQ2 PDTC143TT

VA2 — VA2 45

REFP

VL

200mil

PR92 10K/F_4

PU3 74HCT237

ADISCHG

PU4B LM393

PR91 160K/F_6

PR17 10K/F_4

REF3V

PR10 100K/F_4

PQ5 PDTC143TT

PC10 .1U-50V_6

39 CELL-SET

39 D/C#

39 BL/C#

PQ3 2N7002

PR26 120K/F_4

2ND_BATT_CONN

CN27 — SECOND_BATTERY

TEMP_ABAT — TEMP_ABAT 39

PR27 330_4 | PC20 47P-50V_4 | PR28 330_4 | PC21 47P-50V_4 | PC24 .1U-50V_6 | PC22 47P-50V_4

MBCLK

MBDATA_ABAT

PD6 ZD5.6V | PD5 ZD5.6V

CLOSE TO BATTERY CON

C1C:Remove fuse

ABAT+

PC82 10U/X7R-25V_1210

PQ17 AO4411 | PQ15 AO4411

MDISCHG 2 — PQ13 PDTC143TT | PQ14 IMD2

MCHG

PR90 10K/F_4

REF3V — REF3V 45 — PR29 10K/F_4 — TEMP_ABAT — PC23 .01U-50V_6

+3VPCU

PR88 10K/F_4 | PR87 10K/F_4

1ST_BATT — MBDATA_MBAT

2ND_BATT — MBDATA_ABAT

U39 NC7SB3157P6X — VCC | IN_B1 | IN_B0 | SEL | COM | GND — M/A# — M/A# 39 — MBDATA 5,19,39

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

PROJECT : ZC1

Quanta Computer Inc.

Size	Document Number	Rev
	BATTERY SELECT	A

Date: Saturday, December 10, 2005 Sheet 46 of 46