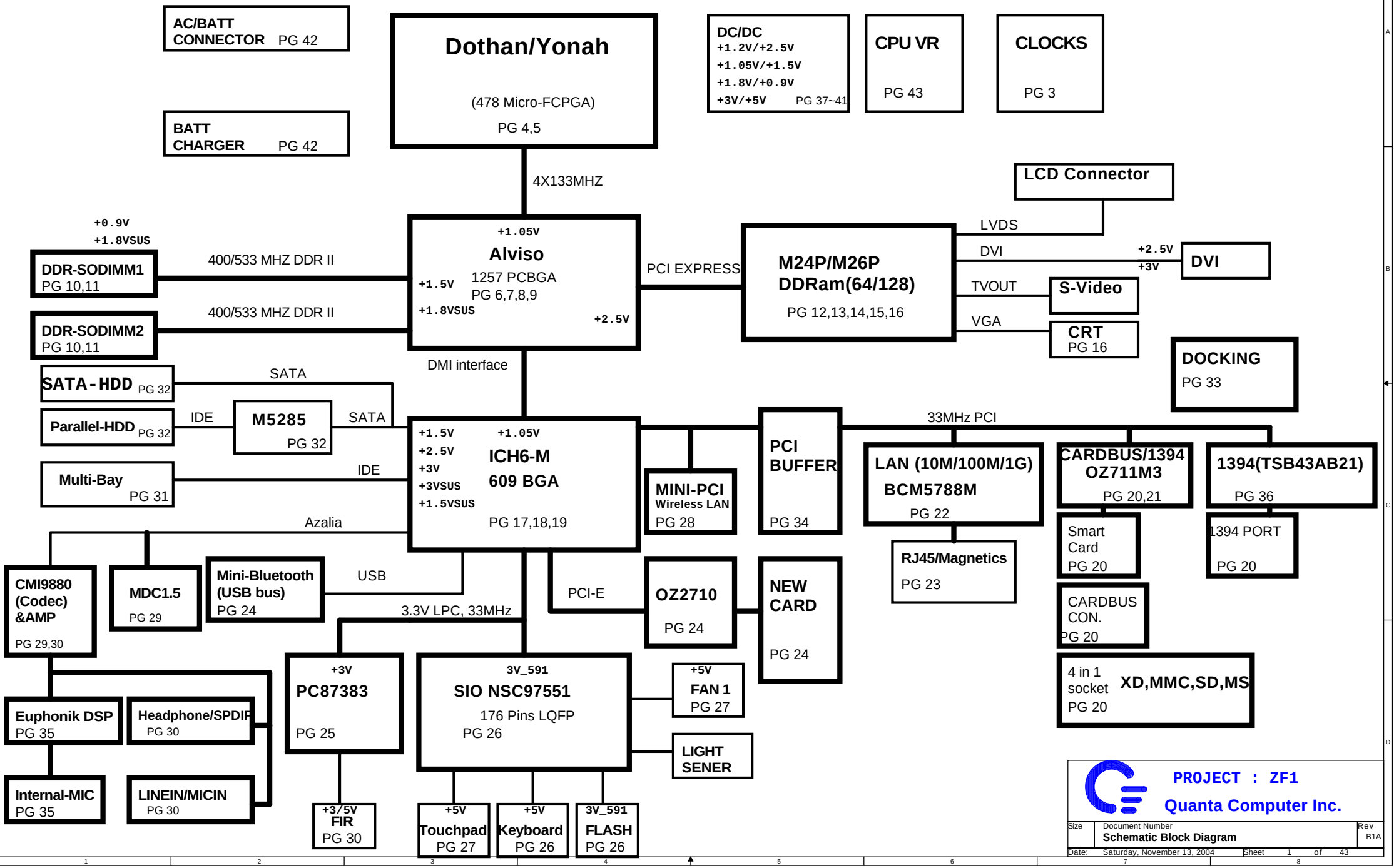
ZF1



PROJECT : ZF1

Quanta Computer Inc.

Size	Document Number	Rev
	Schematic Block Diagram	B1A
Date: Saturday, November 13, 2004	Sheet 1 of 43	

Check again

Voltage Rails		ON S0~S1	ON S3	ON S4	ON S5	Control signal
12VOUT		X	X	X	X	
3V_591		X	X	X	X	
5VPCU		X	X	X	X	
+3V_S5		X	X	X	X	S5_ON
3V_LAN		X	X	X	X	
+1.5V_S5		X	X	X	X	S5_ON
+1.8VSUS		X	X			SUSON
+3VSUS		X	X			SUSD
+5VSUS		X	X			SUSD
SMDDR_VTERM	DDR Termination voltage	X	X			MAINON
SMDDR_VREF		X				MAINON
VGA_PCIE_1.2V		X				MAINON
VCC_CORE	Core voltage for Processor	X				VR_ON
+VCCP	1.05V rail for Processor I/O	X				MAINON
+1.5V		X				MAINON
+1.8V		X				MAIND
+2.5V		X				MAIND
+3V		X				MAIND
+5V						MAIND
+12V		X				MAINON
+3VRUN		X				PCI_Switch_Power_ON
+5VRUN		X				PCI_Switch_Power_ON

Change History

5/28
1.System DVI DET function move in EZ port , So,Del Q47,R557
2.Addition AND gate for DOCKING Power Good AND DockingIN Singal combine Circuit
3.Addition Power led circuit for system
4.Change D34 AND D35 + -
5.Addition LID Switch and LID connector
6.Addition RC Delay for PCIE1.2V
7.Change EC Three GPIO port same to ZL2
5/31
1.Change C145 PCB Footprint to 3528
2.Combine USB and bluetooth connector to 19pin connector 87212-1900
3.Change PCBFootprint 88216-1200 to 88213-1200
4.Change USB connector bypass C to 0805 10u
5.Adujst 80pin connector 3 singal
6/1
1.Update power all circuit for GND name
2.Addition OR to PRST
3.Change IDE RST

6/2
1.Change ICH-6 USB Port
2.Del CDR,CDL,CDGND Singal and DEL prevent CDR,CDL,CDGND noise circuit.
6/4
1.U49,U50, Form 3VRUN change to +3V AND CHANGE MINPCI connector to PCI BUS,And addition PCI_SWRST # AND PCI_SWRST1#
2.Change BT_POWER NAME
3.Change VOIP AGND

6/7
1.Change VOIP AGND TO AGND2 for Layout

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus+Smart Card	AD25	1	PIRQC/B
Mini-PCI	AD19	2	PIRQB/D
LAN	AD22	0	PIRQA
1394	AD23	3	PIRQD

EC SM Bus1 address

Device
Smart Battery
THERMAL SENSOR
LIGHT SENER
VOIP FLASH ROM

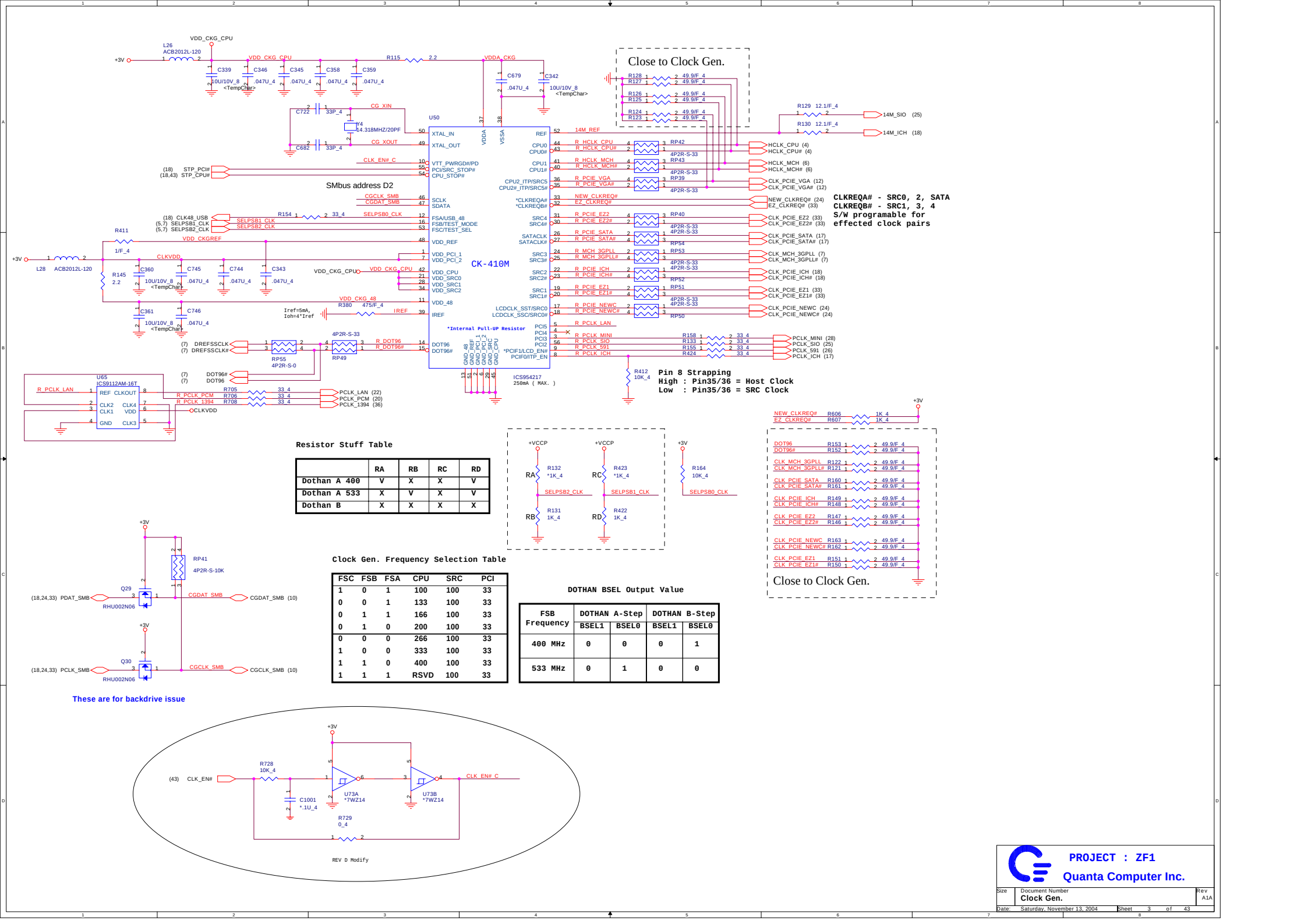
ICH6-M SM Bus address

Device	
SODIMM	**1010 000X b**
Clock Gen	**1101 001x b**

PROJECT : ZF1
Quanta Computer Inc.

Size	Document Number	Rev
		A1A

Date: Saturday, November 13, 2004 Sheet 2 of 43



Resistor Stuff Table

	RA	RB	RC	RD
Dothan A 400	V	X	X	V
Dothan A 533	X	V	X	V
Dothan B	X	X	X	X

Clock Gen. Frequency Selection Table

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

DOTHAN BSEL Output Value

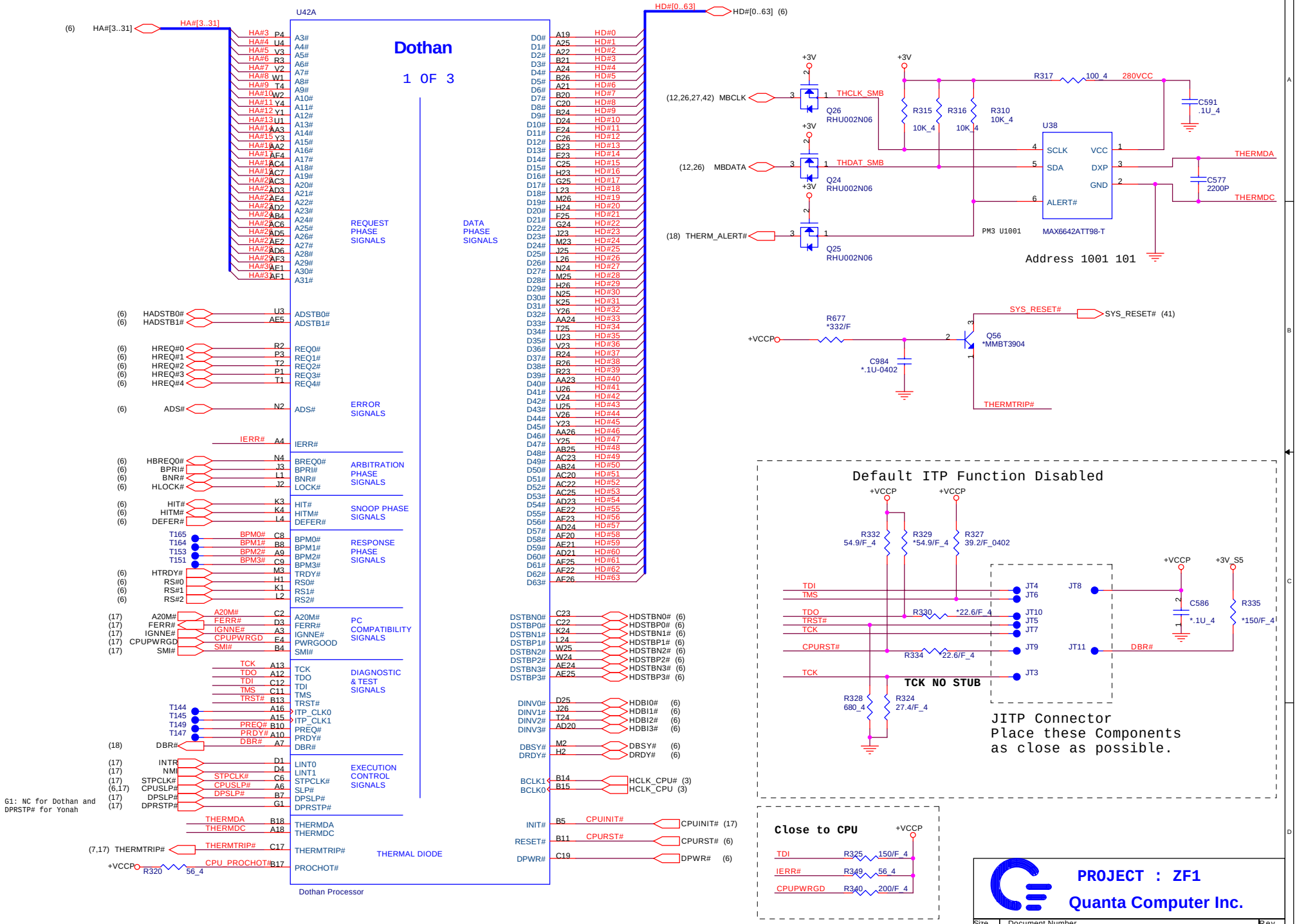
FSB Frequency	DOTHAN A-Step		DOTHAN B-Step	
	BSEL1	BSEL0	BSEL1	BSEL0
400 MHz	0	0	0	1
533 MHz	0	1	0	0

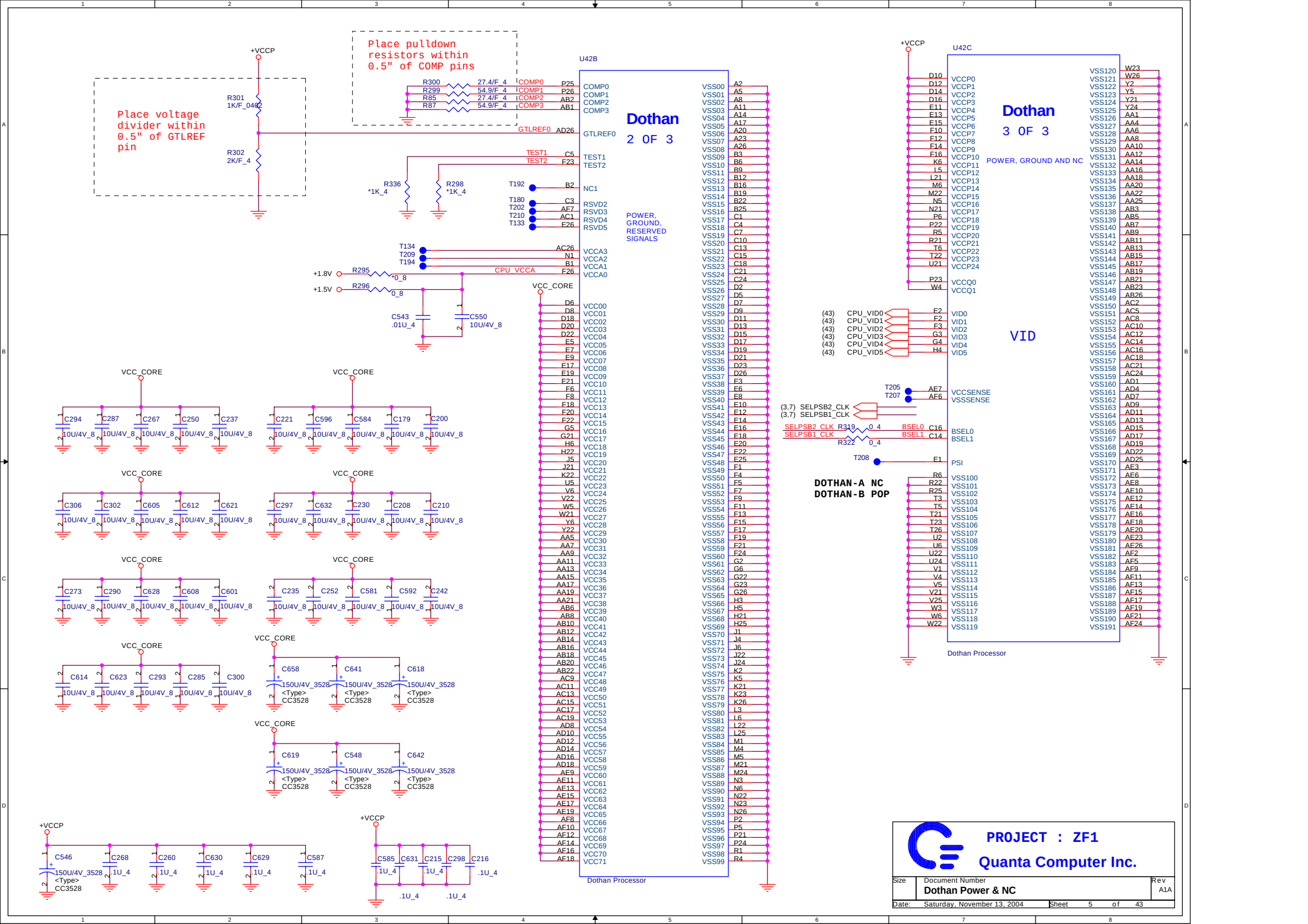
PROJECT : ZF1

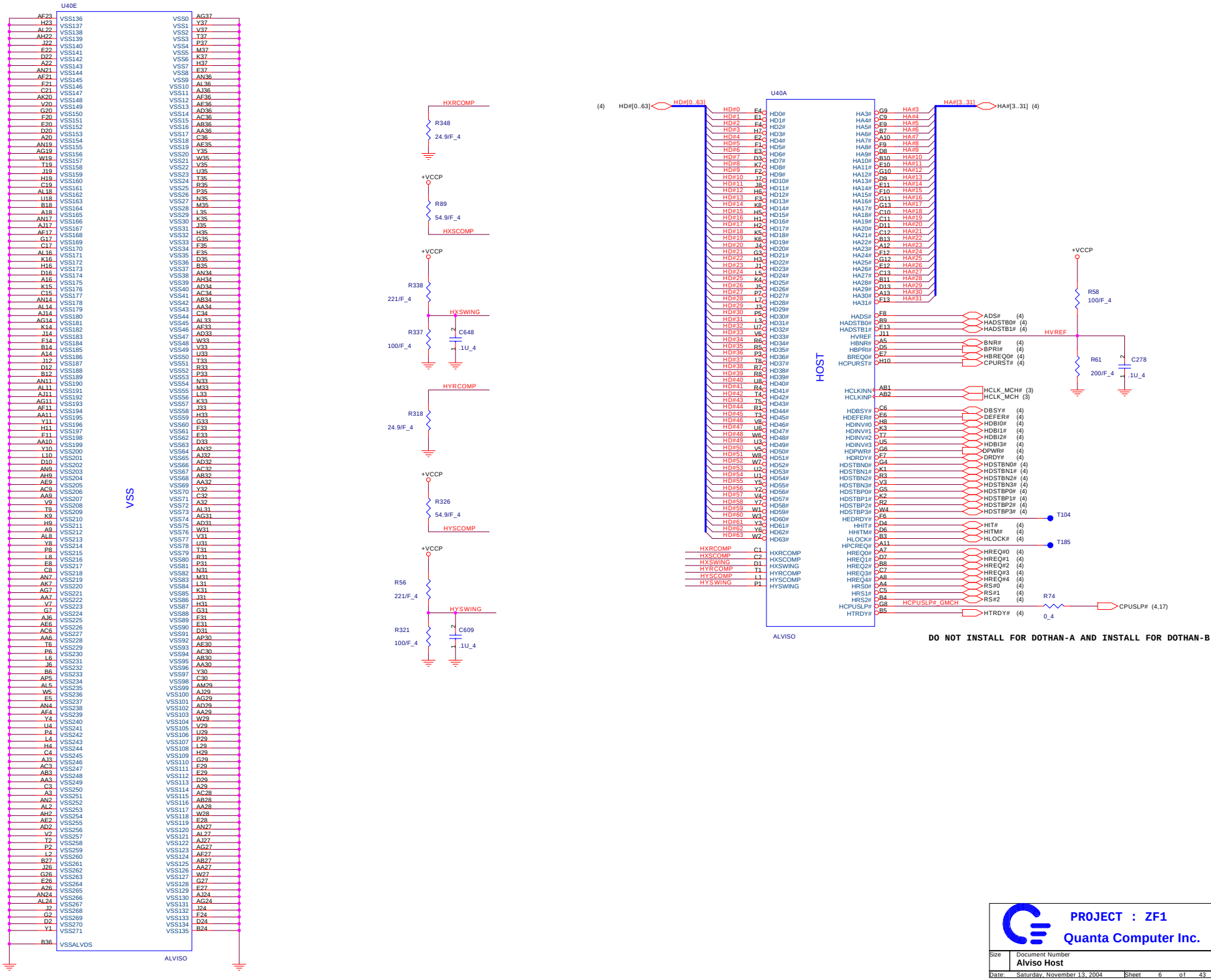
Quanta Computer Inc.

Size	Document Number	Rev
	Clock Gen.	A1A

Date: Saturday, November 13, 2004 Sheet 3 of 43


U42A
Dothan
1 0F 3
HA#[3..31]
HD#[0..63]
REQUEST PHASE SIGNALS
DATA PHASE SIGNALS
ERROR SIGNALS
ARBITRATION PHASE SIGNALS
SNOOP PHASE SIGNALS
RESPONSE PHASE SIGNALS
PC COMPATIBILITY SIGNALS
DIAGNOSTIC & TEST SIGNALS
EXECUTION CONTROL SIGNALS
THERMAL DIODE
Dothan Processor
G1: NC for Dothan and DPRSTP# for Yonah
MBCLK
MBDATA
THERM_ALERT#
THCLK_SMB
THDAT_SMB
Q26 RHU002N06
Q24 RHU002N06
Q25 RHU002N06
U38
MAX6642ATT98-T
Address 1001 101
THERMDA
THERMDC
C591 .1U_4
C577 2200P
SYS_RESET#
Q56 *MMBT3904
R677 *332/F
C984 *.1U-0402
THERMTRIP#
Default ITP Function Disabled
TCK NO STUB
JITP Connector
Place these Components
as close as possible.
Close to CPU
PROJECT : ZF1
Quanta Computer Inc.
Dothan Host
Saturday, November 13, 2004


Place pulldown resistors within 0.5" of COMP pins
Place voltage divider within 0.5" of GTLREF pin
+VCCP
R301 1K/F_0402
R302 2K/F_4
R300 27.4/F_4
R299 54.9/F_4
R85 27.4/F_4
R87 54.9/F_4
COMP0
COMP1
COMP2
COMP3
GTLREF0
TEST1
TEST2
R336 *1K_4
R298 *1K_4
T192
T180
T202
T210
T133
NC1
RSVD2
RSVD3
RSVD4
RSVD5
POWER, GROUND, RESERVED SIGNALS
T134
T209
T194
CPU_VCCA
+1.8V
+1.5V
R295 *0_8
R296 0_8
C543 .01U_4
C550 10U/4V_8
VCC_CORE
U42B
Dothan
2 OF 3
Dothan Processor
U42C
Dothan
3 OF 3
POWER, GROUND AND NC
VID
(43) CPU_VID0
(43) CPU_VID1
(43) CPU_VID2
(43) CPU_VID3
(43) CPU_VID4
(43) CPU_VID5
VCCSENSE
VSSSENSE
(3,7) SELPSB2_CLK
(3,7) SELPSB1_CLK
R319 0_4
R322 0_4
BSEL0
BSEL1
T208
PSI
DOTHAN-A NC
DOTHAN-B POP
C294 C287 C267 C250 C237
C221 C596 C584 C179 C200
C306 C302 C605 C612 C621
C297 C632 C230 C208 C210
C273 C290 C628 C608 C601
C235 C252 C581 C592 C242
C614 C623 C293 C285 C300
C658 C641 C618
C619 C548 C642
C546 C268 C260 C630 C629 C587
C585 C631 C215 C298 C216
10U/4V_8
150U/4V_3528
<Type>
CC3528
.1U_4
PROJECT : ZF1
Quanta Computer Inc.
Dothan Power & NC
Rev A1A
Saturday, November 13, 2004
Sheet 5 of 43


U40E
VSS
VSSALVDS
ALVISO
U40A
HOST
ALVISO
HD#[0..63]
HA#[3..31]
HXRCOMP
HXSCOMP
HXSWING
HYRCOMP
HYSCOMP
HYSWING
R348
24.9/F_4
R89
54.9/F_4
R338
221/F_4
R337
100/F_4
C648
.1U_4
R318
24.9/F_4
R326
54.9/F_4
R56
221/F_4
R321
100/F_4
C609
.1U_4
+VCCP
R58
100/F_4
R61
200/F_4
C278
.1U_4
HVREF
R74
0_4
T104
T185
HCPUSLP#_GMCH
CPUSLP# (4,17)
DO NOT INSTALL FOR DOTHAN-A AND INSTALL FOR DOTHAN-B
PROJECT : ZF1
Quanta Computer Inc.
Size
Document Number
Alviso Host
Rev
A1A
Date: Saturday, November 13, 2004
Sheet 6 of 43

CFG[0:2]=100 FOR FSB 533
CFG[0:2]=101 FOR FSB 400

U40C

DMI
DDR MUXING
CFG/RSVD
PM
LCK
NC

U40F

MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS

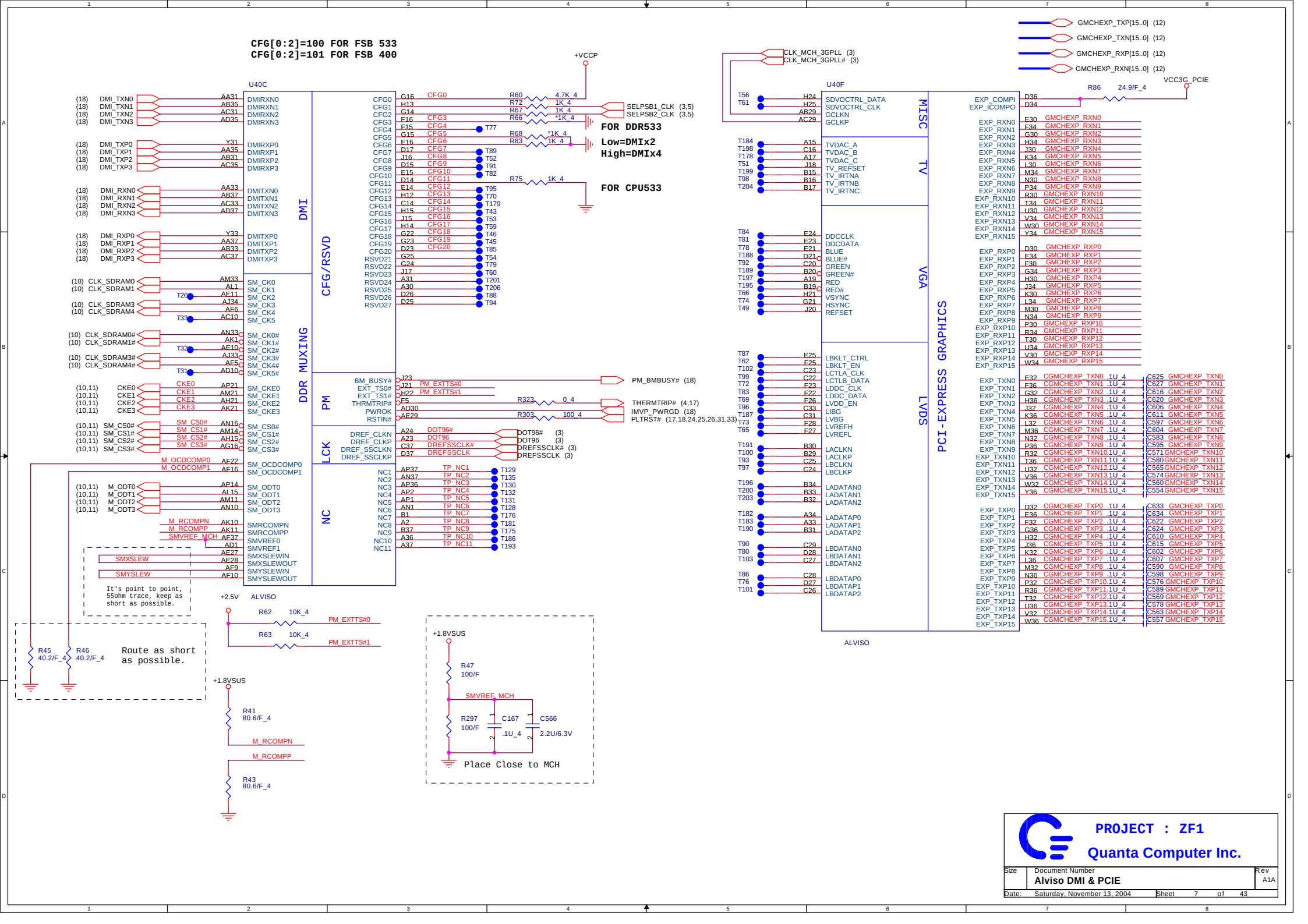
FOR DDR533
Low=DMIx2
High=DMIx4

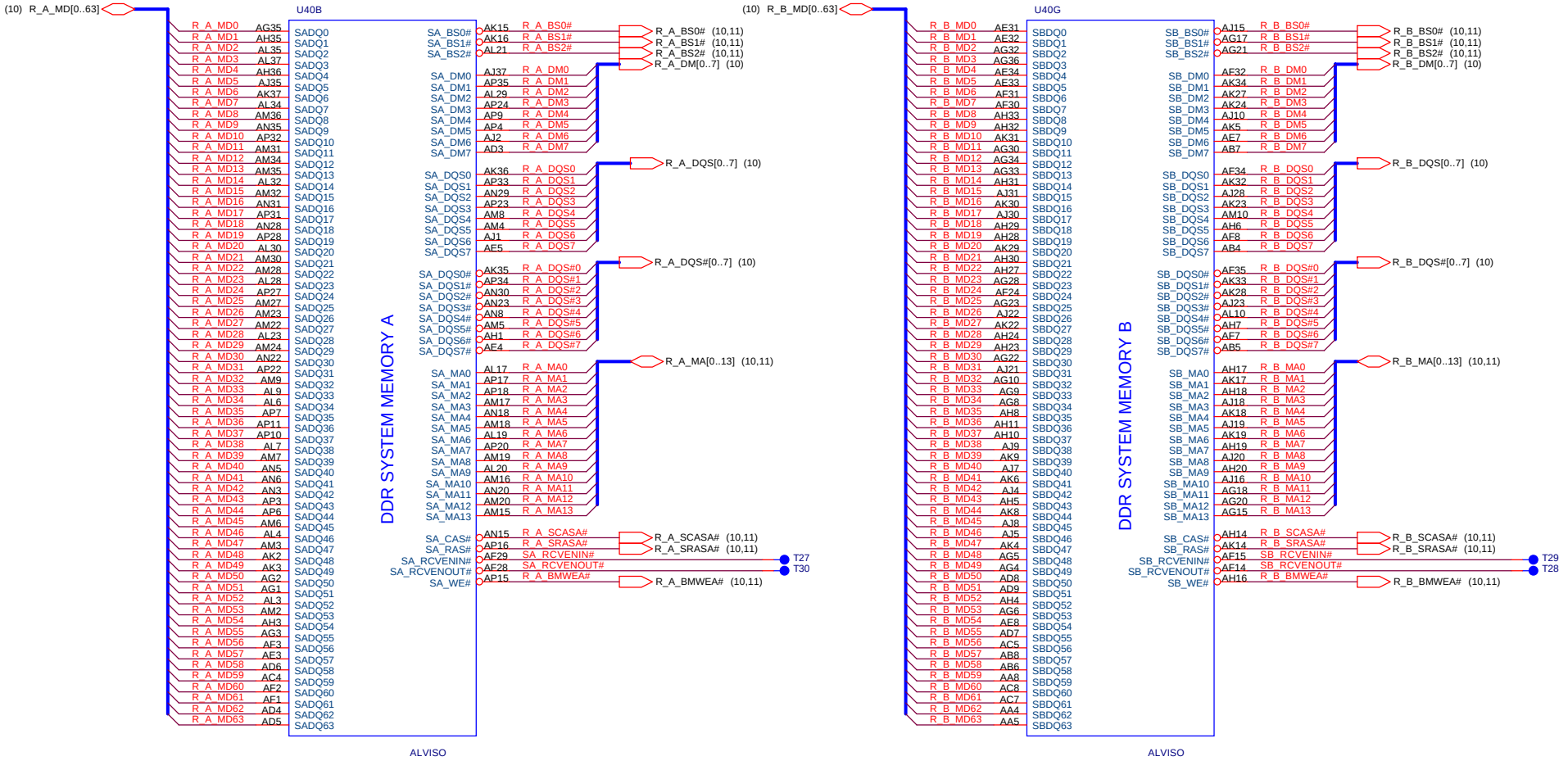
FOR CPU533

Route as short as possible.

It's point to point, 55ohm trace, keep as short as possible.

Place Close to MCH

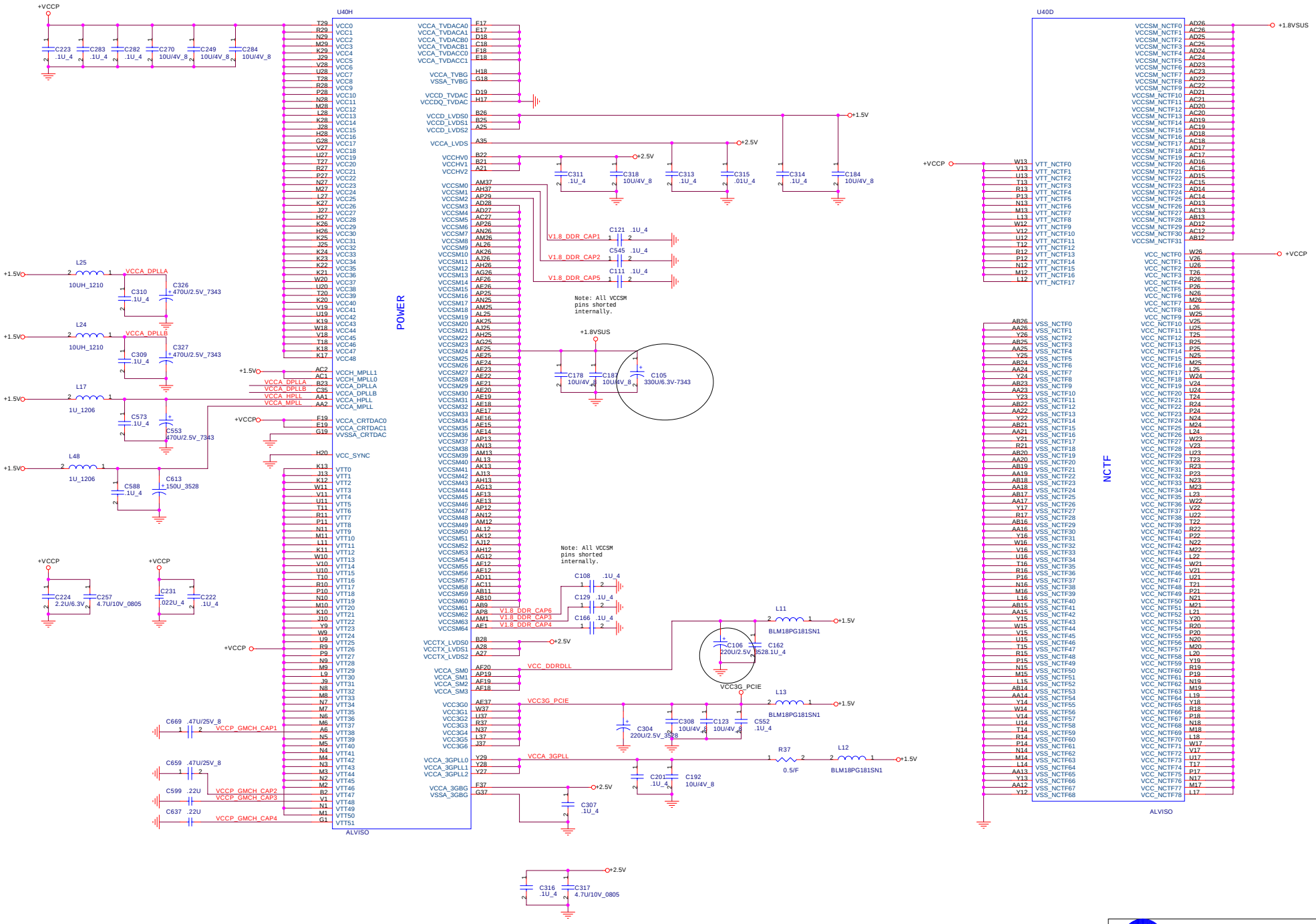


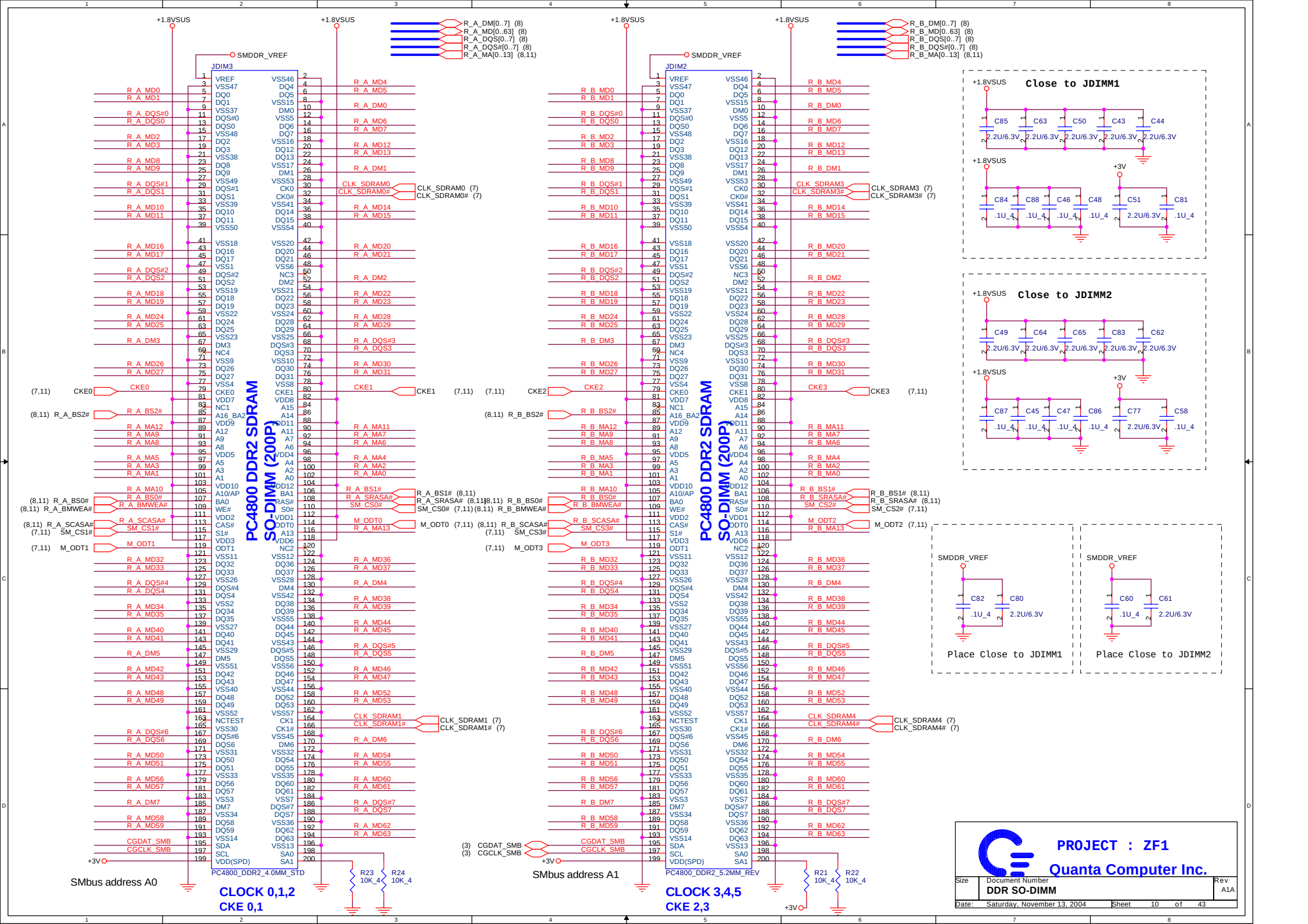


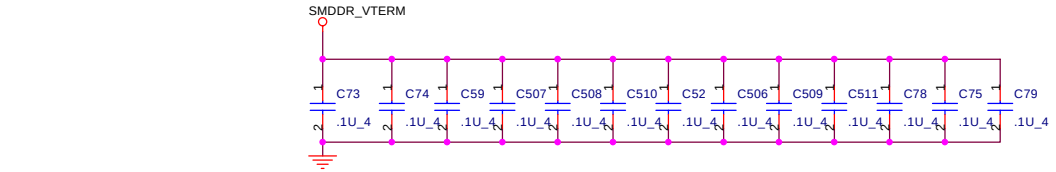
PROJECT : ZF1

Quanta Computer Inc.

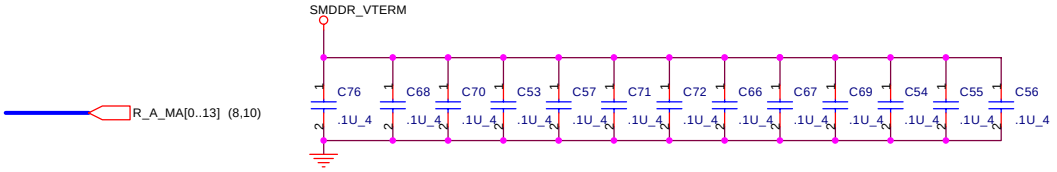
Size	Document Number	Rev
	Alviso DDR	A1A
Date: Saturday, November 13, 2004	Sheet 8 of 43	


U40H
POWER
ALVISO
U40D
NCTF
ALVISO
+VCCP
+1.5V
+2.5V
+1.8VSUS
Note: All VCCSM pins shorted internally.
Note: All VCCSM pins shorted internally.
VCC_DDRDLL
VCC3G_PCIE
VCCA_3GPLL
V1.8_DDR_CAP1
V1.8_DDR_CAP2
V1.8_DDR_CAP5
V1.8_DDR_CAP6
V1.8_DDR_CAP3
V1.8_DDR_CAP4
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_CRTDAC0
VCCA_CRTDAC1
VVSSA_CRTDAC
VCC_SYNC
VCCH_MPLL1
VCCH_MPLL0
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCP_GMCH_CAP1
VCCP_GMCH_CAP2
VCCP_GMCH_CAP3
VCCP_GMCH_CAP4
L25
10UH_1210
L24
10UH_1210
L17
1U_1206
L48
1U_1206
L11
BLM18PG181SN1
L13
BLM18PG181SN1
L12
BLM18PG181SN1
R37
0.5/F
C223 .1U_4
C283 .1U_4
C282 .1U_4
C270 10U/4V_8
C249 10U/4V_8
C284 10U/4V_8
C310 .1U_4
C326 470U/2.5V_7343
C309 .1U_4
C327 470U/2.5V_7343
C573 .1U_4
C553 470U/2.5V_7343
C588 .1U_4
C613 150U_3528
C224 2.2U/6.3V
C257 4.7U/10V_0805
C231 .022U_4
C222 .1U_4
C669 .47U/25V_8
C659 .47U/25V_8
C599 .22U
C637 .22U
C311 .1U_4
C318 10U/4V_8
C313 .1U_4
C315 .01U_4
C314 .1U_4
C184 10U/4V_8
C121 .1U_4
C545 .1U_4
C111 .1U_4
C178 10U/4V_8
C187 10U/4V_8
C105 330U/6.3V-7343
C108 .1U_4
C129 .1U_4
C166 .1U_4
C106 220U/2.5V_3528
C162 .1U_4
C304 220U/2.5V_3528
C308 10U/4V_8
C123 10U/4V_8
C552 .1U_4
C201 .1U_4
C192 10U/4V_8
C307 .1U_4
C316 .1U_4
C317 4.7U/10V_0805
C121 .1U_4
C545 .1U_4
C111 .1U_4
PROJECT : ZF1
Quanta Computer Inc.
Size
Document Number
Alviso Power
Rev
A1A
Date: Saturday, November 13, 2004
Sheet 9 of 43


JDIM3
PC4800 DDR2 SDRAM SO-DIMM (200P)
PC4800_DDR2_4.0MM_STD
SMBus address A0
CLOCK 0,1,2
CKE 0,1
JDIM2
PC4800_DDR2_5.2MM_REV
SMBus address A1
CLOCK 3,4,5
CKE 2,3
SMDDR_VREF
+1.8VSUS
+3V
R_A_DM[0..7] (8)
R_A_MD[0..63] (8)
R_A_DQS[0..7] (8)
R_A_DQS#[0..7] (8)
R_A_MA[0..13] (8,11)
R_B_DM[0..7] (8)
R_B_MD[0..63] (8)
R_B_DQS[0..7] (8)
R_B_DQS#[0..7] (8)
R_B_MA[0..13] (8,11)
Close to JDIMM1
Close to JDIMM2
Place Close to JDIMM1
Place Close to JDIMM2
PROJECT : ZF1
Quanta Computer Inc.
DDR SO-DIMM
Size
Document Number
Rev
A1A
Date: Saturday, November 13, 2004
Sheet 10 of 43



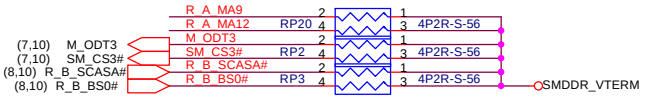
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

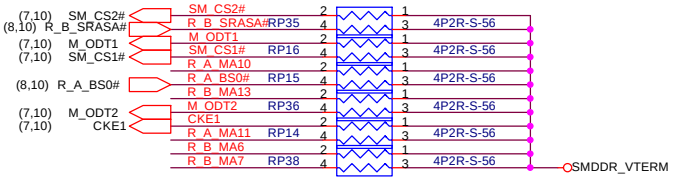


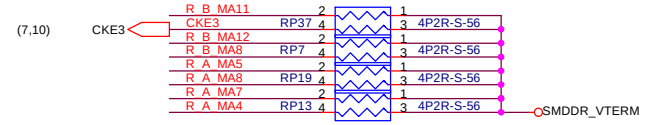
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

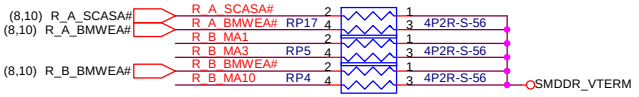
R_A_MA[0..13] (8,10)

R_B_MA[0..13] (8,10)





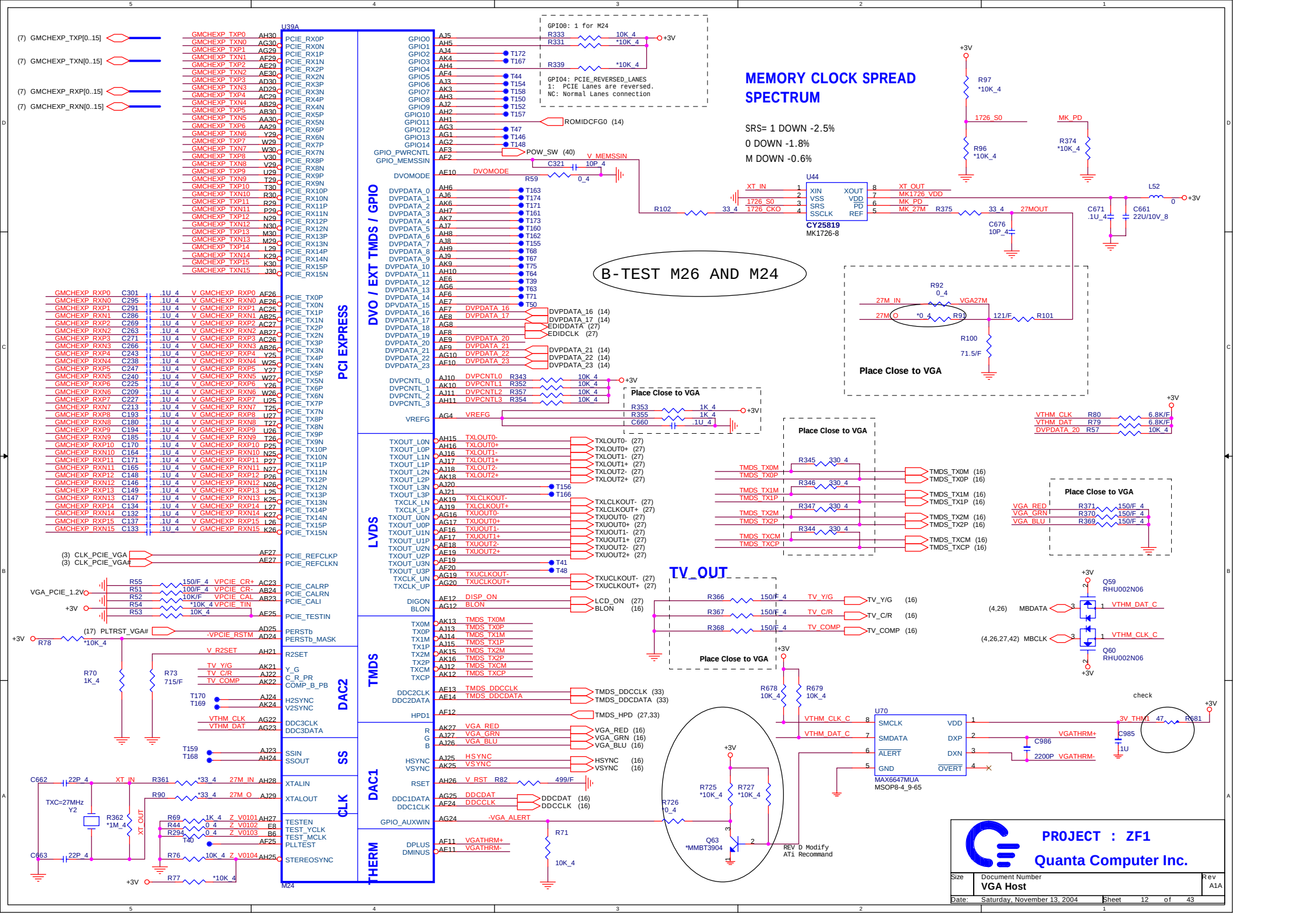


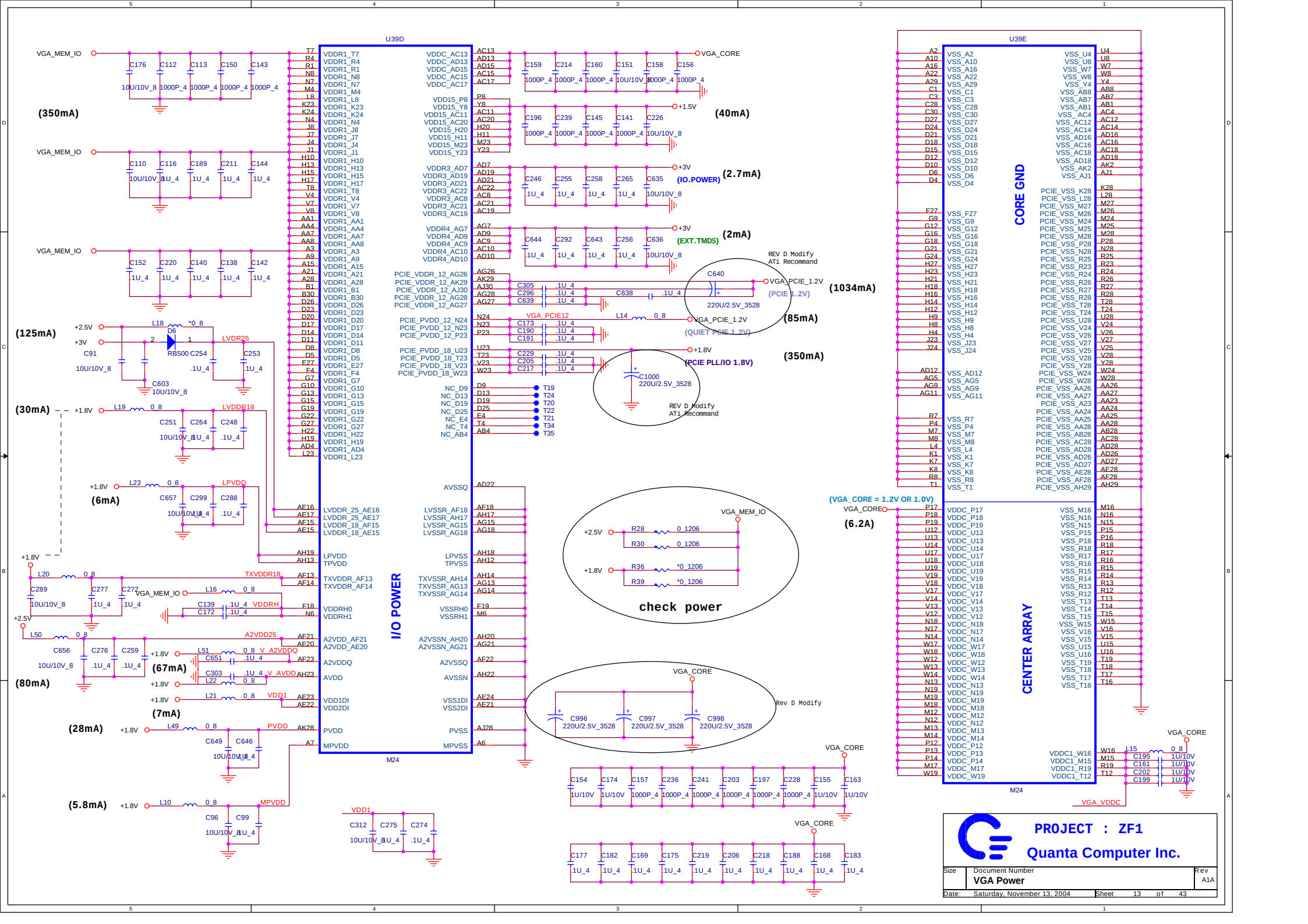


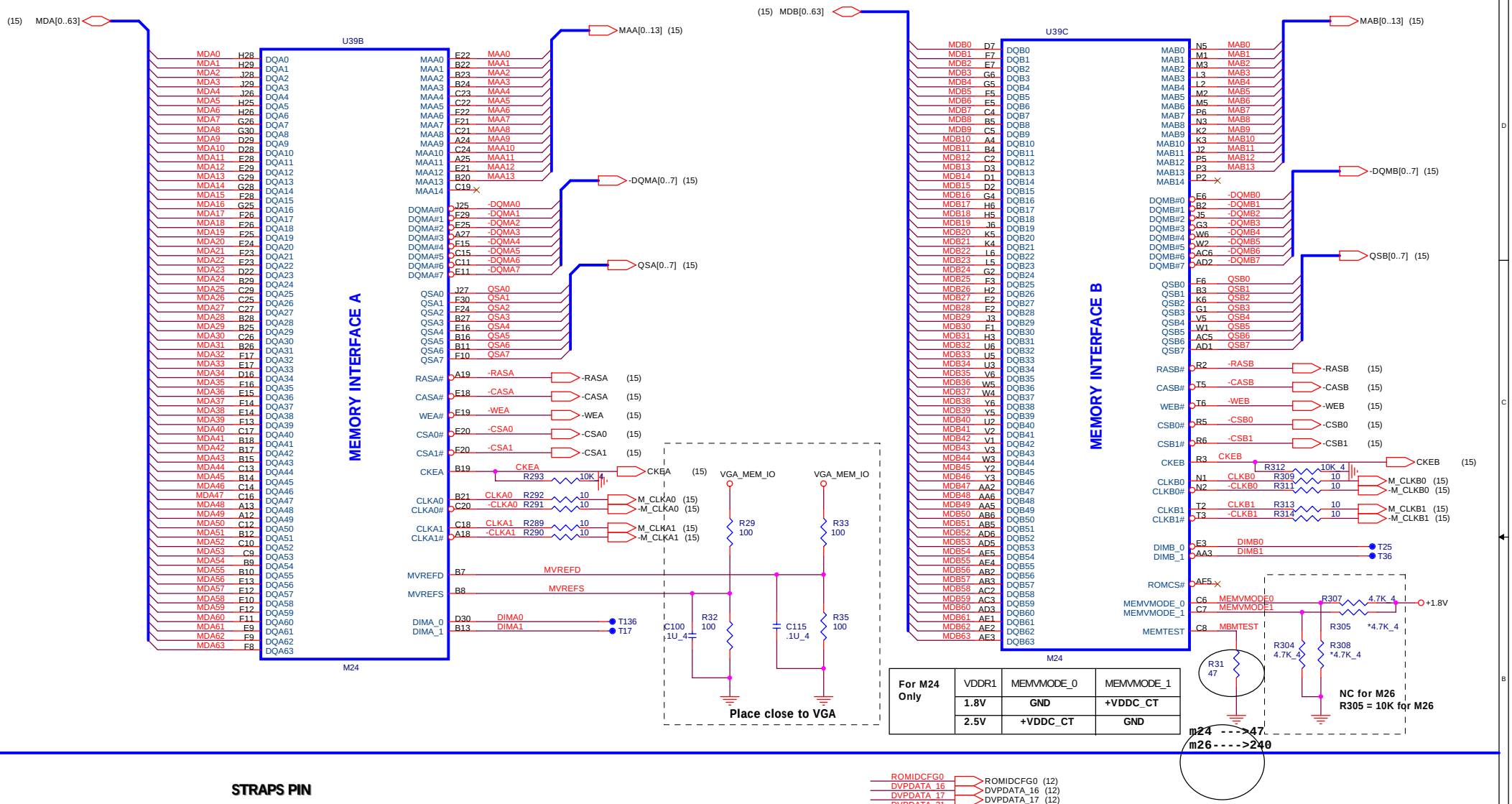
PROJECT : ZF1

Quanta Computer Inc.

Size	Document Number	Rev
	DDR Res. ARRAY	A1A
Date: Saturday, November 13, 2004	Sheet 11 of 43	


MEMORY CLOCK SPREAD SPECTRUM
SRS= 1 DOWN -2.5%
0 DOWN -1.8%
M DOWN -0.6%
B-TEST M26 AND M24
TV_OUT
U39A
PCI EXPRESS
DVO / EXT TMDS / GPIO
LVDS
TMDS
DAC2
SS
CLK
DAC1
THERM
U44
CY25819
MK1726-8
U70
MAX6647MUA
MSOP8-4_9-65
Place Close to VGA
GPIO0: 1 for M24
GPIO4: PCIE_REVERSED_LANES
1: PCIE Lanes are reversed.
NC: Normal Lanes connection
REV D Modify
ATi Recommand
PROJECT : ZF1
Quanta Computer Inc.
VGA Host
Saturday, November 13, 2004

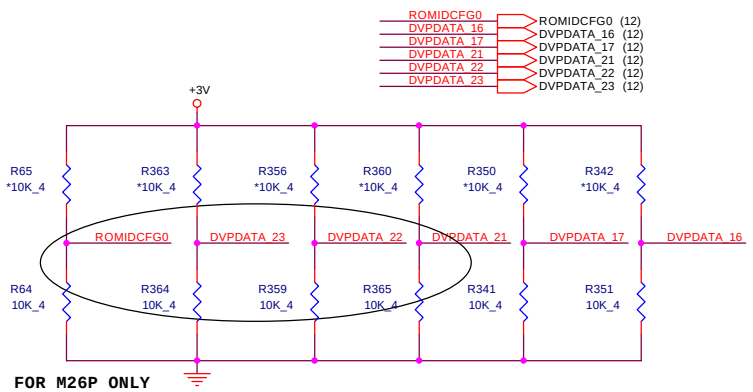

U39D
U39E
I/O POWER
CORE GND
CENTER ARRAY
M24
VGA_MEM_IO
VGA_CORE
VGA_PCIE_1.2V
(PCIE 1.2V)
VGA_PCIE_1.2V
(QUIET PCIE 1.2V)
+1.8V
(PCIE PLL/IO 1.8V)
+1.5V
+3V
(IO.POWER)
+3V
(EXT.TMDS)
VGA_PCIE12
REV D Modify
ATi Recommand
(350mA)
(40mA)
(2.7mA)
(2mA)
(1034mA)
(85mA)
(350mA)
(125mA)
(30mA)
(6mA)
(80mA)
(67mA)
(7mA)
(28mA)
(5.8mA)
(VGA_CORE = 1.2V OR 1.0V)
(6.2A)
check power
Rev D Modify
PROJECT : ZF1
Quanta Computer Inc.
VGA Power
Size
Document Number
Rev
A1A
Date: Saturday, November 13, 2004
Sheet 13 of 43



For M24 Only	VDDR1	MEMVMODE_0	MEMVMODE_1
	1.8V	GND	+VDDC_CT
	2.5V	+VDDC_CT	GND

STRAPS PIN

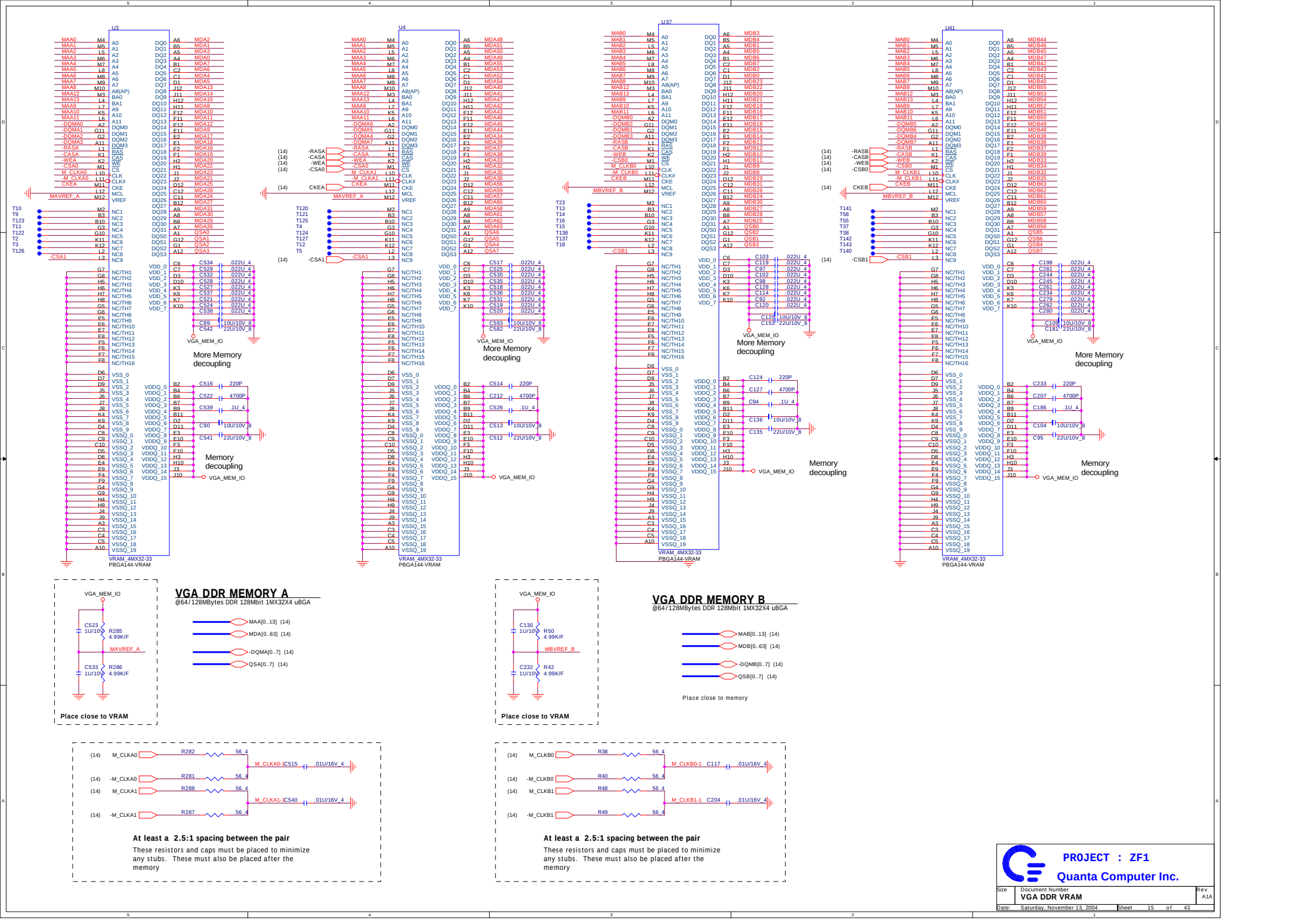
GPIO(9,13:11) INT P/D	ROMIDCFG **0x0x: No ROM, CHG_ID=0** 0x1x: No Rom, CHG_ID=1 1000: Parallel ROM, Chip ID'S from ROM 1000: Parallel ROM, Chip ID'S from ROM
DVPDATA_21~23 MEM TYPE	DVPDATA_21: 0=4Mx32 1=8Mx32 DVPDATA_22: 0=128M 1=64M DVPDATA_23: 0=Hynix 1=Samsung

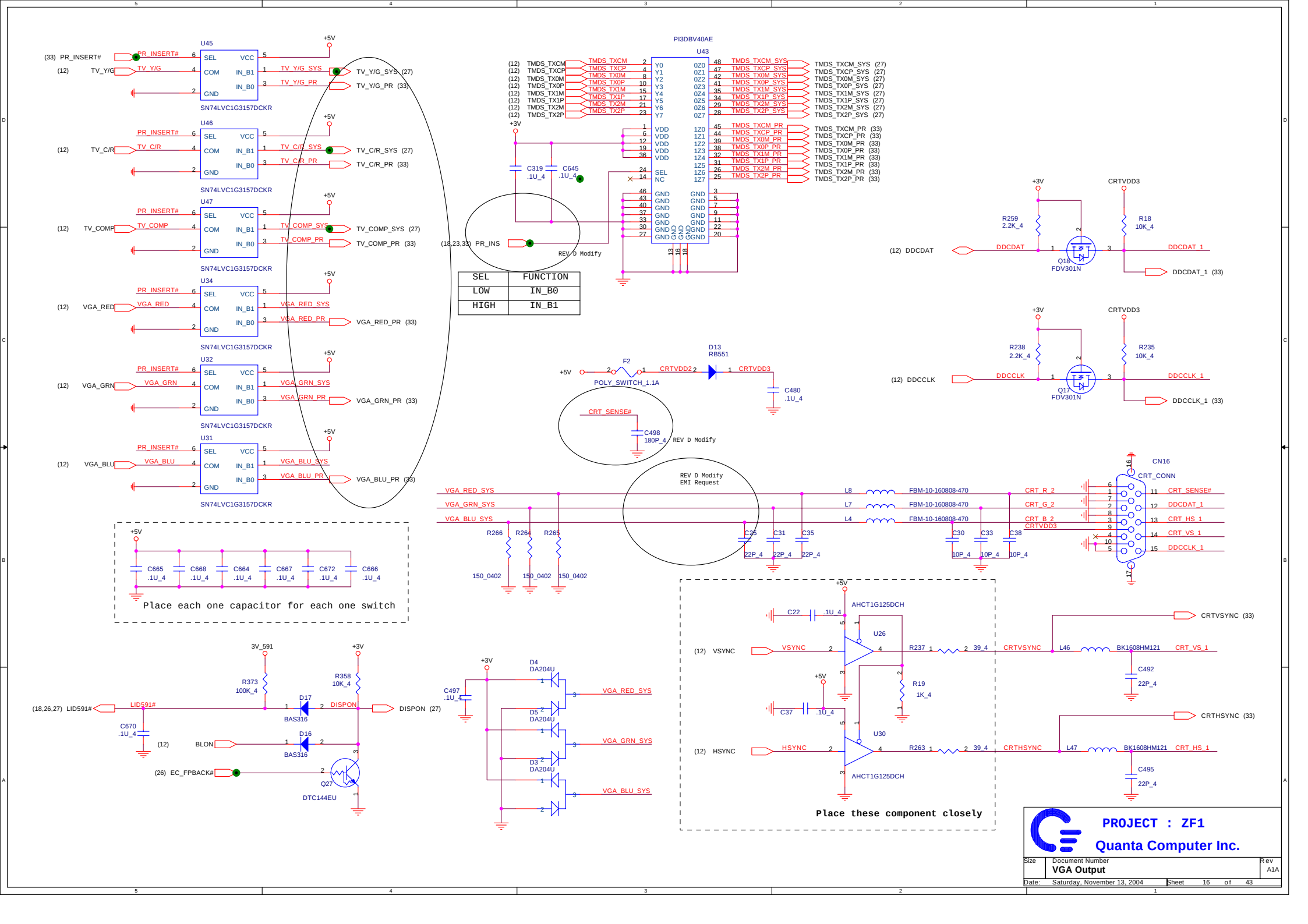


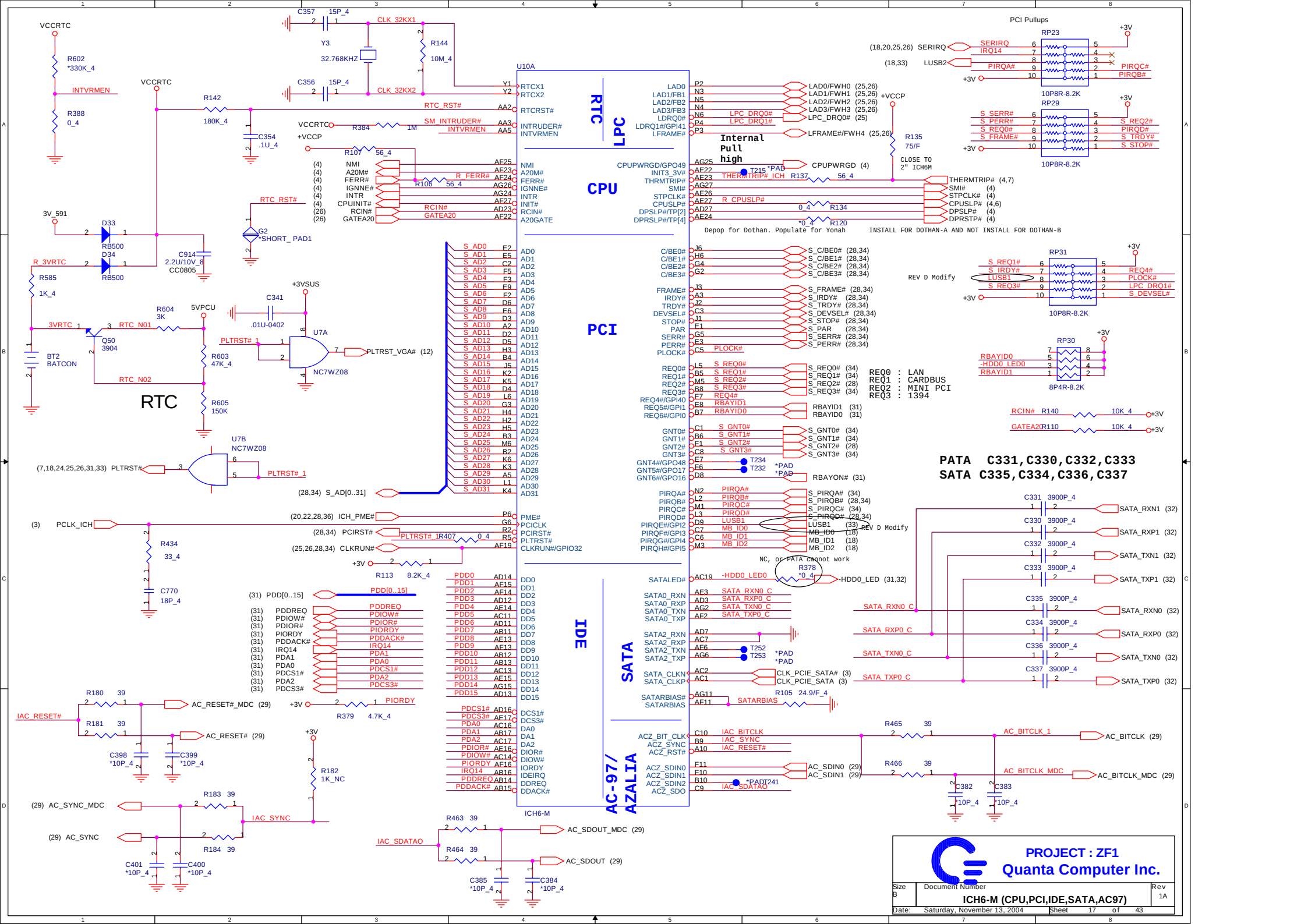
FOR M26P ONLY
0: 128M
1: 256M

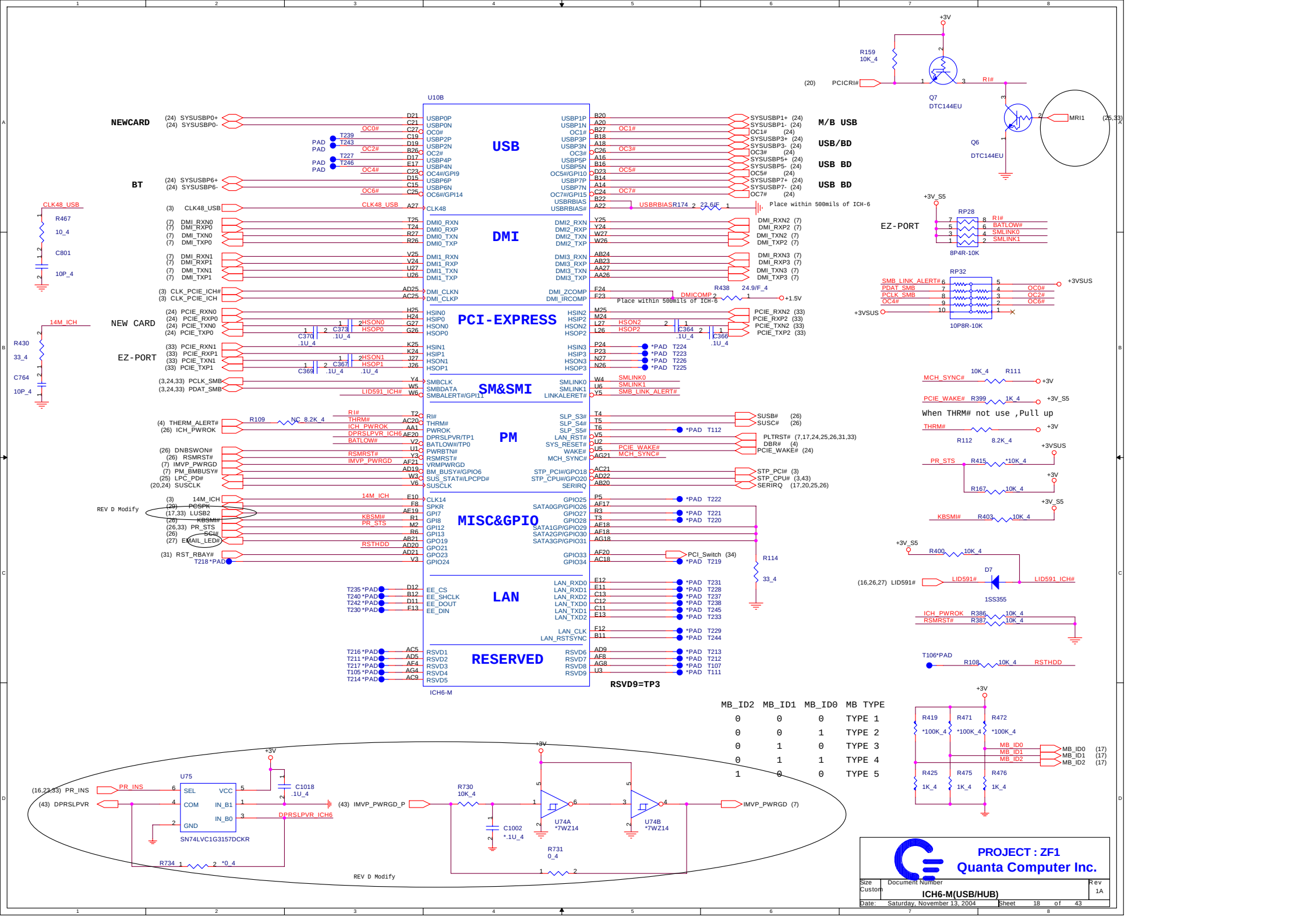
PROJECT : ZF1
Quanta Computer Inc.

Size	Document Number	Rev
	VGA MEM & Strapping	A1A
Date: Saturday, November 13, 2004	Sheet 14 of 43	

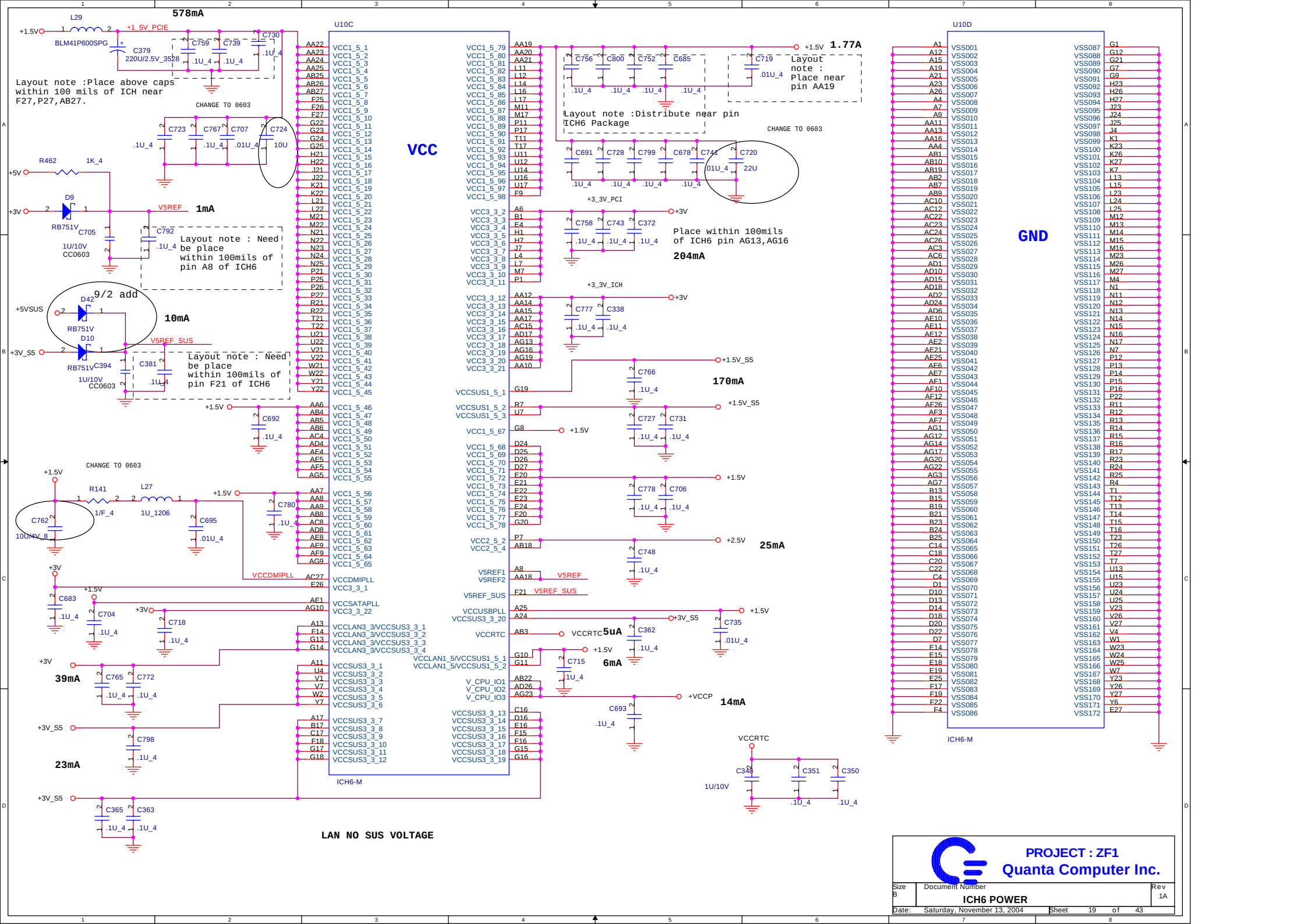

U3
U4
U37
U41
VRAM_4MX32-33
PBGA144-VRAM
VGA_MEM_IO
More Memory decoupling
Memory decoupling
VGA DDR MEMORY A
@64/128MBytes DDR 128Mbit 1MX32X4 uBGA
MAA[0..13] (14)
MDA[0..63] (14)
-DQMA[0..7] (14)
QSA[0..7] (14)
VGA DDR MEMORY B
@64/128MBytes DDR 128Mbit 1MX32X4 uBGA
MAB[0..13] (14)
MDB[0..63] (14)
-DQMB[0..7] (14)
QSB[0..7] (14)
Place close to memory
Place close to VRAM
C523 1U/10V R285 4.99K/F
C533 1U/10V R286 4.99K/F
MAVREF_A
C130 1U/10V R50 4.99K/F
C232 1U/10V R42 4.99K/F
MBVREF_B
M_CLKA0 R282 56_4 M_CLKA0-1 C515 .01U/16V_4
-M_CLKA0 R281 56_4
M_CLKA1 R288 56_4 M_CLKA1-1 C540 .01U/16V_4
-M_CLKA1 R287 56_4
At least a 2.5:1 spacing between the pair
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory
M_CLKB0 R38 56_4 M_CLKB0-1 C117 .01U/16V_4
-M_CLKB0 R40 56_4
M_CLKB1 R48 56_4 M_CLKB1-1 C204 .01U/16V_4
-M_CLKB1 R49 56_4
At least a 2.5:1 spacing between the pair
These resistors and caps must be placed to minimize any stubs. These must also be placed after the memory
PROJECT : ZF1
Quanta Computer Inc.
Size
Document Number
VGA DDR VRAM
Rev A1A
Date: Saturday, November 13, 2004
Sheet 15 of 43


U45
SN74LVC1G3157DCKR
(33) PR_INSERT#
(12) TV_Y/G
TV_Y/G_SYS (27)
TV_Y/G_PR (33)
U46
(12) TV_C/R
TV_C/R_SYS (27)
TV_C/R_PR (33)
U47
(12) TV_COMP
TV_COMP_SYS (27)
TV_COMP_PR (33)
U34
(12) VGA_RED
VGA_RED_PR (33)
U32
(12) VGA_GRN
VGA_GRN_PR (33)
U31
(12) VGA_BLU
VGA_BLU_PR (33)
+5V
SEL
VCC
COM
IN_B1
IN_B0
GND
Place each one capacitor for each one switch
C665 .1U_4
C668 .1U_4
C664 .1U_4
C667 .1U_4
C672 .1U_4
C666 .1U_4
PI3DBV40AE
U43
(12) TMDS_TXCM
(12) TMDS_TXCP
(12) TMDS_TX0M
(12) TMDS_TX0P
(12) TMDS_TX1M
(12) TMDS_TX1P
(12) TMDS_TX2M
(12) TMDS_TX2P
TMDS_TXCM_SYS (27)
TMDS_TXCP_SYS (27)
TMDS_TX0M_SYS (27)
TMDS_TX0P_SYS (27)
TMDS_TX1M_SYS (27)
TMDS_TX1P_SYS (27)
TMDS_TX2M_SYS (27)
TMDS_TX2P_SYS (27)
TMDS_TXCM_PR (33)
TMDS_TXCP_PR (33)
TMDS_TX0M_PR (33)
TMDS_TX0P_PR (33)
TMDS_TX1M_PR (33)
TMDS_TX1P_PR (33)
TMDS_TX2M_PR (33)
TMDS_TX2P_PR (33)
+3V
C319 .1U_4
C645 .1U_4
(18,23,33) PR_INS
REV D Modify
SEL
NC
VDD
GND
SEL | FUNCTION
LOW | IN_B0
HIGH | IN_B1
+5V
F2
POLY_SWITCH_1.1A
CRTVDD2
D13
RB551
CRTVDD3
C480 .1U_4
CRT_SENSE#
C498 180P_4
REV D Modify
REV D Modify
EMI Request
VGA_RED_SYS
VGA_GRN_SYS
VGA_BLU_SYS
R266 150_0402
R264 150_0402
R265 150_0402
L8 FBM-10-160808-470
L7 FBM-10-160808-470
L4 FBM-10-160808-470
C25 22P_4
C31 22P_4
C35 22P_4
C30 10P_4
C33 10P_4
C38 10P_4
CRT_R_2
CRT_G_2
CRT_B_2
CRTVDD3
CN16
CRT_CONN
CRT_SENSE#
DDCDAT_1
CRT_HS_1
CRT_VS_1
DDCCLK_1
(12) DDCDAT
R259 2.2K_4
Q18 FDV301N
R18 10K_4
DDCDAT_1 (33)
(12) DDCCLK
R238 2.2K_4
Q17 FDV301N
R235 10K_4
DDCCLK_1 (33)
3V_591
+3V
R373 100K_4
R358 10K_4
(18,26,27) LID591#
D17 BAS316
DISPON
DISPON (27)
C670 .1U_4
(12) BLON
D16 BAS316
(26) EC_FPBACK#
Q27 DTC144EU
C497 .1U_4
D4 DA204U
D5 DA204U
D3 DA204U
VGA_RED_SYS
VGA_GRN_SYS
VGA_BLU_SYS
AHCT1G125DCH
U26
U30
C22 .1U_4
C37 .1U_4
(12) VSYNC
(12) HSYNC
R237 39_4
R263 39_4
R19 1K_4
CRTVSYNC
CRTHSYNC
L46 BK1608HM121
L47 BK1608HM121
CRT_VS_1
CRT_HS_1
C492 22P_4
C495 22P_4
CRTVSYNC (33)
CRTHSYNC (33)
Place these component closely
PROJECT : ZF1
Quanta Computer Inc.
Size
Document Number
VGA Output
Rev
A1A
Date: Saturday, November 13, 2004
Sheet 16 of 43


U10A
RTC
LPC
CPU
PCI
IDE
SATA
AC-97/ AZALIA
ICH6-M
RTC
PCI Pullups
Internal Pull high
REQ0 : LAN
REQ1 : CARDBUS
REQ2 : MINI PCI
REQ3 : 1394
PATA C331,C330,C332,C333
SATA C335,C334,C336,C337
PROJECT : ZF1
Quanta Computer Inc.
ICH6-M (CPU,PCI,IDE,SATA,AC97)
Saturday, November 13, 2004



MB_ID2	MB_ID1	MB_ID0	MB TYPE
0	0	0	TYPE 1
0	0	1	TYPE 2
0	1	0	TYPE 3
0	1	1	TYPE 4
1	0	0	TYPE 5

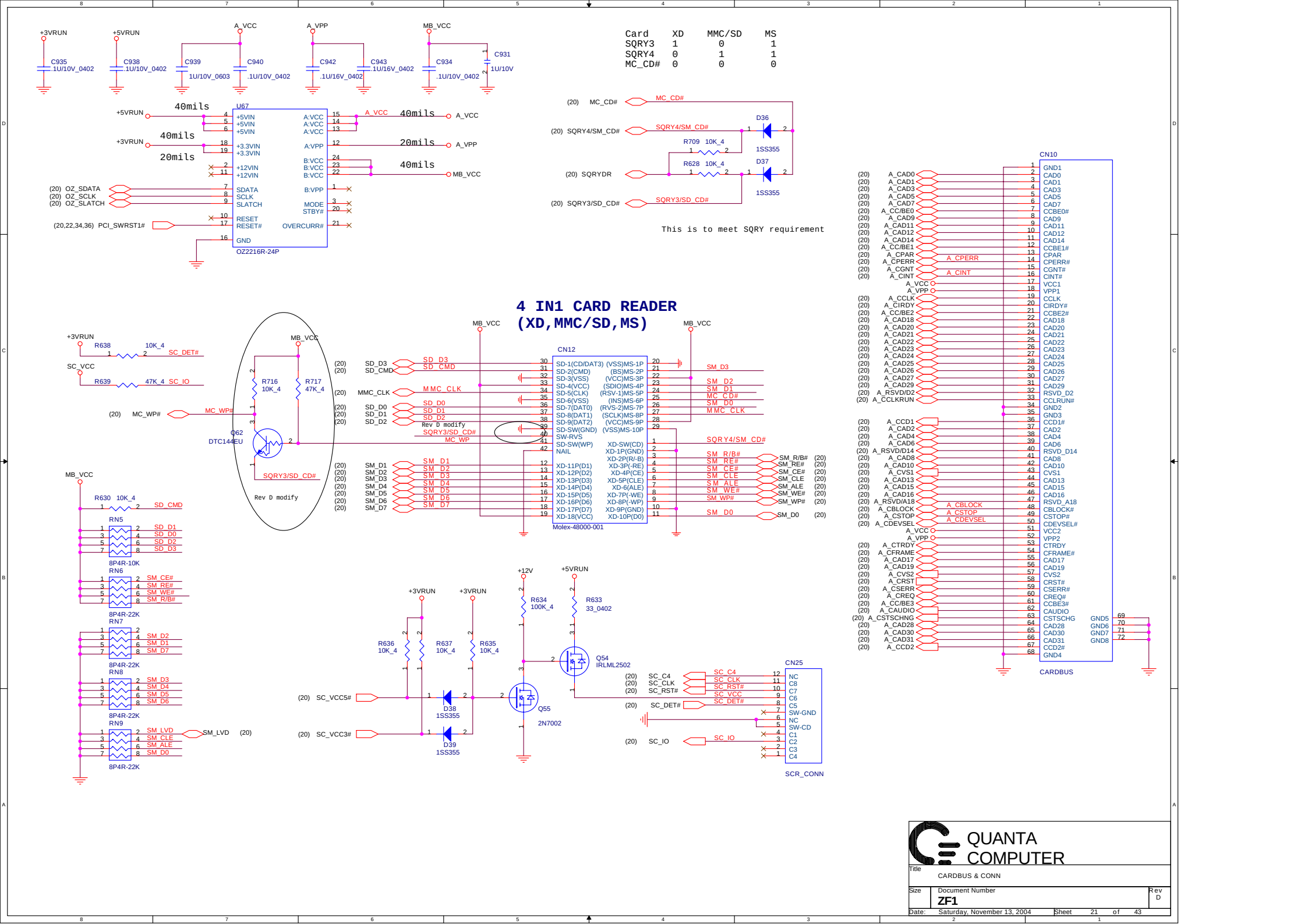

578mA
L29
+1.5V
BLM41P600SPG
+1_5V_PCIE
C379
220U/2.5V_3528
C759
C739
C730
.1U_4
Layout note :Place above caps within 100 mils of ICH near F27,P27,AB27.
CHANGE TO 0603
C723
C767
C707
C724
10U
R462
1K_4
+5V
D9
+3V
V5REF
1mA
RB751V
C705
1U/10V
CC0603
C792
Layout note : Need be place within 100mils of pin A8 of ICH6
9/2 add
D42
+5VSUS
10mA
D10
+3V_S5
V5REF_SUS
C394
C381
Layout note : Need be place within 100mils of pin F21 of ICH6
C692
CHANGE TO 0603
R141
L27
1/F_4
1U_1206
C762
10U/4V_8
C780
C695
.01U_4
VCCDMIPLL
C683
C704
C718
39mA
C765
C772
C798
23mA
C365
C363
LAN NO SUS VOLTAGE
U10C
VCC
ICH6-M
VCC1_5_1
VCC1_5_2
VCC1_5_3
VCC1_5_4
VCC1_5_5
VCC1_5_6
VCC1_5_7
VCC1_5_8
VCC1_5_9
VCC1_5_10
VCC1_5_11
VCC1_5_12
VCC1_5_13
VCC1_5_14
VCC1_5_15
VCC1_5_16
VCC1_5_17
VCC1_5_18
VCC1_5_19
VCC1_5_20
VCC1_5_21
VCC1_5_22
VCC1_5_23
VCC1_5_24
VCC1_5_25
VCC1_5_26
VCC1_5_27
VCC1_5_28
VCC1_5_29
VCC1_5_30
VCC1_5_31
VCC1_5_32
VCC1_5_33
VCC1_5_34
VCC1_5_35
VCC1_5_36
VCC1_5_37
VCC1_5_38
VCC1_5_39
VCC1_5_40
VCC1_5_41
VCC1_5_42
VCC1_5_43
VCC1_5_44
VCC1_5_45
VCC1_5_46
VCC1_5_47
VCC1_5_48
VCC1_5_49
VCC1_5_50
VCC1_5_51
VCC1_5_52
VCC1_5_53
VCC1_5_54
VCC1_5_55
VCC1_5_56
VCC1_5_57
VCC1_5_58
VCC1_5_59
VCC1_5_60
VCC1_5_61
VCC1_5_62
VCC1_5_63
VCC1_5_64
VCC1_5_65
VCCDMIPLL
VCC3_3_1
VCCSATAPLL
VCC3_3_22
VCCLAN3_3/VCCSUS3_3_1
VCCLAN3_3/VCCSUS3_3_2
VCCLAN3_3/VCCSUS3_3_3
VCCLAN3_3/VCCSUS3_3_4
VCCSUS3_3_1
VCCSUS3_3_2
VCCSUS3_3_3
VCCSUS3_3_4
VCCSUS3_3_5
VCCSUS3_3_6
VCCSUS3_3_7
VCCSUS3_3_8
VCCSUS3_3_9
VCCSUS3_3_10
VCCSUS3_3_11
VCCSUS3_3_12
VCC1_5_79
VCC1_5_80
VCC1_5_81
VCC1_5_82
VCC1_5_83
VCC1_5_84
VCC1_5_85
VCC1_5_86
VCC1_5_87
VCC1_5_88
VCC1_5_89
VCC1_5_90
VCC1_5_91
VCC1_5_92
VCC1_5_93
VCC1_5_94
VCC1_5_95
VCC1_5_96
VCC1_5_97
VCC1_5_98
VCC3_3_2
VCC3_3_3
VCC3_3_4
VCC3_3_5
VCC3_3_6
VCC3_3_7
VCC3_3_8
VCC3_3_9
VCC3_3_10
VCC3_3_11
VCC3_3_12
VCC3_3_13
VCC3_3_14
VCC3_3_15
VCC3_3_16
VCC3_3_17
VCC3_3_18
VCC3_3_19
VCC3_3_20
VCC3_3_21
VCCSUS1_5_1
VCCSUS1_5_2
VCCSUS1_5_3
VCC1_5_67
VCC1_5_68
VCC1_5_69
VCC1_5_70
VCC1_5_71
VCC1_5_72
VCC1_5_73
VCC1_5_74
VCC1_5_75
VCC1_5_76
VCC1_5_77
VCC1_5_78
VCC2_5_2
VCC2_5_4
V5REF1
V5REF2
V5REF_SUS
VCCUSBPLL
VCCSUS3_3_20
VCCRTC
VCCLAN1_5/VCCSUS1_5_1
VCCLAN1_5/VCCSUS1_5_2
V_CPU_IO1
V_CPU_IO2
V_CPU_IO3
VCCSUS3_3_13
VCCSUS3_3_14
VCCSUS3_3_15
VCCSUS3_3_16
VCCSUS3_3_17
VCCSUS3_3_18
VCCSUS3_3_19
+1.5V
1.77A
Layout note : Place near pin AA19
Layout note :Distribute near pin ICH6 Package
CHANGE TO 0603
+3_3V_PCI
+3V
Place within 100mils of ICH6 pin AG13,AG16
204mA
+3_3V_ICH
+1.5V_S5
170mA
+2.5V
25mA
V5REF
V5REF_SUS
+3V_S5
5uA
6mA
+VCCP
14mA
U10D
GND
ICH6-M
VSS001
VSS002
VSS003
VSS004
VSS005
VSS006
VSS007
VSS008
VSS009
VSS010
VSS011
VSS012
VSS013
VSS014
VSS015
VSS016
VSS017
VSS018
VSS019
VSS020
VSS021
VSS022
VSS023
VSS024
VSS025
VSS026
VSS027
VSS028
VSS029
VSS030
VSS031
VSS032
VSS033
VSS034
VSS035
VSS036
VSS037
VSS038
VSS039
VSS040
VSS041
VSS042
VSS043
VSS044
VSS045
VSS046
VSS047
VSS048
VSS049
VSS050
VSS051
VSS052
VSS053
VSS054
VSS055
VSS056
VSS057
VSS058
VSS059
VSS060
VSS061
VSS062
VSS063
VSS064
VSS065
VSS066
VSS067
VSS068
VSS069
VSS070
VSS071
VSS072
VSS073
VSS074
VSS075
VSS076
VSS077
VSS078
VSS079
VSS080
VSS081
VSS082
VSS083
VSS084
VSS085
VSS086
VSS087
VSS088
VSS089
VSS090
VSS091
VSS092
VSS093
VSS094
VSS095
VSS096
VSS097
VSS098
VSS099
VSS100
VSS101
VSS102
VSS103
VSS104
VSS105
VSS106
VSS107
VSS108
VSS109
VSS110
VSS111
VSS112
VSS113
VSS114
VSS115
VSS116
VSS117
VSS118
VSS119
VSS120
VSS121
VSS122
VSS123
VSS124
VSS125
VSS126
VSS127
VSS128
VSS129
VSS130
VSS131
VSS132
VSS133
VSS134
VSS135
VSS136
VSS137
VSS138
VSS139
VSS140
VSS141
VSS142
VSS143
VSS144
VSS145
VSS146
VSS147
VSS148
VSS149
VSS150
VSS151
VSS152
VSS153
VSS154
VSS155
VSS156
VSS157
VSS158
VSS159
VSS160
VSS161
VSS162
VSS163
VSS164
VSS165
VSS166
VSS167
VSS168
VSS169
VSS170
VSS171
VSS172
PROJECT : ZF1
Quanta Computer Inc.
Size B
Document Number
ICH6 POWER
Rev 1A
Date: Saturday, November 13, 2004
Sheet 19 of 43

O2 MICRO CORP.
CARDBUS CONTROLLER
OZ711M3 (224CSP)

STRAP FOR SERIAL POWER SW

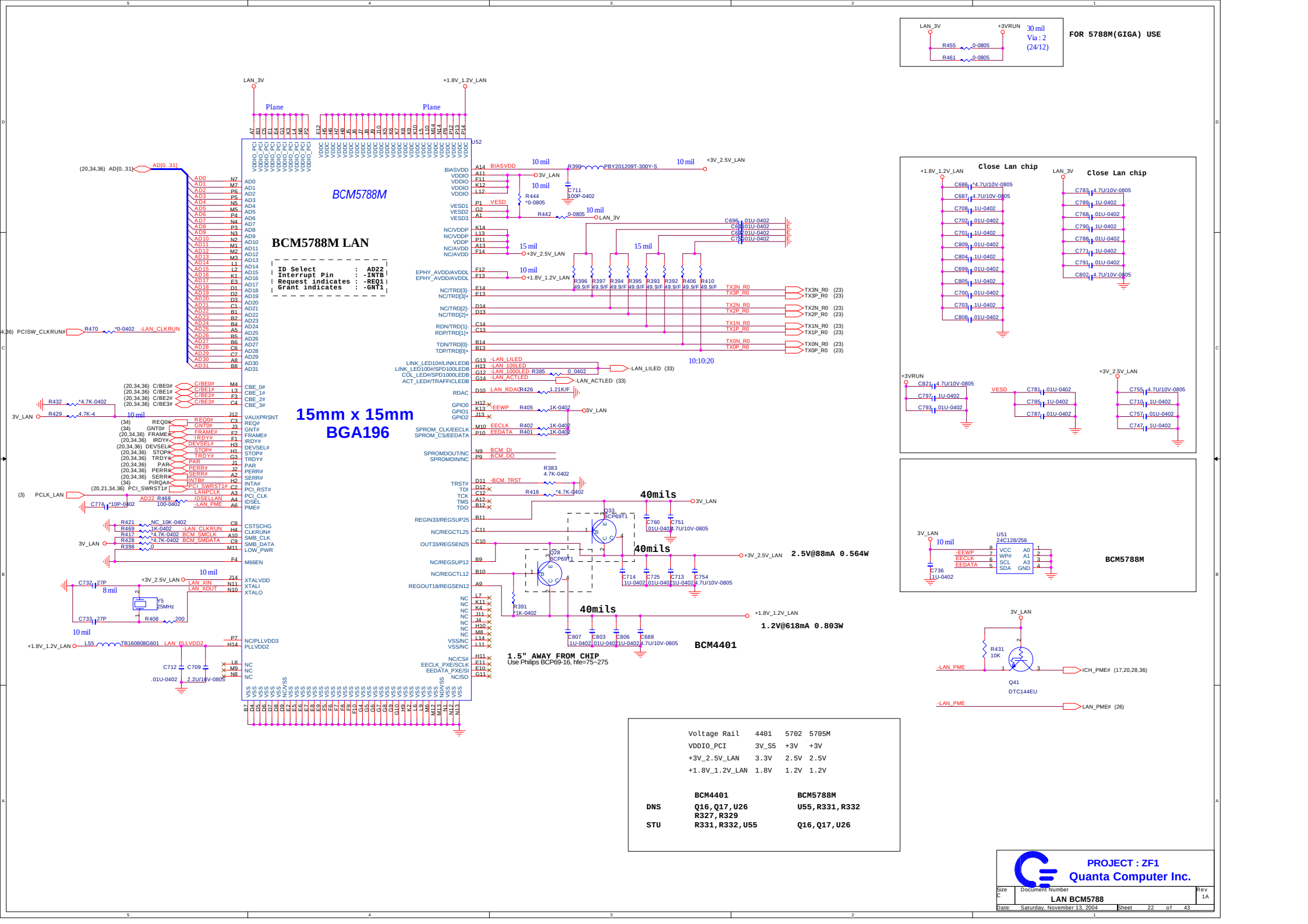
U66
OZ711M3CSP

PROJECT :	ZF1
Quanta Computer Inc.	
Size	Document Number: OZ711M3 — Rev: A1A
Date:	Saturday, November 13, 2004 — Sheet 20 of 43



Title	CARDBUS & CONN
Size	Document Number: ZF1
Rev	D
Date:	Saturday, November 13, 2004
Sheet	21 of 43

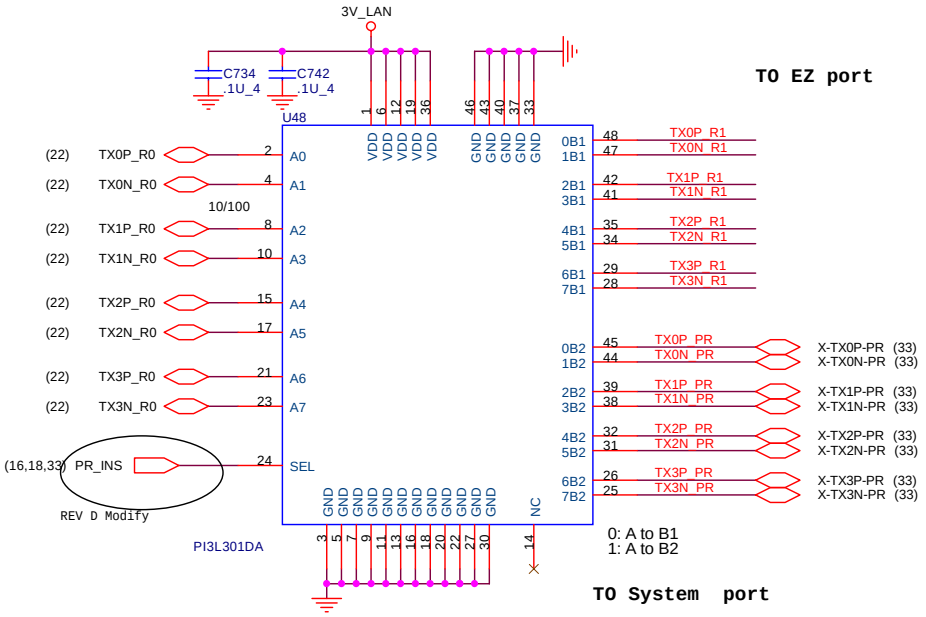
QUANTA COMPUTER



Voltage Rail	4401	5702	5705M
VDDIO_PCI	3V_S5	+3V	+3V
+3V_2.5V_LAN	3.3V	2.5V	2.5V
+1.8V_1.2V_LAN	1.8V	1.2V	1.2V

	BCM4401	BCM5788M
DNS	Q16,Q17,U26 R327,R329	U55,R331,R332
STU	R331,R332,U55	Q16,Q17,U26

Lan Switch

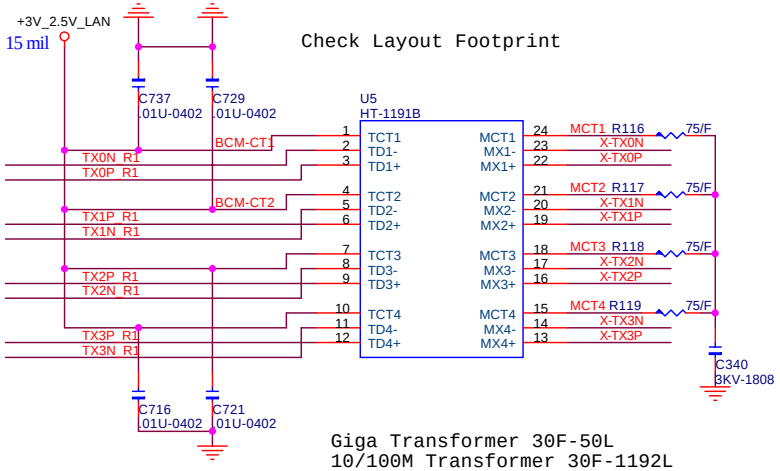


TO EZ port

TO System port

10/100/1000 M TRANSFOMER

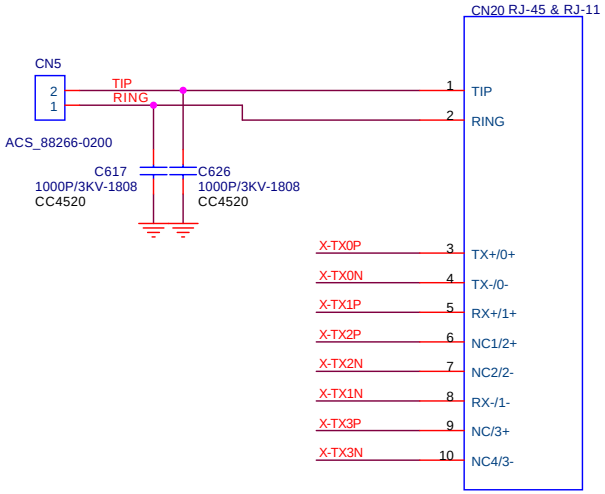
Check Layout Footprint



Giga Transformer 30F-50L
10/100M Transformer 30F-1192L

LAN and RJ11 Jack

Check Layout Footprint

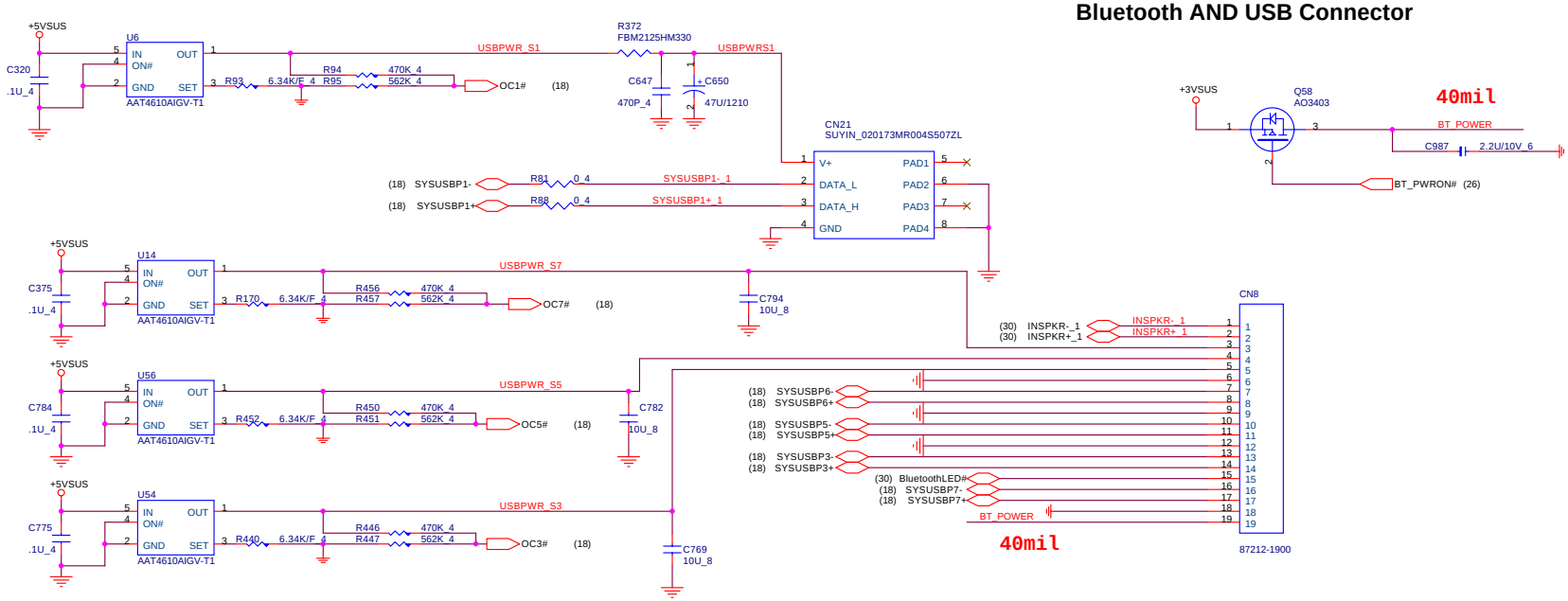


PROJECT : ZF1
Quanta Computer Inc.

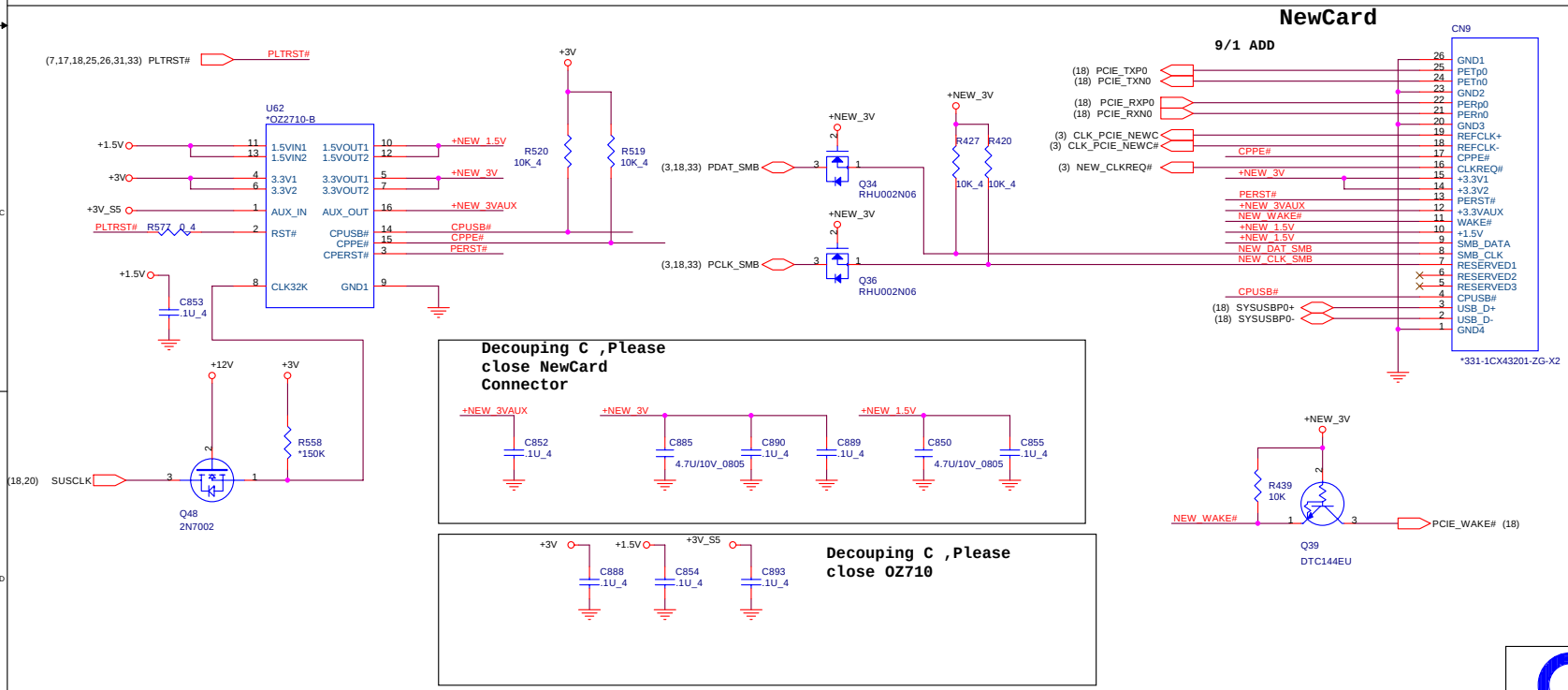
Size	Document Number	Rev
	LAN JACK	A1A
Date: Saturday, November 13, 2004	Sheet 23 of 43	

USB Connector and USB board

Bluetooth AND USB Connector



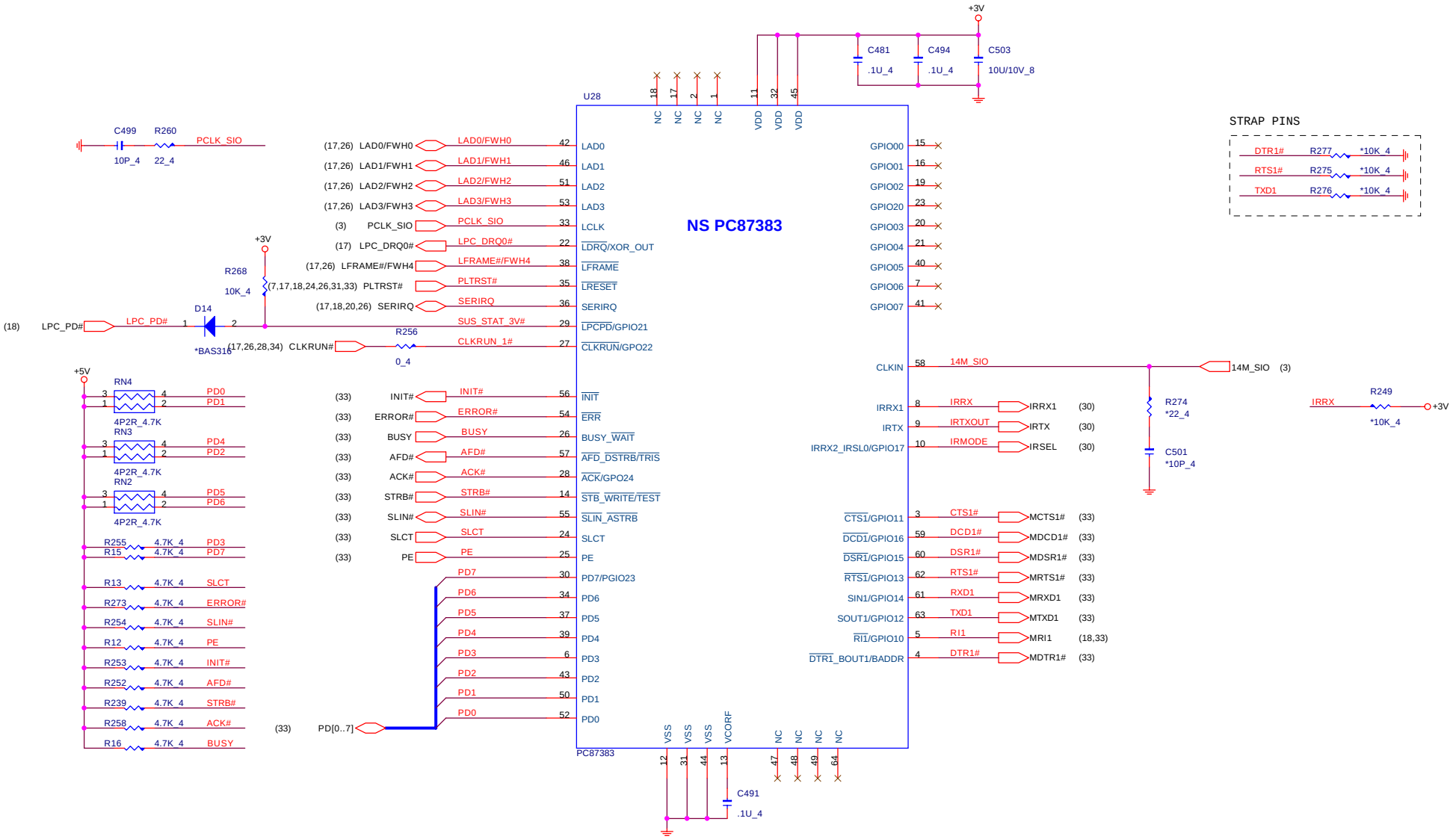
NewCard



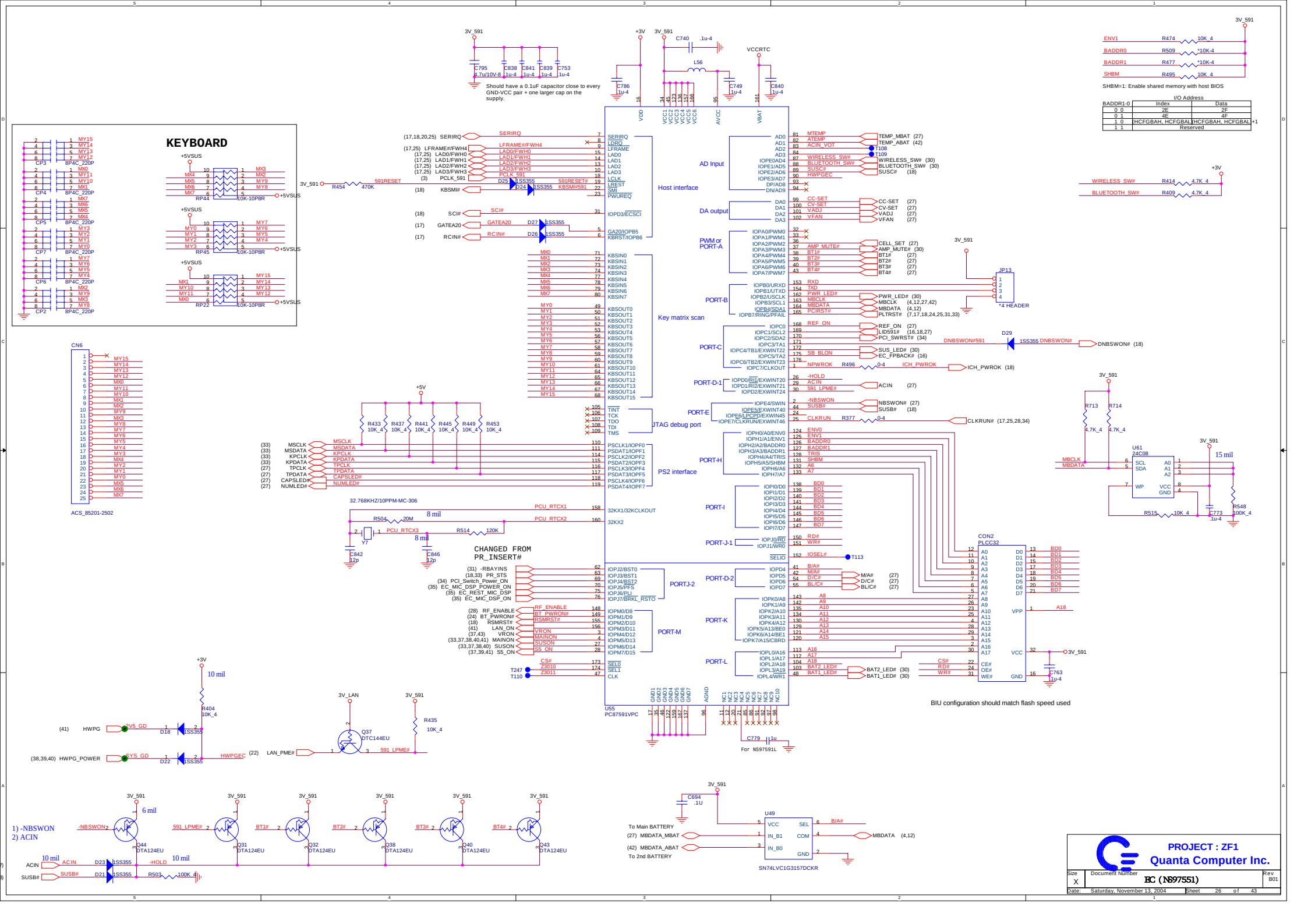
PROJECT : ZF1

Quanta Computer Inc.

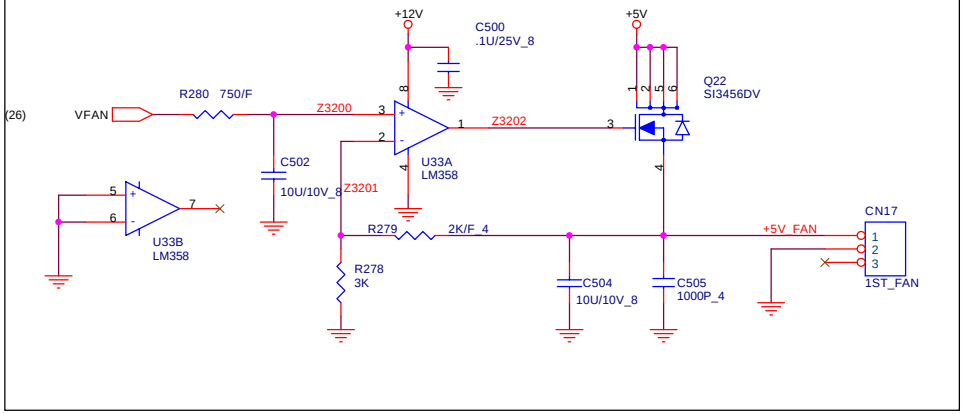
Size	Document Number	Rev
Custom	USB PORTS/NEW CARD	1A
Date: Saturday, November 13, 2004	Sheet 24 of 43	



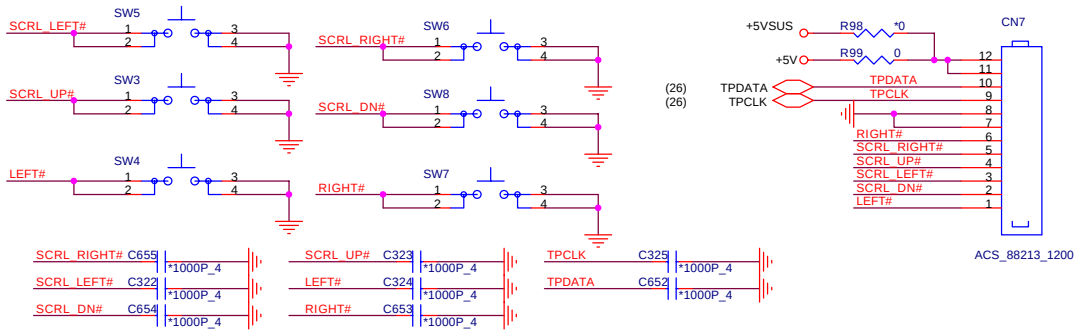
PROJECT : ZF1		
Quanta Computer Inc.		
Size A3	Document Number PC87383 SUPER I/O	Rev 1A
Date: Saturday, November 13, 2004	Sheet 25 of 43	


KEYBOARD
Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.
CHANGED FROM PR_INSERT#
BIU configuration should match flash speed used
1) -NBSWON
2) ACIN
PROJECT : ZF1
Quanta Computer Inc.
EC (NS97551)
Date: Saturday, November 13, 2004
Sheet 26 of 43

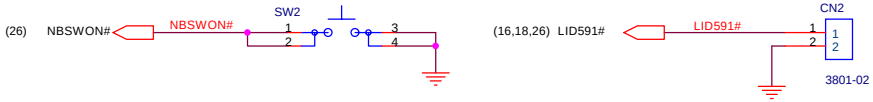
1st FAN OUT CONNECTOR



TouchPad Switch and T/P Module Connector

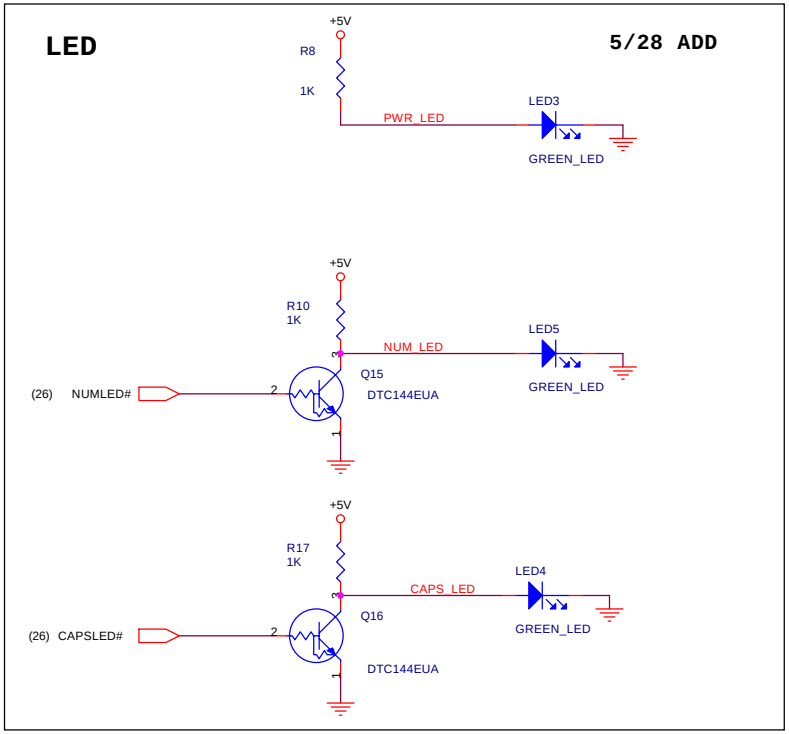


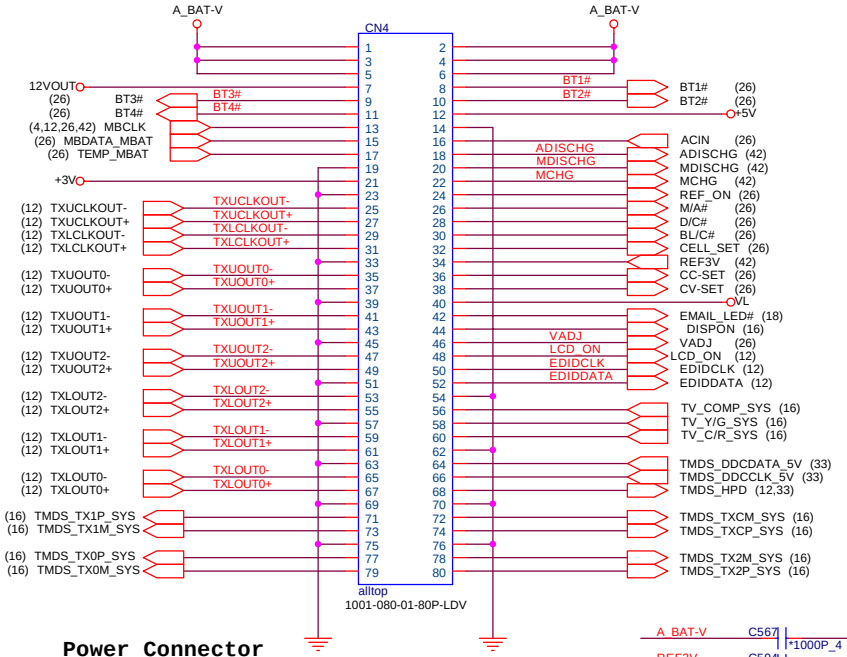
Power Switch



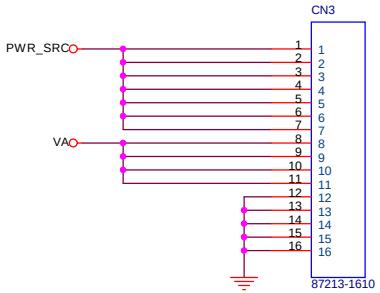
LED

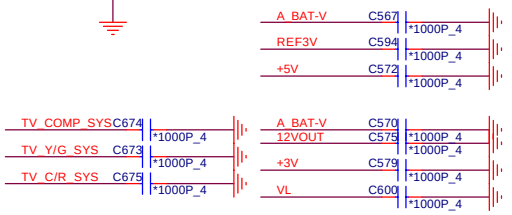
5/28 ADD





Power Connector

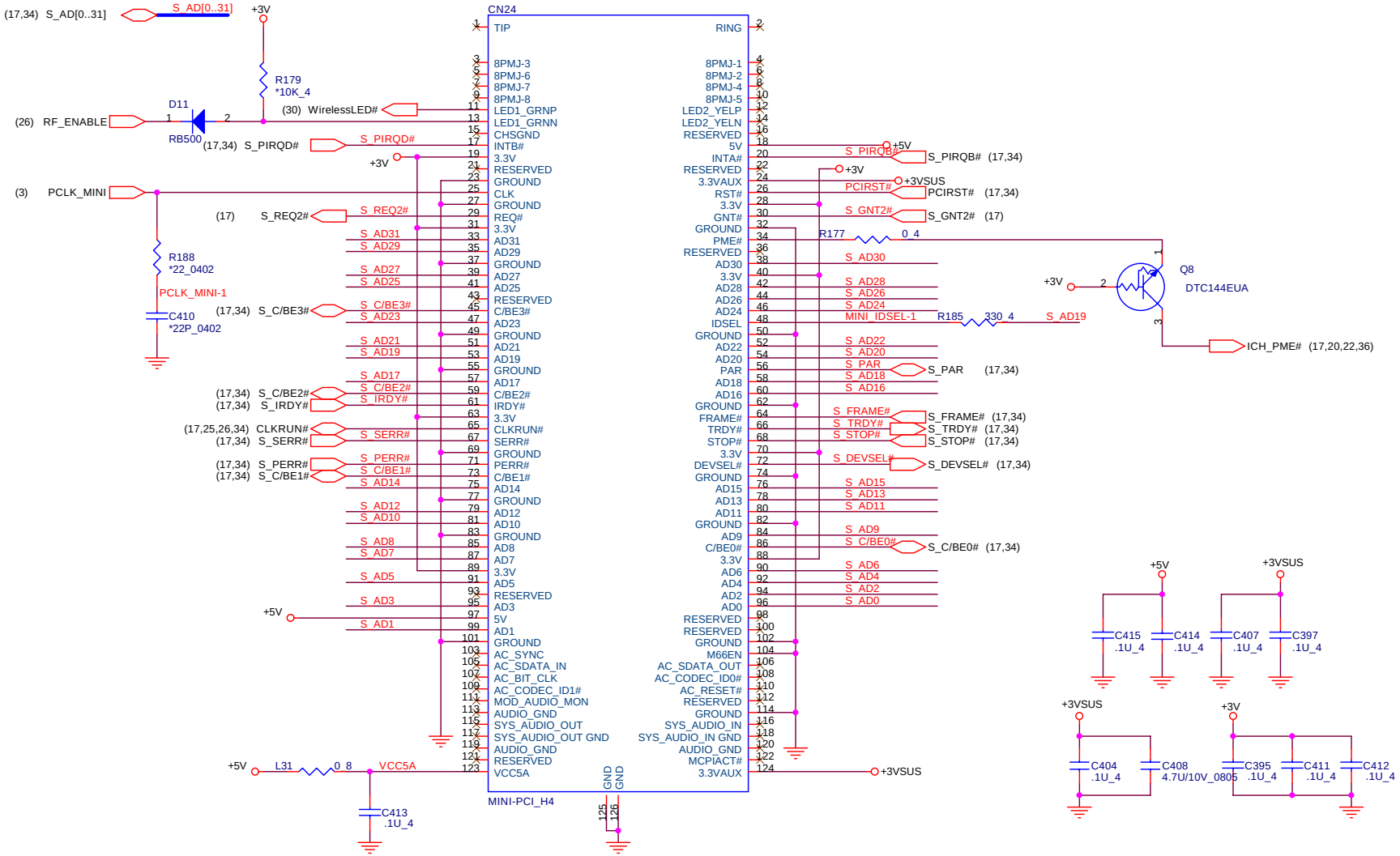




PROJECT : ZF1
Quanta Computer Inc.

Size	Document Number	Rev
A3	LIGHT SENSOR ,TP ,FAN CON	1A

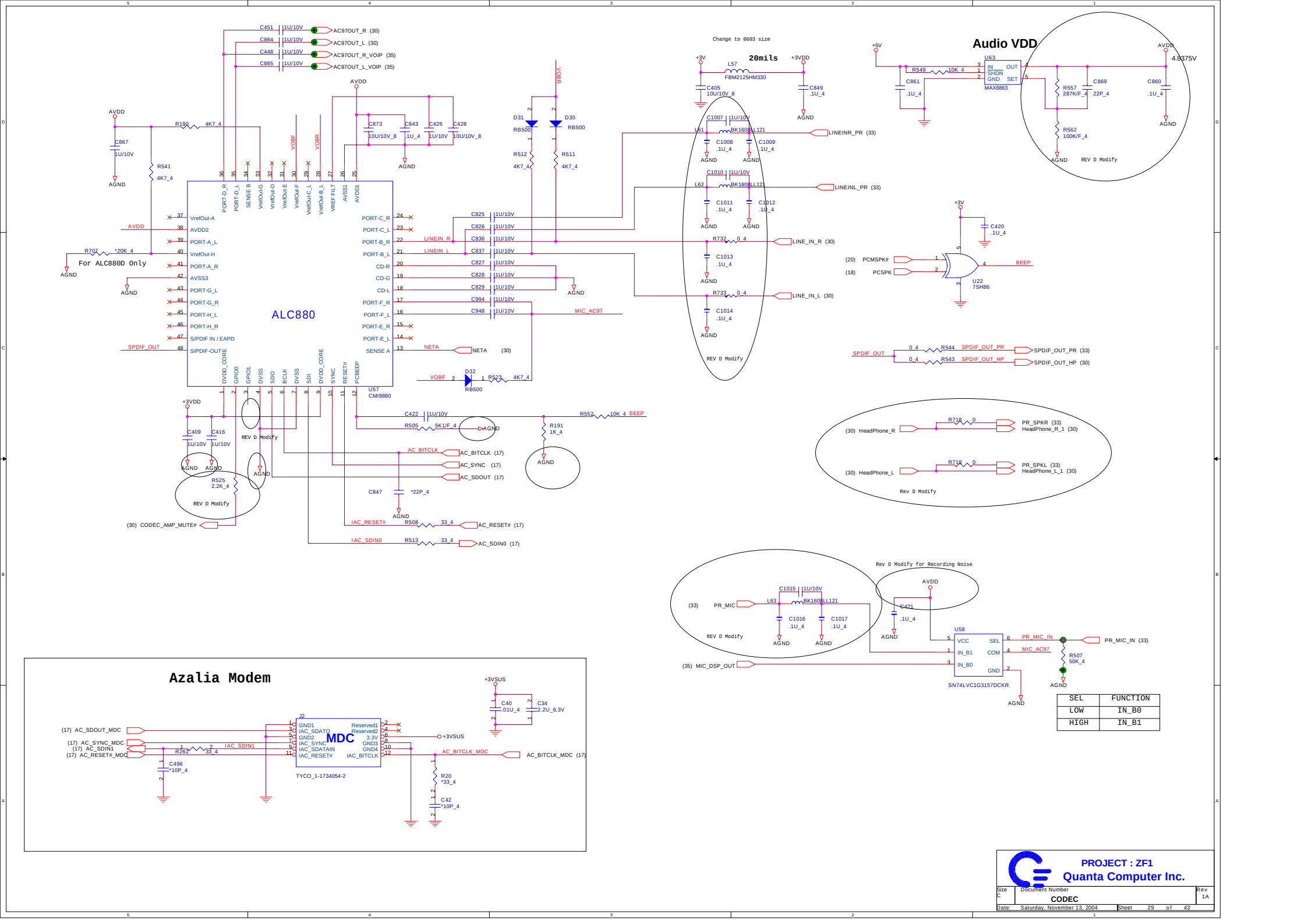
Date: Saturday, November 13, 2004 Sheet 27 of 43



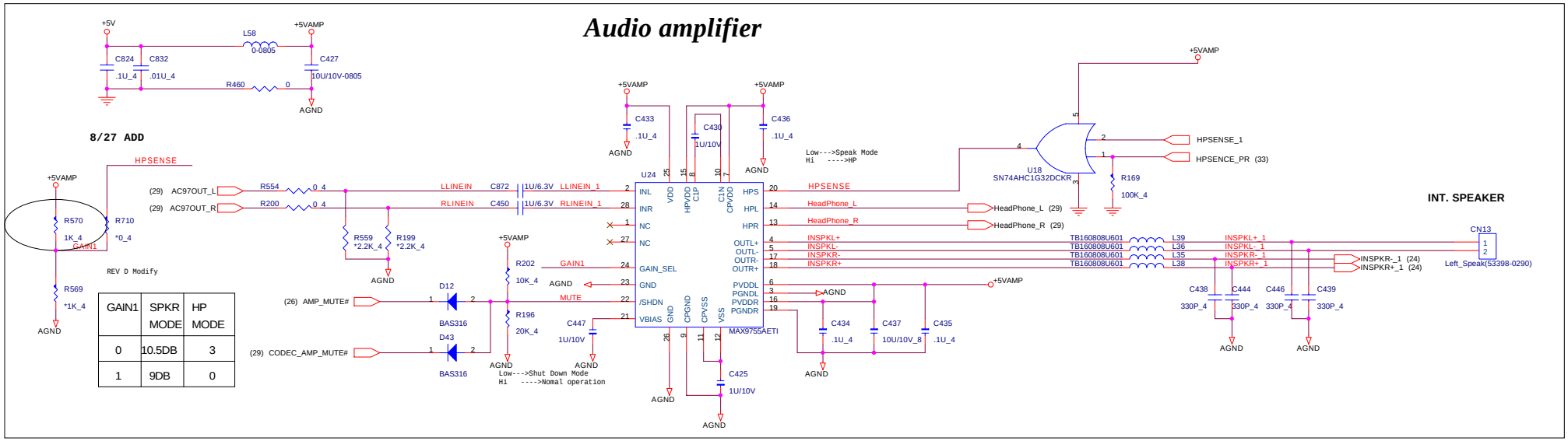
PROJECT : ZF1

Quanta Computer Inc.

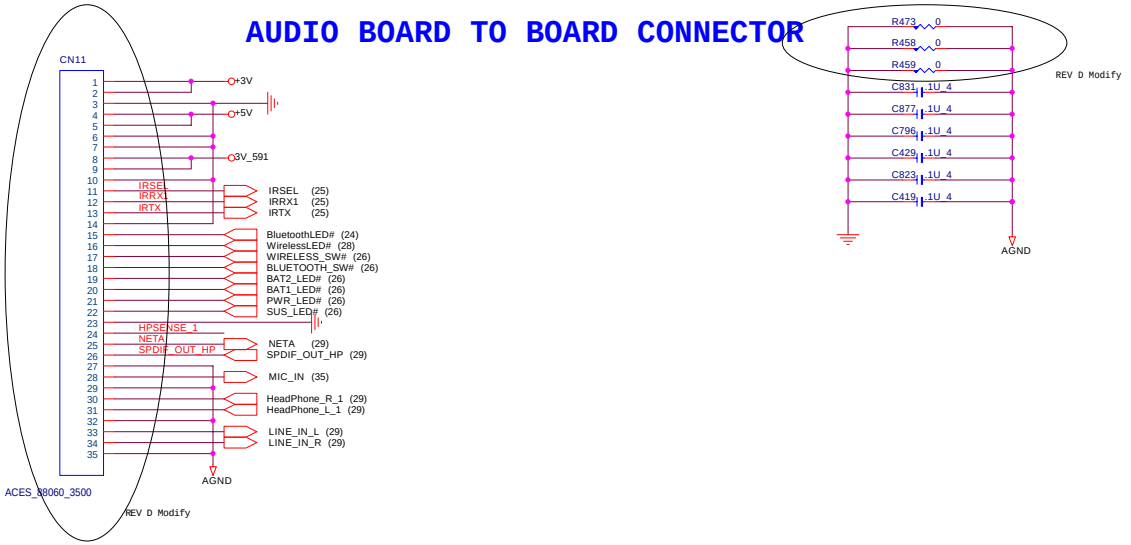
Size	Document Number	Rev
B	MININ PCI	1A
Date: Saturday, November 13, 2004	Sheet 28 of 43	


ALC880
For ALC880D Only
Audio VDD
Azalia Modem
MDC
TYCO_1-1734054-2
U57
CMI9880
U63
MAX8863
U22
7SH86
U58
SN74LVC1G3157DCKR
Change to 0603 size
20mils
REV D Modify
Rev D Modify for Recording Noise
Rev D Modify
AVDD
4.8375V
AGND
+3V
+3VDD
+5V
+3VSUS
LINEIN_R
LINEIN_L
MIC_AC97
NETA
SPDIF_OUT
AC_BITCLK
AC_SYNC
AC_SDOUT
AC_RESET#
IAC_SDIN0
IAC_RESET#
VOBF
VOBR
BEEP
PR_MIC
PR_MIC_IN
MIC_DSP_OUT
CODEC_AMP_MUTE#
LINEINR_PR (33)
LINEINL_PR (33)
LINE_IN_R (30)
LINE_IN_L (30)
SPDIF_OUT_PR (33)
SPDIF_OUT_HP (30)
PR_SPKR (33)
HeadPhone_R_1 (30)
PR_SPKL (33)
HeadPhone_L_1 (30)
PR_MIC_IN (33)
AC97OUT_R (30)
AC97OUT_L (30)
AC97OUT_R_VOIP (35)
AC97OUT_L_VOIP (35)
AC_BITCLK (17)
AC_SYNC (17)
AC_SDOUT (17)
AC_RESET# (17)
AC_SDIN0 (17)
AC_BITCLK_MDC (17)
(17) AC_SDOUT_MDC
(17) AC_SYNC_MDC
(17) AC_SDIN1
(17) AC_RESET#_MDC
PCMSPK#
PCSPK
HeadPhone_R
HeadPhone_L
SEL
FUNCTION
LOW
IN_B0
HIGH
IN_B1
PROJECT : ZF1
Quanta Computer Inc.
CODEC
Saturday, November 13, 2004
Sheet 29 of 43

Audio amplifier



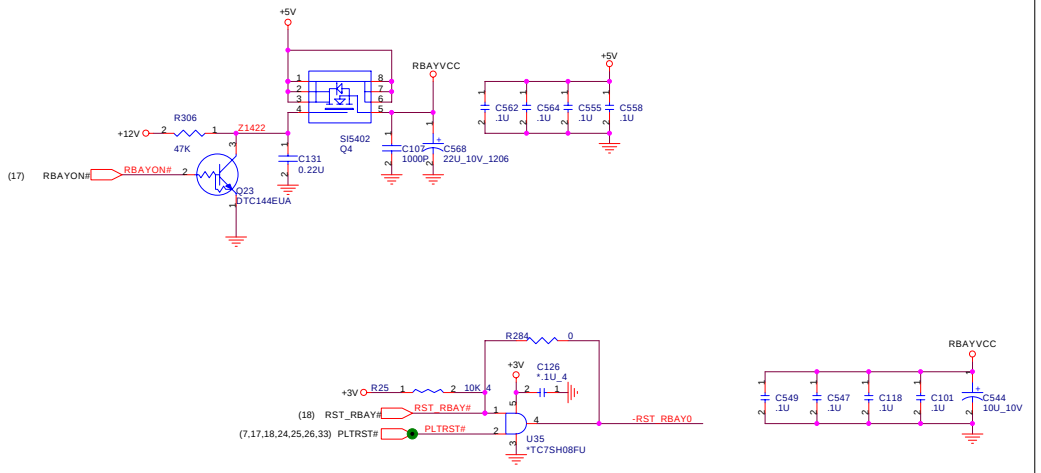
AUDIO BOARD TO BOARD CONNECTOR



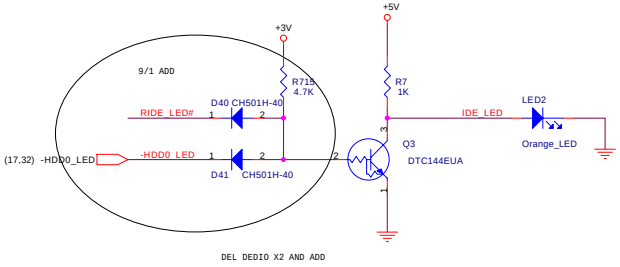
Size: Custom	Document Number: AUDIO AMP & JACK		Rev: 1A
Date: Saturday, November 13, 2004	Sheet 30 of 43		

PROJECT : ZF1
Quanta Computer Inc.

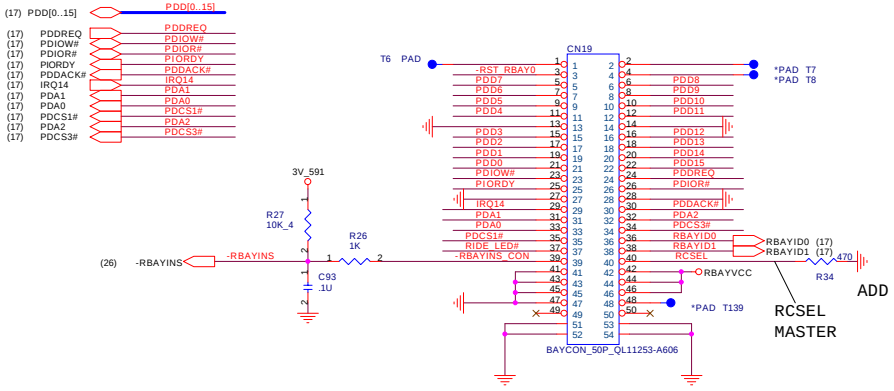
SWAP BAY POWER CONTROL& RESET



IDE LED CONTROL LOGIC

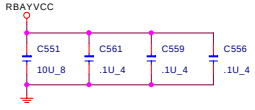


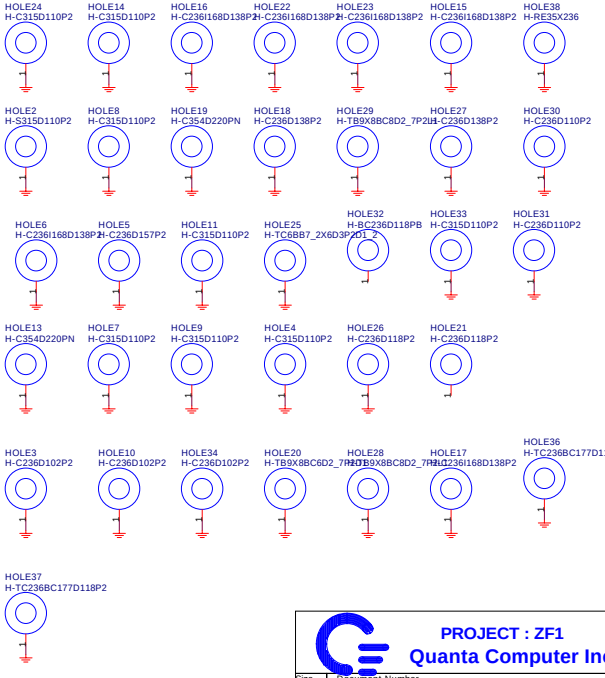
Multi-Bay Connector



BAY ID STATUS

RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	1	HDD
1	0	CD/DVD

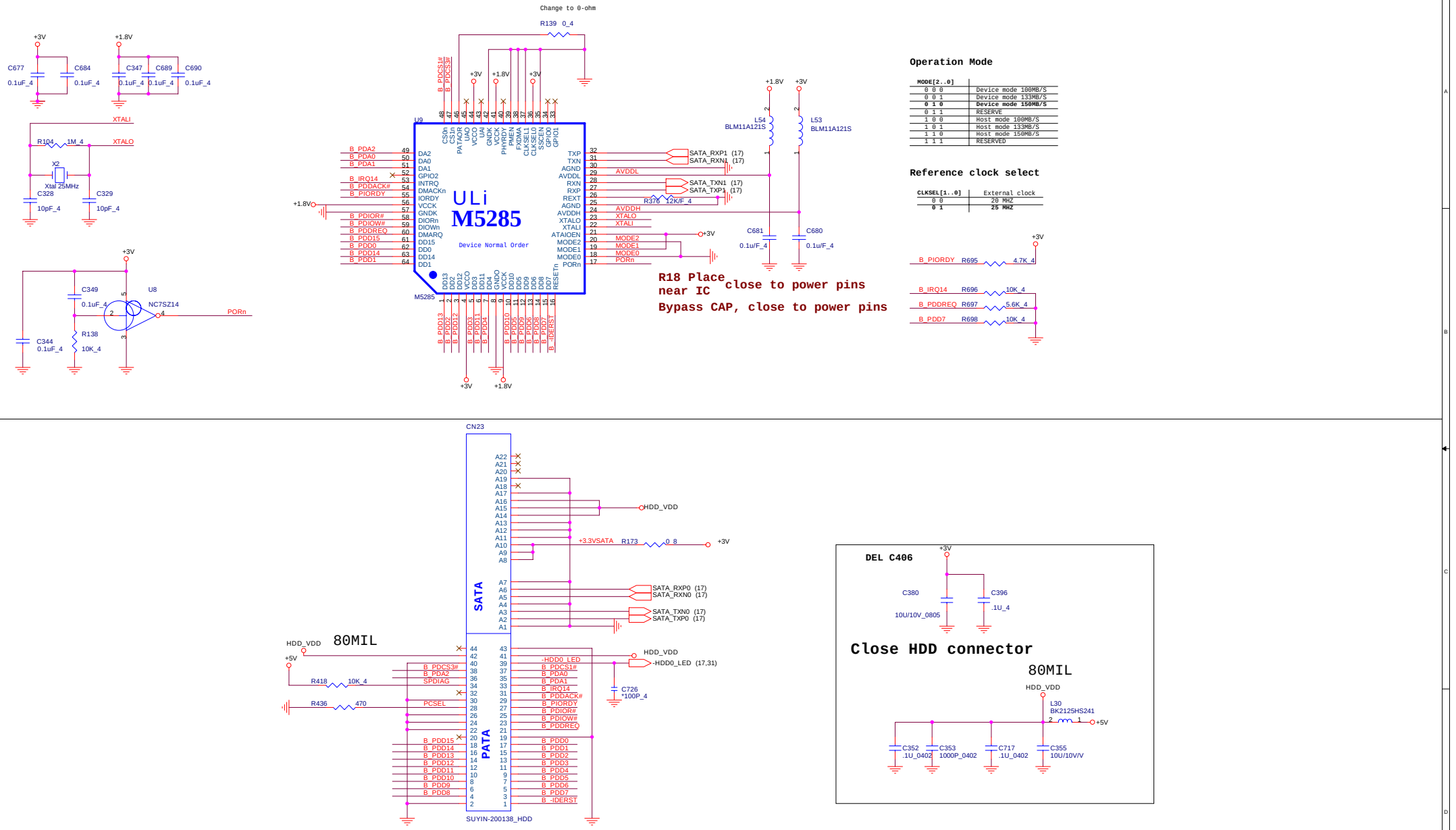


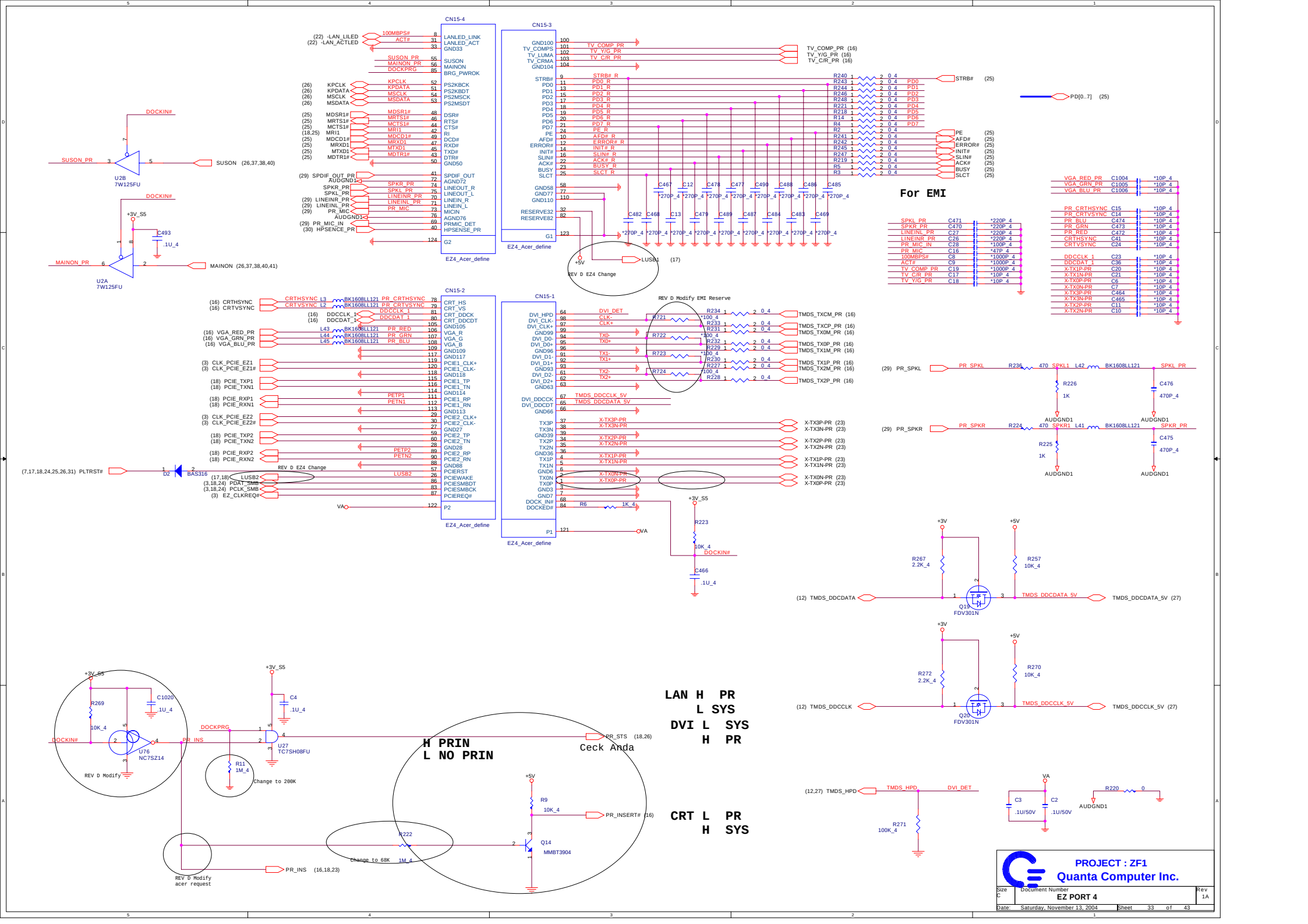


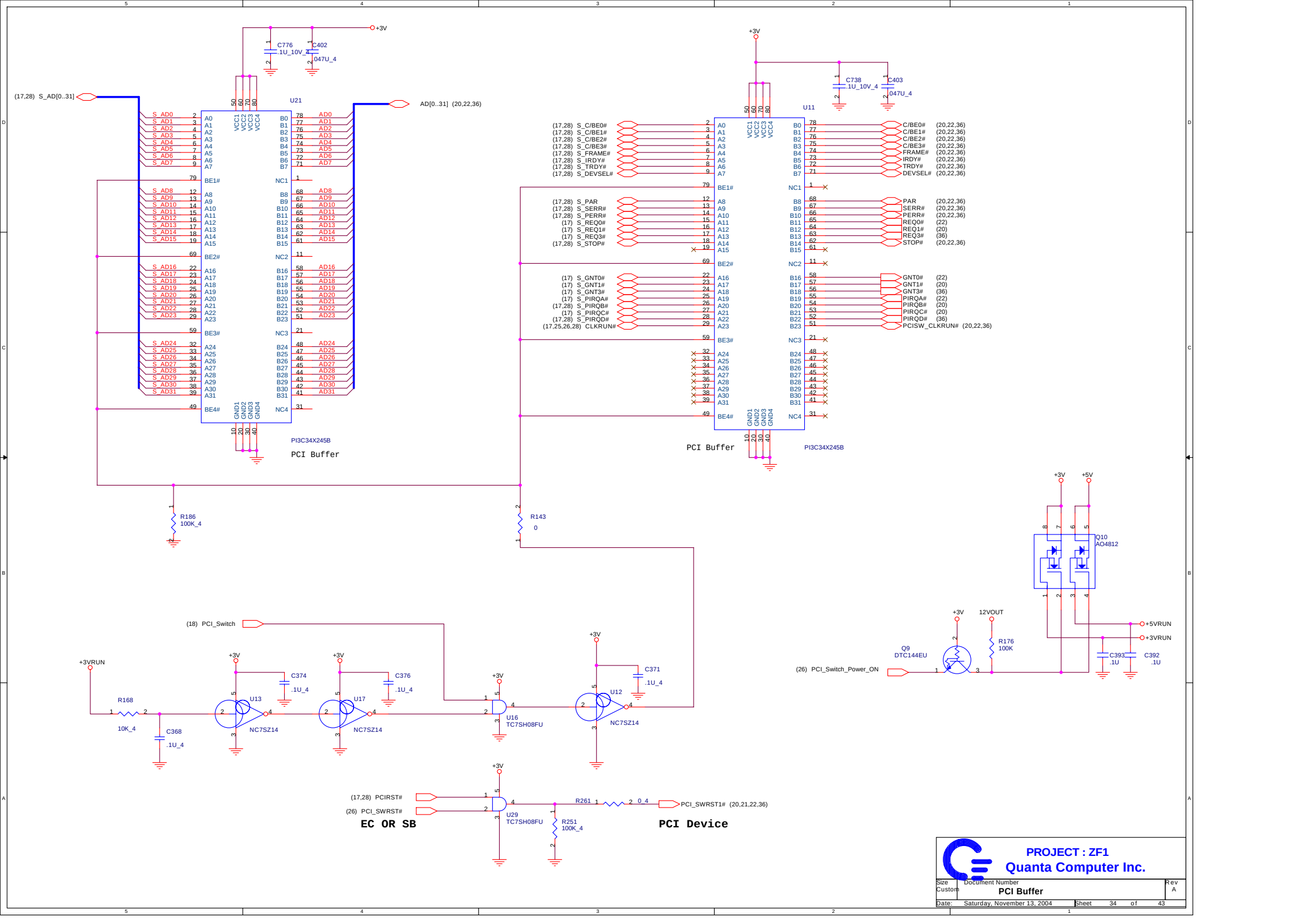
PROJECT : ZF1
Quanta Computer Inc.

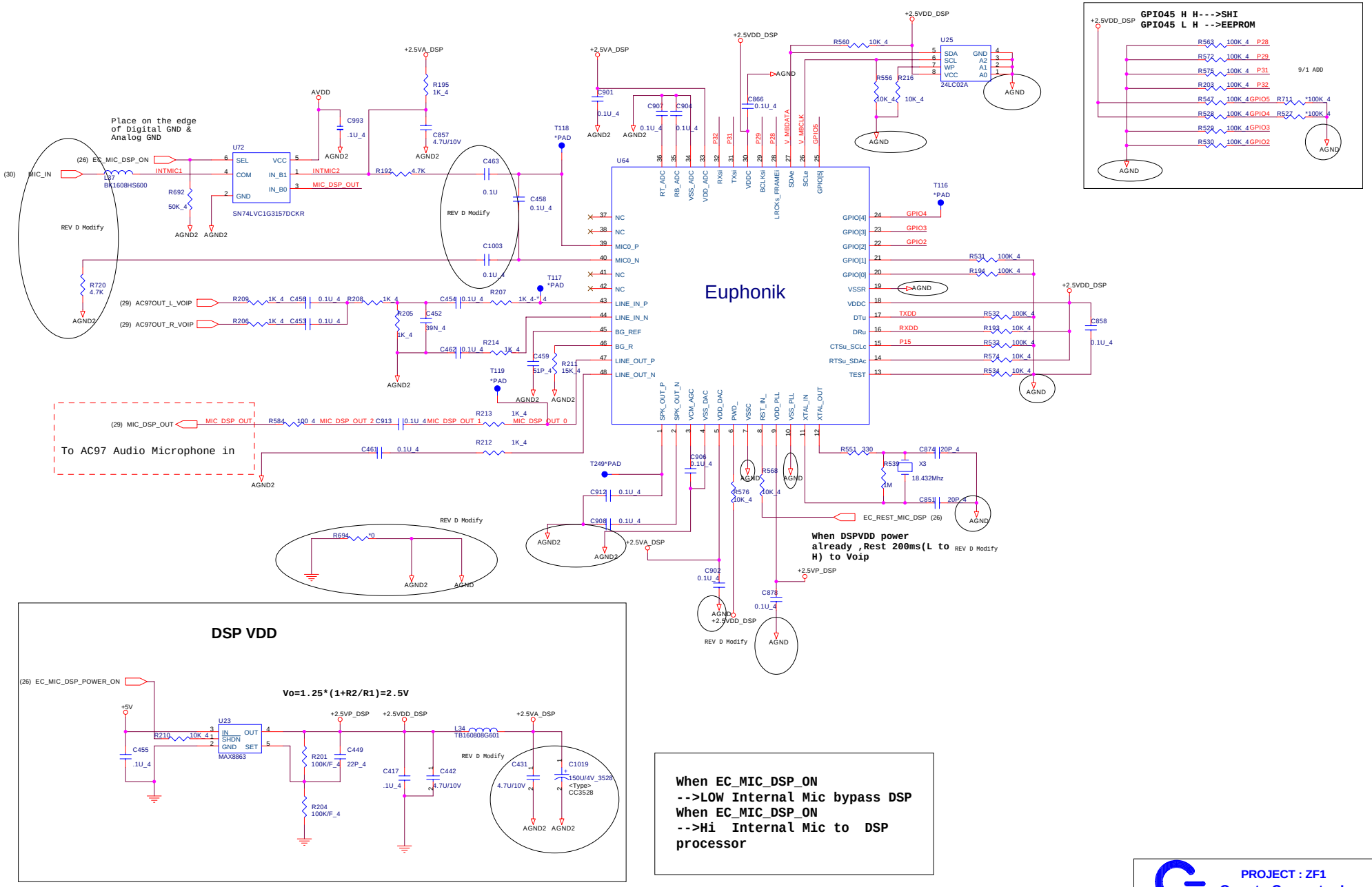
Size	Document Number	Rev
C	Multi-Bay	1A

Date: Monday, November 15, 2004 Sheet 31 of 43


Change to 0-ohm
R139 0_4
U9
ULi
M5285
Device Normal Order
M5285
Operation Mode
MODE[2..0]
0 0 0 Device mode 100MB/S
0 0 1 Device mode 133MB/S
0 1 0 Device mode 150MB/S
0 1 1 RESERVE
1 0 0 Host mode 100MB/S
1 0 1 Host mode 133MB/S
1 1 0 Host mode 150MB/S
1 1 1 RESERVED
Reference clock select
CLKSEL[1..0] External clock
0 0 20 MHZ
0 1 25 MHZ
R18 Place close to power pins near IC
Bypass CAP, close to power pins
CN23
SATA
PATA
80MIL
HDD_VDD
SUYIN-200138_HDD
DEL C406
Close HDD connector
80MIL
PROJECT : ZF1
Quanta Computer Inc.
Size Custom
Document Number HDD
Rev 1A
Date: Saturday, November 13, 2004
Sheet 32 of 43


CN15-4
CN15-3
CN15-2
CN15-1
EZ4_Acer_define
For EMI
REV D Modify EMI Reserve
REV D EZ4 Change
REV D Modify
acer request
Change to 200K
Change to 68K
Ceck Anda
H PRIN
L NO PRIN
LAN H PR
L SYS
DVI L SYS
H PR
CRT L PR
H SYS
PROJECT : ZF1
Quanta Computer Inc.
EZ PORT 4
Document Number
Rev 1A
Size C
Date: Saturday, November 13, 2004
Sheet 33 of 43


(17,28) S_AD[0..31]
AD[0..31] (20,22,36)
U21
PI3C34X245B
PCI Buffer
U11
PI3C34X245B
PCI Buffer
C776 .1U_10V_4
C402 .047U_4
C738 .1U_10V_4
C403 .047U_4
R186 100K_4
R143 0
(18) PCI_Switch
+3VRUN
R168 10K_4
C368 .1U_4
U13 NC7SZ14
U17 NC7SZ14
U16 TC7SH08FU
U12 NC7SZ14
C374 .1U_4
C376 .1U_4
C371 .1U_4
(17,28) PCIRST#
(26) PCI_SWRST#
U29 TC7SH08FU
R251 100K_4
R261 0_4
PCI_SWRST1# (20,21,22,36)
EC OR SB
PCI Device
Q10 AO4812
Q9 DTC144EU
R176 100K
(26) PCI_Switch_Power_ON
12VOUT
+5VRUN
+3VRUN
C393 .1U
C392 .1U
PROJECT : ZF1
Quanta Computer Inc.
Size Custom
Document Number PCI Buffer
Rev A
Date: Saturday, November 13, 2004
Sheet 34 of 43


Euphonik
Place on the edge of Digital GND & Analog GND
REV D Modify
To AC97 Audio Microphone in
When DSPVDD power already ,Rest 200ms(L to H) to Voip
GPIO45 H H--->SHI
GPIO45 L H -->EEPROM
9/1 ADD
DSP VDD
Vo=1.25*(1+R2/R1)=2.5V
When EC_MIC_DSP_ON
-->LOW Internal Mic bypass DSP
When EC_MIC_DSP_ON
-->Hi Internal Mic to DSP processor
PROJECT : ZF1
Quanta Computer Inc.
Document Number
Euphonik
Rev A
Date: Saturday, November 13, 2004
Sheet 35 of 43

IEEE-1394

Used for vccp
(Pin20,35,48,62,78)

Used for vcc3
(Pin15,27,39,51,59,72,88,100)

Used for AVCC
(Pin1,2,107,108,120)

ID Select	: AD23
Interrupt Pin	: PIRQD#
Request indicates	: REQ3#
Grant indicates	: GNT3#

U68 TSB43AB21PDT

PCI INTERFACE

PHY PORT 0 · BIAS CURRENT · CRYSTAL · FILTER · EEPROM BUS · PHY PORT 1 · POWER CLASS

1394 EEPROM U69 NM24C02-WMN6T

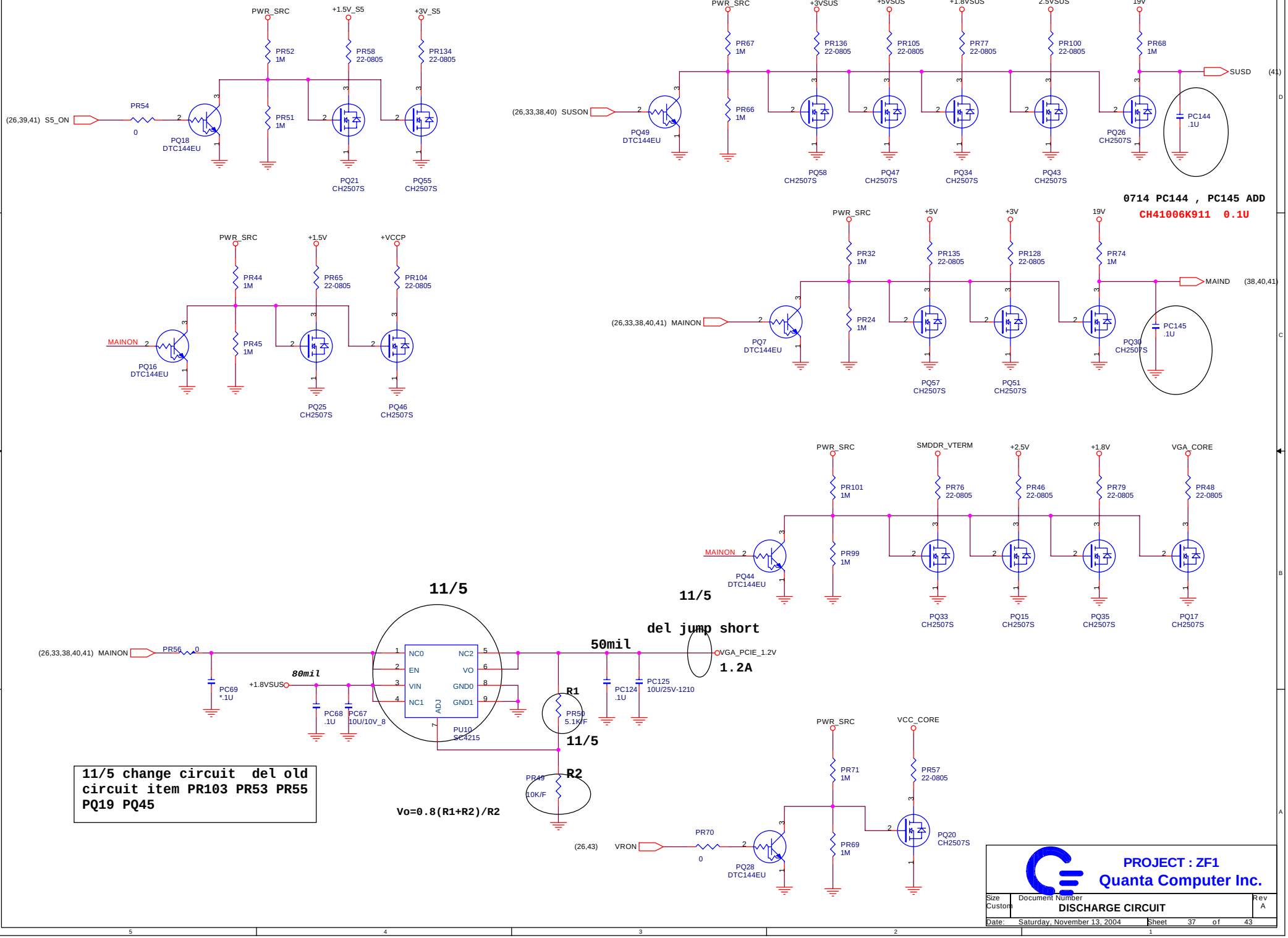
PLW3216S900SQ2B1 CN22 CONN-1394

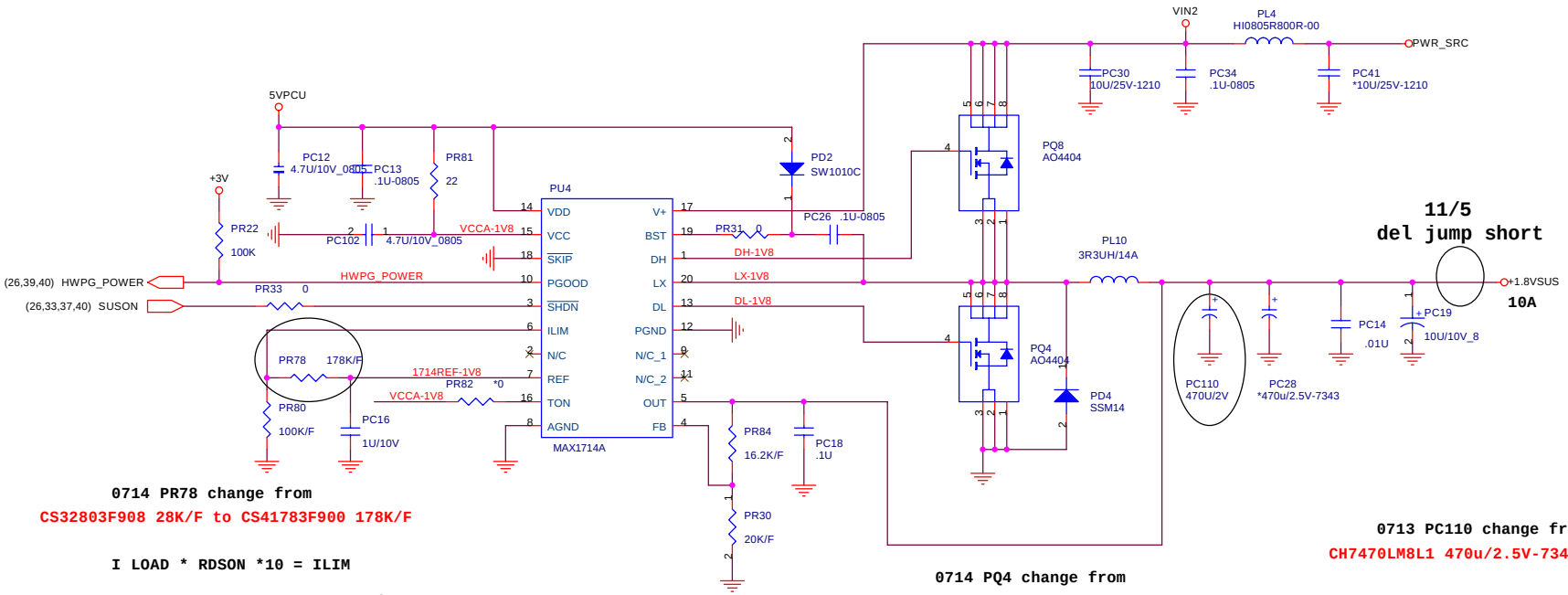
Q61 DTC144EU

For ATE

Title	TSB43AB21[1394]
Size	Document Number ZF1
Rev	D
Date:	Saturday, November 13, 2004
Sheet	36 of 43

QUANTA COMPUTER


PWR_SRC
+1.5V_S5
+3V_S5
PR52 1M
PR58 22-0805
PR134 22-0805
(26,39,41) S5_ON
PR54 0
PQ18 DTC144EU
PR51 1M
PQ21 CH2507S
PQ55 CH2507S
PWR_SRC
+3VSUS
+5VSUS
+1.8VSUS
2.5VSUS
19V
PR67 1M
PR136 22-0805
PR105 22-0805
PR77 22-0805
PR100 22-0805
PR68 1M
SUSD (41)
(26,33,38,40) SUSON
PQ49 DTC144EU
PR66 1M
PQ58 CH2507S
PQ47 CH2507S
PQ34 CH2507S
PQ43 CH2507S
PQ26 CH2507S
PC144 .1U
0714 PC144 , PC145 ADD
CH41006K911 0.1U
PWR_SRC
+1.5V
+VCCP
PR44 1M
PR65 22-0805
PR104 22-0805
MAINON
PQ16 DTC144EU
PR45 1M
PQ25 CH2507S
PQ46 CH2507S
PWR_SRC
+5V
+3V
19V
PR32 1M
PR135 22-0805
PR128 22-0805
PR74 1M
MAIND (38,40,41)
(26,33,38,40,41) MAINON
PQ7 DTC144EU
PR24 1M
PQ57 CH2507S
PQ51 CH2507S
PQ30 CH2507S
PC145 .1U
PWR_SRC
SMDDR_VTERM
+2.5V
+1.8V
VGA_CORE
PR101 1M
PR76 22-0805
PR46 22-0805
PR79 22-0805
PR48 22-0805
MAINON
PQ44 DTC144EU
PR99 1M
PQ33 CH2507S
PQ15 CH2507S
PQ35 CH2507S
PQ17 CH2507S
11/5
11/5
del jump short
50mil
(26,33,38,40,41) MAINON
PR56 0
80mil
+1.8VSUS
PC69 *.1U
PC68 .1U
PC67 10U/10V_8
NC0
EN
VIN
NC1
NC2
VO
GND0
GND1
ADJ
PU10 SC4215
PC124 .1U
PC125 10U/25V-1210
VGA_PCIE_1.2V
1.2A
R1
PR50 5.1K/F
11/5
R2
PR49 10K/F
Vo=0.8(R1+R2)/R2
11/5 change circuit del old circuit item PR103 PR53 PR55 PQ19 PQ45
PWR_SRC
VCC_CORE
PR71 1M
PR57 22-0805
PR70
(26,43) VRON
0
PQ28 DTC144EU
PR69 1M
PQ20 CH2507S
PROJECT : ZF1
Quanta Computer Inc.
Size Custom
Document Number
DISCHARGE CIRCUIT
Rev A
Date: Saturday, November 13, 2004
Sheet 37 of 43



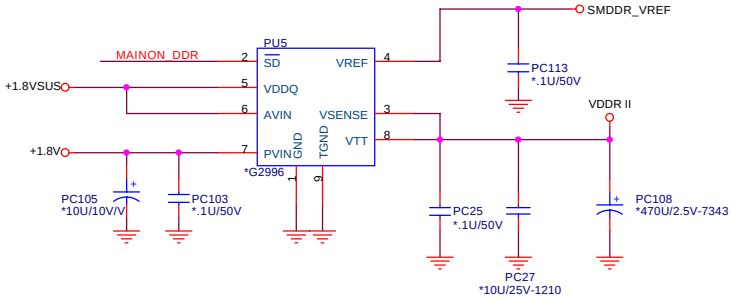
0714 PR78 change from
CS32803F908 28K/F to CS41783F900 178K/F

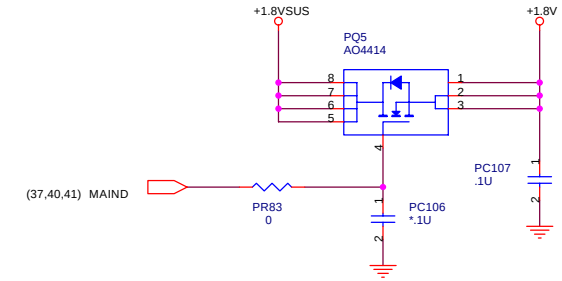
I LOAD * RDSON *10 = ILIM

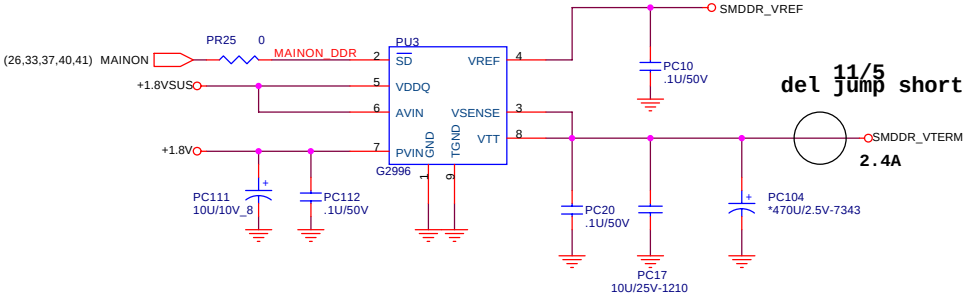
FDD6688 RDSON 4.5V = 0.006 ohm
12 * 0.006 *10 = 0.72V (ILIM)

0714 PQ4 change from
BAM47040005 AO4704 to BAM66880Z01 FDD6688
0714 PD4 change from
NC to BC000014Z01 SSM14

0713 PC110 change from
CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343





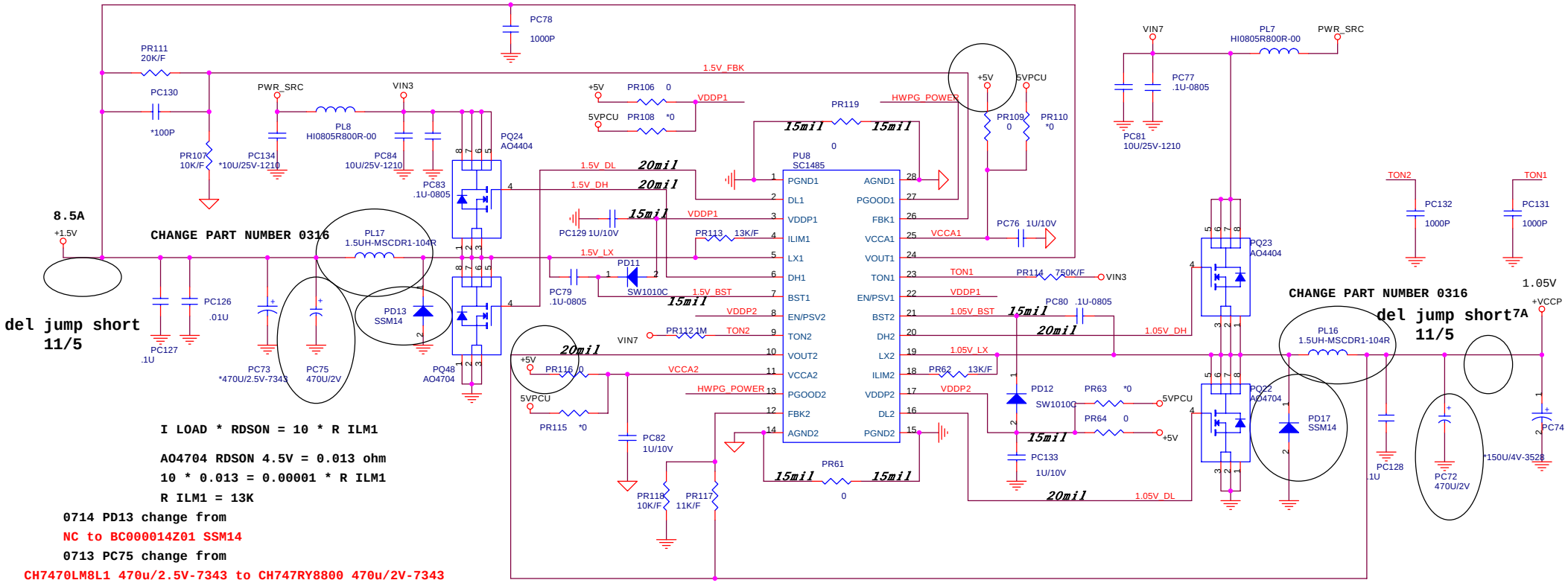


PROJECT : ZF1

Quanta Computer Inc.

Size	Document Number	Rev
	2.5VSUS, +2.5V, & 1.25DDR	2A

Date: Saturday, November 13, 2004 Sheet 38 of 43



I LOAD * RDSON = 10 * R ILM1

AO4704 RDSON 4.5V = 0.013 ohm
10 * 0.013 = 0.00001 * R ILM1
R ILM1 = 13K

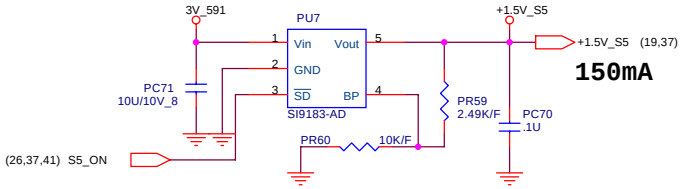
0714 PD13 change from
NC to BC000014Z01 SSM14
0713 PC75 change from
CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343

(26,38,40) HWPG_POWER HWPG_POWER

I LOAD * RDSON = 10 * R ILM

AO4704 RDSON 4.5V = 0.013 ohm
10 * 0.013 = 0.00001 * R ILM
R ILM1 = 13K

0714 PD817change from
NC to BC000014Z01 SSM14
0713 PC72 change from
CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343



PROJECT : ZF1
Quanta Computer Inc.

Size	Document Number	Rev
	2.5VSUS, +2.5V, & 1.25DDR	2A
Date: Saturday, November 13, 2004	Sheet 39 of 43	

0714 PR37 change from
CS21823F902 1.82K/F to CS27683F909 7.68K/F
0714 PL13 change from
CV-15A0MZ05 1R5 to CV-33E0MZ01 3R3
0714 PQ11 change from
BAM44040012 AO4404 to BAM60300Z11 FDD6030L
0714 PQ37 change from
BAM47040005 AO4704 to BAM66880Z01 FDD6688

L / RL(DCR) = Cqe * Rqe

3R3 DCR = 0.0043
3.3u / 0.0043 = 0.1u * Rqe
Rqe = 7.68K

L / RL(DCR) = Cqe * Rqe

3R8 DCR = 0.0130
3.8u / 0.0130 = 0.1u * Rqe
Rqe = 2.94K

del jump short
11/5

del jump short
11/5

1.2V/1.0V
VGA_CORE
12A

2.5VSUS
4A

0714 PC118 change from
NC to CH747RY8800 470u/2.5V-7343

0713 PC57 change from
CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343

0714 PD8 change from
NC to BC000014Z01 SSM14

I LOAD * DCR *10 = ILIM

3R3 DCR = 0.0043
16 * 0.0043 *10 = 0.688V (ILIM1)
1R5 DCR = 0.0081
6 * 0.0130 *10 = 0.78V (ILIM2)

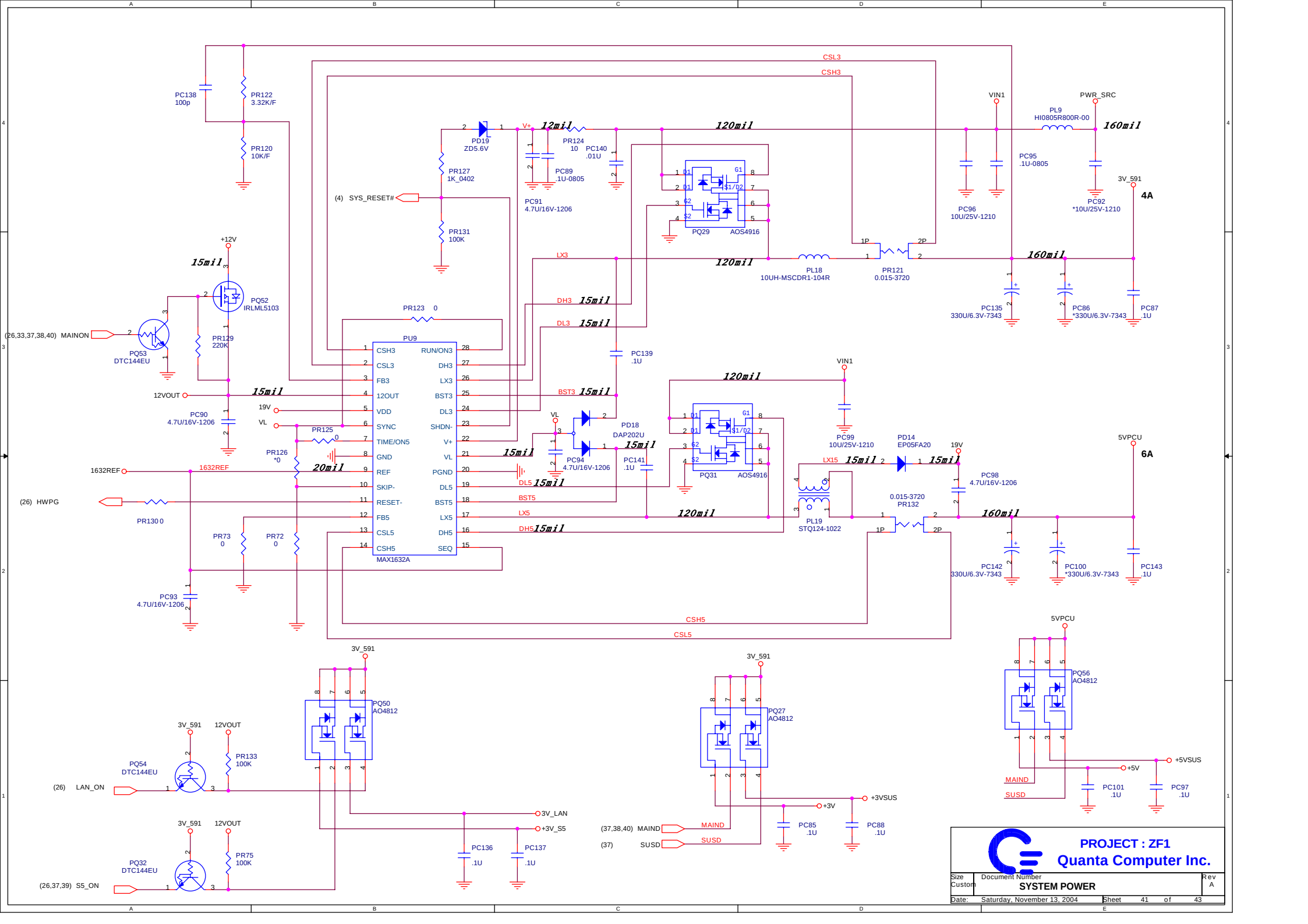
Low: 1.2V
High: 1.0V

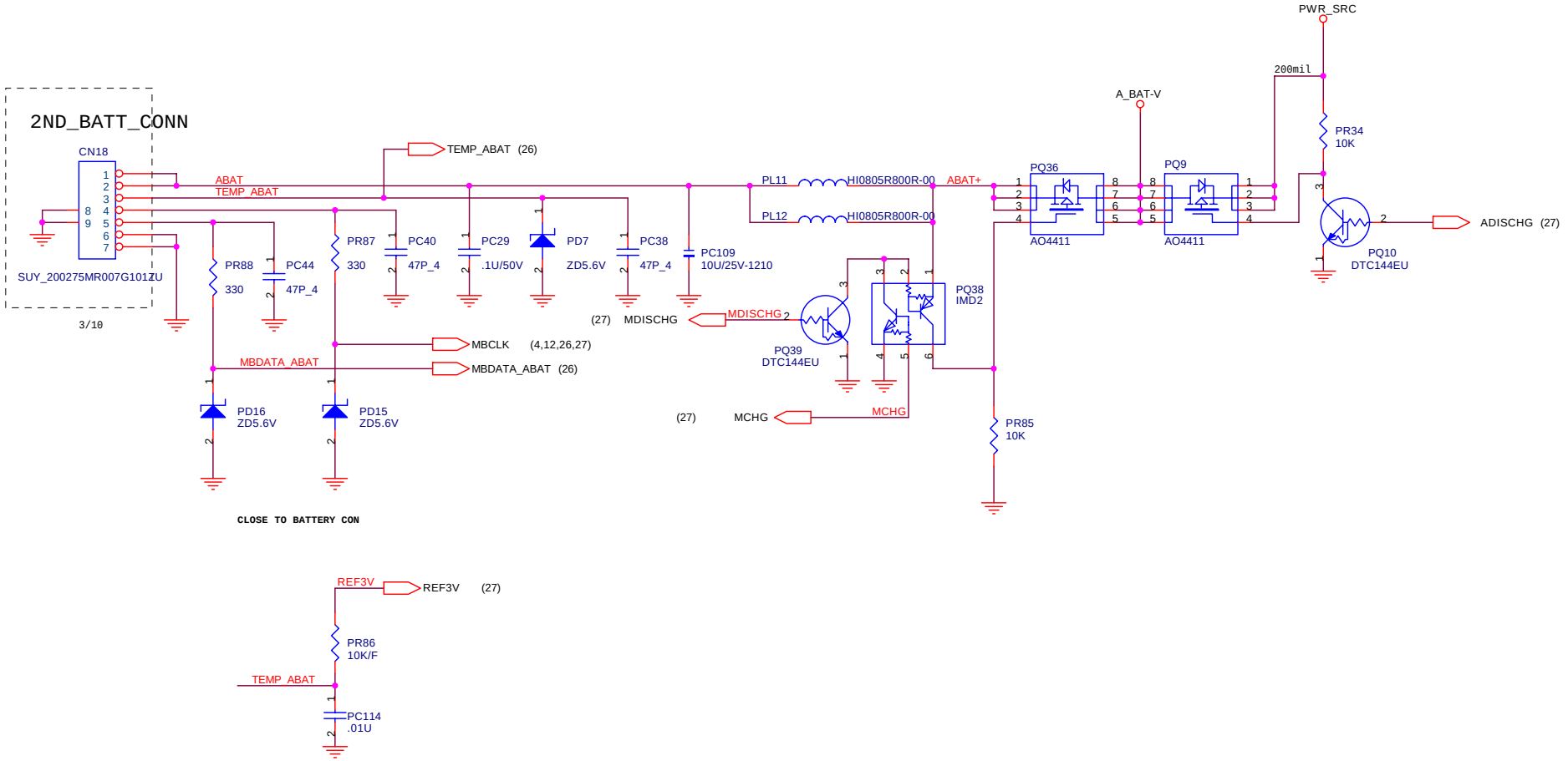
0714 PR137 ADD
CS01003F902 10
0714 PC146 ADD
CH41006K911 0.1U

0714 PR93 change from
CS34993F908 49.9K/F to CS35233F908 52.3K/F

PROJECT : ZF1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA POWER	1A
Date: Saturday, November 13, 2004	Sheet 40 of 43	


PC138 100p
PR122 3.32K/F
PR120 10K/F
CSL3
CSH3
VIN1
PWR_SRC
PL9 HI0805R800R-00
160mil
PD19 ZD5.6V
V+
12mil
PR124 10
PC140 .01U
PC89 .1U-0805
120mil
PC95 .1U-0805
PC96 10U/25V-1210
PC92 *10U/25V-1210
3V_591
4A
PR127 1K_0402
(4) SYS_RESET#
PC91 4.7U/16V-1206
PR131 100K
PQ29 AOS4916
LX3
PL18 10UH-MSCDR1-104R
PR121 0.015-3720
PC135 330U/6.3V-7343
PC86 *330U/6.3V-7343
PC87 .1U
+12V
15mil
PQ52 IRLML5103
(26,33,37,38,40) MAINON
PQ53 DTC144EU
PR129 220K
PR123 0
PU9
DH3
DL3
PC139 .1U
12VOUT
19V
VL
PC90 4.7U/16V-1206
PR125 0
PR126 *0
20mil
BST3
PD18 DAP202U
PC94 4.7U/16V-1206
PC141 .1U
PQ31 AOS4916
VIN1
PC99 10U/25V-1210
PD14 EP05FA20
19V
5VPCU
6A
LX15
PC98 4.7U/16V-1206
0.015-3720
PR132
PL19 STQ124-1022
PC142 330U/6.3V-7343
PC100 *330U/6.3V-7343
PC143 .1U
1632REF
(26) HWPG
PR130 0
PR73 0
PR72 0
PC93 4.7U/16V-1206
BST5
LX5
DH5
DL5
CSH5
CSL5
CSH3
CSL3
FB3
12OUT
VDD
SYNC
TIME/ON5
GND
REF
SKIP-
RESET-
FB5
CSL5
CSH5
RUN/ON3
DH3
LX3
BST3
DL3
SHDN-
V+
VL
PGND
DL5
BST5
LX5
DH5
SEQ
MAX1632A
3V_591
PQ50 AO4812
PQ27 AO4812
PQ56 AO4812
PQ54 DTC144EU
PR133 100K
(26) LAN_ON
PQ32 DTC144EU
PR75 100K
(26,37,39) S5_ON
3V_LAN
+3V_S5
PC136 .1U
PC137 .1U
(37,38,40) MAIND
(37) SUSD
+3V
+3VSUS
PC85 .1U
PC88 .1U
+5V
+5VSUS
PC101 .1U
PC97 .1U
PROJECT : ZF1
Quanta Computer Inc.
Size Custom
Document Number
SYSTEM POWER
Rev A
Date: Saturday, November 13, 2004
Sheet 41 of 43



PROJECT : ZL1

Quanta Computer Inc.

Size	Document Number	Rev
	BATTERY SELECT	A1A
Date: Saturday, November 13, 2004	Sheet 42 of 43	

0714 PR19 change from
CS34223F901 42.2K/F to CS38253F909 82.5K/F

value provied 2.67% offset; old value was for old 4.62% offset.

BG waveforms improved. may delete from future revision.

0714 PR27 change from
CS-33304JA09 3.3 to CS00004JA07 0

CHANGE CHOCK 0316

0714 PR26 change from
CS17503F907 750/F to CS14753F905 475/F

0714 PR29 , PR21 change from
CS21543F901 1.54K/F to CS17153F905 715/F

0714 PC6 change from
CH16806J903 680p to CH12706J909 270p

0714 PC3 change from
CH31006K919 0.01u to CH31506K917 0.015u

0714 PR13 change from
CS32213F901 22.1K/F to CS33653F906 36.5K/F

0714 PR20 change from
CS32003F909 20K/F to CS33323F901 33.2K/F

0714 PR23 change from
CS33323F901 33.2K/F to CS35493F902 54.9K/F

0714 PR11 change from
NC to CS42493F906 249K/F

0713 PC122 , PC66 change from
CH7470LM8L1 470u/2.5V-7343 to CH747RY8800 470u/2V-7343

12mOhm 7343 SP-CAP

Set up for constant-ripple mode. Was constantfrequency mode

20 mil Trace list for layout

Added filter for PBOOT

100 mil Trace list for layout

DH_VCORE
LX_VCORE
DL_VCORE
DH_VCORE2
LX_VCORE2
DL_VCORE2

10 mil Trace list for layout

SC1476
pin 4 pin
5 pin 7
pin 25
pin 30

Change to NOR GATE

160mil

V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

PROJECT : ZF1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU POWER	1A
Date: Saturday, November 13, 2004	Sheet 43 of 43	