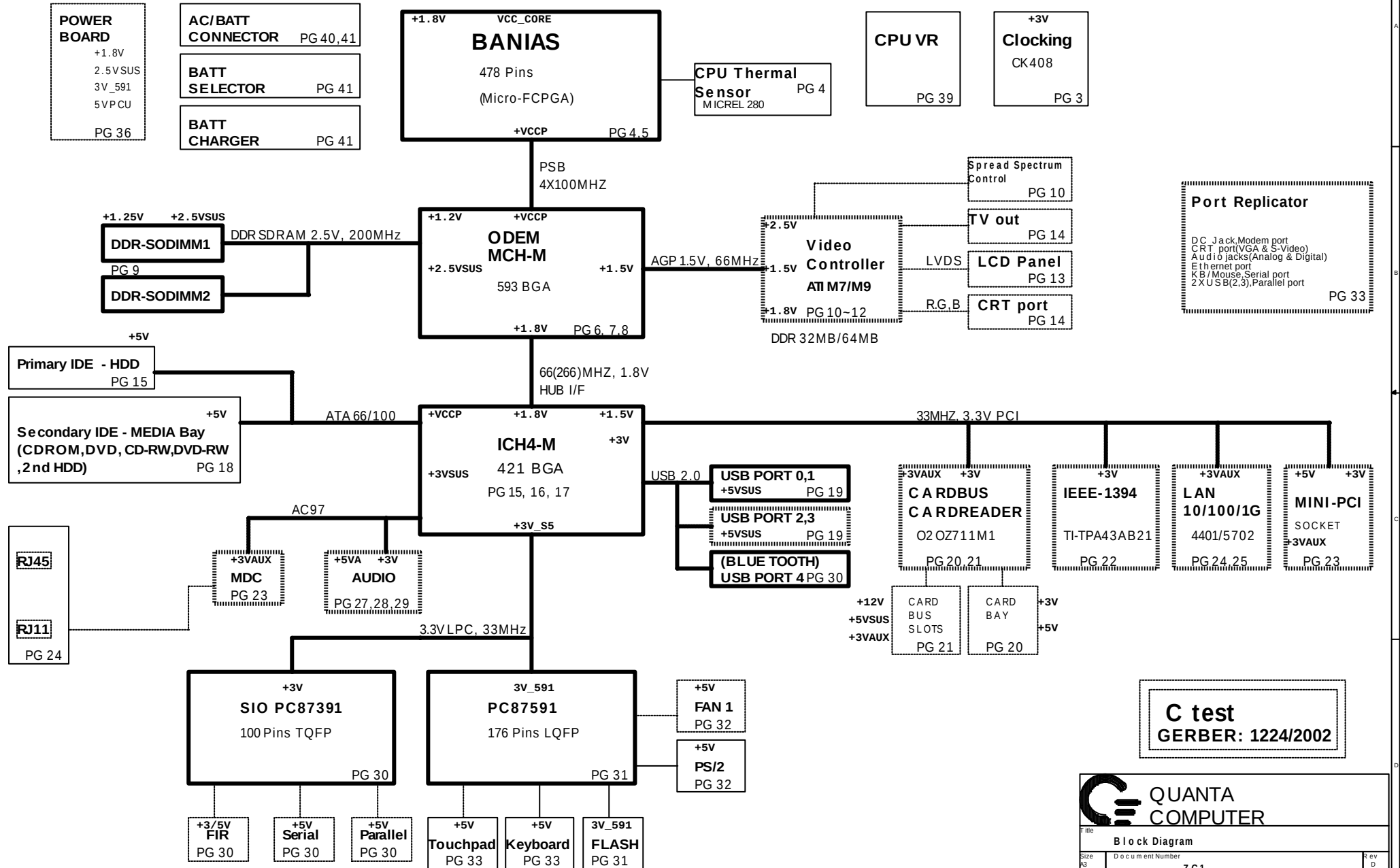


ZG1 BLOCK DIAGRAM

BANIAS / ODEM



Voltage Rails		ON S0-S1	ON S3	ON S4	ON S5	Control signal
CPU_CORE	Core voltage for Processor	X				VR_ON
+VCCP	1.05V rail for Processor I/O	X				VR_ON
+1.2V	1.2V for ODEM Core	X				
+1.25V	1.25V for DDR Termination voltage	X	X			SU_SON
+1.5V		X				
+1.5V		X				
+1.5V S5		X	X	X		
+1.8V		X				
+2.5 VSUS		X	X			
+2.5V		X				
+2.5 VSUS	2.5V for DDR Termination voltage	X				MAINON
3V_S91		X	X	X	X	
+3 VSUS		X	X			
+3V		X				
5VPCU		X	X	X	X	
+5 VSUS		X	X			
+5V		X				
+12V		X				
+12VOUT		X	X	X	X	

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
LAN	AD18	0	RRQD
CardBus	AD22	3	RRQB
Mini-PCI	AD20	1	RRQE/F
Mini-PCI LAN			
IEEE-1394 Controller	AD23	2	RRQC
AGP VGA	AD17 (INTERNAL)		PIRQA

EC SM Bus1 address

Device
Smart Battery
THERMAL SENSOR

ICH4-M SM Bus address

Device
SODIMM 1010 000X b
Clock Gen 1101 001x b



QUANTA
COMPUTER

File

CLOCK GENERATOR

Size

A3

Document Number

Z G1

Date

Friday, December 27, 2002

Sheet

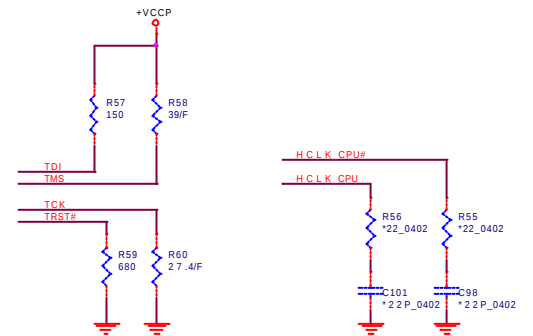
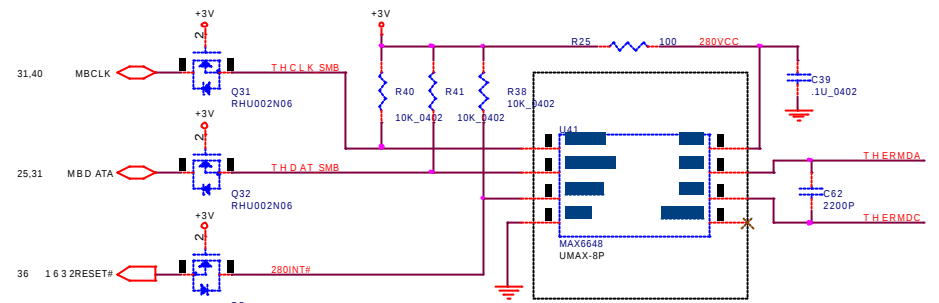
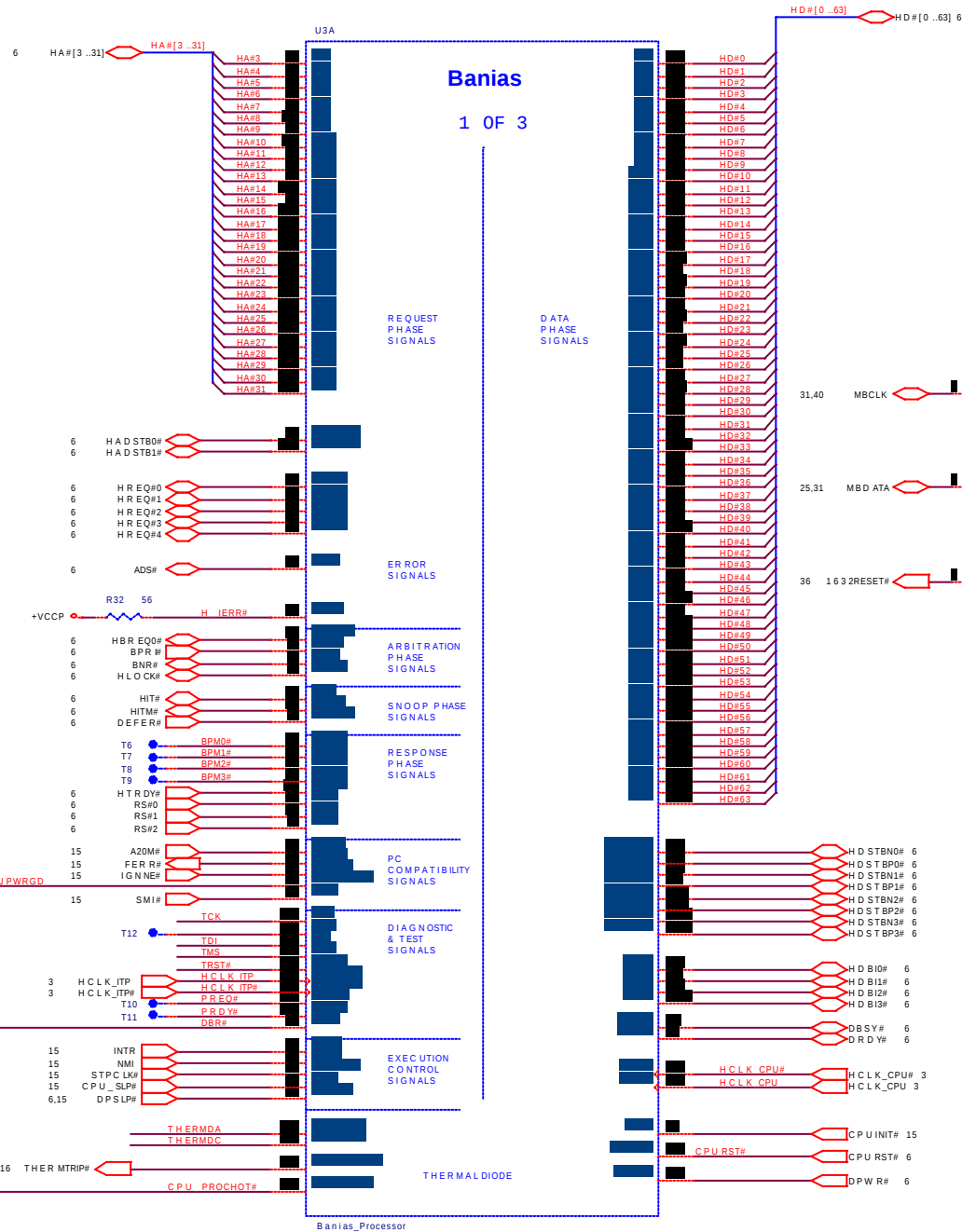
2 of 40

Rev

D

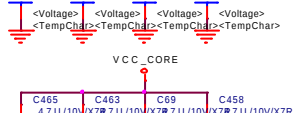
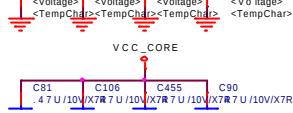
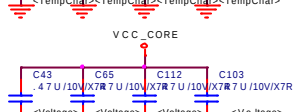
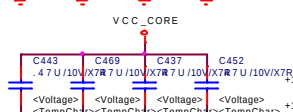
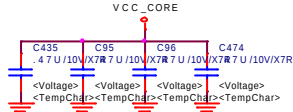
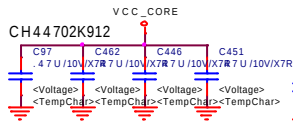
✓





BANIAS CPU - A

ESR < 3m OHM



25 MILS (>50 MILS PREFFERD) SPACE

T < 0.5"

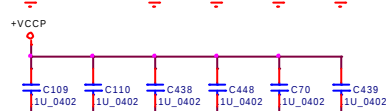
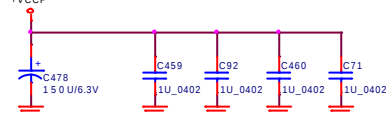
CHECK LAYOUT NOTES

GTLREF: 2/3 VCCP+-2%
T<0.5" 25 mils space

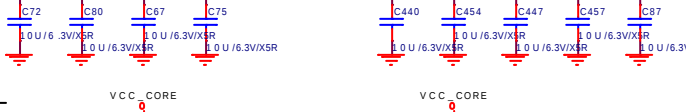
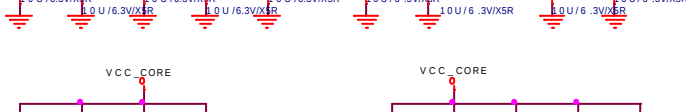
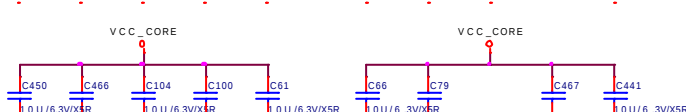
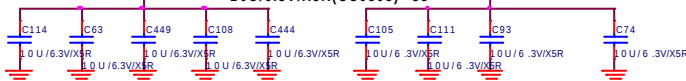
A0: STUFF
A1: NC

CPU VCCA

VCC_CORE



100U/6.3V/X5R(CC0805) *38



Banias
2 OF 3

POWER,
GROUND,
RESERVED
SIGNALS

Banias
3 OF 3

POWER, GROUND AND NC

VID

38 CPU_VID0
38 CPU_VID1
38 CPU_VID2
38 CPU_VID3
38 CPU_VID4
38 CPU_VID5

R39 *5.4 9/F Z0501

R35 *5.4 9/F Z0502

T4 Z0503

T5 Z0504

T13 Z0505

T3 Z0506

T2 Z0507

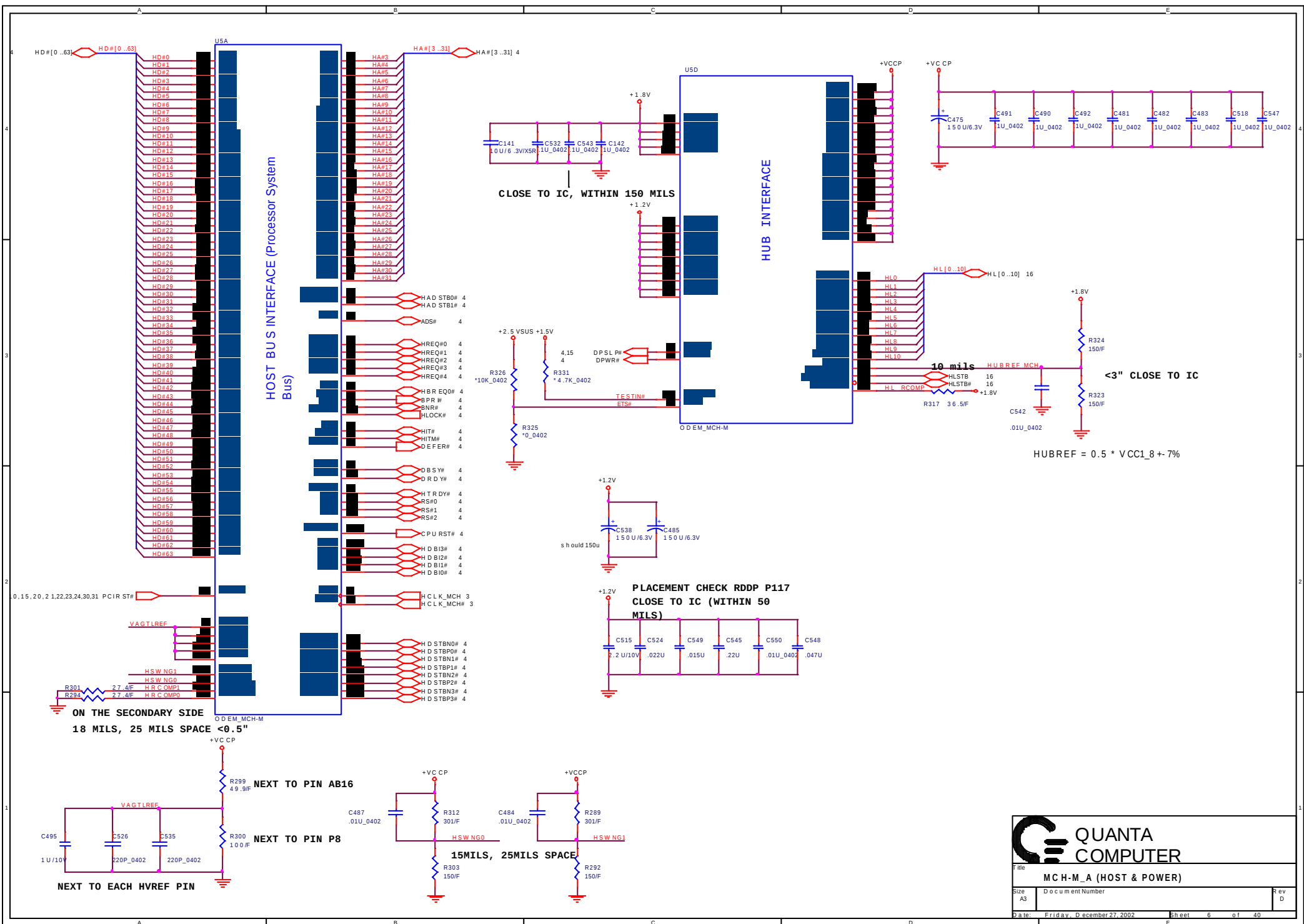
R63 *1K_0402

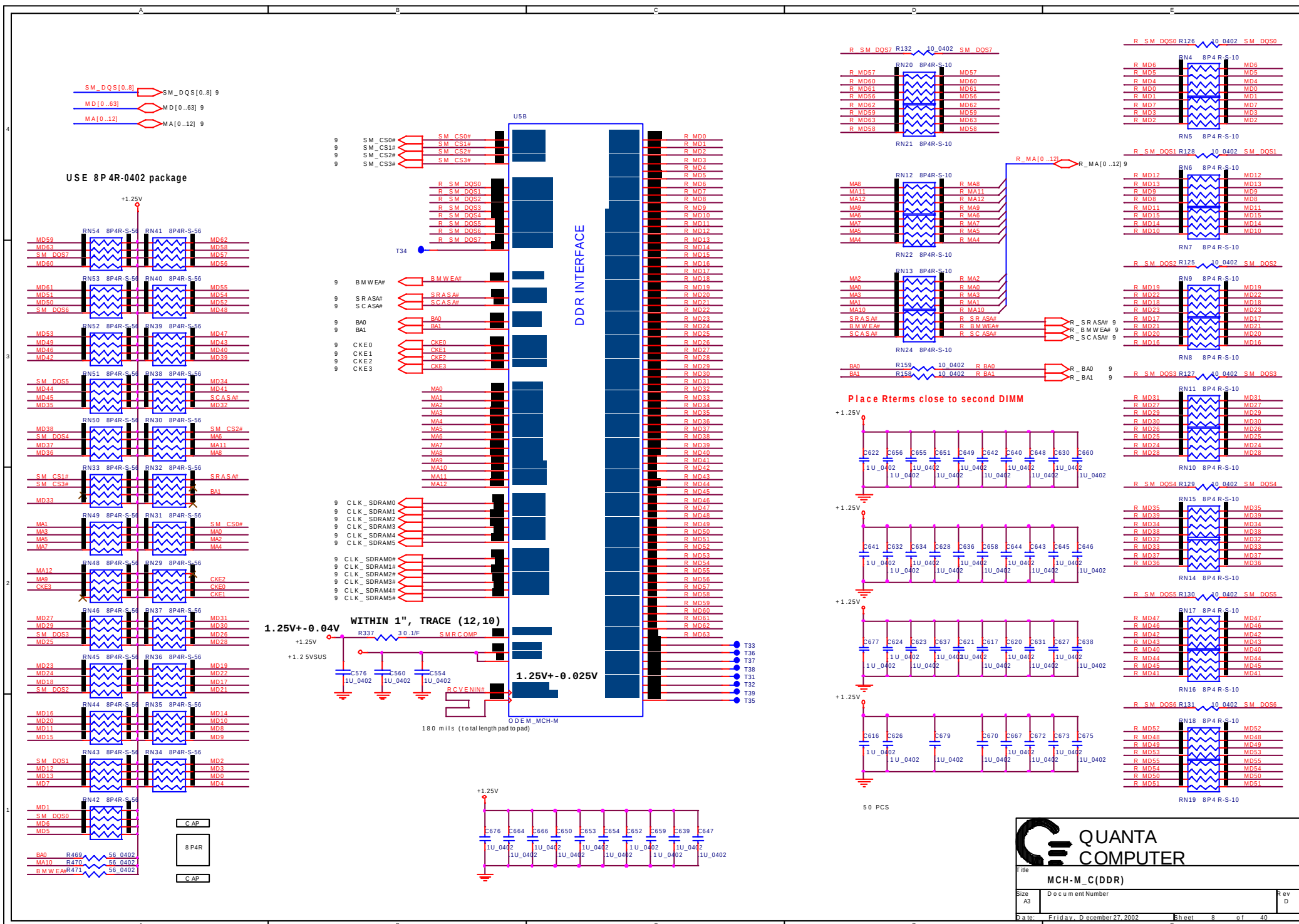
VCC_CORE 1.356V TO 0.844V
0.748V(DEEPER SLEEP)
VCCP 1.05V
VCCA 1.8V

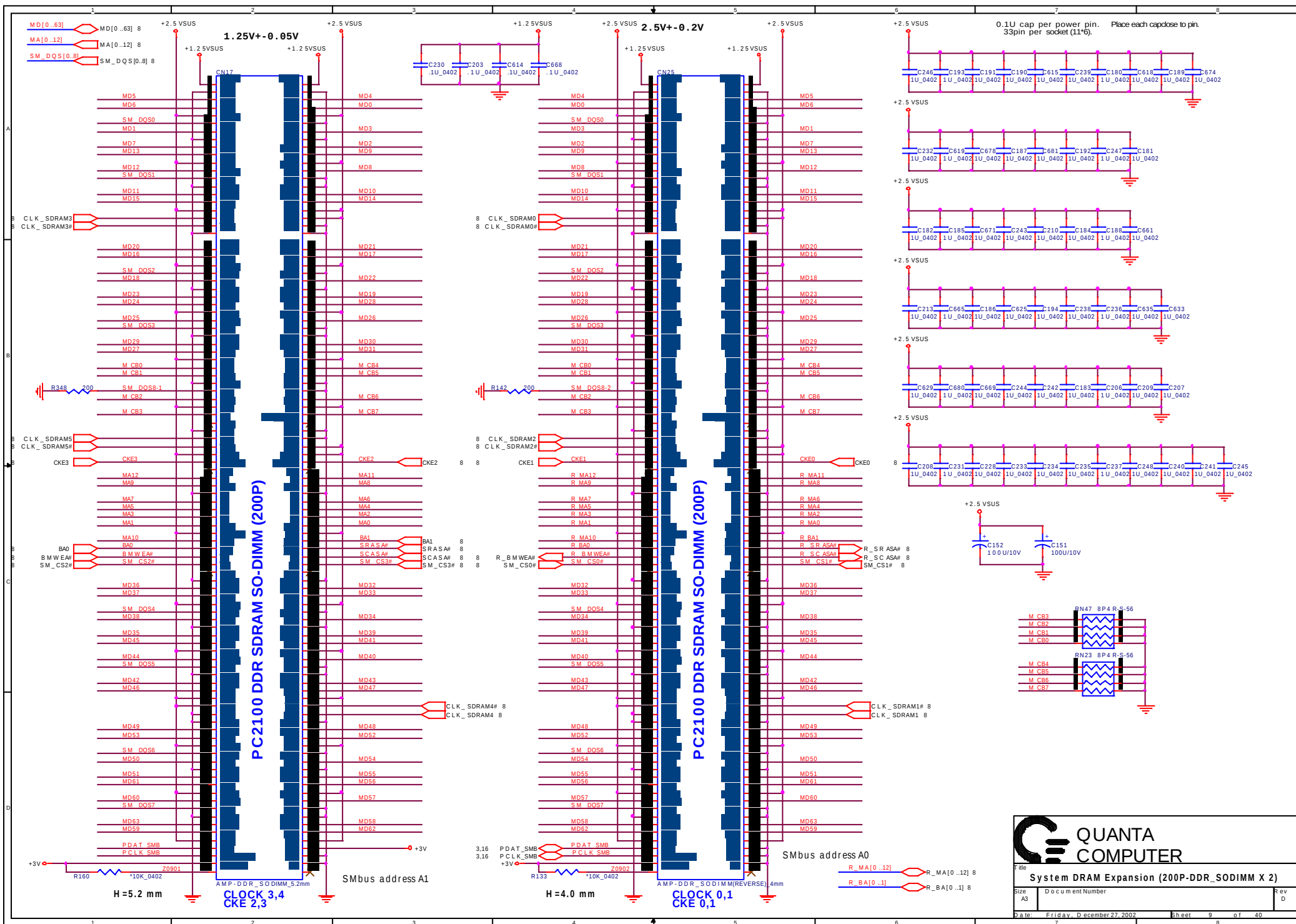


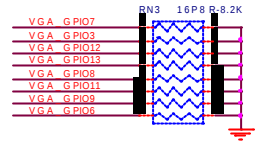
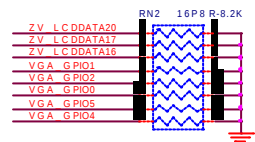
NorthWood CPU - B

File	Size	Document Number	Rev
	B		D
Date:	Friday, December 27, 2002	Sheet	5 of 40

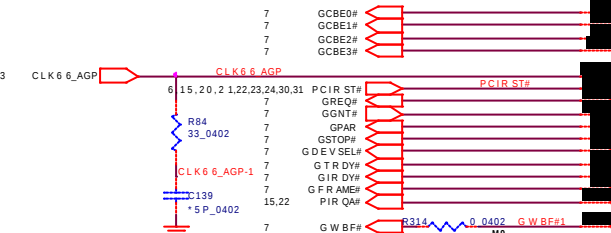




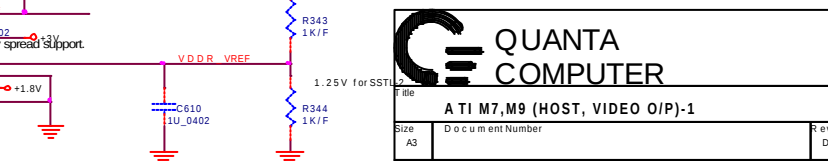
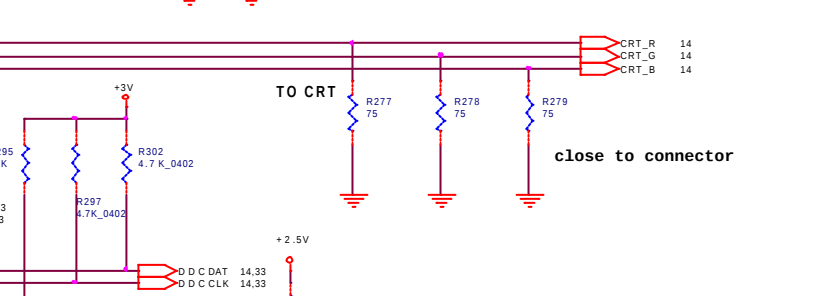
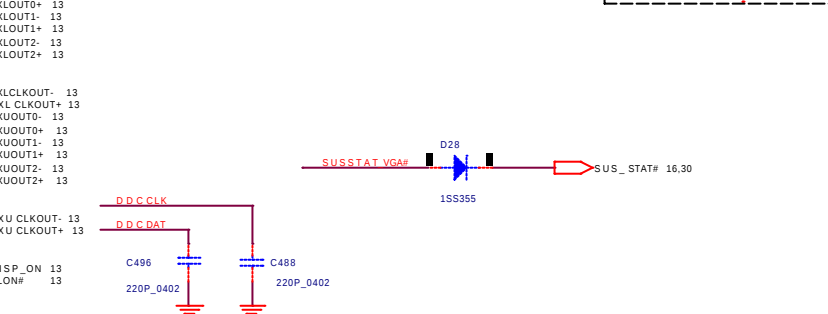
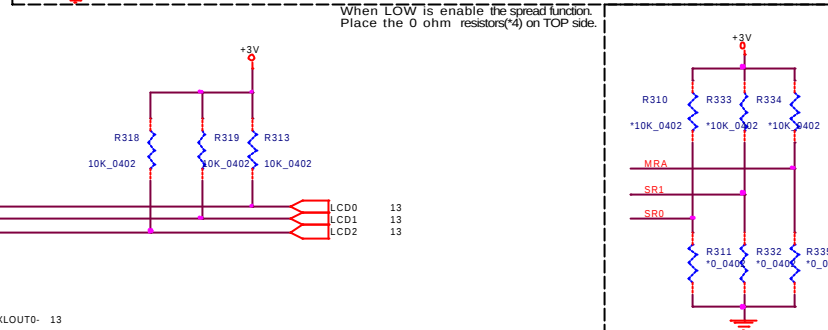
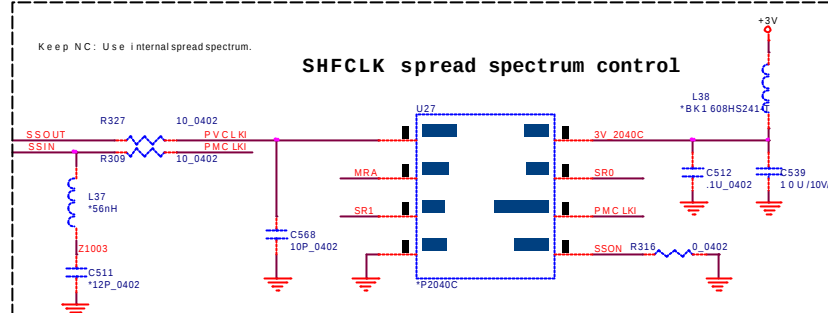
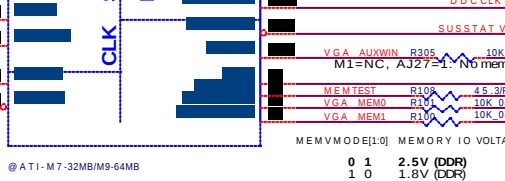
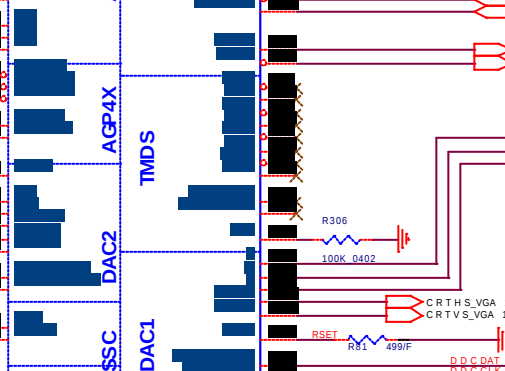
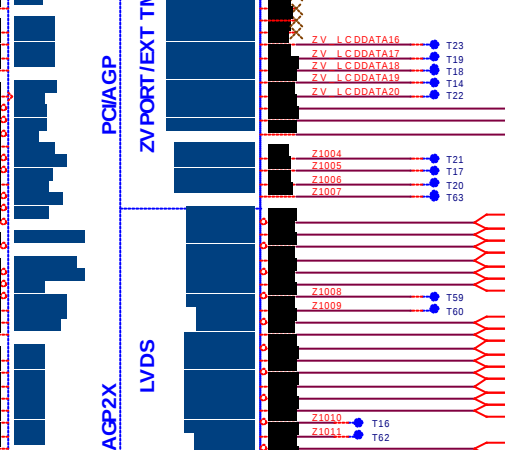
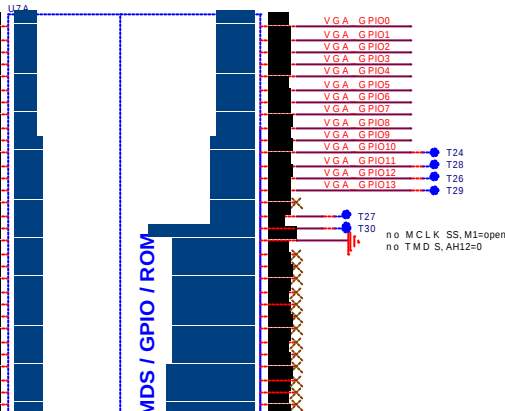
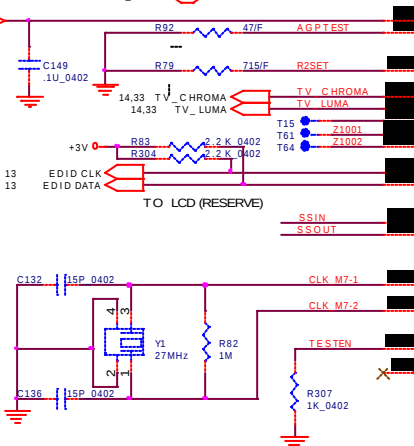
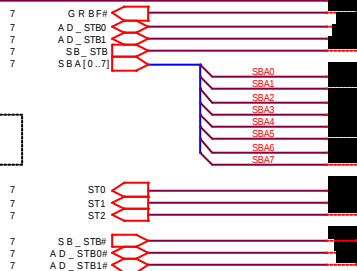




Interrupt Pin : PIRQA#



GWBG# R123--> M7 not mount



QUANTA COMPUTER

ATI M7,M9 (HOST, VIDEO O/P)-1

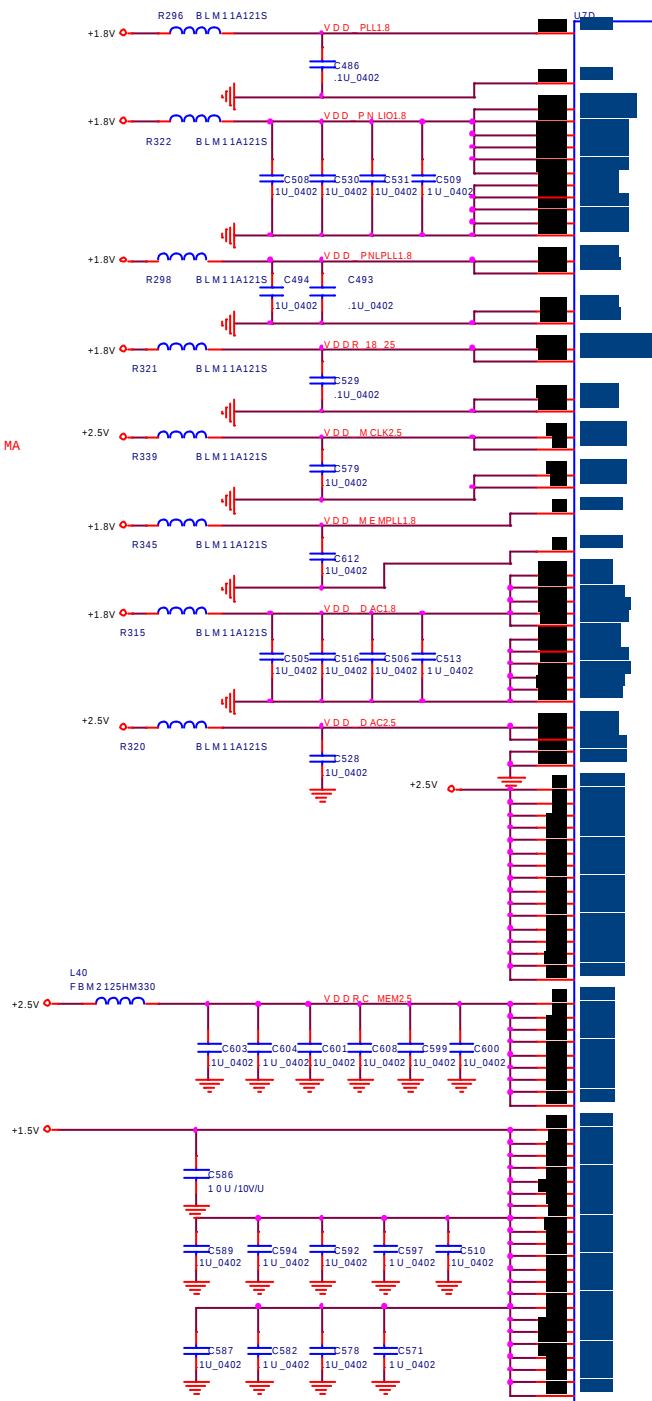
Size A3 Document Number Rev D

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@ ATI-M7-32MB/M9-64MB

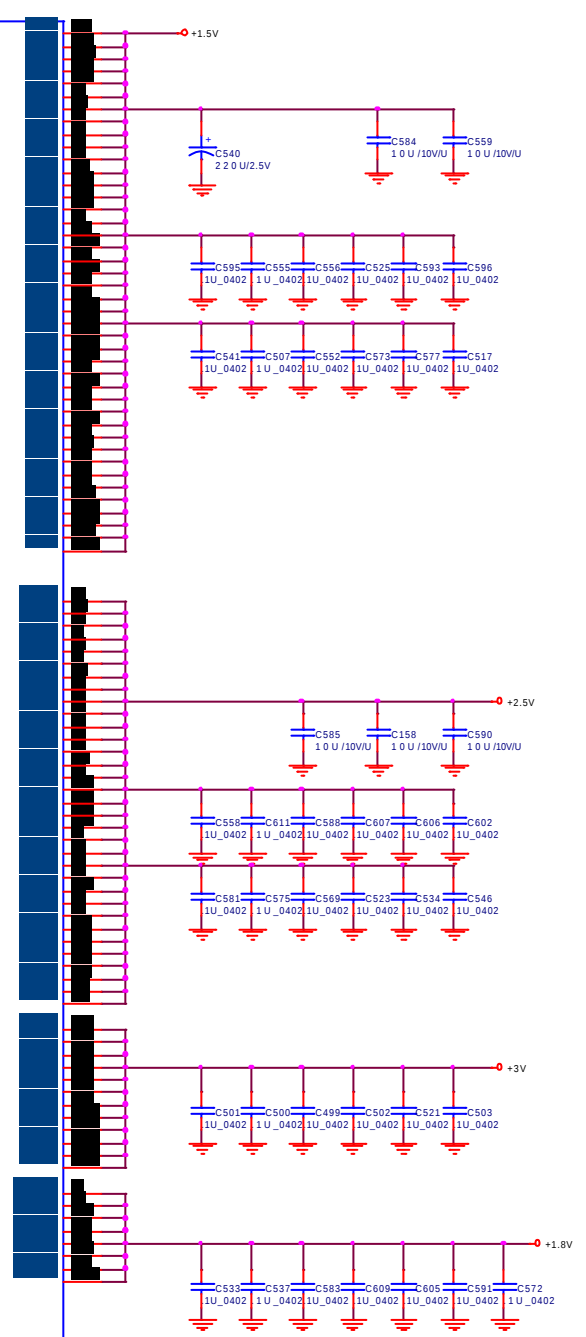
MEMMODE[L:0] MEMORY IO VOLTAGE

0	1	2.5V (DDR)
1	0	1.8V (DDR)
1	1	3.3V (SDR)



VDDR 5 MA

CORE & I/O POWER

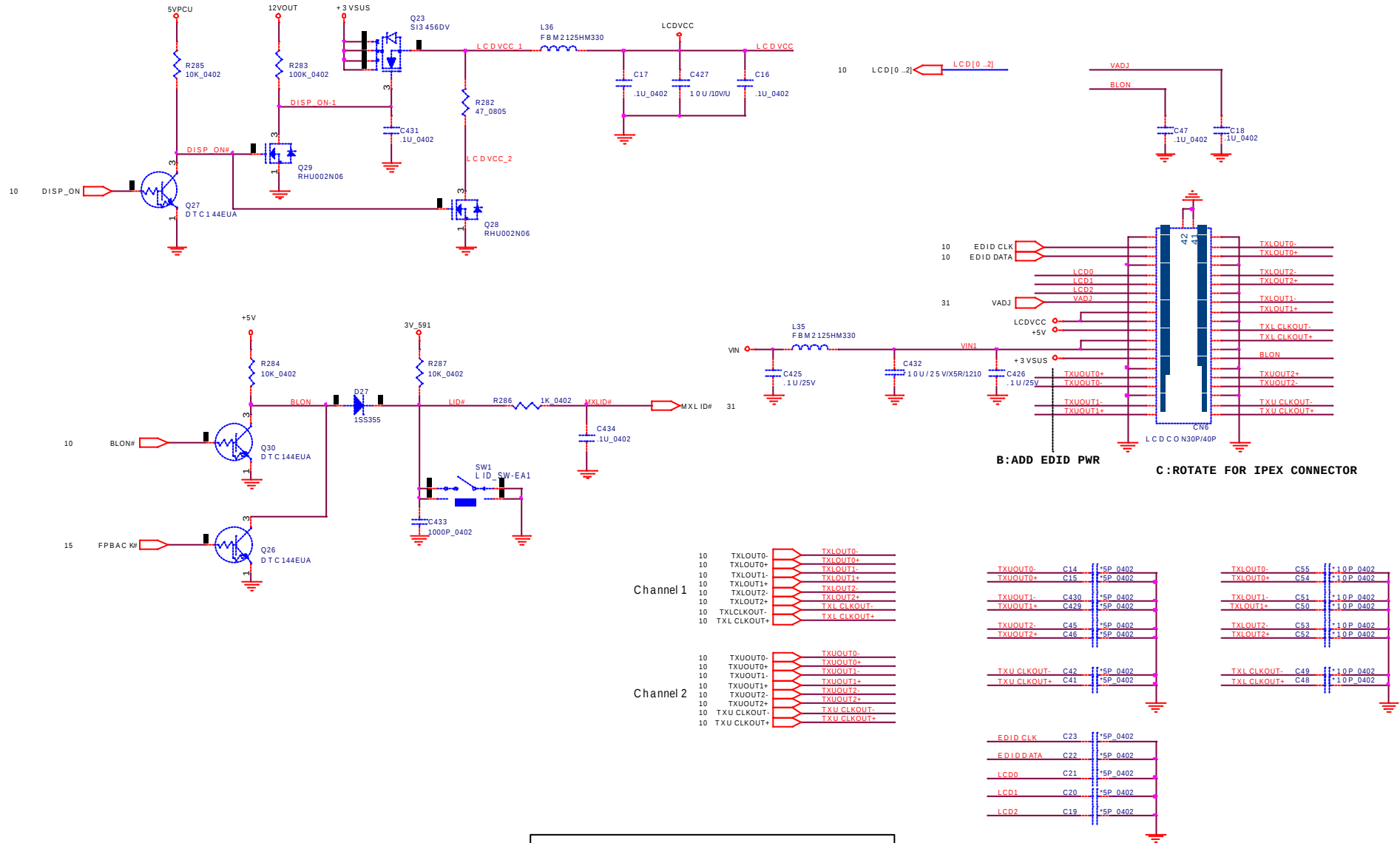


@ AT1-M7-32MB/M9-64MB

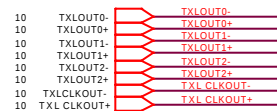


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COMPUTER

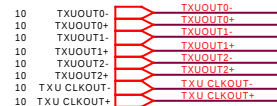
File AT1 M7, M9		
Size A3	Document Number	Rev D
Date Friday, December 27, 2002	Sheet 12	of 40



Channel 1



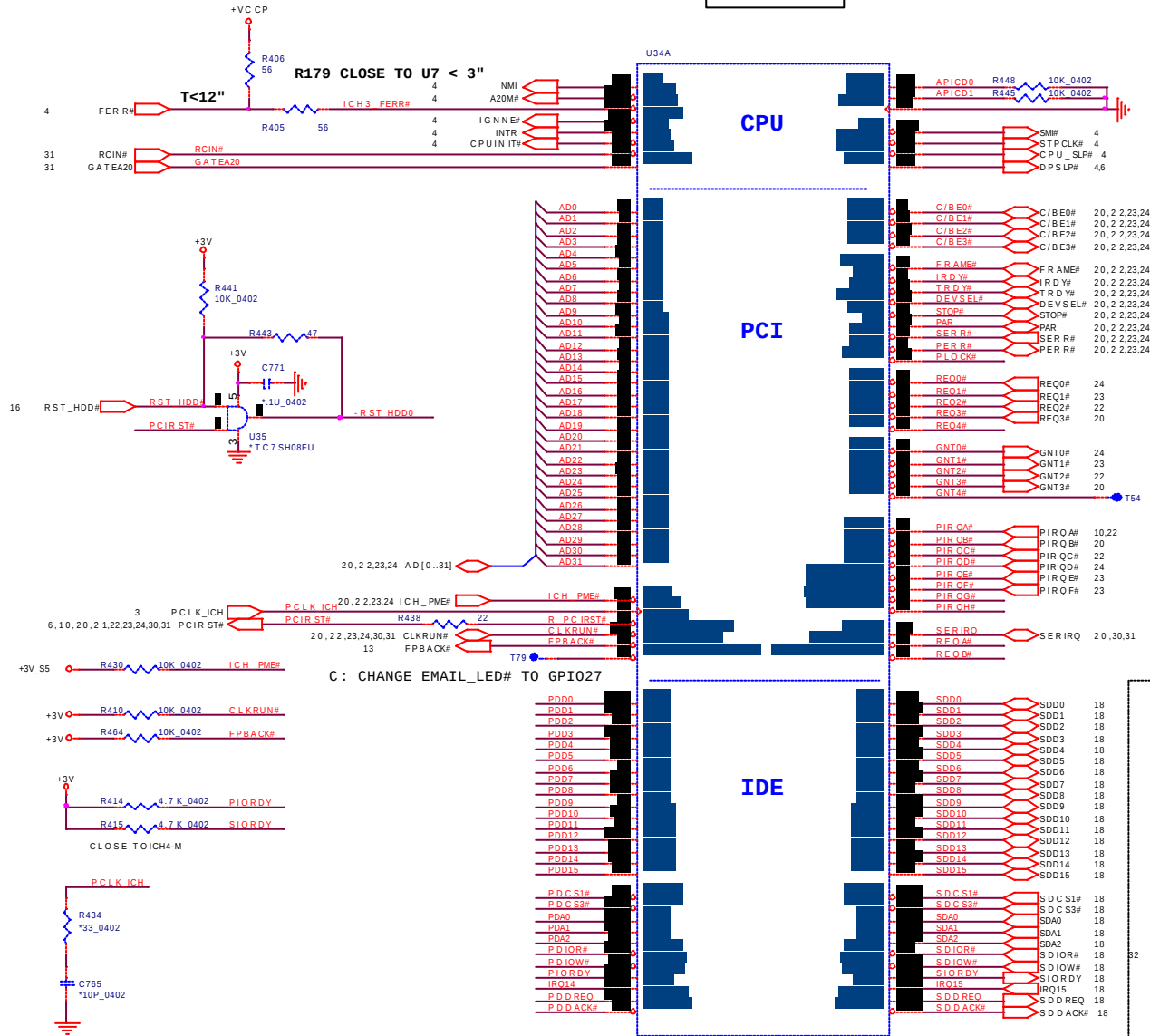
Channel 2



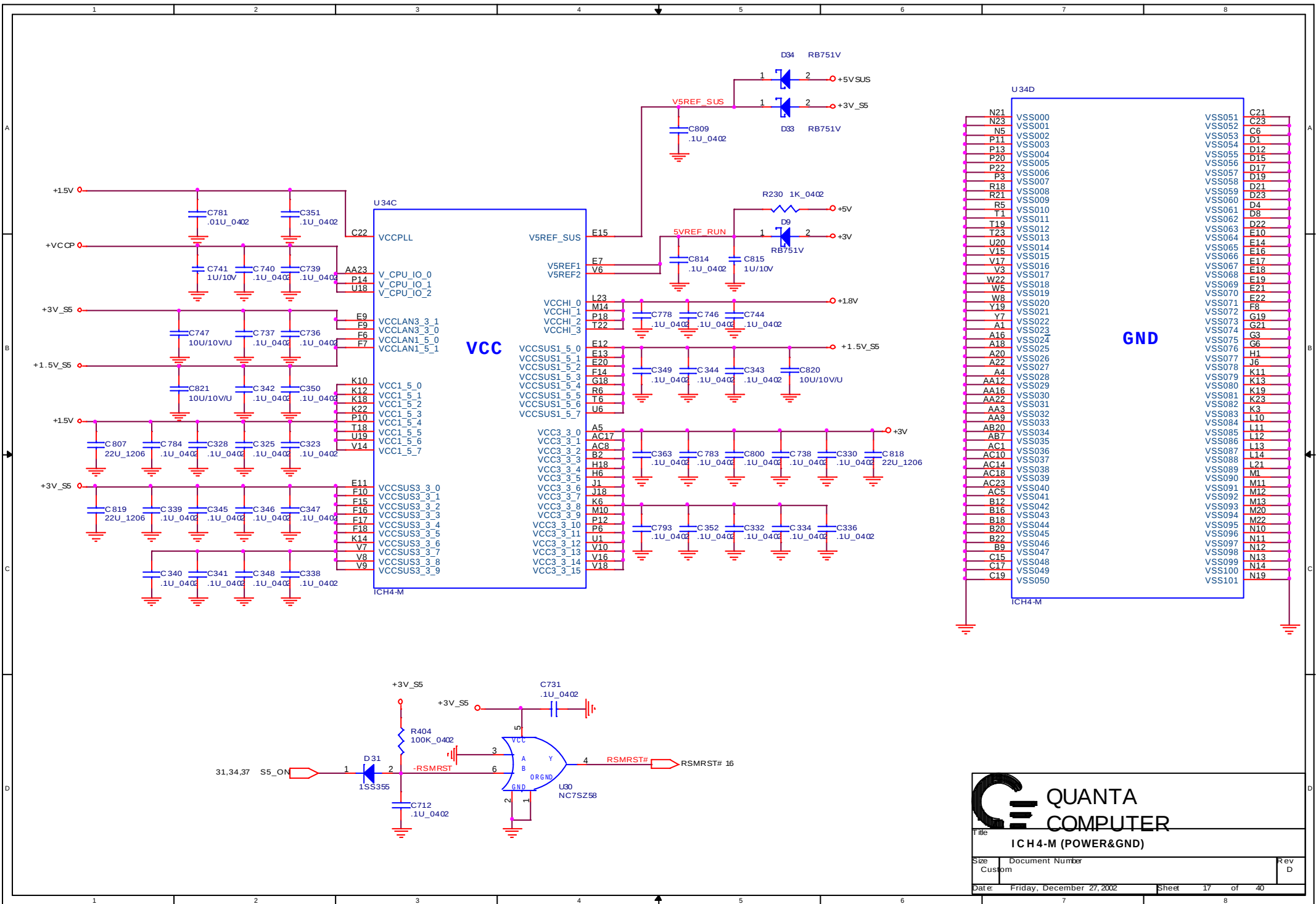
ID1	QDI	14.1" XGA	QD141X1H12	LCD2	LCD1	LCD0
ID2	LG	14.1" XGA	LP141X13	0	1	0
ID3	LG	15" XGA	LP150X05-A2C1	0	1	1
ID4	OPT	15" XGA	CLAA150XH01	1	0	0
ID5	OPT	15" SXGA+	CLAA150PA01	1	0	1
ID6	HannStar	15" SXGA+	HSD150PK12	1	1	0
ID7				1	1	1

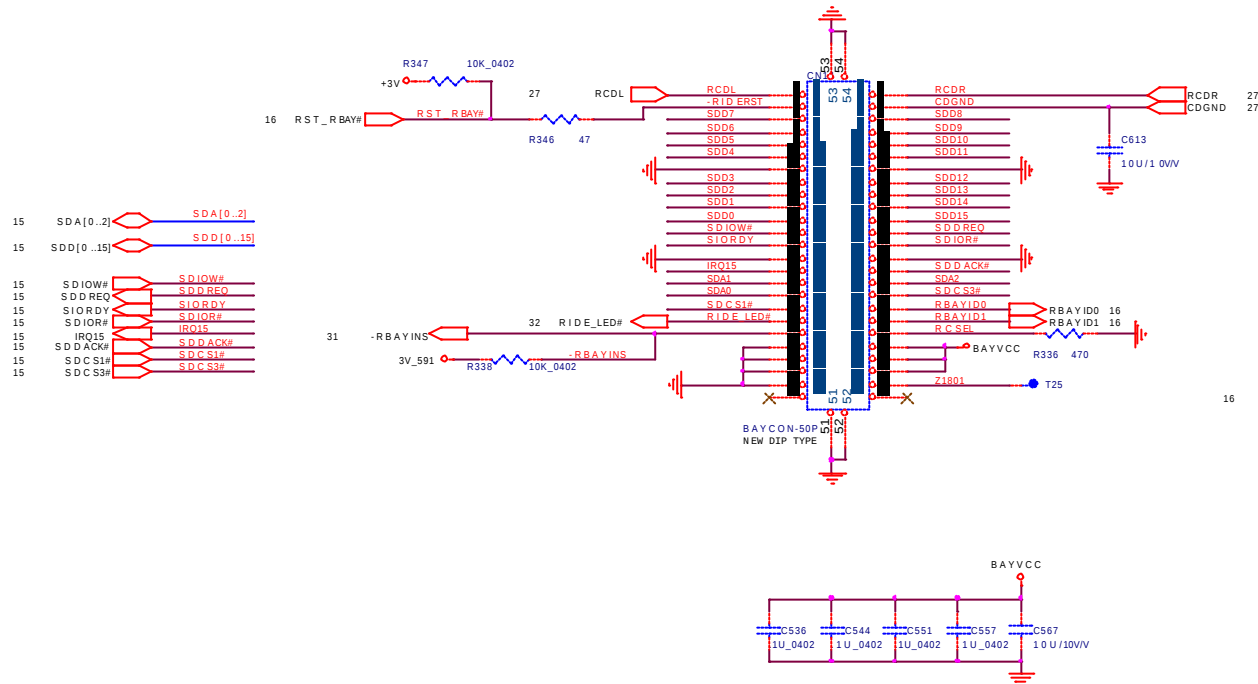


ICH HUB

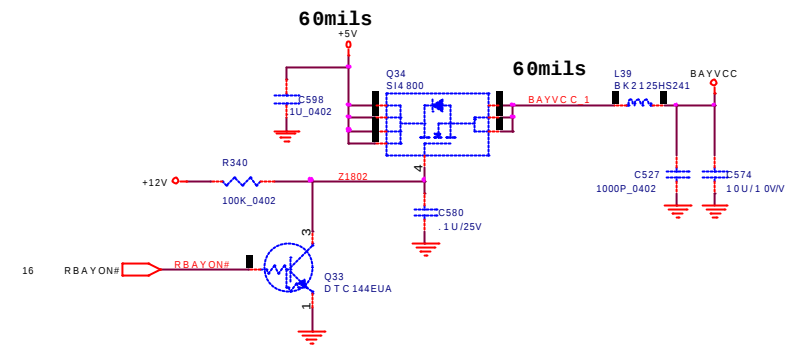




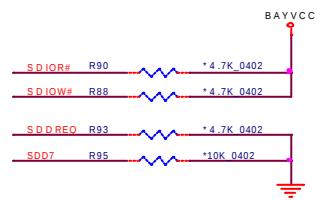




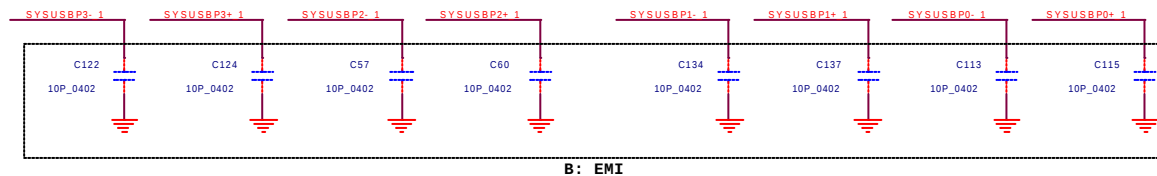
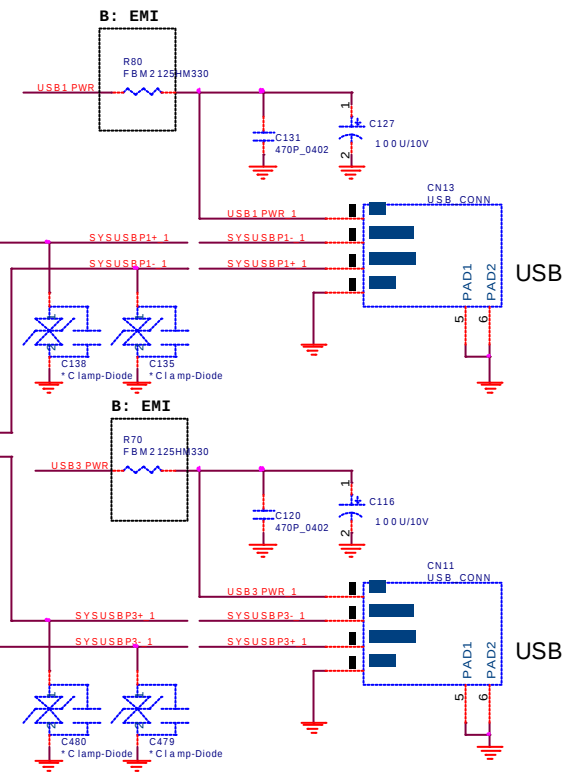
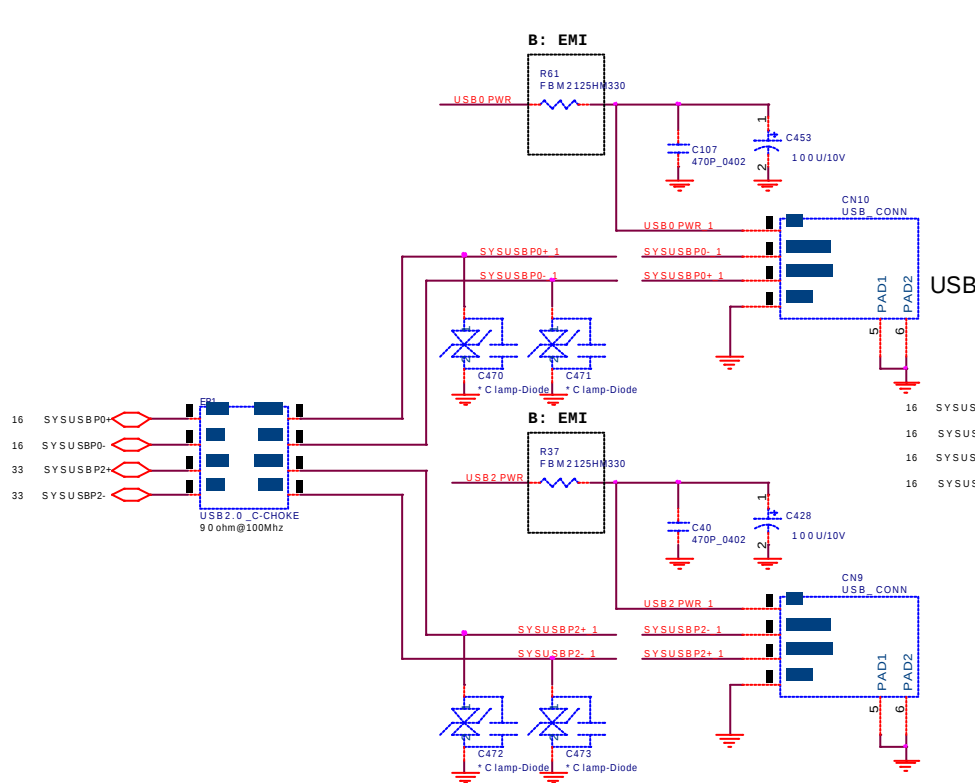
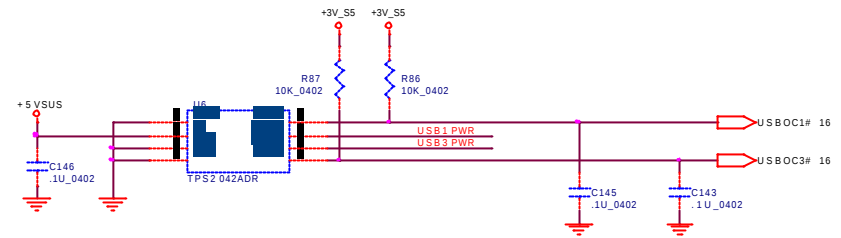
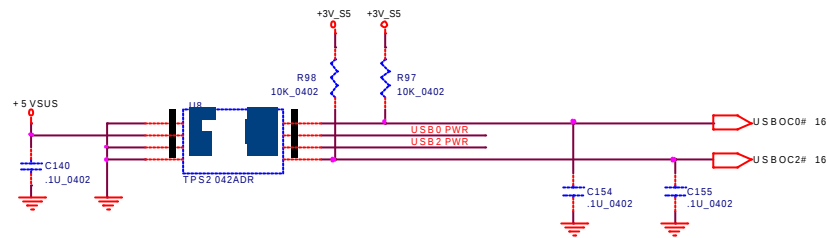
BAY POWER CONTROL & RESET



MEDIA BAY(HDD, CD, DVD, FDD)



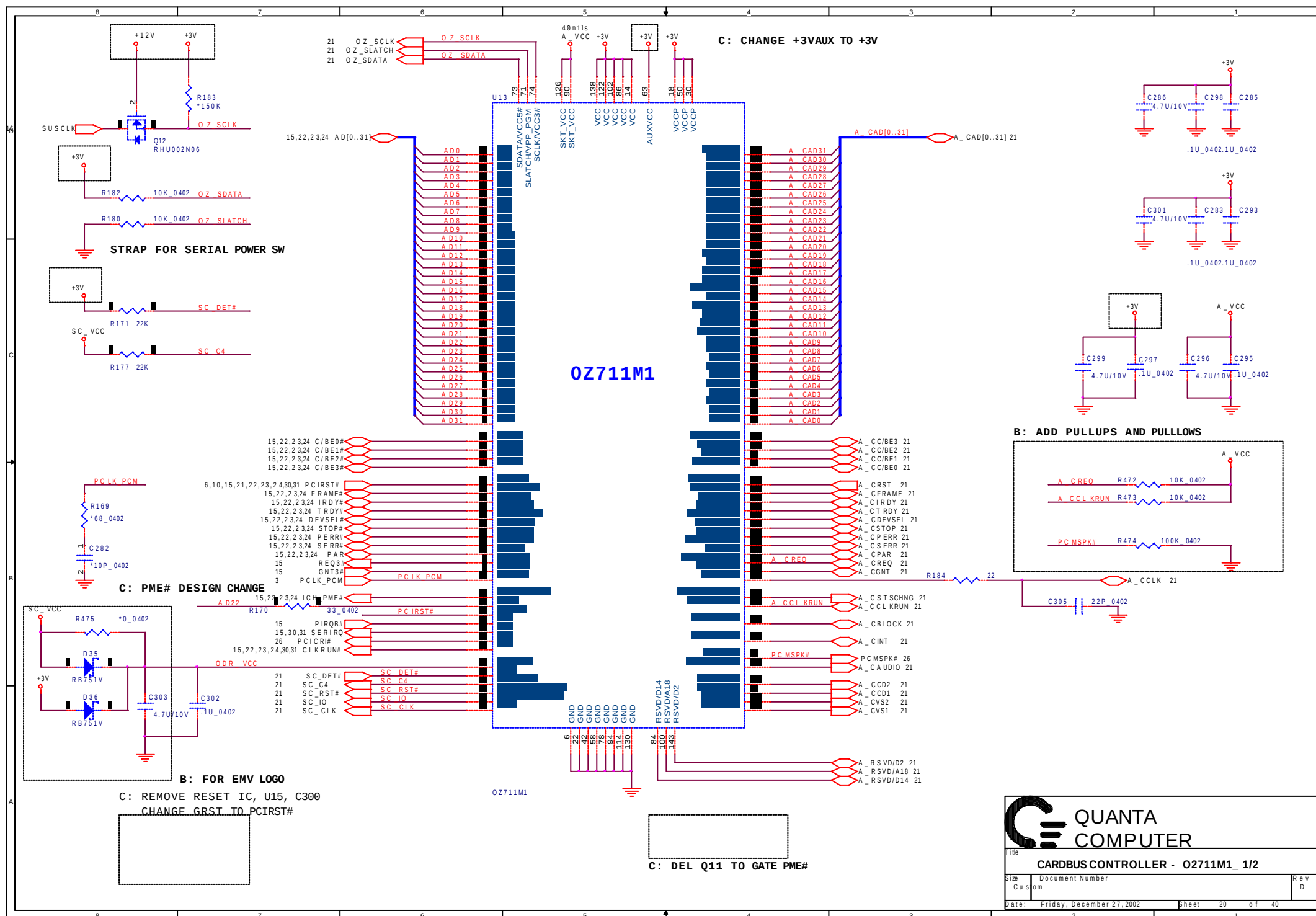
BAYID STATUS		
RBAYID0	RBAYID1	STATUS
0	0	FDD
0	1	HDD
1	0	CD/DVD



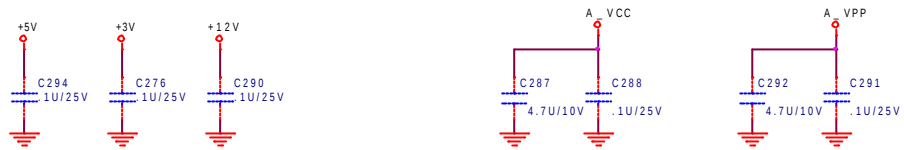
**QUANTA
COMPUTER**

USB & BOARD CON

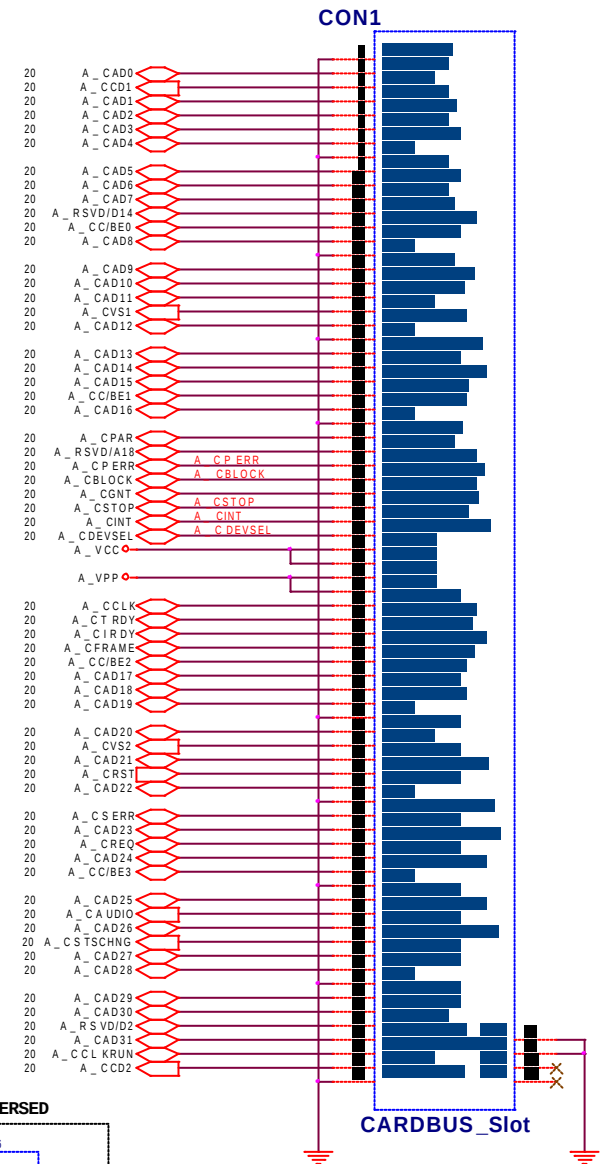
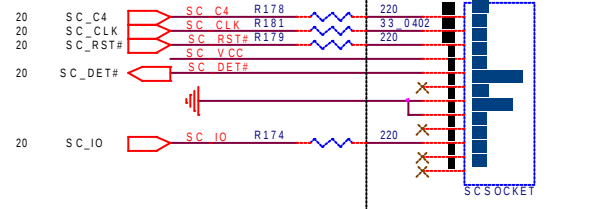
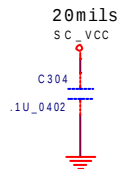
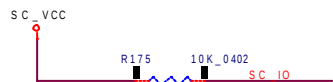
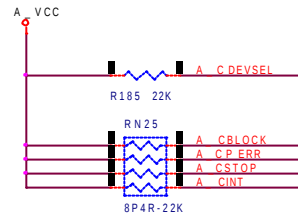
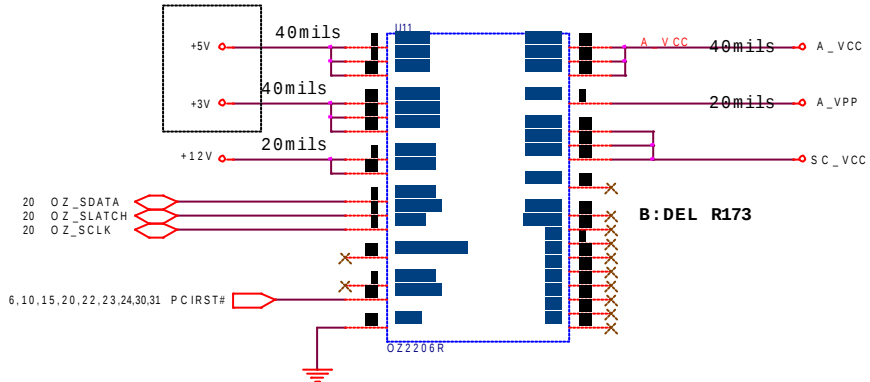
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CARDBUS Slot

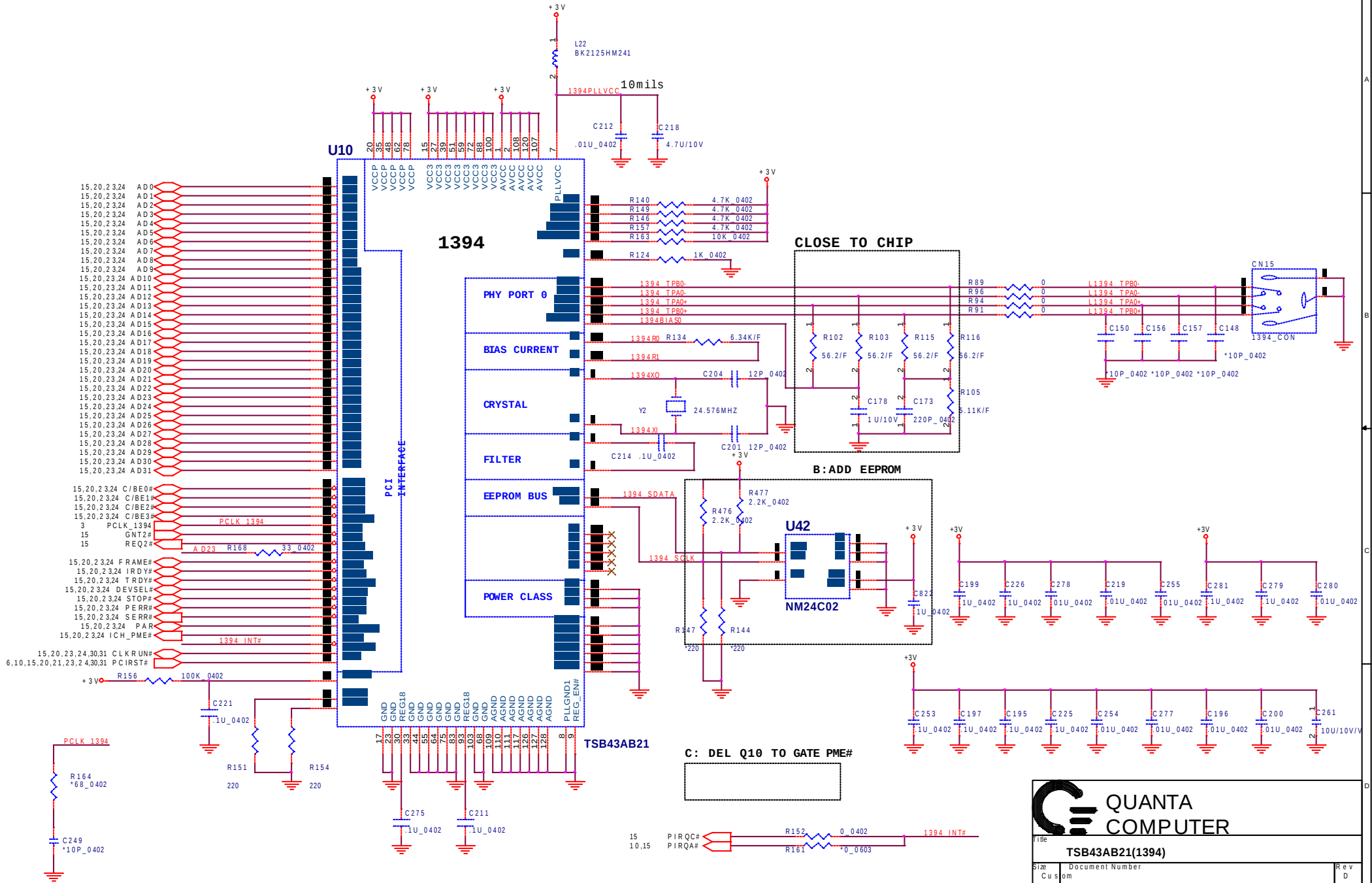


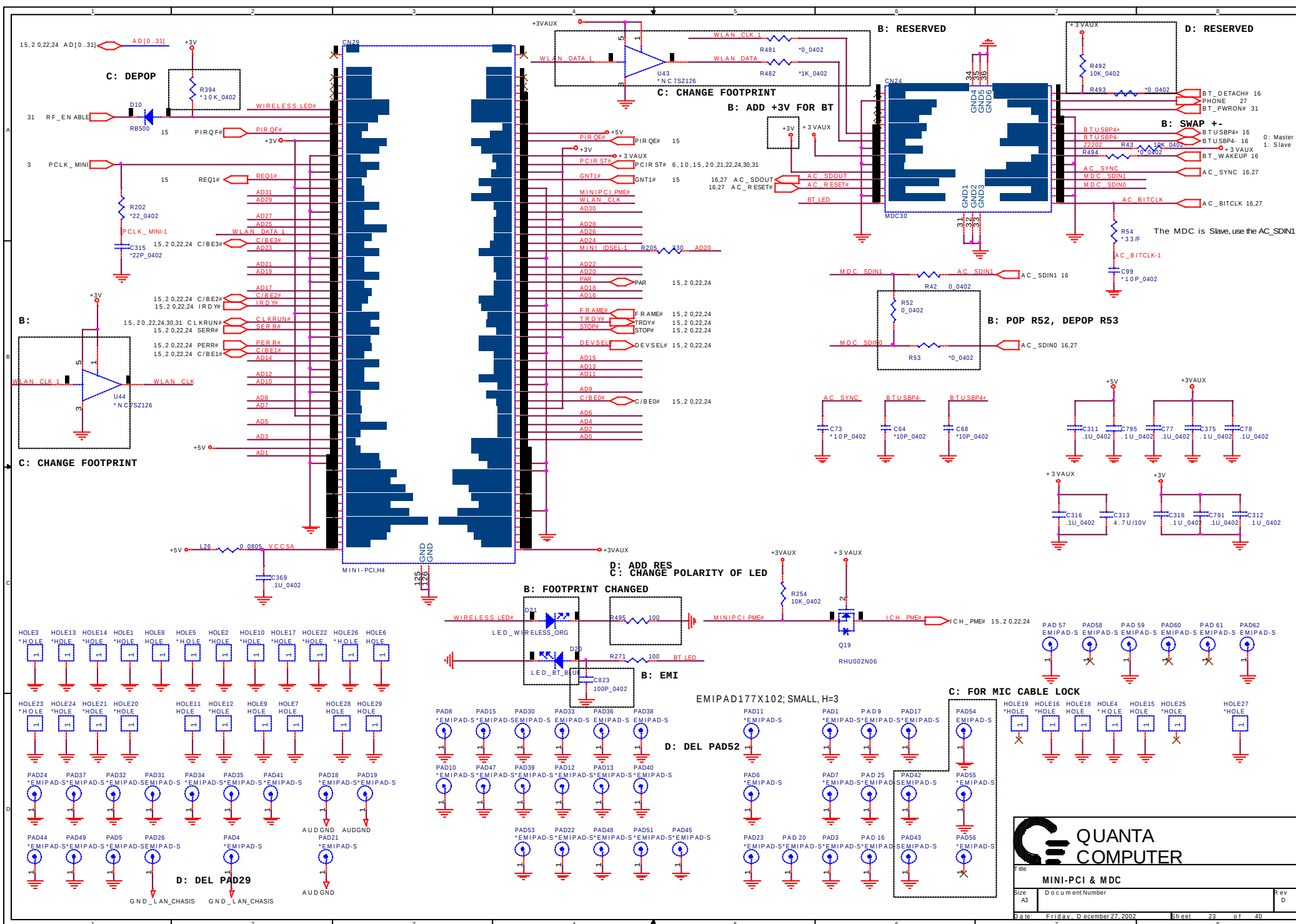
C: CHANGE FROM +5VSUS AND +3VAUX

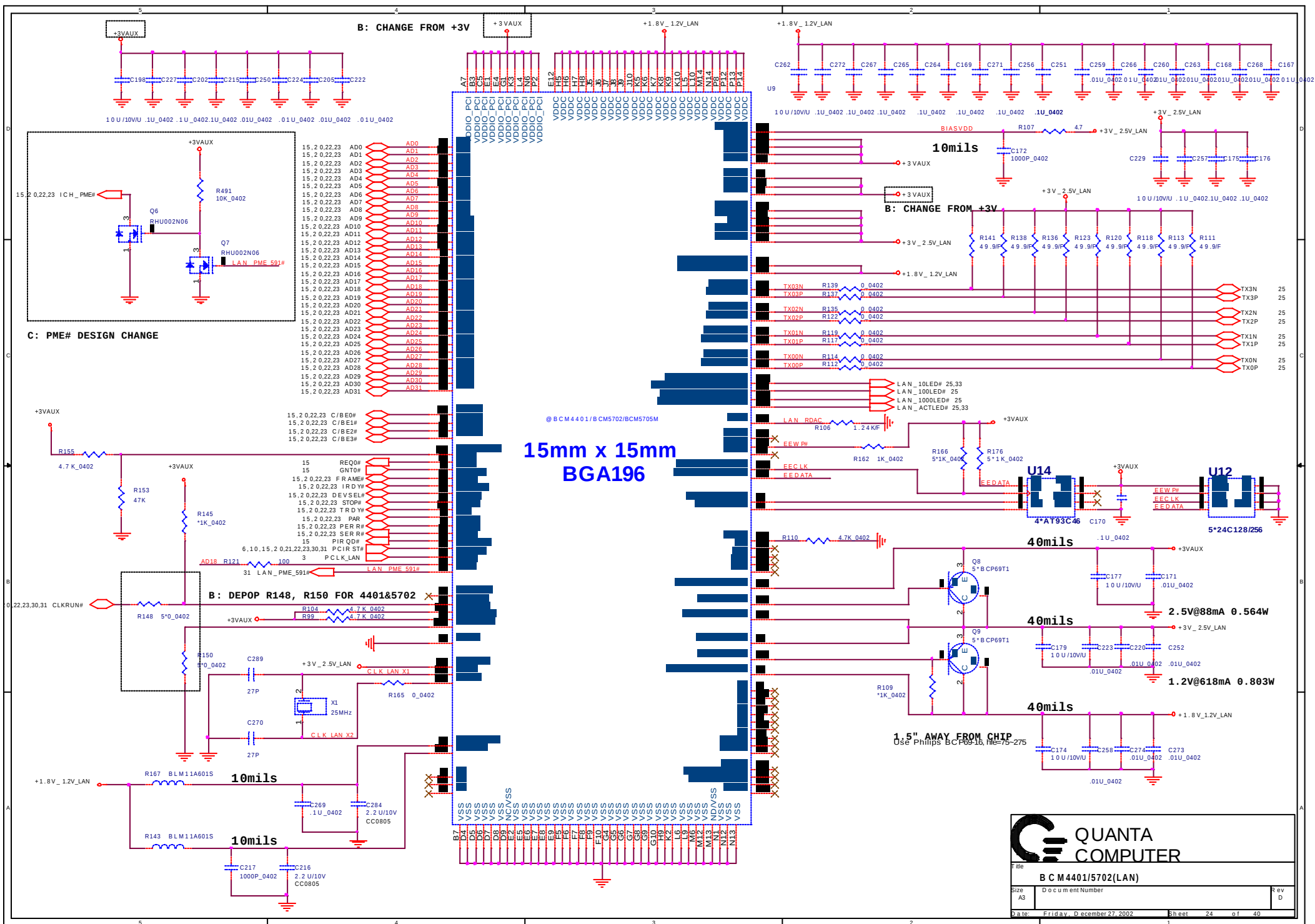


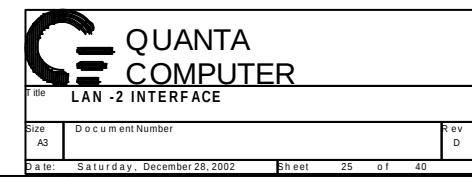
Title		CARDBUS SLOT	
Size	Document Number		
Cu	om		
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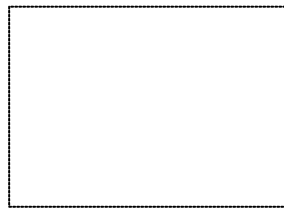
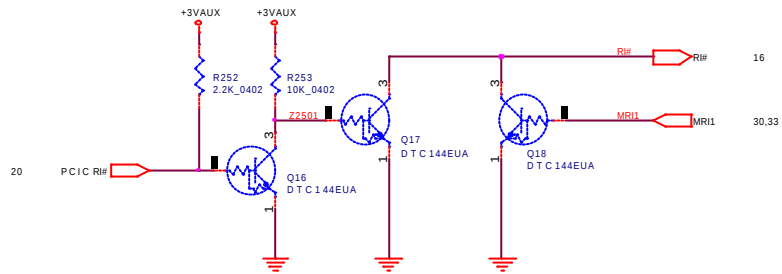
IEEE 1394 CONTROLLER - TI_TSB43AB21



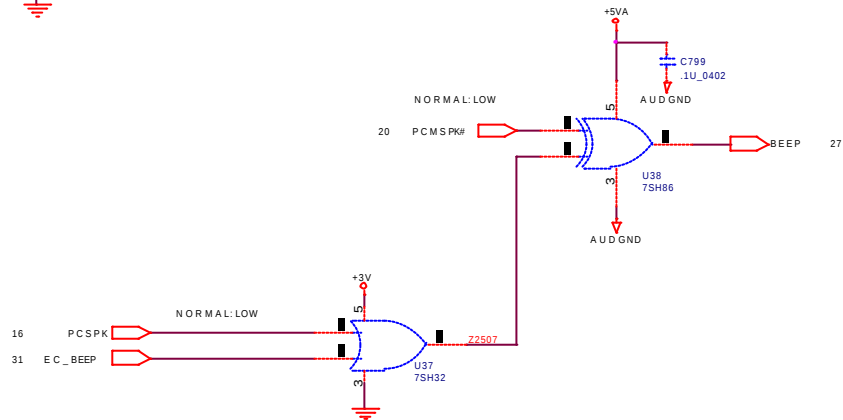


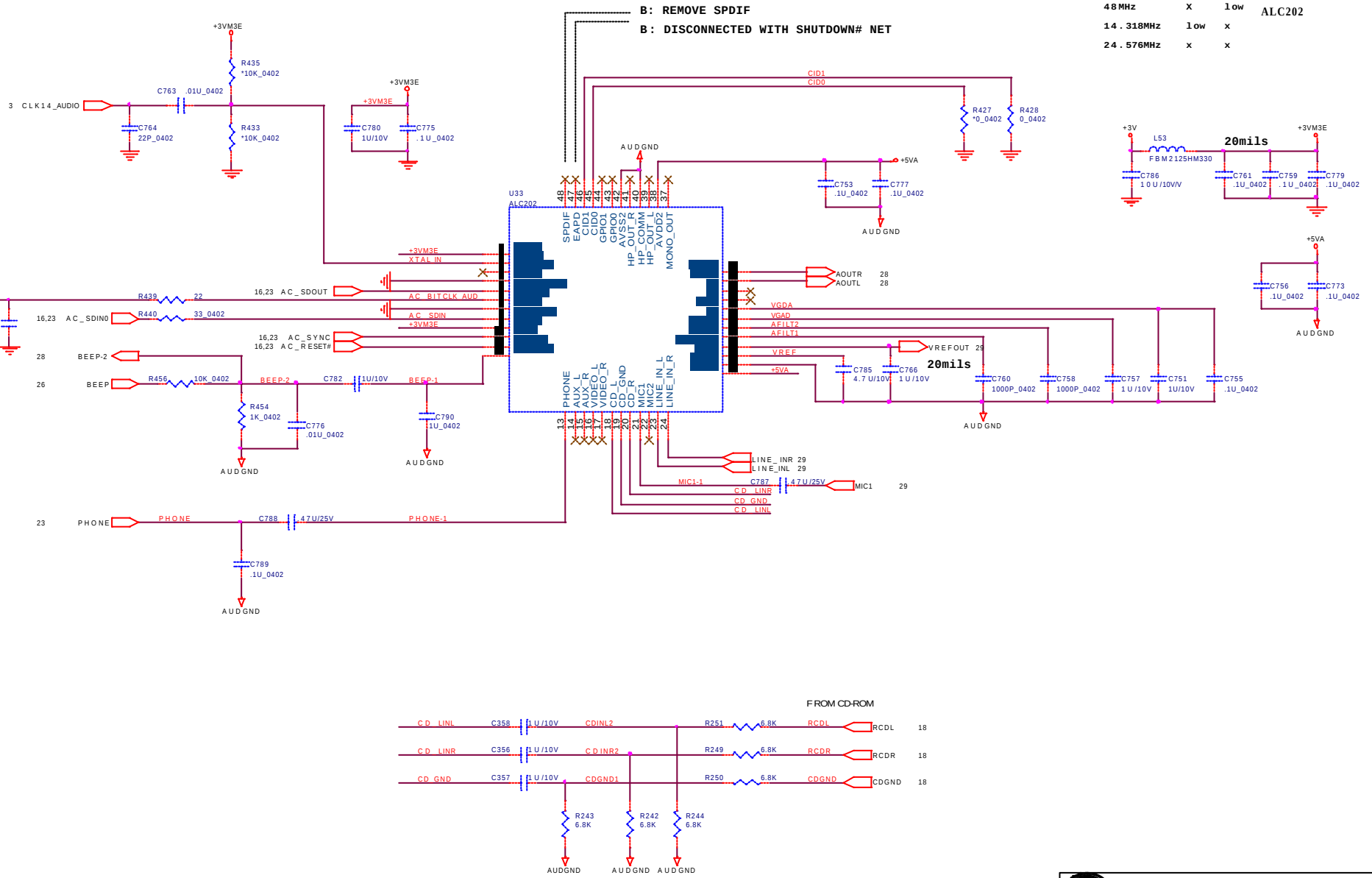






B: REMOVE BEEP CIRCUITS





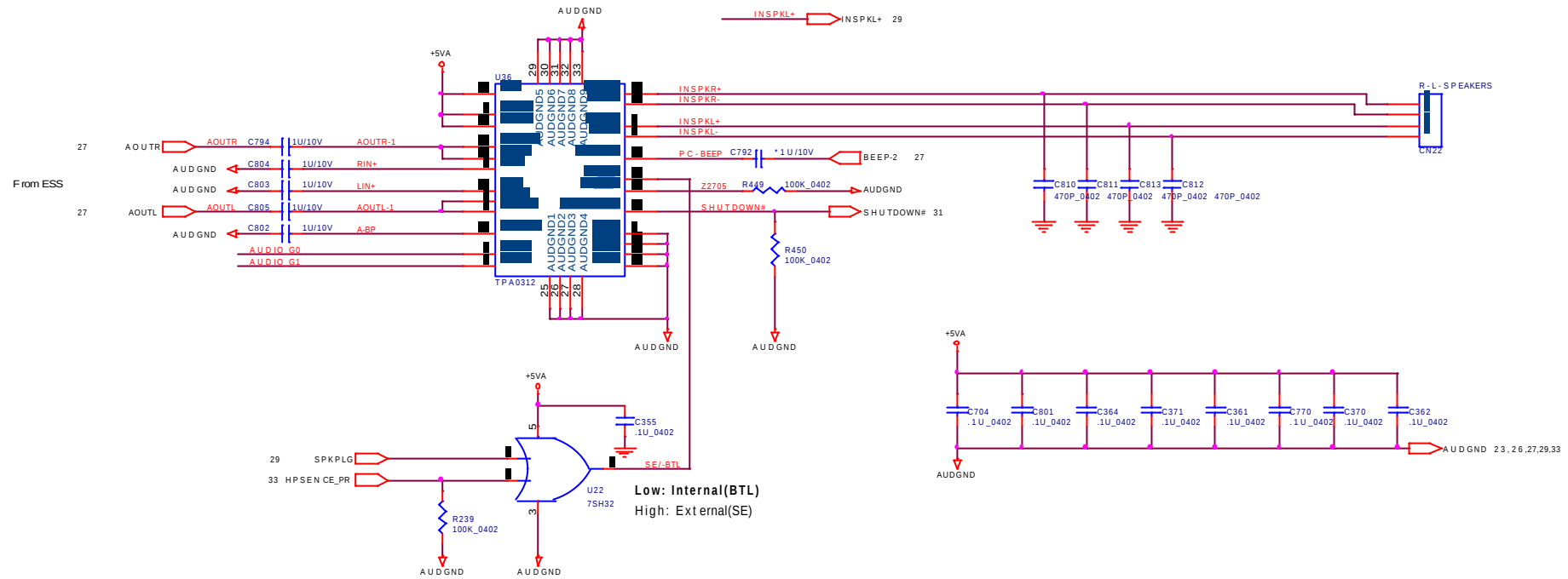
External Clock	ID1	ID0	
48MHz	X	low	ALC202
14.318MHz	low	x	
24.576MHz	x	x	



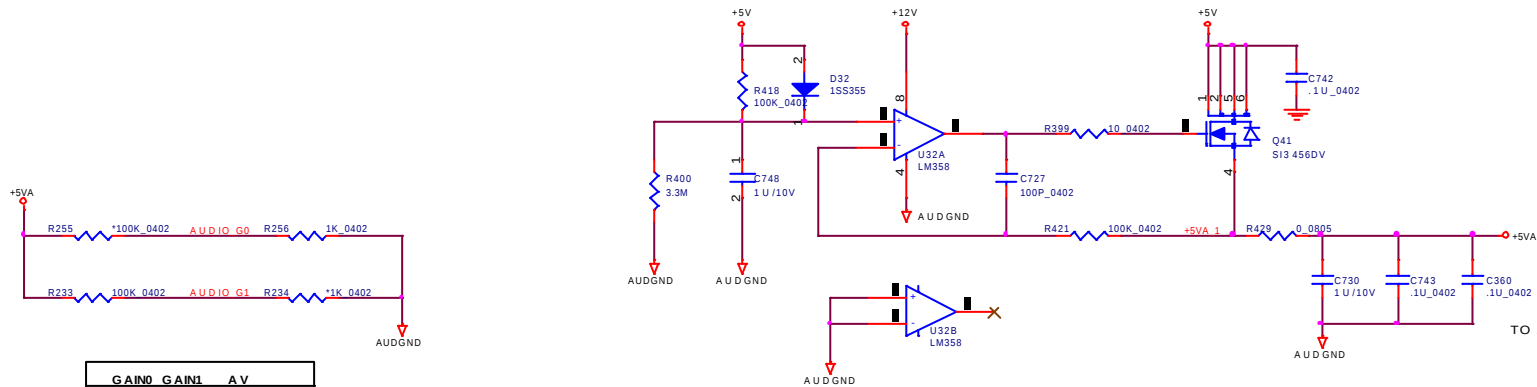
QUANTA
COMPUTER

A AUDIO CONTROLLER[ESS1988]		
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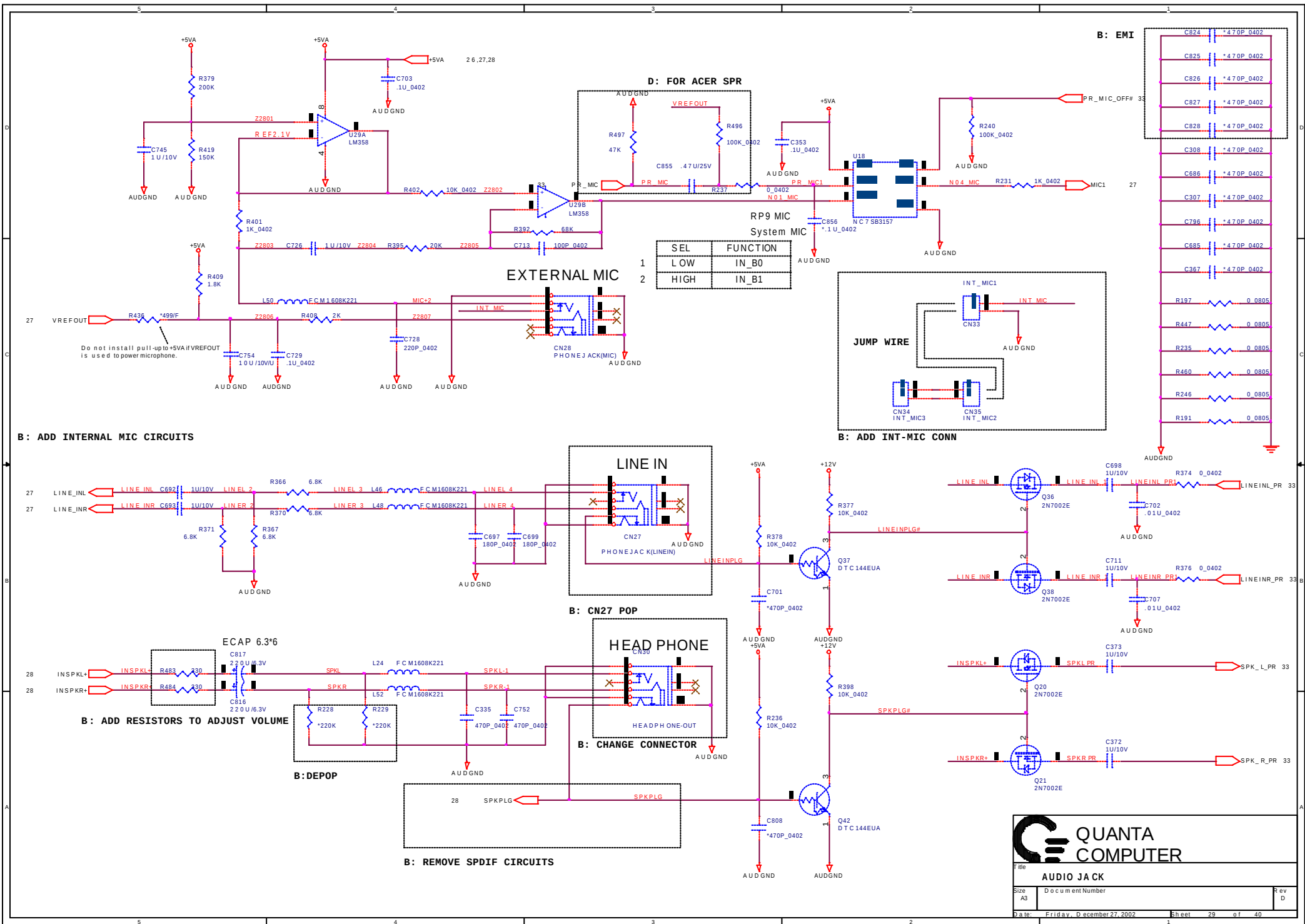
Audio Amplifier



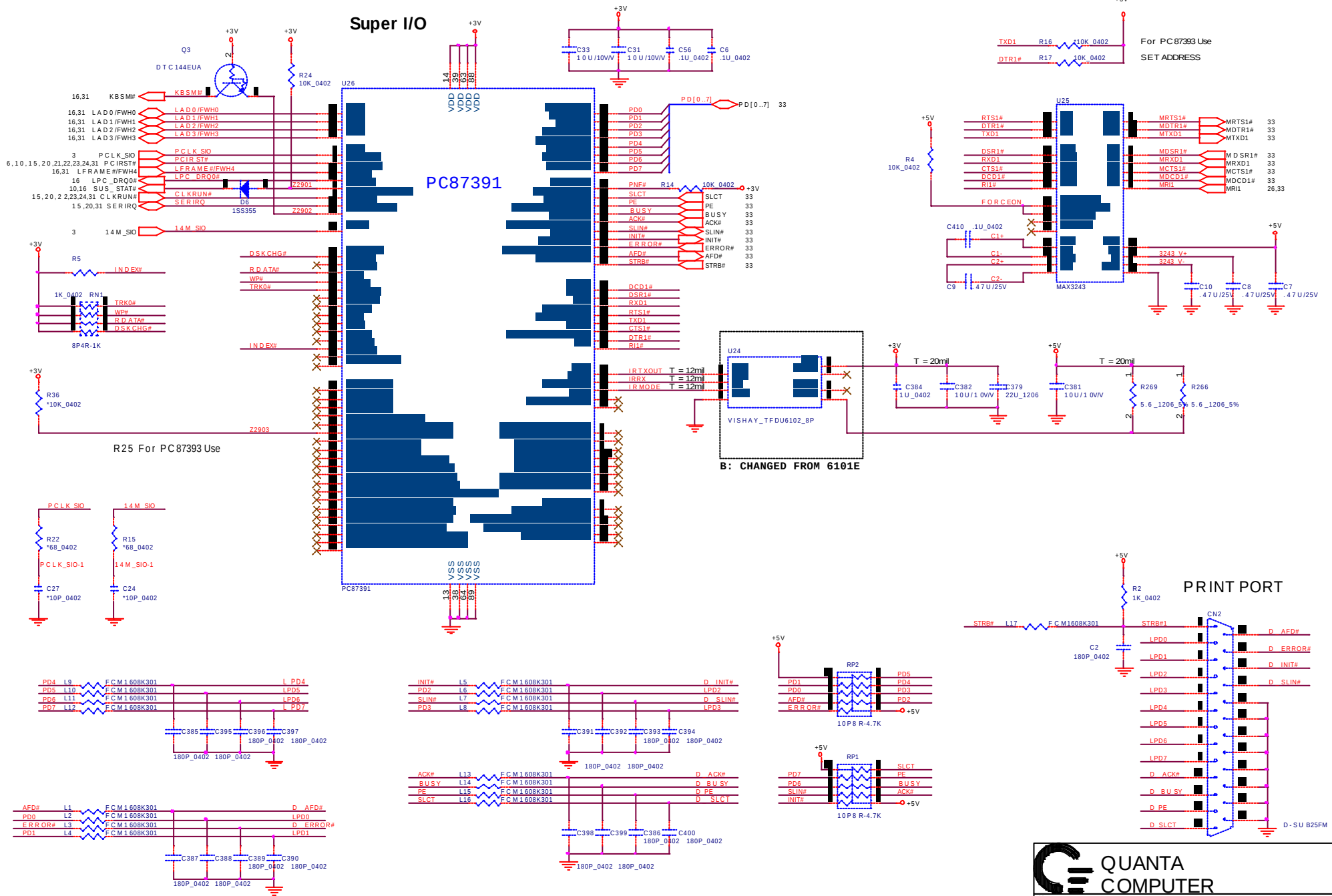
Low: Internal(BTL)
High: External(SE)



GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



Super I/O

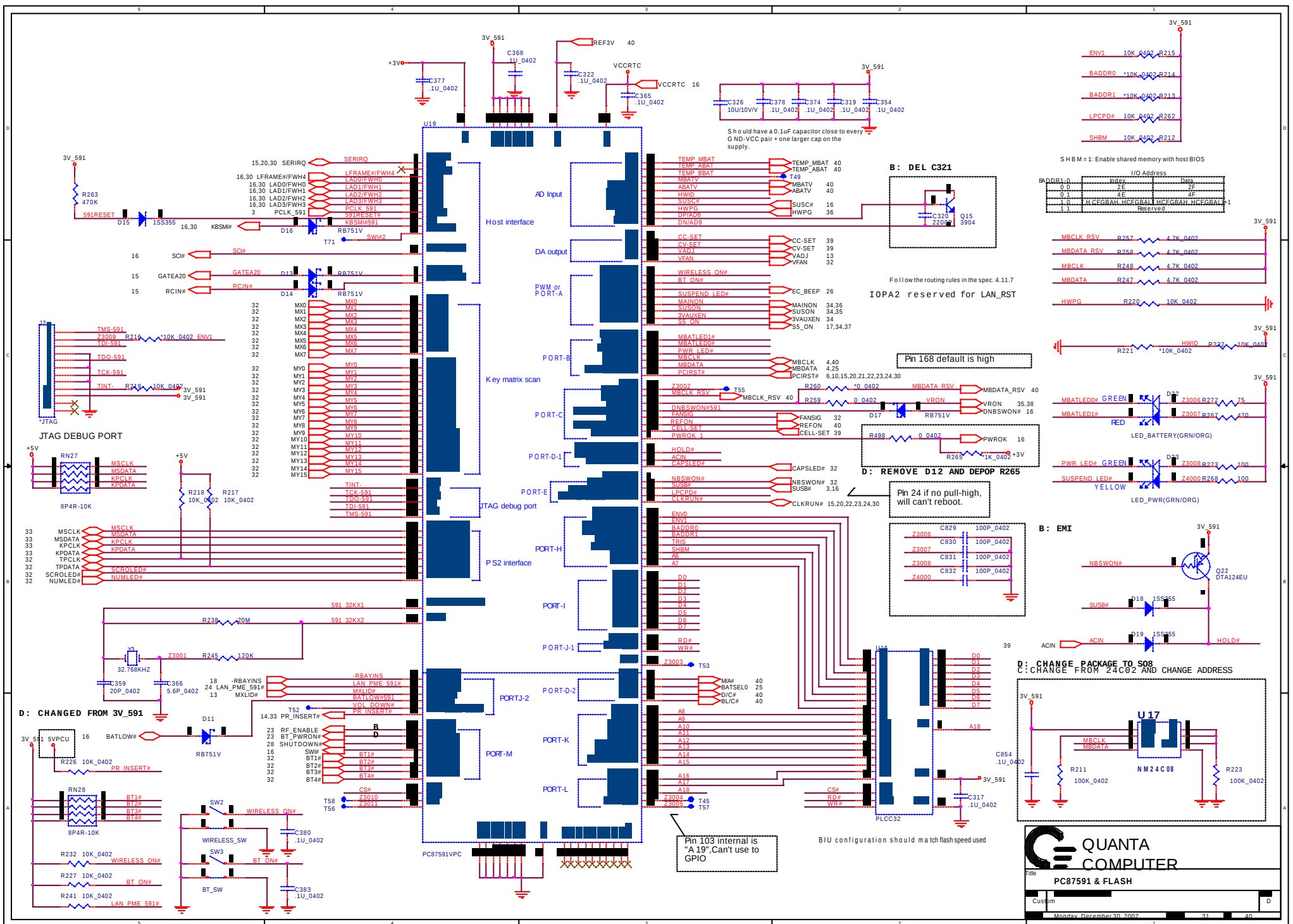


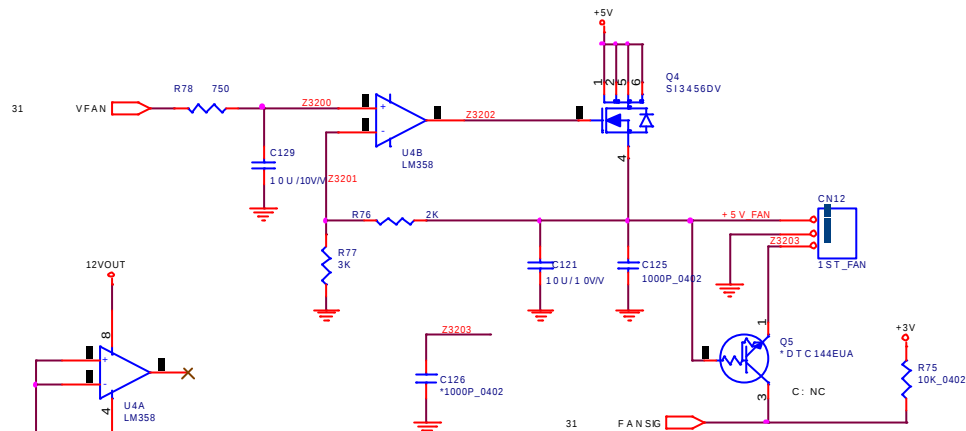


QUANTA COMPUTER

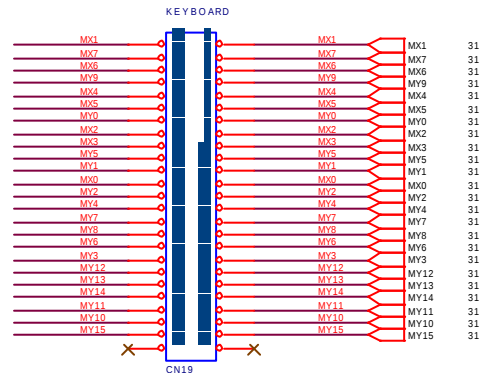
SUPER I/O NS37391

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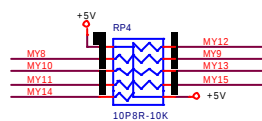
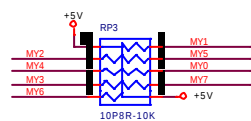
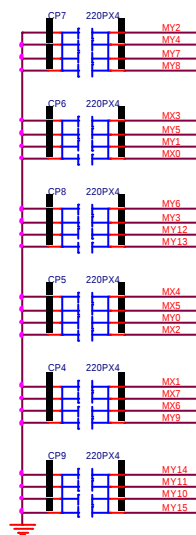




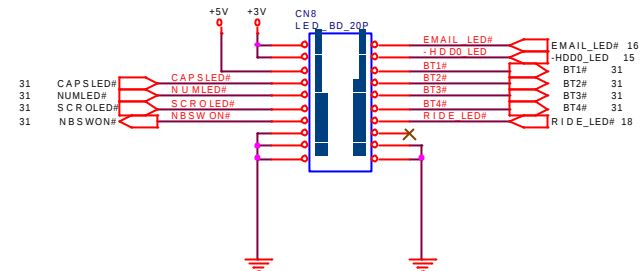
1st FAN OUT CONNECTOR



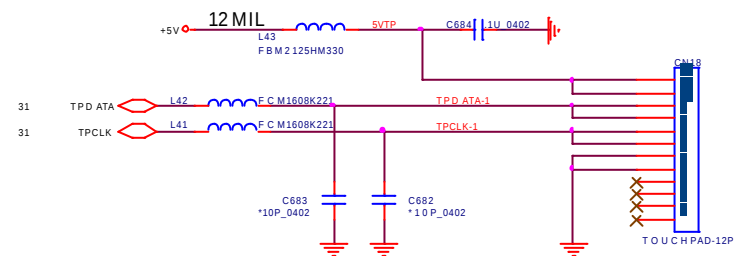
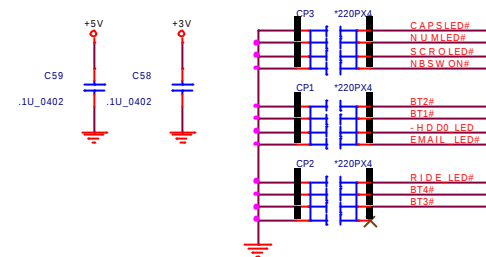
KEYBOARD



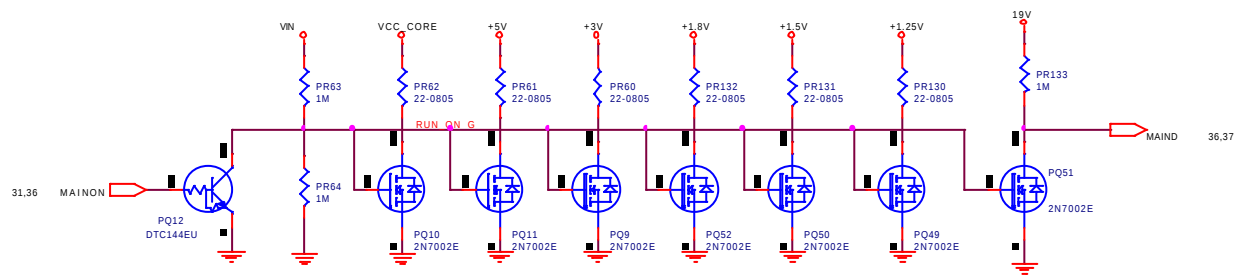
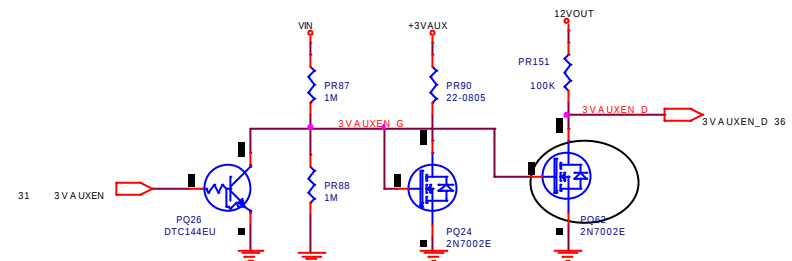
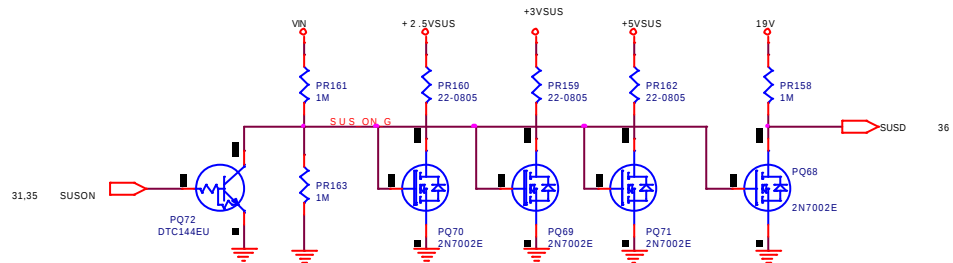
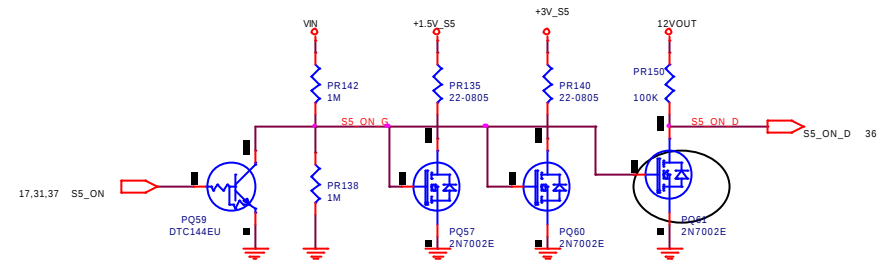
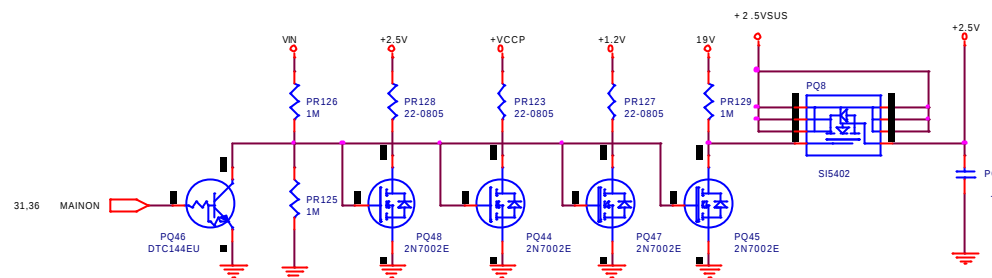
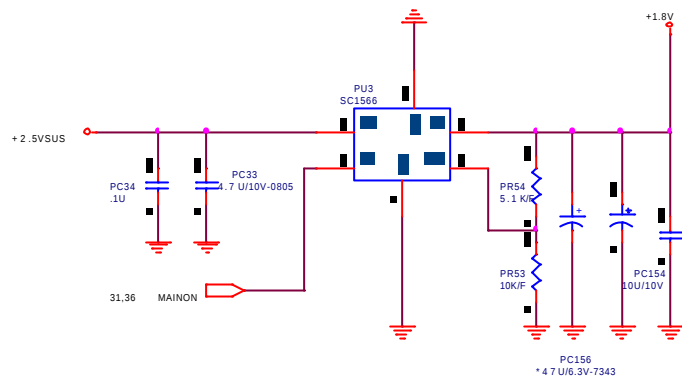
B: FOOTPRINT CHANGED

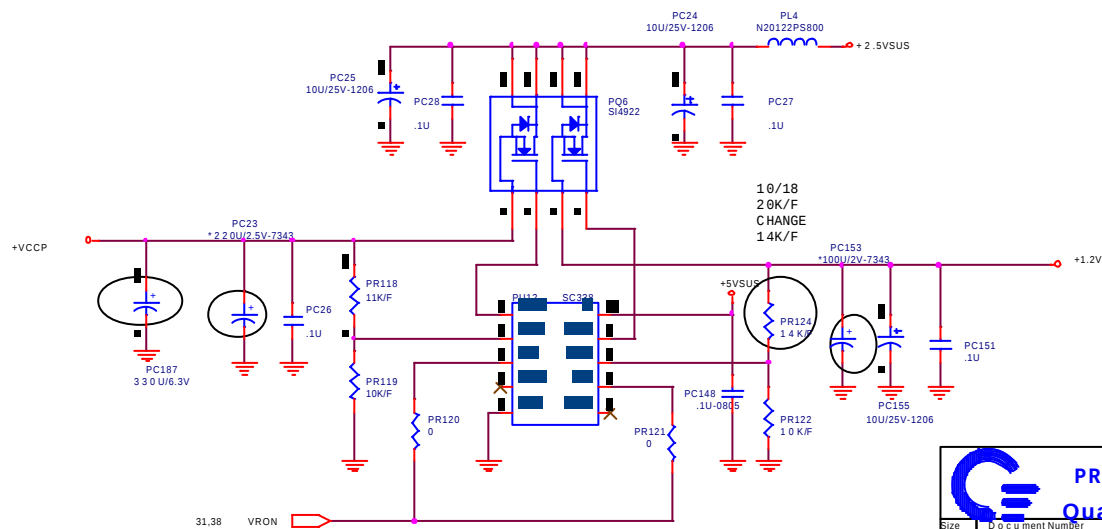


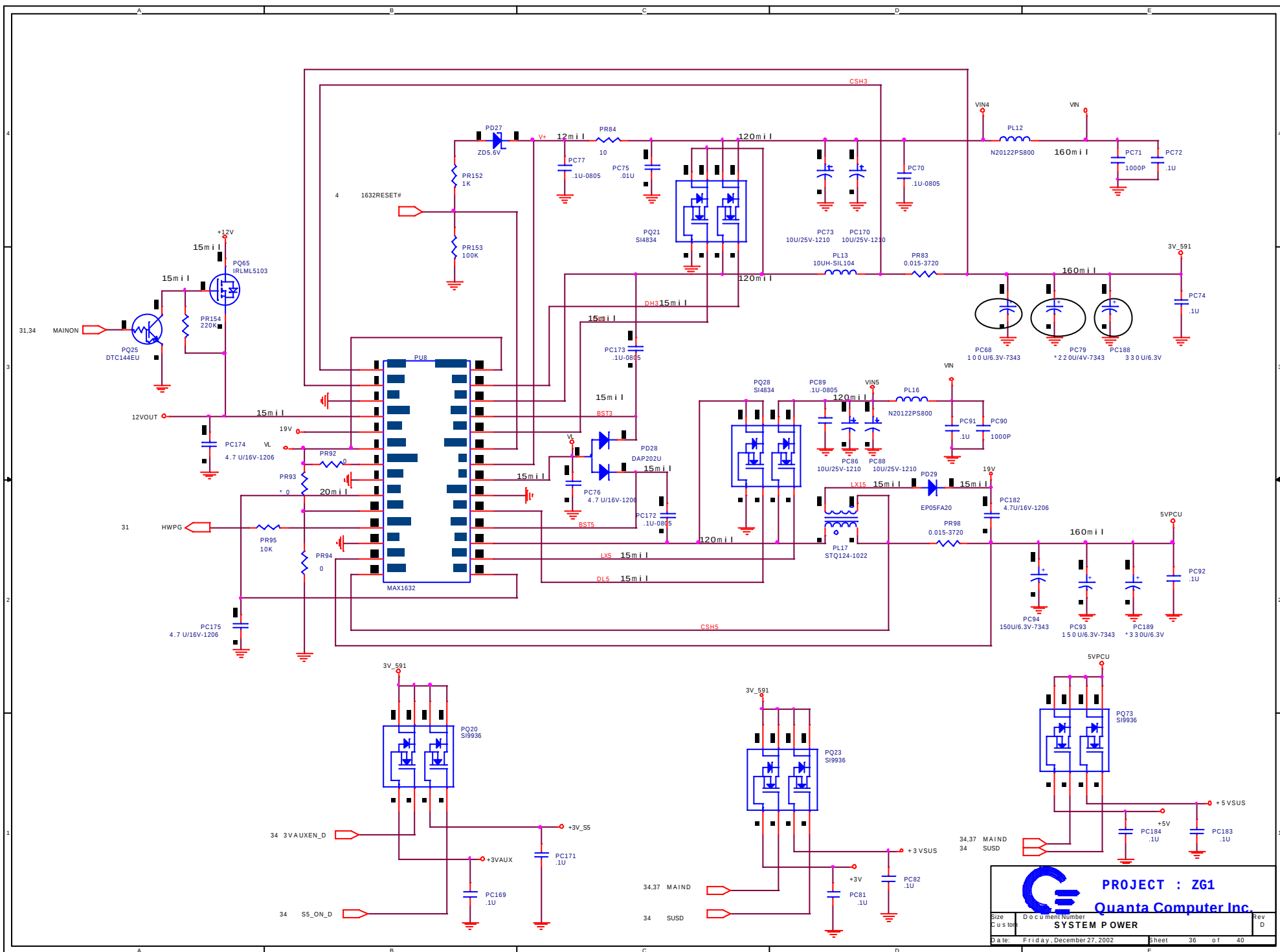
TO LED BOARD 30P

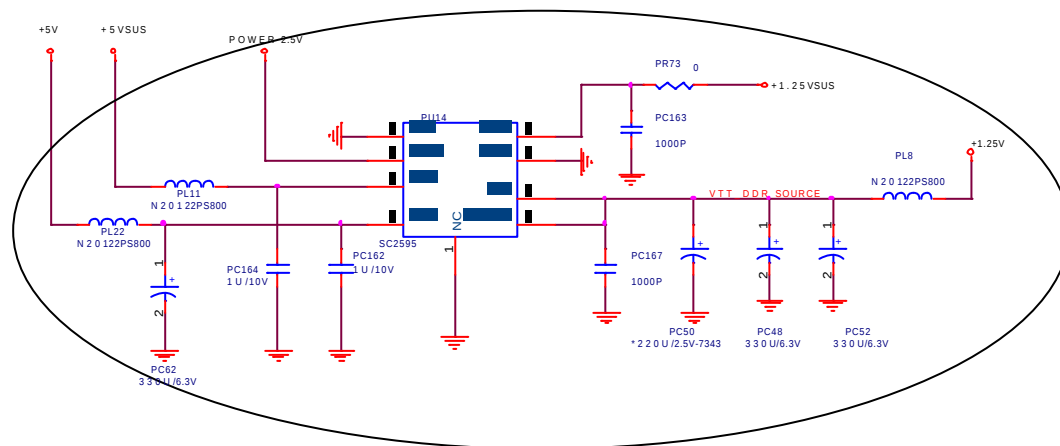
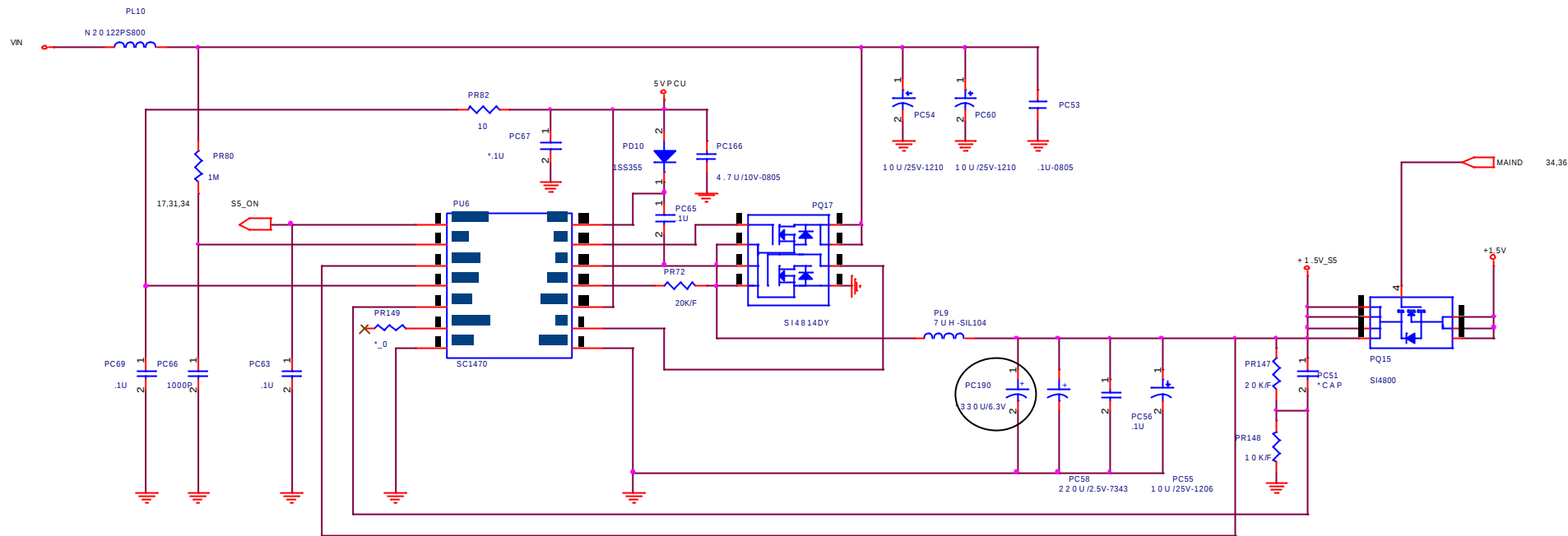


TOUCH PAD



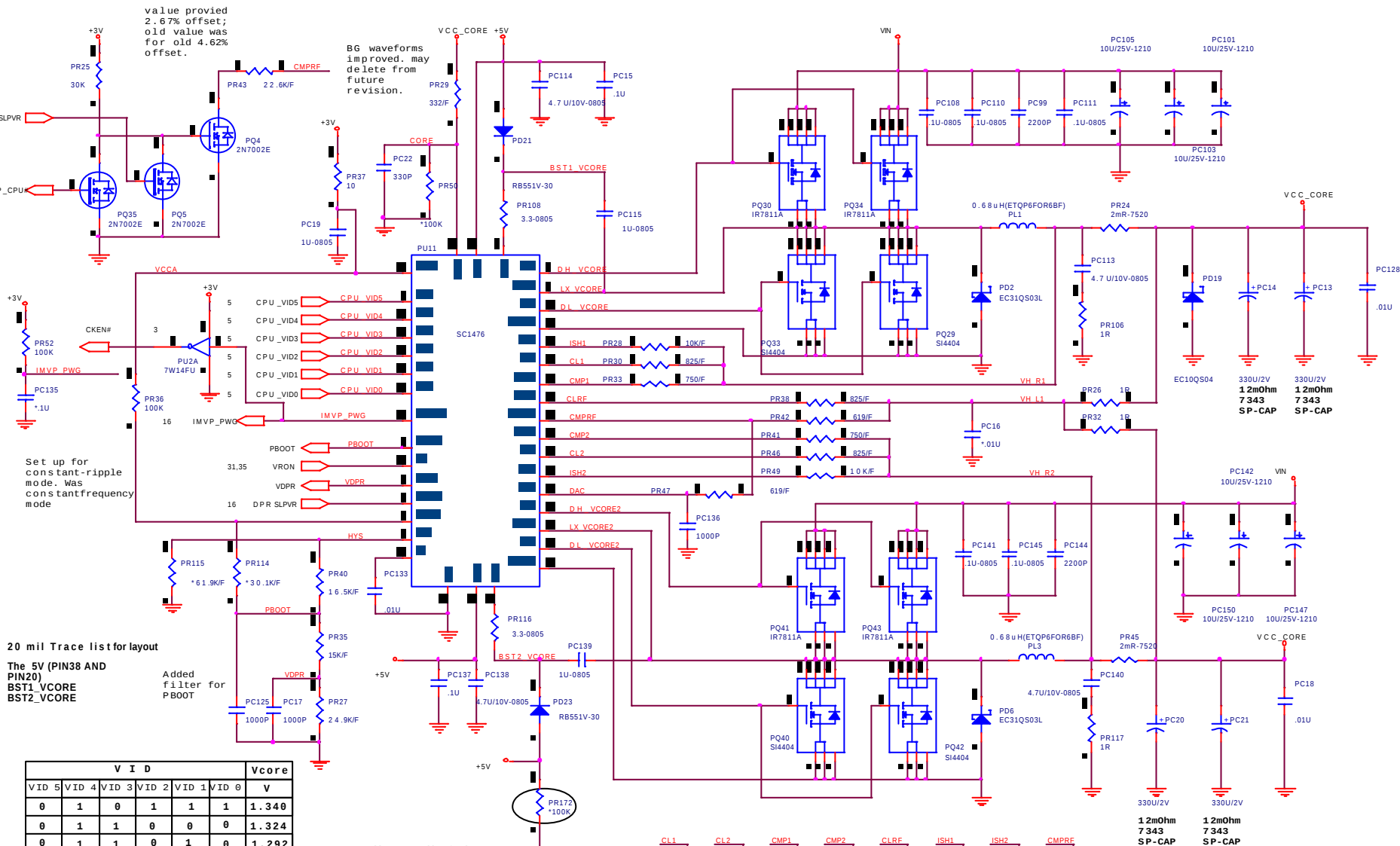






value provided
2.67% offset;
old value was
for old 4.62%
offset.

BG waveforms
improved. may
delete from
future
revision.



20 mil Trace list for layout

The 5V (PIN38 AND
PIN20)
BST1_VCORE
BST2_VCORE

V I D						Vcore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V
0	1	0	1	1	1	1.340
0	1	1	0	0	0	1.324
0	1	1	0	1	0	1.292
0	1	1	1	0	0	1.260
0	1	1	1	0	1	1.244
0	1	1	1	1	1	1.212
1	0	0	0	0	1	1.180
1	0	0	0	1	1	1.148
1	0	0	1	1	0	1.100
1	0	1	0	0	1	1.052
1	0	1	0	1	1	1.020
1	0	1	1	1	0	0.972
1	1	0	0	0	0	0.940

100 mil Trace list for layout

DH_VCORE
LX_VCORE
DL_VCORE
DH_VCORE2
LX_VCORE2
DL_VCORE2

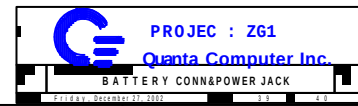
10 mil Trace list for layout

SC1476
pin 4
pin 5
pin 7
pin 25
pin 30



PROJECT : ZG1
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