Acer Flamingo

01200_SD

Project code:
PCB P/N:
REVISION:

PCB LAYER
L1: Signal 1(X)
L2: GND
L3: Signal 2 (Y)
L4: Signal 3 (X/Y)
L5: GND
L6: POWER
L7: Signal 4(weak)
L8: Signal 5 (X)
L9: GND
L10:Signal 6 (Y)

CLK GEN.
ICS
PAGE:03

Mobile CPU
Tualatin
verson :
PAGE:4~5

HOST BUS (133M)

RAM BUFFER (2*32bit)*2

SO-DIMM*2
PAGE:10

(133M) MEM BUS

Almador-M
GMCH
Version : A4
PAGE:7~9

(66M) AGP 4X

VGA
ATI Mobility M6S
version:
PAGE:11~12

CRT
PAGE:13

LCD
PAGE:13

DOCK V

TV OUT

HUB I/F (66M)

ATA100

PRIMARY EIDE **HDD**
PAGE:18

HOT PLUG

SECONDARY EIDE **CDROM**
PAGE:18

USB 1.0X2
PAGE:19

ICH3-M
Version :
PAGE:15~17

LAN
82562EM
PAGE:20

POWER SW
MIC2564A
PAGE:22

PCI BUS (33M)

DOCK V

QSW

CARDBUS
OZ6933T
PAGE:21

CARDBUS
SLOT A,B
PAGE:22

AC-Link

LPC BUS (33M)

LINE IN

INT.SPKR

LINE OUT

OP AMP
APA2020
PAGE:25

VR

MIC

AC'97 CODEC
ALC200
PAGE:23

MODEM Daughter Card
PAGE:19

SMsC SIO
LPC47N267
PAGE:27

KBC
M38859
PAGE:26

FWH
82802AB
PAGE:29

LPC DEBUG CONN.
PAGE:29

CMOS BAT

FIR
PAGE:27

FLOPPY
PAGE:18

PRINTER
PAGE:28

SERIAL
PAGE:28

FINGER PRINTER
PAGE:27

TOUCH PAD
PAGE:28

INT. KB
PAGE:26

PS/2 CONN
PAGE:26

DC/DC&CHARGER
Switching Power
MAX1632/MAX1772

INPUTS	OUTPUTS
DCBATOUT	+6V
AD+	+5VSB
	+3.3V
	+5V
	+12V
	CD+5V
	PAGE:32

CPU DC/DC
Switching Power
MAX1718/MAX1714

INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE
	+VCCT
	PAGE:30/31

OTHER DC/DC
MAX1644/MAX1792
MAX8863

INPUTS	OUTPUTS
+5V	+1.8V
+3.3V	+1.5V
LAN_+3.3V	+3VSB
+5VSB	+1.8VSB
	+3.3V
	PAGE:31/32

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Taiwan, R.O.C.

Title: Block Diagram

Size: A3 | Document Number: Acer Flamingo | Rev: SB

Date: Thursday, July 05, 2001 | Sheet 1 of 38

Acer Flmanigo History

Rev. 0.1 : Jun. /1 / 2001 for PCB team placement

Acer Incorporated
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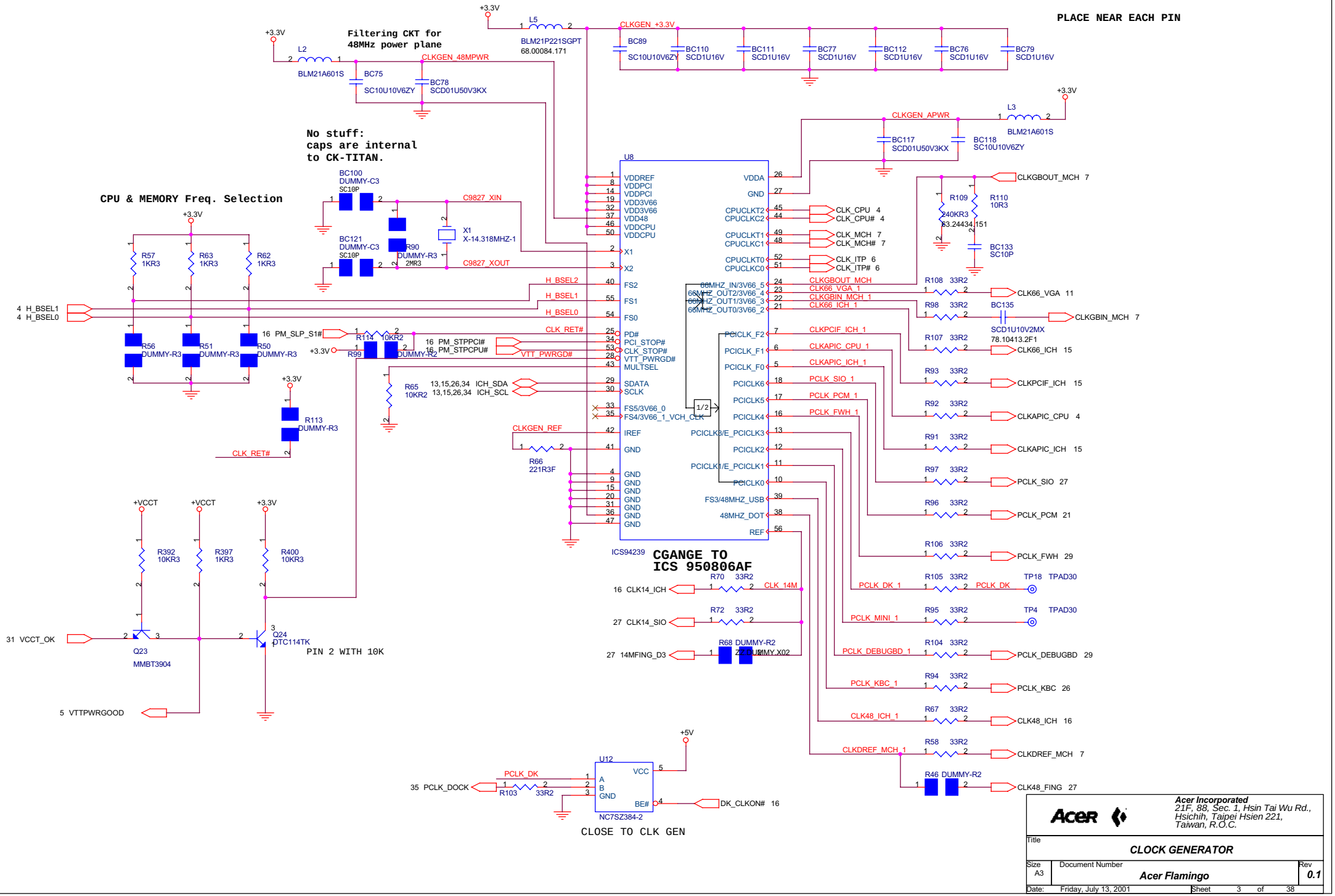
Taiwan, R.O.C.

Title	REVISION HISTORY	
Size: A3	Document Number: Acer Flamingo	Rev: SB
Date: Monday, May 14, 2001	Sheet 2 of 38	


PLACE NEAR EACH PIN
Filtering CKT for
48MHz power plane
No stuff:
caps are internal
to CK-TITAN.
CPU & MEMORY Freq. Selection
U8
ICS94239
CGANGE TO
ICS 950806AF
PIN 2 WITH 10K
CLOSE TO CLK GEN
Acer Incorporated
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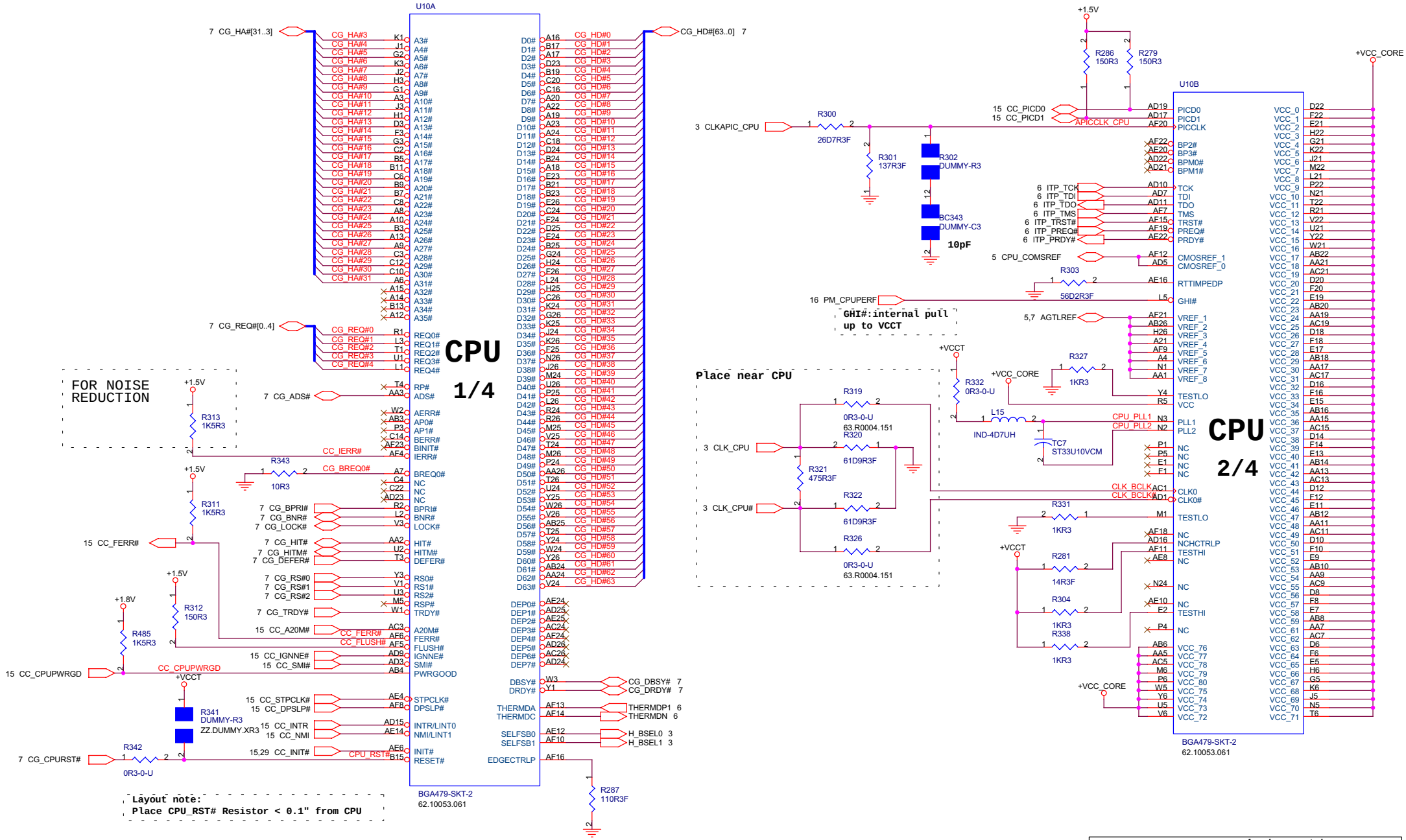
Title
CLOCK GENERATOR
Size
A3
Document Number
Acer Flamingo
Rev
0.1
Date:
Friday, July 13, 2001
Sheet
3
of
38


U10A
CPU 1/4
U10B
CPU 2/4
FOR NOISE REDUCTION
Place near CPU
GHI#:internal pull up to VCCT
Layout note:
Place CPU_RST# Resistor < 0.1" from CPU
BGA479-SKT-2
62.10053.061
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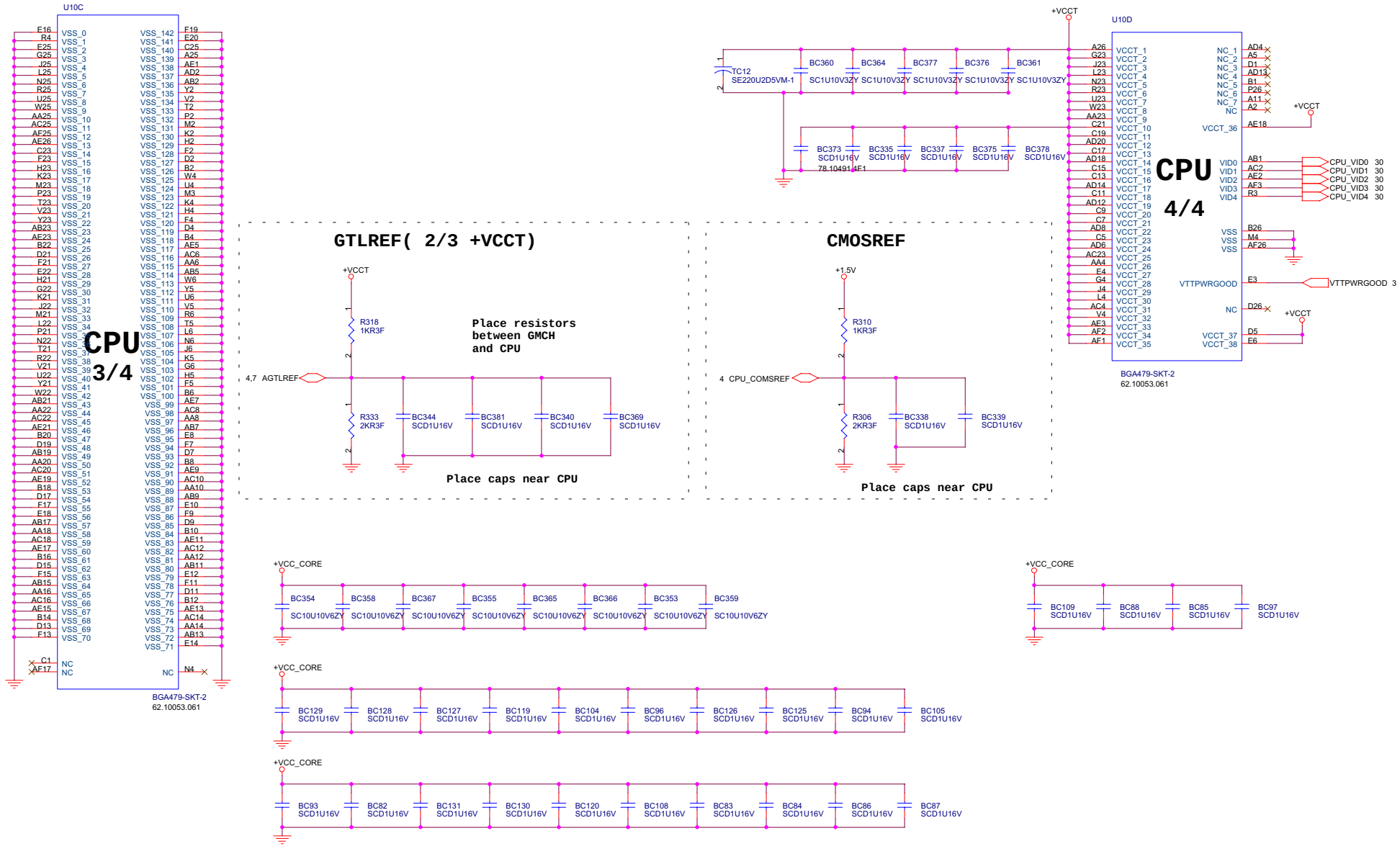
Title
CPU 1/2
Size A3
Document Number
Acer Flamingo
Rev SB
Date: Friday, July 13, 2001
Sheet 4 of 38



Decouping Recommendation

				Freeza	Kodiak Ver. 0.5
VCC_CORE	Underneath balls on solder side	0.47uF * 24	Use 2-3 vias per pad for reduced inductance during layout	0.1uF * 24	10uF / 6.3V * 12
	On the peripheral near balls	10uF / 6.3V * 10	Placement should be near processor for all	10uF / 10V * 10	10uF / 6.3V * 10 + 6 * NS
	Bulk Caps			220uF / 2.5V * 8	150uF / 4V * 12 + 2 * NS
VCCT	Place close to processor for all	1uF * 10	Use 2 vias per pad for reduced inductance during layout	1uF * 10	1uF * 10 + 2 * NS
	Bulk Caps			220uF / 2.5V * 2	150uF / 4V * 5 + 1 * NS

Almador-M Checklist Ver. 0.5 8/28

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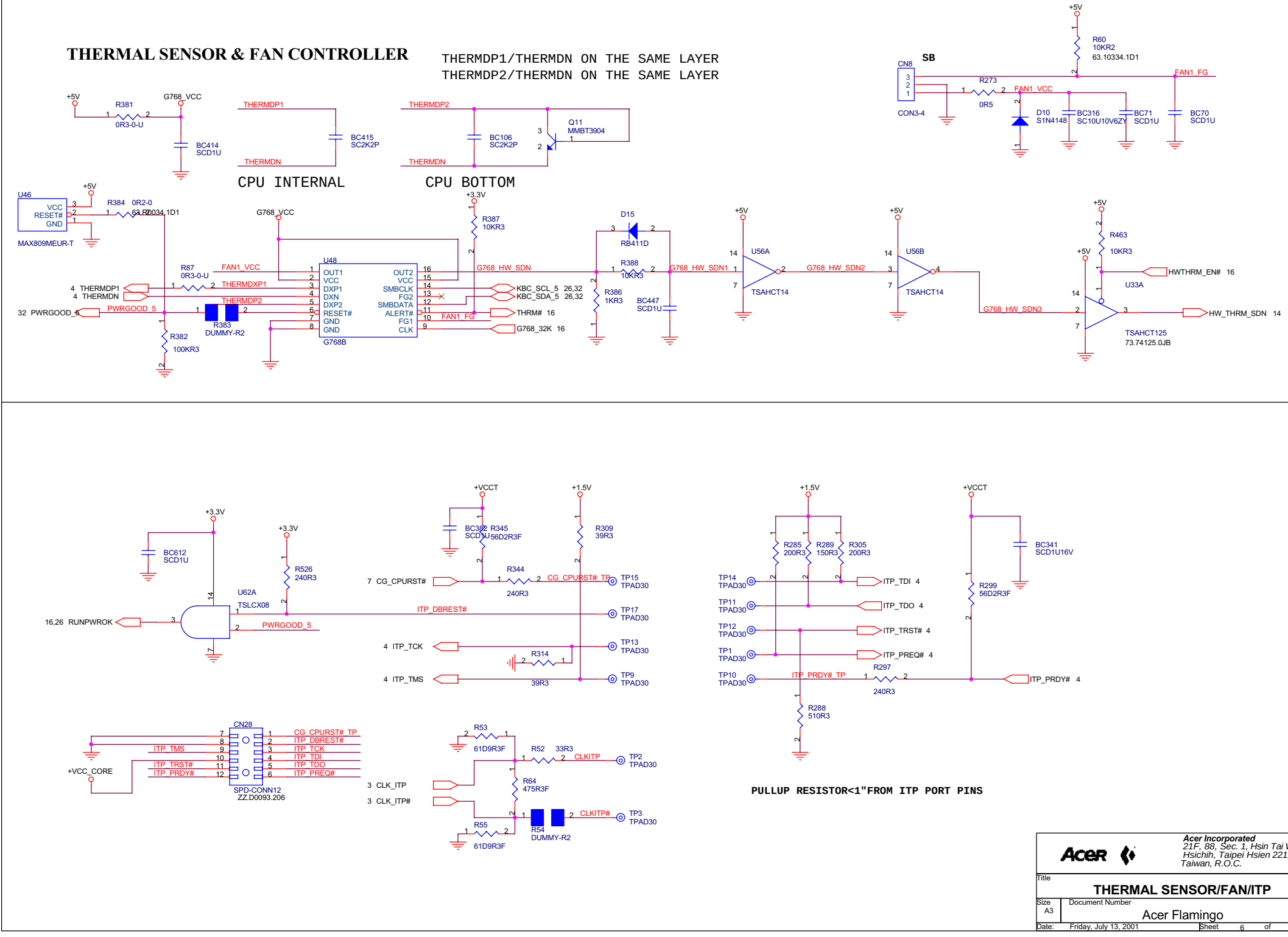
Title: CPU 2/2 CONFIGURATION

Size: Custom | Document Number: Acer Flamingo | Rev: SB

Date: Friday, July 13, 2001 | Sheet 5 of 38

THERMAL SENSOR & FAN CONTROLLER

THERMDP1/THERMDN ON THE SAME LAYER
THERMDP2/THERMDN ON THE SAME LAYER



PULLUP RESISTOR<1"FROM ITP PORT PINS

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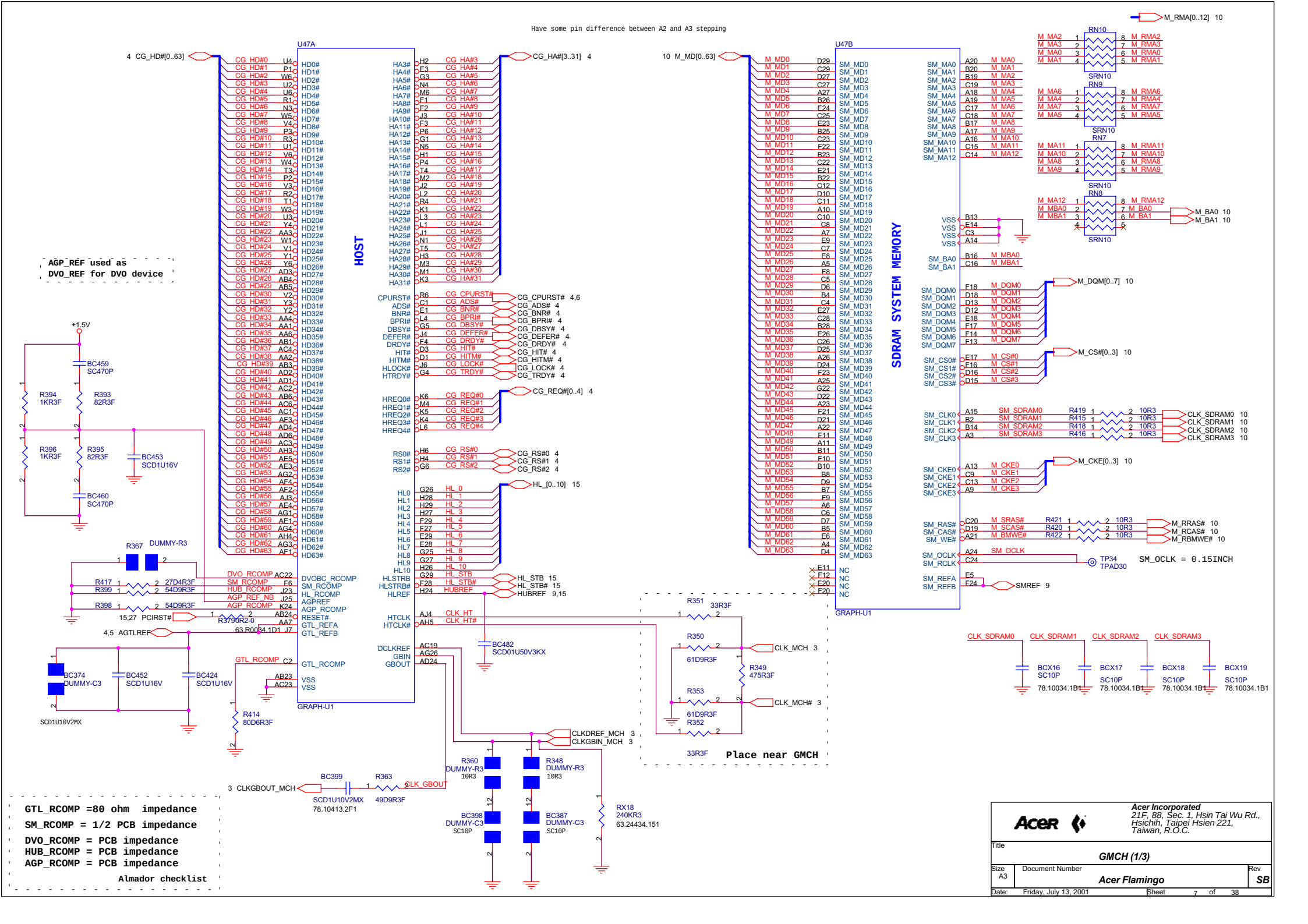
Title: **THERMAL SENSOR/FAN/ITP**

Size	Document Number	Rev
A3	Acer Flamingo	SB

Date: Friday, July 13, 2001 Sheet 6 of 38


Have some pin difference between A2 and A3 stepping
U47A
HOST
GRAPH-U1
U47B
SDRAM SYSTEM MEMORY
GRAPH-U1
AGP_REF used as
DVO_REF for DVO device
GTL_RCOMP =80 ohm impedance
SM_RCOMP = 1/2 PCB impedance
DVO_RCOMP = PCB impedance
HUB_RCOMP = PCB impedance
AGP_RCOMP = PCB impedance
Almador checklist
Place near GMCH
SM_OCLK = 0.15INCH
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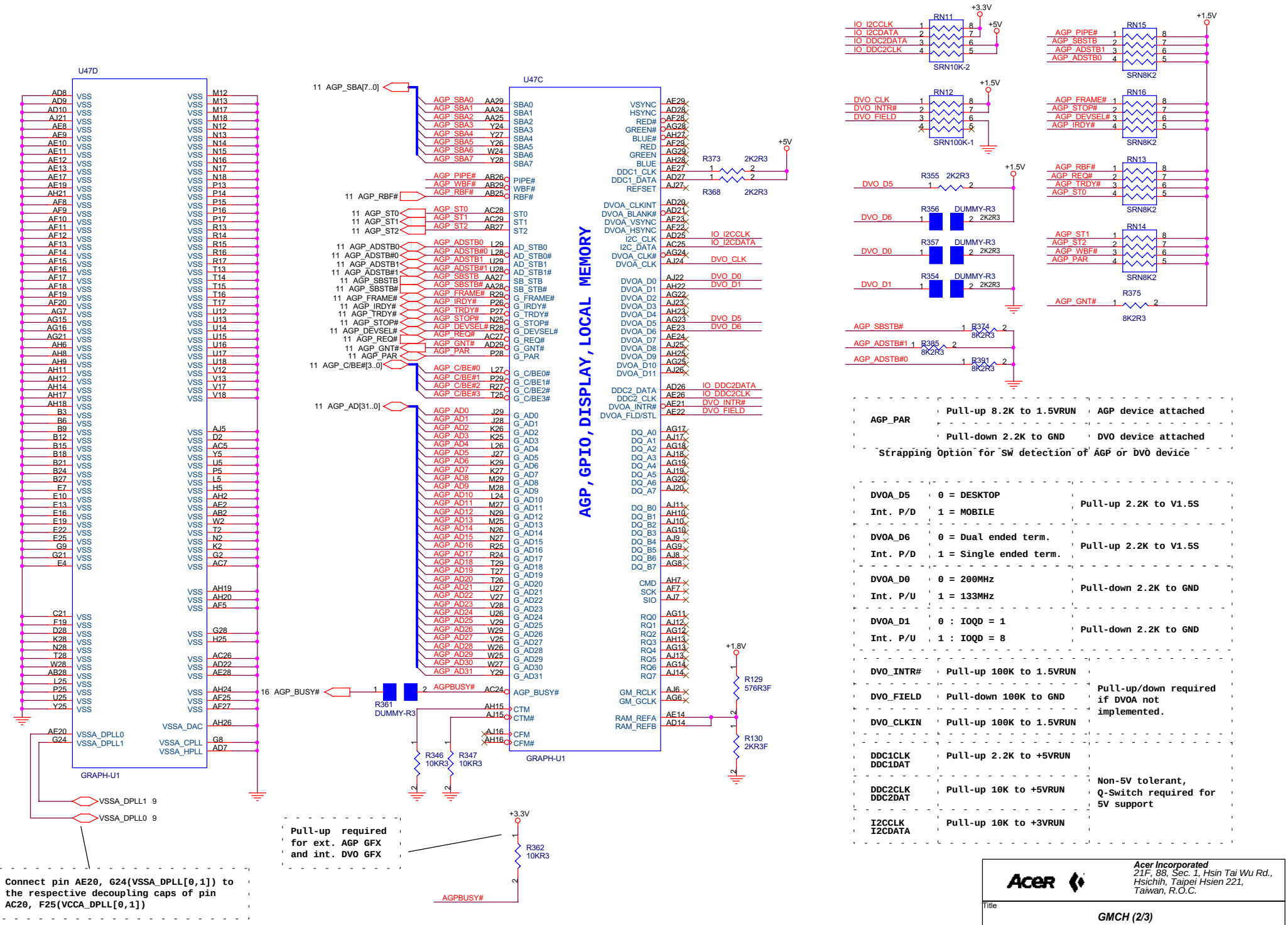
Taiwan, R.O.C.
Title
GMCH (1/3)
Size A3
Document Number
Acer Flamingo
Rev SB
Date: Friday, July 13, 2001
Sheet 7 of 38



AGP_PAR	Pull-up 8.2K to 1.5VRUN	AGP device attached
	Pull-down 2.2K to GND	DVO device attached

Strapping Option for SW detection of AGP or DVO device

DVOA_D5 Int. P/D	0 = DESKTOP 1 = MOBILE	Pull-up 2.2K to V1.5S
DVOA_D6 Int. P/D	0 = Dual ended term. 1 = Single ended term.	Pull-up 2.2K to V1.5S
DVOA_D0 Int. P/U	0 = 200MHz 1 = 133MHz	Pull-down 2.2K to GND
DVOA_D1 Int. P/U	0 : IOQD = 1 1 : IOQD = 8	Pull-down 2.2K to GND
DVO_INTR#	Pull-up 100K to 1.5VRUN	Pull-up/down required if DVOA not implemented.
DVO_FIELD	Pull-down 100K to GND	
DVO_CLKIN	Pull-up 100K to 1.5VRUN	
DDC1CLK DDC1DAT	Pull-up 2.2K to +5VRUN	Non-5V tolerant, Q-Switch required for 5V support
DDC2CLK DDC2DAT	Pull-up 10K to +5VRUN	
I2CCLK I2CDATA	Pull-up 10K to +3VRUN	

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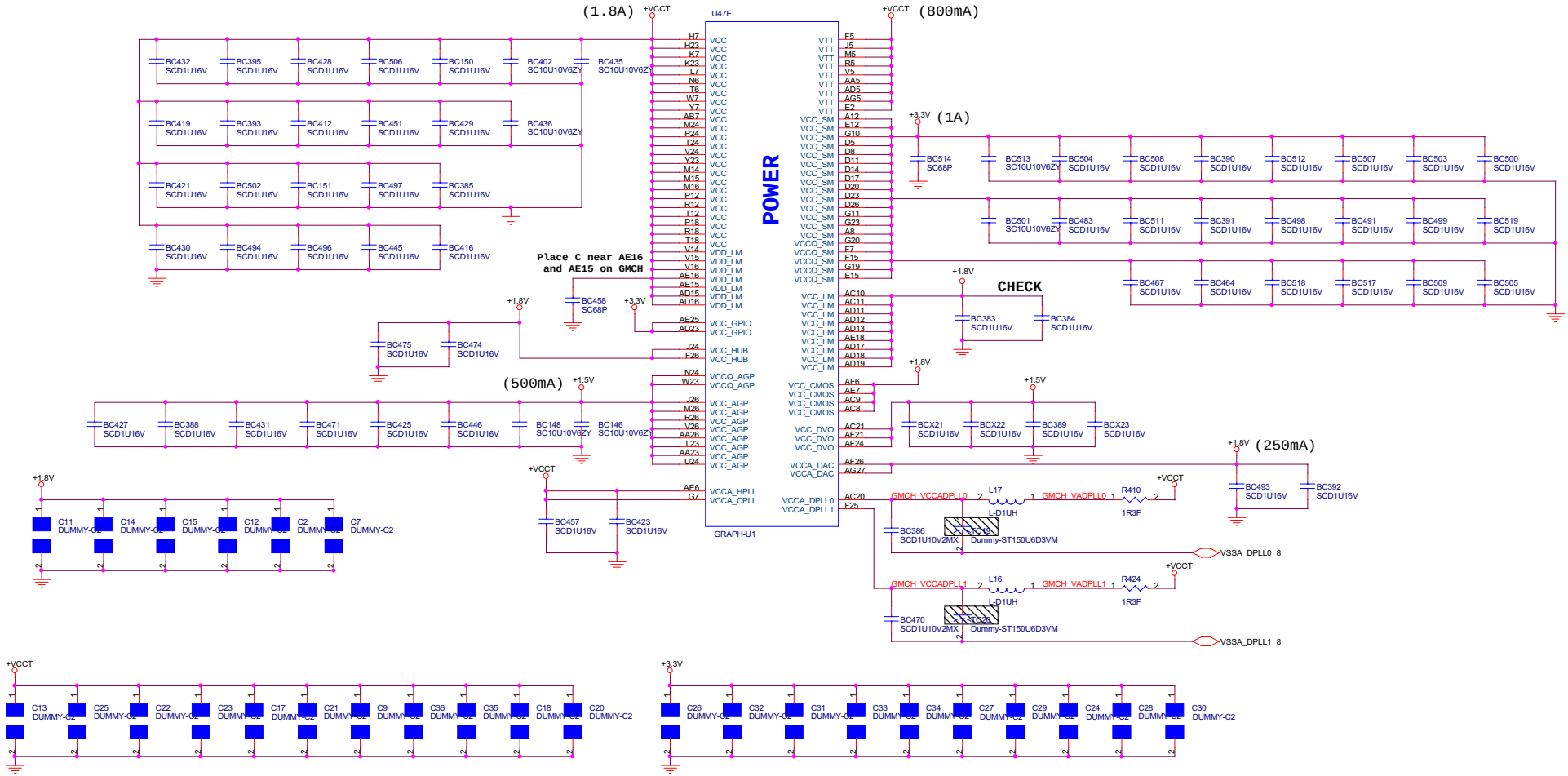
Title: GMCH (2/3)

Size: A3 | Document Number: Acer Flamingo | Rev: SB

Date: Friday, July 13, 2001 | Sheet 8 of 38

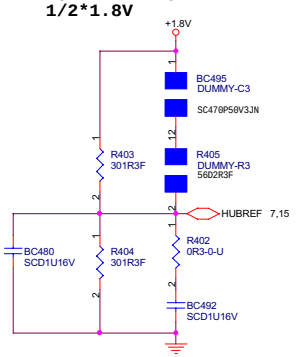


Decoupling Recommendation

				Freeza	Kodiak Ver. 0.5
V1.2S_GMCH	Decoupling Caps	0.1uF * 20	Distribute as close as possible to GMCH-M processor Quadrant	0.1uF * 20	1uF * 20
	Bulk Caps			100uF / 10V * 2	150uF / 4V * 5 + 1 * NS
V1.2S_GMCHCORE	Decoupling Caps	68pF * 1 0.1uF * 40	Close to VDD_LM, near pins AE15 and AE16 on Almador	68pF * 1	68pF * 1 1uF * 40
	Bulk Caps				150uF / 4V * 10 + 1 * NS
V1.5S_GMCH	Decoupling Caps	0.1uF * 9 82pF * 4	Distribute as close as possible to GMCH-M AGP/DVO Quadrant	0.1uF * 8 0.01uF * 3 10uF / 10V * 1	0.1uF * 9 82pF * 4
	Bulk Caps			100uF / 10V * 1	22uF / 20V * 1
V1.8S_GMCH	Decoupling Caps	0.1uF * 4 + 4 82pF * 2	Distribute as close as possible to GMCH-M Local Memory Quadrant Additional 4* 0.1uF shall be distributed as close as possible to VCCPCMOS_LM	0.1uF * 2	0.1uF * 4 + 2 82pF * 2 22uF / 20V * 2
	Bulk Caps				68uF / 10V * 5
V3_GMCH	Decoupling Caps	0.1uF * 12 + 2 82pF * 4	Distribute as close as possible to GMCH-M System Memory Quadrant Additional 4* 0.1uF shall be distributed as close as possible to IO Quadrant	0.1uF * 20 100uF / 10V * 1	0.1uF * 12 + 2 82pF * 4 22uF / 20V * 2
	Bulk Caps				

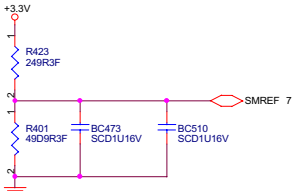
Almador-M Checklist Ver. 0.5 8/28

HUB INTERFACE REF 1/2*1.8V



Layout Note:
Place divider pair in middle of bus.
Place capacitors near GMCH.

SYSTEM MEMORY REF 0.55V



Place capacitor near GMCH.

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Title	GMCH(3/3)		
Size: Custom	Document Number: Acer Flamingo		Rev: SB
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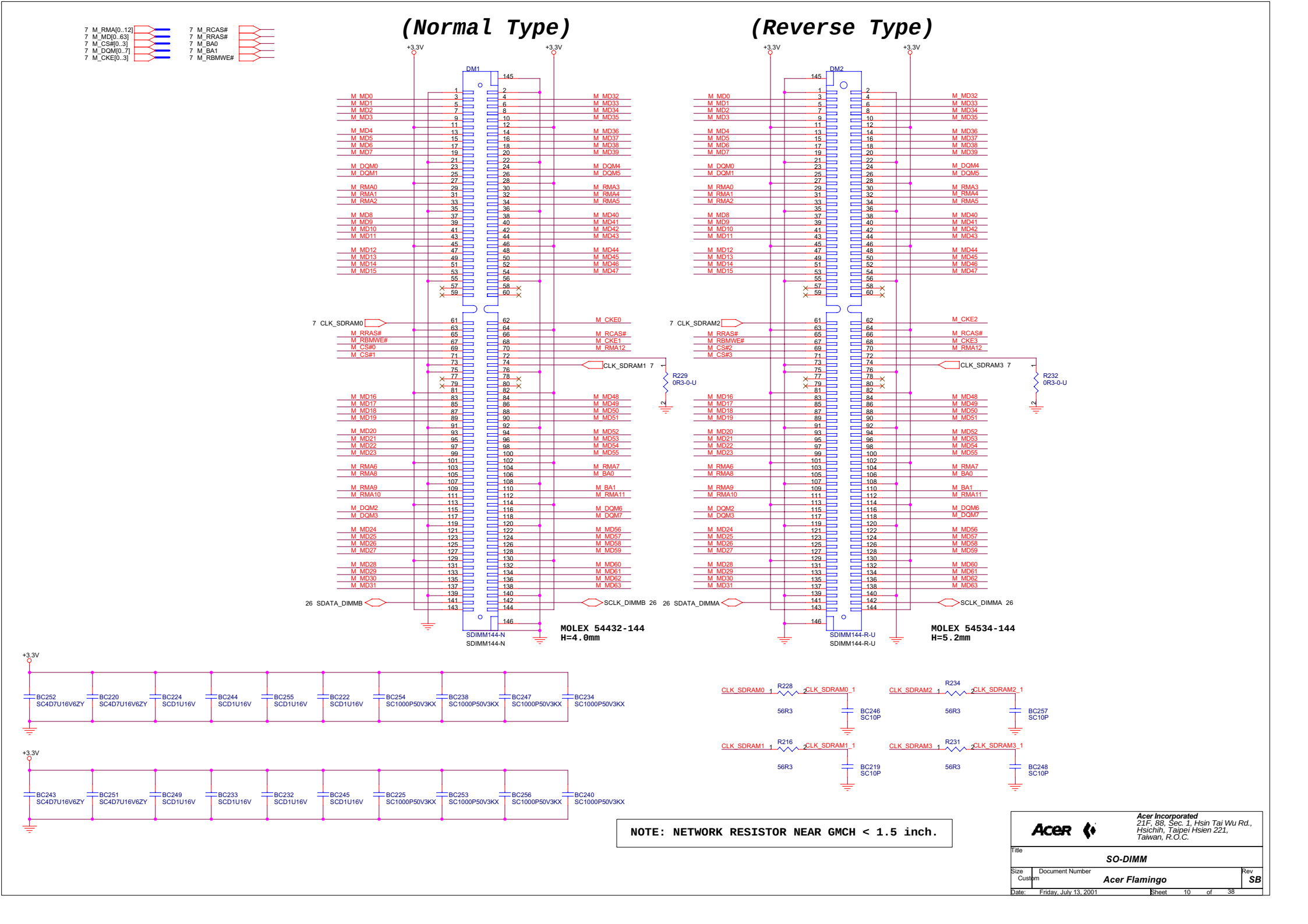

NOTE: NETWORK RESISTOR NEAR GMCH < 1.5 inch.

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Title	SO-DIMM	
Size: Custom	Document Number: Acer Flamingo	Rev: SB
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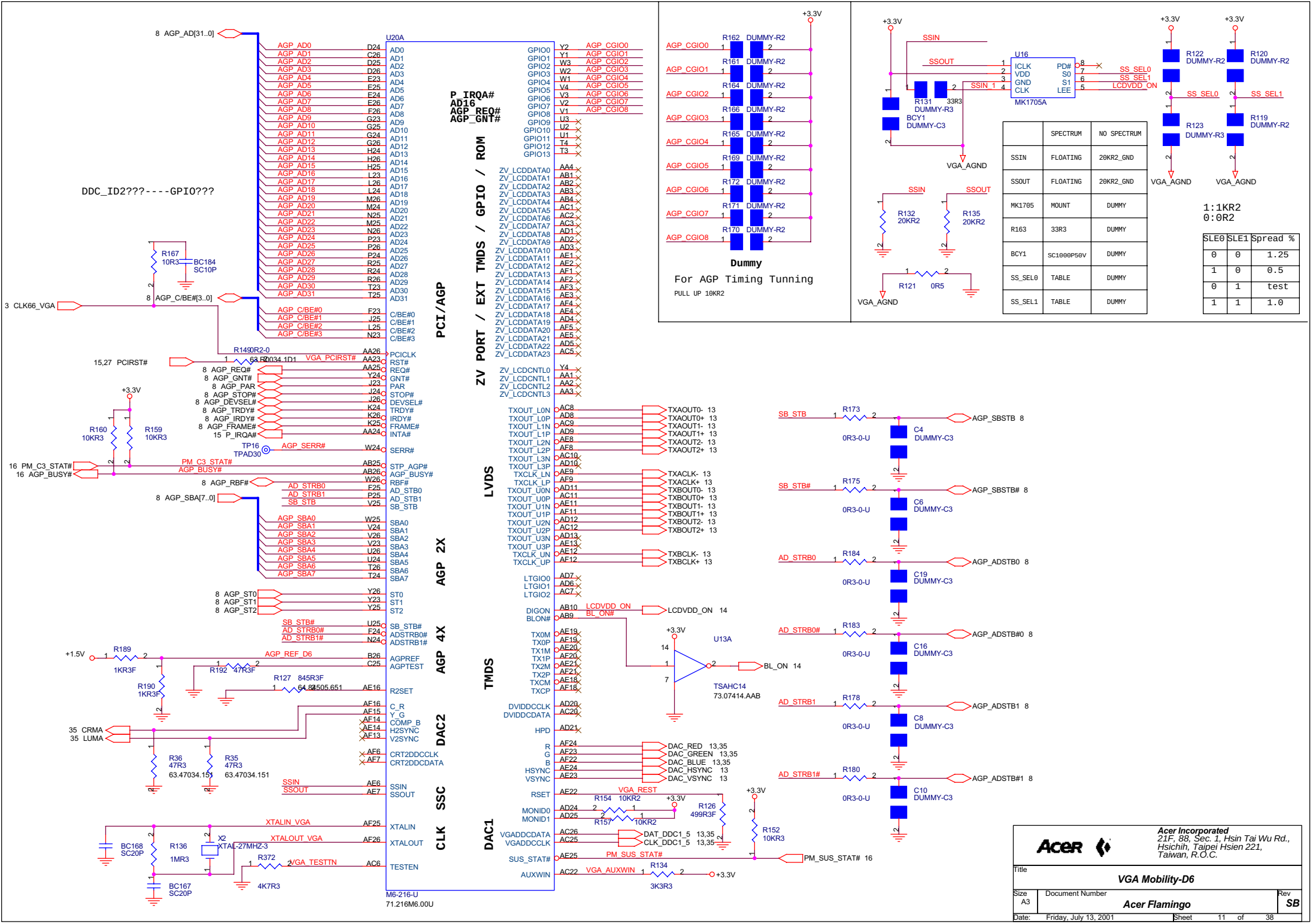
U20A
M6-216-U
71.216M6.00U
PCI/AGP
AGP 2X
AGP 4X
DAC2
SSC
CLK
DAC1
TMDS
LVDS
ZV PORT / EXT TMDS / GPIO / ROM
P_IRQA#
AD16
AGP_REQ#
AGP_GNT#
DDC_ID2???----GPIO???
Dummy
For AGP Timing Tunning
PULL UP 10KR2
U16
MK1705A
SSIN
SSOUT
VGA_AGND
1:1KR2
0:0R2
SLE0 SLE1 Spread %
0 0 1.25
1 0 0.5
0 1 test
1 1 1.0
U13A
TSAHC14
73.07414.AAB
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Taiwan, R.O.C.
Title
VGA Mobility-D6
Size A3
Document Number
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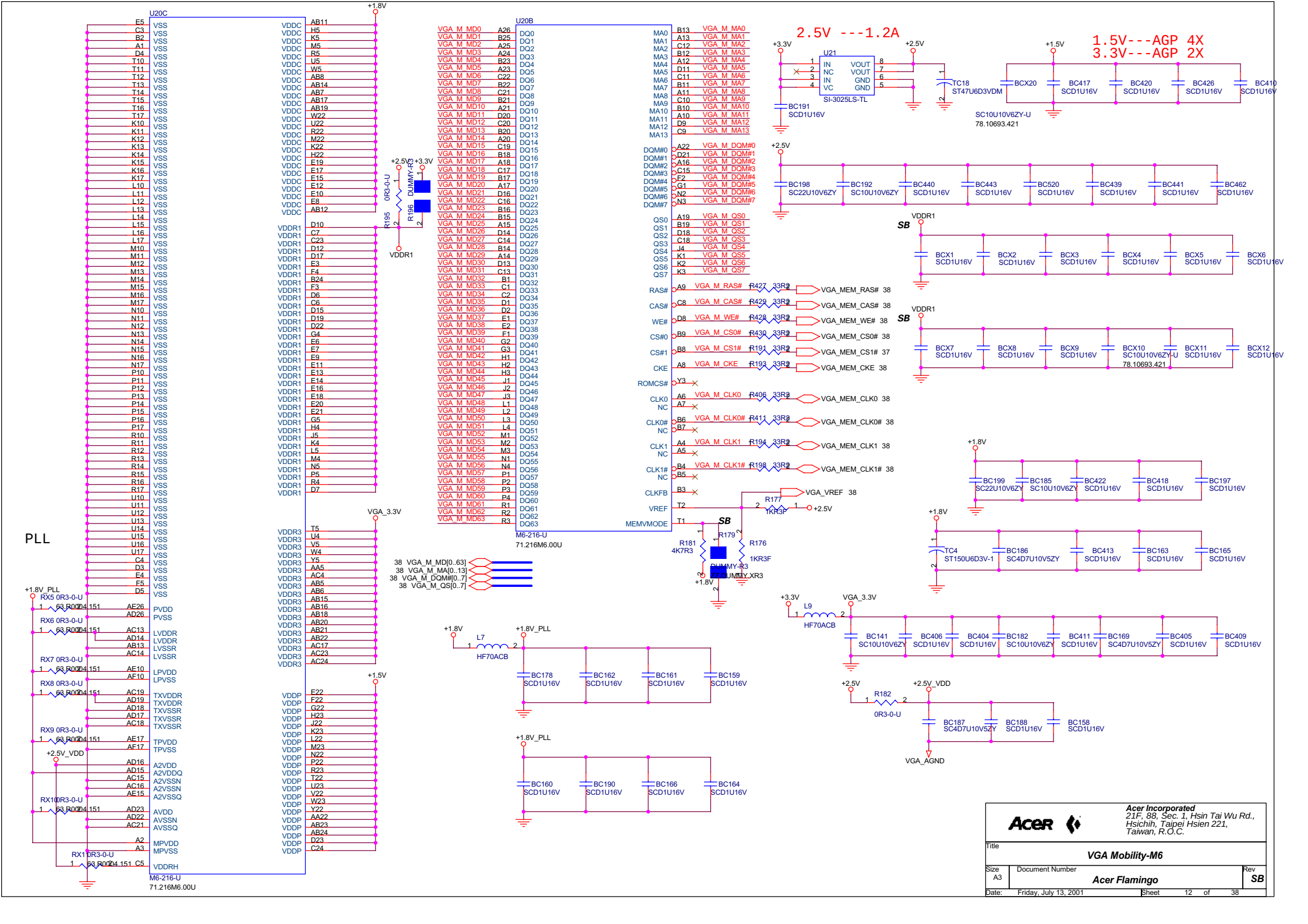
U20C
M6-216-U
71.216M6.00U
U20B
M6-216-U
71.216M6.00U
PLL
2.5V ---1.2A
1.5V---AGP 4X
3.3V---AGP 2X
U21
SI-3025LS-TL
SC10U10V6ZY-U
78.10693.421
SB
VGA_AGND
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Taiwan, R.O.C.
Title
VGA Mobility-M6
Size
A3
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Rev
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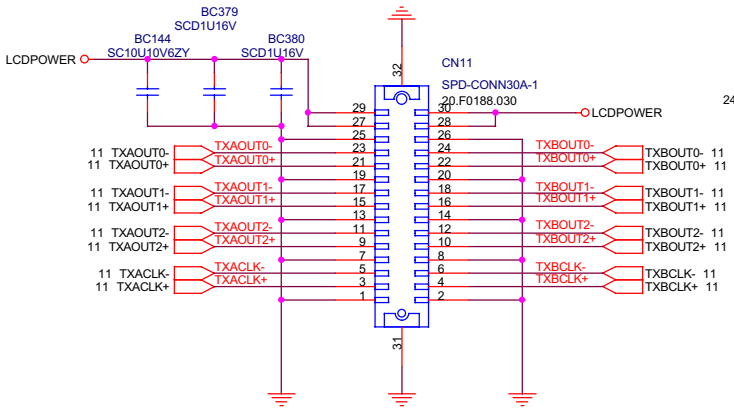
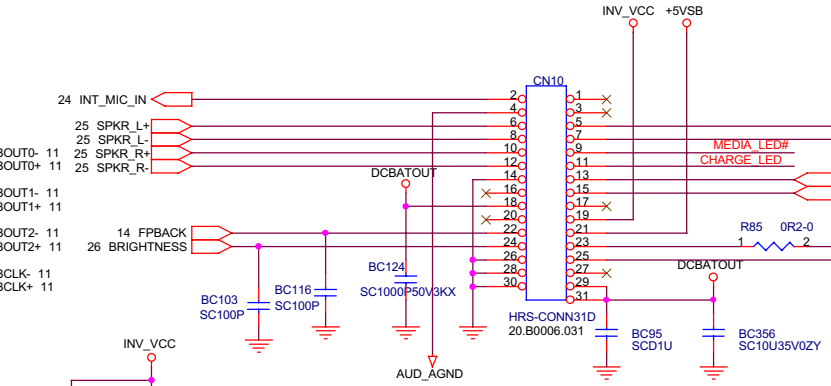
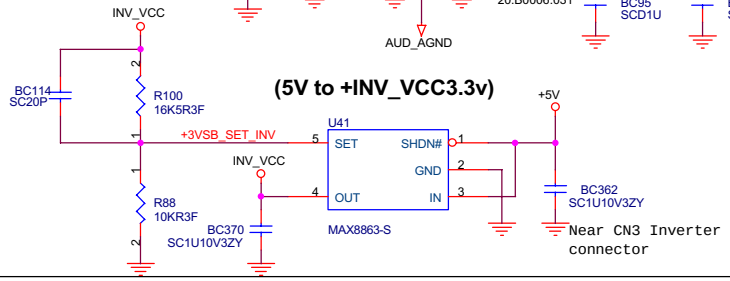
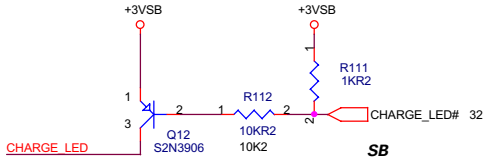
of
38

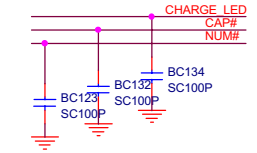
LCD

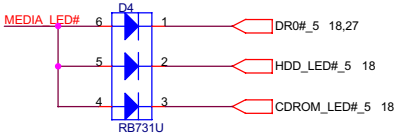




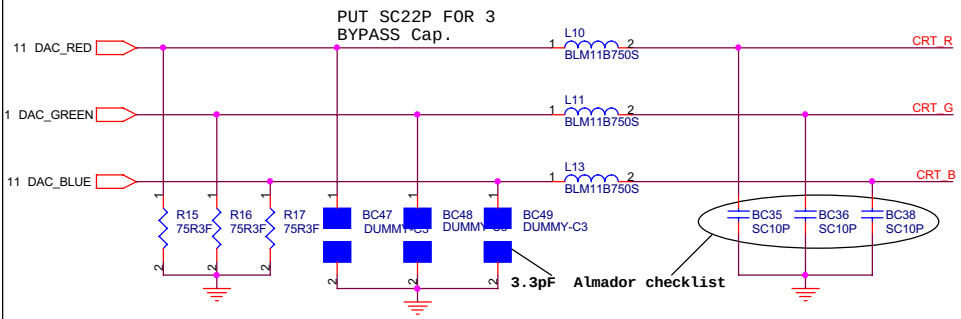


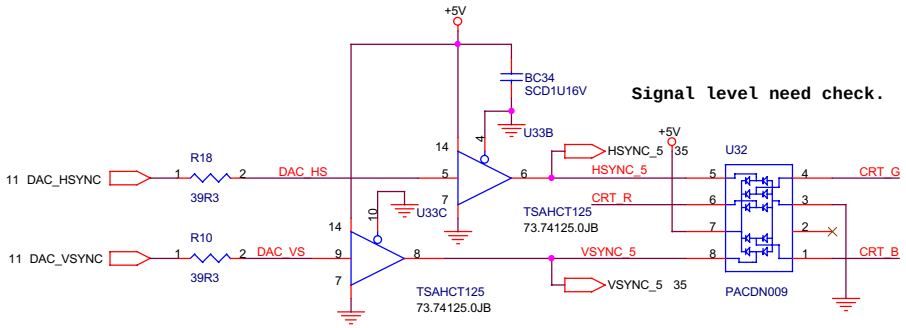


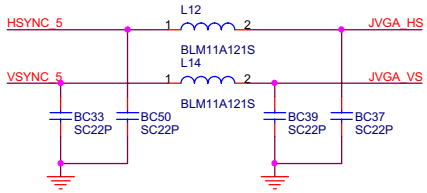


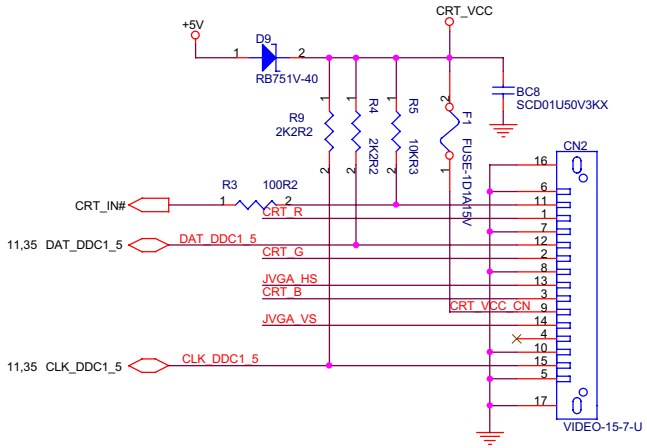


CRT









Layout Note:
Must be a ground return path between this ground and the ground on the VGA connector.

37.4_1% resistors must be placed after RGB pi filter ,near CRT connector.

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Title	LCD/INV/CRT CONN.	
Size A3	Document Number Acer Flamingo	Rev SB
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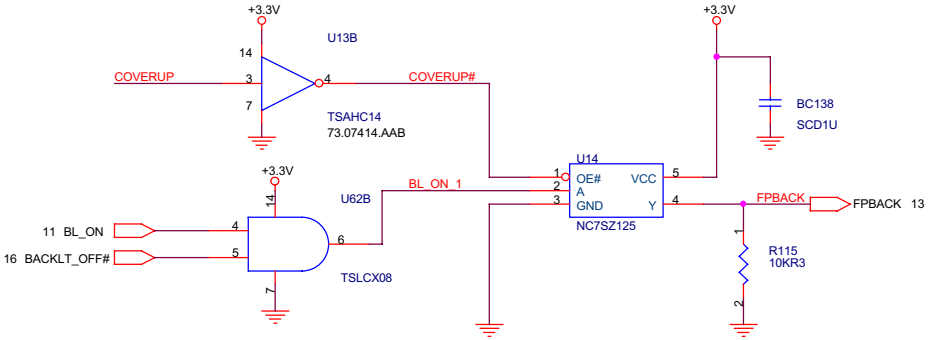

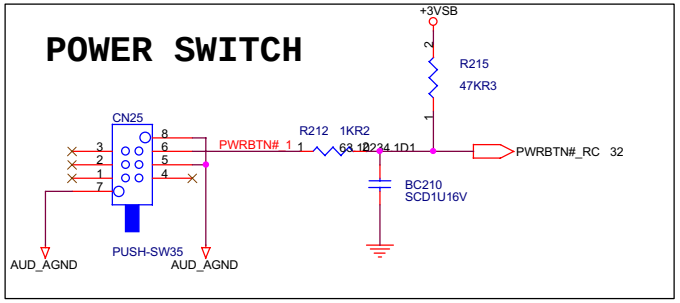

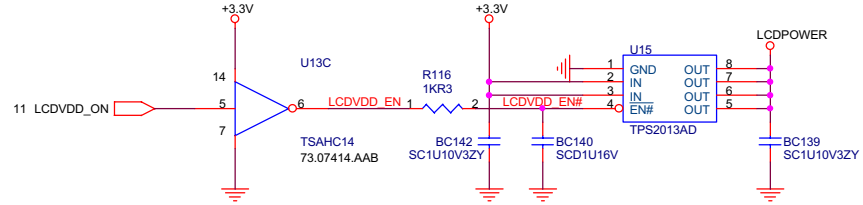

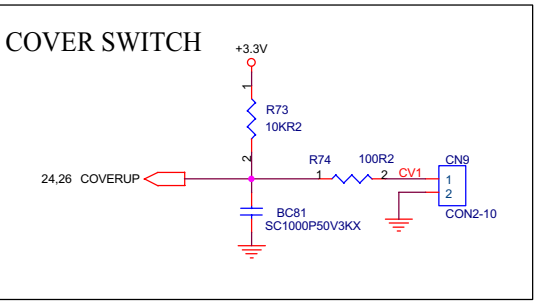

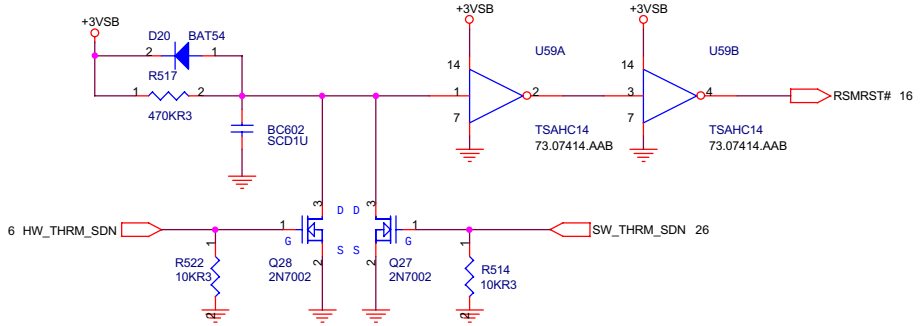

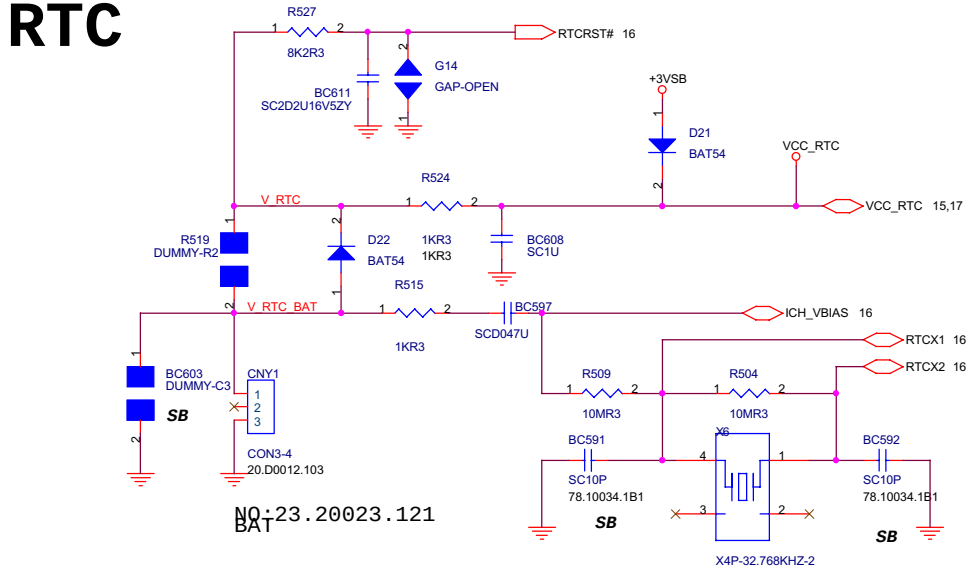

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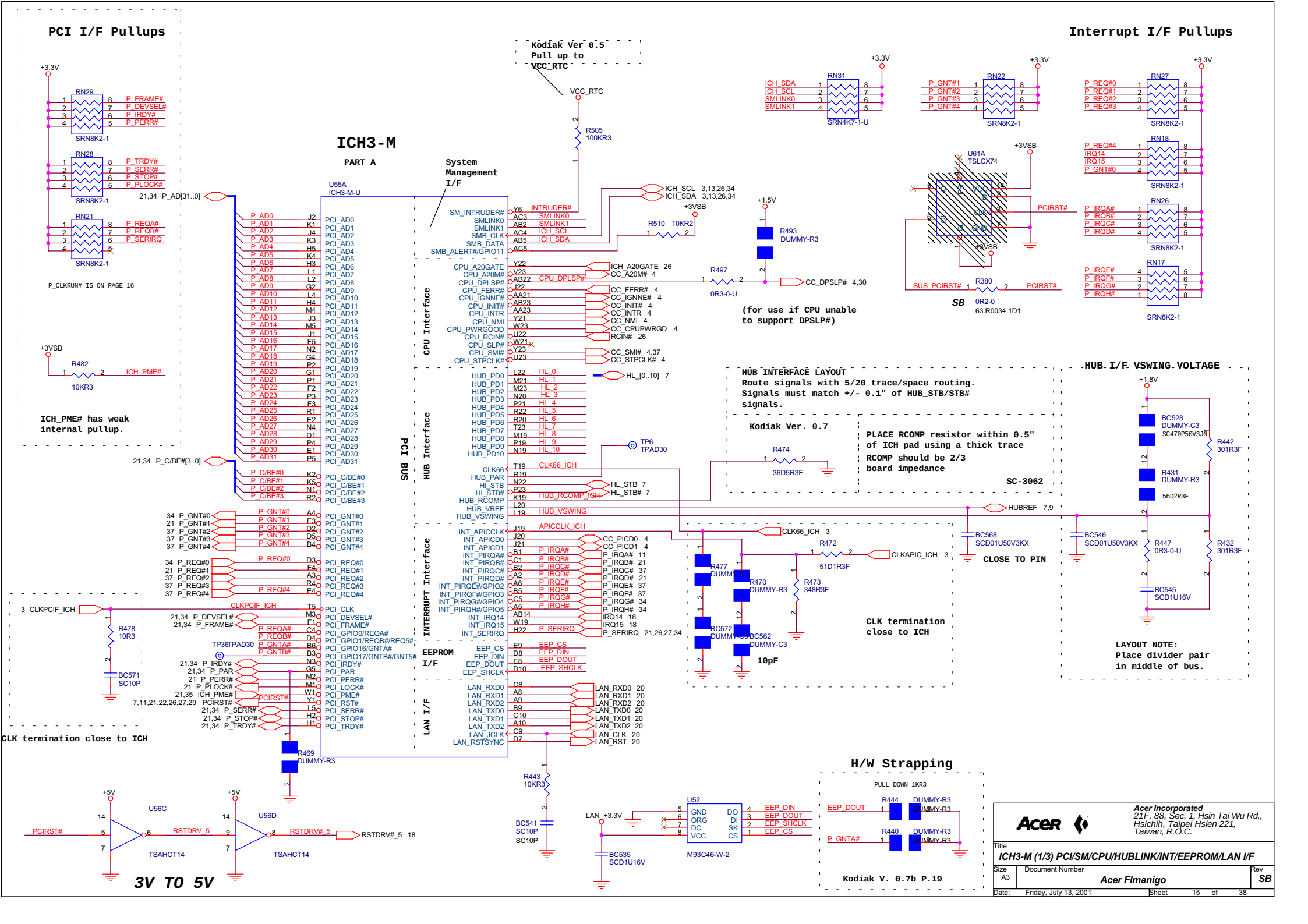
Title	PWR SW/LCD PWR/RTC
Size: A3	Document Number: Acer Flmanigo
Rev: SB	
Date: Friday, July 13, 2001	Sheet 14 of 38


PCI I/F Pullups
Interrupt I/F Pullups
Kodiak Ver 0.5
Pull up to
VCC_RTC
ICH3-M
PART A
System
Management
I/F
U55A
ICH3-M-U
PCI Bus
CPU Interface
HUB Interface
INTERRUPT Interface
EEPROM
I/F
LAN I/F
ICH_PME# has weak
internal pullup.
P_CLKRUN# IS ON PAGE 16
HUB INTERFACE LAYOUT
Route signals with 5/20 trace/space routing.
Signals must match +/- 0.1" of HUB_STB/STB#
signals.
Kodiak Ver. 0.7
PLACE RCOMP resistor within 0.5"
of ICH pad using a thick trace
RCOMP should be 2/3
board impedance
SC-3062
(for use if CPU unable
to support DPSLP#)
SB
HUB I/F VSWING VOLTAGE
CLOSE TO PIN
CLK termination
close to ICH
10pF
LAYOUT NOTE:
Place divider pair
in middle of bus.
CLK termination close to ICH
H/W Strapping
PULL DOWN 1KR3
Kodiak V. 0.7b P.19
3V TO 5V
TSAHCT14
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.
ICH3-M (1/3) PCI/SM/CPU/HUBLINK/INT/EEPROM/LAN I/F
Acer Flmanigo
Size A3
Rev SB
Date: Friday, July 13, 2001
Sheet 15 of 38

BIOS NOTE:
BIOS should disable PM_STPCPU# on CK_Titan.
(Use H_DPSLP# instead)

ICH3-M

PART B

U55B
ICH3-M-U

POWER MANAGEMENT

PM_AGPBUSY#/GPIO6
LAN_RST#
PM_BATLOW#
PM_C3_STAT#/GPIO21
PM_CLKRUN#/GPIO24
PM_DPRSLPVR
PM_PWRBTN#
PM_PWROK
PM_RI#
PM_RSMRST#
PM_SLP_S1#/GPIO19
PM_SLP_S3#
PM_SLP_S5#
PM_STPCPU#/GPIO20
PM_STPPCI#/GPIO18
PM_SUS_CLK
PM_SUS_STAT#
PM_THRM#

PM_GMUXSEL/GPIO23
PM_CPUPERF#/GPIO22
PM_VGATE/VRMPWRGD

AC'97 LINK

AC_BITCLK
AC_RST#
AC_SDATAIN0
AC_SDATAIN1
AC_SDATAOUT
AC_SYNC

LPC Interface

LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_DRQ#0
LPC_DRQ#1
LPC_FRAME#

USB Interface

USB_PP0
USB_PP1
USB_PP2
USB_PP3
USB_PP4
USB_PP5
USB_PN#0
USB_PN#1
USB_PN#2
USB_PN#3
USB_PN#4
USB_PN#5

USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5

USB_LEDA#0/GPIO32
USB_LEDA#1/GPIO33
USB_LEDA#2/GPIO34
USB_LEDA#3/GPIO35
USB_LEDA#4/GPIO36
USB_LEDA#5/GPIO37
USB_LEDG#0/GPIO38
USB_LEDG#1/GPIO39
USB_LEDG#2/GPIO40
USB_LEDG#3/GPIO41
USB_LEDG#4/GPIO42
USB_LEDG#5/GPIO43

USB_RBIAS

UNMASKED GPIO

GPIO_7
GPIO_8
GPIO_12
GPIO_13
GPIO_25
GPIO_27
GPIO_28

IDE BUS

IDE_PDCS1#
IDE_PDCS3#
IDE_SDCS1#
IDE_SDCS3#

IDE_PDA0
IDE_PDA1
IDE_PDA2
IDE_SDA0
IDE_SDA1
IDE_SDA2

IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15

IDE_SDD0
IDE_SDD1
IDE_SDD2
IDE_SDD3
IDE_SDD4
IDE_SDD5
IDE_SDD6
IDE_SDD7
IDE_SDD8
IDE_SDD9
IDE_SDD10
IDE_SDD11
IDE_SDD12
IDE_SDD13
IDE_SDD14
IDE_SDD15

IDE_PDDACK#
IDE_SDDACK#
IDE_PDDREQ
IDE_SDDREQ
IDE_PDIOR#
IDE_SDIOR#
IDE_PDIOW#
IDE_SDIOW#
IDE_PIORDY
IDE_SIORDY

CLK_14
CLK_48
RTCRST#
CLK_RTCX1
CLK_RTCX2
CLK_VBIAS

SPKR

+3VSB
R486 DUMMY-R3
PM_LANPWROK
BC581 DUMMY-C3
R488 0R3-0-U
LAN_RST# 32
63.R0004.151

+3.3V +3.3V +3VSB
R502 10KR3
R503 10KR3
R498 100KR3
28 COM_RI0#
21 CBUS_RI#
ICH_RI#
Dummy-NC7SZ86

32K suspend clock output

+3VSB
8,11 AGP_BUSY#
RY1 10KR3
63.10334.151
PM_C3_STAT#
21,34 P_CLKRUN#
30 PM_DPRSLPVR
32 PWRBTN#
6 RUNPWROK
ICH_RI#
14 RSMRST#
3 PM_SLP_S3#
TPAD30 TP-33
PM_SLP_S1#
PM_SLP_S3#
PM_SLP_S5#
3 PM_STPCPU#
3 PM_STPPCI#
PM_SUSCLK
11,26 PM_SUS_STAT#
THRM#_1

6 THRM#
R479 0R2-0
THRM#

23 ICH_AC_BITCLK
R455 DUMMY-R3

30 ICH_GMUXSEL
4 PM_CPUPERF
30 VCORE_PWRGD

19,23 ICH_AC_RST#
23 ICH_AC_DIN0
19 ICH_AC_DIN1
19,23 ICH_AC_DOUT
R451 33R3
R453 33R3
AC_SYNC
19,23 ICH_AC_SYNC
R454 33R3

LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
26,27,29 LPC_LAD[0..3]
27 LPC_LDRQ#0
LPC_LDRQ#1
26,27,29 LPC_LFRAME#

19 USBP0P
19 USBP3P
USBP5P
19 USBP0N
19 USBP3N
USBP5N

USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
BLTH_USB_OC#

EEPWP#
29 FWH_WP#
FWH_WP#
BLTH_RST#
BLTH_EN#
BLTH_PWCTL

14 BACKLT_OFF#
32 CHRG_OFF
6 HWTHRM_EN#
3 DK_CLKON#
35 DK_SUS#
34,35 DK_PCIRST#
BACKLT_OFF#
CHRG_OFF
HWTHRM_EN#
DK_CLKON#
DK_SUS#
DK_PCIRST#

R433 18K2R3F

23 ICH_SPKR

3 CLK48_ICH
3 CLK14_ICH
CLK14_ICH
CLK48_ICH

R446 10R3
R445 10R3
BC529 SC10P
BC530 SC10P

CLK termination close to ICH

RTCRST# 14
RTCX1 14
RTCX2 14
ICH_VBIAS 14

ECSMI 26
ECSWI 26
ECSCI 26
BAT_RTC_WK# 32
DK_PWRON
DK_PWRON 34

+3VSB
R487 8K2R3
R481 8K2R3
MPCIACT#

IDE_PDCS1# PIDE_CS1# 18
IDE_PDCS3# PIDE_CS3# 18
IDE_SDCS1# SIDE_CS1# 18
IDE_SDCS3# SIDE_CS3# 18

IDE_PDA0 PIDE_A0
IDE_PDA1 PIDE_A1
IDE_PDA2 PIDE_A2
IDE_SDA0 SIDE_A0
IDE_SDA1 SIDE_A1
IDE_SDA2 SIDE_A2

IDE_PDD0 PIDE_D0
IDE_PDD1 PIDE_D1
IDE_PDD2 PIDE_D2
IDE_PDD3 PIDE_D3
IDE_PDD4 PIDE_D4
IDE_PDD5 PIDE_D5
IDE_PDD6 PIDE_D6
IDE_PDD7 PIDE_D7
IDE_PDD8 PIDE_D8
IDE_PDD9 PIDE_D9
IDE_PDD10 PIDE_D10
IDE_PDD11 PIDE_D11
IDE_PDD12 PIDE_D12
IDE_PDD13 PIDE_D13
IDE_PDD14 PIDE_D14
IDE_PDD15 PIDE_D15

IDE_SDD0 SIDE_D0
IDE_SDD1 SIDE_D1
IDE_SDD2 SIDE_D2
IDE_SDD3 SIDE_D3
IDE_SDD4 SIDE_D4
IDE_SDD5 SIDE_D5
IDE_SDD6 SIDE_D6
IDE_SDD7 SIDE_D7
IDE_SDD8 SIDE_D8
IDE_SDD9 SIDE_D9
IDE_SDD10 SIDE_D10
IDE_SDD11 SIDE_D11
IDE_SDD12 SIDE_D12
IDE_SDD13 SIDE_D13
IDE_SDD14 SIDE_D14
IDE_SDD15 SIDE_D15

PIDE_D[0..15] 18
PIDE_A[0..2] 18
SIDE_D[0..15] 18
SIDE_A[0..2] 18

IDE_PDDACK# PIDE_DACK# 18
IDE_SDDACK# SIDE_DACK# 18
IDE_PDDREQ PIDE_DREQ 18
IDE_SDDREQ SIDE_DREQ 18
IDE_PDIOR# PIDE_IOR# 18
IDE_SDIOR# SIDE_IOR# 18
IDE_PDIOW# PIDE_IOW# 18
IDE_SDIOW# SIDE_IOW# 18
IDE_PIORDY PIDE_IORDY 18
IDE_SIORDY SIDE_IORDY 18

AC97 AC terminations

ICH_AC_BITCLK
ICH_AC_DIN0
ICH_AC_DIN1
R457 DUMMY-R3
R450 DUMMY-R3
R439 DUMMY-R3
BC540 DUMMY-C3
BC539 DUMMY-C3
BC536 DUMMY-C3

FPET7 Elec. P3-54

+3.3V
R511 4K7R3
PIDE_IORDY 2
R512 4K7R3
SIDE_IORDY 2

LPC I/F PULLL-UPs

+3.3V
RN30 SRN10K-2
LPC_LAD2
LPC_LAD1
LPC_LAD3
LPC_LAD0
22,1033,06A
No Stuff

KAHUNA SPEC. LPC47N252ENG.PDF
P22 NOTE.24

+3.3V
R476 DUMMY-R3 10KR3 LPC_LDRQ#0
R480 DUMMY-R3 10KR3 LPC_LDRQ#1

LPC_LDRQ#0, 1 have weak internal pullups

+3.3V
RN20 SRN10K-2
THRM# 1
USB_OC#0
USB_OC#3
EEPWP#

RN24 SRN10K-2
USB_OC#4
USB_OC#1
USB_OC#2
BLTH_USB_OC#

RN19 SRN10K-2
USBP5P
USBP5N

RN23 SRN10K-2
BLTH_RST#
BLTH_EN#
BLTH_PWCTL

Almador checklist ver. 0.5

SB

Kodiak Ver. 0.7b

ICH3 Integrated Pull-up and Pull-down Resistors

EE_DIN , EE_DOUT , LDRQ[1:0] , PME# GNT[B:A]#/GNT[5]#/GPIO[17:16] , LAD[3:0]#/FWH[3:0]# , PWRBTN#	ICH3 internal 24K pull-ups
LAN_RXD[2:0]	ICH3 internal 9K pull-ups
AC_BITCLK, AC_SDIN[0], AC_SDOUT, AC_SDIN[1]/GPIO[9], AC_SYNC,	ICH3 internal 20K pull-downs
SPKR	ICH3 internal 24K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ	ICH3 internal 5.9K pull-downs
DPRSLPVR	ICH3 internal TBD K pull-downs

FM-1882 P4-1,2

+3.3V
R490 10KR3
P_CLKRUN#

H/W Strapping

1KR3
+3.3V
ICH_SPKR
R465 DUMMY-R3
ICH_AC_DOUT
R452 DUMMY-R3

Kodiak V. 0.7b P.19

+3.3V
U57
OE#
A
GND
VCC
Y
NC7SZ125
PM_SUSCLK
32KHZ
R499 10R3 G768_32K 6
R506 10R3 OZ998_32K 26
R496 10R3 OZ711_32K 21
R494 10R3 OZSW_32K 22

+3.3V
PM_SLP_S5#
R500 10KR2
BC589 DUMMY-C3

+3VSB
U59C
PM_SLP_S5#
PM_SLP_S5# 32
PM_SLP_S5 32
TSAHC14

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21F, 88, Sec. 1, Hsin Tai Wu Rd.,
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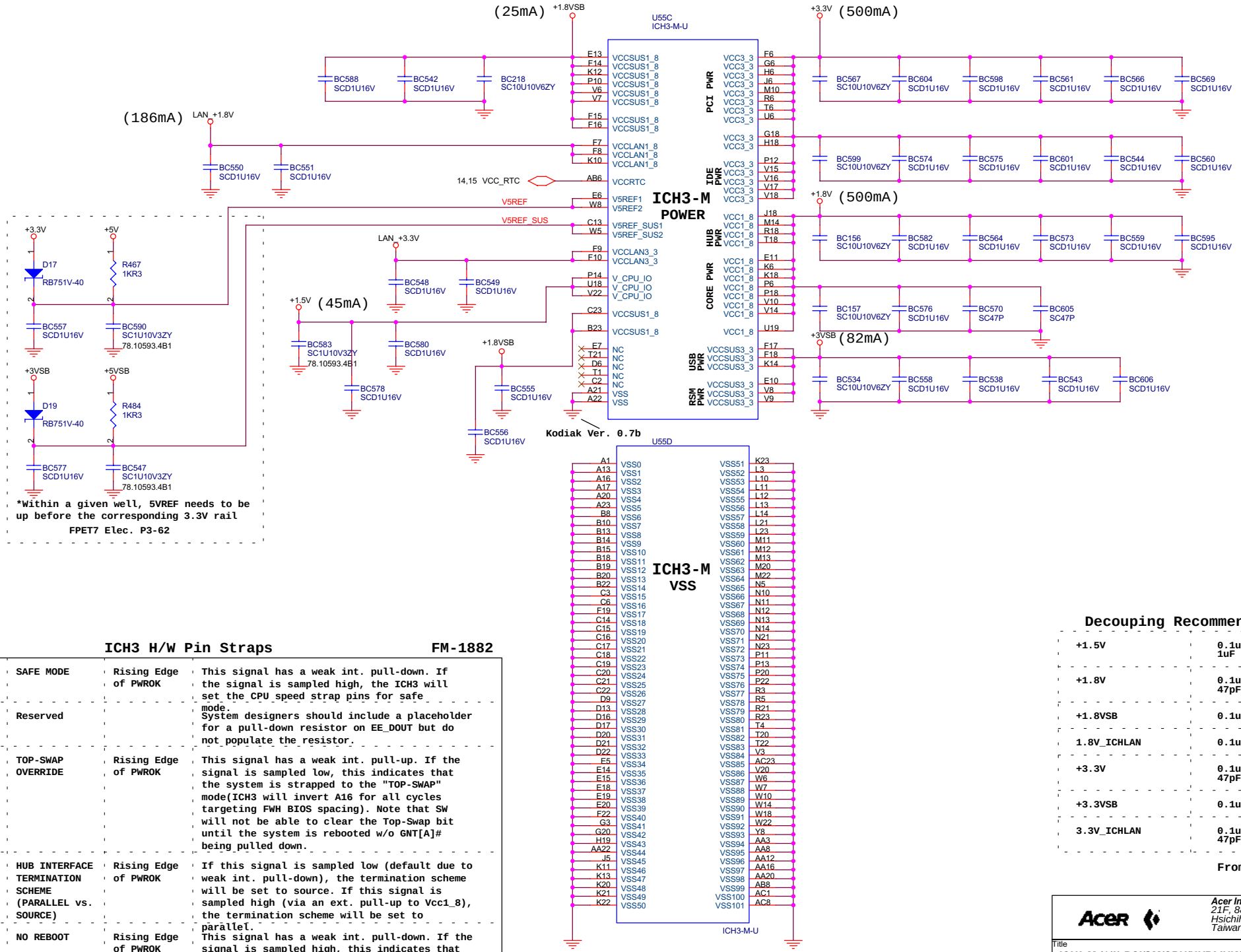
Taiwan, R.O.C.

Title: ICH3-M (2/3) PM,USB,AC'97,LPC,IDE,RTC

Size: A3 | Document Number: Acer Flmanigo | Rev: SB

Date: Friday, July 13, 2001 | Sheet 16 of 38



ICH3 H/W Pin Straps

FM-1882

AC_SDOUT	SAFE MODE	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, the ICH3 will set the CPU speed strap pins for safe mode.
EE_DOUT	Reserved		System designers should include a placeholder for a pull-down resistor on EE_DOUT but do not populate the resistor.
GNT[A]#	TOP-SWAP OVERRIDE	Rising Edge of PWROK	This signal has a weak int. pull-up. If the signal is sampled low, this indicates that the system is strapped to the "TOP-SWAP" mode(ICH3 will invert A16 for all cycles targeting FWH BIOS spacing). Note that SW will not be able to clear the Top-Swap bit until the system is rebooted w/o GNT[A]# being pulled down.
DPRSLPVR	HUB INTERFACE TERMINATION SCHEME (PARALLEL vs. SOURCE)	Rising Edge of PWROK	If this signal is sampled low (default due to weak int. pull-down), the termination scheme will be set to source. If this signal is sampled high (via an ext. pull-up to Vcc1_8), the termination scheme will be set to parallel.
SPKR	NO REBOOT	Rising Edge of PWROK	This signal has a weak int. pull-down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot " mode (ICH3 will disable the TXO Timer system reboot feature).

Decouping Recommendation

+1.5V	0.1uF * 2 1uF / 16V * 1
+1.8V	0.1uF * 5 47pF * 2
+1.8VSB	0.1uF * 3
1.8V_ICHLAN	0.1uF * 2
+3.3V	0.1uF * 13 47pF * 5
+3.3VSB	0.1uF * 8
3.3V_ICHLAN	0.1uF * 2 47pF * 1

From Kris 8/10

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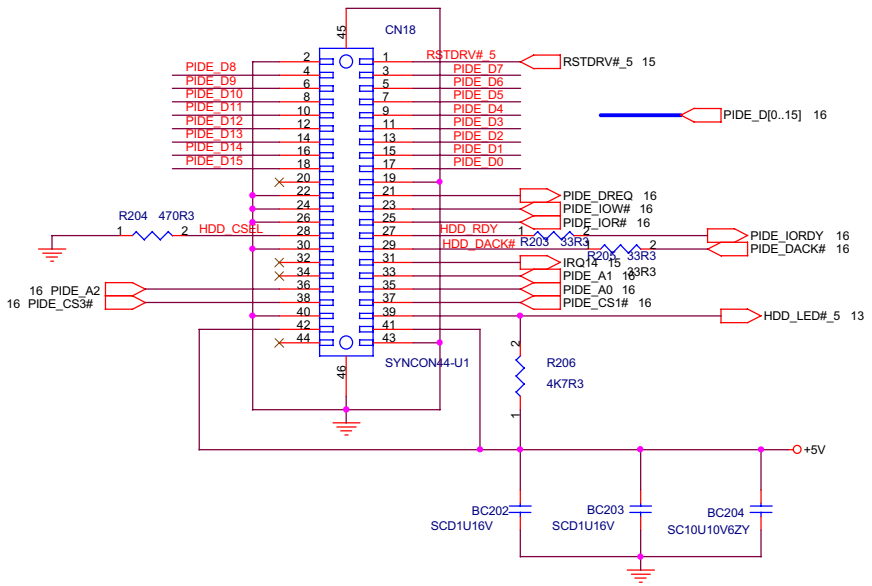
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title: ICH3-M (1/3) PCI/SM/CPU/HUBLINK/INT/EEPROM/LAN I/F

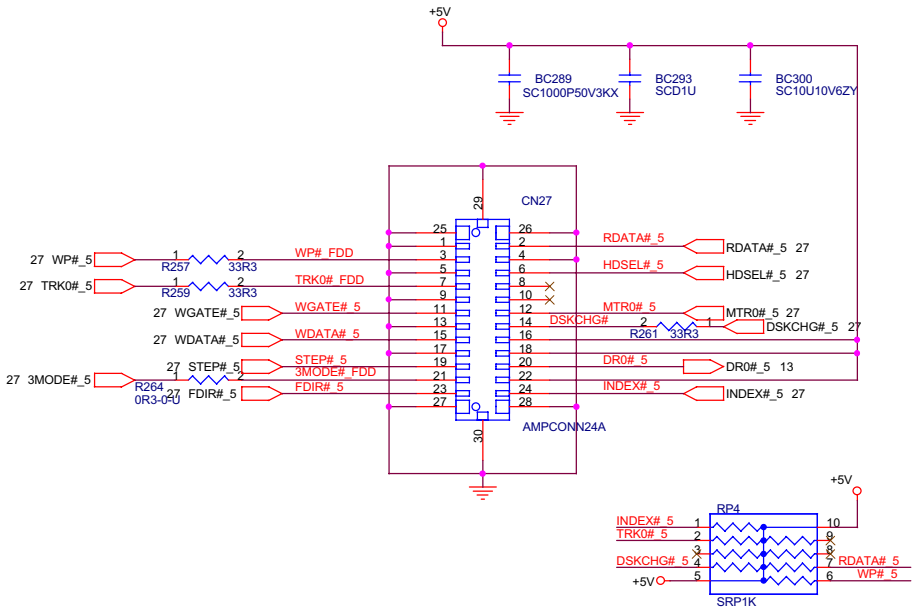
Size: A3 | Document Number: Acer FImanigo | Rev: SB

Date: Friday, July 13, 2001 | Sheet 17 of 38

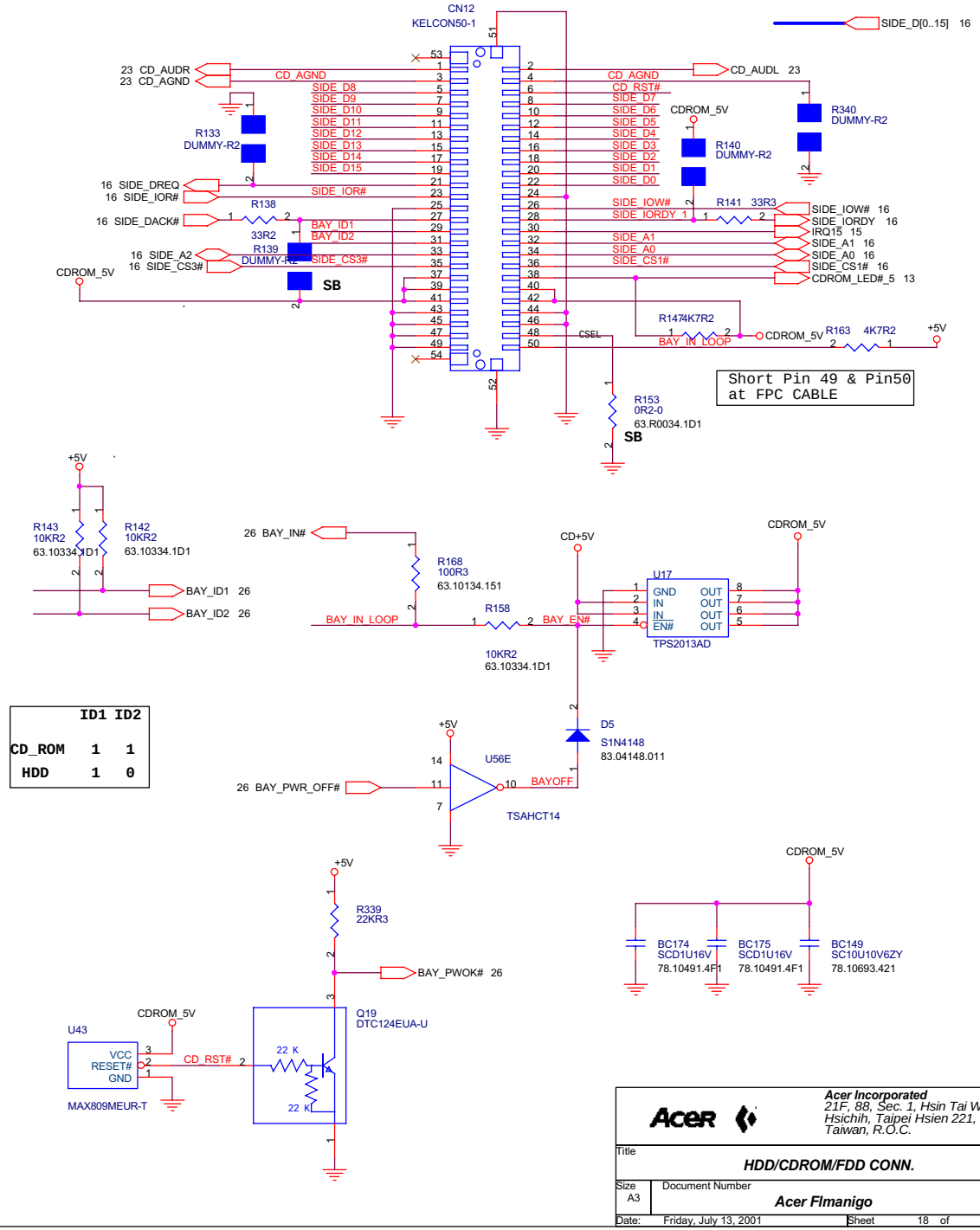
HDD



FDD



CDROM



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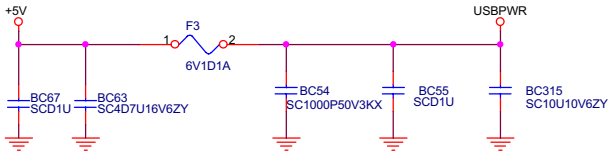
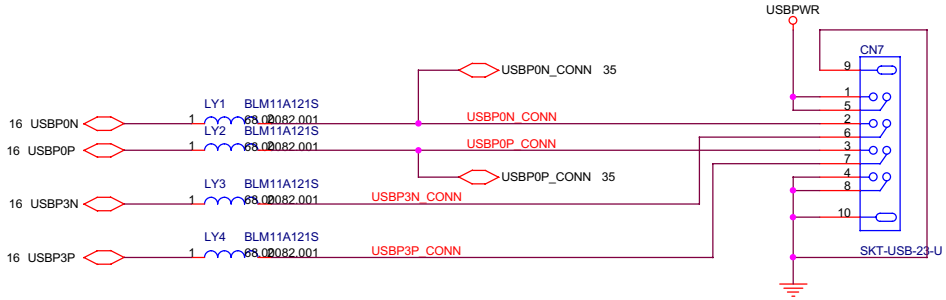
Taiwan, R.O.C.

Title	HDD/CDROM/FDD CONN.	
Size A3	Document Number: Acer FImanigo	Rev SB
Date: Friday, July 13, 2001	Sheet 18 of 38	

USB Common mode choke
MURATA
PLW3216S900SQ2

Filtering RC network located near ICH3-M
FPET7 Elec. P3-14

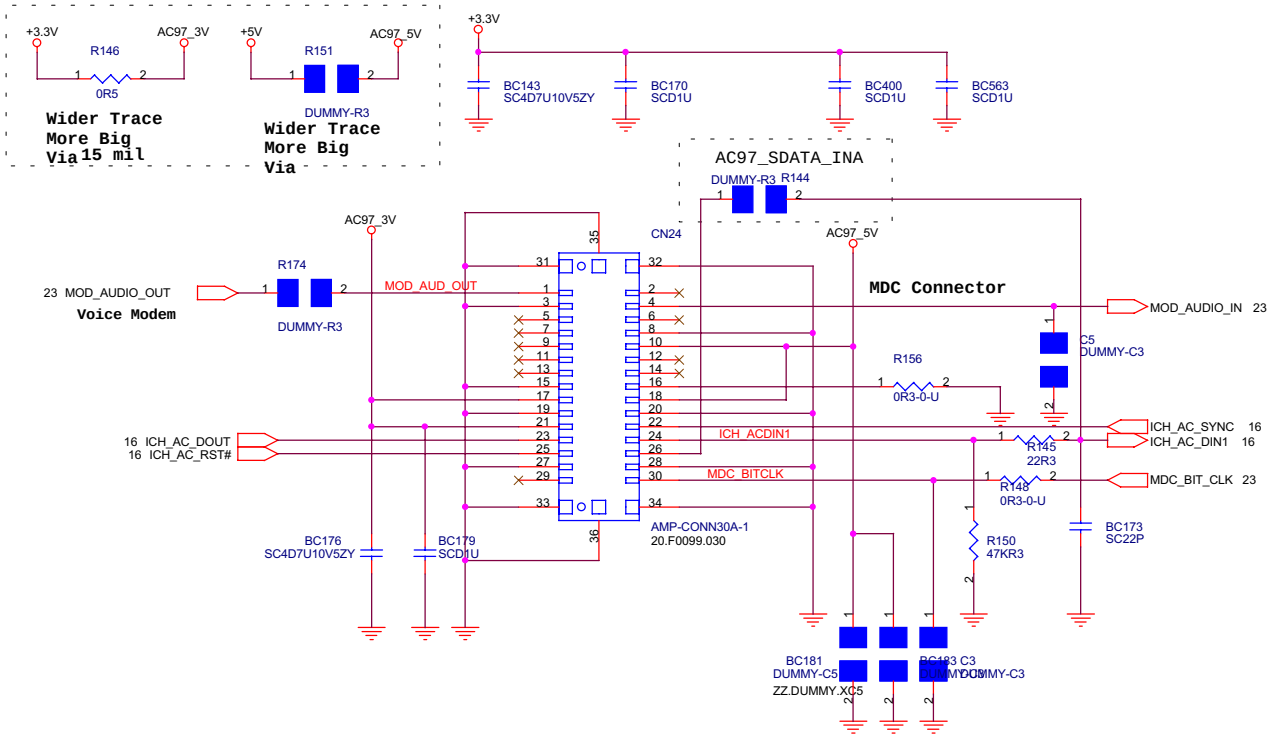




Filtering RC network located near ICH3-M
FPET7 Elec. P3-14

USB Common mode choke
MURATA
PLW3216S900SQ2

MDC



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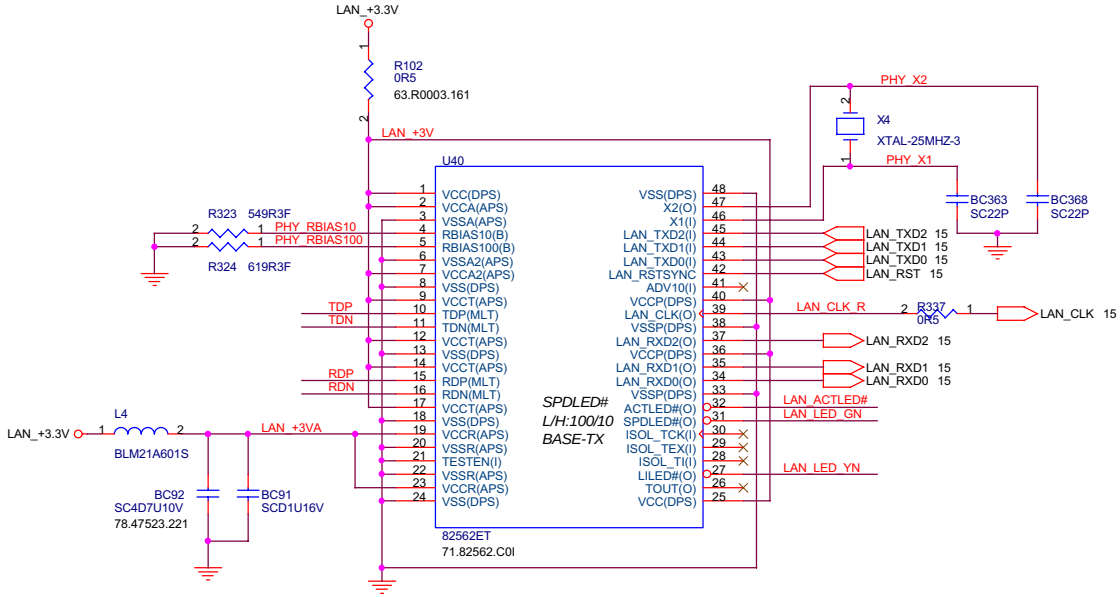
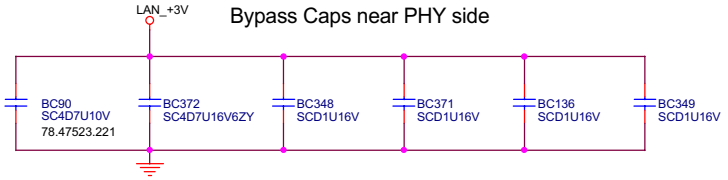
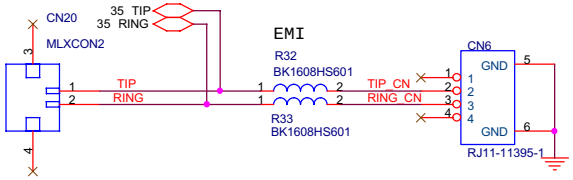
Title: **USB / MDC CONN.**

Size	Document Number	Rev
A3	Acer FImanigo	SB

Date: Friday, July 13, 2001 Sheet 19 of 38



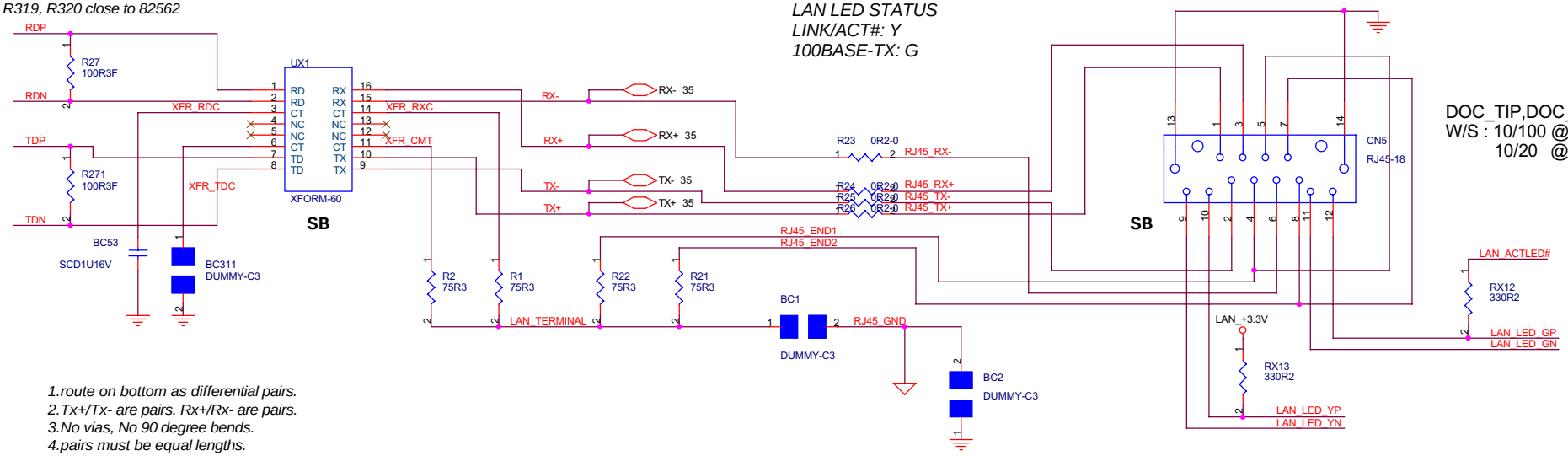




Use 50 ohm trace

R319, R320 close to 82562

LAN LED STATUS
LINK/ACT#: Y
100BASE-TX: G



DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

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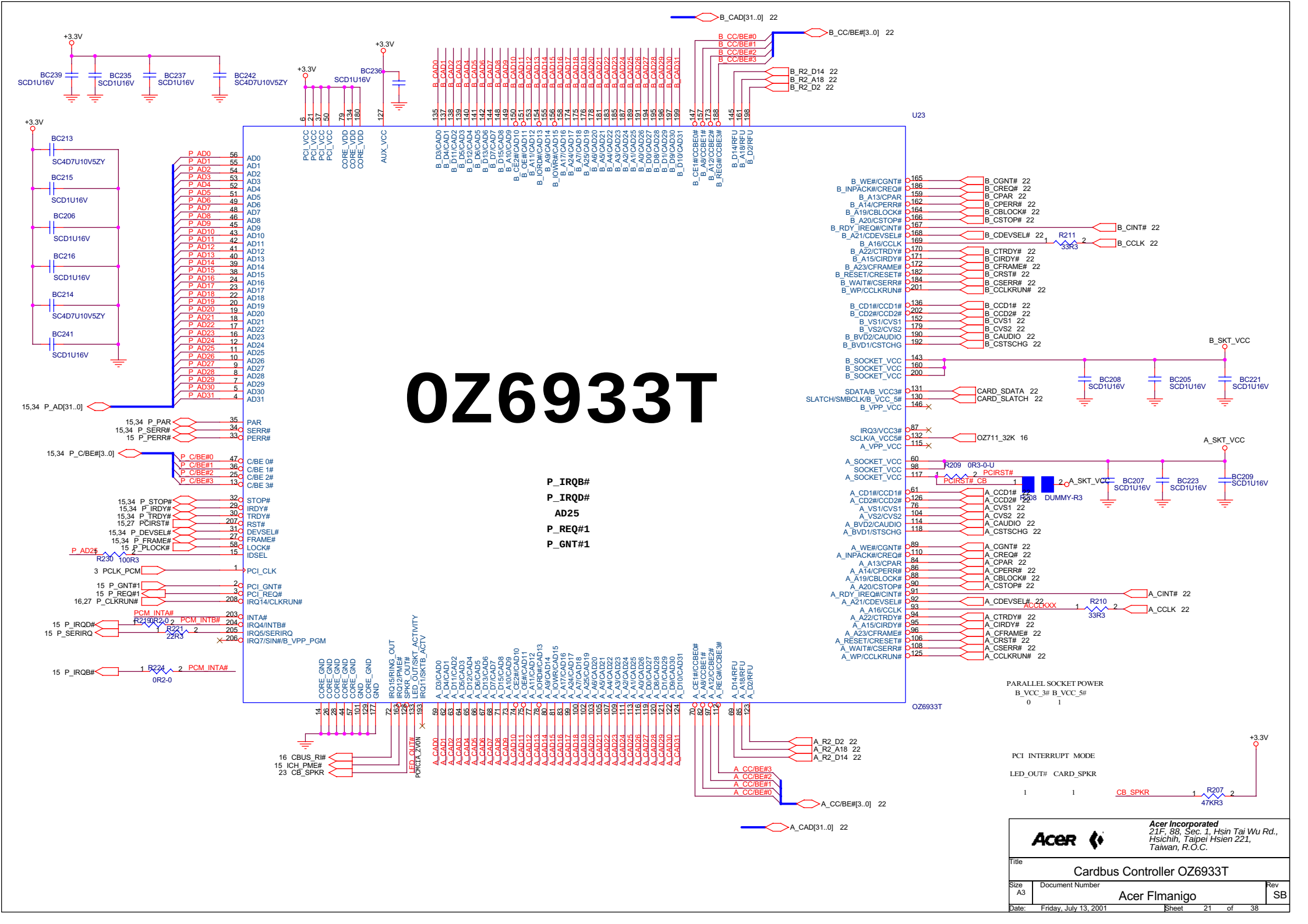
Title	LAN	
Size A3	Document Number Acer FImanigo	Rev SB
Date: Friday, July 13, 2001	Sheet 20 of 38	


OZ6933T
P_IRQB#
P_IRQD#
AD25
P_REQ#1
P_GNT#1
U23
OZ6933T
B_CAD[31..0] 22
B_CC/BE#[3..0] 22
A_CAD[31..0] 22
A_CC/BE#[3..0] 22
15,34 P_AD[31..0]
15,34 P_C/BE#[3..0]
PARALLEL SOCKET POWER
B_VCC_3# B_VCC_5#
0 1
PCI INTERRUPT MODE
LED_OUT# CARD_SPKR
1 1
CB_SPKR
R207
47KR3
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd.,
Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.
Title
Cardbus Controller OZ6933T
Size A3
Document Number
Acer FImanigo
Rev SB
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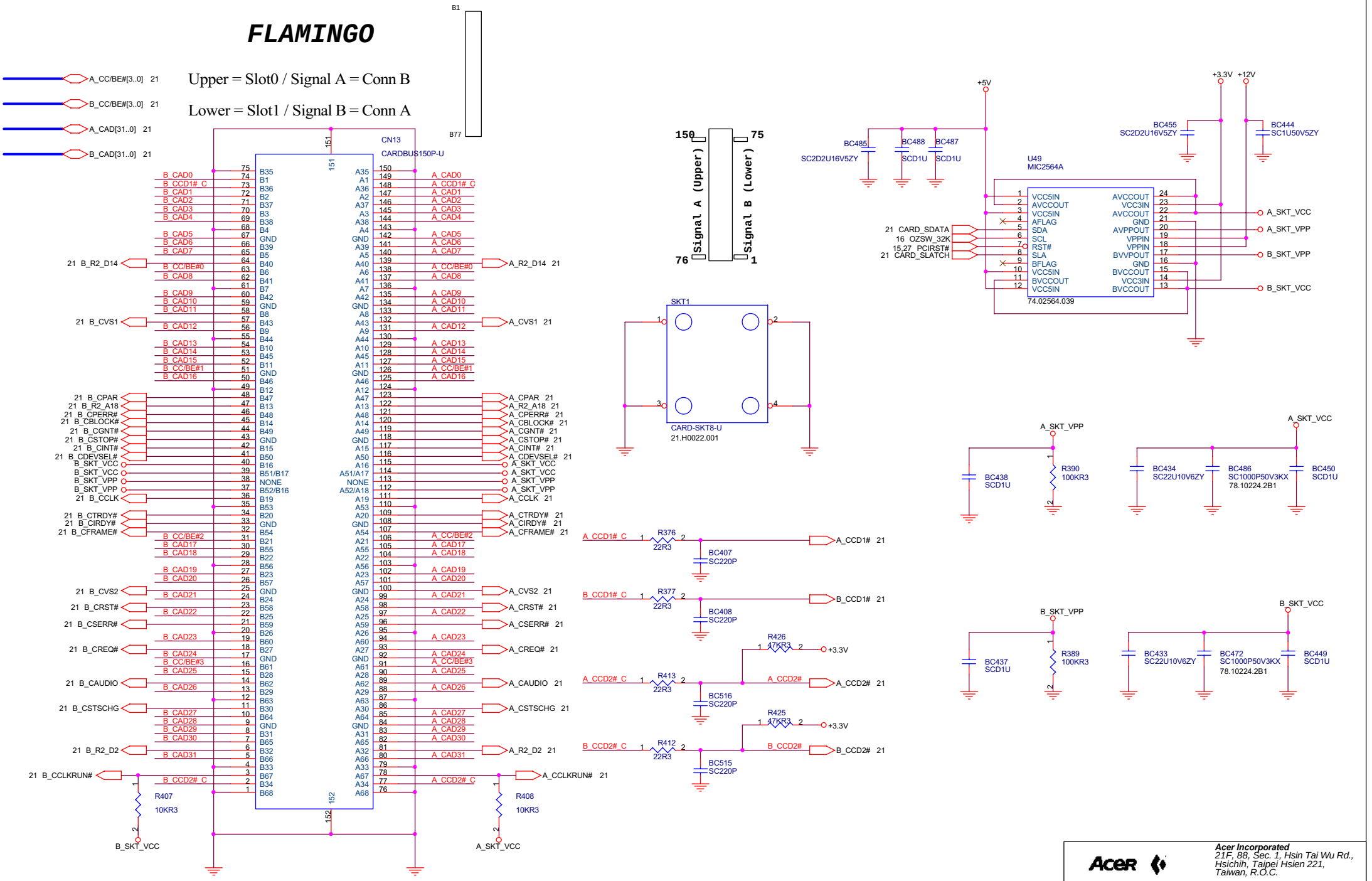
FLAMINGO

Upper = Slot0 / Signal A = Conn B

Lower = Slot1 / Signal B = Conn A



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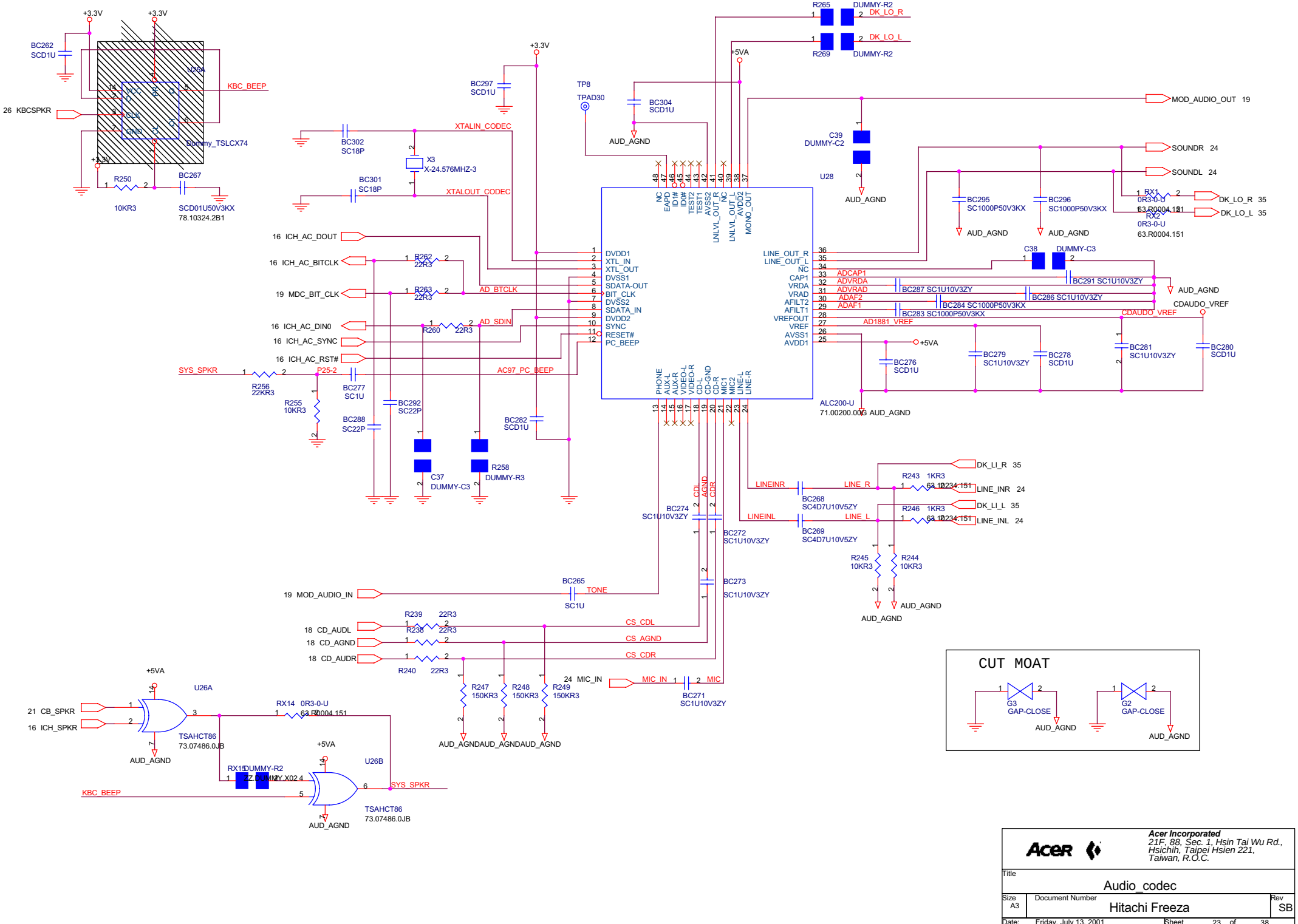
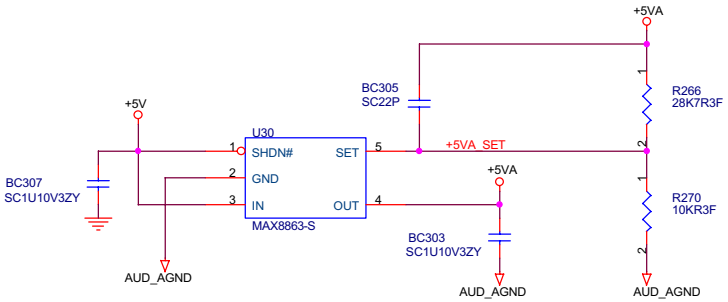
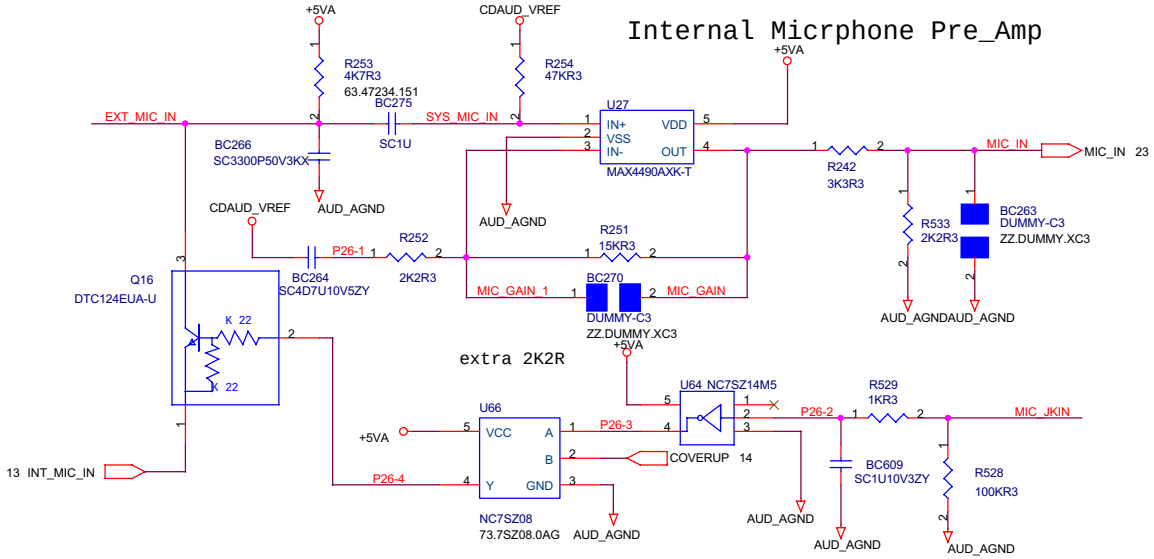
Taiwan, R.O.C.

Title	Cardbus Connector/Power SW	
Size: A3	Document Number: Acer Flmanigo	Rev: SB
Date: Friday, July 13, 2001	Sheet 22 of 38	



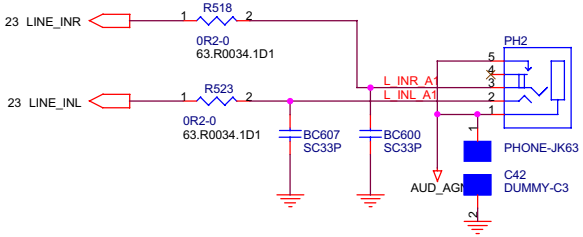
Acer Incorporated	21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Audio_codec
Size	A3
Document Number	Hitachi Freeza
Rev	SB
Date:	Friday, July 13, 2001
Sheet	23 of 38



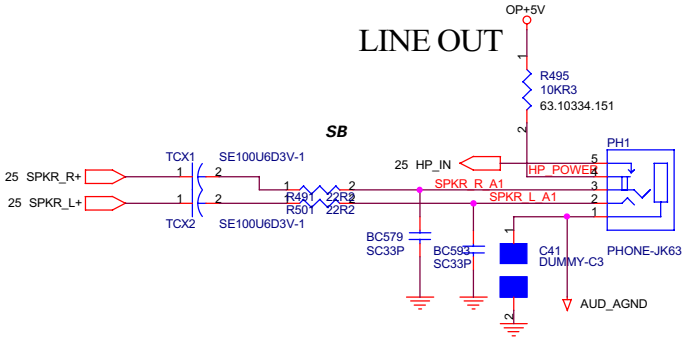


Reserve for Special Request When LCD Off, Int Mic turn off

LINE IN

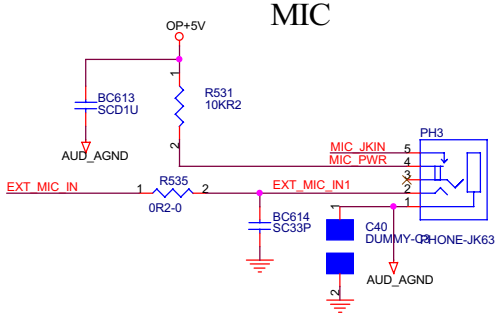


LINE OUT

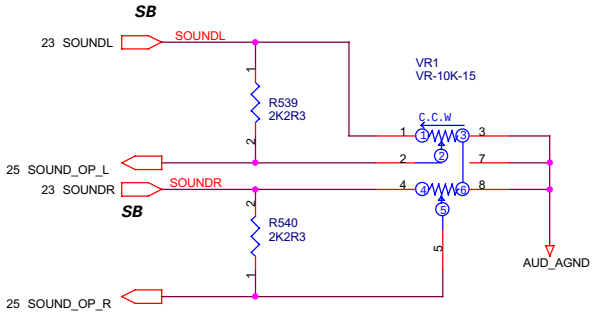


All 33pF capacitors are used for EMI concern

MIC



VR



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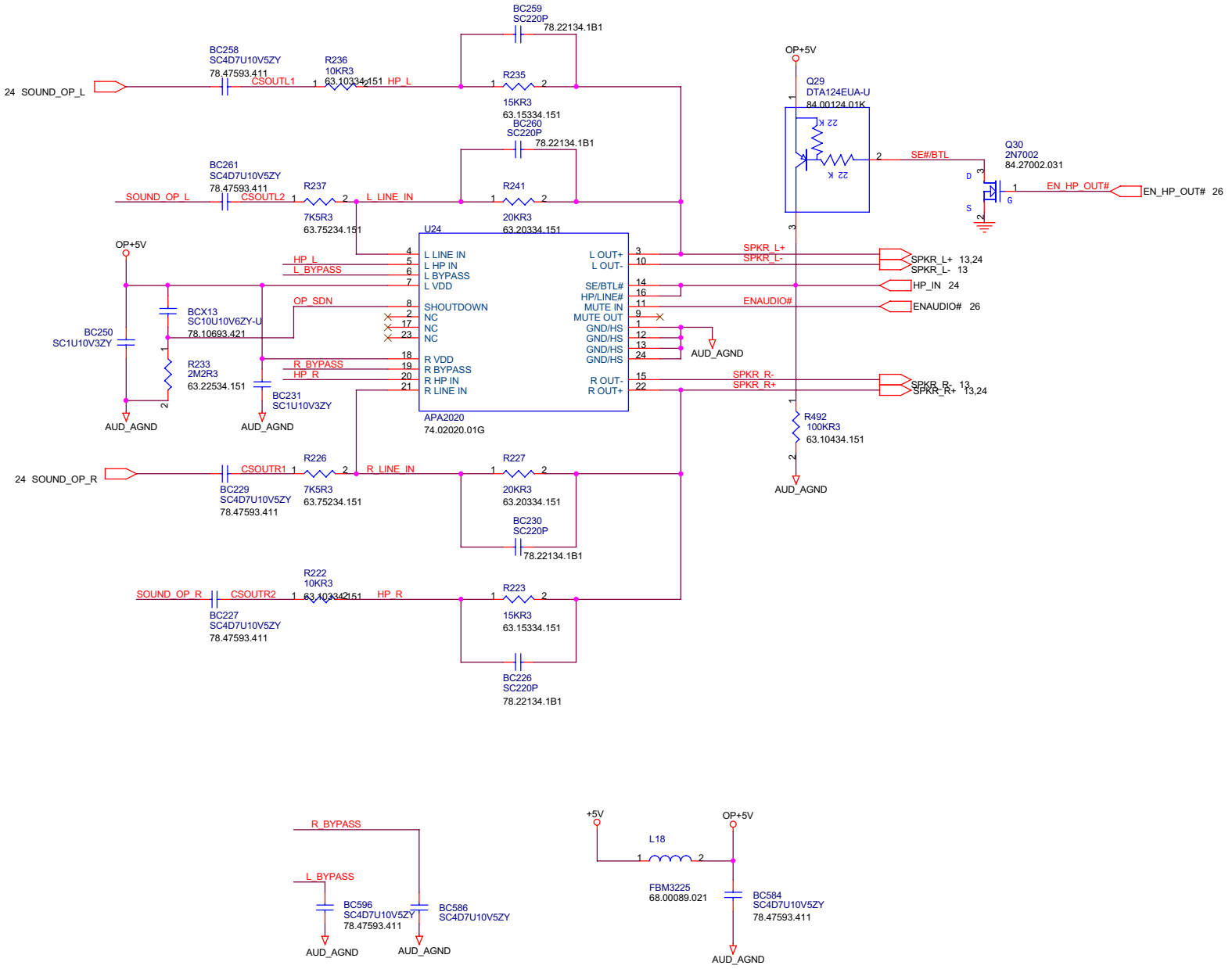
Title	CD AUDIO SWITCH	
Size A3	Document Number Acer Flamingo	Rev SB
Date: Friday, July 13, 2001	Sheet 24 of 38	



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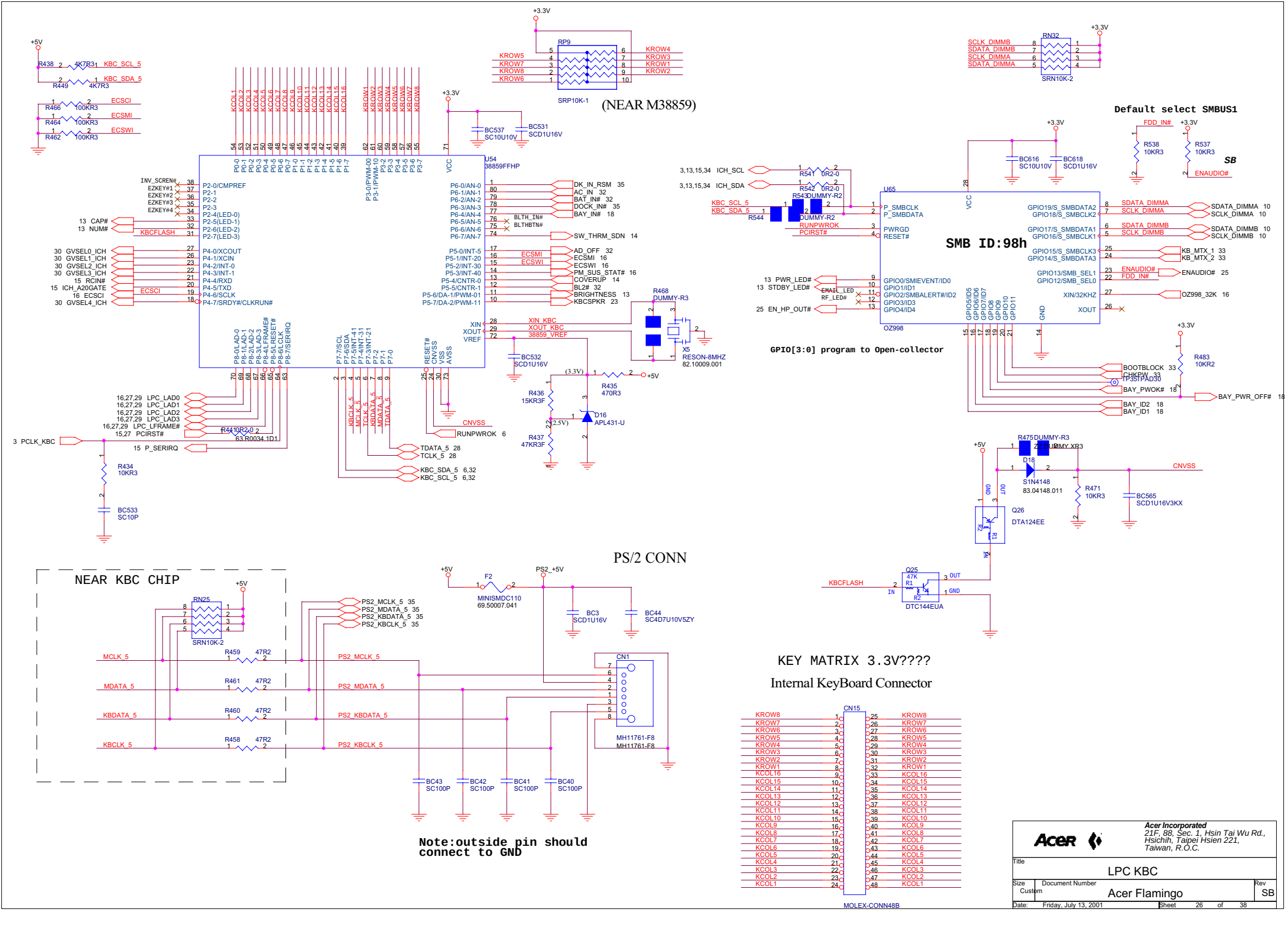
Taiwan, R.O.C.

Title	LINE_IN, LINE_OUT, MIC	
Size A3	Document Number: Acer Flamingo	Rev SB
Date: Friday, July 13, 2001	Sheet 25 of 38	


(NEAR M38859)
Default select SMBUS1
SB
SMB ID:98h
GPIO[3:0] program to Open-collector
PS/2 CONN
NEAR KBC CHIP
KEY MATRIX 3.3V????
Internal KeyBoard Connector
Note:outside pin should connect to GND
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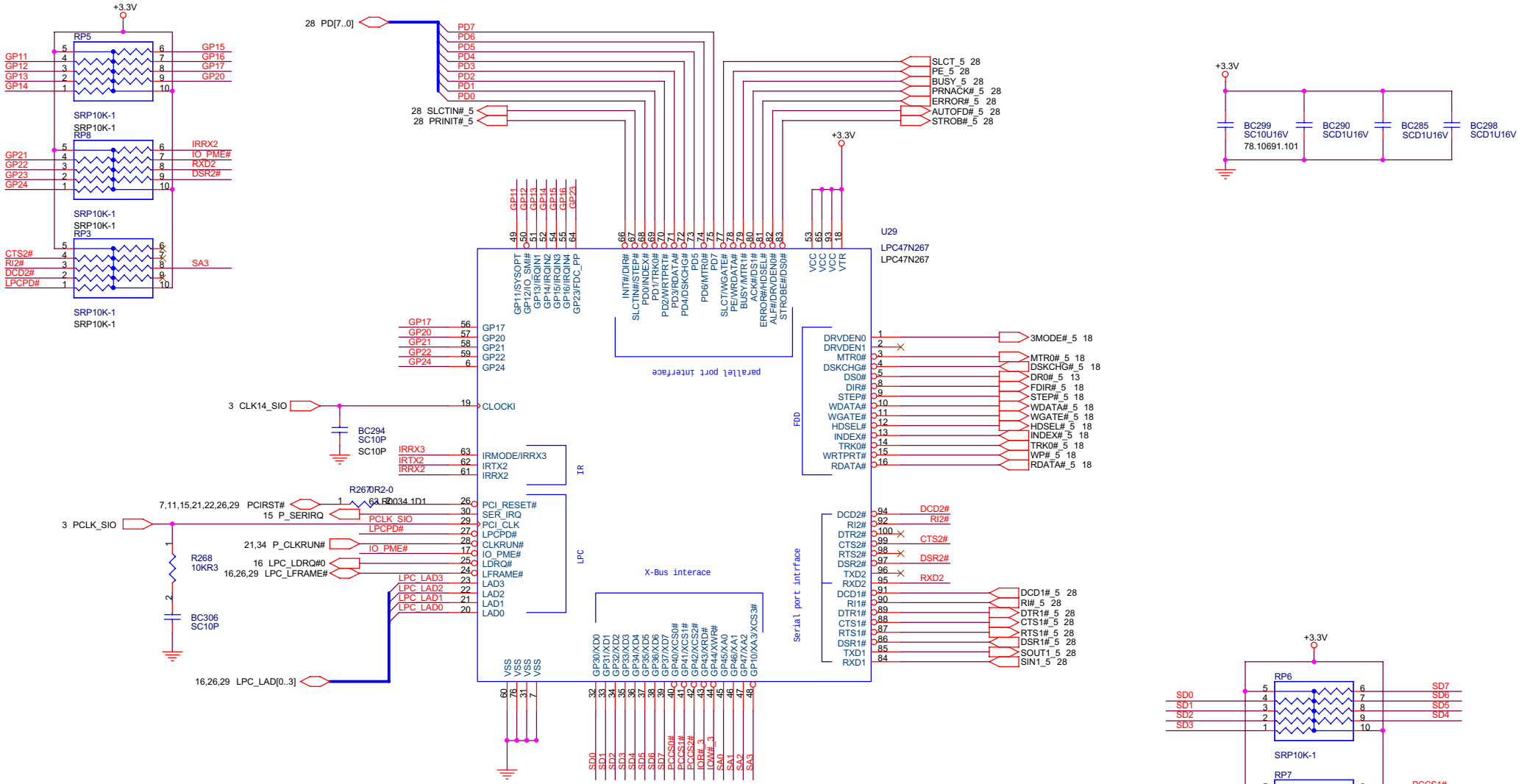
Title
LPC KBC
Size
Custom
Document Number
Acer Flamingo
Rev
SB
Date: Friday, July 13, 2001
Sheet 26 of 38



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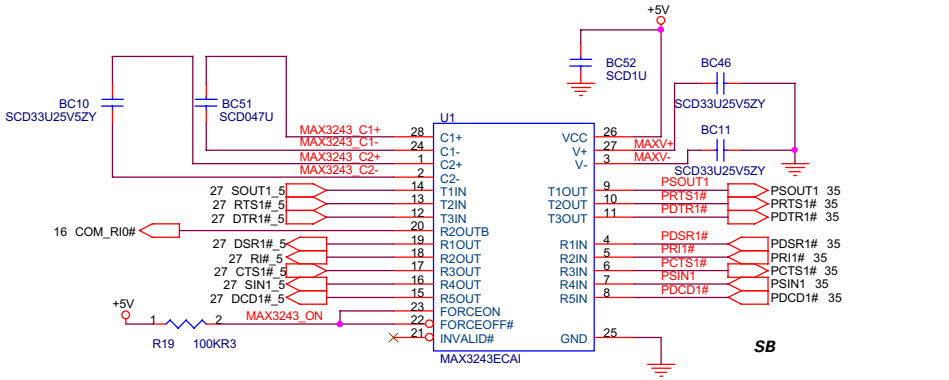
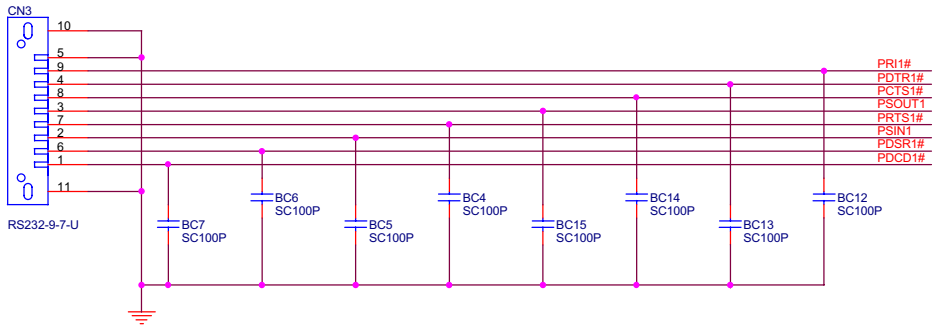
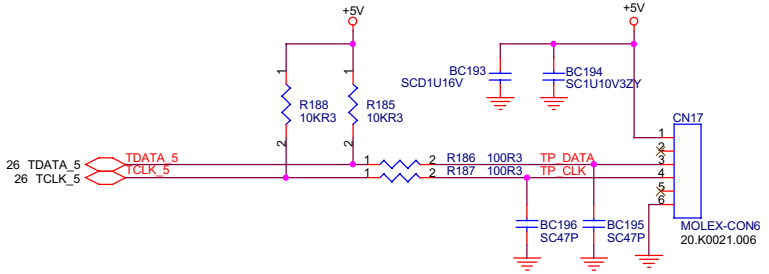
Title	LPC SIO	
Size A3	Document Number: Acer Flamingo	Rev SB
Date: Friday, July 13, 2001	Sheet 27 of 38	

SERIAL PORT

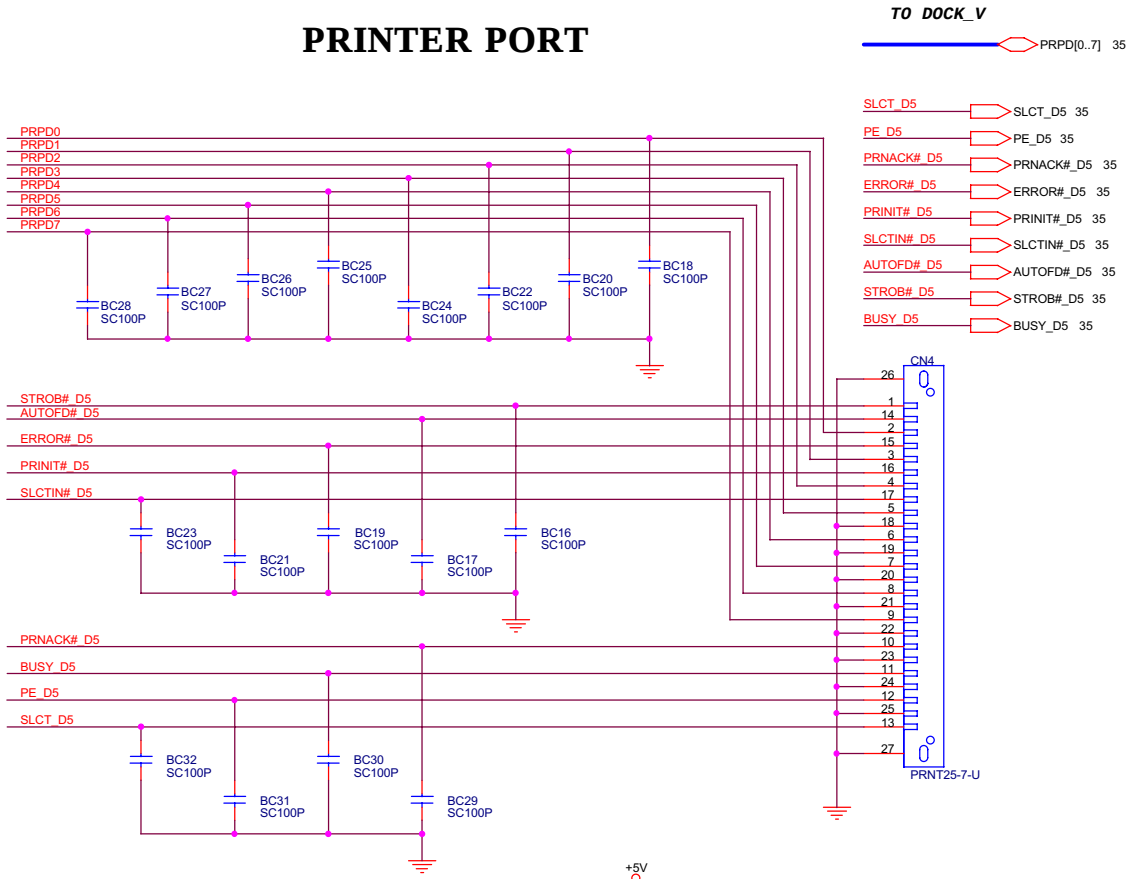


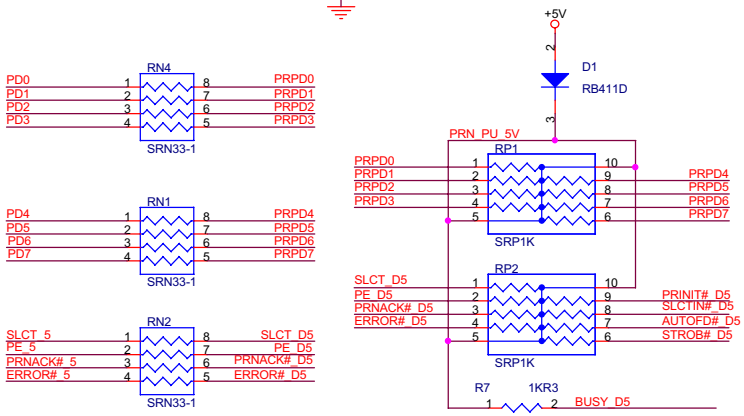


TOUCH PAD

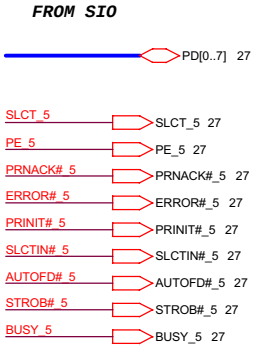


PRINTER PORT





CHECK PULL HIGH



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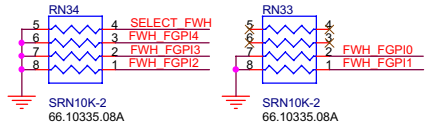
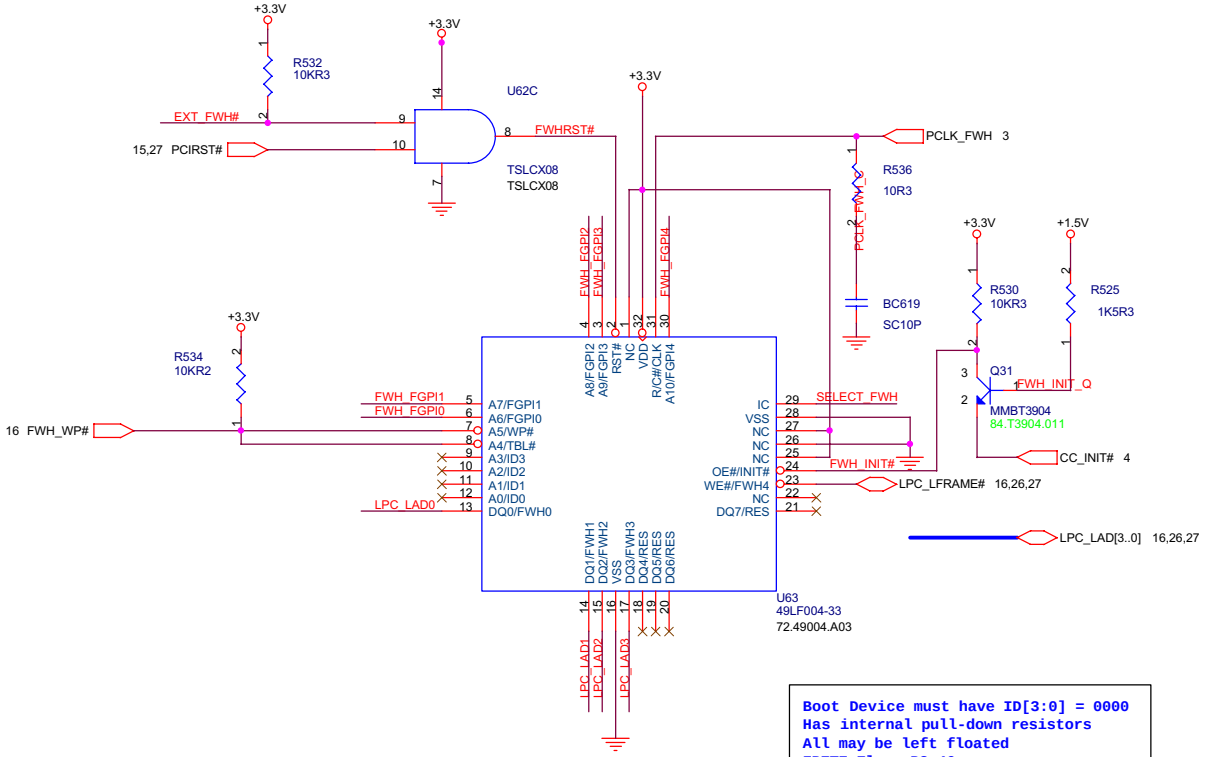
Title	Serial, Parallel Port	
Size A3	Document Number: Acer Flamingo	Rev SB
Date: Friday, July 13, 2001	Sheet 28 of 38	

Unused FGPI pins must not be float





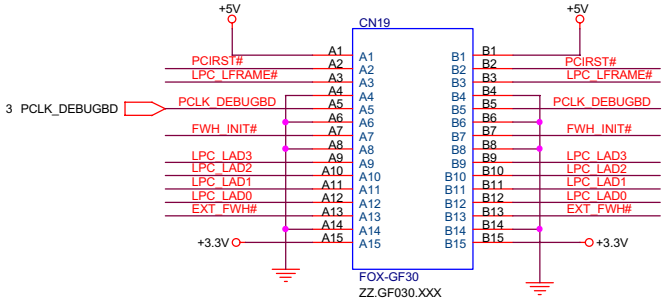
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

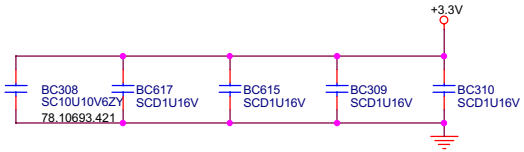
TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD





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Title: **FIRMWARE HUB & DEBUG PORT**

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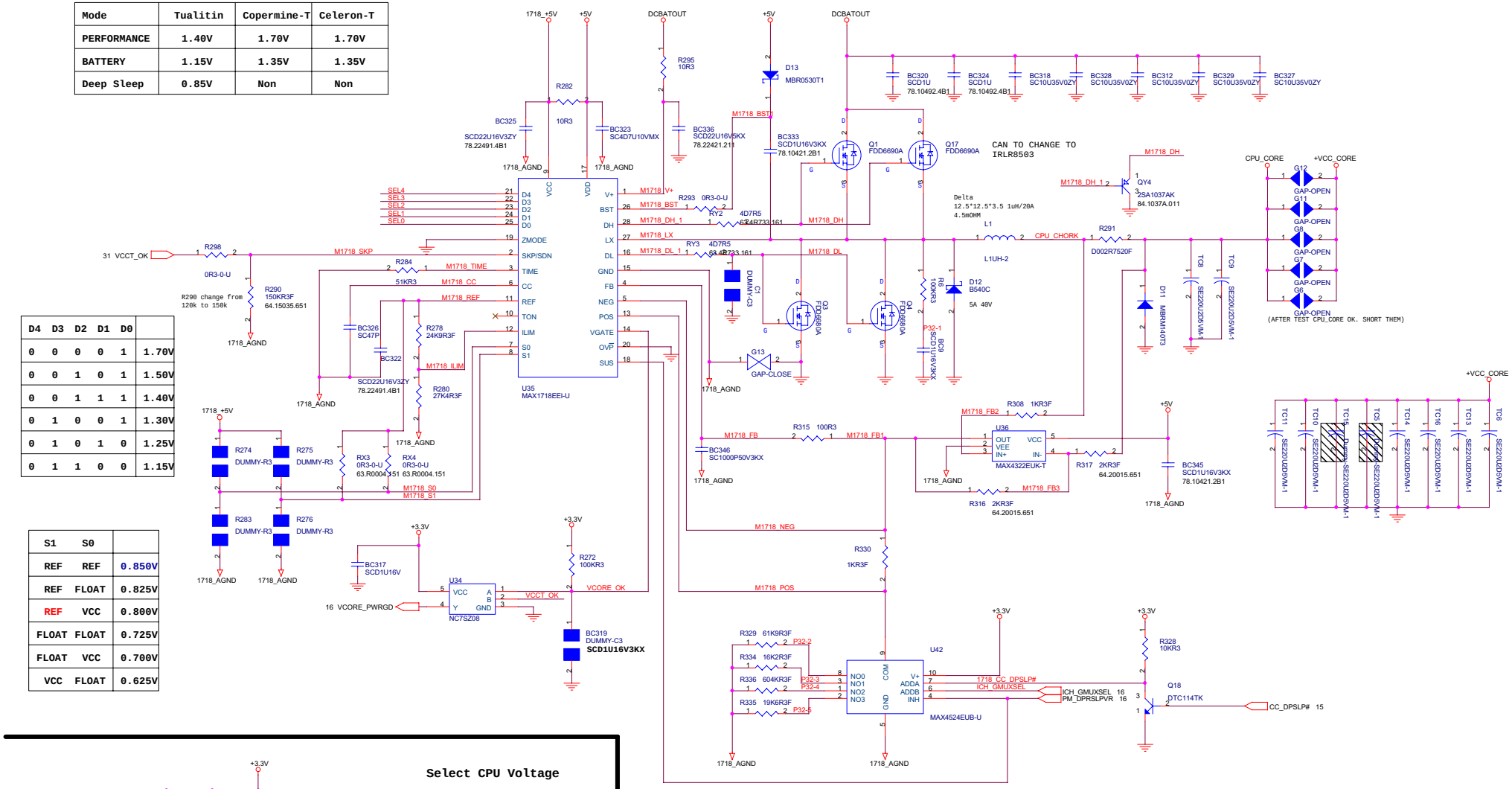
A3	Acer Flamingo	SB

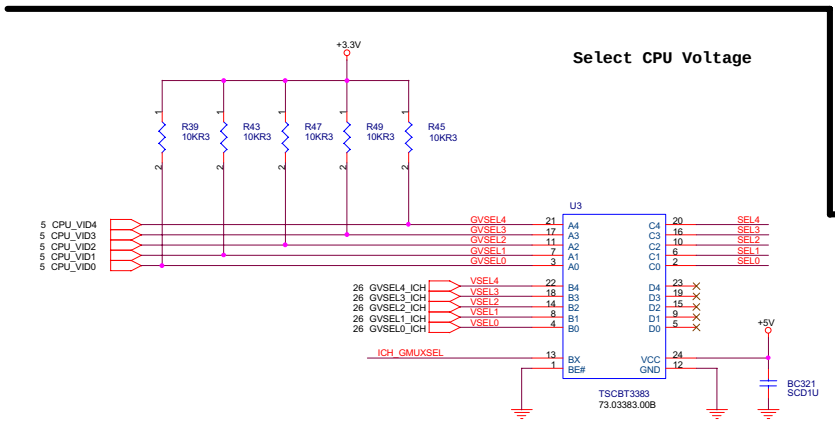
Date: Friday, July 13, 2001 Sheet 29 of 38

Mode	Tualitin	Copermine-T	Celeron-T
PERFORMANCE	1.40V	1.70V	1.70V
BATTERY	1.15V	1.35V	1.35V
Deep Sleep	0.85V	Non	Non

D4	D3	D2	D1	D0	
0	0	0	0	1	1.70V
0	0	1	0	1	1.50V
0	0	1	1	1	1.40V
0	1	0	0	1	1.30V
0	1	0	1	0	1.25V
0	1	1	0	0	1.15V

S1	S0	
REF	REF	0.850V
REF	FLOAT	0.825V
REF	VCC	0.800V
FLOAT	FLOAT	0.725V
FLOAT	VCC	0.700V
VCC	FLOAT	0.625V





TRUE TABLE

BE#	BX	A0~A4	B0~B4
H	X	HIGH-Z	HIGH-Z
L	L	C0~C4	D0~D4
L	H	D0~D4	C0~C4

Offset Truth Table

PM_DPRSLPVR	CC_DPSLP#	ICH_GMUXSEL	Voffset
1	X	X	0mV
0	0	0	-59mV
0	0	1	-52mV
0	1	0	-29mV
0	1	1	-3mV

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Title: **CPU VCORE**

Size: Custom | Document Number: Acer Flamingo | Rev: SB

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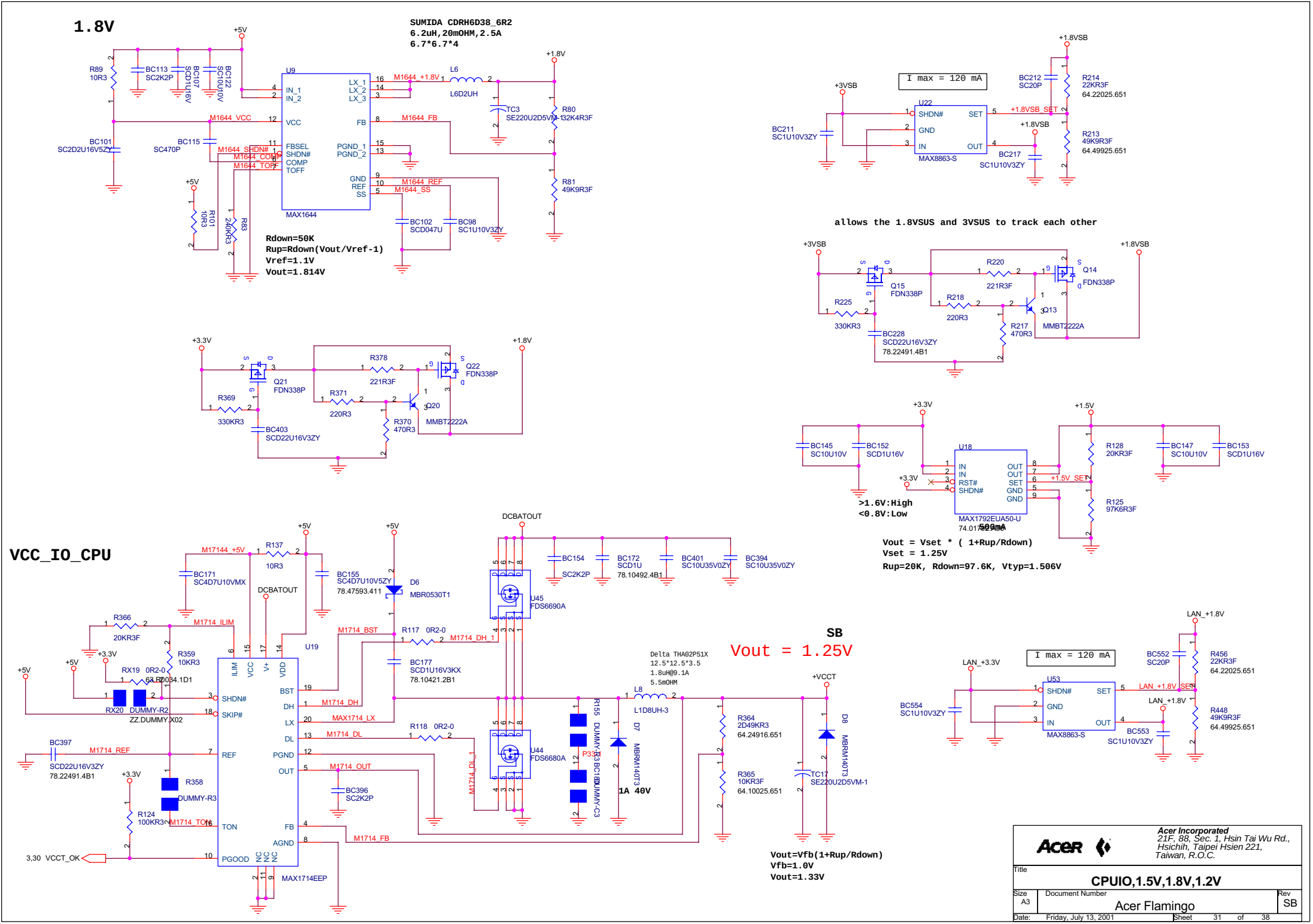
1.8V
SUMIDA CDRH6D38_6R2
6.2uH,20mOHM,2.5A
6.7*6.7*4
MAX1644
Rdown=50K
Rup=Rdown(Vout/Vref-1)
Vref=1.1V
Vout=1.814V
I max = 120 mA
MAX8863-S
allows the 1.8VSUS and 3VSUS to track each other
>1.6V:High
<0.8V:Low
MAX1792EUA50-U
500mA
Vout = Vset * (1+Rup/Rdown)
Vset = 1.25V
Rup=20K, Rdown=97.6K, Vtyp=1.506V
VCC_IO_CPU
SB
Vout = 1.25V
Delta THA02P51X
12.5*12.5*3.5
1.8uH@9.1A
5.5mOHM
1A 40V
MAX1714EEP
Vout=Vfb(1+Rup/Rdown)
Vfb=1.0V
Vout=1.33V
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Taiwan, R.O.C.
Title
CPUIO,1.5V,1.8V,1.2V
Size A3
Document Number
Acer Flamingo
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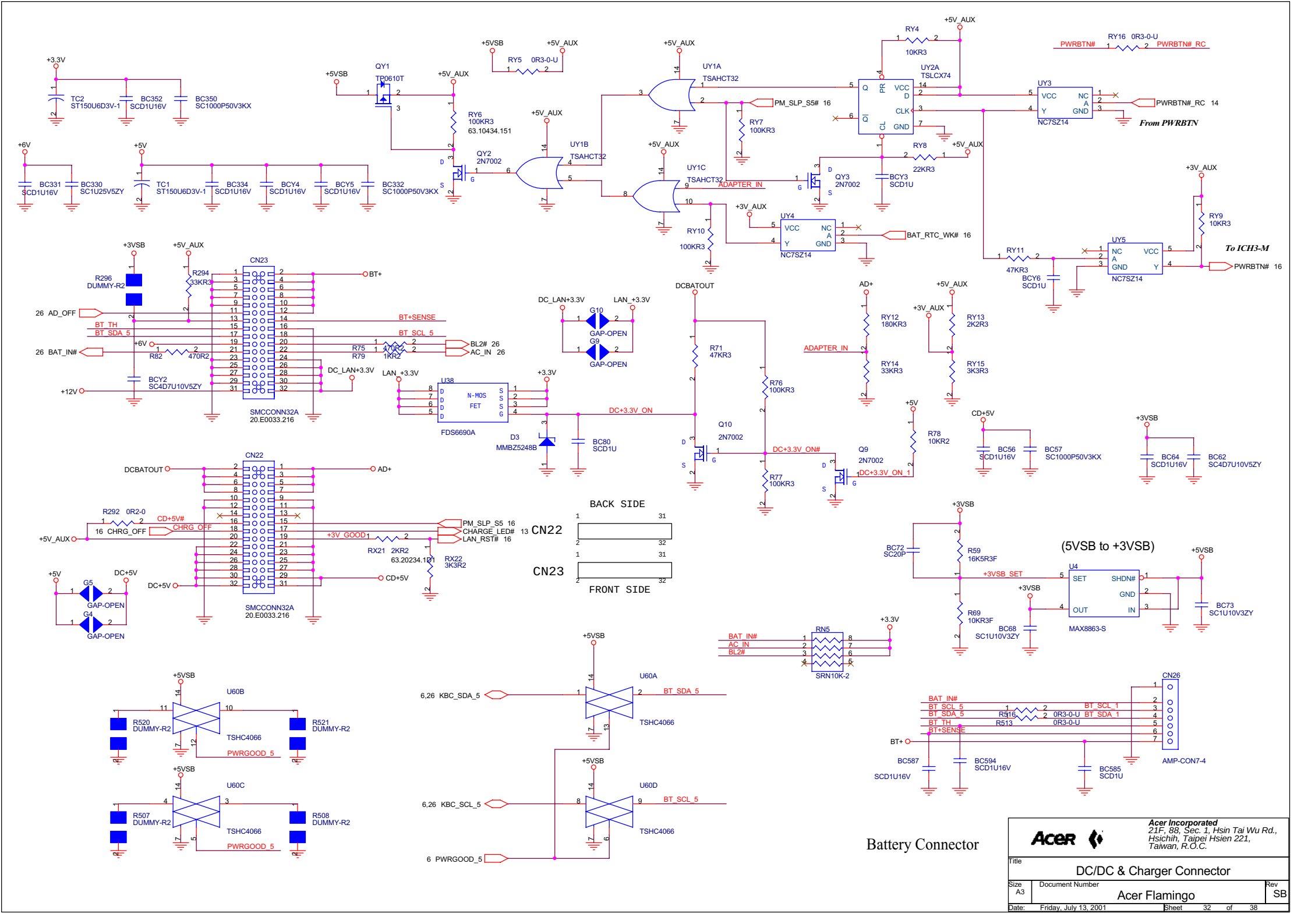
+3.3V
TC2 ST150U6D3V-1
BC352 SCD1U16V
BC350 SC1000P50V3KX
+6V
BC331 SCD1U16V
BC330 SC1U25V5ZY
+5V
TC1 ST150U6D3V-1
BC334 SCD1U16V
BC4 SCD1U16V
BC5 SCD1U16V
BC332 SC1000P50V3KX
+5VSB
QY1 TP0610T
+5V_AUX
RY5 0R3-0-U
RY6 100KR3 63.10434.151
QY2 2N7002
UY1A TSAHCT32
UY1B TSAHCT32
UY1C TSAHCT32
RY4 10KR3
UY2A TSLCX74
PM_SLP_S5# 16
RY7 100KR3
ADAPTER_IN
QY3 2N7002
RY8 22KR3
BCY3 SCD1U
UY3 NC7SZ14
PWRBTN# RY16 0R3-0-U PWRBTN#_RC
PWRBTN#_RC 14
From PWRBTN
UY4 NC7SZ14
BAT_RTC_WK# 16
+3V_AUX
RY9 10KR3
RY11 47KR3
BCY6 SCD1U
UY5 NC7SZ14
To ICH3-M
PWRBTN# 16
CN23
R296 DUMMY-R2
R294 33KR3
BT+
26 AD_OFF
BT_TH
BT_SDA_5
BT+SENSE
BT_SCL_5
26 BAT_IN#
R82 470R2
R75 470R2
R79 1KR2
BL2# 26
AC_IN 26
BCY2 SC4D7U10V5ZY
DC_LAN+3.3V
+12V
SMCCONN32A 20.E0033.216
LAN_+3.3V
U38 N-MOS FET
FDS6690A
DC+3.3V_ON
D3 MMBZ5248B
BC80 SCD1U
G10 GAP-OPEN
G9 GAP-OPEN
DCBATOUT
R71 47KR3
R76 100KR3
Q10 2N7002
DC+3.3V_ON#
Q9 2N7002
DC+3.3V_ON_1
R77 100KR3
AD+
RY12 180KR3
RY13 2K2R3
RY14 33KR3
RY15 3K3R3
R78 10KR2
CD+5V
BC56 SCD1U16V
BC57 SC1000P50V3KX
BC64 SCD1U16V
BC62 SC4D7U10V5ZY
CN22
DCBATOUT
AD+
R292 0R2-0
CD+5V#
16 CHRG_OFF
CHRG_OFF
+5V_AUX
+3V_GOOD
PM_SLP_S5 16
CHARGE_LED# 13
LAN_RST# 16
RX21 2KR2 63.20234.121
RX22 3KR3
CD+5V
DC+5V
G5 GAP-OPEN
G4 GAP-OPEN
SMCCONN32A 20.E0033.216
BACK SIDE
CN22
CN23
FRONT SIDE
(5VSB to +3VSB)
BC72 SC20P
R59 16K5R3F
+3VSB_SET
U4 MAX8863-S
SET
SHDN#
GND
OUT
IN
R69 10KR3F
BC68 SC1U10V3ZY
BC73 SC1U10V3ZY
RN5 SRN10K-2
BAT_IN#
AC_IN
BL2#
U60B TSHC4066
R520 DUMMY-R2
R521 DUMMY-R2
PWRGOOD_5
U60C TSHC4066
R507 DUMMY-R2
R508 DUMMY-R2
U60A TSHC4066
6,26 KBC_SDA_5
BT_SDA_5
U60D TSHC4066
6,26 KBC_SCL_5
BT_SCL_5
6 PWRGOOD_5
CN26
BAT_IN#
BT_SCL_5
BT_SDA_5
BT_TH
BT+SENSE
R516 0R3-0-U
R513 0R3-0-U
BT_SCL_1
BT_SDA_1
BT+
BC587 SCD1U16V
BC594 SCD1U16V
BC585 SCD1U
AMP-CON7-4
Battery Connector
Acer Incorporated
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
DC/DC & Charger Connector
Size A3
Document Number
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CHKPW

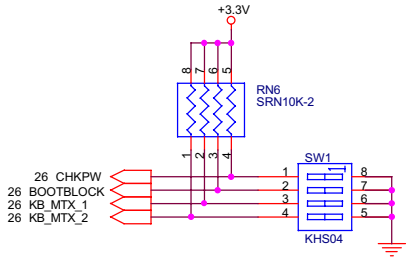
	Enable	Disable
SW1-1	ON	OFF

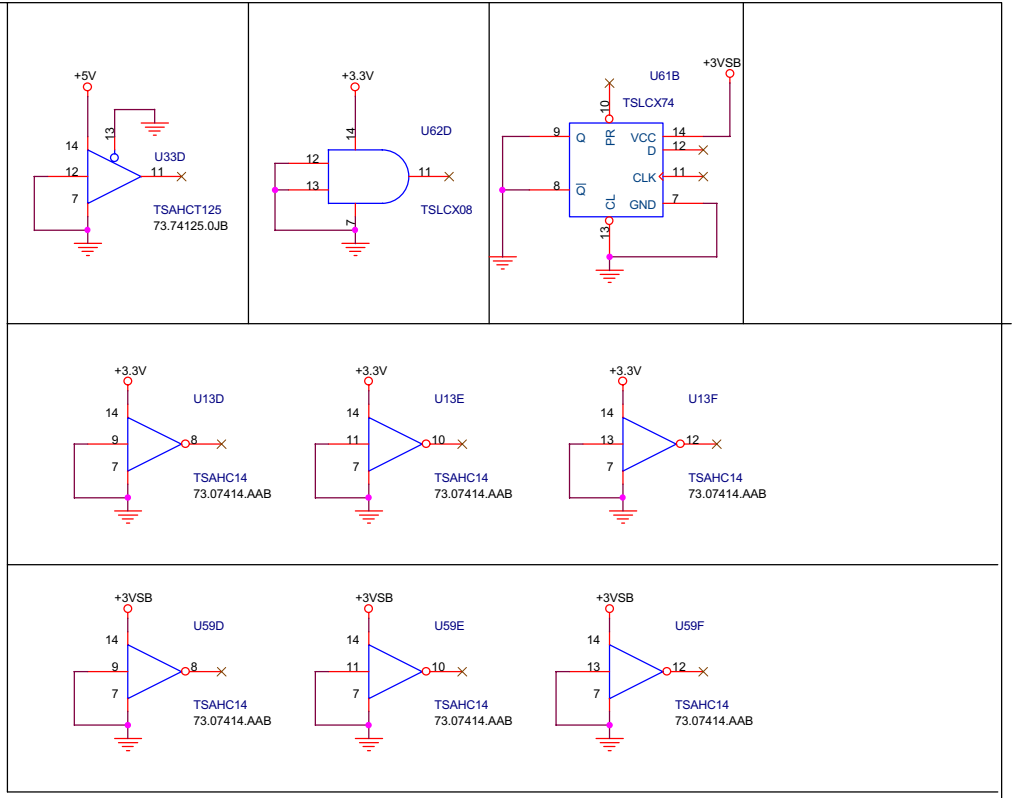
BIOS Bootblock erasable

	Enable	Disable
SW1-2	ON	OFF

Keyboard matrix

	US	Jap	Europe	US international
SW1-3	OFF	ON	OFF	OFF
SW1-4	OFF	OFF	ON	OFF





OEM Logo setting

COOLING SYSTEM SELECT

	Enable	Disable
SW1-8	ACER	HITACHI

	ACER	HITACHI	OEM2	OEM3
SW1-4	OFF	ON	OFF	ON
SW1-5	OFF	OFF	ON	ON

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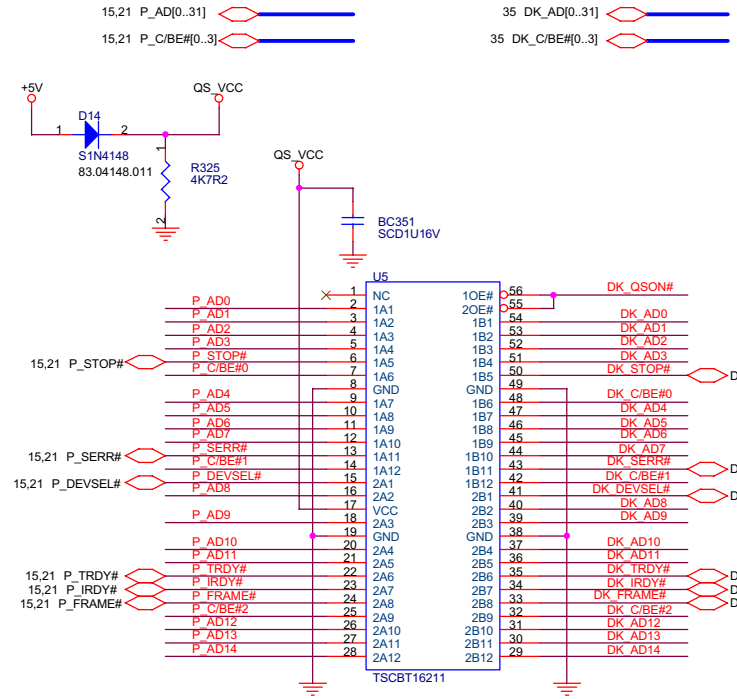
Title: **JUMP SETTING & NO USE GATE**

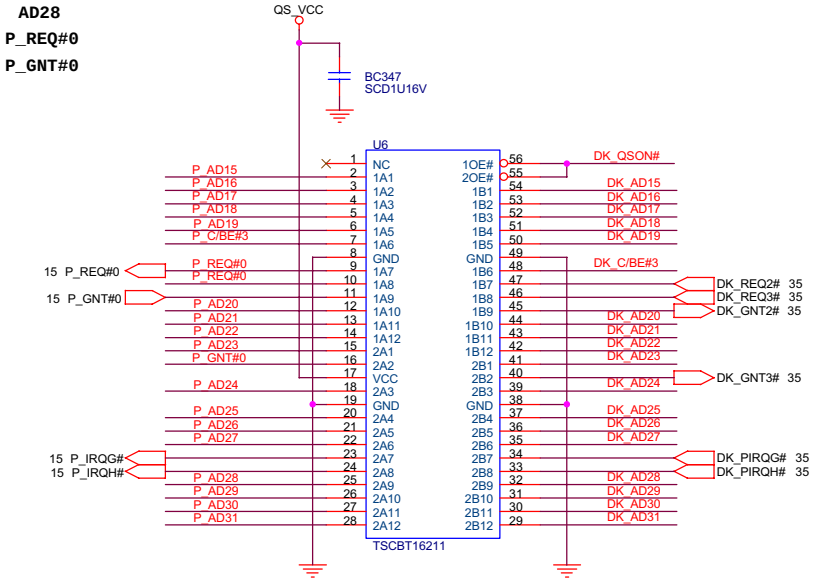
Size: A3 | Document Number: Acer Flamingo | Rev: SB

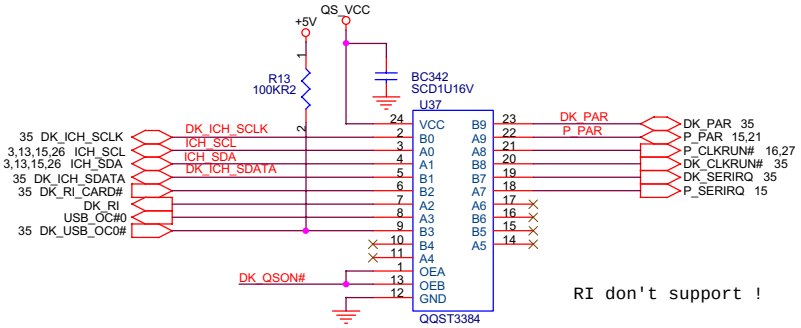
Date: Friday, July 13, 2001 | Sheet 33 of 38

(CHANGE TO TSSOP PACKAGE)



P_IRQG#
P_IRQH#
AD28
P_REQ#0
P_GNT#0





RI don't support !

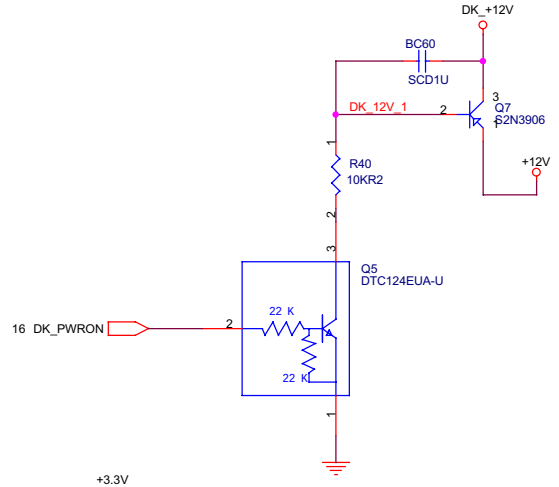
(STEP 1) SYSTEM CONTACT TO DOCK (GPIO[16] / DK_IN_5)

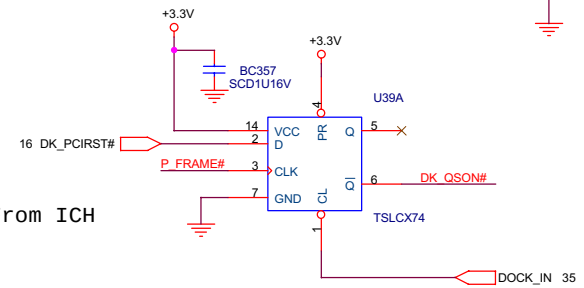
(STEP 2) TURN ON POWER (GPIO[14] / DK_PWR_ON_5) (POWER MOS AT DOCKING SIDE)

(STEP 3) CLK GEN. TURN ON DK PCICLK (KBC P61 / DK_CLK_ON#_3)

(STEP 4) GPO GENERATE PCIRST# (KBC P63 / DK_PCIRST)

(STEP5) TURN ON Q-SW





From ICH

From DOCK

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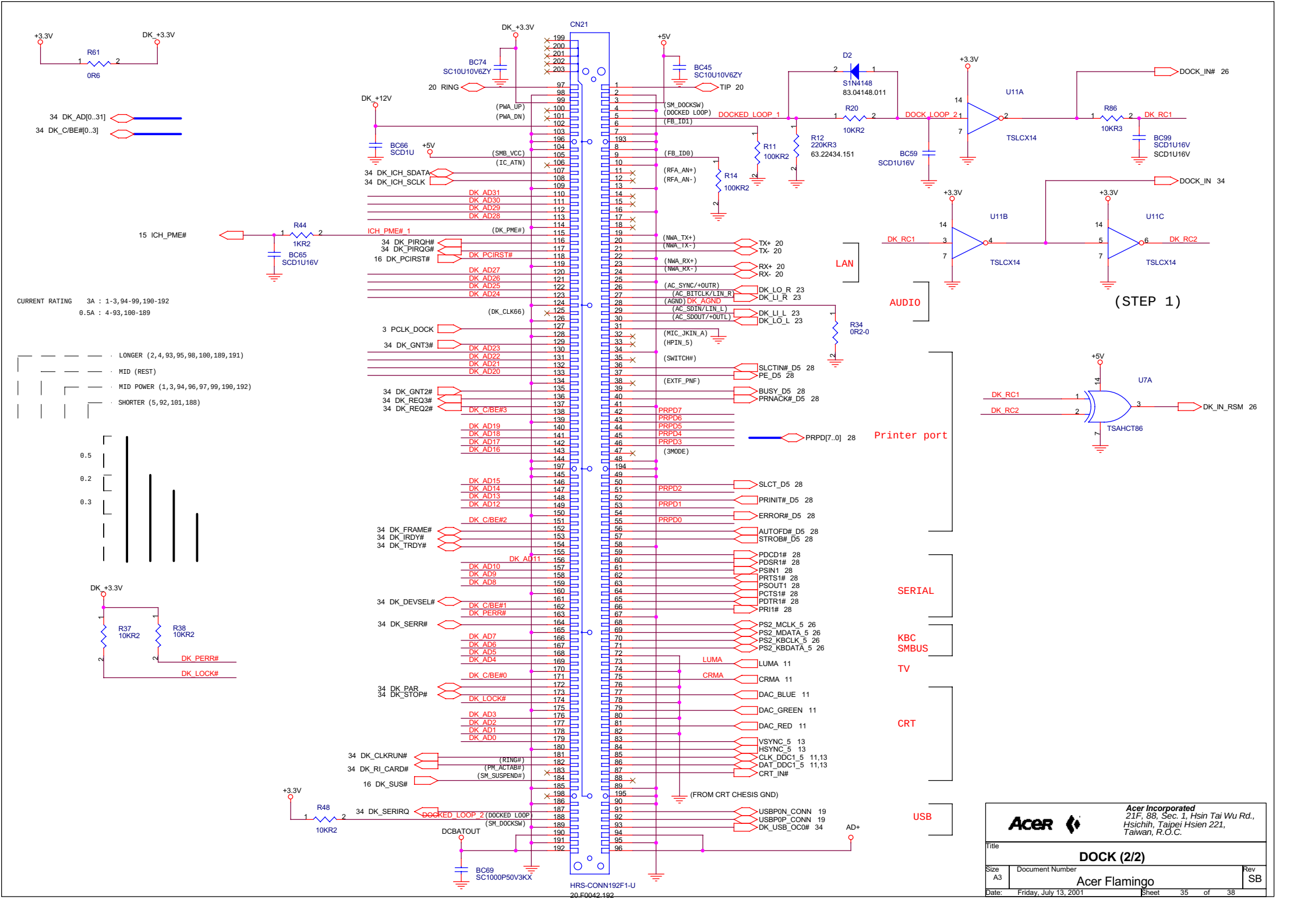
Taiwan, R.O.C.

Title: **DOCK (1/2)**

Size	Document Number	Rev
A3	Acer Flamingo	SB

Date: Monday, July 16, 2001 Sheet 34 of 38



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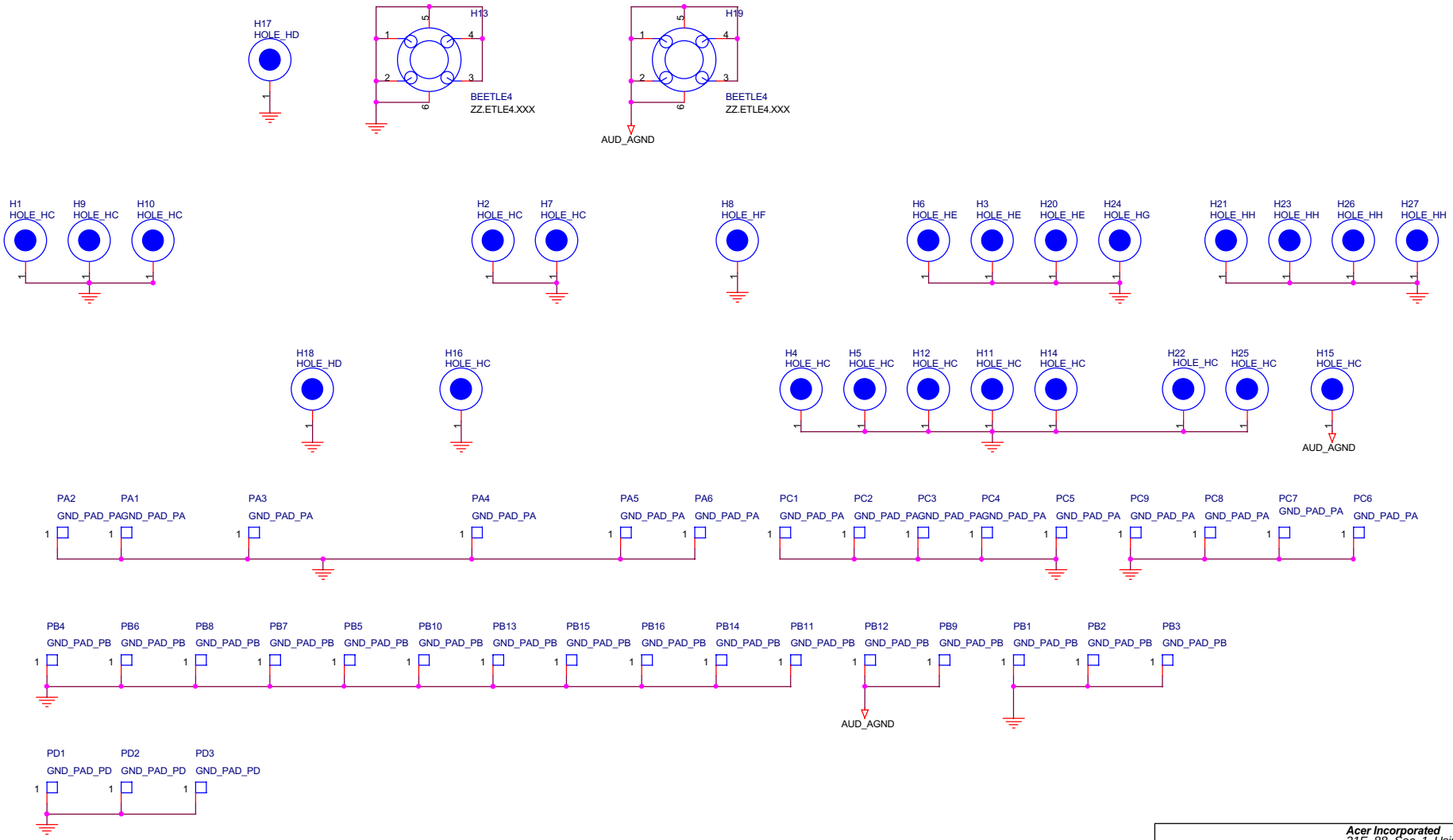
Title: DOCK (2/2)			
Size: A3	Document Number: Acer Flamingo		Rev: SB
Date: Friday, July 13, 2001	Sheet 35 of 38		



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Title

MACH. HOLE

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NEAR CPU

TP23 TPAD30 ZZ.PAD30.XXX CC_SMI# 15

NEAR GMCH

NEAR VGA

TP22 TPAD30 ZZ.PAD30.XXX VGA_MEM_CS1# 12

NEAR ICH3-M

TP24 TPAD30 ZZ.PAD30.XXX P_IRQC# 15
TP26 TPAD30 ZZ.PAD30.XXX P_IRQE# 15
TP28 TPAD30 ZZ.PAD30.XXX P_IRQF# 15

15 P_REQ#2 TP25 TPAD30 ZZ.PAD30.XXX
15 P_REQ#3 TP27 TPAD30 ZZ.PAD30.XXX
15 P_REQ#4 TP29 TPAD30 ZZ.PAD30.XXX

15 P_GNT#2 TP30 TPAD30 ZZ.PAD30.XXX
15 P_GNT#3 TP31 TPAD30 ZZ.PAD30.XXX
15 P_GNT#4 TP32 TPAD30 ZZ.PAD30.XXX

NEAR IEEE1394

NEAR CARDBUS

Acer Incorporated
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Hsichih, Taipei Hsien 221,
Taiwan, R.O.C.

Title: **TEST POINT**

Size	Document Number	Rev
A3	Acer Flamingo	SB

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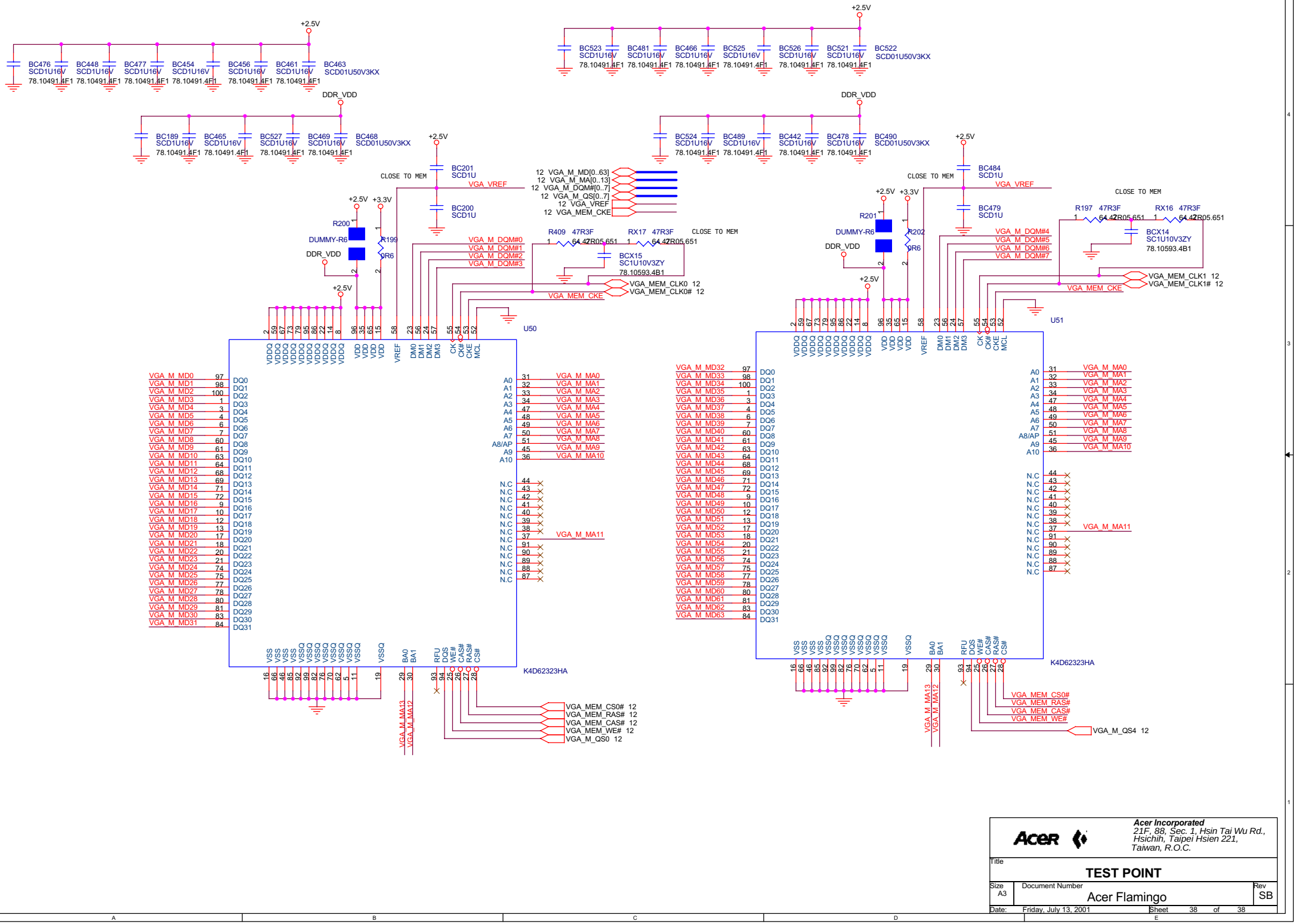
+2.5V
BC476 SCD1U16V 78.10491.4F1
BC448 SCD1U16V 78.10491.4F1
BC477 SCD1U16V 78.10491.4F1
BC454 SCD1U16V 78.10491.4F1
BC456 SCD1U16V 78.10491.4F1
BC461 SCD1U16V 78.10491.4F1
BC463 SCD01U50V3KX
BC523 SCD1U16V 78.10491.4F1
BC481 SCD1U16V 78.10491.4F1
BC466 SCD1U16V 78.10491.4F1
BC525 SCD1U16V 78.10491.4F1
BC526 SCD1U16V 78.10491.4F1
BC521 SCD1U16V 78.10491.4F1
BC522 SCD01U50V3KX
DDR_VDD
BC189 SCD1U16V 78.10491.4F1
BC465 SCD1U16V 78.10491.4F1
BC527 SCD1U16V 78.10491.4F1
BC469 SCD1U16V 78.10491.4F1
BC468 SCD01U50V3KX
BC524 SCD1U16V 78.10491.4F1
BC489 SCD1U16V 78.10491.4F1
BC442 SCD1U16V 78.10491.4F1
BC478 SCD1U16V 78.10491.4F1
BC490 SCD01U50V3KX
CLOSE TO MEM
BC201 SCD1U
VGA_VREF
BC200 SCD1U
12 VGA_M_MD[0..63]
12 VGA_M_MA[0..13]
12 VGA_M_DQM#[0..7]
12 VGA_M_QS[0..7]
12 VGA_VREF
12 VGA_MEM_CKE
+3.3V
R200
DUMMY-R6
R199
0R6
R409 47R3F 64.47R05.651
RX17 47R3F 64.47R05.651
BCX15 SC1U10V3ZY 78.10593.4B1
VGA_M_DQM#0
VGA_M_DQM#1
VGA_M_DQM#2
VGA_M_DQM#3
VGA_MEM_CLK0 12
VGA_MEM_CLK0# 12
VGA_MEM_CKE
U50
VDDQ VDD VREF DM0 DM1 DM2 DM3 CK CK# CKE MCL
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31
A0 A1 A2 A3 A4 A5 A6 A7 A8/AP A9 A10
N.C
VSS VSSQ BA0 BA1 RFU DQS WE# CAS# RAS# CS#
K4D62323HA
VGA_M_MA13
VGA_M_MA12
VGA_MEM_CS0# 12
VGA_MEM_RAS# 12
VGA_MEM_CAS# 12
VGA_MEM_WE# 12
VGA_M_QS0 12
R201
R202
0R6
R197 47R3F 64.47R05.651
RX16 47R3F 64.47R05.651
BCX14 SC1U10V3ZY 78.10593.4B1
VGA_M_DQM#4
VGA_M_DQM#5
VGA_M_DQM#6
VGA_M_DQM#7
VGA_MEM_CLK1 12
VGA_MEM_CLK1# 12
U51
VGA_M_MD32 VGA_M_MD33 VGA_M_MD34 VGA_M_MD35 VGA_M_MD36 VGA_M_MD37 VGA_M_MD38 VGA_M_MD39 VGA_M_MD40 VGA_M_MD41 VGA_M_MD42 VGA_M_MD43 VGA_M_MD44 VGA_M_MD45 VGA_M_MD46 VGA_M_MD47 VGA_M_MD48 VGA_M_MD49 VGA_M_MD50 VGA_M_MD51 VGA_M_MD52 VGA_M_MD53 VGA_M_MD54 VGA_M_MD55 VGA_M_MD56 VGA_M_MD57 VGA_M_MD58 VGA_M_MD59 VGA_M_MD60 VGA_M_MD61 VGA_M_MD62 VGA_M_MD63
VGA_M_QS4 12
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TEST POINT
Size A3
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Rev SB
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