ZY7 SYSTEM BLOCK DIAGRAM

AMD Smarter Choice

CPU CORE ISL6265A PAGE 29

NB CORE (RT8202) PAGE XX

DDR II SMDDR_VTERM 1.8VSUS(TPS51116REGR) PAGE 31

SYSTEM POWER ISL6237 PAGE 28

SYSTEM CHARGER (ISL6251A) PAGE 27

DDRII-SODIMM1 PAGE 7 — DDRII 667/800 MHz

DDRII-SODIMM2 PAGE 7 — DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5,6

CPU THERMAL SENSOR PAGE 5

CPU Fan

HT3 LINK

14.318MHz

CLOCK GEN
ICS9LPRS476AKLFT-->HP
SLG8SP626VTR-->HP
RTM880N-795 -->HP
PAGE 2

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK
SBSRC_CLK

LVDS PAGE 18 — LVDS

SWITCH — CRT, HDMI

MXM Connector PAGE 17 — PCI-Express 16X

Internal selector Resistor PAGE 17 — LVDS, CRT, HDMI

NORTH BRIDGE
RX780 / RS780M
21mm X 21mm, 528pin BGA
PAGE 8,9,10,11

PCI-E

PCIE2 / 3 X2 — Mini PCI-E Card Wireless /TV PAGE 19

PCIE1 X1 — Express Card (NEW CARD) PAGE 19

PCIE4 X1 — LAN PCIE-LAN BCM5764M (10/100/GagaLAN) PAGE 21 — RJ45 PAGE 21

PCIE5 X1 — JMB385 4 IN 1 CARD READER PAGE 24

PCIE X4

DVI-D PAGE 26
CRT PAGE 26
AUDIO PAGE 26
LAN PAGE 26
USB PAGE 26
DOCKING

HDMI PAGE 18
CRT PAGE 18
M/B

SATA - HDD PAGE 20 — SATA0

SATA - HDD PAGE 20 — SATA1

ODD(SATA) PAGE 20 — SATA4

SOUTH BRIDGE
SB700
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13,14,15,16

USB2.0 — 1,11 / 5 / 3,4 / 8,9 / 6 / 2 / 10 / 7

USB2.0 Ports x4 PAGE 19
Bluetooth x1 PAGE 19
PC-cam x1 PAGE 18
Fingerprint x1 PAGE 19
USB Docking x1 PAGE 19

PCI BUS / 33MHz

O2 OZ601 PAGE 23 — PCMCIA CARD BUS PAGE 23

Azalia

Azalia AudioController RealTek ALC268 PAGE 22

MDC 1.5 PAGE 22

LPC

Keyboard PAGE 25

KBC (WPCE775) PAGE 25

Touch Pad PAGE 20

SPI ROM PAGE 25

Audio Amplifier

Int MIC

Speaker

SPIDF/Phone Jack

Line in

MIC Jack

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD20	INTF#	OZ601

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	Block Diagram	1A

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CLK_GEN_SLG8SP628

+3V L39 BK1608HS600 +3V_CLK_VDD
C399 22U-10V_8 C365 .1u/10V_4 C373 .1u/10V_4 C364 .1u/10V_4 C394 .1u/10V_4 C409 .1u/10V_4 C390 .1u/10V_4 C402 .1u/10V_4 C381 .1u/10V_4

Change C1000/C1008 from 10u to 22u.-1001

+1.2V L42 BK1608HS600 +1.2V_CLK_VDDIO
C407 22U-10V_8 C405 .1u/10V_4 C378 .1u/10V_4 C406 .1u/10V_4 C408 .1u/10V_4 C374 .1u/10V_4 C389 .1u/10V_4

ICS9LPRS480 P/N :

SLG8SP628 P/N : AL8SP628000

RTM880N-796 P/N : AL000880000

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

Place within 0.5" of CLKGEN

CHECK

R255 *261/F_4

+3V +3V_CLK_48 L38 BK1608HS600 C363 2.2U/6.3V/06

C367 20p/50V_4 CG_XIN
Y3 14.318MHZ
C366 20p/50V_4 CG_XOUT

Follow CLK ~~14.318~~ Check 20p 11/19

U14 QFN64 SLG8SP628

+3V_CLK_VDD	4	VDDDOT	CPUK8_0T	50	CPUCLKP_R RP25 1 2 0X2 CPU_CLKP → CPU_CLKP 5 To CPU
	16	VDDSRC	CPUK8_0C	49	CPUCLKN_R 3 4 CPU_CLKN → CPU_CLKN 5
	26	VDDATIG			
	35	VDDSB_SRC	ATIG0T	30	NBGFX_CLKP_R RP35 1 2 0X2 → NBGFX_CLKP 10 To NB
	40	VDDSATA	ATIG0C	29	NBGFX_CLKN_R 3 4 → NBGFX_CLKN 10
	48	VDDCPU	ATIG1T	28	CLK_PCIE_MXM_R RP34 1 2 *EV^0X2 → CLK_PCIE_MXM 17 To MXM Card
	55	VDDHTT	ATIG1C	27	CLK_PCIE_MXM#_R 3 4 → CLK_PCIE_MXM# 17
	56	VDDREF			External VGA Card only
	63	VDD48	SB_SRC0T	37	SBLINK_CLKP_R RP30 1 2 0X2 → SBLINK_CLKP 10 To NB
+1.2V_CLK_VDDIO	11	VDDSRC_IO0	SB_SRC0C	36	SBLINK_CLKN_R 3 4 → SBLINK_CLKN 10
	17	VDDSRC_IO1	SB_SRC1T	32	SBSRC_CLKP_R RP36 1 2 0X2 → SBSRC_CLKP 12 To SB
	25	VDDATIG_IO	SB_SRC1C	31	SBSRC_CLKN_R 3 4 → SBSRC_CLKN 12
	34	VDDSB_SRC_IO			
	47	VDDCPU_IO	SRC0T	22	NBGPP_CLKP_R RP33 1 2 *EV^0X2 → NBGPP_CLKP 10
	1	GND48	SRC0C	21	NBGPP_CLKN_R 3 4 → NBGPP_CLKN 10
	7	GNDDOT	SRC1T	20	CLK_PCIE_NEW_R RP32 1 2 0X2 → CLK_PCIE_NEW 19 To New Card
	10	GNDSRC0	SRC1C	19	CLK_PCIE_NEW#_R 3 4 → CLK_PCIE_NEW# 19
	18	GNDSRC1	SRC2T	15	CLK_PCIE_MINI_R RP31 1 2 0X2 → CLK_PCIE_MINI 19 To Mini PCIE Slot
	24	GNDATIG	SRC2C	14	CLK_PCIE_MINI#_R 3 4 → CLK_PCIE_MINI# 19
	33	GNDSB_SRC	SRC3T	13	CLK_PCIE_TV_R RP29 1 2 0X2 → CLK_PCIE_TV 19 To TV PCIE Slot
	43	GNDSATA	SRC3C	12	CLK_PCIE_TV#_R 3 4 → CLK_PCIE_TV# 19
	46	GNDCPU	SRC4T	9	CLK_PCIE_LAN_R RP27 1 2 0X2 → CLK_PCIE_LAN 21 To LAN Controller
	52	GNDHTT	SRC4C	8	CLK_PCIE_LAN#_R 3 4 → CLK_PCIE_LAN# 21
	60	GNDREF			
			SRC6T/SATAT	42	CLK_PCIE_CR_R RP28 1 2 0X2 → CLK_PCIE_CR 24 To Card Reader Controller
			SRC6C/SATAC	41	CLK_PCIE_CR#_R 3 4 → CLK_PCIE_CR# 24
CG_XIN	61	X1	SRC7T/27M_SS	6	T82
CG_XOUT	62	X2	SRC7C/27M_NS	5	T81
CGCLK_SMB	2	SMBCLK	HTT0T/66M	54	NBHT_REFCLKP_R RP26 1 2 0X2 → NBHT_REFCLKP 10 To NB
CGDAT_SMB	3	SMBDAT	HTT0C/66M	53	NBHT_REFCLKN_R 3 4 → NBHT_REFCLKN 10
CLK_PD#	51	PD#	48MHz_0	64	CLK_48M_USB_R R268 33_4 → CLK_48M_USB 13 To SB
T87	23	CLKREQ0#	REF0/SEL_HTT66	59	SEL_HTT66
13,19 NEW_CLKREQ#	45	CLKREQ1#	REF1/SEL_SATA	58	SEL_SATA
19 MINI_CLKREQ#	44	CLKREQ2#	REF2/SEL_27	57	SEL_27 R265 158/F_4 R250 90.9/F_4 → EXT_NB_OSC 10 To NB
19 TV_CLKREQ#	39	CLKREQ3#			
21 LAN_CLKREQ#	38	CLKREQ4#			
		TGND0 TGND1 TGND2 TGND3 TGND4 TGND5 TGND6 TGND7 TGND8 TGND9			
		65 66 67 68 69 70 71 72 73 74			

+3V_CLK_VDD
R272 8.2K_4 NEW_CLKREQ#
R286 8.2K_4 LAN_CLKREQ#
R264 8.2K_4 CLK_PD#
R277 8.2K_4 MINI_CLKREQ#
R283 8.2K_4 TV_CLKREQ#

New Card CLKREQ#

CLK_48M_USB_R C372 *10p_4
SEL_27 C350 22P/50V_4

REV B:Change to Stuff 22PF for EMI request --0215

R1004/R1005 (value may change)

	NB_OSC
RX780	1.8V 82.5R/130R
RS780	1.1V 158R/90.9R

RES CHIP 82.5 1/16W +-1%(0402) --> CS08252FB11
RES CHIP 130 1/16W +-1%(0402)L-F --> CS11302FB15

RES CHIP 158 1/16W +-1%(0402) --> CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) --> CS09092FB15

NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

Clock Gen I2C

+3V Q26 RHU002N06 R275 10K_4
7,13,18,19 PDAT_SMB PDAT_SMB CGDAT_SMB

Check Chipset Power Domain

+3V Q25 RHU002N06 R274 10K_4
7,13,18,19 PCLK_SMB PCLK_SMB CGCLK_SMB

+3V_CLK_VDD
R260 *8.2K_4
R259 8.2K_4 R258 8.2K_4 R249 8.2K_4
SEL_SATA
SEL_HTT66
SEL_27

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

* default

Quanta Computer Inc.
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	CLOCK GENERATOR_SLG8SP628	1A

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8 HT_RXD#[15..0] HT_RXD#[15..0]
8 HT_RXD[15..0] HT_RXD[15..0]
8 HT_TXD[15..0] HT_TXD[15..0]
8 HT_TXD#[15..0] HT_TXD#[15..0]

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

VLDT_RUN

U25A

HT LINK

	D1	VLDT_A0	VLDT_B0	AE2	
	D2	VLDT_A1	VLDT_B1	AE3	
	D3	VLDT_A2	VLDT_B2	AE4	
	D4	VLDT_A3	VLDT_B3	AE5	
HT_RXD0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	HT_TXD0
HT_RXD#0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	HT_TXD#0
HT_RXD1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	HT_TXD1
HT_RXD#1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	HT_TXD#1
HT_RXD2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	HT_TXD2
HT_RXD#2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	HT_TXD#2
HT_RXD3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	HT_TXD3
HT_RXD#3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	HT_TXD#3
HT_RXD4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	HT_TXD4
HT_RXD#4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	HT_TXD#4
HT_RXD5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	HT_TXD5
HT_RXD#5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	HT_TXD#5
HT_RXD6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	HT_TXD6
HT_RXD#6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	HT_TXD#6
HT_RXD7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	HT_TXD7
HT_RXD#7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	HT_TXD#7
HT_RXD8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	HT_TXD8
HT_RXD#8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	HT_TXD#8
HT_RXD9	E3	L0_CADIN_H9	L0_CADOUT_H9	AD5	HT_TXD9
HT_RXD#9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	HT_TXD#9
HT_RXD10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	HT_TXD10
HT_RXD#10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	HT_TXD#10
HT_RXD11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	HT_TXD11
HT_RXD#11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	HT_TXD#11
HT_RXD12	K3	L0_CADIN_H12	L0_CADOUT_H12	Y5	HT_TXD12
HT_RXD#12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	HT_TXD#12
HT_RXD13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	HT_TXD13
HT_RXD#13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	HT_TXD#13
HT_RXD14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	HT_TXD14
HT_RXD#14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	HT_TXD#14
HT_RXD15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	HT_TXD15
HT_RXD#15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	HT_TXD#15
8 HT_CPU_UPCLK0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	HT_CPU_DWNCLK0 8
8 HT_CPU_UPCLK#0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	HT_CPU_DWNCLK#0 8
8 HT_CPU_UPCLK1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	HT_CPU_DWNCLK1 8
8 HT_CPU_UPCLK#1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	HT_CPU_DWNCLK#1 8
8 HT_CPU_UPCTL0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	HT_CPU_DWNCTL0 8
8 HT_CPU_UPCTL#0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	HT_CPU_DWNCTL#0 8
8 HT_CPU_UPCTL1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	HT_CPU_DWNCTL1 8
8 HT_CPU_UPCTL#1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	HT_CPU_DWNCTL#1 8

C519 4.7u/6.3V_6

Athlon 64 S1g2 SOCKET_638_PIN

Athlon 64 S1g2 Processor Socket SOCKET_638_PIN

NO STUB for HT3

R135 *51_4

R133 *51_4

VLDT_RUN

HOLE27 *MINI_HOLE
HOLE28 MINI_HOLE
HOLE36 MINI_HOLE
HOLE37 MINI_HOLE

HOLE9 CPU_HOLE
HOLE10 CPU_HOLE
HOLE19 CPU_HOLE
HOLE20 CPU_HOLE

HOLE8 MXM_HOLE
HOLE17 MXM_HOLE
HOLE16 MXM_HOLE
HOLE7 MXM_HOLE

HOLE6 *EV^MXM1_HOLE
HOLE21 *EV^MXM1_HOLE
HOLE11 MDC_HOLE
HOLE13 MDC_HOLE

HOLE14 *H-C295D118P2
HOLE5 *H-C295D118P2
HOLE2 *H-C295D118P2
HOLE23 *H-C295D118P2

HOLE4 *H-C295D118P2
HOLE35 *H-C295D118P2
HOLE25 *H-C295D118P2
HOLE24 *H-C295D118P2

ADOGND

HOLE32 *H-C295D118P2
HOLE34 *H-C295D118P2
HOLE33 *H-C295D118P2
HOLE1 *H-C295D118P2

HOLE39 *FAN_HOLE
HOLE38 FAN_HOLE
HOLE15 *NONP_HOLE1
HOLE3 *H-C295D118P2

REV B: Add Hole39 for ME request---0215

HOLE26 ODD1_HOLE
HOLE30 ODD1_HOLE
HOLE31 HDD1_HOLE
HOLE29 HDD1_HOLE
HOLE22 HDD2_HOLE
HOLE18 HDD2_HOLE

PAD2 EMIPAD
PAD3 EMIPAD
PAD1 *EMIPAD

SPAD1 *SPAD

+1.2V
VLDT_RUN

L50 FBJ3216HS800_1206
L54 FBJ3216HS800_1206

80 ohm(4A)

C555 4.7u/6.3V_6
C560 4.7u/6.3V_6
C569 .22U_4
C527 .22U_4
C522 180P_4
C565 180P_4

Note:on MCP77,(HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.

LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

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	AMD Griffin HT I/F	1A
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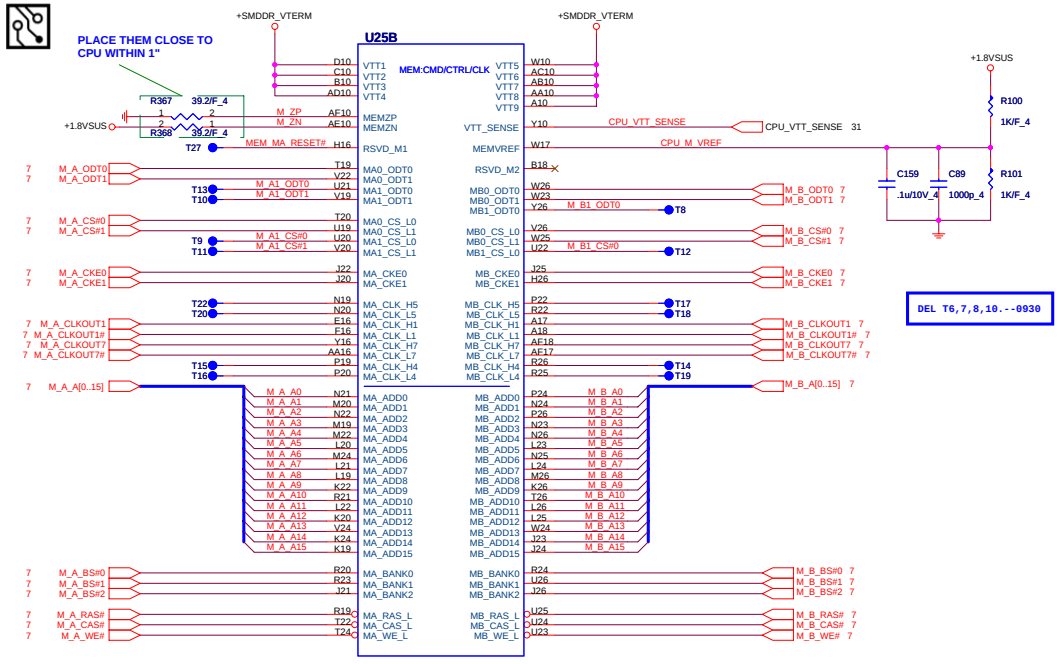
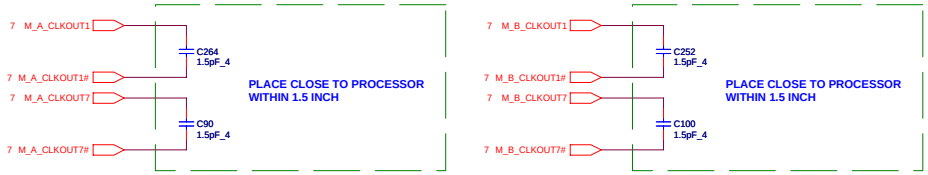
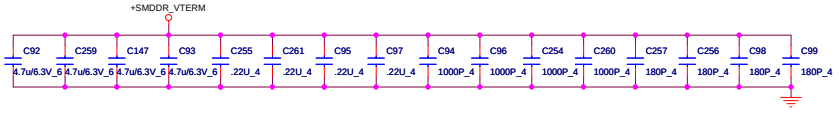
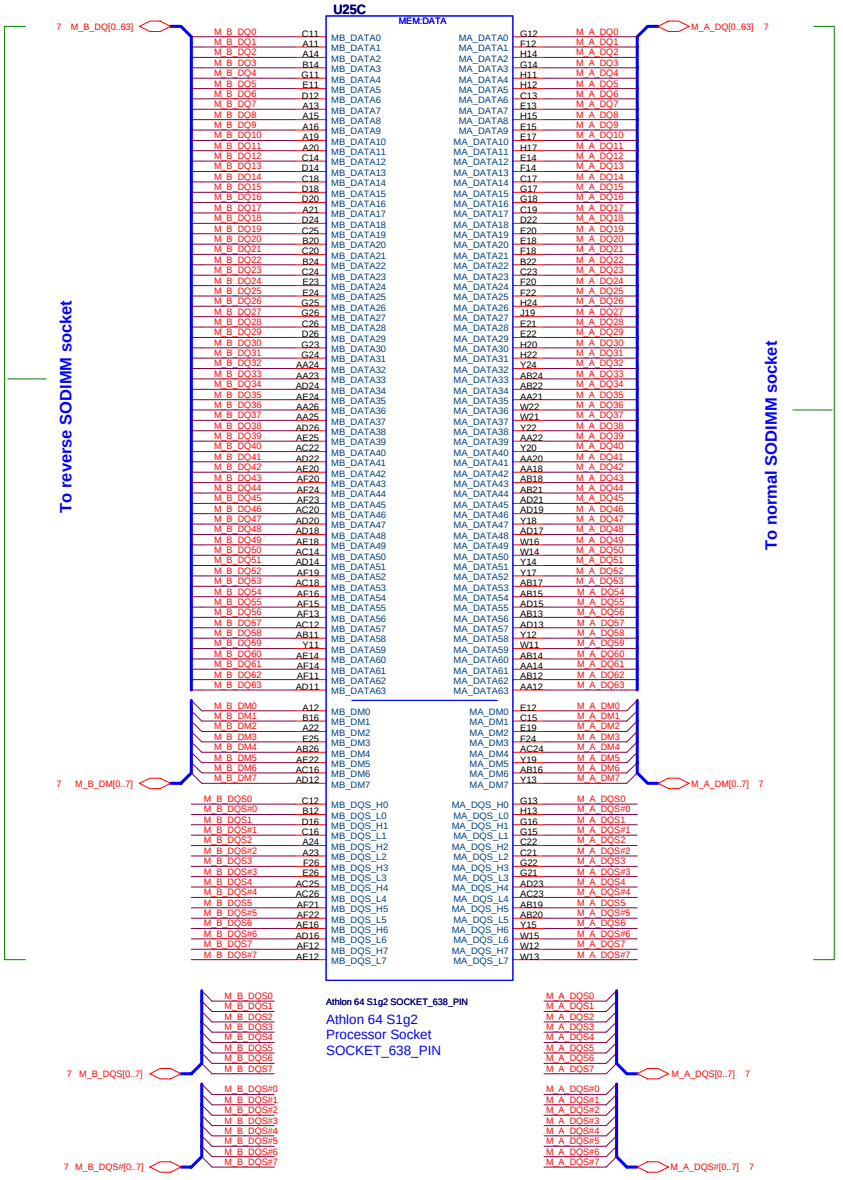
VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

Processor DDR2 Memory Interface









Quanta Computer Inc.		
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Size	Document Number: AMD Griffin DDRII MEMORY I/F	Rev: 1A
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ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

+2.5V — L57 BLM18PG330SN1D_6 — CPU_VDDA_RUN

C602 100U-6.3V_3528 | C593 4.7u/6.3V_B | C235 .22U_4 | C246 3300p/50V_4

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 390- (±5%) pulldown to VSS.

+1.8VSUS — R363 390_4 CPU_SID; R366 390_4 CPU_SIC; R374 *390_4; R373 1K/F_4 CPU_ALERT

390 Ohm

Need Check .-1001

16,29,32 CPU_COREPG — Q15 2N7002 — R93 *0_4; R97 1K_4; R96 100K_4; R92 300_4; Q16 MMBT3904; R87 0_4 CPU_THERMTRIP_L#; R91 33_4; 13 CPU_THERMTRIP#; SYS_SHDN# 28,32

11/19

U25D

CPU_VDDA_RUN — F8 VDDA1, F9 VDDA2

CPU_CLKP C262 3900P_4 — CPU_CLKIN_SC_P A9; CPU_CLKIN_SC_N A8 — CPU_CLKN C263 3900P_4

Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"

2 CPU_CLKP; 2 CPU_CLKN — R175 169/F_6

place them to CPU within 1.5"

LDT_RST# B7; PWRGD_C A7; LDT_STOP# F10; CPU_LDT_REQ#_CPU C6 — RESET_L, PWROK, LDTSTOP_L, LDTREQ_L

CPU_SIC AE4; CPU_SID AE5; CPU_ALERT AE6 — SIC, SID, ALERT_L

VLDT_RUN — R132 44.2/F_4 CPU_HTREF0; R129 44.2/F_4 CPU_HTREF1 — R6 HT_REF0, P6 HT_REF1

29 CPU_VDD0_FB_H — F6 VDD0_FB_H; 29 CPU_VDD0_FB_L — E6 VDD0_FB_L

29 CPU_VDD1_FB_H — Y6 VDD1_FB_H; 29 CPU_VDD1_FB_L — AB6 VDD1_FB_L

connect to CPU CORE power FB

CPU_DBRDY G10; CPU_TMS AA9; CPU_TCK AC9; CPU_TRST# AD9; CPU_TDI AF9 — DBRDY, TMS, TCK, TRST_L, TDI

Add Pull H/L RES.--0610

Add Pull H/L RES.--0610

T91 CPU_TEST23_TSTUPD AD7 — TEST23

T32 CPU_TEST18_PLLTEST1 H10; T29 CPU_TEST19_PLLTEST0 G9 — TEST18, TEST19

T34 CPU_TEST25_H_BYPASSCLK_H E9; T31 CPU_TEST25_L_BYPASSCLK_L E8 — TEST25_H, TEST25_L

T94 CPU_TEST21_SCANEN AB8; T90 CPU_TEST20_SCANCLK2 AE7; CPU_TEST24_SCANCLK1 AE7; T168 CPU_TEST22_SCANSHIFTEN AE8; T93 CPU_TEST12_SCANSHIFTENB AC8; T1 CPU_TEST27_SINGLECHAIN AF8; T92 CPU_TEST27 — TEST21, TEST20, TEST24, TEST22, TEST12, TEST27

R165 0_4 CPU_TEST9_ANALOGIN — C2 TEST9, AA6 TEST6

A3 RSVD1, A5 RSVD2, B3 RSVD3, B5 RSVD4, C1 RSVD5

M11 KEY1, W18 KEY2

A6 SVC — CPU_SVC_R; A4 SVD — CPU_SVD_R

AF6 THERMTRIP_L — CPU_THERMTRIP_L#; AC7 PROCHOT_L — CPU_PROCHOT#; AA8 MEMHOT_L — CPU_MEMHOT#

W7 THERMDC — CPU_THERMDC; W8 THERMDA — CPU_THERMDA

W9 VDDIO_FB_H — CPU_VDDIO_FB_H 31; Y9 VDDIO_FB_L — CPU_VDDIO_FB_L 31

H6 VDDNB_FB_H — VDD_NB_FB_H 29; G6 VDDNB_FB_L — VDD_NB_FB_L 29

F10 DBREQ_L — CPU_DBREQ#; AF9 TDO — CPU_TDO

route as differential as short as possible testpoint under package

J7 CPU_TEST28_H_PLLCHRZ_P — T25; H8 CPU_TEST28_L_PLLCHRZ_N — T26

D7 CPU_TEST17_BP3 — T35; E7 CPU_TEST16_BP2 — T33; E7 CPU_TEST15_BP1 — T106; C7 CPU_TEST14_BP0 — T105

C9 CPU_TEST29_H_FBCLKOUT_P — T36; C8 CPU_TEST29_L_FBCLKOUT_N — T104

Athlon 64 S1g2 SOCKET_638_PIN

Athlon 64 S1g2
Processor Socket
SOCKET_638_PIN

+1.8VSUS — R89 300_4; R90 330_4; Q14 MMBT3904 — CPU_PROCHOT# — R88 *0_4 — EC_PROCHOT# 25; SB_PROCHOT# 12

+1.8VSUS — R122 *300_4; R99 *330_4; Q17 *MMBT3904 — CPU_MEMHOT# — CPUMEMHOT# 25

connect to CPU CORE power controlier

VID Override Circuit

+1.8VSUS — R434 1K_4; R433 1K_4

CPU_SVC_R R432 0_4 — Serial VID Clock SVC 29

CPU_SVD_R R431 0_4 — Serial VID Data SVD 29

CPU_PWRGD R438 0_4 — PGD_IN 29

R442 *220_4; R441 *220_4

+1.8VSUS — R435 300_4

12 CPU_PWRGD — R439 0_4 — PWRGD_C — C652 .1u/10V_4

+1.8VSUS — R447 300_4

10,12 CPU_LDT_STOP# — R446 0_4 — LDT_STOP#

+1.8VSUS — R436 300_4

10,12 CPU_LDT_RST# — R437 0_4 — LDT_RST#

+1.8VSUS — R448 300_4

Add pull up

CPU_LDT_REQ#_CPU — R449 0_4 — CPU_LDT_REQ# — CPU_LDT_REQ# 10

VFIX MODE

SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V

+1.8VSUS — CPU_TEST27_SINGLECHAIN R369 300_4; CPU_TEST25_L_BYPASSCLK_L R559 300_4

CPU_TEST18_PLLTEST1 R141; CPU_TEST19_PLLTEST0 R140; CPU_TEST15_BP1 R450; CPU_TEST14_BP0 R451 — 300_4

CPU_TEST21_SCANEN R383; CPU_TEST20_SCANCLK2 R371; CPU_TEST24_SCANCLK1 R372; CPU_TEST22_SCANSHIFTEN R370; CPU_TEST12_SCANSHIFTENB R379; CPU_TEST25_H_BYPASSCLK_H R560; CPU_TEST23_TSTUPD R561 — 300_4

HDT CONNECTOR

+1.8VSUS — R532 300_4 — CPU_DBREQ#

CN22 *ASP-68200-07-25P-LDV

CPU_DBRDY, CPU_TCK, CPU_TMS, CPU_TDI, CPU_TRST#, CPU_TDO

GND1, RSVD1, RSVD0, DBREQ_L, DBRDY, TCK, TMS, TDI, TRST_L, TDO, VCC_PROC_IO_21, VCC_PROC_IO_23, RESET_L, KEY, GND2, GND4, GND6, GND8, GND10, GND12, GND14, GND16, GND18, GND20, GND22, GND26

H_LDT_RST#

CPU H/W MONITOR

2/20/08' Reserve 0 ohm for CPU thermal issue on C-test

15 MIL

+3V — R112 47/F_6 3V_THM — C105 .1u/10V_4 — R615 *0_4 — CPU_THERMDC — C102 2200P_4 — CPU_THERMDA

10 mil trace / 10 mil space

Address 98H

U6 G781: VCC, DXN, DXP, -OVT, -ALT, SMDATA, SMCLK, GND

KBSMDAT, KBSMCLK

R105 10K_4 — Q37 2N7002E — To SB GPIO — THERM_ALERT# 13

R107 4.7K_4 — Q41 2N7002E — 2ND_MBDATA 25

R108 4.7K_4 — Q40 2N7002E — 2ND_MBCLK 25

R104 10K_4 — To FAN — CPUFAN#_ON 20

+1.8VSUS — R462 10K_4; R456 1K/F_4 — H_LDT_RST# — LDT_RST# — Q51 MMBT3904

Quanta Computer Inc.

PROJECT : ZY7

Size	Document Number	Rev
	AMD Griffin CTRL & DEBUG	1A

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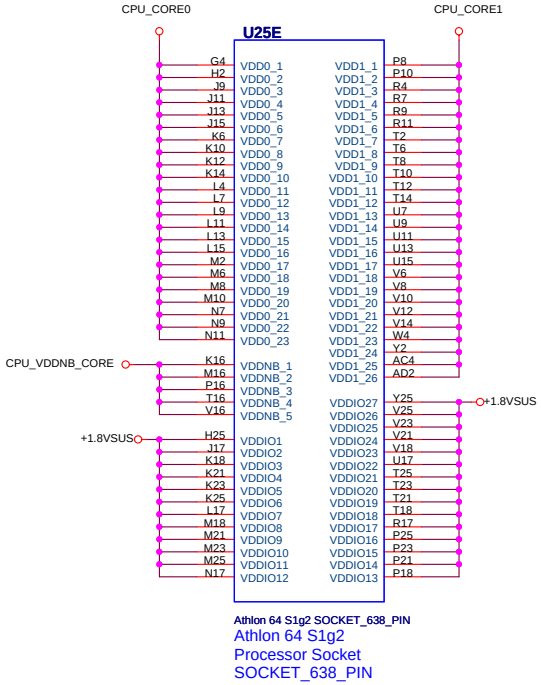
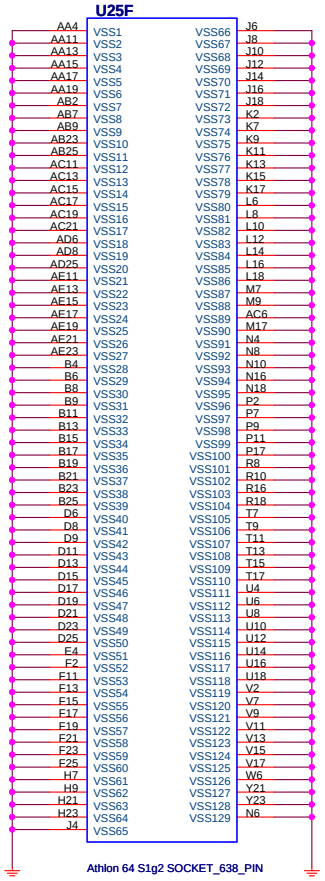
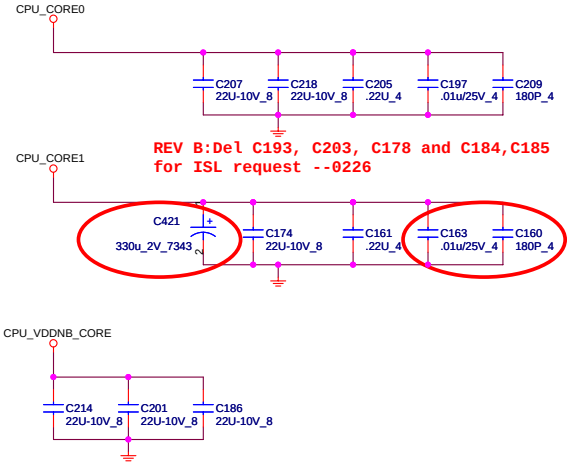
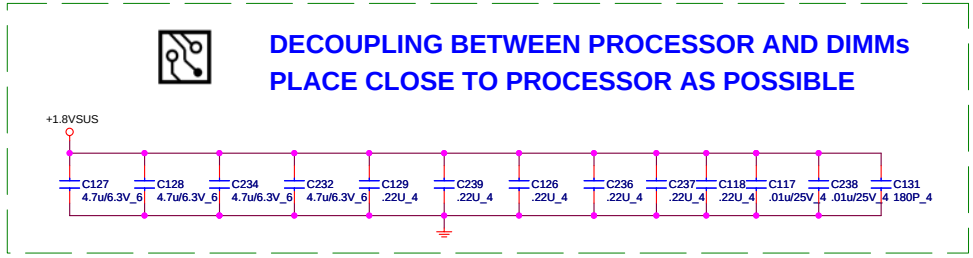
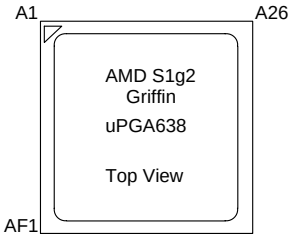
PROCESSOR POWER AND GROUND



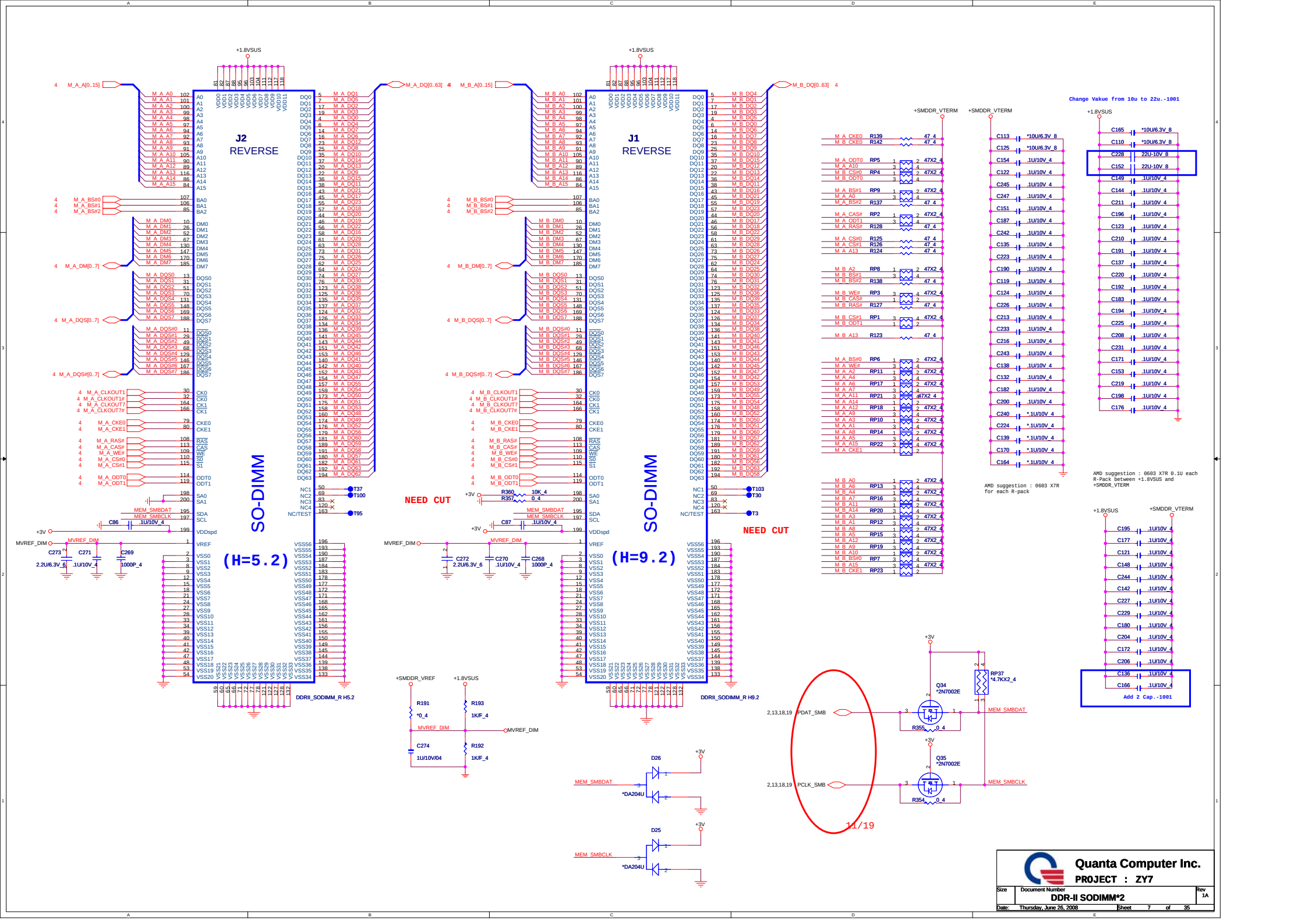








Quanta Computer Inc.		
PROJECT : ZY7		
Size	Document Number: AMD Griffin PWR & GND	Rev: 1A
Date: Thursday, June 26, 2008	Sheet 6 of 35	


J2
REVERSE
SO-DIMM
(H=5.2)
DDRII_SODIMM_R H5.2
J1
REVERSE
SO-DIMM
(H=9.2)
DDRII_SODIMM_R H9.2
NEED CUT
NEED CUT
+1.8VSUS
+SMDDR_VTERM
+SMDDR_VREF
+3V
MVREF_DIM
Change Vakue from 10u to 22u.-1001
AMD suggestion : 0603 X7R 0.1U each R-Pack between +1.8VSUS and +SMDDR_VTERM
AMD suggestion : 0603 X7R for each R-pack
Add 2 Cap.-1001
Q34 *2N7002E
Q35 *2N7002E
RP37 *4.7KX2_4
D26 *DA204U
D25 *DA204U
2,13,18,19 PDAT_SMB
2,13,18,19 PCLK_SMB
MEM_SMBDAT
MEM_SMBCLK
11/19
Quanta Computer Inc.
PROJECT : ZY7
DDR-II SODIMM*2
Rev 1A
Date: Thursday, June 26, 2008
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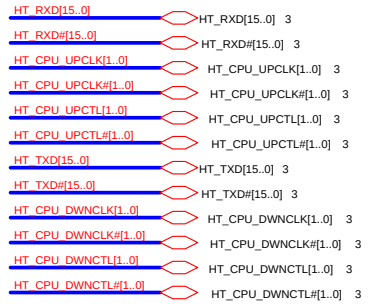
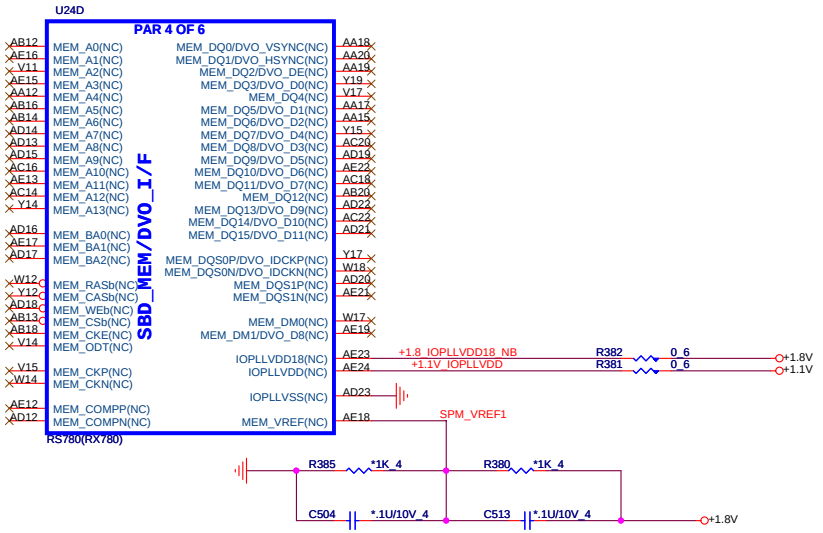


signals	RS780	RX780
HT_TXCALP	R641 301ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R661 301 ohm 1%	R661 1.21k ohm 1%
HT_RXCALN		

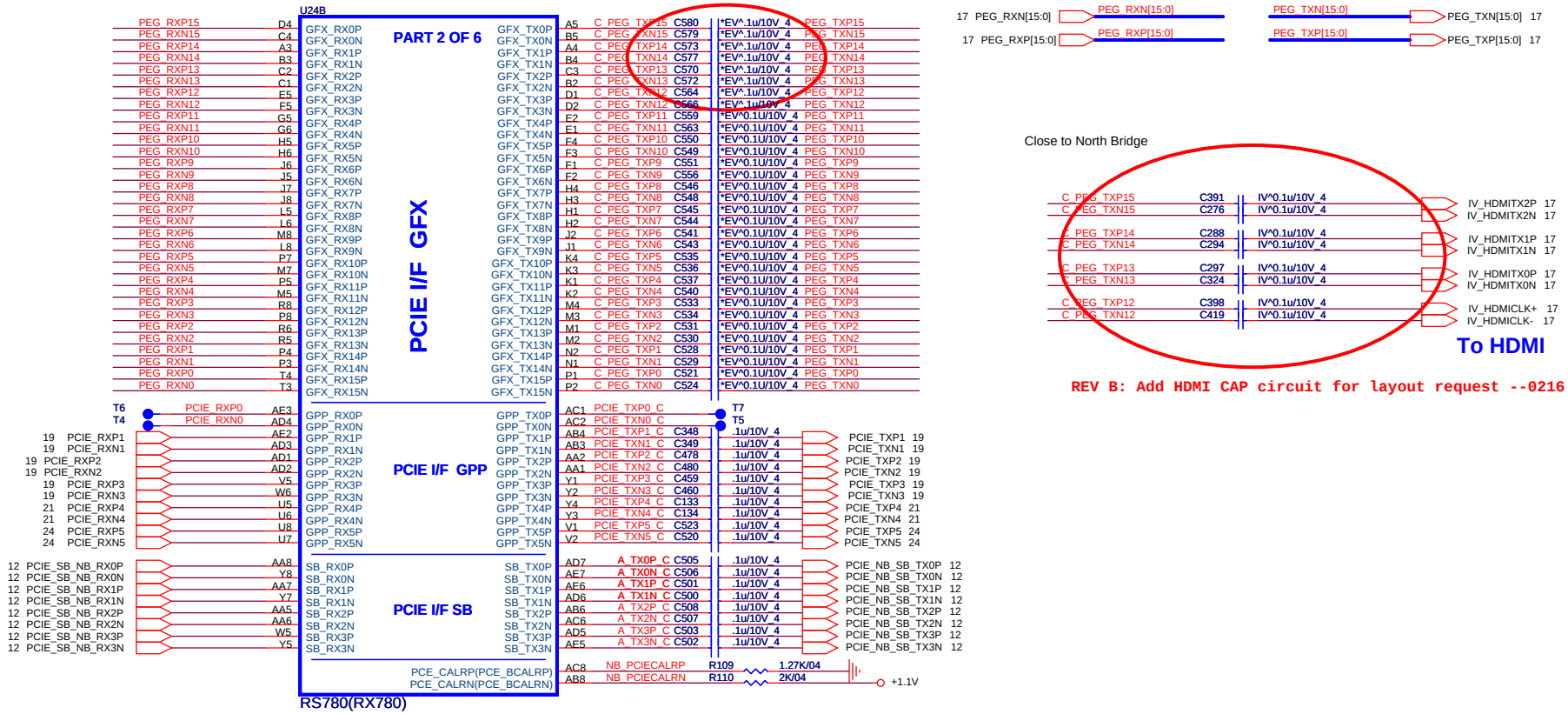
This block is for UMA RS780 only , RX780 can remove all component



Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	RS740/RS780-HT LINK I/F 1/4	1A

Date: Thursday, June 26, 2008 Sheet 8 of 35



Quanta Computer Inc.		
PROJECT : ZY7		
Size	Document Number: RX780/RS780-PCIE I/F 2/4	Rev: 1A
Date: Thursday, June 26, 2008	Sheet 9 of 35	

Need Check RGB Pull Low RES value!--1026

REV E: Change R393 value from 150ohm to 133ohm following AMD change---0214

RX780: Powered from the 1.8-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.
RS780: Powered from the 3.3-V rail and driven by SB600 LDT_RST#, or SB700 LDT_RST# or A_RST#.

RX780
5,12 CPU_LDT_RST# — R146 *0_4 — NB_RST#_IN
RS780
12 NB_PLTRST# — R155 0_4
North Bridge RESET

RS780 only
+3V — R418 4.7K/04 — HDTV_DET

RS780 only
VDDG_NB
R416 IV^4.7K/04 NB_I2C_DATA
R412 IV^4.7K/04 NB_I2C_CLK

Change PU from +3V to VDDG_NB.--1015

U24C — PART 3 OF 6 — RS780(RX780)

CRT/TVOUT
+3V_AVDD_NB — F12 AVDD1(NC)
E12 AVDD2(NC)
+1.8V_AVDDDI_NB — F14 AVDDDI(NC)
G15 AVSSDI(NC)
+1.8V_AVDDQ_NB — H15 AVDDQ(NC)
H14 AVSSQ(NC)

R136 *150R_4 TV_C/R1
R130 *150R_4 TV_Y/G1
R134 *150R_4 TV_COMP1
F17 C_Pr(DFT_GPIO5)
F17 Y(DFT_GPIO2)
F15 COMP_Pb(DFT_GPIO4)

17 INT_CRT_RED — R148 IV^0_4 — R149 IV^150R_4 — CRT_R_1 — G18 RED(DFT_GPIO0)
17 INT_CRT_GRN — R151 IV^0_4 — R150 IV^150R_4 — CRT_G_1 — G17 REDb(NC) / E18 GREEN(DFT_GPIO1)
17 INT_CRT_BLU — R152 IV^0_4 — R153 IV^150R_4 — CRT_B_1 — F18 GREENb(NC) / E19 BLUE(DFT_GPIO3)
F19 BLUEb(NC)

17 INT_HSYNC — R408 IV^0_4 — HSYNC_INT — A11 DAC_HSYNC(PWM_GPIO4)
17 INT_VSYNC — R407 IV^0_4 — VSYNC_INT — B11 DAC_VSYNC(PWM_GPIO6)
17 INT_CRT_DDCDAT — R162 IV^0_4 — DDCDATA_INT — E8 DAC_SDA(PCE_TCALRN)
17 INT_CRT_DDCCLK — R163 IV^0_4 — DDCCLK_INT — F8 DAC_SCL(PCE_RCALRN)
R159 715R/06 — DAC_RSET_NB — G14 DAC_RSET(PWM_GPIO1)

TXOUT_U0P(NC) A22 — INT_TXLOUT0 17
TXOUT_U0N(NC) B22 — INT_TXLOUT0# 17
TXOUT_L1P(NC) A21 — INT_TXLOUT1 17
TXOUT_L1N(NC) B21 — INT_TXLOUT1# 17
TXOUT_L2P(NC) B20 — INT_TXLOUT2 17
TXOUT_L2N(DBG_GPIO0) A20
TXOUT_L3P(NC) A19 — LA_DATAP3 — T24
TXOUT_L3N(DBG_GPIO2) B19 — LA_DATAN3 — T28

TXOUT_U0P(NC) B18 — INT_TXUOUT0 17
TXOUT_U0N(NC) A18 — INT_TXUOUT0# 17
TXOUT_U1P(PCIE_RESET_GPIO3) A17 — INT_TXUOUT1 17
TXOUT_U1N(PCIE_RESET_GPIO2) B17 — INT_TXUOUT1# 17
TXOUT_U2P(NC) D20 — INT_TXUOUT2 17
TXOUT_U2N(NC) D21 — INT_TXUOUT2# 17
TXOUT_U3P(PCIE_RESET_GPIO5) D18 — LB_DATAP3 — T21
TXOUT_U3N(NC) D19 — LB_DATAN3 — T23

TXCLK_LP(DBG_GPIO1) B16 — INT_TXCLKOUT 17
TXCLK_LN(DBG_GPIO3) A16 — INT_TXCLKOUT# 17
TXCLK_UP(PCIE_RESET_GPIO4) D16 — INT_TXUCLKOUT 17
TXCLK_UN(PCIE_RESET_GPIO1) D17 — INT_TXUCLKOUT# 17

PLL PWR LVTM
VDDLTP18(NC) A13 — +1.8V_VDDLTP18_NB
VSSLTP18(NC) B13
+1.1V_PLLVDD — A12 PLLVDD(NC)
+1.8V_PLLVDD18 — D14 PLLVDD18(NC)
B12 PLLVSS(NC)
+1.8V_VDDA18HTPLL — H17 VDDA18HTPLL
+1.8V_VDDA18PCIEPLL — D7 VDDA18PCIEPLL1
E7 VDDA18PCIEPLL2
VDDLT18_1(NC) A15 — +1.8V_VDDLT_18_NB
VDDLT18_2(NC) B15
VDDLT33_1(NC) A14
VDDLT33_2(NC) B14

PM
NB_RST#_IN — D8 SYSRESETb
16 NB_PWRGD_IN — NB_PWRGD_IN — A10 POWERGOOD
NB_LDT_STOP# — C10 LDTSTOPb
ALLOW_LDTSTOP — C12 ALLOW_LDTSTOP

VSSLT1(VSS) C14
VSSLT2(VSS) D15
VSSLT3(VSS) C16
VSSLT4(VSS) C18
VSSLT5(VSS) C20
VSSLT6(VSS) E20
VSSLT7(VSS) C22

RS780 only

2 NBHT_REFCLKP — NBHT_REFCLKP — C25 HT_REFCLKP
2 NBHT_REFCLKN — NBHT_REFCLKN — C24 HT_REFCLKN

CLOCKs
2 EXT_NB_OSC — R167 0R/04 — R166 0_4 — NB_REFCLK_P — NB_REFCLK_N — E11 REFCLK_P/OSCIN(OSCIN) / F11 REFCLK_N(PWM_GPIO3)
+1.1V — R171 4.7K/04 — R172 4.7K/04
NBGFX_CLKP — T2 GFX_REFCLKP
NBGFX_CLKN — T1 GFX_REFCLKN
2 NBGFX_CLKP
2 NBGFX_CLKN
2 NBGPP_CLKP
2 NBGPP_CLKN
2 SBLINK_CLKP
2 SBLINK_CLKN
NBGPP_CLKP — U1 GPP_REFCLKP
NBGPP_CLKN — U2 GPP_REFCLKN
SBLINK_CLKP — V4 GPPSB_REFCLKP(SB_REFCLKP)
SBLINK_CLKN — V3 GPPSB_REFCLKN(SB_REFCLKN)

LVDS_DIGON(PCE_TCALRP) E9 — R164 IV^0_4 — INT_LVDS_DIGON 17
LVDS_BLON(PCE_RCALRP) F7 — R157 IV^0_4 — INT_LVDS_BL_BRGHT 18
LVDS_ENA_BL(PWM_GPIO2) G12 — R144 IV^0_4 — INT_LVDS_BLON 17
SWAP BLON/BRGHT.--1108

17 INT_LVDS_EDIDDATA — R414 IV^0_4 — NB_I2C_DATA — A9 I2C_DATA
17 INT_LVDS_EDIDCLK — R415 IV^0_4 — NB_I2C_CLK — B9 I2C_CLK
17 INT_HDMI_DATA — R410 IV^0_4 — HDTV_DET — B8 DDC_DATA/AUX0N(NC)
17 INT_HDMI_CLK — R409 IV^0_4 — A8 DDC_CLK/AUX0P(NC)
B7 AUX1P(NC)
A7 AUX1N(NC)

MIS.
T99 — RS740_DFT_GPIO0
T101 — RS740_DFT_GPIO1
30 +NB_CORE_ON — R428 0_4 — STRP_DATA — B10 STRP_DATA
G11 RSVD
T102 — RS780_AUX_CAL — C8 AUX_CAL(NC)

TMDS_HPD(NC) D9 — INT_HDMI_HPD_R — R417 IV^0_4 — INT_HDMI_HPD 17
HPD(NC) D10 — TMDS_HPD1 — T98
TVCLKIN(PWM_GPIO5) D12 — SUS_STAT#_NB — R168 0R/04 — SUS_STAT# 13
THERMALDIODE_P AE8 — R_NB_THRMDA — T96
THERMALDIODE_N AD8 — R_NB_THRMDC — T97
TESTMODE D13 — TEST_EN
R413 1.82K/04

selects Loading of straps from EPROM
1 : use default vaule , default
0 : I2C Master can load strap values from EEPROM
if connected, or use default values if not connected
RX780 --RS780_AUX_CAL
RS780 -- SUS_ATAT

RX780
RS780_AUX_CAL — R419 *3K/04

Enables Debug Bus acess through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)

RS780
INT_VSYNC — R424 3K_4 — +3V

Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)

RS780
INT_HSYNC — R426 3K/04 — +3V
R425 *3K_4

For extrnal EEPROM Debug only

RS780/RX780
STRP_DATA — R423 *10K_4 — VDDG_NB
R427 2.2K_4

REV B: Change PU from +3V_S5 to +3V follow AMD CRB suggest.--0201

+3V — L21 TI160808U300 — +3V_AVDD_NB — C241 10U/6.3V/06
AVDD-DAC Analog not applicable to RX780

+1.1V — L56 BLM18PG221SN1D — +1.1V_PLLVDD — C575 2.2U/6.3V/06
PLLVDD - Graphics PLL not applicable to RX780

+1.8V — L22 TI160808U300 — +1.8V_PLLVDD18 — C248 10U/6.3V/08 — C217 10U/6.3V/06
PLLVDD18 - Graphics PLL not applicable to RX780

+1.8V — R158 TI160808U300 — +1.8V_AVDDDI_NB — C221 10U/6.3V/06
AVDDI-DAC Digital not applicable to RX780

L20 TI160808U300 — +1.8V_AVDDQ_NB — C215 10U/6.3V/06
AVDDQ-DAC Bandgap Reference not applicable to RX780

+1.8V — BLM18PG221SN1D L55 — +1.8V_VDDLTP18_NB — C574 2.2U/6.3V/06 — C601 100p/50V_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

BLM21PG221SN1D L53 — +1.8V_VDDLT_18_NB — C646 100p/50V_6 — C576 4.7u/6.3V_6 — C571 .1U/10V_4
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

REV B: Add C601,C646,C647,C648 100PF for EMI request.--0201

+1.8V — TI160808U300 L18 — 20mils width — +1.8V_VDDA18PCIEPLL — C230 4.7U/6.3V/06
VDDA18PCIEPLL -PCIE PLL

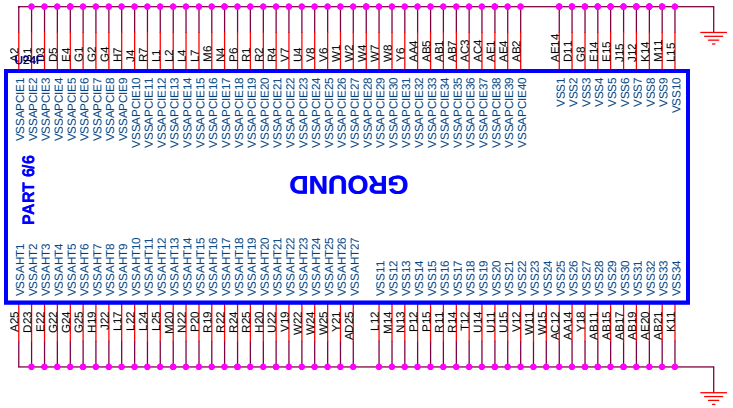
L17 TI160808U300 — 20mils width — +1.8V_VDDA18HTPLL — C647 100p/50V_6 — C107 4.7U/6.3V/06
VDDA18HTPLL -HT LINK PLL

+1.8V — R452 *4.7K_4 — VDDG_NB
5,12 CPU_LDT_STOP# — Q30 *BSS138_NL/SOT23 — NB_LDT_STOP#
R459 0_4
C:REV Change it follow AMD suggest.

5 CPU_LDT_REQ# — R460 0_4 — ALLOW_LDTSTOP
12 ALLOW_LDTSTOP

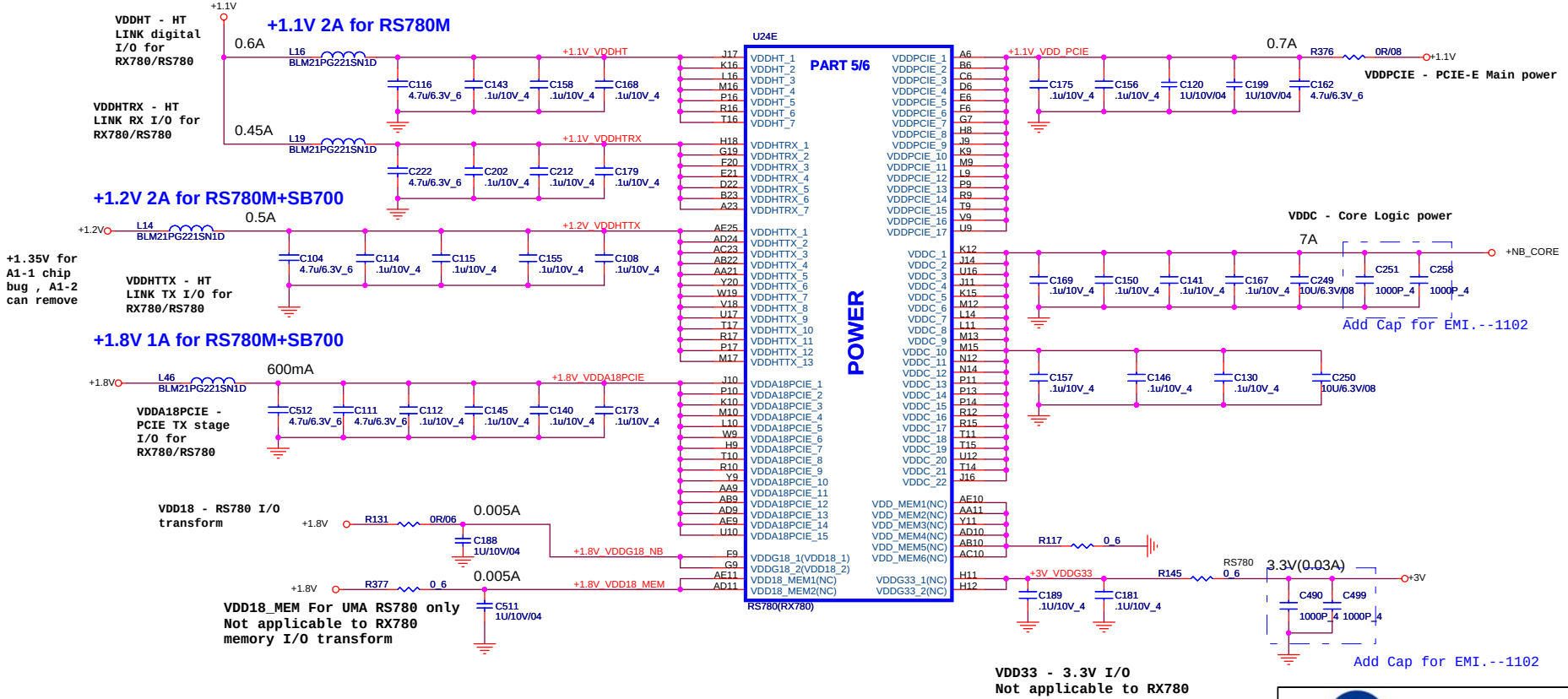
RX780 — R457 *0R/06 — +1.8V — VDDG_NB
RS780 — R458 0_6 — +3V
C648 100p/50V_6

Quanta Computer Inc.
PROJECT : ZY7
Size — Document Number: RX780/RS780-SYS I/F 3/4 — Rev 1A
Date: Thursday, June 26, 2008 — Sheet 10 of 35

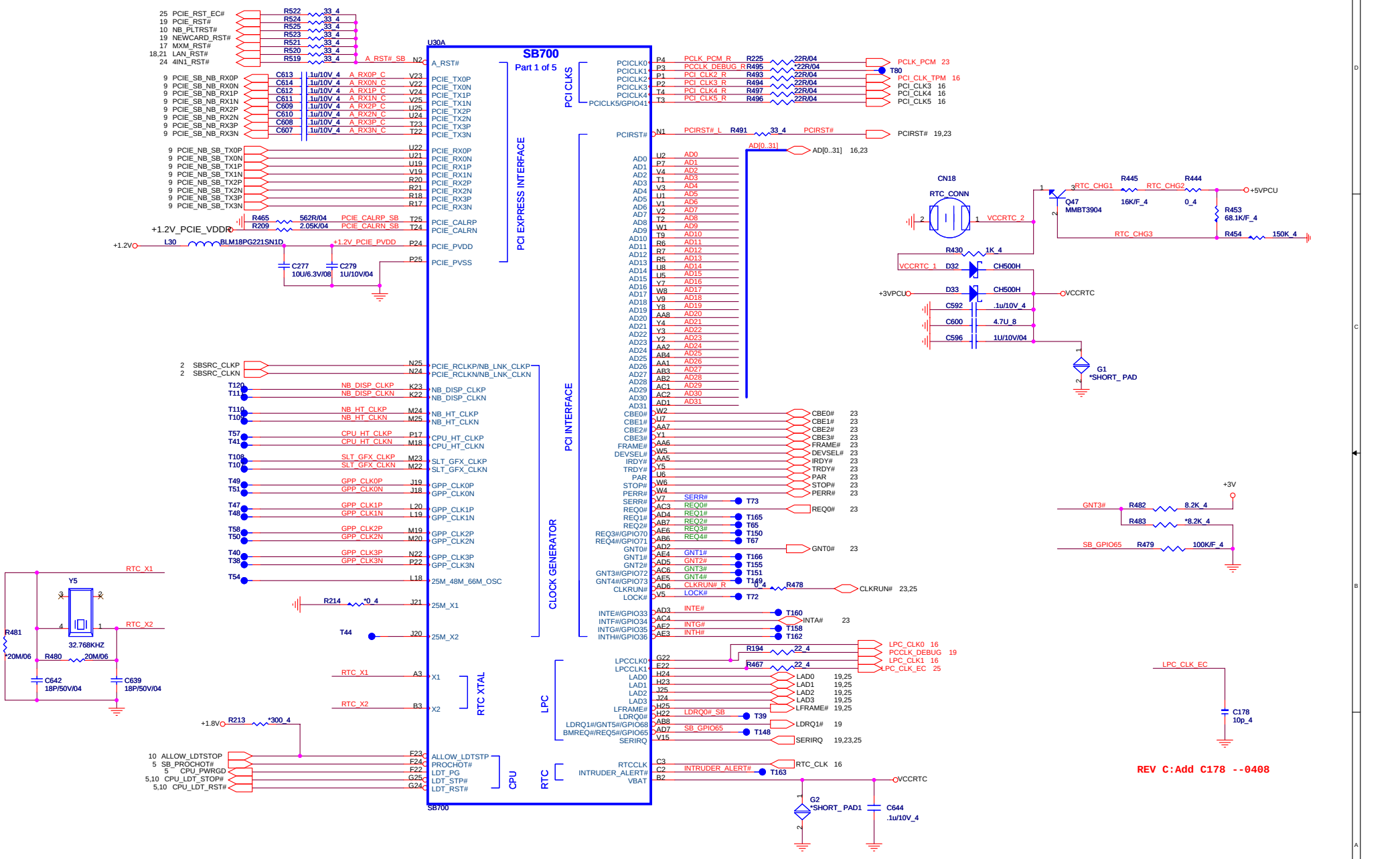


RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC



Quanta Computer Inc.	
PROJECT : ZY7	
Size	Document Number: RX780/RS780-POWER 4/4 — Rev: 1A
Date: Thursday, June 26, 2008	Sheet 11 of 35



Quanta Computer Inc.			
PROJECT : ZY7			
Size	Document Number		Rev
	SB700-PCIE/PCI/CPU/LPC 1/4		1A
Date: Thursday, June 26, 2008	Sheet 12	of 35	

NC only ,Can't be install

R518 *2.2K_4 SB_TEST0
R233 *2.2K/04 SB_TEST1
R232 *2.2K/04 SB_TEST2

Add Pull high RES.--1011

+3V R464 4.7K_4 KBSMI#

R504 *10K/04 SWI#

SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R472 2.2K_4 PCLK_SMB
R473 2.2K_4 PDAT_SMB

Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

SCL1/SDATA1 is 3V/5S tolerance
AMD datasheet define it
R488 2.2K_4 MSMB_CLK
R487 2.2K_4 MSMB_DATA
Change Net name .-1001

SCL2/SDATA2 is 3V/5S tolerance
AMD datasheet define it
epress card
R210 2.2K_4 SB_SCLK2
R208 2.2K_4 SB_SDATA2

R238 4.7K/04 SUS_STAT#
R463 *10K_4 SB_NWD_CLK_REQ#

G3 *SHORT_PAD1 SYS_RST#

Add HDA for MXM.--1015

Ver D: Change---0520

To Azalia

ACZ_SDOUT R511 33R/04 ACZ_SDOUT_AUDIO 22
R490 *EV^33R/04 ACZ_SDOUT_MXM 17
ACZ_SYNC R242 33R/04 ACZ_SYNC_AUDIO 22
R243 *EV^33R/04 ACZ_SYNC_MXM 17
ACZ_BCLK R505 33R/04 ACZ_BITCLK_AUDIO 22
R489 *EV^33R/04 ACZ_BITCLK_MXM 17
ACZ_RST# R236 33R/04 ACZ_RESET#_AUDIO 22
R235 *EV^33R/04 ACZ_RESET#_MXM 17
ACZ_SDIN2_R R217 0R/04 ACZ_SDIN2 17

ACZ_SDIN0_R R221 0R/04 ACZ_SDIN0 22

To Modem Board

ACZ_SDOUT R510 33R/04 ACZ_SDOUT_MDC 22
ACZ_SYNC R240 33R/04 ACZ_SYNC_MDC 22
ACZ_BCLK R506 33R/04 ACZ_BITCLK_MDC 22
ACZ_RST# R237 33R/04 ACZ_RESET#_MDC 22
ACZ_SDIN1_R R241 0R/04 ACZ_SDIN1 22

For EMI
ACZ_SDOUT C650 *10p_4
ACZ_SYNC C344 *10p_4
ACZ_BCLK C649 *10p_4
ACZ_RST# C345 *10p_4
ACZ_SDIN0_R C329 *10p_4
ACZ_SDIN1_R C336 *10p_4

U30D SB700 Part 4 of 5

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOCO#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
GPIO

USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
HD AUDIO

IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
INTEGRATED uC

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB MISC

USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB 1.1

USB_HSD11P/N TV Min-Card
USB_HSD10P/N Fingerprint
USB_HSD9P/N
USB_HSD8P/N USB Connector
USB_HSD7P/N Docking
USB_HSD6P/N BLUETOOTH
USB_HSD5P/N EXT USB Connector
USB_HSD4P/N EXT USB Connector
USB_HSD3P/N EXT USB Connector
USB_HSD2P/N Carama USB
USB_HSD1P/N Wirless Min-Card
USB_HSD0P/N USB Connector
USB 2.0

IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPO16
IMC_PWM3/IMC_GPO17
SPI/LPC define

IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
INTEGRATED uC

HD audio interface is 3.3V voltage

Add GPIO pin.--1008

SB700

CLK_48M_USB
R222 *10_6
C327 *10p_4
for EMI

SB JTAG
CN8
C319 10p_4
SB_JTAG_TCK
SB_JTAG_TDO
CPPE#_EC
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG

Quanta Computer Inc.
PROJECT : ZY7
Size
Document Number SB700-ACPI/GPIO/USB 2/4
Rev 1A
Date: Thursday, June 26, 2008 Sheet 13 of 35

SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

U30B

SB700
Part 2 of 5

SATA1
SATA2
SATA ODD

SERIAL ATA

ATA 66/100/133

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

SPI ROM

HW MONITOR

SATA PWR

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:
R361 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

5mA

Change from +3V to +3V_S5.--1212

AVDD--H/W monitor Analog power

77mA

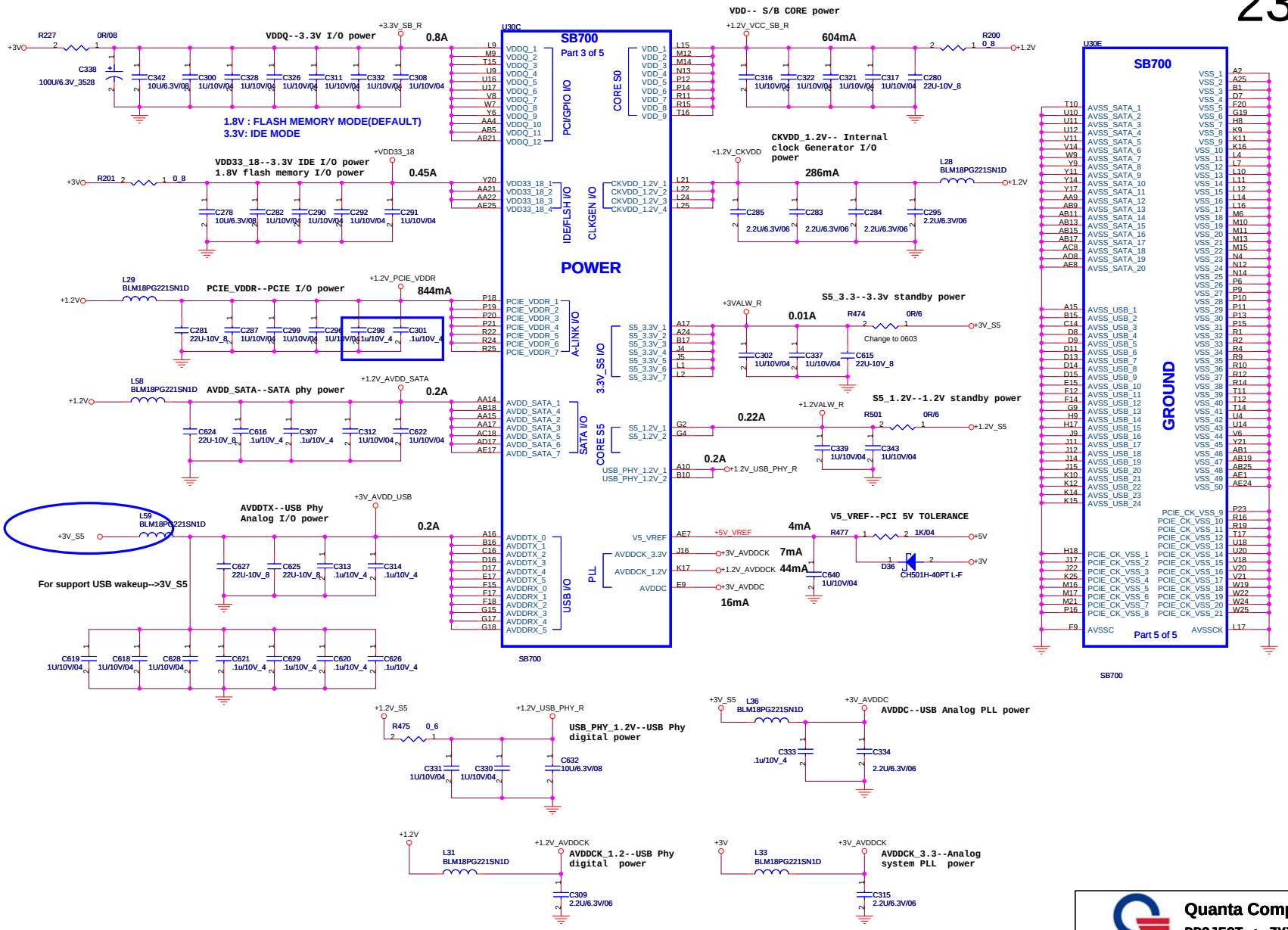
1mA

Place near ball

SB700

Quanta Computer Inc. PROJECT : ZY7			
Size	Document Number SB700-SATA/IDE/HWM/SPI 3/4		Rev 1A
Date: Thursday, June 26, 2008	Sheet 14 of 35		

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

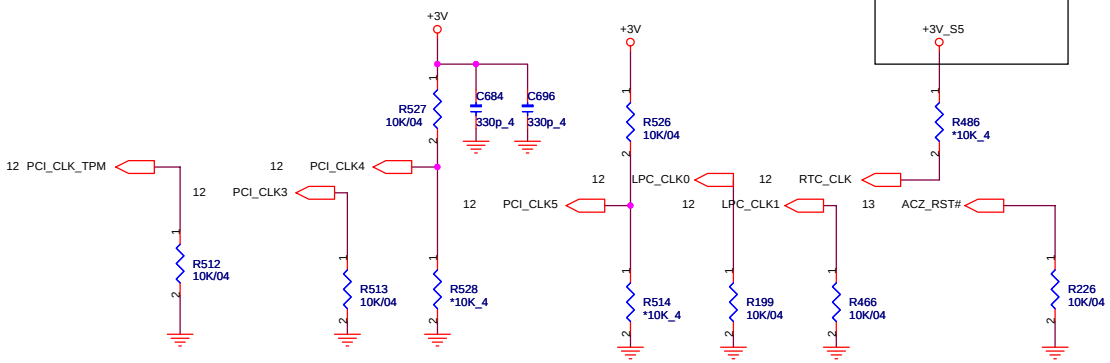


Quanta Computer Inc.	
PROJECT : ZY7	
Size	Document Number: SB700-PWR/DECOUPLING 4/4 — Rev: 1A
Date: Thursday, June 26, 2008	Sheet 15 of 35

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

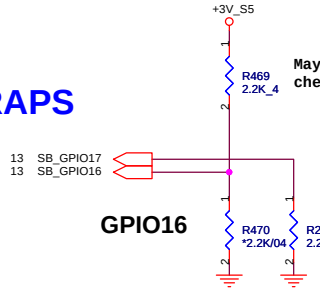
REV C:Add C684 and C696 --0408

It must ready refore RSMRST#



	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

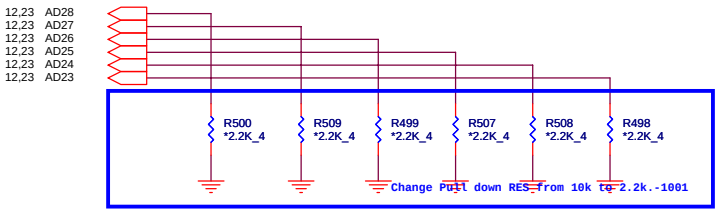
REQUIRED STRAPS



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

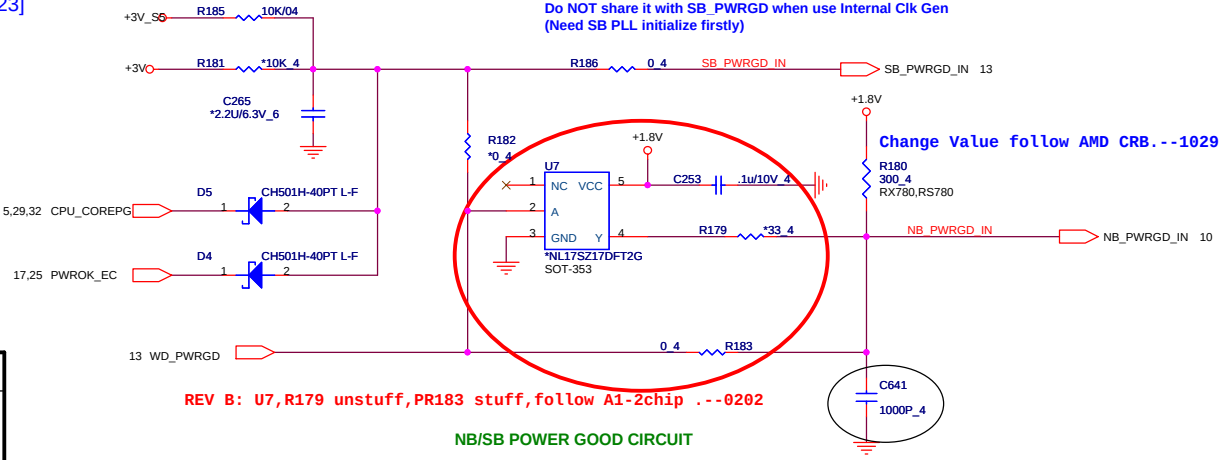
DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



REV B: U7,R179 unstuff,PR183 stuff,follow A1-2chip .--0202

NB/SB POWER GOOD CIRCUIT

REV B: Add 1N Capacitor to Smoothing NB_PWRGD_IN ---0202

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

Quanta Computer Inc.
PROJECT : ZY7

Size	Document Number	Rev
	SB700-STRAPS,PWRGD	1A
Date: Thursday, June 26, 2008	Sheet 16 of 35	

REV B:Del MXM_POWEREN circuit
follow AMD request--0214

CN16B

LVDS_TXUCK# 148 LVDS_UCLK#
LVDS_TXUCK 150 LVDS_UCLK
LVDS_TXU0# 172 LVDS_UTX0#
LVDS_TXU1# 166 LVDS_UTX1#
LVDS_TXU2# 160 LVDS_UTX2#
154 LVDS_UTX3#
LVDS_TXU0 174 LVDS_UTX0
LVDS_TXU1 168 LVDS_UTX1
LVDS_TXU2 162 LVDS_UTX2
156 LVDS_UTX3
LVDS_TXLCK# 178 LVDS_LCLK#
LVDS_TXLCK 180 LVDS_LCLK
LVDS_TXL0# 202 LVDS_LTX0#
LVDS_TXL1# 196 LVDS_LTX1#
LVDS_TXL2# 190 LVDS_LTX2#
184 LVDS_LTX3#
LVDS_TXL0 204 LVDS_LTX0
LVDS_TXL1 198 LVDS_LTX1
LVDS_TXL2 192 LVDS_LTX2
186 LVDS_LTX3
LCD_ON 212 LVDS_PPEN
LVDS_BLON 216 LVDS_BLEN
214 LVDS_BL_BRGHT
18 EV_LVDS_BL_BRGHT — EV_LVDS_BL_BRGHT
LCD_EDIDCLK 210 DDCC_CLK
LCD_EDIDDAT 208 DDCC_DAT

LVDS / DVI / HDMI / DVI-A / DVI-B

HDMI_DVI_CLK# / DVI_A_CLK# 207 HDMI_CLK#
HDMI_DVI_CLK / DVI_A_CLK 209 HDMI_CLK
HDMI_DVI_TX0# / DVI_A_TX0# 225 HDMI_TX0#
HDMI_DVI_TX1# / DVI_A_TX1# 219 HDMI_TX1#
HDMI_DVI_TX2# / DVI_A_TX2# 213 HDMI_TX2#
HDMI_DVI_TX0 / DVI_A_TX0 227 HDMI_TX0
HDMI_DVI_TX1 / DVI_A_TX1 221 HDMI_TX1
HDMI_DVI_TX2 / DVI_A_TX2 215 HDMI_TX2
HDMI_DVI_HPD / DVI_A_HPD 205 HDMI_HPD
DDCB_CLK 220 HDMI_DCCLK
DDCB_DAT 218 HDMI_DCDATA
DP_L0 / IGP/DVI_B_CLK# 177
DP_L0# / IGP/DVI_B_CLK 179
DP_L1 / IGP/DVI_B_TX0# 201
DP_L2 / IGP/DVI_B_TX1# 195
DP_L3 / IGP_/DVI_B_TX2# 189
DP_L1# / IGP/DVI_B_TX0 203
DP_L2# / IGP/DVI_B_TX1 197
DP_L3# / IGP_DVI_B_TX2 191
DP_HPD / DVI_B_HPD/GND 181 — DVI_B_HPD R365 *EV^100K_4

CRT

CRTHSYNC 139 VGA_HSYNC
CRTVSYNC 141 VGA_VSYNC
VGA_RED 136 VGA_RED
VGA_GRN 140 VGA_GREEN
VGA_BLU 144 VGA_BLUE
CRTDCLK 143 DDCA_CLK
CRTDDAT 145 DDCA_DAT
HDA_SDI / IGP 147 — SDIN2_MXM R390 *EV^22_4 — R607 *0_4 — ACZ_SDIN2 13 / ACZ_SDOUT_MXM 13
HDA_SDO / IGP
IGP_RSVD / IGP 151
DP_AUX# / IGP 159
DP_AUX / IGP 161
IGP_RSVD / IGP 163
IGP_RSVD / IGP 165
IGP_RSVD / IGP 167
IGP_RSVD / IGP 169
IGP_RSVD / IGP 171
IGP_RSVD / IGP 173

TV

128 TV_Y/HDTV_Y/TV_CVBS
124 TV_C/HDTV_Pr
132 TV_CVBS/HDTV_Pb
RSVD 185
RSVD 183
IGP_RSVD / RSVD 155
IGP_RSVD / RSVD 153
HDA_BCLK / RSVD 131 — R608 *0_4 — ACZ_BITCLK_MXM 13
HDA_SYNC / RSVD 129 — R609 *0_4 — ACZ_SYNC_MXM 13

20,25 VGA_THERM# — VGA_THERM# 137 THERM#
133 SMB_DAT
135 SMB_CLK
*EV^MXM_TYPEII
RUNPWROK 16 — R443 *EV^0_4 — PWROK_EC 16,25
AC/BATT# 157 — R461 *0_4 — PWROK_MXM 25

18,25 MXM_DATA — Q42 *EV^2N7002 — 3 / 1
+3V — Q43 *EV^2N7002 — 3 / 1
18,25 MXM_CLK — VTHM_CLK

D30 *BAS316 ACIN
R386 *10K_4 — +3V
Q38 *EV^DTA114YUA — R378 *EV^10K_4
13 ACZ_RESET#_MXM
R610 *0_4
Q39 *EV^2N7002 — ACIN 25,27
22 MXM_SPDIF_OUT
MXM_SPDIF_OUT

VIN
CN16A

*EV^10u/25V_1206 C603 — 1 PWR_SRC
*EV^1u/25V_6 C591 — 3 PWR_SRC
*EV^1000p_4 C586 — 5 PWR_SRC
7 PWR_SRC
9 PWR_SRC
11 PWR_SRC
13 PWR_SRC
15 PWR_SRC
*EV^1u/10V_4 C582 — +5V
*EV^1u/16V_4 C583
*EV^1000p_4 C581 — 18 5VRUN
+3V
*EV^10u/6.3V_6 C487 — 226 3V3RUN
*EV^1u/16V_4 C488 — 228 3V3RUN
*EV^1000p_4 C489 — 230 3V3RUN
+2.5V
*EV^1u/10V_4 C496
*EV^1u/16V_4 C495
*EV^1000p_4 C493 — 222 2V5RUN
+1.8V
*EV^100u/6.3V_3528 C604 — 2 / 4 1V8RUN
*EV^10u/10V_8 C598 — 6 / 8 1V8RUN
*EV^1u/10V_8 C595 — 10 1V8RUN
*EV^1u/16V_4 C589 — 12 1V8RUN
14 1V8RUN

17 GND
19 GND
20 GND
21 GND
22 GND
23 GND
24 GND
29 GND
32 GND
35 GND
38 GND
41 GND
44 GND
47 GND
50 GND
53 GND
56 GND
59 GND
62 GND
65 GND
68 GND
71 GND
74 GND
77 GND
80 GND
83 GND
86 GND
89 GND
92 GND
95 GND
98 GND
101 GND
104 GND
107 GND
110 GND
113 GND
116 GND
119 GND
126 GND
130 GND
134 HDA_RST# / GND
138 GND
142 GND
146 GND
152 GND
158 SPDIF / GND
164 GND
170 GND
175 GND
176 GND
182 GND
187 GND
188 GND
193 GND
194 GND
199 GND
200 GND
206 GND
211 GND
217 GND
223 GND
224 GND
229 GND

CLK_REQ# 125
R397 *0_4 — PE_RESET_MXM# 13
PEX_RST# 127 — R398 *EV^0_4 — MXM_RST# 12
PEX_REFCLK# 121 — CLK_PCIE_MXM# 2
PEX_REFCLK 123 — CLK_PCIE_MXM 2

PEG_RXN[15:0] 9
PEX_RX0# 115 PEG_RXN0
PEX_RX1# 109 PEG_RXN1
PEX_RX2# 103 PEG_RXN2
PEX_RX3# 97 PEG_RXN3
PEX_RX4# 91 PEG_RXN4
PEX_RX5# 85 PEG_RXN5
PEX_RX6# 79 PEG_RXN6
PEX_RX7# 73 PEG_RXN7
PEX_RX8# 67 PEG_RXN8
PEX_RX9# 61 PEG_RXN9
PEX_RX10# 55 PEG_RXN10
PEX_RX11# 49 PEG_RXN11
PEX_RX12# 43 PEG_RXN12
PEX_RX13# 37 PEG_RXN13
PEX_RX14# 31 PEG_RXN14
PEX_RX15# 25 PEG_RXN15

PEG_RXP[15:0] 9
PEX_RX0 117 PEG_RXP0
PEX_RX1 111 PEG_RXP1
PEX_RX2 105 PEG_RXP2
PEX_RX3 99 PEG_RXP3
PEX_RX4 93 PEG_RXP4
PEX_RX5 87 PEG_RXP5
PEX_RX6 81 PEG_RXP6
PEX_RX7 75 PEG_RXP7
PEX_RX8 69 PEG_RXP8
PEX_RX9 63 PEG_RXP9
PEX_RX10 57 PEG_RXP10
PEX_RX11 51 PEG_RXP11
PEX_RX12 45 PEG_RXP12
PEX_RX13 39 PEG_RXP13
PEX_RX14 33 PEG_RXP14
PEX_RX15 27 PEG_RXP15

PEG_TXN[15:0] 9
PEX_TX0# 118 PEG_TXN0
PEX_TX1# 112 PEG_TXN1
PEX_TX2# 106 PEG_TXN2
PEX_TX3# 100 PEG_TXN3
PEX_TX4# 94 PEG_TXN4
PEX_TX5# 88 PEG_TXN5
PEX_TX6# 82 PEG_TXN6
PEX_TX7# 76 PEG_TXN7
PEX_TX8# 70 PEG_TXN8
PEX_TX9# 64 PEG_TXN9
PEX_TX10# 58 PEG_TXN10
PEX_TX11# 52 PEG_TXN11
PEX_TX12# 46 PEG_TXN12
PEX_TX13# 40 PEG_TXN13
PEX_TX14# 34 PEG_TXN14
PEX_TX15# 28 PEG_TXN15

PEG_TXP[15:0] 9
PEX_TX0 120 PEG_TXP0
PEX_TX1 114 PEG_TXP1
PEX_TX2 108 PEG_TXP2
PEX_TX3 102 PEG_TXP3
PEX_TX4 96 PEG_TXP4
PEX_TX5 90 PEG_TXP5
PEX_TX6 84 PEG_TXP6
PEX_TX7 78 PEG_TXP7
PEX_TX8 72 PEG_TXP8
PEX_TX9 66 PEG_TXP9
PEX_TX10 60 PEG_TXP10
PEX_TX11 54 PEG_TXP11
PEX_TX12 48 PEG_TXP12
PEX_TX13 42 PEG_TXP13
PEX_TX14 36 PEG_TXP14
PEX_TX15 30 PEG_TXP15

PAD1 231
PAD2 232
PRSNT1# 122
PRSNT2# 26
R396 *EV^0_4 — MXM_PRESENT# 14

*EV^MXM_TYPEII

10 INT_CRT_RED — R394 IV^0_4 — VGA_RED 18
10 INT_CRT_GRN — R392 IV^0_4 — VGA_GRN 18
10 INT_CRT_BLU — R391 IV^0_4 — VGA_BLU 18
10 INT_HSYNC — R120 IV^0_4 — CRTHSYNC 18
10 INT_VSYNC — R121 IV^0_4 — CRTVSYNC 18
10 INT_CRT_DDCCLK — R119 IV^0_4 — CRTDCLK 18
10 INT_CRT_DDCDAT — R118 IV^0_4 — CRTDDAT 18
10 INT_LVDS_BLON — R356 IV^0_4 — LVDS_BLON 18
10 INT_LVDS_DIGON — R359 IV^0_4 — LCD_ON 18
RN20 IV^0_4P2R
10 INT_LVDS_EDIDDATA — LCD_EDIDDAT 18
10 INT_LVDS_EDIDCLK — LCD_EDIDCLK 18
RN6 IV^0_4P2R
10 INT_HDMI_CLK — HDMI_DCCLK 18
10 INT_HDMI_DATA — HDMI_DCDATA 18
10 INT_HDMI_HPD — R147 IV^0_4 — HDMI_HPD 18

18 LVDS_TXLCK# — RN24 IV^0_4P2R — INT_TXLCLKOUT# 10
18 LVDS_TXLCK — INT_TXLCLKOUT 10
18 LVDS_TXL0# — RN21 IV^0_4P2R — INT_TXLOUT0# 10
18 LVDS_TXL0 — INT_TXLOUT0 10
18 LVDS_TXL1# — RN22 IV^0_4P2R — INT_TXLOUT1# 10
18 LVDS_TXL1 — INT_TXLOUT1 10
18 LVDS_TXL2# — RN23 IV^0_4P2R — INT_TXLOUT2# 10
18 LVDS_TXL2 — INT_TXLOUT2 10
18 LVDS_TXUCK# — RN28 IV^0_4P2R — INT_TXUCLKOUT# 10
18 LVDS_TXUCK — INT_TXUCLKOUT 10
18 LVDS_TXU0# — RN25 IV^0_4P2R — INT_TXUOUT0# 10
18 LVDS_TXU0 — INT_TXUOUT0 10
18 LVDS_TXU1# — RN26 IV^0_4P2R — INT_TXUOUT1# 10
18 LVDS_TXU1 — INT_TXUOUT1 10
18 LVDS_TXU2# — RN27 IV^0_4P2R — INT_TXUOUT2# 10
18 LVDS_TXU2 — INT_TXUOUT2 10
18 HDMI_CLK — RN19 IV^0_4P2R — IV_HDMICLK+ 9
18 HDMI_CLK# — IV_HDMICLK- 9
18 HDMI_TX0 — RN16 IV^0_4P2R — IV_HDMITX0P 9
18 HDMI_TX0# — IV_HDMITX0N 9
18 HDMI_TX1 — RN17 IV^0_4P2R — IV_HDMITX1P 9
18 HDMI_TX1# — IV_HDMITX1N 9
18 HDMI_TX2 — RN18 IV^0_4P2R — IV_HDMITX2P 9
18 HDMI_TX2# — IV_HDMITX2N 9

Quanta Computer Inc.
PROJECT : ZY7
Size | Document Number: MXM | Rev: 1A
Date: Thursday, June 26, 2008 | Sheet 17 of 35

REV C: unstuff R3, Q1,Q4,Q5, Add and stuff D17, D21---0410

To IV/EV VGA Hot Plug Detect

Quanta Computer Inc.	
PROJECT : ZY7	
Size	Document Number: LVDS/CRT/TVOUT/CCD/DVI
Rev	1A
Date: Thursday, June 26, 2008	Sheet 18 of 35

To NEW-CARD & EXT. USB

650mA 2A 1.3A 275mA

CN9

NEW CARD_CON20X2

CL-2M2012-121JT

REV B:Modify it for EMI.--0218

Fingerprint

CN7

Finger_H1.95

*DLW21HN900SQ2L

REV C:Add R198 and R207 --0408

MODULE 'A' TV card

MODULE 'B' Wireless card

Double Stack MINI CARD

Bluetooth

Q29 AO3403

20mil

USB_BT_5P

*DLW21HN900SQ2L

INT. USB

REV B:Modify it for ESD issue on 2/20

CN21

CL-2M2012-121JT

R0IV18_ESD

SYUIN_USB

Add CAP--1107

U8 RT9711BPF

60mil

MINI-CARD

CAPACITOR on Module

REV B:Modify footprint--- 2/22

MODULE 'A' MODULE 'B'

CN33

SP@QUASAR-CA0404-071N21_92P

A/B MODULE Share pin

Modify it for Debug.--1017.

TV use +3V

TV use +5V

For EMI

Debug

+3V for WWAN card is 2.75A

500mA, 25mil

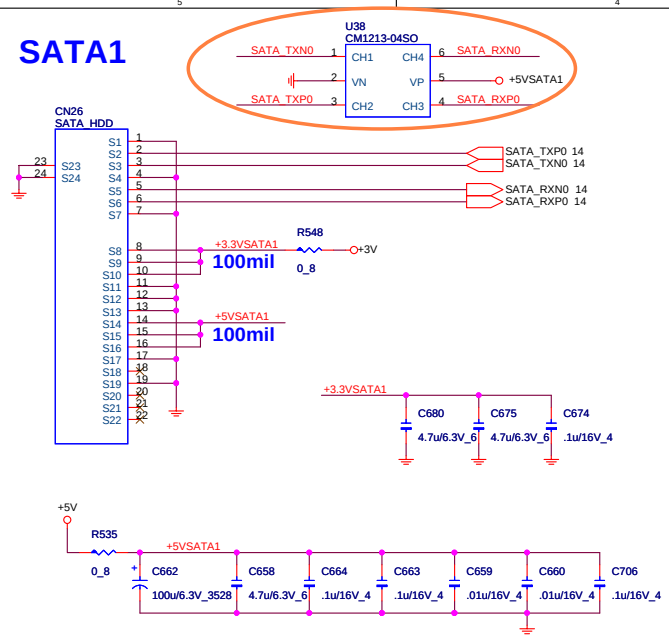
Q30 *DTC144EUA

Q27 2N7002

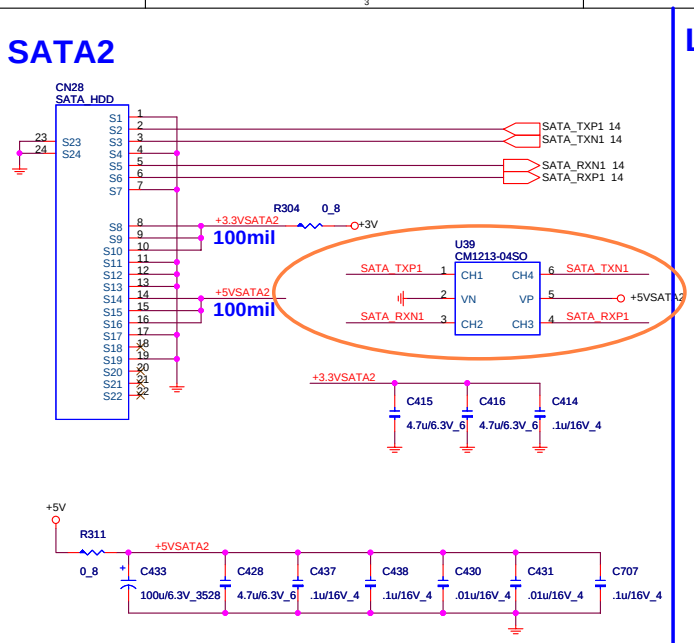
Q28 2N7002

Quanta Computer Inc.		
PROJECT : ZY7		
Size	Document Number	Rev
	NEW&MINI&TV CARD/USB/BT/CIR	1A
Date: Thursday, June 26, 2008	Sheet 19 of 35	

SATA1

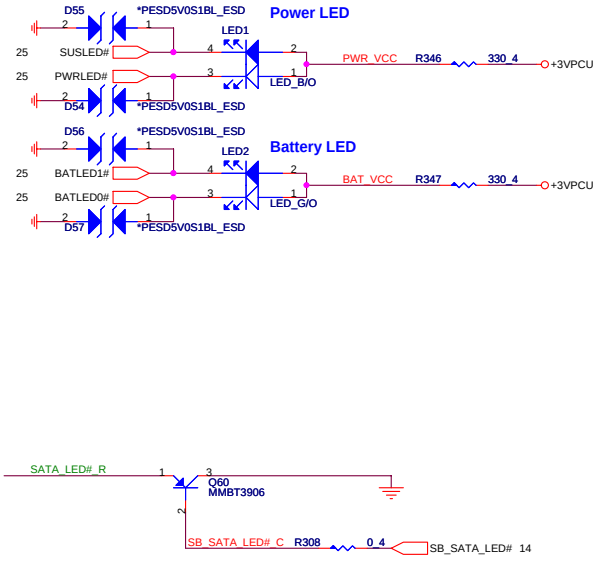


SATA2

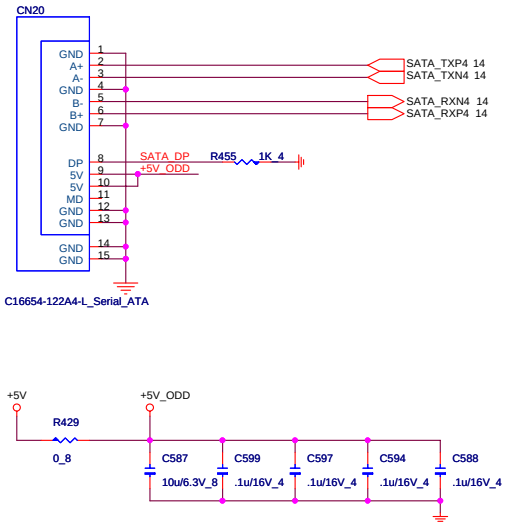


LED

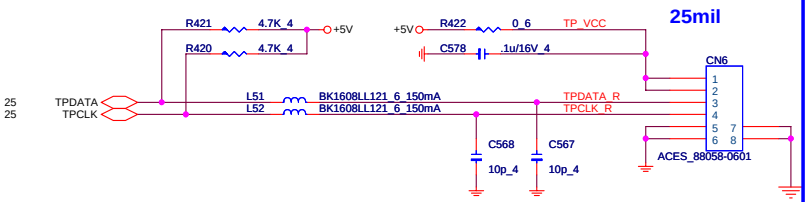
Power/Suspend: Blue/ Amber



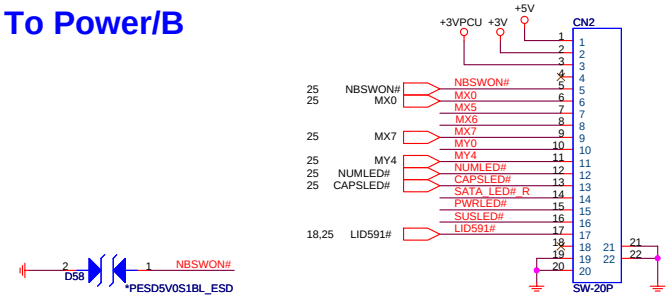
ODD (SATA)



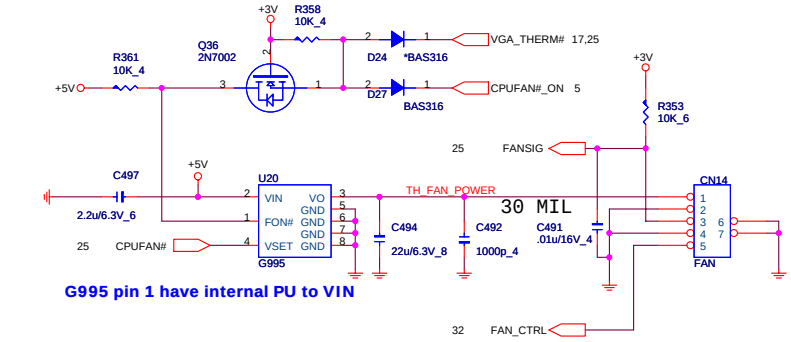
TP CONN



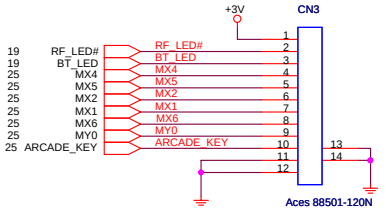
To Power/B



FAN



To Switch/B



Quanta Computer Inc.

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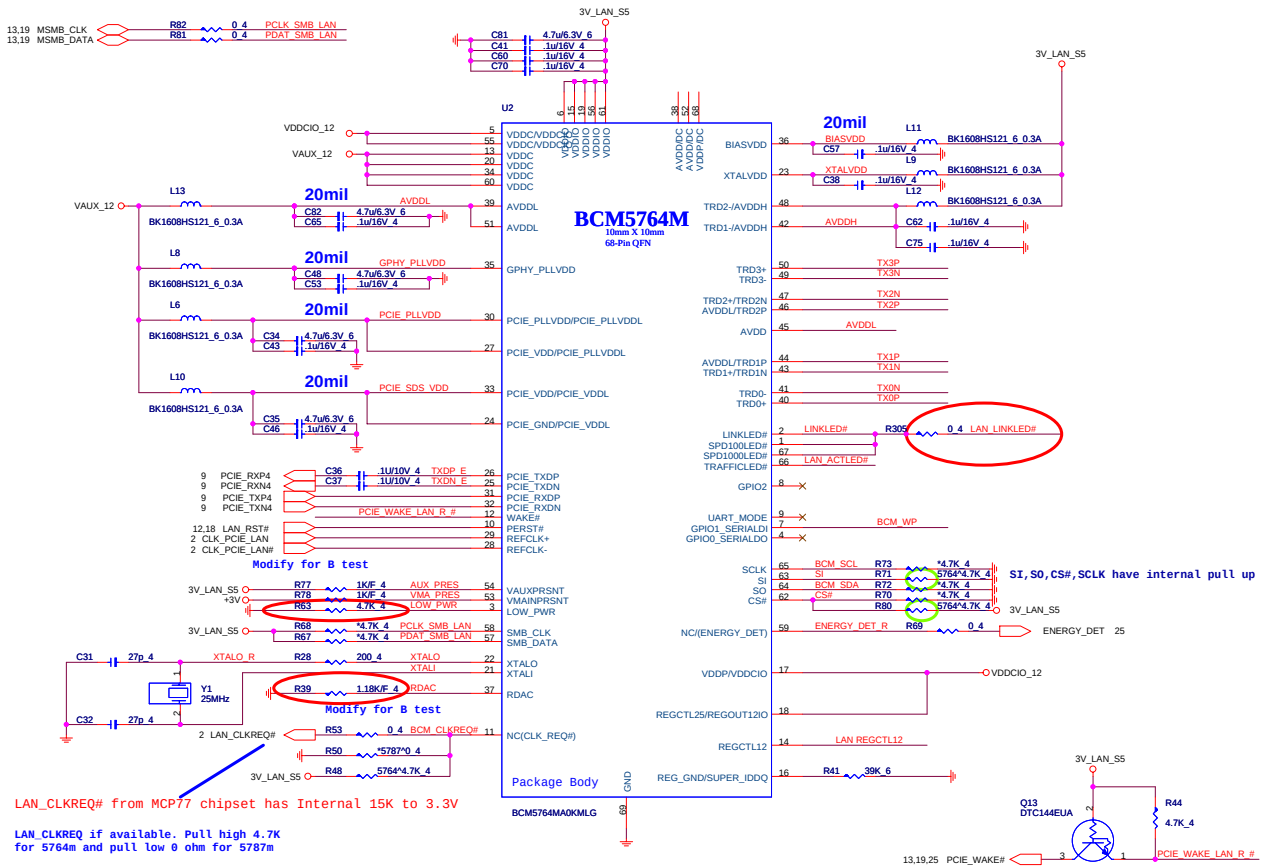
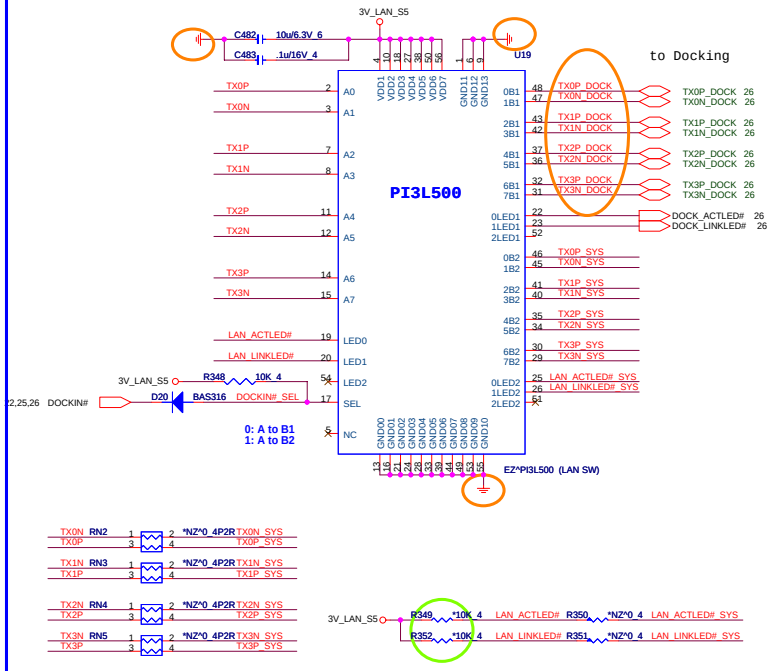
Giga LAN BCM5787M/5764M



LAN SWITCH

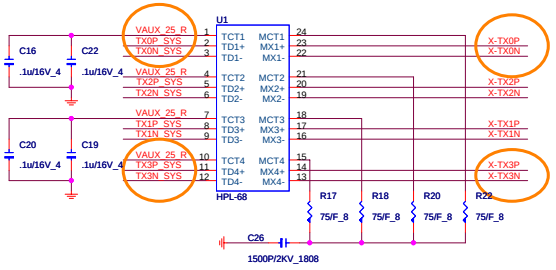


Transfomer

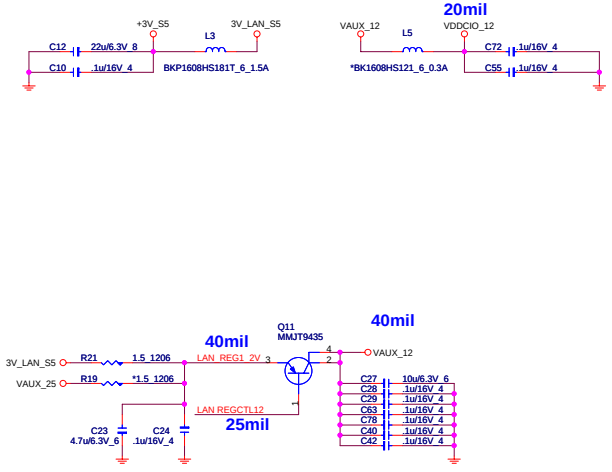
Source 1: DELTA LFE9249 DB0ZR1LAN11

Source 2: Bothand GST5009 DBKN1NLAN03

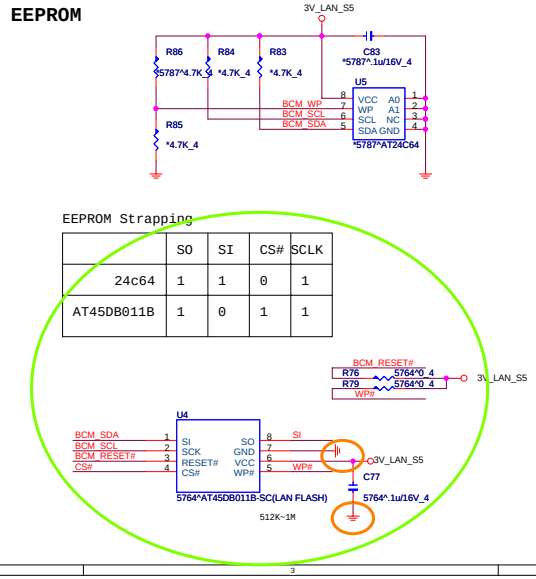
REV B: SWAP net for layout issue---0214



LAN POWER



EEPROM

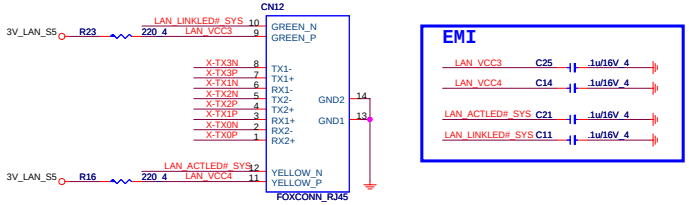


EEPROM Strapping

	SO	SI	CS#	SCLK
24c64	1	1	0	1
AT45DB011B	1	0	1	1

RJ45 connector

Modify for C test



Quanta Computer Inc. PROJECT : ZY7			
Size	Document Number: GigaLAN BCM5787M/5764M & RJ45		Rev 1A
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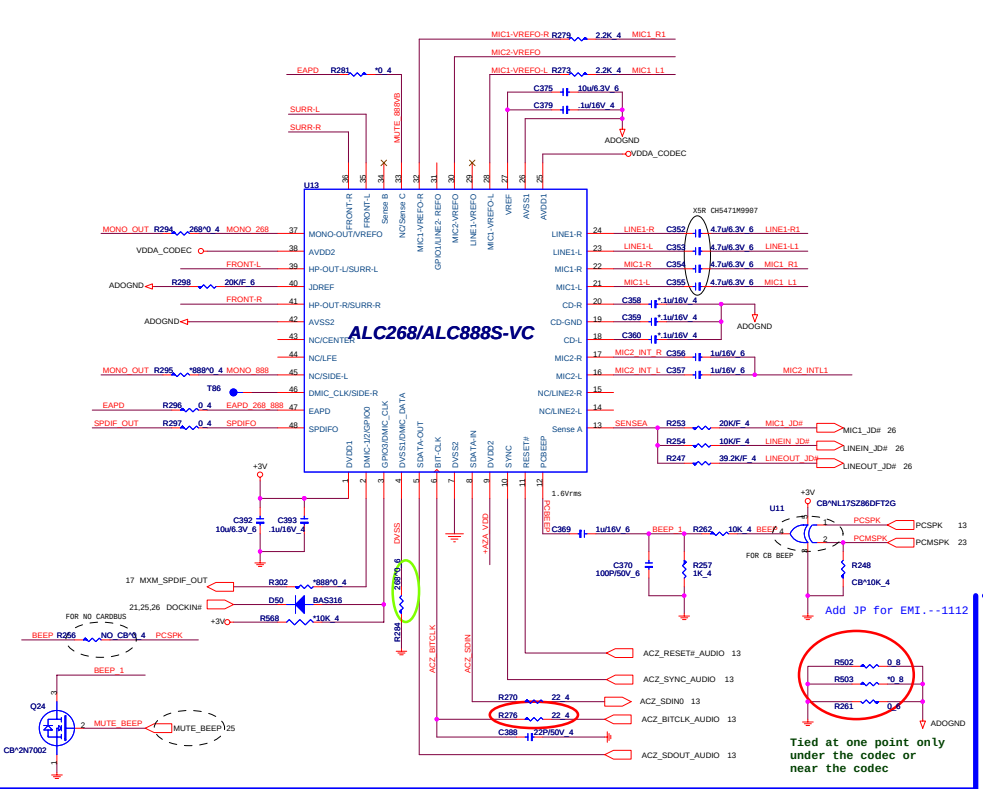
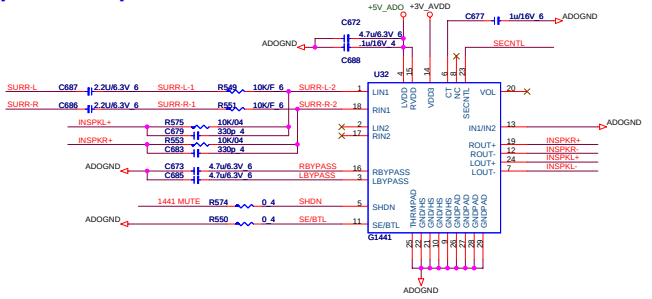
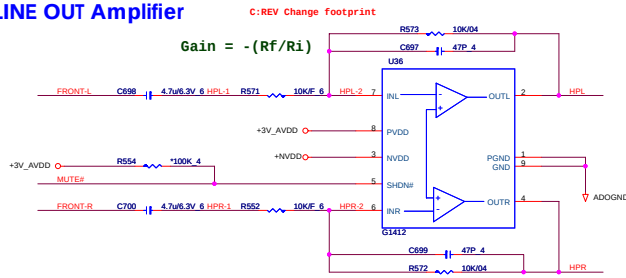
CODEC



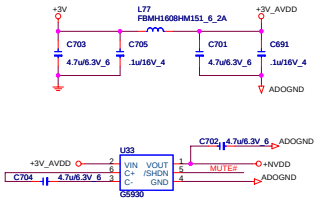
Speaker Amplifier



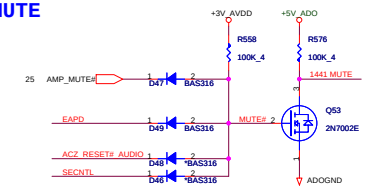
LINE OUT Amplifier



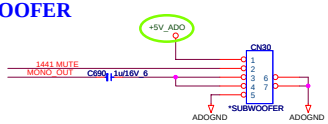
Amplifier POWER



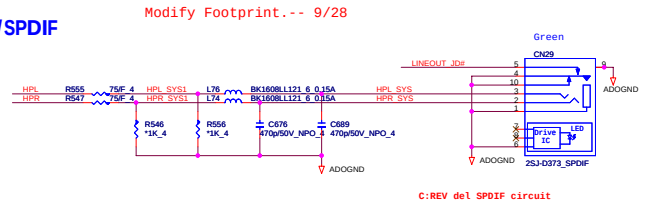
MUTE



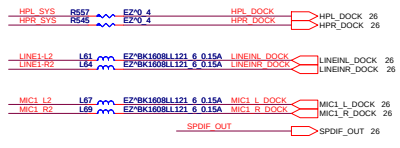
SUBWOOFER



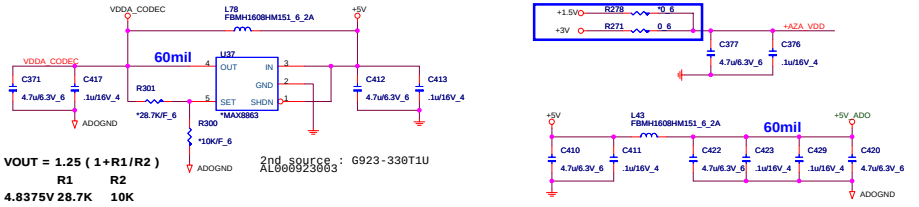
LINE OUT/SPDIF



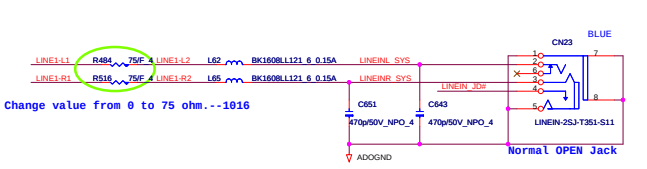
TO DOCKING



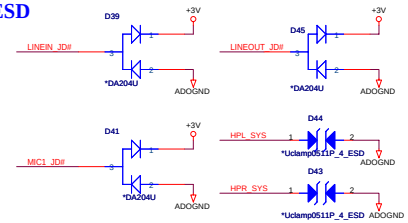
Codec/AMP Power



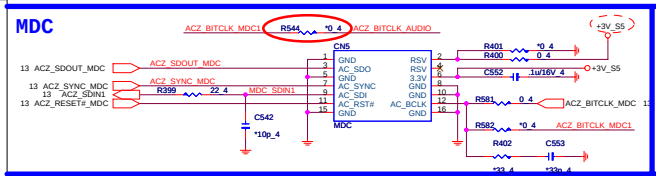
LINE IN



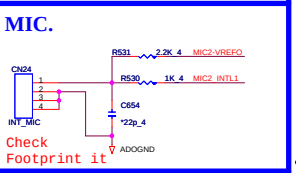
ESD



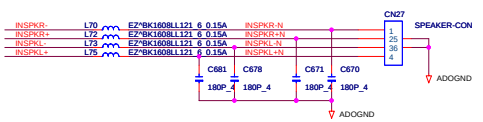
MDC



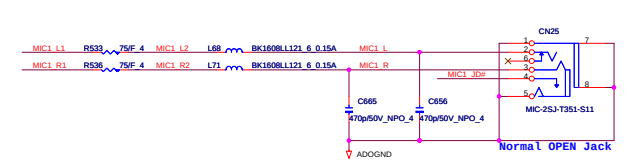
INT MIC.

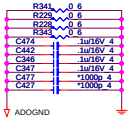


SPEAKER



MIC





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NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

Modify it from 150 to 100ohm.--0928

AD20 R328 100/F_4 PCM_IDSEL

ID Select : AD20
Interrupt Pin : INTA#
Request Indicate : REQ0#
Grant Indicate : GNT0#

For EMI

PCLK_PCM — R329 *22_4 — C463 *22p_4

IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)

+3V — C424 4.7u/6.3V_6, C451 .1u/16V_4, C458 .1u/16V_4, C439 .1u/16V_4

R321 33K/F_6 — VPPD0
R322 33K/F_6

U16
OZ601T

CORE_VCC ×4, PCI_VCC ×3

12,16 AD[31..0] — AD31 … AD0

PCM_IDSEL

12 CBE3# CBE2# CBE1# CBE0#

12 PCLK_PCM

12 DEVSEL# FRAME# IRDY# TRDY# STOP# PAR

12 PERR#

12 REQ0# GNT0#

12,19 PCIRST# — R334 0_4 — PCIRST#_R
13 PCI_PME# — R330 0_4 — PCM_PME#

12,25 CLKRUN#
22 PCMSPK
12,19,25 SERIRQ
12 INTA#

VCC5#/VCCD0#/SDATA
VCC3#/VCCD1#/SCLK
VPP_PGM/VPPD0/SLATCH

VCCD0
VCCD1

CAD31 … CAD0

R_A_CCLK
A_CFRAME#
A_CIRDY#
A_CTRDY#
A_CDEVSEL#
A_CSTOP#
A_CPAR
A_CPERR#
A_CSERR#
A_CREQ#
A_CGNT#
A_CINT#
A_CBLOCK#
A_CCLKRUN#
A_CRST# — R312 47K — SKT_VCC
A_CRSVD/D2
A_CRSVD/D14
A_CRSVD/A18
A_CVS1#
A_CVS2#
A_CCD1#
A_CCD2#
A_CAUDIO
A_CSTSCHG
A_CC/BE3#
A_CC/BE2#
A_CC/BE1#
A_CC/BE0#

CCLK
CFRAME#
CIRDY#
CTRDY#
CDEVSEL#
CSTOP#
CPAR
CPERR#
CSERR#
CREQ#
CGNT#
CINT#
CBLOCK#
CCLKRUN#
CRST#
R2_D2
R2_D14
R2_A18
CVS1
CVS2
CCD1#
CCD2#
CAUDIO
CSTSCHG
CC/BE3#
CC/BE2#
CC/BE1#
CC/BE0#

MF6 (CLKRUN#)
MF4 (RI_OUT#)
MF3 (SERIRQ#)
MF0 (INTA#)

PERR#/SPKR_OUT
REQ#
GNT#
RST#
PME#/RI_OUT#
PCI_CLK

GND ×6 — 32 45 65 96 128

SKT_VCC — C472 4.7u/6.3V_6, C471 .1u/16V_4 — C475 4.7u/6.3V_6, C473 .1u/16V_4 — C465 4.7u/6.3V_6, C467 .1u/16V_4

U18
VCC1 +3.3 — 1
VCC2 +3.3 — 2
VCC5# +5V — 3
VCC3# GND — 4
6 5 7 8
VCCD0
VCCD1
OZ2210G

Check Footprint

22K TO 47K PULL-UPS MUST BE PLACED
ON INTA#, PME#, SERIRQ# & CLKRUN#.

R_A_CCLK R306 33_4 A_CCLK

PCMCIA SOCKET

Check it

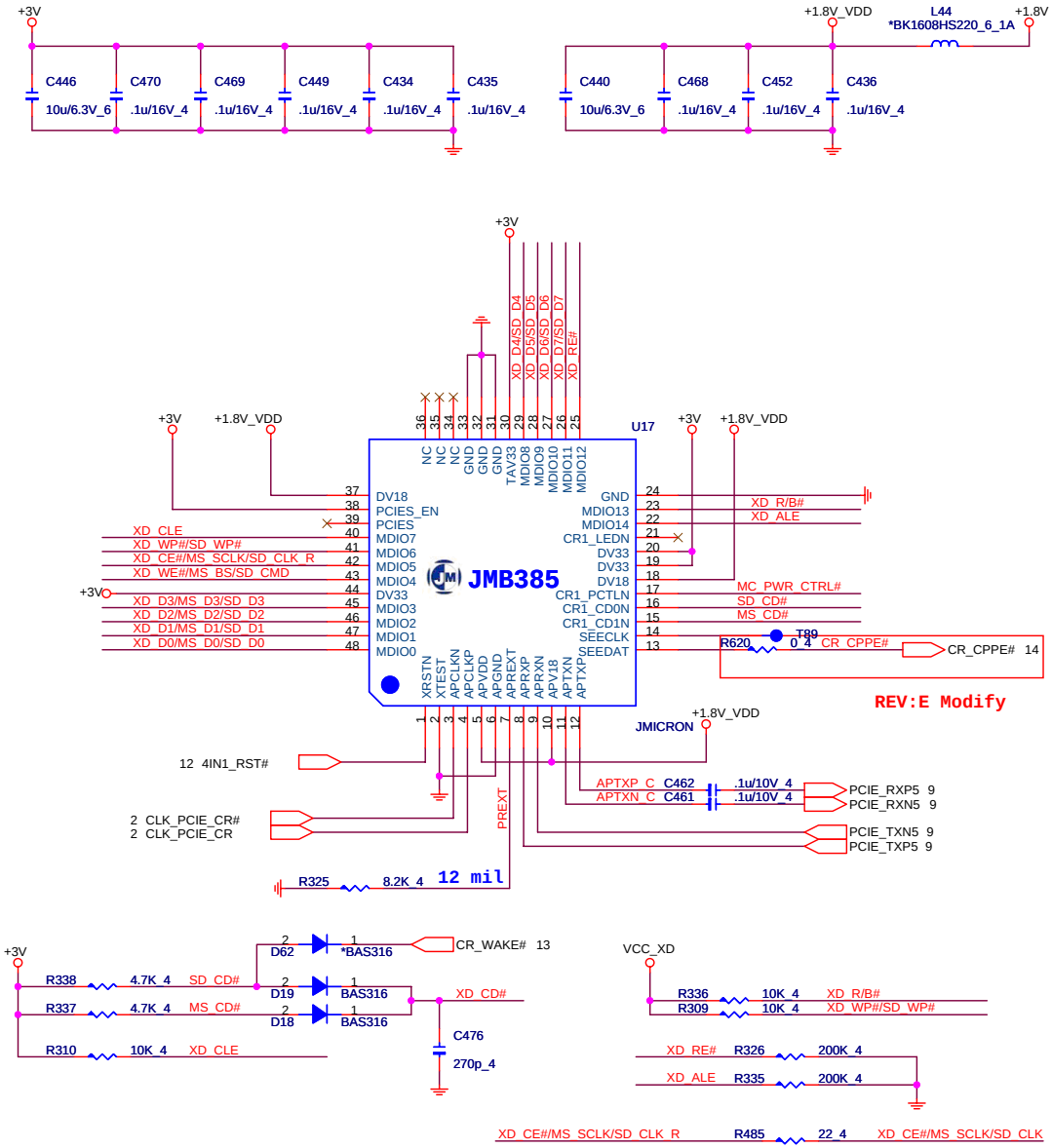
CN10

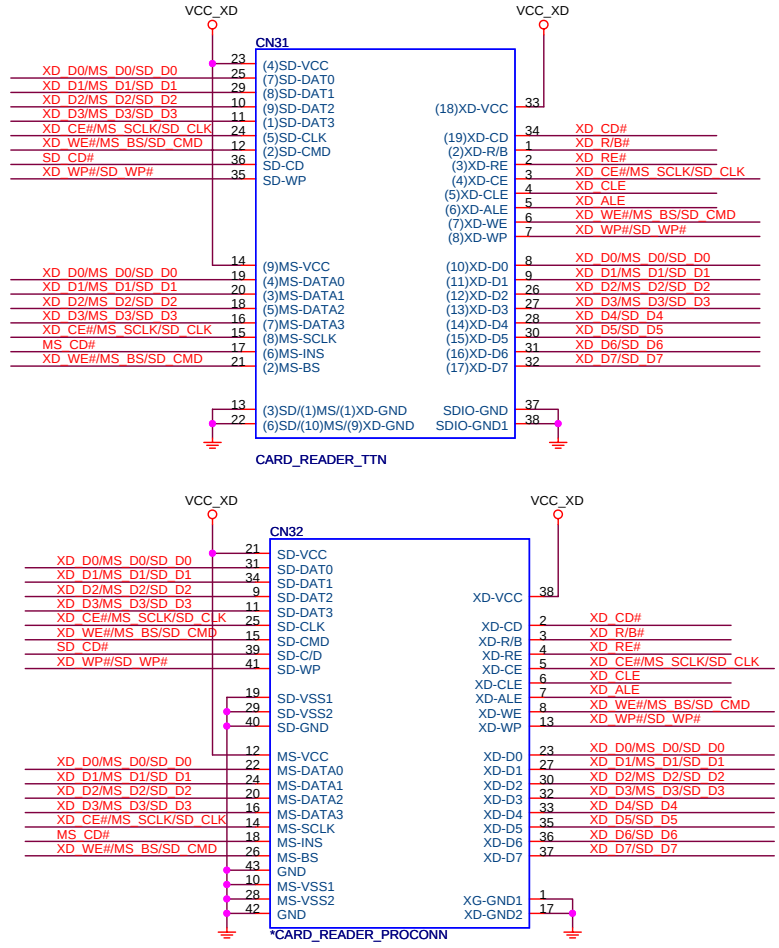
A_CAD0	2	GND1	SKTAVCC1	17	SKT_VCC
A_CAD1	3	SKTAAD0/D3	SKTAVCC2	51	
A_CAD3	4	SKTAAD1/D4			
A_CAD5	5	SKTAD3/D5	SKTAVPP1	18	
A_CAD7	6	SKTAD5/D6	SKTAVPP2	52	
A_CC/BE0#	7	SKTAAD7/D7			
A_CAD9	8	-SKTACBE0/CE1#			
A_CAD11	9	SKTAAD9/A10			
A_CAD12	10	SKTABAD11/OE#	GND5	69	
A_CAD14	11	SKTAAD12/A11	GND6	70	
A_CC/BE1#	12	SKTAAD14/A9	GND7	71	
A_CPAR	13	-SKTACBE1/A8	GND8	72	
A_CPERR#	14	SKTAPAR/A13	GND9	73	
A_CGNT#	15	-SKTAPERR/A14	GND10	74	
A_CINT#	16	-SKTAGNT/WE#	GND11	75	
		-SKTAINT/RDY	GND12	76	
		UPPER PIN	GND13	77	
A_CCLK	19	SKTAPCLK/A16	GND14	78	
A_CIRDY#	20	-SKTAIRDY/A15	GND15	79	
A_CC/BE2#	21	-SKTACBE2/A12	GND16	80	
A_CAD18	22	SKTAAD18/A7	GND17	81	
A_CAD20	23	SKTAAD20/A6	GND18	82	
A_CAD21	24	SKTAAD21/A5	GND19	83	
A_CAD22	25	SKTAAD22/A4	GND20	84	
A_CAD23	26	SKTAAD23/A3			
A_CAD24	27	SKTAAD24/A2			
A_CAD25	28	SKTAAD25/A1			
A_CAD26	29	SKTAAD26/A0	NC	85	
A_CAD27	30	SKTAAD27/D0	NC	86	
A_CAD29	31	SKTAAD29/D1	NC	87	
A_CRSVD/D2	32	SKTARSVD/D2	NC	88	
A_CCLKRUN#	33	-SKTACLKRUN/WP			
	34	GND2			
	35	GND3			
A_CCD1#	36	-SKTACD1/CD1#			
A_CAD2	37	SKTAAD2/D11			
A_CAD4	38	SKTAD4/D12			
A_CAD6	39	SKTAAD6/D13			
A_CRSVD/D14	40	SKTARSVD/D14			
A_CAD8	41	SKTAAD8/D15			
A_CAD10	42	SKTAAD10/CE2#			
A_CVS1#	43	-SKTAVS1/VS1#			
A_CAD13	44	SKTAAD13/IORD#			
A_CAD15	45	SKTAAD15/IOWR#			
A_CRSVD/A18	46	SKTAAD16/A17			
A_CBLOCK#	47	-SKTRSVD/A18			
A_CSTOP#	48	-SKTALOCK/A19			
A_CDEVSEL#	49	-SKTASTOP/A20			
	50	-SKTADEVSEL/A21			
		LOWER PIN			
A_CTRDY#	53	-SKTATRDY/A22			
A_CFRAME#	54	-SKTAFRAME/A23			
A_CAD17	55	SKTAAD17/A24			
A_CAD19	56	SKTAAD19/A25			
A_CVS2#	57	-SKTAVS2/VS2#			
A_CRST#	58	-SKTARST/RESET			
A_CSERR#	59	0SKTASERR/WAIT#			
A_CREQ#	60	-SKTAREQ/INPACK#			
A_CC/BE3#	61	-SKTACBE3/REG#			
A_CAUDIO	62	SKTAAUDIO/BVD2			
A_CSTSCHG	63	-SKTASTSCHG/BVD1			
A_CAD28	64	SKTAAD28/D8			
A_CAD30	65	SKTAAD30/D9			
A_CAD31	66	SKTAAD31/D10			
A_CCD2#	67	-SKTACD2/CD2#			
	68	GND4			

PCMCIA_SOCKET

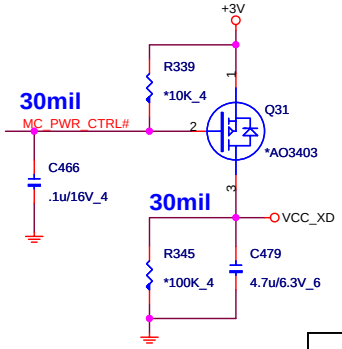
Del SKT_VCC.-0927

4 IN 1 CARD READER

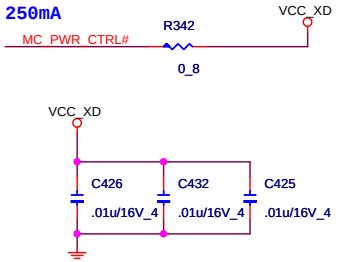




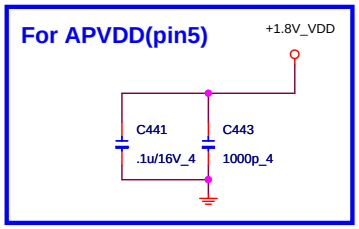
Memory Card Power Supply



Use 0805 type and over 20 mils trace width on both side



APVDD(pin5) must put C601/1000pF close to APVDD(pin5) (length must under 120mil) and trace width = 20mil, after C601, pls put one more 0.1uF for it.



Quanta Computer Inc.

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Size	Document Number	Rev
	CARD READER JMB385	1A
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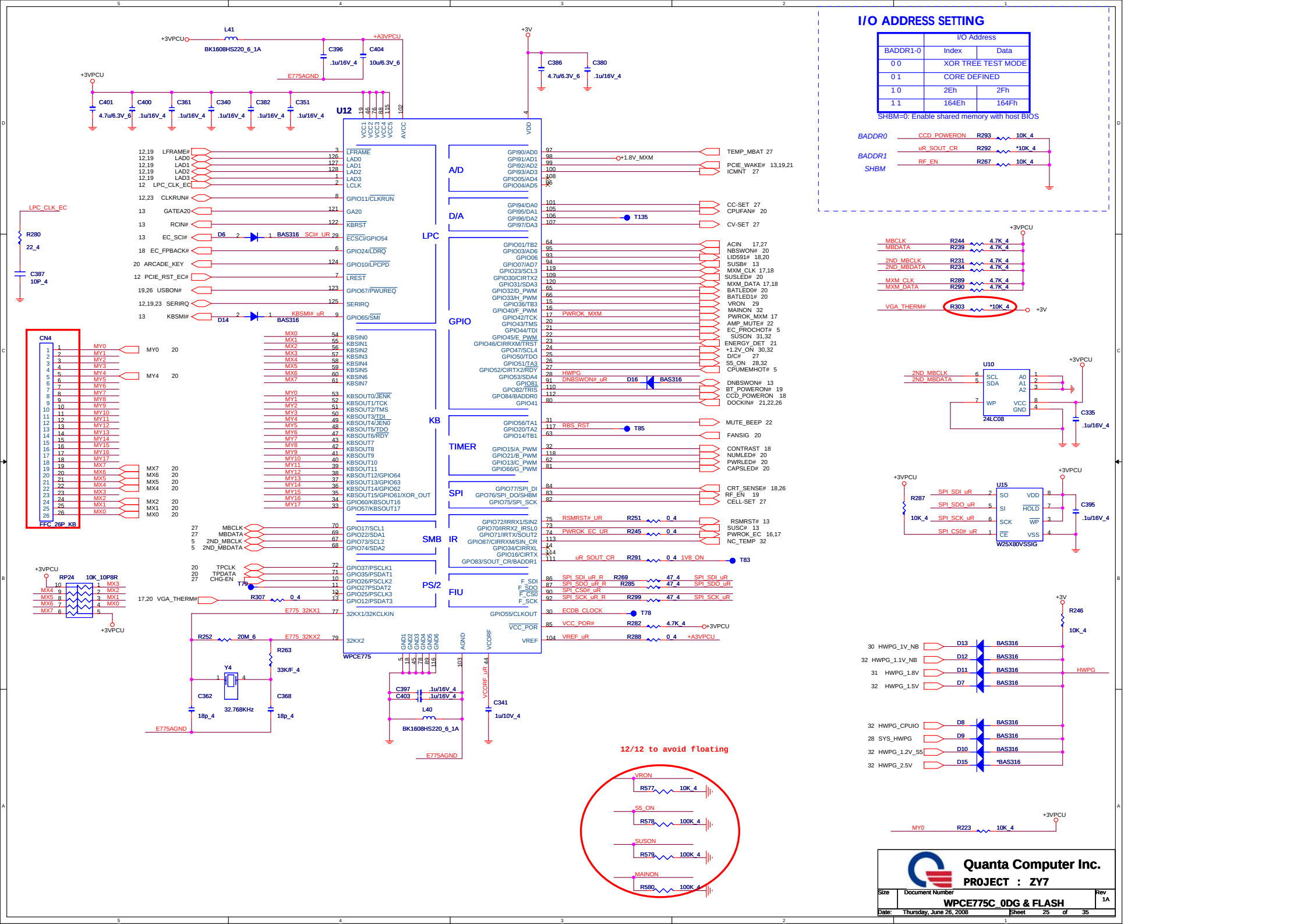
I/O ADDRESS SETTING
I/O Address
BADDR1-0
Index
Data
0 0
XOR TREE TEST MODE
0 1
CORE DEFINED
1 0
2Eh
2Fh
1 1
164Eh
164Fh
SHBM=0: Enable shared memory with host BIOS
BADDR0
BADDR1
SHBM
CCD_POWERON R293 10K_4
uR_SOUT_CR R292 *10K_4
RF_EN R267 10K_4
U12
WPCE775
LPC
A/D
D/A
GPIO
KB
TIMER
SPI
SMB
IR
PS/2
FIU
LFRAME#
LAD0
LAD1
LAD2
LAD3
LCLK
CLKRUN#
GATEA20
KBRST
RCIN#
EC_SCI#
ECSCI/GPIO54
EC_FPBACK#
GPIO24/LDRQ
ARCADE_KEY
GPIO10/LPCPD
PCIE_RST_EC#
LREST
USBON#
GPIO67/PWUREQ
SERIRQ
KBSMI#
GPIO65/SMI
KBSIN0
KBSIN1
KBSIN2
KBSIN3
KBSIN4
KBSIN5
KBSIN6
KBSIN7
KBSOUT0/JENK
KBSOUT1/TCK
KBSOUT2/TMS
KBSOUT3/TDI
KBSOUT4/JEN0
KBSOUT5/TDO
KBSOUT6/RDY
KBSOUT7
KBSOUT8
KBSOUT9
KBSOUT10
KBSOUT11
KBSOUT12/GPIO64
KBSOUT13/GPIO63
KBSOUT14/GPIO62
KBSOUT15/GPIO61/XOR_OUT
GPIO60/KBSOUT16
GPIO57/KBSOUT17
GPIO17/SCL1
GPIO22/SDA1
GPIO73/SCL2
GPIO74/SDA2
GPIO37/PSCLK1
GPIO35/PSDAT1
GPIO26/PSCLK2
GPIO27/PSDAT2
GPIO25/PSCLK3
GPIO12/PSDAT3
32KX1/32KCLKIN
32KX2
GPI90/AD0
GPI91/AD1
GPI92/AD2
GPI93/AD3
GPIO05/AD4
GPIO04/AD5
GPI94/DA0
GPI95/DA1
GPI96/DA2
GPI97/DA3
GPIO01/TB2
GPIO03/AD6
GPIO06
GPIO07/AD7
GPIO23/SCL3
GPIO30/CIRTX2
GPIO31/SDA3
GPIO32/D_PWM
GPIO33/H_PWM
GPIO36/TB3
GPIO40/F_PWM
GPIO42/TCK
GPIO43/TMS
GPIO44/TDI
GPIO45/E_PWM
GPIO46/CIRRXM/TRST
GPO47/SCL4
GPIO50/TDO
GPIO51/TA3
GPIO52/CIRTX2/RDY
GPIO53/SDA4
GPIO81
GPO82/TRIS
GPO84/BADDR0
GPIO41
GPIO56/TA1
GPIO20/TA2
GPIO14/TB1
GPIO15/A_PWM
GPIO21/B_PWM
GPIO13/C_PWM
GPIO66/G_PWM
GPIO77/SPI_DI
GPO76/SPI_DO/SHBM
GPIO75/SPI_SCK
GPIO72/IRRX1/SIN2
GPIO70/IRRX2_IRSL0
GPIO71/IRTX/SOUT2
GPIO87/CIRRXM/SIN_CR
GPIO34/CIRRXL
GPIO16/CIRTX
GPO83/SOUT_CR/BADDR1
F_SDI
F_SDO
F_CS0
F_SCK
GPIO55/CLKOUT
VCC_POR
VREF
TEMP_MBAT 27
+1.8V_MXM
PCIE_WAKE# 13,19,21
ICMNT 27
CC-SET 27
CPUFAN# 20
T135
CV-SET 27
ACIN 17,27
NBSWON# 20
LID591# 18,20
SUSB# 13
MXM_CLK 17,18
SUSLED# 20
MXM_DATA 17,18
BATLED0# 20
BATLED1# 20
VRON 29
MAINON 32
PWROK_MXM 17
AMP_MUTE# 22
EC_PROCHOT# 5
SUSON 31,32
ENERGY_DET 21
+1.2V_ON 30,32
D/C# 27
S5_ON 28,32
CPUMEMHOT# 5
DNBSWON# 13
BT_POWERON# 19
CCD_POWERON 18
DOCKIN# 21,22,26
MUTE_BEEP 22
T85
FANSIG 20
CONTRAST 18
NUMLED# 20
PWRLED# 20
CAPSLED# 20
CRT_SENSE# 18,26
RF_EN 19
CELL-SET 27
RSMRST# 13
SUSC# 13
PWROK_EC 16,17
NC_TEMP 32
T83
T78
+3VPCU
+A3VPCU
+3V
L41
BK1608HS220_6_1A
C396 .1u/16V_4
C404 10u/6.3V_6
C386 4.7u/6.3V_6
C380 .1u/16V_4
C401 4.7u/6.3V_6
C400 .1u/16V_4
C361 .1u/16V_4
C340 .1u/16V_4
C382 .1u/16V_4
C351 .1u/16V_4
E775AGND
LPC_CLK_EC
R280 22_4
C387 10P_4
D6 BAS316 SCI# UR
D14 BAS316 KBSMI# uR
CN4
FFC_26P_KB
RP24 10K_10P8R
R307 0_4
VGA_THERM#
R252 20M_6
R263 33K/F_4
Y4 32.768KHz
C362 18p_4
C368 18p_4
E775_32KX1
E775_32KX2
C397 .1u/16V_4
C403 .1u/16V_4
L40 BK1608HS220_6_1A
C341 1u/10V_4
VCORF uR 44
R269 47_4 SPI_SDI uR
R285 47_4 SPI_SDO uR
SPI_CS0# uR
R299 47_4 SPI_SCK uR
R251 0_4
R245 0_4
R291 0_4 1V8_ON
R282 4.7K_4
R288 0_4 +A3VPCU
ECDB_CLOCK
VCC_POR#
VREF uR
MBCLK R244 4.7K_4
MBDATA R239 4.7K_4
2ND_MBCLK R231 4.7K_4
2ND_MBDATA R234 4.7K_4
MXM_CLK R289 4.7K_4
MXM_DATA R290 4.7K_4
VGA_THERM# R303 *10K_4
U10
24LC08
C335 .1u/16V_4
U15
W25X80VSSIG
C395 .1u/16V_4
R287 10K_4
R246 10K_4
HWPG
HWPG_1V_NB D13 BAS316
HWPG_1.1V_NB D12 BAS316
HWPG_1.8V D11 BAS316
HWPG_1.5V D7 BAS316
HWPG_CPUIO D8 BAS316
SYS_HWPG D9 BAS316
HWPG_1.2V_S5 D10 BAS316
HWPG_2.5V D15 *BAS316
MY0 R223 10K_4
12/12 to avoid floating
VRON R577 10K_4
S5_ON R578 100K_4
SUSON R579 100K_4
MAINON R580 100K_4
Quanta Computer Inc.
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WPCE775C_0DG & FLASH
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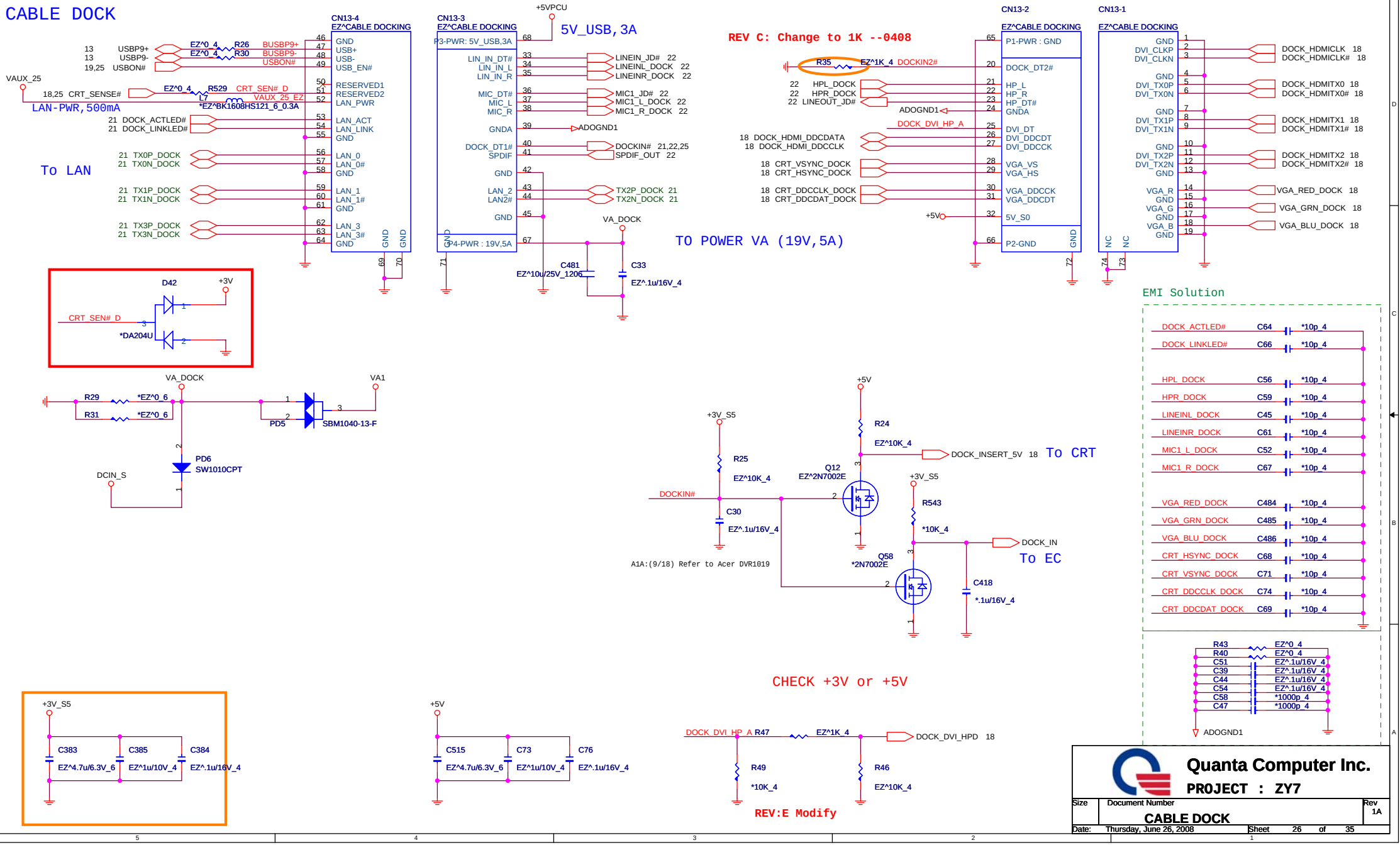
CABLE DOCK


CN13-4
EZ^CABLE DOCKING
CN13-3
EZ^CABLE DOCKING
CN13-2
EZ^CABLE DOCKING
CN13-1
EZ^CABLE DOCKING
5V_USB, 3A
REV C: Change to 1K --0408
To LAN
LAN-PWR, 500mA
TO POWER VA (19V, 5A)
EMI Solution
To CRT
To EC
CHECK +3V or +5V
REV:E Modify
Quanta Computer Inc.
PROJECT : ZY7
CABLE DOCK
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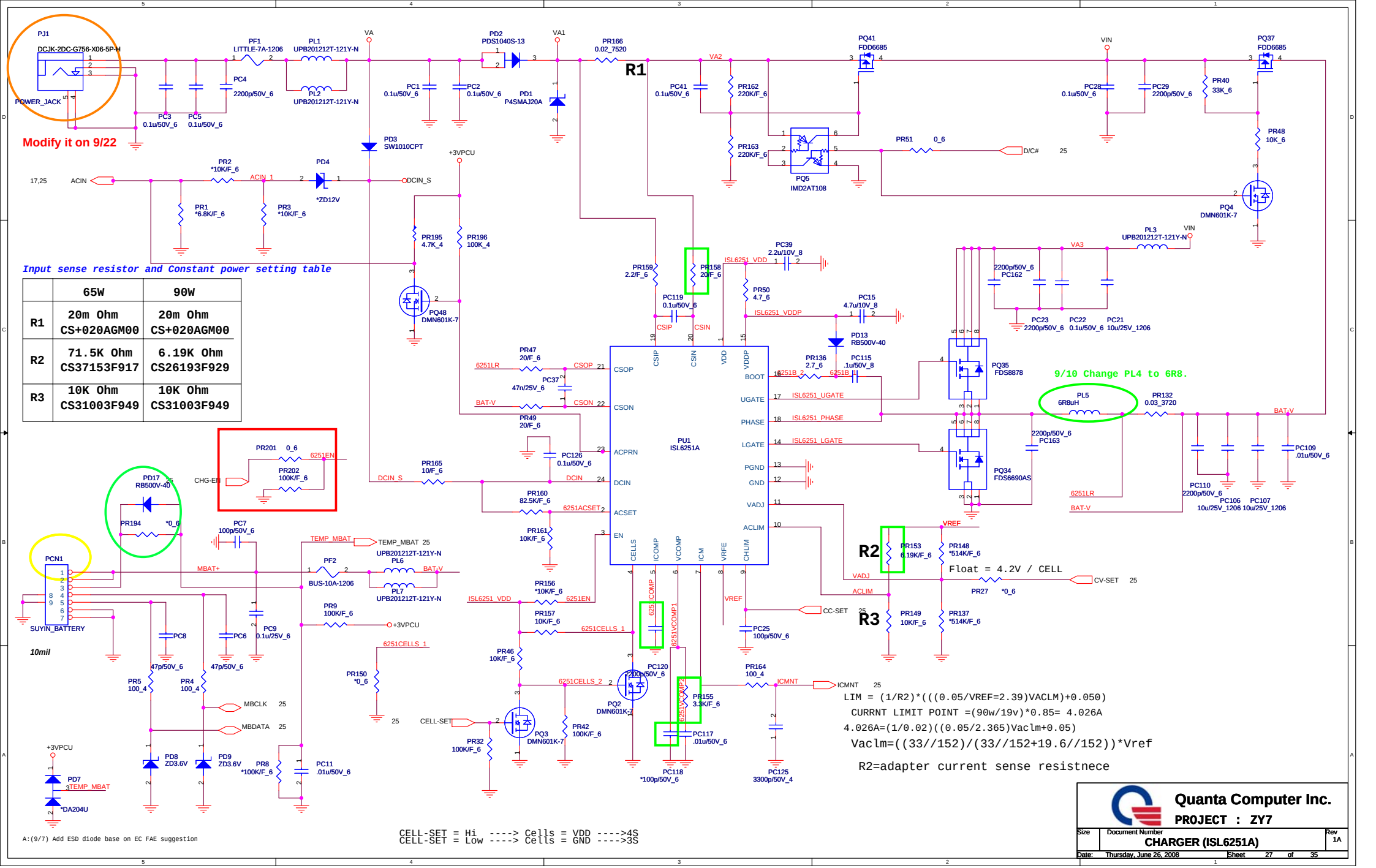
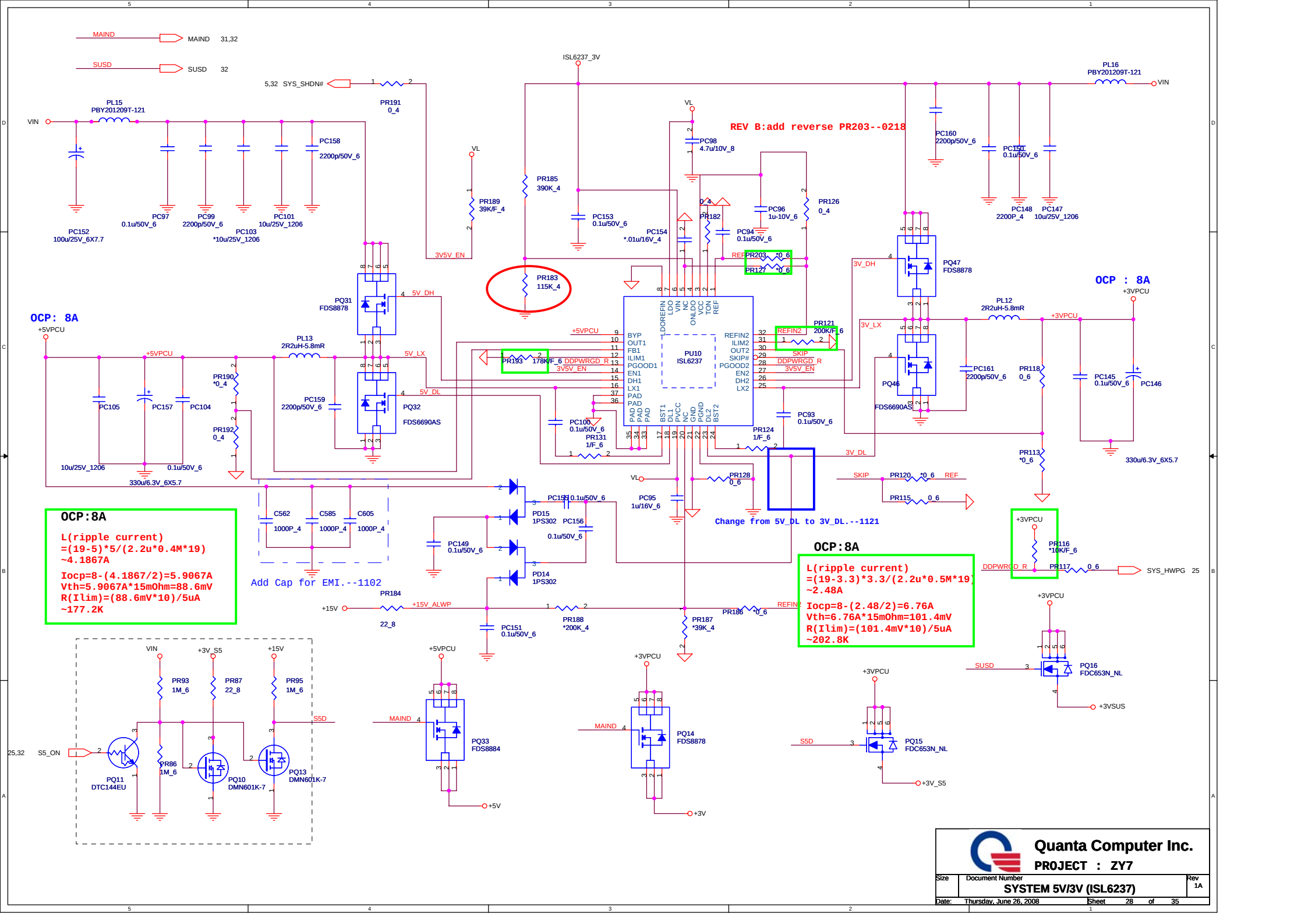


	65W	90W
R1	20m Ohm CS+020AGM00	20m Ohm CS+020AGM00
R2	71.5K Ohm CS37153F917	6.19K Ohm CS26193F929
R3	10K Ohm CS31003F949	10K Ohm CS31003F949


MAIND
MAIND 31,32
SUSD
SUSD 32
5,32 SYS_SHDN#
ISL6237_3V
PL16
PBY201209T-121
VIN
PL15
PBY201209T-121
PR191
0_4
PC158
2200p/50V_6
PC152
100u/25V_6X7.7
PC97
0.1u/50V_6
PC99
2200p/50V_6
PC103
*10u/25V_1206
PC101
10u/25V_1206
VL
PR189
39K/F_4
3V5V_EN
PR185
390K_4
PC153
0.1u/50V_6
PC154
*.01u/16V_4
PC98
4.7u/10V_8
PR182
0_4
PC96
1u-10V_6
PC94
0.1u/50V_6
PR126
0_4
REF
PR203 *0_6
PR127 *0_6
PR183
115K_4
REV B:add reverse PR203--0218
PC160
2200p/50V_6
PC150
0.1u/50V_6
PC148
2200P_4
PC147
10u/25V_1206
OCP : 8A
OCP: 8A
+5VPCU
PQ31
FDS8878
5V_DH
5V_LX
5V_DL
PQ32
FDS6690AS
PL13
2R2uH-5.8mR
PR190
*0_4
PR192
0_4
PC105
PC157
PC104
10u/25V_1206
0.1u/50V_6
330u/6.3V_6X5.7
PC159
2200p/50V_6
PU10
ISL6237
PR193
178K/F_6
DDPWRGD_R
3V5V_EN
PC100
0.1u/50V_6
PR131
1/F_6
PC93
0.1u/50V_6
PR124
1/F_6
3V_DL
PR121
200K/F_6
REFIN2
SKIP
PQ47
FDS8878
3V_DH
3V_LX
PQ46
FDS6690AS
PL12
2R2uH-5.8mR
PC161
2200p/50V_6
PR118
0_6
PC145
0.1u/50V_6
PC146
330u/6.3V_6X5.7
PR113
*0_6
PR120 *0_6 REF
PR115 0_6
PR128
0_6
PC95
1u/16V_6
PC155 0.1u/50V_6
PD15
1PS302
PC156
0.1u/50V_6
PC149
0.1u/50V_6
PD14
1PS302
C562
1000P_4
C585
1000P_4
C605
1000P_4
Add Cap for EMI.--1102
Change from 5V_DL to 3V_DL.--1121
OCP:8A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.1867A
Iocp=8-(4.1867/2)=5.9067A
Vth=5.9067A*15mOhm=88.6mV
R(Ilim)=(88.6mV*10)/5uA
~177.2K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.76A
Vth=6.76A*15mOhm=101.4mV
R(Ilim)=(101.4mV*10)/5uA
~202.8K
PR184
22_8
+15V
+15V_ALWP
PR188
*200K_4
PR187
*39K_4
PR186 *0_6
PC151
0.1u/50V_6
PR116
*10K/F_6
PR117 0_6
SYS_HWPG 25
DDPWRGD_R
PQ16
FDC653N_NL
+3VSUS
PR93
1M_6
PR87
22_8
PR95
1M_6
S5D
25,32 S5_ON
PR86
1M_6
PQ11
DTC144EU
PQ10
DMN601K-7
PQ13
DMN601K-7
PQ33
FDS8884
PQ14
FDS8878
PQ15
FDC653N_NL
+5V
+3V
+3V_S5
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OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	0	0	X
+3.3V	X	X	0
+5V	X	0	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

add it.--1023

Pin 49 is GND Pin

REV B:Add PC172,PC173 for ISL request --0226

Close to CPU socket

Parallel

Close to CPU socket

Quanta Computer Inc.
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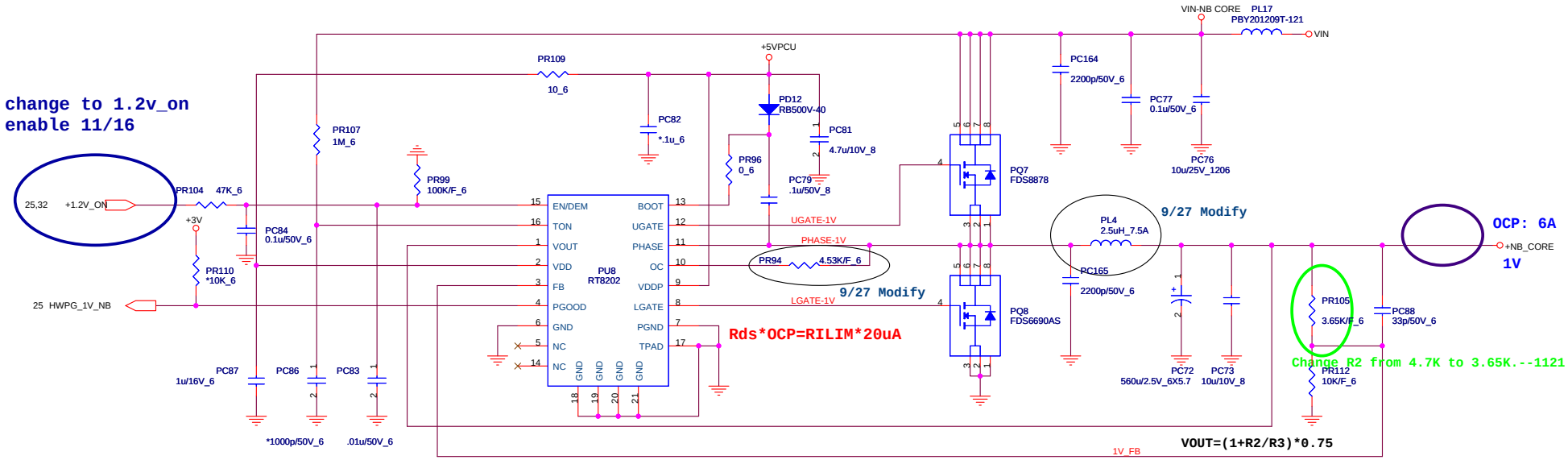
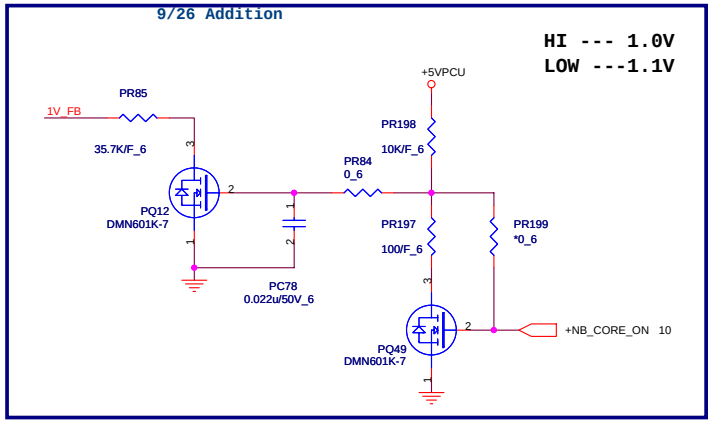


TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

6A OCP --- OC=4.53K
FDS6690AS Rds=15mOhm



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Size	Document Number	Rev
	NB_CORE(RT8202)	1A
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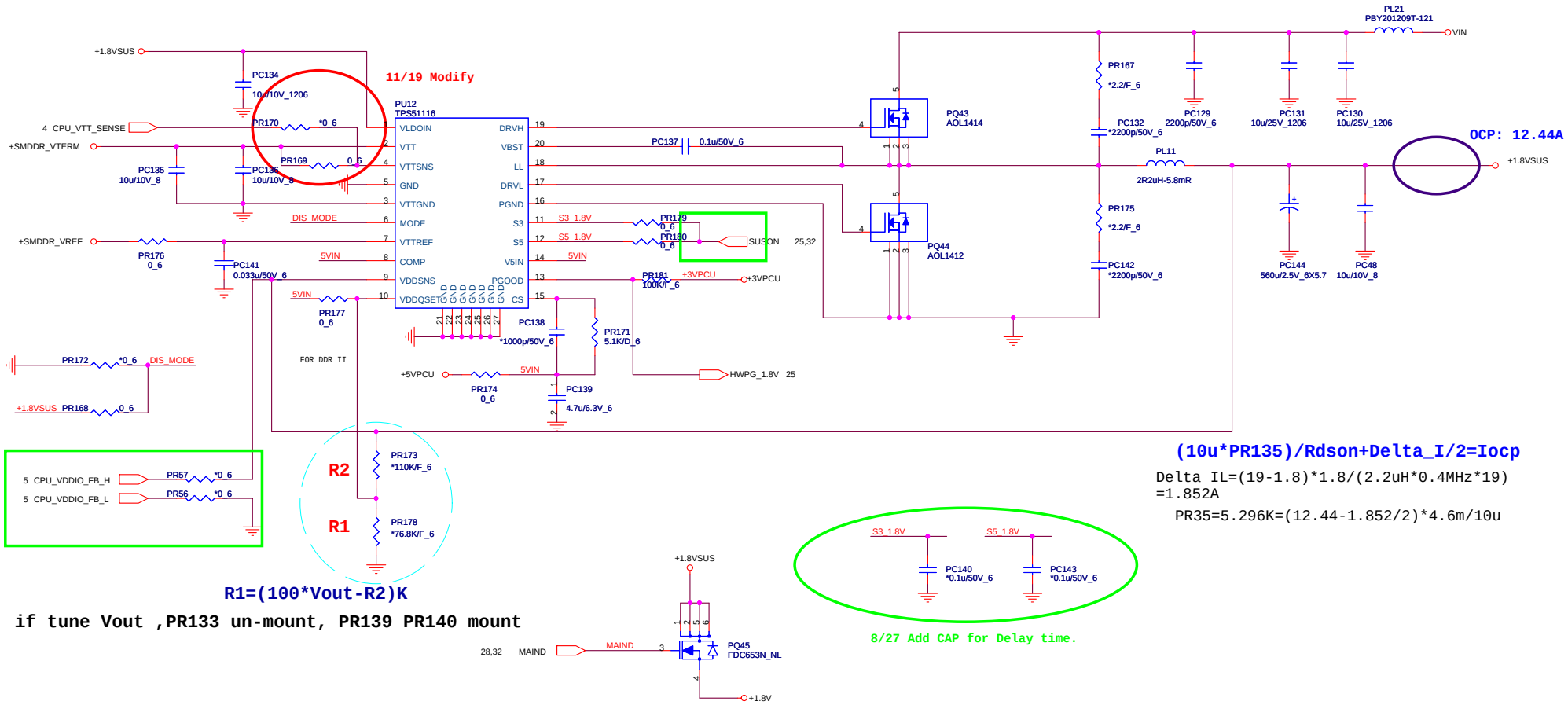


(10u*PR135)/Rdson+Delta_I/2=Iocp

Delta IL=(19-1.8)*1.8/(2.2uH*0.4MHz*19)
=1.852A

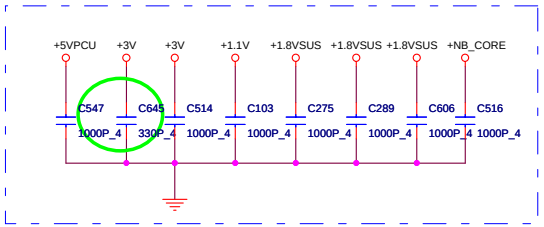
PR35=5.296K=(12.44-1.852/2)*4.6m/10u

R1=(100*Vout-R2)K

if tune Vout ,PR133 un-mount, PR139 PR140 mount

8/27 Add CAP for Delay time.

C REV: change to 330PF for EMI request



Add Cap for EMI.--1112

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Size	Document Number	Rev
	DDR 1.8V(TPS51116)	1A
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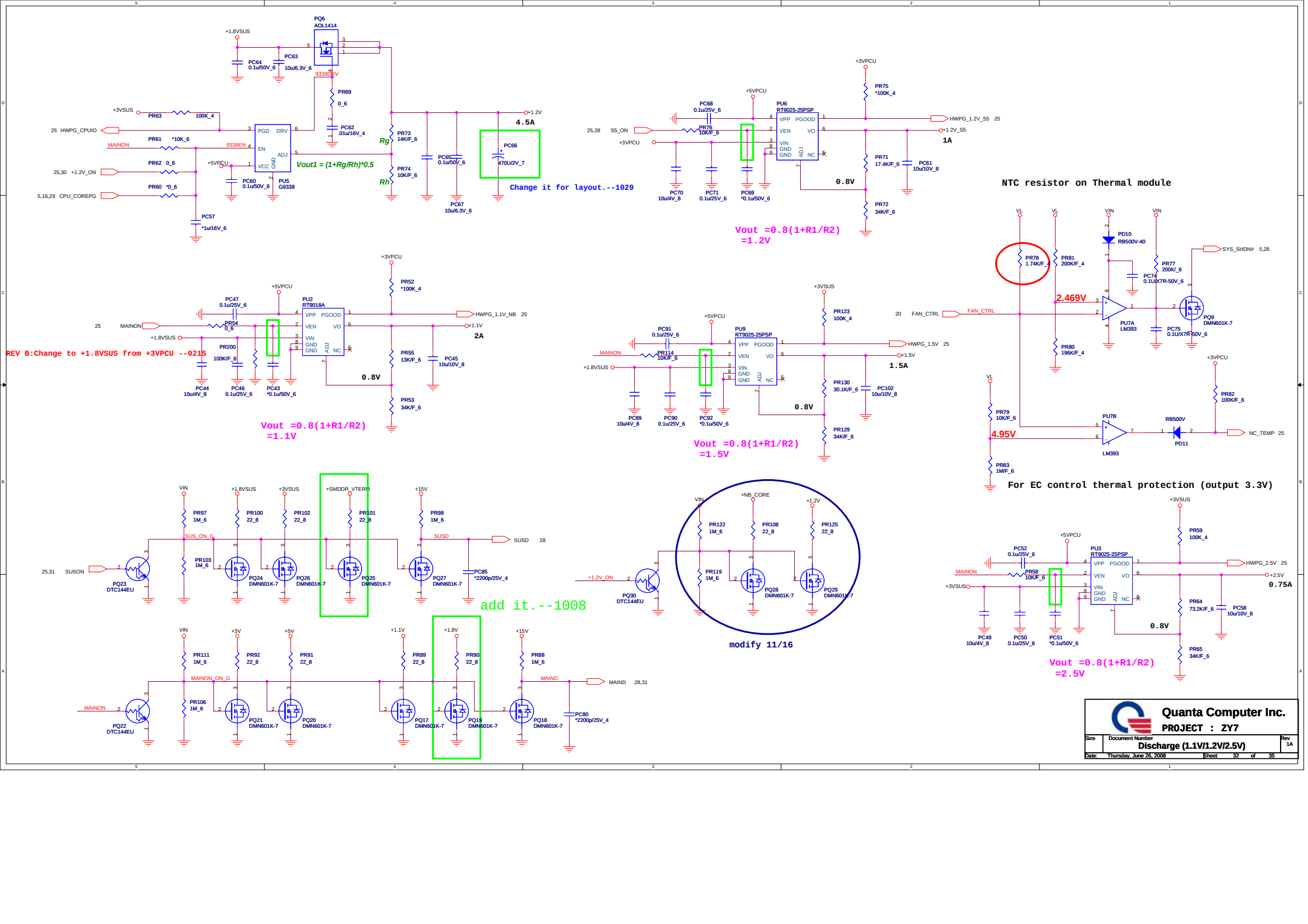
PQ6 AOL1414
+1.8VSUS
PC64 0.1u/50V_6
PC63 10u/6.3V_6
9338DEN
PR69 0_6
+3VSUS
PR63 100K_4
25 HWPG_CPUIO
MAINON
PR61 *10K_6
9338EN
PR62 0_6
25,30 +1.2V_ON
+5VPCU
PR60 *0_6
5,16,29 CPU_COREPG
PC57 *1u/16V_6
PC62 .01u/16V_4
PR73 14K/F_6
Rg
PR74 10K/F_6
Rh
PC65 0.1u/50V_6
PC67 10u/6.3V_6
PC66 470U/2V_7
+1.2V
4.5A
PU5 G9338
PGD DRV EN ADJ VCC GND
Vout1 = (1+Rg/Rh)*0.5
Change it for layout.--1029
+3VPCU
PR75 *100K_4
PC68 0.1u/25V_6
+5VPCU
PU6 RT9025-25PSP
VPP PGOOD VEN VO VIN GND GND ADJ NC
25,28 S5_ON
PR76 10K/F_6
+3VPCU
HWPG_1.2V_S5 25
+1.2V_S5
1A
PR71 17.4K/F_6
PC61 10u/10V_8
0.8V
PR72 34K/F_6
PC70 10u/4V_8
PC71 0.1u/25V_6
PC69 *0.1u/50V_6
Vout =0.8(1+R1/R2)
=1.2V
NTC resistor on Thermal module
+3VPCU
PR52 *100K_4
+5VPCU
PC47 0.1u/25V_6
PU2 RT9018A
VPP PGOOD VEN VO VIN GND GND ADJ NC
25 MAINON
PR54 0_6
+1.8VSUS
HWPG_1.1V_NB 25
+1.1V
2A
PR200 100K/F_6
PR55 13K/F_6
PC45 10u/10V_8
0.8V
PR53 34K/F_6
PC44 10u/4V_8
PC46 0.1u/25V_6
PC43 *0.1u/50V_6
REV B:Change to +1.8VSUS from +3VPCU --0215
Vout =0.8(1+R1/R2)
=1.1V
+3VSUS
PR123 100K_4
20 FAN_CTRL
PC91 0.1u/25V_6
+5VPCU
PU9 RT9025-25PSP
VPP PGOOD VEN VO VIN GND GND ADJ NC
MAINON
PR114 10K/F_6
+1.8VSUS
HWPG_1.5V 25
+1.5V
1.5A
PR130 30.1K/F_6
PC102 10u/10V_8
0.8V
PR129 34K/F_6
PC89 10u/4V_8
PC90 0.1u/25V_6
PC92 *0.1u/50V_6
Vout =0.8(1+R1/R2)
=1.5V
VL
VIN
PR78 1.74K/F_4
PR81 200K/F_4
PD10 RB500V-40
PR77 200K/_6
SYS_SHDN# 5,28
PC74 0.1U/X7R-50V_6
2.469V
PU7A LM393
PC75 0.1U/X7R-50V_6
PQ9 DMN601K-7
PR80 196K/F_4
+3VPCU
PR82 100K/F_6
PU7B
RB500V
NC_TEMP 25
4.95V
PD11
LM393
PR79 10K/F_6
PR83 1M/F_6
For EC control thermal protection (output 3.3V)
VIN
+1.8VSUS
+3VSUS
+SMDDR_VTERM
+15V
PR97 1M_6
PR100 22_8
PR102 22_8
PR101 22_8
PR98 1M_6
SUS_ON_G
SUSD
SUSD 28
25,31 SUSON
PR103 1M_6
PQ23 DTC144EU
PQ24 DMN601K-7
PQ26 DMN601K-7
PQ25 DMN601K-7
PQ27 DMN601K-7
PC85 *2200p/25V_4
add it.--1008
+1.2V_ON
PQ30 DTC144EU
+NB_CORE
+1.2V
PR122 1M_6
PR108 22_8
PR125 22_8
PR119 1M_6
PQ28 DMN601K-7
PQ29 DMN601K-7
modify 11/16
+3VSUS
PR59 100K_4
+5VPCU
PC52 0.1u/25V_6
PU3 RT9025-25PSP
VPP PGOOD VEN VO VIN GND GND ADJ NC
MAINON
PR58 10K/F_6
+3VSUS
HWPG_2.5V 25
+2.5V
0.75A
PR64 73.2K/F_6
PC58 10u/10V_8
0.8V
PR65 34K/F_6
PC49 10u/4V_8
PC50 0.1u/25V_6
PC51 *0.1u/50V_6
Vout =0.8(1+R1/R2)
=2.5V
VIN
+3V
+5V
+1.1V
+1.8V
+15V
PR111 1M_6
PR92 22_8
PR91 22_8
PR89 22_8
PR90 22_8
PR88 1M_6
MAINON_ON_G
MAIND
MAIND 28,31
MAINON
PR106 1M_6
PQ22 DTC144EU
PQ21 DMN601K-7
PQ20 DMN601K-7
PQ17 DMN601K-7
PQ19 DMN601K-7
PQ18 DMN601K-7
PC80 *2200p/25V_4
Quanta Computer Inc.
PROJECT : ZY7
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Discharge (1.1V/1.2V/2.5V)
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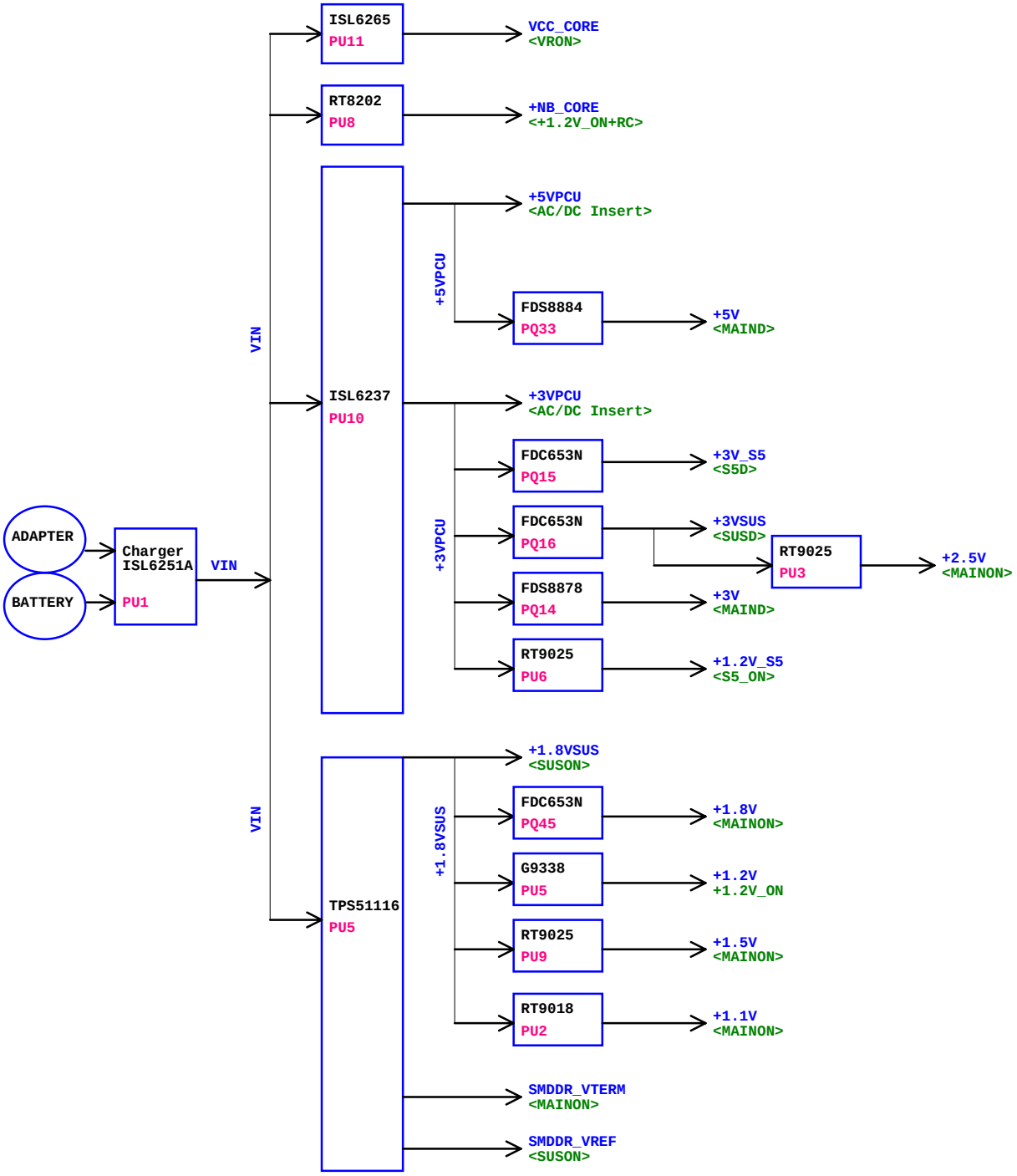

Quanta Computer Inc.
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	Power Tree	1A
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CHANGE LIST

Model	REV	CHANGE LIST
ZY7 MB	1A	1A First release--0107
	2B	Page 02 change C350 from unstuff to 22P for EMI request--0215 Page 03 Add HOLE39 for ME request--0215 Page 06 Del C193, C203, C178 and C184,C185 for ISL6265 request--0226 Page 29 PC172,PC173 for ISL6265 request--0226 Page 09 Add HDMI CAP circuit for layout request --0216 page 10 Add C601,C646,C647,C648 100PF for EMI request--0201 Page 10 Change R149 value from 150ohm to 140 ohm following AMD change---0214 Page 10 Change +3V_AVDD_NB PU from +3V_S5 to +3V follow AMD CRB suggest.--0201 Page 16 Add C641 1N Capacitor to Smoothing NB_PWRGD_IN ---0202 Page 16 Change U7,R179 unstuff,PR183 stuff,follow A1-2chip .--0202 Page 17 Del MXM_POWEREN circuit follow AMD request--0214 Page 18 Change R393 value from 150ohm to 140 ohm following AMD change---0214 Page 19 Add L79,L80 for EMI request--0218 Page 19 add reseve D34,D35,D37,D38 for ESD request--0218 Page 21 SWAP TX0P/N with TX3P/N net for LAN layout issue--0214 Page 21 change R39 Value from 1.24K to 1.2K and sutff R63 for LAN issue--0215 Page 22 del VR button function follow Spec--0218 Page 28 add reverse PR203 ---0218 page 32 PU2 Power source change to +1.8VSUS from +3VPCU--0128
	2C	page 18 add R617,R616,R618,R619 for HDMI vendor suggest--0331 page 21 SWAP CN12 LAN_LINKLED#_SYS and LAN_ACTLED#_SYS net for LAN LED issue---0331 page 22 change u36 footprint---0331 page 22 del SPDF circuit, C684, R561,Q52 cancel, U34 cancel----0331 page 10 unstuff Q50 and R452,stuff R459 follow AMD suggest---0402 page 19 add R198 and R207(reserve) for FP S3 issue---0408 Page 31 change C645 from 1000P to 330P for EMI issue---0408 Page 16 add C684, C696 330PF for EMI issue---0408 Page 12 add C178 10PF for EMI issue ---0408 Page 26 change R35 to 1K for Docking AC issue---0408 Page 18 unstuff R3, Q1,Q4,Q5, Add and stuff D17, D21---0410
	2D	

MODEL	ZY7 FROM	To
	X	1A
	X	1A
	X	1A
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
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	2A	2B
	2A	2B
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	2A	2B
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	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2B	3A

DOC NO.	PROJECT MODEL :	ZY7	APPROVED BY:		DATE:	2008/01/07
	PART NUMBER:		DRAWING BY:		REVISON:	3A

Title <Title>

Size Custom | Document Number <Doc> | Rev <RevCode>

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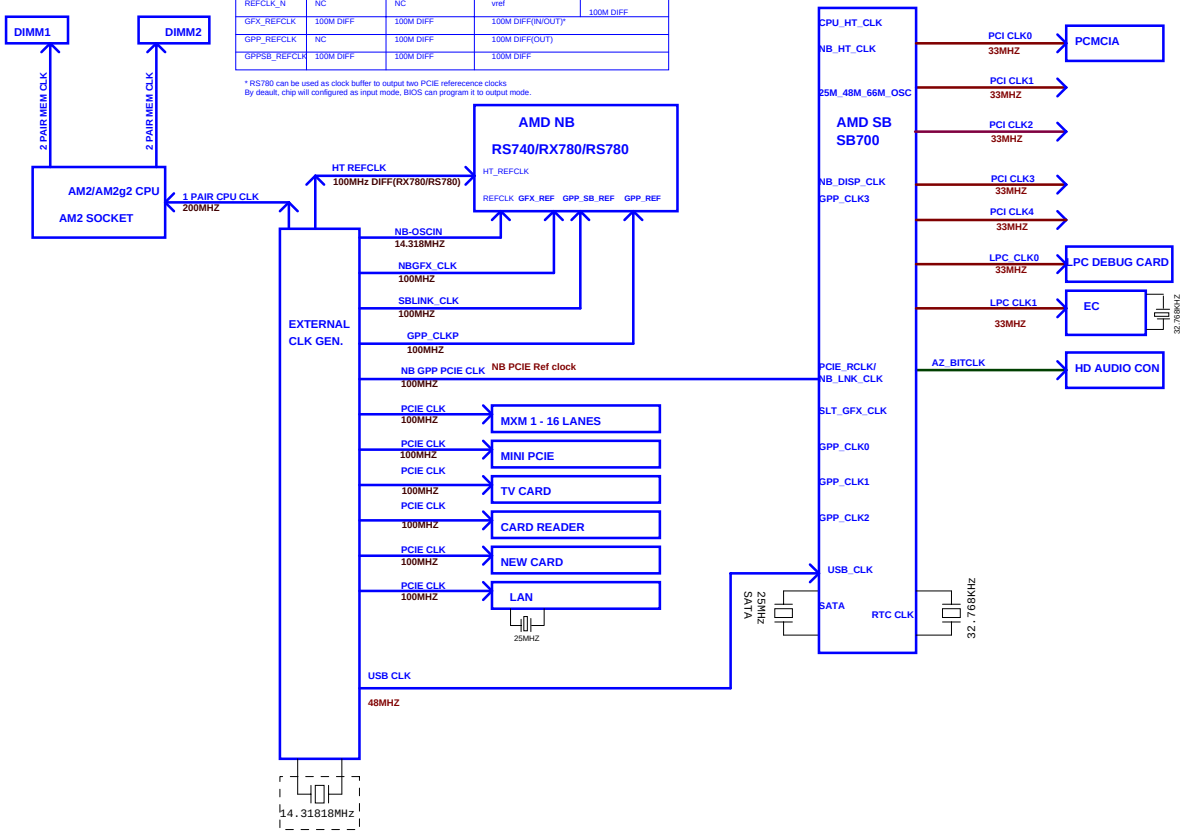
NB CLOCK INPUT TABLE

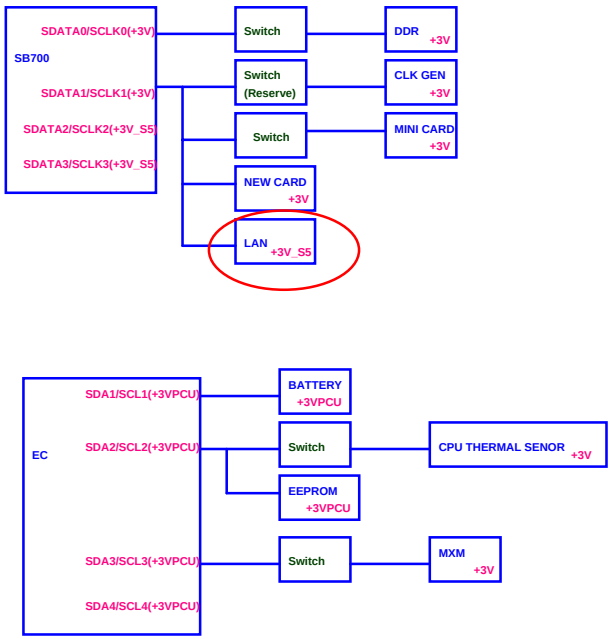
NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* RS780 can be used as clock buffer to output two PCIE refereence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

Clock distribution



SMBUS Table



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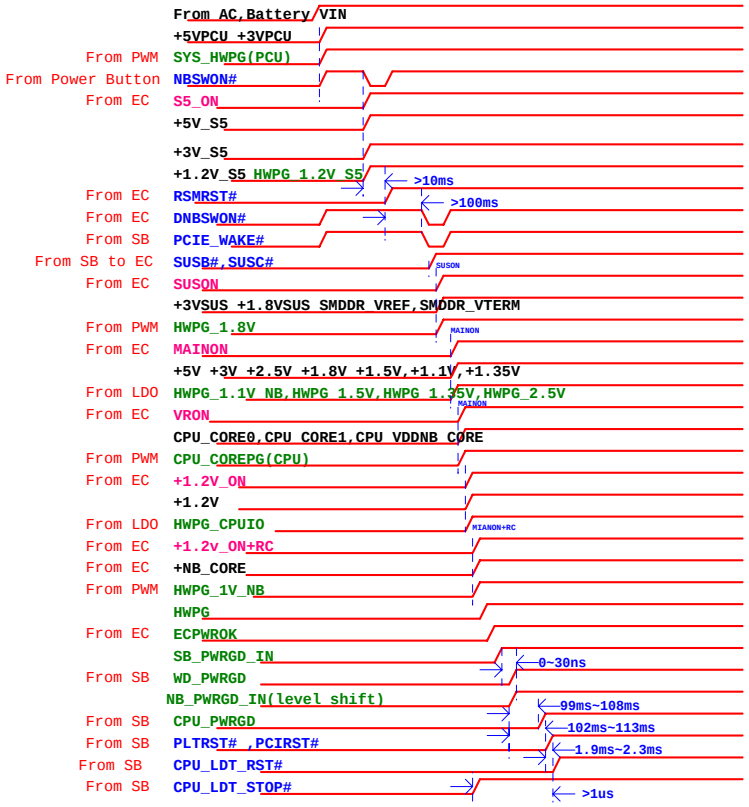
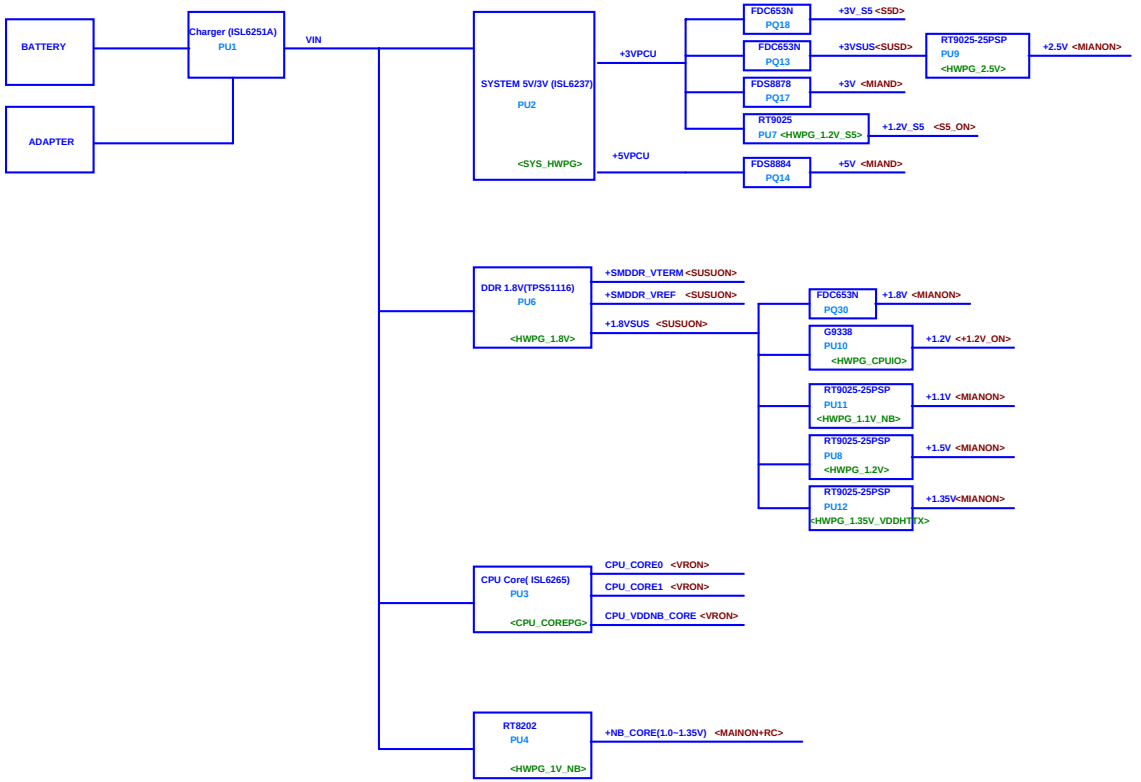
ZY7 Power On Sequence



Power State / Voltage Rail Activity Summary

SYSTEM STATE	SLEEP STATE	PROCESSOR STATE	Description		RTC	ALWAYS	S5	SUS	RUN
G0	S0	C0	RUNNING		ON	ON	ON	ON	ON
G0	S0	C0	RUNNING	P-state transitions under OS control	ON	ON	ON	ON	ON
G0	S0	C1		HALT	ON	ON	ON	ON	ON
G0	S0	C2		Stop grant,caches snoopable	ON	ON	ON	ON	ON
G0	S0	C1E/C3		Stop grant, no LDTSTOP,not expected,cache snoops	ON	ON	ON	ON	ON
G0	S0	C1E/C3		Stop grant with LDTSTOP, cache not snoopable	ON	ON	ON	ON	ON
G1	S1	OFF	SLEEPING	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF		Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF		Suspend to disk	ON	ON	ON	OFF	OFF
G2	S5	OFF	SOFT OFF		ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	POWER BUTTON ONLY		ON	ON	OFF	OFF	OFF
G3		OFF	MECHANICAL OFF		ON	OFF	OFF	OFF	OFF



POWER	Distribution
VCC_CORE	CPU
+5VPCU	FINGERPRINT
+3VPCU	CIR,EC,SW/B,SUSLED,PWR LED,BAT LED,SPI FLASH
+1.1V	RS780
+NB_CORE	RS780
+5V	CRT,HDMI,DOCK,PCMCIA,AUDIO,HDD,ODD,FAN,TP,TV CARD,SB700,MXM
+3V	CPU,CLK GEN,SB700,RS780,MXM,DDR,DOCK,EC,CARD READER,PCMCIA,CODEC,LAN,HDD,NEW CARD,MINI CARD,LCD,CM2009,HDMI,CAMERA,CODEC,HEADPHONE,AMP
+3V_S5	DOCK,MDC,LAN,NEW CARD
+3VSUS	SUSLED,BT
+2.5V	CPU,MXM
+1.2V_S5	SB700
+1.8VSUS	CPU,SB700
+1.8V	CARD READER,RS780,SB700
+1.2V	SB600 , RS780 , CPU , CLK GEN
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+1.5V	NEW CARD,MINI CARD
+5V_S5	

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