C743

ZRJ BLOCK DIAGRAM

01

GPU CORE PWR RT8204 P45	CHARGER ISL88731 P53
GPU IO PWR UP6111AQDD P46	3/5V SYS PWR RT8206 P52
Discharger/+3V_M P54	CPU CORE PWR ISL95831 P43~P44
+1.8V UP61111AQDD P51	CPU +1.05V_VTT UP61111AQDD P47
CPU iGPU_CORE RT8204 P45	PCH +1.05V UP61111AQDD P49
+0.85V ISL62871 P48	DDR3 PWR RT8207A P50

intel
<MCH Processor>
SandyBridge
QC /DC 35W
PCI-E X16
rPGA 988
(37.5mm X 37.5mm)
DDR SYSTEM MEMORY
FDI CLK DMI
P4~P7

DDR III - SODIMM 0
DDR III - SODIMM 1
P14, 15

Dual Channel DDR III
1066/1333 MHz

PCIE X16

X'TAL 27.0MHz

nVIDIA GPU
N12GS & N12GV Fermi
Package GB2-128
Optimus (Muxless)
P16~P22

Channel A
Channel B
VRAM GDDR3
64(or 128)Mb x16 x8 pcs
P14, 15

EXT_HDMI
EXT_CRT
EXT_LVDS

CRT P24
LVDS P24
USB-8
HDMI P24

5GT/s

FDI interface *2.7GT/s*
X4 DMI interface *5GT/s*

HDD (SATA) P25
ODD (SATA) P25
SATA0
SATA1

USB 2.0 * 3
USB0,1,2 P27
Bluetooth
USB9 P27
CCD
USB6 P24
USB 2.0

Azalia

intel
<PCH>
FDI CLK DMI
SATA Gen3
SATA Gen2
iGFX Interfaces
CougarPoint 0.7
USB
PCI-E
HDA
mBGA 989
(25mm X 25mm)
Note:
HM65 not support USB 6 & 7
HM65 not support SATA 2 & 3
RTC
P9
P8~P13
SPI
LPC

INT_CRT
INT_LVDS
INT_HDMI

PCI-Express Gen2
5GT/s

PCIE6
PCIE1
PCIE2

X'TAL 32.768KHz
X'TAL 25MHz
X'TAL 25MHz

Giga LAN
Arthohorus AR8151
P26

Mini Card
WiFi +BT (Half)
USB3 P28
USB3

Mini Card
3G
USB4 P28
USB4

CardReader
Realtek RTS5209
USB5 P23

Transformer
P26

RJ45
P26

SIM Card Conn
DB P28

Audio CODEC
CONEXANT CX20584-21Z
P30

Dual SPI ROM
4MB x1 (Basic ME+Braidwood)
P9

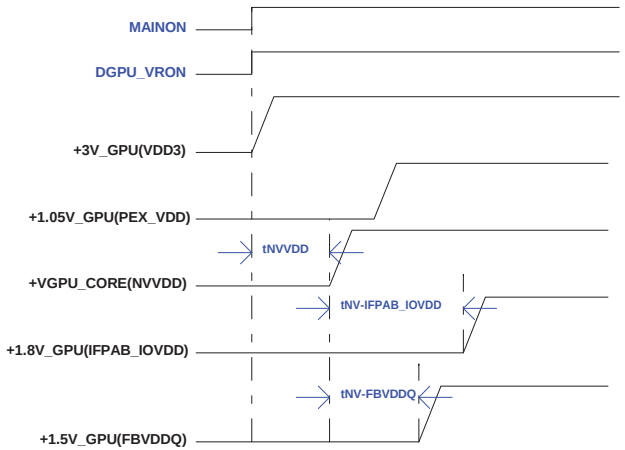
WPCE791/FLASH
NPCE971
P31

HP Jack P30
MIC Jack P30
SPK P30
DMIC P24
SPI ROM P31
Touch Pad P29
Keyboard P29
Light Sensor P33
Button on mechanical key P31
Fan Driver (PWM Type) P42

Quanta Computer Inc.
PROJECT : ZRJ

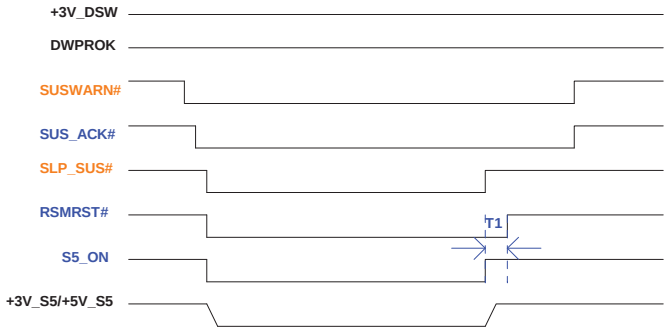
Size	Document Number	Rev
	Block Diagram	1A
Date: Friday, February 11, 2011	Sheet 1 of 41	

N12P-GE Power Up Sequence



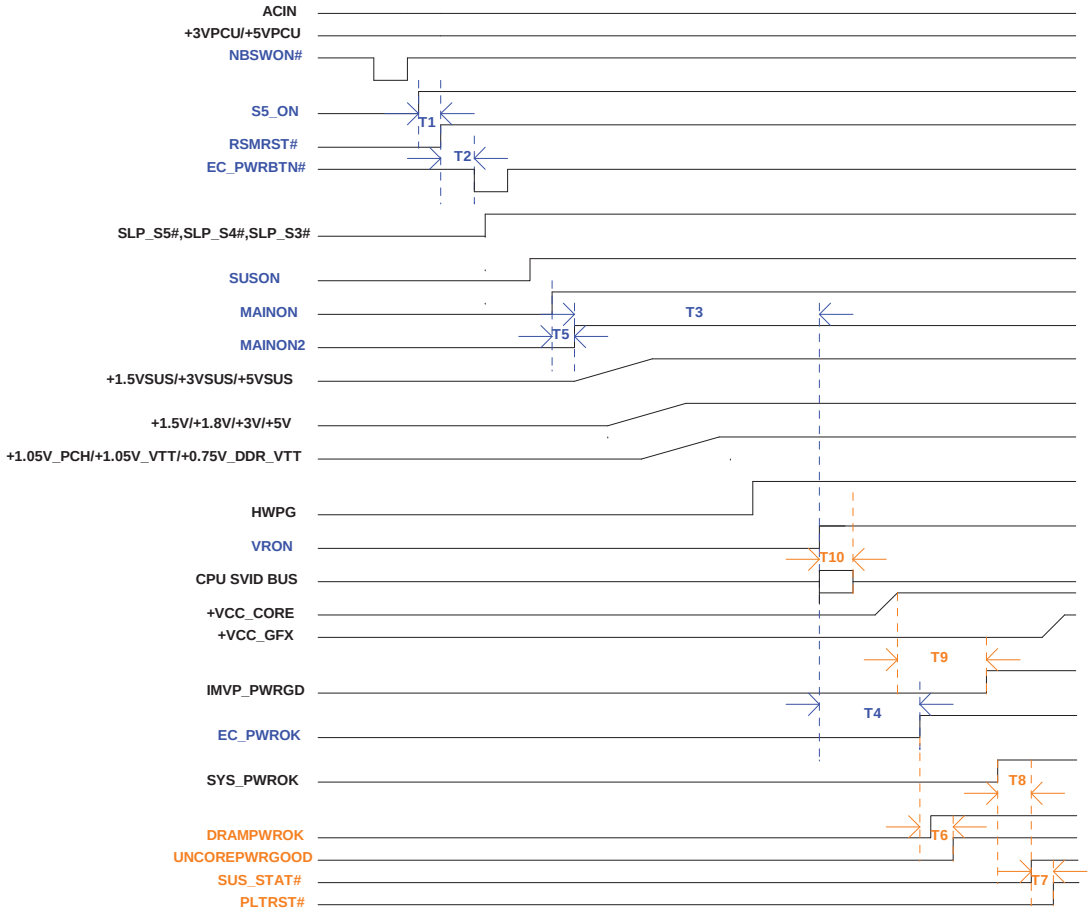
N12P-GE Power up Sequence
tNVVDD>0
tNV-IFPAB_IOVDD>0
tNV-FBVDDQ>0

Deep S4/S5 off-on Sequence

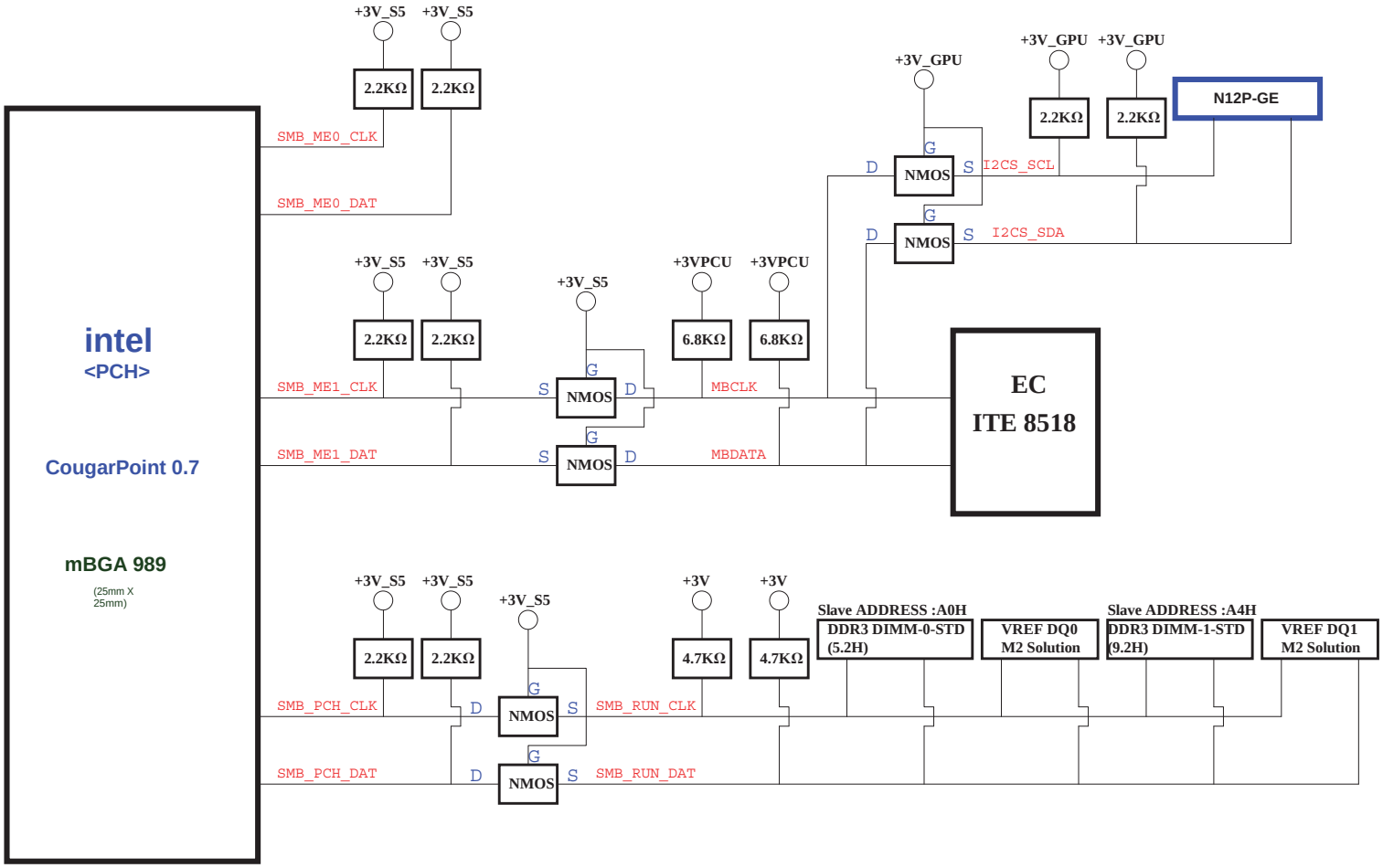


Deep S4/S5 Sequence
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)

MS15-UMA Power-ON Sequence



System Power Sequence
T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO EC_PWRBTN# = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO EC_PWROK = 10ms (HWPG NEED TO BE HIGH at that time)
T5: MAINON to MAINON2 =500us
T6: EC_PWROK to UNCOREPWRGOOD =2ms(Min)
T7: SUS_STAT# to PLTRST# =60us(Min)
T8: SYS_PWROK to SUS_STAT# =1ms(Min)
T9: +VCC_CORE to IMVP_PWRGD =5ms(Max)
T10: VRON to accept SVID command. =5ms(Max)



Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	SMBus Address	1A
Date: Monday, December 13, 2010	Sheet 3 of 41	

Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

04

U26A

DMI

Intel(R) FDI

eDP

PCI EXPRESS* - GRAPHICS

CPU-989P-rPGA

U26B

MISC

THERMAL

PWR MANAGEMENT

CLOCKS

DDR3 MISC

JTAG & BPM

CPU-989P-rPGA

SNB_IVB# N.A at SNB EDS #27637 0.7v1

0.22uF AC coupling Caps for PCIE GEN1/2/3

DP & PEG Compensation

+1.05V_VTT

R125 24.9/F_4 eDP_COMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V_VTT

R154 24.9/F_4 PEG_COMP

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms

PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up(CPU)

+1.05V_VTT

H_PROCHOT#	R192	62_4
XDP_TDO	R215	51_4
XDP_TMS	R218	51_4
XDP_TDI	R217	51_4
XDP_PREQ#	R214	*51_4
XDP_TCLK	R219	51_4
XDP_TRST#	R208	51_4

+1.05V_VTT

[8,35] IMVP_PWRGD

Q13 FDV301N

R209 1K_4

Q12 MMBT3904

PM_THRMTRIP#

SYS_SHDN# [34,41]

eDP Hot-plug

+1.05V_VTT

HPD disable

R126 1K_4

INT_eDP_HPD_Q

Quanta Computer Inc.

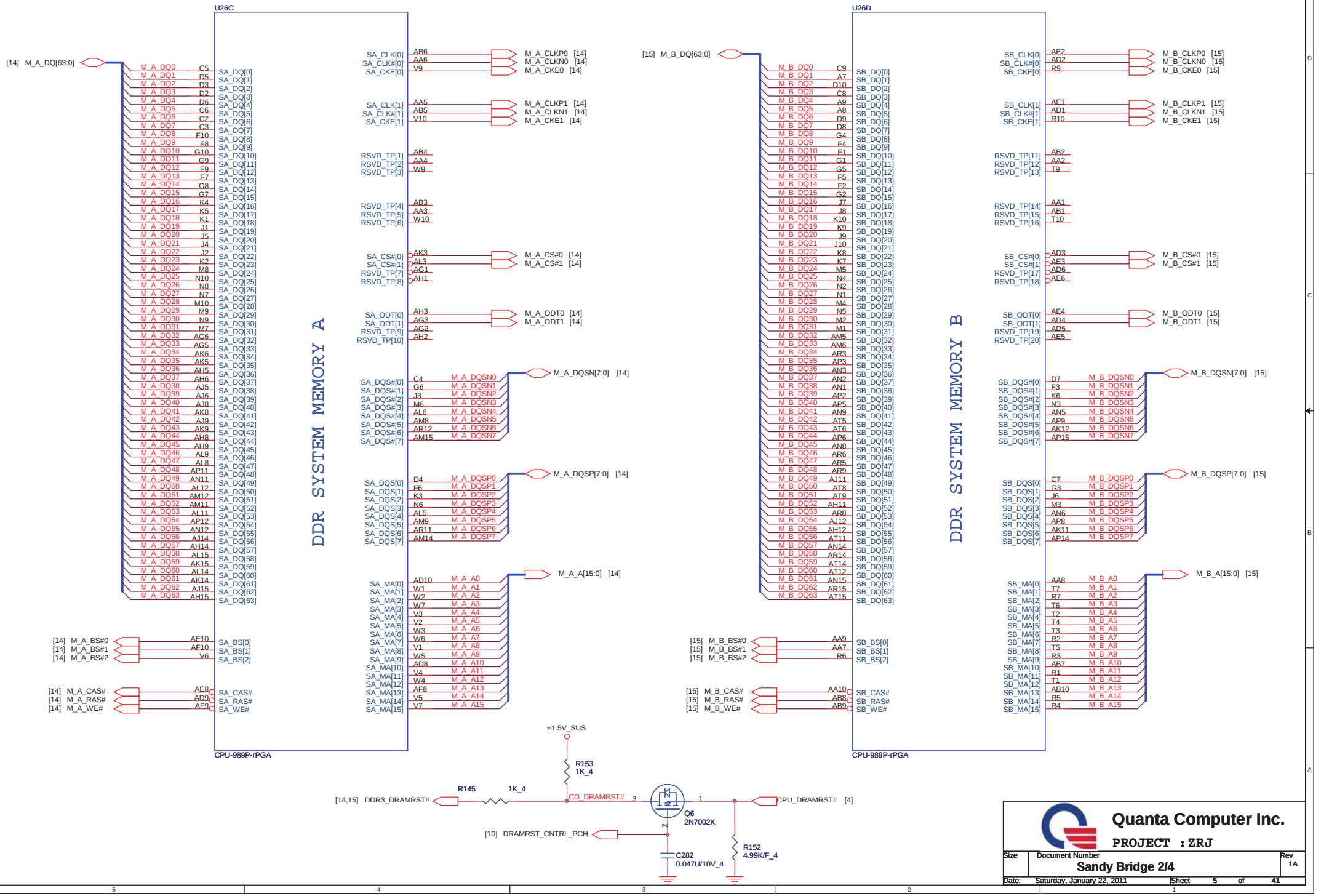
PROJECT : ZRJ

Size	Document Number	Rev
	Sandy Bridge 1/4	1A

Date: Saturday, January 22, 2011 Sheet 4 of 41

Sandy Bridge Processor (DDR3)

05



Quanta Computer Inc.

PROJECT : ZRJ

Size	Document Number	Rev
	Sandy Bridge 2/4	1A
Date: Saturday, January 22, 2011	Sheet 5 of 41	

Sandy Bridge Processor (POWER) CPU VTT

Sandy Bridge Processor (GRAPHIC POWER)

06

POWER

U26F

CPU Core Power
SNB 45W:52A

Spec
470uF/4mohm x 4
22uF x 16
10uF x 10

+VCC_CORE

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

C358 *22U/6.3V_8, C323 10U/6.3V_8, C338 10U/6.3V_8, C307 10U/6.3V_8, C337 10U/6.3V_8, C304 10U/6.3V_8, C318 10U/6.3V_8
C661 10U/6.3V_8, C666 10U/6.3V_8, C672 10U/6.3V_8, C320 10U/6.3V_8, C662 10U/6.3V_8, C671 10U/6.3V_8, C667 10U/6.3V_8
C334 *22U/6.3V_8, C313 10U/6.3V_8, C302 10U/6.3V_8, C319 10U/6.3V_8, C301 10U/6.3V_8, C336 10U/6.3V_8, C314 10U/6.3V_8
C303 *22U/6.3V_8, C316 *22U/6.3V_8, C315 10U/6.3V_8, C317 10U/6.3V_8, C335 10U/6.3V_8, C333 10U/6.3V_8, C332 10U/6.3V_8
C298 *470u/2V_7343, C299 *470u/2V_7343, C340 470u/2V_7343, C306 10U/6.3V_8, C305 10U/6.3V_8

CORE SUPPLY

CPU Core Power
SNB 45W:8.5A

Spec
330uF/6mohm x 2
22uF x 12
22uF x 7 (Non-stuff)

+1.05V_VTT

VCCIO1 AH13, VCCIO2 AH10, VCCIO3 AG10, VCCIO4 AC10, VCCIO5 Y10, VCCIO6 U10, VCCIO7 P10, VCCIO8 L10, VCCIO9 J14, VCCIO10 J13, VCCIO11 J12, VCCIO12 J11, VCCIO13 H14, VCCIO14 H12, VCCIO15 H11, VCCIO16 G14, VCCIO17 G13, VCCIO18 G12, VCCIO19 F14, VCCIO20 F13, VCCIO21 F12, VCCIO22 F11, VCCIO23 E14, VCCIO24 E12, VCCIO25 E11, VCCIO26 D14, VCCIO27 D13, VCCIO28 D12, VCCIO29 D11, VCCIO30 C14, VCCIO31 C13, VCCIO32 C12, VCCIO33 C11, VCCIO34 B14, VCCIO35 B12, VCCIO36 A14, VCCIO37 A13, VCCIO38 A12, VCCIO39 A11, VCCIO40 J23

C616 330u/2V_7343, C326 *330U/2V_7343
C660 10U/6.3V_8, C262 10U/6.3V_8, C673 10U/6.3V_8, C640 10U/6.3V_8, C677 10U/6.3V_8
C668 10U/6.3V_8, C658 10U/6.3V_8, C258 10U/6.3V_8, C265 10U/6.3V_8, C264 10U/6.3V_8
C260 10U/6.3V_8, C639 10U/6.3V_8, C294 10U/6.3V_8
C670 *22U/6.3V_8, C295 *22U/6.3V_8, C663 *22U/6.3V_8, C292 *22U/6.3V_8
R492 *short_4 +1.05V_VTT

PEG AND DDR

SVID

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 VR_SVID_CLK
VIDSOUT AJ28 VR_SVID_DATA

SENSE LINES

VCC_SENSE AJ35, VSS_SENSE AJ34
R180 100/F_4 +VCC_CORE
R181 100/F_4
VCCSENSE [35]
VSSSENSE [35]

VCCIO_SENSE B10, VSSIO_SENSE A10
R487 10/F_4 +1.05V_VTT
R486 10/F_4
VCCP_SENSE [36]
VSSP_SENSE [36]

CPU-989P-rPGA

CPU VGT
SNB 45W:21.5A

Spec
470uF/4mohm x 2
22uF x 12

+VCC_GFX

VAXG1 AT24, VAXG2 AT23, VAXG3 AT21, VAXG4 AT20, VAXG5 AT18, VAXG6 AT17, VAXG7 AR24, VAXG8 AR23, VAXG9 AR21, VAXG10 AR20, VAXG11 AR18, VAXG12 AR17, VAXG13 AP24, VAXG14 AP23, VAXG15 AP21, VAXG16 AP20, VAXG17 AP18, VAXG18 AP17, VAXG19 AN24, VAXG20 AN23, VAXG21 AN21, VAXG22 AN20, VAXG23 AN18, VAXG24 AN17, VAXG25 AM24, VAXG26 AM23, VAXG27 AM21, VAXG28 AM20, VAXG29 AM18, VAXG30 AM17, VAXG31 AL24, VAXG32 AL23, VAXG33 AL21, VAXG34 AL20, VAXG35 AL18, VAXG36 AL17, VAXG37 AK24, VAXG38 AK23, VAXG39 AK21, VAXG40 AK20, VAXG41 AK18, VAXG42 AK17, VAXG43 AJ24, VAXG44 AJ23, VAXG45 AJ21, VAXG46 AJ20, VAXG47 AJ18, VAXG48 AJ17, VAXG49 AH24, VAXG50 AH23, VAXG51 AH21, VAXG52 AH20, VAXG53 AH18, VAXG54 AH17

C694 *330U/2V_7343, C696 *330U/2V_7343, C695 *330U/2V_7343
C387 10U/6.3V_8, C379 10U/6.3V_8, C388 10U/6.3V_8, C381 10U/6.3V_8
C382 10U/6.3V_8, C390 10U/6.3V_8, C380 10U/6.3V_8, C384 10U/6.3V_8
C391 4.7U/25V_8, C392 4.7U/25V_8, C675 4.7U/25V_8, C691 4.7U/25V_8
C690 *22U/6.3V_8, C676 *22U/6.3V_8, C689 *22U/6.3V_8, C386 *22U/6.3V_8

GRAPHICS

CPU VCCPL
SNB 45W:1.5A

Spec
330uF/7mohm x 1
10uF x 1
1uF x 2

+1.8V

VCCPLL1 B6, VCCPLL2 A6, VCCPLL3 A2

C270 4.7U/6.3V_6, C268 1U/6.3V_4, C269 1U/6.3V_4, C619 *330u/6.3V_7343

1.8V RAIL

CPU-989P-rPGA

SENSE LINES

VAXG_SENSE AK35, VSSAXG_SENSE AK34
R182 10/F_4 +VCC_GFX
R183 10/F_4
VCC_AXG_SENSE [35]
VSS_AXG_SENSE [35]

VREF

SM_VREF AL1
+VDDR_REF_CPU
+VDDR_REF_CPU
CAD Note: +VDDR_REF_CPU should have 10 mil trace width

CPU MCH
SNB 45W: 5A

Spec
330uF/6mohm x 1
10uF x 6

Real
10uF x 6

DDR3 -1.5V RAILS

+1.5V_CPU

VDDQ1 AF7, VDDQ2 AF4, VDDQ3 AF1, VDDQ4 AC7, VDDQ5 AC4, VDDQ6 AC1, VDDQ7 Y7, VDDQ8 Y4, VDDQ9 Y1, VDDQ10 U7, VDDQ11 U4, VDDQ12 U1, VDDQ13 P7, VDDQ14 P4, VDDQ15 P1

C348 4.7U/25V_8, C324 4.7U/25V_8, C288 4.7U/25V_8, C309 4.7U/25V_8, C289 4.7U/25V_8
C359 4.7U/25V_8, C360 10U/6.3V_8, C290 10U/6.3V_8, C354 *330U/2V_7343

SA RAIL

VCCSA

VCCSA1 M27, VCCSA2 M26, VCCSA3 L26, VCCSA4 J26, VCCSA5 J25, VCCSA6 J24, VCCSA7 H26, VCCSA8 H25

C291 4.7U/25V_8, C283 4.7U/25V_8, C286 4.7U/25V_8, C287 *330U/2V_7343

CPU SA
SNB 45W: 6A

Spec
330uF/7mohm x 1
10uF x 3

MISC

VCCSA_SENSE H23
VCCSA_SENSE [39]

FC_C22 C22, VCCSA_VID1 C24
H_FC_C22 R129 10K_4
VCCSA_SEL [39]

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

VR_SVID_CLK
VR_SVID_CLK [35]

Place PU resistor close to CPU

+1.05V_VTT
R190 130/F_4

SVID DATA

VR_SVID_DATA
VR_SVID_DATA [35]

Place PU resistor close to CPU

+1.05V_VTT
R191 75_4

SVID ALERT

H_CPU_SVIDALRT# R184 43_4 VR_SVID_ALERT#
VR_SVID_ALERT# [35]

+SMDDR_VREF R195 *short_8 +VDDR_REF_CPU
Q11 *2N7002E
[34,37,40] MAIND
R196 *100K_4

4.5A

+1.5V_SUS R178 *short_1206 +1.5V_CPU
R168 *short_1206
Q10 *AO4496
MAIND
C357 *470P/50V_4
R155 *220_8
[4,40] MAINON_ON_G
Q7 *DMN601K-7

Quanta Computer Inc.		
PROJECT : ZRJ		
Size	Document Number: Sandy Bridge 3/4	Rev: 1A
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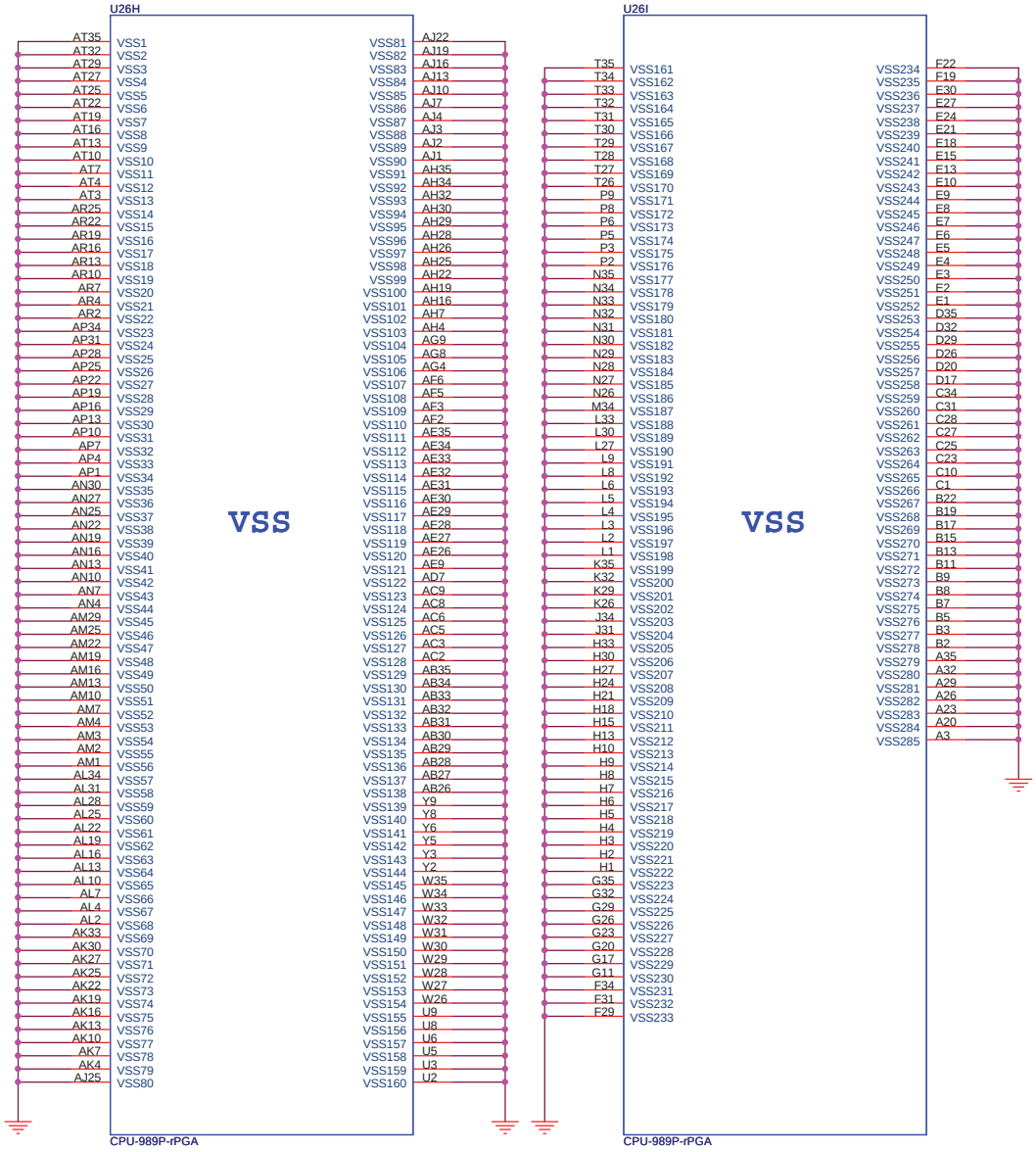
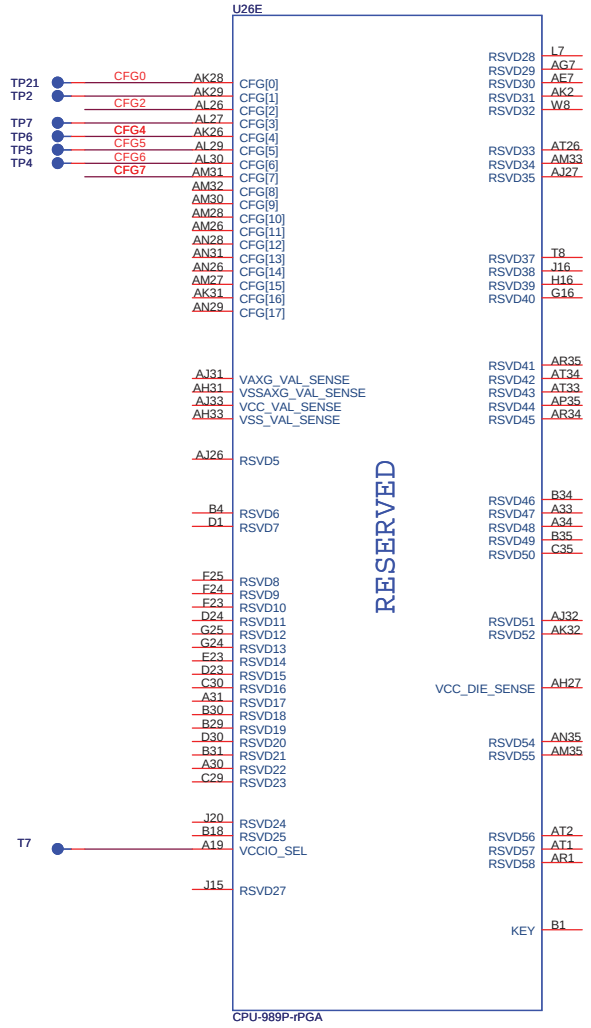
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

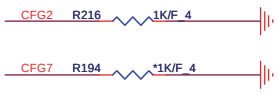
07



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	Sandy Bridge 4/4	1A
Date: Monday, December 20, 2010	Sheet 7 of 41	

Cougar Point (DMI,FDI,PM)

U28C

DMI0RXN / DMI1RXN / DMI2RXN / DMI3RXN
DMI0RXP / DMI1RXP / DMI2RXP / DMI3RXP
DMI0TXN / DMI1TXN / DMI2TXN / DMI3TXN
DMI0TXP / DMI1TXP / DMI2TXP / DMI3TXP
DMI_ZCOMP
DMI_IRCOMP
DMI2RBIAS

DMI

FDI_RXN0 FDI_RXN1 FDI_RXN2 FDI_RXN3 FDI_RXN4 FDI_RXN5 FDI_RXN6 FDI_RXN7
FDI_RXP0 FDI_RXP1 FDI_RXP2 FDI_RXP3 FDI_RXP4 FDI_RXP5 FDI_RXP6 FDI_RXP7
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

FDI

+1.05V_VTT R237 49.9/F_4 DMI_COMP
R235 750/F_4 DMI2RBIAS

System Power Management

SUSACK# SYS_RESET# SYS_PWROK PWROK APWROK DRAMPWROK RSMRST# SUSWARN#/SUSPWRDNACK/GPIO30 PWRBTN# ACPRESENT / GPIO31 BATLOW# / GPIO72 RI# SLP_LAN# / GPIO29

DSWVRMEN DSWVREN
DPWROK R596 *short_4 ICH_RSMRST#
WAKE# PCIE_WAKE# [25]
CLKRUN# / GPIO32 CLKRUN# [32]
SUS_STAT# / GPIO61 SUS_STAT# [32]
SUSCLK / GPIO62 PCH_SUSCLK [32]
SLP_S5# / GPIO63 T13
SLP_S4# SUSC# [32]
SLP_S3# SUSB# [32]
SLP_A# T11
SLP_SUS# T12
PMSYNCH PM_SYNC [4]
SLP_LAN# K14 SLP_LAN#

CougarPoint_R1P0

Cougar Point (LVDS,DDI)

+3V R274 2.2K_4 INT_LVDS_EDIDCLK
R275 2.2K_4 INT_LVDS_EDIDDATA

U28D

L_BKLTEN L_VDD_EN L_BKLTCTL L_DDC_CLK L_DDC_DATA L_CTRL_CLK L_CTRL_DATA LVD_IBG LVD_VBG LVD_VREFH LVD_VREFL
LVDSA_CLK# LVDSA_CLK LVDSA_DATA#0 LVDSA_DATA#1 LVDSA_DATA#2 LVDSA_DATA#3 LVDSA_DATA0 LVDSA_DATA1 LVDSA_DATA2 LVDSA_DATA3
LVDSB_CLK# LVDSB_CLK LVDSB_DATA#0 LVDSB_DATA#1 LVDSB_DATA#2 LVDSB_DATA#3 LVDSB_DATA0 LVDSB_DATA1 LVDSB_DATA2 LVDSB_DATA3

LVDS

CRT_BLUE CRT_GREEN CRT_RED CRT_DDC_CLK CRT_DDC_DATA CRT_HSYNC CRT_VSYNC DAC_IREF CRT_IRTN

CRT

Digital Display Interface

SDVO_TVCLKINN SDVO_TVCLKINP SDVO_STALLN SDVO_STALLP SDVO_INTN SDVO_INTP SDVO_CTRLCLK SDVO_CTRLDATA
DDPB_AUXN DDPB_AUXP DDPB_HPD DDPB_0N DDPB_0P DDPB_1N DDPB_1P DDPB_2N DDPB_2P DDPB_3N DDPB_3P
DDPC_CTRLCLK DDPC_CTRLDATA DDPC_AUXN DDPC_AUXP DDPC_HPD DDPC_0N DDPC_0P DDPC_1N DDPC_1P DDPC_2N DDPC_2P DDPC_3N DDPC_3P
DDPD_CTRLCLK DDPD_CTRLDATA DDPD_AUXN DDPD_AUXP DDPD_HPD DDPD_0N DDPD_0P DDPD_1N DDPD_1P DDPD_2N DDPD_2P DDPD_3N DDPD_3P

INT_HDMI_SCL INT_HDMI_SDA INT_HDMI_HPD INT_HDMI_TXDN2 INT_HDMI_TXDP2 INT_HDMI_TXDN1 INT_HDMI_TXDP1 INT_HDMI_TXDN0 INT_HDMI_TXDP0 INT_HDMI_TXCN INT_HDMI_TXCP

INT. HDMI

INT. DP

R place close to PCH
R300 150/F_4 INT_CRT_BLU
R292 150/F_4 INT_CRT_GRE
R284 150/F_4 INT_CRT_RED

+3V R285 2.7K_4 INT_CRT_DDCCLK
R293 2.7K_4 INT_CRT_DDCDAT

R320 20/F_4 INT_CRT_HSYNC_R
R306 20/F_4 INT_CRT_VSYNC_R

DAC_IREF R287 1K/F_4

CougarPoint_R1P0

PCH Pull-high/low(CLG)

+3V: CLKRUN# R547 8.2K_4; XDP_DBRST# R554 10K_4; R555 *1K_4; ICH_RSMRST# R578 10K_4; SYS_PWROK R277 10K_4

+3V_S5: PM_RI# R564 10K_4; PM_BATLOW# R341 8.2K_4; PCIE_WAKE# R565 10K_4; SLP_LAN# R360 *10K_4; SUS_PWR_ACK R568 10K_4; AC_PRESENT R362 10K_4; PM_DRAM_PWRGD R572 200/F_4

System PWR_OK(CLG)

+3V_S5 C461 *0.1U/10V_4

U17 TC7SH08

[4,32] SYS_PWROK SYS_PWROK_4 IMVP_PWRGD [4,35] PWROK_EC R263 100K_4

+3V_RTC R588 330K_4 DSWVREN R574 *330K_4

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

Quanta Computer Inc.
PROJECT : ZRJ

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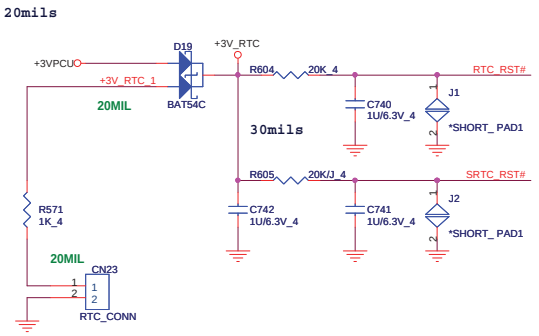
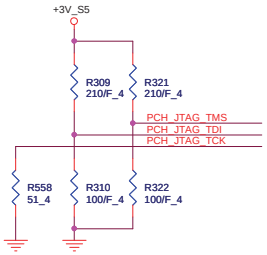
RTC Circuitry(RTC)



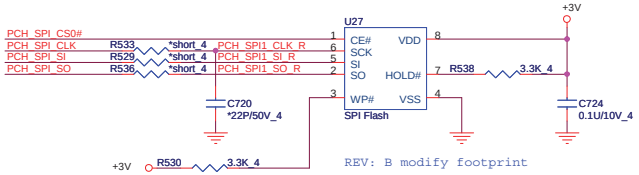
HDA Bus(CLG)

PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

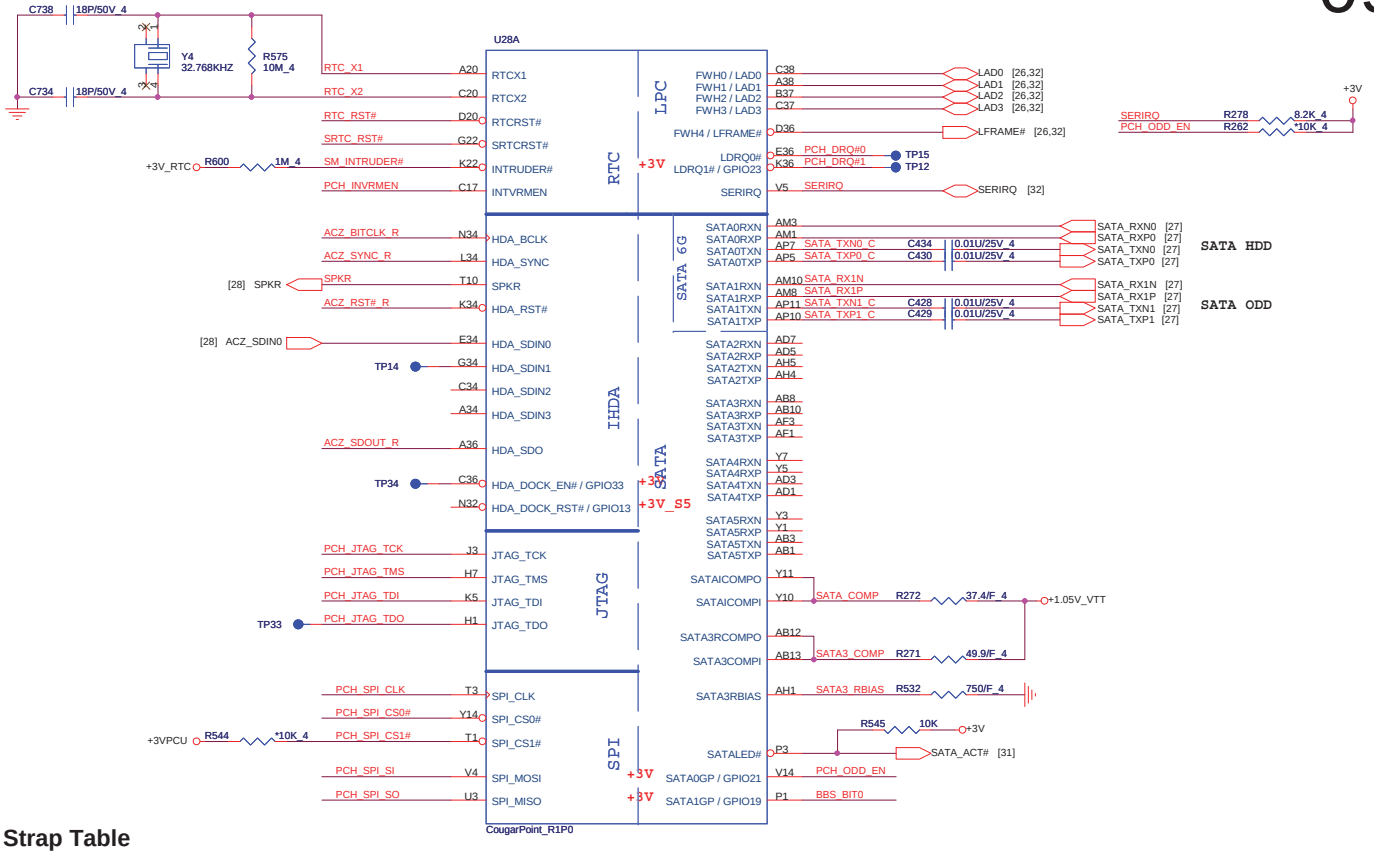
MX25L3205DM2I-12G: AKE39FP0Z00
W25X32VSSIG: AKE39ZP0N00



PCH2 (CLG)

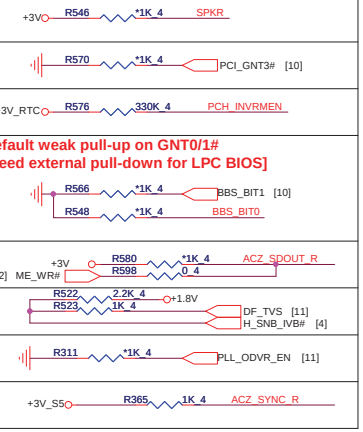
Cougar Point (HDA,JTAG,SATA)

09



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)



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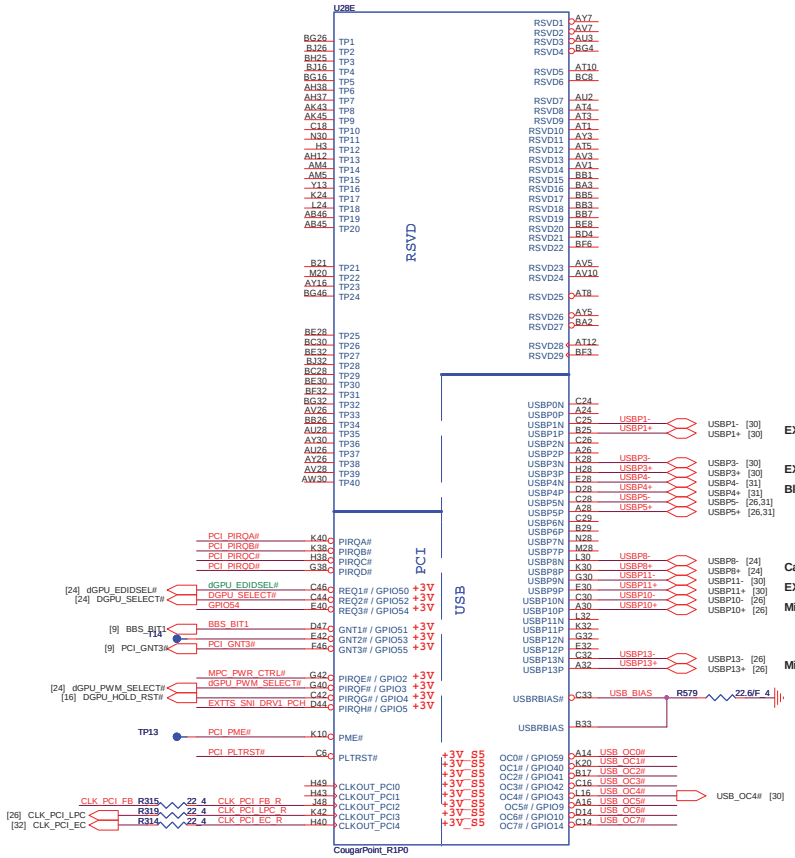
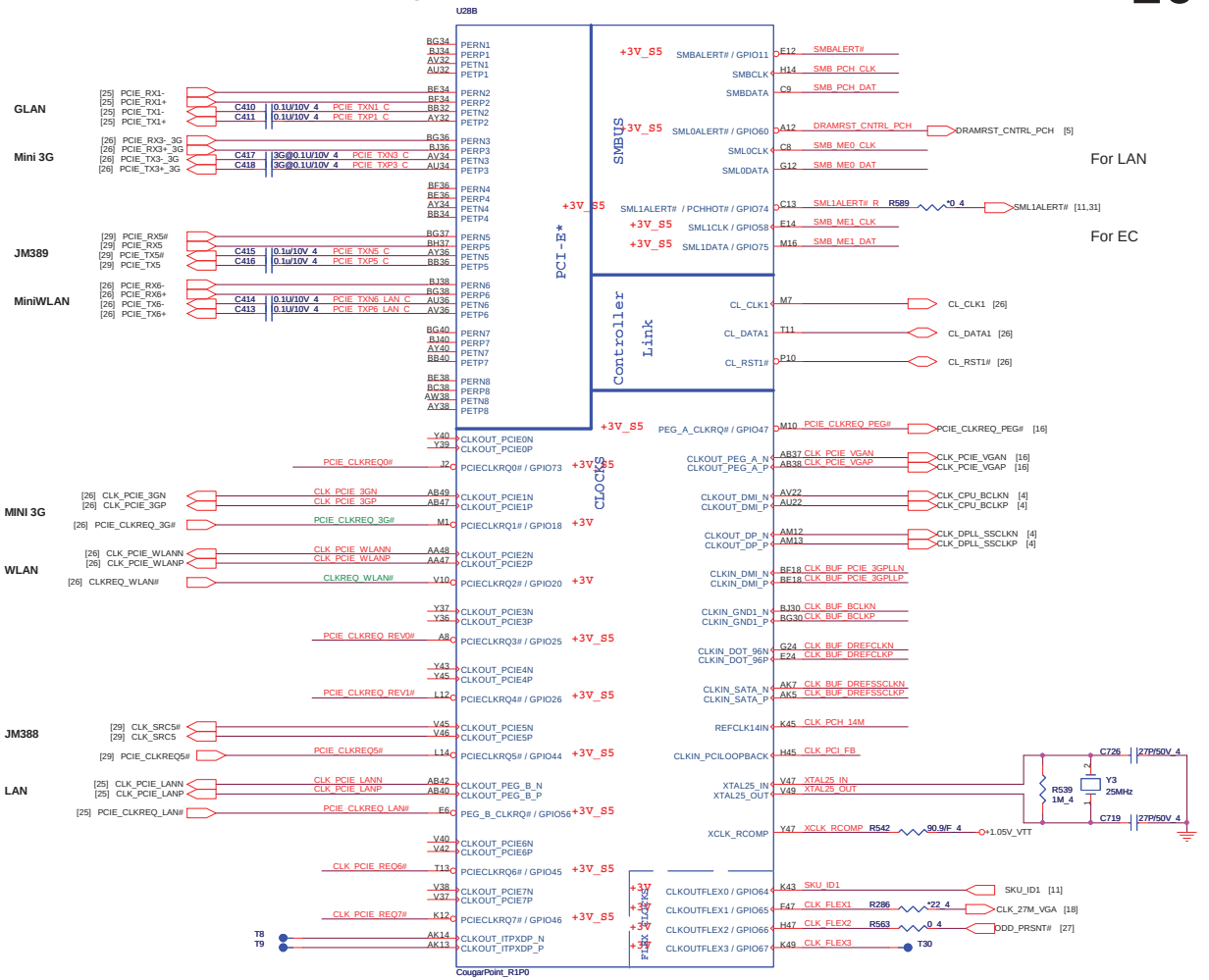
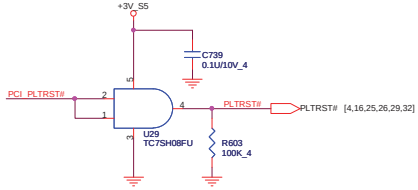
Cougar Point-M (PCI,USB,NVRAM)



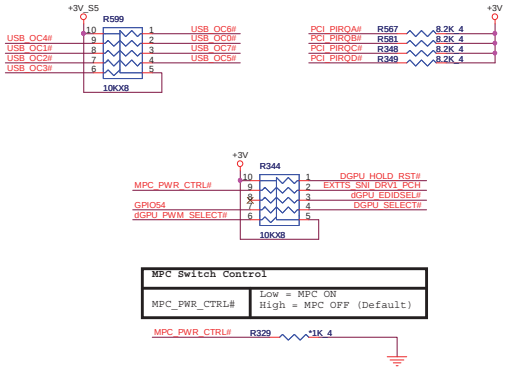
Cougar Point-M (PCI-E,SMBUS,CLK)



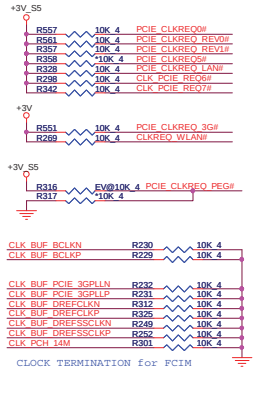
PLTRST#(CLG)



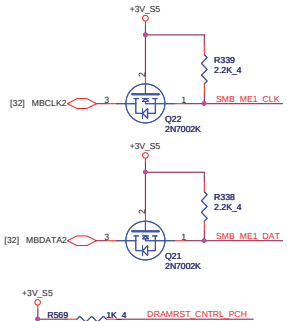
PCI/USBOC# Pull-up(CLG)



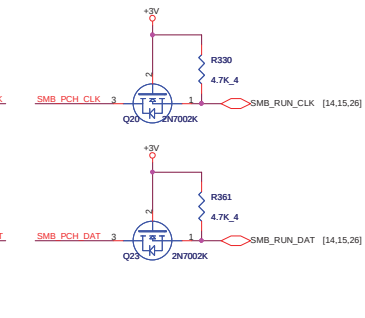
CLK_REQ/Strap Pin(CLG)

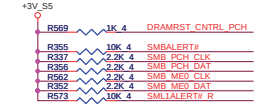


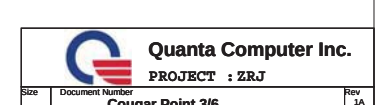
SMBus/Pull-up(CLG)



SMBus(PCH)







Cougar Point (GPIO,VSS_NCTF,RSVD)

U28F

S_GPIO	R283	100_4	T7	BMBUSY# / GPIO0	+3V	+3V	TACH4 / GPIO68	C40	DGPU_PRSNT#
[32] EC_EXT_SMI#	EC_EXT_SMI#		A42	TACH1 / GPIO1	+3V	+3V	TACH5 / GPIO69	B41	R583 1.5K/F_4
	BOARD_ID1		H36	TACH2 / GPIO6	+3V	+3V	TACH6 / GPIO70	C41	R593 1.5K/F_4 +3V
[32] EC_EXT_SCI#	EC_EXT_SCI#		E38	TACH3 / GPIO7	+3V	+3V	TACH7 / GPIO71	A40	R592 1.5K/F_4
TP16			C10	GPIO8	+3V_S5				
	SMIB#		C4	LAN_PHY_PWR_CTRL / GPIO12		+3V_S5			
	PCH_GPIO15		G2	GPIO15	+3V_S5				
check VR_ON GPIO	SKU_ID0		U2	SATA4GP / GPIO16	+3V				
[16,32] dGPU_PWROK	dGPU_PWROK		D40	TACH0 / GPIO17	+3V				
	BIOS_REC		T5	SCLOCK / GPIO22	+3V				
	CR_WAKER#		E8	GPIO24 / MEM_LED	+3V_S5				
	GPIO27		E16	GPIO27	DSW				
[9] PLL_ODVR_EN	R308 *short_4	PLL_ODVR_EN_R	P8	GPIO28	+3V_S5				
Need Check	STP_PCI#		K1	STP_PCI# / GPIO34	+3V				
[32,38,40] dGPU_VRON			K4	GPIO35	+3V				
[40] DGPU_PWR_EN	DGPU_PWR_EN R280	0_4 DMI_OVRVLTG	V8	SATA2GP / GPIO36	+3V				
	FDI_OVRVLTG		M5	SATA3GP / GPIO37	+3V				
	MFG_MODE		N2	SLOAD / GPIO38	+3V				
	BOARD_ID0		M3	SDATAOUT0 / GPIO39	+3V				
	TEST_SET_UP		V13	SDATAOUT1 / GPIO48	+3V				
[10,31] SML1ALERT#	R534 0_4	CRIT_TEMP_REP#	V3	SATA5GP / GPIO49	+3V				
	SV_DET		D6	GPIO57	+3V_S5				

GPIO

CPU/MISC

A20GATE	P4	EC_A20GATE [32]	
PECI	AU16	R188 *0_4	EC_PECI [4,32]
RCIN#	P5	EC_RCIN	EC_RCIN# [32]
PROCPWRGD	AY11		H_PWRGOOD [4,32]
THRMTRIP#	AY10	PCH_THRMTRIP# R245 390_4	PM_THRMTRIP# [4]
INIT3_3V#	T14		
DF_TVS	AY1		DF_TVS [9]
TS_VSS1	AH8		
TS_VSS2	AK11		
TS_VSS3	AH10		
TS_VSS4	AK10		
NC_1	P37		

NCTF

VSS_NCTF_1	A4	VSS_NCTF_15	BG2
VSS_NCTF_2	A44	VSS_NCTF_16	BG48
VSS_NCTF_3	A45	VSS_NCTF_17	BH3
VSS_NCTF_4	A46	VSS_NCTF_18	BH47
VSS_NCTF_5	A5	VSS_NCTF_19	BJ4
VSS_NCTF_6	A6	VSS_NCTF_20	BJ44
VSS_NCTF_7	B3	VSS_NCTF_21	BJ45
VSS_NCTF_8	B47	VSS_NCTF_22	BJ46
VSS_NCTF_9	BD1	VSS_NCTF_23	BJ5
VSS_NCTF_10	BD49	VSS_NCTF_24	BJ6
VSS_NCTF_11	BE1	VSS_NCTF_25	C2
VSS_NCTF_12	BE49	VSS_NCTF_26	C48
VSS_NCTF_13	BF1	VSS_NCTF_27	D1
VSS_NCTF_14	BF49	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

CougarPoint_R1P0

	DGPU_PRSNT# (GPIO68)	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
Discrete Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	DIS/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
1 = GPU power is control by H/W (pure Discrete SKU)

+3V
R591 IV@10K_4 DGPU_PRSNT#
R582 EV@100K_4

+3V
R594 EV@10K_4 SKU_ID1 [10]
R585 IV@10K_4

+3V
R543 *10K_4 SKU_ID0
R541 10K_4

+3V
R553 10K_4 BOARD_ID0 R552 *10K_4
R590 10K_4 BOARD_ID1 R601 *10K_4

+3V_S5
R327 *10K_4 SV_DET R331 100K_4

SV_SET_UP

High = Strong (Default)

+3V
TEST_SET_UP R265 10K_4
R270 *0_4

SGPIO

+3V
S_GPIO R289 1K/F_4
R282 *0_4

+3V_S5
PCH_GPIO15 R559 1K_4

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

MFG-TEST

+3V
MFG_MODE R549 10K_4
R550 *0_4

GPIO Pull-up/Pull-down(CLG)

+3V_S5
CR_WAKER# R332 10K_4
SMIB# R560 10K_4
PLL_ODVR_EN R296 *10K_4

+3V
EC_EXT_SMI# R584 10K_4
EC_EXT_SCI# R351 10K_4
STP_PCI# R556 *10K_4
EC_A20GATE R299 10K_4
EC_RCIN# R297 10K_4
CRIT_TEMP_REP# R535 10K_4

GPIO27 R353 *10K_4
dGPU_PWROK R354 *10K_4

+3V
FDI_OVRVLTG R318 *10K/F_4

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

+3V
DMI_OVRVLTG R279 *200K/F_4

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

+3V
BIOS_REC R290 10K_4
R291 *0_4

BIOS RECOVERY	High = Disable (Default) Low = Enable

Quanta Computer Inc.
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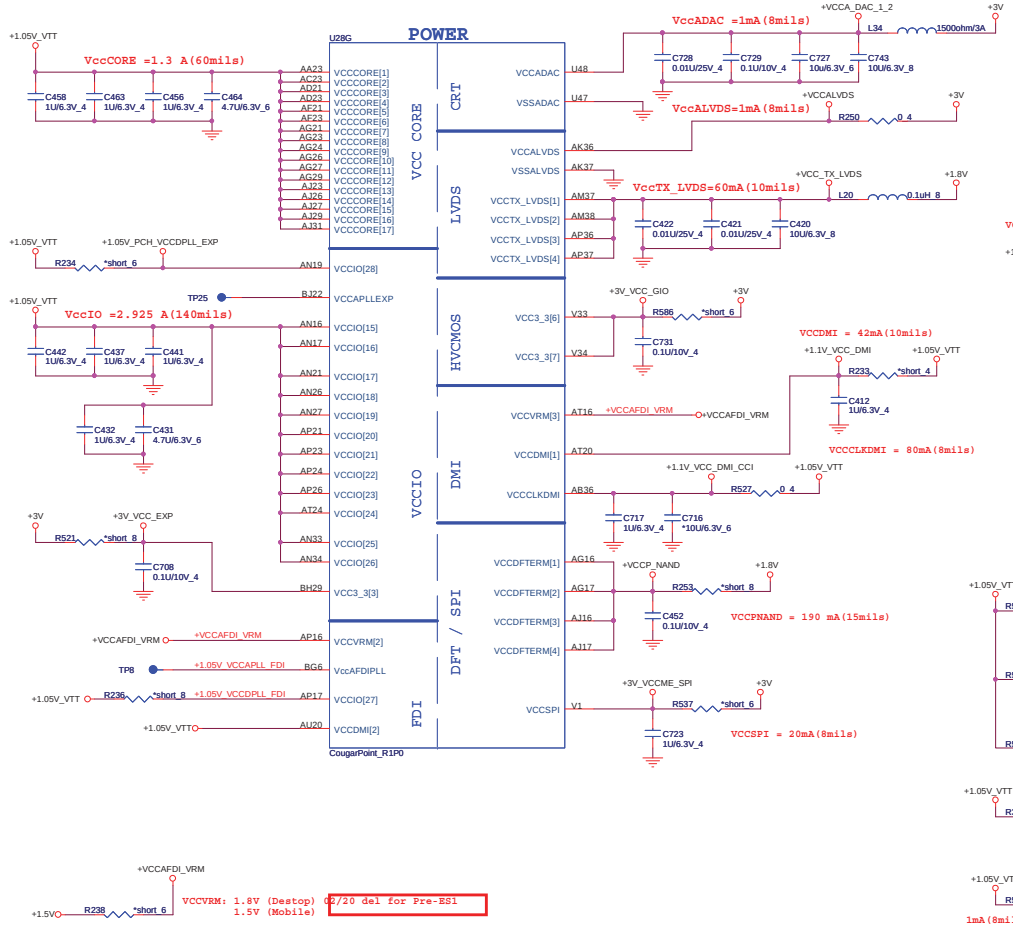
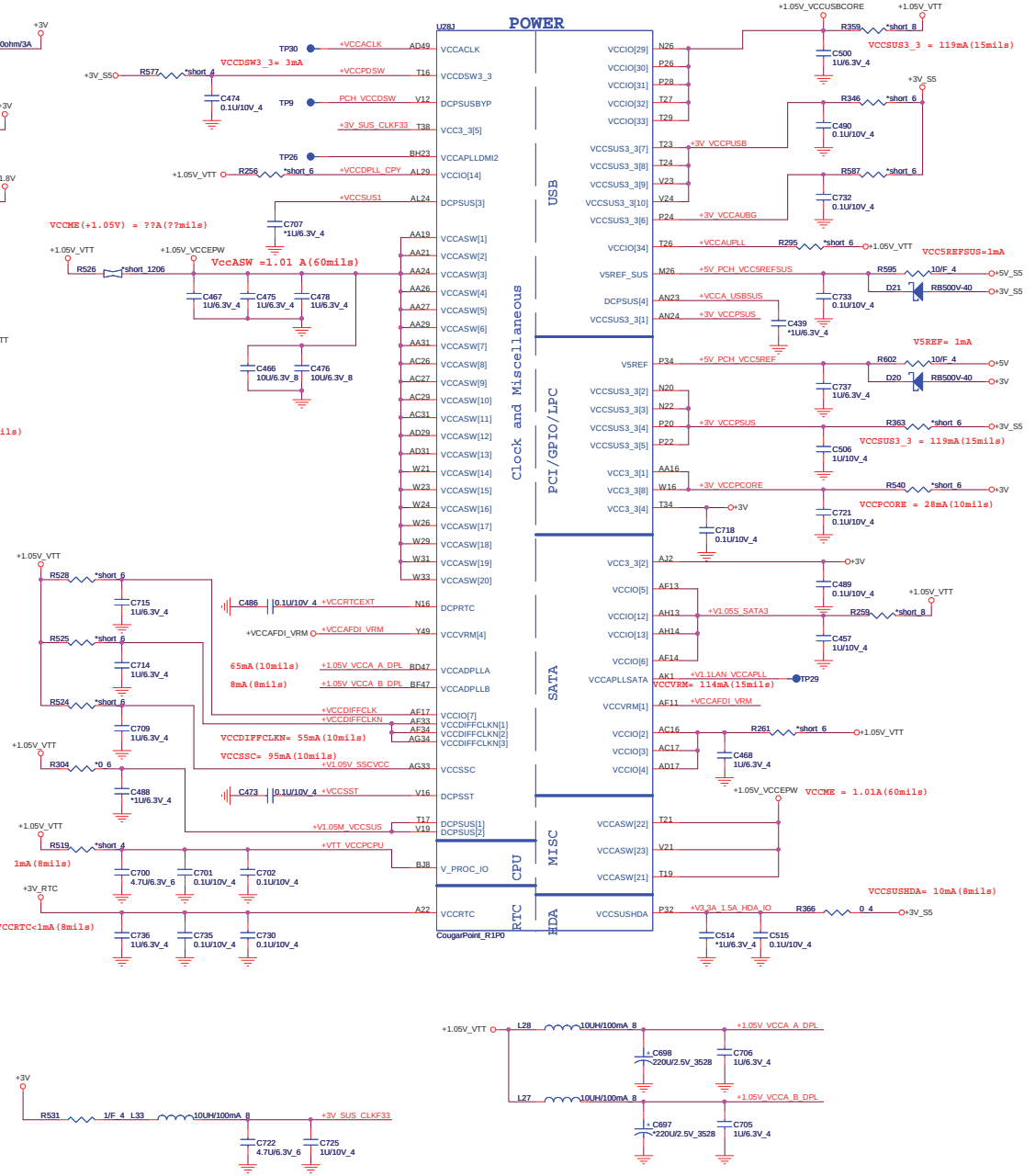
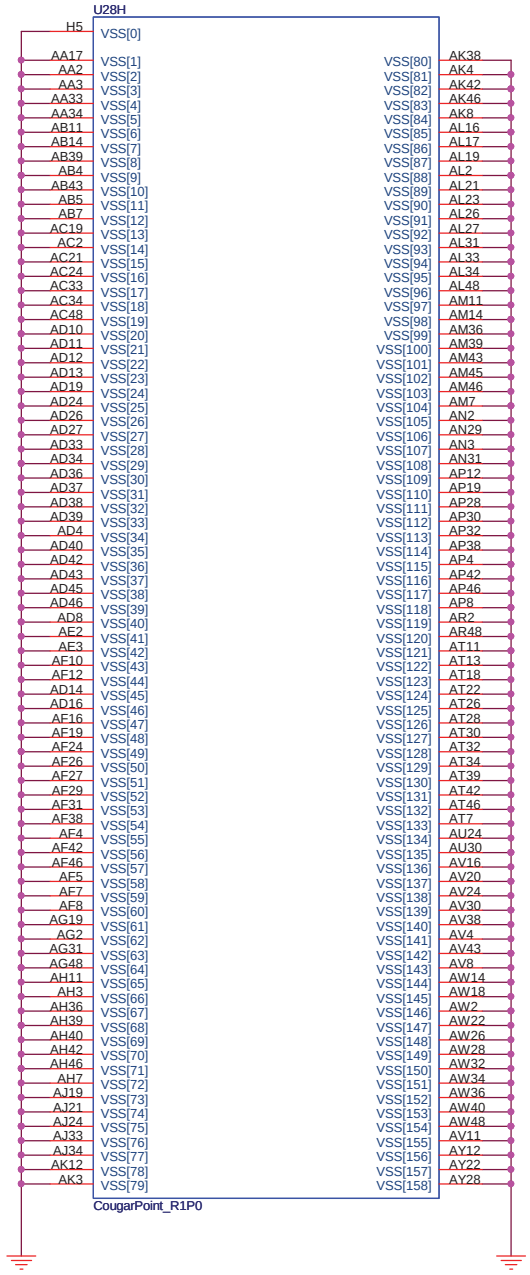
COUGAR POINT (POWER)

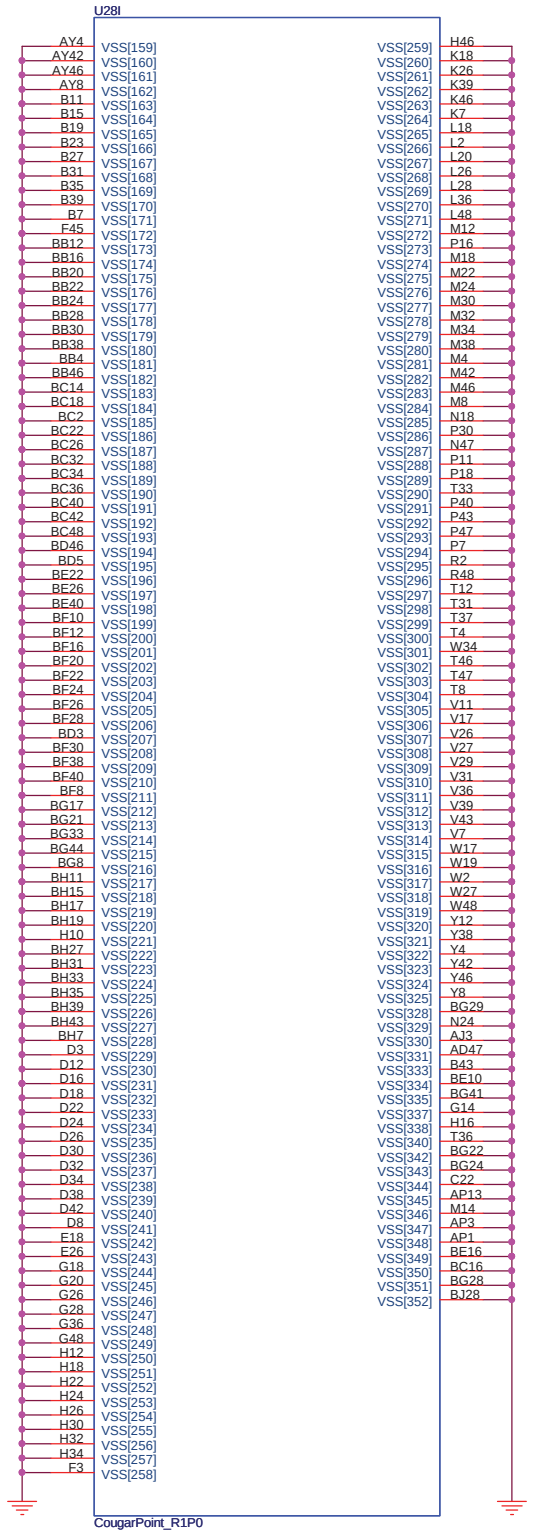


Cougar Point-M (POWER)



IBEX PEAK-M (GND)





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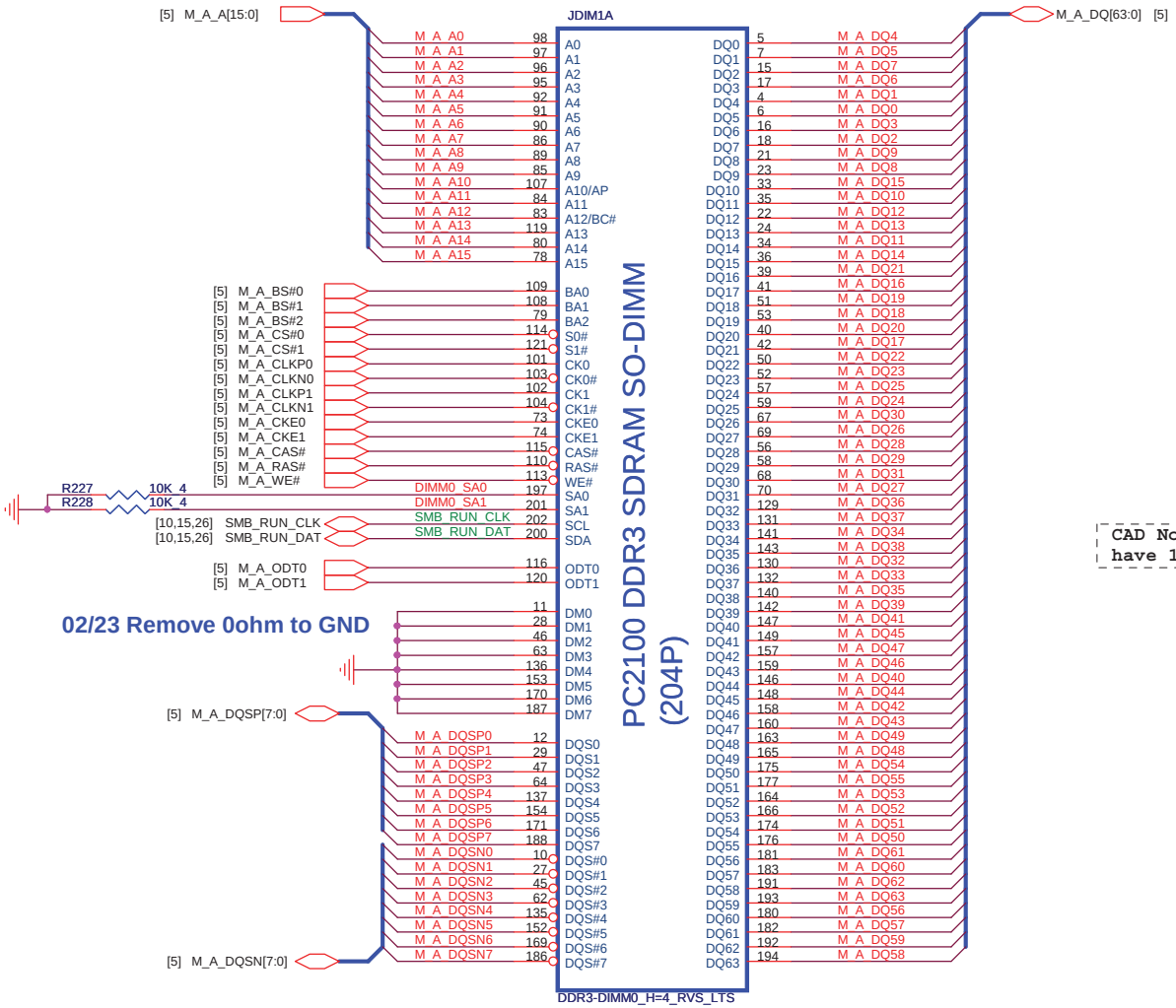
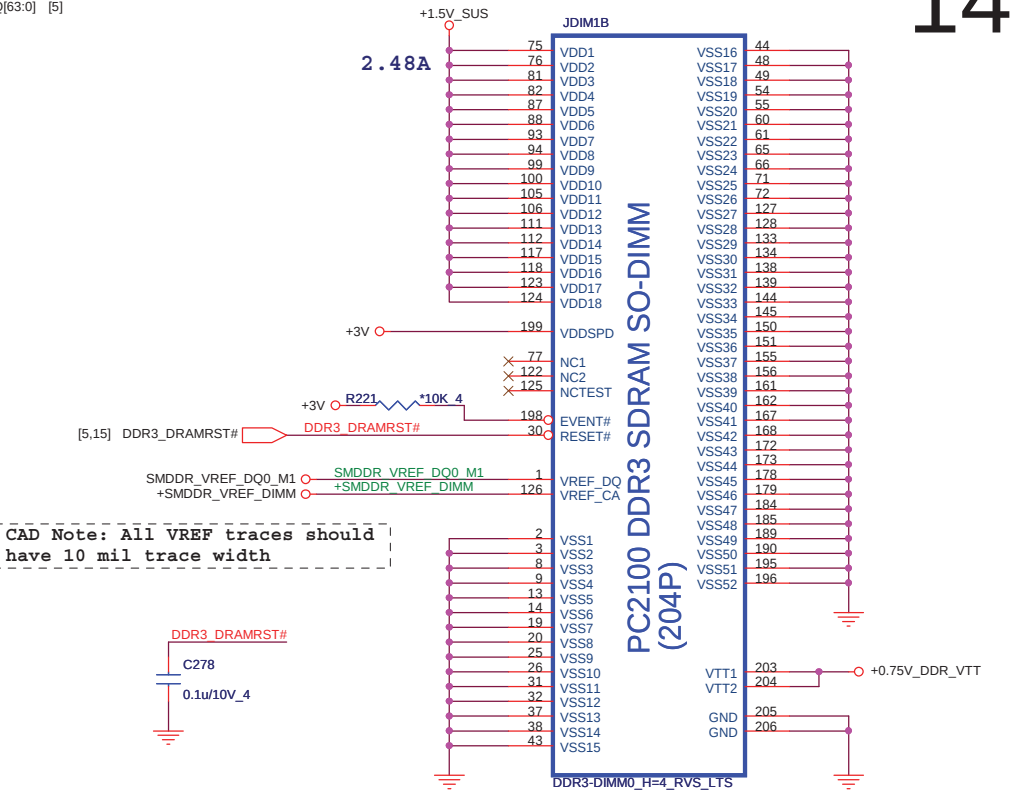
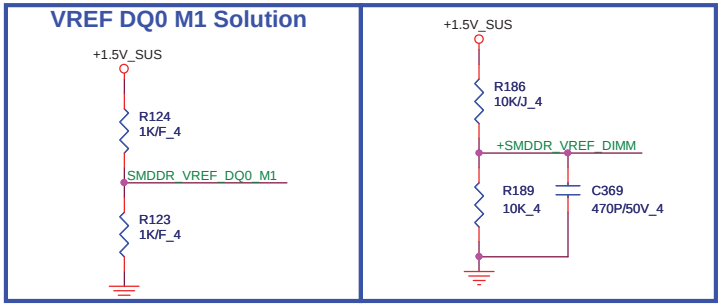
DDR_STD(DDR)



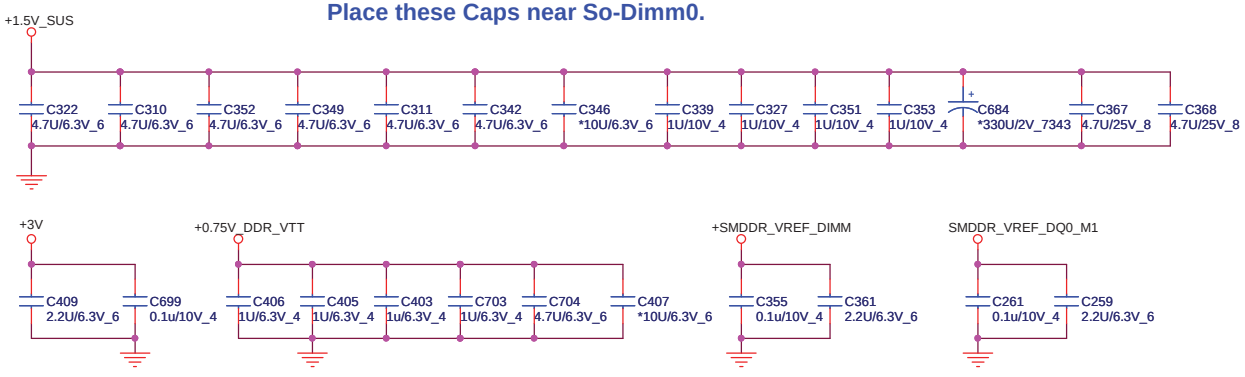
02/23 Remove 0ohm to GND



VREF DQ0 M1 Solution



Place these Caps near So-Dimm0.



Quanta Computer Inc.

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	DDRIII SO-DIMM-0	1A
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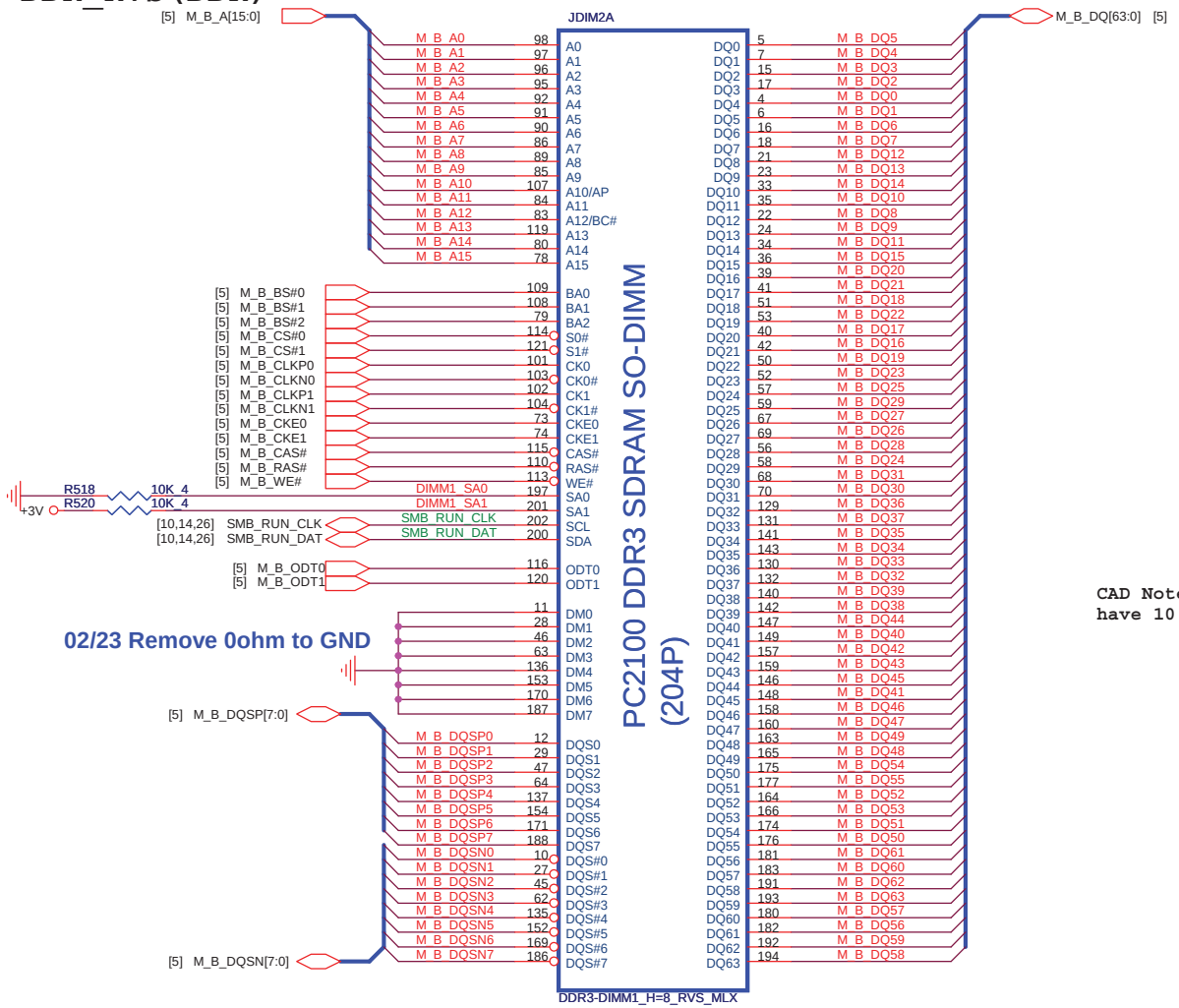
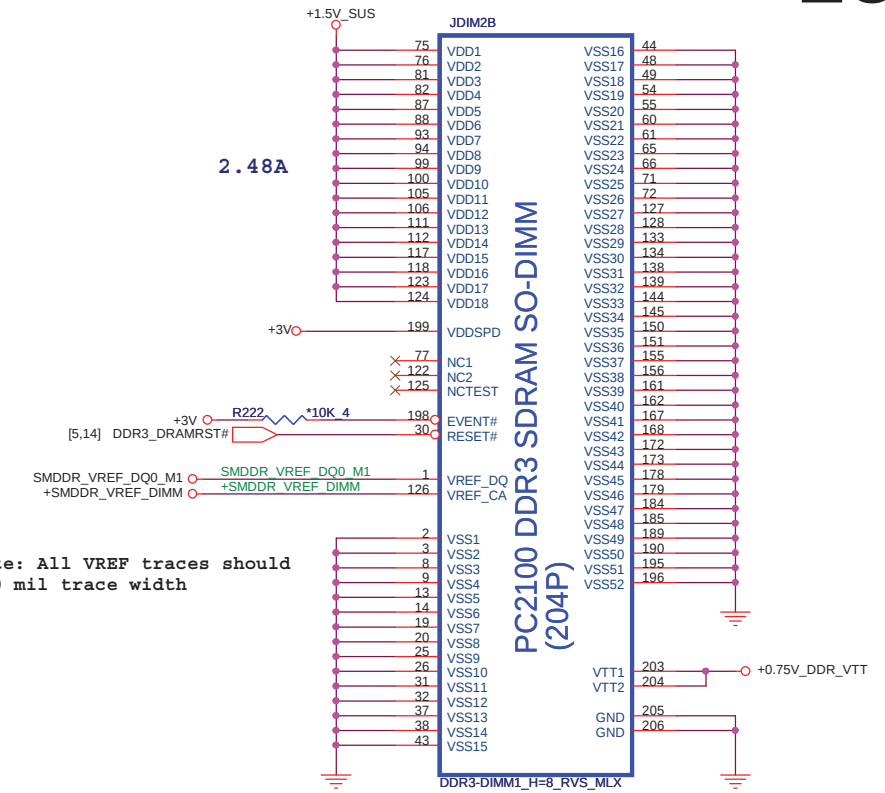
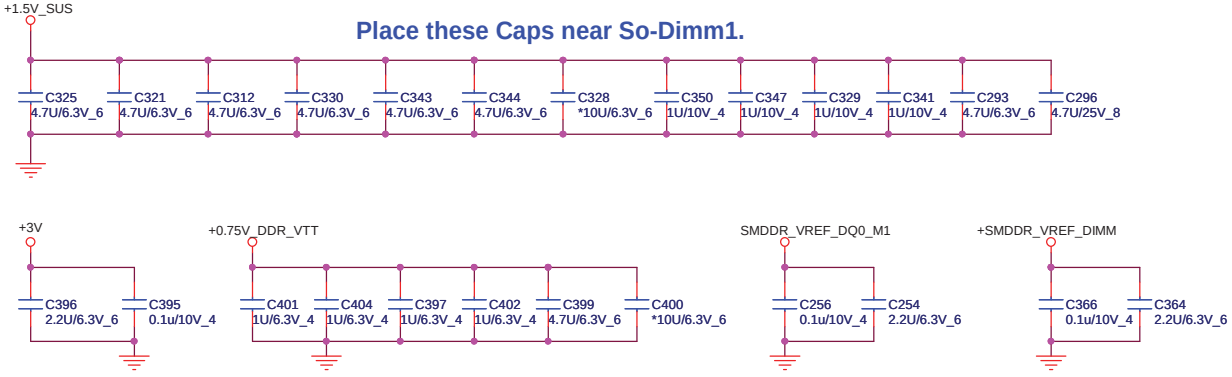
DDR_RVS (DDR)





CAD Note: All VREF traces should have 10 mil trace width

Place these Caps near So-Dimm1.



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 8H type:DDR-C-2013310-204p-1

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	DDRIII SO-DIMM-1	1A

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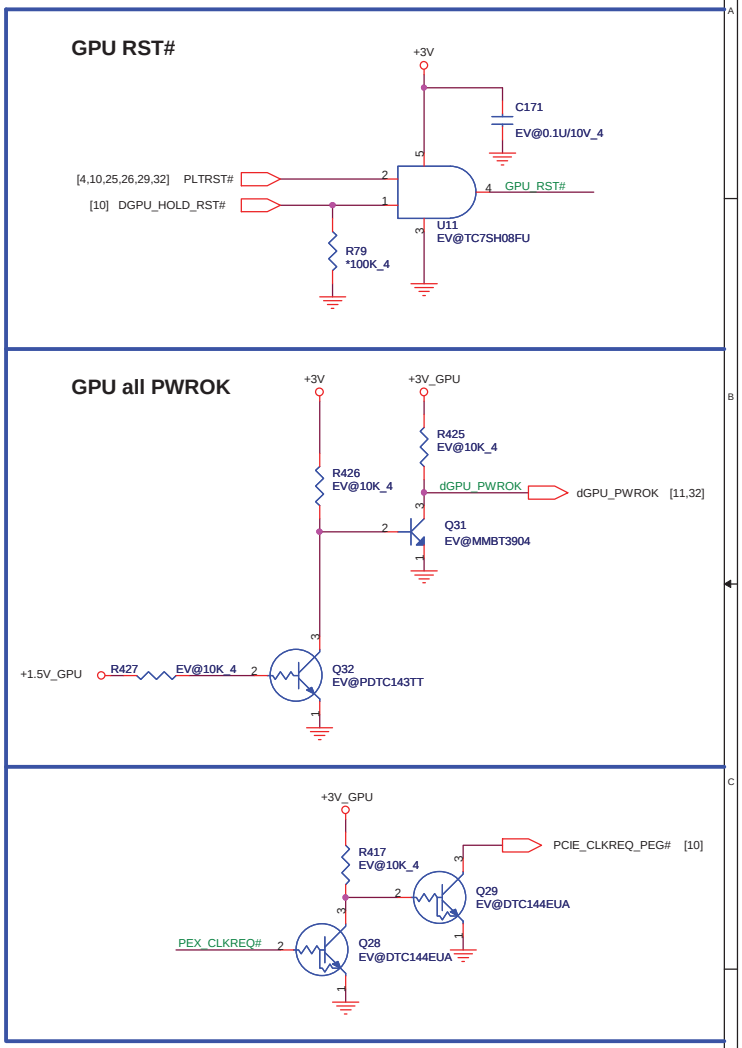
PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A



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GPU1B

MEMORY I/F A

SP@U_GPU_GB1_128

GPU1C

MEMORY I/F C

SP@U_GPU_GB1_128

5500mA

100mA

POP For Debug only
Place close to ball

30-ohm ESR=0.01-ohm

EV@BLM18AG331SN1D

Check

PLACE NEAR BGA

PLACE NEAR BALLS

Near PQ7

Quanta Computer Inc.
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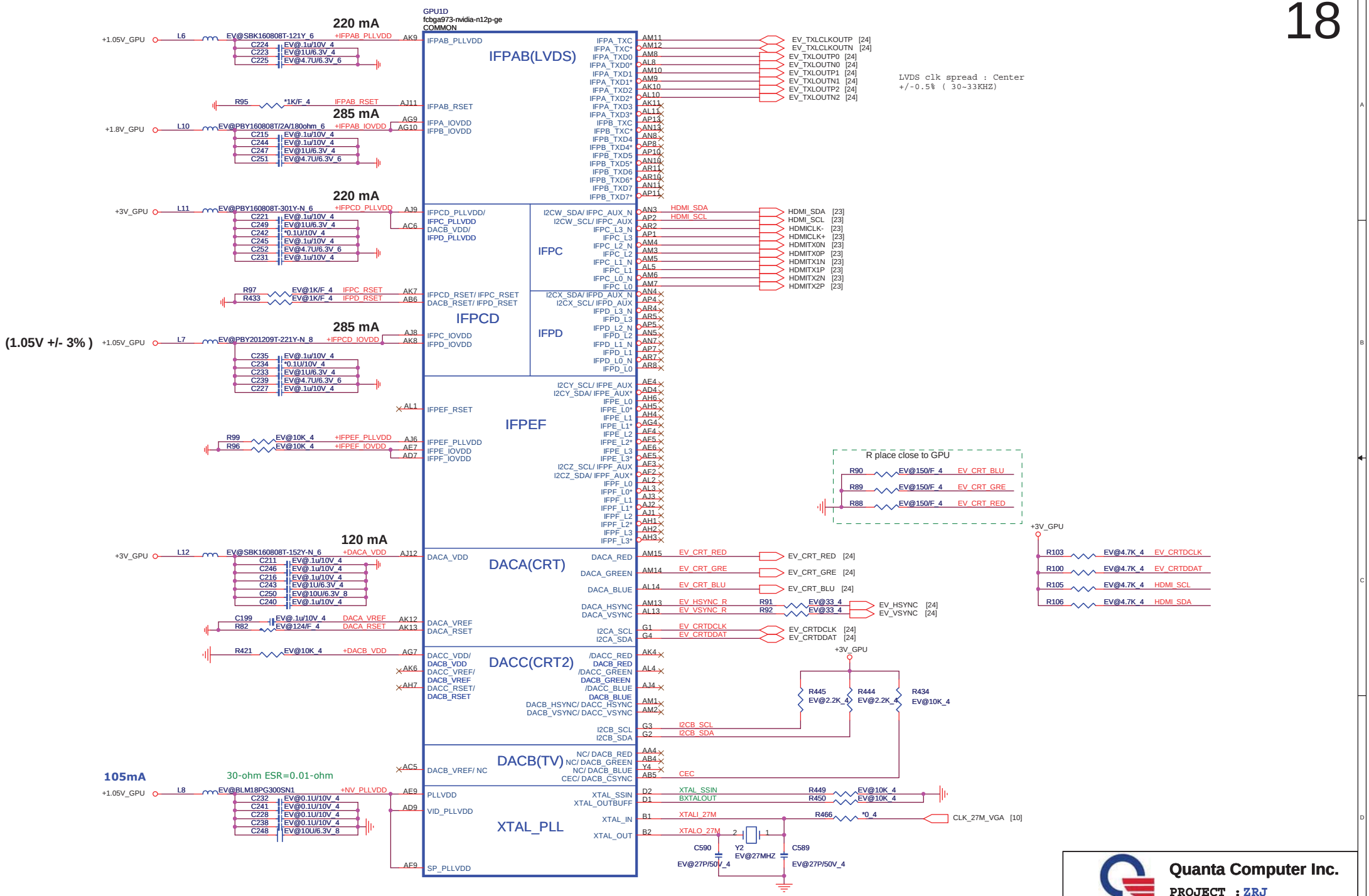
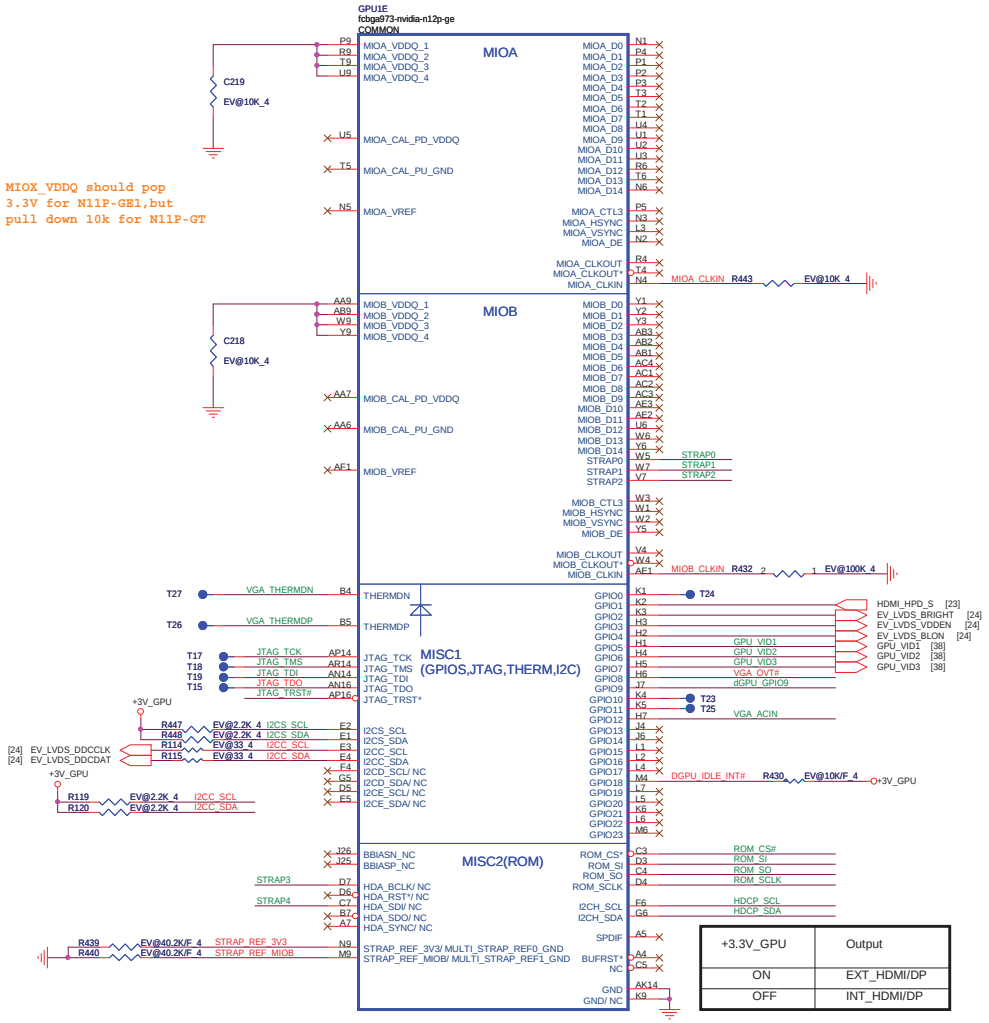
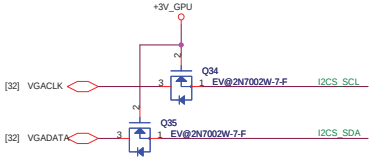
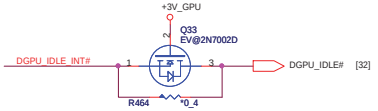
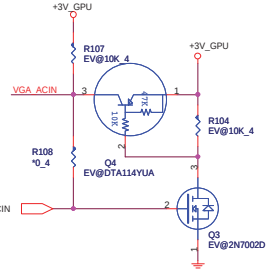
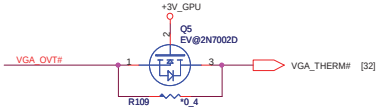

GPU1D
fcbga973-nvidia-n12p-ge
COMMON
IFPAB(LVDS)
IFPCD
IFPC
IFPD
IFPEF
DACA(CRT)
DACC(CRT2)
DACB(TV)
XTAL_PLL
220 mA
285 mA
220 mA
285 mA
120 mA
105mA
(1.05V +/- 3%)
30-ohm ESR=0.01-ohm
LVDS clk spread : Center
+/-0.5% (30~33KHZ)
R place close to GPU
Quanta Computer Inc.
PROJECT : ZRJ
N12P-GE (DISPLAY) 3/5
Saturday, January 22, 2011











	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	N12P-GS	N12P-GV
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001	1001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	1010	1000
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	xxxx	xxxx
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0100	0000
STRAP3	SOR_EXPOSED[3]	SOR_EXPOSED[2]	SOR_EXPOSED[1]	SOR_EXPOSED[0]	TBD	xxxx
STRAP4	Reserve	Reserve	PCI_MAX_SPEED	DP_PLL_VDD3	TBD	0001

	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

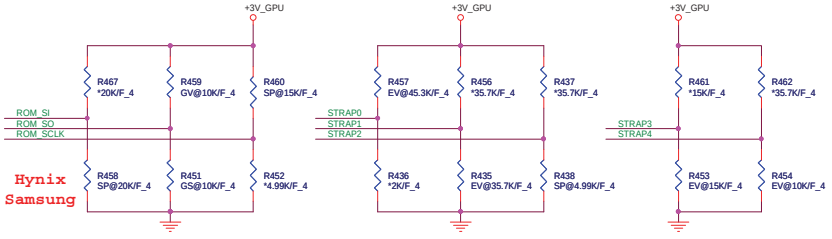
VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
* 0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHT500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW01	AKD5LZWTW00	H5TQ1G63BFR-11C
0x6(0110)	800MHz 1GB(128M*16) Hynix	AKD5MGGTW00	AKD5MGGTW01	H5TQ2G63BFR-12C
0x7(0111)	800MHz 1GB(128M*16) Samsung	AKD5MGGT501	AKD5MGGT502	K4W2G1646B-HC12

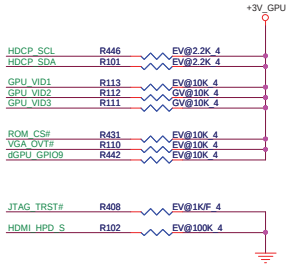
```
4.99K/F_4 ==> CS24992FB26
10K/F_4 ==> CS31002FB26
15K/F_4 ==> CS31502FB24
20K/F_4 ==> CS32002FB29
30.1K/F_4 ==> CS33012FB18
35.7K/F_4 ==> CS33572FB13
45.3K/F_4 ==> CS34532FB18
```

	Register value
ROM_SO	N12P-GS 10k pull down; N12P-GV 10K pull up.
ROM_SCLK	N12P-GS need 15K pull up; N12P-GV need 5K pull up
ROM_SI	1G: Hynix =15K pull down ,Samsung =20k pull down 2G: Hynix =35K pull down ,Samsung =45k pull down
STRAP0	N12P-GS and N12P-GV both 45K pull high
STRAP1	N12P-GS and N12P-GV both 35k pull down
STRAP2	N12P-GS need 25K pull down; N12P-GV need 5K pull down
STRAP3	STRAP3 need 15K pull down by R3513.
STRAP4	STRAP4 need 10K pull down by R3519.

ROM_SI Strap Bit for RAM Mapping

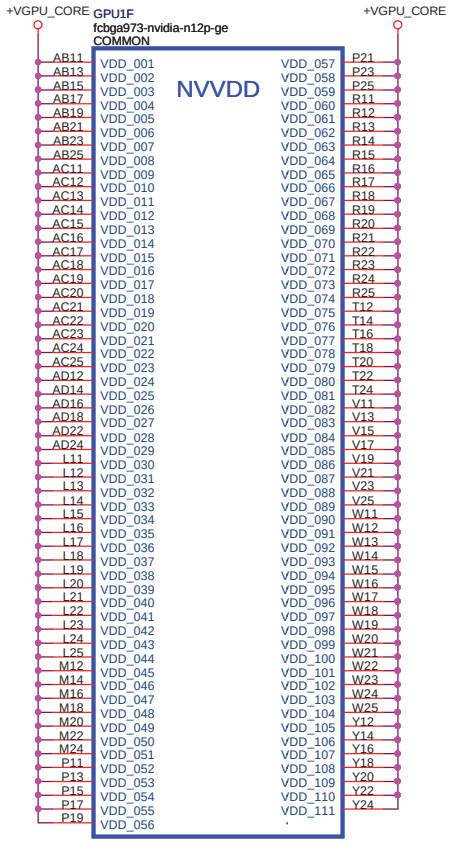


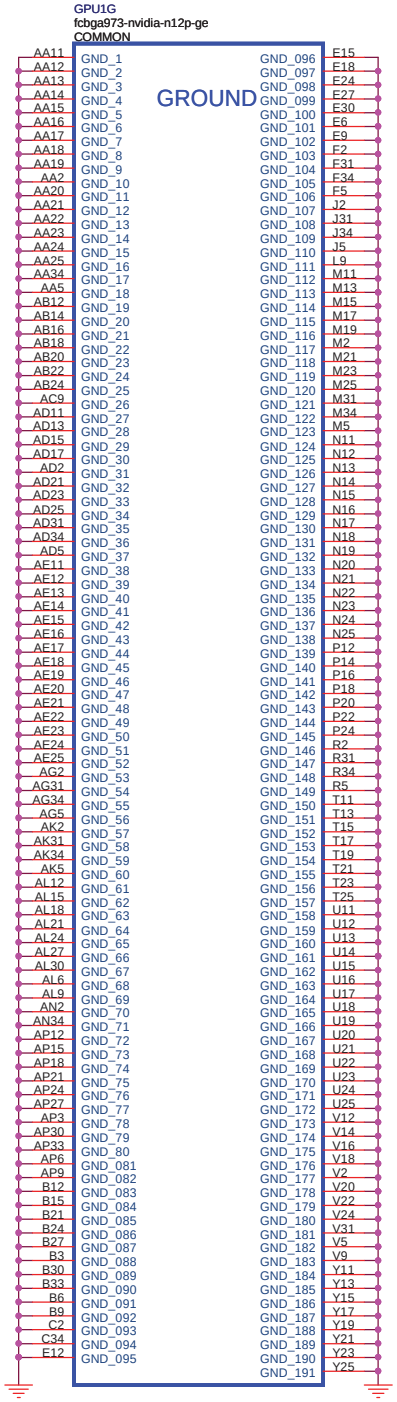
N11P-GE1 DevID is 0x0DFE, so pull up
ROM_SCLK with 15Kohm and STRAP2
pull up 35Kohm

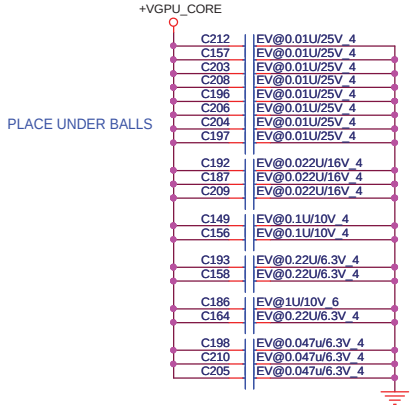


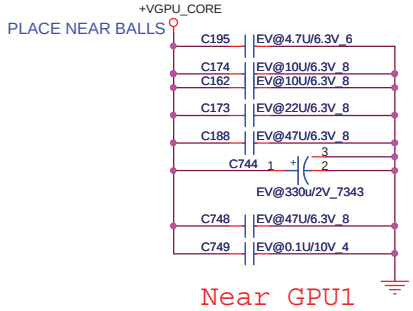
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	N/A	
3	OUT	N/A	
4	OUT	N/A	
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL









Quanta Computer Inc.

PROJECT : ZRJ

Size	Document Number	Rev
	N12P-GE(POWER&THM)5/5	1A

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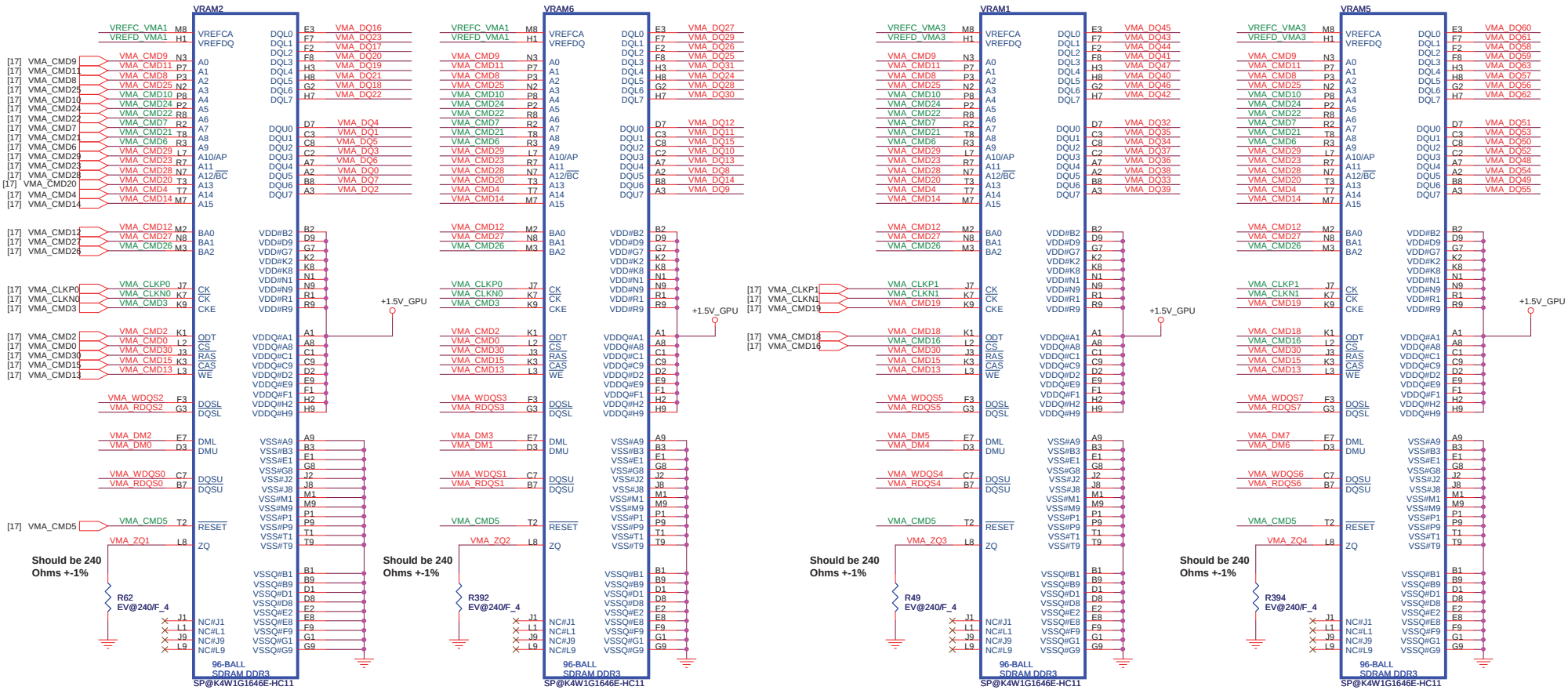
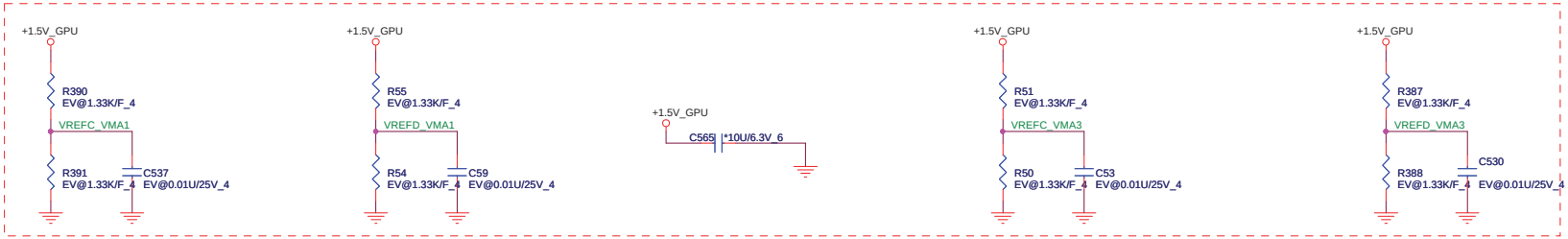
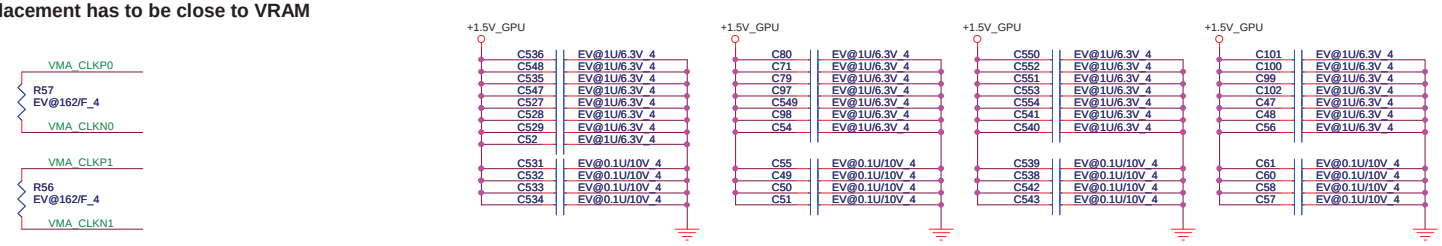
CHANNEL A: 512MB/1024MB DDR3

[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]





Placement has to be close to VRAM



Quanta Computer Inc.

PROJECT : ZRJ

Size	Document Number	Rev
	N12P-GE VRAM-1	1A

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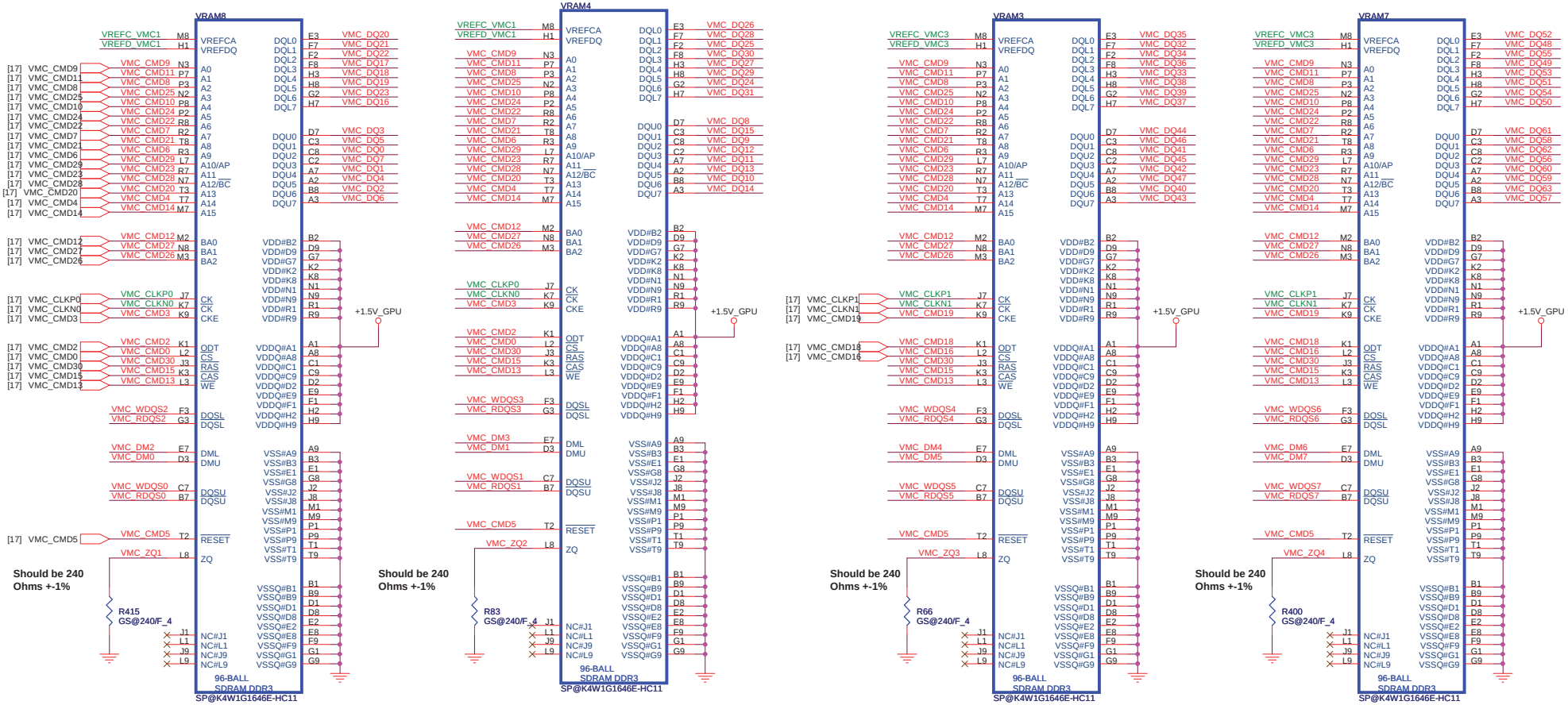
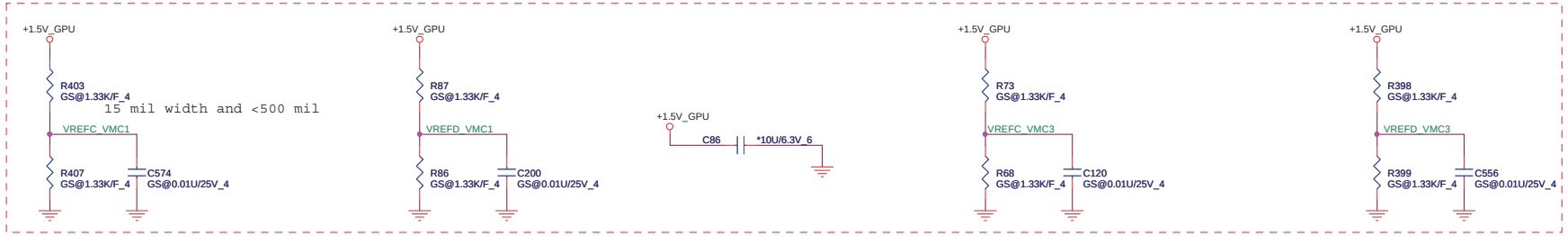
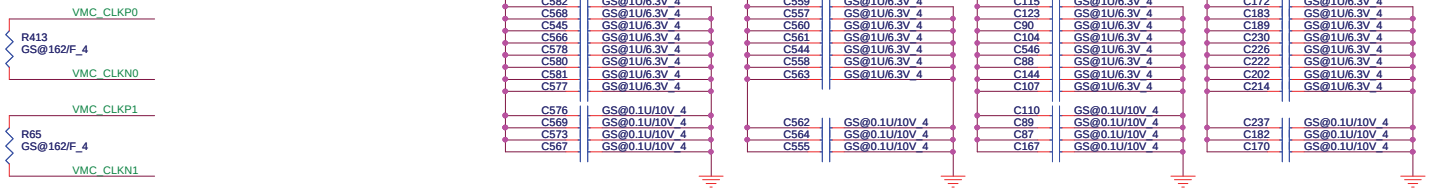
CHANNEL B: 512MB/1024MB DDR3

[17] VMC_DQ[63..0]
[17] VMC_DM[7..0]
[17] VMC_WDQS[7..0]
[17] VMC_RDQS[7..0]





Placement has to be close to VRAM



Quanta Computer Inc.
PROJECT : ZRJ

Size	Document Number	Rev
	N12P-GE VRAM-2	1A

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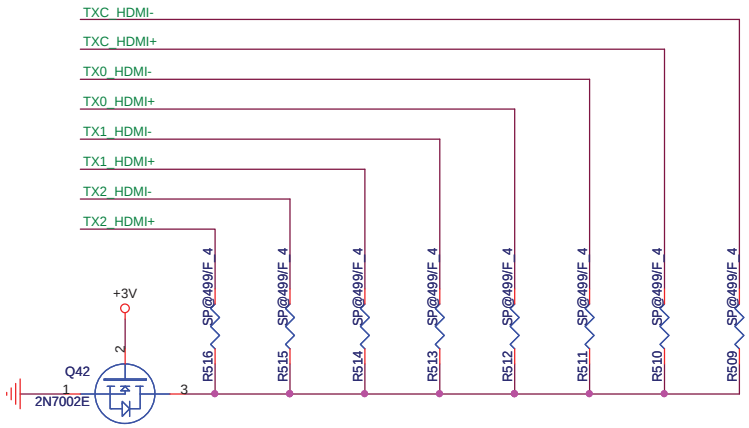
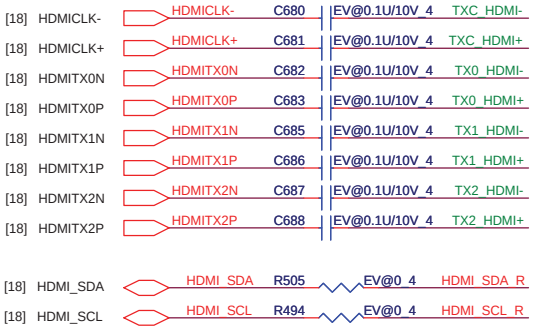


	EV@	IV@
SP@	500 ohm	680 ohm

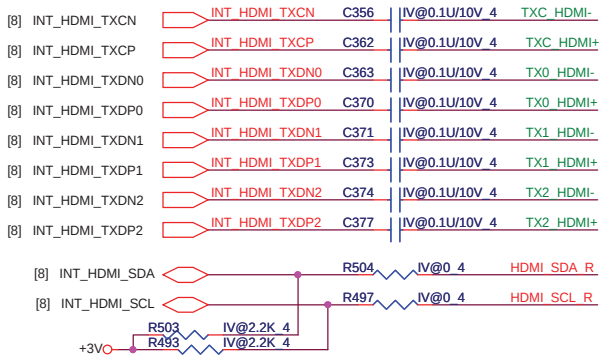
PLACE PULL DOWN RESISTORS CLOSE TO DIFFERENTIAL PAIRS CONNECTED TO SOLID GROUND FLOOD WHICH IS CONTROLLED BY THE FET
AVOID STUBS TO ALL DIFFERENTIAL TRACES

EXT-HDMI

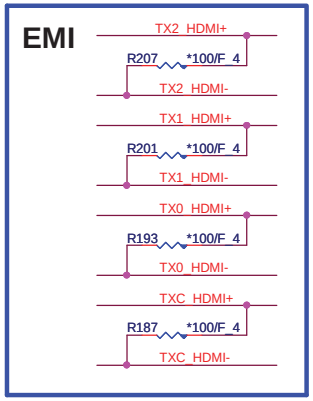


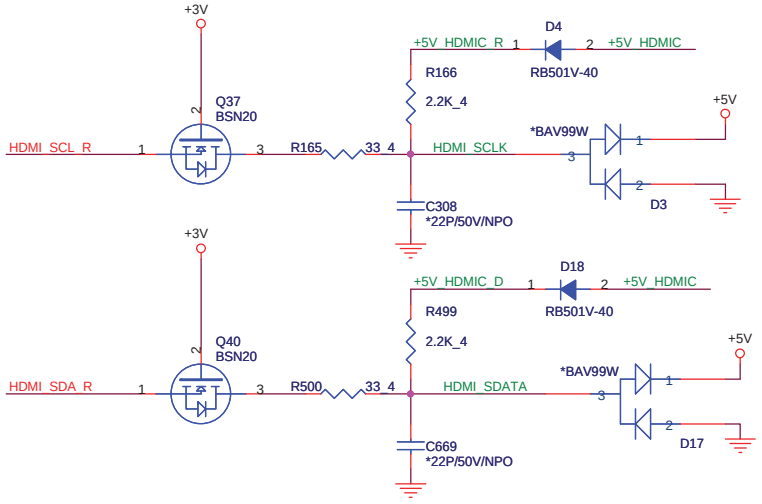
INT-HDMI

PLACE AC CAP CLOSE TO CONNECTOR



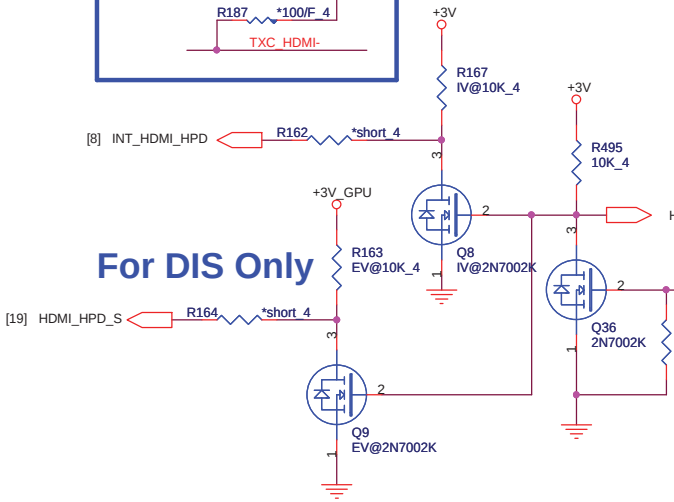
EMI



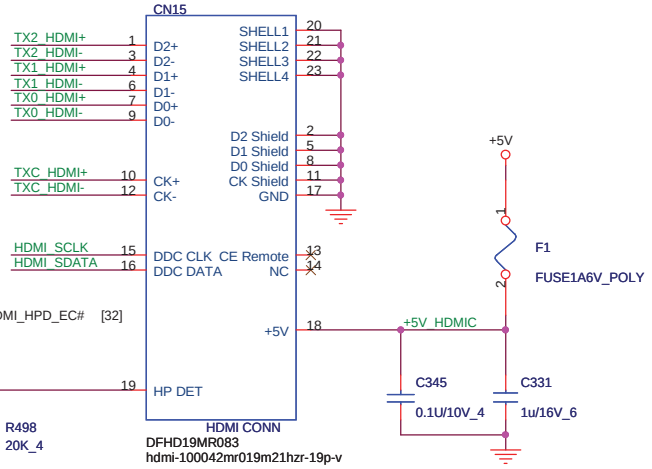


For UMA / Optimus HDMI function

For DIS Only



HDMI CONN



Quanta Computer Inc.
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Size	Document Number	Rev
	CRT CONN/HDMI	1A
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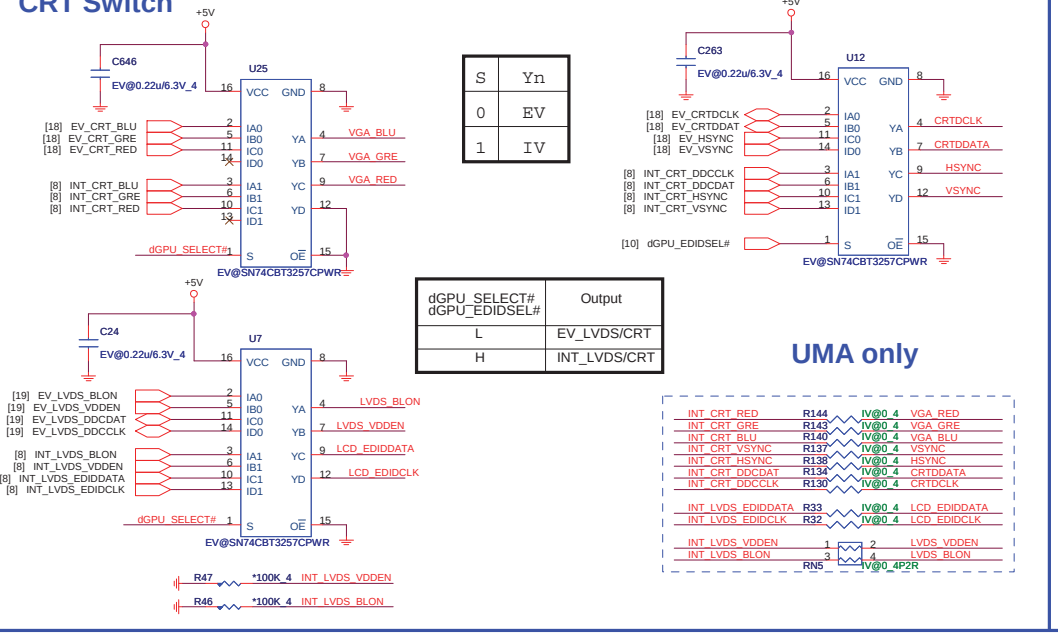
CRT Switch

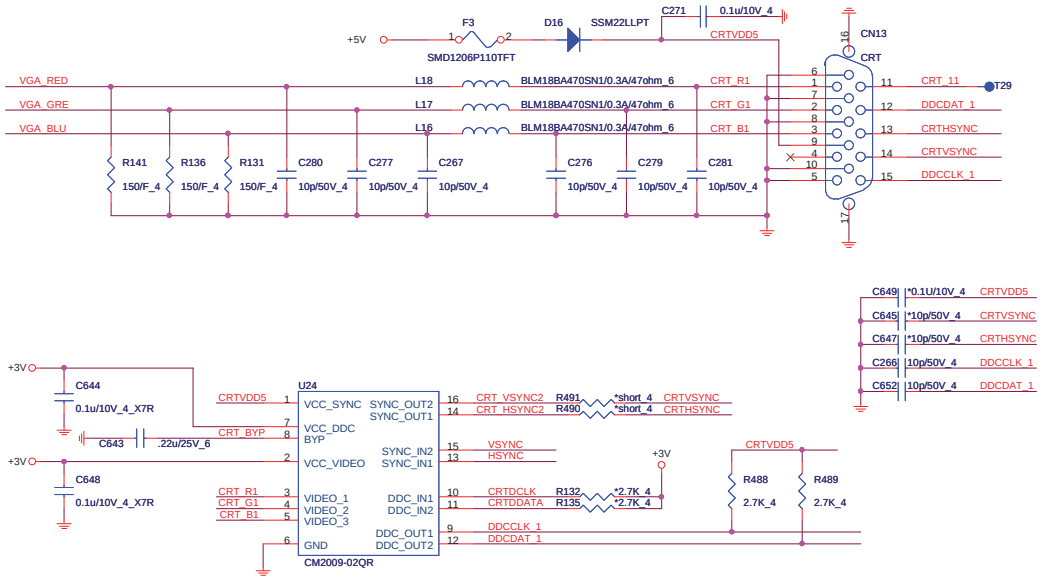


S	Yn
0	EV
1	IV

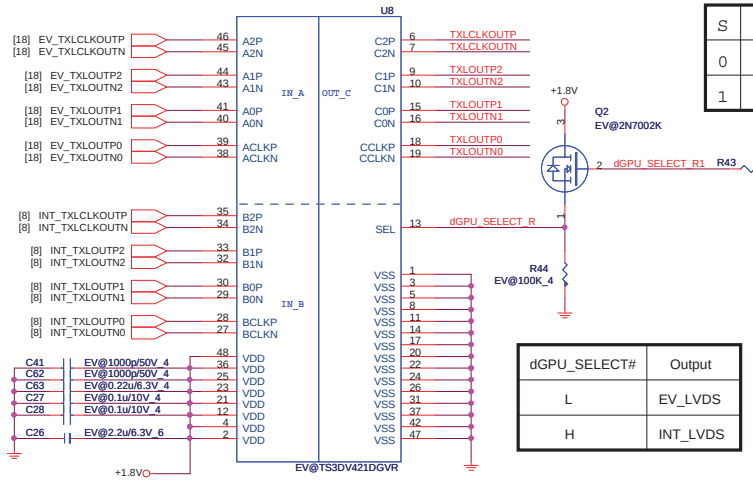
dGPU_SELECT# dGPU_EDIDSEL#	Output
L	EV_LVDS/CRT
H	INT_LVDS/CRT

UMA only

CRT



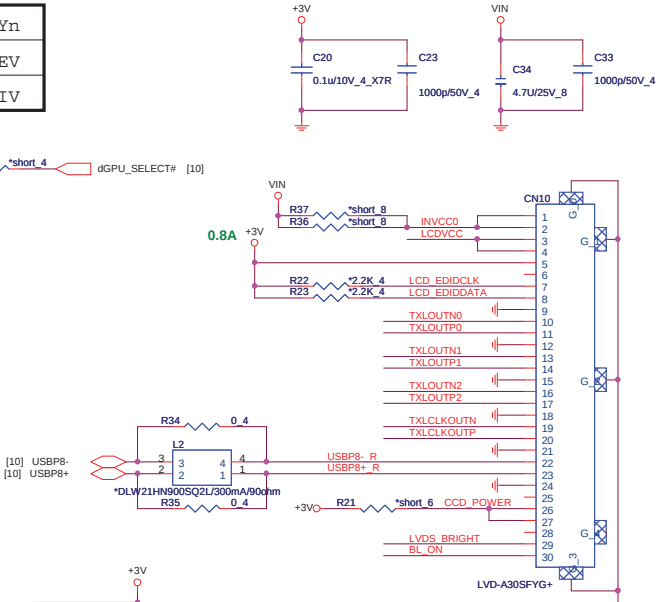
LVDS Switch



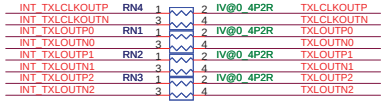
S	Yn
0	EV
1	IV

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

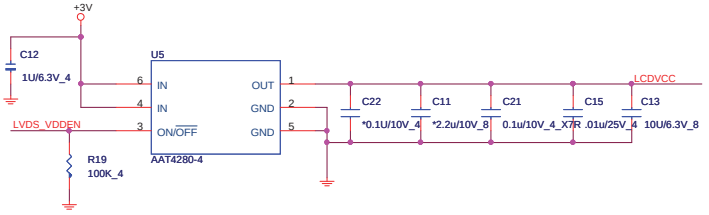
LVDS



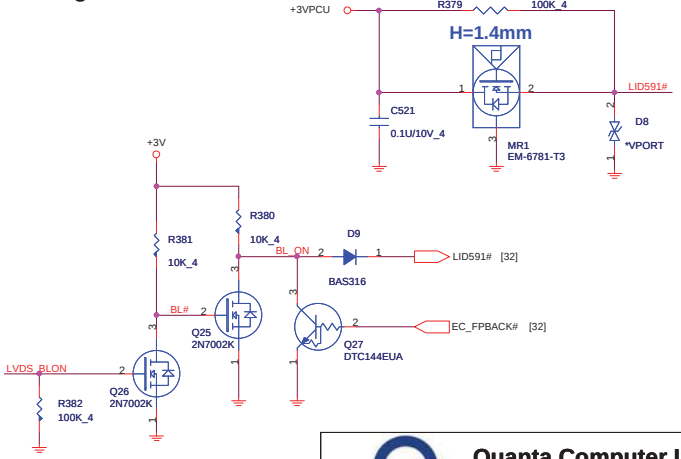
UMA only



LCD Power



Backlight Control



Quanta Computer Inc.			
PROJECT : ZRJ			
Size	Document Number	CRT/LVDS/CCD/HALL	Rev 1A
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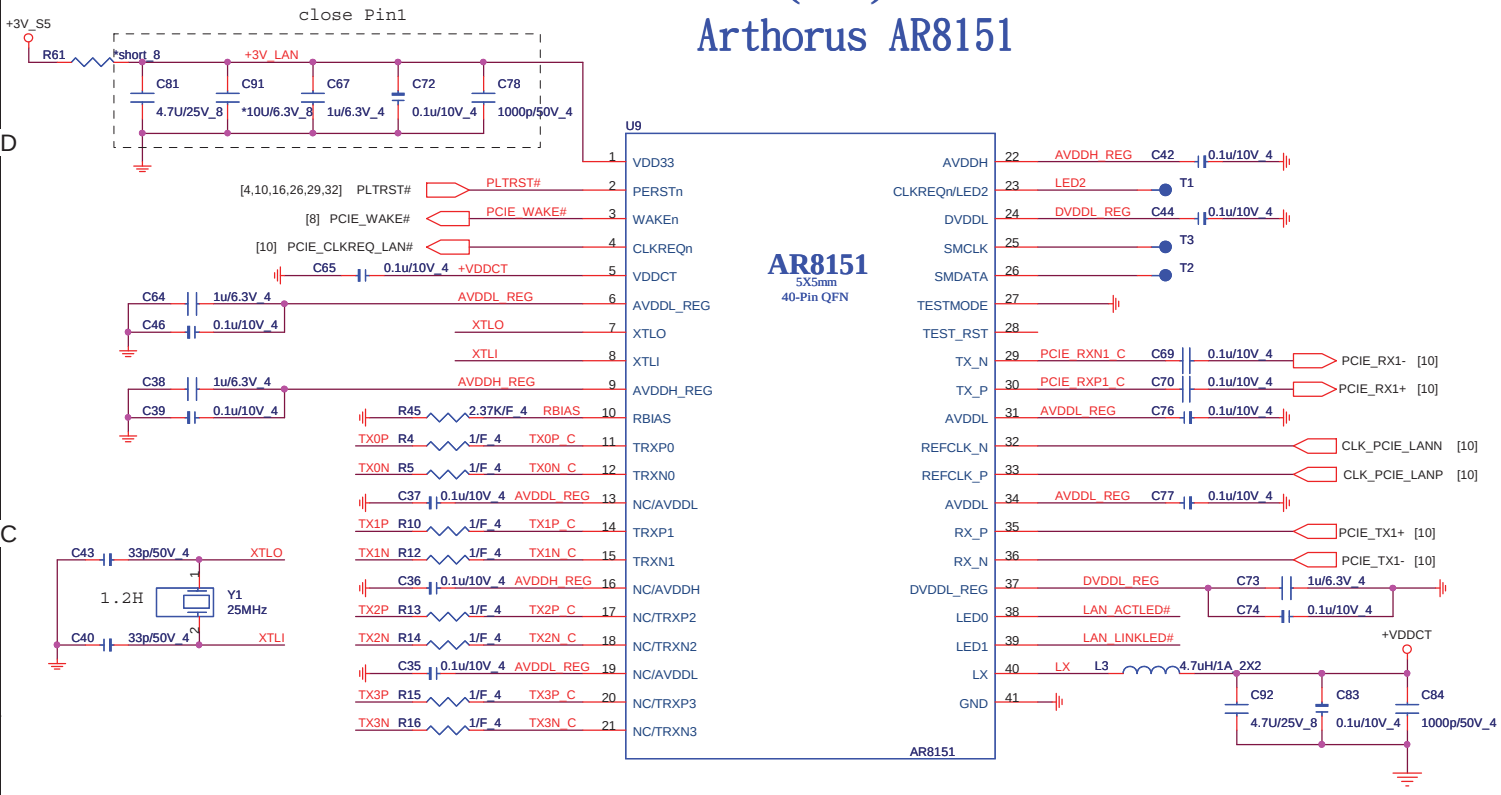
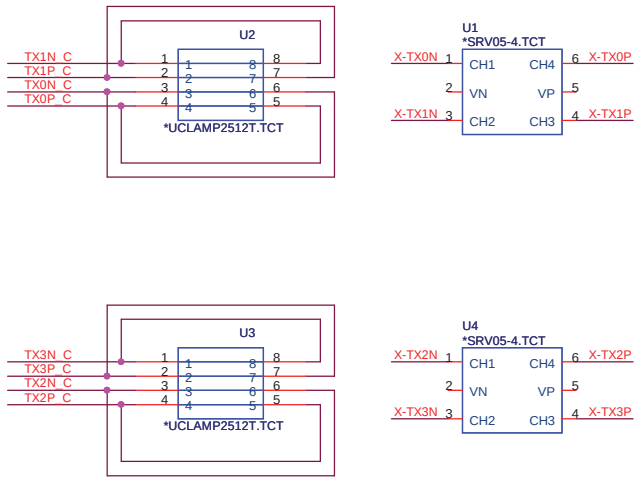
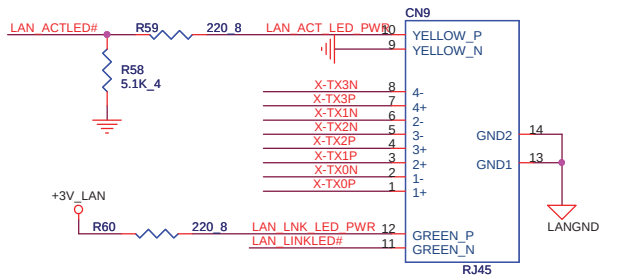
LAN (LAN)
Arthorus AR8151

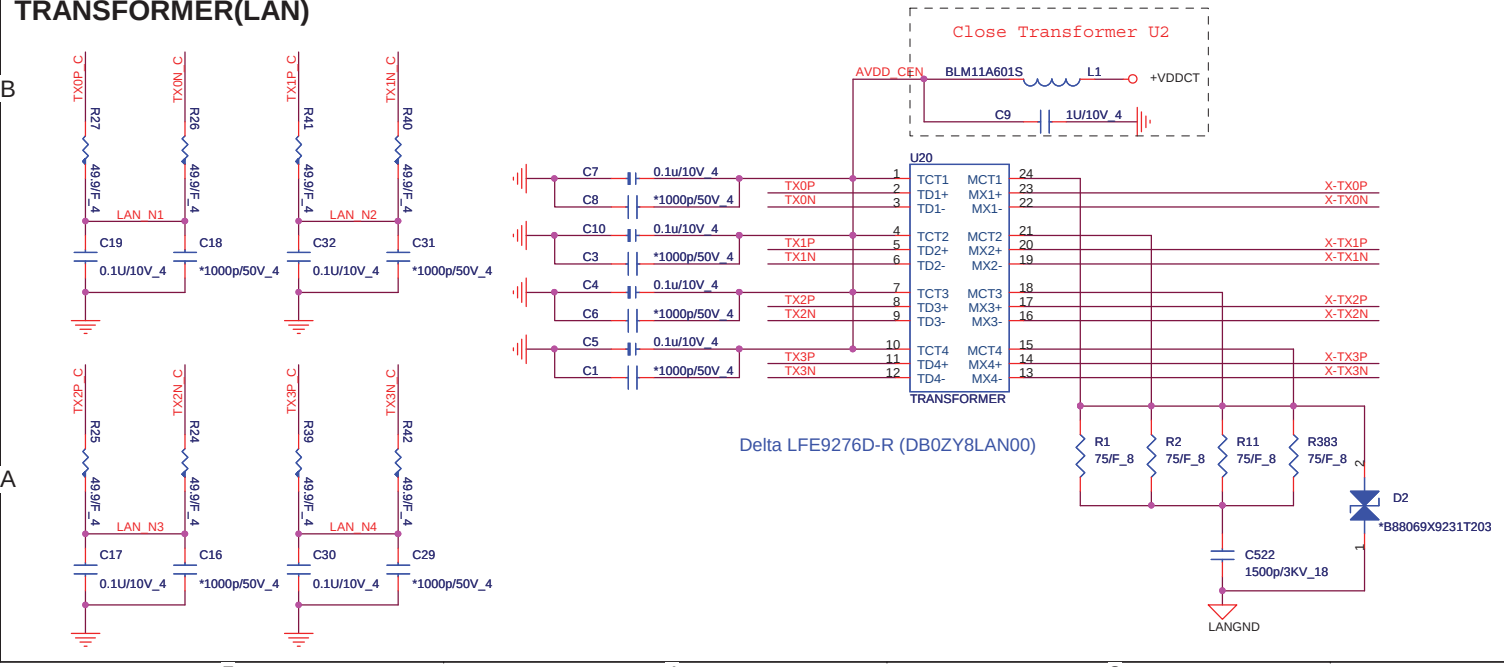


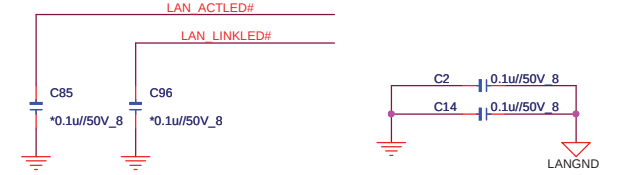


RJ45(LAN)



TRANSFORMER(LAN)





Quanta Computer Inc.		
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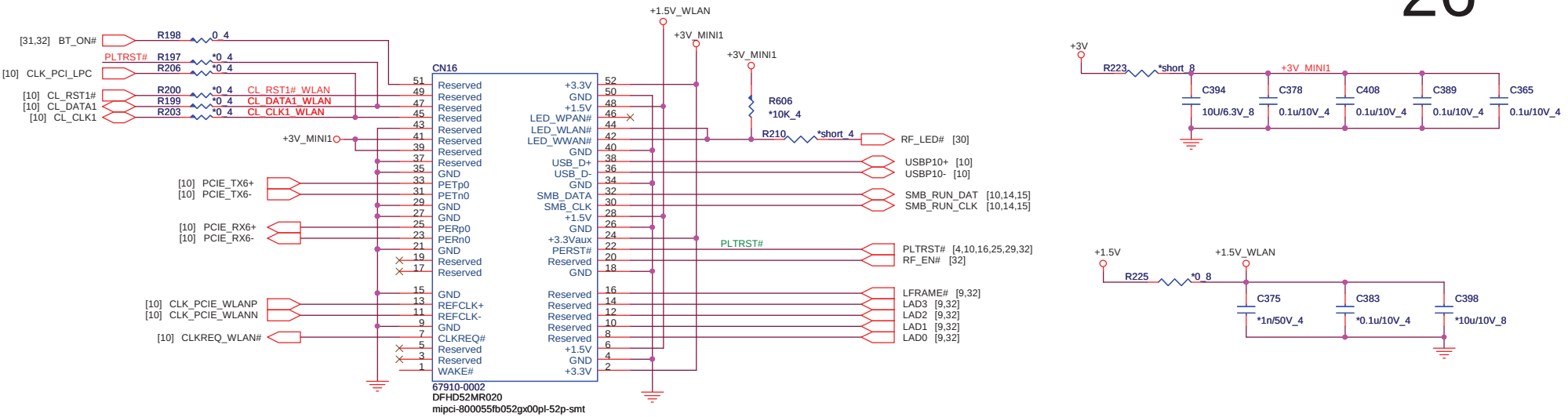
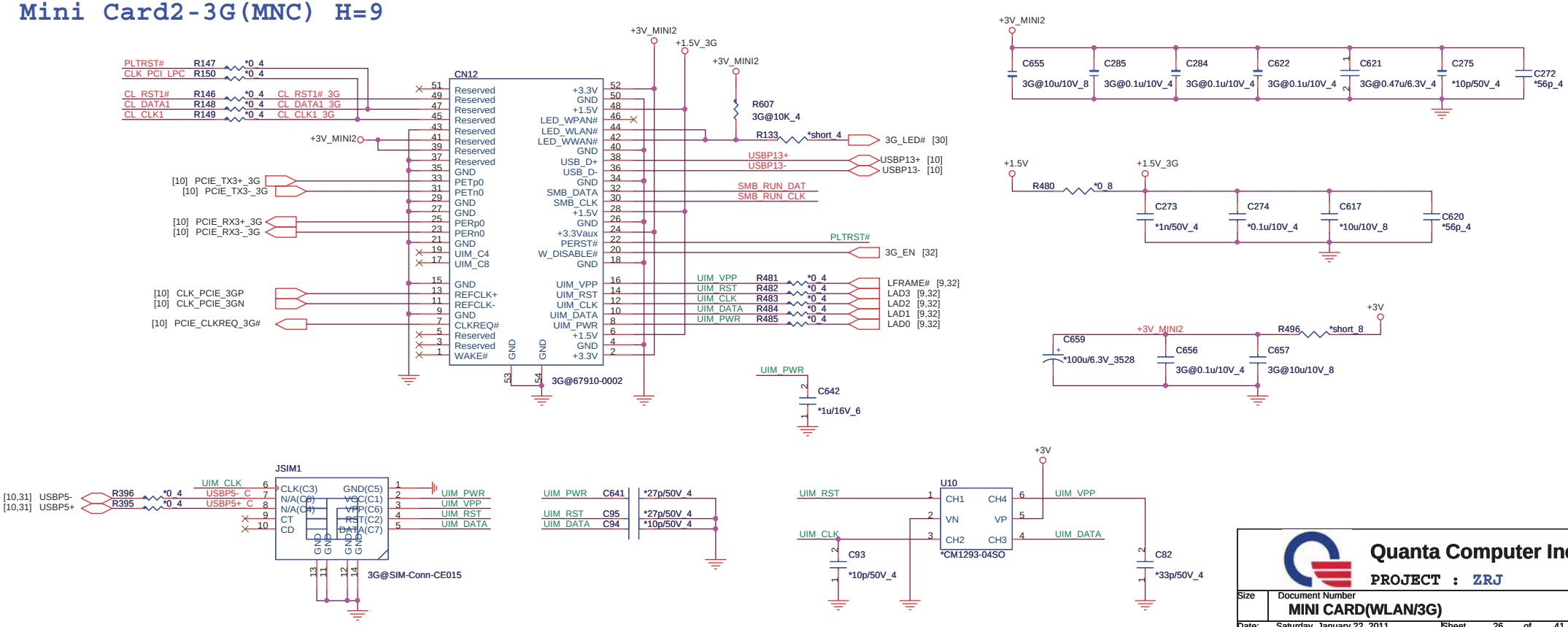
MINI CARD (WLAN) H=7



Mini Card2-3G(MNC) H=9



Quanta Computer Inc.

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Size	Document Number	Rev
	MINI CARD(WLAN/3G)	1A
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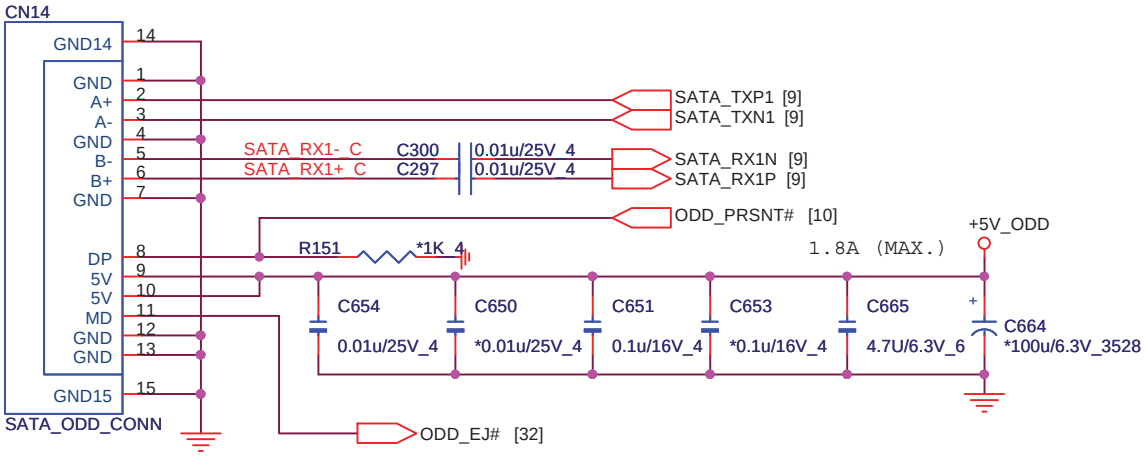
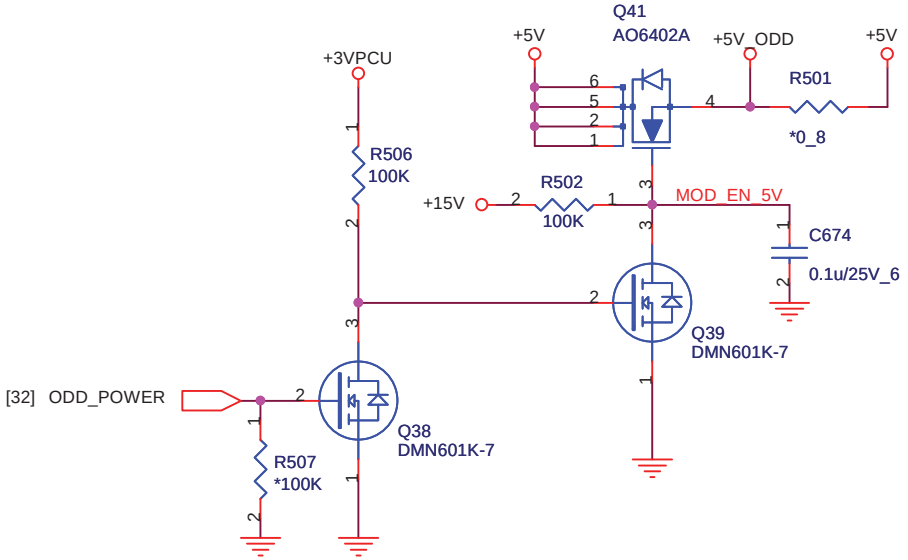
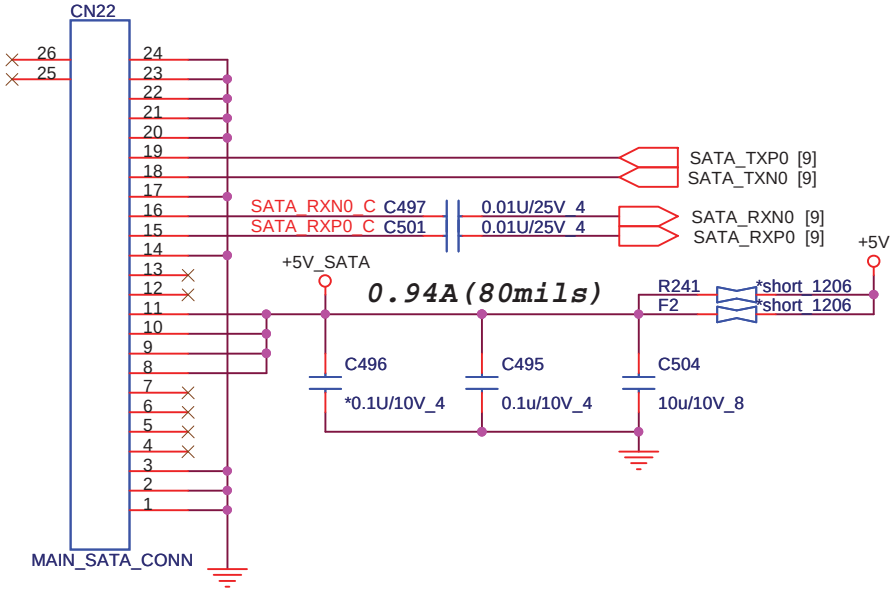
ODD (SATA)

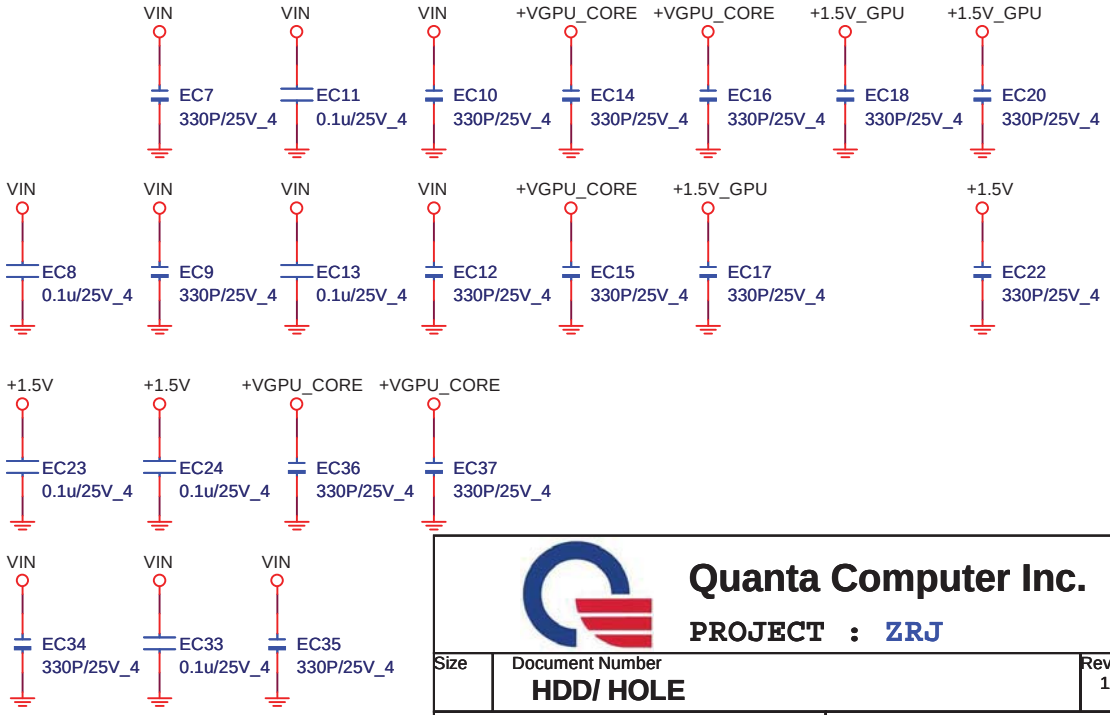


ODD Power (SATA)



2.5" SATA HDD





Quanta Computer Inc.

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Size	Document Number	Rev
	HDD/ HOLE	1A
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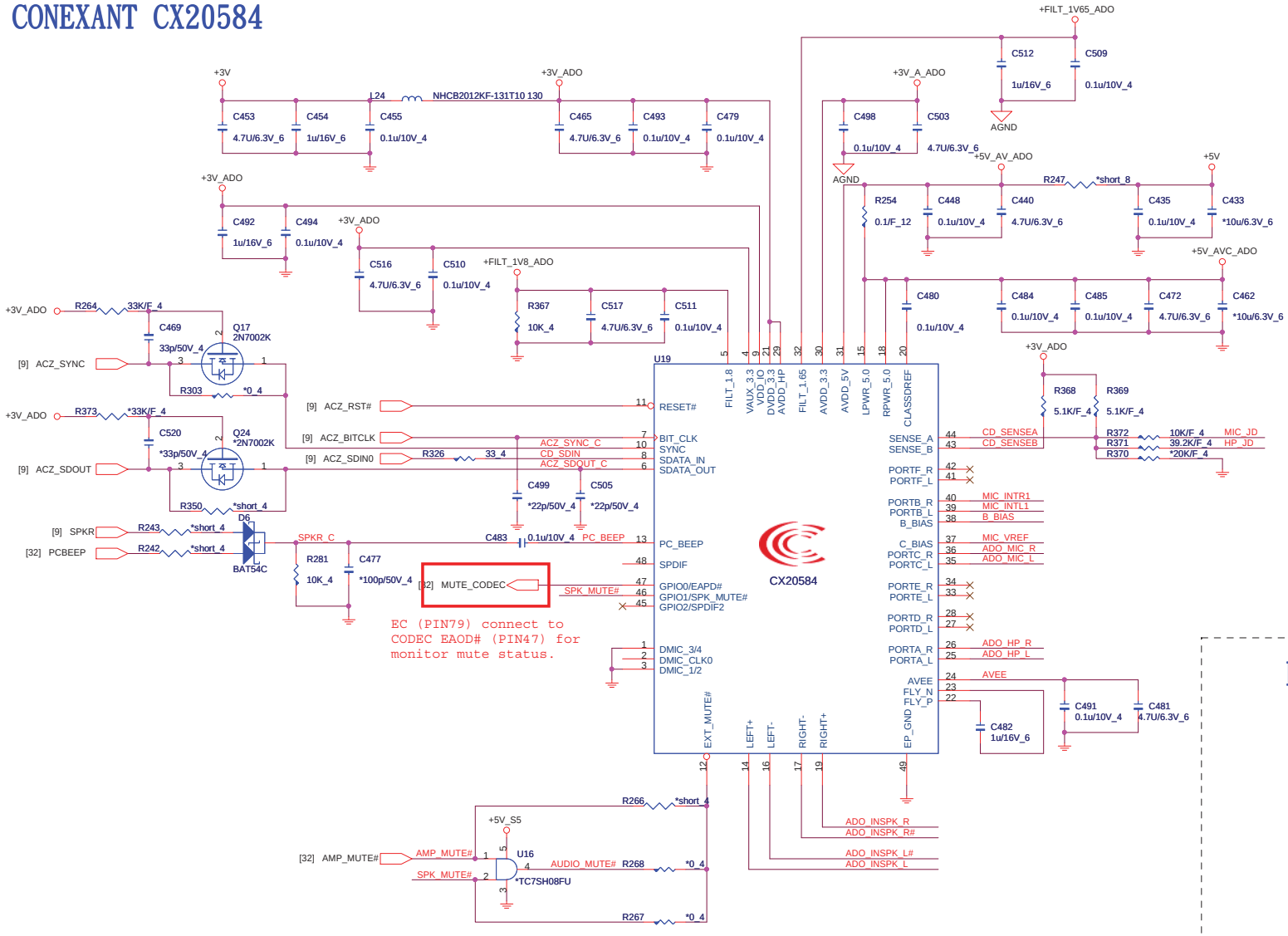
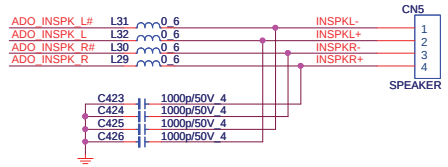
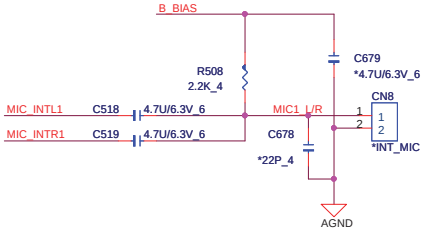
CODEC (ADO)
CONEXANT CX20584



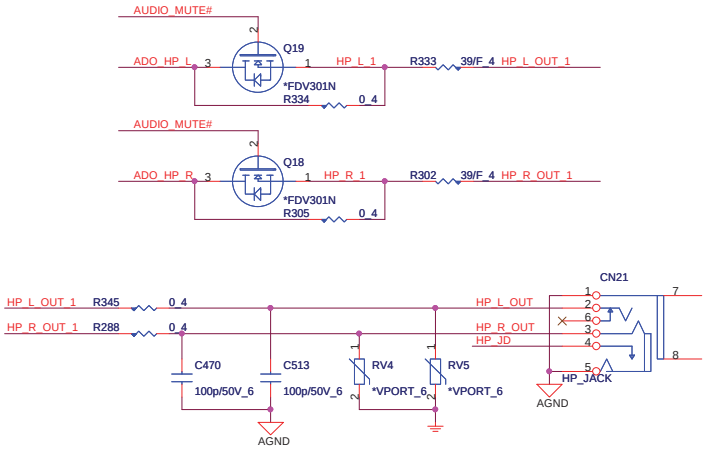
Speaker



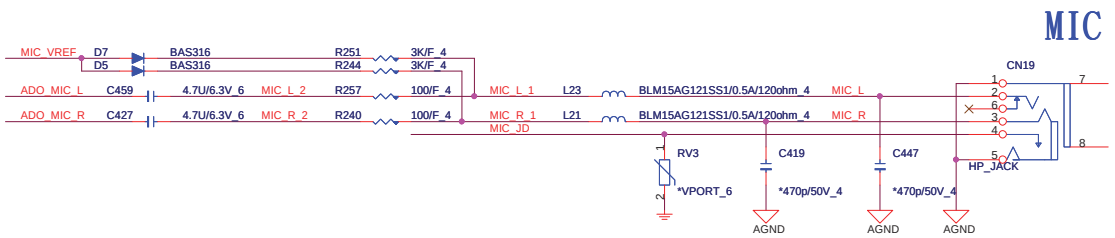
INT MIC



HP/SPDIF



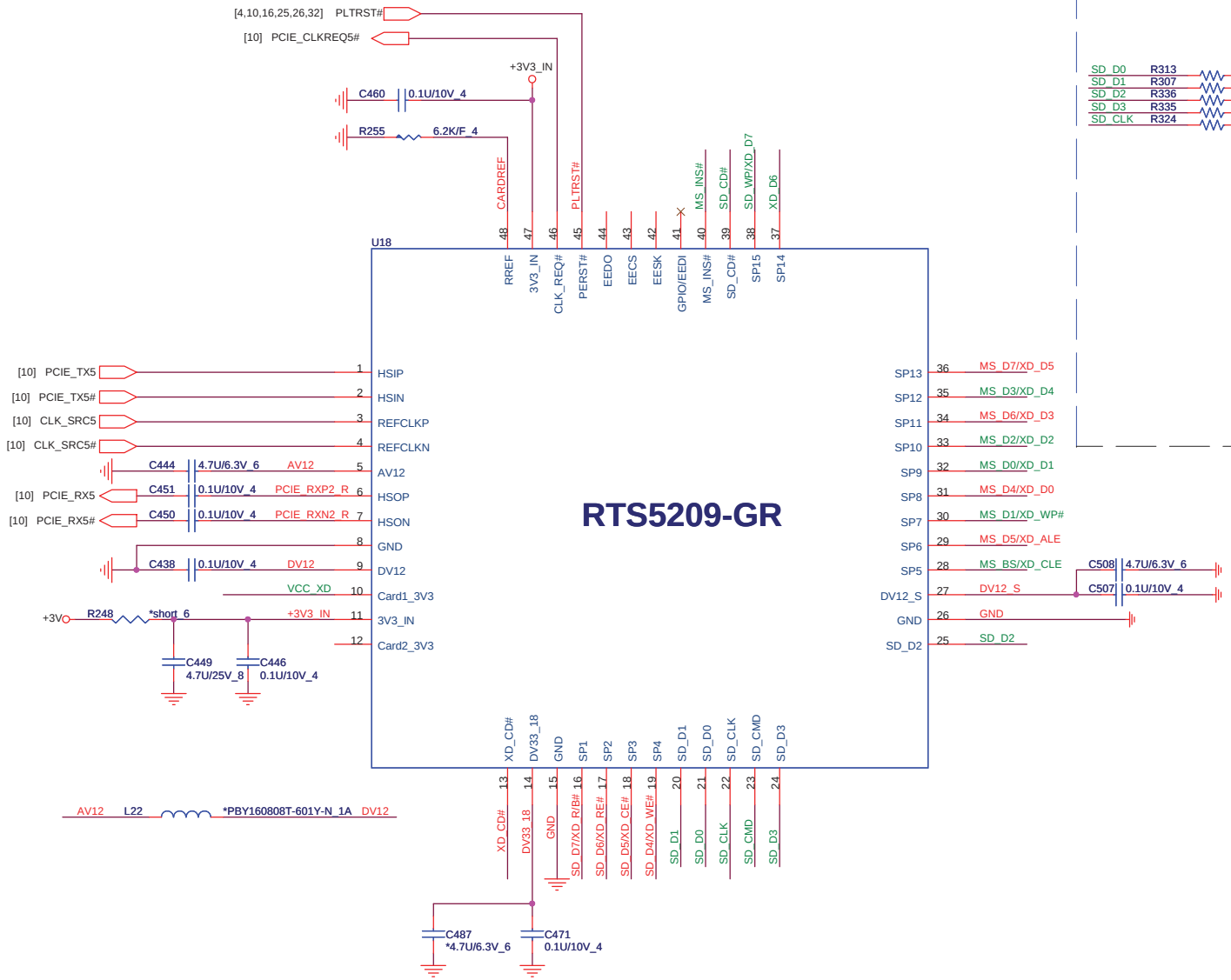
MIC



Quanta Computer Inc.		
PROJECT : ZRJ		
Size	Document Number: CODEC CX20584	Rev: 1A
Date: Saturday, January 22, 2011	Sheet 28 of 41	

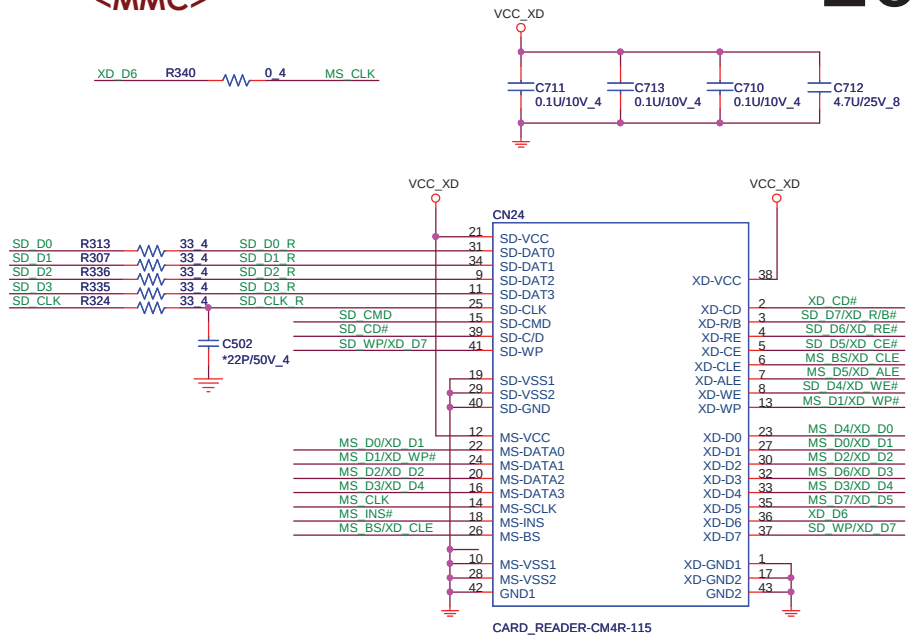
Card reader controller

<MMC>



5 IN 1 Card reader CONN

<MMC>



Quanta Computer Inc.

PROJECT : ZRJ

Size	Document Number	Rev
	RTS5209 (Card Reader)	3G
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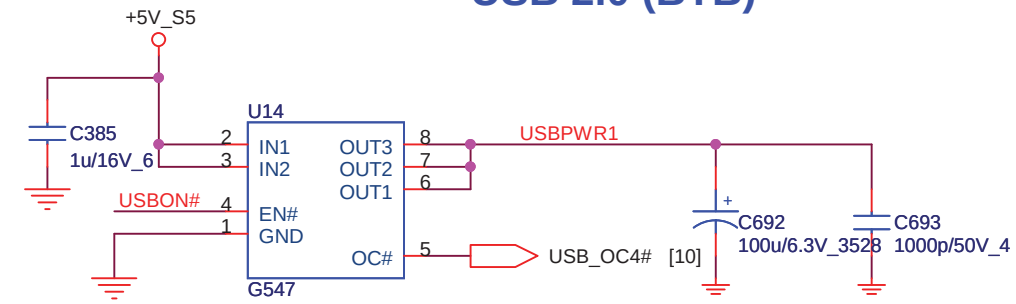
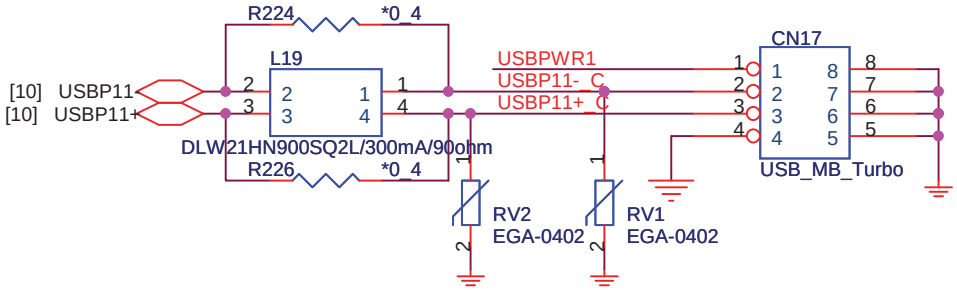
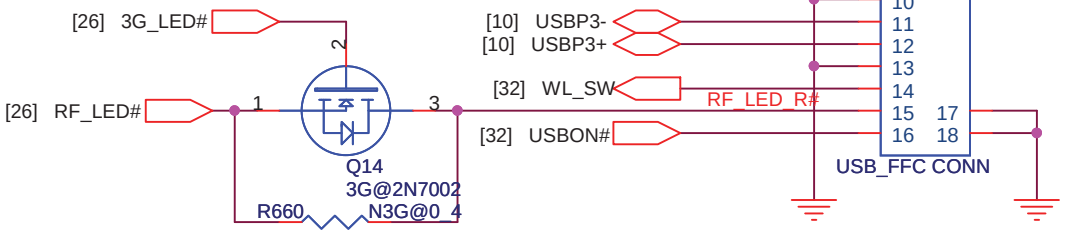
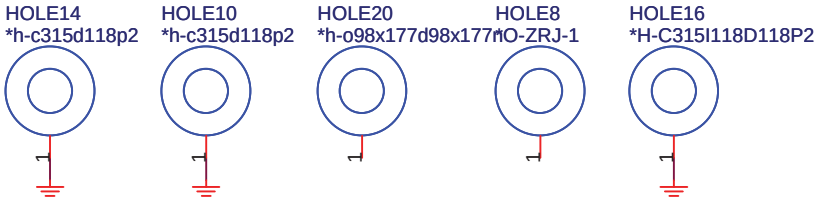
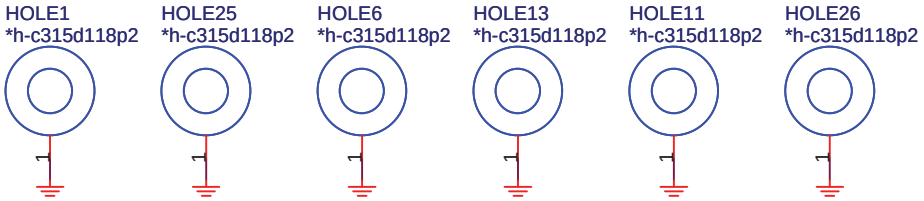
USB 2.0 (BTB)

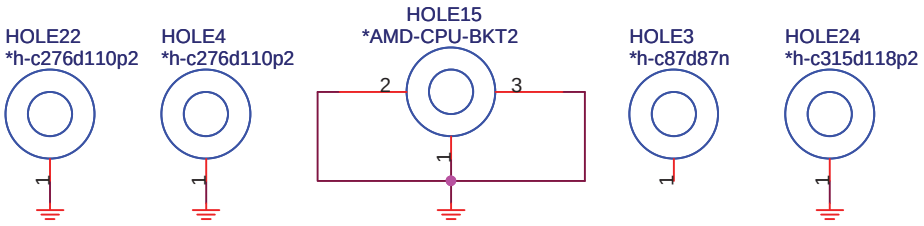


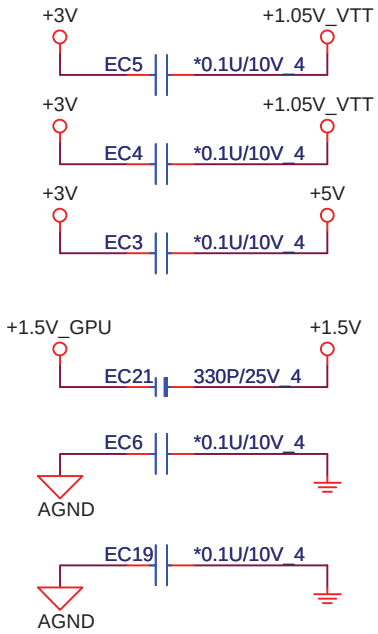


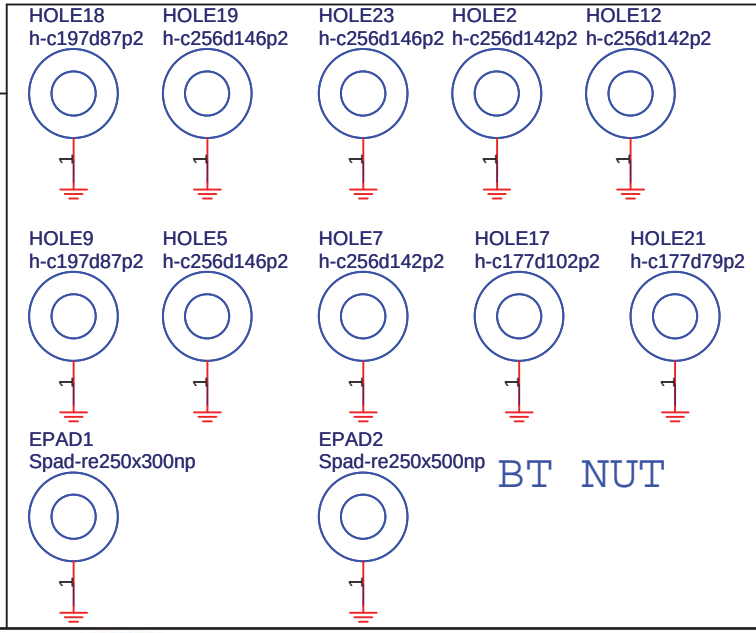










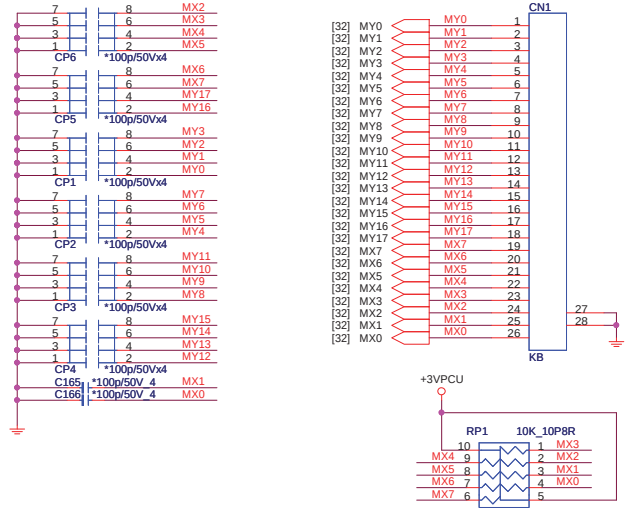


Quanta Computer Inc.

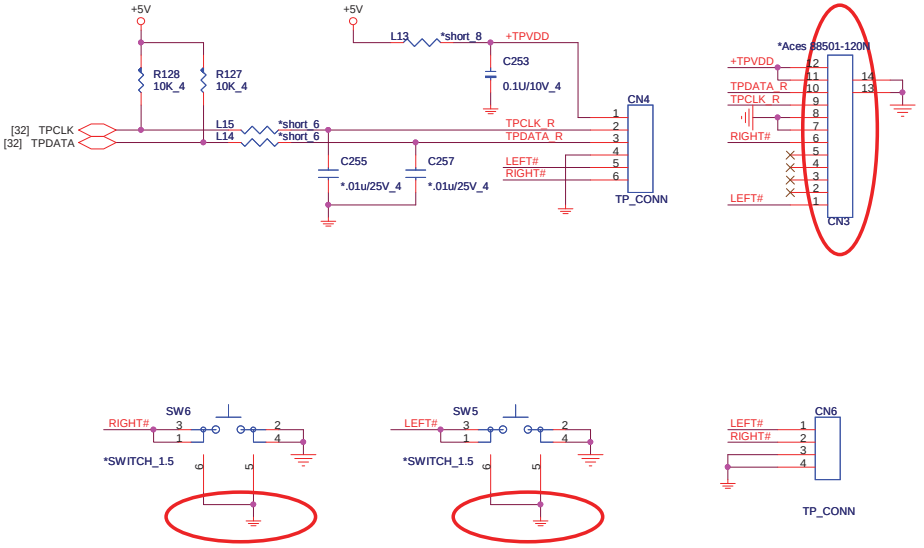
PROJECT : ZRJ

Size	Document Number	Rev
	USB2.0 Board (Dual Way)	1A
Date: Monday, January 24, 2011	Sheet 30 of 41	

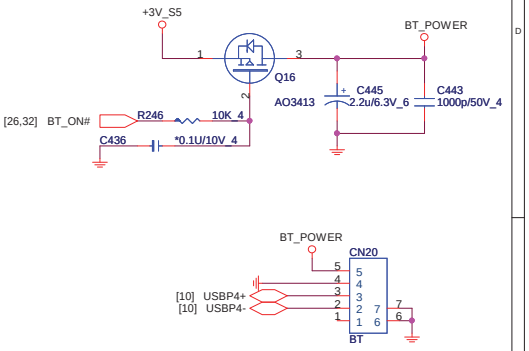
Keyboard (KBC)



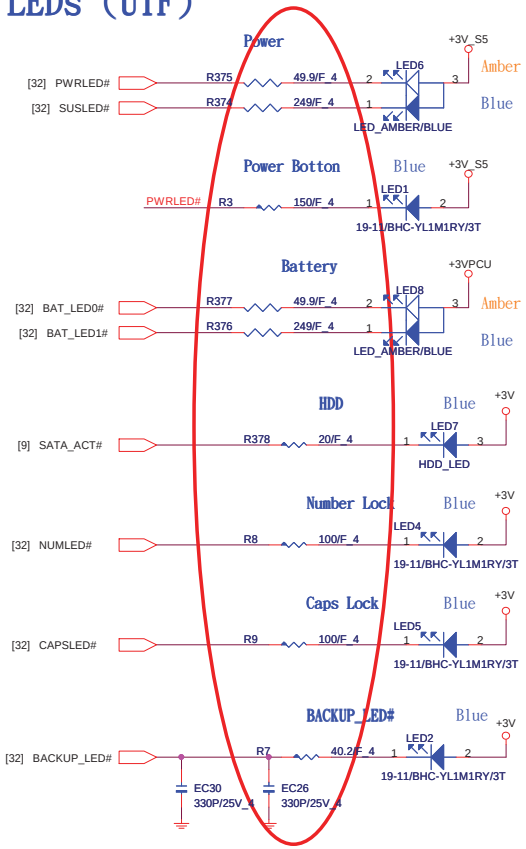
TouchPad (TPD)

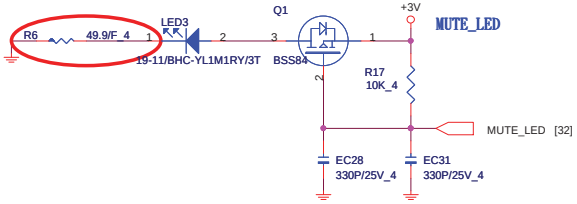


Bluetooth (BTM)

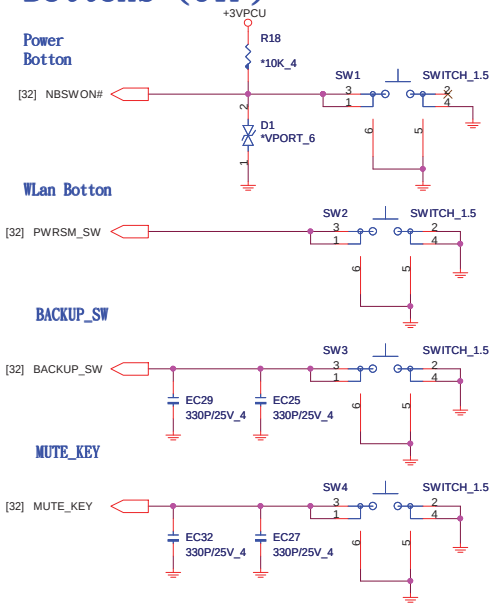


LEDs (UIF)

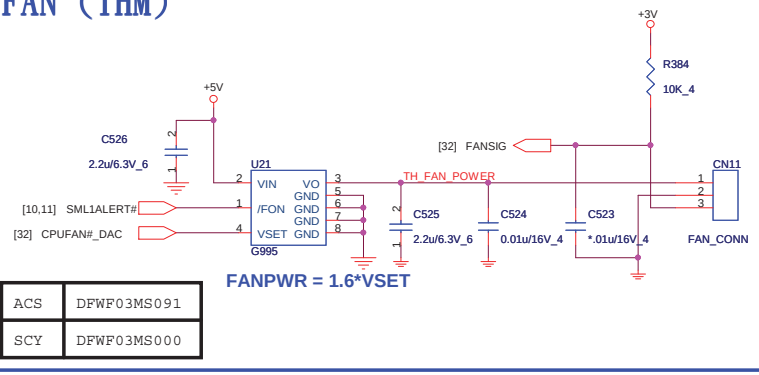




Bottons (UIF)

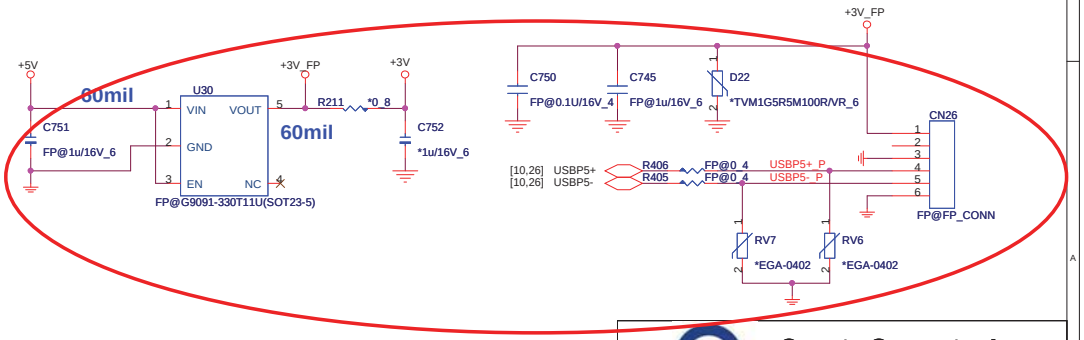


FAN (THM)



ACS	DFWF03MS091
SCY	DFWF03MS000

Finger-Printer CONN.



Quanta Computer Inc.

PROJECT : ZRJ

Size	Document Number	Rev
	KB/TP/BT/FAN/USB/LED/Bottom	1A

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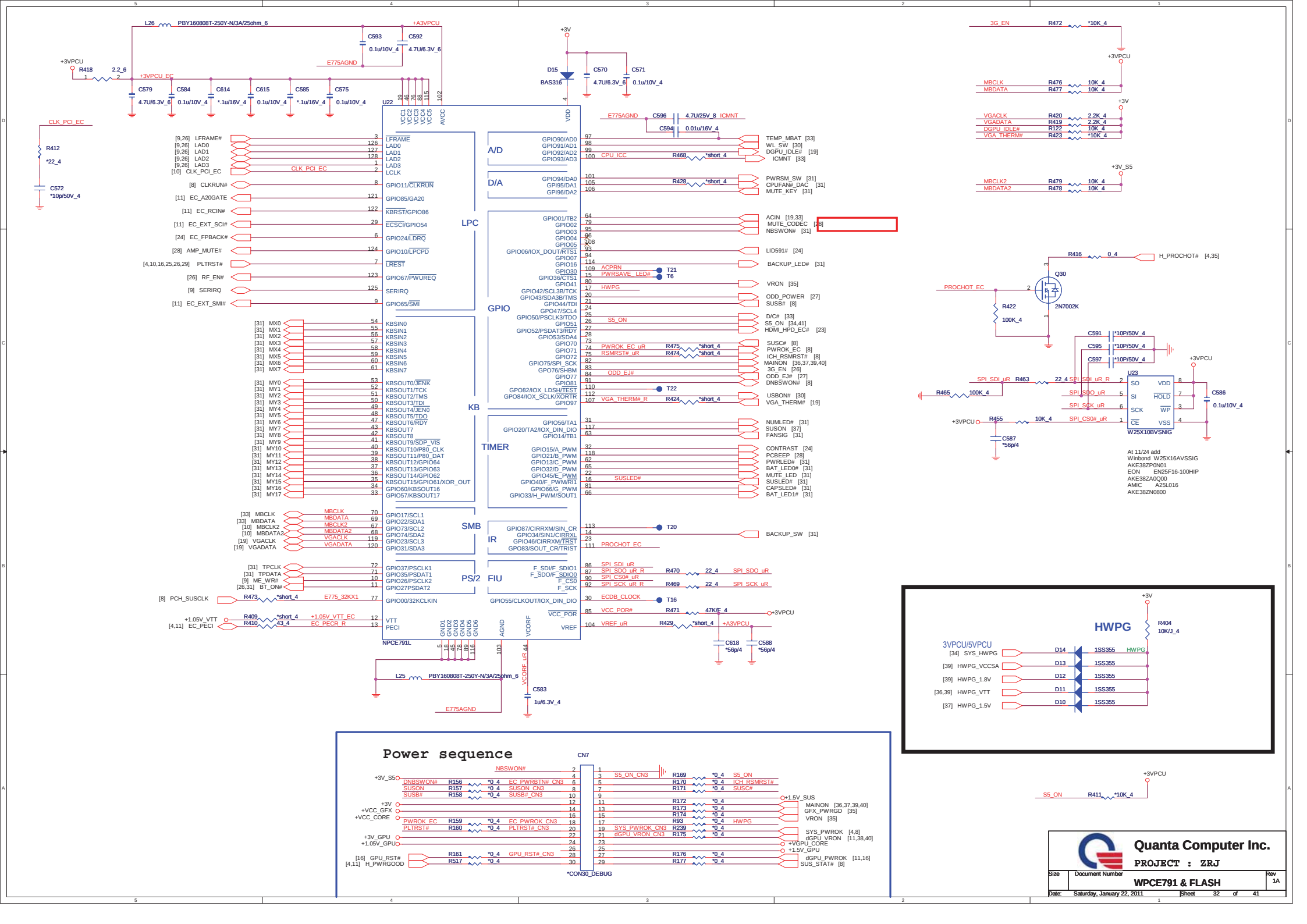
L26 PBY160808T-250Y-N/3A/25ohm_6
+A3VPCU
C593 0.1u/10V_4
C592 4.7U/6.3V_6
E775AGND
+3VPCU
R418 2.2_6
+3VPCU_EC
C579 4.7U/6.3V_6
C584 0.1u/10V_4
C614 *.1u/16V_4
C615 0.1u/10V_4
C585 *.1u/16V_4
C575 0.1u/10V_4
U22
VCC1 VCC2 VCC3 VCC4 VCC5 AVCC
VDD
+3V
D15 BAS316
C570 4.7U/6.3V_6
C571 0.1u/10V_4
CLK_PCI_EC
R412 *22_4
C572 *10p/50V_4
E775AGND C596 4.7U/25V_8 ICMNT
C594 0.01u/16V_4
[9,26] LFRAME#
[9,26] LAD0
[9,26] LAD1
[9,26] LAD2
[9,26] LAD3
[10] CLK_PCI_EC
CLK_PCI_EC
LFRAME
LAD0
LAD1
LAD2
LAD3
LCLK
LPC
[8] CLKRUN#
GPIO11/CLKRUN
[11] EC_A20GATE
GPIO85/GA20
[11] EC_RCIN#
KBRST/GPIO86
[11] EC_EXT_SCI#
ECSCI/GPIO54
[24] EC_FPBACK#
GPIO24/LDRQ
[28] AMP_MUTE#
GPIO10/LPCPD
[4,10,16,25,26,29] PLTRST#
LREST
[26] RF_EN#
GPIO67/PWUREQ
[9] SERIRQ
SERIRQ
[11] EC_EXT_SMI#
GPIO65/SMI
A/D
GPIO90/AD0
GPIO91/AD1
GPIO92/AD2
GPIO93/AD3
D/A
GPIO94/DA0
GPIO95/DA1
GPIO96/DA2
GPIO
GPIO01/TB2
GPIO02
GPIO03
GPIO04
GPIO05
GPIO06/IOX_DOUT/RTS1
GPIO07
GPIO16
GPIO30
GPIO36/CTS1
GPIO41
GPIO42/SCL3B/TCK
GPIO43/SDA3B/TMS
GPIO44/TDI
GPO47/SCL4
GPIO50/PSCLK3/TDO
GPIO51
GPIO52/PSDAT3/RDY
GPIO53/SDA4
GPIO70
GPIO71
GPIO72
GPIO75/SPI_SCK
GPO76/SHBM
GPIO77
GPIO81
GPO82/IOX_LDSH/TEST
GPO84/IOX_SCLK/XORTR
GPIO97
KB
[31] MX0
[31] MX1
[31] MX2
[31] MX3
[31] MX4
[31] MX5
[31] MX6
[31] MX7
KBSIN0
KBSIN1
KBSIN2
KBSIN3
KBSIN4
KBSIN5
KBSIN6
KBSIN7
[31] MY0
[31] MY1
[31] MY2
[31] MY3
[31] MY4
[31] MY5
[31] MY6
[31] MY7
[31] MY8
[31] MY9
[31] MY10
[31] MY11
[31] MY12
[31] MY13
[31] MY14
[31] MY15
[31] MY16
[31] MY17
KBSOUT0/JENK
KBSOUT1/TCK
KBSOUT2/TMS
KBSOUT3/TDI
KBSOUT4/JEN0
KBSOUT5/TDO
KBSOUT6/RDY
KBSOUT7
KBSOUT8
KBSOUT9/SDP_VIS
KBSOUT10/P80_CLK
KBSOUT11/P80_DAT
KBSOUT12/GPIO64
KBSOUT13/GPIO63
KBSOUT14/GPIO62
KBSOUT15/GPIO61/XOR_OUT
GPIO60/KBSOUT16
GPIO57/KBSOUT17
TIMER
GPIO56/TA1
GPIO20/TA2/IOX_DIN_DIO
GPIO14/TB1
GPIO15/A_PWM
GPIO21/B_PWM
GPIO13/C_PWM
GPIO32/D_PWM
GPIO45/E_PWM
GPIO40/F_PWM/RI1
GPIO66/G_PWM
GPIO33/H_PWM/SOUT1
SMB
[33] MBCLK
[33] MBDATA
[10] MBCLK2
[10] MBDATA2
[19] VGACLK
[19] VGADATA
GPIO17/SCL1
GPIO22/SDA1
GPIO73/SCL2
GPIO74/SDA2
GPIO23/SCL3
GPIO31/SDA3
MBCLK
MBDATA
MBCLK2
MBDATA2
VGACLK
VGADATA
IR
GPIO87/CIRRXM/SIN_CR
GPIO34/SIN1/CIRRXL
GPIO46/CIRRXM/TRST
GPO83/SOUT_CR/TRIST
PS/2
[31] TPCLK
[31] TPDATA
[9] ME_WR#
[26,31] BT_ON#
GPIO37/PSCLK1
GPIO35/PSDAT1
GPIO26/PSCLK2
GPIO27/PSDAT2
FIU
F_SDI/F_SDIO1
F_SDO/F_SDIO0
F_CS0
F_SCK
[8] PCH_SUSCLK
R473 *short_4
E775_32KX1
GPIO00/32KCLKIN
GPIO55/CLKOUT/IOX_DIN_DIO
+1.05V_VTT
[4,11] EC_PECI
R409 *short_4
R410 43_4
+1.05V_VTT_EC
EC_PECR_R
VTT
PECI
VCC_POR
VREF
GND1 GND2 GND3 GND4 GND5 GND6 AGND VCORF
NPCE791L
L25 PBY160808T-250Y-N/3A/25ohm_6
VCORF_uR_44
C583 1u/6.3V_4
E775AGND
R429 *short_4
+A3VPCU
C618 *56p/4
C588 *56p/4
R471 47K/F_4
+3VPCU
ECDB_CLOCK
T16
T20
BACKUP_SW [31]
PROCHOT_EC
SPI_SDI_uR
SPI_SDO_uR_R
SPI_CS0#_uR
SPI_SCK_uR_R
R470 22_4
R469 22_4
SPI_SDO_uR
SPI_SCK_uR
TEMP_MBAT [33]
WL_SW [30]
DGPU_IDLE# [19]
ICMNT [33]
CPU_ICC
R468 *short_4
PWRSM_SW [31]
CPUFAN#_DAC [31]
MUTE_KEY [31]
ACIN [19,33]
MUTE_CODEC [28]
NBSWON# [31]
LID591# [24]
BACKUP_LED# [31]
ACPRN
PWRSAVE_LED#
T21
T6
VRON [35]
ODD_POWER [27]
SUSB# [8]
D/C# [33]
S5_ON
S5_ON [34,41]
HDMI_HPD_EC# [23]
SUSC# [8]
PWROK_EC_uR
RSMRST#_uR
R475 *short_4
R474 *short_4
PWROK_EC [8]
ICH_RSMRST# [8]
MAINON [36,37,39,40]
3G_EN [26]
ODD_EJ# [27]
ODD_EJ#
DNBSWON# [8]
T22
USBON# [30]
VGA_THERM#_R
R424 *short_4
VGA_THERM# [19]
NUMLED# [31]
SUSON [37]
FANSIG [31]
CONTRAST [24]
PCBEEP [28]
PWRLED# [31]
BAT_LED0# [31]
MUTE_LED [31]
SUSLED# [31]
CAPSLED# [31]
BAT_LED1# [31]
SUSLED#
3G_EN R472 *10K_4
MBCLK R476 10K_4
MBDATA R477 10K_4
VGACLK R420 2.2K_4
VGADATA R419 2.2K_4
DGPU_IDLE# R422 10K_4
VGA_THERM# R423 *10K_4
MBCLK2 R479 10K_4
MBDATA2 R478 10K_4
+3V_S5
R416 0_4
H_PROCHOT# [4,35]
PROCHOT_EC
Q30 2N7002K
R422 100K_4
C591 *10P/50V_4
C595 *10P/50V_4
C597 *10P/50V_4
U23
SPI_SDI_uR R463 22_4
SPI_SDO_uR
SPI_SCK_uR
SPI_CS0#_uR
R465 100K_4
R455 10K_4
C587 *56p/4
SO VDD SI HOLD SCK WP CE VSS
W25X10BVSNIG
C586 0.1u/10V_4
At 11/24 add
Winbond W25X16AVSSIG
AKE38ZP0N01
EON EN25F16-100HIP
AKE38ZA0Q00
AMIC A25L016
AKE38ZN0800
HWPG
3VPCU/5VPCU
[34] SYS_HWPG
[39] HWPG_VCCSA
[39] HWPG_1.8V
[36,39] HWPG_VTT
[37] HWPG_1.5V
D14 D13 D12 D11 D10
1SS355
R404 10K/J_4
Power sequence
CN7
NBSWON#
+3V_S5
DNBSWON# R156 *0_4 EC_PWRBTN#_CN3
SUSON R157 *0_4 SUSON_CN3
SUSB# R158 *0_4 SUSB#_CN3
+3V
+VCC_GFX
+VCC_CORE
PWROK_EC R159 *0_4 EC_PWROK_CN3
PLTRST# R160 *0_4 PLTRST#_CN3
+3V_GPU
+1.05V_GPU
[16] GPU_RST#
[4,11] H_PWRGOOD
R161 *0_4 GPU_RST#_CN3
R517 *0_4
S5_ON_CN3
R169 *0_4 S5_ON
R170 *0_4 ICH_RSMRST#
R171 *0_4 SUSC#
+1.5V_SUS
R172 *0_4
R173 *0_4
R174 *0_4
R93 *0_4 HWPG
SYS_PWROK_CN3
dGPU_VRON_CN3
R239 *0_4
R175 *0_4
MAINON [36,37,39,40]
GFX_PWRGD [35]
VRON [35]
SYS_PWROK [4,8]
dGPU_VRON [11,38,40]
+VGPU_CORE
+1.5V_GPU
R176 *0_4
R177 *0_4
dGPU_PWROK [11,16]
SUS_STAT# [8]
*CON30_DEBUG
S5_ON R411 *10K_4
Quanta Computer Inc.
PROJECT : ZRJ
Size
Document Number
WPCE791 & FLASH
Rev 1A
Date: Saturday, January 22, 2011
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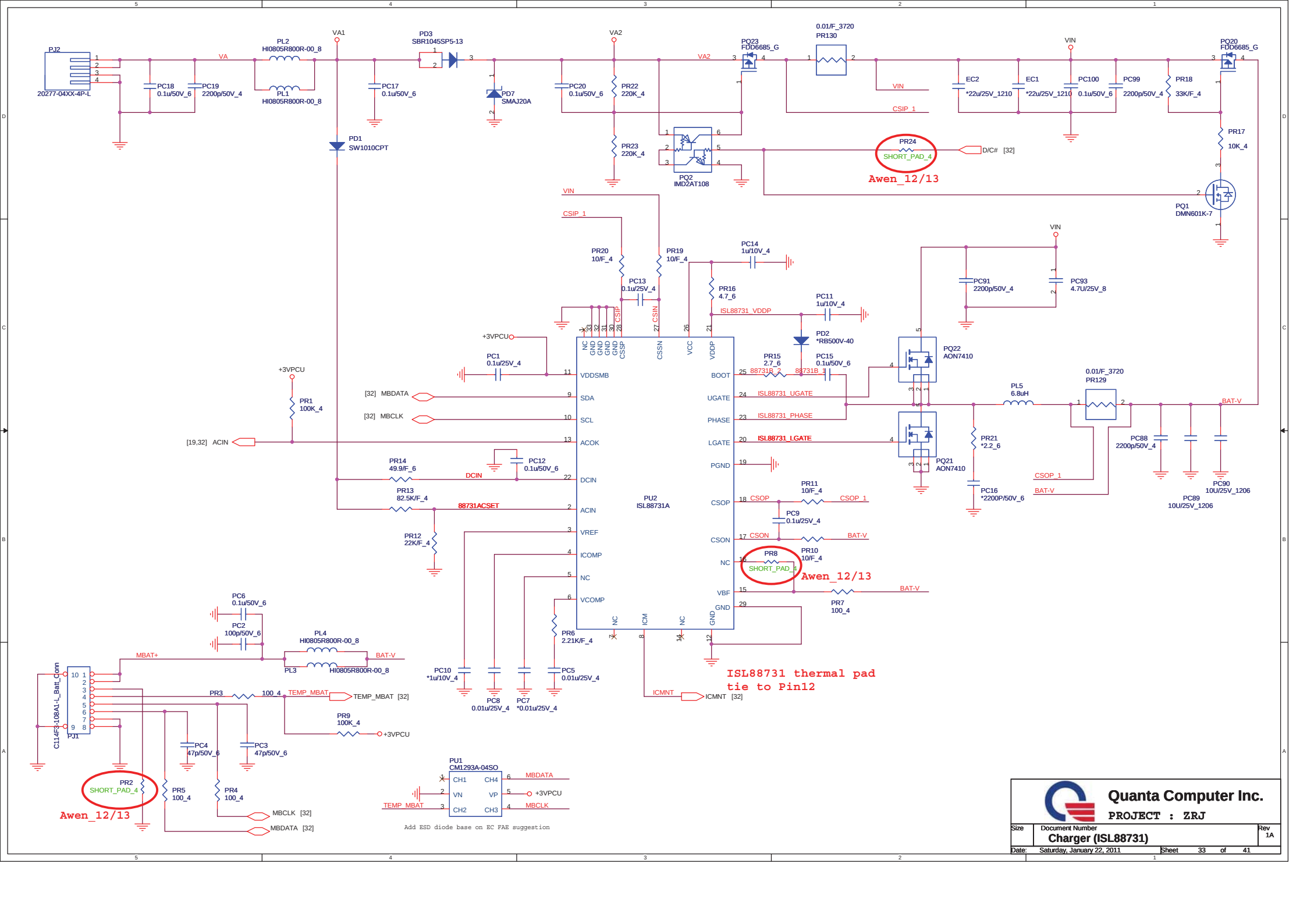
PJ2
20277-04XX-4P-L
PC18 0.1u/50V_6
PC19 2200p/50V_4
PL2 HI0805R800R-00_8
PL1 HI0805R800R-00_8
VA1
PC17 0.1u/50V_6
PD3 SBR1045SP5-13
PD7 SMAJ20A
PD1 SW1010CPT
VA2
PC20 0.1u/50V_6
PR22 220K_4
PR23 220K_4
PQ2 IMD2AT108
PQ23 FDD6685_G
0.01/F_3720 PR130
PR24 SHORT_PAD_4
D/C# [32]
Awen_12/13
EC2 *22u/25V_1210
EC1 *22u/25V_1210
PC100 0.1u/50V_6
PC99 2200p/50V_4
PR18 33K/F_4
PQ20 FDD6685_G
PR17 10K_4
PQ1 DMN601K-7
VIN
CSIP_1
PR20 10/F_4
PR19 10/F_4
PC13 0.1u/25V_4
PC14 1u/10V_4
PR16 4.7_6
PC11 1u/10V_4
ISL88731_VDDP
PD2 *RB500V-40
PC91 2200p/50V_4
PC93 4.7U/25V_8
+3VPCU
PC1 0.1u/25V_4
PR1 100K_4
[19,32] ACIN
[32] MBDATA
[32] MBCLK
PR14 49.9/F_6
DCIN
PC12 0.1u/50V_6
PR13 82.5K/F_4
88731ACSET
PR12 22K/F_4
PU2 ISL88731A
NC GND GND GND CSIP CSSN VCC VDDP
VDDSMB SDA SCL ACOK DCIN ACIN VREF ICOMP NC VCOMP
BOOT UGATE PHASE LGATE PGND CSOP CSON NC VBF GND
PR15 2.7_6
PC15 0.1u/50V_6
88731B_2
88731B_1
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
PQ22 AON7410
PQ21 AON7410
PL5 6.8uH
0.01/F_3720 PR129
BAT-V
PR21 *2.2_6
PC16 *2200P/50V_6
PC88 2200p/50V_4
PC90 10U/25V_1206
PC89 10U/25V_1206
CSOP_1
PR11 10/F_4
PC9 0.1u/25V_4
CSON
PR8 SHORT_PAD_4
PR10 10/F_4
Awen_12/13
PR7 100_4
PR6 2.21K/F_4
PC10 *1u/10V_4
PC8 0.01u/25V_4
PC7 *0.01u/25V_4
PC5 0.01u/25V_4
ISL88731 thermal pad tie to Pin12
ICMNT
ICMNT [32]
PC6 0.1u/50V_6
PC2 100p/50V_6
PL4 HI0805R800R-00_8
PL3 HI0805R800R-00_8
MBAT+
C114F3-10BA1-L_Batt_Conn
PJ1
PR3 100_4
TEMP_MBAT
TEMP_MBAT [32]
PR9 100K_4
PC4 47p/50V_6
PC3 47p/50V_6
PR2 SHORT_PAD_4
PR5 100_4
PR4 100_4
MBCLK [32]
MBDATA [32]
Awen_12/13
PU1 CM1293A-04SO
CH1 CH4 VN VP CH2 CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
Quanta Computer Inc.
PROJECT : ZRJ
Size
Document Number
Charger (ISL88731)
Rev 1A
Date: Saturday, January 22, 2011
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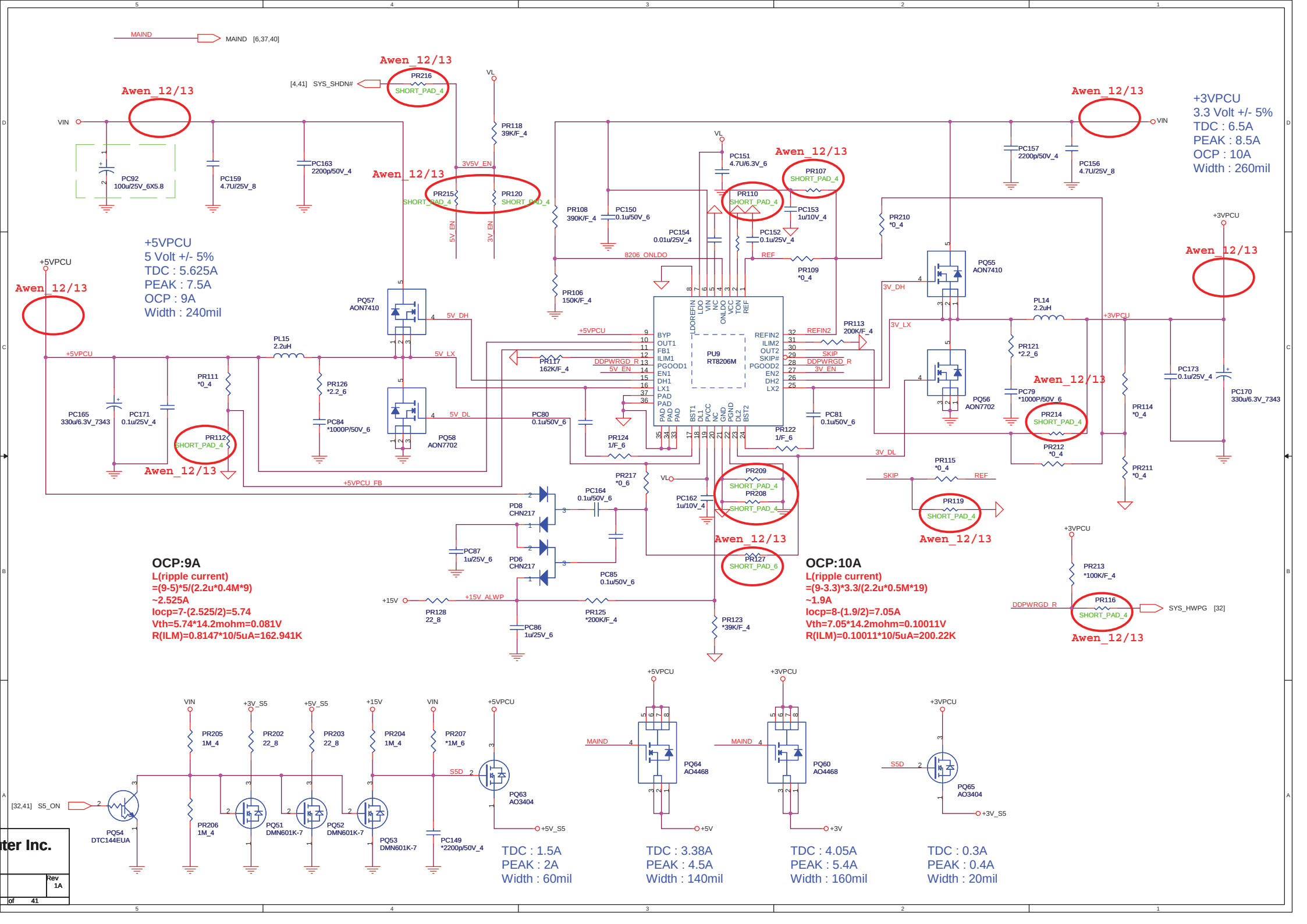
MAIND
MAIND [6,37,40]
Awen_12/13
[4,41] SYS_SHDN#
PR216
SHORT_PAD_4
VL
VIN
PR118
39K/F_4
3V5V_EN
PR215
SHORT_PAD_4
PR120
SHORT_PAD_4
5V_EN
3V_EN
PC92
100u/25V_6X5.8
PC159
4.7U/25V_8
PC163
2200p/50V_4
+5VPCU
5 Volt +/- 5%
TDC : 5.625A
PEAK : 7.5A
OCP : 9A
Width : 240mil
PR108
390K/F_4
PC150
0.1u/50V_6
PC151
4.7U/6.3V_6
PR107
SHORT_PAD_4
PR110
SHORT_PAD_4
PC153
1u/10V_4
PC154
0.01u/25V_4
PC152
0.1u/25V_4
8206_ONLDO
REF
PR109
*0_4
PR106
150K/F_4
PR210
*0_4
PC157
2200p/50V_4
PC156
4.7U/25V_8
+3VPCU
3.3 Volt +/- 5%
TDC : 6.5A
PEAK : 8.5A
OCP : 10A
Width : 260mil
PQ57
AON7410
5V_DH
5V_LX
PL15
2.2uH
PR111
*0_4
PR126
*2.2_6
PC84
*1000P/50V_6
PC165
330u/6.3V_7343
PC171
0.1u/25V_4
PR112
SHORT_PAD_4
PQ58
AON7702
5V_DL
PC80
0.1u/50V_6
PR117
162K/F_4
DDPWRGD_R
5V_EN
PU9
RT8206M
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
PVCC
NC
GND
PGND
DL2
BST2
PR113
200K/F_4
SKIP
3V_EN
PC81
0.1u/50V_6
PR122
1/F_6
PR124
1/F_6
PQ55
AON7410
3V_DH
3V_LX
PL14
2.2uH
PR121
*2.2_6
PC79
*1000P/50V_6
PR214
SHORT_PAD_4
PR212
*0_4
PQ56
AON7702
PR114
*0_4
PR211
*0_4
PC173
0.1u/25V_4
PC170
330u/6.3V_7343
3V_DL
PR115
*0_4
REF
PR119
SHORT_PAD_4
PR217
*0_6
PC164
0.1u/50V_6
PR209
SHORT_PAD_4
PR208
SHORT_PAD_4
PC162
1u/10V_4
PD8
CHN217
PD6
CHN217
PC87
1u/25V_6
PC85
0.1u/50V_6
PR127
SHORT_PAD_6
+15V
+15V_ALWP
PR128
22_8
PC86
1u/25V_6
PR125
*200K/F_4
PR123
*39K/F_4
+5VPCU_FB
OCP:9A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
~2.525A
Iocp=7-(2.525/2)=5.74
Vth=5.74*14.2mohm=0.081V
R(ILM)=0.8147*10/5uA=162.941K
OCP:10A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*19)
~1.9A
Iocp=8-(1.9/2)=7.05A
Vth=7.05*14.2mohm=0.10011V
R(ILM)=0.10011*10/5uA=200.22K
PR213
*100K/F_4
DDPWRGD_R
PR116
SHORT_PAD_4
SYS_HWPG [32]
[32,41] S5_ON
PQ54
DTC144EUA
PR205
1M_4
PR206
1M_4
+3V_S5
PR202
22_8
PQ51
DMN601K-7
+5V_S5
PR203
22_8
PQ52
DMN601K-7
PR204
1M_4
PQ53
DMN601K-7
PR207
*1M_6
S5D
PQ63
AO3404
PC149
*2200p/50V_4
TDC : 1.5A
PEAK : 2A
Width : 60mil
PQ64
AO4468
TDC : 3.38A
PEAK : 4.5A
Width : 140mil
PQ60
AO4468
TDC : 4.05A
PEAK : 5.4A
Width : 160mil
PQ65
AO3404
TDC : 0.3A
PEAK : 0.4A
Width : 20mil
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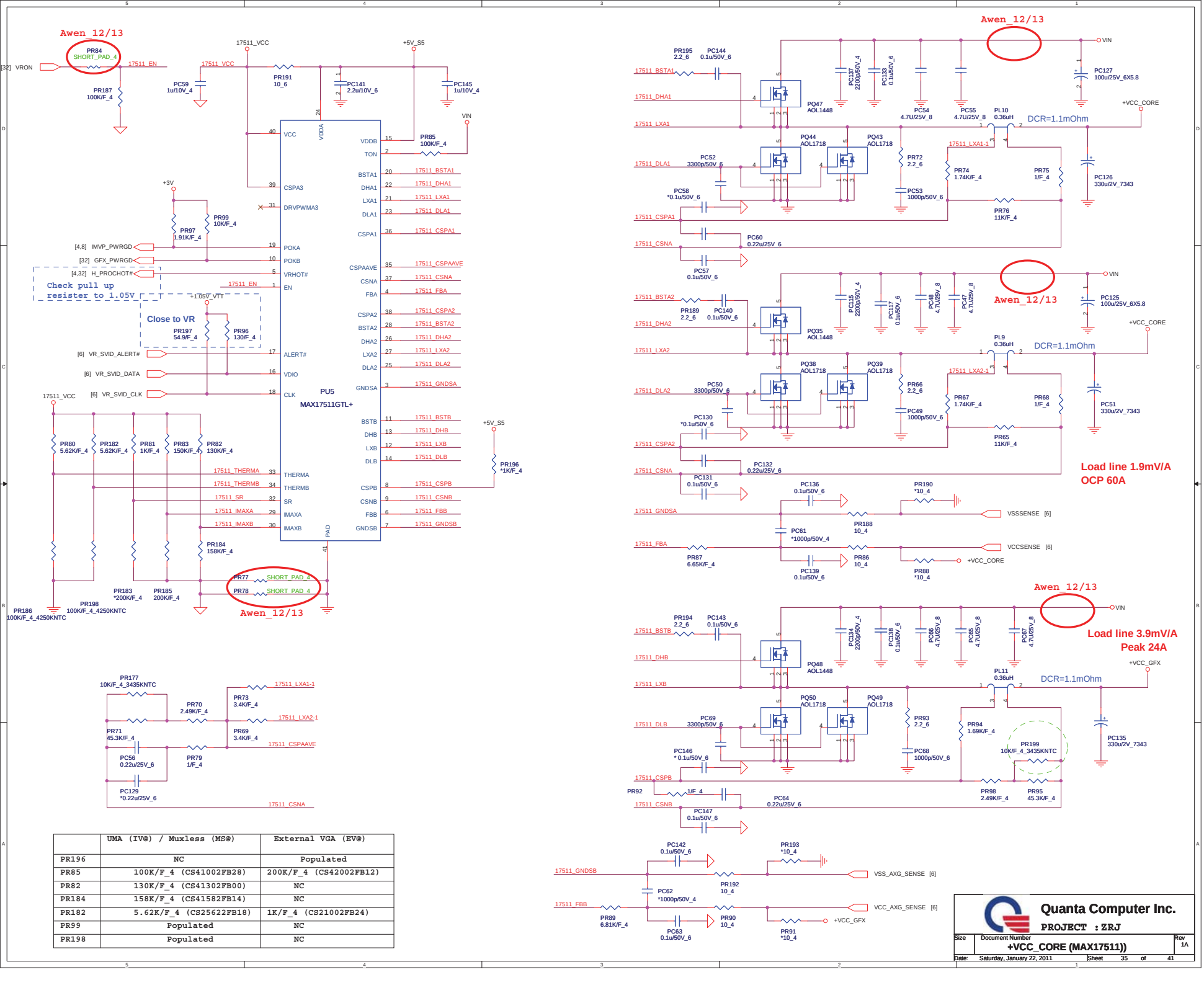

	UMA (IV@) / Muxless (MS@)	External VGA (EV@)
PR196	NC	Populated
PR85	100K/F_4 (CS41002FB28)	200K/F_4 (CS42002FB12)
PR82	130K/F_4 (CS41302FB00)	NC
PR184	158K/F_4 (CS41582FB14)	NC
PR182	5.62K/F_4 (CS25622FB18)	1K/F_4 (CS21002FB24)
PR99	Populated	NC
PR198	Populated	NC

Quanta Computer Inc.
PROJECT : ZRJ
Size | Document Number: +VCC_CORE (MAX17511)) | Rev: 1A
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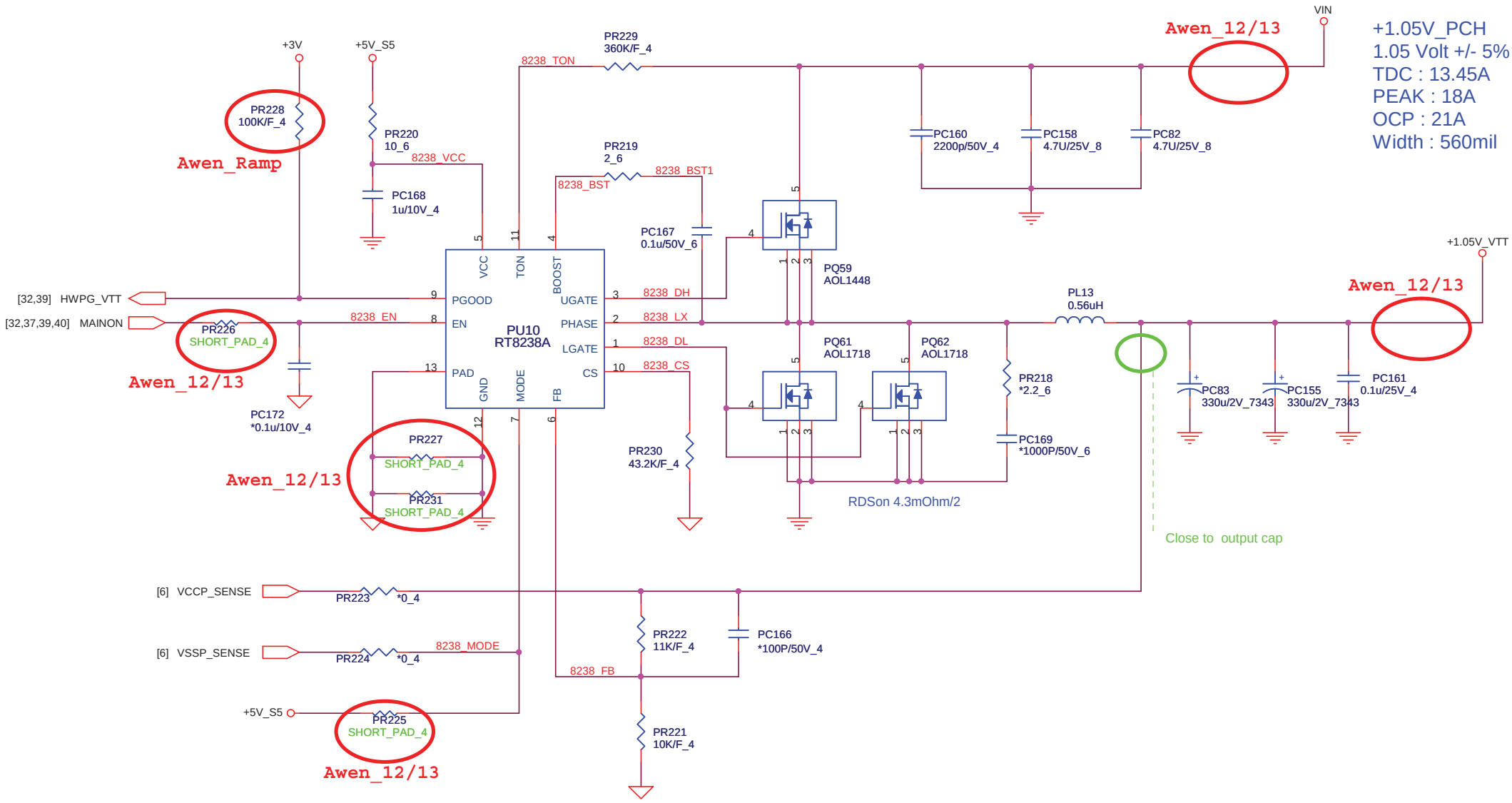

Current limit =10uA*Rth/RDSon

VOUT=(1+R1/R2)*0.5

Quanta Computer Inc.		
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Size	Document Number: +PCH&VTT (RT8238A)	Rev 1A
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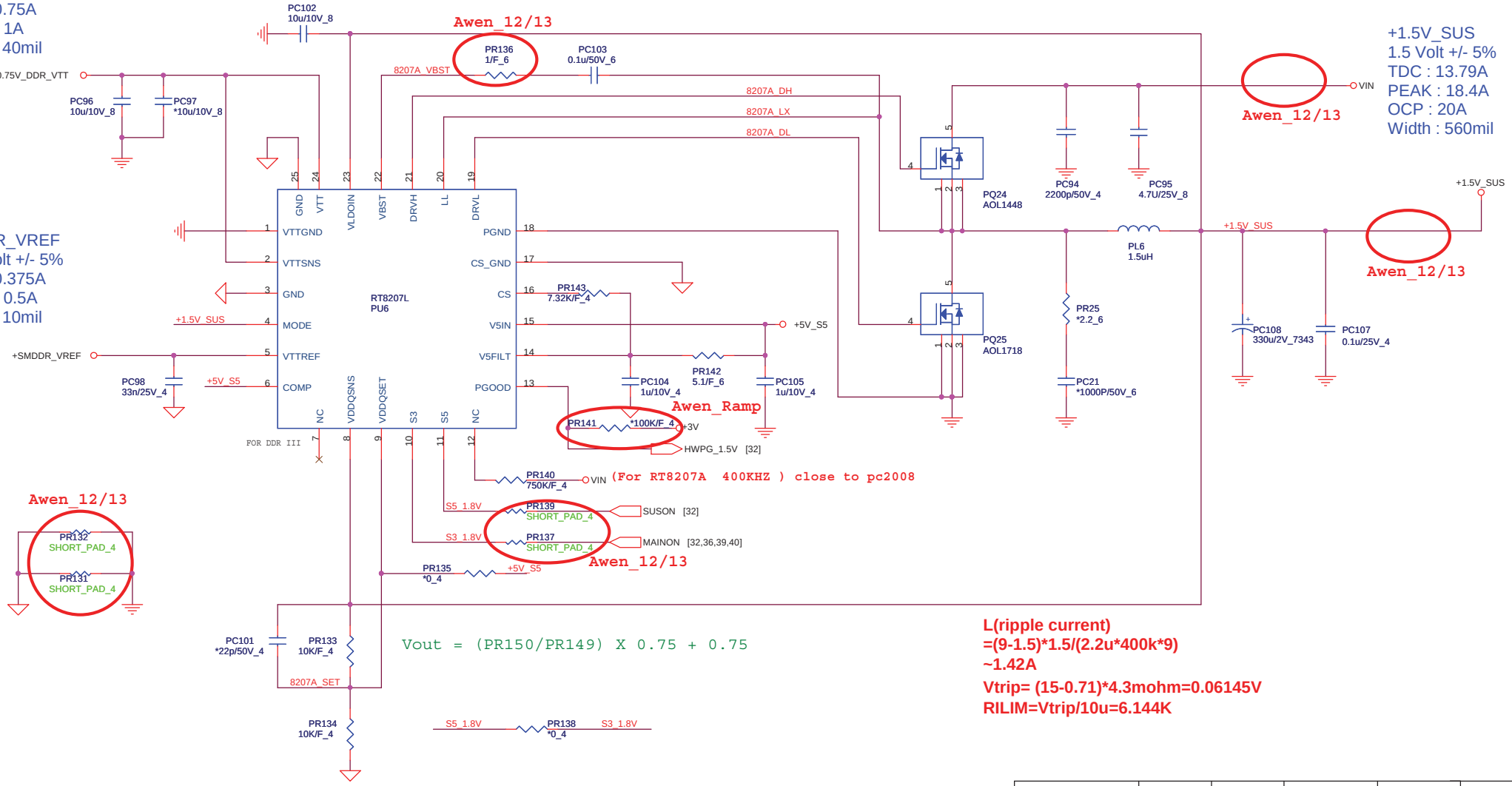
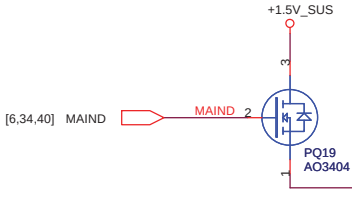
[PWM]

+0.75V_DDR_VTT
0.75 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

SMDDR_VREF
0.75 Volt +/- 5%
TDC : 0.375A
PEAK : 0.5A
Width : 10mil



L(ripple current)
=(9-1.5)*1.5/(2.2u*400k*9)
~1.42A
Vtrip= (15-0.71)*4.3mohm=0.06145V
RILIM=Vtrip/10u=6.144K



+1.5V
1.5 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 25mil

	S3	S5	+1.5V_SUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
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Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A

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NV VID Table for N12P-GV			
GPU_VID1	GPU_VID2	GPU_VID3	+VGPU_CORE
0	0	0	1.025V
1	0	0	1
0	1	0	0.9V
1	1	1	0.85V(Boot)

N12P-GV resister change table		
R1	32.4K	CS33242FB19
R2	19.1K	CS31912FB15
R3	487K	CS44872FB19
R4	86.6K	CS38662FB16
R5	267K	CS42672FB16

Awen_12/13

+VGPU_CORE
1 Volt +/- 5%
TDC : 24A
PEAK : 31.5A
OCP : 35.8A
Width : 1320mil

Close to Phase 1 Inductor

Awen_12/16

Awen_12/18

NV VID Table for N12P-GS			
GPU_VID1	GPU_VID2	GPU_VID3	+VGPU_CORE
0	0	0	1.00V
1	0	0	0.975V(Boot)
0	1	0	0.9V
1	1	1	0.825V

Quanta Computer Inc.
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Size	Document Number	Rev
	GPU CORE(OZ8117)	1A
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VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCCSA
0.9 Volt +/- 5%
TDC : 4.5A
PEAK : 6A
Width : 240mil

+3V
Awen_12/13
PC119 0.1u/25V_4
PC46 10u/10V_8
PC120 10u/10V_8
+5V_S5
PC124 2.2u/10V_6
PR170 SHORT_PAD_6
Awen_Ramp
Awen_12/13
PR172 *100K/F_4
PC123 1u/10V_4
51461_FILT
[32] HWPG_VCCSA
[32,36] HWPG_VTT
Awen_12/13
PR174 SHORT_PAD_4
PC122 *0.1u/25V_4
[6] VCCSA_SEL
Awen_12/13
PR162 SHORT_PAD_4
PR163 SHORT_PAD_4
PR173 1K_4
TPS51461 PU7
VIN VIN VIN PGND PGND PGND
V5DRV V5FILT PGOOD EN VID0 VID1 AGND
BST SW SW SW SW SW SW
MODE GND VREF COMP SLEW VOUT
PC121 0.1u/50V_6
51461_BST
51461_SW
51461_EN
PL8 1uH_7X7X3
VCCSA
Awen_12/13
PC113 330u/2V_7343
PC118 0.1u/25V_4
PR166 100_4
51461_MODE
51461_VREF
51461_SLEW
PR164 4.99K/F_4
PR167 *0_4
PC116 0.01u/25V_4
PC114 0.22u/25V_6
PC112 3.3n/50V_4
51461_VOUT
PR165 SHORT_PAD_4
VCCSA_SENSE [6]
Awen_12/13

VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V

+1.8V
1.8 Volt +/- 5%
TDC : 1.54A
PEAK : 2.05A
Width : 70mil

+3VPCU
Awen_12/13
PC76 10u/10V_8
PC148 0.1u/10V_4
PU8 HPA0835RTER
VIN VIN VIN EN VSNS COMP RT/CLK SS
PH PH PH BOOT PWRGD GND GND AGND
835_PH
Awen_12/13
PR104 SHORT_PAD_6
PC74 0.1u/50V_6
PL12 1uH_7X7X3
+1.8V
Awen_12/13
MAINON
Awen_12/13
PR201 SHORT_PAD_4
835_EN
54418-1.8_VFB
835_COMP
835_RTCLK
835_SS
PR105 *100K/F_4
PC78 1000p/50V_4
PR100 8.06K/F_4
PR103 182K/F_4
PC72 *100P/50V_4
PC75 0.01u/25V_4
PC71 2700p/50V_4
HWPG_1.8V [32]
PR200 *100K/F_4
+3V
Awen_Ramp
R1
R2
PR101 100K/F_4
PR102 78.7K/F_4
PC70 0.1u/10V_4
PC73 10u/10V_8
PC77 10u/10V_8
V0=0.8*(R1+R2)/R2
MAINON
MAINON [32,36,37,40]

Quanta Computer Inc.
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Size	Document Number	Rev
	VCCSA(TPS51461)/+1.8V(HPA00835)	1A
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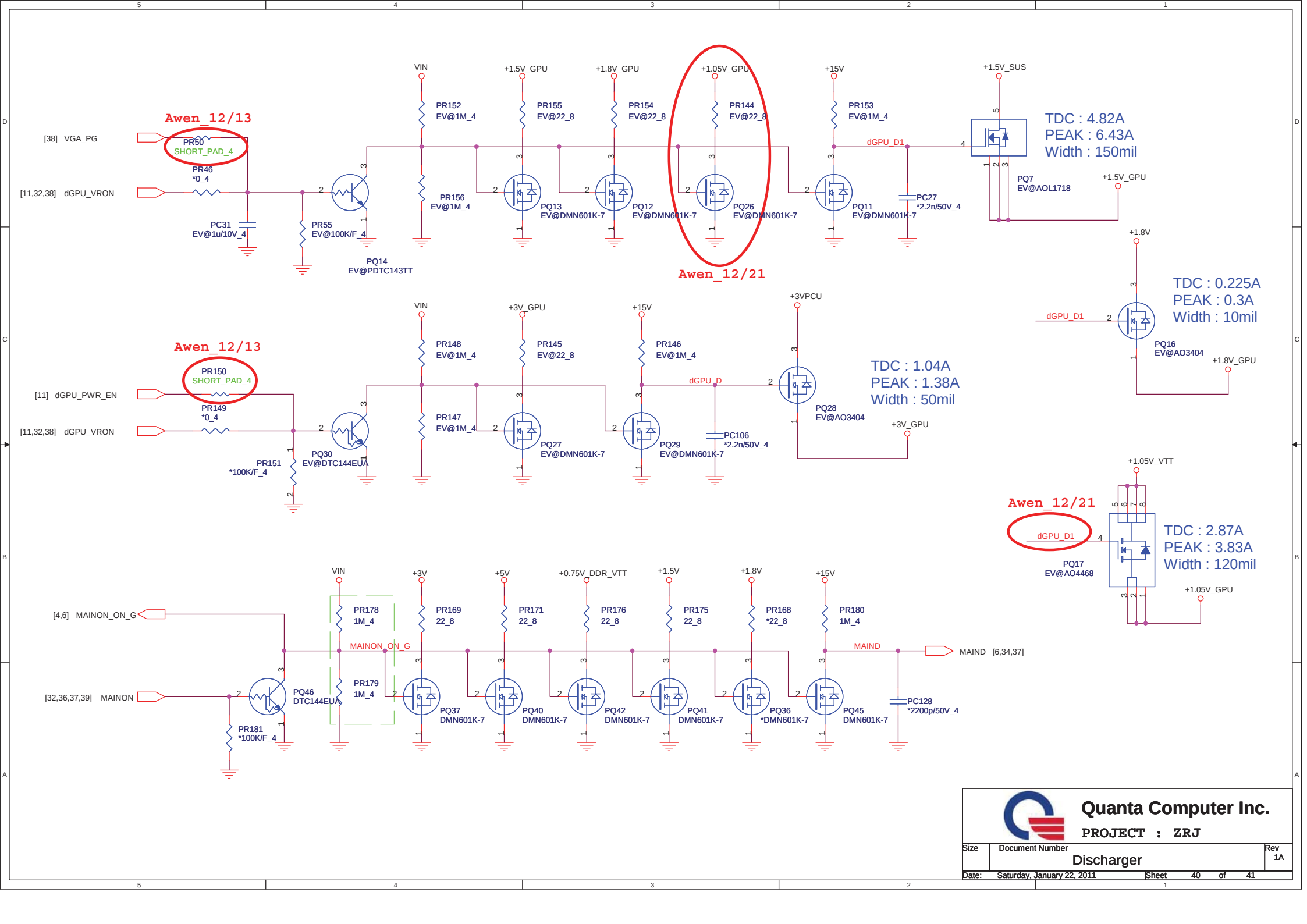
Awen_12/13
[38] VGA_PG
PR50
SHORT_PAD_4
PR46
*0_4
[11,32,38] dGPU_VRON
PC31
EV@1u/10V_4
PR55
EV@100K/F_4
PQ14
EV@PDTC143TT
VIN
PR152
EV@1M_4
PR156
EV@1M_4
+1.5V_GPU
PR155
EV@22_8
PQ13
EV@DMN601K-7
+1.8V_GPU
PR154
EV@22_8
PQ12
EV@DMN601K-7
+1.05V_GPU
PR144
EV@22_8
PQ26
EV@DMN601K-7
Awen_12/21
+15V
PR153
EV@1M_4
PQ11
EV@DMN601K-7
dGPU_D1
PC27
*2.2n/50V_4
+1.5V_SUS
PQ7
EV@AOL1718
+1.5V_GPU
TDC : 4.82A
PEAK : 6.43A
Width : 150mil
Awen_12/13
[11] dGPU_PWR_EN
PR150
SHORT_PAD_4
PR149
*0_4
[11,32,38] dGPU_VRON
PR151
*100K/F_4
PQ30
EV@DTC144EUA
VIN
PR148
EV@1M_4
PR147
EV@1M_4
+3V_GPU
PR145
EV@22_8
PQ27
EV@DMN601K-7
+15V
PR146
EV@1M_4
PQ29
EV@DMN601K-7
dGPU_D
PC106
*2.2n/50V_4
+3VPCU
PQ28
EV@AO3404
+3V_GPU
TDC : 1.04A
PEAK : 1.38A
Width : 50mil
+1.8V
dGPU_D1
PQ16
EV@AO3404
+1.8V_GPU
TDC : 0.225A
PEAK : 0.3A
Width : 10mil
+1.05V_VTT
Awen_12/21
dGPU_D1
PQ17
EV@AO4468
+1.05V_GPU
TDC : 2.87A
PEAK : 3.83A
Width : 120mil
[4,6] MAINON_ON_G
[32,36,37,39] MAINON
PQ46
DTC144EUA
PR181
*100K/F_4
VIN
PR178
1M_4
PR179
1M_4
MAINON_ON_G
+3V
PR169
22_8
PQ37
DMN601K-7
+5V
PR171
22_8
PQ40
DMN601K-7
+0.75V_DDR_VTT
PR176
22_8
PQ42
DMN601K-7
+1.5V
PR175
22_8
PQ41
DMN601K-7
+1.8V
PR168
*22_8
PQ36
*DMN601K-7
+15V
PR180
1M_4
PQ45
DMN601K-7
MAIND
PC128
*2200p/50V_4
MAIND [6,34,37]
Quanta Computer Inc.
PROJECT : ZRJ
Size
Document Number
Discharger
Rev
1A
Date: Saturday, January 22, 2011
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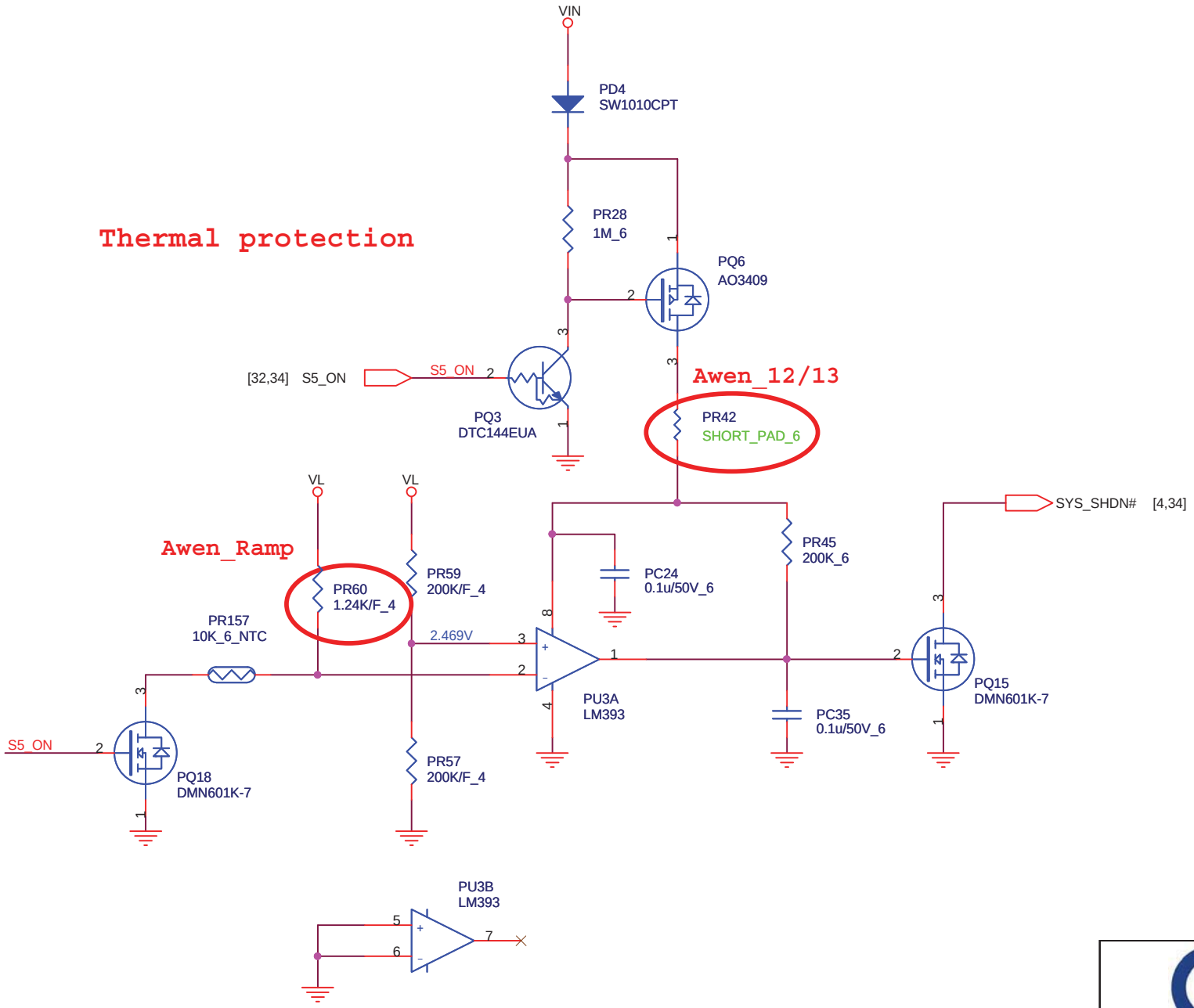
Thermal protection



For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
PROJECT : ZRJ		
Size	Document Number: Thermal protect	Rev: 1A
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CHANGE LIST

Model	REV	CHANGE LIST
ZRJ MB	1A	FIRST RELEASED
	2A	Page 9 : U27 Change footprint Page 12 : R244 ,R260 & R526 Change to short pad. Page 12 : Add C743 Page 19 : Remove R116 ,R117 & R118 Page 19 : GPU1.K3 Change to EV_LVDS_BRIGHT & GPU1.H3 Change to EV_LVDS_VDDEN Page 23 : D4 & D18 Change footprint Page 26 : CN12.45 ,47 & 49 modify PIN name from *_WLN to *_3G Page 30 : CN17 Change footprint Page 31 : Led6 & Led8 change pin define. Page 31 : Led8 change form +3V_S5 to +3VPCU Page 32 : U23 Change footprint. Page 38 : PR47 PU Change to +3V_GPU Page All : Remove 0 ohm Location : R121 ,R406 ,R405 ,R20 & R273 Page All : Change from 0 ohm to short pad Location : R468 ,R428 ,R475 ,R474 ,R424 ,R429 ,R409 ,R178 ,R168 ,L13 ,R195 ,R236 ,R253 ,R259 ,R359 ,R521 ,R61 ,R223 ,R247 ,R210 ,R133 ,R395 ,R396 ,R496 ,R162 ,R164 ,R43 ,L14 ,L15 ,R234 ,R256 ,R261 ,R295 ,R346 ,R363 ,R524 ,R525 ,R528 ,R537 ,R540 ,R586 ,R587 ,R248 ,R596 ,R533 ,R529 ,R536 ,R233 ,R519 ,R490 ,R491 ,R350 ,R242 ,R243 ,R266 ,R345 & R288
	2B	Page 26 : Add R606 , R607 Page 27 : (1) F2 Change to short pad. (2) Add R241(Short pad) Page 28 : Add net : MUTE_LED in U19.47 Page 30 : (1) Add Q14 & R660 (2) Del. Q44 & R223 (3) Change CN18.5 connect to +3V(originally : USB_OC1) (4) Change CN18.6 connect to 3G_LED(originally : USB_OC0) Page 31 : (1) Add LDO (Location : U30) (2) Change CN26 (FP pin define) (3) Add R273 & R260 Page 32 : Del. T28
	3A	Page 31 : (1) C751 & C752 Change from 0805 to 0603 (2) Remove R385 & R386 Page 38 : (1) PC42 replace C747
	3C	

MODEL	ZRJ	
	FROM	To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
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	3A	3B
	3A	3B
	3A	3B

DOC NO.	PROJECT MODEL :	ZRJ	APPROVED BY:	DATE:	2009/05/??
	PART NUMBER:		DRAWING BY:	REVISON:	1A