

Compal Confidential

PEW52 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRII + ICH9M

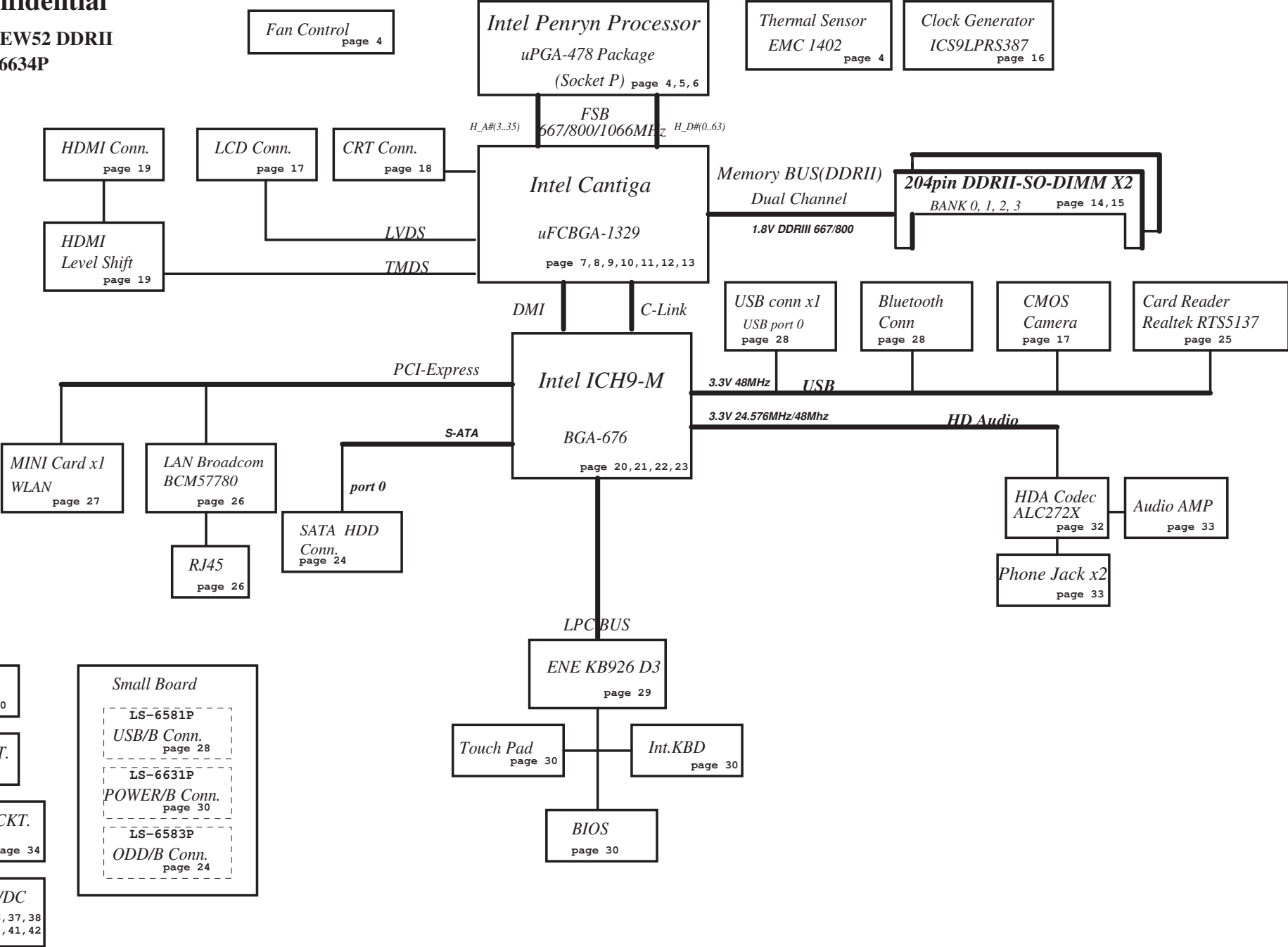
2010-08-06

REV : 0 . 1

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Model Name : PEW52 DDRII
File Name : LA6634P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for LVDS	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSb always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	SMSC EMC1402	100 1100 b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LVRS367, RTM890N)	1101 001Xb
DDR DIMM1	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
GM45 B3	GM@
GM40 A1	GLA1@
Bluetooth	BT@

PCIe table

PCIe port1	
PCIe port2	Wireless Card
PCIe port3	PCIe LAN
PCIe port4	
PCIe port5	
PCIe port6	

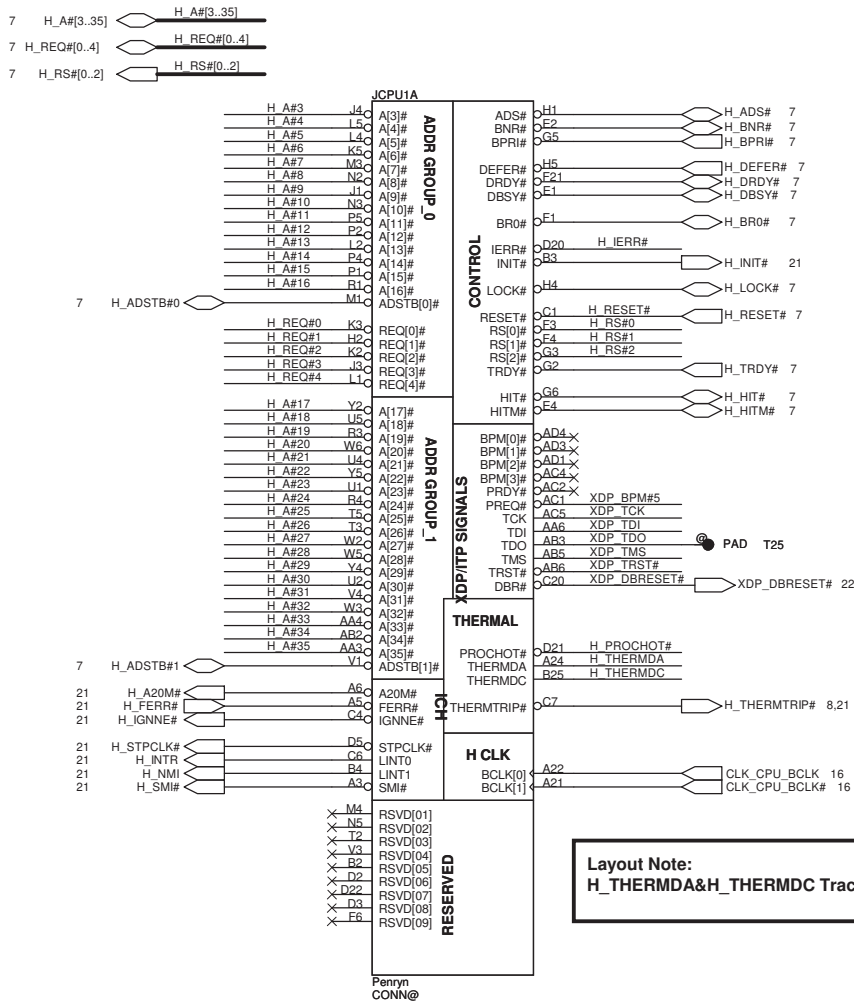
SATA table

SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	
SATA port5	

USB table

EHCI1	UHCI1	Port0	MB USB Conn.
		Port1	USB/B Conn.
	UHCI2	Port2	
		Port3	CMOS Camera
	UHCI3	Port4	Card Reader
Port5			
EHCI2	UHCI4	Port6	USB/B Conn.
		Port7	
	UHCI5	Port8	Blue Tooth
		Port9	
	UHCI6	Port10	Wireless Card
Port11			

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BSEL2	BSEL1	BSEL0	BCLK
0	0	0	266
0	1	0	200
0	1	1	166

PCB

777

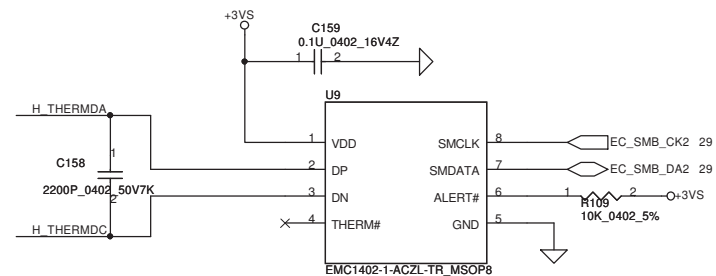
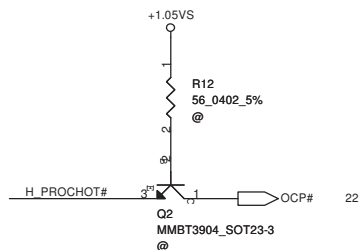
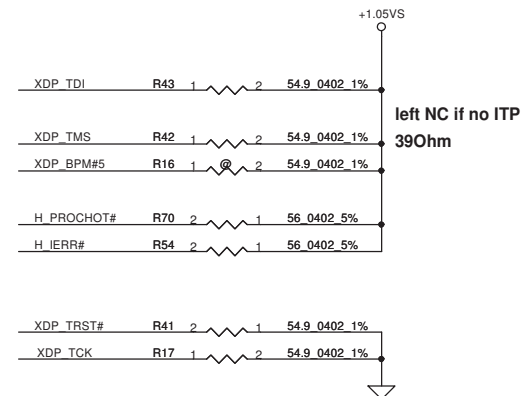
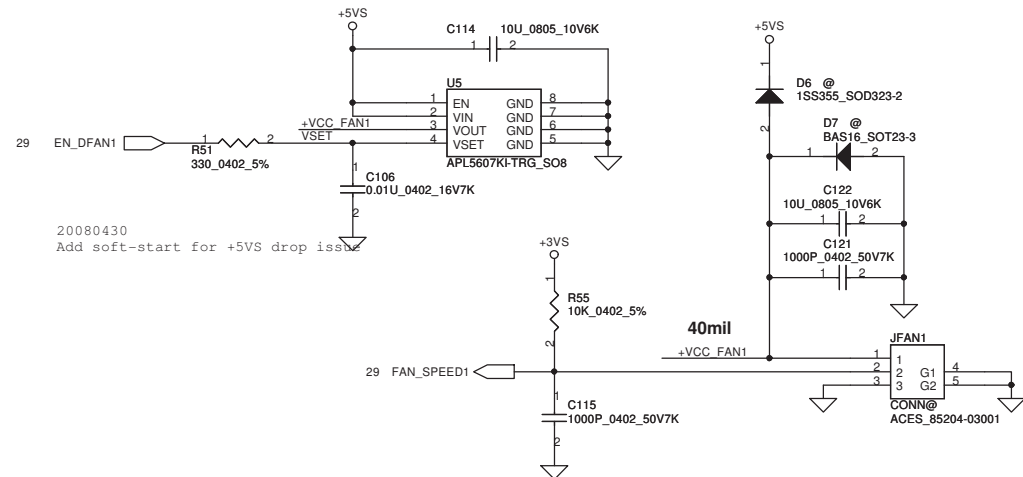
LA-6634P MB Rev0
 DA60000JS00

LA-6634P MB Rev0: DA60000JS00

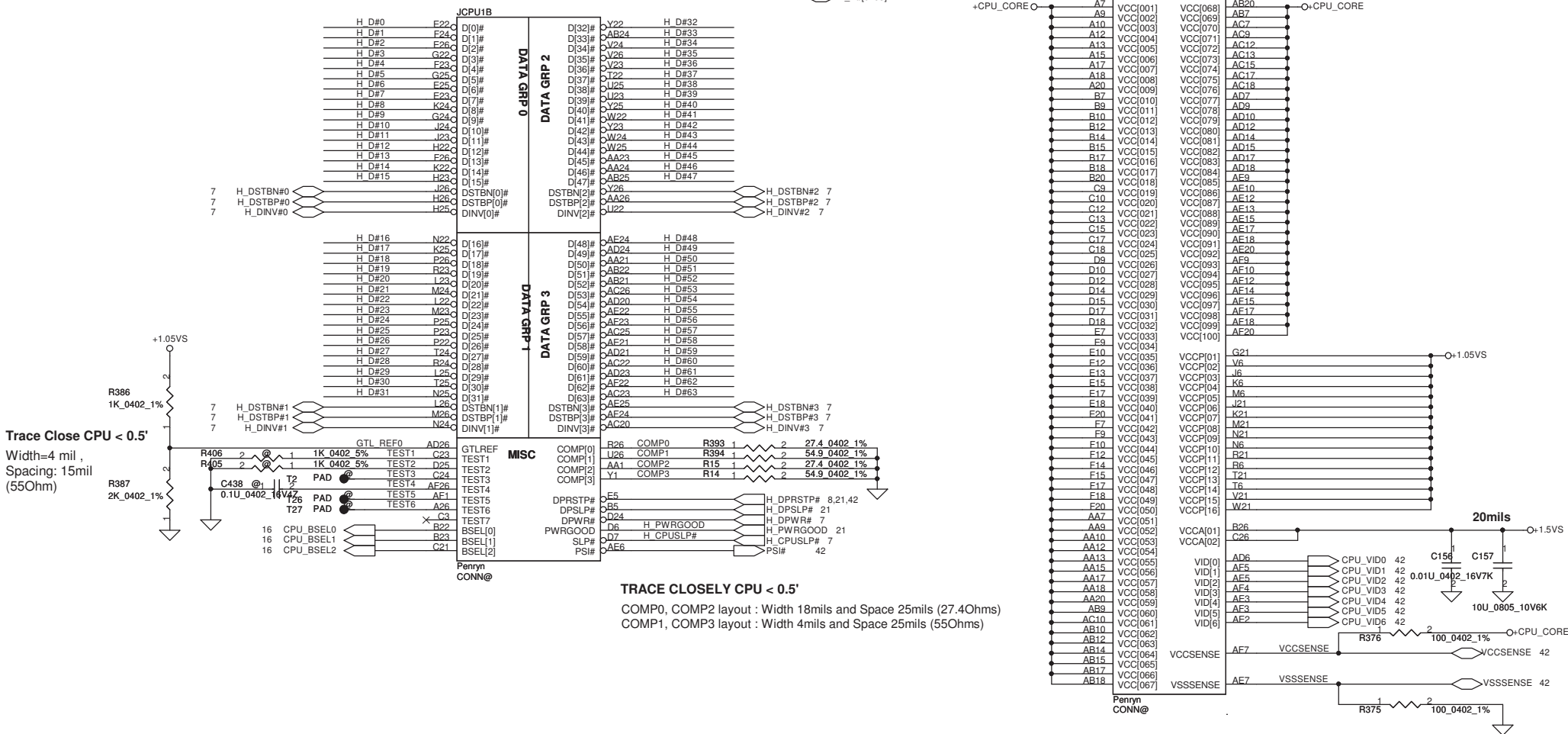
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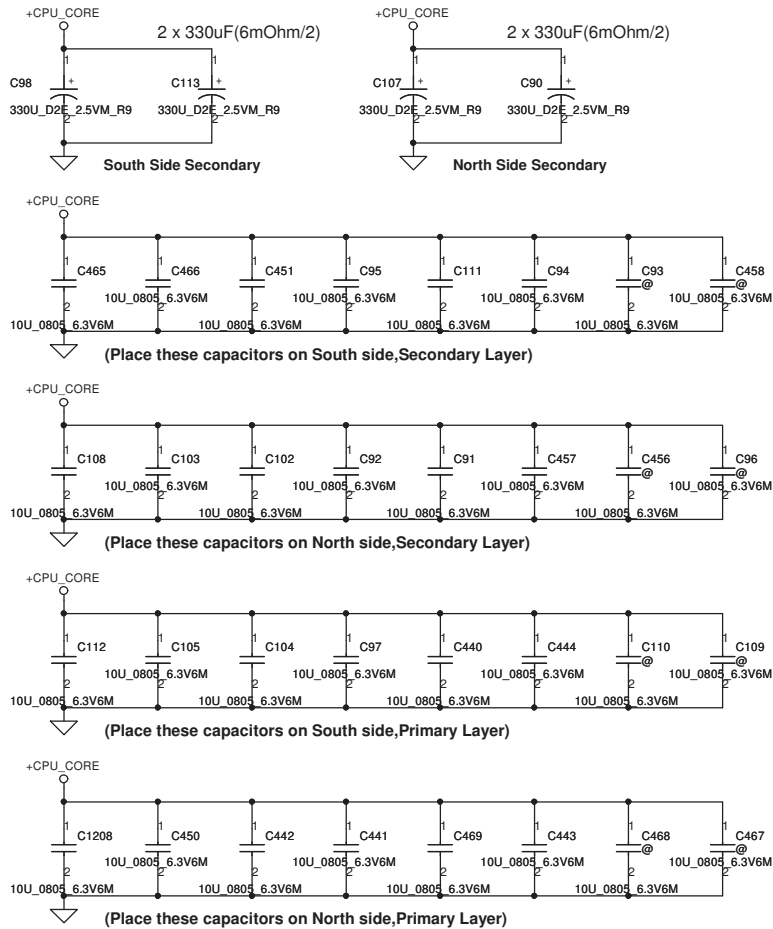
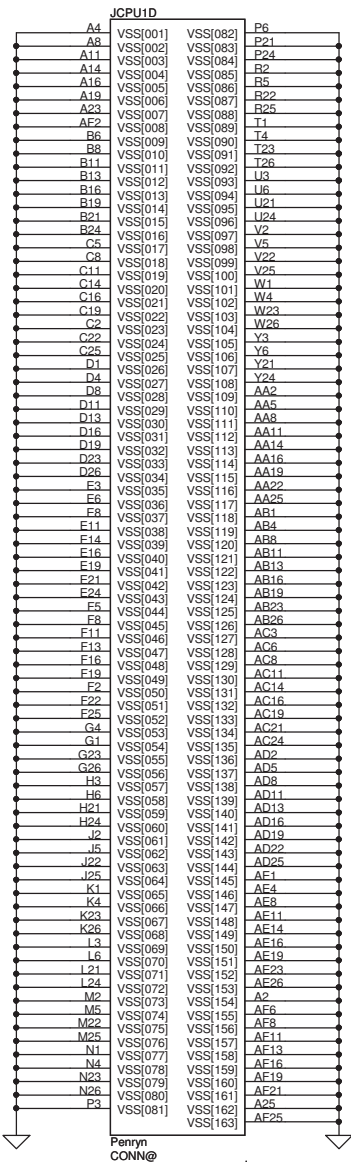
LA-6634P MB with Small Board Rev1:

PCB PEW72 LA-6631P LS-6631P/6581P/6583P

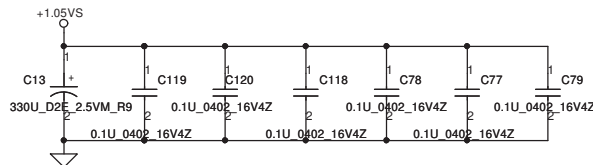


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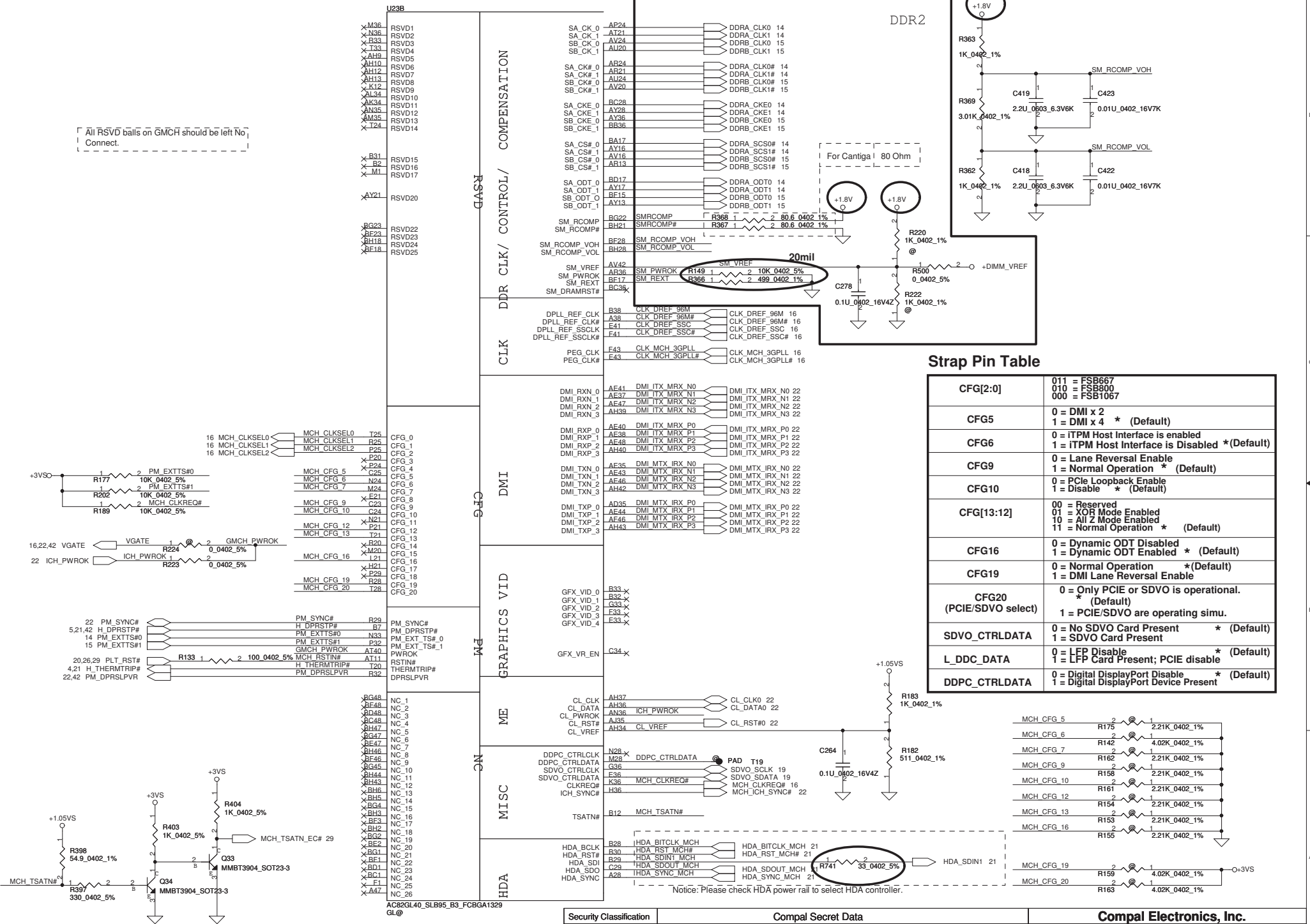


+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



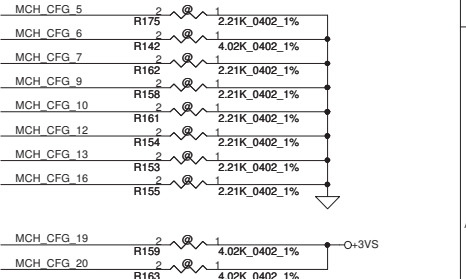
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All RSVD balls on GMCH should be left No Connect.



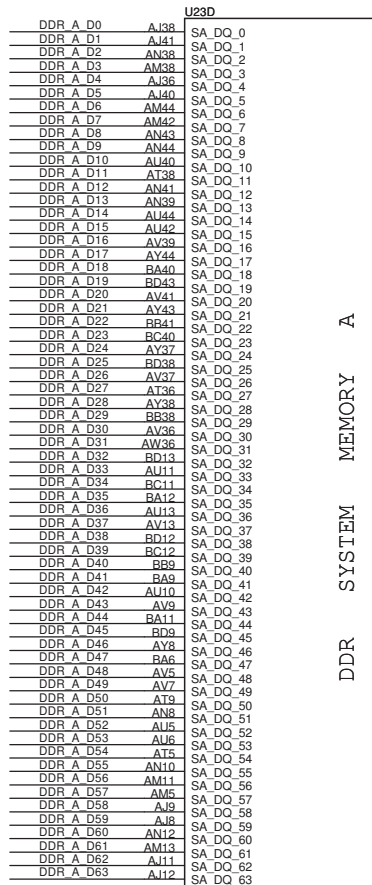
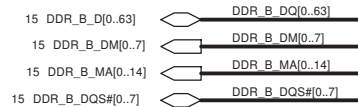
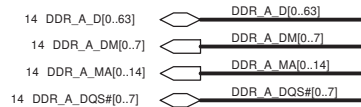
Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All 2 Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present * (Default) 1 = SDVO Card Present
L_DDC_DATA	0 = LFP Disable 1 = All Card Present; PCIe disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable 1 = Digital DisplayPort Device Present * (Default)



Notice: Please check HDA power rail to select HDA controller.

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SA_BS_0
SA_BS_1
SA_BS_2

SA_RAS#
SA_CAS#
SA_WE#

SA_DM_0
SA_DM_1
SA_DM_2
SA_DM_3
SA_DM_4
SA_DM_5
SA_DM_6
SA_DM_7

SA_DQS_0
SA_DQS_1
SA_DQS_2
SA_DQS_3
SA_DQS_4
SA_DQS_5
SA_DQS_6
SA_DQS_7

SA_DQS#_0
SA_DQS#_1
SA_DQS#_2
SA_DQS#_3
SA_DQS#_4
SA_DQS#_5
SA_DQS#_6
SA_DQS#_7

SA_MA_0
SA_MA_1
SA_MA_2
SA_MA_3
SA_MA_4
SA_MA_5
SA_MA_6
SA_MA_7
SA_MA_8
SA_MA_9
SA_MA_10
SA_MA_11
SA_MA_12
SA_MA_13
SA_MA_14

BD21
BG18
AT25

BB20
BD20
AY20

AM37
AT41
AY41
AJ39
BB12
AY6
AT7
AJ5

AJ44
AT44
BA43
BG37
AW12
BC8
AJ8
AM7

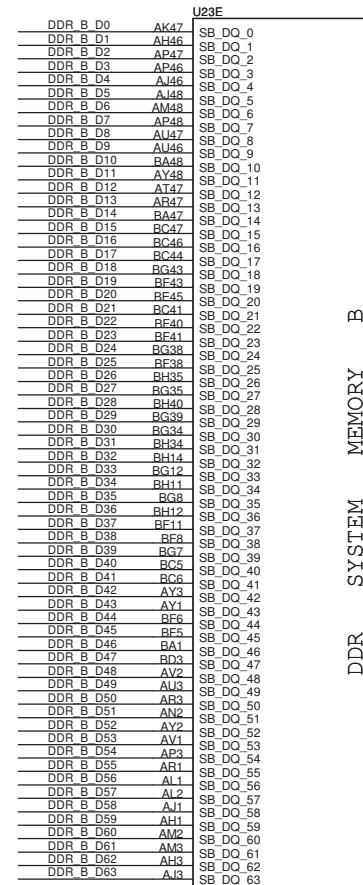
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AJ9
AM8

BA21
BC24
BG24
BH24
BG25
BA24
BD24
BG27
BE25
AW24
BC21
BG26
BH26
BH17
AY25

DDR A BS0 14
DDR A BS1 14
DDR A BS2 14

DDR A RAS# 14
DDR A CAS# 14
DDR A WE# 14

DDR A DQS0 14
DDR A DQS1 14
DDR A DQS2 14
DDR A DQS3 14
DDR A DQS4 14
DDR A DQS5 14
DDR A DQS6 14
DDR A DQS7 14



SB_BS_0
SB_BS_1
SB_BS_2

SB_RAS#
SB_CAS#
SB_WE#

SB_DM_0
SB_DM_1
SB_DM_2
SB_DM_3
SB_DM_4
SB_DM_5
SB_DM_6
SB_DM_7

SB_DQS_0
SB_DQS_1
SB_DQS_2
SB_DQS_3
SB_DQS_4
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SB_DQS_6
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SB_MA_0
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SB_MA_2
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SB_MA_6
SB_MA_7
SB_MA_8
SB_MA_9
SB_MA_10
SB_MA_11
SB_MA_12
SB_MA_13
SB_MA_14

BC16
BB17
RB33

AJ17
BG16
BF14

AM47
AY47
BD40
BC35
BG11
BA3
AP1
AK2

AI47
AV48
BG41
RG37
BH9
BB2
AJ1
AN6

AI46
AV47
BH41
BH37
BG9
BC2
AT2
AN5

AV17
BA25
BC25
AJ25
AW25
BB28
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AW28
AT33
BD33
BH16
AY33
BH15
AJ33

DDR B BS0 15
DDR B BS1 15
DDR B BS2 15

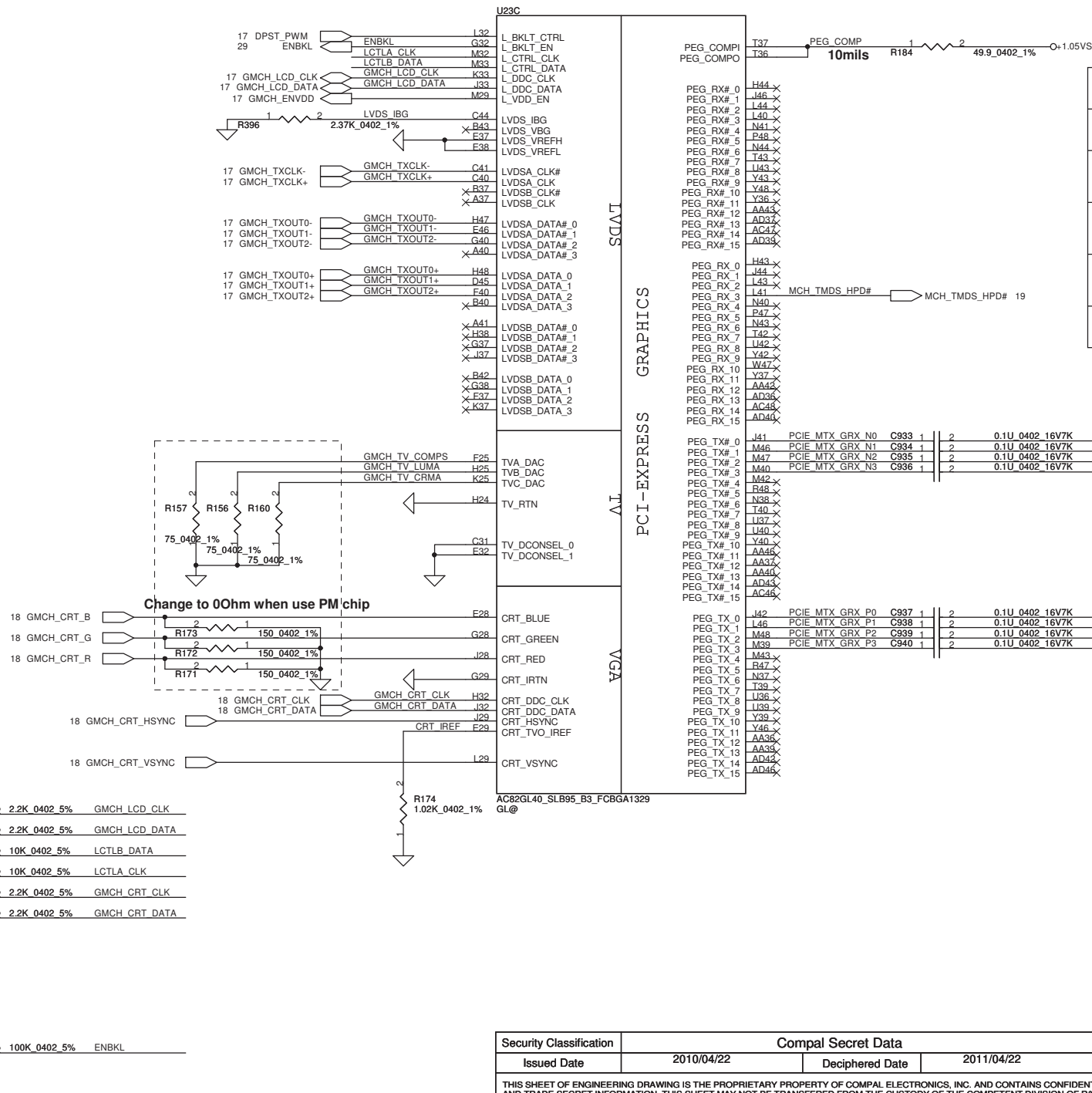
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DDR B CAS# 15
DDR B WE# 15

DDR B DQS0 15
DDR B DQS1 15
DDR B DQS2 15
DDR B DQS3 15
DDR B DQS4 15
DDR B DQS5 15
DDR B DQS6 15
DDR B DQS7 15

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GL@

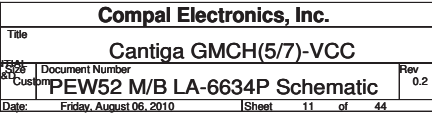
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GL@

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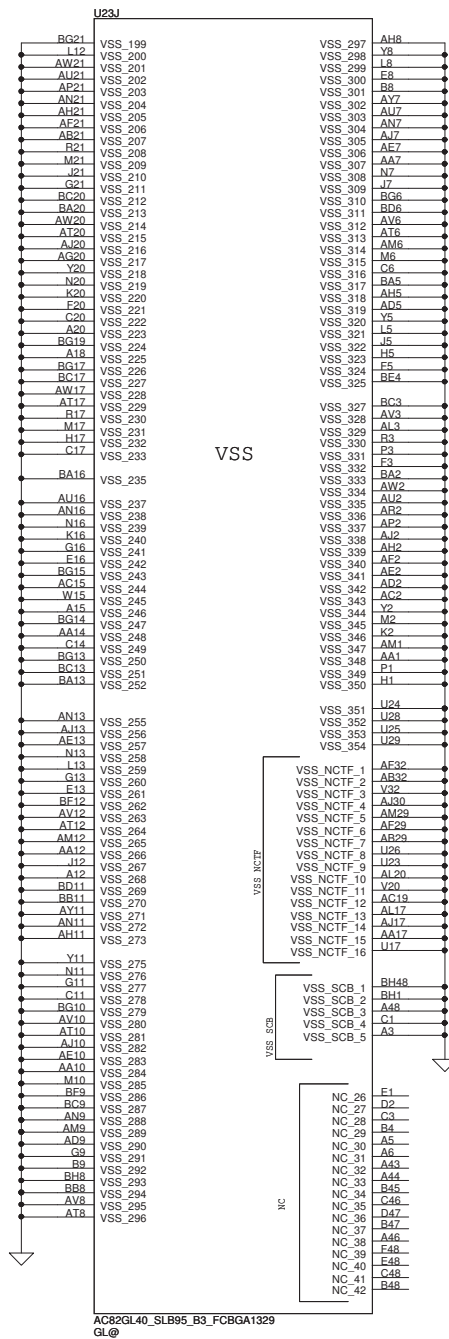
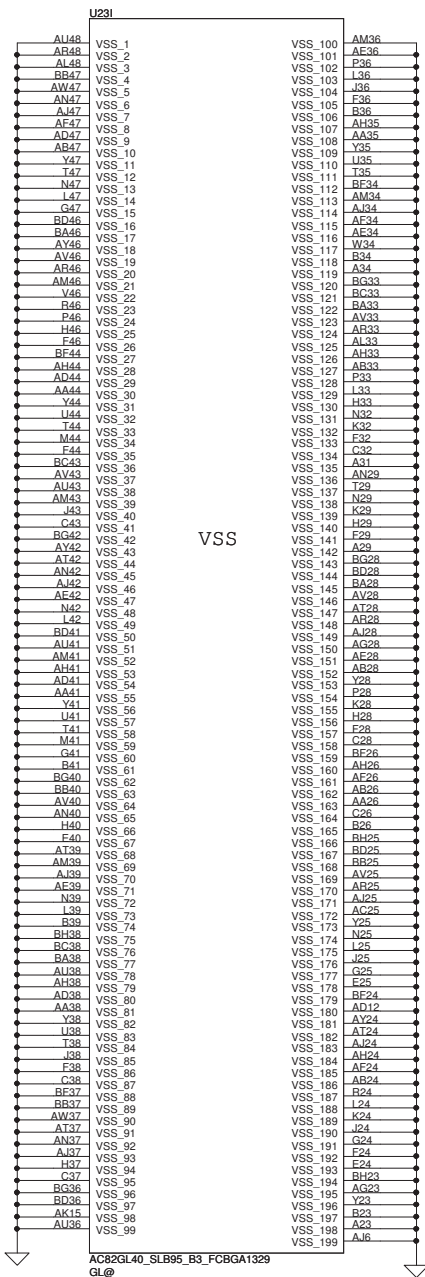


Intel Cantiga TMD5 Pin Definition

TMDS_B_CLK	PEG_TXP_3
TMDS_B_CLK#	PEG_TXN_3
TMDS_B_DATA0	PEG_TXP_2
TMDS_B_DATA0#	PEG_TXN_2
TMDS_B_DATA1	PEG_TXP_1
TMDS_B_DATA1#	PEG_TXN_1
TMDS_B_DATA2	PEG_TXP_0
TMDS_B_DATA2#	PEG_TXN_0
TMDS_B_HPDP#	PEG_RXP_3



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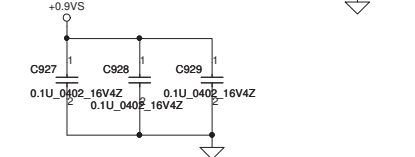
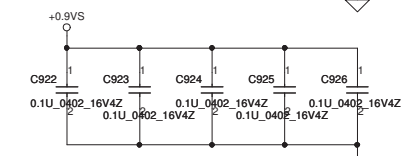
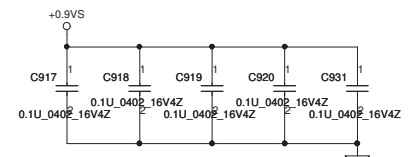
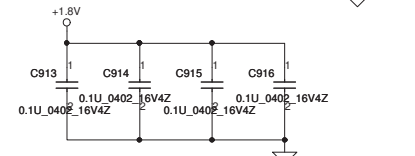
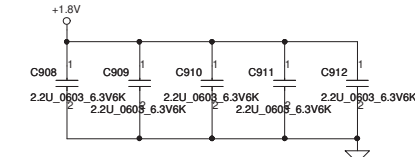
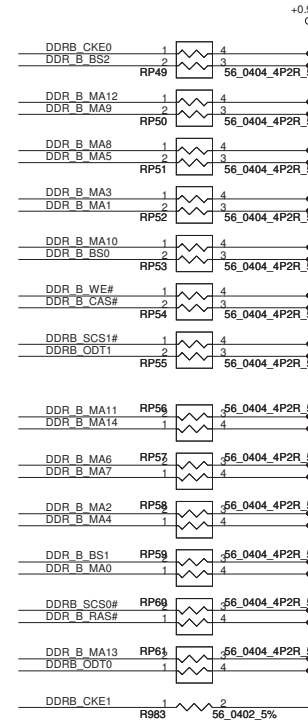
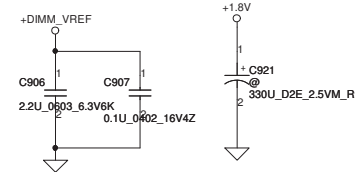
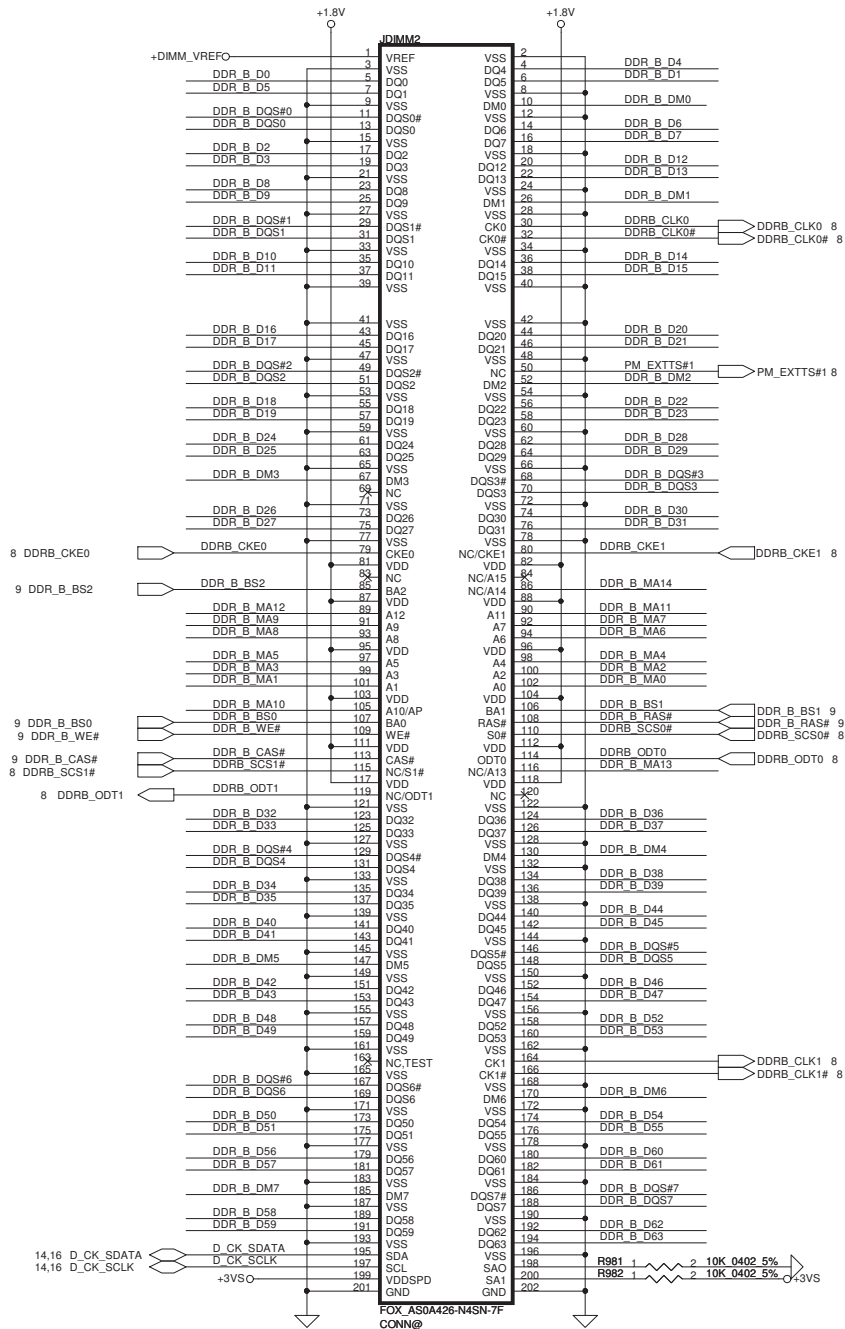


VSS

VSS NCTF

VSS SCB

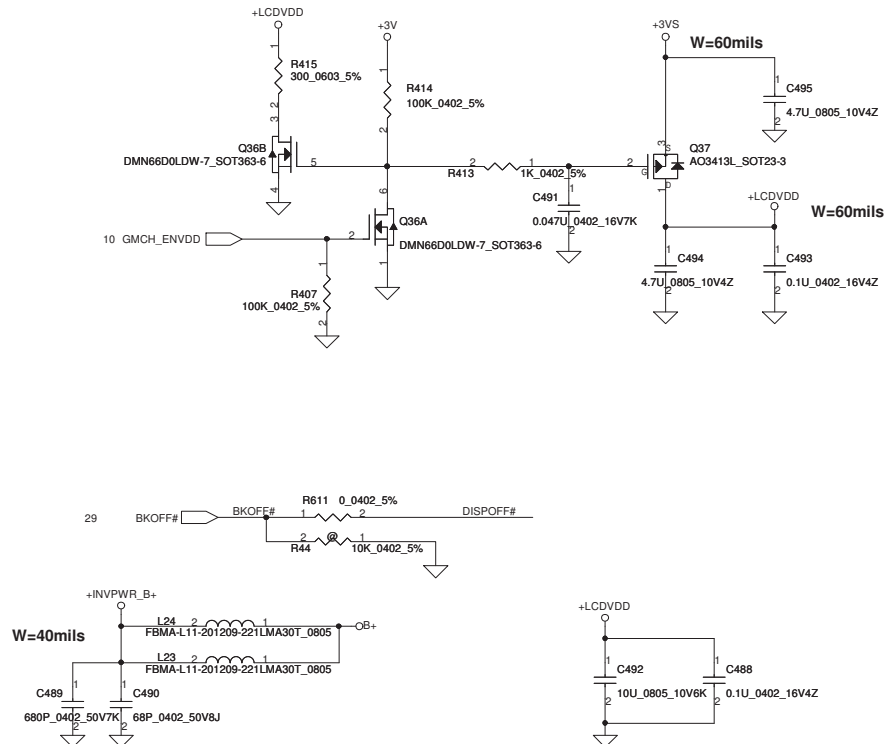
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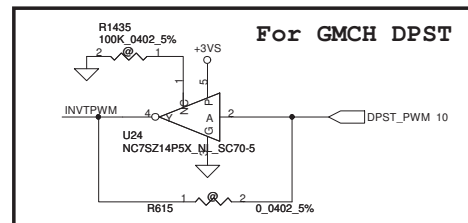
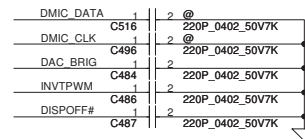
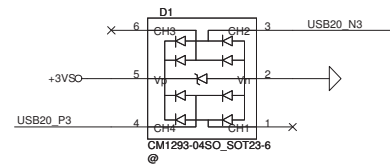
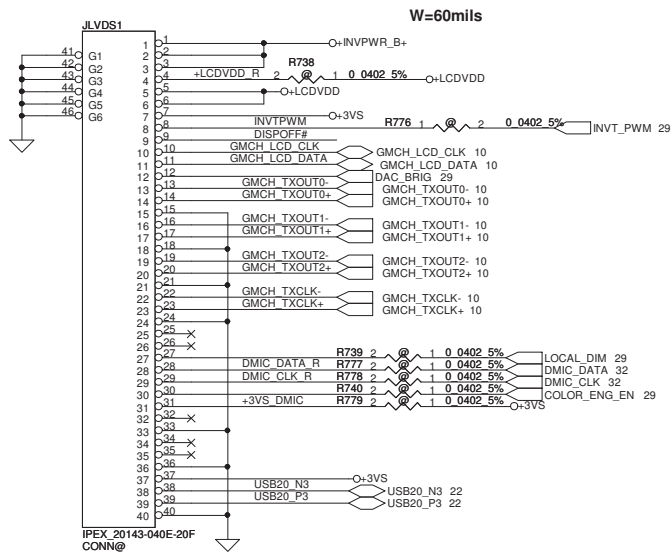
DIMM2 STD H:4mm (BOT)

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						Date:	Friday, August 06, 2010	1 Sheet 15 of 44

LCD POWER CIRCUIT

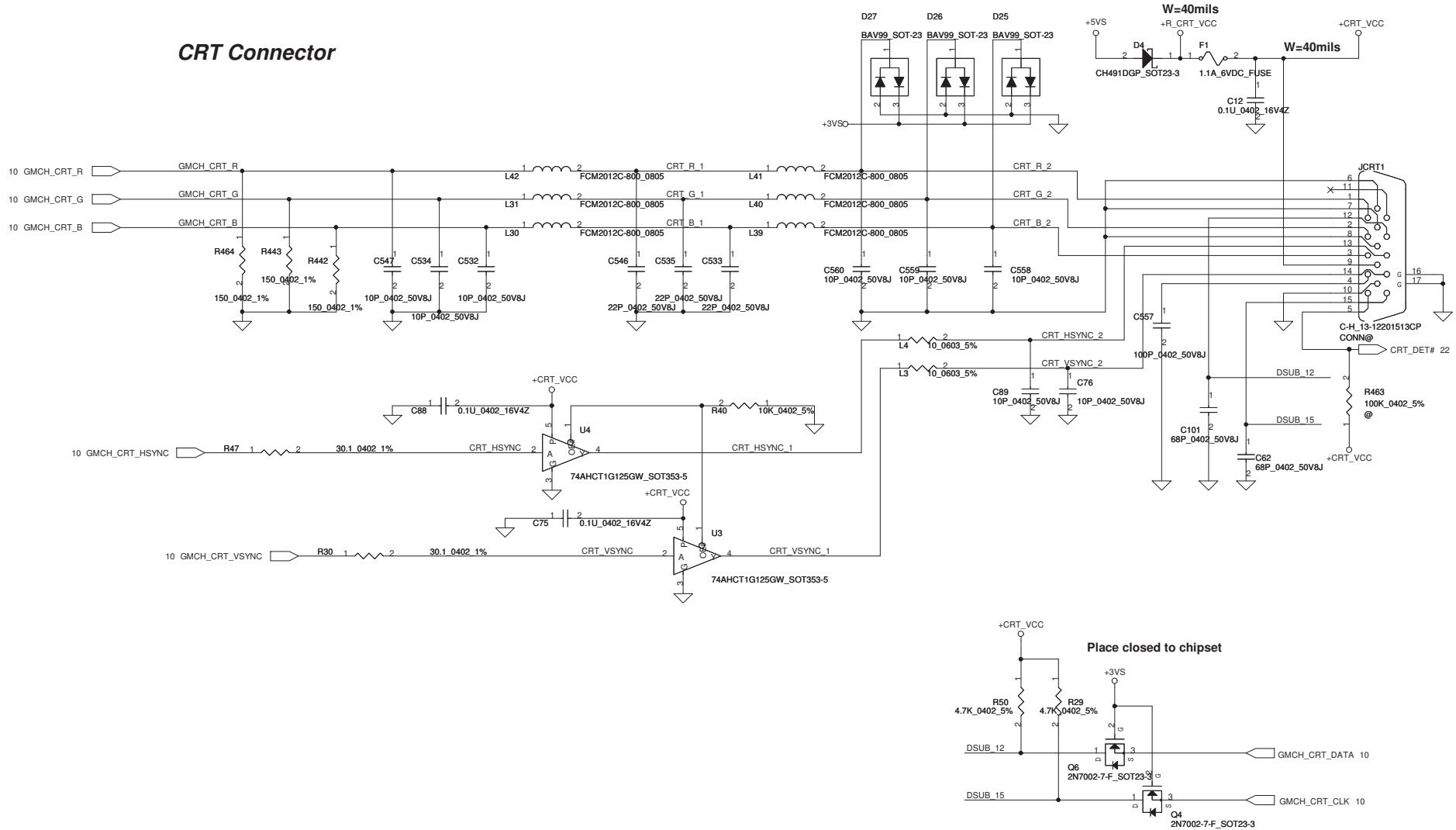


LCD/PANEL BD. Conn.

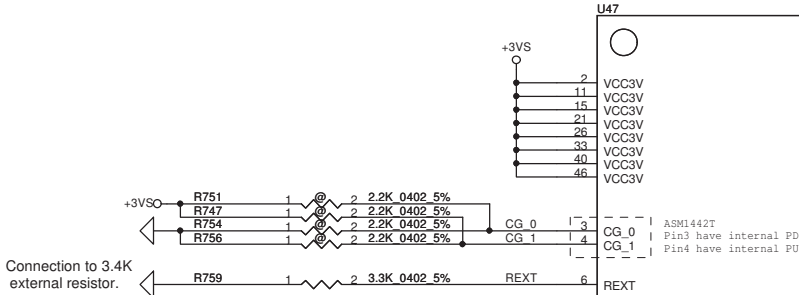
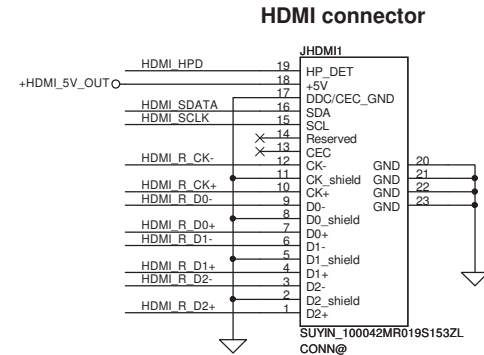
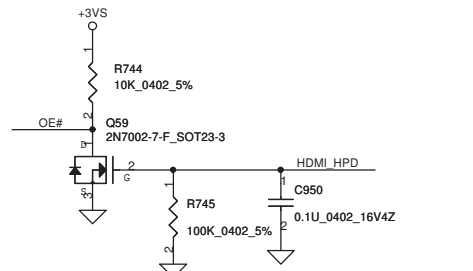
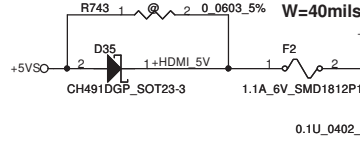
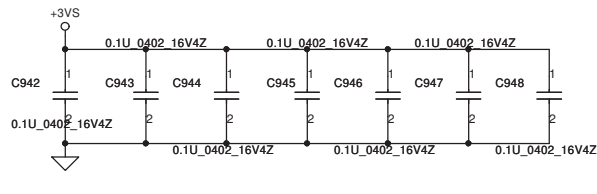


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				Customer Part Number		
				Date	Friday, August 06, 2010	Sheet 17 of 44
				PEW52 M/B LA-6634P Schematic		

CRT Connector

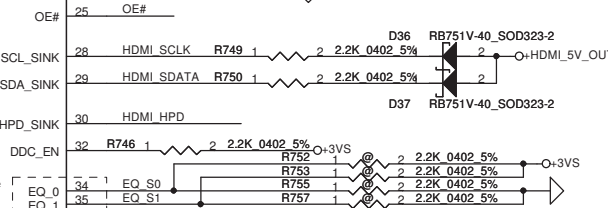


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						Document Number		PEW52 M/B LA-6634P Schematic		Rev	
						Date		Friday, August 06, 2010		Sheet 18 of 44	



CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

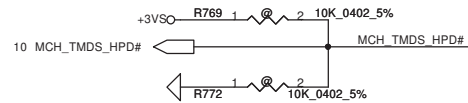
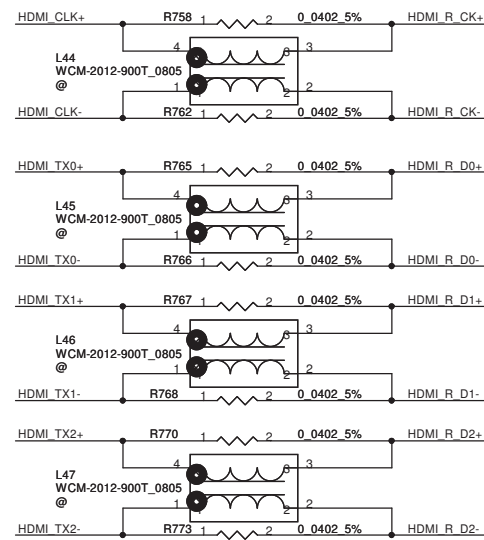
HDMI TX2+	13	OUT_D4+
HDMI TX2-	14	OUT_D4-
HDMI TX1+	16	OUT_D3+
HDMI TX1-	17	OUT_D3-
HDMI CLK+	19	OUT_D2+
HDMI CLK-	20	OUT_D2-
HDMI TX0+	22	OUT_D1+
HDMI TX0-	23	OUT_D1-



EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

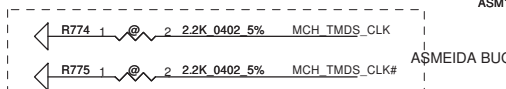
IN_D4+	48	MCH_TMDS_DATA2	10
IN_D4-	47	MCH_TMDS_DATA2#	10
IN_D3+	45	MCH_TMDS_DATA1	10
IN_D3-	44	MCH_TMDS_DATA1#	10
IN_D2+	42	MCH_TMDS_CLK	10
IN_D2-	41	MCH_TMDS_CLK#	10
IN_D1+	39	MCH_TMDS_DATA0	10
IN_D1-	38	MCH_TMDS_DATA0#	10

SM070001310 400ma 90ohm@100mhz DCR 0.3

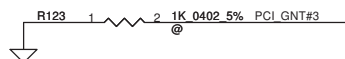
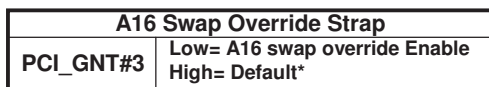
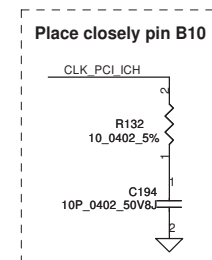
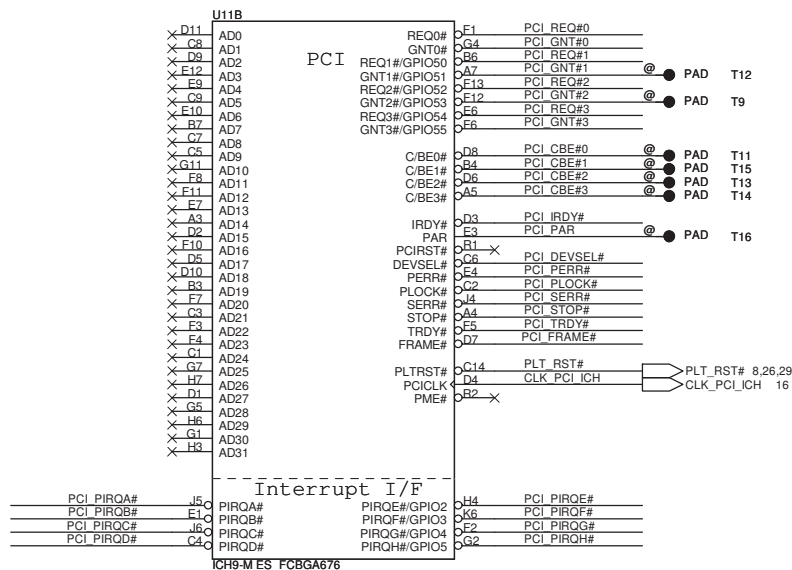
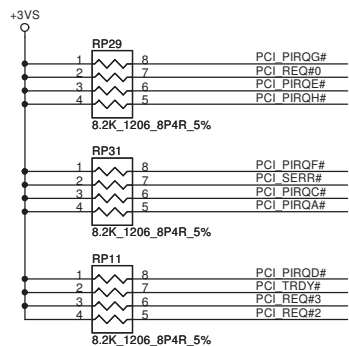


ASM1442T PN: SA00003BB00

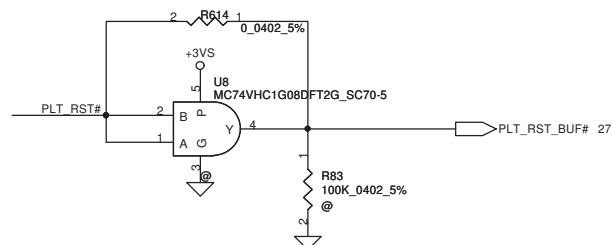
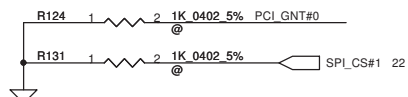
ASM1442T_QFN48_7X7



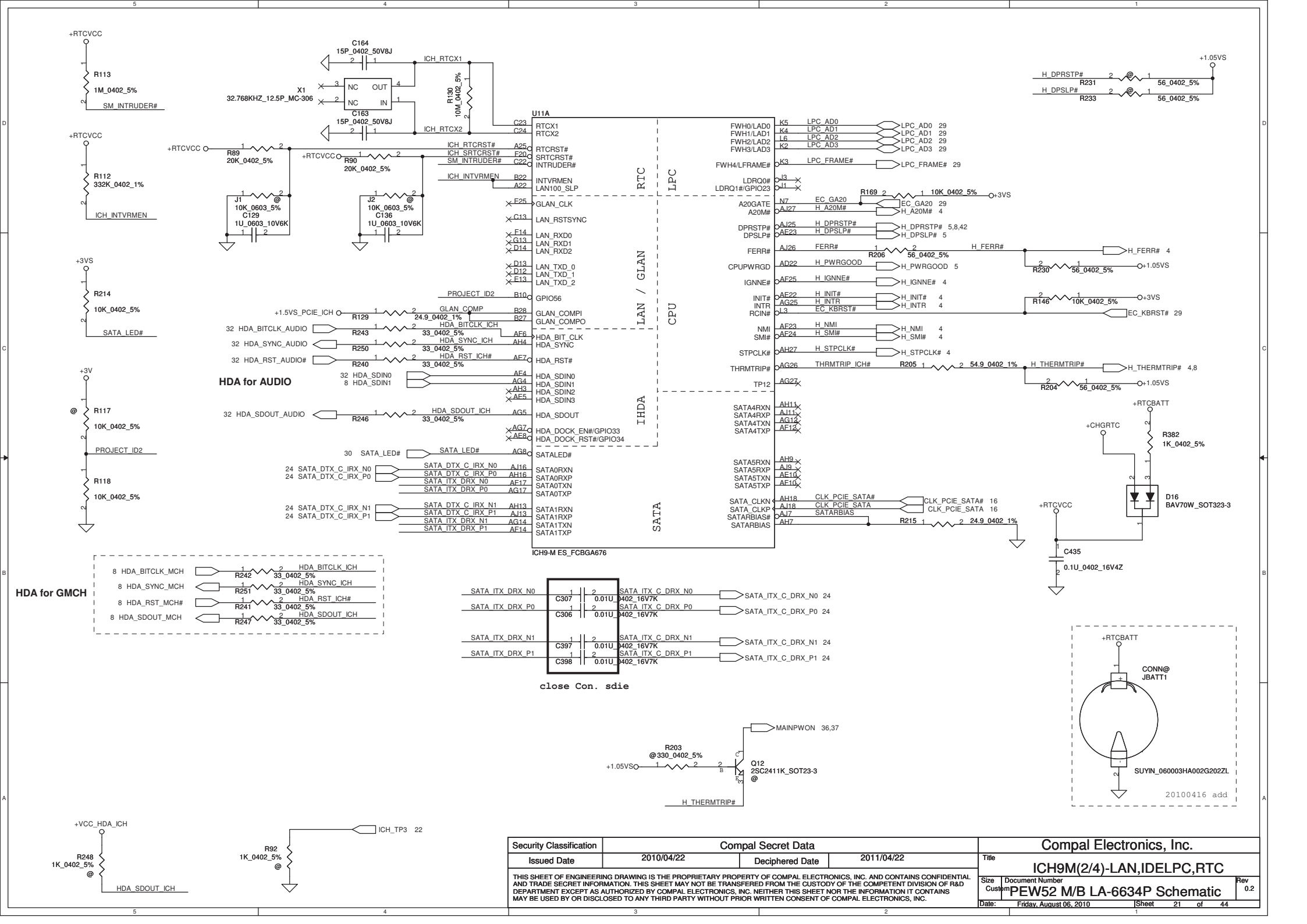
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Size	Document Number	PEW52 M/B LA-6634P Schematic		Rev	0.2
Date:	Friday, August 06, 2010	Sheet	19	of	44

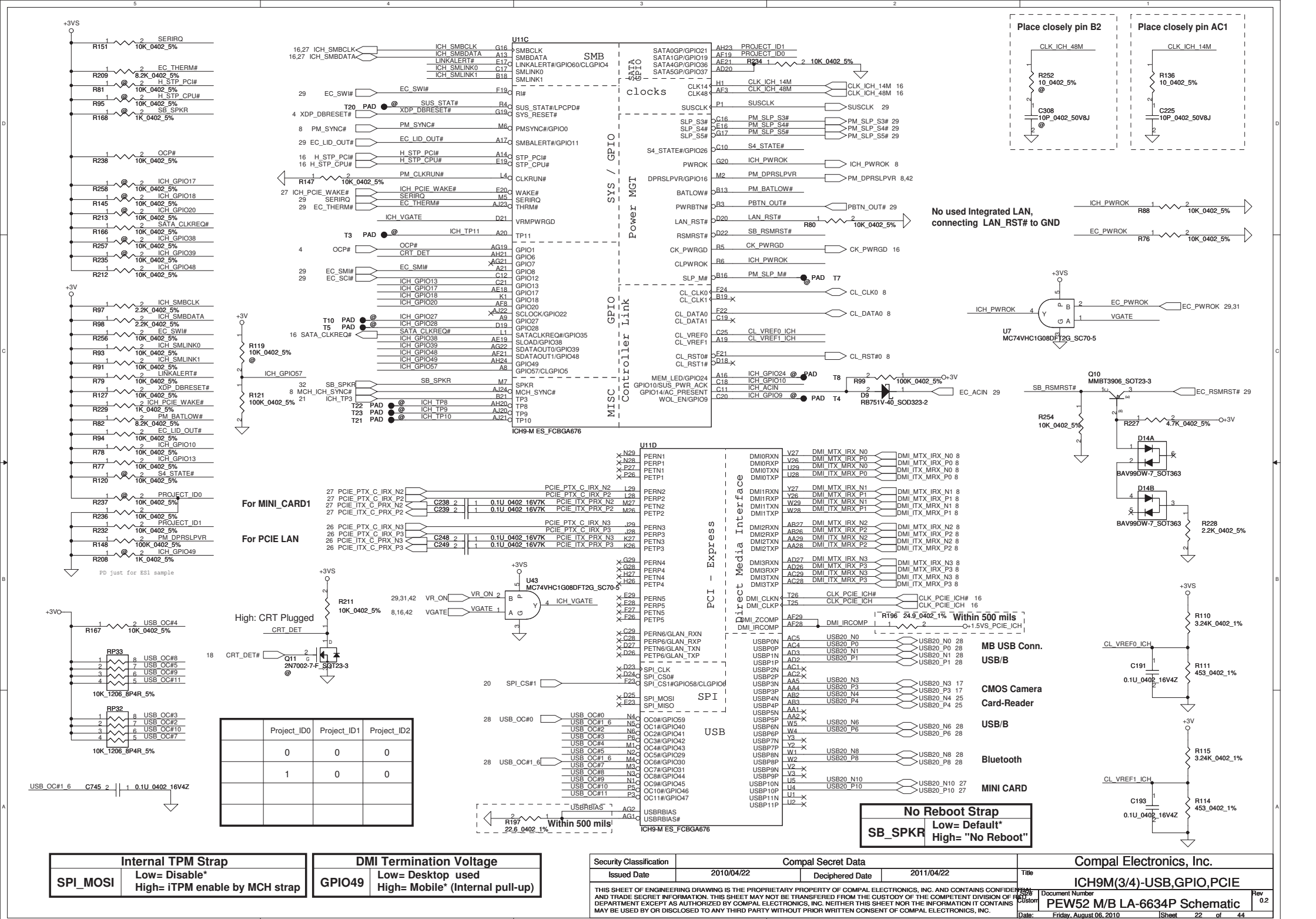


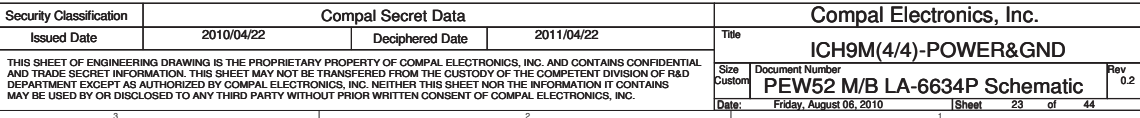
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

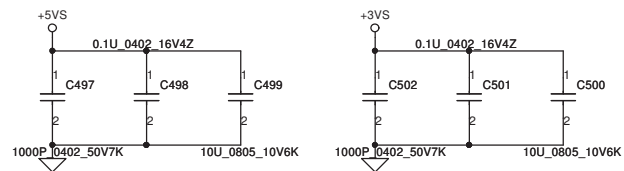


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				Size	Document Number		Rev		
				PEW52 M/B LA-6634P Schematic					0.2
				Date:	Friday, August 06, 2010		Sheet	20	of 44

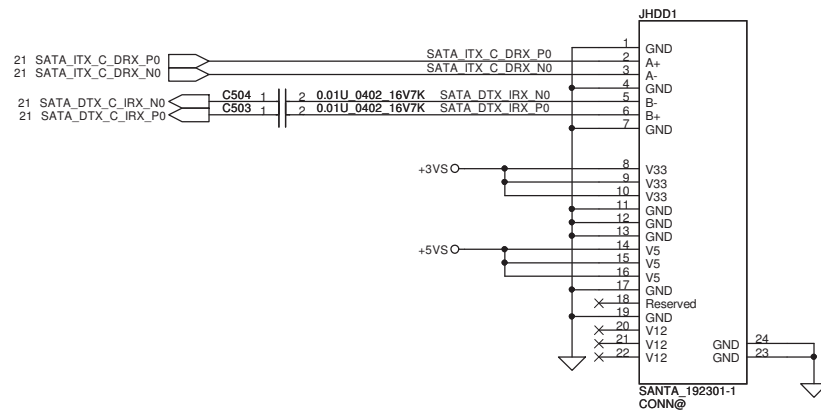




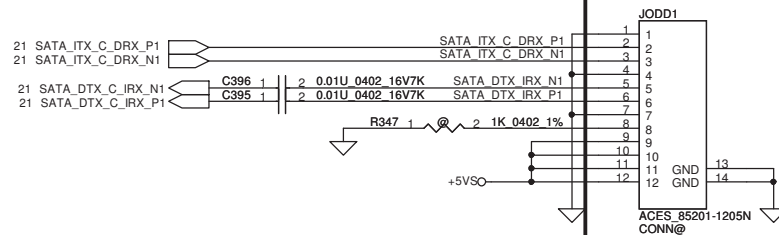




SATA HDD Conn.

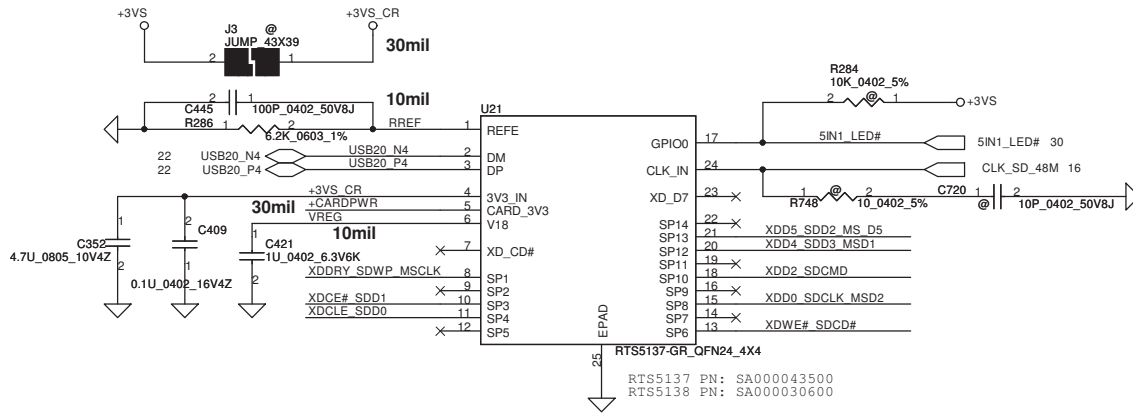


SATA ODD Conn. LS-6583

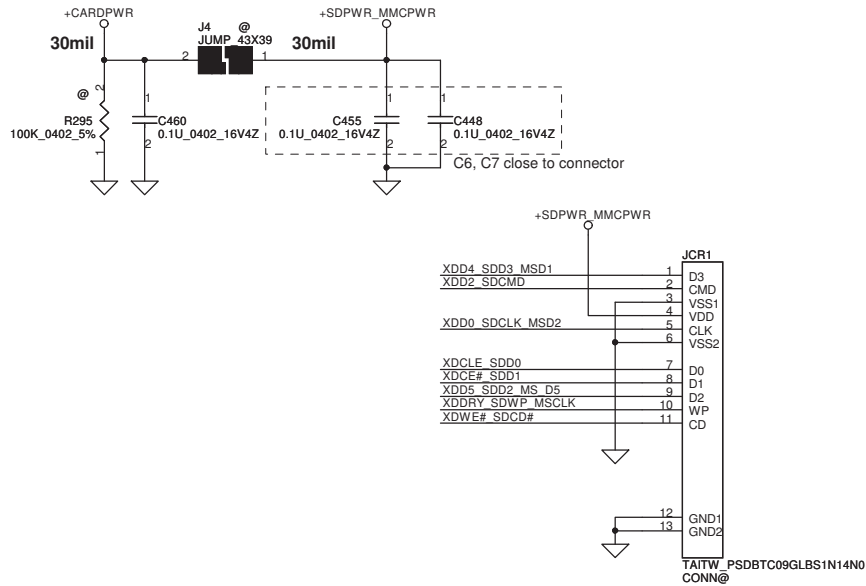


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Size	Custom	Document Number	PEW52 M/B LA-6634P Schematic	Rev	0.2
Date:	Friday, August 06, 2010	Sheet	24	of	44

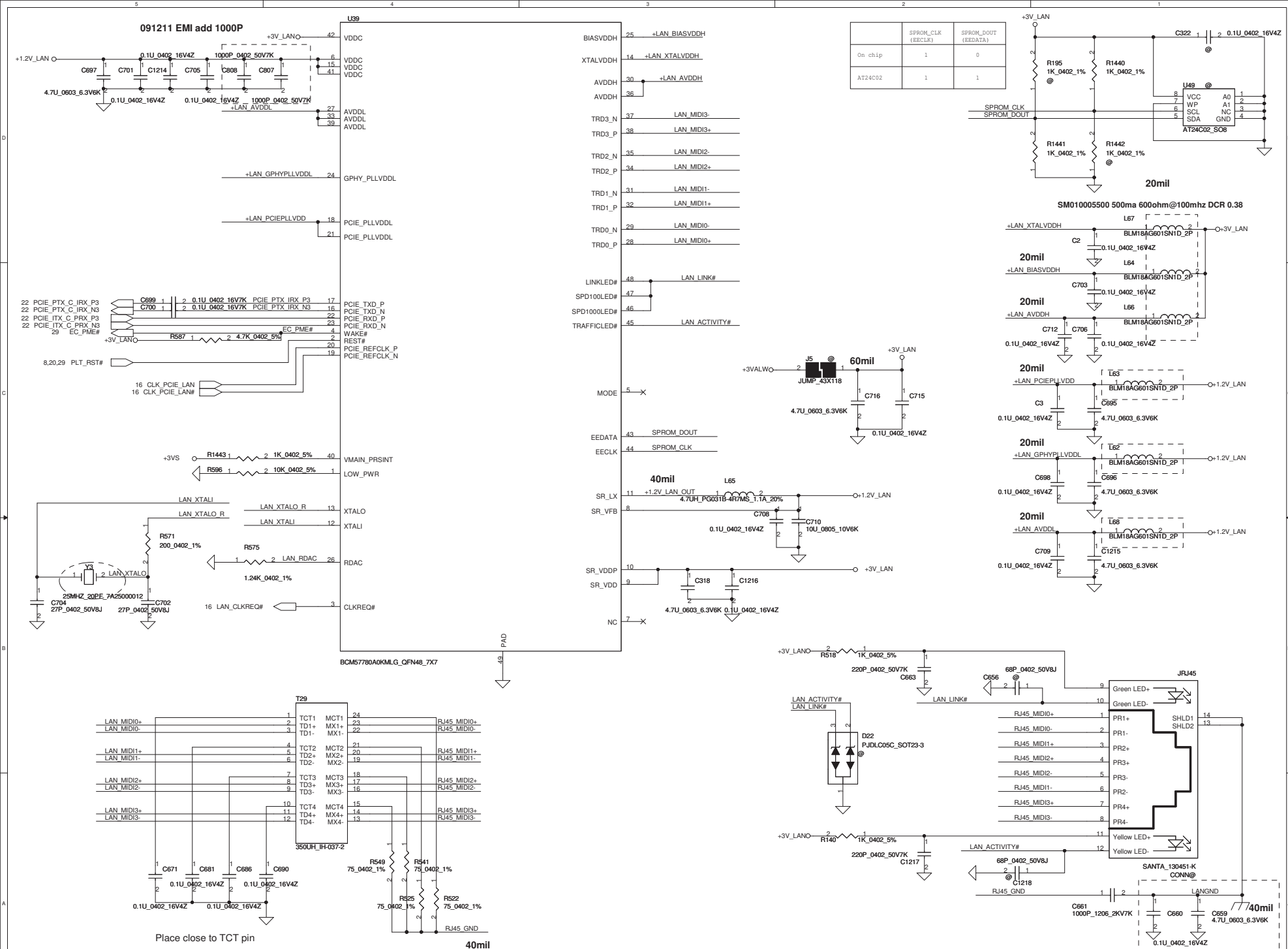
Card Reader RTS5138 / RTS5137
(only SD+MMC function)



Card Reader Connector

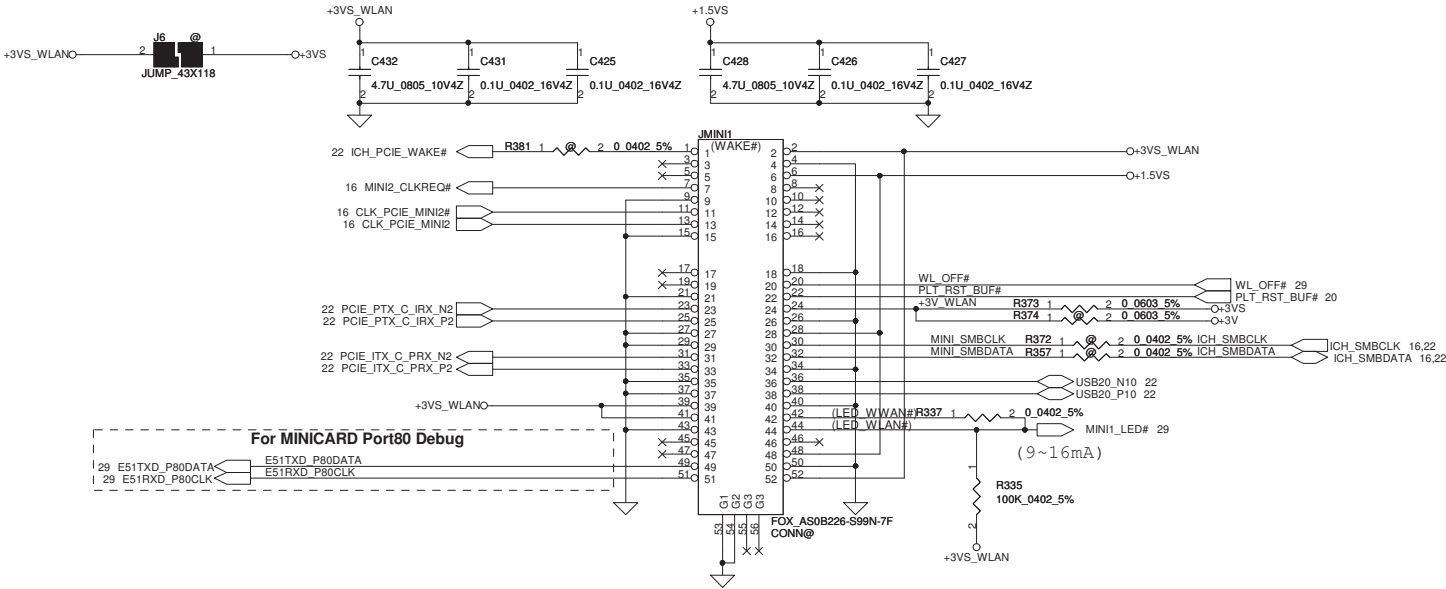


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				Customer	0.2
				Date: Friday, August 06, 2010 Sheet 25 of 44	

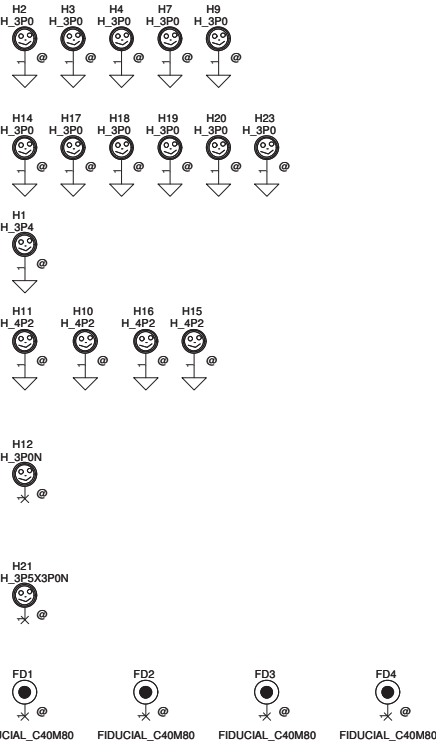


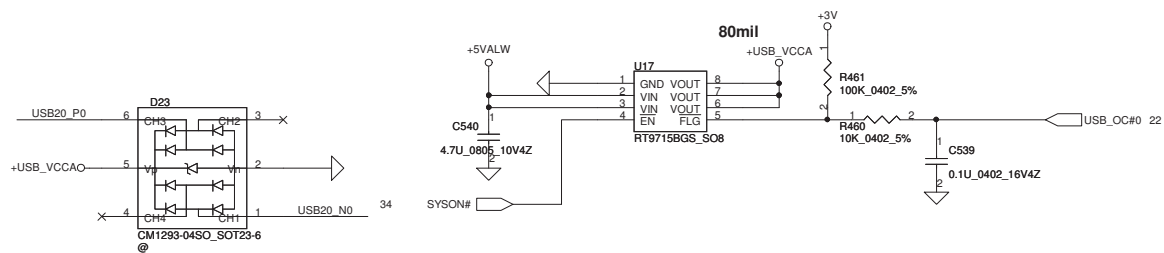
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Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title	Broadcom BCM57780
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For Wireless LAN

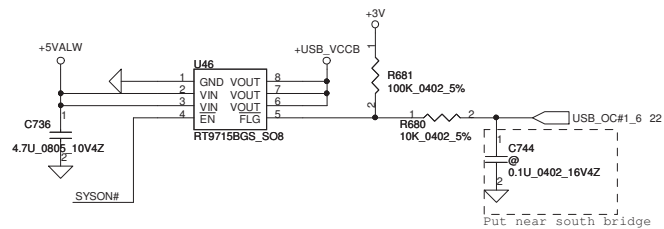
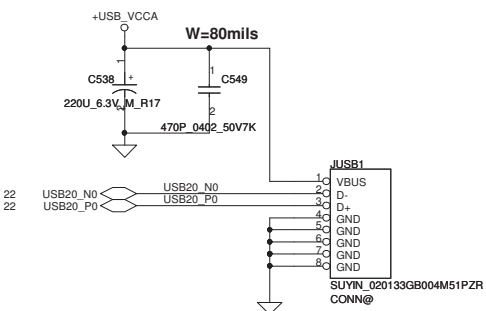


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	
+3VS	1000	750	Normal
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

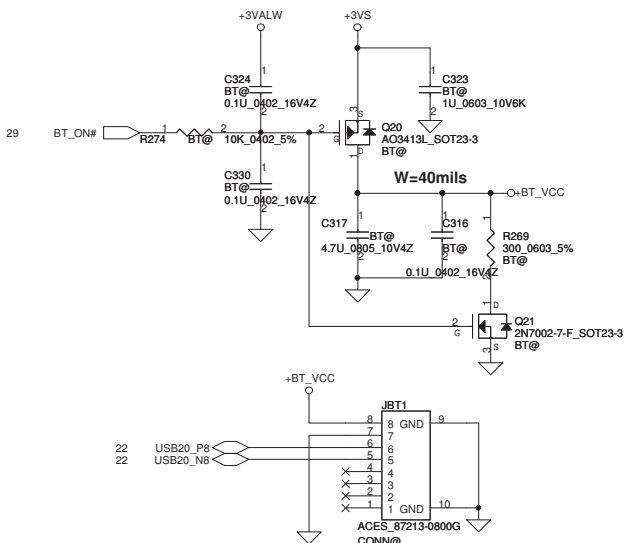




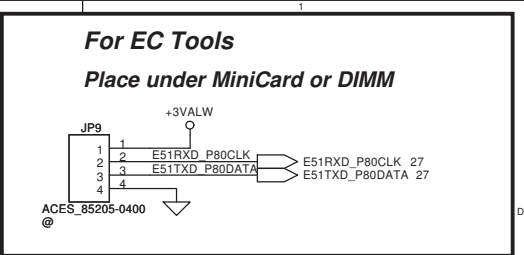
USB Conn.
(Port 0)

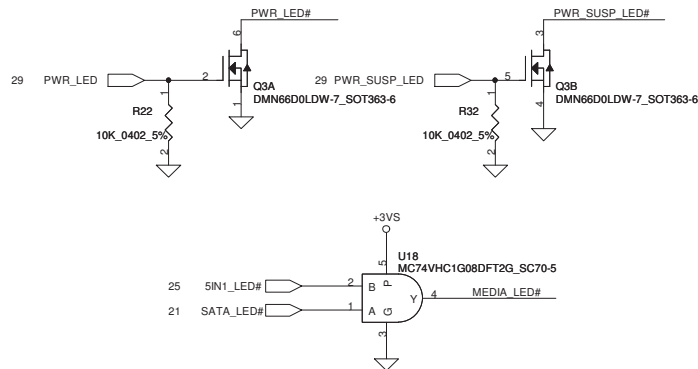
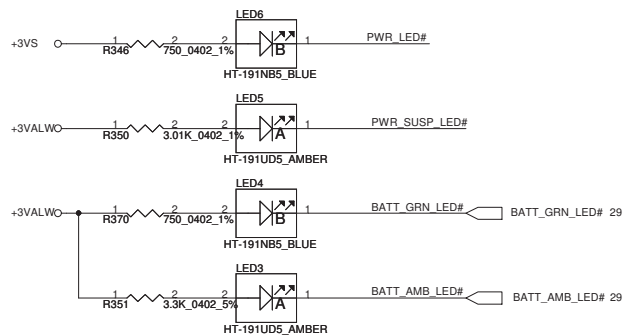
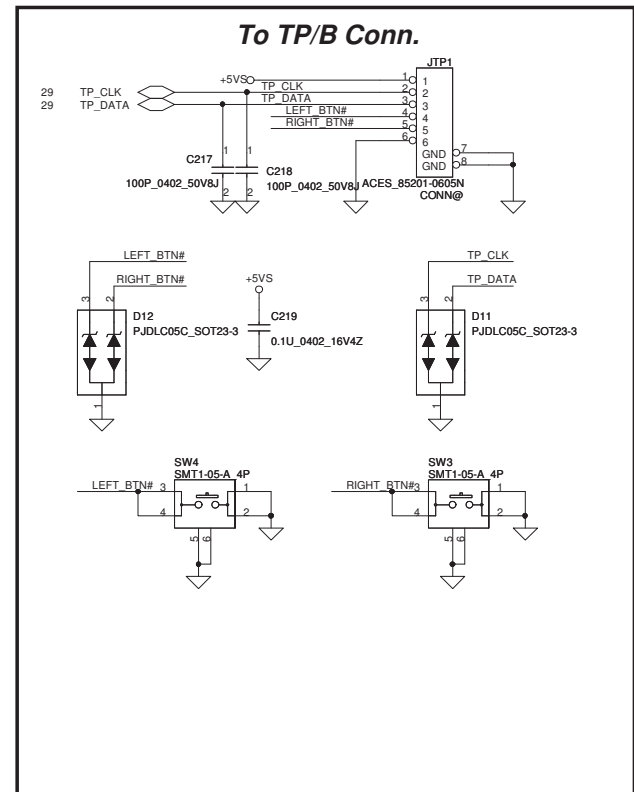
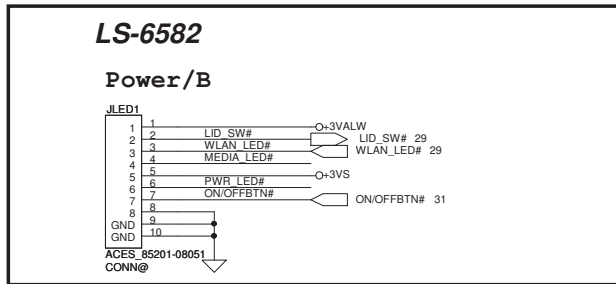
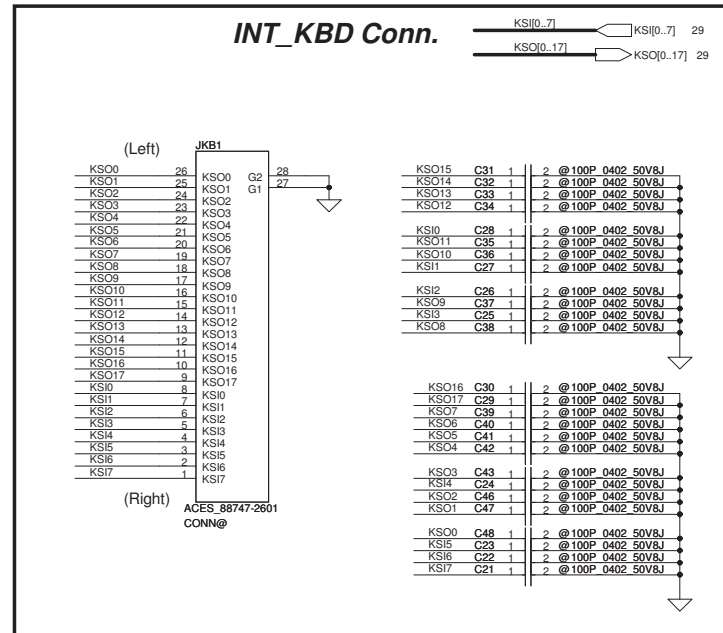
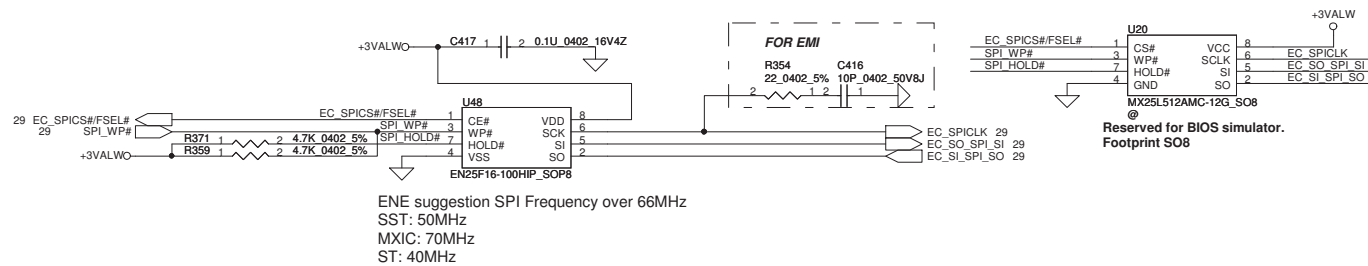


Bluetooth Conn.



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				Date	Friday, August 06, 2010
				Sheet	28 of 44
				Rev	0.2

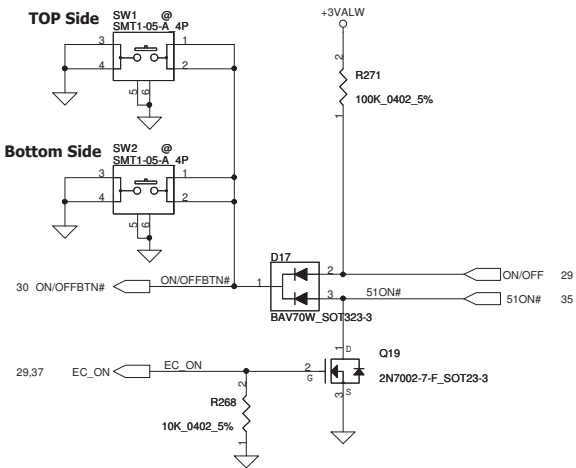




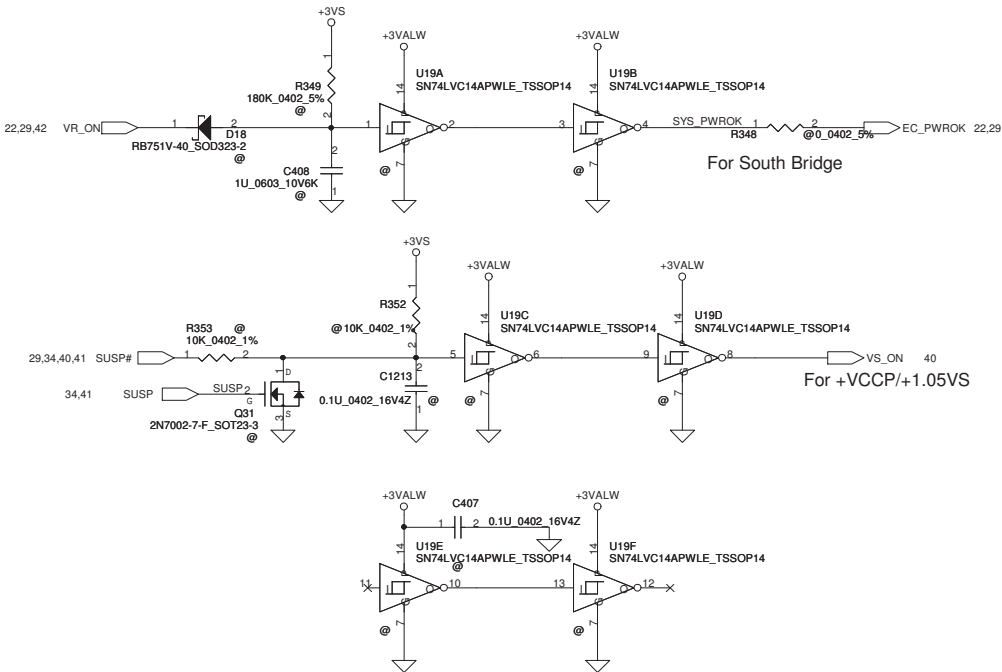
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/04/22				Deciphered Date			
2011/04/22				2011/04/22				Title			
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Date: Friday, August 06, 2010				Sheet 30 of 44				Rev 0.2			

Power Button

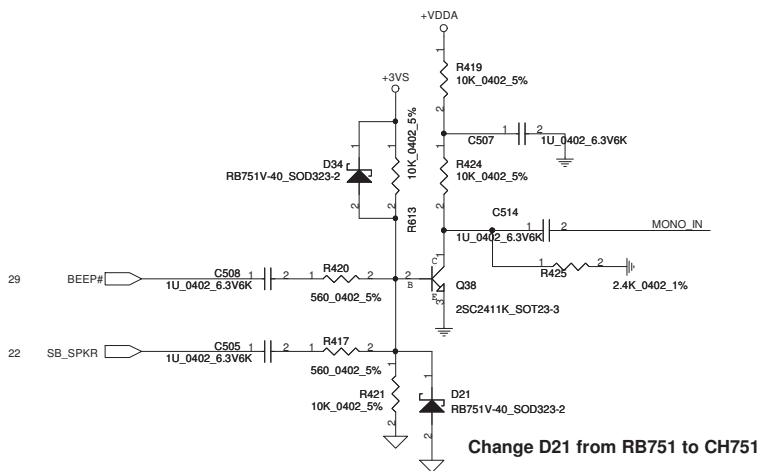
ON/OFF switch



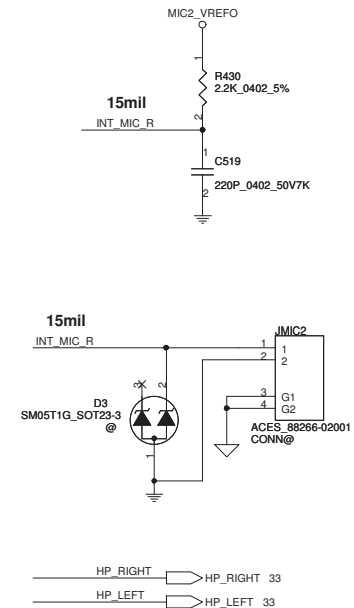
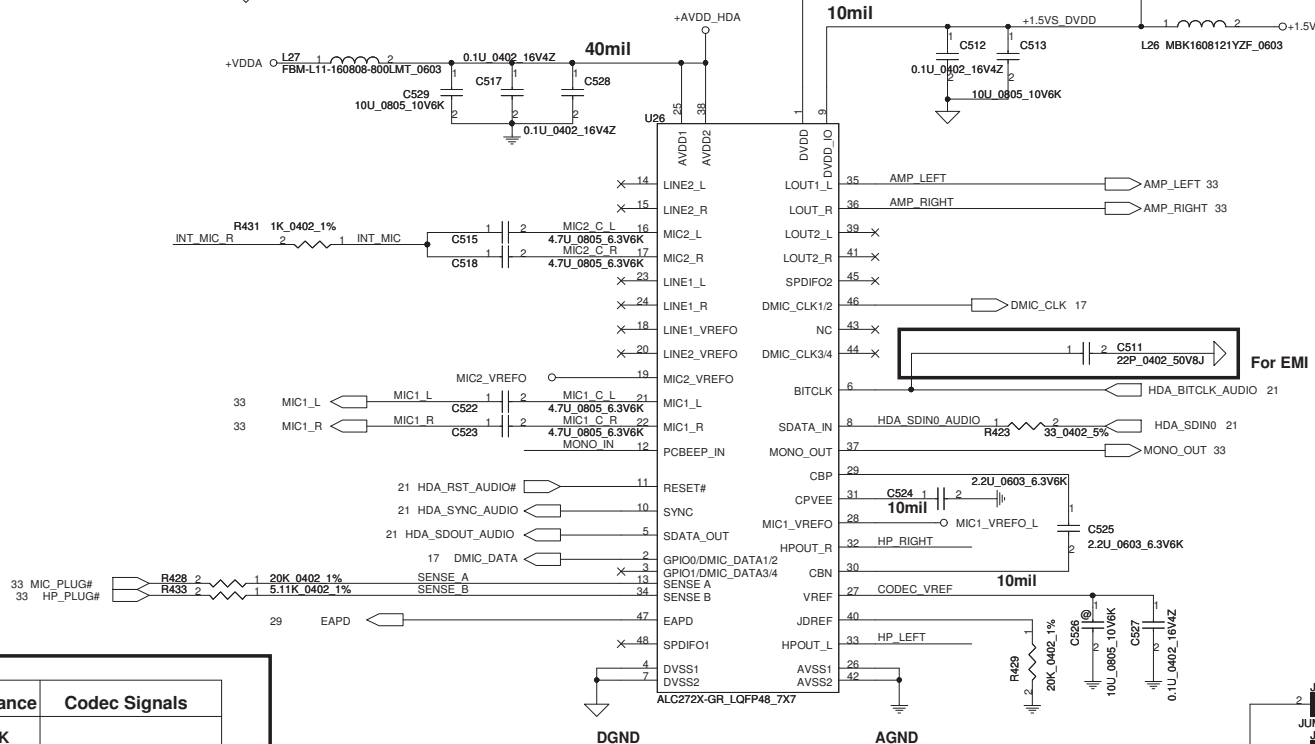
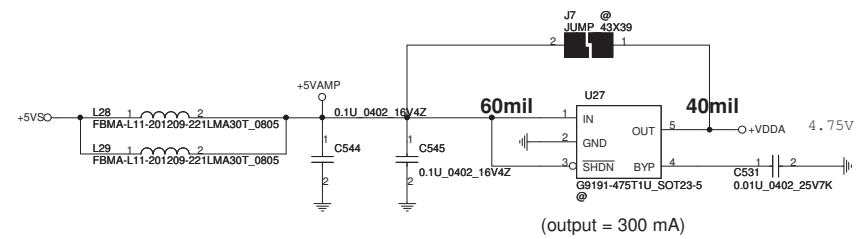
Power ON Circuit



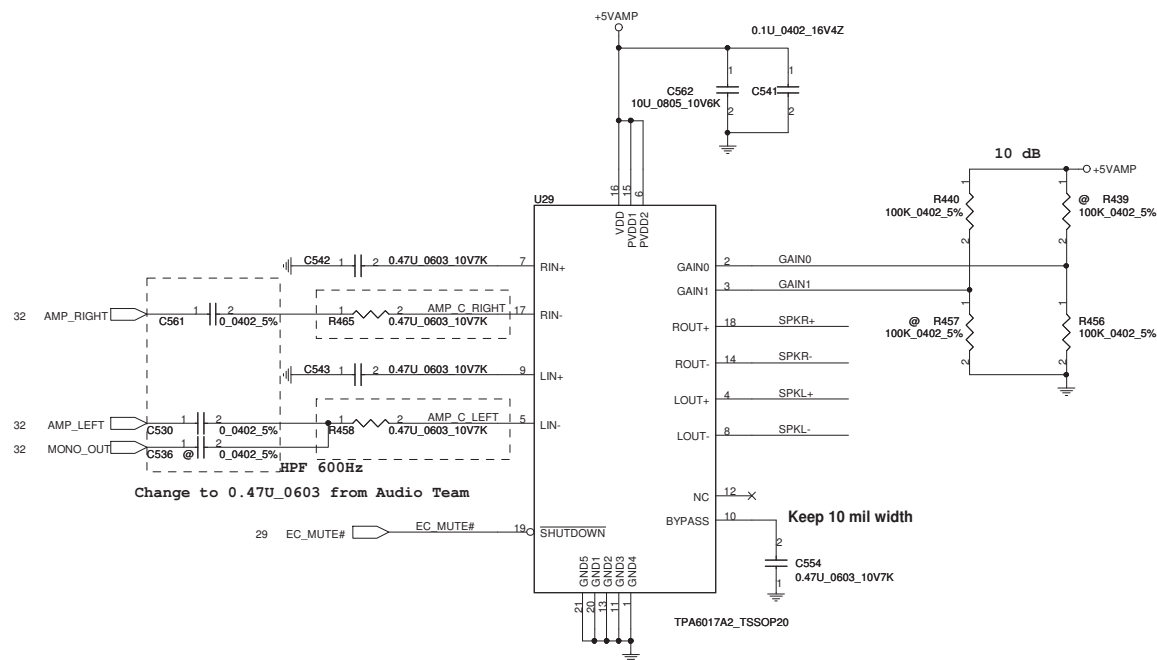
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2010/04/22		Deciphered Date		2011/04/22		Title			
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								Document Number		Rev	
								PEW52 M/B LA-6634P Schematic		0.2	
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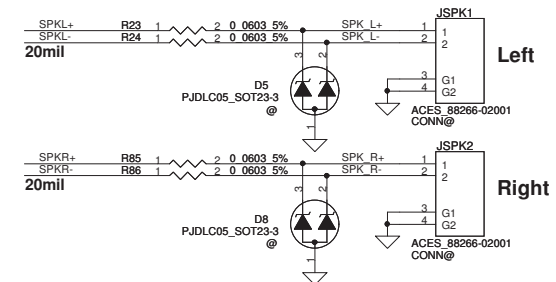
HD Audio Codec



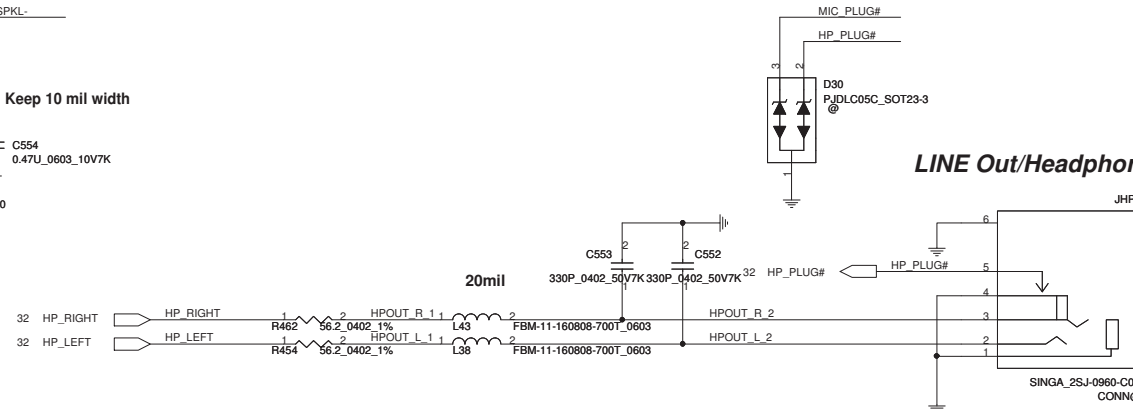
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/04/22				Title			
Deciphered Date				2011/04/22				HD Audio Codec ALC272X			
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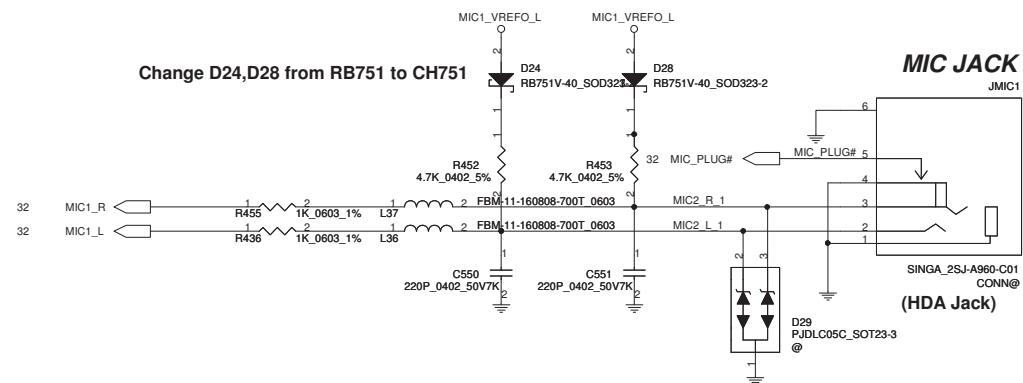
Int. Speaker Conn.



LINE Out/Headphone Out

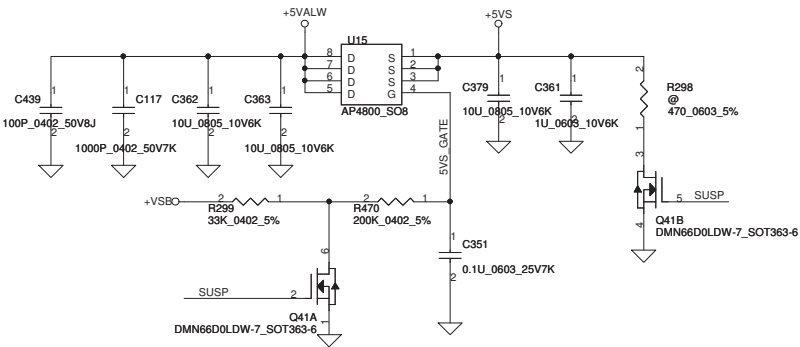


Change D24,D28 from RB751 to CH751

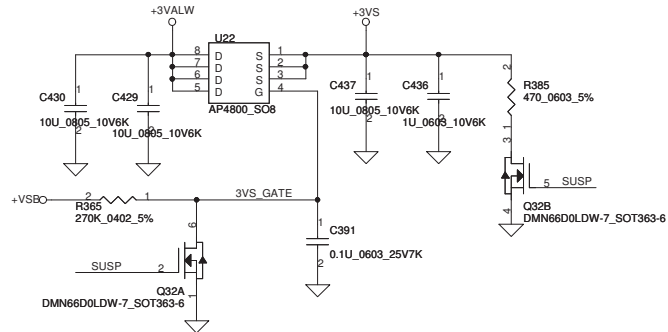


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								Document Number		PEW52 M/B LA-6634P Schematic				Rev 0.2	
								Date		Friday, August 06, 2010		Sheet 33 of 44			

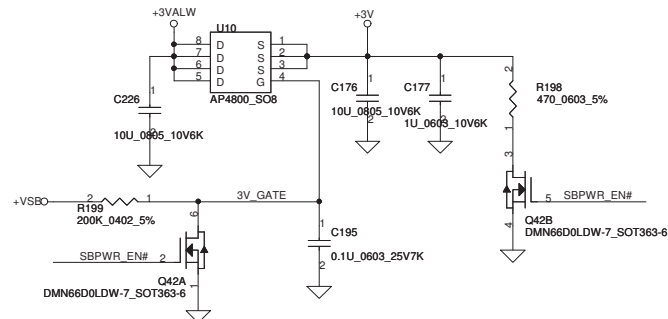
+5VALW TO +5VS



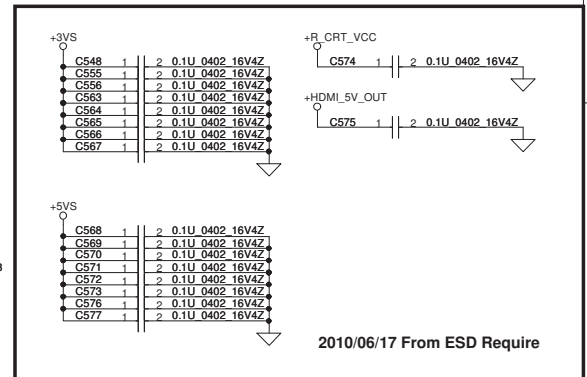
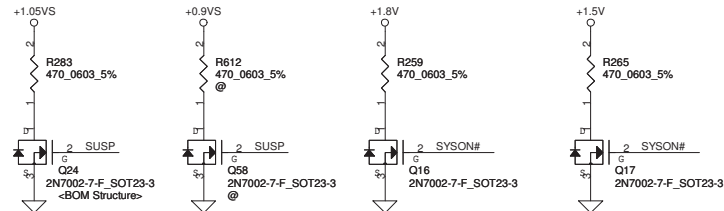
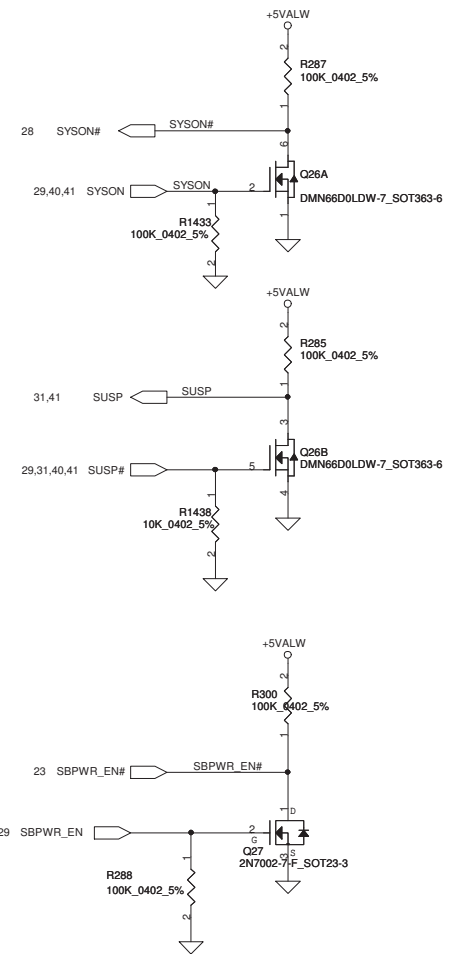
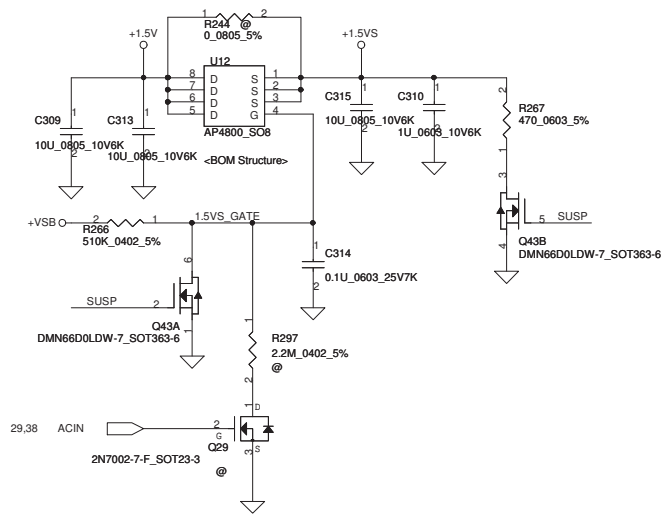
+3VALW TO +3VS



+3VALW TO +3V_SB(ICH8M AUX Power)

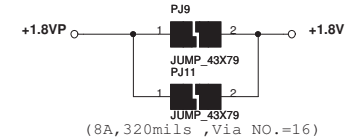
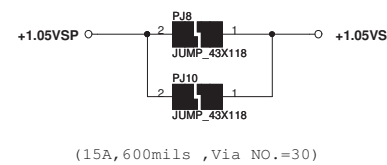
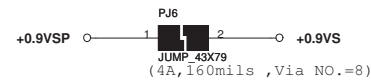
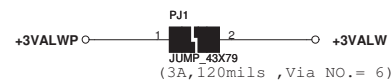
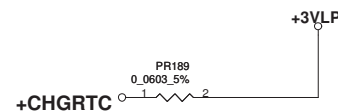
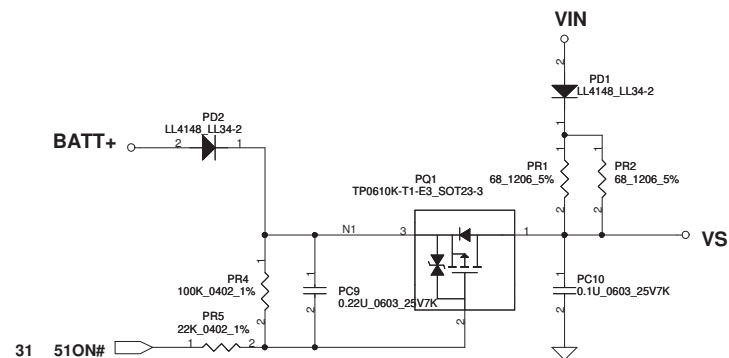
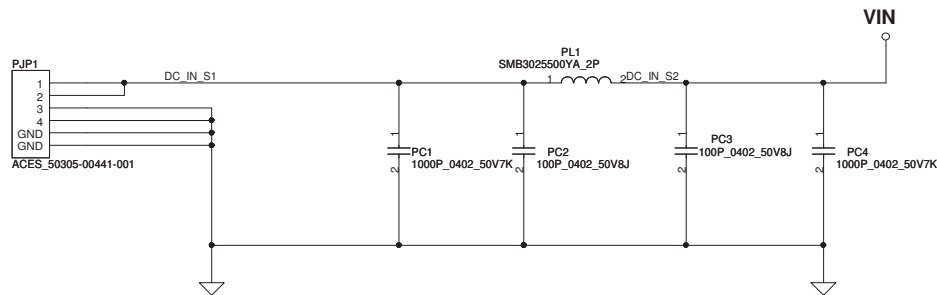


+1.5V to +1.5VS

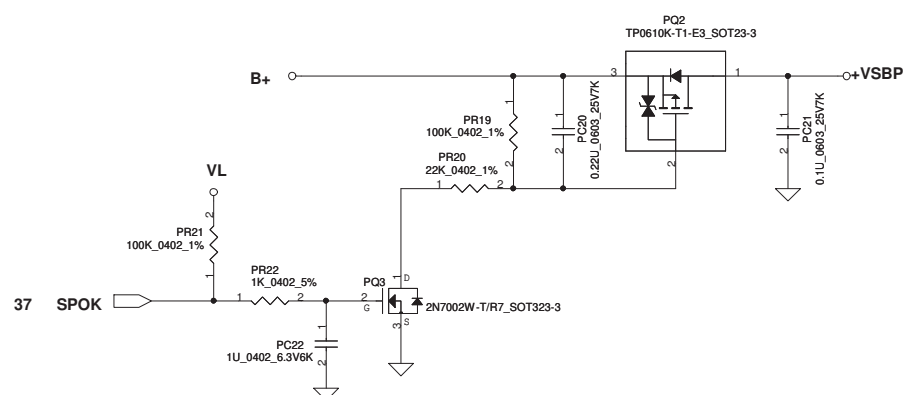
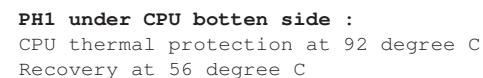


2010/06/17 From ESD Require

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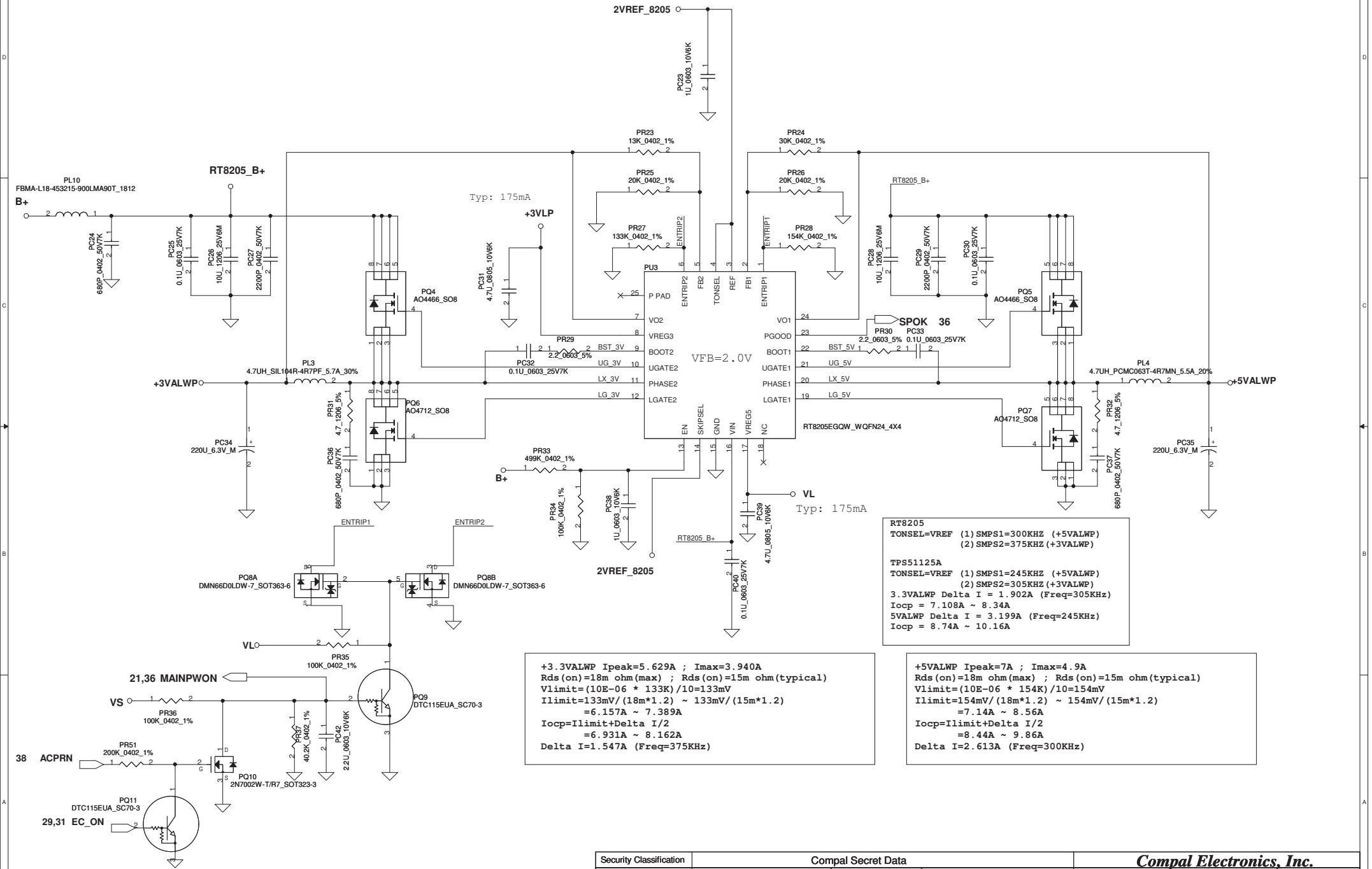


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Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO

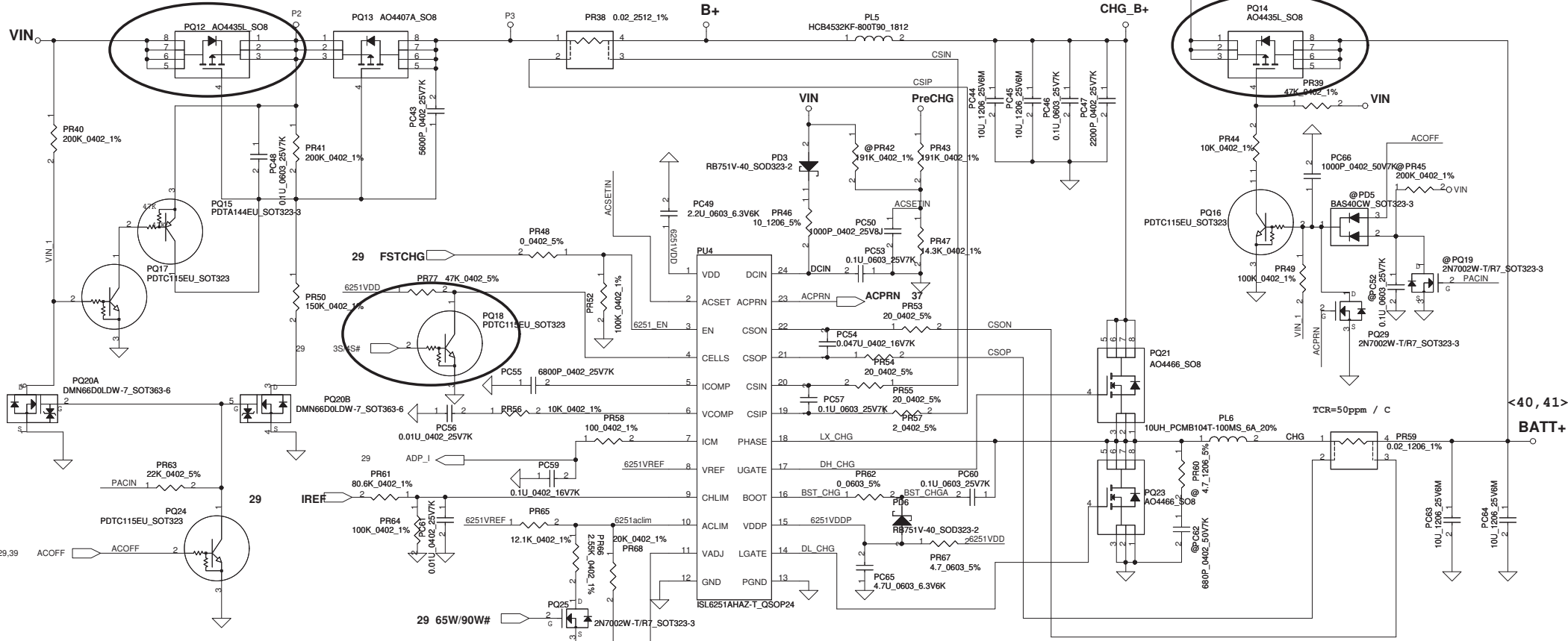


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		Size	Document Number			Rev
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Iada=0~4.74A (90W/19V=4.736A)
Iada=0~3.42A (90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



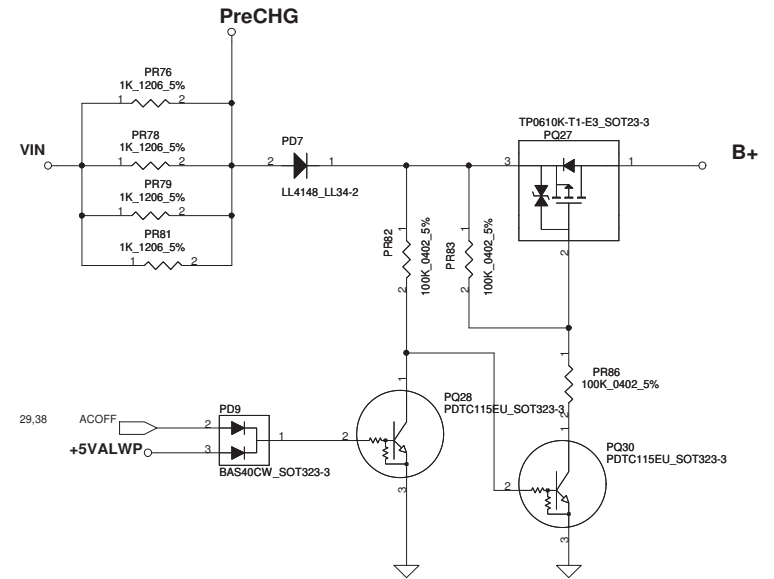
CP mode
Iinput=(1/0.02) (0.05*Vac1m/2.39+0.05)
where Vac1m=1.502V, Iinput=4.07A

CC=0.6~4.48A
IREF=0.7224*Icharge
Ki=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Icharge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.384*Iref
Iref=0.7224*Icharge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K/(15.4K+3K)=11.372K
r=514K//514K//31.6K=28.14K
Vce1l=0.175*Vadj+3.99V
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r+514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vce1l+0.175))*Kv=(4.2-(4.2+0.175))*Kv
Kv=Vref*(R/(R+514K))=0.052
Kv=9.451

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V



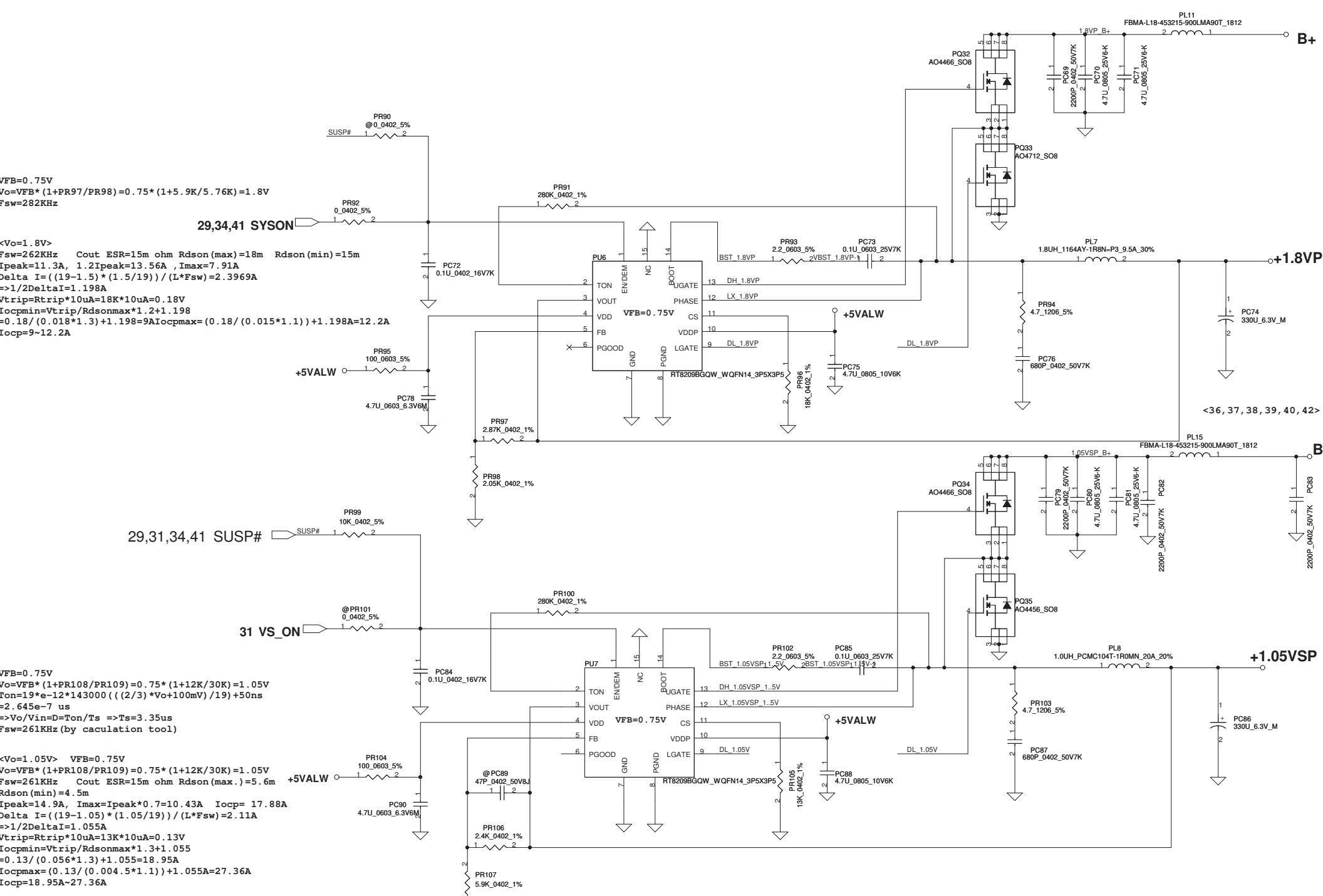
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Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title	PRECHARGE	
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VFB=0.75V
Vo=VFB*(1+PR97/PR98)=0.75*(1+5.9K/5.76K)=1.8V
Fsw=282KHz

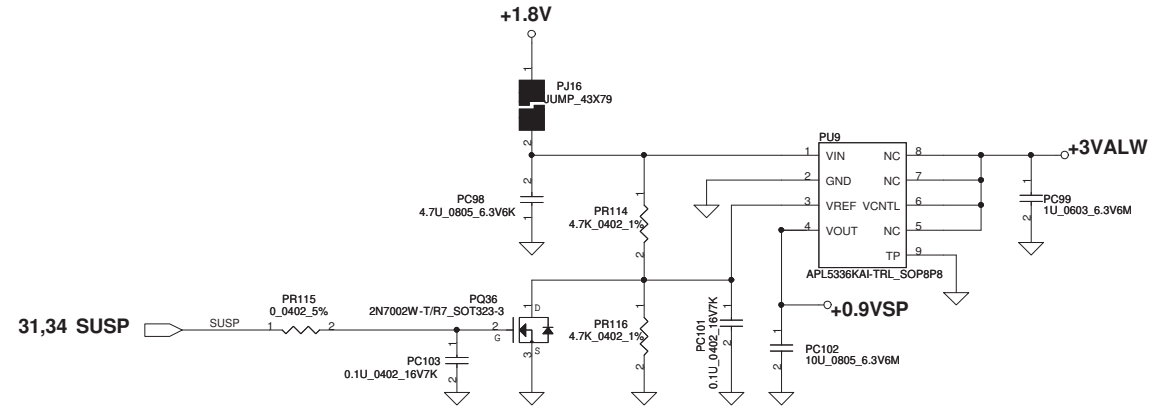
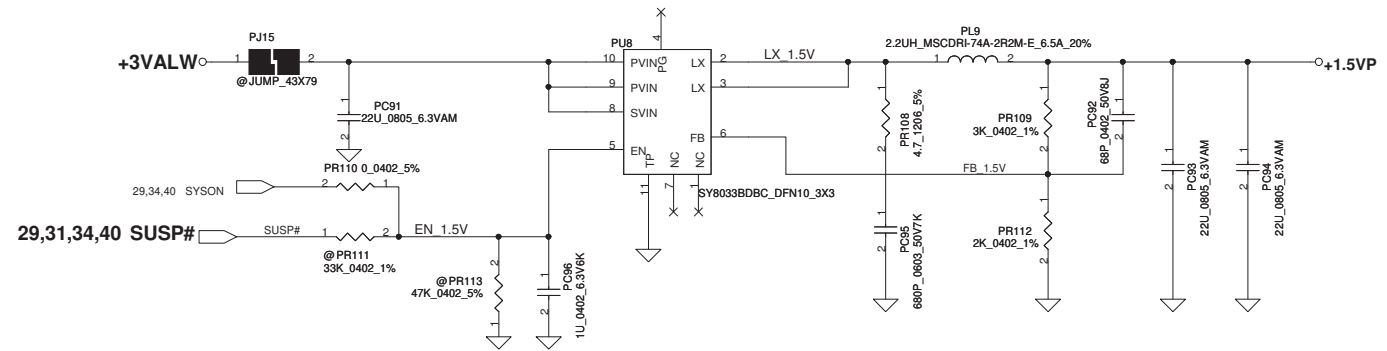
<Vo=1.8V>
Fsw=262KHz Cout ESR=15m ohm Rdson(max)=18m Rdson(min)=15m
Ipeak=11.3A, 1.2Ipeak=13.56A, Imax=7.91A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=2.3969A
=>1/2DeltaI=1.198A
Vtrip=Rtrip*10uA=18K*10uA=0.18V
Iocpmin=Vtrip/Rdsonmax*1.2+1.198
=0.18/(0.018*1.3)+1.198=9AIocpmax=(0.18/(0.015*1.1))+1.198A=12.2A
Iocp=9~12.2A

VFB=0.75V
Vo=VFB*(1+PR108/PR109)=0.75*(1+12K/30K)=1.05V
Ton=19uA-12*143000*((2/3)*Vo/100mV)/19)+50ns
=2.645e-7 us
=>Vo/Vin=D=Ton/Ts =>Ts=3.35us
Fsw=261KHz (by caculation tool)

<Vo=1.05V> VFB=0.75V
Vo=VFB*(1+PR108/PR109)=0.75*(1+12K/30K)=1.05V
Fsw=261KHz Cout ESR=15m ohm Rdson(max.)=5.6m
Rdson(min)=4.5m
Ipeak=14.9A, Imax=Ipeak*0.7=10.43A Iocp= 17.88A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=2.11A
=>1/2DeltaI=1.055A
Vtrip=Rtrip*10uA=13K*10uA=0.13V
Iocpmin=Vtrip/Rdsonmax*1.3+1.055
=0.13/(0.056*1.3)+1.055=18.95A
Iocpmax=(0.13/(0.004*1.1))+1.055A=27.36A
Iocp=18.95A~27.36A



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add 3S/4S pin function	add 4 cell battery	0.2	45	add PQ18 PDC115EU_SOT323 (SB301150200) and PR77 47K +-5% 0402 (SD028470280)	2010/06/11	EVT
2	ACSETIN net	ACSETIN net no connect	0.2	45		2010/06/11	EVT
3	1.5V enable	1.5V enable BOM error	0.2	45	add PR92 and delete PR90 0_0402_5% (SD028000080)	2010/06/11	EVT
4	EMI issue	add boost R and snubber	0.2	45	add 3/5V 1..05V/1.5V CPU sunbber		
5							
6							
7							
8							
9							
10							
11							
12							
13							
16							
17							

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A --> C Change List

20100806 Update Revision to 0.2

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