

Compal confidential

Schematics Document

Mobile P4 uFCBGA/uFCPGA with INTEL
MONTARA-GML/ICH4-M core logic

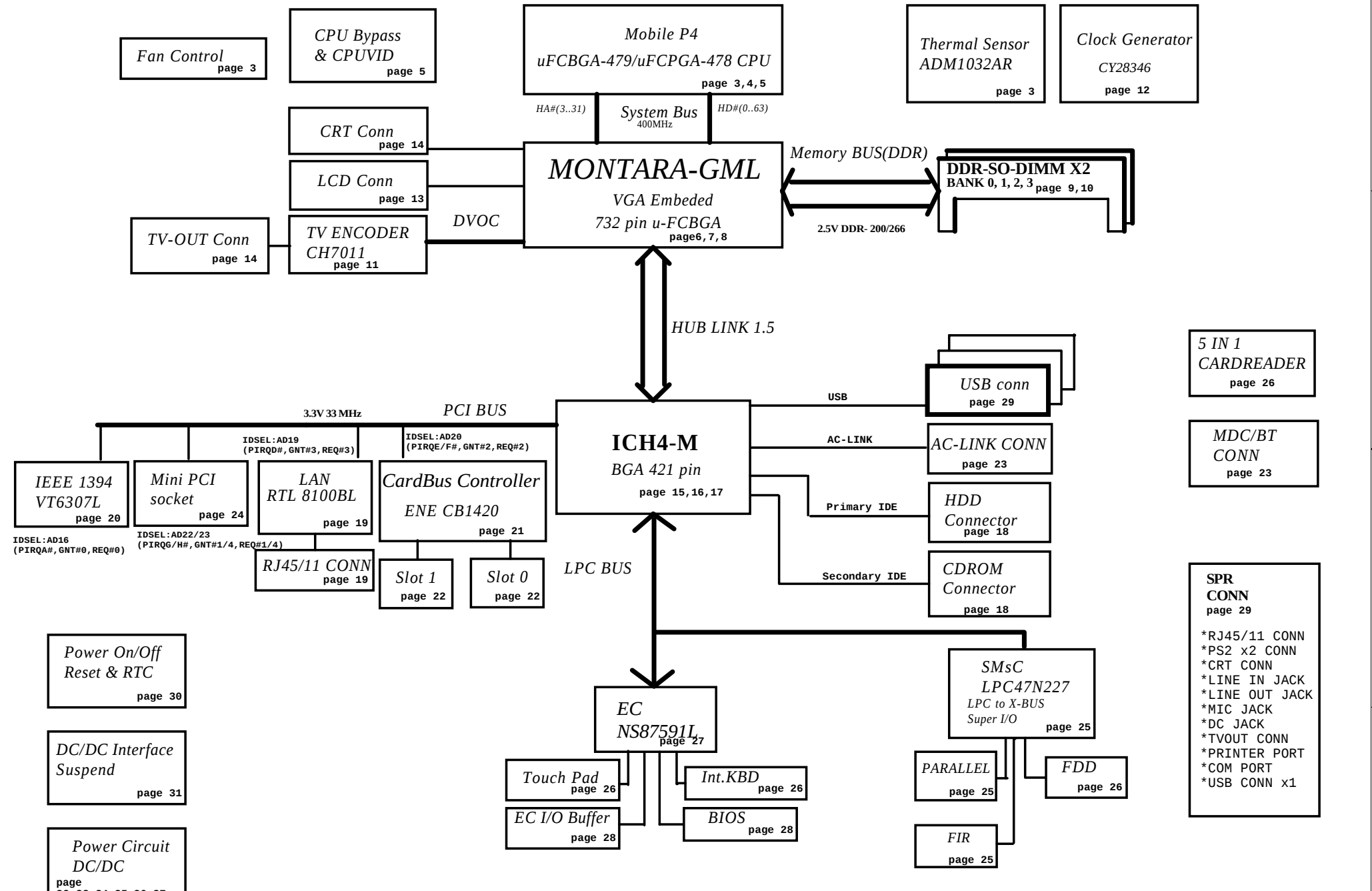
2002-02-10

REV:1.0

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Title			
SCHEMATIC, M/B LA-1571			
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	401238		1A
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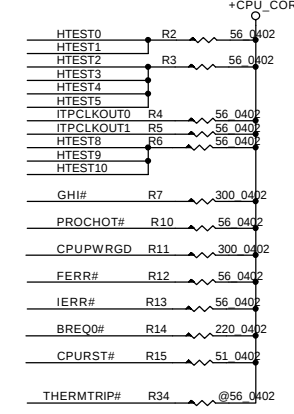
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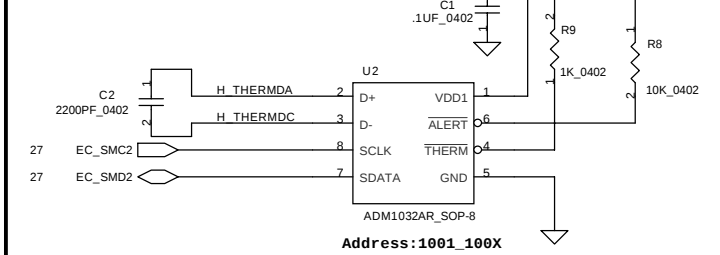
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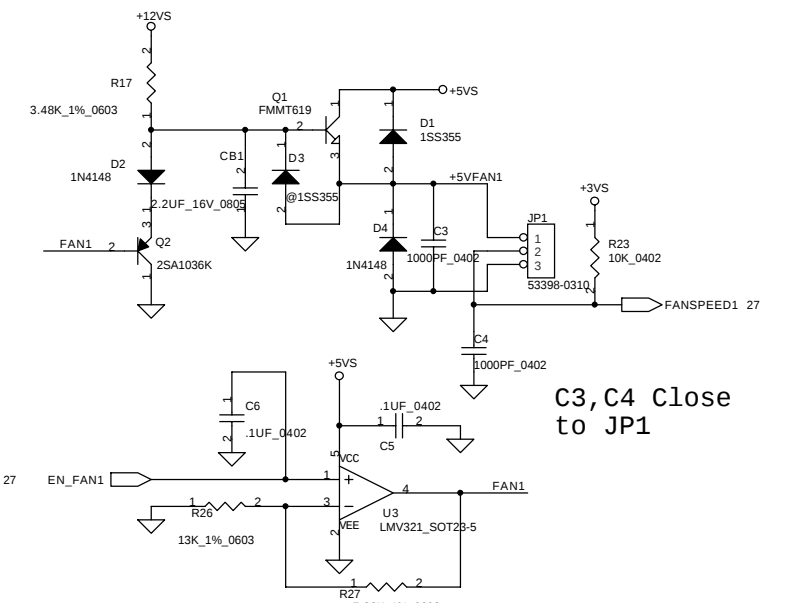
PULL UP



Thermal Sensor ADM1032AR

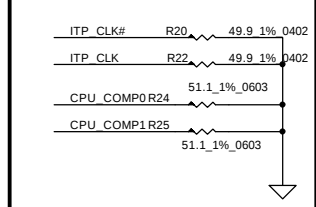


Fan Control circuit

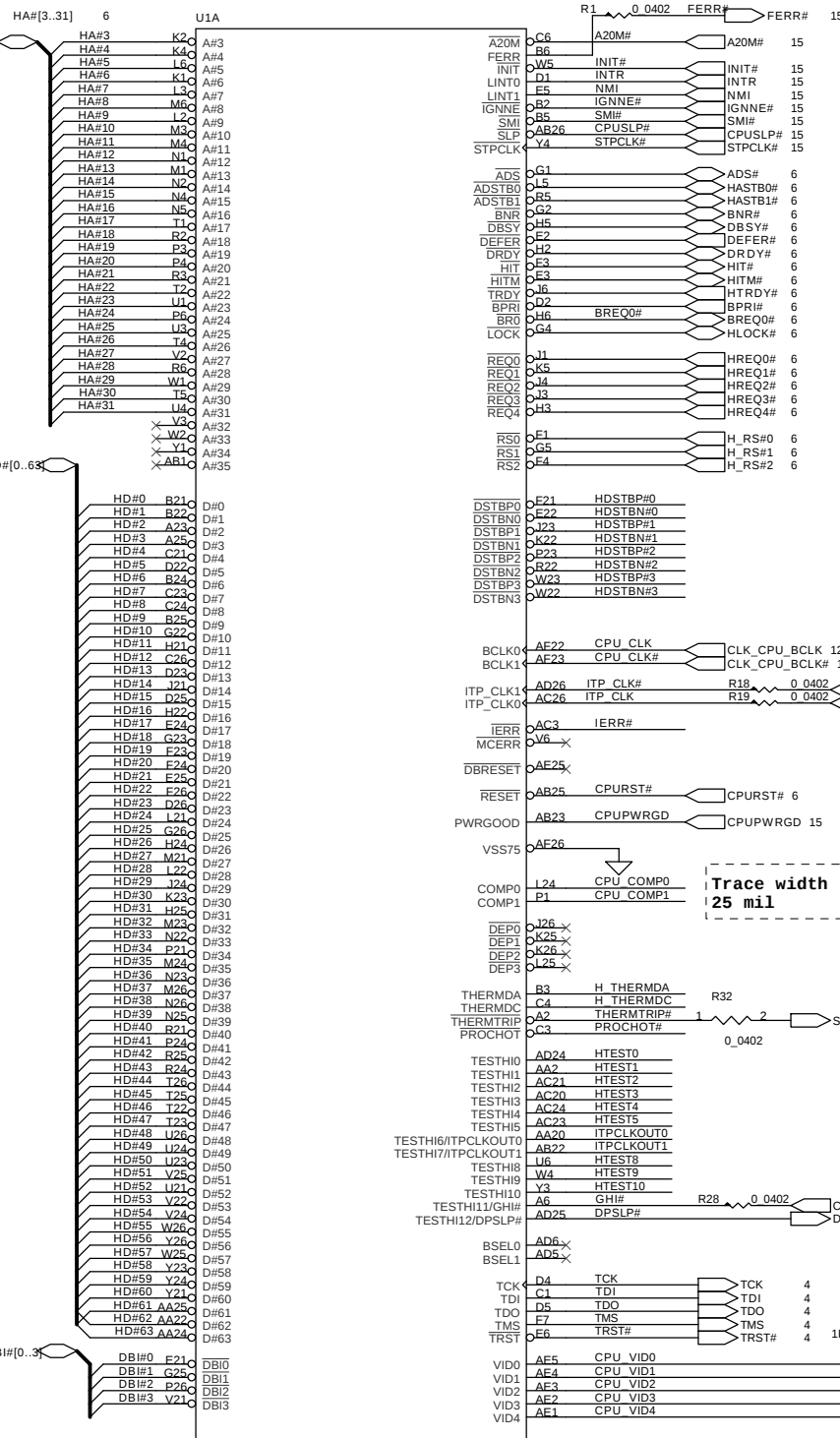


C3,C4 Close to JP1

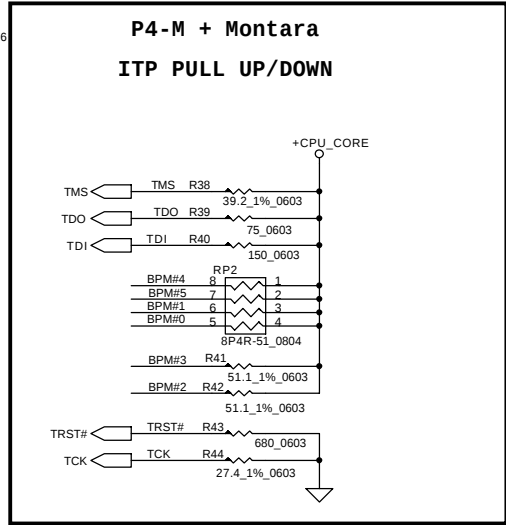
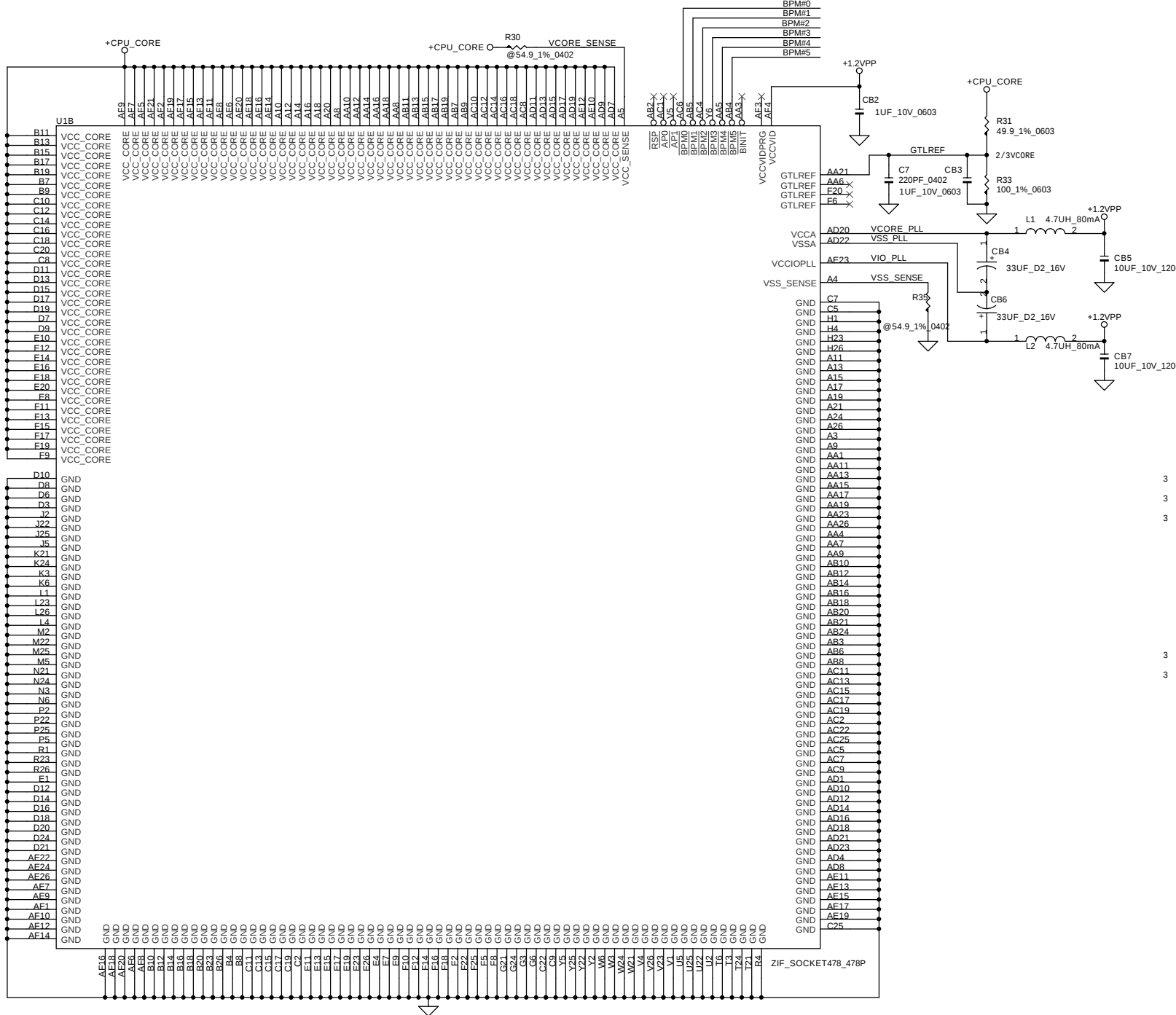
PULL DOWN



Trace width : 25 mil



ZIF_SOCKET478_478P

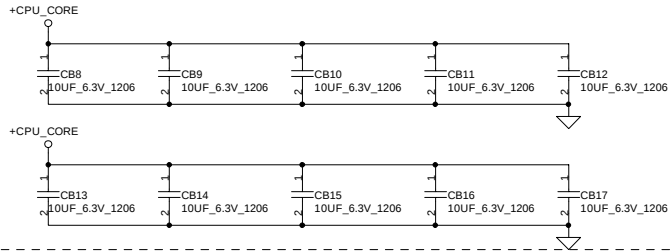


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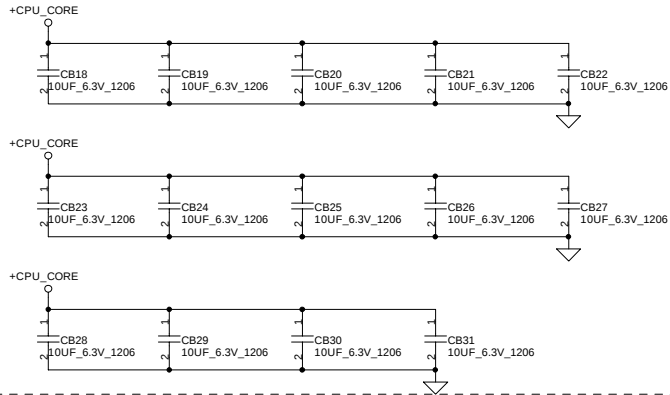
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Layout note :
Place close to CPU. Use 2-3 vias per PAD.
Place 22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2-3 vias per PAD.

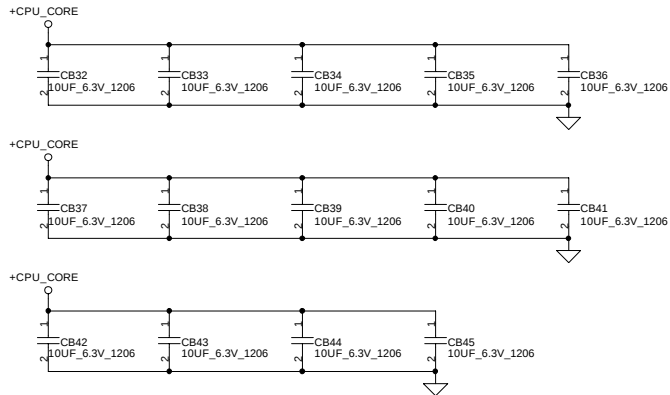
Please place these cap in the socket cavity area



Please place these cap on the socket north side

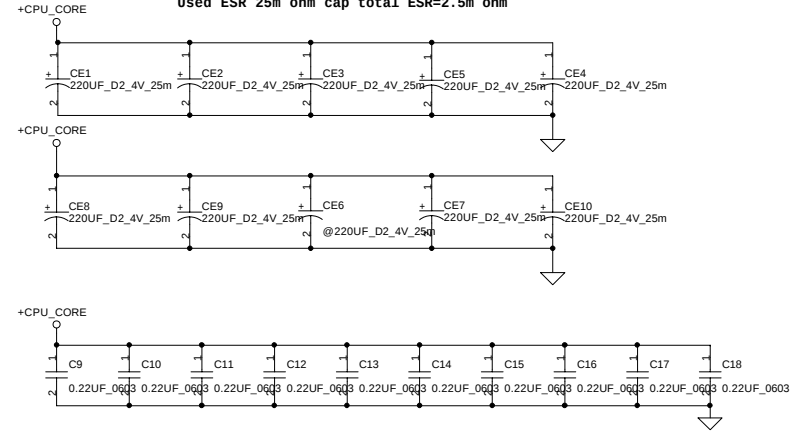


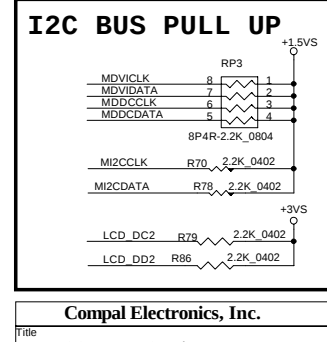
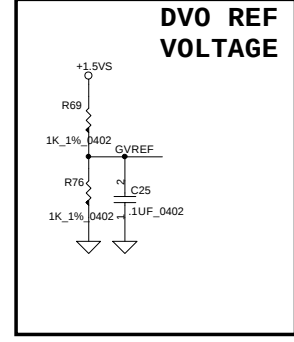
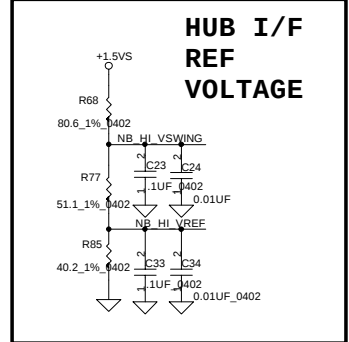
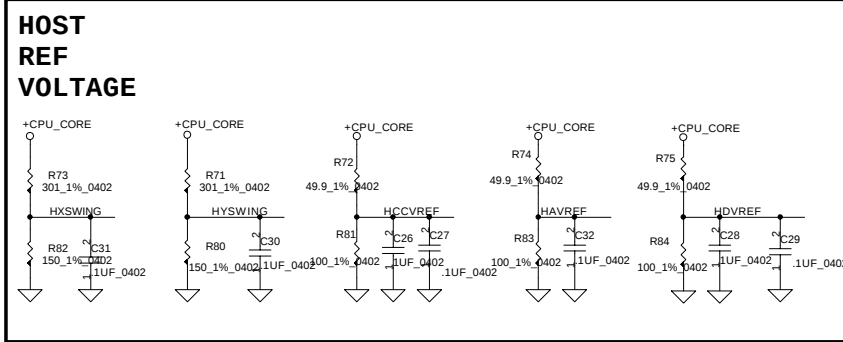
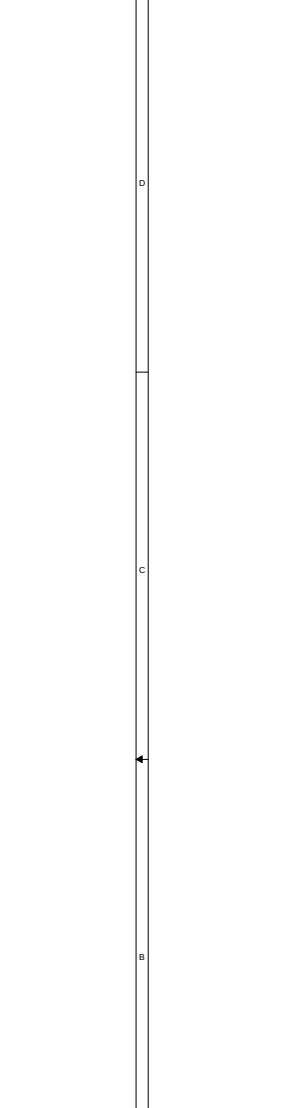
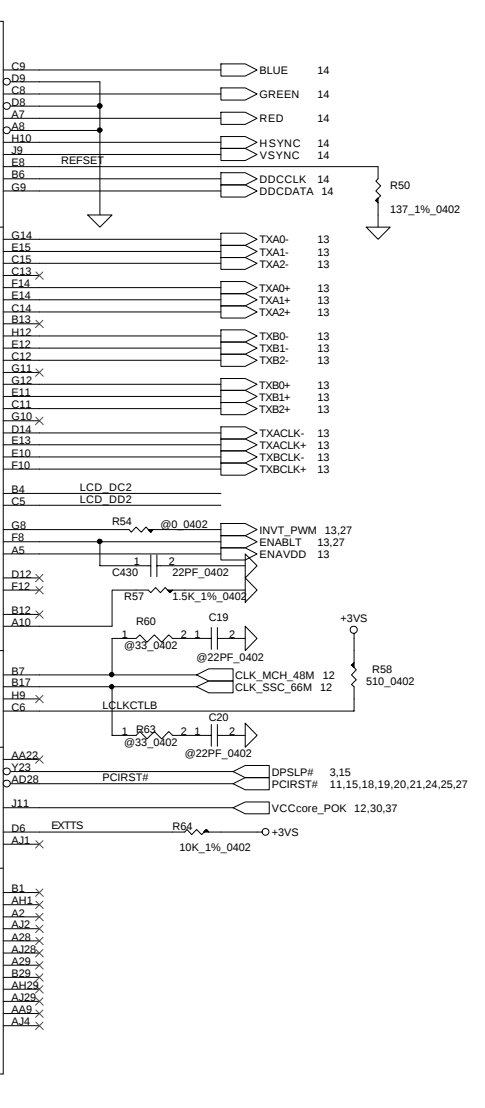
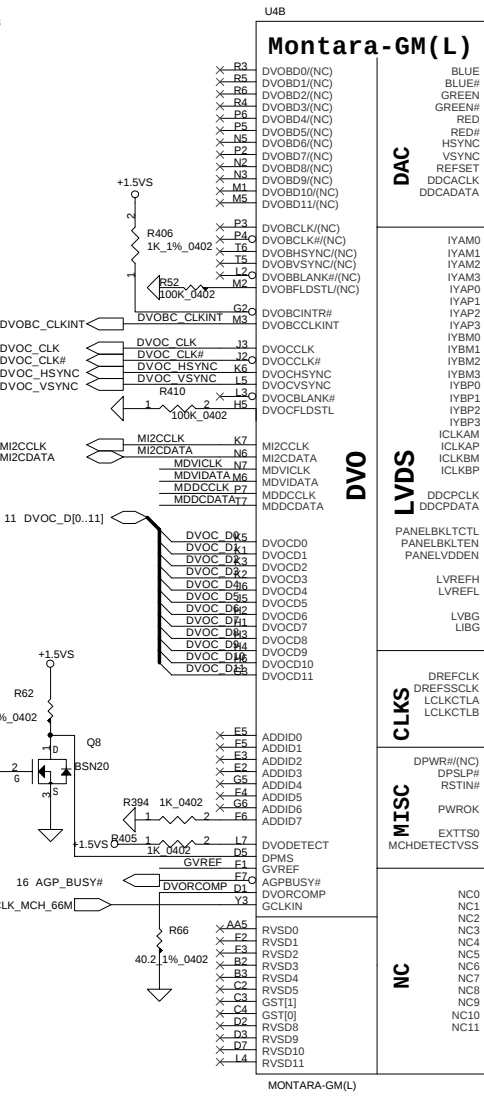
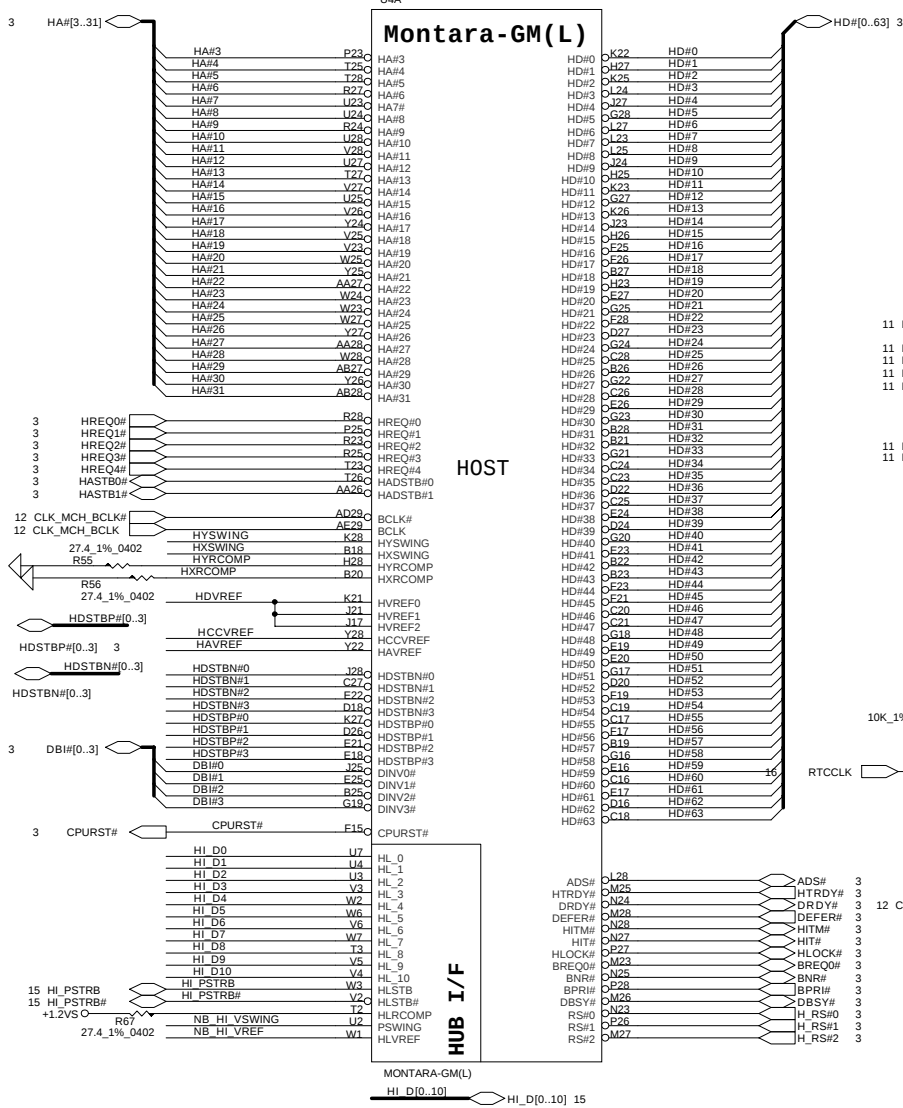
Please place these cap on the socket south side



Layout note :
Place close to CPU power and
ground pin as possible
(<1inch)

Used ESR 25m ohm cap total ESR=2.5m ohm





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U4C

Montara-GM(L)

DDR SMA0 AC18C SMA0
DDR SMA1 AD14C SMA1
DDR SMA2 AD12C SMA2
DDR SMA3 AD17C SMA3
DDR SMA4 AD11C SMA4
DDR SMA5 AC12C SMA5
DDR SMA6 AD5C SMA6
DDR SMA7 AD7C SMA7
DDR SMA8 AC6C SMA8
DDR SMA9 AC5C SMA9
DDR SMA10 AC19C SMA10
DDR SMA11 AD5C SMA11
DDR SMA12 AB5C SMA12

MEMORY

DDR SDQ50 AG2 SDQ50
DDR SDQ51 AH5 SDQ51
DDR SDQ52 AH8 SDQ52
DDR SDQ53 AE12 SDQ53
DDR SDQ54 AH17 SDQ54
DDR SDQ55 AE21 SDQ55
DDR SDQ56 AH24 SDQ56
DDR SDQ57 AH27 SDQ57
DDR SDQ58 AD15 SDQ58

DDR SWE# AD25C SWE#
DDR SRAS# AC21C SRAS#
DDR SCAS# AC24C SCAS#

9 DDR_CLK0 AB2 SCK0
9 DDR_CLK0# AB2 SCK0#
9 DDR_CLK1 AC26 SCK1
9 DDR_CLK1# AC26 SCK1#
9 DDR_CLK3 AC2 SCK2
9 DDR_CLK3# AC2 SCK2#
9 DDR_CLK4 AC23 SCK3
9 DDR_CLK4# AC23 SCK3#
9 DDR_CLK4# AC23 SCK4
9 DDR_CLK4# AC23 SCK4#
9 DDR_CLK4# AC23 SCK5
9 DDR_CLK4# AC23 SCK5#

9.10 DDR_CKE0 AC7 SCKE0
9.10 DDR_CKE1 AB7 SCKE1
9.10 DDR_CKE2 AC9 SCKE2
9.10 DDR_CKE3 AC10 SCKE3
9.10 DDR_CSC#0 AD23C SCS#0
9.10 DDR_CSC#1 AD23C SCS#1
9.10 DDR_CSC#2 AC22C SCS#2
9.10 DDR_CSC#3 AC25C SCS#3

DDR SBS0 AD22 SBA0
DDR SBS1 AD20 SBA1

DDR SDM0 AE5 SDM0
DDR SDM1 AE5 SDM1
DDR SDM2 AE5 SDM2
DDR SDM3 AH12 SDM3
DDR SDM4 AD19 SDM4
DDR SDM5 AD21 SDM5
DDR SDM6 AD24 SDM6
DDR SDM7 AH28 SDM7
DDR SDM8 AH15 SDM8

DDR SMA B1 AD16 SMA_B1
DDR SMA B2 AC12 SMA_B2
DDR SMA B4 AF11 SMA_B4
DDR SMA B5 AD10 SMA_B5

AC15C RCVENOUT#
AC16C RCVENIN#
MRCOMP AB1 SMRCOMP
MVSWINGL AJ22 SMVSWINGL
MVSWINGH AJ19C SMVSWINGH

MONTARA-GM(L)

SMVREF0

AJ24

O SDRF

C36

1UF_0402

SDQ64

SDQ65

SDQ66

SDQ67

SDQ68

SDQ69

SDQ70

SDQ71

AG14

AE17

AG16

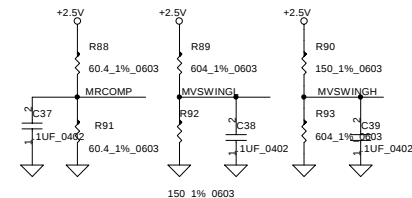
AH14

AE15

AE16

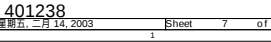
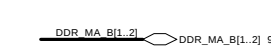
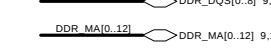
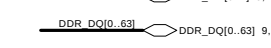
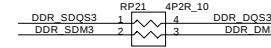
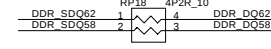
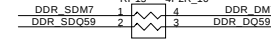
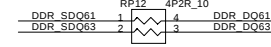
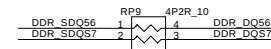
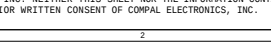
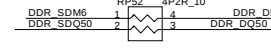
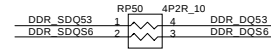
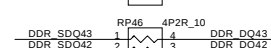
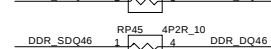
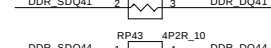
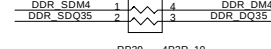
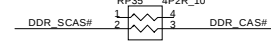
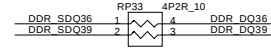
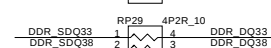
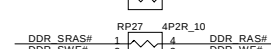
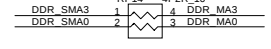
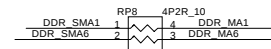
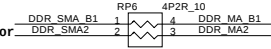
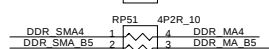
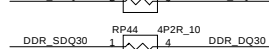
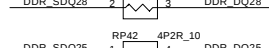
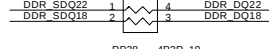
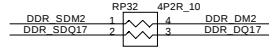
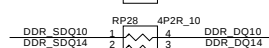
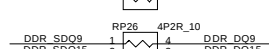
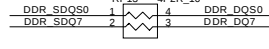
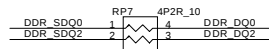
AE17

DDR REF & SWING VOLTAGE



Layout note

Place these resistor
closely DIMM0,
all trace length
Max=0.75"



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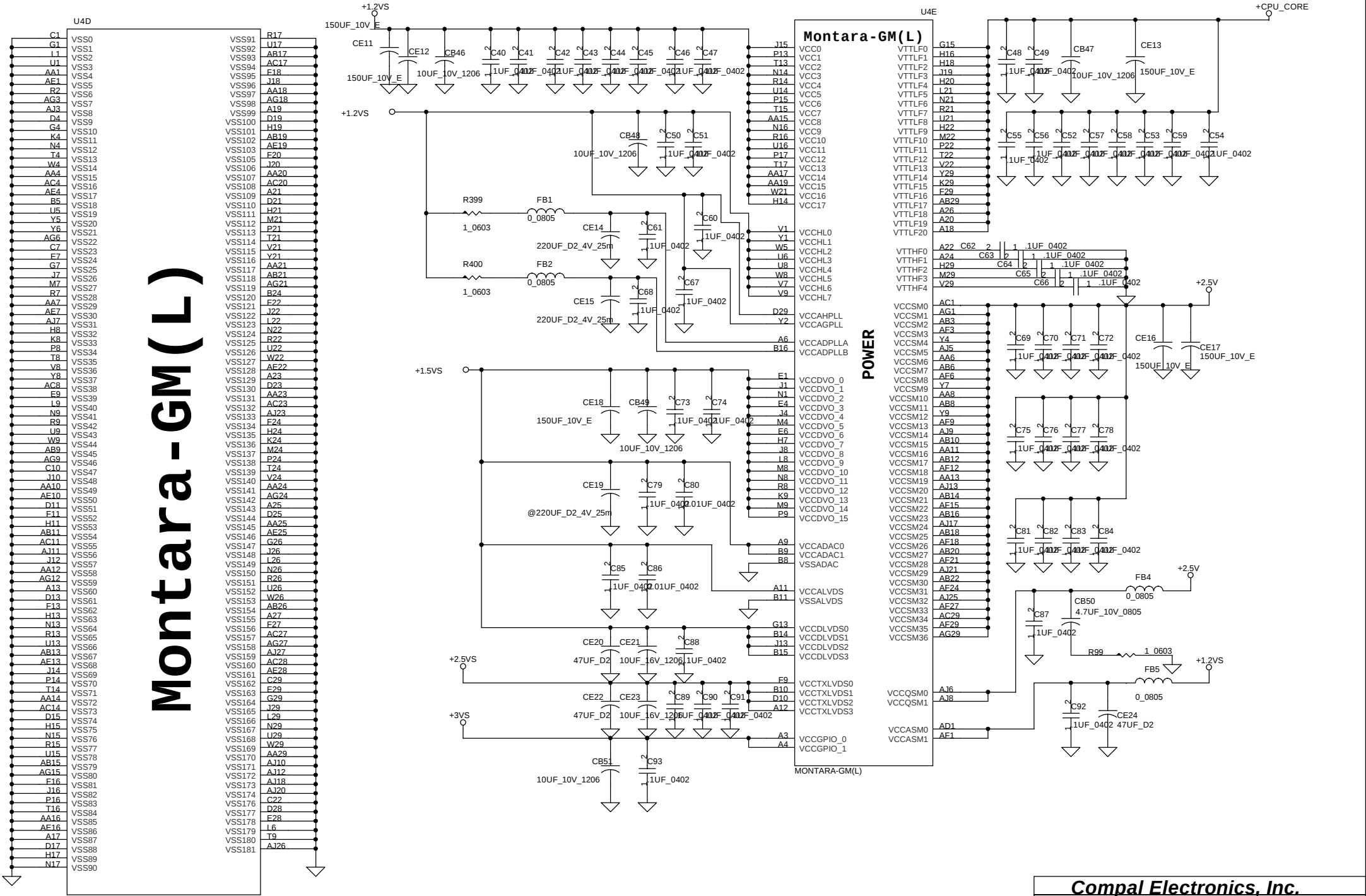
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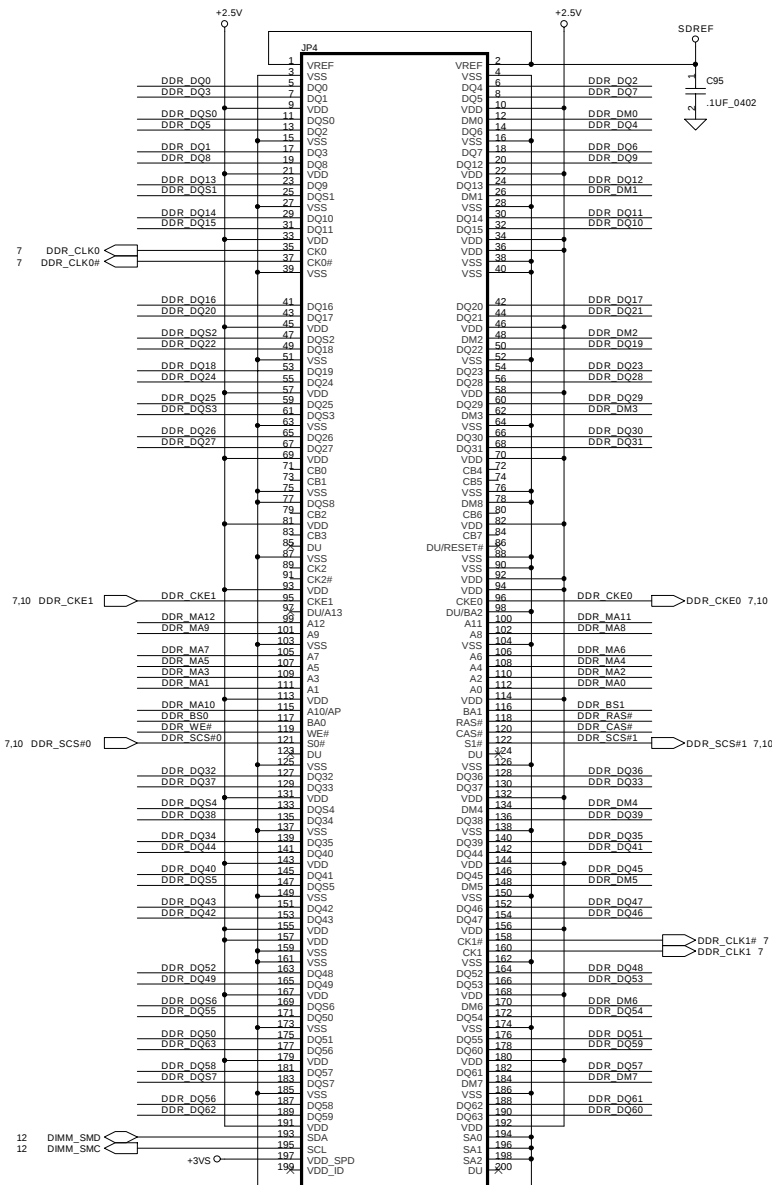
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Montara-GM(L)



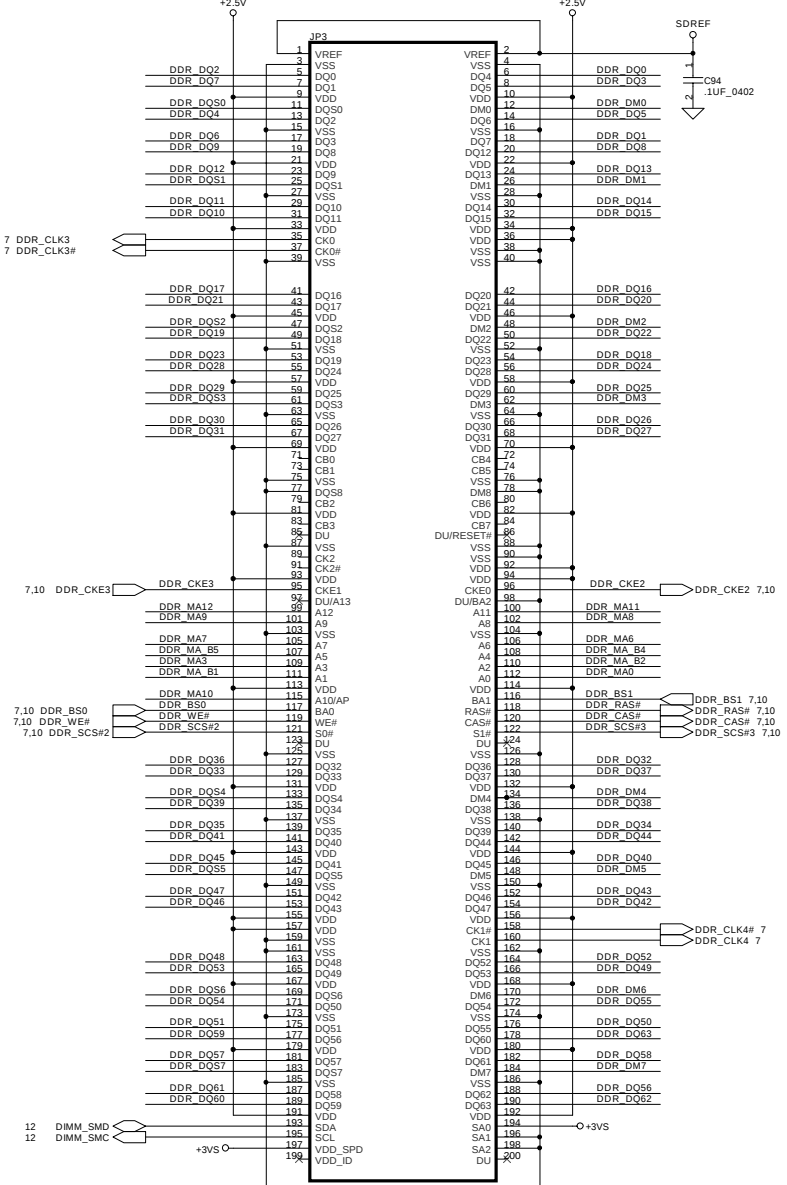
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DIMM0
TOP SIDE

DDR_DM[0..8] 7.10
DDR_DQ[0..63] 7.10
DDR_DQS[0..8] 7.10
DDR_MA[0..12] 7.10
DDR_MA_B[1..2] 7.10
DDR_MA_B[4..5] 7.10

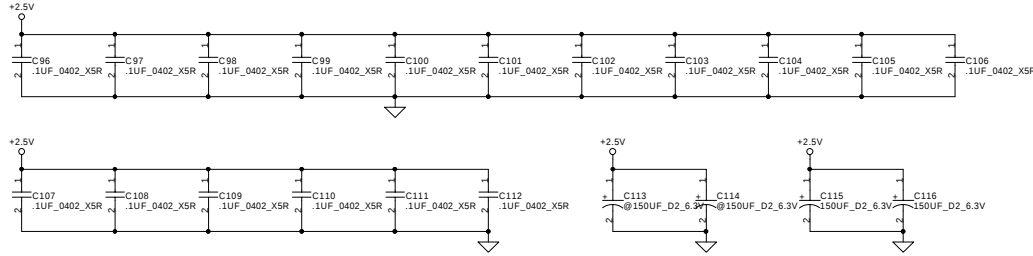


DIMM1
BOTTOM SIDE

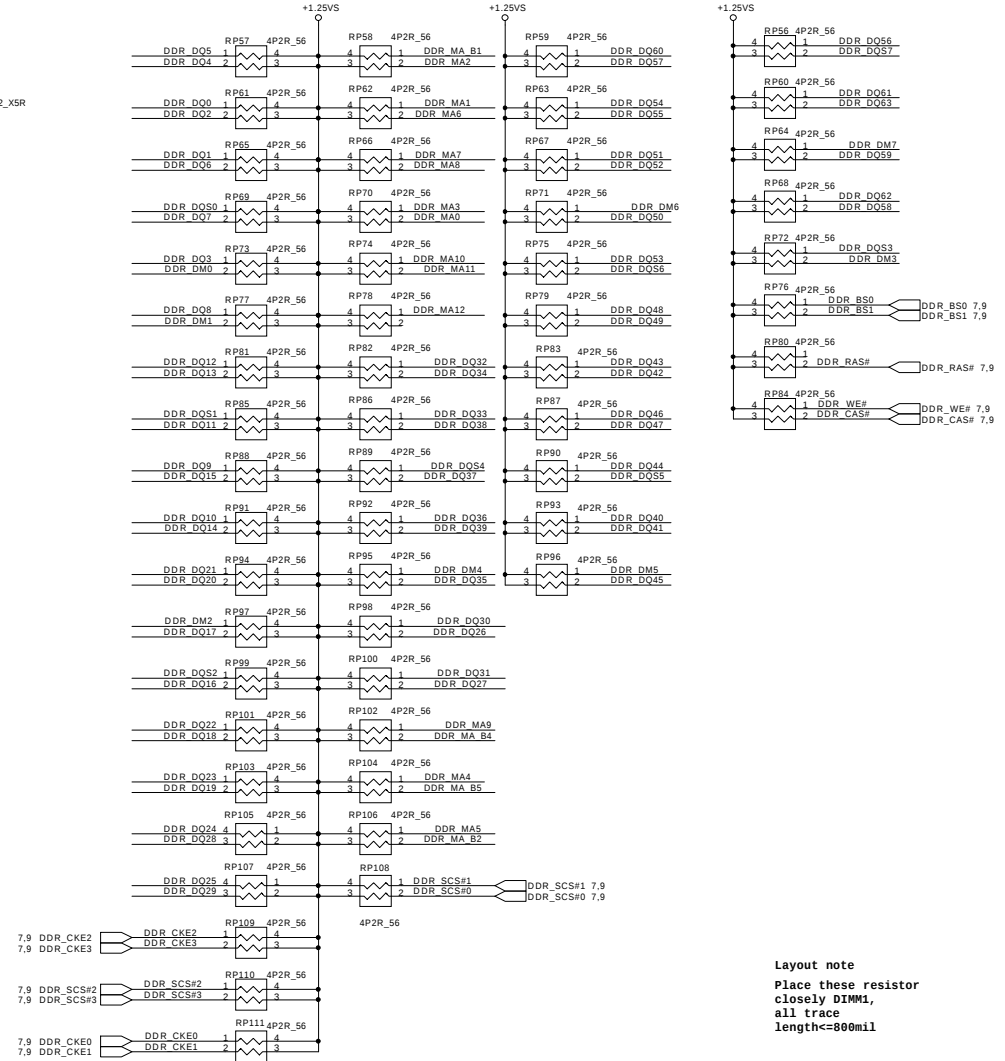
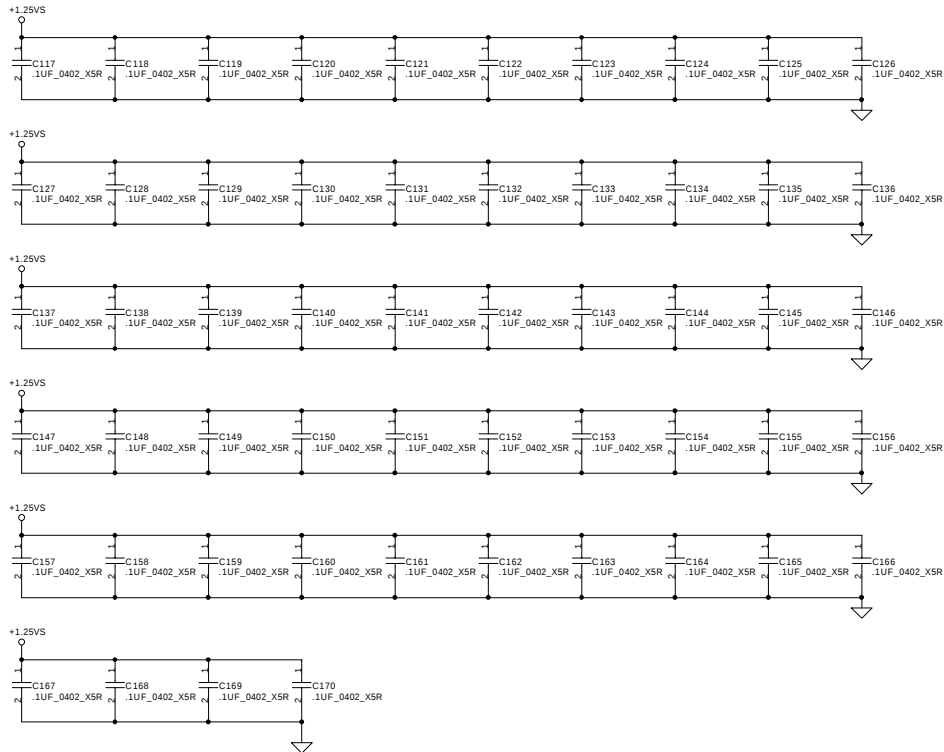
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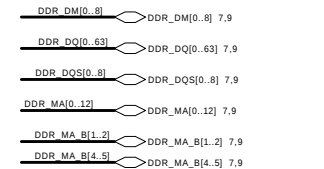
Layout note :
Distribute as close as possible
to DDR-SODIMM.

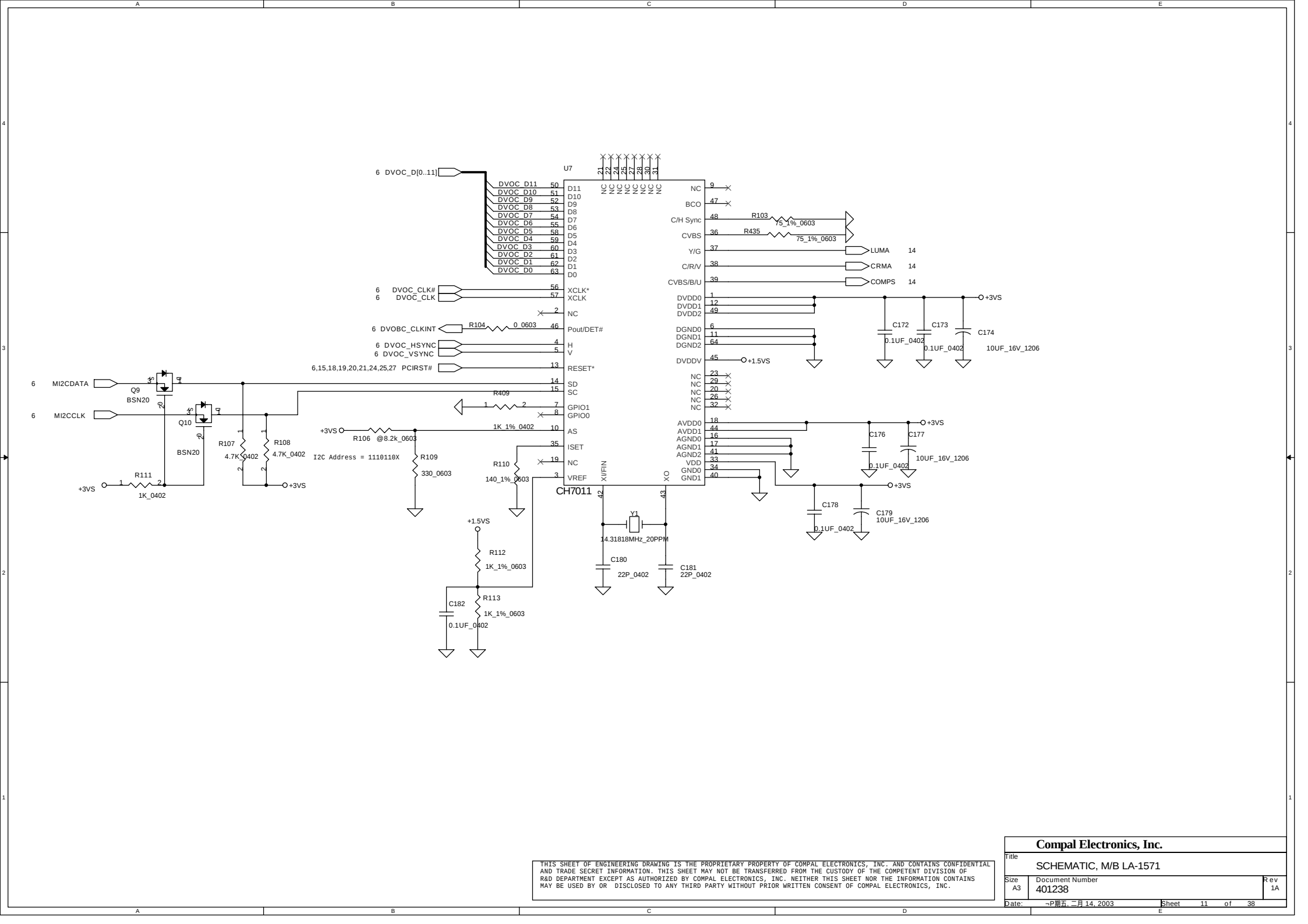


Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



Layout note
Place these resistor
closely DIMM1,
all trace
length<=800m11

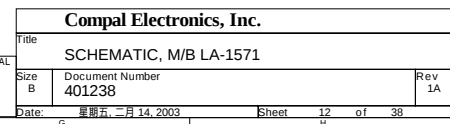




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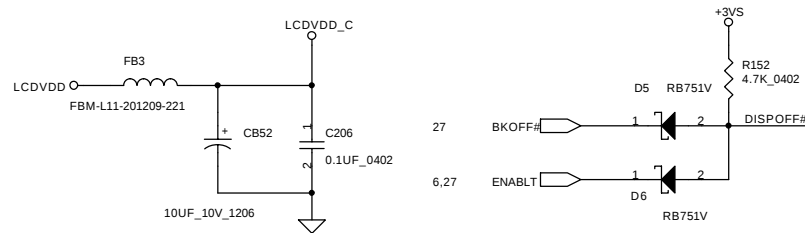
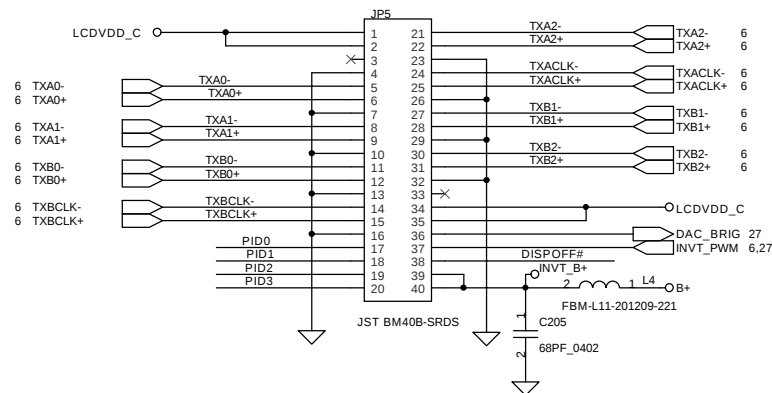
Compal Electronics, Inc.		
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SEL2	SEL1	SEL0	CPUCCLK[0..2]	CPUCCLK[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

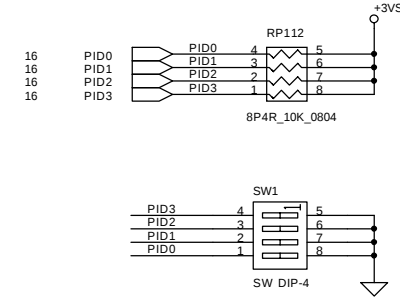


Size B	Document Number 401238	Rev 1A
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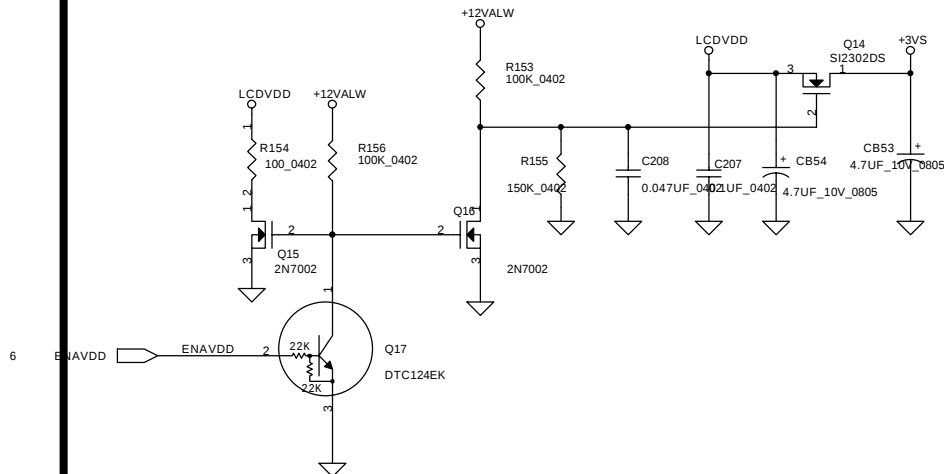
LCD CONN



PANEL ID switch



LCD POWER CIRCUIT

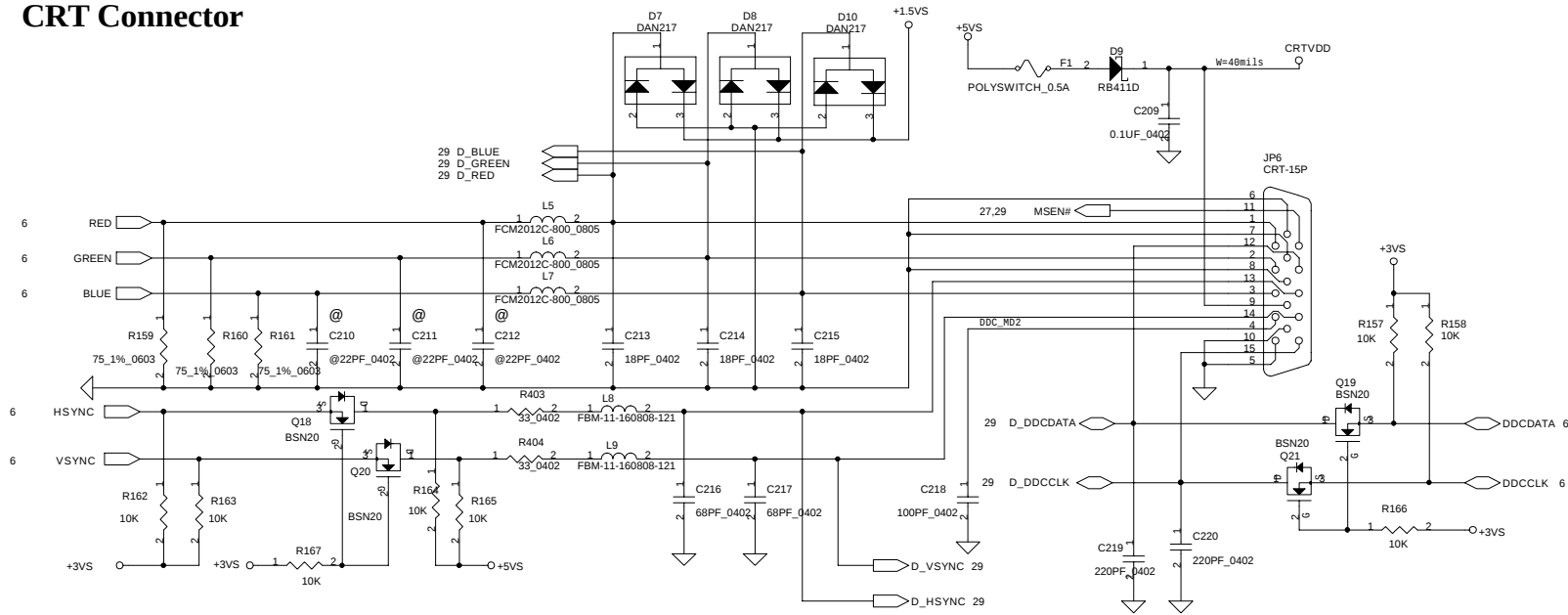


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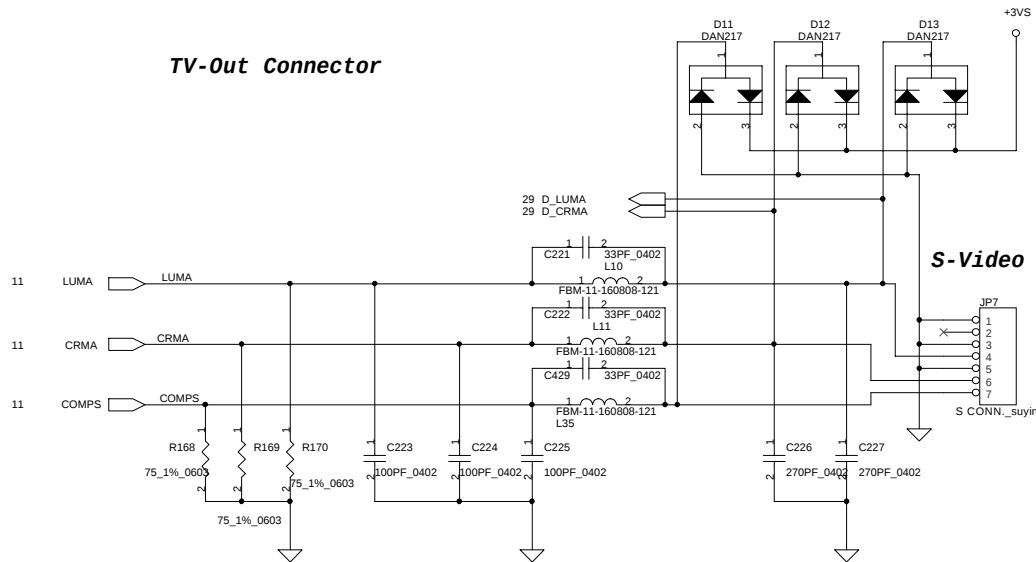
Compal Electronics, Inc.

Title			SCHEMATIC, M/B LA-1571
Size	A3	Document Number	401238
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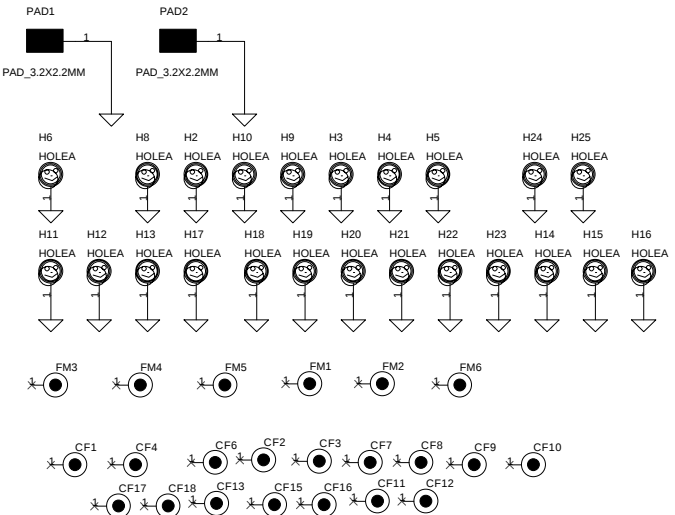
CRT Connector



TV-Out Connector

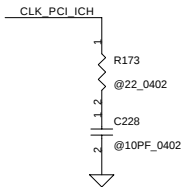


S-Video

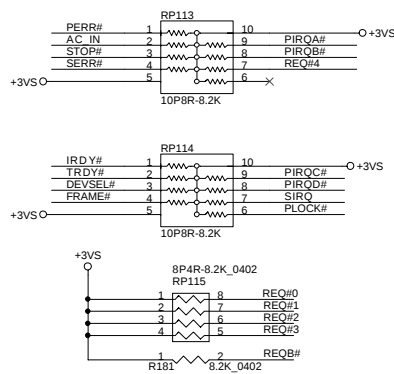


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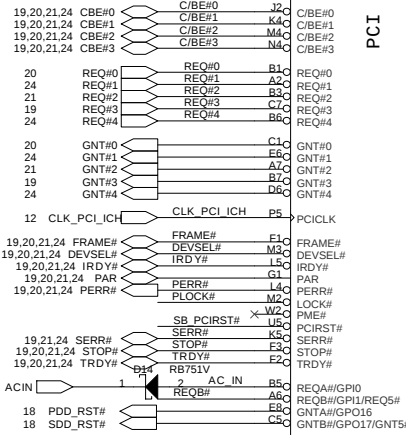
Compal Electronics, Inc.			
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PCI Pullups



19,20,21,24 AD[0..31] AD[0..31]



U9A

ICH4-M

SM I/F
INTRUDER#
SMLINK0
SMLINK1
SMB_CLK
SMB_DATA
SMB_ALERT#/GPIO11

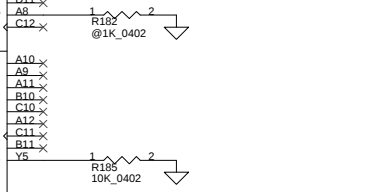
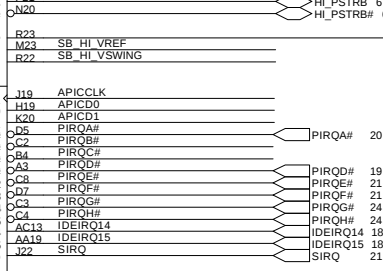
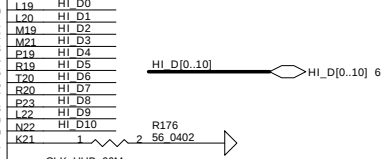
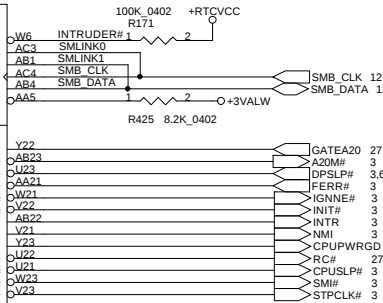
CPU I/F
A20GATE
A20M#
DPSLP#
FERR#
IGNNE#
INTR#
INTR#
NMI
CPU_PWRGOOD
RCIN#
SLP#
SMI#
STPCLK#

HUB I/F
CLK66
HI_STB
HI_STB#
HICOMP
HUB_VREF
HUB_VSWING

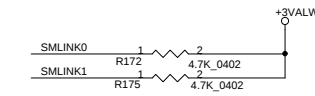
Interrupt I/F
APICCLK
APICD0
APICD1
PIRQA#
PIRQB#
PIRQC#
PIRQD#
PIRQE#/GPIO2
PIRQF#/GPIO3
PIRQG#/GPIO4
PIRQH#/GPIO5
IRQ14
IRQ15
SERIRQ

EEPROM I/F
EE_CS
EE_IN
EE_OUT
EE_SHCLK

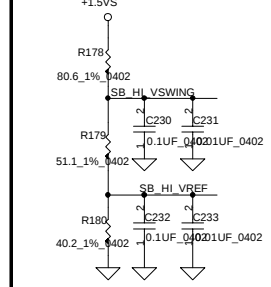
LAN I/F
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_CLK
LAN_RSTSYNC
LAN_RST#



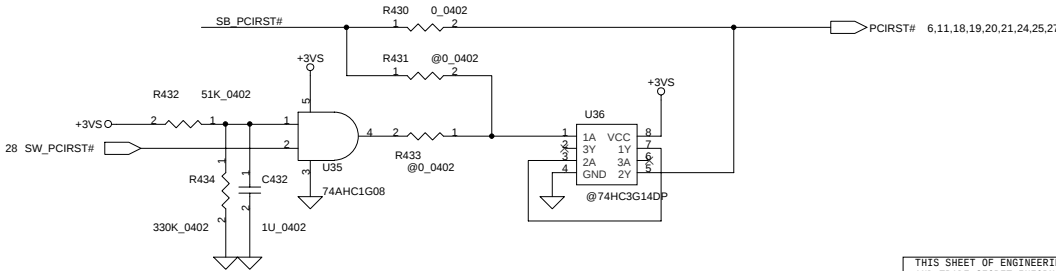
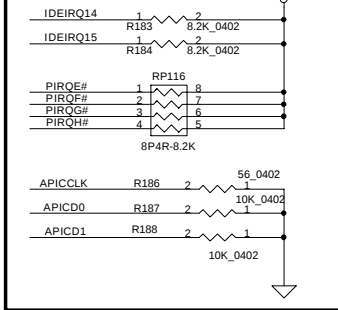
SM BUS



HL REF & SWING VOLTAGE



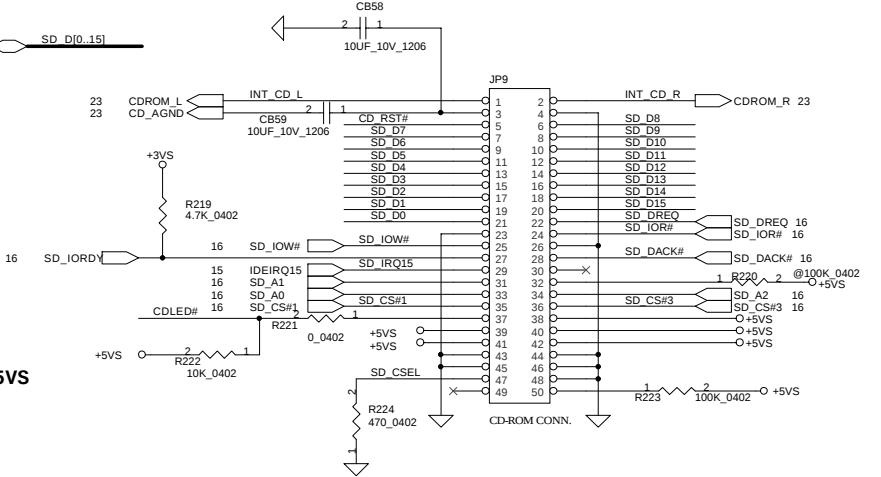
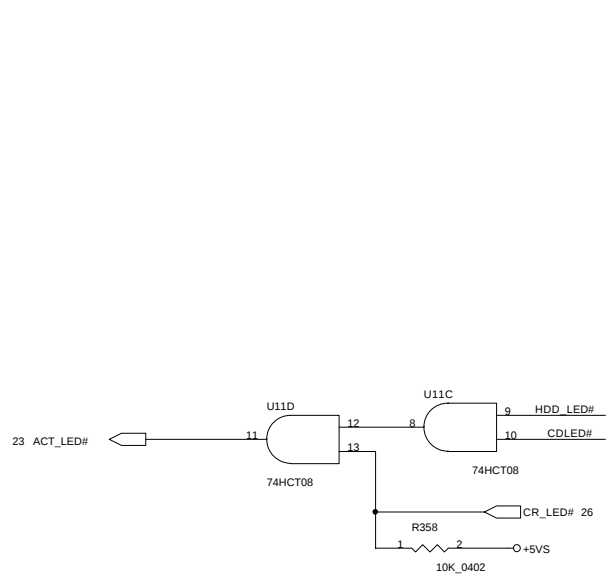
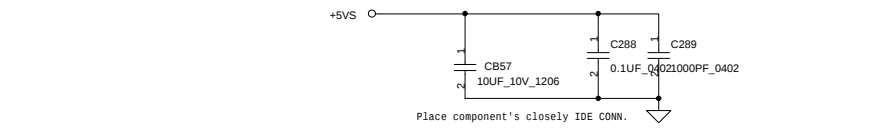
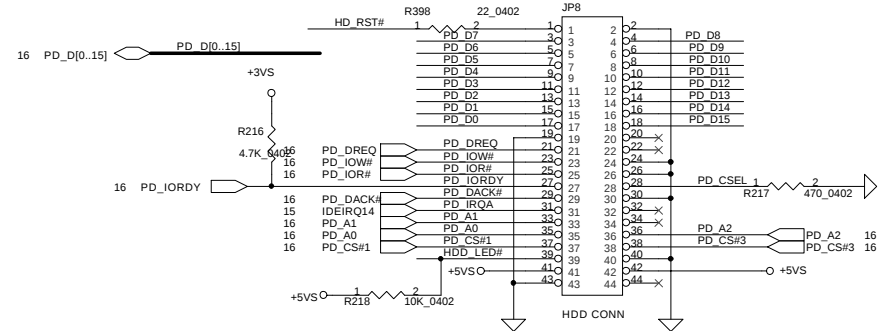
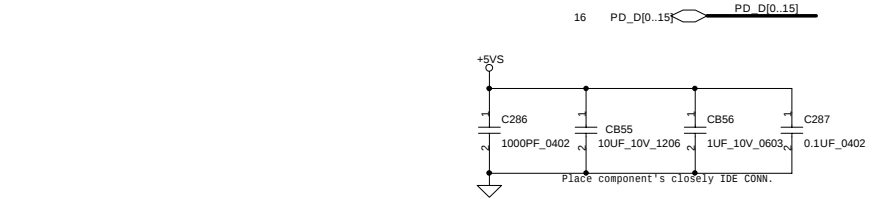
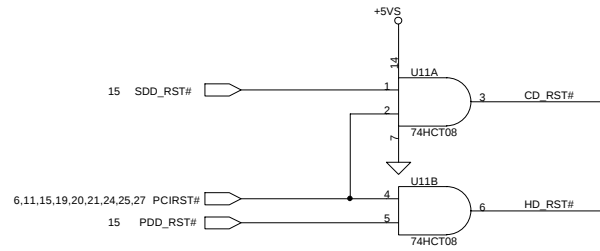
INT I/F



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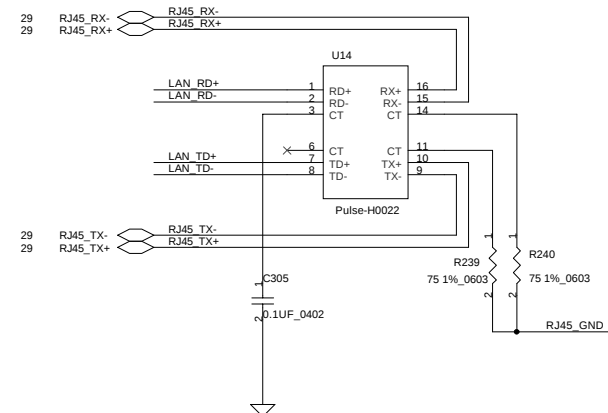
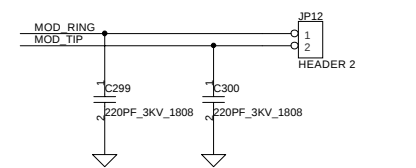
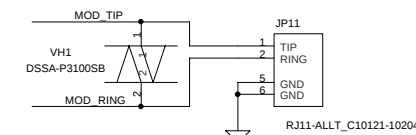
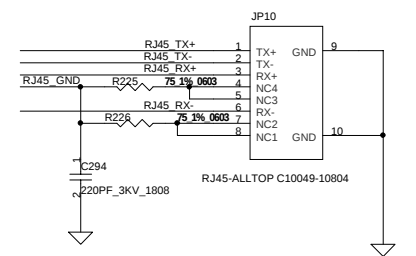
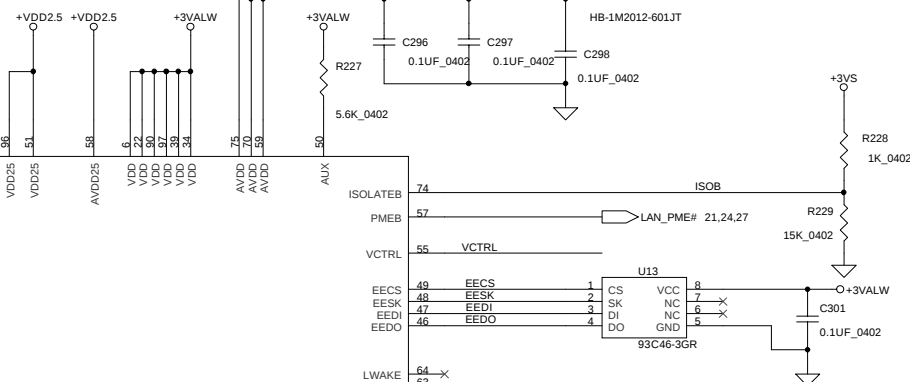
Compal Electronics, Inc.			
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HDD/CD-ROM Module



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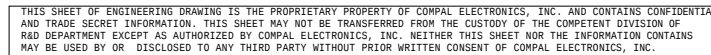
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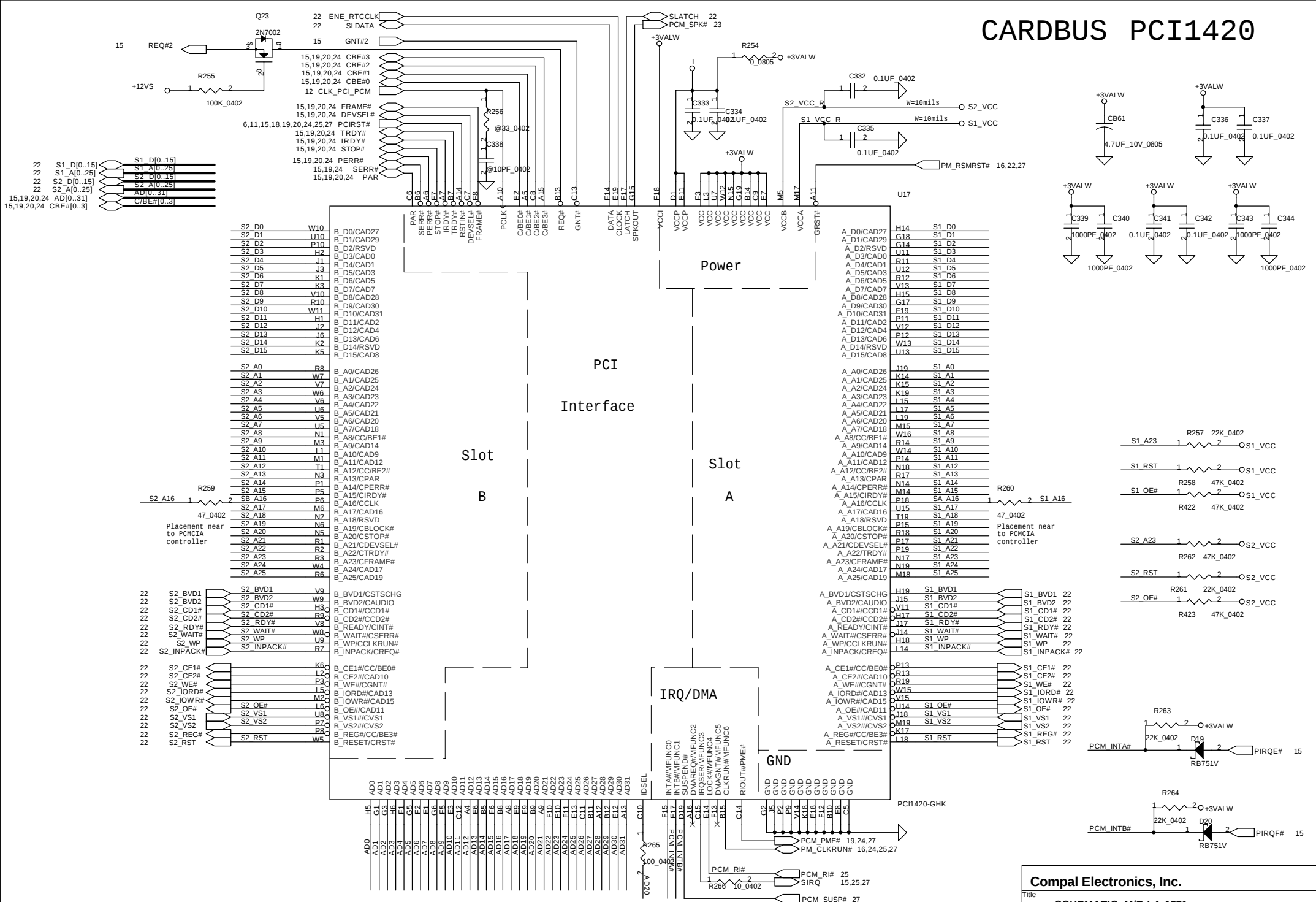
LAN CONTROLLER
RTL8100BL

Place close to U12

Place close to
U14



CARDBUS PCI1420

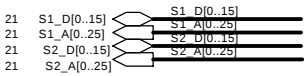
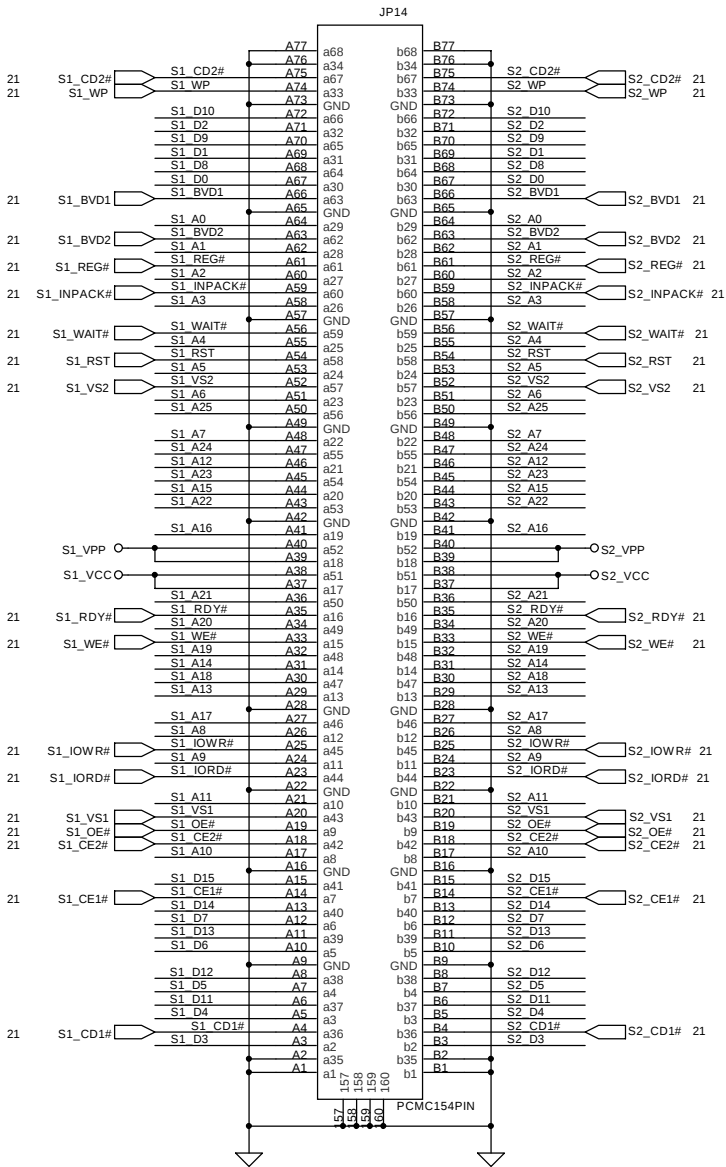


Compal Electronics, Inc.

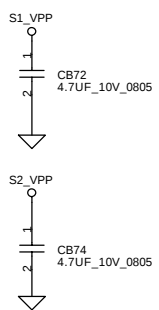
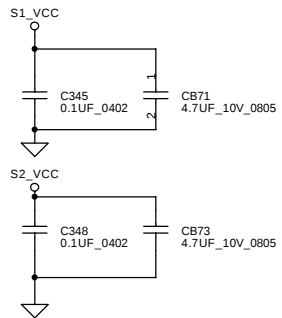
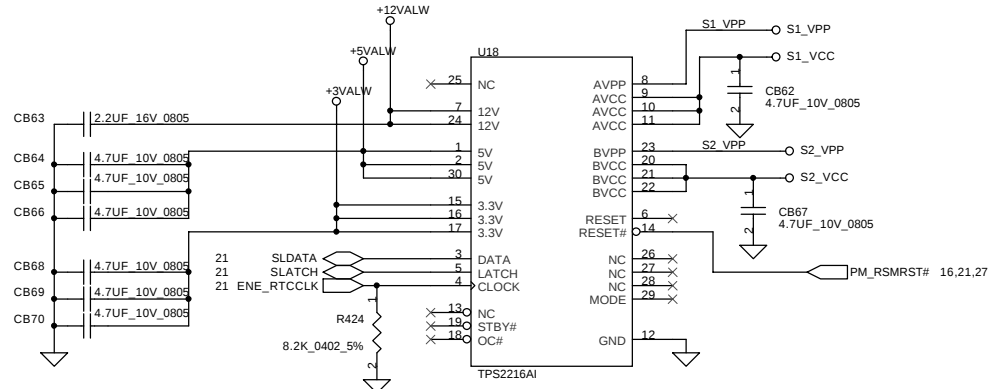
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CARDBUS SOCKET

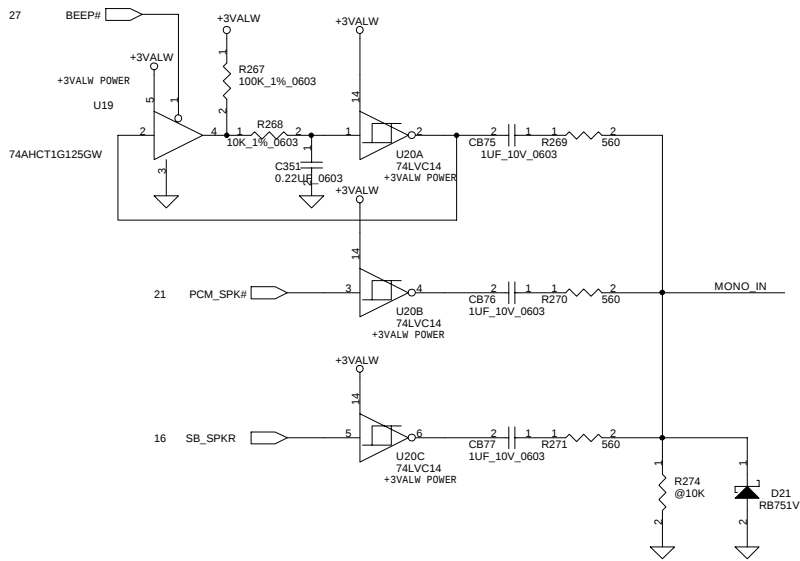


PCMCIA POWER CTRL.

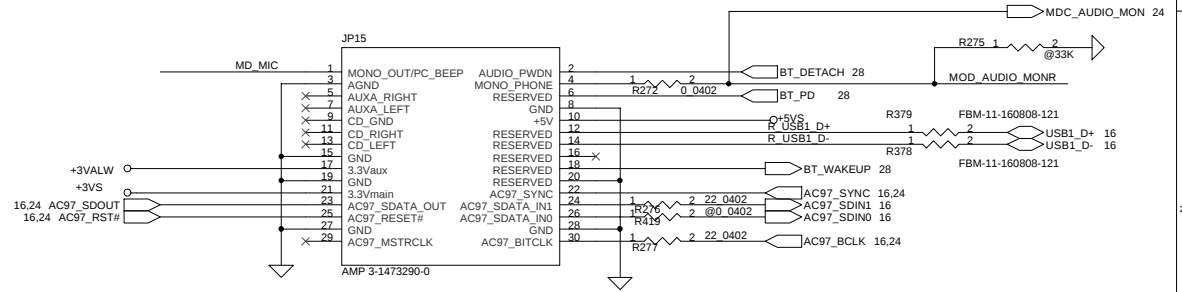


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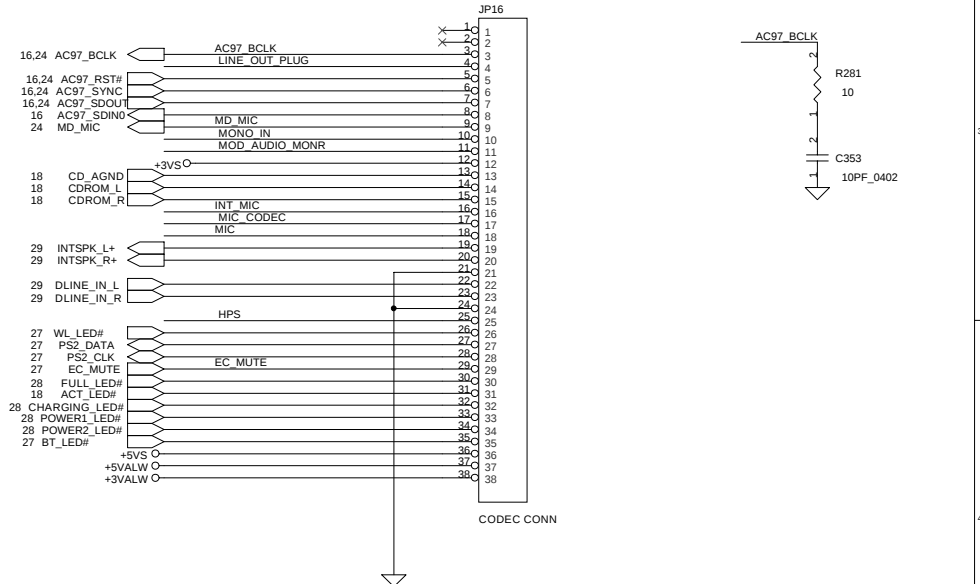
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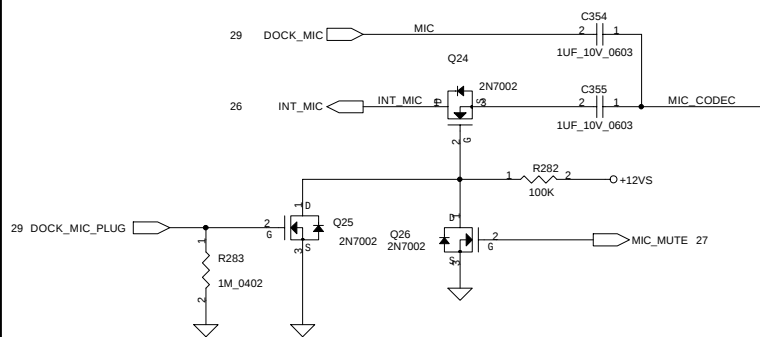
BT/MDC CONN



AC97 CODEC ALC202 CONN



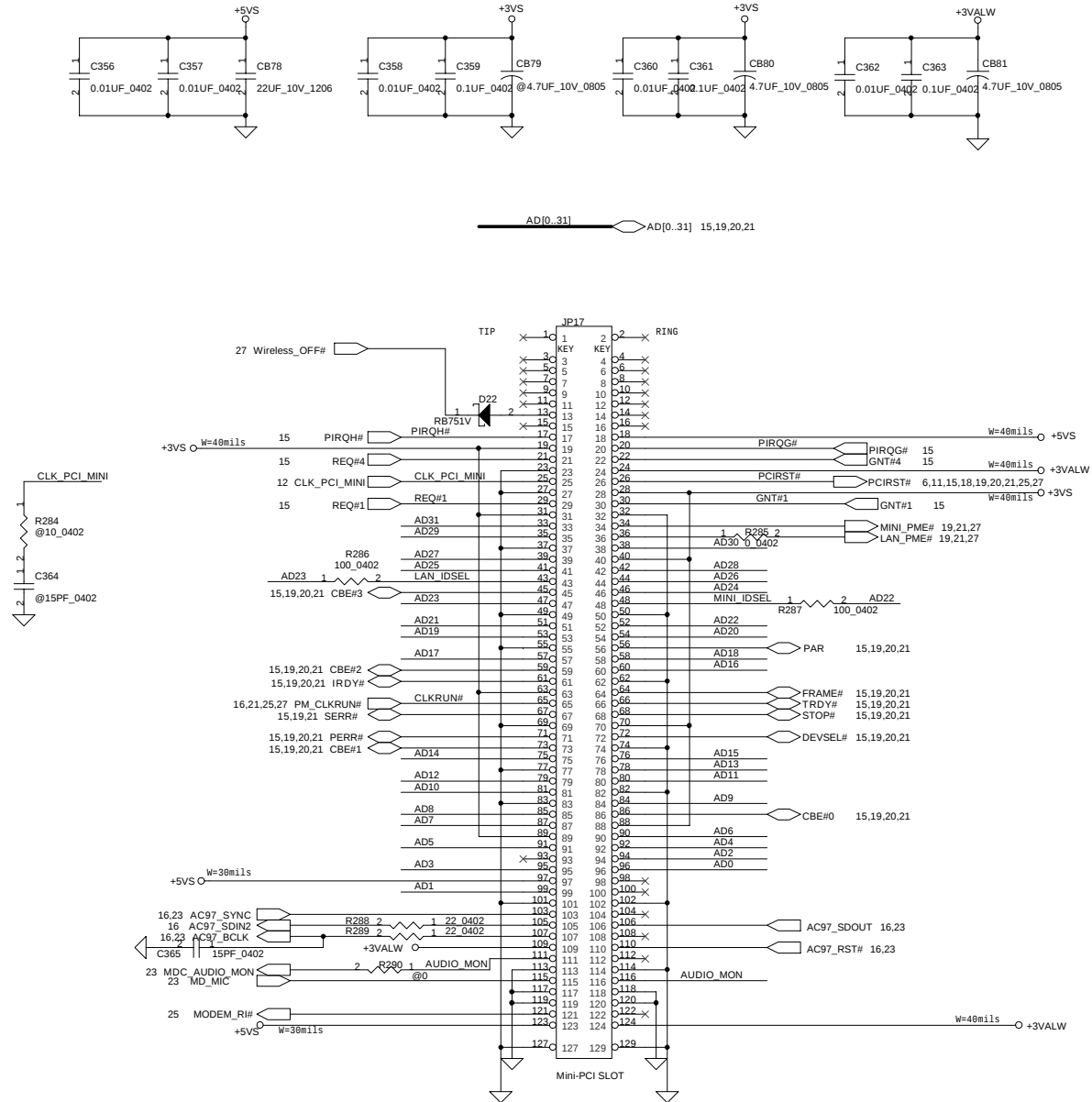
Place close to JP29



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Mini-PCI Slot



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Compal Electronics, Inc.

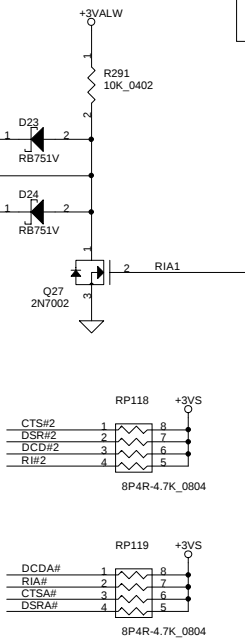
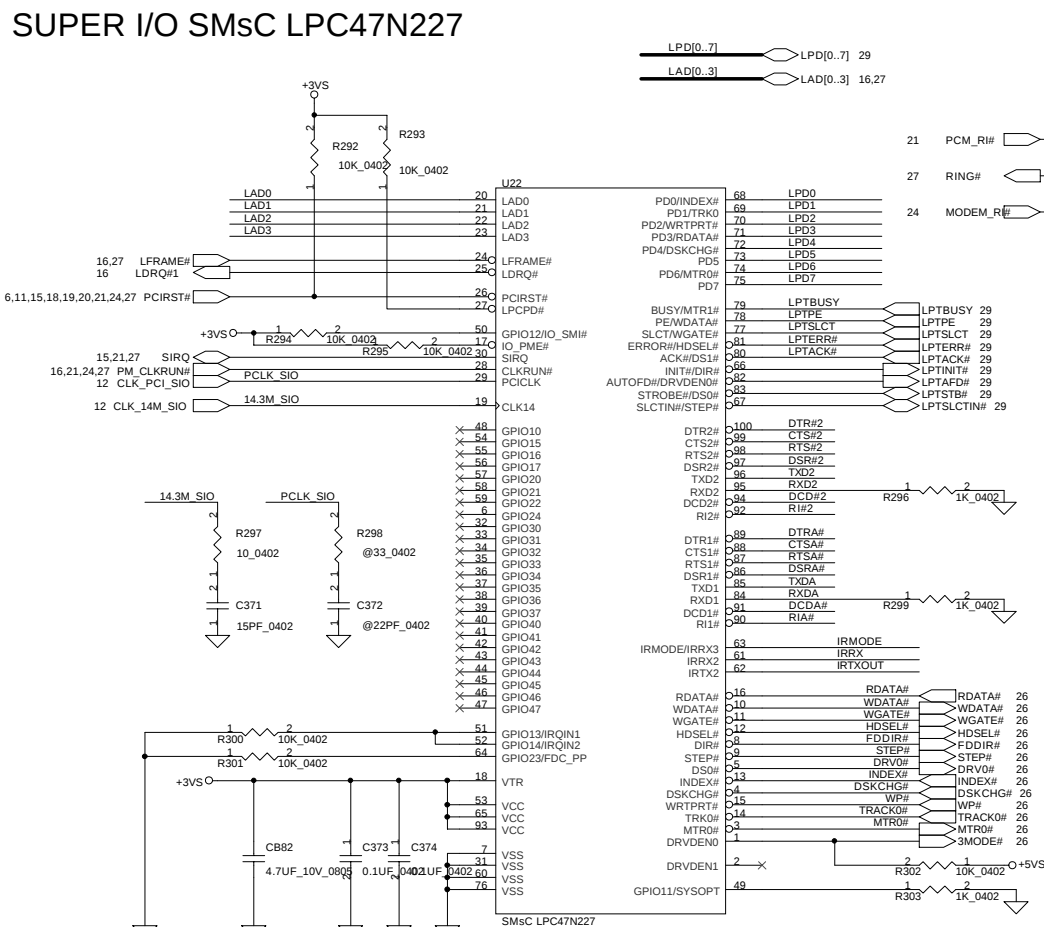
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Size	Document Number 401238	Rev 1A
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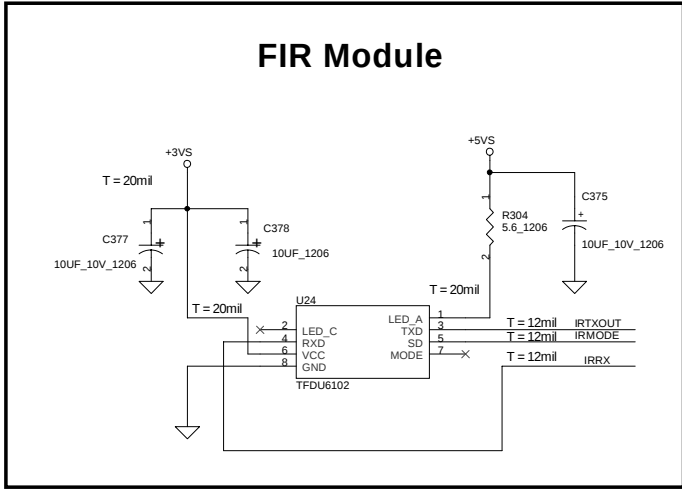
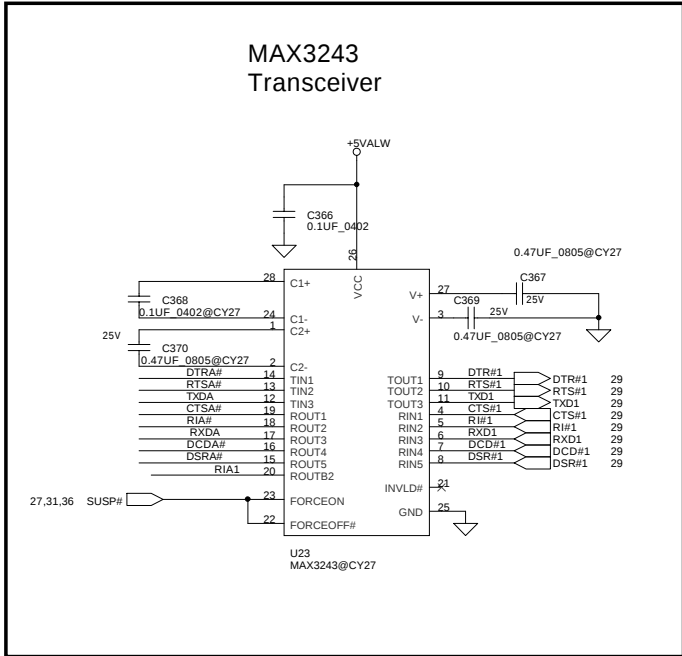
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SUPER I/O SMsC LPC47N227

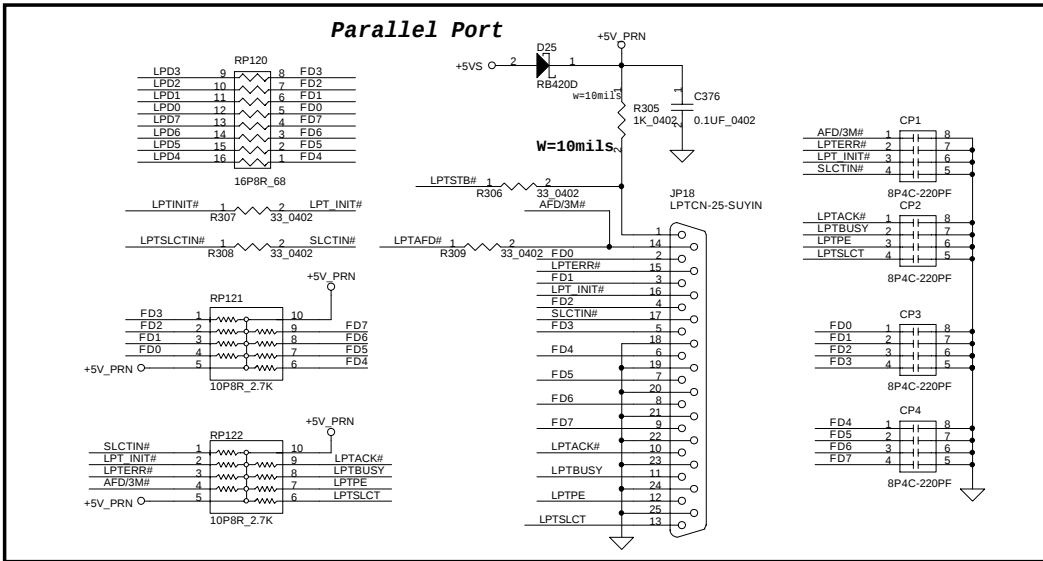
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Base I/O Address
 * 0 = 02Eh
 1 = 04Eh



FIR Module



Parallel Ports

Compal Electronics, Inc

Title
SCHEMATIC, M/B LA-1571

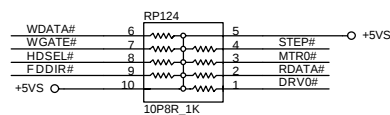
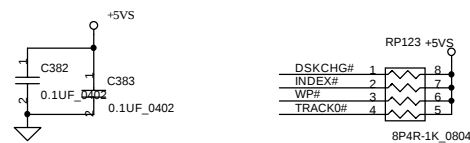
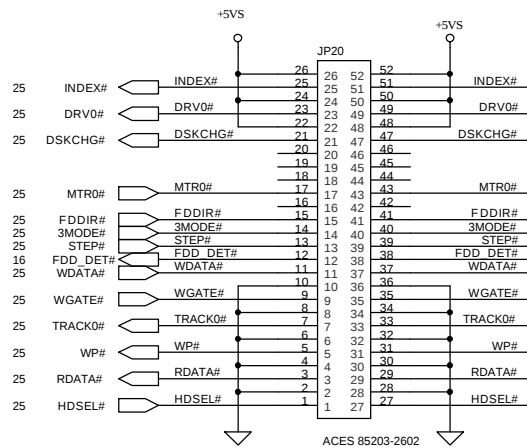
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Rev	1A
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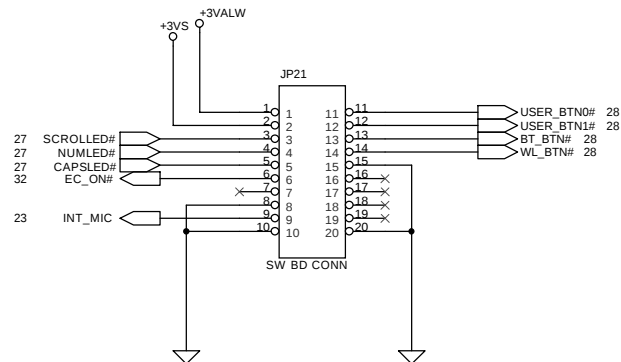
Date: 星期五, 二月 14, 2003

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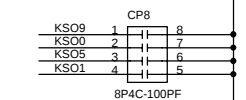
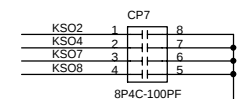
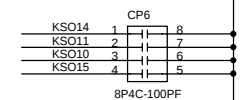
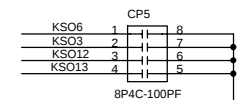
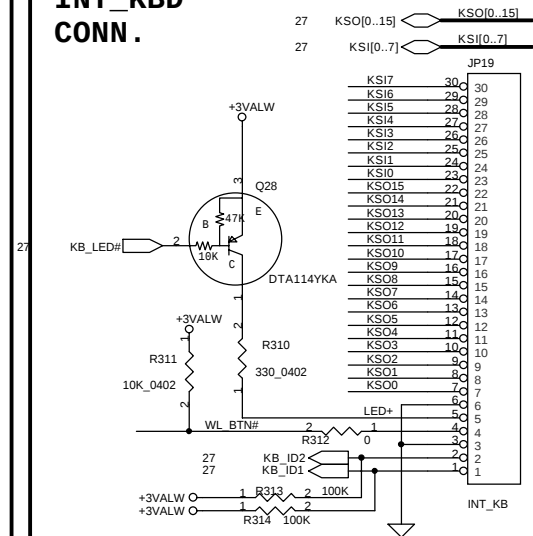
FDD CONN.



SWITCH BOARD CONN.

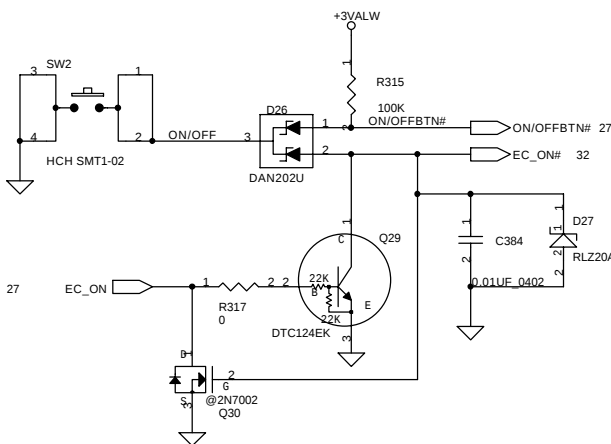


INT_KBD CONN.

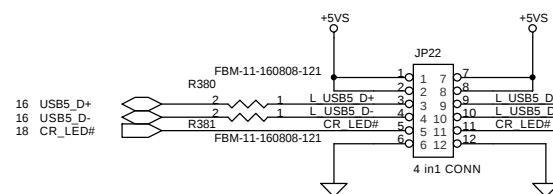


NEED CLOSEST JP18 ADD BY EMI REQUEST

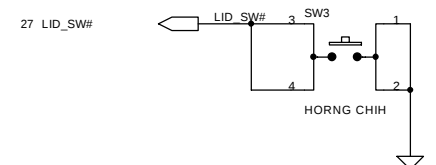
ON/OFF BUTTON



5 IN 1 CONN



LID SW



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Compal Electronics, Inc.

Title SCHEMATIC, M/BLA-1571

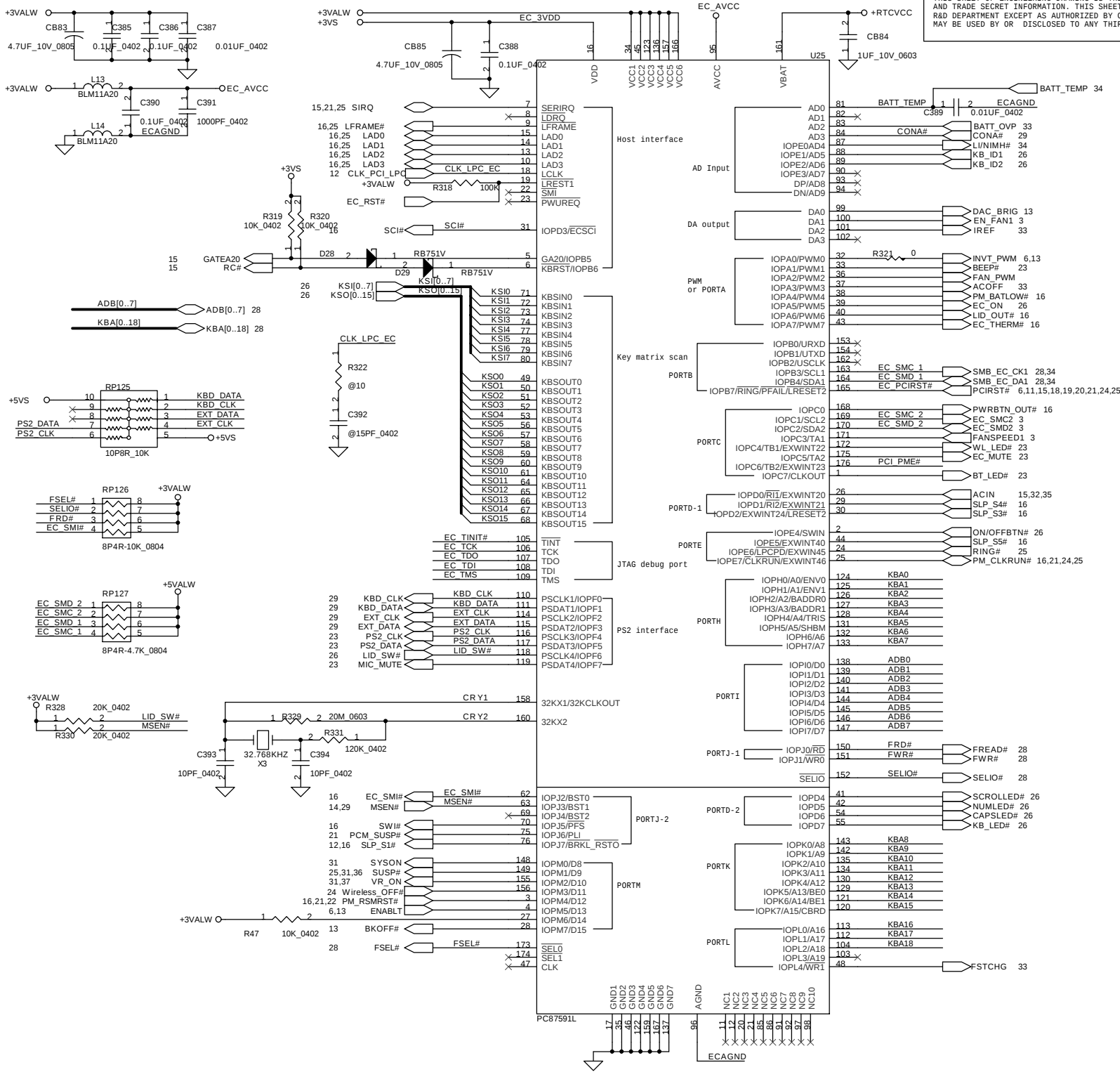
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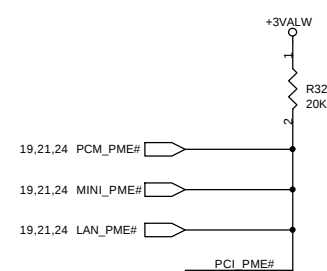
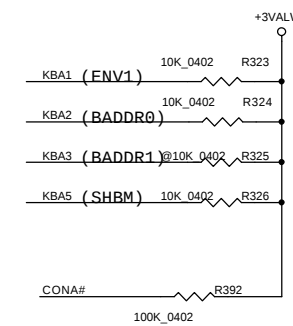
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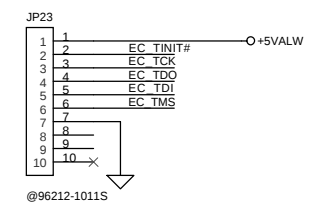
		I/O Address	
BADDR1-0	Index	Data	
0 0	2E	2F	
0 1	4E	4F	
* 1 0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1		
1 1	Reserved		

	ENV0	ENV1	TRIS
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

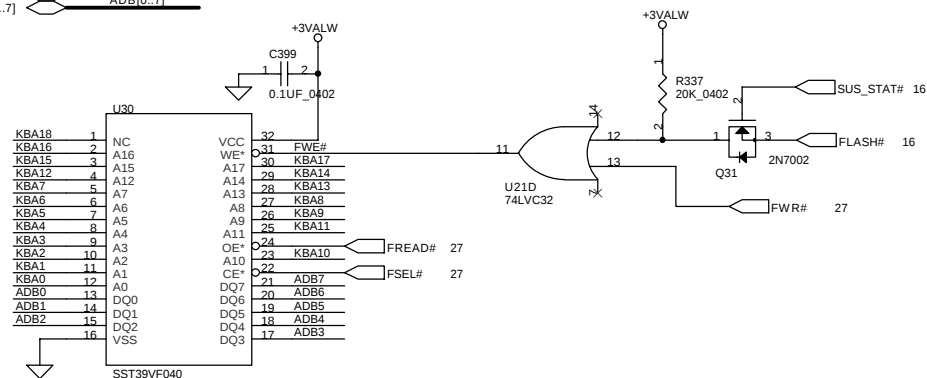
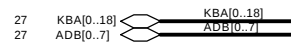
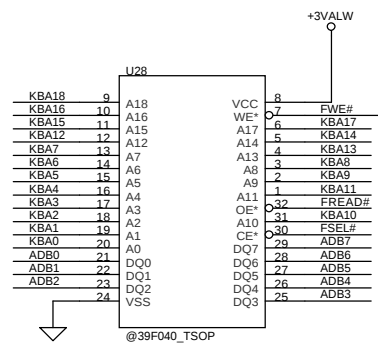
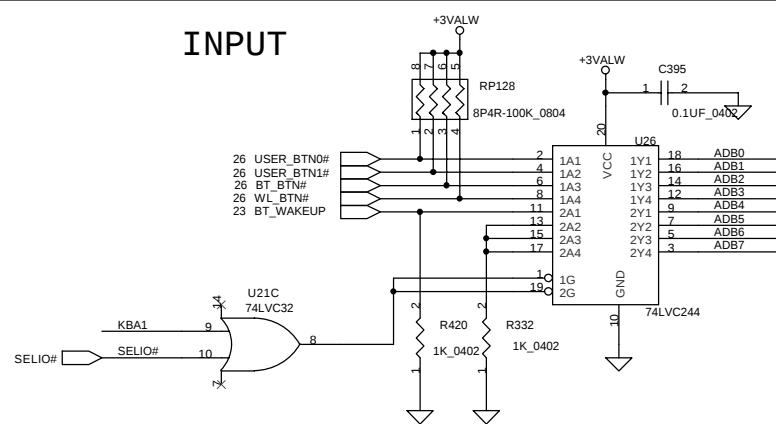
```
SHBM=1: Enable shared memory with host BIOS
TRIS=1: While in IRE and OBD, float all the
        signals for clip-on ISE use
```



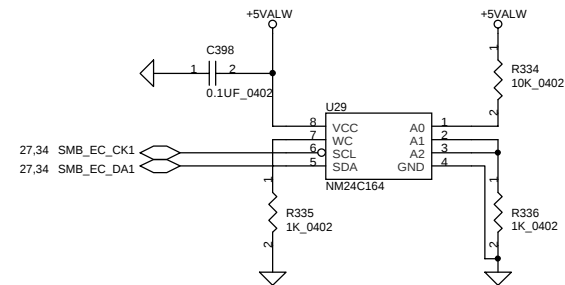
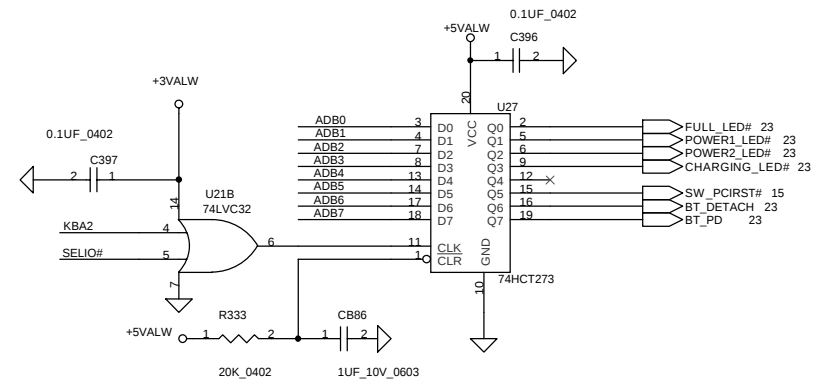
EC DEBUG port

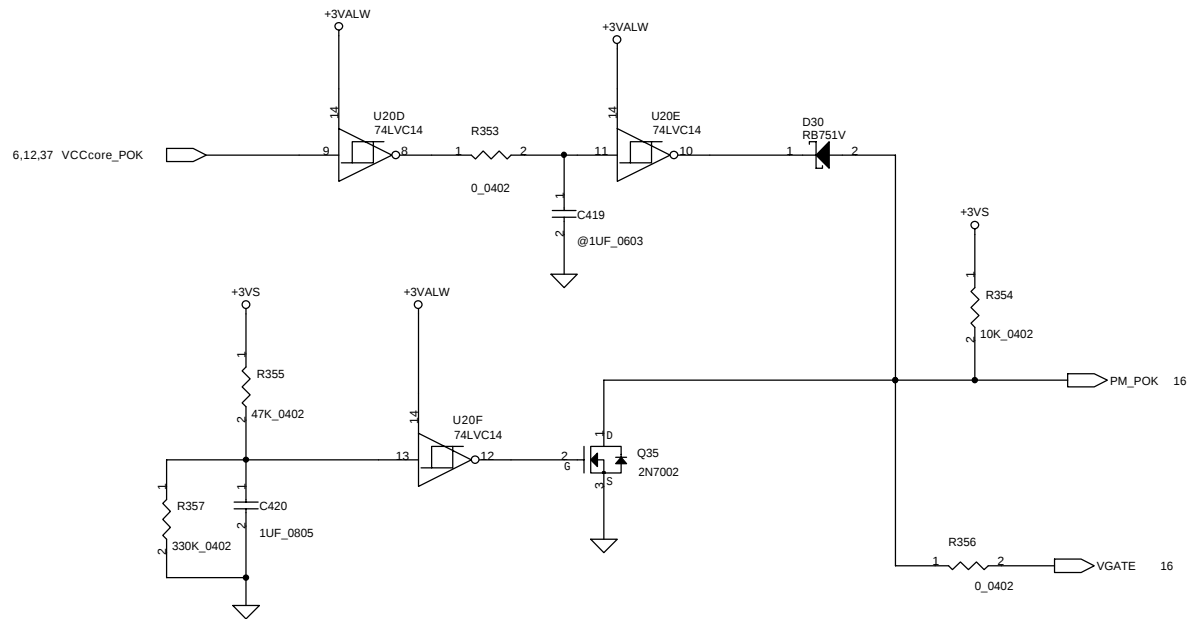


INPUT



OUTPUT

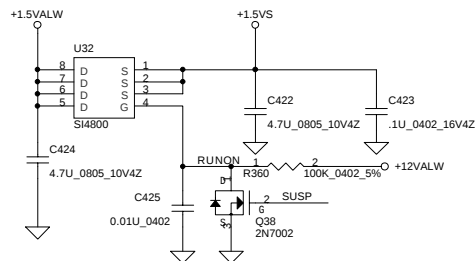




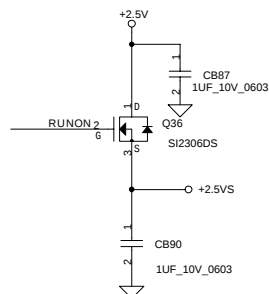
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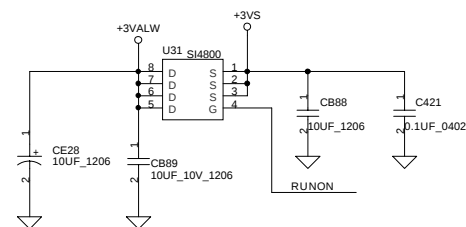
+1.5VALW To +1.5VS Transfer



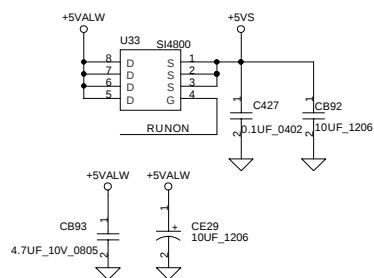
+2.5V to +2.5VS Transfer



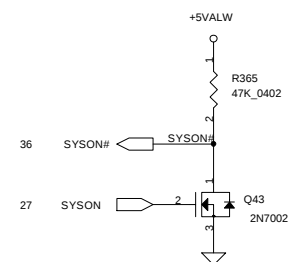
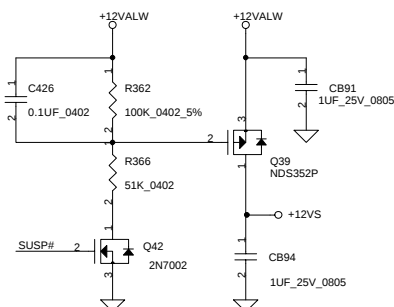
+3VALW to +3VS Transfer



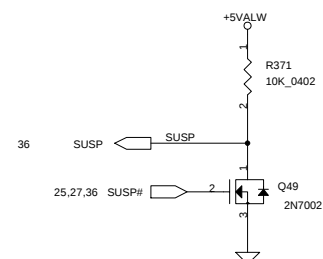
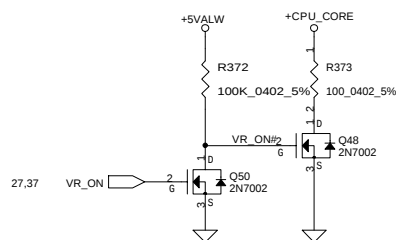
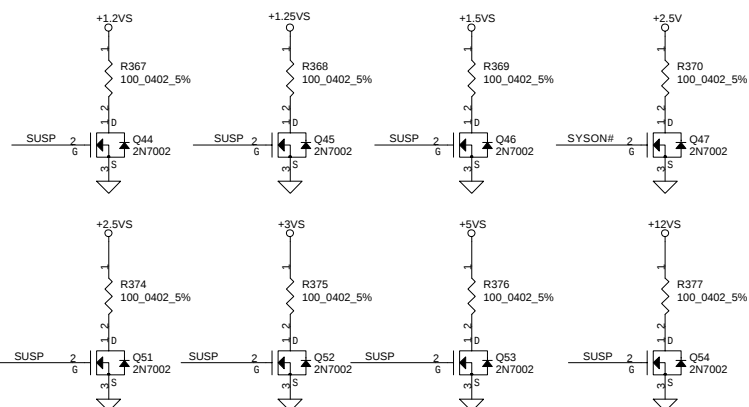
+5VALW to +5VS Transfer



+12VALW TO +12VS Transfer

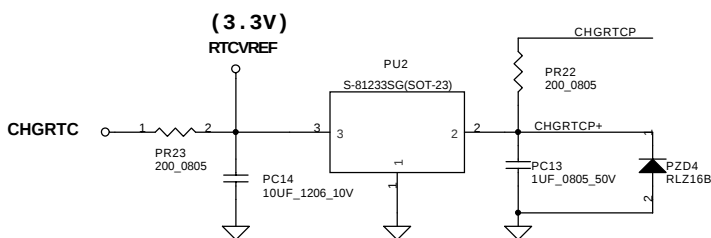
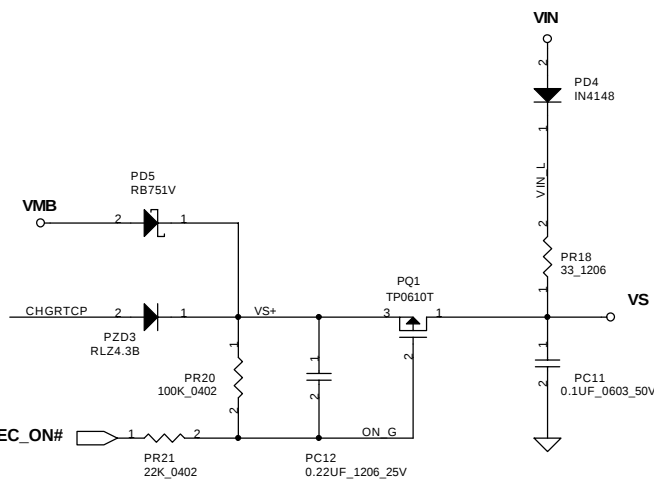
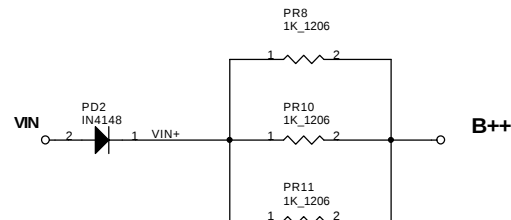
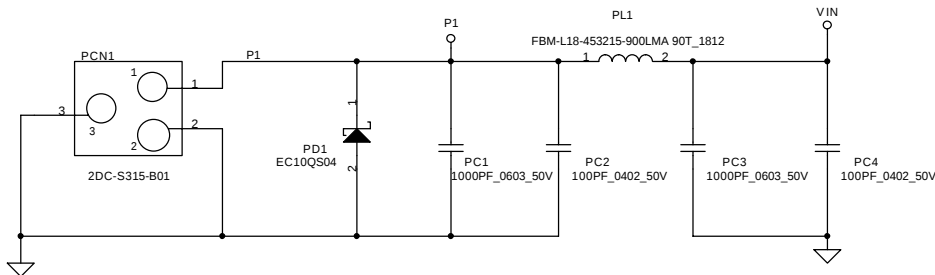


Discharge circuit



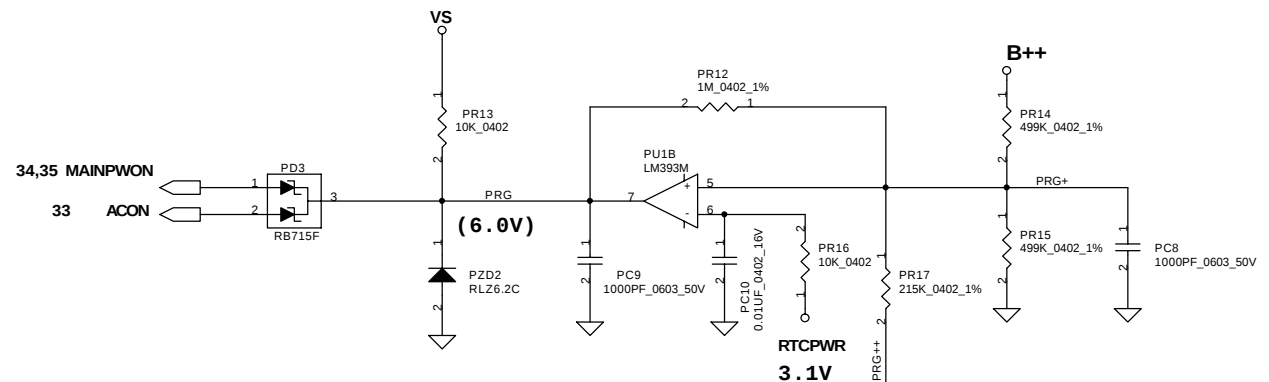
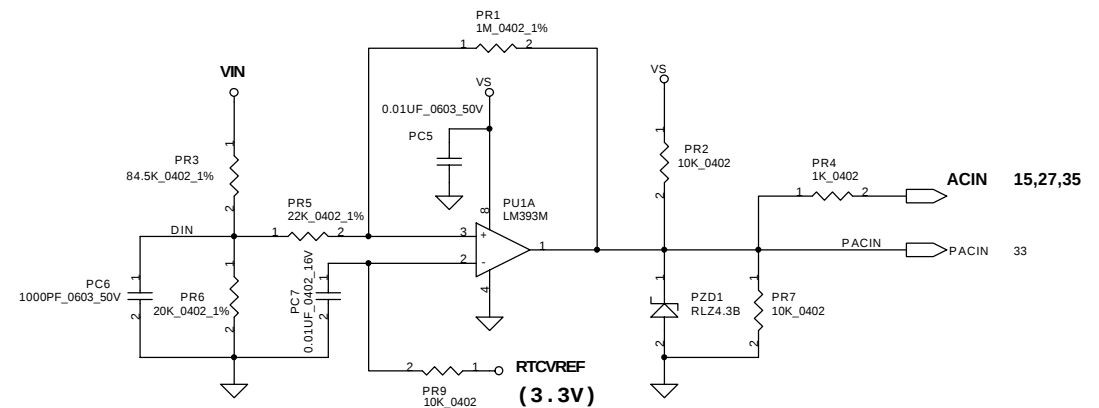
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Vin Detector

High 18.784 17.901 17.077 V
Low 17.877 17.043 16.195 V

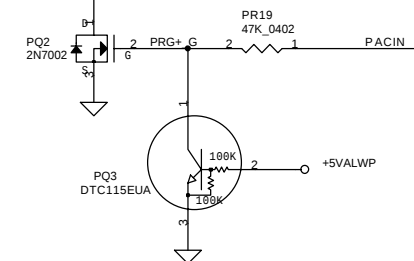


ACIN

Precharge detector
16.6 15.9 15.2
13.48 12.93 12.09

BAT ONLY

Precharge detector
8.597 8.247 7.904
6.310 6.101 5.683

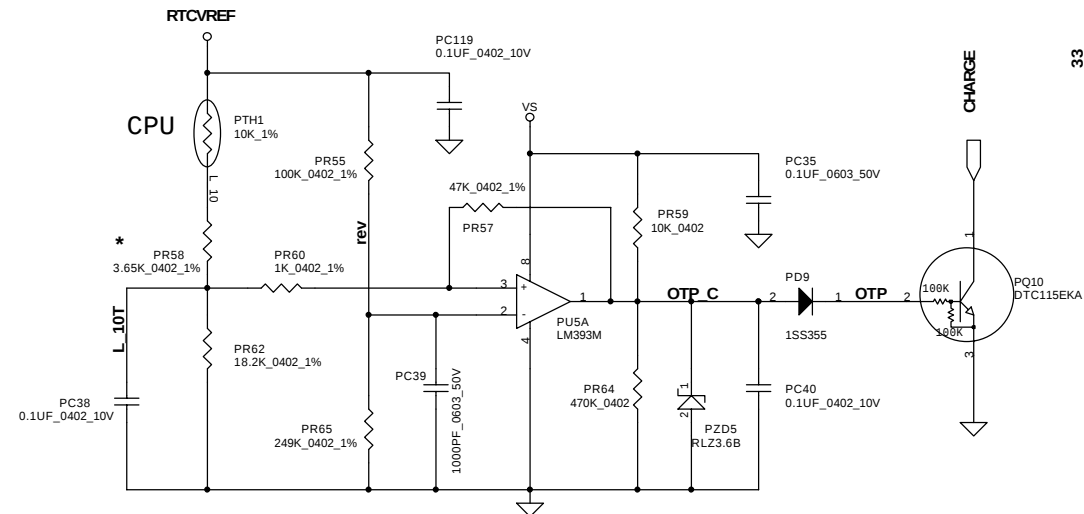
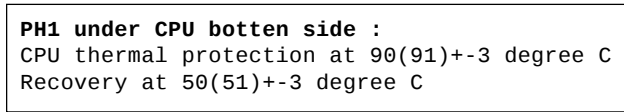


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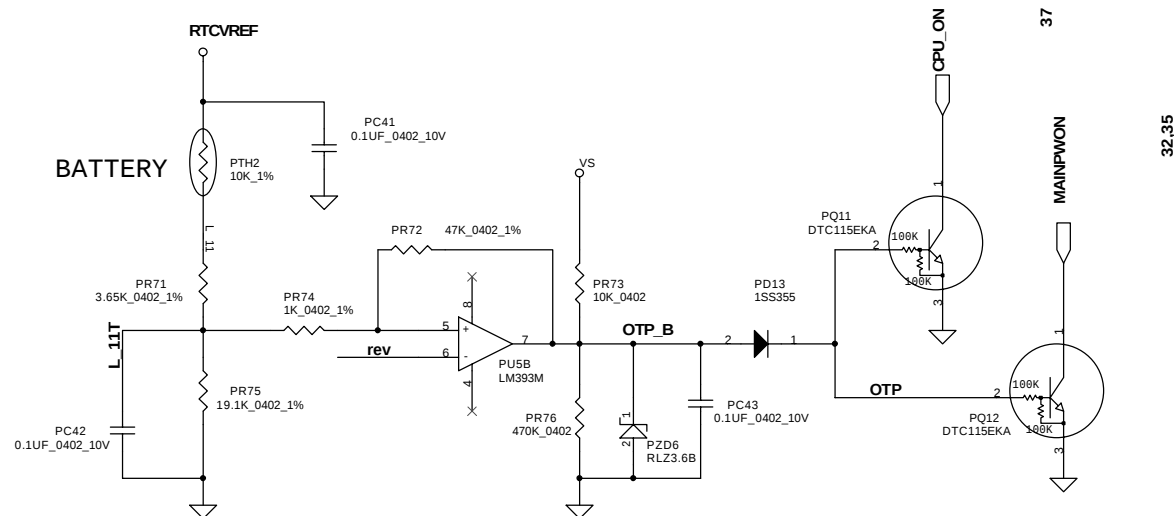
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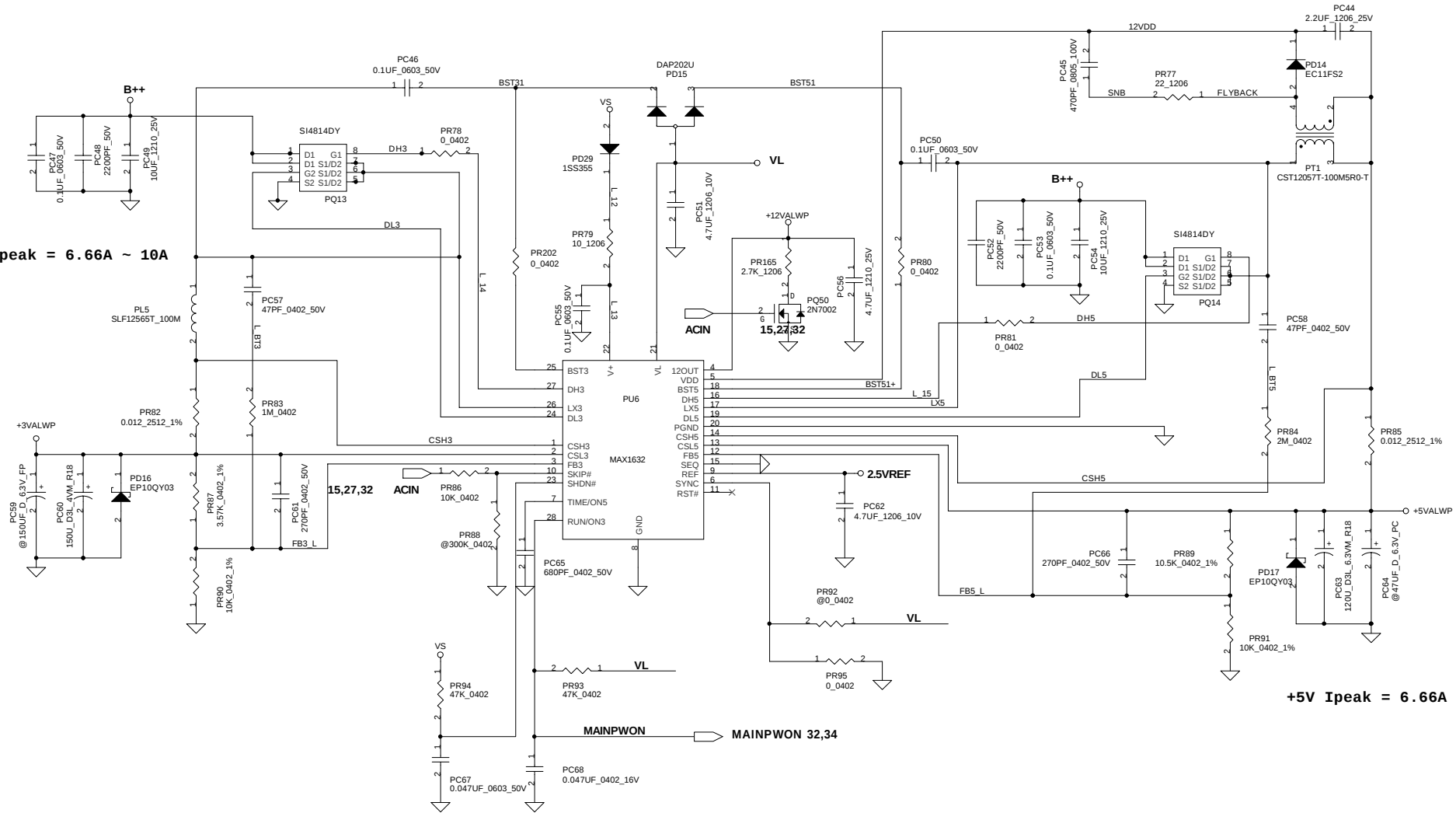
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PH2 near main Battery CONN :
BAT. thermal protection at 85(86)+-3 degree C
Recovery at 50(51) degree C



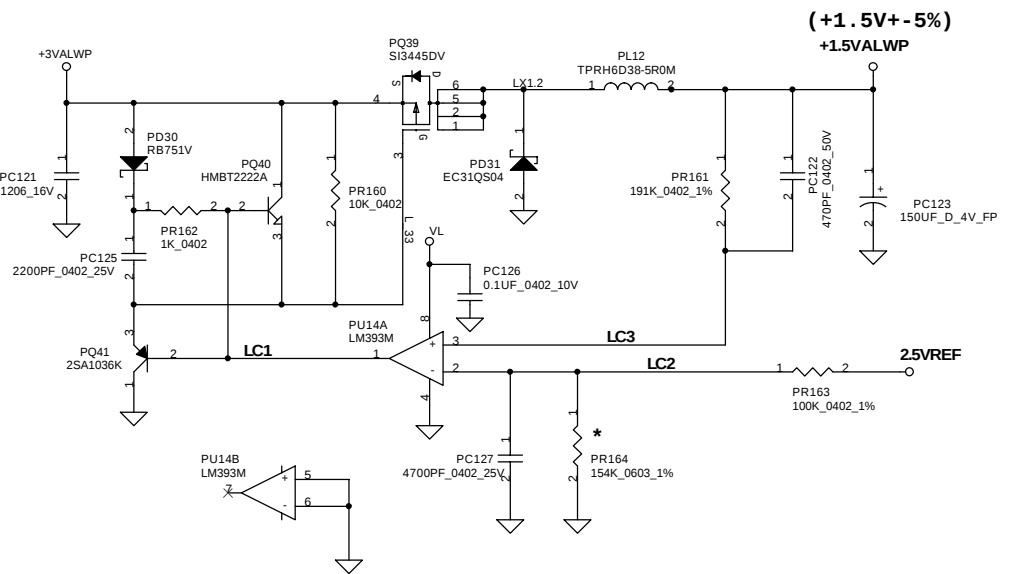
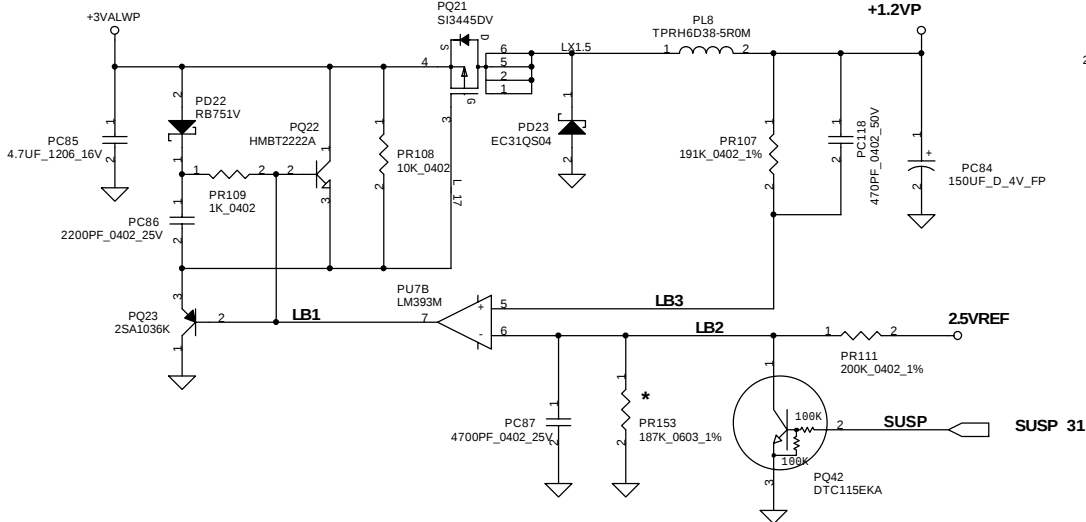
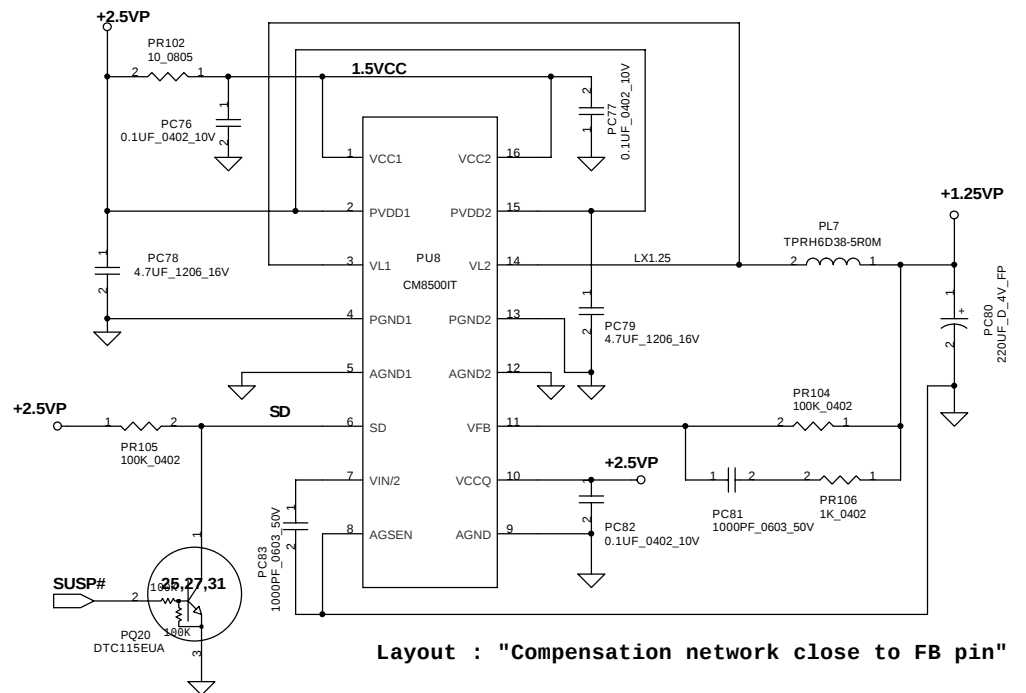
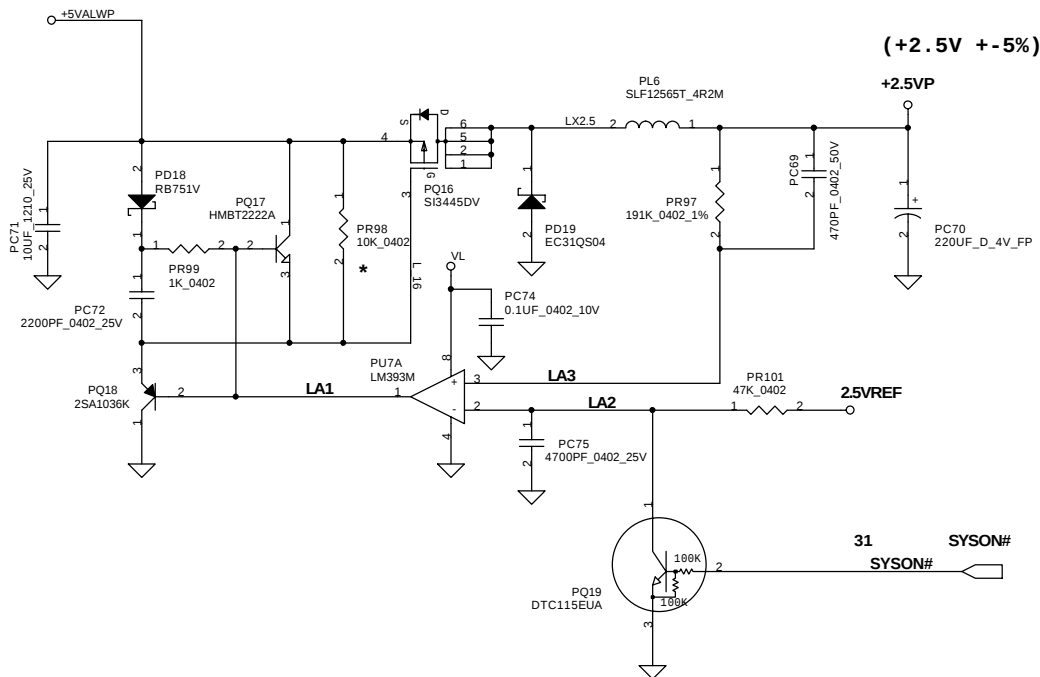
+3.3V Ipeak = 6.66A ~ 10A



+5V Ipeak = 6.66A ~ 10A

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	PM_SSMUXSEL	STP_CPU#	PM DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0	1.239V	4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0	1.144V	4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

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+3VALW/+5VALW/
+12VALW/+1.5VALW

PM_RSMRST#

>10 ms

ON/OFF

PWRBTN_OUT#

>1ms

110ms

SYSON / SUSP#

10ms

+1.25VS/+1.5VS/+2.5V/
+3VS/+5VS/+12VS

10ms

CLOCK

7.5ms

VR_ON

+1.2VPP

1.6ms

1ms

+CPU_CORE

VCCcore_P0K

3ms

PM_P0K/CPUPWRGD

1.3ms

PCIRST#

12ms

CPURST#

1ms

1ms

A-TEST (2002-09-09)

Fine tune power on sequence

- 1.C425 change to 0.01U
- 2.Delete R364
- 3.R396 change to 4.7K_0402
- 4.Delete R194
- 5.Delete R351
- 6.Delete R87
- 7.Delete R359 , Q37 , R361 , Q40 , R364 , C428 , R363 , Q41
- 8.Delete U10
- 9.Add D31

Page04 =To solve 4 sec shutdown restart issue : Delete Q3

Page03 = JP1 change to 3 pin connector(No PWM)

Page11 : EMI solution

- 1.Add U35 , L36 , C432 , R414 , R415 , R416

Page12 : TV-OUT issue

1. R107 , R108 changeto 4.7K

Page06 = Base on Intel spec : Delete Q6 , Q7 , R59 , R61 , C21, R87

Page20 = Delete R248 , C327

Page21 = R258 , R261 change to 47K_0402
Add R422 , R423 47K_0402
Delete R256 , C338

Page22 : Add R424 8.2K_0402

Page25 : Delete R298 , C372

Page28 : Add R420 pull low

Page29 : Add R421 , Q58

Page15 : Add R425 PULL UP

Page16 : Add R426 pull up , R427 pull down

B-TEST (2002-10-10)

Page08 : FB1,2,4,5 change to 0_0805

Page11 : R111 change to 1K_0402

Page12 : Del L36,C432,R414,R415,R416,U35,R148

Page16 : Add R428,R429 for FDD_DET#

Page23 : Add R195,C235
Del R273,R275
Add R281,C353

Page29 : Del R382,3,4,5,6,7. L30,31,32
Add RP129,130,131

Page30 : C420 change to 1UF_0805

B2-TEST (2002-12-26)

Page27 : Change RP125 to 10K

Page29 : Delete Q57, Q58 , R421 , R388 , R391

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