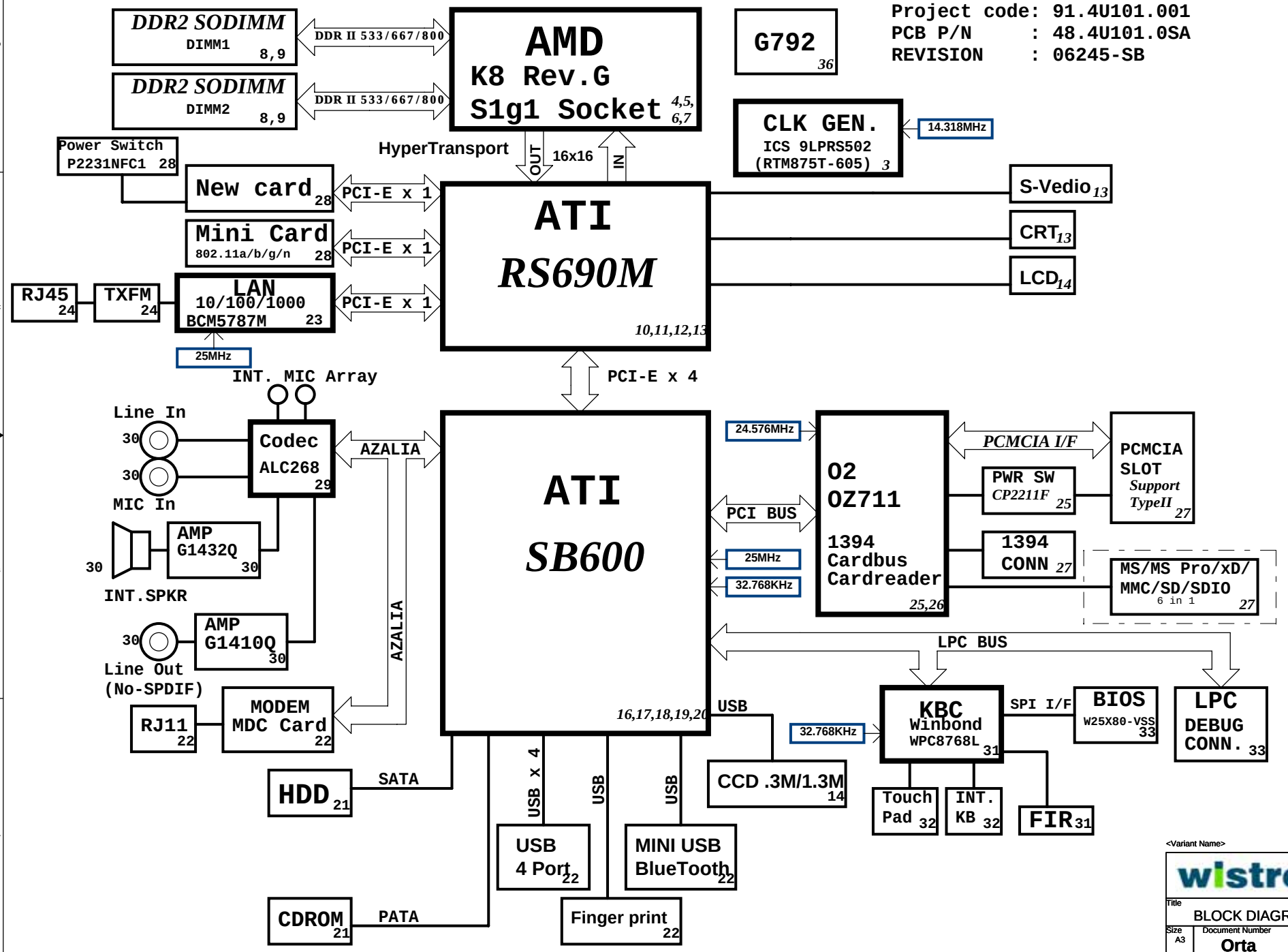
Orta Block Diagram



PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BLOCK DIAGRAM

Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 1 of 46

SA: 07/31/06 Start

SB change
power team
1.change L7, L9 to 68.1R510.10D
2.changge U12 to 84.04706.037
3.change R66 to 10K ohm

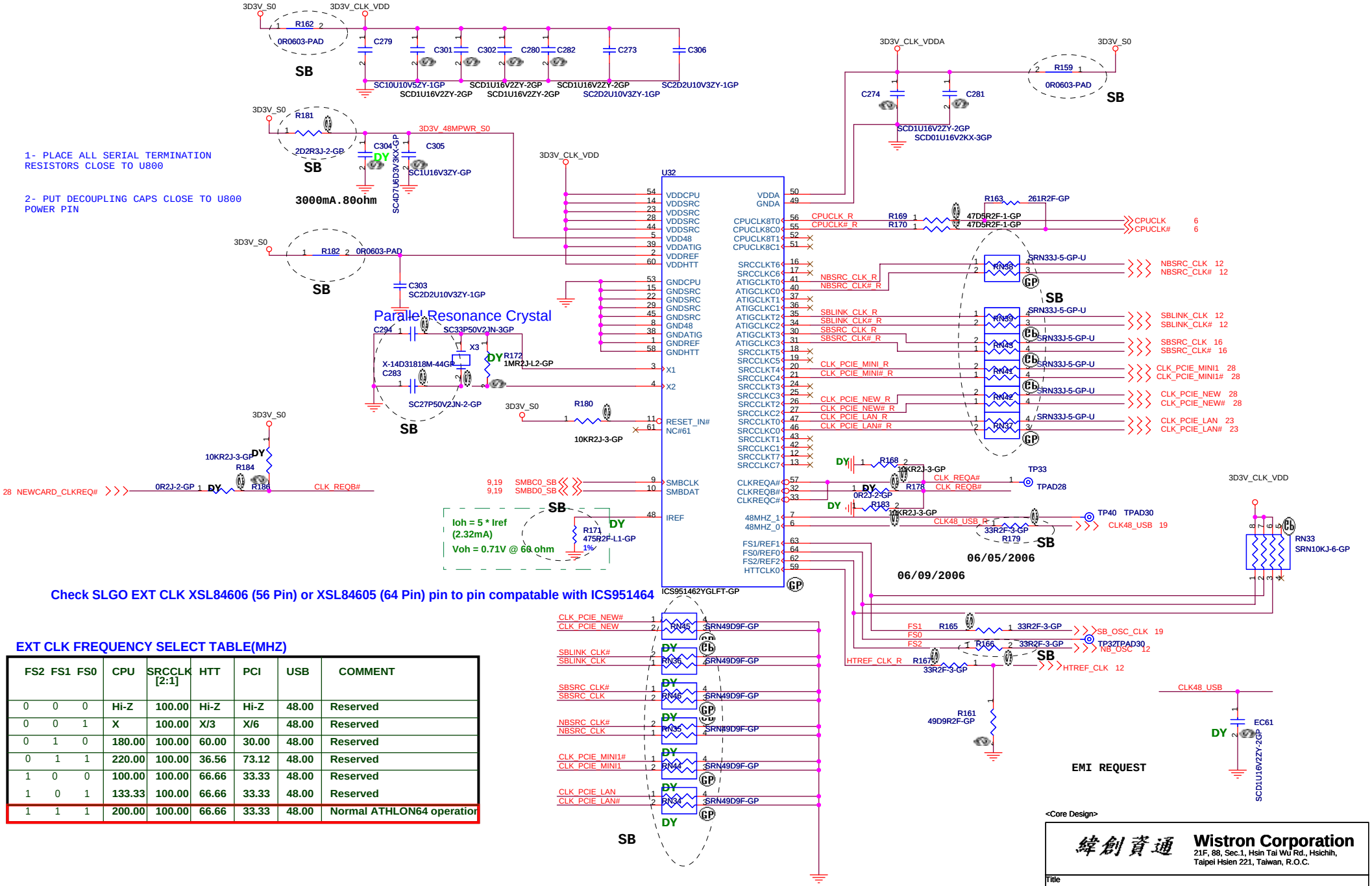
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHANGE HISTORY

Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 2 of 46



EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

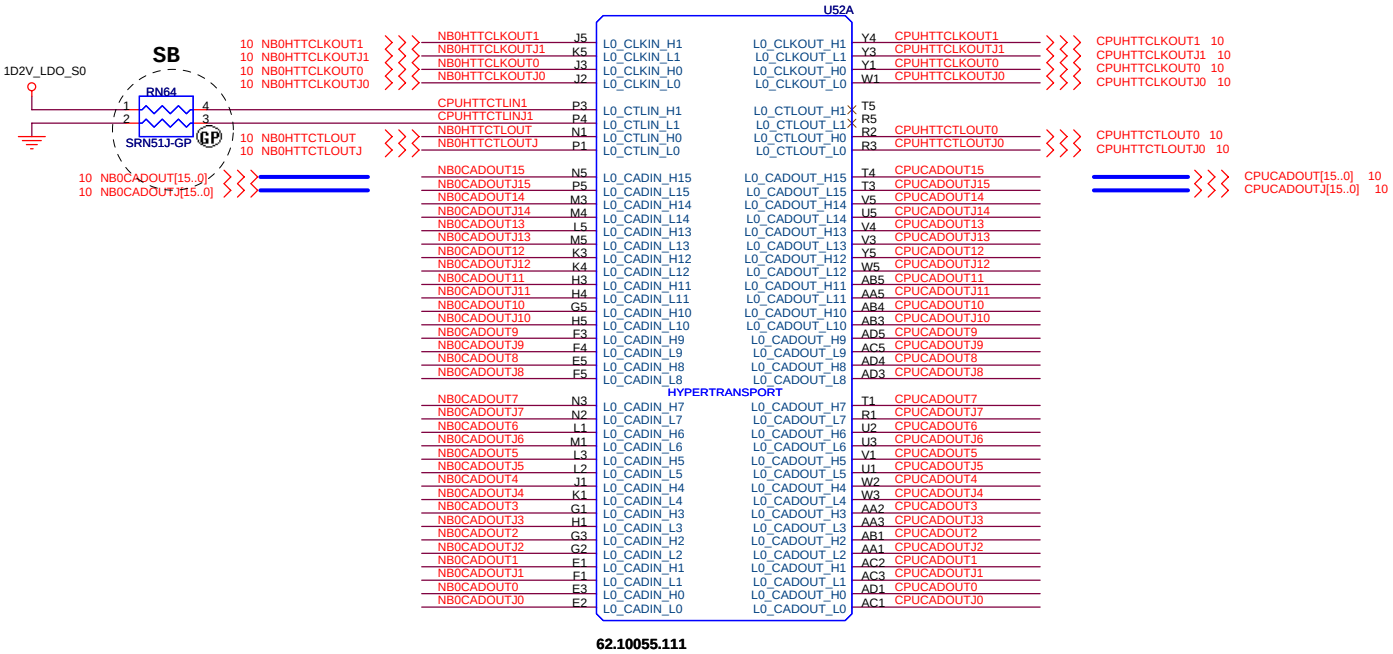
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS951412

Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 3 of 46



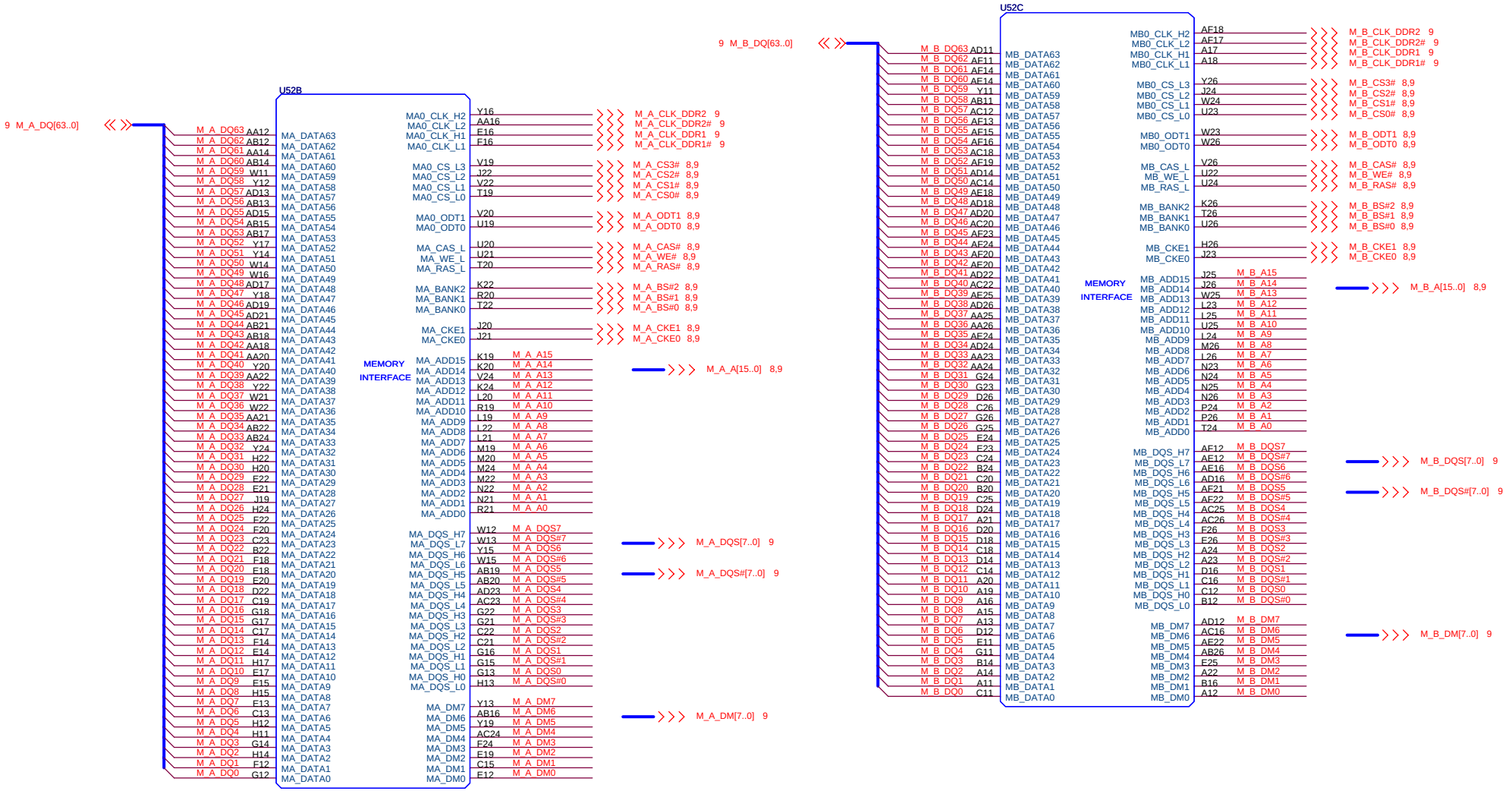
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(1/4)_HyperTransport I/F

Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 4 of 46



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(2/4)_DDR

Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 5 of 46

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

IF 0 ohm IS_NOT_GOOD ENOUGH, TRY 68.00082.491

Near To CPU

20061031 for Power Test

Remove these resistor when using EVT CPU

Change;Add

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

VREF_DDR_CLAW

LAYOUT: Locate close to CPU.

HDT Connectors

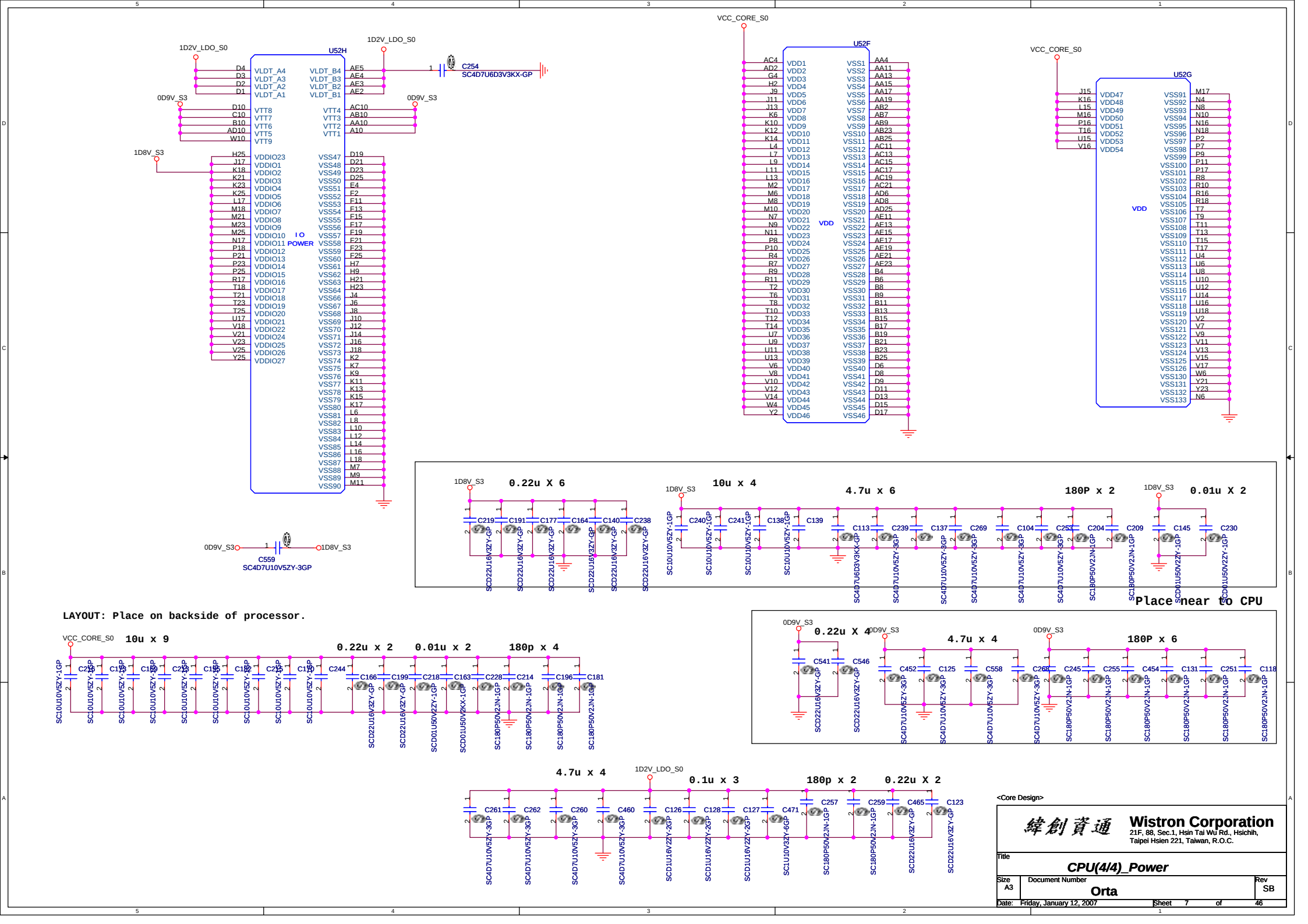
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(3/4)_Control & Debug

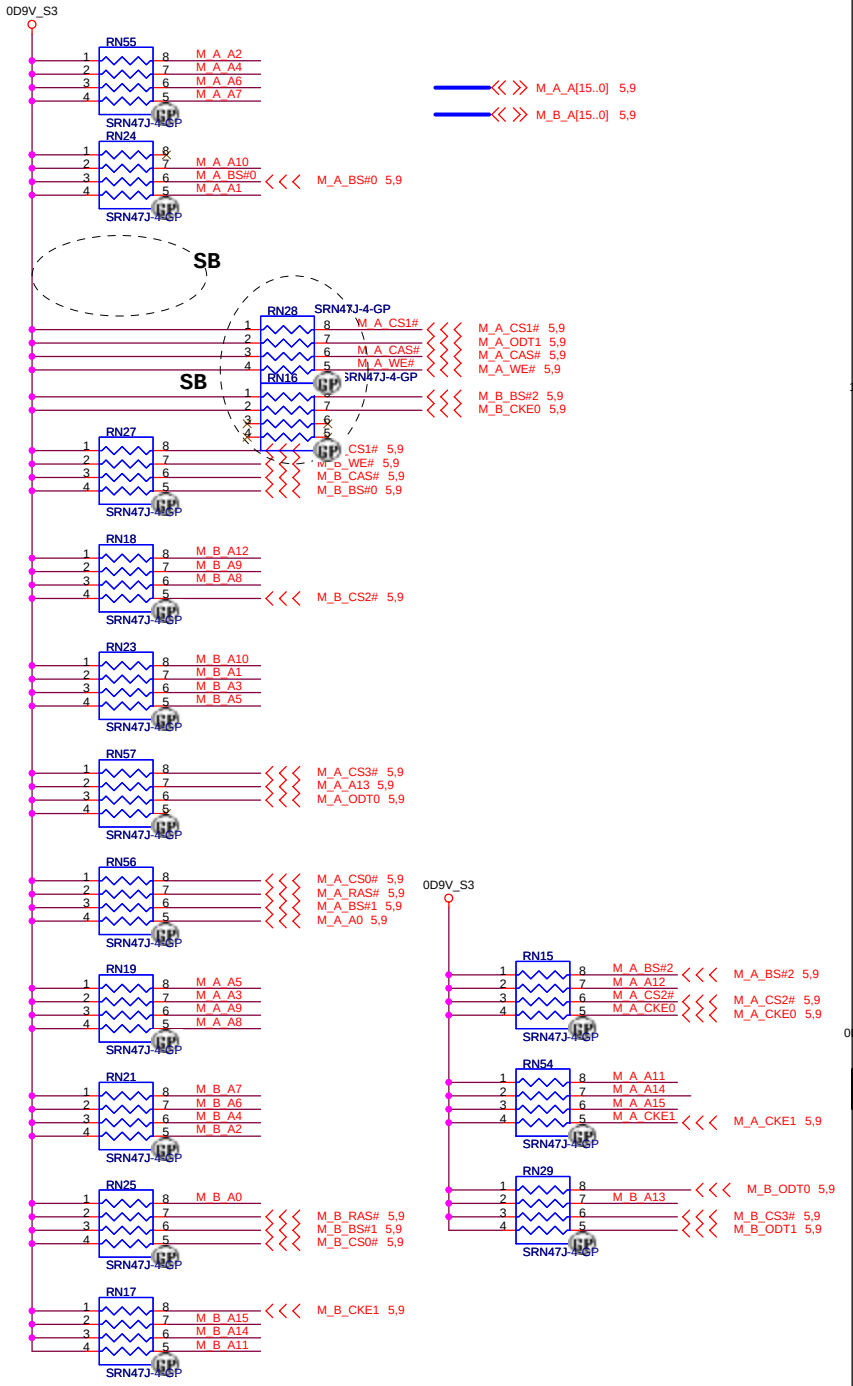
Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 6 of 46


1D2V_LDO_S0
U52H
VLDT_A4
VLDT_A3
VLDT_A2
VLDT_A1
VLDT_B4
VLDT_B3
VLDT_B2
VLDT_B1
C254
SC4D7U6D3V3KX-GP
0D9V_S3
VTT8
VTT7
VTT6
VTT5
VTT9
VTT4
VTT3
VTT2
VTT1
1D8V_S3
VDDIO23
VDDIO1
VDDIO2
VDDIO3
VDDIO4
VDDIO5
VDDIO6
VDDIO7
VDDIO8
VDDIO9
VDDIO10
VDDIO11
VDDIO12
VDDIO13
VDDIO14
VDDIO15
VDDIO16
VDDIO17
VDDIO18
VDDIO19
VDDIO20
VDDIO21
VDDIO22
VDDIO24
VDDIO25
VDDIO26
VDDIO27
I O
POWER
VSS47
VSS48
VSS49
VSS50
VSS51
VSS52
VSS53
VSS54
VSS55
VSS56
VSS57
VSS58
VSS59
VSS60
VSS61
VSS62
VSS63
VSS64
VSS66
VSS67
VSS68
VSS69
VSS70
VSS71
VSS72
VSS73
VSS74
VSS75
VSS76
VSS77
VSS78
VSS79
VSS80
VSS81
VSS82
VSS83
VSS84
VSS85
VSS86
VSS87
VSS88
VSS89
VSS90
C559
SC4D7U10V5ZY-3GP
VCC_CORE_S0
U52F
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDD10
VDD11
VDD12
VDD13
VDD14
VDD15
VDD16
VDD17
VDD18
VDD19
VDD20
VDD21
VDD22
VDD23
VDD24
VDD25
VDD26
VDD27
VDD28
VDD29
VDD30
VDD31
VDD32
VDD33
VDD34
VDD35
VDD36
VDD37
VDD38
VDD39
VDD40
VDD41
VDD42
VDD43
VDD44
VDD45
VDD46
VDD
VSS1
VSS2
VSS3
VSS4
VSS5
VSS6
VSS7
VSS8
VSS9
VSS10
VSS11
VSS12
VSS13
VSS14
VSS15
VSS16
VSS17
VSS18
VSS19
VSS20
VSS21
VSS22
VSS23
VSS24
VSS25
VSS26
VSS27
VSS28
VSS29
VSS30
VSS31
VSS32
VSS33
VSS34
VSS35
VSS36
VSS37
VSS38
VSS39
VSS40
VSS41
VSS42
VSS43
VSS44
VSS45
VSS46
VCC_CORE_S0
U52G
VDD47
VDD48
VDD49
VDD50
VDD51
VDD52
VDD53
VDD54
VDD
VSS91
VSS92
VSS93
VSS94
VSS95
VSS96
VSS97
VSS98
VSS99
VSS100
VSS101
VSS102
VSS103
VSS104
VSS105
VSS106
VSS107
VSS108
VSS109
VSS110
VSS111
VSS112
VSS113
VSS114
VSS115
VSS116
VSS117
VSS118
VSS119
VSS120
VSS121
VSS122
VSS123
VSS124
VSS125
VSS126
VSS130
VSS131
VSS132
VSS133
1D8V_S3
0.22u X 6
C219
C191
C177
C164
C140
C238
SCD22U16V3ZY-GP
10u x 4
C240
C241
C138
C139
SC10U10V5ZY-1GP
4.7u x 6
C113
C239
C137
C269
C104
C253
C204
C209
SC4D7U10V5ZY-3GP
180P x 2
SC180P50V2JN-1GP
0.01u X 2
C145
C230
SCD01U50V2ZY-1GP
Place near to CPU
LAYOUT: Place on backside of processor.
VCC_CORE_S0
10u x 9
C250
C249
C248
C247
C246
C244
SC10U10V5ZY-1GP
0.22u x 2
C166
C199
SCD22U16V3ZY-GP
0.01u x 2
C218
C163
SCD01U50V2KX-1GP
180p x 4
C228
C214
C196
C181
SC180P50V2JN-1GP
0D9V_S3
0.22u X 4
C541
C546
4.7u x 4
C452
C125
C558
C268
SC4D7U10V5ZY-3GP
180P x 6
C245
C255
C454
C131
C251
C118
4.7u x 4
1D2V_LDO_S0
0.1u x 3
180p x 2
0.22u X 2
C261
C262
C260
C460
C126
C128
C127
C471
C257
C259
C465
C123
SC4D7U10V5ZY-3GP
SCD1U16V2ZY-2GP
SC1U10V3ZY-6GP
SC180P50V2JN-1GP
SCD22U16V3ZY-GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU(4/4)_Power
Size
A3
Document Number
Orta
Rev
SB
Date: Friday, January 12, 2007
Sheet 7 of 46

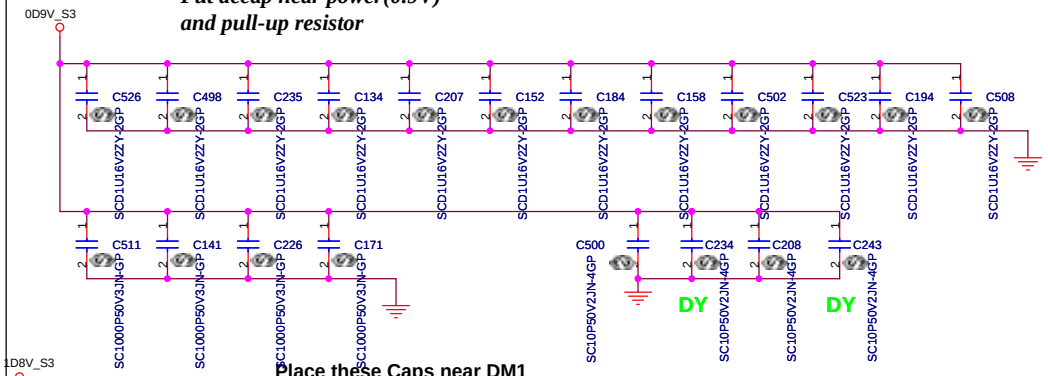
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

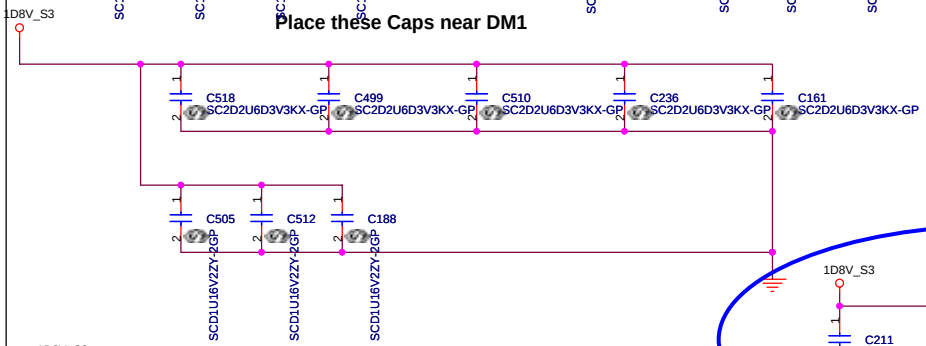


Decoupling Capacitor

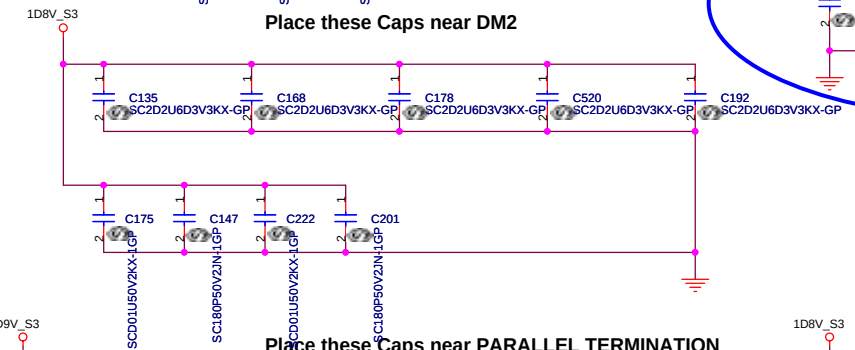
Put decap near power(0.9V) and pull-up resistor

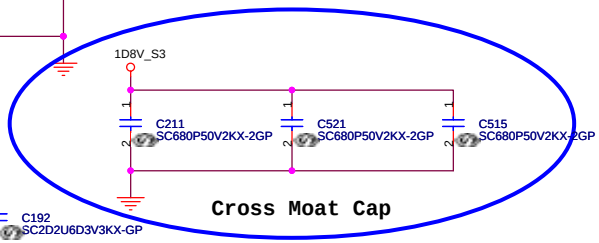


Place these Caps near DM1

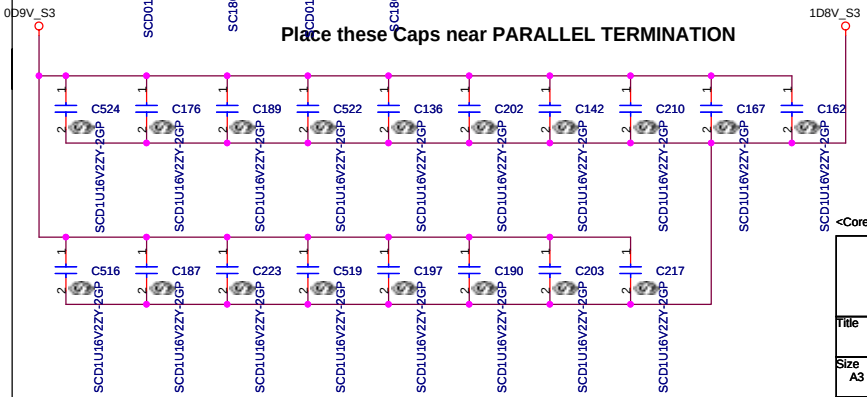


Place these Caps near DM2





Place these Caps near PARALLEL TERMINATION



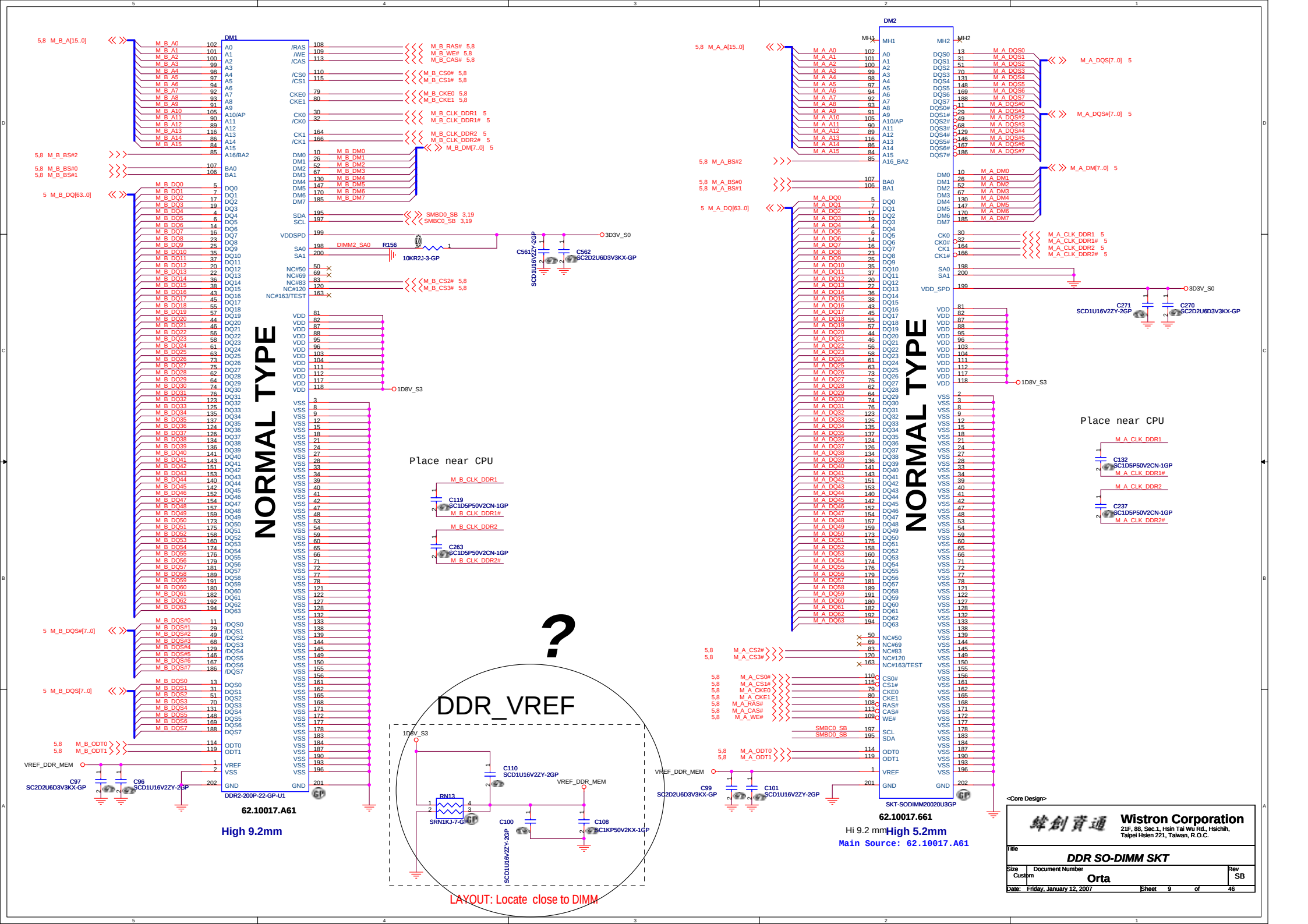
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR DAMPING & TERMINATION

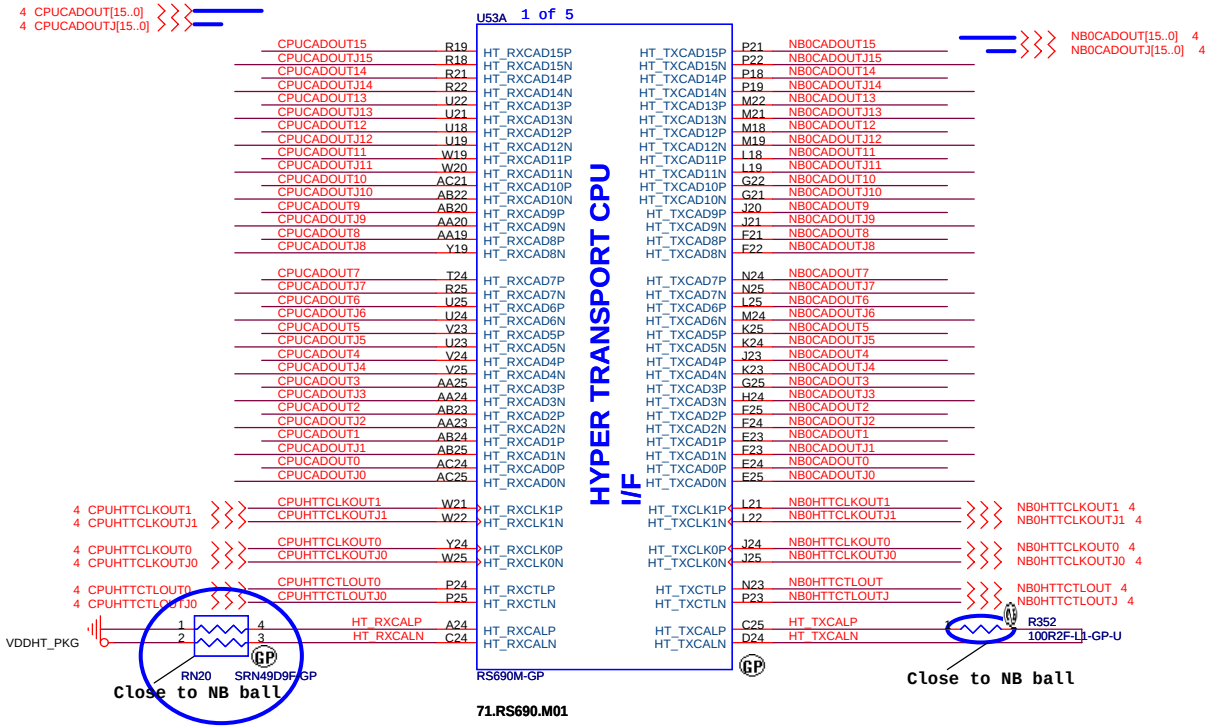
Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 8 of 46


DM1
NORMAL TYPE
DDR2-200P-22-GP-U1
62.10017.A61
High 9.2mm
Place near CPU
C119 SC1D5P50V2CN-1GP
C263 SC1D5P50V2CN-1GP
C97 SC2D2U6D3V3KX-GP
C96 SCD1U16V2ZY-2GP
R156 10KR2J-3-GP
C561 SCD1U16V2ZY-2GP
C562 SC2D2U6D3V3KX-GP
?
DDR_VREF
RN13 SRN1KJ-7-GP
C110 SCD1U16V2ZY-2GP
C100 SCD1U16V2ZY-2GP
C108 SC1KP50V2KX-1GP
LAYOUT: Locate close to DIMM
DM2
NORMAL TYPE
SKT-SODIMM20020U3GP
62.10017.661
Hi 9.2 mm High 5.2mm
Main Source: 62.10017.A61
C99 SC2D2U6D3V3KX-GP
C101 SCD1U16V2ZY-2GP
C271 SCD1U16V2ZY-2GP
C270 SC2D2U6D3V3KX-GP
C132 SC1D5P50V2CN-1GP
C237 SC1D5P50V2CN-1GP
Place near CPU
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR SO-DIMM SKT
Size Custom
Document Number Orta
Rev SB
Date: Friday, January 12, 2007
Sheet 9 of 46

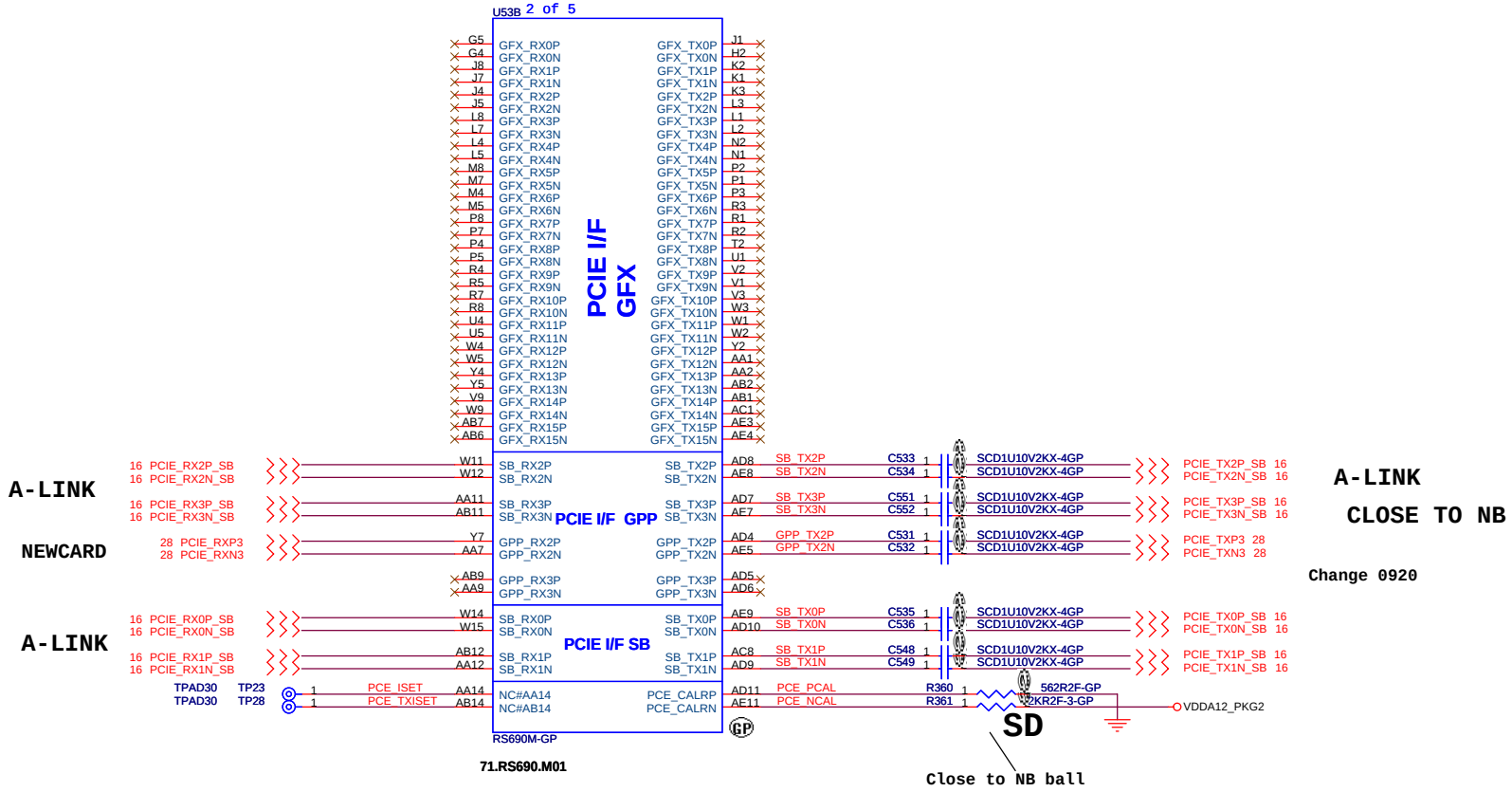
CLAW HAMMER TO NB

NB TO CLAW HAMMER



<Core Design>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	NB-RS690M_HT
Size A3 / Document Number	Orta / Rev SB
Date: Friday, January 12, 2007	Sheet 10 of 46



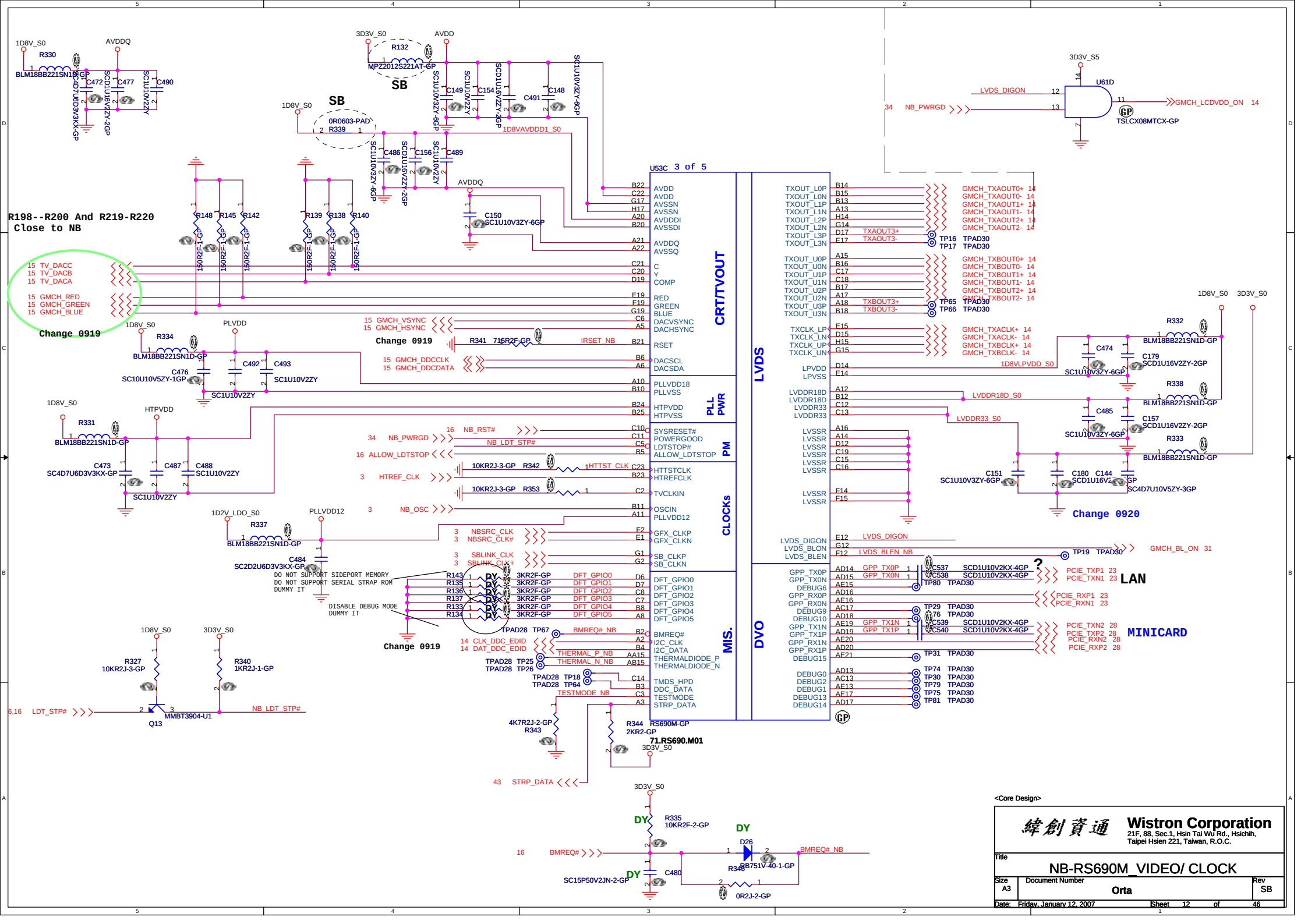
<Core Design>

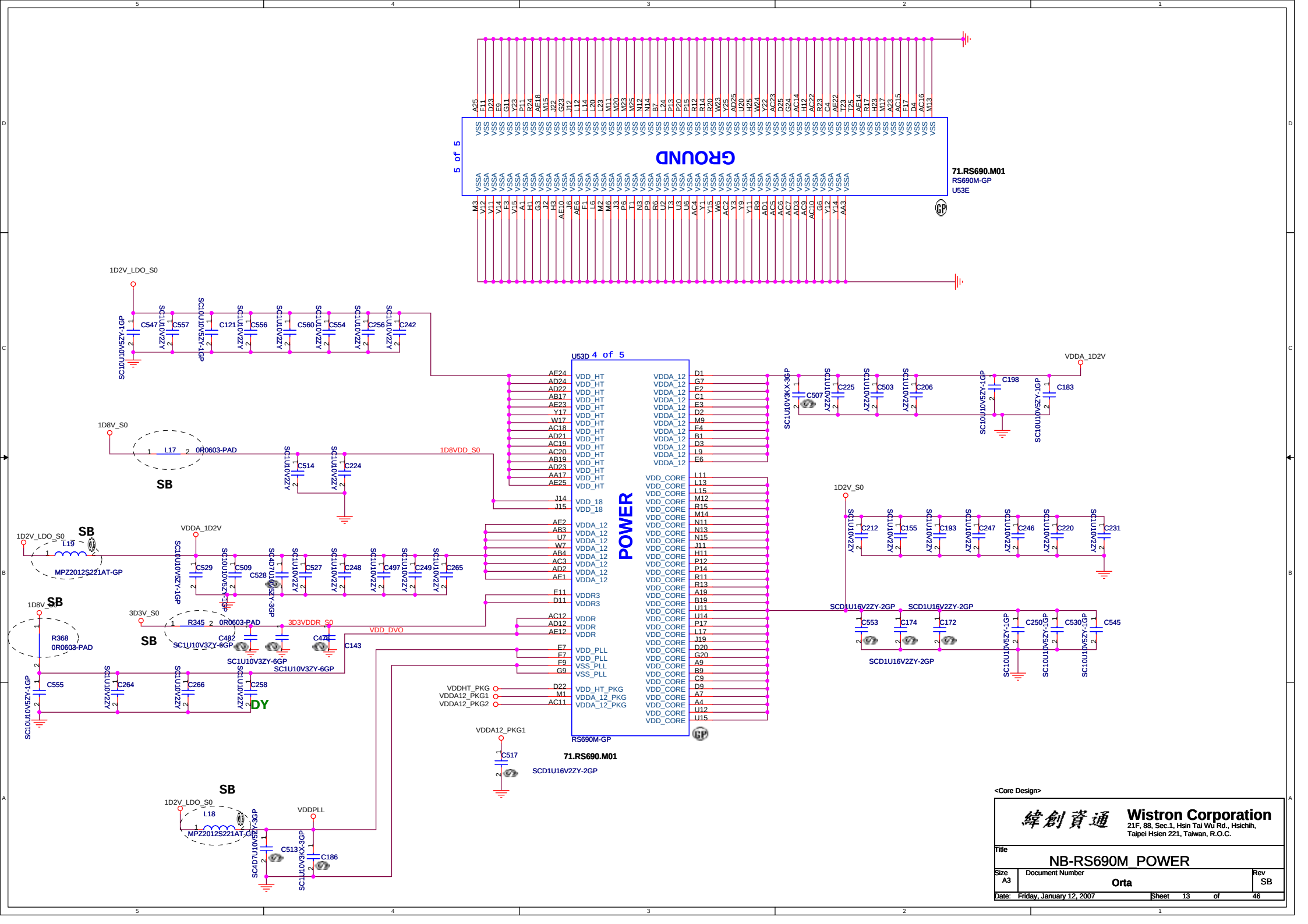
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

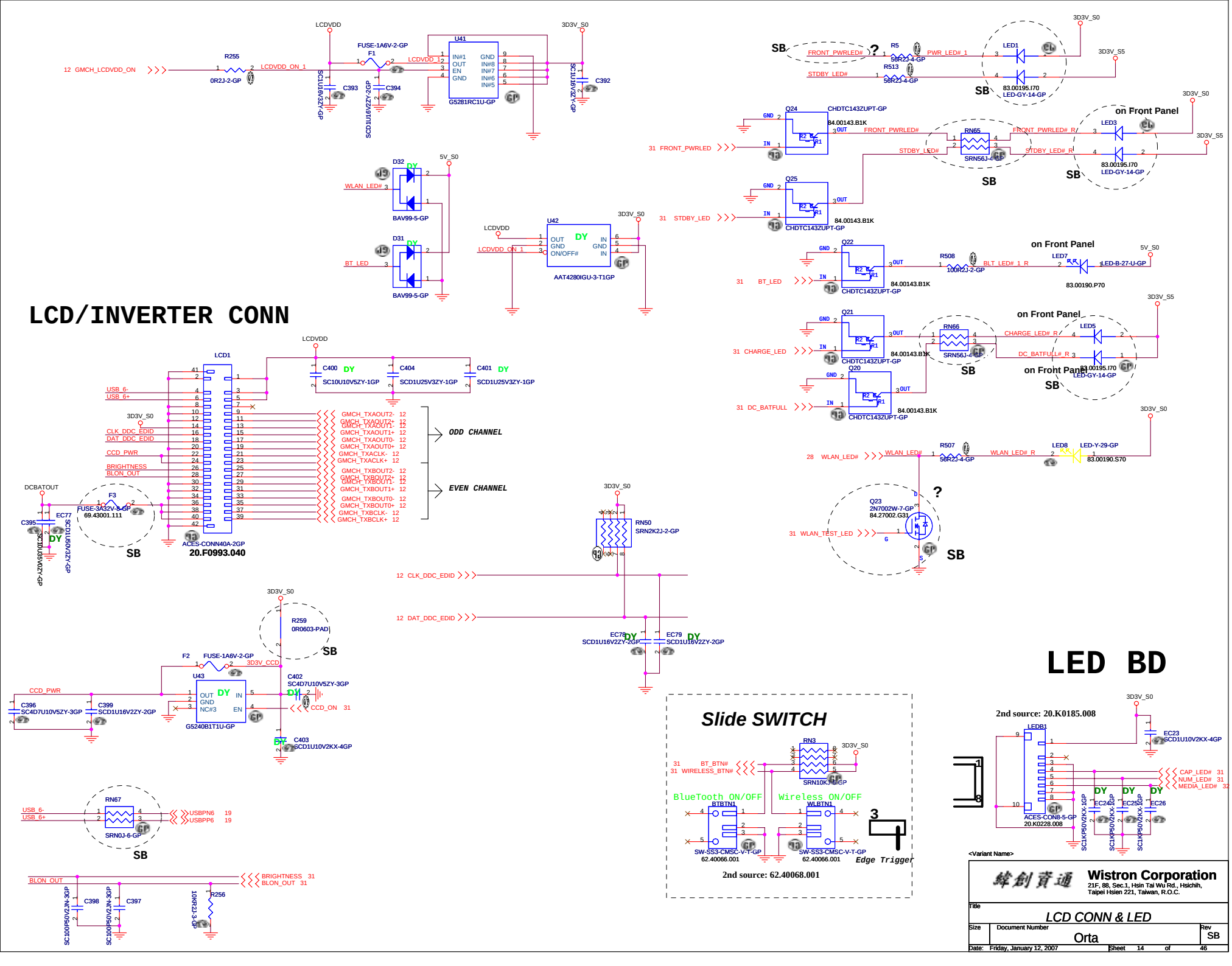
Title: NB-RS690M_MEM/PCIE_LINK I/F

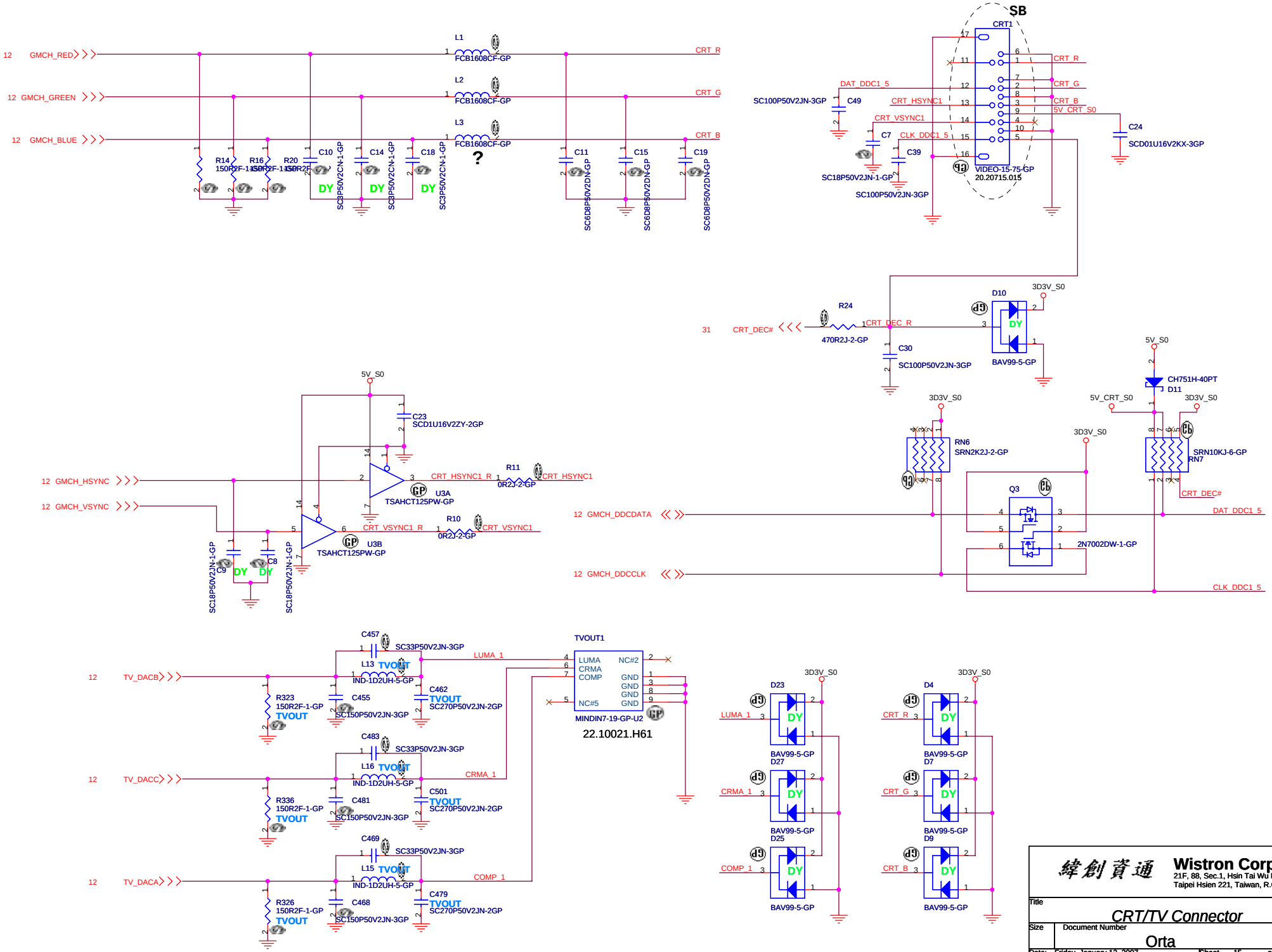
Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 11 of 46


R198--R200 And R219-R220
Close to NB
Change 0919
Change 0920
SB
U53C 3 of 5
CRT/TVOUT
PLL PWR
PM
CLOCKs
MIS.
LVDS
DVO
71.RS690.M01
LAN
MINICARD
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
NB-RS690M_VIDEO/ CLOCK
Orta
Size A3
Rev SB
Date: Friday, January 12, 2007
Sheet 12 of 46


GROUND
5 of 5
71.RS690.M01
RS690M-GP
U53E
POWER
U53D 4 of 5
RS690M-GP
71.RS690.M01
1D2V_LDO_S0
1D8V_S0
1D8VDD_S0
VDDA_1D2V
1D2V_S0
3D3V_S0
3D3VDDR_S0
VDD_DVO
VDDPLL
VDDA12_PKG1
VDDA12_PKG2
VDDHT_PKG
SB
DY
0R0603-PAD
MPZ2012S221AT-GP
SC1U10V3ZY-6GP
SC1U10V5ZY-1GP
SC1U10V2ZY
SCD1U16V2ZY-2GP
SC4D7U10V5ZY-3GP
SC1U10V3KX-3GP
SC1U10V3KX-3GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS690M_POWER
Size A3
Document Number
Orta
Rev SB
Date: Friday, January 12, 2007
Sheet 13 of 46


LCD/INVERTER CONN
LED BD
Slide SWITCH
ODD CHANNEL
EVEN CHANNEL
BlueTooth ON/OFF
Wireless ON/OFF
Edge Trigger
2nd source: 62.40068.001
2nd source: 20.K0185.008
20.F0993.040
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LCD CONN & LED
Orta
Friday, January 12, 2007
Sheet 14 of 46



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	*CRT/TV Connector*		
Size	Document Number: Orta		Rev: SB
Date: Friday, January 12, 2007	Sheet 15 of 46		

Place these components close to U13
and use groud guard for 32K_X1 and 32K_X2.

SB600 asserts PLTRST# to reset
devices on the platform.

PCIRST

Change 0921

<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	SB600 PCI/CPU/LPC/RTC (1 of 5)
Size A3	Document Number: Orta
Rev	SB
Date: Friday, January 12, 2007	Sheet 16 of 46

SB
62.70001.011

71.SB600.00U

2nd source: 20.D0198.103

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB460

SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP
SCD01U50V2KX-1GP

U57B 2 of 4

SATA_TXP0 SATA_TXN0 SATA_RXN0 SATA_RXP0

SATA_TXP0_SB SATA_TXN0_SB SATA_RXN0_SB SATA_RXP0_SB

C586 C587 C590 C593

SATA_TX0+ SATA_TX0- SATA_RX0- SATA_RX0+ SATA_TX1+ SATA_TX1- SATA_RX1- SATA_RX1+ SATA_TX2+ SATA_TX2- SATA_RX2- SATA_RX2+ SATA_TX3+ SATA_TX3- SATA_RX3- SATA_RX3+

SATA_CAL SATA_X1 SATA_X2 SATA_ACT#/GPIO67

SERIAL ATA

SATA

SATA_X1 SATA_X2

R381 1MR2J-L2-GP

XTAL-25MHZ-67GP

C582 SC12P50V2JN-3GP C576 SC10P50V2JN-4GP

According to PA_IXP600AD9
Change C936 and C937 from 27P to 10P.

R397 1KR2F-3-GP

3D3V_S0

R191 10KR2J-3-GP

SATA_LED# 32

PLLVDD_ATA XTLVDD_ATA AVDD_SATA

PLLVDD_SATA XTLVDD_SATA AVDD_SATA

SERIAL ATA POWER

AVSS_SATA

ATA 66/100

IDE_IORDY IDE_IRQ IDE_A0 IDE_A1 IDE_A2 IDE_DACK# IDE_DRQ IDE_IOR# IDE_IOW# IDE_CS1# IDE_CS3#

IDE_PDIORDY INT_IRQ14 IDE_PDA0 IDE_PDA1 IDE_PDA2 IDE_PDDACK# IDE_PDDREQ IDE_PDIOR# IDE_PDIOW# IDE_PDCS1# IDE_PDCS3#

IDE_D0/GPIO15 IDE_D1/GPIO16 IDE_D2/GPIO17 IDE_D3/GPIO18 IDE_D4/GPIO19 IDE_D5/GPIO20 IDE_D6/GPIO21 IDE_D7/GPIO22 IDE_D8/GPIO23 IDE_D9/GPIO24 IDE_D10/GPIO25 IDE_D11/GPIO26 IDE_D12/GPIO27 IDE_D13/GPIO28 IDE_D14/GPIO29 IDE_D15/GPIO30

IDE_PDD0 IDE_PDD1 IDE_PDD2 IDE_PDD3 IDE_PDD4 IDE_PDD5 IDE_PDD6 IDE_PDD7 IDE_PDD8 IDE_PDD9 IDE_PDD10 IDE_PDD11 IDE_PDD12 IDE_PDD13 IDE_PDD14 IDE_PDD15

SPI ROM

SPI_DI/GPIO12 SPI_DO/GPIO11 SPI_CLK/GPIO47 SPI_HOLD#/GPIO31 SPI_CS#/GPIO32 LAN_RST#/GPIO13 ROM_RST#/GPIO14

TP54 TP45 TP50 TP101 TP46 TP41 TP47 TPAD30

HW MONITOR

FANOUT0/GPIO3 FANOUT1/GPIO48 FANOUT2/GPIO49 FANIN0/GPIO50 FANIN1/GPIO51 FANIN2/GPIO52 TEMP_COMM TEMPIN0/GPIO61 TEMPIN1/GPIO62 TEMPIN2/GPIO63 TEMPIN3/TALERT#/GPIO64 VIN0/GPIO53 VIN1/GPIO54 VIN2/GPIO55 VIN3/GPIO56 VIN4/GPIO57 VIN5/GPIO58 VIN6/GPIO59 VIN7/GPIO60

ALERT# 6,35 PSW_CLR# UMA_DIS CLK_ID FP_ID FP_ID 32 FP_DETECT# 32

AVDD AVSS

SB600-GP

71.SB600.00U

SB

3D3V_S0 XTLVDD_ATA R187 0R0603-PAD EC117 SCD1U16V2ZY-2GP C318 SC2D2U6D3V3KX-GP

1D2V_LDO_S0 PLLVDD_ATA R193 0R0603-PAD EC118 SCD1U16V2ZY-2GP C320 SC2D2U6D3V3KX-GP

1D2V_LDO_S0 R177 0R0603-PAD EC114 SCD1U16V2ZY-2GP C311 SC10U6D3V5KX-1GP

AVDD_SATA C307 SC10U6D3V5KX-1GP EC63 EC65 EC62 EC60 EC64 SCD1U16V2ZY-2GP DY

SATA

SB

3D3V_S0 R149 10KR2J-3-GP R519 10KR2J-3-GP

FP_DETECT# PSW_CLR#

G41 GAP-OPEN

0 => DIS
1 => UMA

3D3V_S0 R214 10KR2J-3-GP R197 RTL R198 DY

UMA_DIS CLK_ID FP_ID

R217 DY R206 ICS R207 DY

AVDD_HWM 3D3V_S0 R432 0R3-0-U-GP

C613 SCD1U16V2ZY-2GP C614 SC2D2U6D3V3KX-GP DY

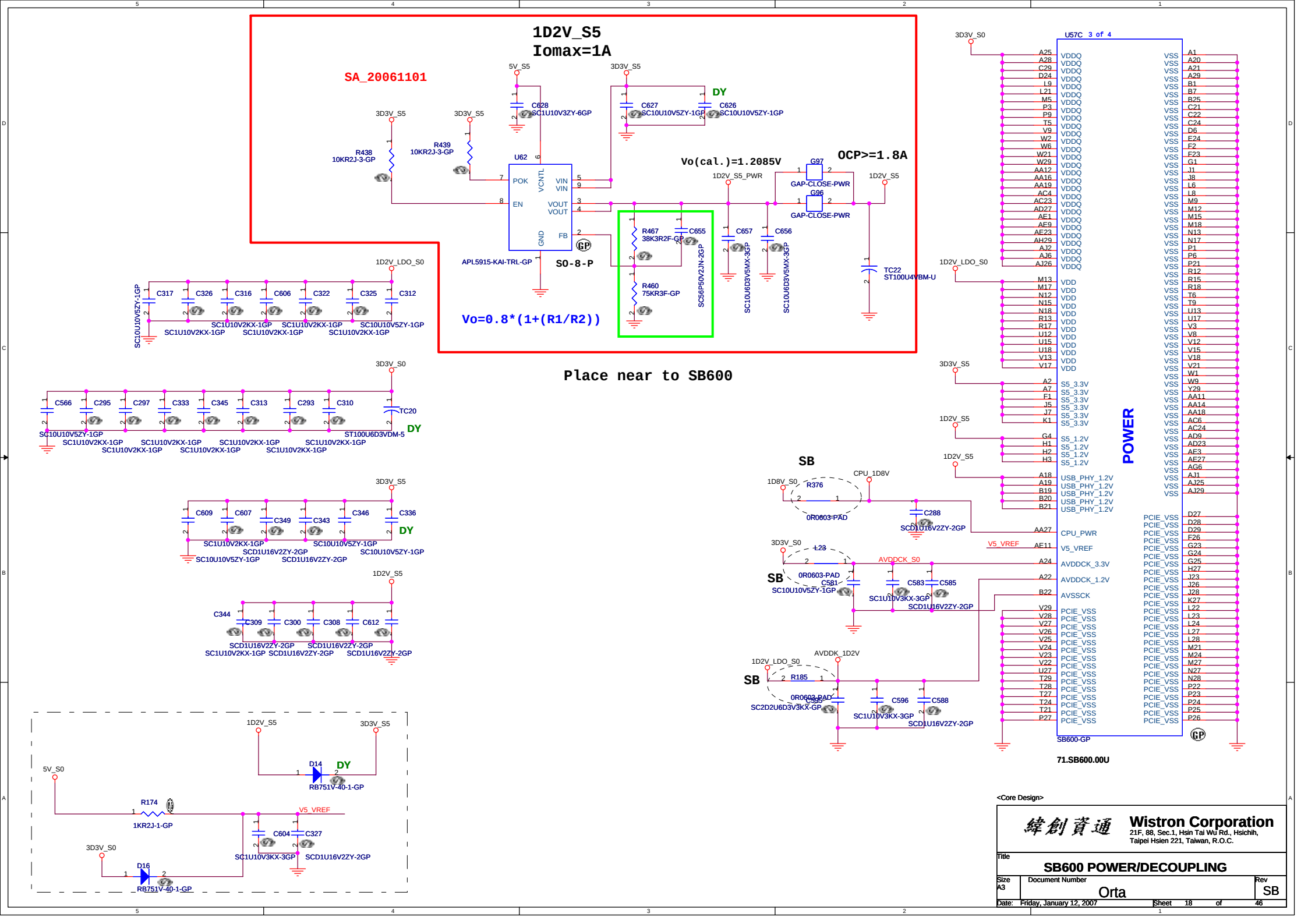
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB600 ACPI/GPIO/SATA/IDE (2 of 5)

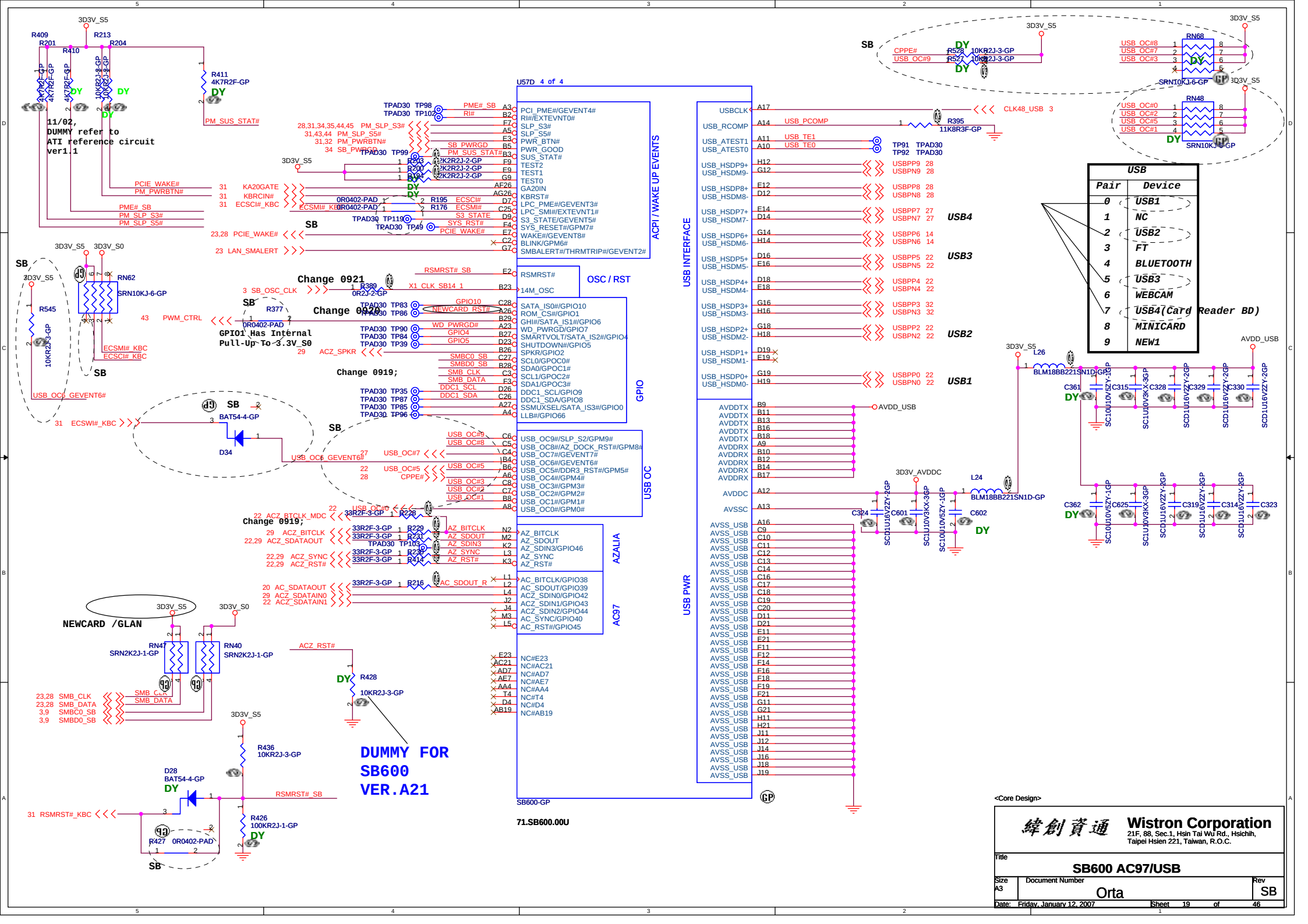
Size: A3 | Document Number: Orta | Rev: SB

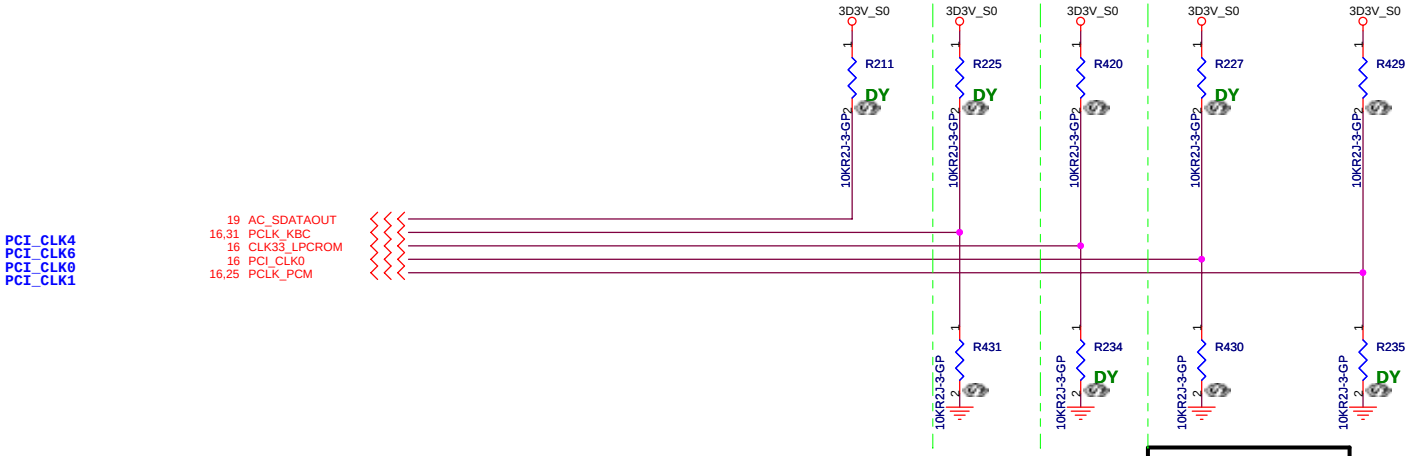
Date: Friday, January 12, 2007 | Sheet 17 of 46



<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	SB600 POWER/DECOUPLING	
Size A3	Document Number: Orta	Rev: SB
Date: Friday, January 12, 2007	Sheet 18 of 46	

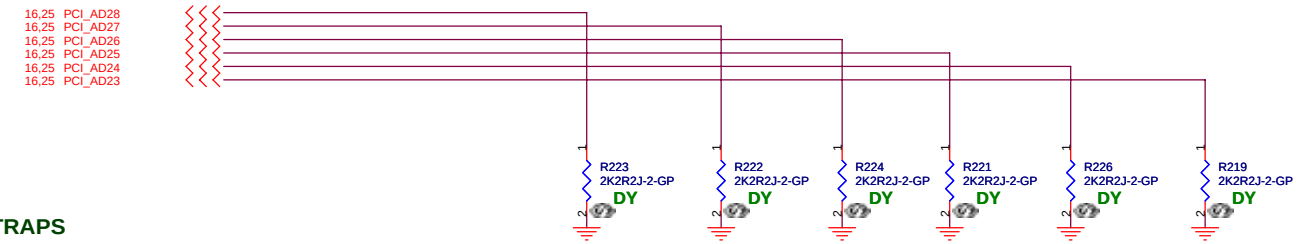

11/02,
DUMMY refer to
ATI reference circuit
ver1.1
Change 0921
Change 0920
Change 0919;
Change 0919;
GPIO1 Has Internal
Pull-Up To 3.3V_S0
NEWCARD /GLAN
DUMMY FOR
SB600
VER.A21
U57D 4 of 4
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
SB600-GP
71.SB600.00U
USB
Pair Device
0 USB1
1 NC
2 USB2
3 FT
4 BLUETOOTH
5 USB3
6 WEBCAM
7 USB4(Card Reader BD)
8 MINICARD
9 NEW1
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB600 AC97/USB
Size A3
Document Number Orta
Rev SB
Date: Friday, January 12, 2007
Sheet 19 of 46



REQUIRED SYSTEM STRAPS

	SB600				
	AC_SDOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

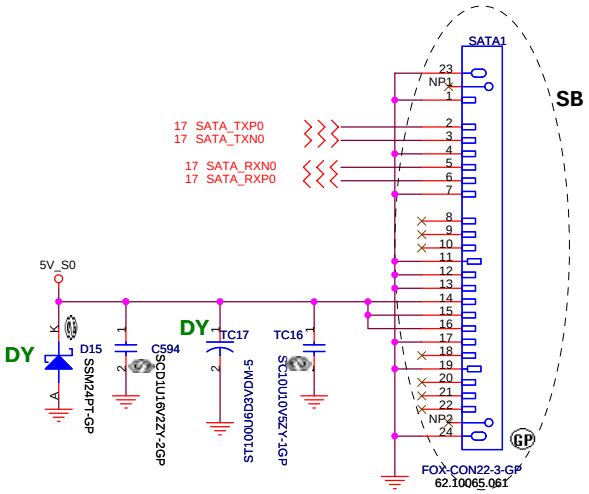
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *SB600 STRAPPING PIN*

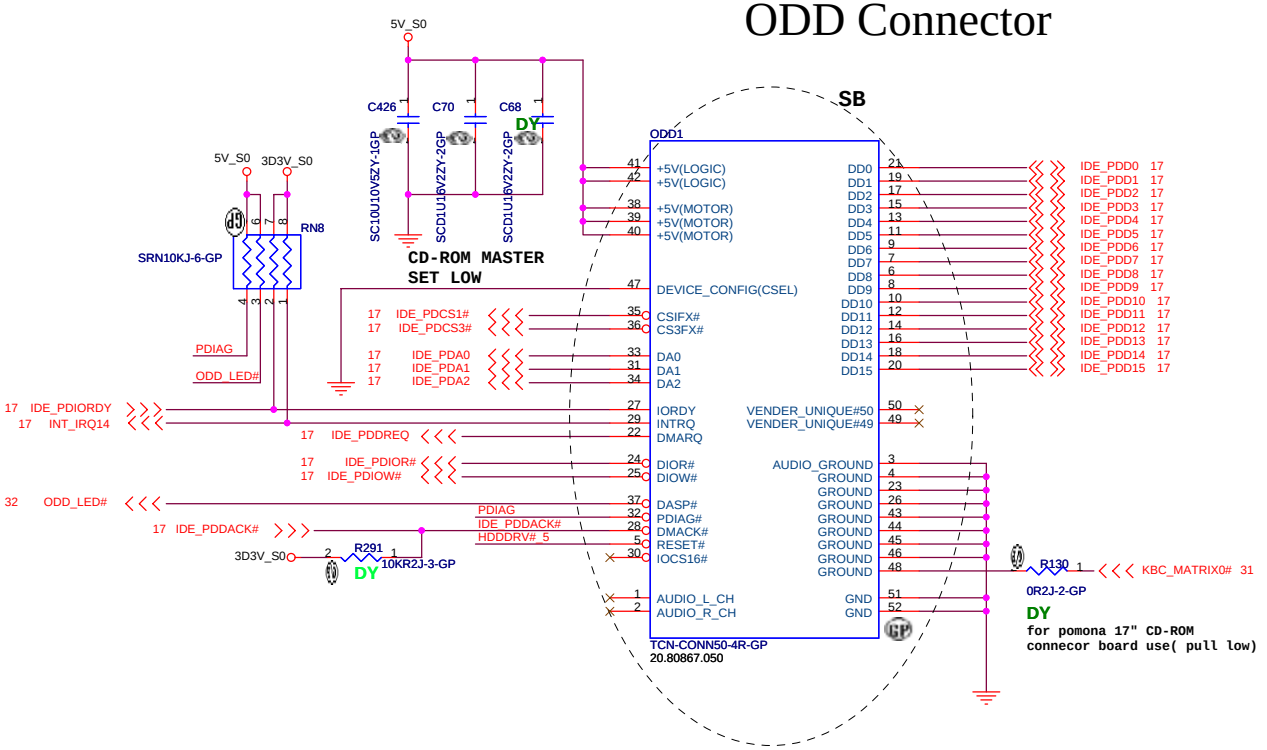
Size: A3 | Document Number: Orta | Rev: SB

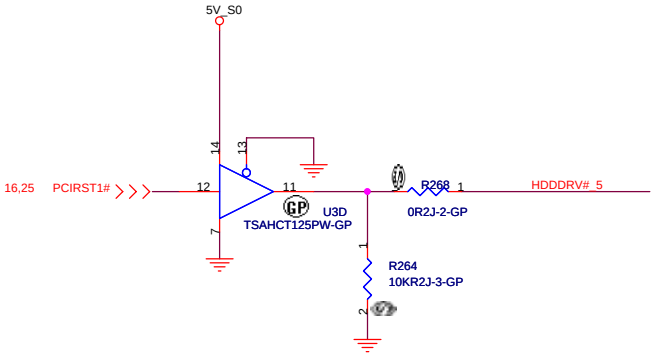
Date: Friday, January 12, 2007 | Sheet 20 of 46

SATA HD Connector



ODD Connector





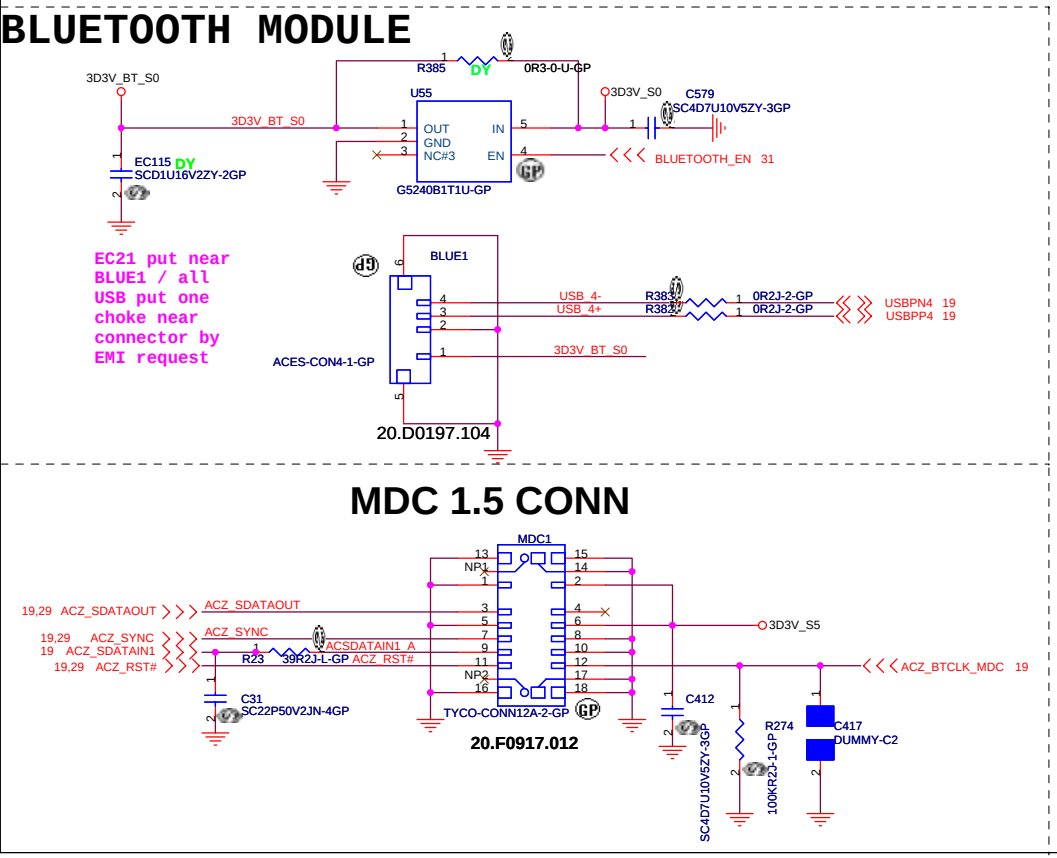
bom1

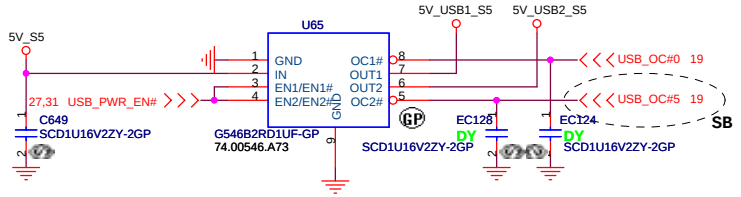
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

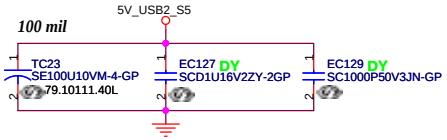
Title: ***HDD and CDROM***

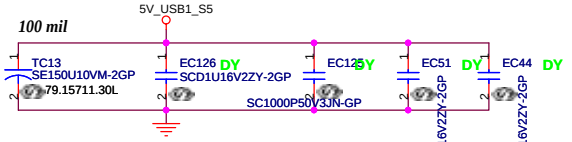
Size	Document Number	Rev
	Orta	SB

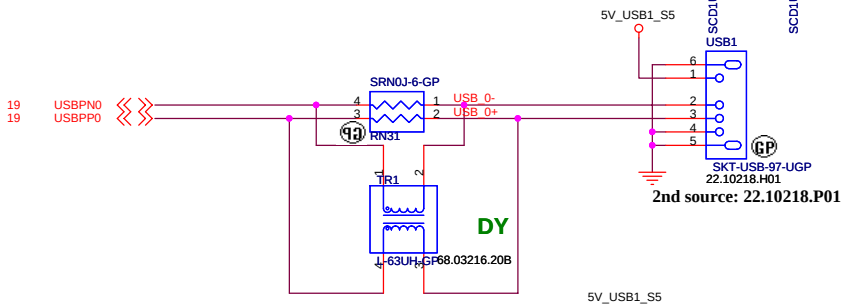
Date: Friday, January 12, 2007 Sheet 21 of 46

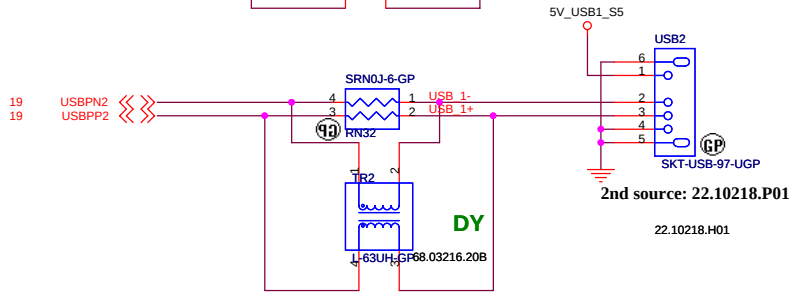


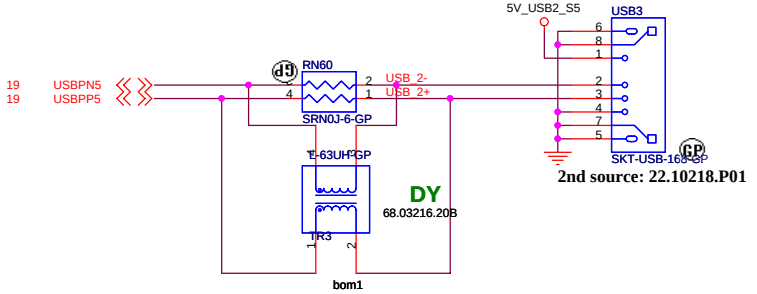










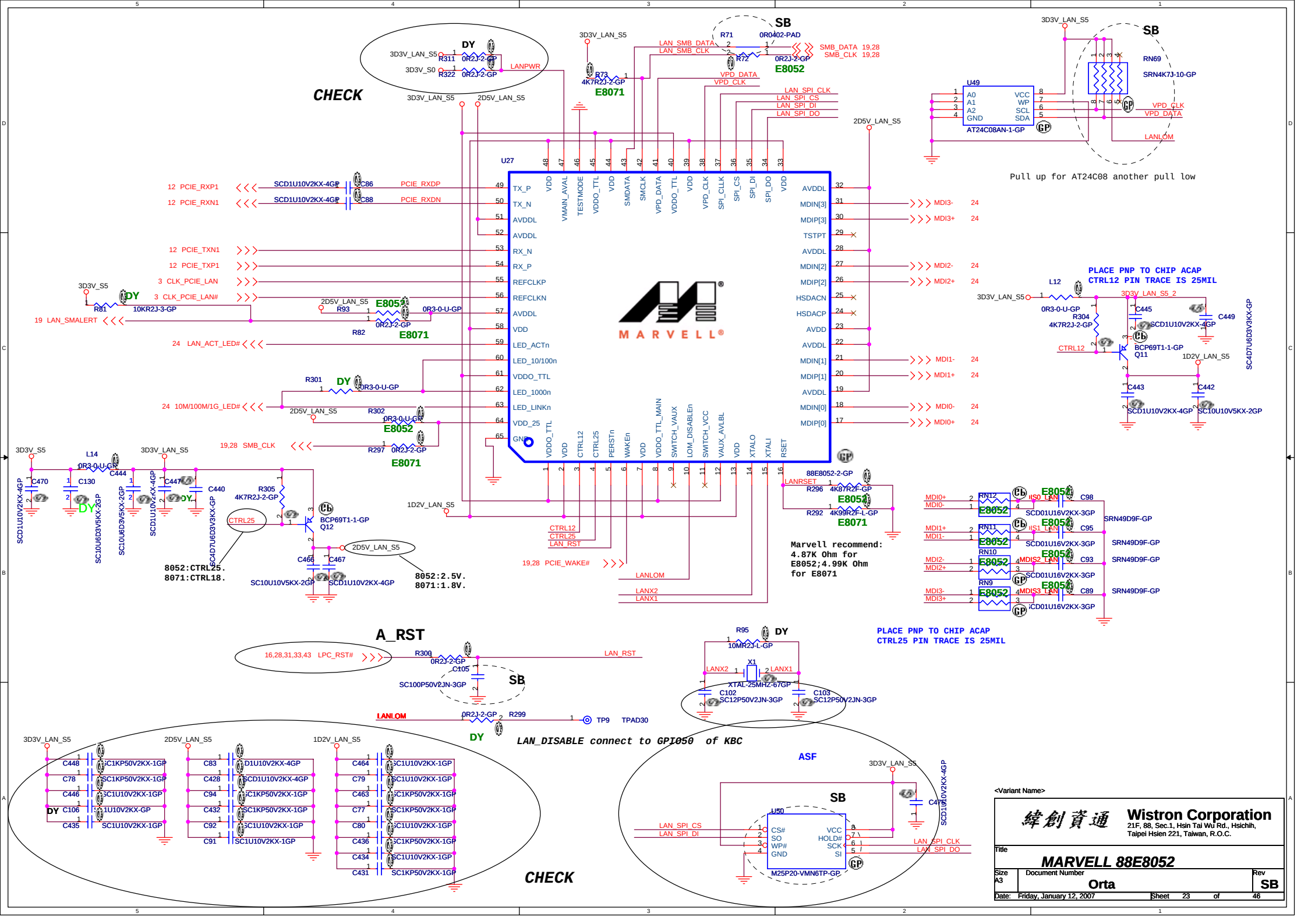


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

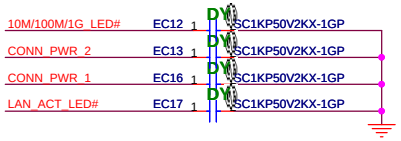
Title: **USB / MDC / BLUETOOTH**

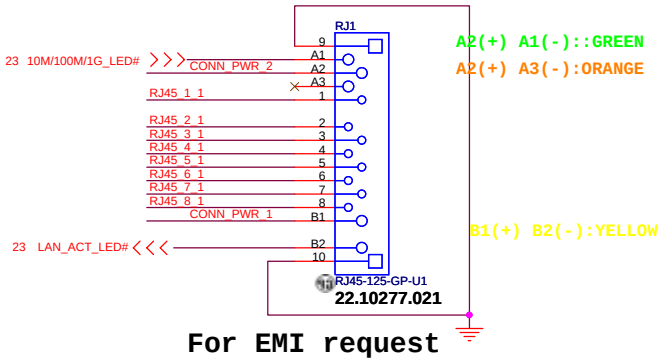
Size	Document Number	Rev
	Orta	SB

Date: Friday, January 12, 2007 Sheet 22 of 46

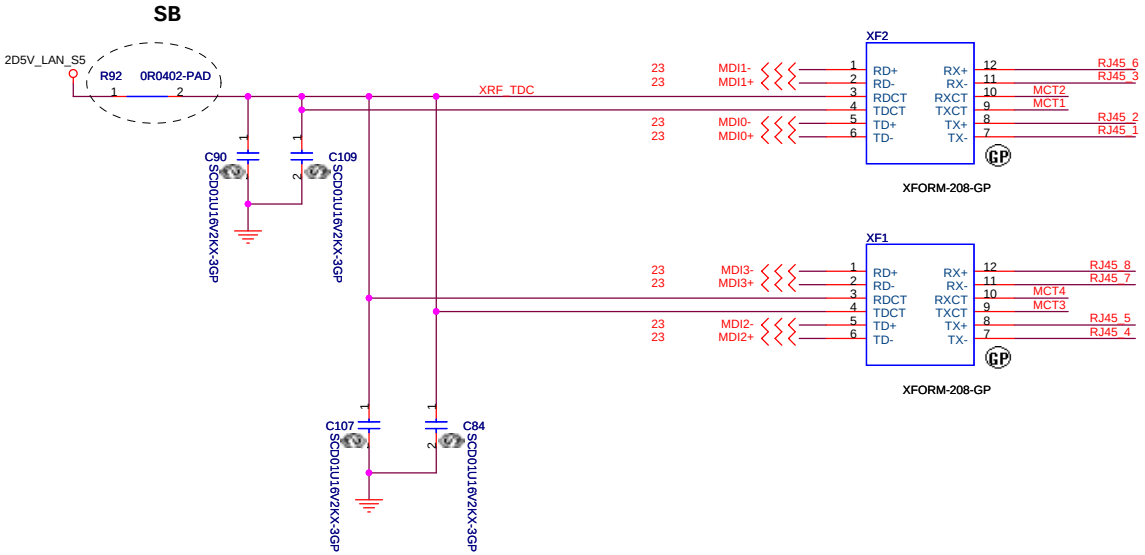

CHECK
DY
SB
U27
MARVELL
E8052
E8071
E8051
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
Marvell recommend:
4.87K Ohm for
E8052;4.99K Ohm
for E8071
8052:CTRL25.
8071:CTRL18.
8052:2.5V.
8071:1.8V.
Pull up for AT24C08 another pull low
A_RST
LAN_DISABLE connect to GPI050 of KBC
ASF
CHECK
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
MARVELL 88E8052
Orta
Friday, January 12, 2007

LAN Connector

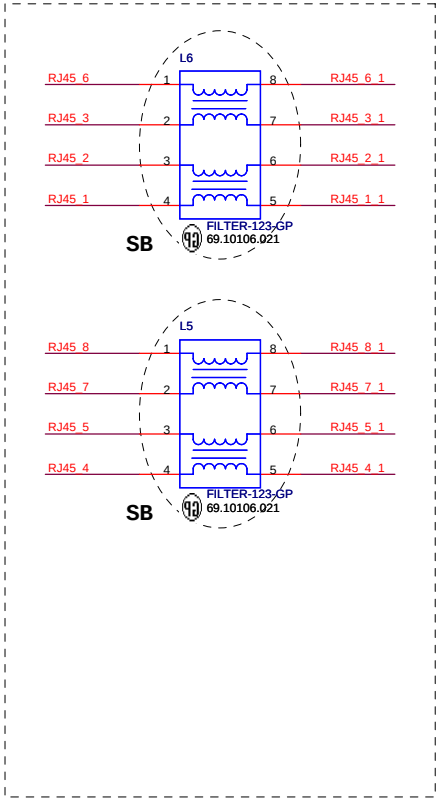




GIGA Lan Transformer



For EMI request

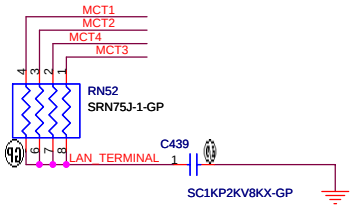


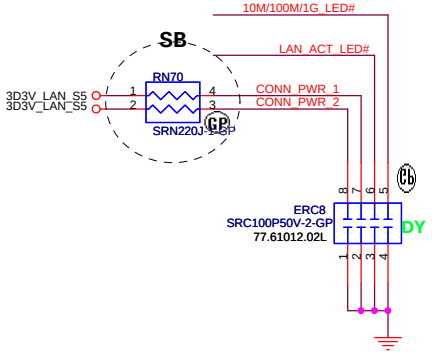
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6





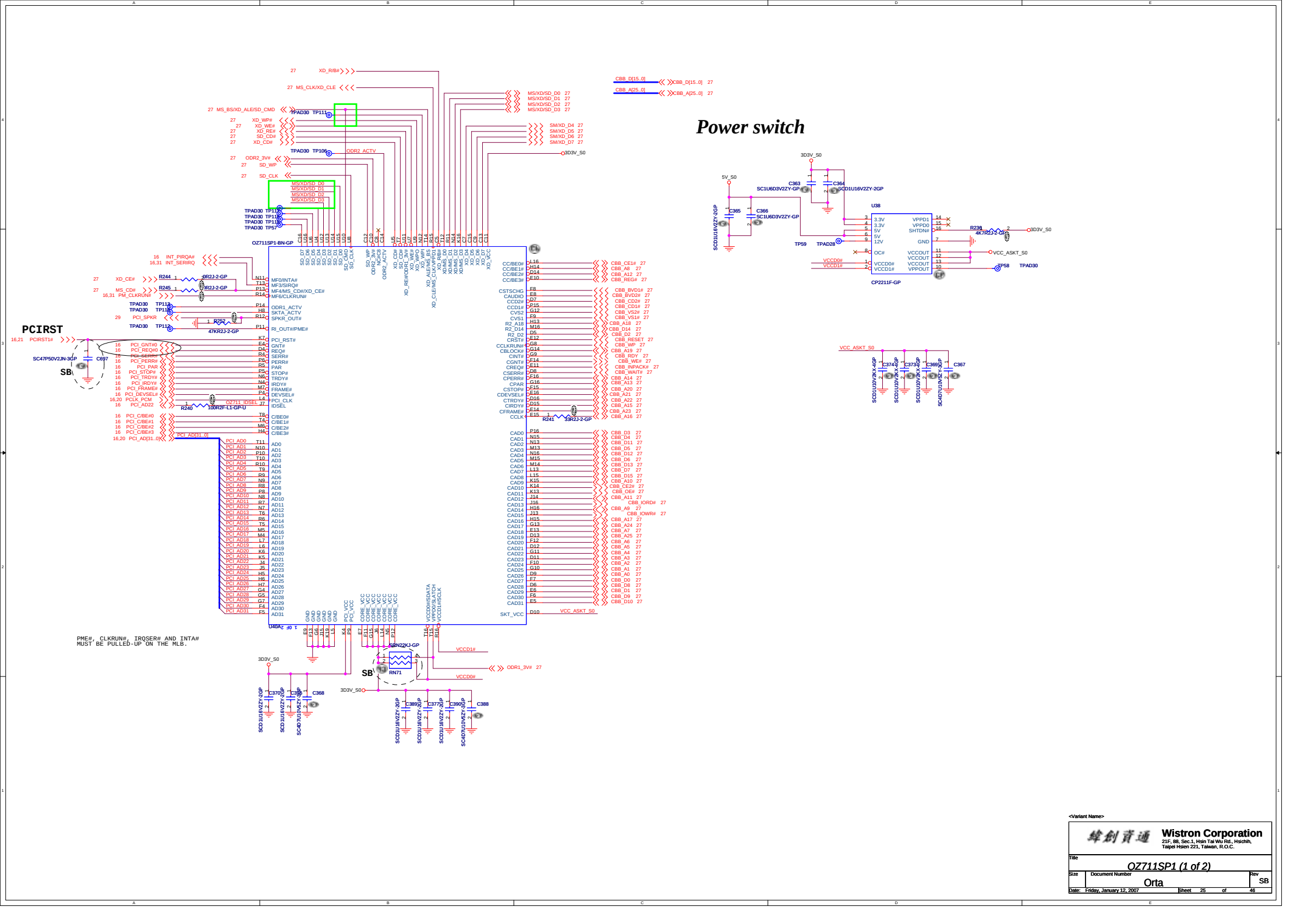
<Variant Name>

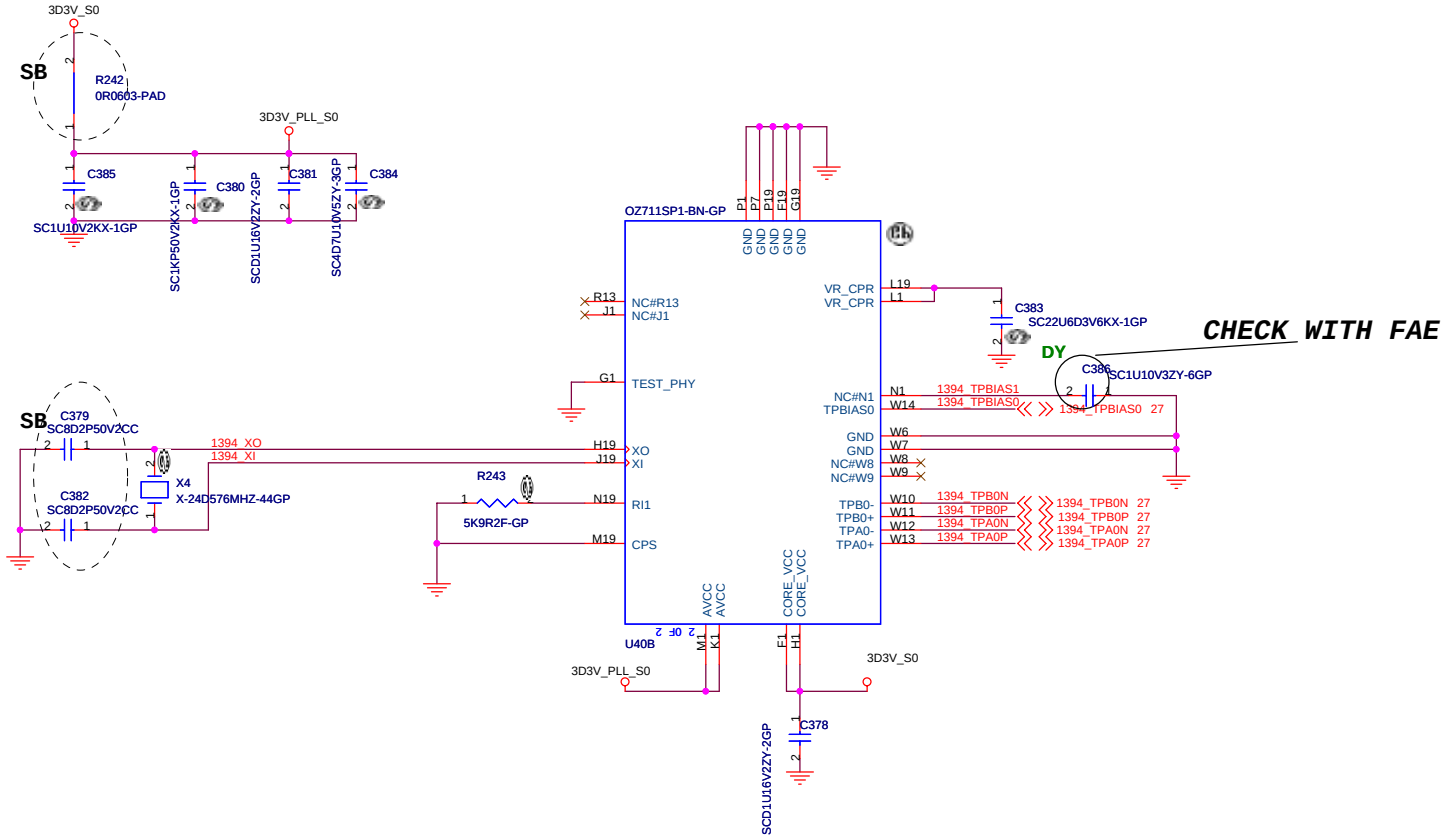
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 24 of 46


Power switch
PCIRST
PME#, CLKRUN#, IRQSER# AND INTA#
MUST BE PULLED-UP ON THE MLB.
OZ711SP1-BN-GP
U40A
SB
3D3V_S0
5V_S0
VCC_ASKT_S0
U38
CP2211F-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
OZ711SP1 (1 of 2)
Size
Document Number
Orta
Rev
SB
Date: Friday, January 12, 2007
Sheet 25 of 46



<Variant Name>

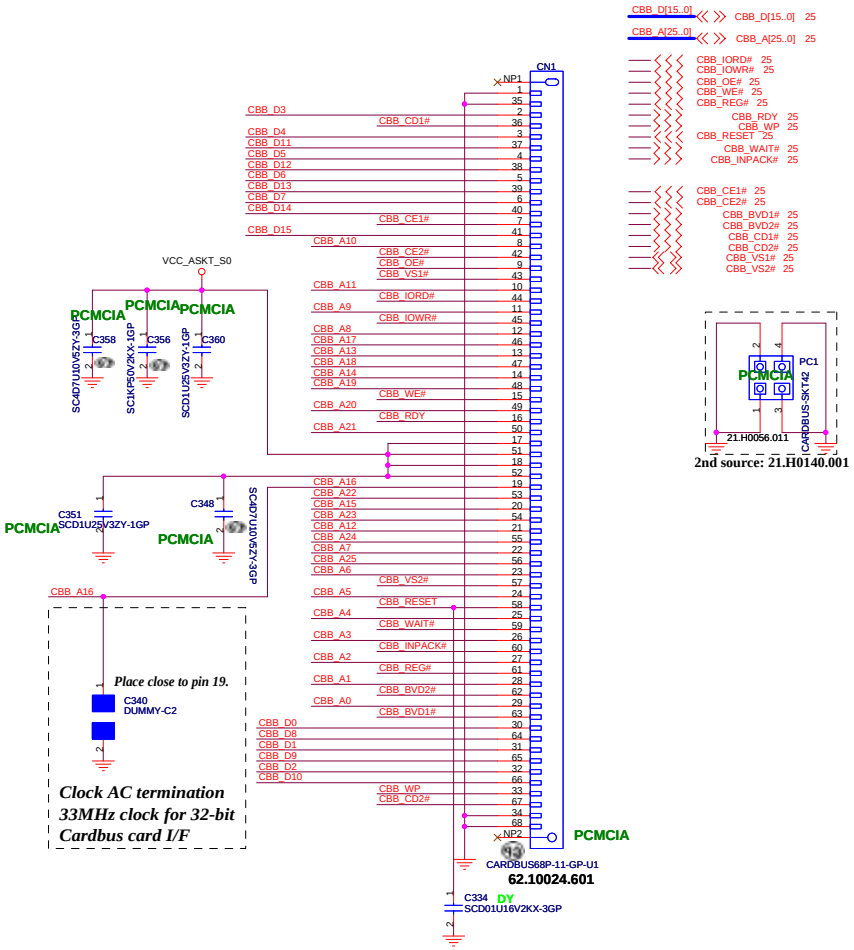
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *OZ711SP1 (2 of 2)*

Size	Document Number	Rev
	Orta	SB

Date: Friday, January 12, 2007 Sheet 26 of 46

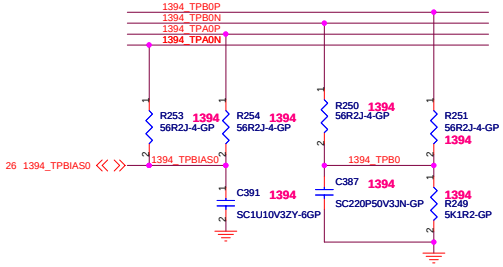
PCMCIA Socket

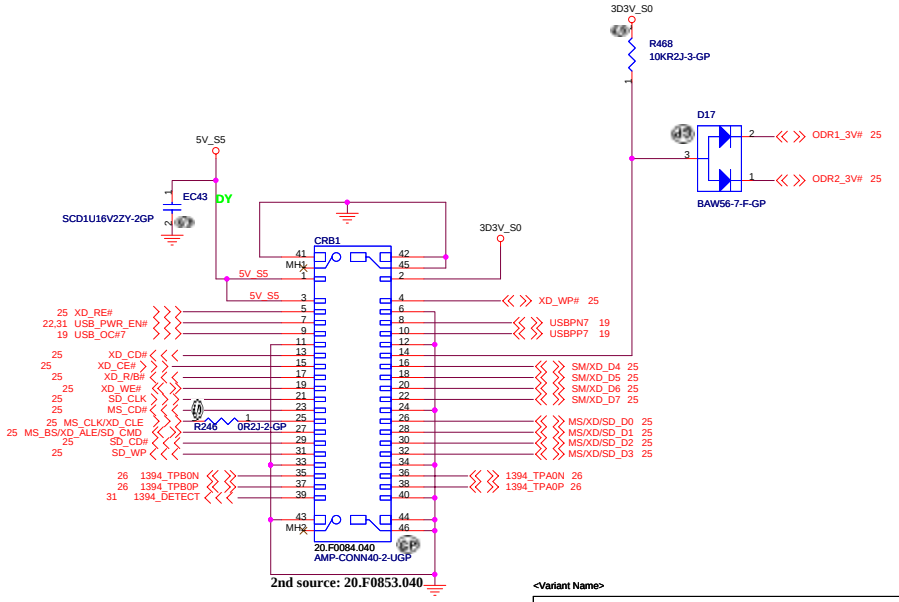


Cardbus I/F

2nd source: 21.H0140.001

CLOSE TO CHIP





2nd source: 20.F0853.040

XD
MS / MS PRO
SD / SD IO / MMC

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA / 1394 / CARD READER

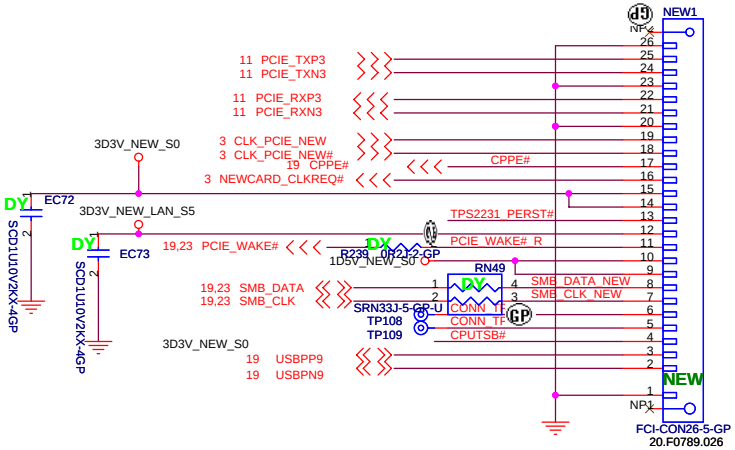
Size	Document Number	Rev
	Orta	SB

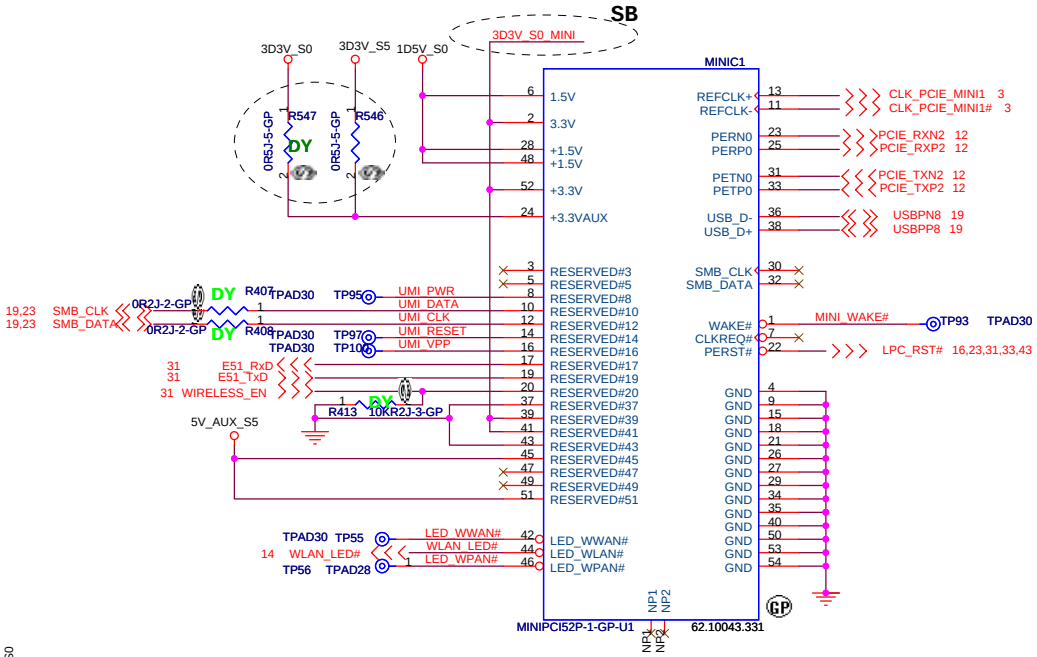
Date: Friday, January 12, 2007 Sheet 27 of 46

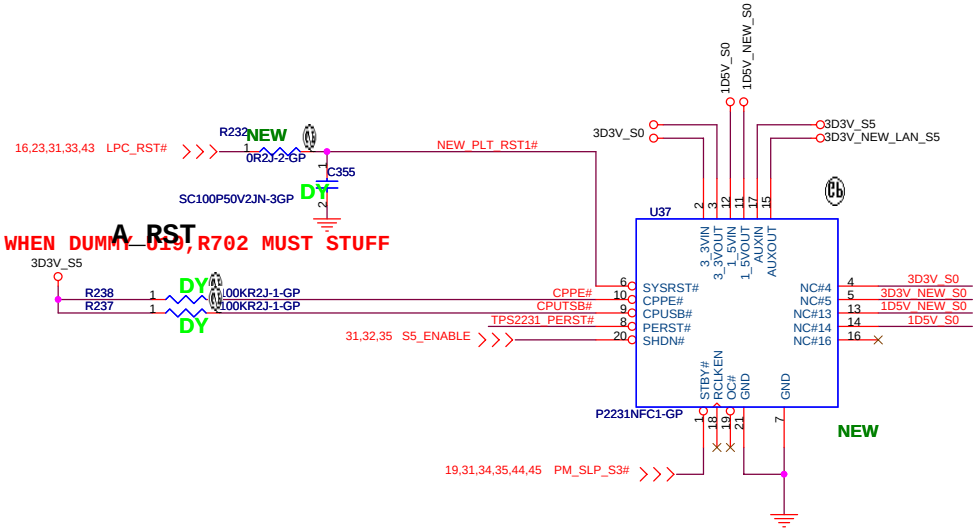
Mini Card Connector

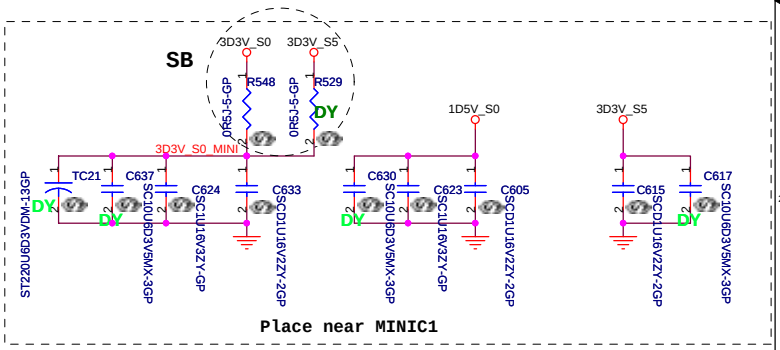
NEWCARD Connector

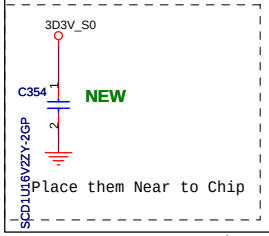
Reserve the symbol for bottom side connector

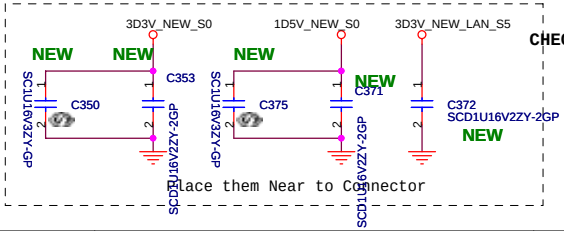










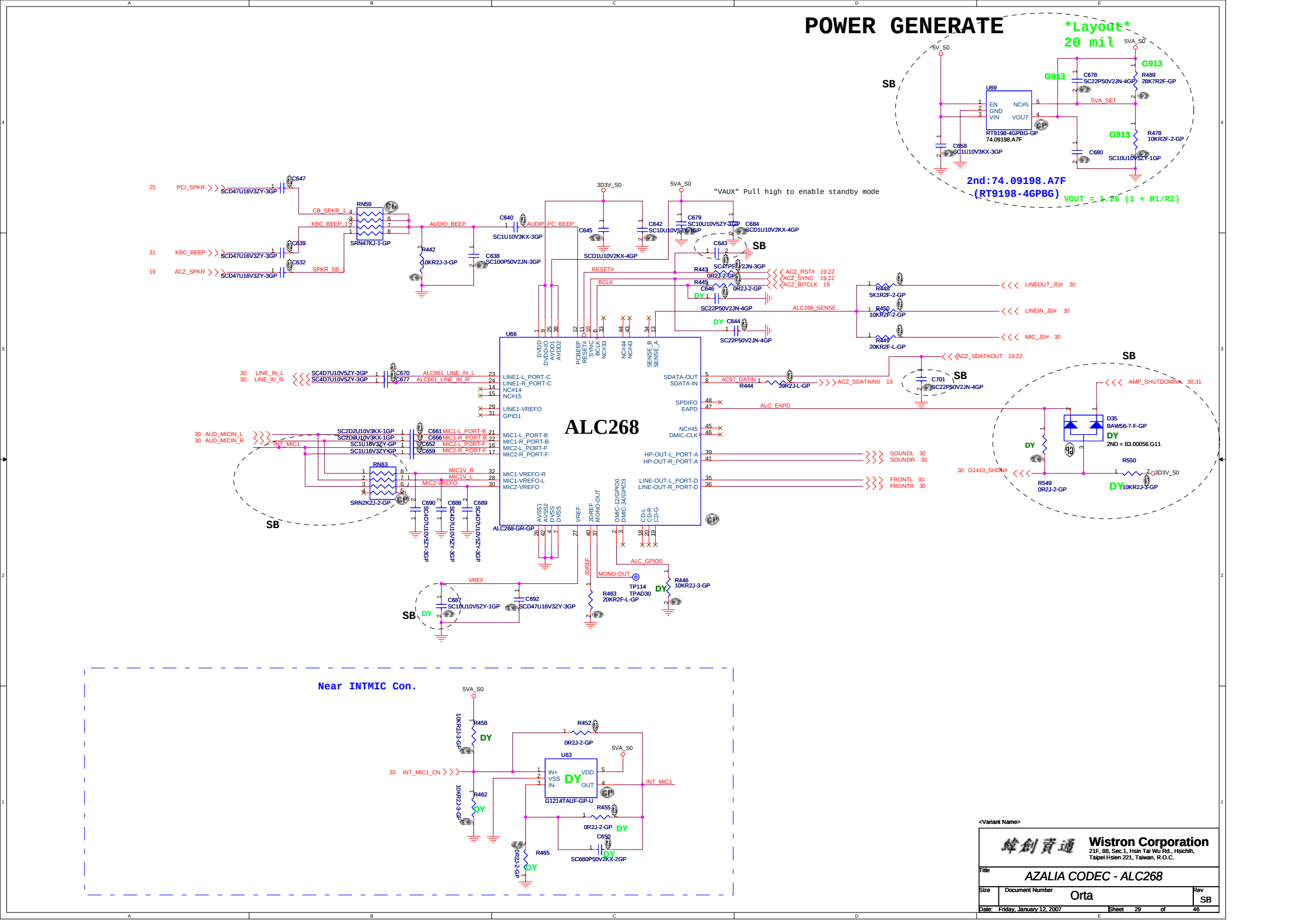


CHECK WITH COLUMBIA

bom1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD / NEW CARD***	
Size	Document Number **Orta**	Rev SB
Date: Friday, January 12, 2007	Sheet 28 of 46	

POWER GENERATE



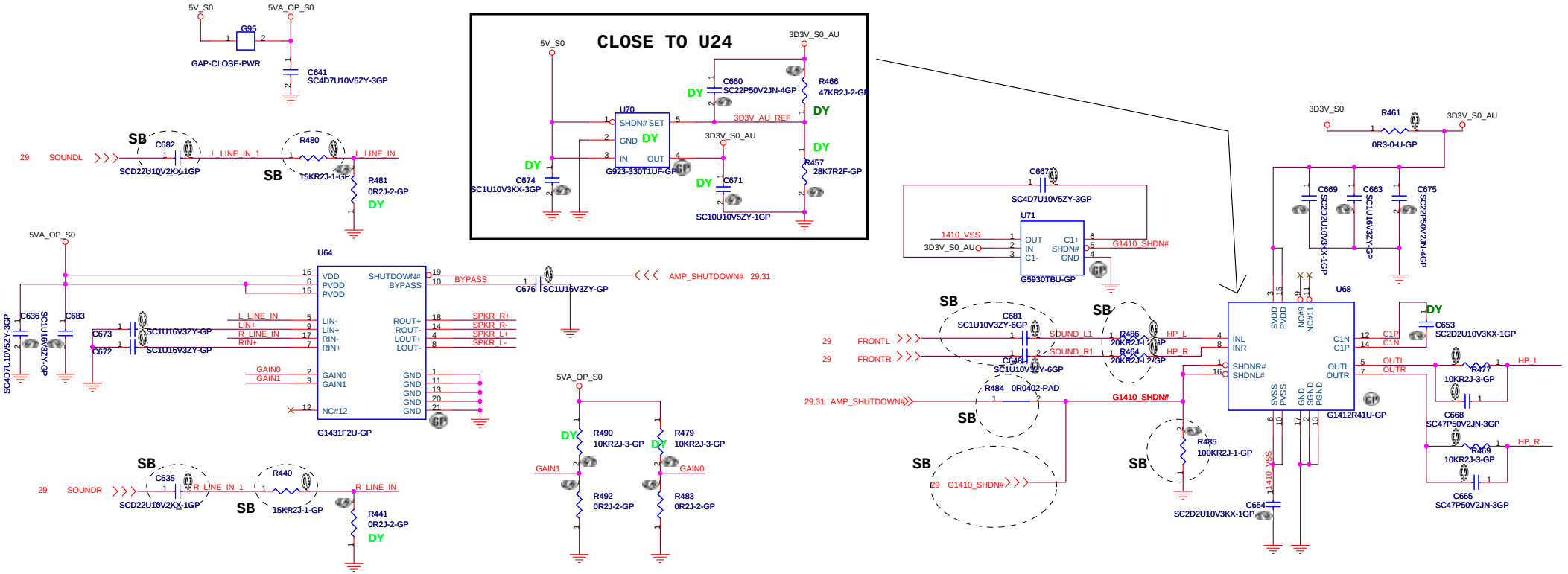
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

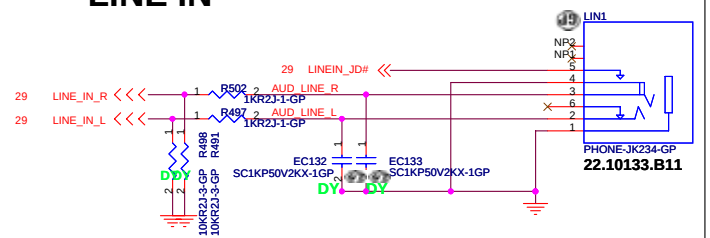
Title	AZALIA CODEC - ALC268	
Size	Document Number: Orta	Rev: SB
Date: Friday, January 12, 2007	Sheet 29 of 46	

AUDIO OP AMPLIFIER

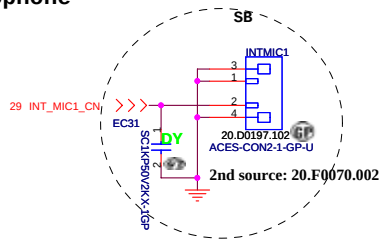
KBC_MUTE_GPIO8



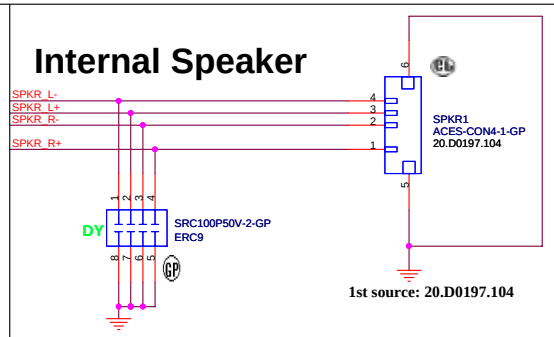
LINE IN



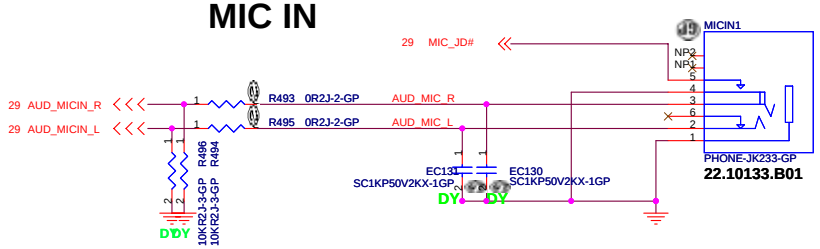
Internal Microphone



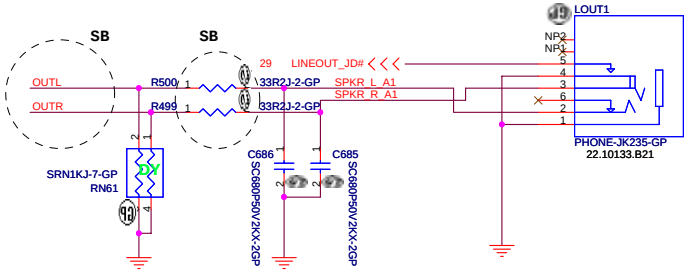
Internal Speaker



MIC IN



LINE OUT



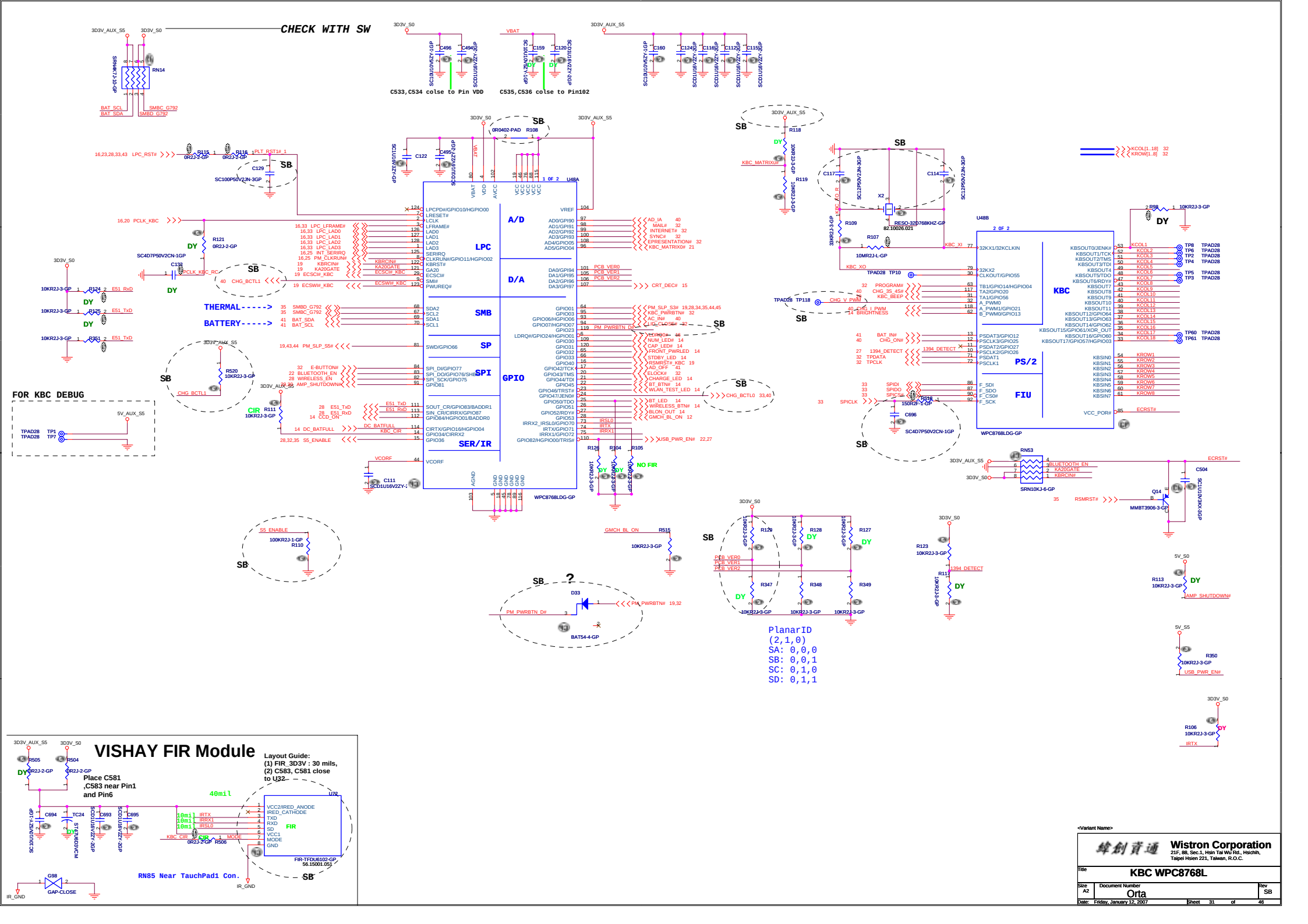
<Variant Name>

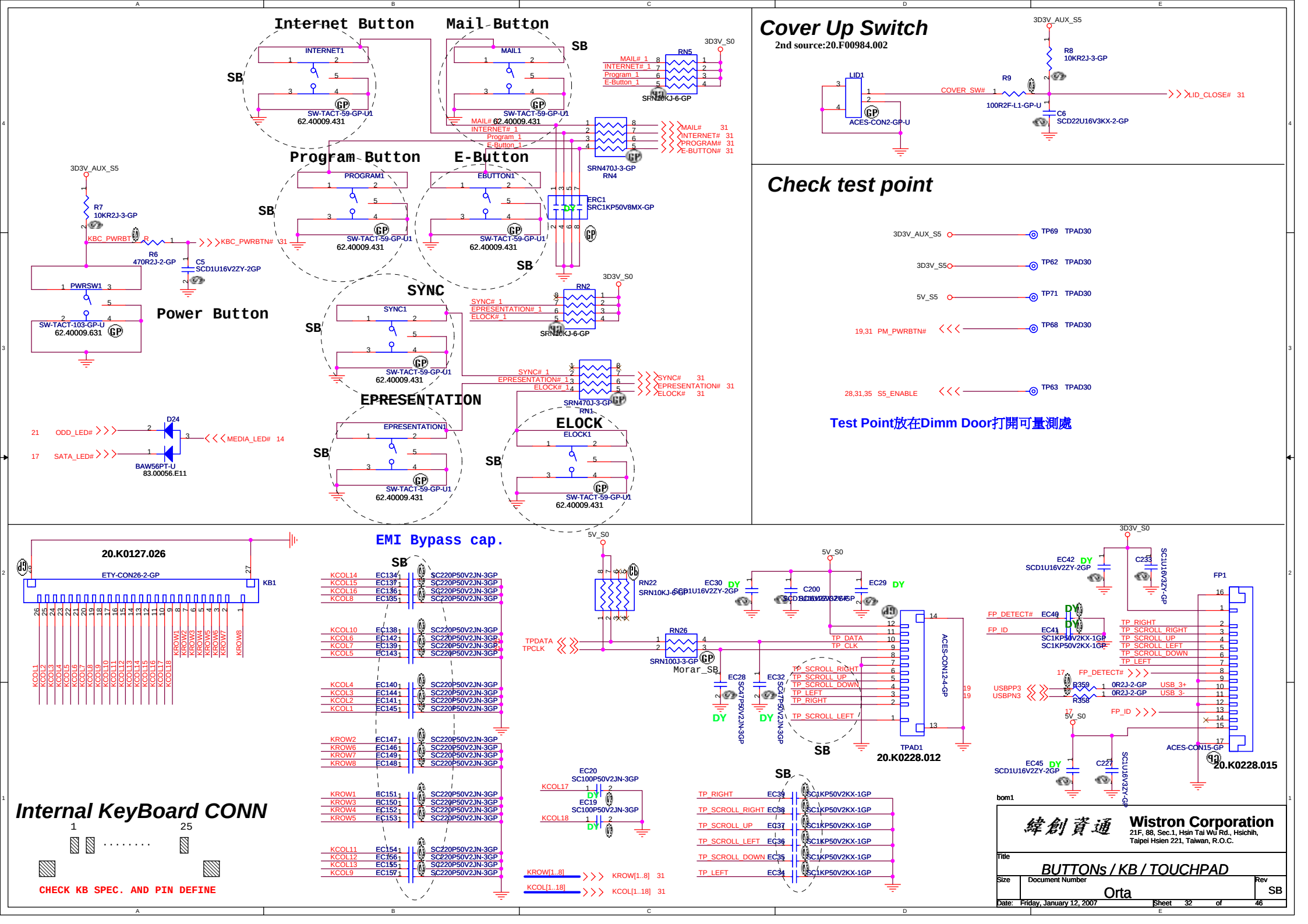
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP AND JACK

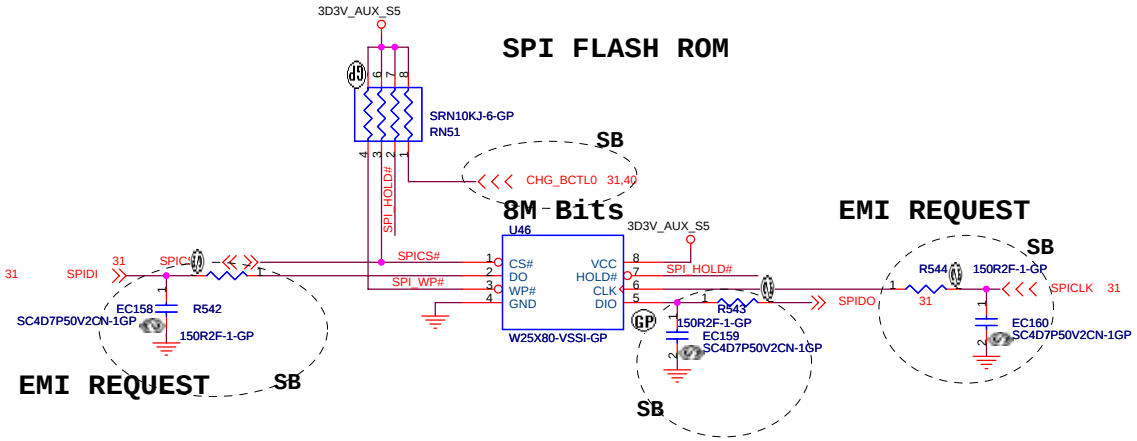
Size	Document Number	Rev
	Orta	SB

Date: Friday, January 12, 2007 Sheet 30 of 46

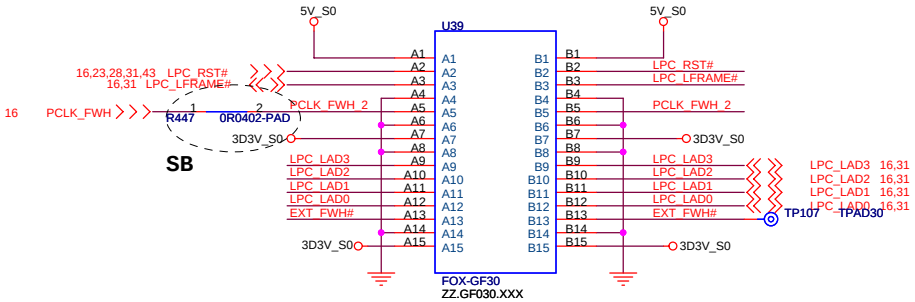

CHECK WITH SW
C533,C534 colse to Pin VDD
C535,C536 colse to Pin102
FOR KBC DEBUG
THERMAL----->
BATTERY----->
U48A
U48B
WPC8768LDG-GP
KBC
PS/2
FIU
GPIO
SER/IR
SPI
SMB
LPC
A/D
D/A
PlanarID
(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
VISHAY FIR Module
Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32
Place C581 ,C583 near Pin1 and Pin6
RN85 Near TauchPad1 Con.
FIR-TFDU6102-GP
56.15001.051
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
Orta
Friday, January 12, 2007
Sheet 31 of 46


Internet Button
Mail Button
Program Button
E-Button
SYNC
EPRESENTATION
ELOCK
Power Button
Cover Up Switch
2nd source:20.F00984.002
Check test point
Test Point放在Dimm Door打開可量測處
EMI Bypass cap.
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
20.K0127.026
20.K0228.012
20.K0228.015
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BUTTONs / KB / TOUCHPAD
Orta
Date: Friday, January 12, 2007
Sheet 32 of 46

SPI FLASH ROM



GOLDEN FINGER FOR DEBUG BOARD



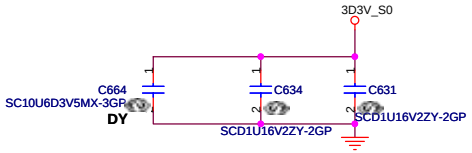
TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

EMI REQUEST

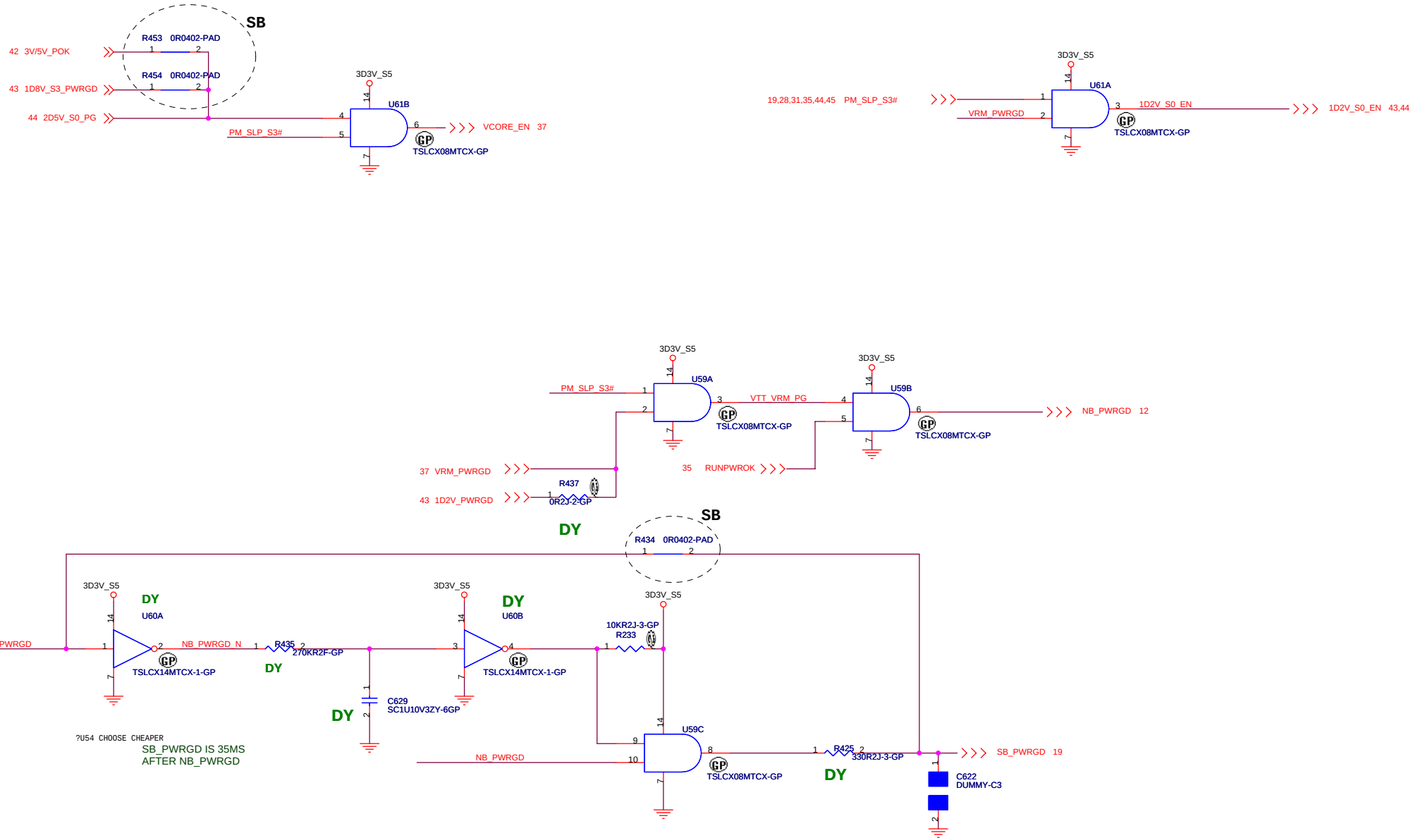
Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS		
Size: A3	Document Number: Orta	Rev: SB
Date: Friday, January 12, 2007	Sheet 33 of 46	



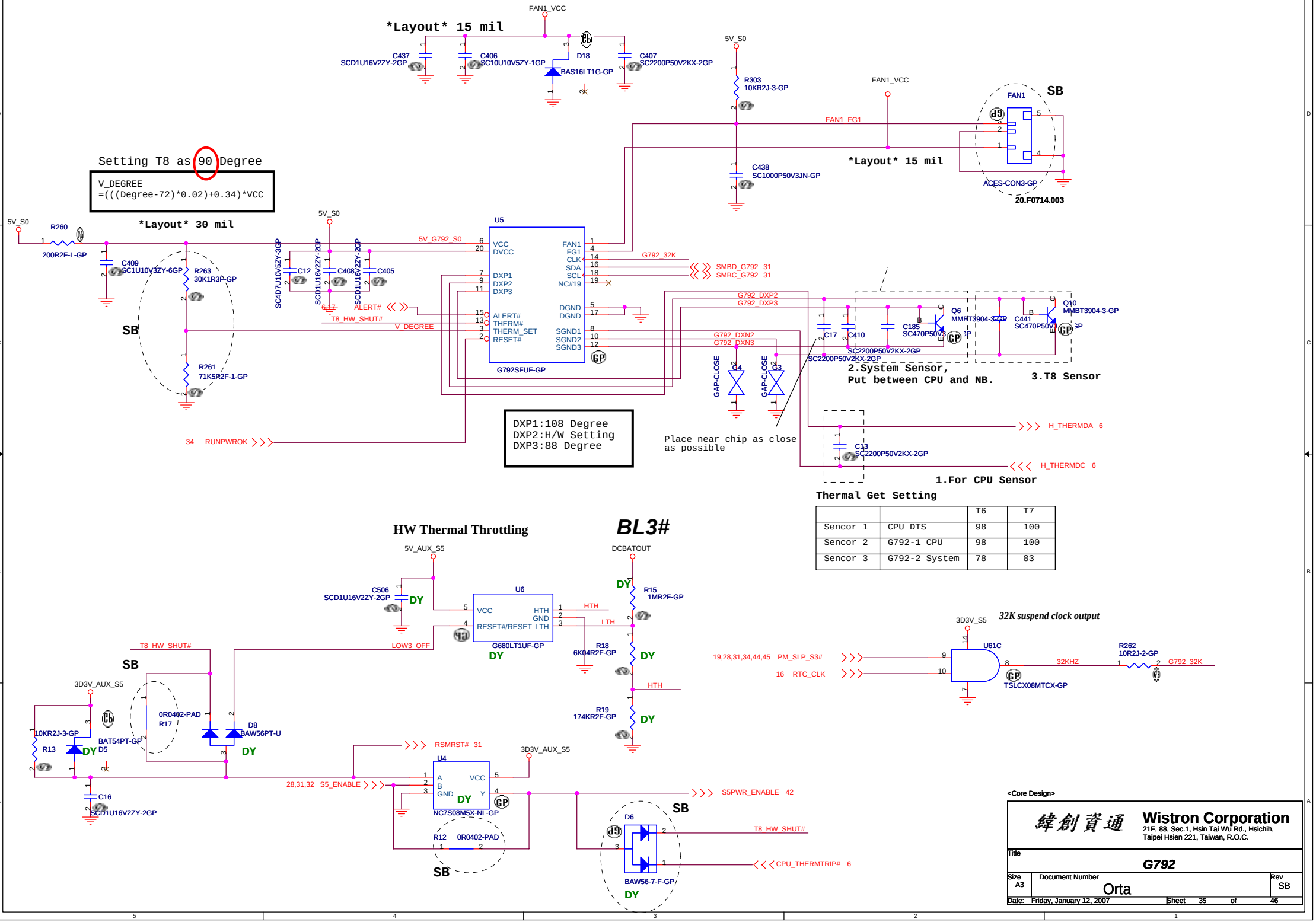
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWERGOOD&ENABLES(1/2)

Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 34 of 46



		T6	T7
Sencor 1	CPU DTS	98	100
Sencor 2	G792-1 CPU	98	100
Sencor 3	G792-2 System	78	83

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **G792**

Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 35 of 46

CPU_CORE
ISL6264CRZ

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS51120
3D3V/5V

DCBATOUT_51120

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

Input Power
VIN
REG5V_IN(I / 5V)

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

APL5913

1D8V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

APL5332KAC-TRLGP

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal (I)
Input Power VCC(I) VCC(I)

Output Signal (O) → AD_IN
Output Power VCC(O) → AD+

Charger_ISL6255

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V) → AD_IN
XTAL2/PB4 (O/5V) → CHARGE_LED#
XTAL1/PB3 (O/5V) → BL2#

Output Power
VCC (O) → DCBATOUT
VCC (O) → BT+

Input Power
DCIN (I) ← AD+

TI TPS51116
1.8V / 0.9V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V) → 1D8V_S3_PG

DCBATOUT
5V_S5

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O) → 1.8V_S3
VCC(O) → 0.9V_S3

ISL6268_1D2V

1D2V_S0_EN
5V_S5
DCBATOUT

Input Signal SS_STBY1(I / 5V) FOR 1.2V
Input Power VCC VIN

Output Power
1D2V_PWR → 1D2V (6.5A)

ISL6268_VGA_CORE

VGA_CORE_EN
5V_S5
DCBATOUT

Input Signal SS_STBY1(I / 5V) FOR 1.2V
Input Power VCC VIN

Output Power
1D2V_PWR → VGA_CORE_S0 (15A)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

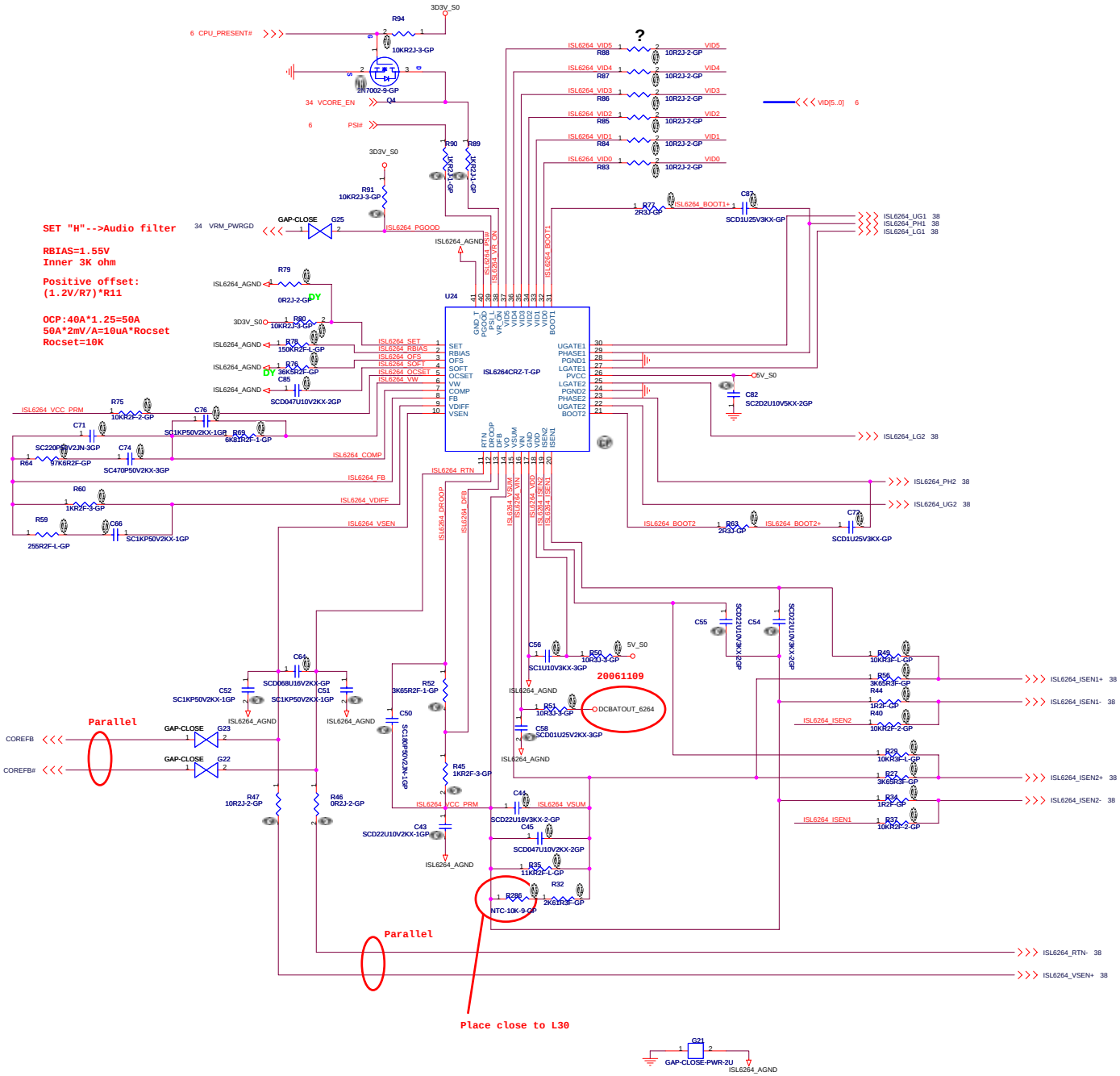
Size	Document Number	Rev
A3	Orta	SB

Date: Friday, January 12, 2007 Sheet 36 of 46

CPU_VCORE
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375



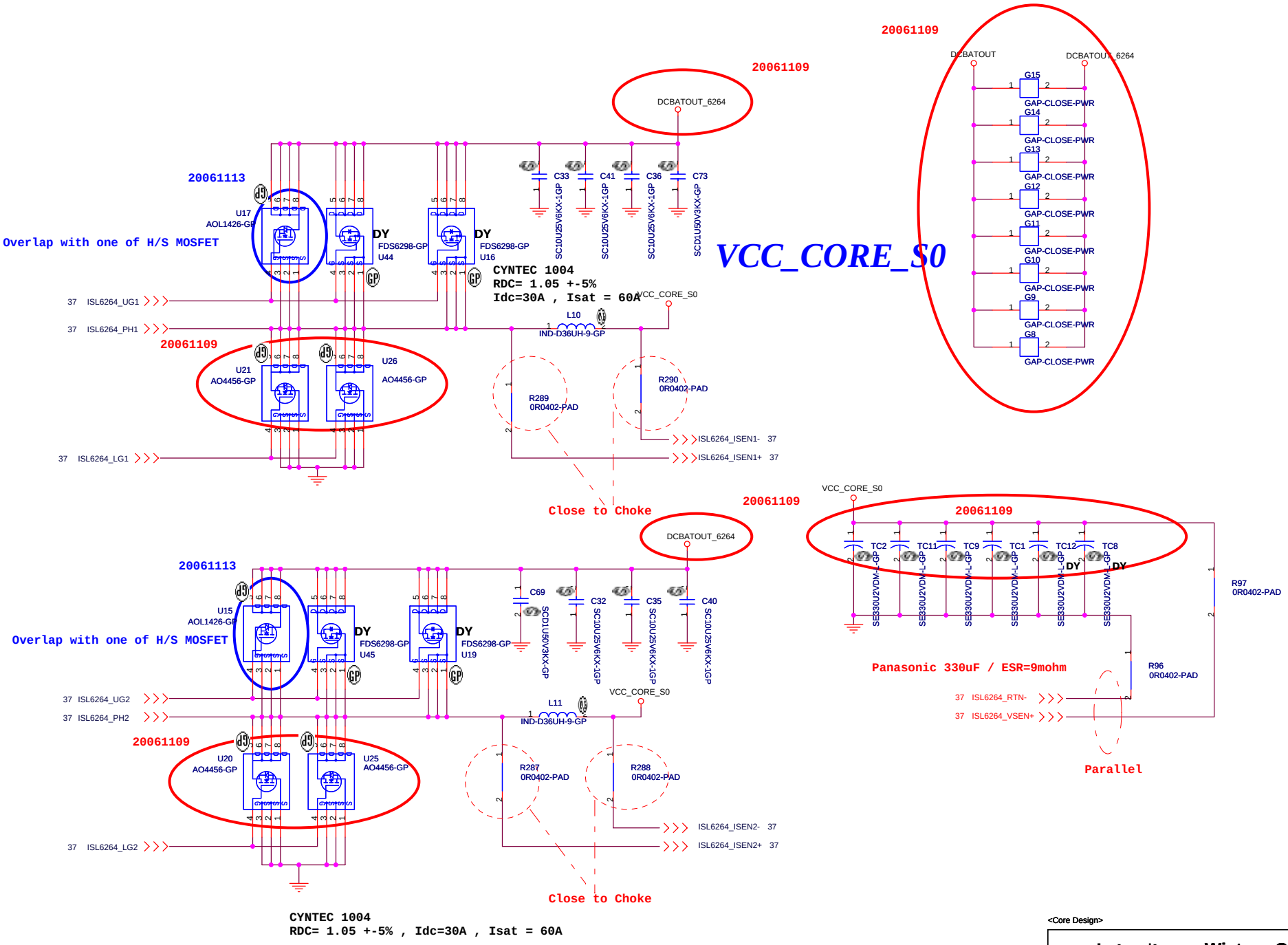
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_1

Size: A2 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 37 of 46



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_2

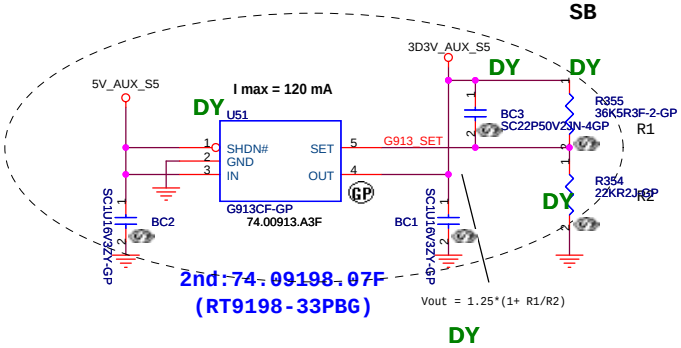
Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 38 of 46

Aux Power

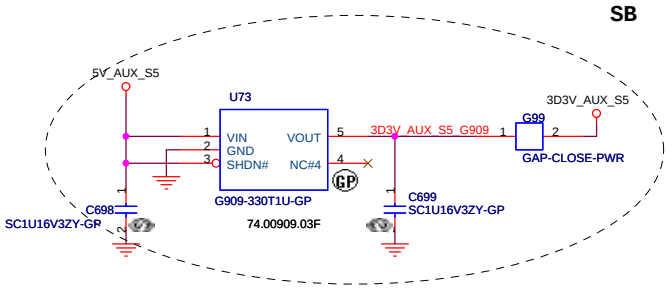
3D3V_AUX_S5

SB



Aux Power 3D3V_AUX_S5

SB

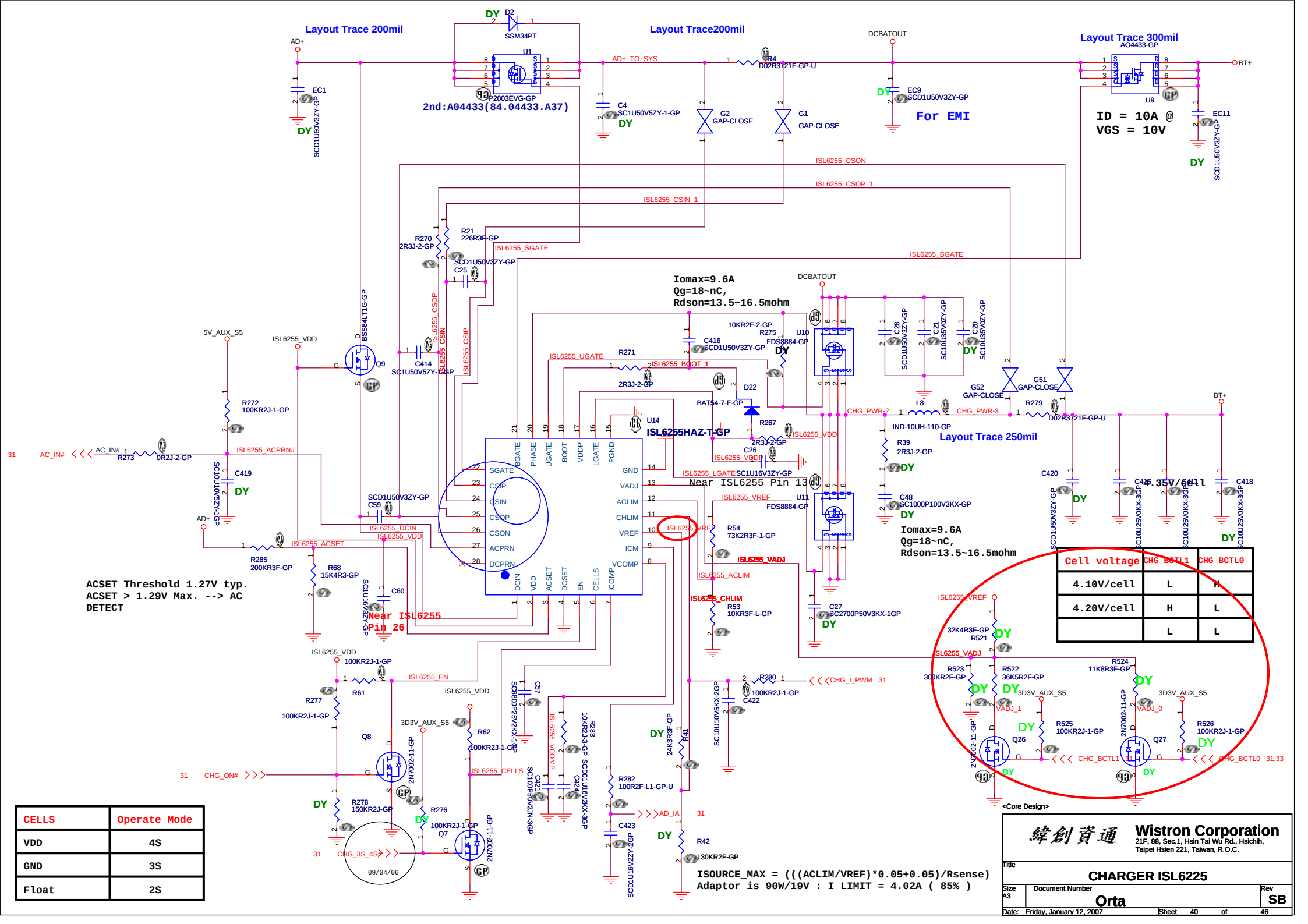


<Core Design>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3D3V_AUX		
Size: A3	Document Number: Orta	Rev: SB
Date: Friday, January 12, 2007	Sheet 39 of 46	



Cell voltage	CHG_BCTL1	CHG_BCTL0
4.10V/cell	L	H
4.20V/cell	H	L
	L	L

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

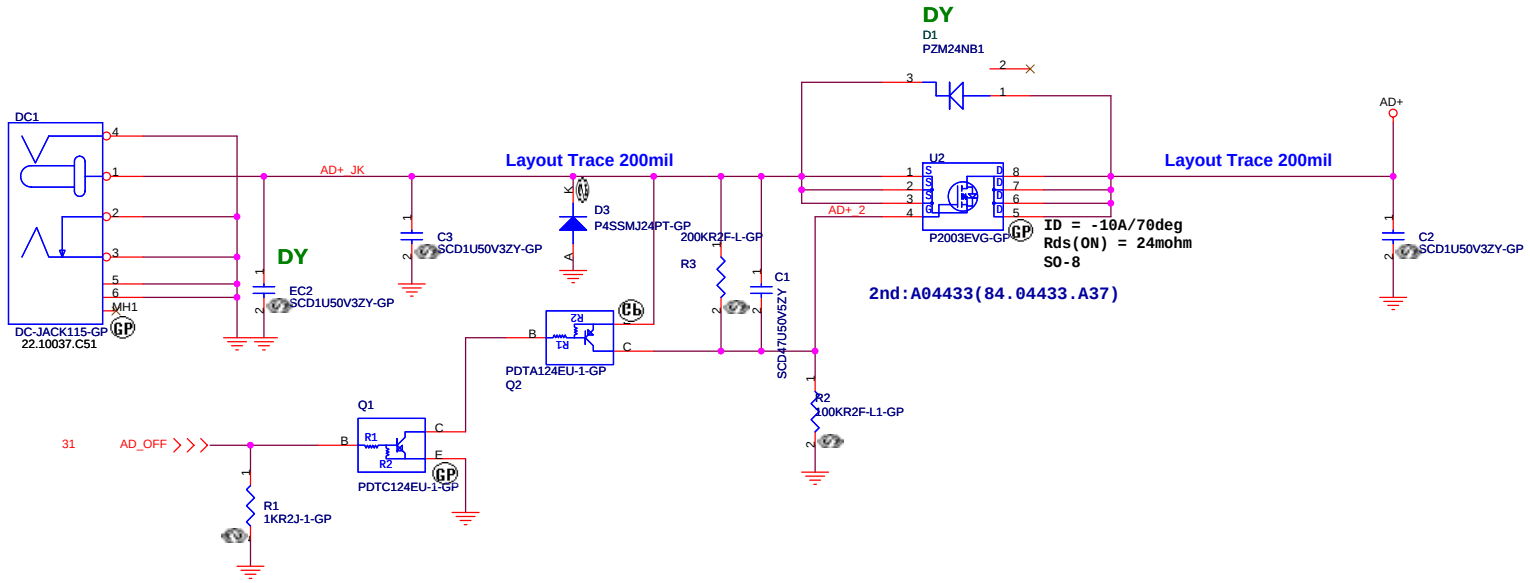
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6225

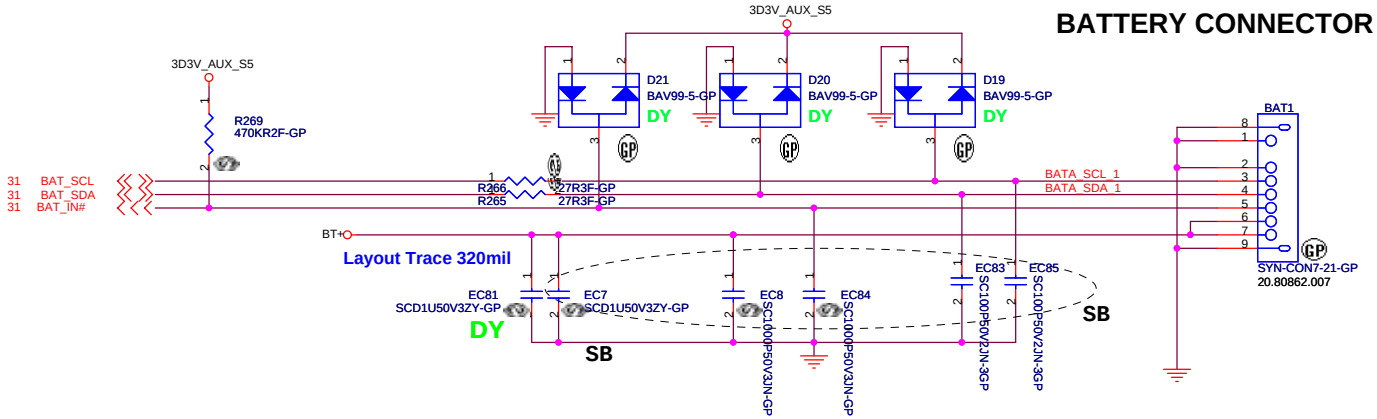
Size: A3 | Document Number: Orta | Rev: SB

Date: Friday, January 12, 2007 | Sheet 40 of 46

Adaptor in to generate DCBATOUT



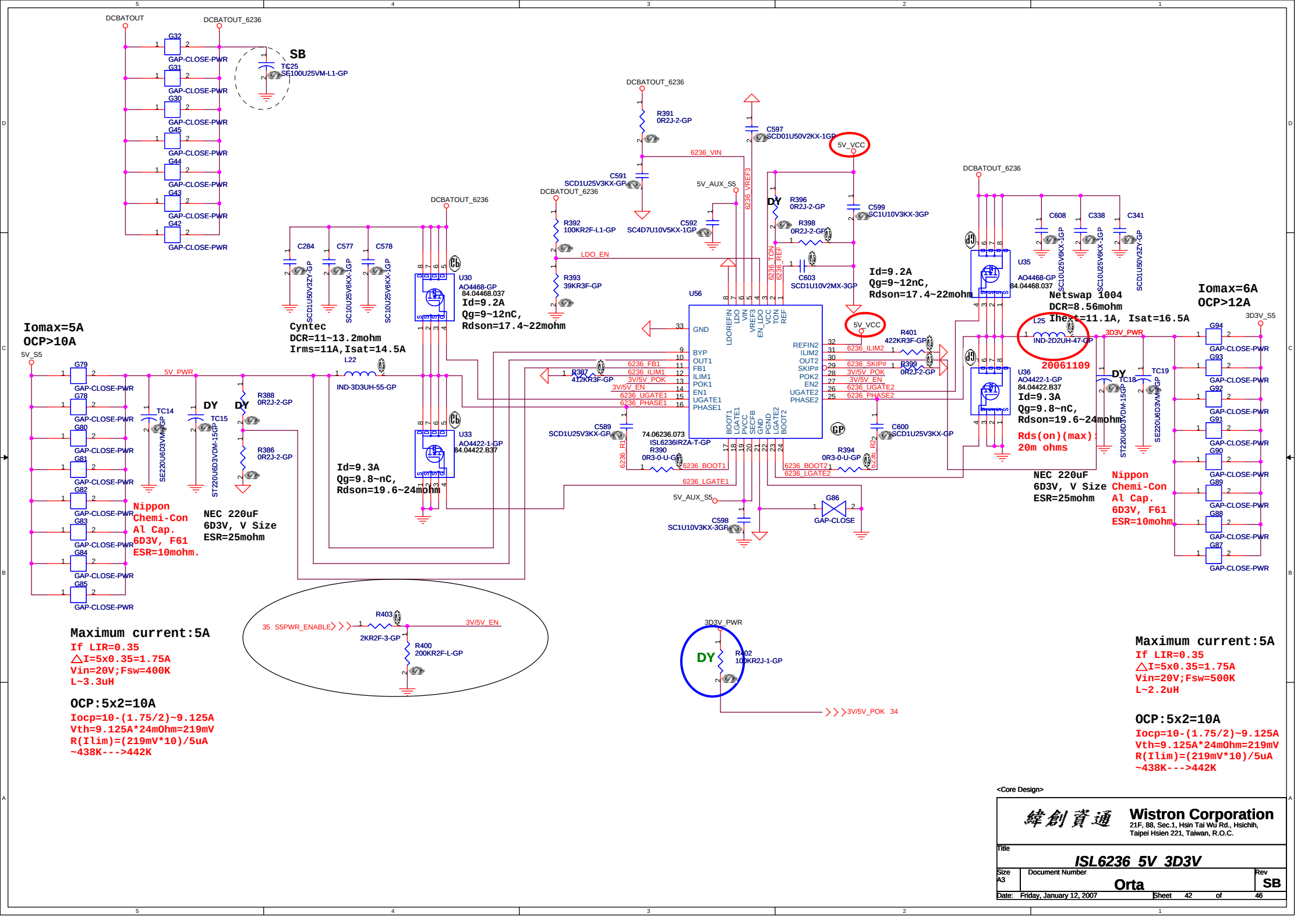
BATTERY CONNECTOR

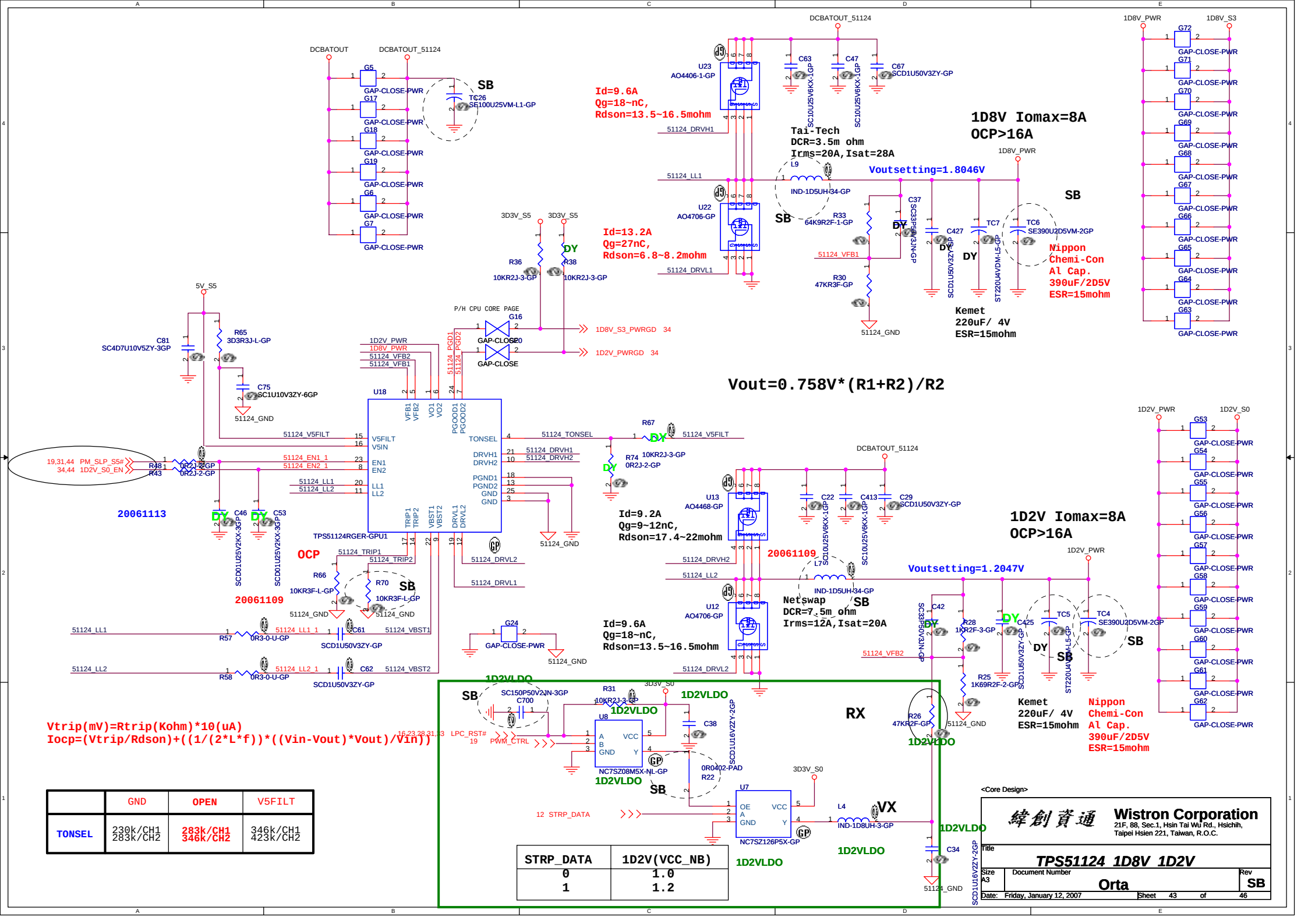


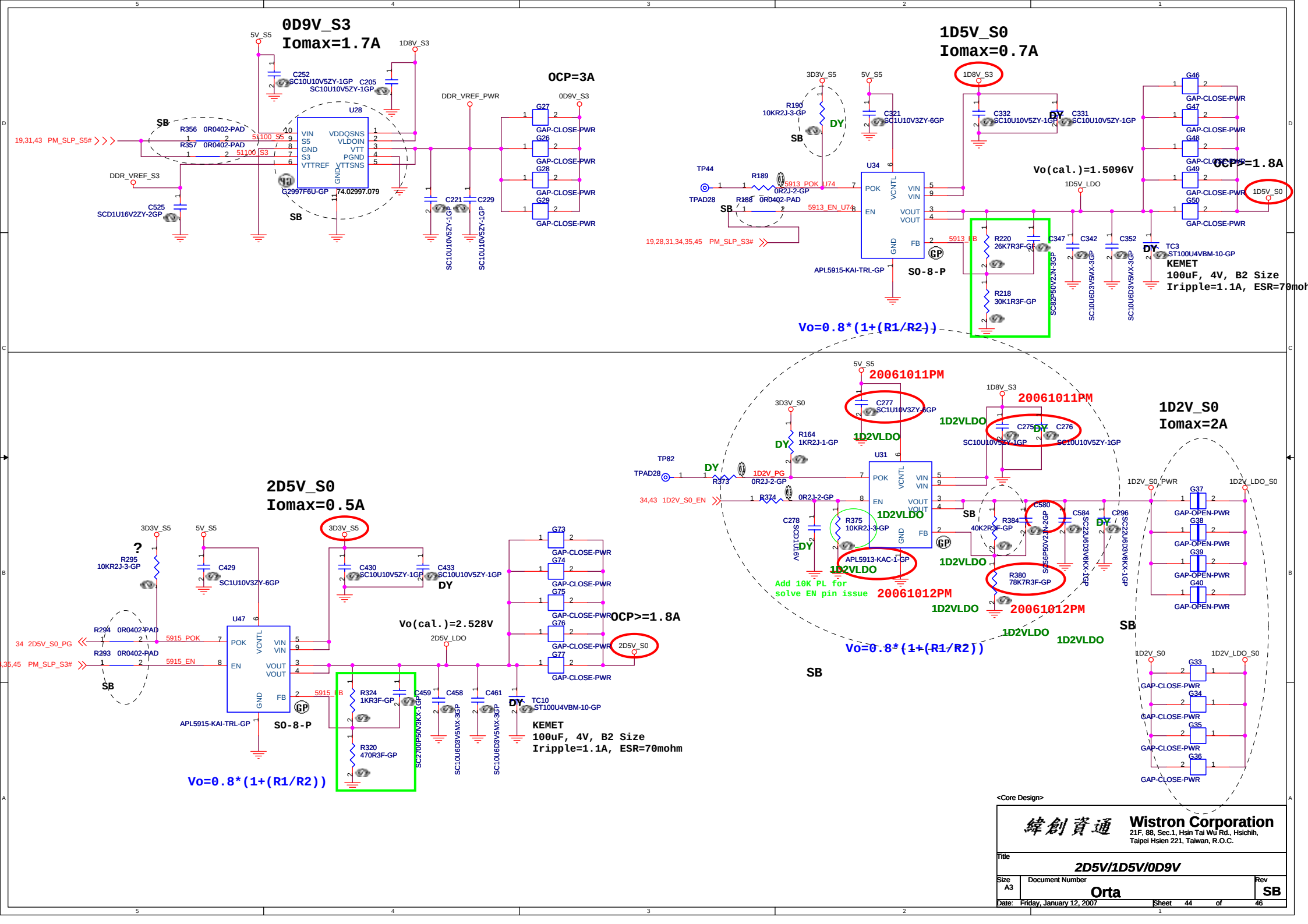
<Variant Name>

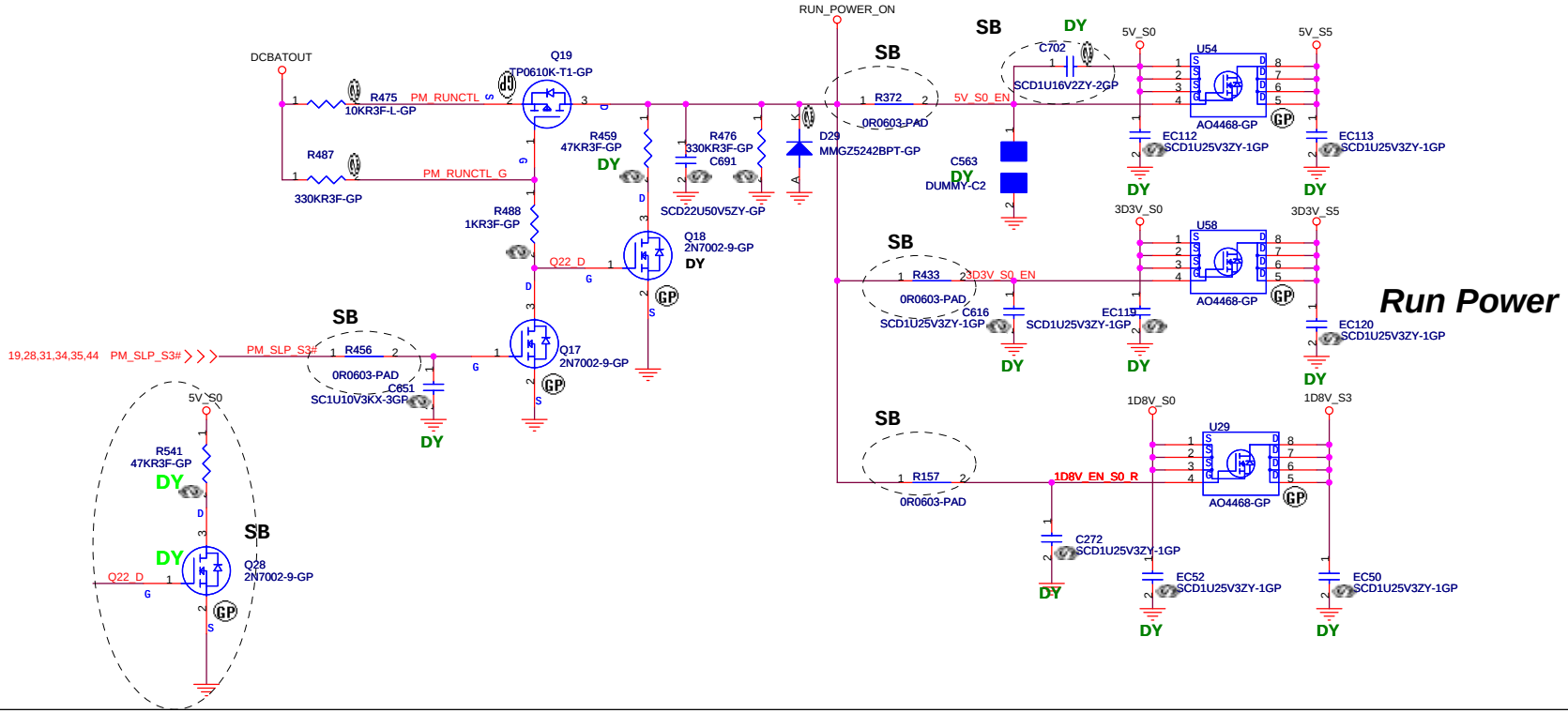
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size A3	Document Number Orta	Rev SB
Date: Friday, January 12, 2007	Sheet 41 of 46	

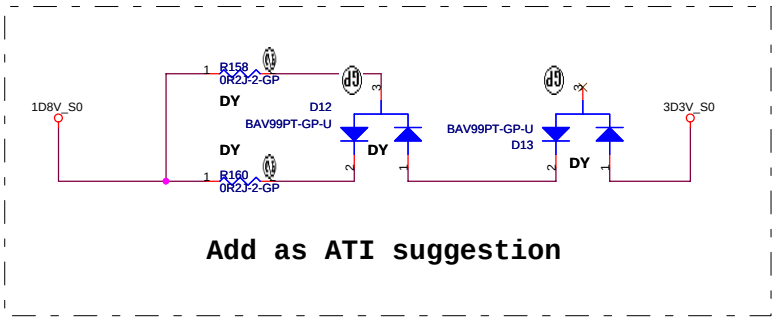

DCBATOUT
DCBATOUT_6236
SB
TC25 SE100U25VM-L1-GP
G32 G31 G30 G45 G44 G43 G42 GAP-CLOSE-PWR
C284 C577 C578
SCD1U50V3ZY-GP SC10U25V6KX-1GP SC10U25V6KX-1GP
U30 AO4468-GP 84.04468.037
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
Cyntec
DCR=11~13.2mohm
Irms=11A,Isat=14.5A
Iomax=5A
OCP>10A
5V_S5
G79 G78 G80 G81 G82 G83 G84 G85 GAP-CLOSE-PWR
5V_PWR
TC14 SE220U6D3VM-GP
TC15 ST220U6D3VDM-15GP
DY
R388 0R2J-2-GP
R386 0R2J-2-GP
L22 IND-3D3UH-55-GP
U33 AO4422-1-GP 84.04422.B37
Id=9.3A
Qg=9.8~nC,
Rdson=19.6~24mohm
Nippon
Chemi-Con
Al Cap.
6D3V, F61
ESR=10mohm.
NEC 220uF
6D3V, V Size
ESR=25mohm
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=400K
L~3.3uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
R391 0R2J-2-GP
C591 SCD1U25V3KX-GP
R392 100KR2F-L1-GP
R393 39KR3F-GP
LDO_EN
6236_VIN
5V_AUX_S5
C592 SC4D7U10V5KX-1GP
C597 SCD01U50V2KX-1GP
5V_VCC
R396 0R2J-2-GP
R398 0R2J-2-GP
C599 SC1U10V3KX-3GP
C603 SCD1U10V2MX-3GP
U56
GND BYP OUT1 FB1 ILIM1 POK1 EN1 UGATE1 PHASE1
LDOREFIN LDO VIN VREF3 EN_LDO VCC TON REF
REFIN2 ILIM2 OUT2 SKIP# POK2 EN2 UGATE2 PHASE2
BOOT1 LGATE1 PVCC SECFB GND PGND LGATE2 BOOT2
6236_FB1 6236_ILIM1 3V/5V_POK 3V/5V_EN 6236_UGATE1 6236_PHASE1
R387 412KR3F-GP
C589 SCD1U25V3KX-GP
74.06236.073 ISL6236IRZA-T-GP
R390 0R3-0-U-GP
6236_BOOT1
6236_LGATE1
R394 0R3-0-U-GP
C600 SCD1U25V3KX-GP
6236_BOOT2
6236_LGATE2
R401 422KR3F-GP
R399 0R2J-2-GP
6236_ILIM2 6236_SKIP# 3V/5V_POK 3V/5V_EN 6236_UGATE2 6236_PHASE2
5V_AUX_S5
C598 SC1U10V3KX-3GP
G86 GAP-CLOSE
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
Netswap 1004
DCR=8.56mohm
Iheat=11.1A, Isat=16.5A
L25 IND-2D2UH-47-GP
20061109
U35 AO4468-GP 84.04468.037
U36 AO4422-1-GP 84.04422.B37
Id=9.3A
Qg=9.8~nC,
Rdson=19.6~24mohm
Rds(on)(max):
20m ohms
C608 C338 C341
SC10U25V6KX-1GP SC10U25V6KX-1GP SCD1U50V3ZY-GP
TC18 ST220U6D3VDM-15GP
TC19 SE220U6D3VM-GP
NEC 220uF
6D3V, V Size
ESR=25mohm
Nippon
Chemi-Con
Al Cap.
6D3V, F61
ESR=10mohm
Iomax=6A
OCP>12A
3D3V_S5
3D3V_PWR
G94 G93 G92 G91 G90 G89 G88 G87 GAP-CLOSE-PWR
Maximum current:5A
If LIR=0.35
△I=5x0.35=1.75A
Vin=20V;Fsw=500K
L~2.2uH
OCP:5x2=10A
Iocp=10-(1.75/2)~9.125A
Vth=9.125A*24mOhm=219mV
R(Ilim)=(219mV*10)/5uA
~438K--->442K
35 S5PWR_ENABLE
R403 2KR2F-3-GP
3V/5V_EN
R400 200KR2F-L-GP
3D3V_PWR
DY
R402 100KR2J-1-GP
3V/5V_POK 34
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6236 5V 3D3V
Size A3
Document Number
Orta
Rev
SB
Date: Friday, January 12, 2007
Sheet 42 of 46


DCBATOUT
DCBATOUT_51124
SB
TC26 SE100U25VM-L1-GP
GAP-CLOSE-PWR
Id=9.6A
Qg=18~nC,
Rdson=13.5~16.5mohm
U23 AO4406-1-GP
C63 SC10U25V6KX-1GP
C47 SC10U25V6KX-1GP
C67 SCD1U50V3ZY-GP
51124_DRVH1
51124_LL1
Tai-Tech
DCR=3.5m ohm
Irms=20A,Isat=28A
L9 IND-1D5UH-34-GP
1D8V_PWR
1D8V Iomax=8A
OCP>16A
Voutsetting=1.8046V
U22 AO4706-GP
R33 64K9R2F-1-GP
DY
C37 SC33PSH50V3JN-GP
C427 SCD1U50V3ZY-GP
TC7 ST220U4VDM-L5-GP
TC6 SE390U2D5VM-2GP
Nippon Chemi-Con
Al Cap.
390uF/2D5V
ESR=15mohm
51124_VFB1
R30 47KR3F-GP
51124_DRVL1
51124_GND
Kemet
220uF/ 4V
ESR=15mohm
1D8V_S3
G72 G71 G70 G69 G68 G67 G66 G65 G64 G63
3D3V_S5
R36 10KR2J-3-GP
R38 10KR2J-3-GP
Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm
P/H CPU CORE PAGE
G16
GAP-CLOSE
1D8V_S3_PWRGD 34
1D2V_PWRGD 34
5V_S5
C81 SC4D7U10V5ZY-3GP
R65 3D3R3J-L-GP
C75 SC1U10V3ZY-6GP
1D2V_PWR
1D8V_PWR
51124_VFB2
51124_VFB1
51124_PGD1
51124_PGD2
U18
VFB1 VFB2 VO1 VO2
PGOOD1 PGOOD2
V5FILT V5IN EN1 EN2 LL1 LL2 TRIP1 TRIP2 VBST1 VBST2 DRVL1 DRVL2
TONSEL DRVH1 DRVH2 PGND1 PGND2 GND GND
51124_V5FILT
51124_TONSEL
R67
R74 10KR2J-3-GP
0R2J-2-GP
19,31,44 PM_SLP_S5#
34,44 1D2V_S0_EN
R43 0R2J-2-GP
51124_EN1_1
51124_EN2_1
51124_LL1
51124_LL2
20061113
C46 SCD01U25V2KX-3GP
C53 SCD01U25V2KX-3GP
TPS51124RGER-GPU1
OCP
51124_TRIP1
51124_TRIP2
R66 10KR3F-L-GP
R70 10KR3F-L-GP
20061109
51124_DRVL2
51124_DRVL1
51124_VBST1
51124_VBST2
R57 0R3-0-U-GP
R58 0R3-0-U-GP
C61 SCD1U50V3ZY-GP
C62 SCD1U50V3ZY-GP
G24
GAP-CLOSE-PWR
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
U13 AO4468-GP
C22 SC10U25V6KX-1GP
C413 SC10U25V6KX-1GP
C29 SCD1U50V3ZY-GP
L7 IND-1D5UH-34-GP
Netswap
DCR=7.5m ohm
Irms=12A,Isat=20A
U12 AO4706-GP
Id=9.6A
Qg=18~nC,
Rdson=13.5~16.5mohm
1D2V_PWR
1D2V Iomax=8A
OCP>16A
Voutsetting=1.2047V
C42 SC33PSH50V3JN-GP
R28 1KR2F-3-GP
C425 SCD1U50V3ZY-GP
TC5 ST220U4VDM-L5-GP
TC4 SE390U2D5VM-2GP
R25 1K69R2F-2-GP
R26 47KR2F-GP
Kemet
220uF/ 4V
ESR=15mohm
Nippon Chemi-Con
Al Cap.
390uF/2D5V
ESR=15mohm
1D2V_S0
G53 G54 G55 G56 G57 G58 G59 G60 G61 G62
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
Vout=0.758V*(R1+R2)/R2
1D2VLDO
SC150P50V2JN-3GP
C700
R31 10KR2J-3-GP
3D3V_S0
U8 NC7SZ08M5X-NL-GP
C38 SCD1U16V2ZY-2GP
0R0402-PAD
R22
16,23,28,31,33 LPC_RST#
19 PWM_CTRL
12 STRP_DATA
U7 NC7SZ126P5X-GP
L4 IND-1D8UH-3-GP
VX
C34
RX
STRP_DATA | 1D2V(VCC_NB)
0 | 1.0
1 | 1.2
GND | OPEN | V5FILT
TONSEL | 230k/CH1 283k/CH2 | 283k/CH1 346k/CH2 | 346k/CH1 423k/CH2
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51124 1D8V 1D2V
Size A3
Document Number
Orta
Rev SB
Date: Friday, January 12, 2007
Sheet 43 of 46


0D9V_S3
Iomax=1.7A
OCP=3A
5V_S5
1D8V_S3
C252
SC10U10V5ZY-1GP
C205
SC10U10V5ZY-1GP
U28
SB
R356 0R0402-PAD
R357 0R0402-PAD
19,31,43 PM_SLP_S5#
51100_S5
51100_S3
VIN
S5
GND
S3
VTTREF
VDDQSNS
VLDOIN
VTT
PGND
VTTSNS
GND
G2997F6U-GP
74.02997.079
DDR_VREF_PWR
DDR_VREF_S3
C525
SCD1U16V2ZY-2GP
C221
C229
SC10U10V5ZY-1GP
0D9V_S3
G27
G26
G28
G29
GAP-CLOSE-PWR
1D5V_S0
Iomax=0.7A
OCP=1.8A
3D3V_S5
5V_S5
1D8V_S3
R190
10KR2J-3-GP
DY
SB
C321
SC1U10V3ZY-6GP
C332
SC10U10V5ZY-1GP
C331
SC10U10V5ZY-1GP
TP44
TPAD28
R189
0R2J-2-GP
R188 0R0402-PAD
5913_POK_U74
5913_EN_U74
19,28,31,34,35,45 PM_SLP_S3#
U34
POK
EN
VCNTL
VIN
VOUT
GND
FB
APL5915-KAI-TRL-GP
SO-8-P
Vo(cal.)=1.5096V
1D5V_LDO
R220
26K7R3F-GP
R218
30K1R3F-GP
SC82P50V2JN-3GP
C347
C342
C352
SC10U6D3V5MX-3GP
TC3
ST100U4VBM-10-GP
KEMET
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70moh
Vo=0.8*(1+(R1/R2))
G46
G47
G48
G49
G50
2D5V_S0
Iomax=0.5A
OCP>=1.8A
3D3V_S5
5V_S5
R295
10KR2J-3-GP
C429
SC1U10V3ZY-6GP
C430
SC10U10V5ZY-1GP
C433
SC10U10V5ZY-1GP
DY
U47
34 2D5V_S0_PG
R294 0R0402-PAD
R293 0R0402-PAD
5915_POK
5915_EN
5915_FB
R324
1KR3F-GP
R320
470R3F-GP
C459
C458
C461
SC2700P50V3KX-1GP
SC10U6D3V5MX-3GP
TC10
ST100U4VBM-10-GP
KEMET
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm
Vo(cal.)=2.528V
2D5V_LDO
2D5V_S0
G73
G74
G75
G76
G77
Vo=0.8*(1+(R1/R2))
1D2V_S0
Iomax=2A
20061011PM
20061012PM
3D3V_S0
1D8V_S3
TP82
TPAD28
R164
1KR2J-1-GP
R373
1D2V_PG
0R2J-2-GP
34,43 1D2V_S0_EN
R374
C277
SC1U10V3ZY-6GP
C275
C276
SC10U10V5ZY-1GP
U31
C278
SCD1U16V
R375
10KR2J-3-GP
APL5913-KAC-1-GP
1D2VLDO
Add 10K PL for
solve EN pin issue
R384
40K2R3F-GP
R380
78K7R3F-GP
C580
C584
C296
SC2R2D6D3V6MX-1GP
SC2R2D6D3V6KX-1GP
SC82P50V2JN-2GP
1D2V_S0_PWR
1D2V_LDO_S0
G37
G38
G39
G40
GAP-OPEN-PWR
G33
G34
G35
G36
GAP-CLOSE-PWR
Vo=0.8*(1+(R1/R2))
SB
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
2D5V/1D5V/0D9V
Size
A3
Document Number
Orta
Rev
SB
Date: Friday, January 12, 2007
Sheet 44 of 46



Run Power

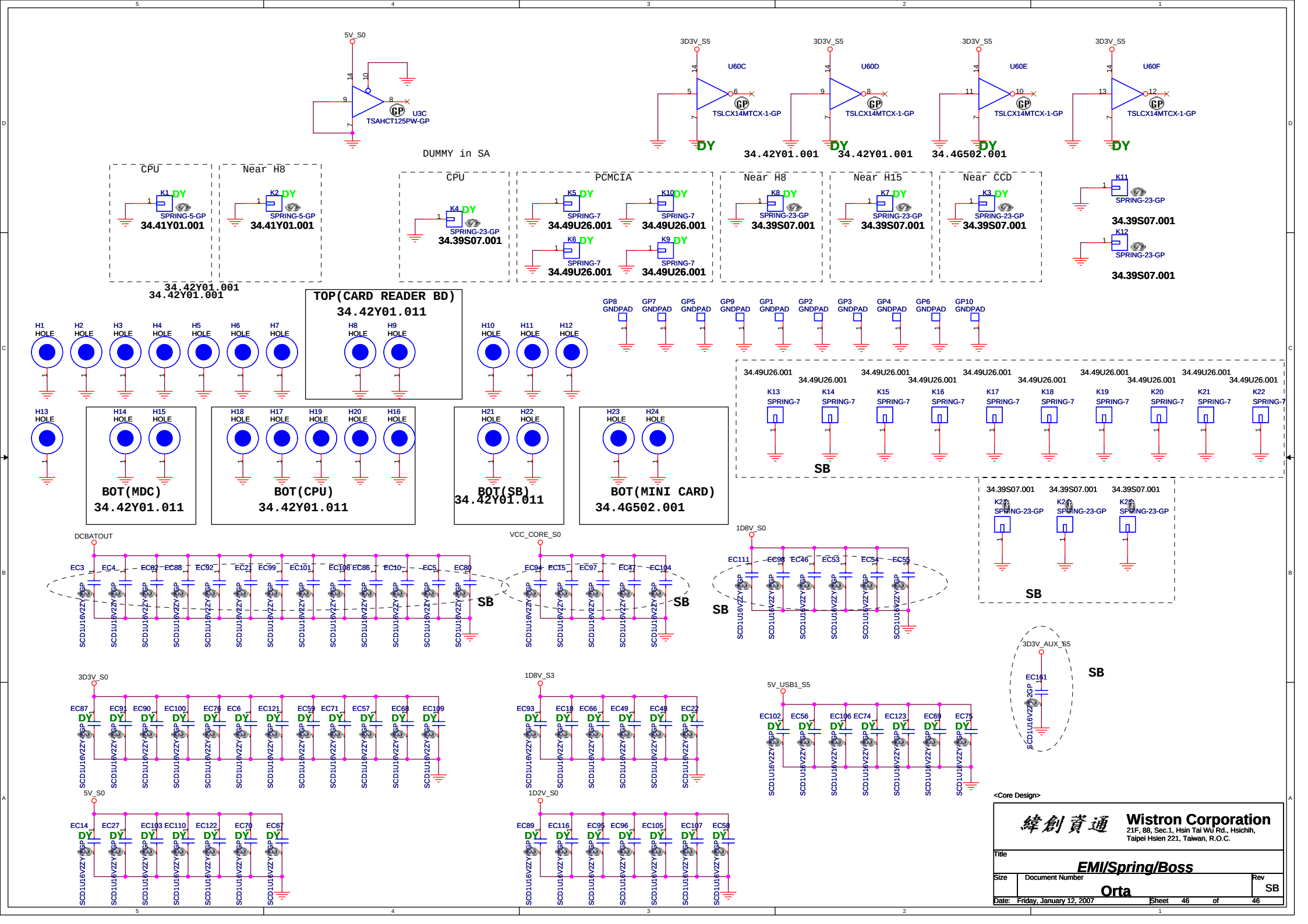


Add as ATI suggestion

Power On Logic

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***PWR CTL LOGIC / PWR PLANE***
Size: A3	Document Number: Orta
Rev: SB	
Date: Friday, January 12, 2007	Sheet 45 of 46


5V_S0
U3C
TSAHCT125PW-GP
DUMMY in SA
3D3V_S5
U60C
U60D
U60E
U60F
TSLCX14MTCX-1-GP
DY
34.42Y01.001
34.42Y01.001
34.4G502.001
CPU
Near H8
K1 DY
K2 DY
SPRING-5-GP
34.41Y01.001
34.41Y01.001
34.42Y01.001
34.42Y01.001
CPU
PCMCIA
Near H8
Near H15
Near CCD
K4 DY
SPRING-23-GP
34.39S07.001
K5 DY
K10 DY
K6 DY
K9 DY
SPRING-7
34.49U26.001
K8 DY
K7 DY
K3 DY
34.39S07.001
K11
K12
TOP(CARD READER BD)
34.42Y01.011
H1 HOLE
H2 HOLE
H3 HOLE
H4 HOLE
H5 HOLE
H6 HOLE
H7 HOLE
H8 HOLE
H9 HOLE
H10 HOLE
H11 HOLE
H12 HOLE
GP8 GNDPAD
GP7 GNDPAD
GP5 GNDPAD
GP9 GNDPAD
GP1 GNDPAD
GP2 GNDPAD
GP3 GNDPAD
GP4 GNDPAD
GP6 GNDPAD
GP10 GNDPAD
K13
K14
K15
K16
K17
K18
K19
K20
K21
K22
SB
H13 HOLE
H14 HOLE
H15 HOLE
H18 HOLE
H17 HOLE
H19 HOLE
H20 HOLE
H16 HOLE
H21 HOLE
H22 HOLE
H23 HOLE
H24 HOLE
BOT(MDC)
34.42Y01.011
BOT(CPU)
34.42Y01.011
BOT(SB)
34.42Y01.011
BOT(MINI CARD)
34.4G502.001
DCBATOUT
VCC_CORE_S0
1D8V_S0
SCD1U16V2ZY-2GP
3D3V_S0
1D8V_S3
5V_USB1_S5
3D3V_AUX_S5
5V_S0
1D2V_S0
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
Orta
Rev
SB
Date: Friday, January 12, 2007
Sheet 46 of 46