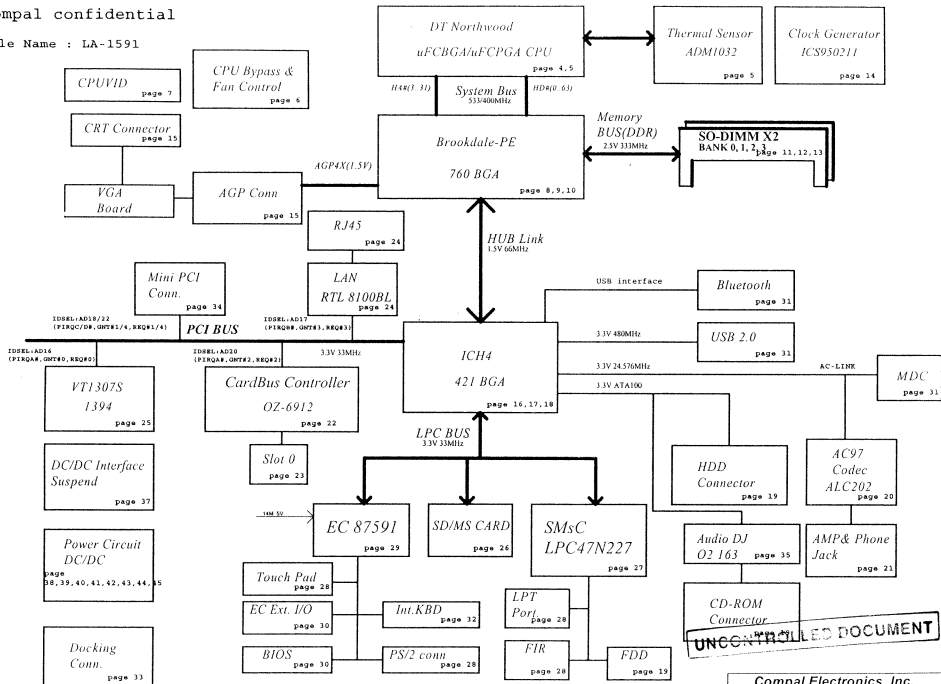




UNCONTROLLED DOCUMENT

SCHEMATICS VERSION LIST

VERSION	ISSUE DATE	REMARK
0.00		FIRST PREVIEW
0.01		
0.02		

Power Management table

Signal State	+3VALW +5VALW +12VALW	+3V +5V +2.5V	+3VS +5VS +1.5VS +1.2VP +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

	PCB Rev	CHIPS Rev
SST-Build	0.1	
PT-Build		
ST-Build		
QT-Build		

Ceramic Capacitor Spec Guide:

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7
CODE	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R

S	D	A	B	C	D	E	F	G
NP0	C0G		BJ	CM	CJ	CK	SH	SJ

H	I	J	
UJ	UK	SL	

Tolerance:

Symbol	A	B	C	D	F	G	H	J
CODE	±0.05PF	±0.1PF	±0.25PF	±0.5PF	±1PF	±2%	±3%	±5%

K	M	N	P	Q	V	X	Z	
±10%	±20%	±30%	±100, -0%	±30, -10%	±20, -10%	±40, -20%	±80, -20%	

SMBUS Control Table

	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (U43)	THERMAL SENSOR (U91)	S001MM	CLK CHIP	MINI PCI
SMB_EC_CK1 SMB_EC_DA1	NS 87591	✓	✓	✓ (10019)	✗	✗	✗	✗	✗
SMB_EC_CK2 SMB_EC_DA2	NS 87591	✗	✗	✗	✓	✓	✗	✗	✗
SMB_CLK SMB_DATA	ICH4	✗	✗	✗	✗	✗	✓	✓	✓

NOTE1:

@XX : Depop component

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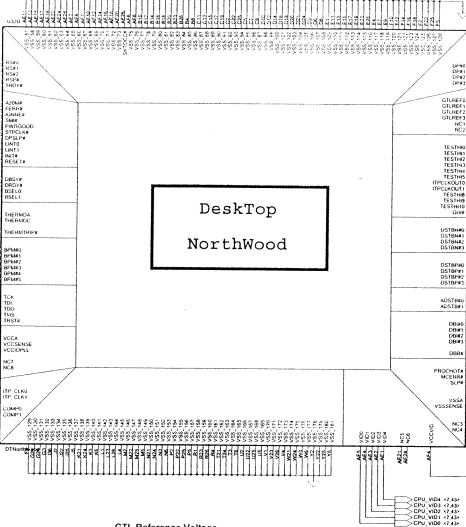
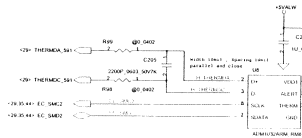
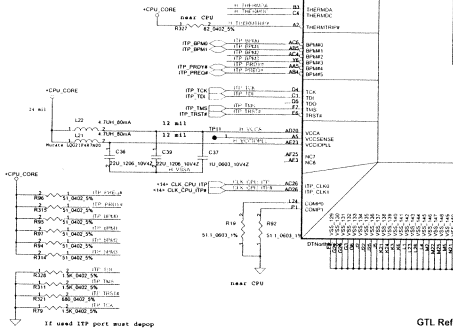
SCHEMATIC, M/B LA-1591

Docuement Number
401235

Date: 2001.11.19

Sheet 3 of 47

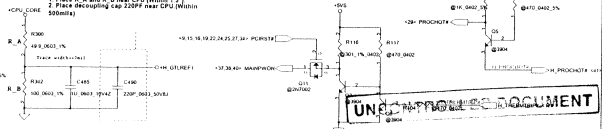
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GTL Reference Voltage

Layout note :

1. Place R_A and R_B near CPU (Within 1.5").
2. Place decoupling cap 220PF near CPU.(Within 500mils)



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Date	Document Number
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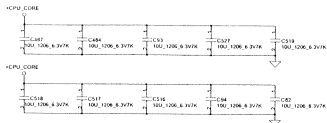
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Exponent	5	61	4
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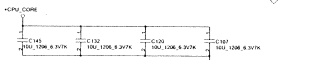
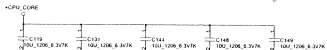
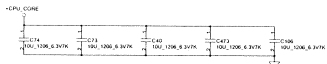
Layout note

Place close to CPU, Use 2-3 vias per PAD.
Place .22uF caps underneath balls on solder side
Place 10uF caps on the peripheral near balls.
Use 2-3 vias per PAD.

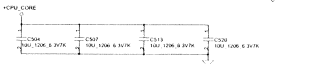
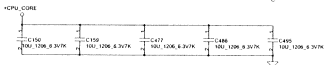
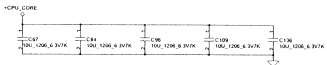
Please place these cap in the socket cavity area



Please place these cap on the socket south side



Please place these cap on the socket south side



Layout note :

Place close to CPU power and ground pin as possible
(c) (tech)

For Desktop's CPU:

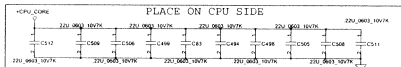
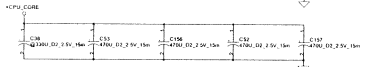
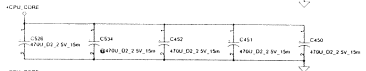
ESR total=0.75m ohm
C total=6350uF

For Mobile's CPU:

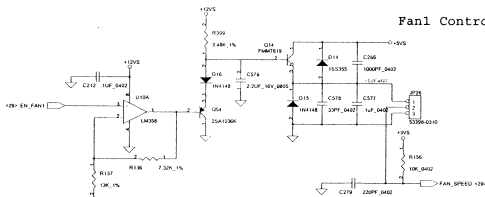
```

R3R total=1.875m ohm
C total=2590uF

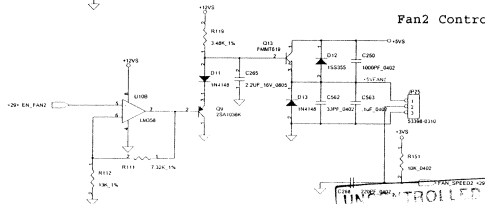
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Fan1 Control circuit



Fan2 Control circuit

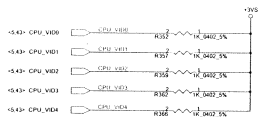


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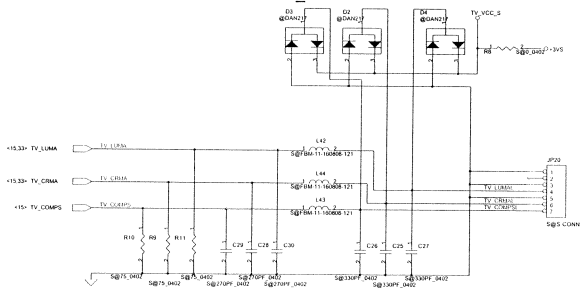
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SCHEMATIC, MVB LA-1591

Size	Document Number				
Content	401235				
Date	1997	01/10	2003	Sheet	6 of 4



TV_OUT CONNECTOR



MO/DT_CPU	Mobile CPU					Desktop CPU				
	1					0				
VID	4	3	2	1	0	4	3	2	1	0
VCC										
1.750V	0	0	0	0	0	0	0	1	0	0
1.700V	0	0	0	0	1	0	0	1	1	0
1.650V	0	0	0	1	0	0	1	0	0	0
1.600V	0	0	0	1	1	0	1	0	1	0
1.550V	0	0	1	0	0	0	1	1	0	0
1.500V	0	0	1	0	1	0	1	1	1	0
1.450V	0	0	1	1	0	1	0	0	0	0
1.400V	0	0	1	1	1	1	0	0	1	0
1.350V	0	1	0	0	0	1	0	1	0	0
1.300V	0	1	0	0	1	1	0	1	1	0
1.250V	0	1	0	1	0	1	1	0	0	0
1.200V	0	1	0	1	1	1	1	0	1	0
1.150V	0	1	1	0	0	1	1	1	0	0
1.100V	0	1	1	0	1	1	1	1	1	0
1.050V	0	1	1	1	0	X	X	X	X	X
1.000V	0	1	1	1	1	X	X	X	X	X
0.975V	1	0	0	0	0	X	X	X	X	X
0.950V	1	0	0	0	1	X	X	X	X	X
0.925V	1	0	0	1	0	X	X	X	X	X
0.900V	1	0	0	1	1	X	X	X	X	X
0.875V	1	0	1	0	0	X	X	X	X	X
0.850V	1	0	1	0	1	X	X	X	X	X
0.825V	1	0	1	1	0	X	X	X	X	X
0.800V	1	0	1	1	1	X	X	X	X	X
0.775V	1	1	0	0	0	X	X	X	X	X
0.750V	1	1	0	0	1	X	X	X	X	X
0.725V	1	1	0	1	0	X	X	X	X	X
0.700V	1	1	0	1	1	X	X	X	X	X
0.675V	1	1	1	0	0	X	X	X	X	X
0.650V	1	1	1	0	1	X	X	X	X	X
0.625V	1	1	1	1	0	X	X	X	X	X
0.600V	1	1	1	1	1	X	X	X	X	X
VRM output off						1	1	1	1	1

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Document Number

401235

Date 11/19/2003

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```

DDR_CLK4 <= 12>
DDR_CLK4# <= 12>
DDR_CLK5 <= 12>
DDR_CLK5# <= 12>

```



1. HX_RCOMP, HY_RCOMP Trace width 10 mil
2. Terminator Max 500 mil.

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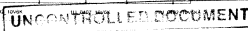
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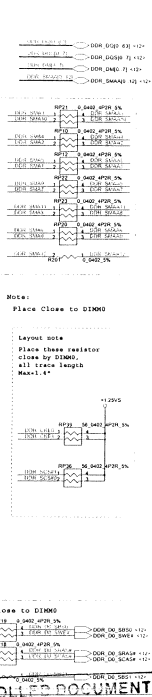
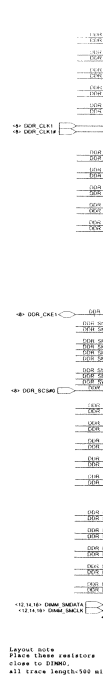
416 SCHEMATIC, M/B LA-159

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Note: Place Close to DIM000

DB - DGR, SR405 $\frac{1}{2}$ 2.5K 1% 0.040 5% $\frac{1}{2}$ 2.5K 1% 0.040 5% DGR, DO, SR450 +12V
DB - DGR, SR406 $\frac{1}{2}$ 2.5K 1% 0.040 5% $\frac{1}{2}$ 2.5K 1% 0.040 5% DGR, DO, SR450 +12V

DB - DGR, SR407 $\frac{1}{2}$ 2.5K 1% 0.040 5% $\frac{1}{2}$ 2.5K 1% 0.040 5% DGR, DO, SR450 +12V
DB - DGR, SR408 $\frac{1}{2}$ 2.5K 1% 0.040 5% $\frac{1}{2}$ 2.5K 1% 0.040 5% DGR, DO, SR450 +12V

DB - DGR, SR409 $\frac{1}{2}$ 2.5K 1% 0.040 5% $\frac{1}{2}$ 2.5K 1% 0.040 5% DGR, DO, SR450 +12V
DB - DGR, SR410 $\frac{1}{2}$ 2.5K 1% 0.040 5% $\frac{1}{2}$ 2.5K 1% 0.040 5% DGR, DO, SR450 +12V

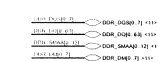
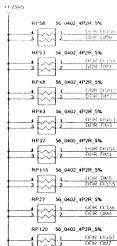
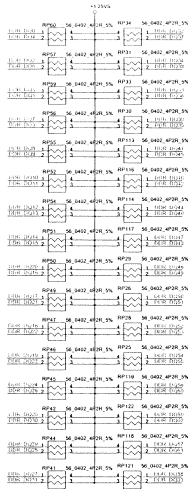
DB - DGR, SR411 $\frac{1}{2}$ 2.5K 1% 0.040 5% $\frac{1}{2}$ 2.5K 1% 0.040 5% DGR, DO, SR450 +12V

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SCHEMATIC: MIB LA-1591

Date: Document Number: Rev:
4/01/15 4011215 1

DESIGNED BY: CHECKED BY: DATE:
NED/JS



0- DOR_CLK#
 0- DOR_CLK#

0- DOR_CKE#
 0- DOR_CKE#

0- DOR_CS#
 0- DOR_CS#

0- DOR_CS#
 0- DOR_CS#

0- DOR_CS#
 0- DOR_CS#

0- DOR_CS#
 0- DOR_CS#

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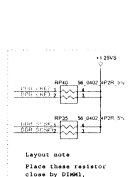
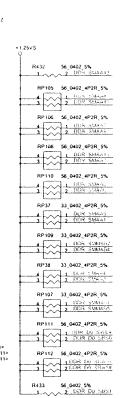
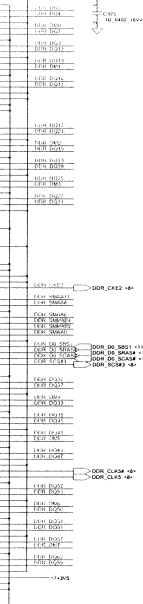
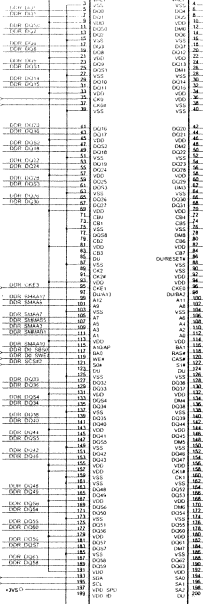
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 0- DOR_CS#

0- DOR_CS#
 0- DOR_CS#

0- DOR_CS#
 0- DOR_CS#

0- DOR_CS#
 0- DOR_CS#

0- DOR_CS#
 0- DOR_CS#



Layout note
 Place these resistor
 closely ESDS,
 all trace
 length=800mil

Layout note
 Place these resistor
 close by DIMM1,
 all trace length
 Max=0.8"

DIMM1
 Back side / H=2mm

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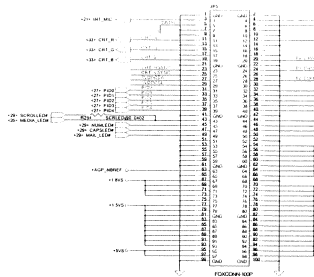
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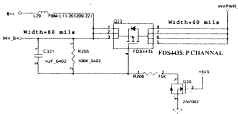
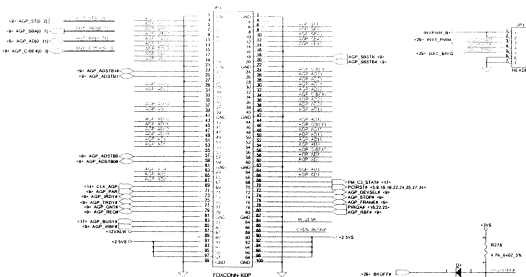
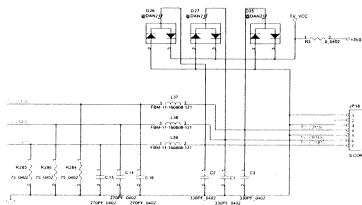
SEL[2:0]	CK-408 Speed
001	100 MHZ
011	133 MHZ

ground plane inside the part pads
one power plane inside the part pads

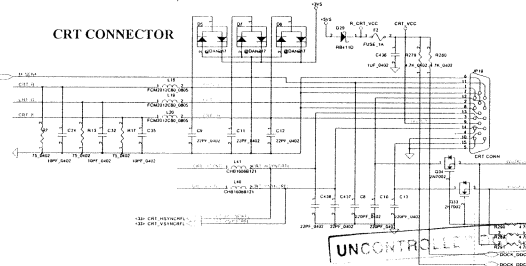
AGP 100X2 Pin connector



TV_OUT CONNECTOR



CRT CONNECTOR



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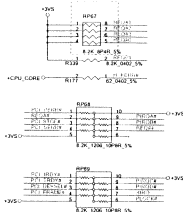
SCHEMATICALLY LA-1591

Document Number

401215

400000

PCI Pullups



Place closely pin P5



Place closely pin T21



+22.24.25.34+ A500 31K



V50A

ICH4

SM I/F

CPU I/F

HUB I/F

LAN I/F

PCI I/F

SM I/F

CPU I/F

HUB I/F

LAN I/F

PCI I/F

SM I/F

CPU I/F

HUB I/F

LAN I/F

PCI I/F

SM I/F

CPU I/F

HUB I/F

LAN I/F

PCI I/F

SM I/F

CPU I/F

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HUB I/F

LAN I/F

PCI I/F

SM I/F

CPU I/F

HUB I/F

LAN I/F

PCI I/F

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PCI I/F

SM I/F

CPU I/F

HUB I/F

LAN I/F

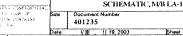
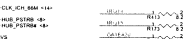
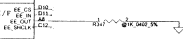
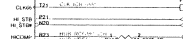
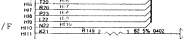
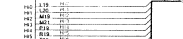
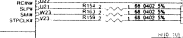
PCI I/F

SM I/F

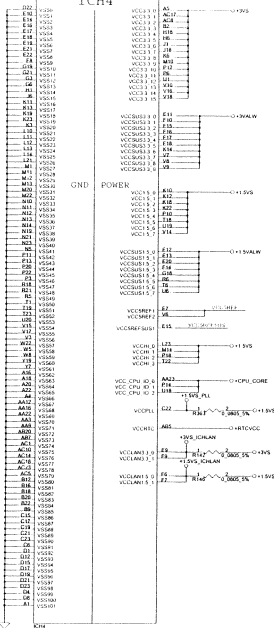
CPU I/F

HUB I/F

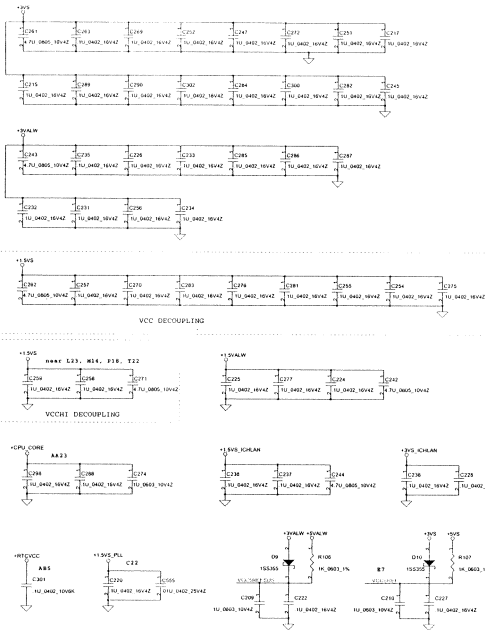
LAN I/F



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A4 A1 H1 T1 AC10 AC10 A22 AC5 R23 C23 A16 AC1 A16 T23 H23

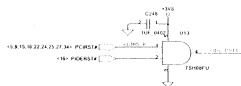


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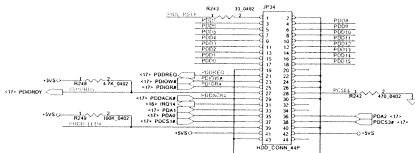
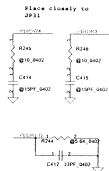
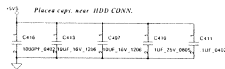
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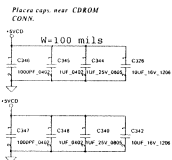
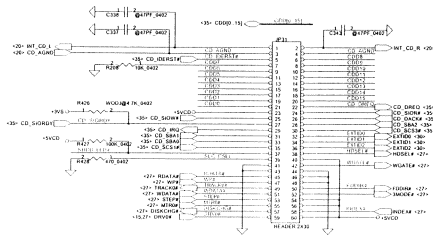
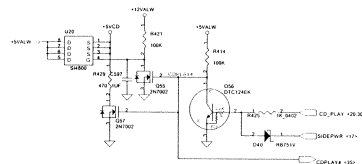
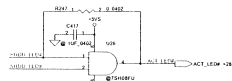
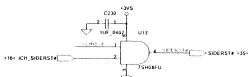
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HDD Connector



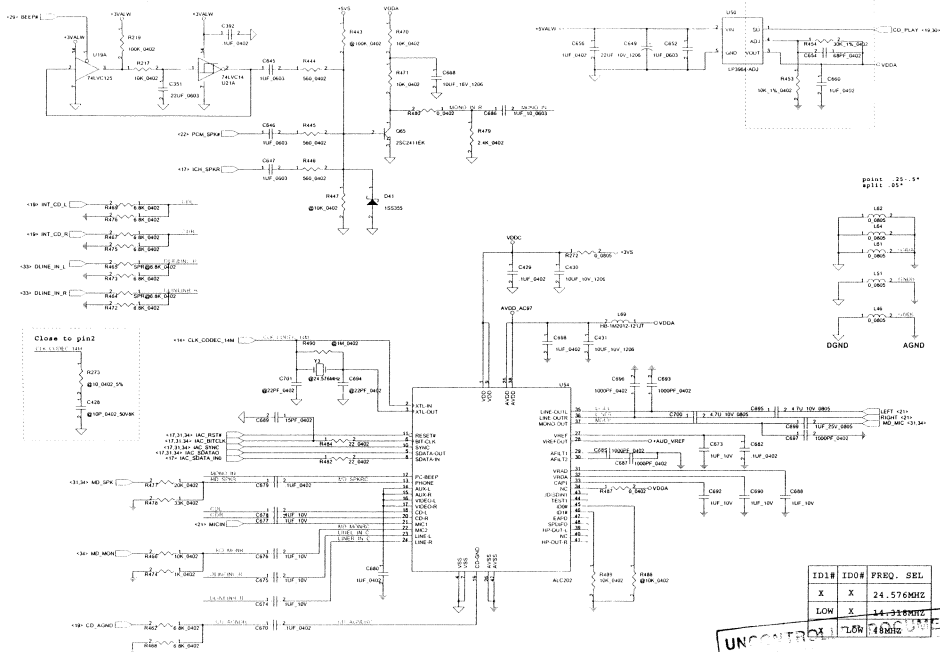
CD-ROM Connector



Extend Module ID list

DEVICE	EXTID3	EXTID1	EXTID0
FDG	0	0	0
CD-ROM	0	0	1
1.8-3.20	0	1	0
2"ud HDD	0	1	1
NONE	1	1	1

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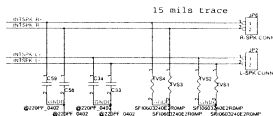
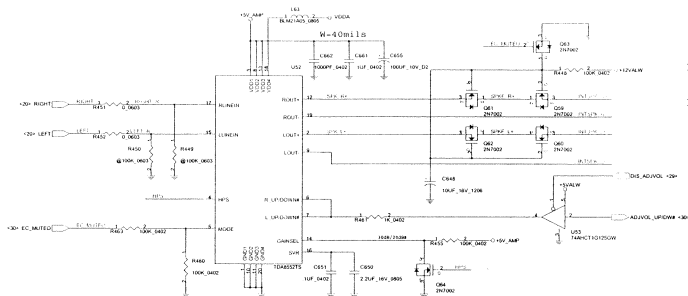
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ID1#	ID0#	FREQ. SEL
X	X	24.576MHz
LOW	X	14.318MHz
X	LOW	48MHz

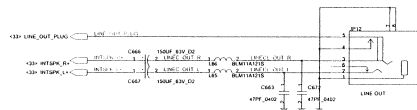
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Layout note:

- Trace widths: 15 mils.
1. SFR, R, SFR, L, SFR, R, SFR, L
2. INTSPK, R, INTSPK, L
3. LINEOUT, L, LINEOUT, R



HEADPHONE OUT



EXT. MIC



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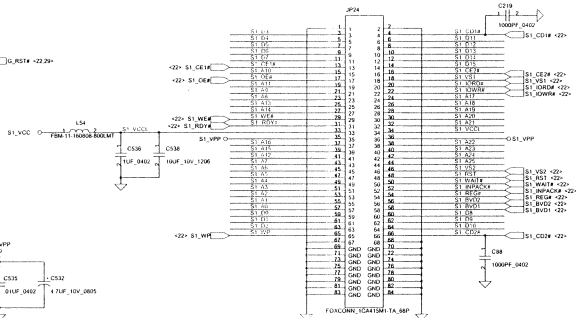
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CAREFUL HOUSING

```

<22> S1_A[0..25]
<22> S1_D[0..15]

```



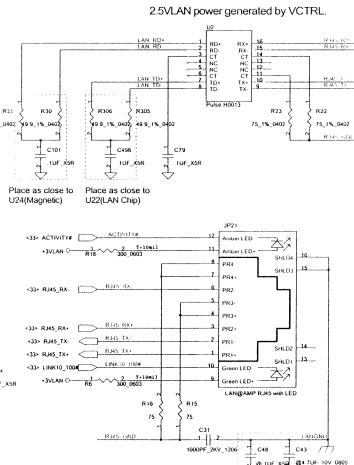
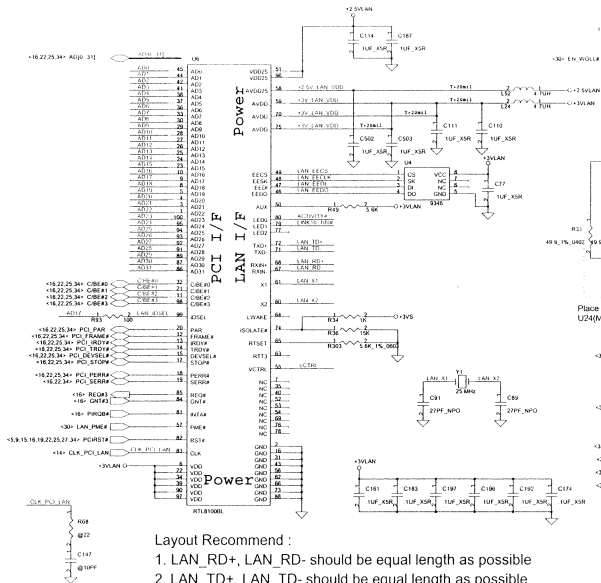
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Note : I_{max} for VDD25 = 40mA
2.5V should be ready before +3V is ready



Layout Recommend :

1. LAN_RD+, LAN_RD- should be equal length as possible
2. LAN_TD+, LAN_TD- should be equal length as possible
3. The Maximum trace length between LAN chip(U22) and Magnetic(U24) is 12cm(4.7")
4. The distance between RJ45(Conn.) and Magnetic(U24) should be as short as possible

Termination plane should be controlled
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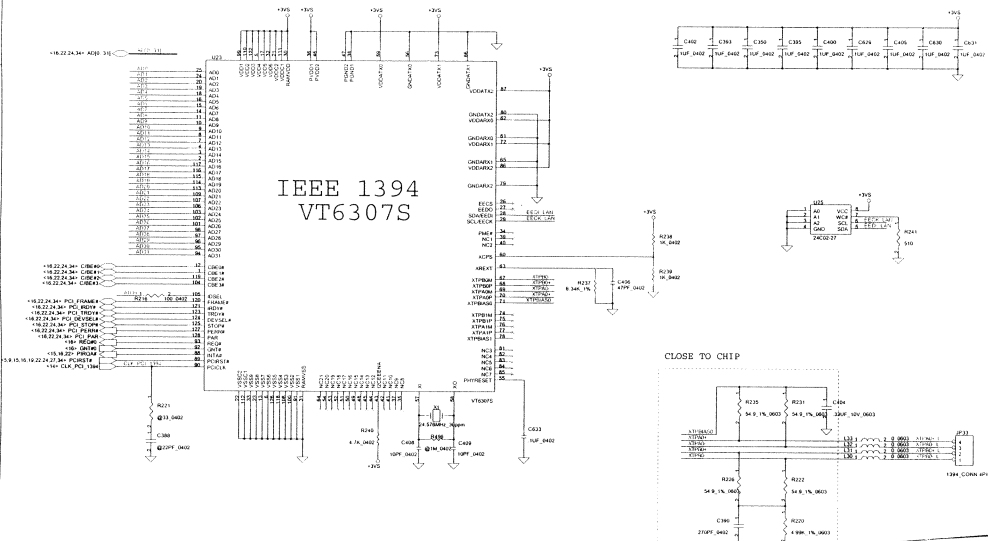
Compal Electronics, Inc.

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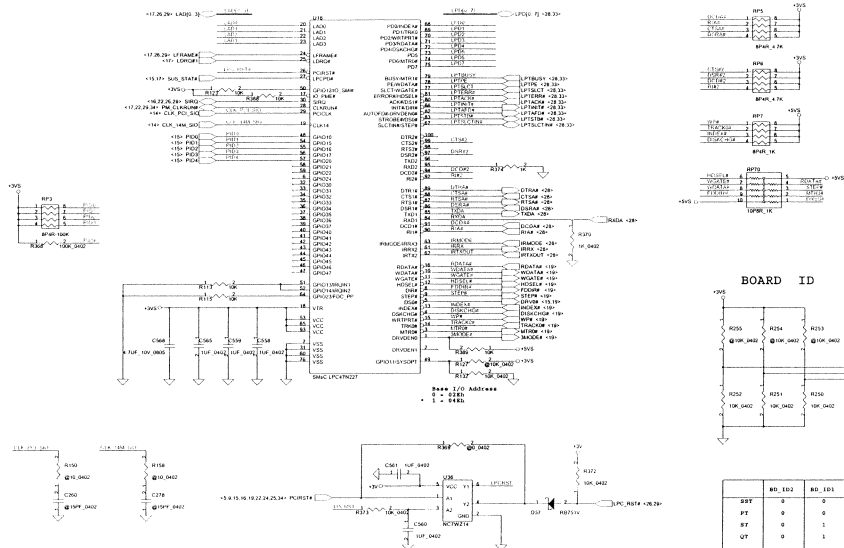
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SUPER I/O SMsC FDC47N227



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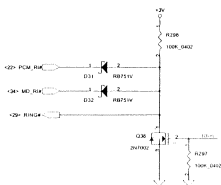
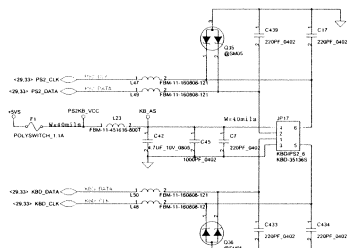
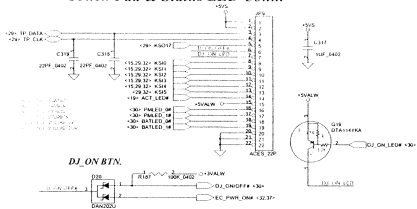
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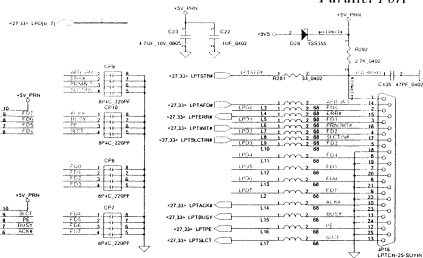
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1. *Journal of the American Medical Association*, 1997; 278: 1039-1044.

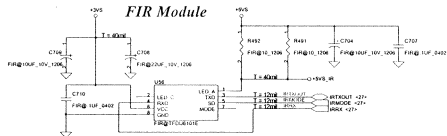
Touch Pad & Status LED Conn.



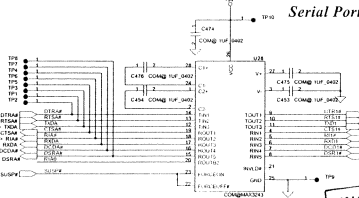
Parallel Port



FIR Module



Serial Port

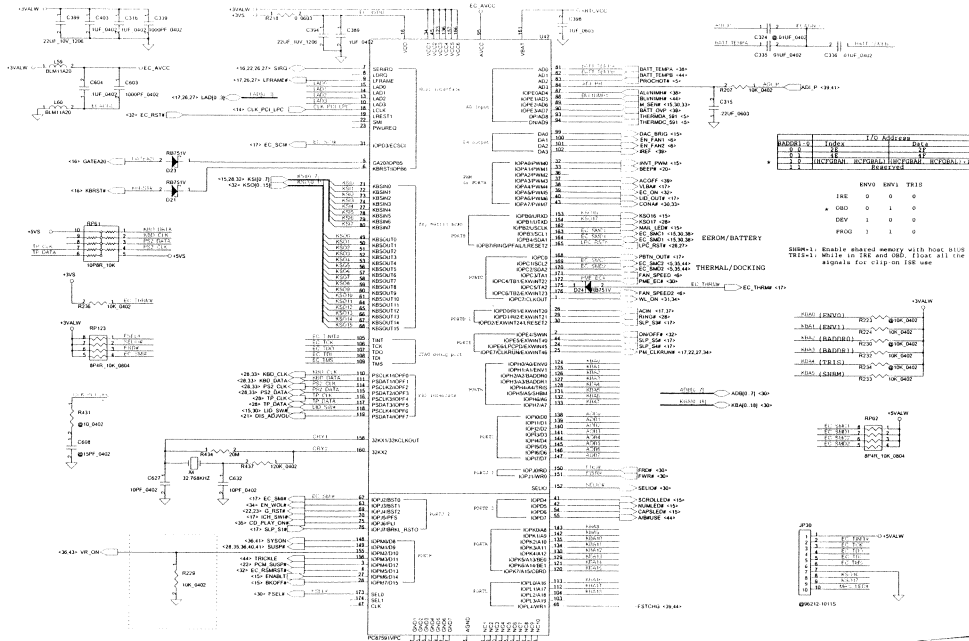


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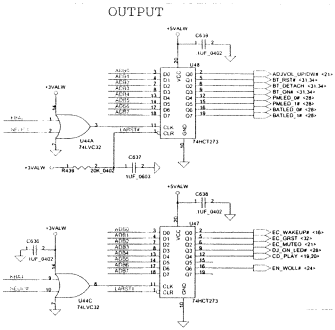
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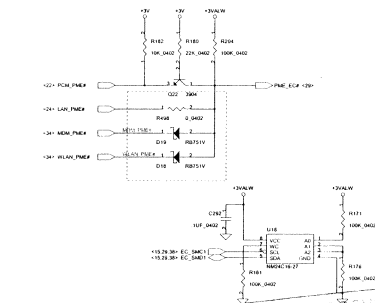
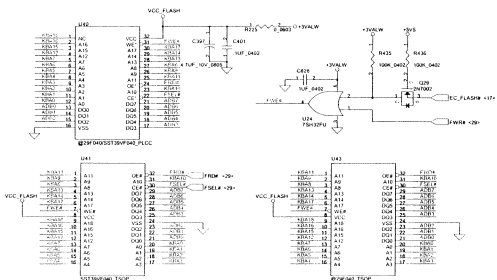
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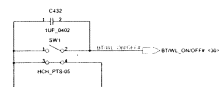
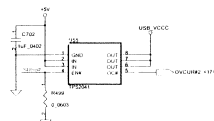
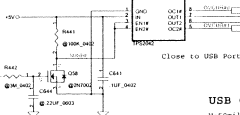
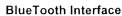
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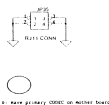
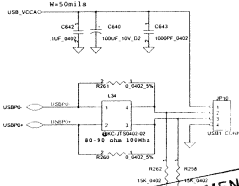
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<i>Compal Electronics, Inc.</i>			
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Document Number 401235		Rev. 2A	
Date 1/18/83	Drawn By JLH	Checked By NO	Approved By af af

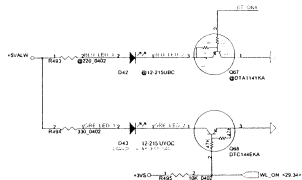
Pin 1 is NC for Pctel and connexant MDC modems
Pin 2 is NC for Pctel and connexant MDC modems



The schematic diagram shows a USB-to-serial interface circuit. At the top, a USB_VCC5V supply is connected to a 5-0hm1le resistor. Below this, there are three capacitors: C650 (10uF), C653 (100kF), and C658 (1000pF). The circuit includes a USB-D+ and USB-D- input, a USB-D+ and USB-D- output, and a USB-D+ and USB-D- output. The circuit is powered by a 5V supply and includes a 10k resistor and a 100k resistor. The output is connected to a 15k resistor and a 100k resistor.



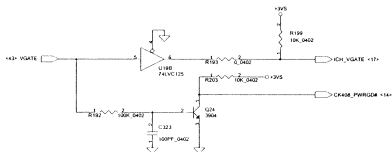
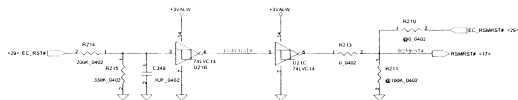
B: have primary CUBIC on either board



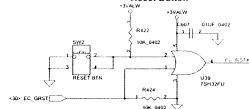
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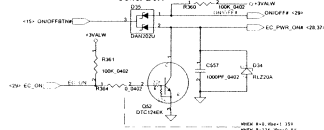
Power ON Circuit



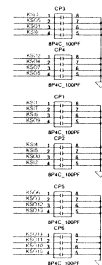
Reset Button



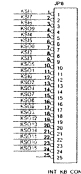
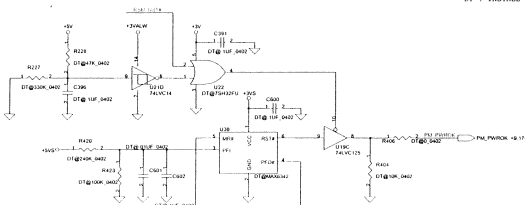
Power BTN



INT_KBD_CONN.



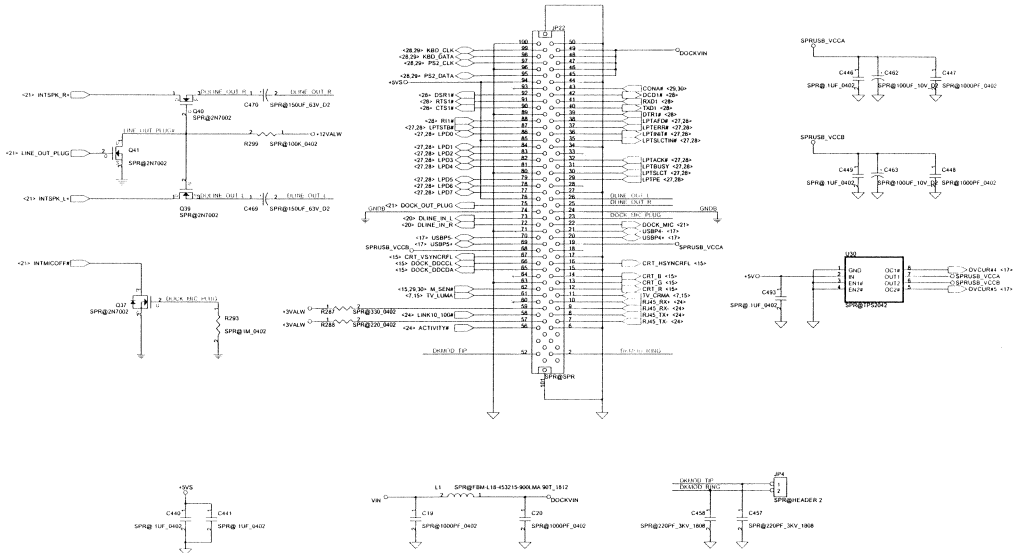
D7 : INSTALL



INT_KBD_CONN

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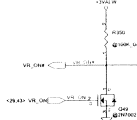
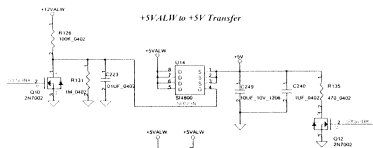
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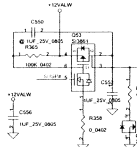
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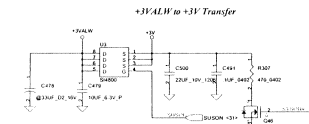
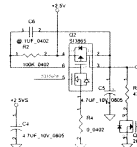
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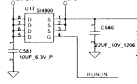
+12VALW to +12V Transfer



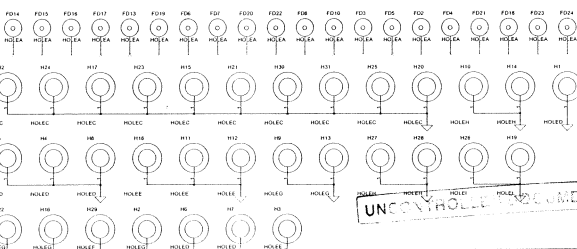
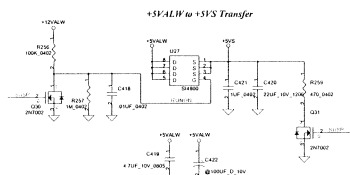
+2.5V to +2.5VS Transfer



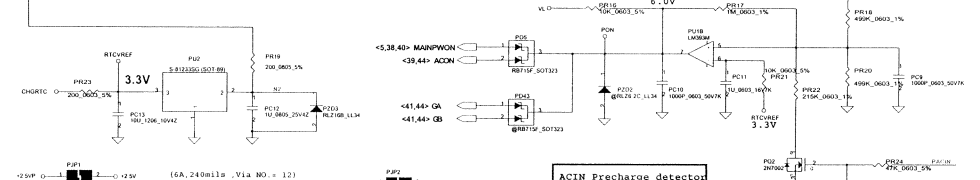
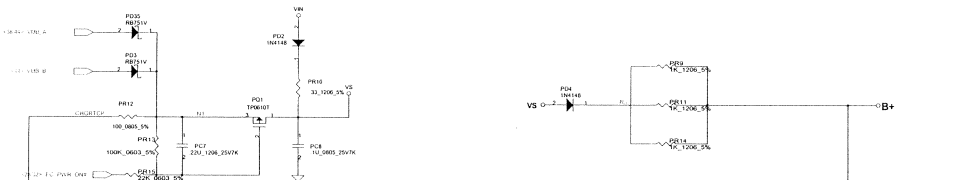
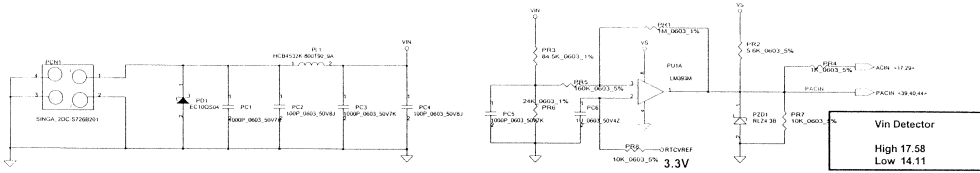
+1.5VALW to +1.5VS Transfer



RTC Battery



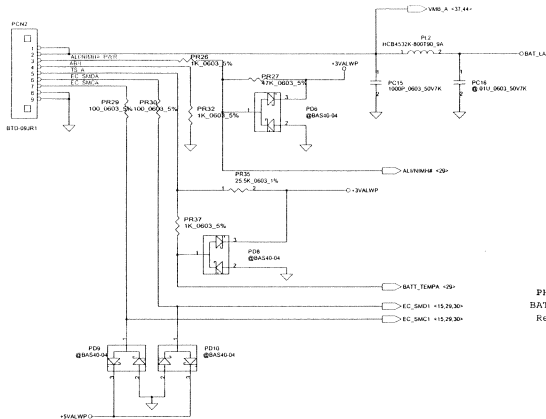
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ACIN Precharge detector

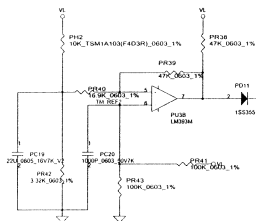
15.34	15.90	16.48
13.13	13.71	14.20

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PH1 under CPU bottom side :
CPU thermal protection at 84 degree C
Recovery at 45 degree C

PH2 near main Battery CONN :
BAT. thermal protection at 84 degree C
Recovery at 45 degree C



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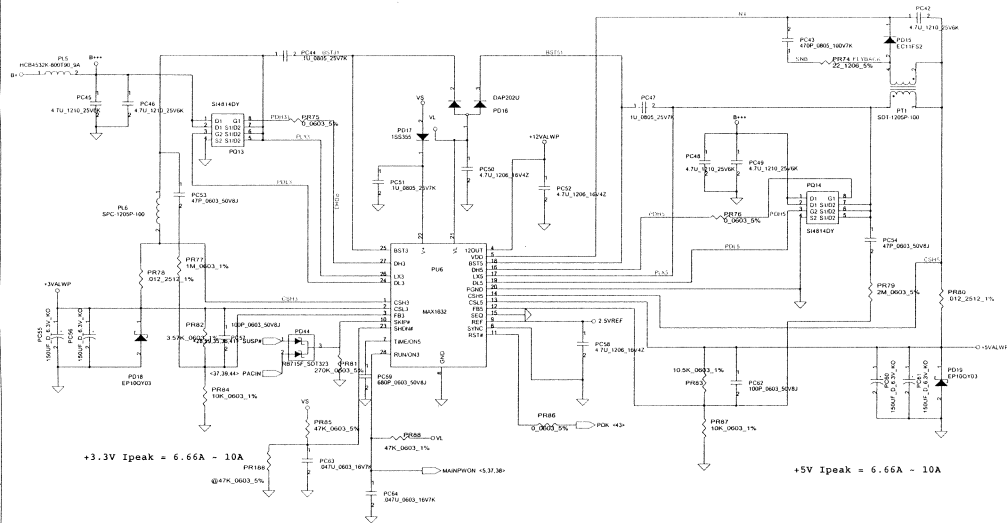
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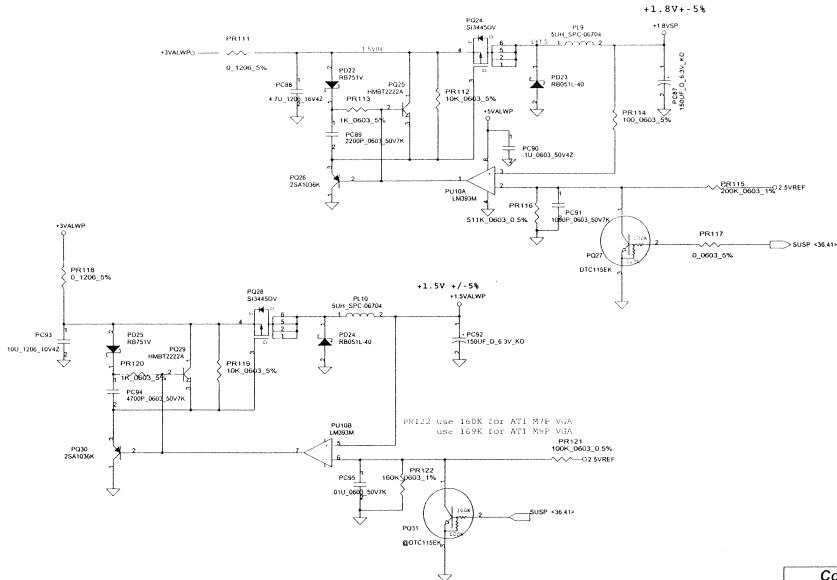


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SCHEMATIC MBL-15512

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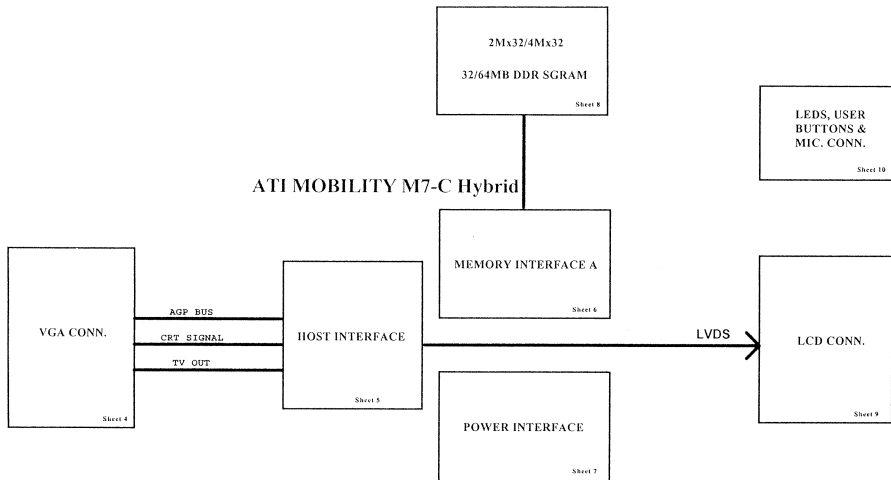
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405628

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Capacitor Naming Note

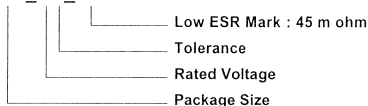
Ceramic Capacitors :

0.1U_0402_XX



Tantalum or Polymer Capacitors :

10U_D2_XX_R45



Rated Voltage :

Symbol	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	G	H	I	J	K
W.V.	2	2.5	3	3.15	4	5.5	6	6.15	6.3	8	10	12	12.5	15	16	20	25	30	35	40	50

Symbol	L	M	N	P	Q	R	S	T	U	V	W	X	Y	Z	a	b
W.V.	63	90	100	110	125	160	200	250	400	500	630	1K	2K	2.5K	3K	5K

Temperature Characteristics :

Symbol	0	1	2	3	4	5	6	7	8	9	A
Code	NPO	X5R	X7R	Y5V	Y5P	Y5U	Z5V	Z5P	Z5U	T2M	COG

Tolerance :

Symbol	A	B	C	D	F	G	H	J	K	M	N
Tolerance	+0.05PF	+0.1PF	+0.25PF	+0.5PF	+1%	+2%	+3%	+5%	+10%	+20%	+30%

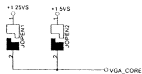
Symbol	P	Q	V	X	Z
Tolerance	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%

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SCHEMATIC, VGA/B LS-1593	
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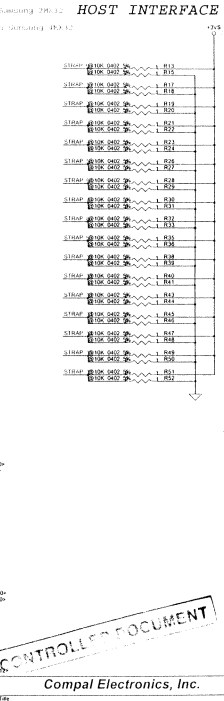
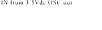
+5' AGP AD[0 3] 1'
 +5' AGP C[0B[0 3] 1'
 +5' AGP SBA[0 3] 1'
 +5' AGP ST[0 2] 1'



AGP WBF/SERR#(JP2.87) FOR M9P

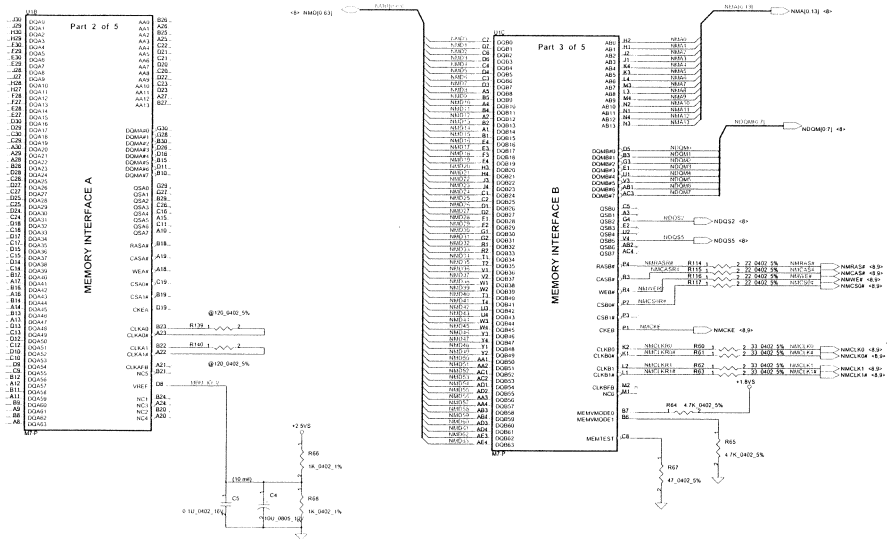
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MEMORY INTERFACE



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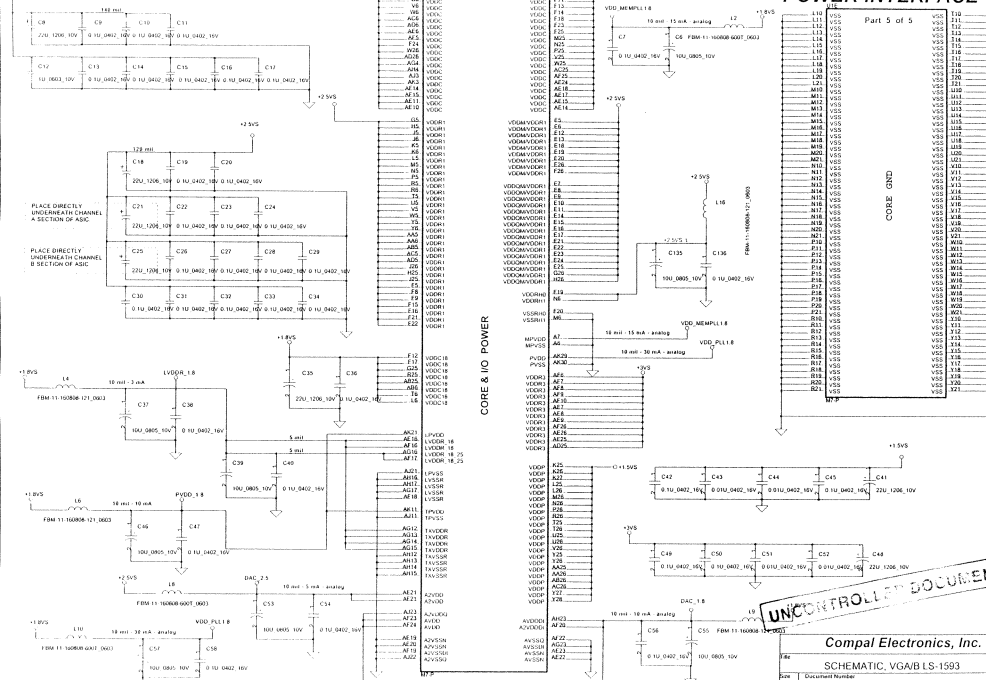
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POWER INTERFACE

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CORE GND

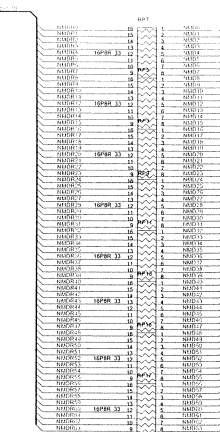
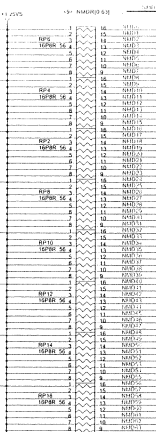
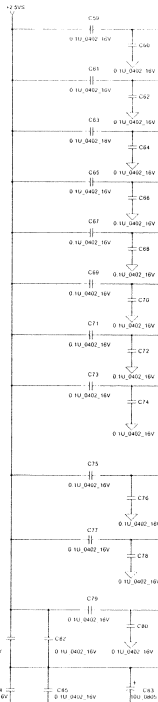


PARALLEL TERMINATION SSTL_2 CLASS I

PARALLEL TERMINATION COULD BE
OMITTED UNDER SOME
CIRCUMSTANCES. PLEASE CONSULT
WITH AHS FOR DETAIL.

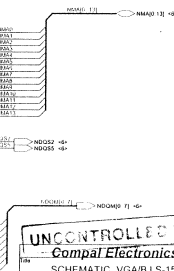
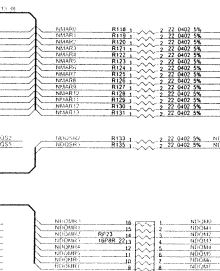
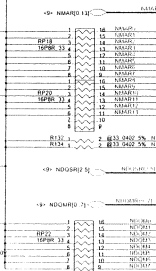
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-6.9: AMCKE#	R77	1	2	33 0402 5%

+1.25VS



TERMINATION FOR
MEMORY
CHANNEL B

SERIES TERMINATION
PLACE CLOSE TO MEMORIES



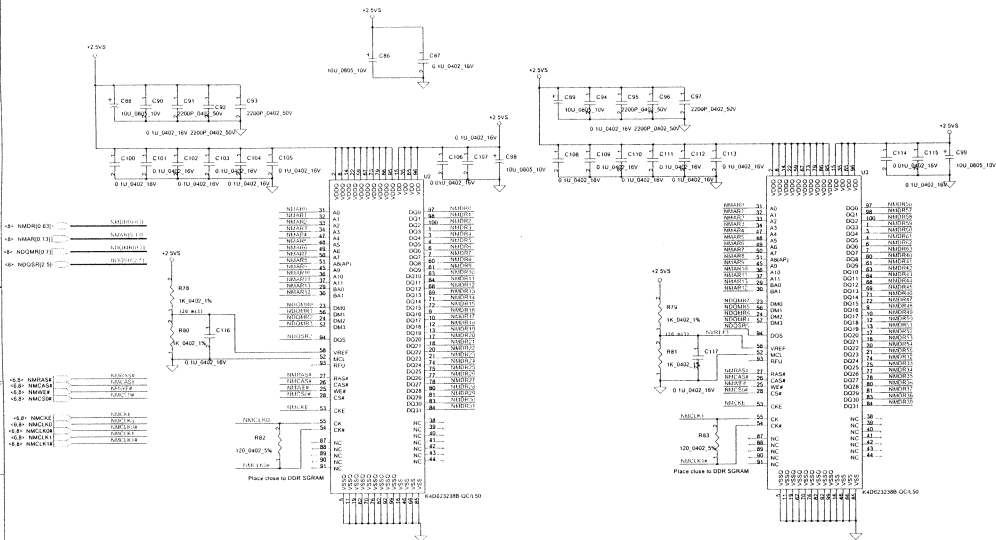
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SCHEMATIC, VGA/B LS-193

DDR SGRAM

NOTE: MA11 CONNECTION REQUIRED
FOR 4Mx32 DDR SGRAM ONLY



NOTE Results of NDQ50 and NDQ54 closed to

16/32MB DDR 2/4MX32 SGRAM

16MB 64 BIT INTERFACE WITH TWO PIECES 2MX32
32MB 64 BIT INTERFACE WITH TWO PIECES 4MX32

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