Myna II

Project code: 91.4C201.001
PCB REVISION: 05216-SB

CLK GEN.
IDT CV125
3

Mobile CPU
Dothan
CLE-1.5G / Dothan2.13G
(CPU on board,no socket)
4, 5

G792
19

HOST BUS 533MHz

DDR II
400/533 MHz
11,12

DDR II
400/533 MHz
11,12

400/533MHz

400/533MHz

Alviso-GM
KI.91501.017
6,7,8,9,10

LVDS
TV
(EZ4 only)
LCD 13

RGB CRT
CRT 14

CH7307C 53 TMDS
DVI-D
(EZ4 only) 35

DMI I/F 100MHz

Int. MIC
Mic In
Line In
Codec
ALC655
ACLINK

Line Out
OP AMP
G1421B

INT.SPKR

RJ11 CONN
MODEM
MDC Card

IO Board

ICH6-M
Ver. : B2, KI.80101.011
15,16,17,18

PCI BUS

TI
PCI 7411
1* Slot Cardbus
1* 1394
CardReader
24,25

PCMCIA I/F
PWR SW
TSP2220A
26

PCMCIA
SLOT
Support
TypeII
26

1394 6pin
Conn 27

MS/MS Pro/
xD/ MMC/SD
5 in 1 26

Mini-PCI
802.11A/B/G
(only smaller) 30

LAN 22, 23
Giga
BCM5788-M

TXFM 23

RJ45 CONN
23

LPC BUS

(co-lay with PCMCIA)
New card
29

PCI-E

PATA

two USB port
on IO Board

USB
3 PORT
21

HDD 20

MINI USB
Blue-tooth
21

NS
SIO
87392
31

KBC
Renesas RE144B
30

BIOS ROM
4M BITS
PM49F004T-33VC
33

LPC
DEBUG
CONN.
33

FIR

Touch
Pad 32

INT.
KB 32

IO Board

PWR SW
TPS2231 29

Easy Port 4 (124 PIN)

AC IN | RJ45-11 | SEARIAL PORT | CRT | PRINTER | PS2 | MIC | LINE IN | LINE OUT | TV OUT | DVI | PCIeX2 | SMBUS

34, 35

SYSTEM DC/DC TPS5130 41,42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5 1D5V_S0 2D5V_S0(LDO)

SYSTEM DC/DC ISL6227 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

TPS51100DGQ 43	
1D8V_S3	VTT_S0(0.9V)

MAXIM CHARGER MAX8725ETI 44	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 16.8V 3.2A UP+5V 5V 100mA

CPU DC/DC ISL6218CV-T 40	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size: Custom | Document Number: Myna II | Rev: SB

Date: Monday, September 26, 2005 | Sheet 1 of 47

Alviso Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott **1 = Dothan** (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

1.CHECK P5[1D5V & 1D5V-AVDD]
2.CHECK P8[PM & GM]

PCI Routing

	IDSEL	IRQ	REQ/GNT
7411	25	B.F.G	0
MiniPCI	21	E	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

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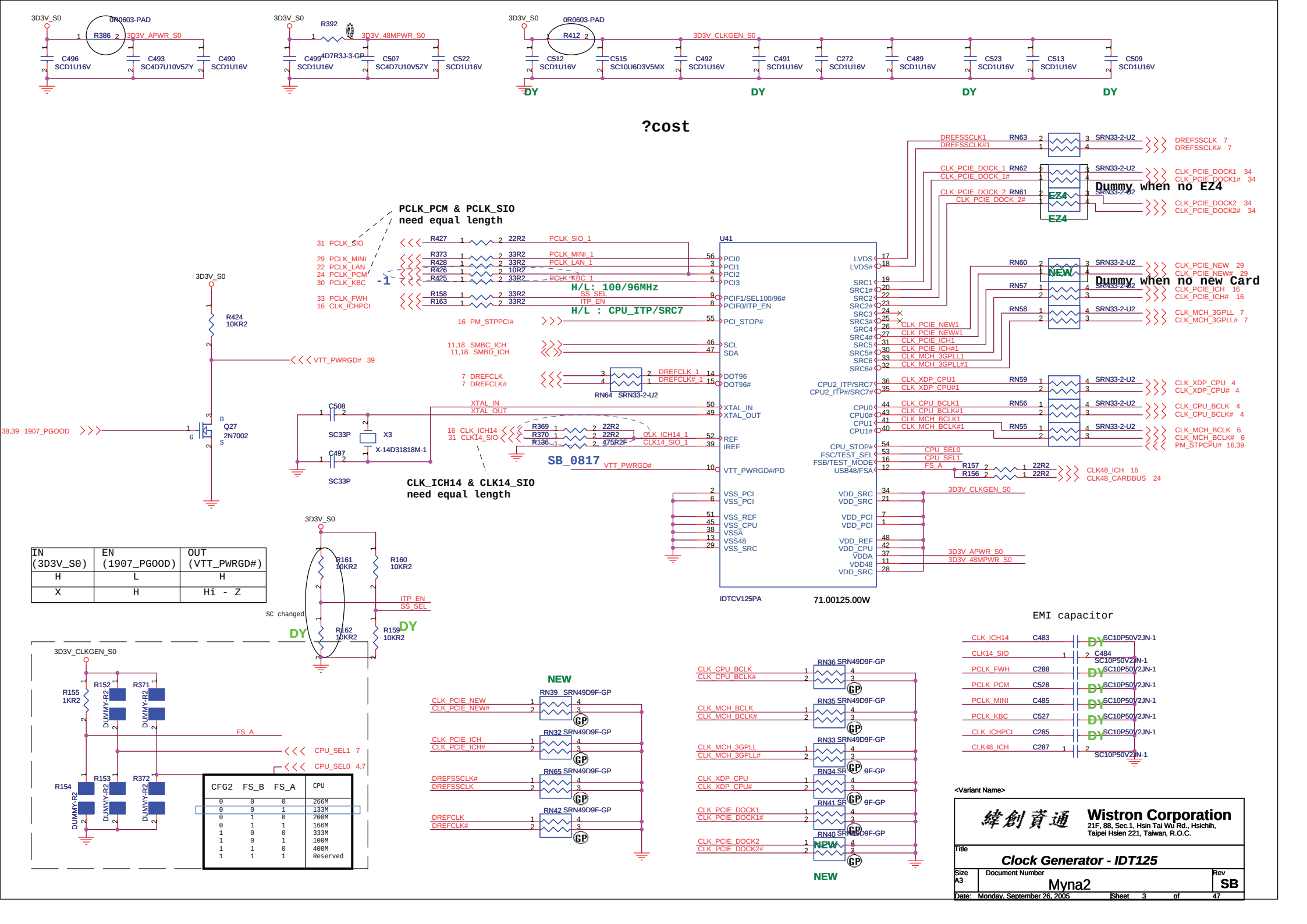
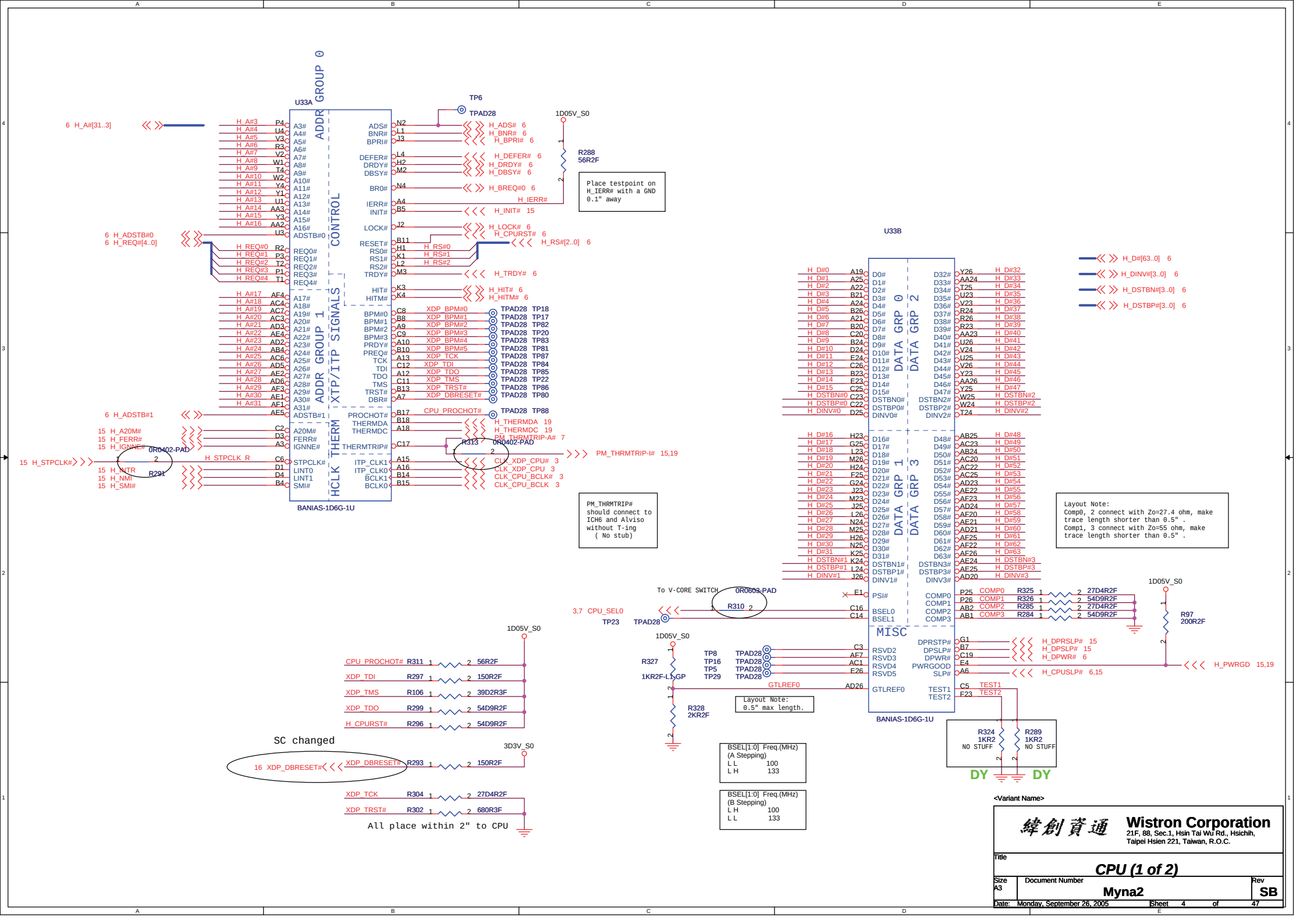
Title: WISTRON
Size: A3 | Document Number: Myna2 | Rev: SB
Date: Monday, September 26, 2005 | Sheet 2 of 47



IN (3D3V_S0)	EN (1907_PGOOD)	OUT (VTT_PWRGD#)
H	L	H
X	H	Hi - Z

CFG2	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved


U33A
BANIAS-1D6G-1U
U33B
BANIAS-1D6G-1U
TP6
TPAD28
1D05V_S0
R288
56R2F
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH6 and Alviso without T-ing (No stub)
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
To V-CORE SWITCH
0R0603-PAD
R310
3,7 CPU_SEL0
TP23
R97
200R2F
R327
1KR2F-L1-GP
R328
2KR2F
Layout Note: 0.5" max length.
BSEL[1:0] Freq.(MHz) (A Stepping) L L 100 L H 133
BSEL[1:0] Freq.(MHz) (B Stepping) L H 100 L L 133
R324
1KR2
NO STUFF
R289
1KR2
NO STUFF
DY
DY
SC changed
All place within 2" to CPU
0R0402-PAD
R291
R313
PM_THRMTRIP-I# 15,19
3D3V_S0
<Variant Name>
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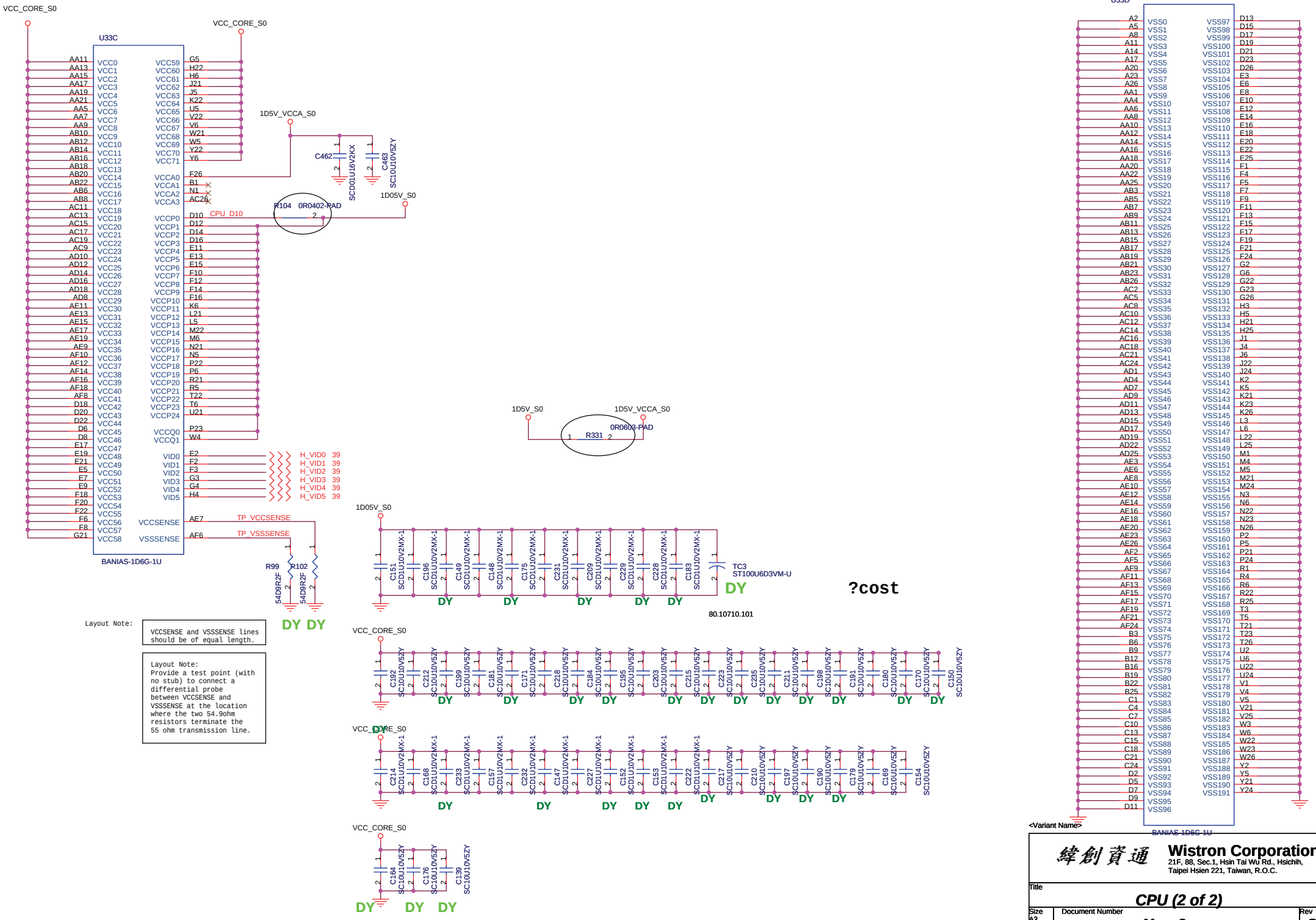
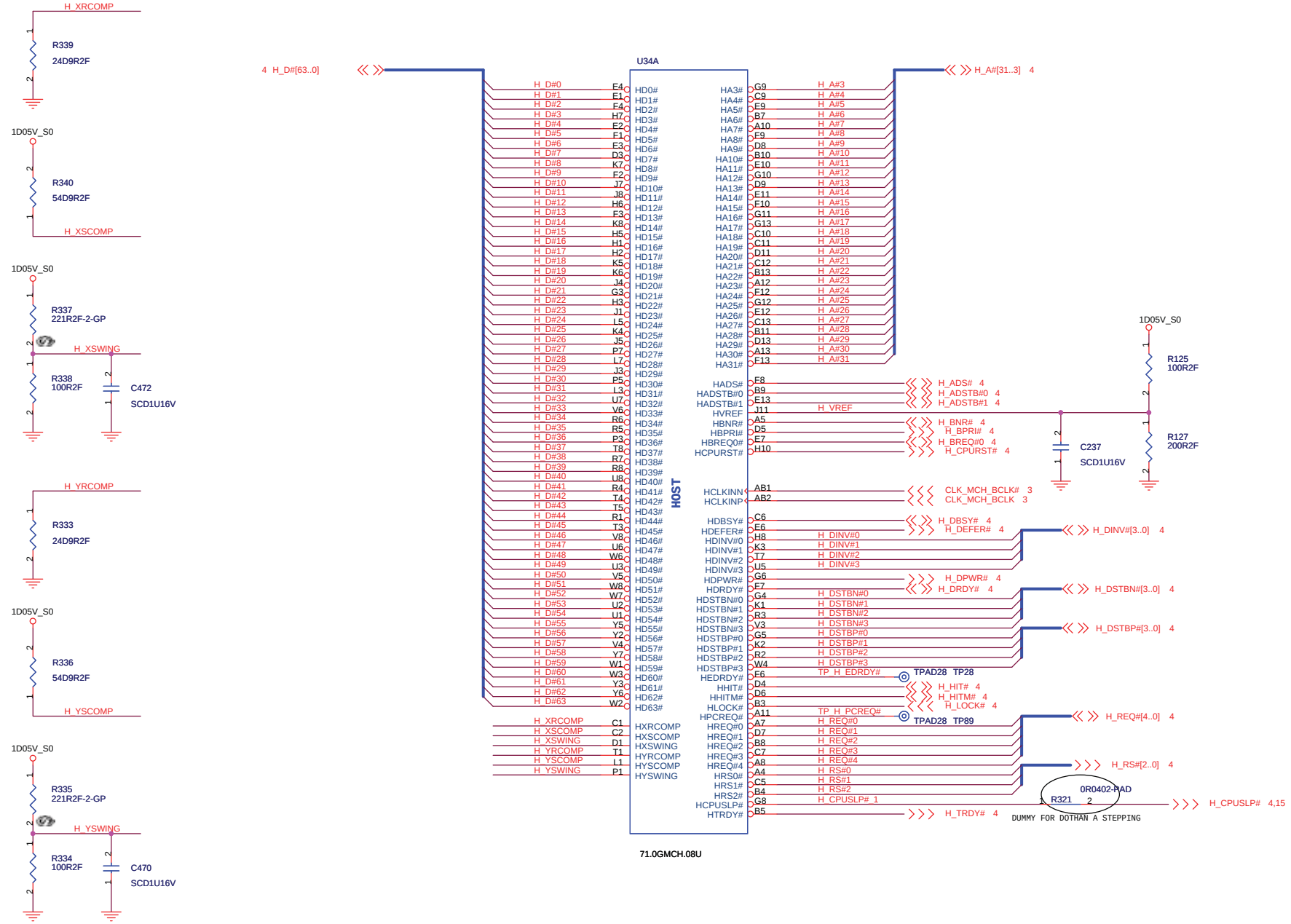
Title
CPU (1 of 2)
Size A3
Document Number
Myna2
Rev SB
Date: Monday, September 26, 2005
Sheet 4 of 47


VCC_CORE_S0
U33C
BANIAS-1D6G-1U
1D5V_VCCA_S0
C462
SCD01U16V2KX
C463
SC10U10V5ZY
1D05V_S0
R104 0R0402-PAD
CPU_D10
H_VID0 39
H_VID1 39
H_VID2 39
H_VID3 39
H_VID4 39
H_VID5 39
TP_VCCSENSE
TP_VSSSENSE
R99 54D9R2F
R102 54D9R2F
DY DY
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
1D5V_S0
1D5V_VCCA_S0
0R0603-PAD
R331
TC3
ST100U6D3VM-U
DY
?cost
80.10710.101
U33D
BANIAS-1D6G-1U
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (2 of 2)
Size A3
Document Number
Myna2
Rev SB
Date: Monday, September 26, 2005
Sheet 5 of 47



Place them near to the chip

<Variant Name>

緯創資通 Wistron Corporation
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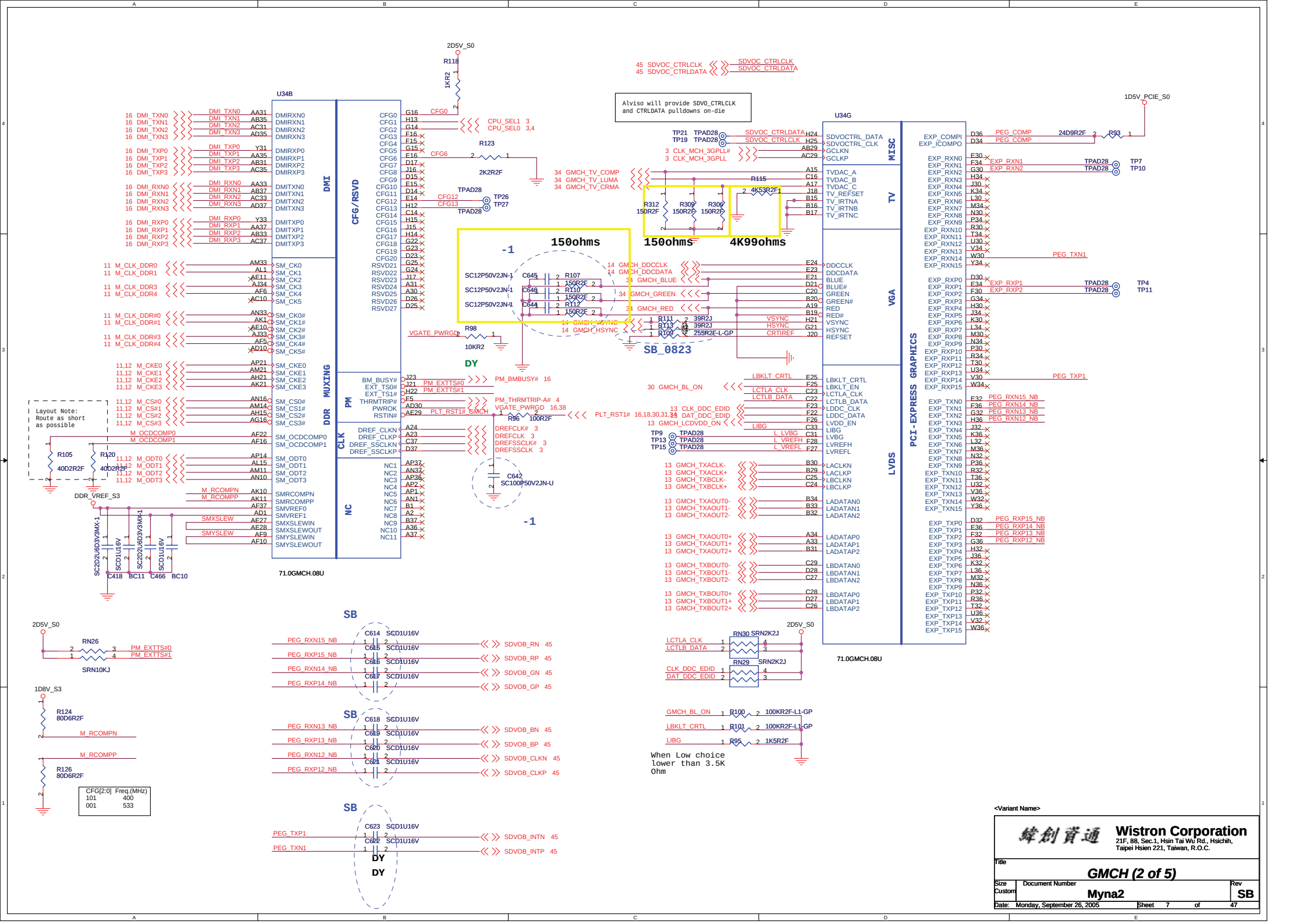
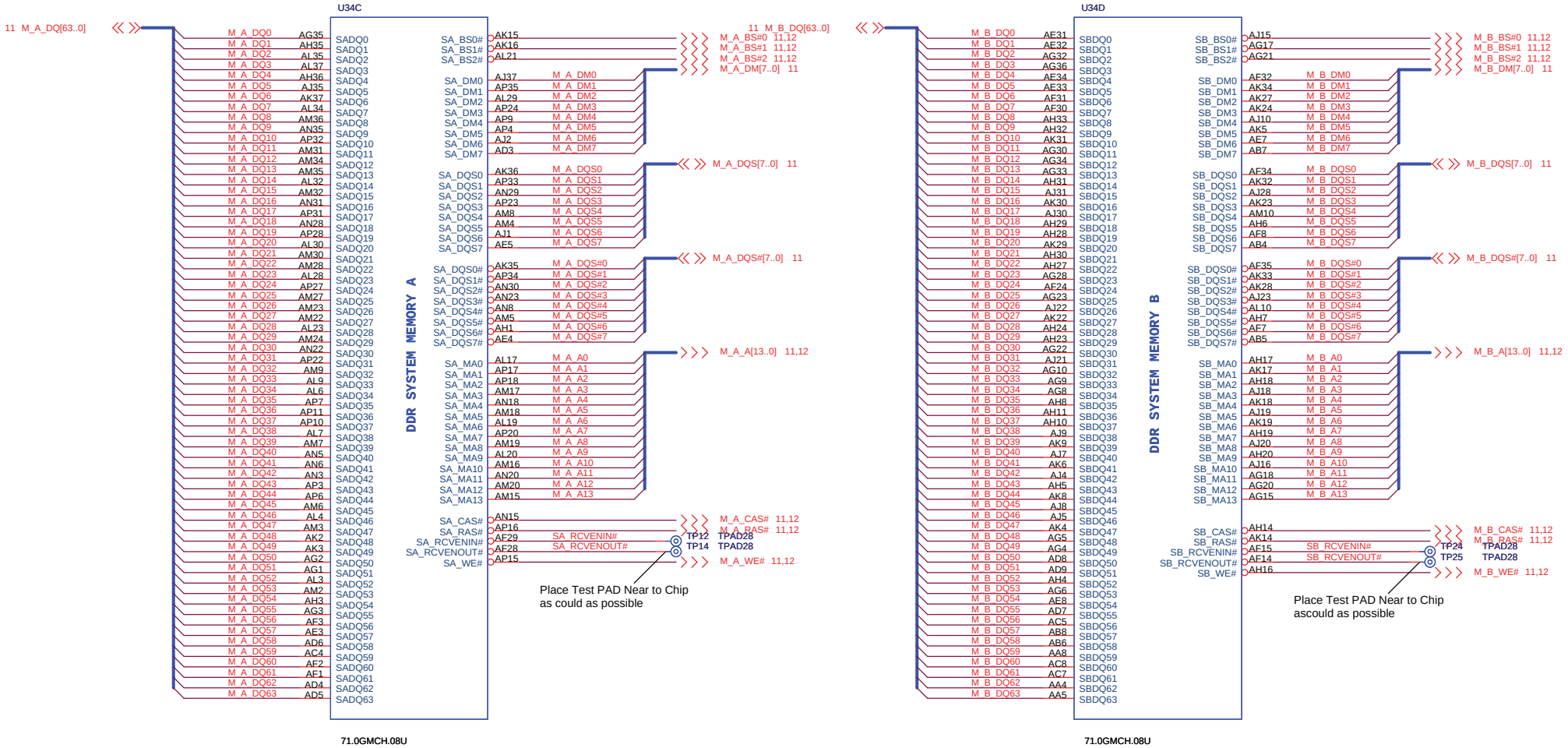
Title: GMCH (1 of 5)

Size	Document Number	Rev
A3	Myna2	SB

Date: Monday, September 26, 2005 Sheet 6 of 47


U34B
DMI
CFG/RSVD
DDR MUXING
PM
CLK
NC
71.0GMCH.08U
U34G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
71.0GMCH.08U
Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die
150ohms
150ohms
4K99ohms
SB_0823
DY
Layout Note: Route as short as possible
When Low choice lower than 3.5K Ohm
SB
DY
CFG[2:0] Freq.(MHz)
101 400
001 533
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
GMCH (2 of 5)
Myna2
SB
Monday, September 26, 2005
7 of 47



<Variant Name>

緯創資通
Wistron Corporation
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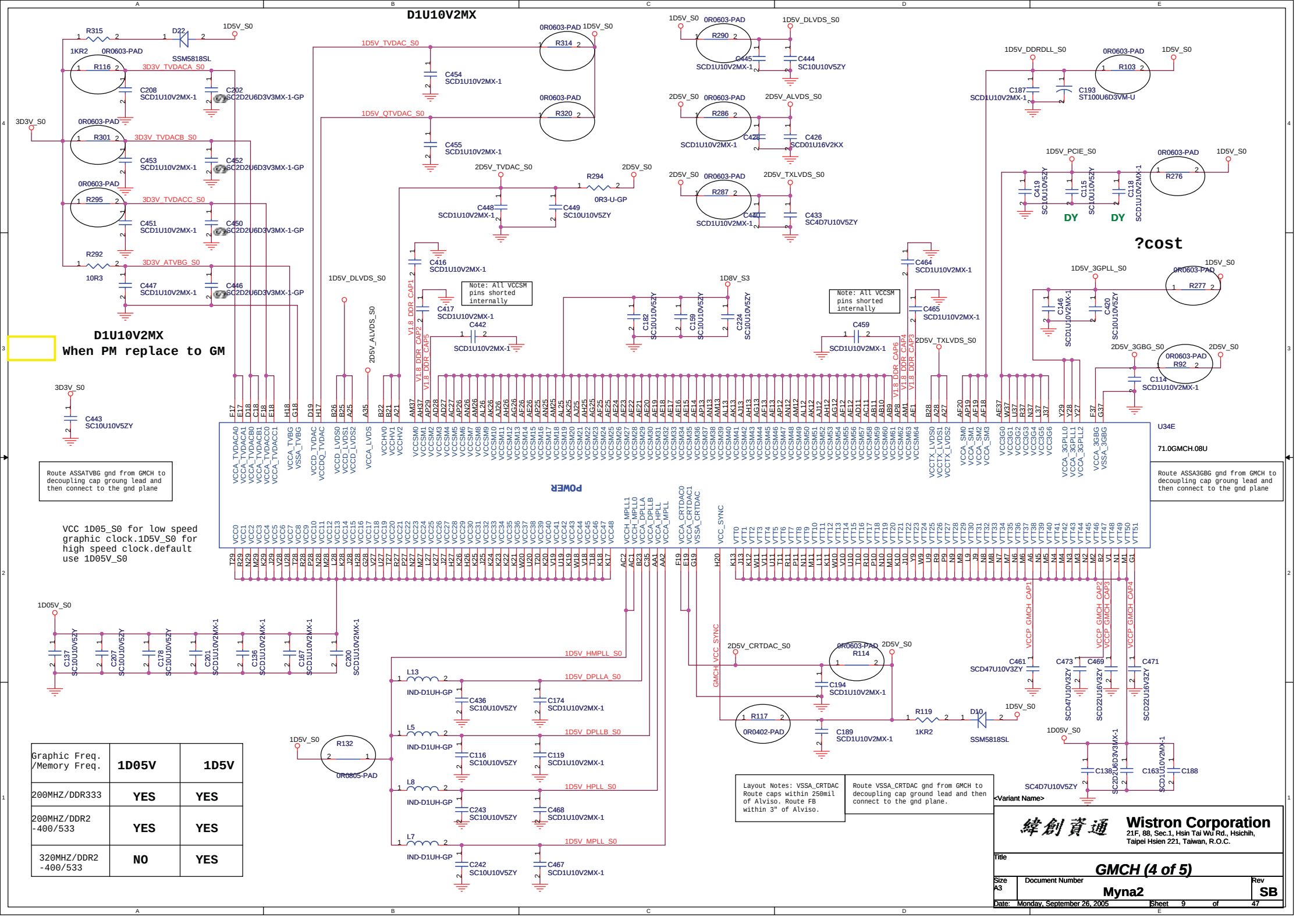
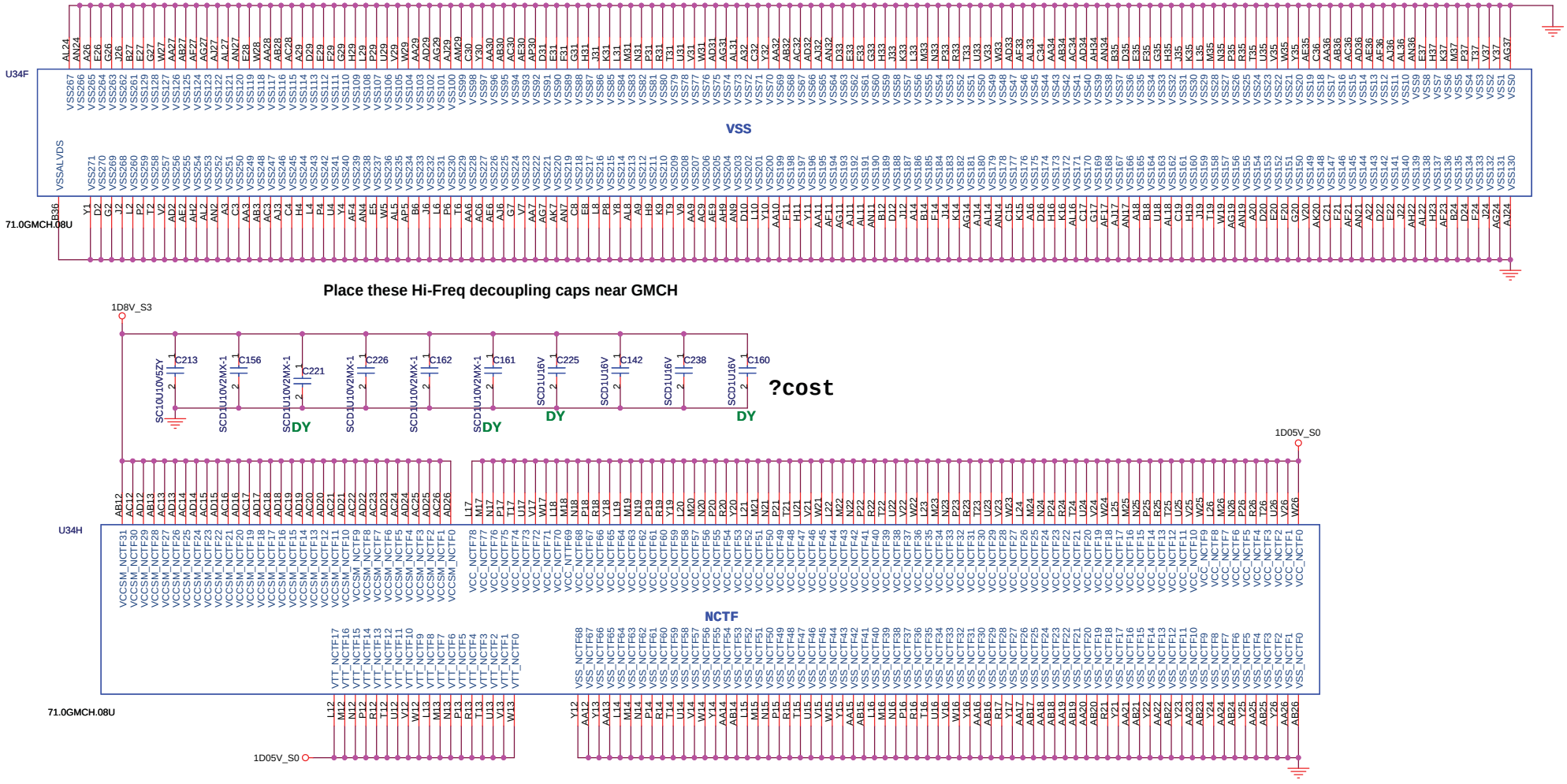
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (3 of 5)

Size: A3 | Document Number: Myna2 | Rev: SB

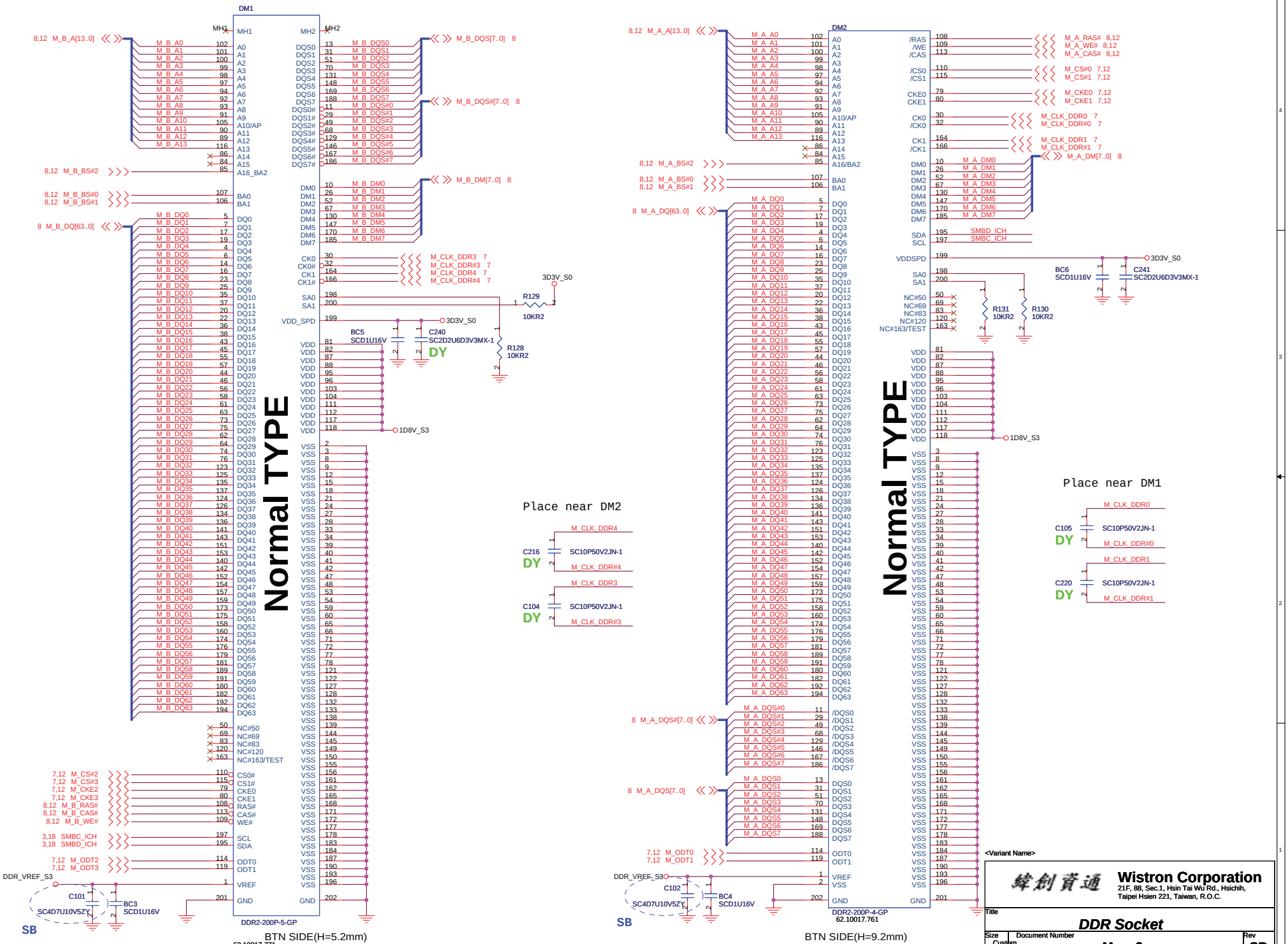
Date: Monday, September 26, 2005 | Sheet 8 of 47


D1U10V2MX
D1U10V2MX
When PM replace to GM
?cost
DY
DY
POWER
U34E
71.0GMCH.08U
Note: All VCCSM pins shorted internally
Note: All VCCSM pins shorted internally
Route ASSATVBG gnd from GMCH to decoupling cap groung lead and then connect to the gnd plane
Route ASSA3GBG gnd from GMCH to decoupling cap groung lead and then connect to the gnd plane
VCC 1D05_S0 for low speed graphic clock.1D5V_S0 for high speed clock.default use 1D05V_S0
Layout Notes: VSSA_CRTDAC Route caps within 250mil of Alviso. Route FB within 3" of Alviso.
Route VSSA_CRTDAC gnd from GMCH to decoupling cap ground lead and then connect to the gnd plane.
Graphic Freq. /Memory Freq. | 1D05V | 1D5V
200MHZ/DDR333 | YES | YES
200MHZ/DDR2 -400/533 | YES | YES
320MHZ/DDR2 -400/533 | NO | YES
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (4 of 5)
Size A3
Document Number
Myna2
Rev SB
Date: Monday, September 26, 2005
Sheet 9 of 47
<Variant Name>



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***GMCH (5 of 5)***
Size: A3	Document Number: **Myna2**
Rev: **SB**	
Date: Monday, September 26, 2005	Sheet 10 of 47



蜂創資通
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: **DDR Socket**

Size	Document Number	Rev
Custom	Myna2	SB

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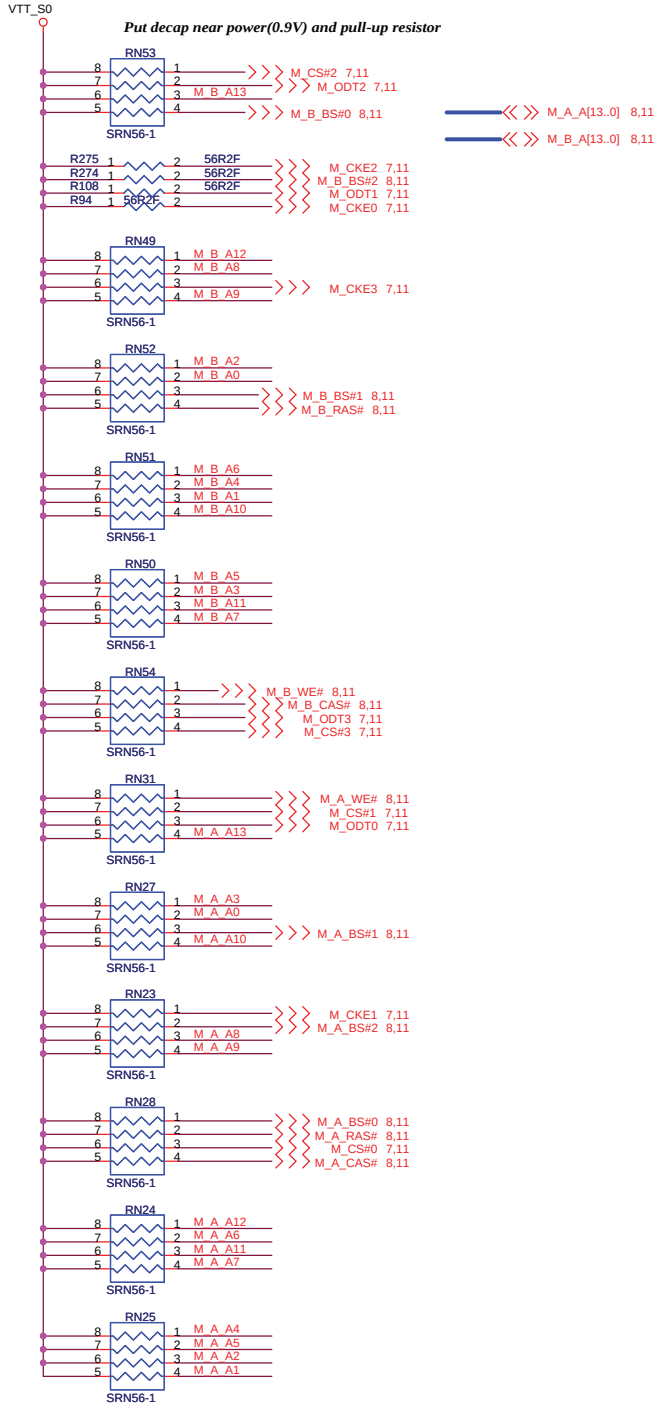
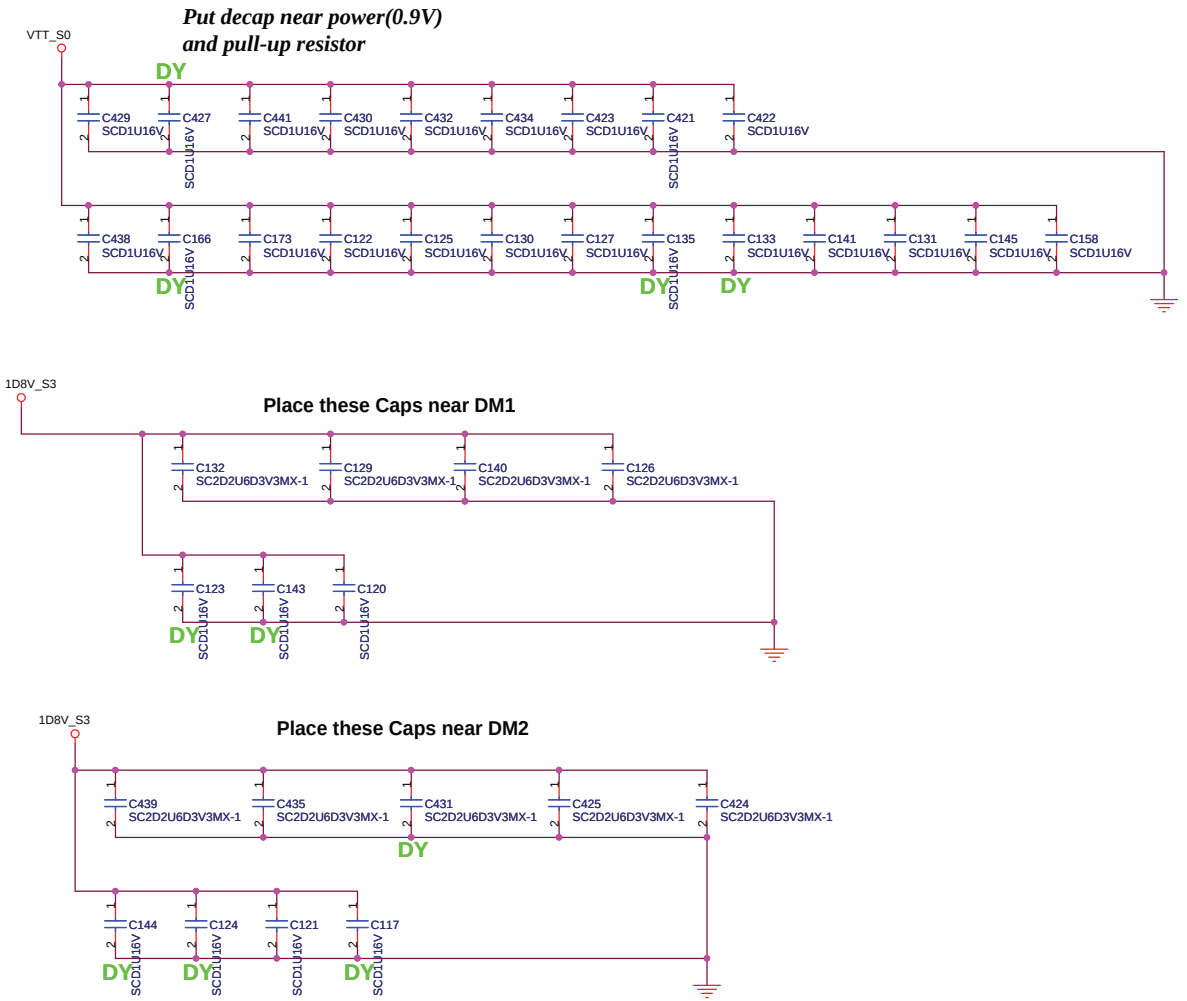
PARALLEL TERMINATION

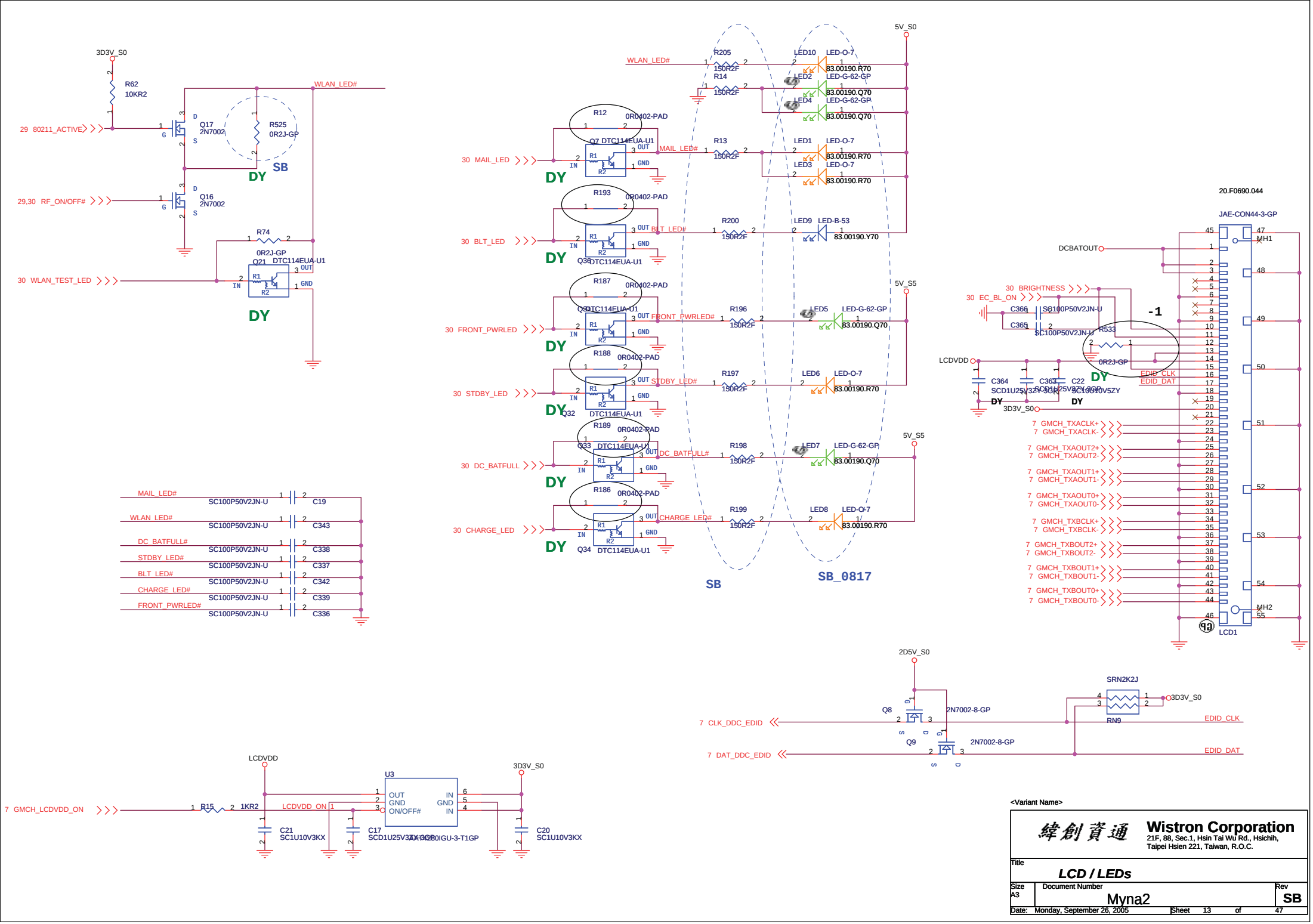


Decoupling Capacitor



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR2 Termination Resistor		
Size: A3	Document Number: Myna2	Rev: SB
Date: Monday, September 26, 2005	Sheet 12 of 47	



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD / LEDs**

Size	Document Number	Rev
A3	Myna2	SB

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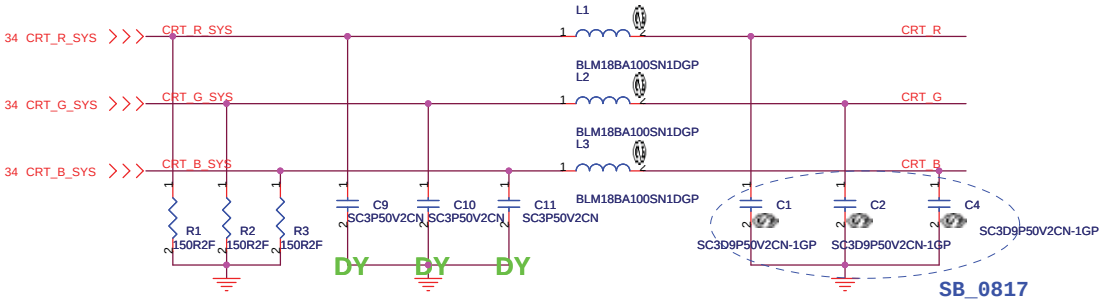
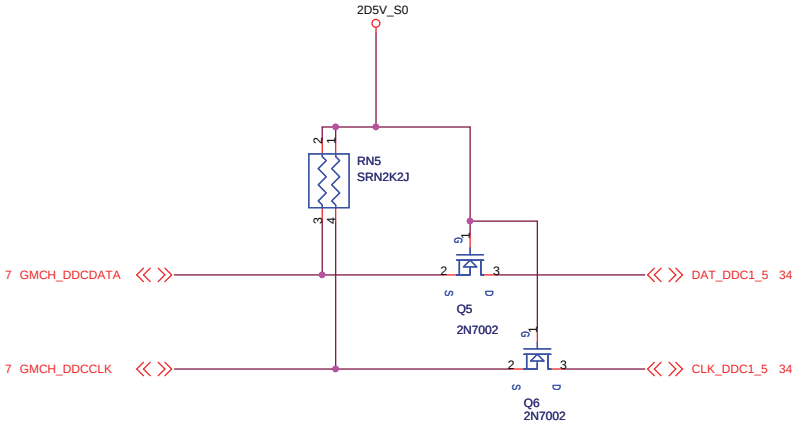
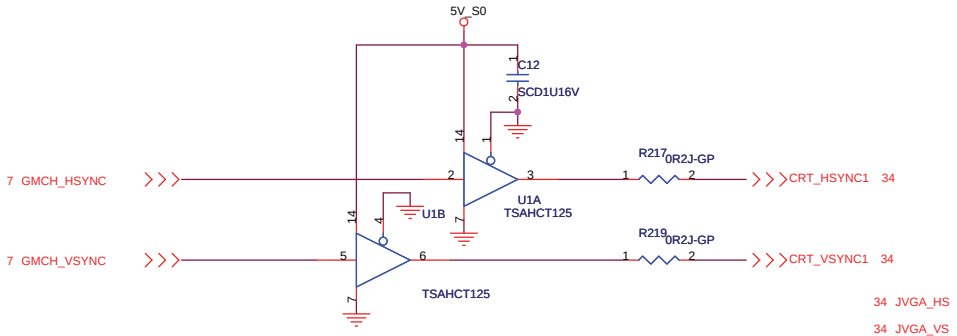
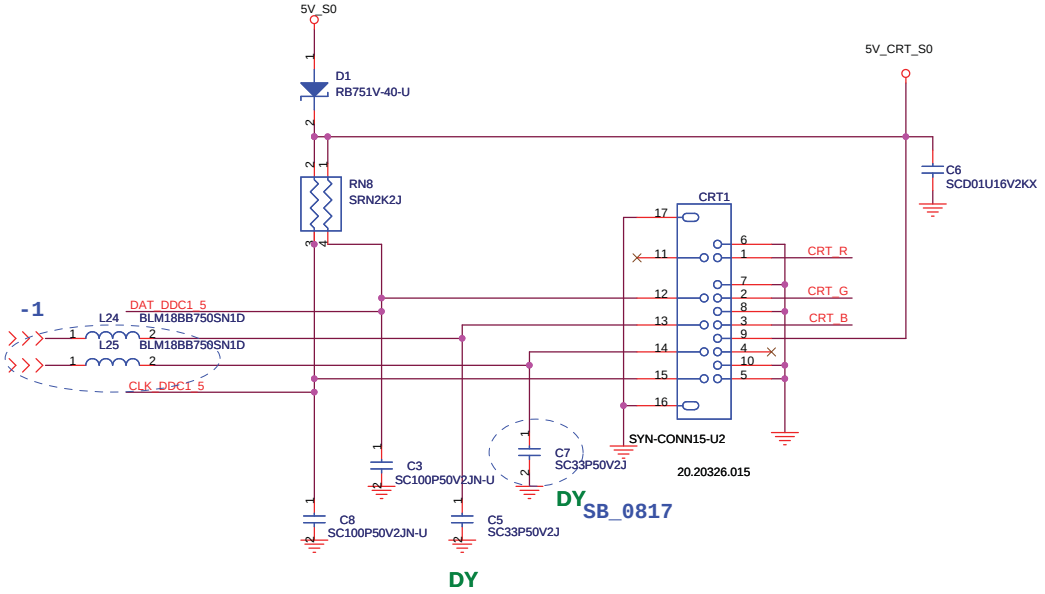








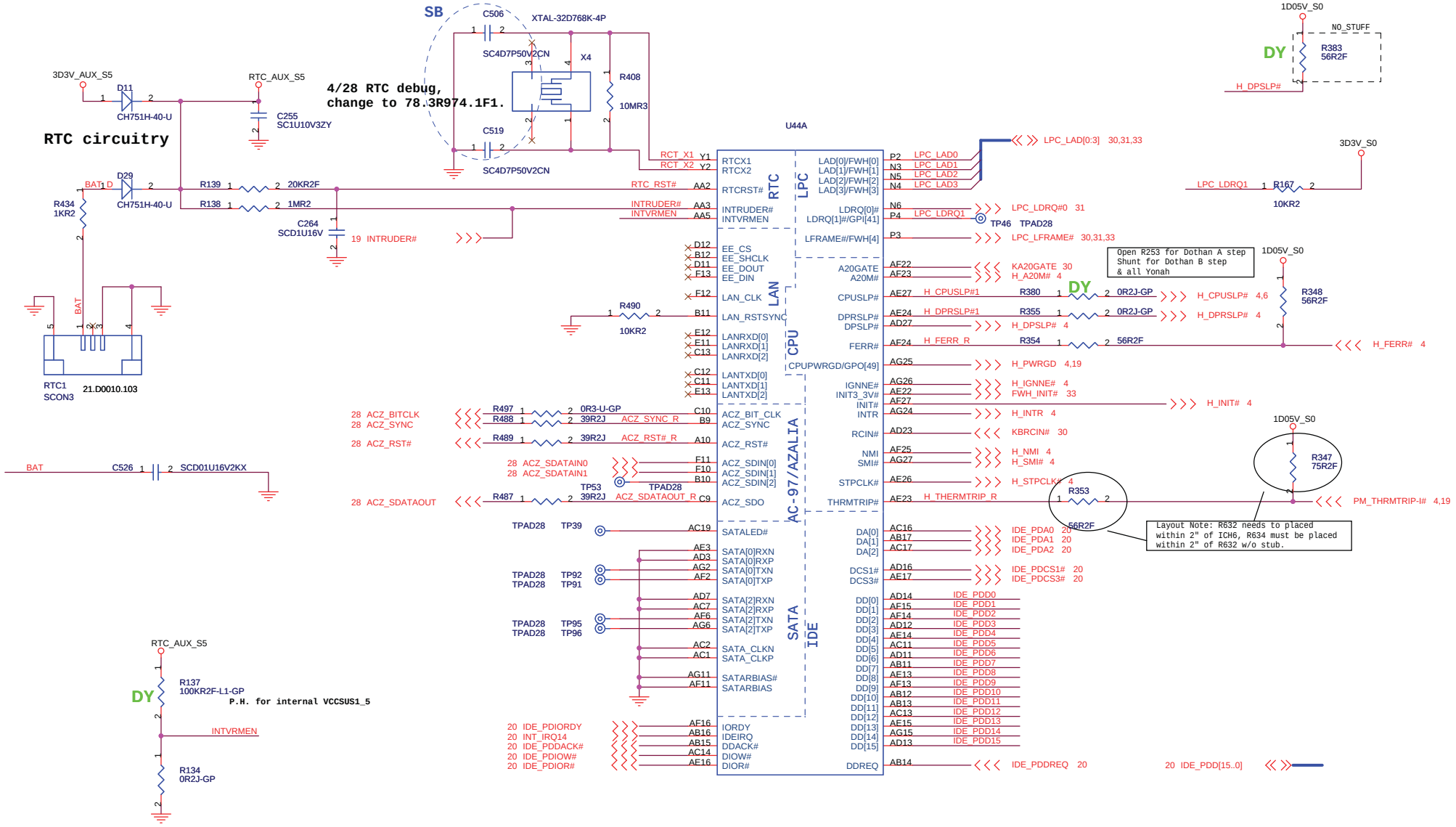
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CRT Connector***

Size	Document Number	Rev
A3	Myna2	SB

Date: Monday, September 26, 2005 Sheet 14 of 47


RTC circuitry
4/28 RTC debug,
change to 78.3R974.1F1.
SB
U44A
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
XTAL-32D768K-4P
SC4D7P50V2CN
CH751H-40-U
SC1U10V3ZY
SCD1U16V
10MR3
20KR2F
1MR2
1KR2
10KR2
0R3-U-GP
39R2J
0R2J-GP
56R2F
75R2F
SCD01U16V2KX
100KR2F-L1-GP
P.H. for internal VCCSUS1_5
RTC1
SCON3
21.D0010.103
TP46 TPAD28
TP53 TPAD28
TP39
TP92
TP91
TP95
TP96
Open R253 for Dothan A step
Shunt for Dothan B step
& all Yonah
Layout Note: R632 needs to placed
within 2" of ICH6, R634 must be placed
within 2" of R632 w/o stub.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH6-M (1 of 4)
Myna2
SB
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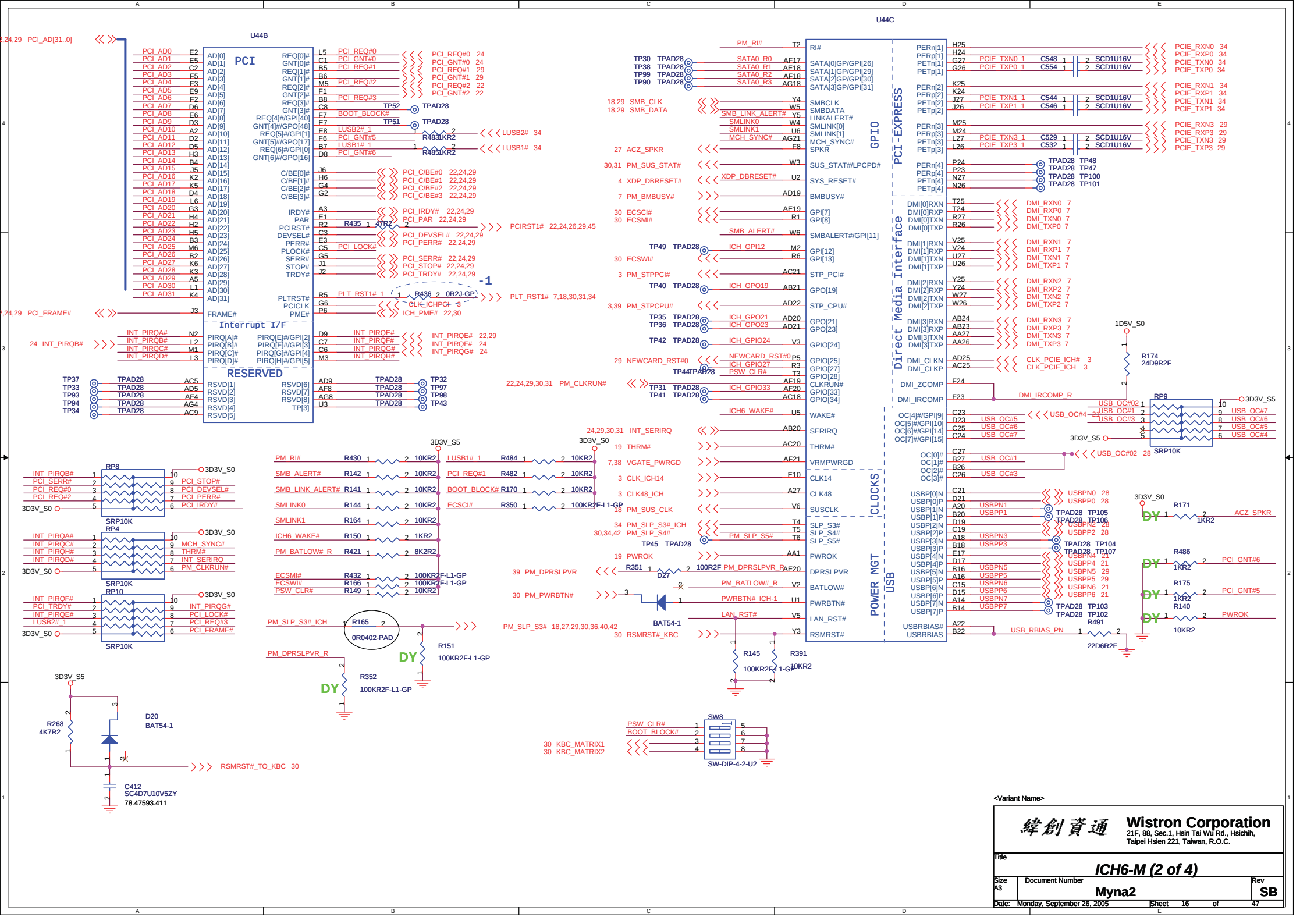
U44B
PCI
Interrupt I/F
RESERVED
U44C
GPIO
PCI-EXPRESS
Direct Media Interface
CLOCKS
USB
POWER MGT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH6-M (2 of 4)
Myna2
SB
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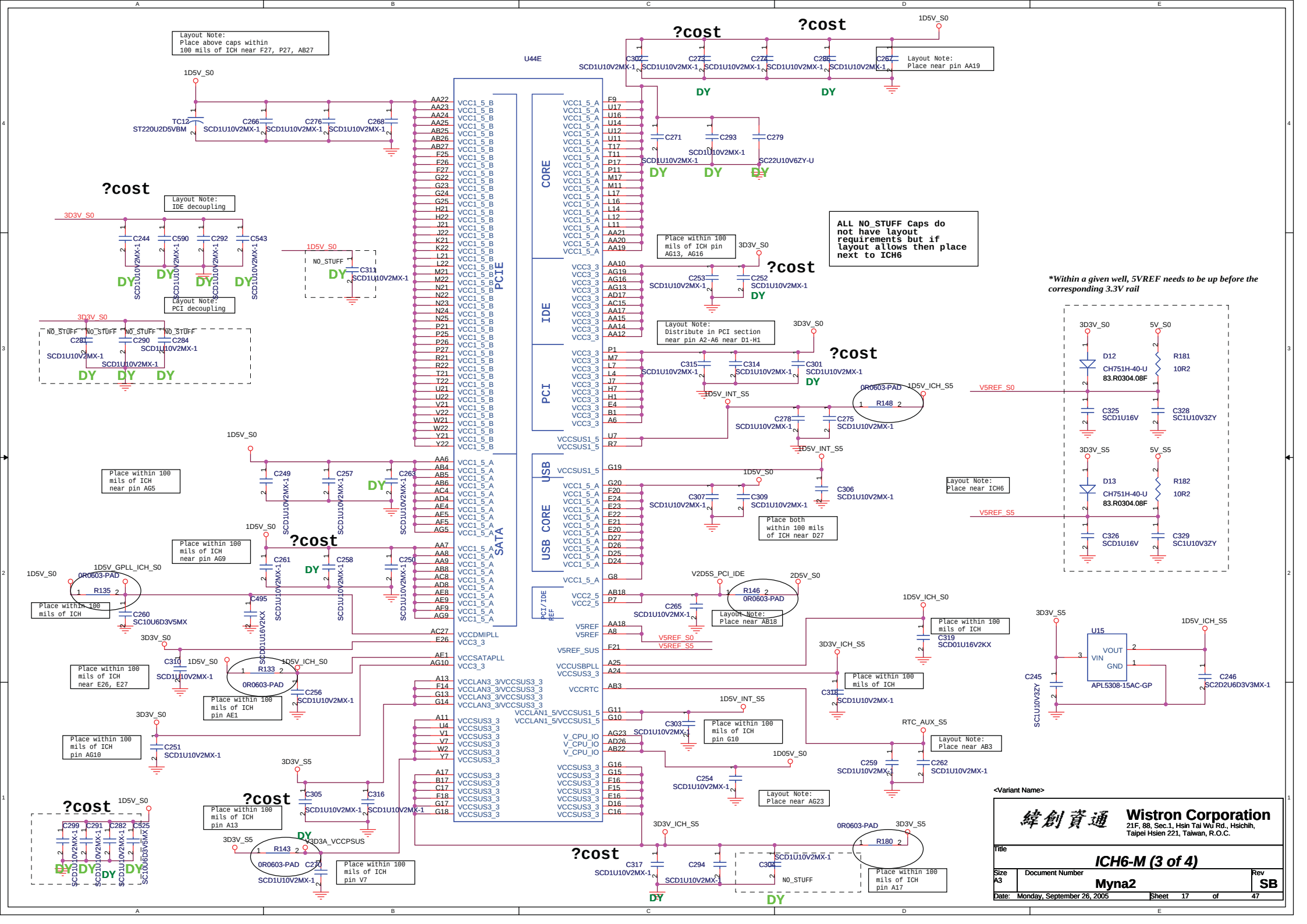
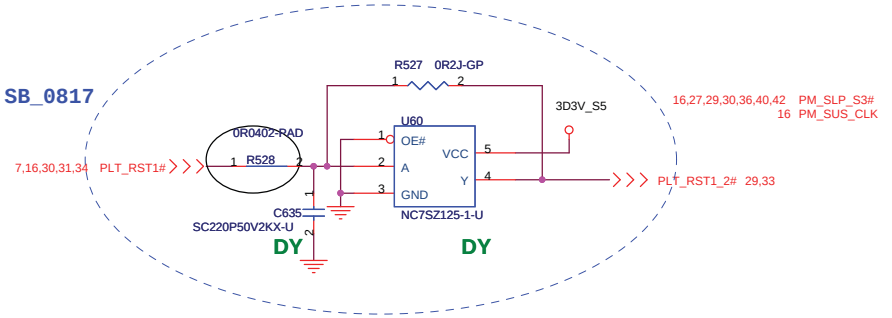
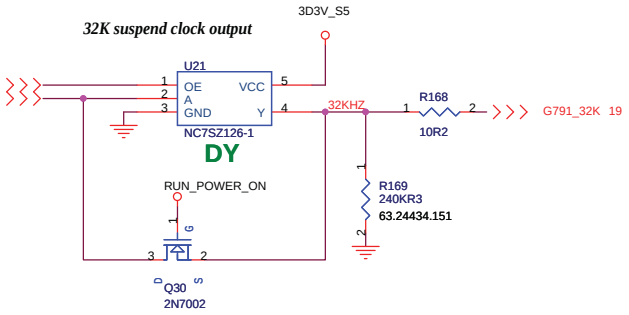
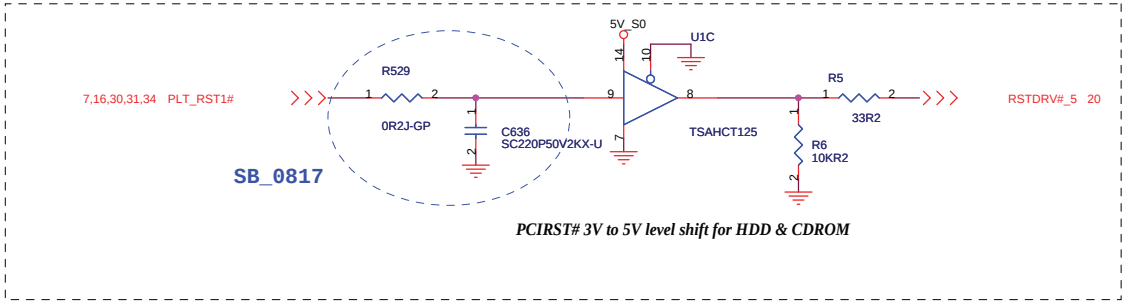
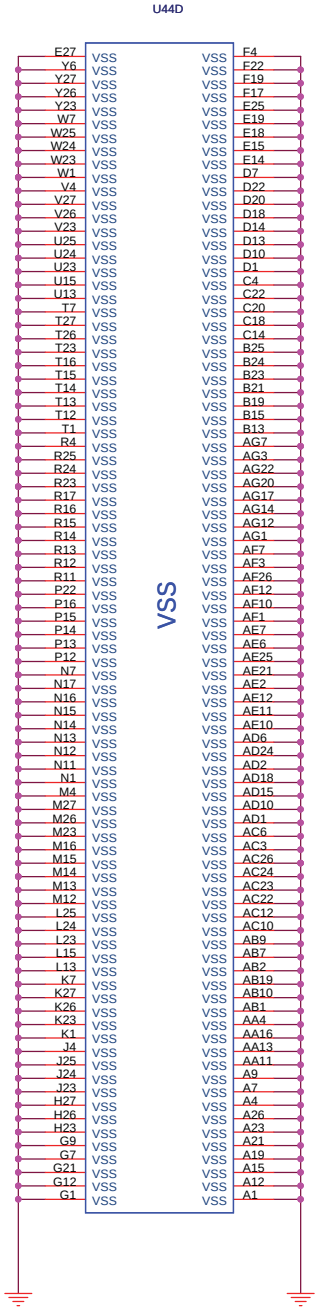
Sheet 16 of 47


U44E
CORE
IDE
PCI
USB
USB CORE
SATA
PCIE
PCI/IDE REF
Layout Note: Place above caps within 100 mils of ICH near F27, P27, AB27
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Layout Note: Place near pin AA19
Place within 100 mils of ICH pin AG13, AG16
Layout Note: Distribute in PCI section near pin A2-A6 near D1-H1
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin AG10
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin V7
Place within 100 mils of ICH pin G10
Place within 100 mils of ICH pin A17
Place both within 100 mils of ICH near D27
Layout Note: Place near AB18
Layout Note: Place near AB3
Layout Note: Place near AG23
Layout Note: Place near ICH6
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
?cost
DY
NO_STUFF
1D5V_S0
3D3V_S0
5V_S0
1D5V_ICH_S5
3D3V_ICH_S5
3D3V_S5
5V_S5
1D5V_ICH_S0
1D5V_INT_S5
1D5V_GPLL_ICH_S0
V2D5S_PCI_IDE
2D5V_S0
1D05V_S0
RTC_AUX_S5
V3D3A_VCCPSUS
V5REF_S0
V5REF_S5
0R0603-PAD
SCD1U10V2MX-1
SC22U10V6ZY-U
SC10U6D3V5MX
SCD01U16V2KX
SCD1U16V
SC1U10V3ZY
SC2D2U6D3V3MX-1
APL5308-15AC-GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (3 of 4)
Size A3
Document Number
Myna2
Rev SB
Date: Monday, September 26, 2005
Sheet 17 of 47

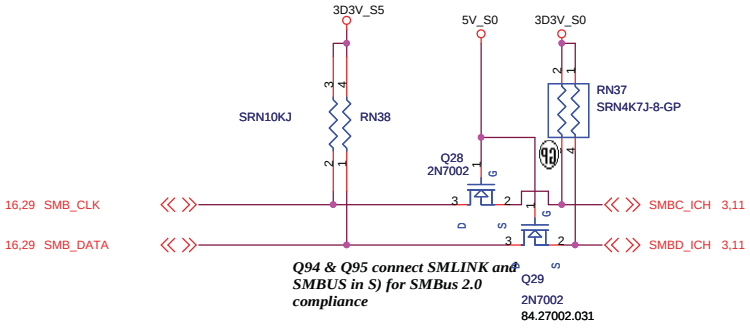








SMBUS



Q94 & Q95 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

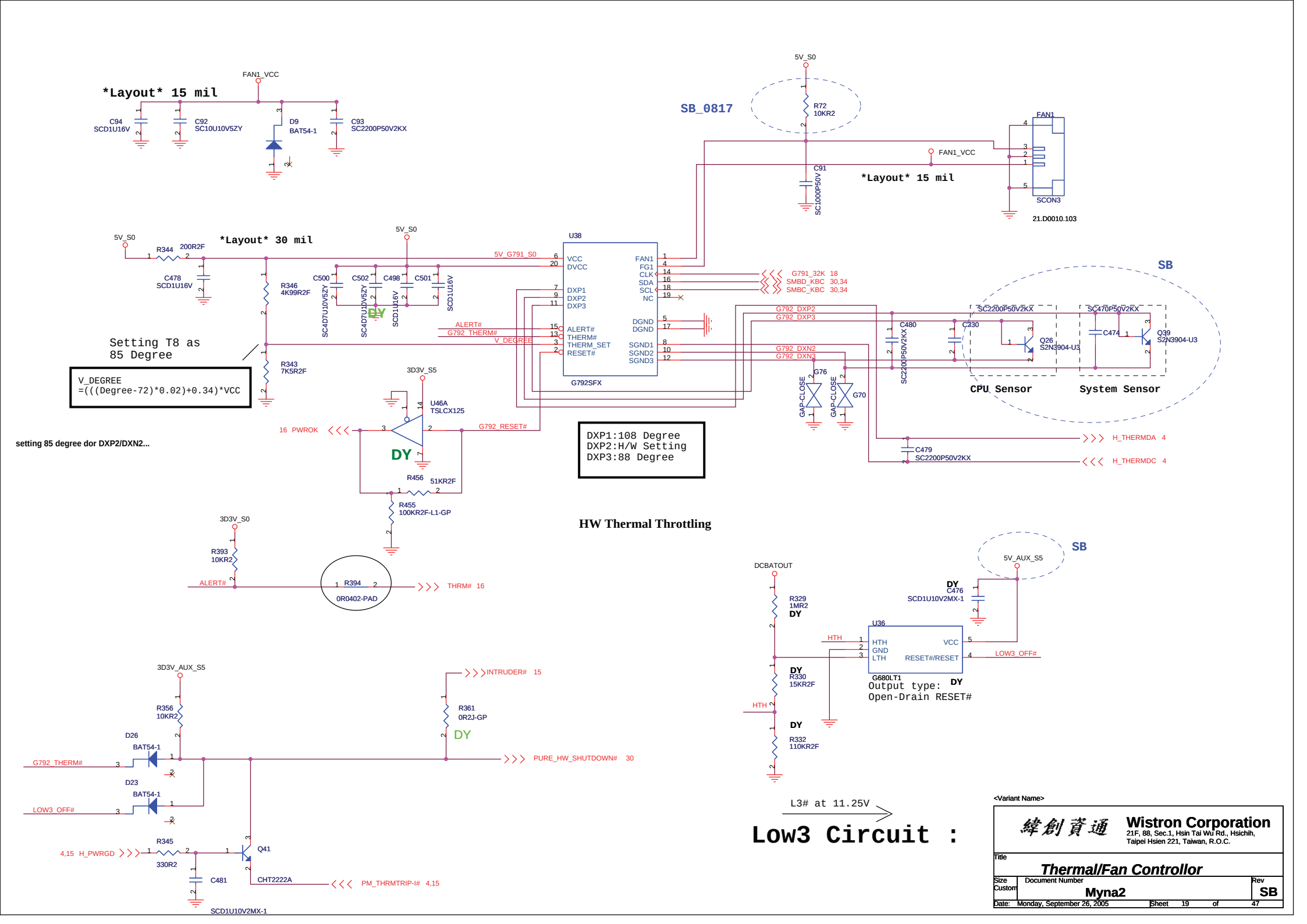
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

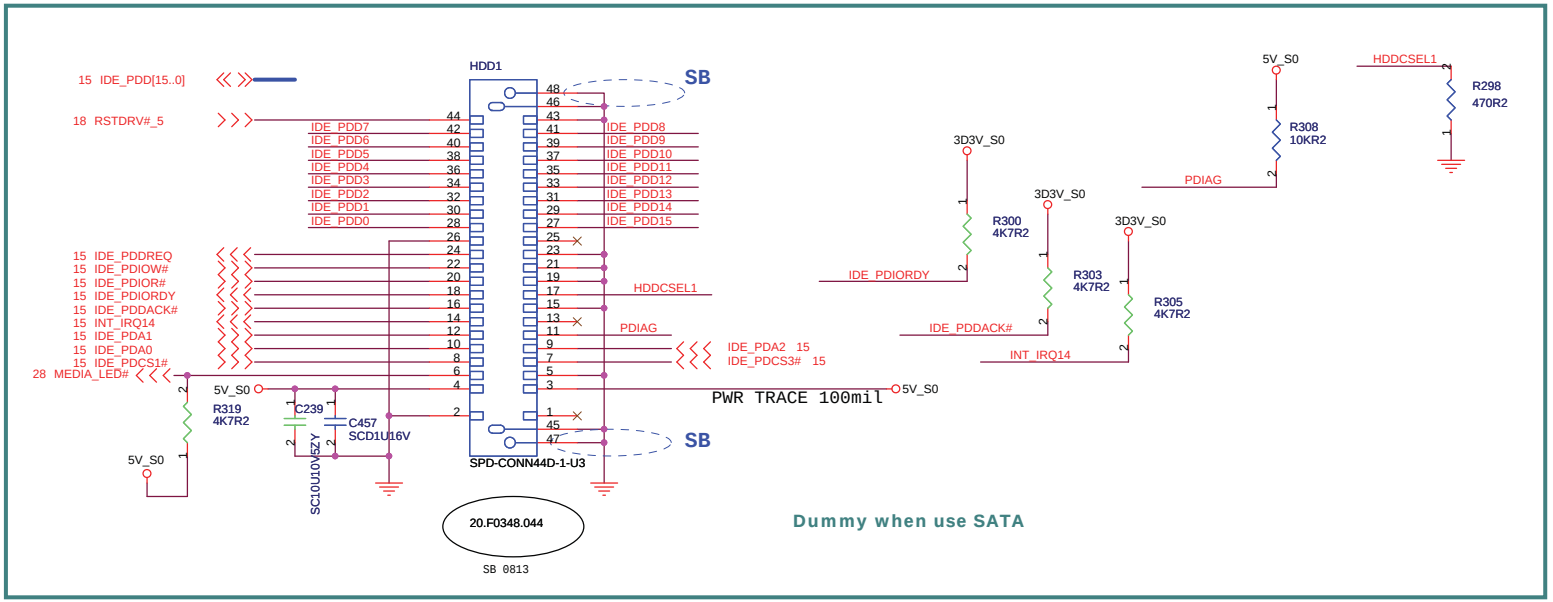
Title: ICH6-M (4 of 4)

Size: A3 | Document Number: Myna2 | Rev: SB

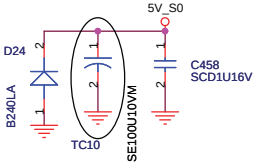
Date: Monday, September 26, 2005 | Sheet 18 of 47


Layout 15 mil
FAN1_VCC
C94 SCD1U16V
C92 SC10U10V5ZY
D9 BAT54-1
C93 SC2200P50V2KX
SB_0817
5V_S0
R72 10KR2
C91 SC1000P50V
FAN1_VCC
Layout 15 mil
FAN1
SCON3
21.D0010.103
Layout 30 mil
5V_S0
R344 200R2F
C478 SCD1U16V
R346 4K99R2F
R343 7K5R2F
C500
C502
C498
C501
SC4D7U10V5ZY
SCD1U16V
DY
5V_G791_S0
ALERT#
G792_THERM#
V_DEGREE
U38
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC
DGND
DGND
SGND1
SGND2
SGND3
G792SFX
G791_32K 18
SMBD_KBC 30,34
SMBC_KBC 30,34
G792_DXP2
G792_DXP3
G792_DXN2
G792_DXN3
SB
SC2200P50V2KX
SC470P50V2KX
C480
C230
C474
Q26 S2N3904-U3
Q39 S2N3904-U3
CPU Sensor
System Sensor
G76
G70
GAP-CLOSE
C479 SC2200P50V2KX
H_THERMDA 4
H_THERMDC 4
Setting T8 as 85 Degree
V_DEGREE =(((Degree-72)*0.02)+0.34)*VCC
setting 85 degree dor DXP2/DXN2...
3D3V_S5
U46A TSLCX125
16 PWROK
G792_RESET#
R456 51KR2F
R455 100KR2F-L1-GP
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
HW Thermal Throttling
3D3V_S0
R393 10KR2
ALERT#
R394 0R0402-PAD
THRM# 16
DCBATOUT
R329 1MR2 DY
R330 15KR2F DY
R332 110KR2F DY
HTH
U36
HTH
GND
LTH
VCC
RESET#/RESET
LOW3_OFF#
G680LT1
Output type: Open-Drain RESET#
C476 SCD1U10V2MX-1 DY
5V_AUX_S5
SB
3D3V_AUX_S5
R356 10KR2
D26 BAT54-1
D23 BAT54-1
G792_THERM#
LOW3_OFF#
R361 0R2J-GP DY
INTRUDER# 15
PURE_HW_SHUTDOWN# 30
R345 330R2
4,15 H_PWRGD
Q41 CHT2222A
C481 SCD1U10V2MX-1
PM_THRMTRIP-I# 4,15
L3# at 11.25V
Low3 Circuit :
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size Custom
Document Number
Myna2
Rev SB
Date: Monday, September 26, 2005
Sheet 19 of 47

HDD



For HDD & SATA both



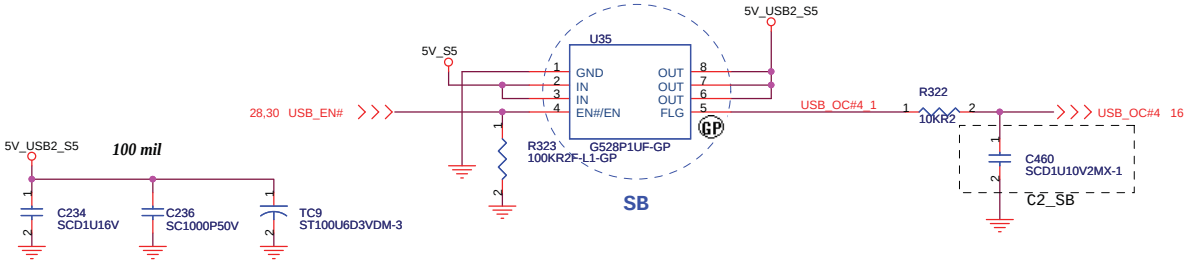
79.10711.4C1

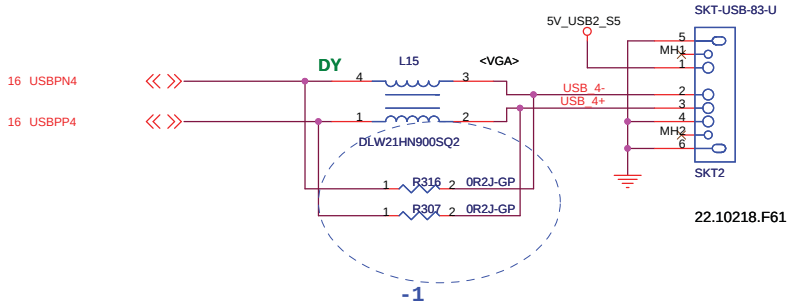
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

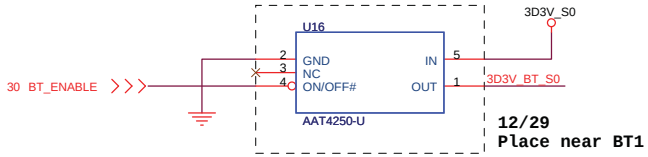
Title: **PATA / SATA-HDD**		
Size: A3	Document Number: **Myna2**	Rev: SB
Date: Monday, September 26, 2005	Sheet 20 of 47	

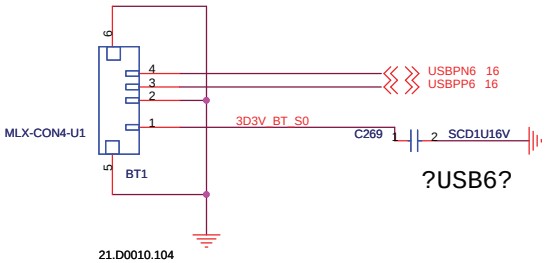
USB PORT





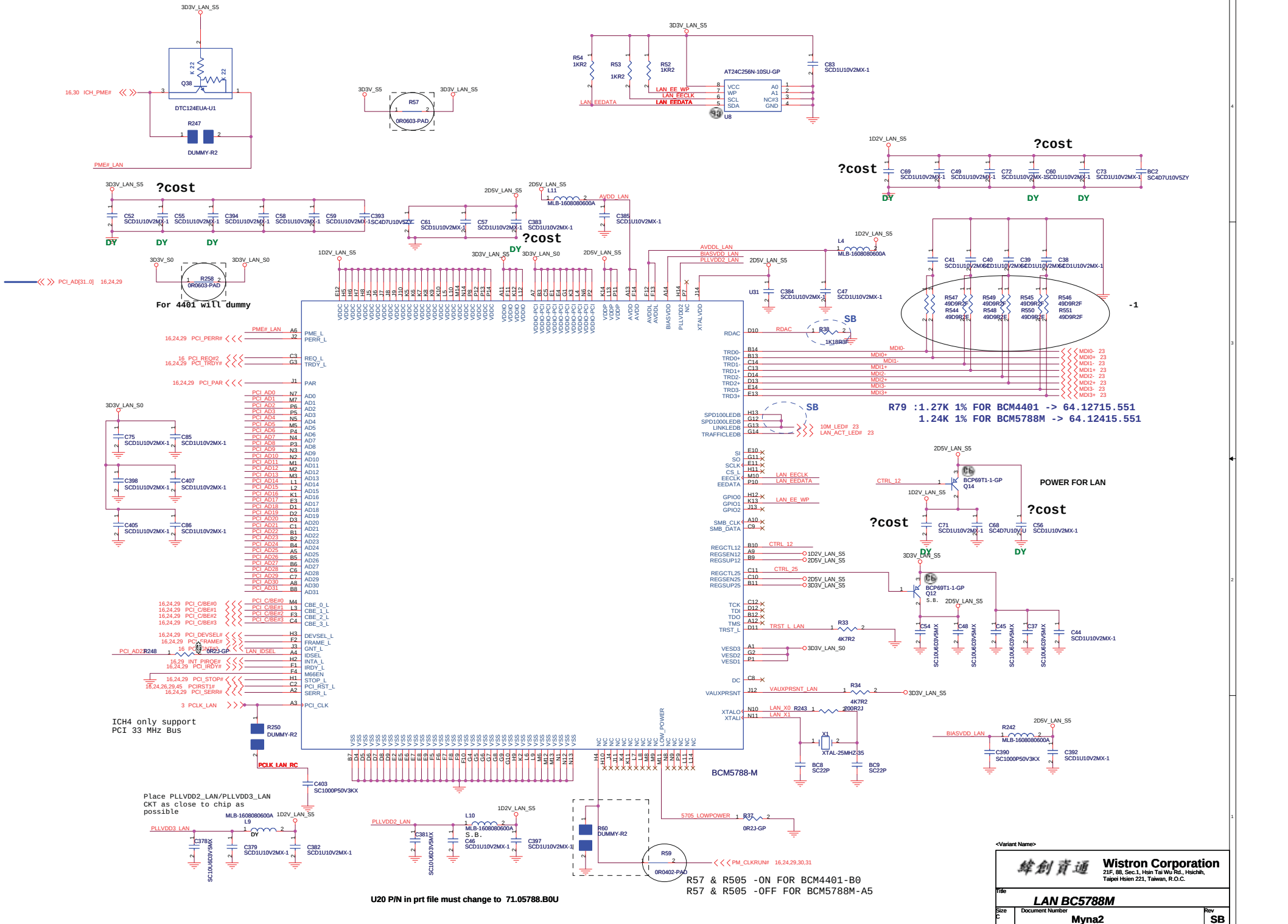
BLUETOOTH MODULE CONNECTOR





<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB & MDC & BTOOTH		
Size: A3	Document Number: Myna2	Rev: SB
Date: Monday, September 26, 2005	Sheet 21 of 47	


3D3V_LAN_S5
DTC124EUA-U1
Q38
R247
DUMMY-R2
16,30 ICH_PME#
PME# LAN
R57
0R0603-PAD
AT24C256N-10SU-GP
U8
LAN_EE_WP
LAN_EECLK
LAN_EEDATA
?cost
DY
2D5V_LAN_S5
1D2V_LAN_S5
3D3V_LAN_S0
MLB-1608080600A
L4
L11
L10
L9
AVDDL_LAN
BIASVDD_LAN
PLLVDD2_LAN
PLLVDD3_LAN
PCI_AD[31..0] 16,24,29
For 4401 will dummy
R258
0R0603-PAD
BCM5788-M
SB
1K18R3F
R38
RDAC
MDI0-
MDI0+
MDI1-
MDI1+
MDI2-
MDI2+
MDI3-
MDI3+
R79 :1.27K 1% FOR BCM4401 -> 64.12715.551
1.24K 1% FOR BCM5788M -> 64.12415.551
POWER FOR LAN
BCP69T1-1-GP
Q14
Q12
CTRL_12
CTRL_25
TRST_L_LAN
VAUXPRSNT_LAN
LAN_X0
LAN_X1
XTAL-25MHZ-35
ICH4 only support
PCI 33 MHz Bus
PCLK_LAN_RC
Place PLLVDD2_LAN/PLLVDD3_LAN
CKT as close to chip as
possible
5705_LOWPOWER
PM_CLKRUN# 16,24,29,30,31
R57 & R505 -ON FOR BCM4401-B0
R57 & R505 -OFF FOR BCM5788M-A5
U20 P/N in prt file must change to 71.05788.B0U
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN BC5788M
Size C
Document Number Myna2
Rev SB
Date: Monday, September 26, 2005
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RJ45 Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

Green LED: Speed 100: ON / Speed 10:OFF
Yellow LED: Link: ON, TX/RX: Flash(10Hz)

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

Function	SEL
An to nB1(MB)	L
An to nB2(DUCK)	H

PI3L500ZFEX-GP

Giga Lan Transformer

XFORM-209-GP

EMI

22.10123.051

Link: Green - 10Mbps/802.11b
Orange - 100Mbps/802.11a
Yellow - 1Gbps
Activity: Yellow

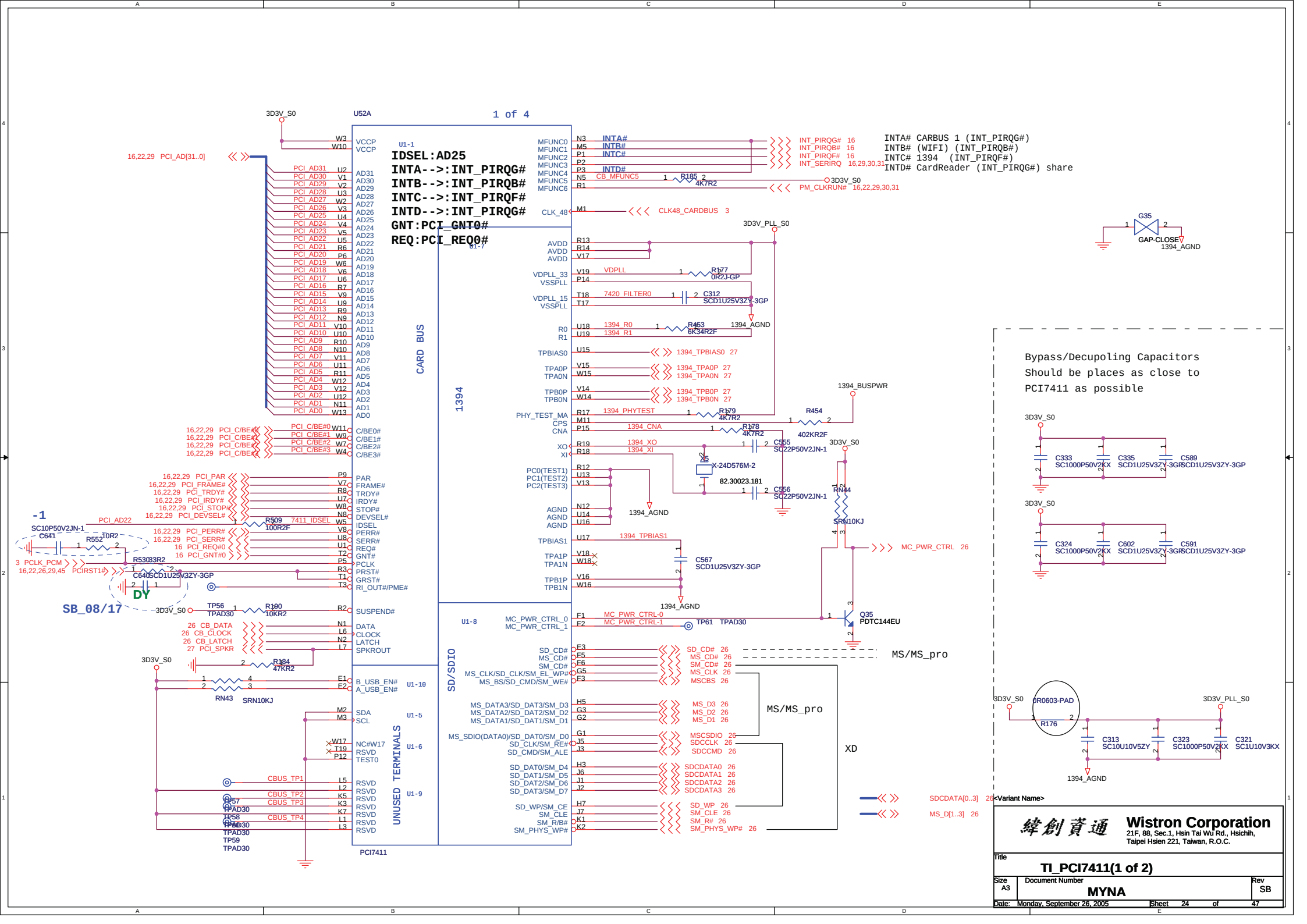
<Variant Name>

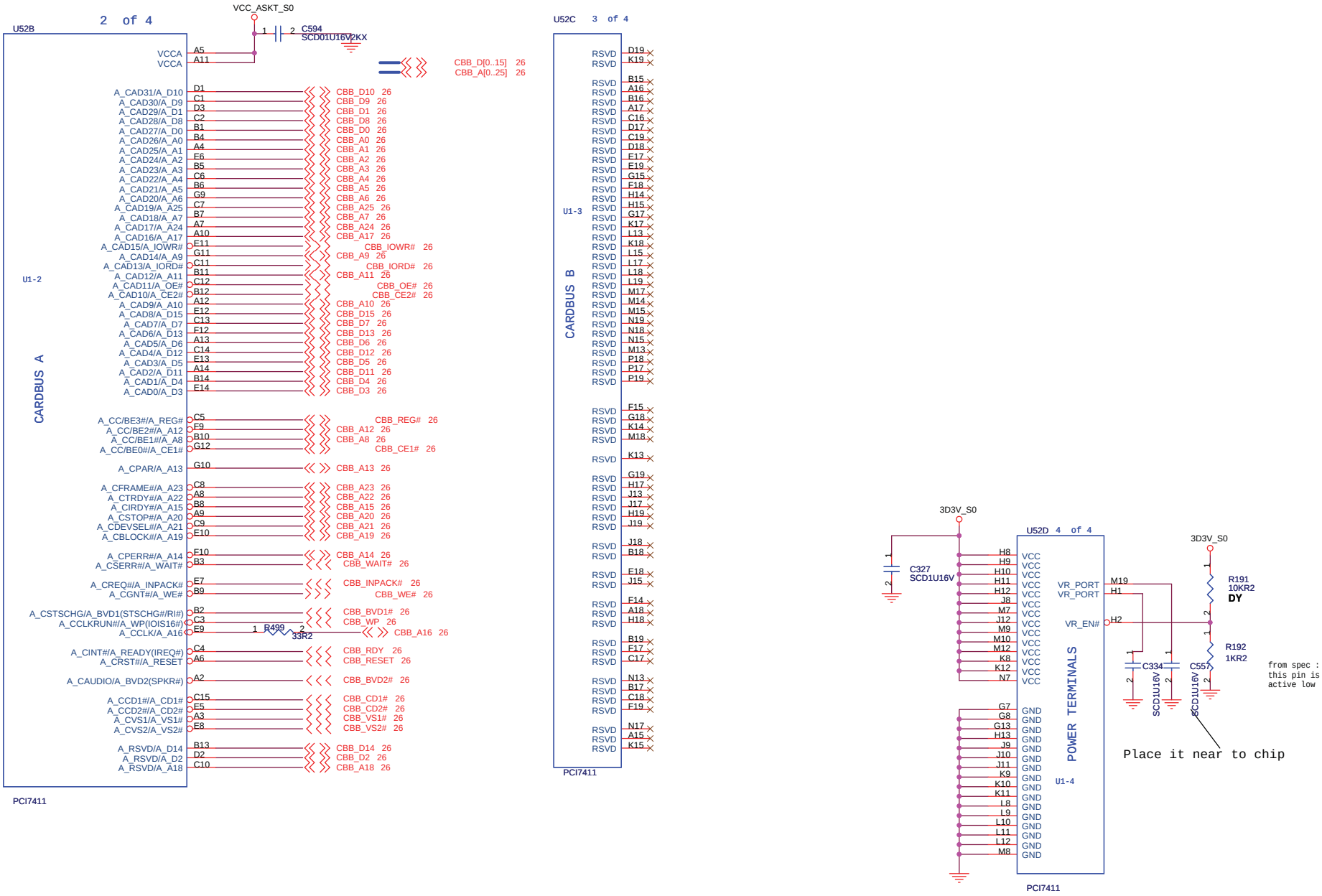
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
Custom	Myna2	SB

Date: Monday, September 26, 2005 Sheet 23 of 47


1 of 4
U52A
IDSEL:AD25
INTA-->:INT_PIRQG#
INTB-->:INT_PIRQB#
INTC-->:INT_PIRQF#
INTD-->:INT_PIRQG#
GNT:PCI_GNT0#
REQ:PCI_REQ0#
CARD BUS
1394
SD/SDIO
UNUSED TERMINALS
PCI7411
INTA# CARBUS 1 (INT_PIRQG#)
INTB# (WIFI) (INT_PIRQB#)
INTC# 1394 (INT_PIRQF#)
INTD# CardReader (INT_PIRQG#) share
Bypass/Decupoling Capacitors
Should be places as close to
PCI7411 as possible
MS/MS_pro
XD
SB_08/17
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TI_PCI7411(1 of 2)
MYNA
Date: Monday, September 26, 2005
Sheet 24 of 47

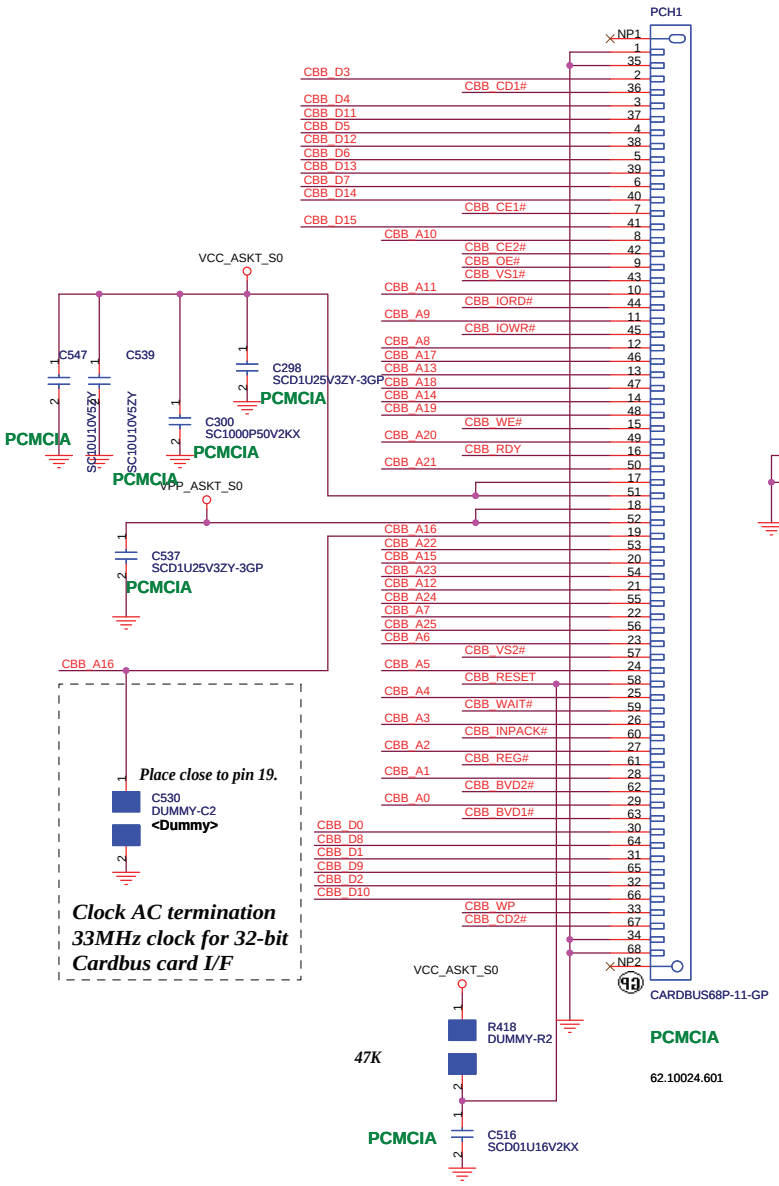


<Variant Name>

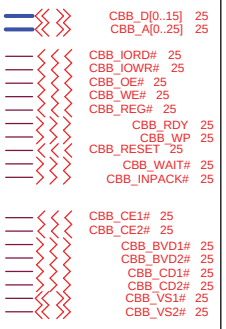
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

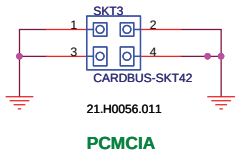
Title	TI_PCI7411(2 of 2)	
Size A3	Document Number MYNA	Rev SB
Date: Monday, September 26, 2005	Sheet 25 of 47	

PCMCIA Socket

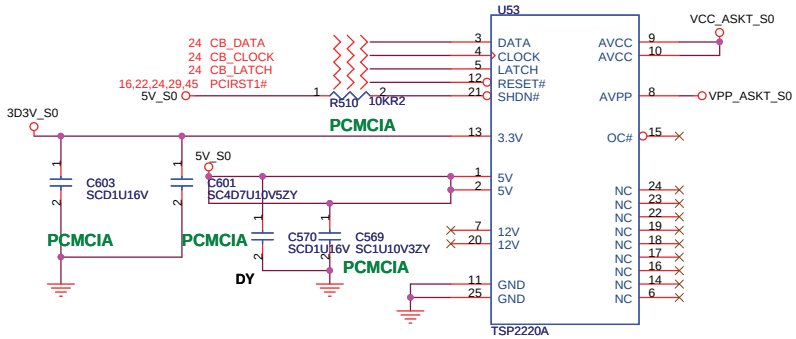


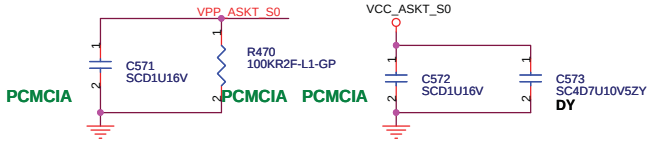
Cardbus I/F

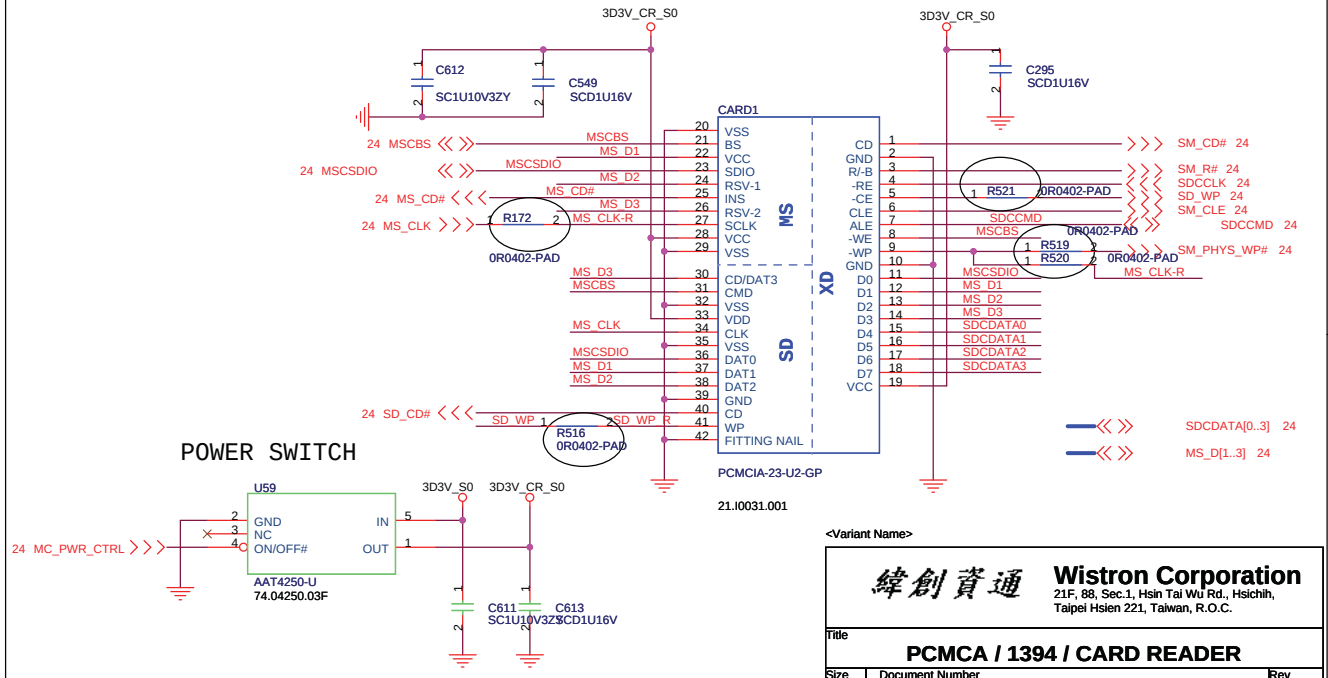




Power switch







<Variant Name>

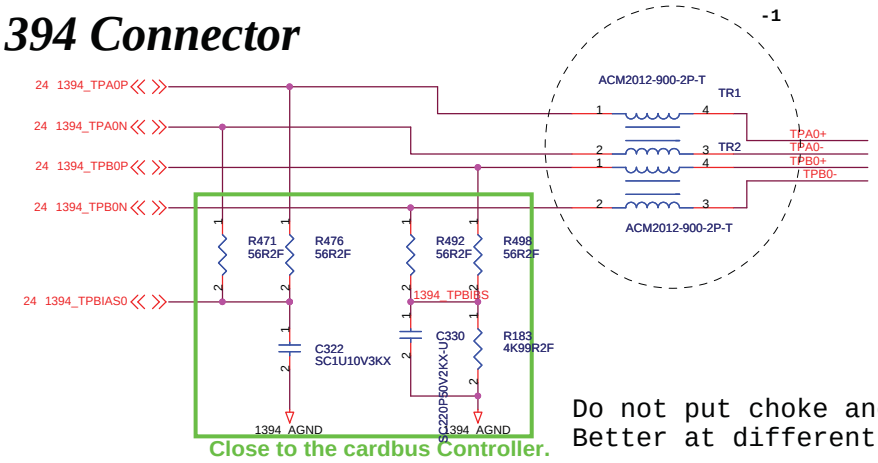
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

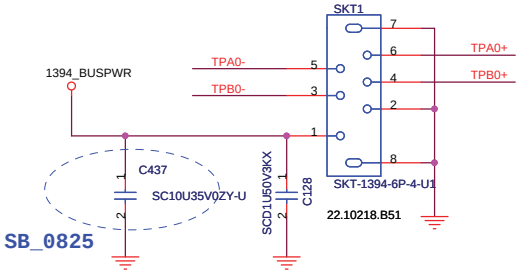
Title: **PCMCA / 1394 / CARD READER**

Size	Document Number	Rev
A3	Myna2	SB

Date: Monday, September 26, 2005 Sheet 26 of 47

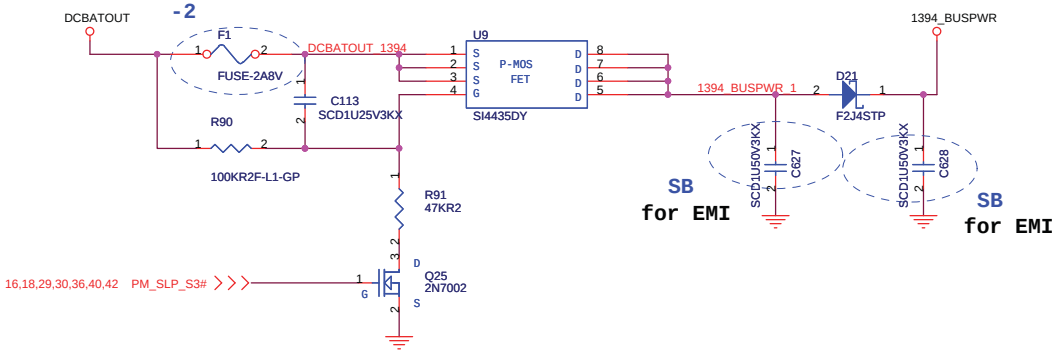
1394 Connector

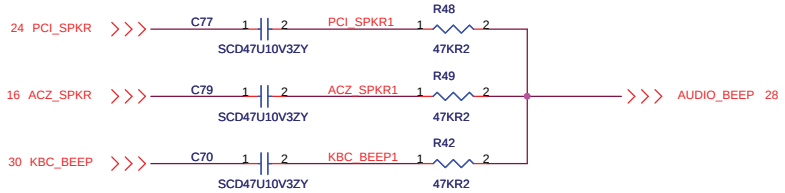




Do not put choke and 0 ohm at same location.
Better at different side.

4/21 External ODD will suck more than 1.5A when battery mode



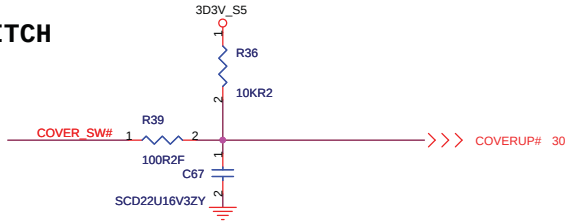


<Variant Name>

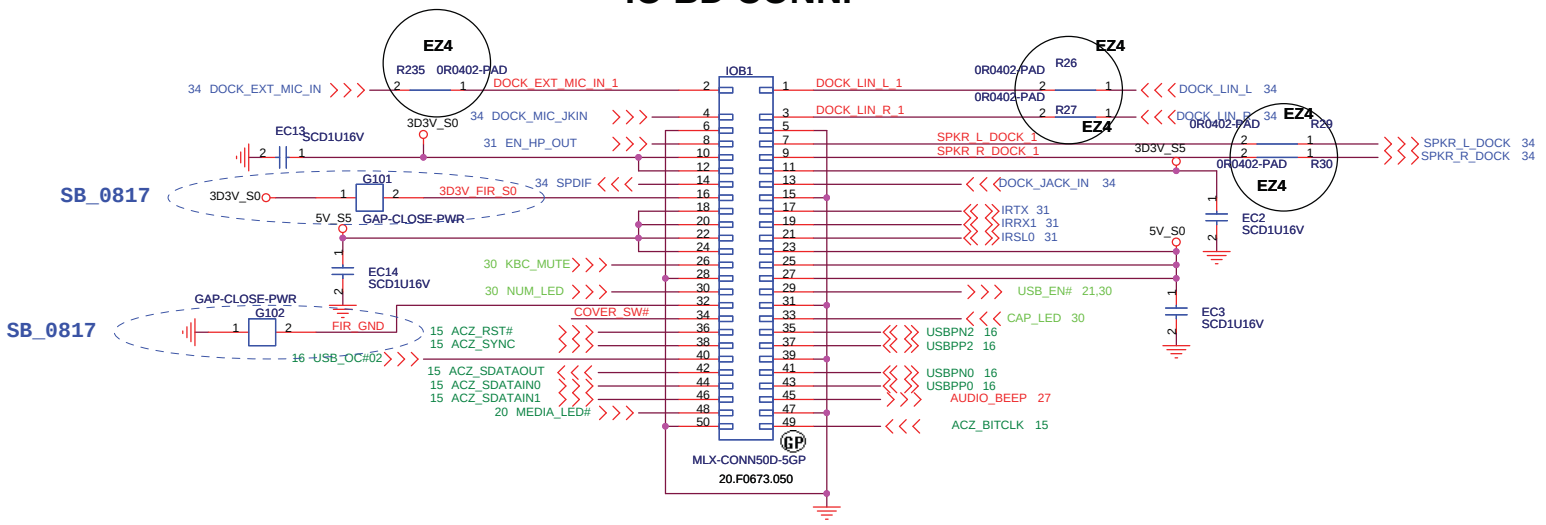
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1394 Connector		
Size: A3	Document Number: Myna2	Rev: SB
Date: Monday, September 26, 2005	Sheet 27 of 47	

COVER SWITCH



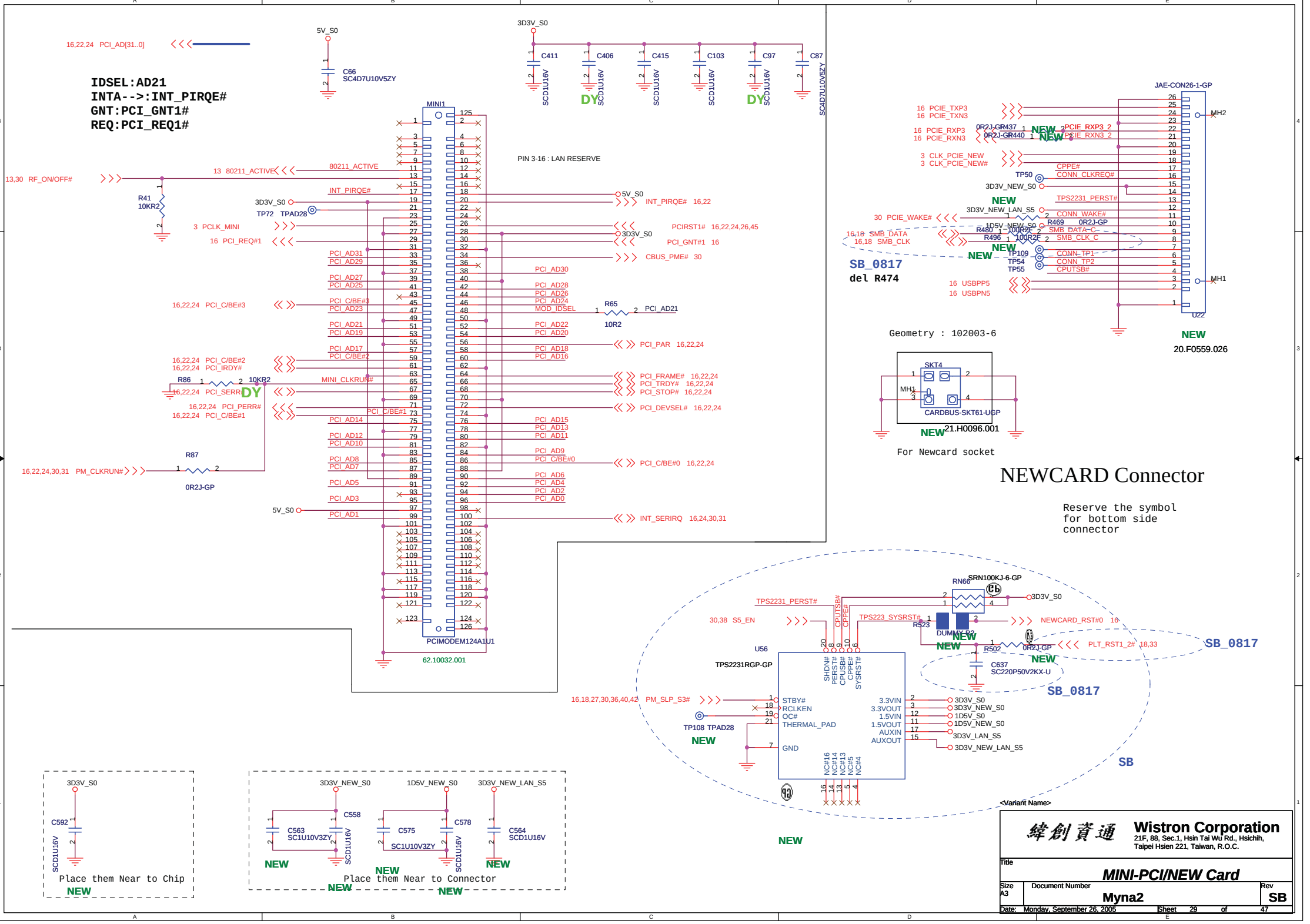
IO BD CONN.

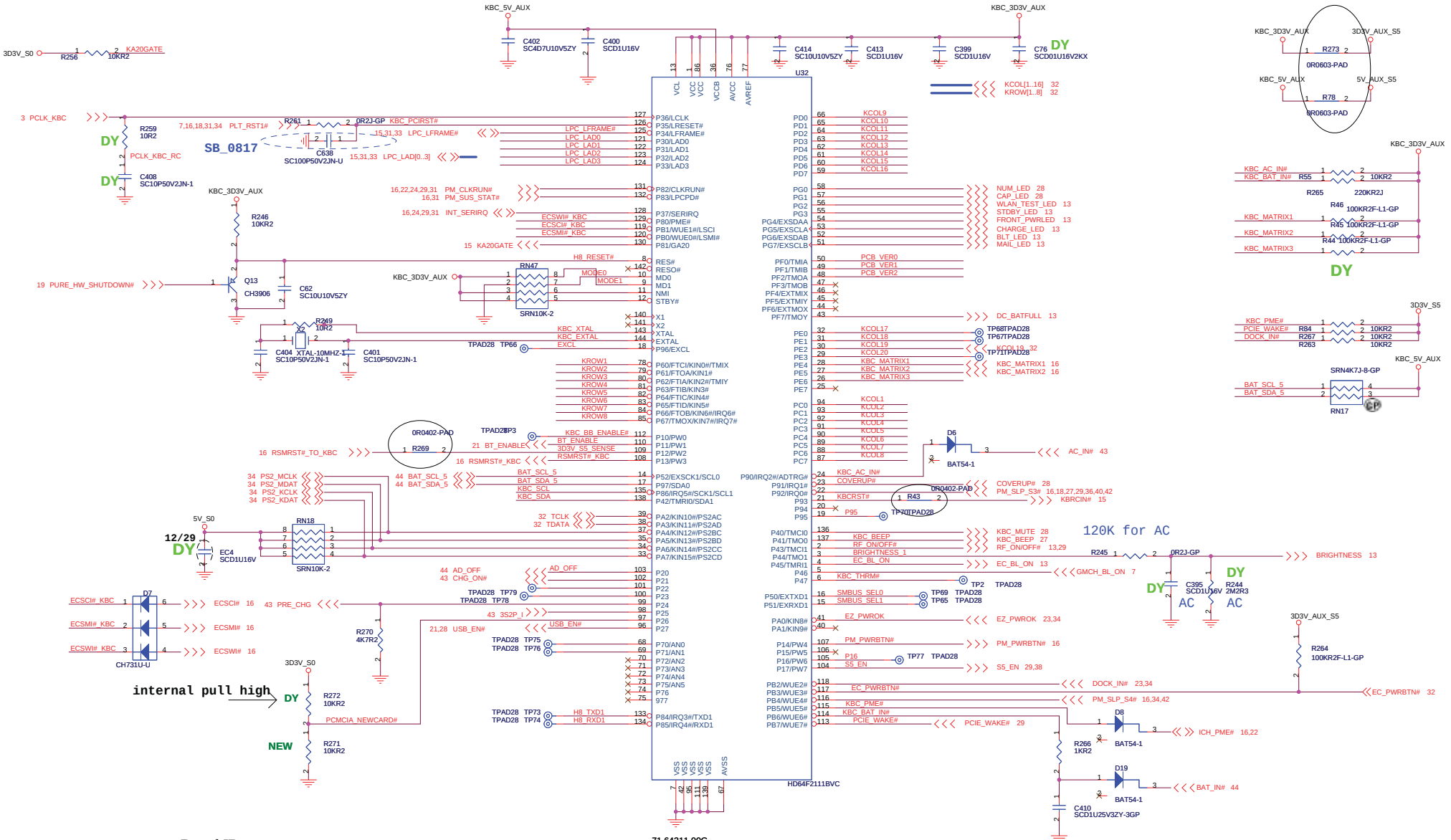


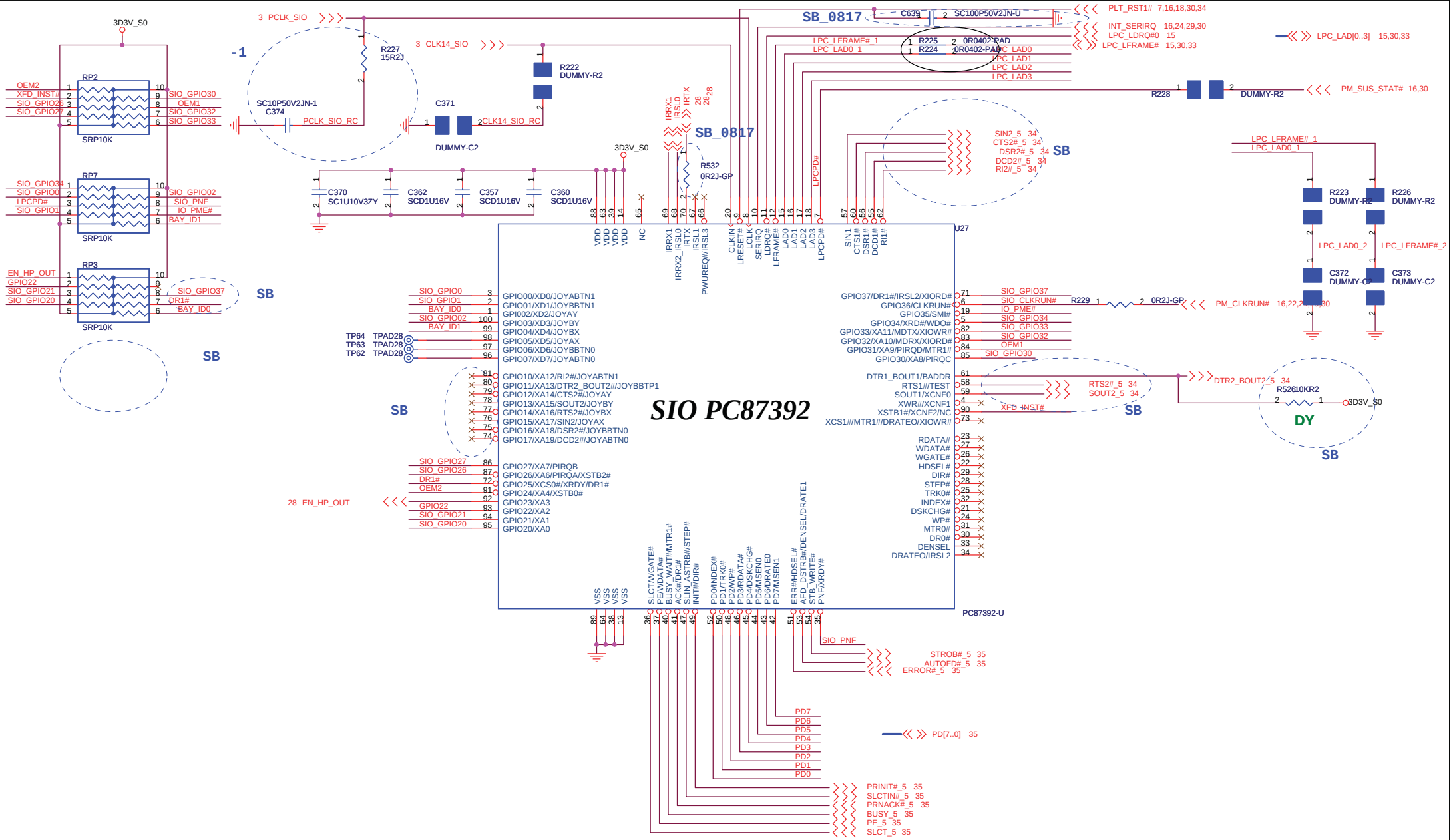
Blue -> Dock or SuperIO
Light Green -> KBC
Green -> SouthBridge

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AC'97 CODEC - ALC655		
Size: A3	Document Number: Myna2	Rev: SB
Date: Monday, September 26, 2005	Sheet 28 of 47	


IDSEL:AD21
INTA-->:INT_PIRQE#
GNT:PCI_GNT1#
REQ:PCI_REQ1#
MINI1
PCIMODEM124A1U1
62.10032.001
PIN 3-16 : LAN RESERVE
16,22,24 PCI_AD[31..0]
13,30 RF_ON/OFF#
13 80211_ACTIVE
80211_ACTIVE
INT_PIRQE#
3 PCLK_MINI
16 PCI_REQ#1
PCIRST1# 16,22,24,26,45
PCI_GNT#1 16
CBUS_PME# 30
INT_PIRQE# 16,22
INT_SERIRQ 16,24,30,31
PCI_PAR 16,22,24
PCI_FRAME# 16,22,24
PCI_TRDY# 16,22,24
PCI_STOP# 16,22,24
PCI_DEVSEL# 16,22,24
PCI_C/BE#0 16,22,24
16,22,24 PCI_C/BE#3
16,22,24 PCI_C/BE#2
16,22,24 PCI_IRDY#
16,22,24 PCI_SERR#
16,22,24 PCI_PERR#
16,22,24 PCI_C/BE#1
MINI_CLKRUN#
PCI_C/BE#1
MOD_IDSEL
16,22,24,30,31 PM_CLKRUN#
R41 10KR2
R86 10KR2
R87 0R2J-GP
R65 10R2
DY
3D3V_S0
5V_S0
TP72 TPAD28
C66 SC4D7U10V5ZY
C411 C406 C415 C103 C97 C87
SCD1U16V
SC4D7U10V5ZY
JAE-CON26-1-GP
MH1 MH2
U22
16 PCIE_TXP3
16 PCIE_TXN3
16 PCIE_RXP3
16 PCIE_RXN3
PCIE_RXP3_2
PCIE_RXN3_2
0R2J-GR437
0R2J-GR440
NEW
3 CLK_PCIE_NEW
3 CLK_PCIE_NEW#
CPPE#
CONN_CLKREQ#
TP50
3D3V_NEW_S0
TPS2231_PERST#
30 PCIE_WAKE#
3D3V_NEW_LAN_S5
CONN_WAKE#
1D5V_NEW_S0
R469 0R2J-GP
16,18 SMB_DATA
16,18 SMB_CLK
R480 100R2F
R496 100R2F
SMB_DATA_C
SMB_CLK_C
TP109
TP54
TP55
CONN_TP1
CONN_TP2
CPUTSB#
16 USBPP5
16 USBPN5
SB_0817
del R474
Geometry : 102003-6
SKT4
CARDBUS-SKT61-UGP
21.H0096.001
20.F0559.026
For Newcard socket
NEWCARD Connector
Reserve the symbol
for bottom side
connector
RN66 SRN100KJ-6-GP
TPS2231_PERST#
30,38 S5_EN
TPS223_SYSRST#
R523 DUMMY_R3
NEWCARD_RST#0 10
R502 0R2J-GP
PLT_RST1_2# 18,33
C637 SC220P50V2KX-U
U56
TPS2231RGP-GP
SHDN#
PERST#
CPUSB#
CPPE#
SYSRST#
16,18,27,30,36,40,42 PM_SLP_S3#
TP108 TPAD28
STBY#
RCLKEN
OC#
THERMAL_PAD
GND
3.3VIN
3.3VOUT
1.5VIN
1.5VOUT
AUXIN
AUXOUT
3D3V_LAN_S5
3D3V_NEW_LAN_S5
1D5V_S0
1D5V_NEW_S0
NC#16
NC#14
NC#13
NC#5
NC#4
SB_0817
SB
C592
C563 SC1U10V3ZY
C558
C575 SC1U10V3ZY
C578
C564 SCD1U16V
Place them Near to Chip
Place them Near to Connector
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MINI-PCI/NEW Card
Size A3
Document Number
Myna2
Rev SB
Date: Monday, September 26, 2005
Sheet 29 of 47

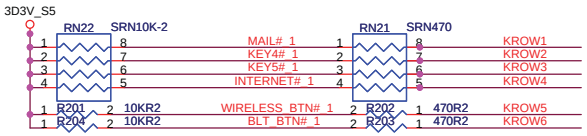

U32
HD64F2111BVC
71.64211.00G
internal pull_high
SB_0817
DY
NEW
120K for AC
Board ID
Planar ID(2,1,0)
SA: 0, 0, 0
SB: 0, 0, 1
SC: 0, 1, 0
SD: 0, 1, 1
-1: 1, 0, 0
-2: 1, 0, 1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC H8
Myna2
Monday, September 26, 2005



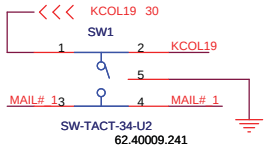
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***SIO***		
Size: A3	Document Number: Myna2	Rev: **SB**
Date: Monday, September 26, 2005	Sheet 31 of 47	

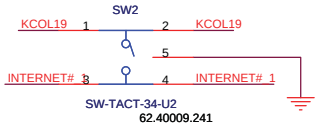
Launch BD CONN



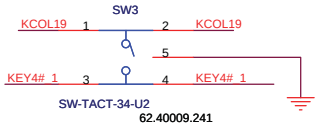
MAIL BUTTON



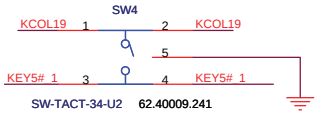
INTERNET BUTTON

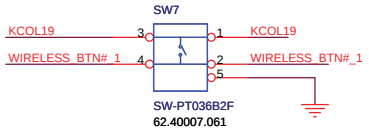


P4 BUTTON

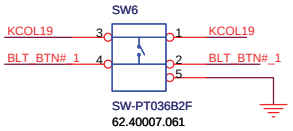


P5 BUTTON

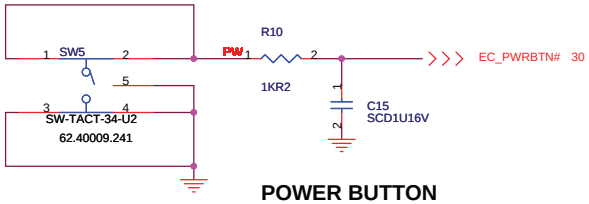




WIRELESS BUTTON

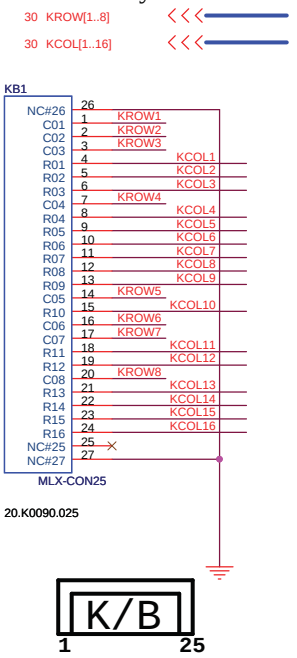


BLUETOOTH BUTTON

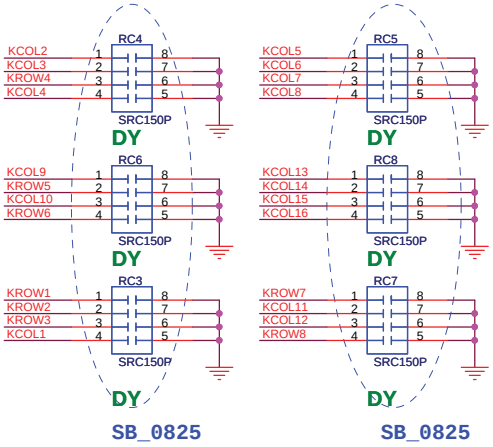


POWER BUTTON

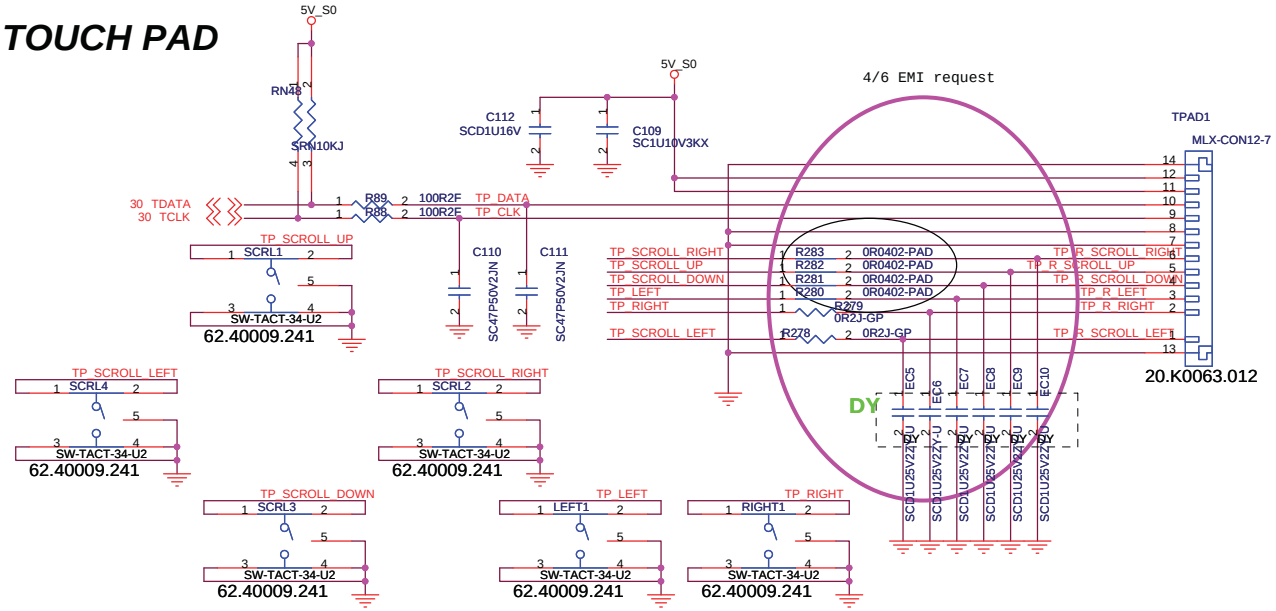
Internal KeyBoard Connector



EMI CAPS



TOUCH PAD



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: KBC&TPAD CONN		
Size: A3	Document Number: Myna2	Rev: SB
Date: Monday, September 26, 2005	Sheet 32 of 47	

? if use Debug Board, remove this R

SB_0817

PLT_RST1_2# — R195 100R2F — FWHRST#

C643 SC150P50V2JN

-1

Unused FGPI pins must not be float

RP11

SELECT_FWH, FWH_FGPI4, FWH_FGPI3, FWH_FGPI2, FWH_FGPI1, FWH_FGPI0

SRP10K 66.10336.100

15,30,31 LPC_LAD[0:3]

TOP VIEW

A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)

(BOTTOM VIEW)

FLASH ROM

512K Bits X 8 = 4M Bits

3D3V_S0

C341 SCD1U16V

C340 SC1U10V3ZY

U58

NC, NC, NC, VSS, IC, A10/FGPI4, R/C#(CLK), VDD, NC, RST#, A9(FGPI3), A8(FGPI2), A7(FGPI1), A6(FGPI0), A5(WP#), A4(TBL#)

OE#/INIT#, WE#/FWH4, NC, DQ7/RES, DQ6/RES, DQ5/RES, DQ4/RES, DQ3/LAD3, VSS, DQ2/LAD2, DQ1/LAD1, DQ0/LAD0, A0/ID0, A1/ID1, A2/ID2, A3/ID3

FWH_INIT#, LPC_LFRAME#, LPC_LAD3, LPC_LAD2, LPC_LAD1, LPC_LAD0

SELECT_FWH, FWH_FGPI4, PCLK_FWH, FWHRST#, FWH_FGPI3, FWH_FGPI2, FWH_FGPI1, FWH_FGPI0

BC15 DUMMY-C3, R515 DUMMY-R3

R522 10KR2 — 3D3V_S0

49LF004A-33

SECOND SOURCE
72.39040.H09

GOLDEN FINGER FOR DEBUG BOARD

SB_0817

18,29 PLT_RST1_2#
15,30,31 LPC_LFRAME#
3 PCLK_FWH
15 FWH_INIT#

5V_S0

U23

A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15

B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15

PLT_RST1_2#, LPC_LFRAME#, PCLK_FWH, FWH_INIT#, LPC_LAD3, LPC_LAD2, LPC_LAD1, LPC_LAD0, EXT_FWH#

3D3V_S0

FOX-GF30
ZZ.GF030.XXX

SB_0817

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

3D3V_S0

C331 SC10U6D3V5MX, C605 SCD1U16V, C320 SCD1U16V

DY DY DY

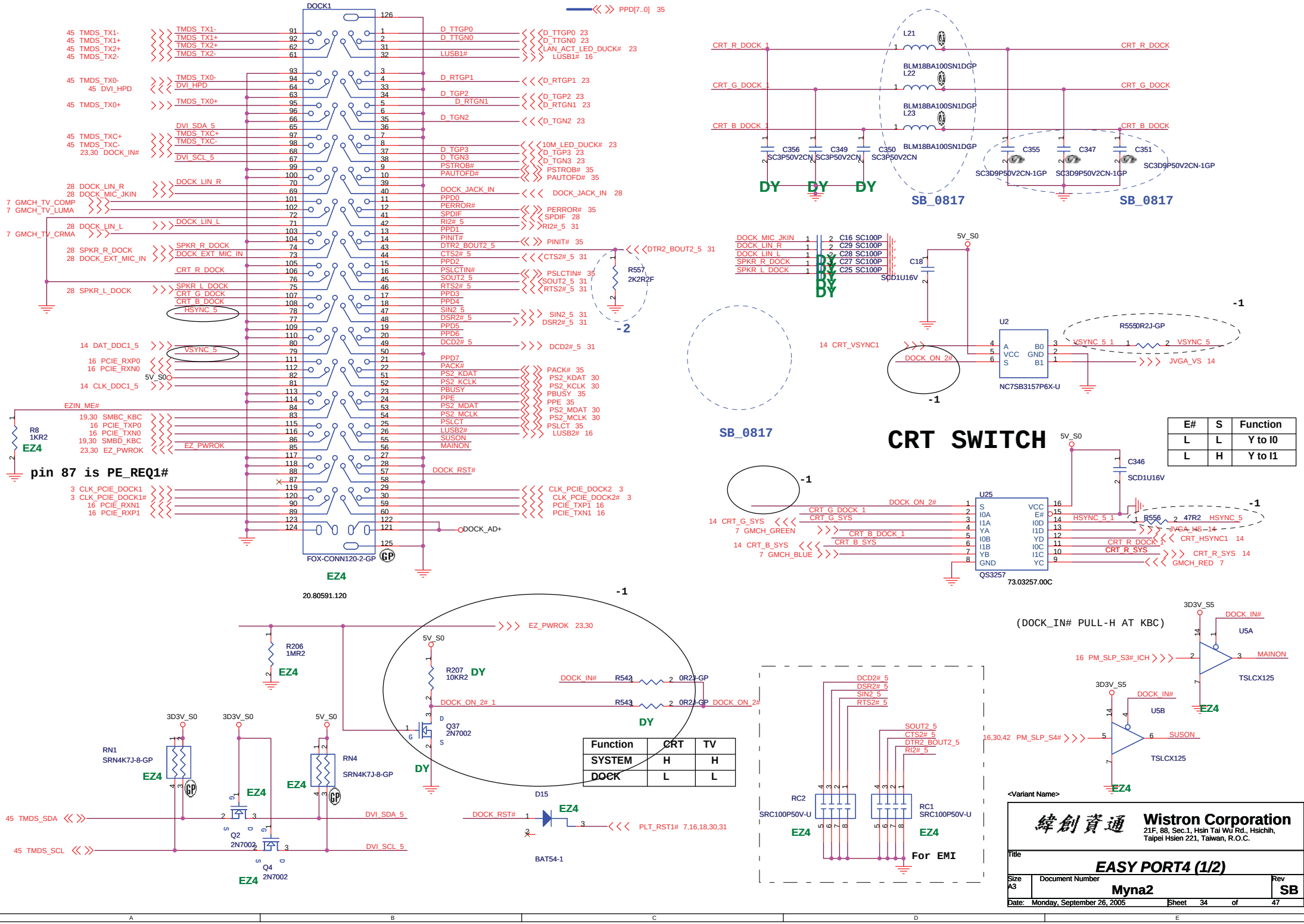
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: FWH and Debug

Size: A3 | Document Number: Myna2 | Rev: SB

Date: Monday, September 26, 2005 | Sheet 33 of 47



E#	S	Function
L	L	Y to I0
L	H	Y to I1

Function	CRT	TV
SYSTEM	H	H
DOCK	L	L

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

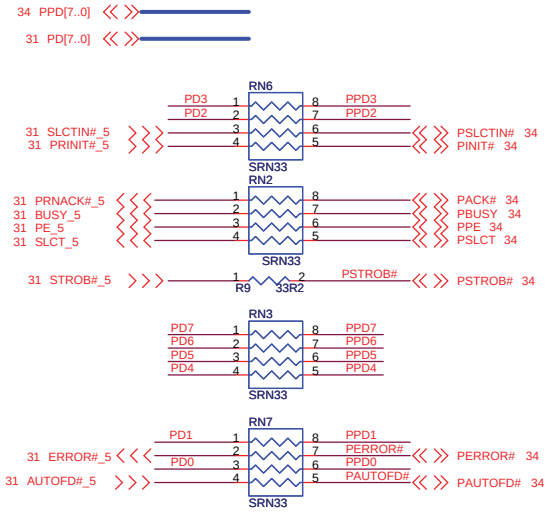
Title: EASY PORT4 (1/2)

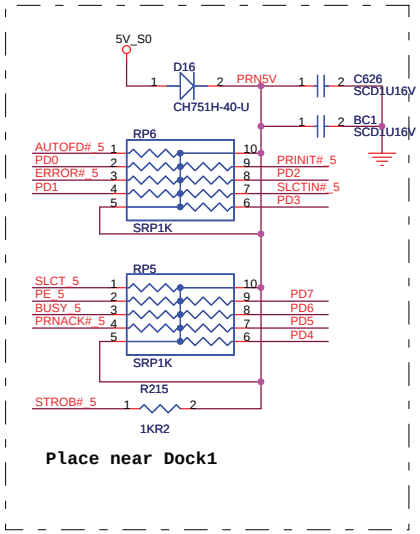
Size: A3 | Document Number: Myna2 | Rev: SB

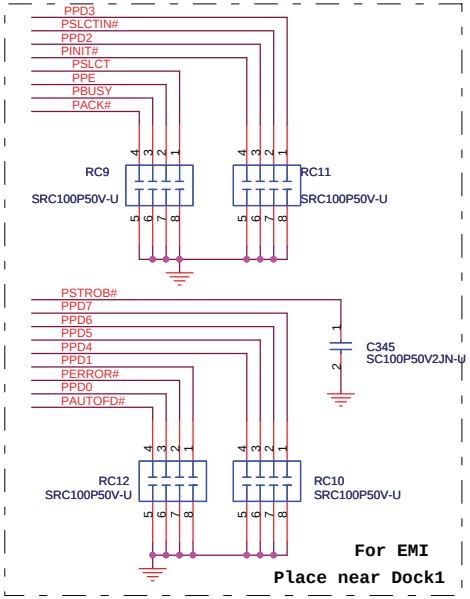
Date: Monday, September 26, 2005 | Sheet 34 of 47

<Variant Name>

PRINT PORT





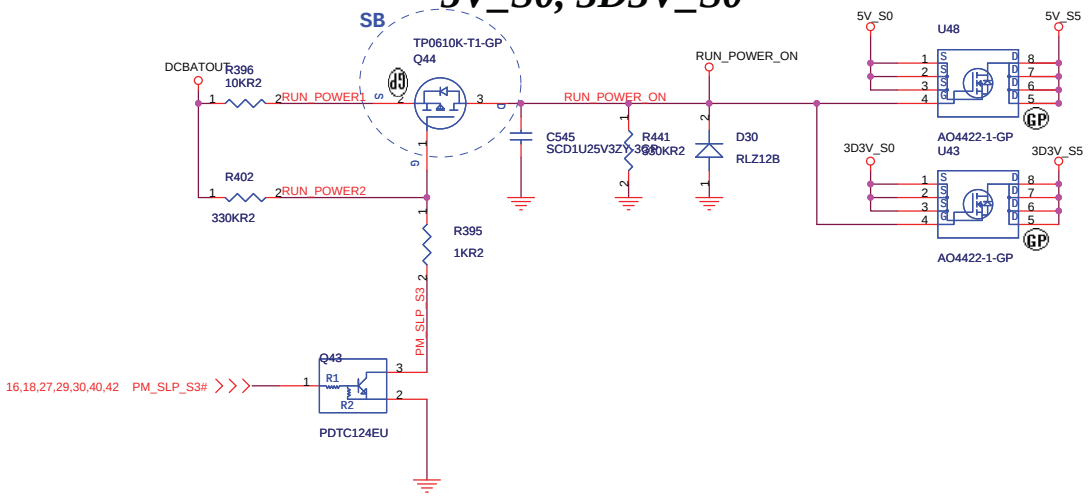


<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***EASY PORT4 (2/2)***	
Size A3	Document Number Myna2	Rev **SB**
Date: Monday, September 26, 2005	Sheet 35 of 47	

5V_S0, 3D3V_S0



<Variant Name>

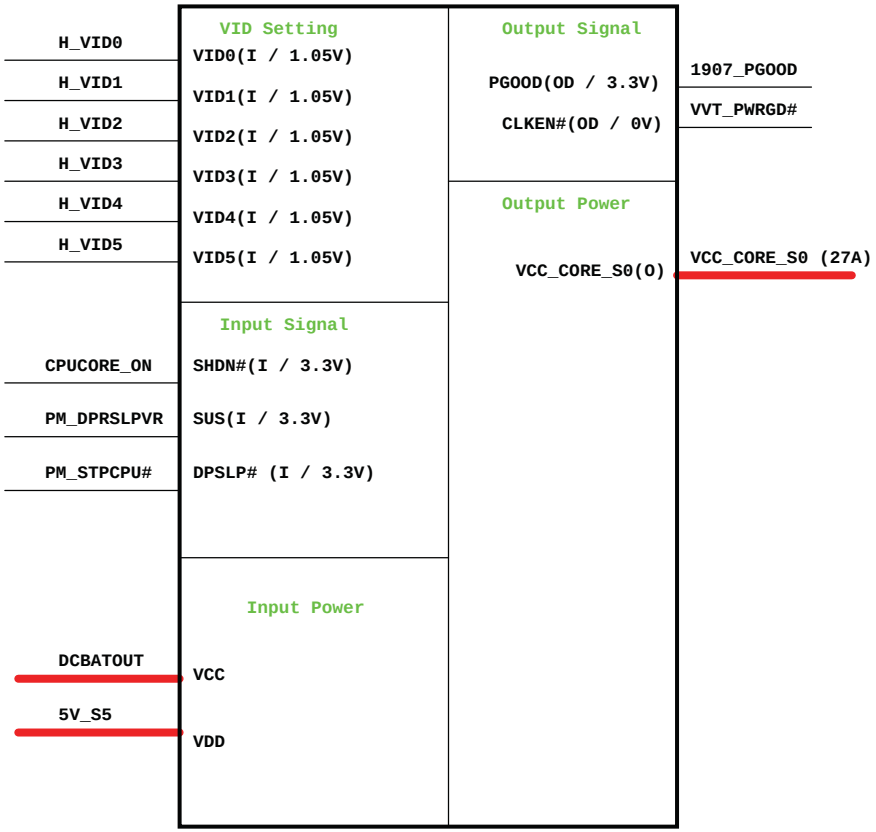
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RUN Power***

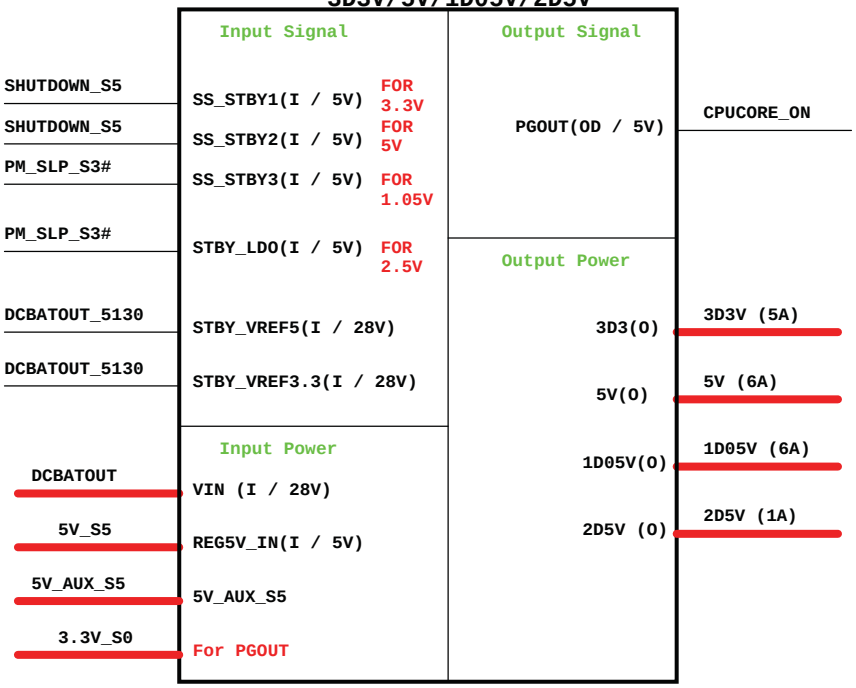
Size	Document Number	Rev
A3	Myna2	SB

Date: Monday, September 26, 2005 Sheet 36 of 47

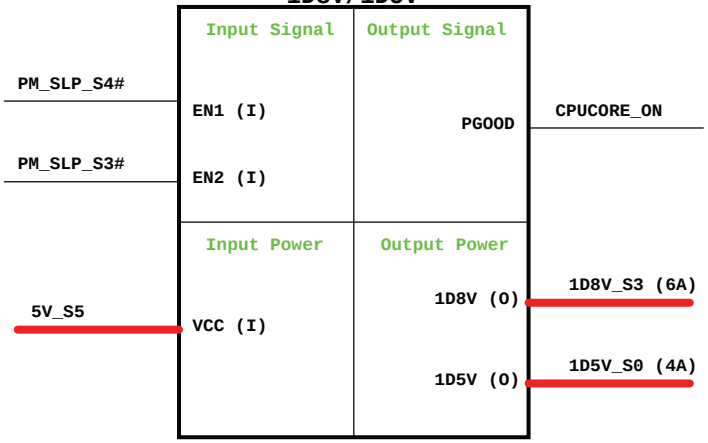
CPU_CORE MAX1907AETL-U



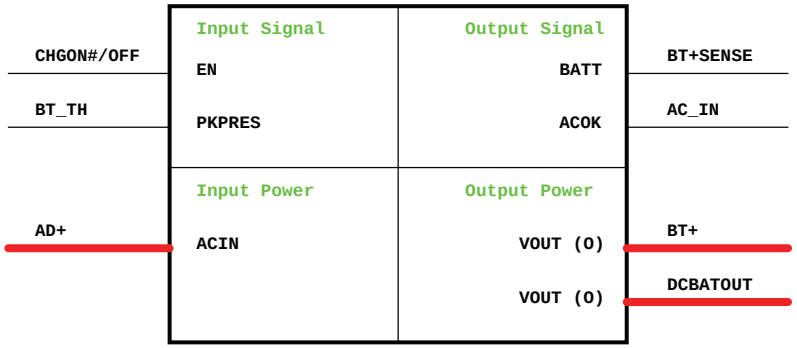
TPS5130 3D3V/5V/1D05V/2D5V



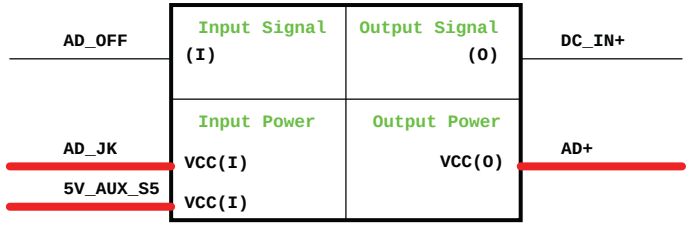
MAX8743 1D8V/1D5V



Charger ISL6225



Adapter



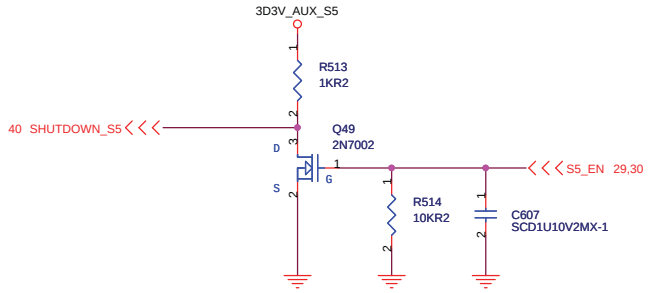
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

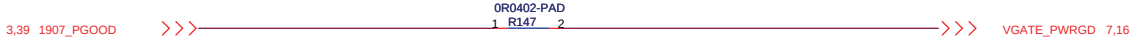
Title: Power Diagram

Size	Document Number	Rev
A3	Myna2	SB

Date: Monday, September 26, 2005 Sheet 37 of 47



PWRGD for NB and SB



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***POWER ON CIRCUIT***

Size	Document Number	Rev
A3	Myna2	SB

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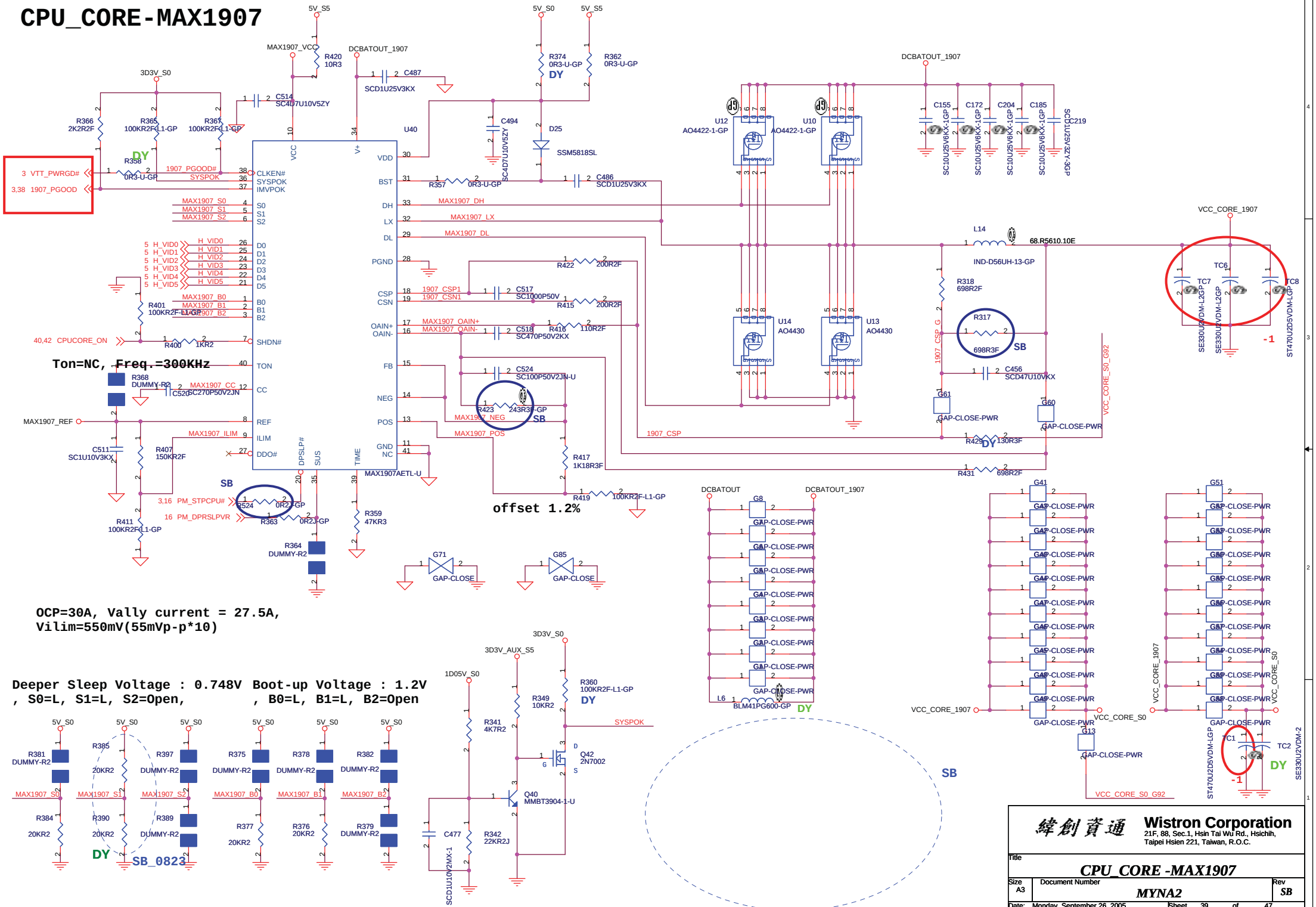
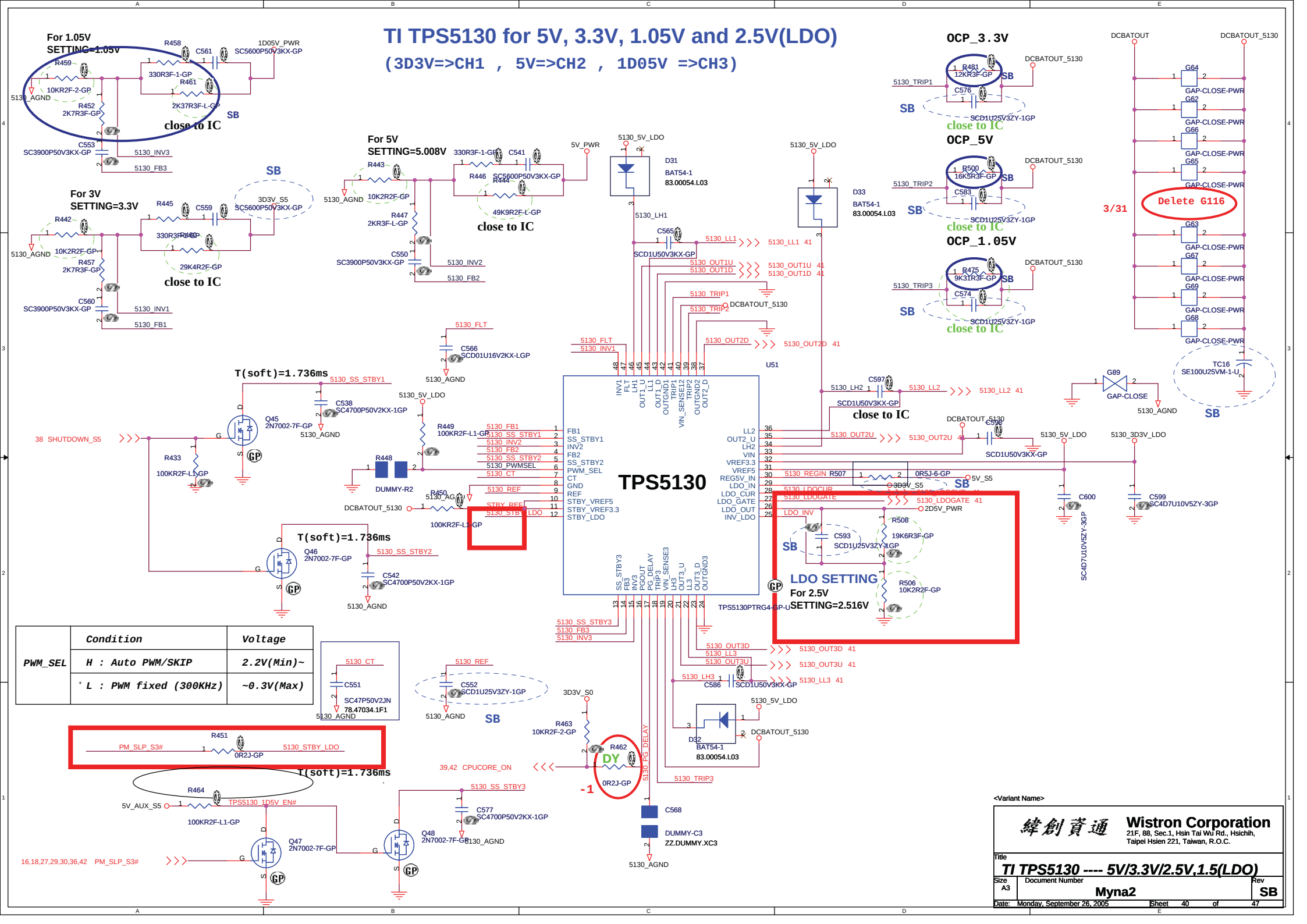
CPU_CORE-MAX1907



TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V(LDO)

(3D3V=>CH1 , 5V=>CH2 , 1D05V =>CH3)

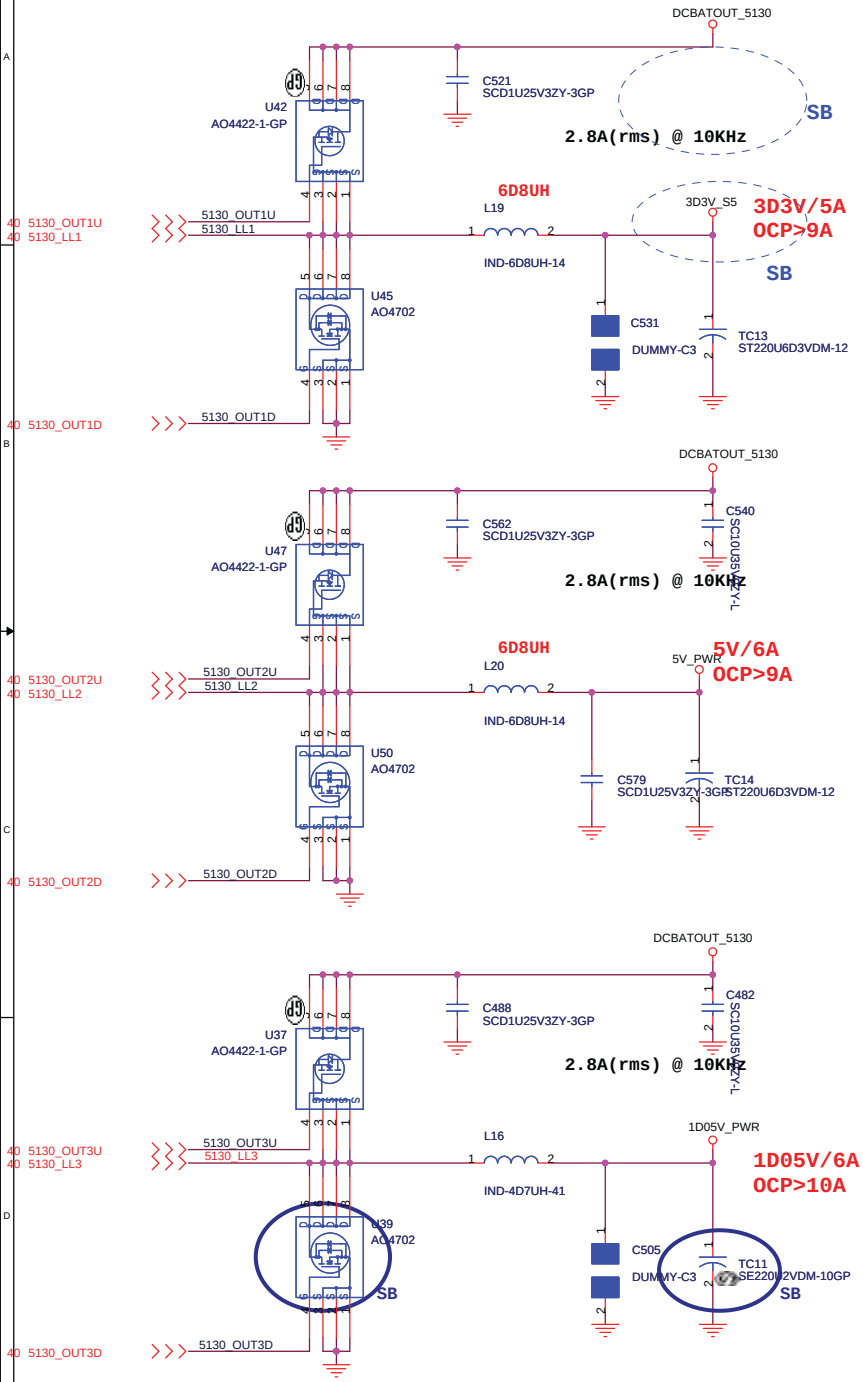


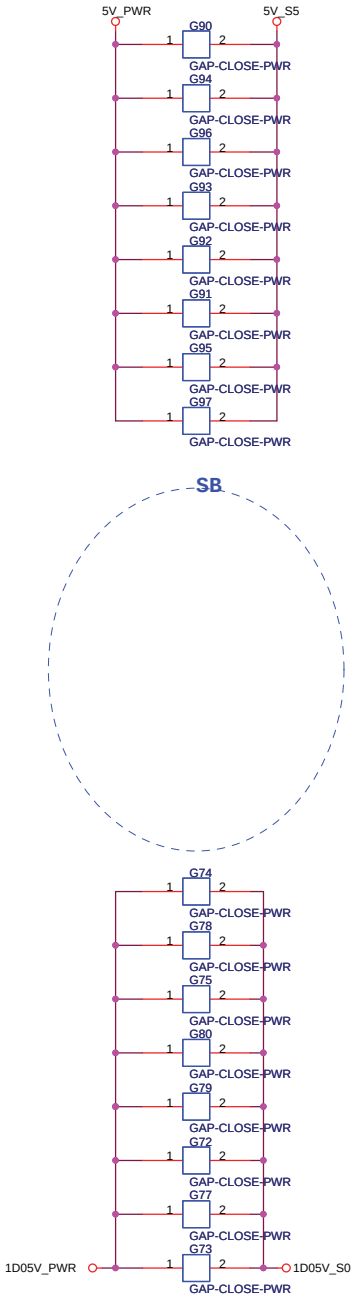
<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	TI TPS5130 ---- 5V/3.3V/2.5V,1.5(LDO)
Size: A3	Document Number: Myna2
Rev	SB
Date: Monday, September 26, 2005	Sheet 40 of 47

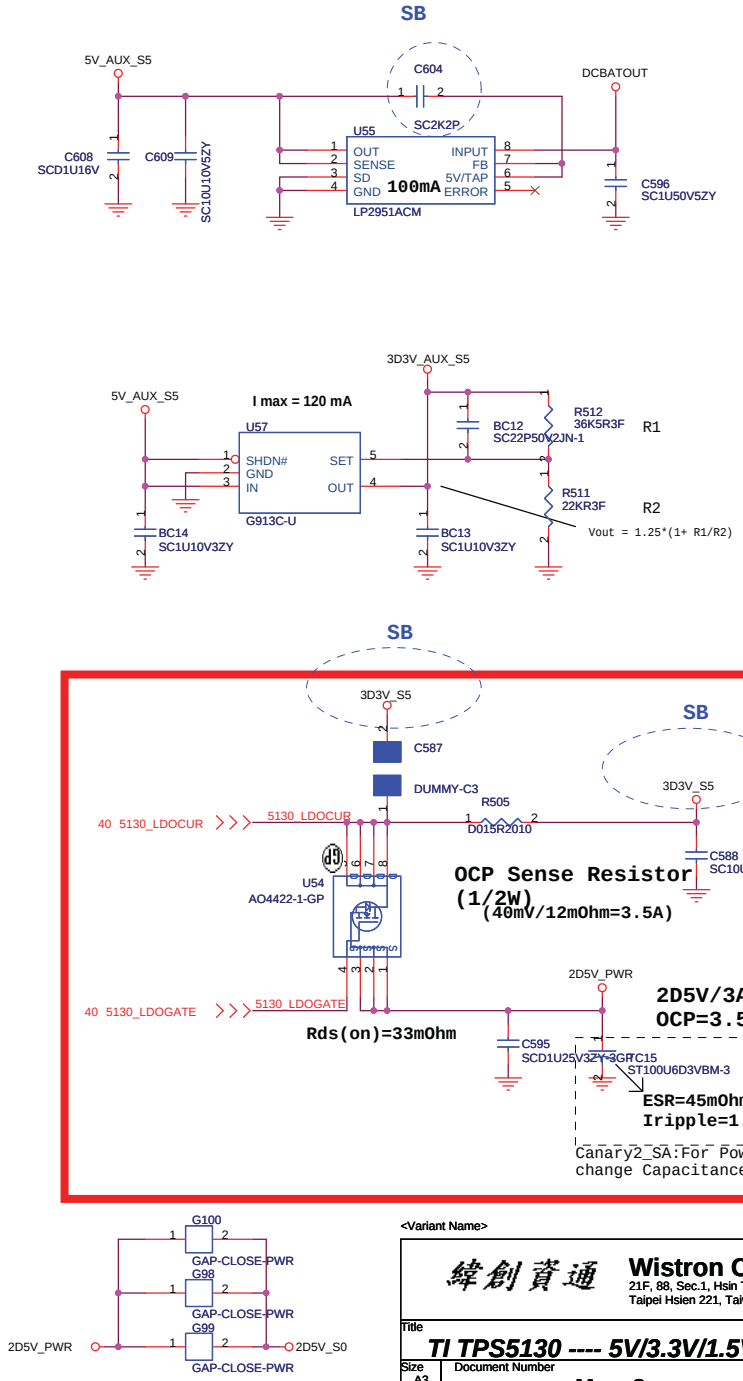
TI TPS5130 for 5V, 3.3V, 1.05V and 2.5V(LDO)

(3D3V=>CH1 , 5V=>CH2 , 1D05V =>CH3)





Aux Power



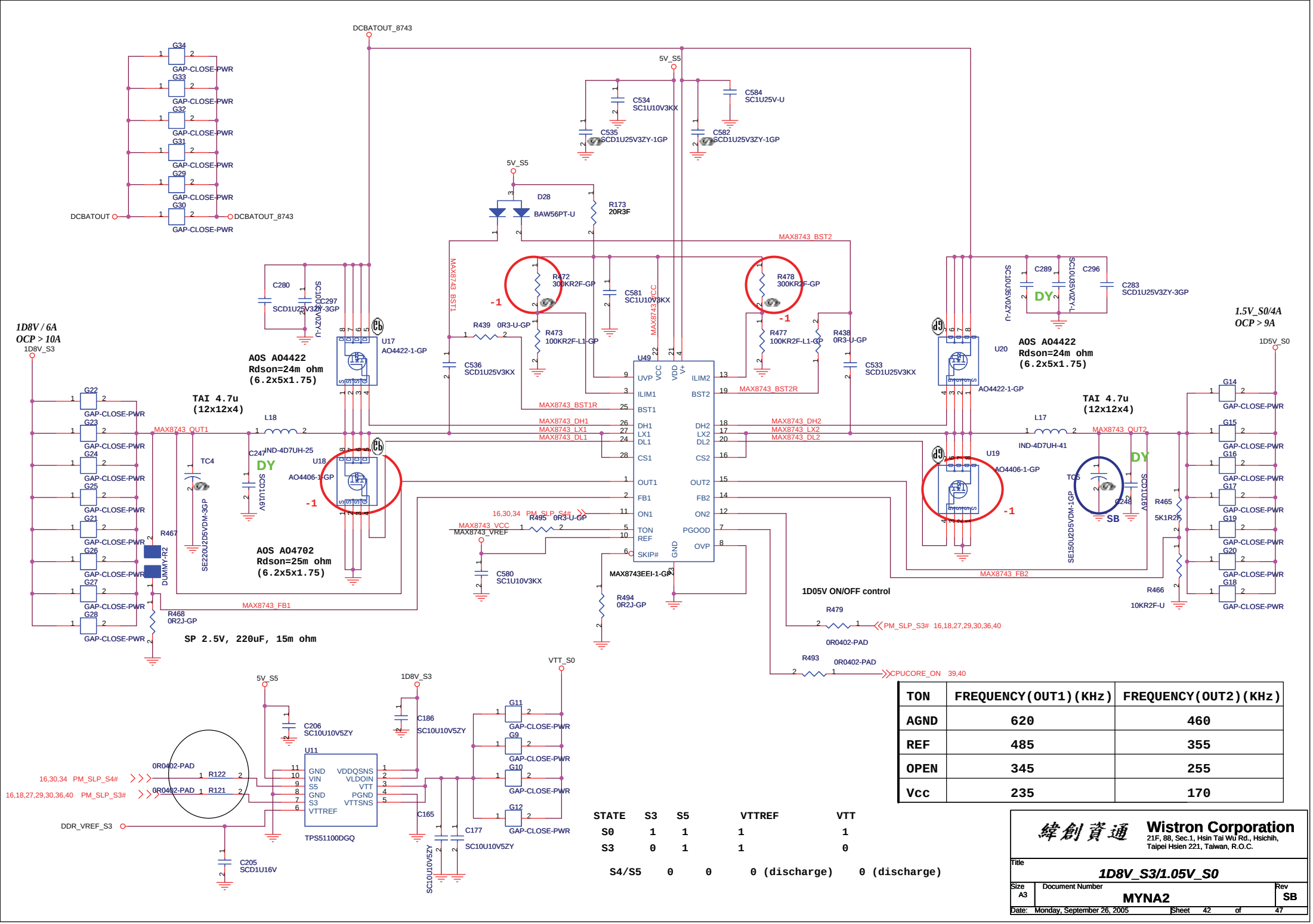
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *TI TPS5130 ---- 5V/3.3V/1.5V,2.5(LDO)*

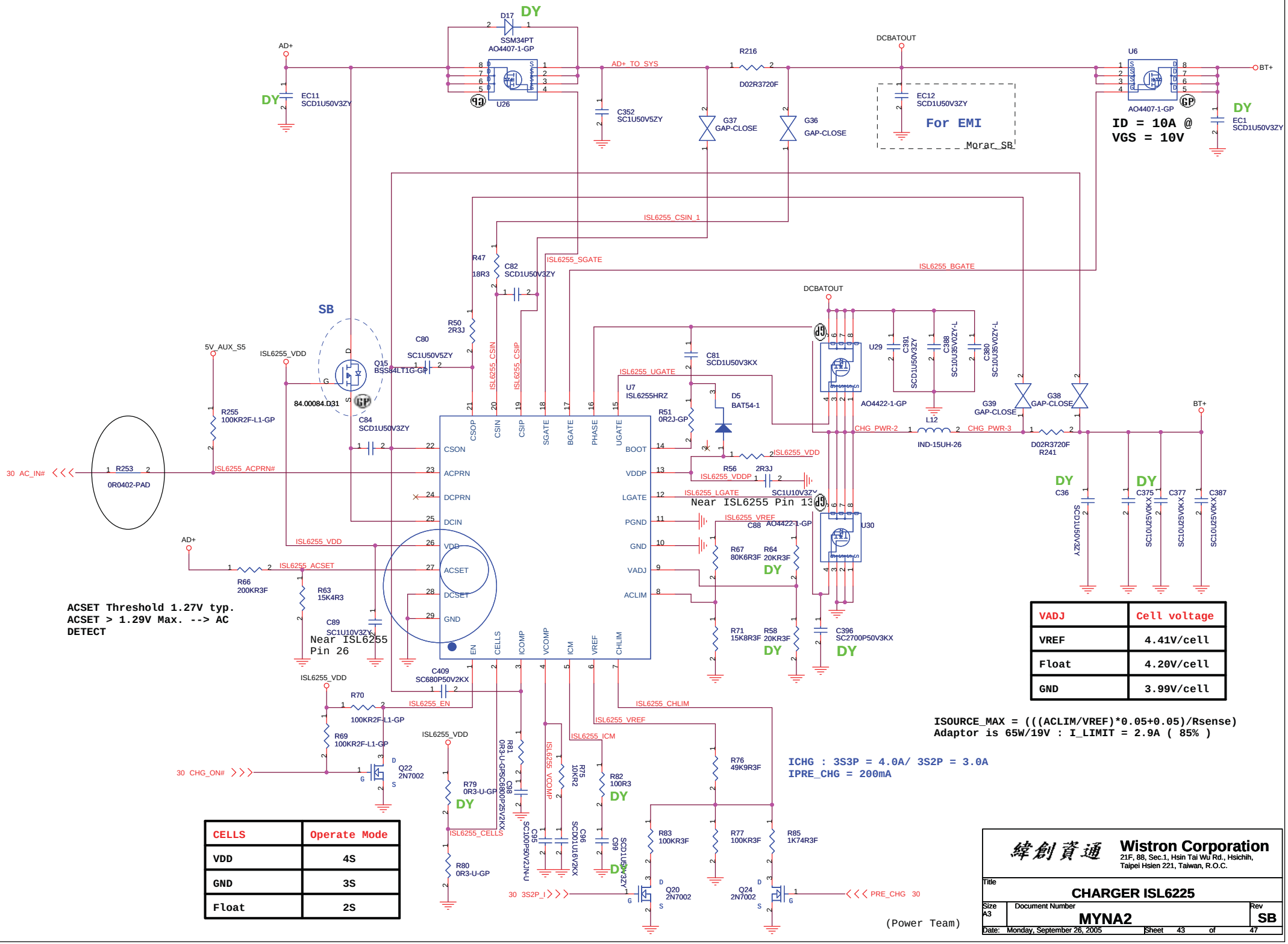
Size	Document Number	Rev
A3	Myna2	SB

Date: Monday, September 26, 2005 Sheet 41 of 47



TON	FREQUENCY(OUT1)(KHz)	FREQUENCY(OUT2)(KHz)
AGND	620	460
REF	485	355
OPEN	345	255
Vcc	235	170

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: 1D8V_S3/1.05V_S0	
Size: A3	Document Number: MYNA2
Rev: SB	
Date: Monday, September 26, 2005	Sheet 42 of 47



VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 65W/19V : I_LIMIT = 2.9A (85%)

ICHG : 3S3P = 4.0A/ 3S2P = 3.0A
IPRE_CHG = 200mA

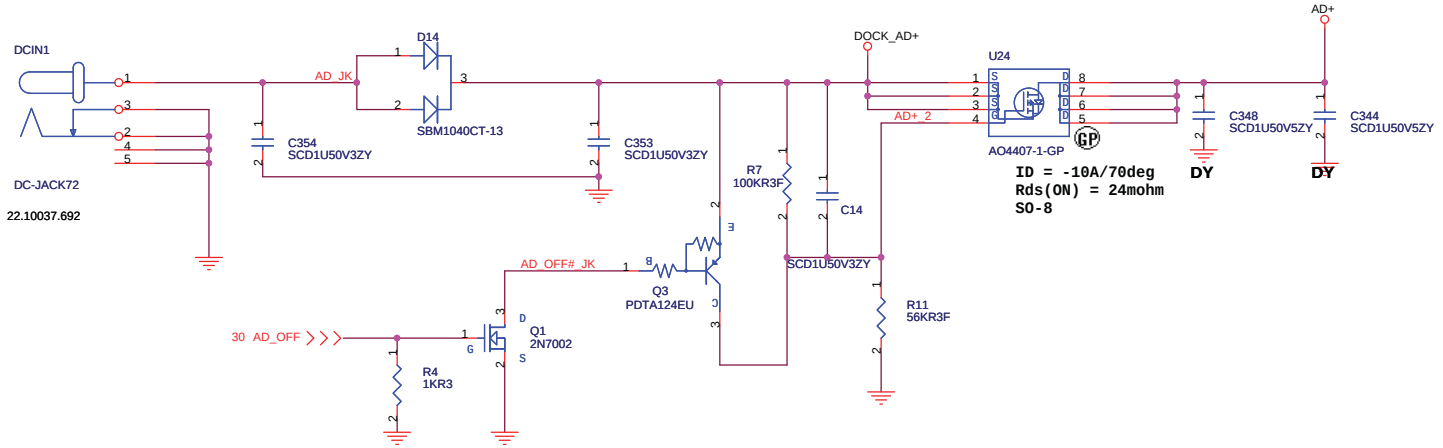
CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

(Power Team)

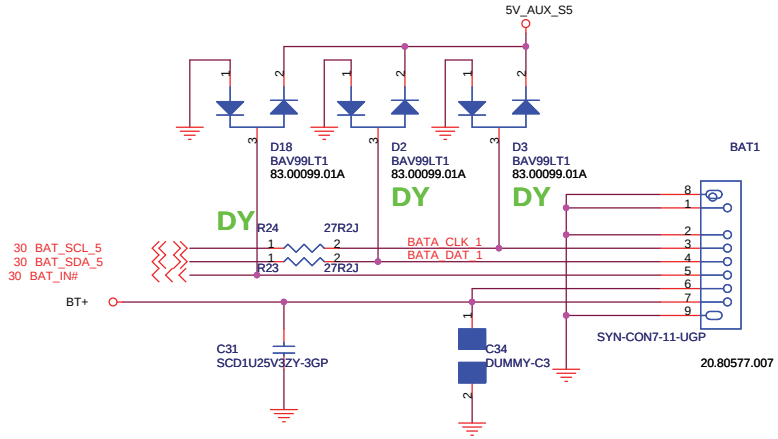
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER ISL6225
Size: A3 | Document Number: MYNA2 | Rev: SB
Date: Monday, September 26, 2005 | Sheet 43 of 47

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BAT CONN**

Size	Document Number	Rev
A3	Myna2	SB

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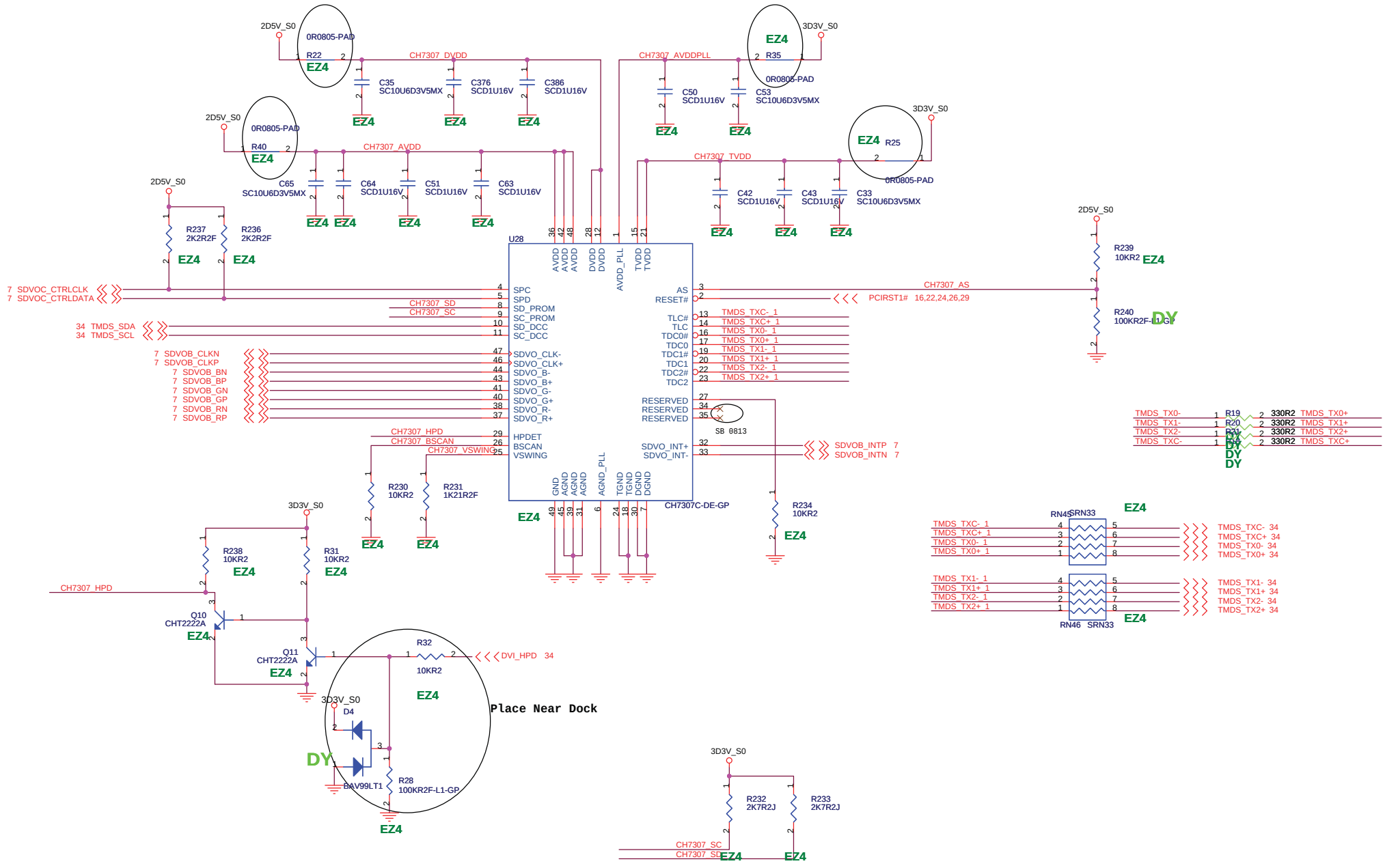

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DVI Transmitter-CH7307C***

Size	Document Number	Rev
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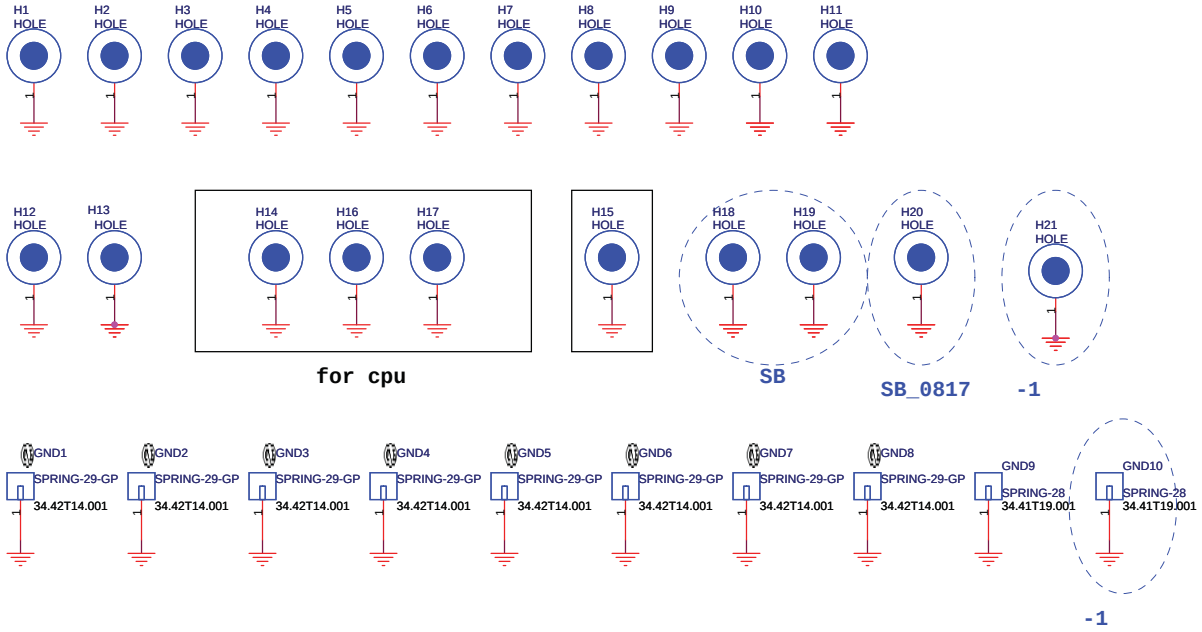

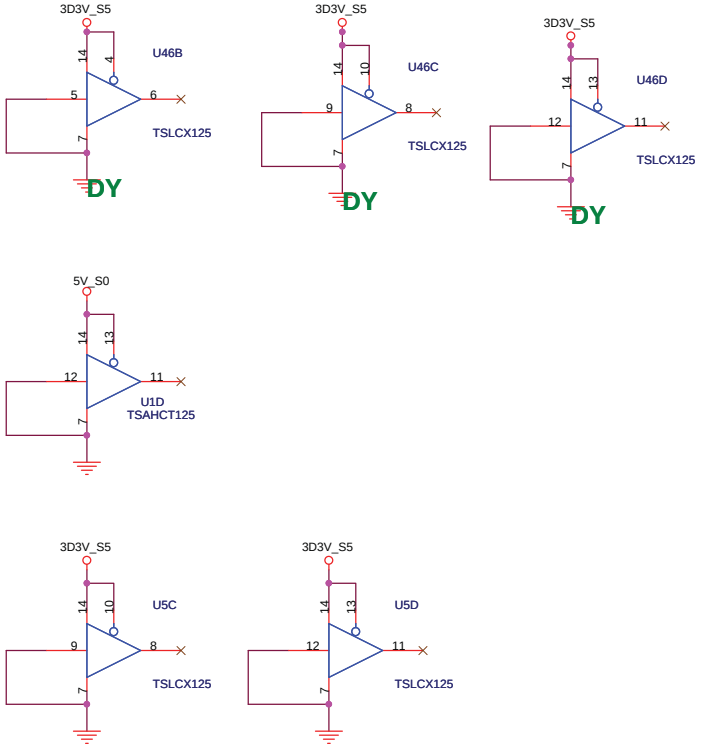

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Title: ***SPRING,BOSS & UNUSED TTL***

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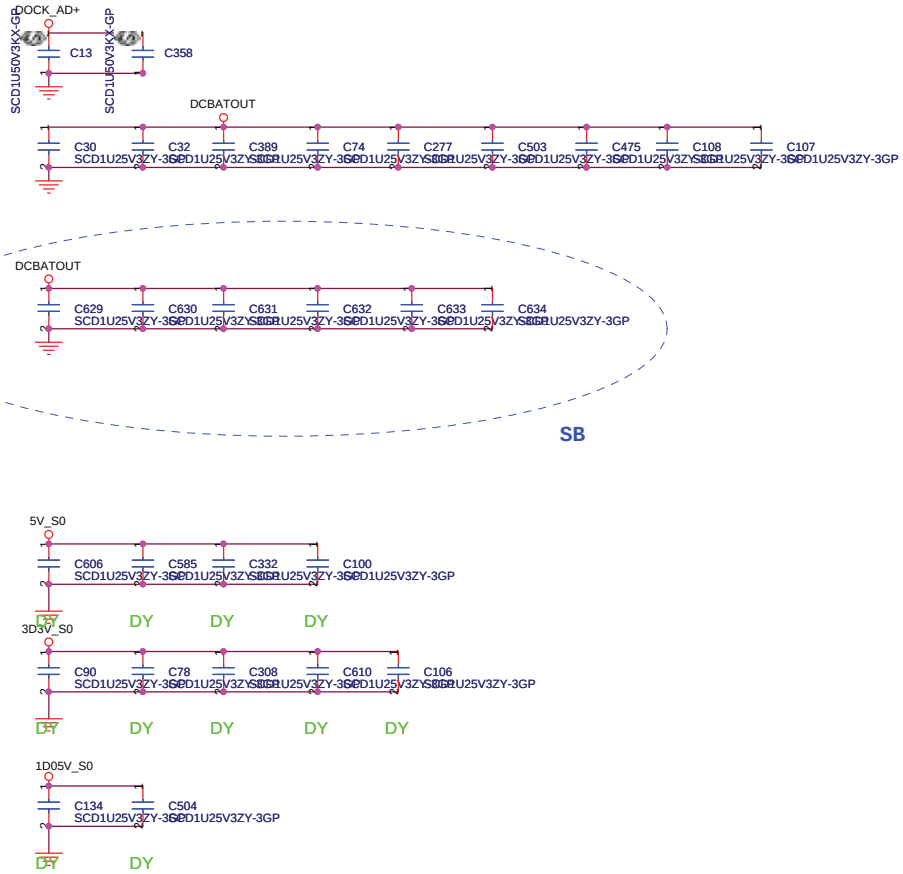

<Core Design>

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