ZH2 Block Diagram

PA@ PATA
SA@ SATA
MP@ MINI PCI
MC@ MINI CARD
GS@ G-SENSOR
G9@ 5789
G7@ 5787

CLOCK GEN
ICS954310BG
Page : 2

HOST 133MHz/166MHz
PCI-E 100MHz
VGA 96MHz
USB 48MHz
PCI 33MHz
REF 14MHz

X'TAL
14.318MHZ

Clock Generator
P2

Yonah/Merom
INTEL Mobile_479 CPU
Page : 3,4

CPU
Thermal Sensor
P5

HOST BUS
533/667
MHz

DDR2-SODIMM
Page : 12

Channel A

DDR2 533/667
MHz
Channel B

DDR2-SODIMM
Page : 12

CALISTOGA-GM
1466
FCBGA
Page : 6 ~ 11

SDVO
TVOUT
RGB
LVDS

DVI
Chrontel 7307
Page : 31

DVI

Docking
Page : 32

CRT Switch
SN74CBTLV3257PWR
Page : 18

CRT
Page : 18

LVDS
Page : 17

5V / 3.3V / 10V
Page : 34

+5VPCU
+3V_PCU
+3V_S5
+5V_S5
+3VSUS
+5VSUS
+3V
+5V
+10V

1.8V / 0.9V
/ 2.5V
Page : 35

+1.8VSUS
+1.8V
+0.9VSUS
+0.9V
+2.5V

1.5V / 1.05V
Page : 36

+1.5V
+1.05V

CPU CORE
Page : 33

VCC_CORE

BATTERY
CHARGER
Page : 37

USB3
BT
Page : 20

USB0,1,2
SYSTEM
ext
USB * 3
Page : 20

USB7
CCD
Page : 17

IDE - HDD
Page : 25

ATA 66/100

SATA - HDD
Page : 25

SATA

USB 2.0

DMI I/F

ICH7-M
652 BGA
Page : 13~16

PCI BUS
Azalia
PCI-E

X'TAL
32.768KHZ

X'TAL24.576MHZ

AD19 REQ2# / GNT2# INT C/D#

MINI PCI
Page :20

AD25 REQ0# / GNT0# INT E/F/G#

OSC
48MHZ

TI
PCMCIA+1394
+6 IN 1
PCI7412
Page :21~23

1394
Page: 21

PCMCIA
Page: 22

6 IN 1
Page: 23

LPC

X'TAL
32.768K

X'TAL
32.768K

G-SENSOR
KXP84-0200
Page : 25

NS
KBC(97551)
Page : 29

TPM 1.2

NS
SIO (87383)
Page : 27

Touchpad
Page : 30

Keyboard
Page : 30

FIR
Page : 27

COM

LPT

PS2

Docking
Page : 32

PCI-E CARD
/ WLAN

USB4

NEW CARD

USB5

X'TAL
25M

BROADCOM
10/100/1G LAN
5789M
Page : 19

LAN Switch
MAX4892
Page : 19

RJ45

DOCKING AUDIO

MDC 1.5
Page : 26

AUDIO CODEC
ALC883
Page : 26

AMP

MIC

ECHO
CANCELLATION
VP1020-G
Page : 26

LINEIN

HP
OUT

INT
SPK

AUDIO/B

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7412	AD25	REQ0# / GNT0#	INT E/F/G#
MINI PCI	AD19	REQ2# / GNT2#	INT C/D#

PROJECT : ZH2
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Monday, January 02, 2006 Sheet 1 of 38

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

Default

Close to IC <500mils

Place these termination to close CK410M.

CK-410M

25 mils

25 mils

REQ3 Latched Select
"0" : CLK Enable
"1" : CLK Disable Control : PCIE 2,4

REQ4 Latched Select
"0" : CLK Enable
"1" : CLK Disable
Control : PCIE
3,5,7

BSEL strappings need to be set for 533MHz Moby Dick (Intel?915GM - Calistoga Interposer)
(if Calistoga is designed for 667MHz board).

ITP/SRC7 SELECT
0: SRC7 1: ITP

SELLCD_27# Select. (Pin 17,18)
"0" : 27MHzSS/27MHzSS# pair
"1" : LCD CLK pair

Latched Select. (Pin 17,18)
"0" : LCD CLK
"1" : PCIEX CLK

modify C: del R375,R384

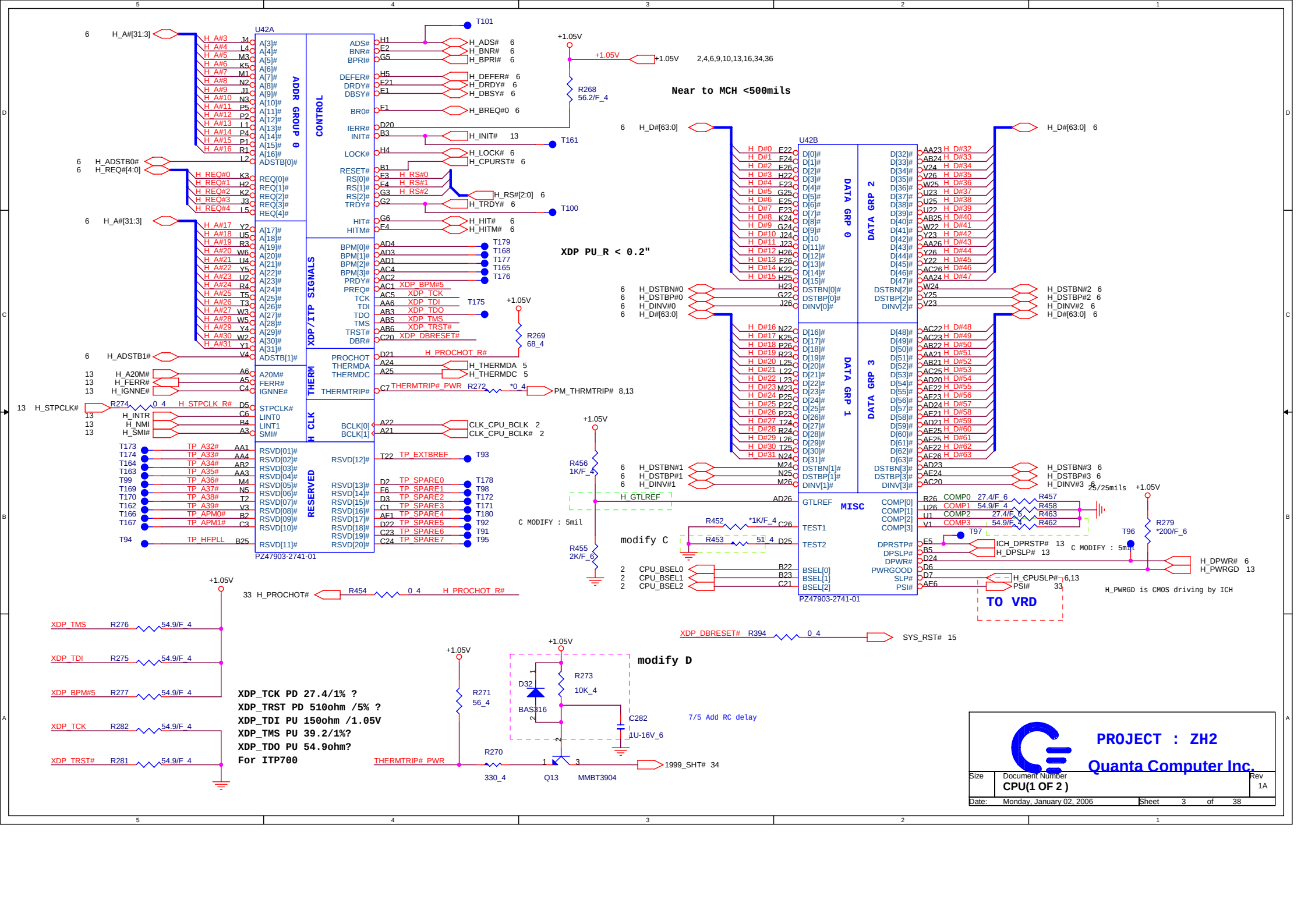
del R408

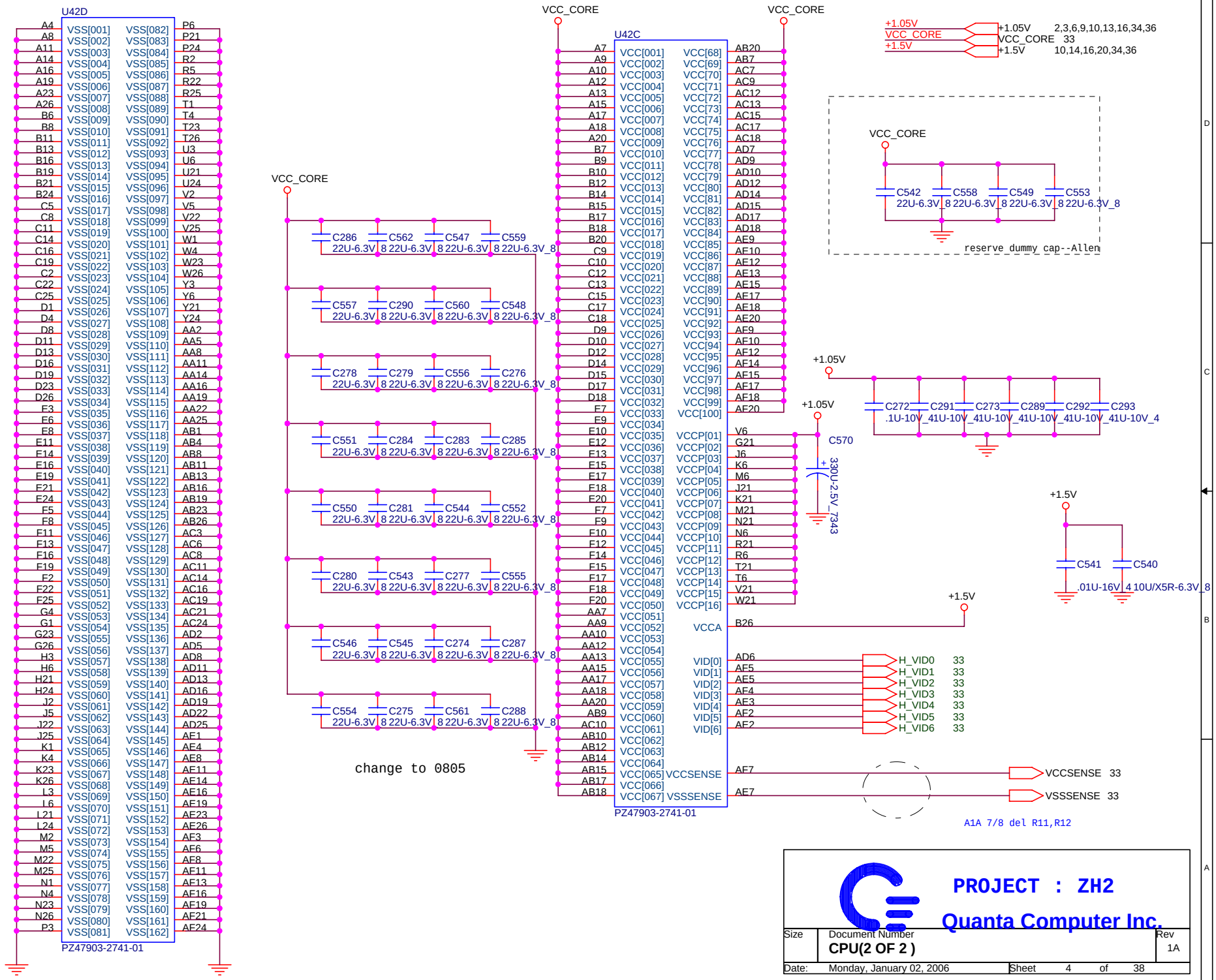
PROJECT : ZH2

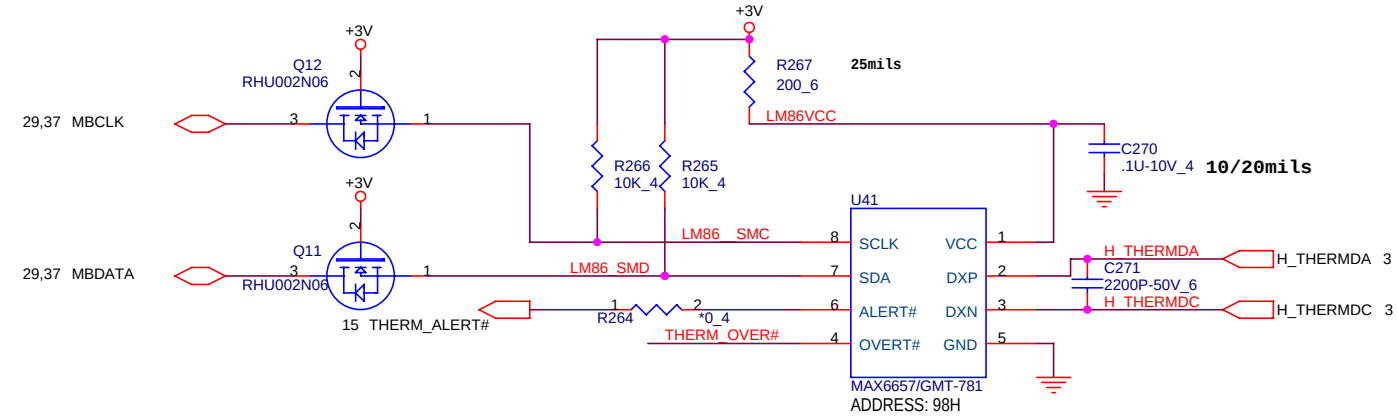
Quanta Computer Inc.

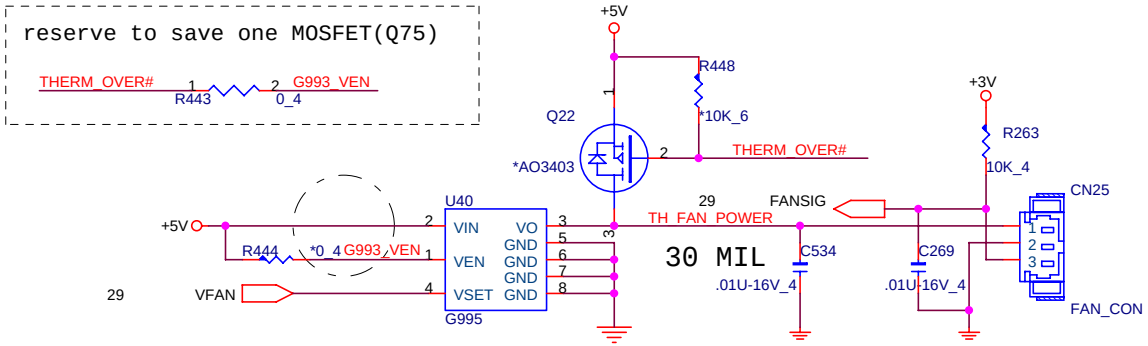
Size	Document Number	Rev
	CLOCK GENERATOR	1A

Date: Monday, January 02, 2006 Sheet 2 of 38

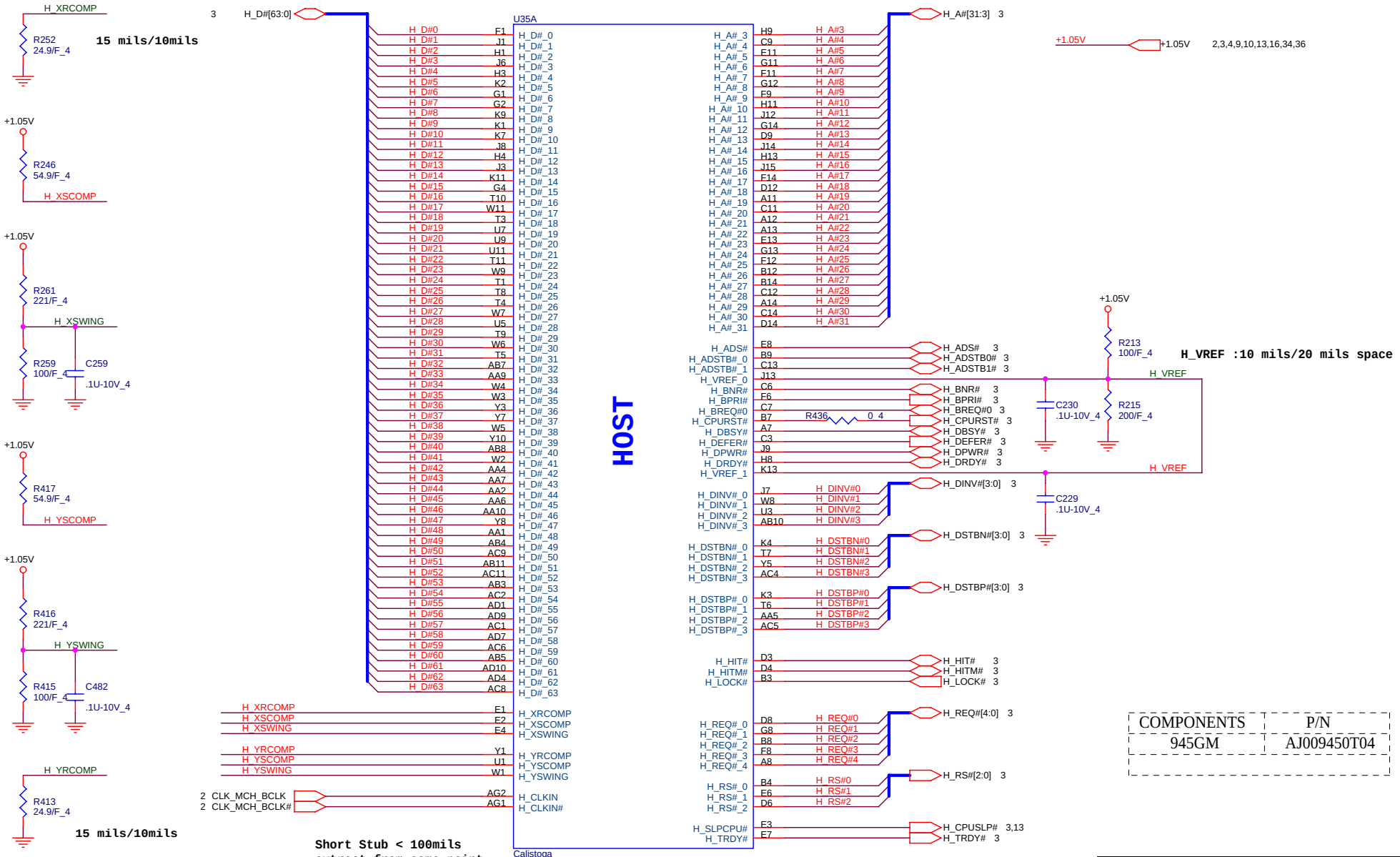

U42A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
PZ47903-2741-01
U42B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
PZ47903-2741-01
Near to MCH <500mils
XDP PU_R < 0.2"
modify C
modify D
C MODIFY : 5mil
C MODIFY : 5mil
H_PWRGD is CMOS driving by ICH
TO VRD
XDP_TCK PD 27.4/1% ?
XDP_TRST PD 510ohm /5% ?
XDP_TDI PU 150ohm /1.05V
XDP_TMS PU 39.2/1%?
XDP_TDO PU 54.9ohm?
For ITP700
7/5 Add RC delay
PROJECT : ZH2
Quanta Computer Inc.
CPU(1 OF 2)
Monday, January 02, 2006
Sheet 3 of 38
1A

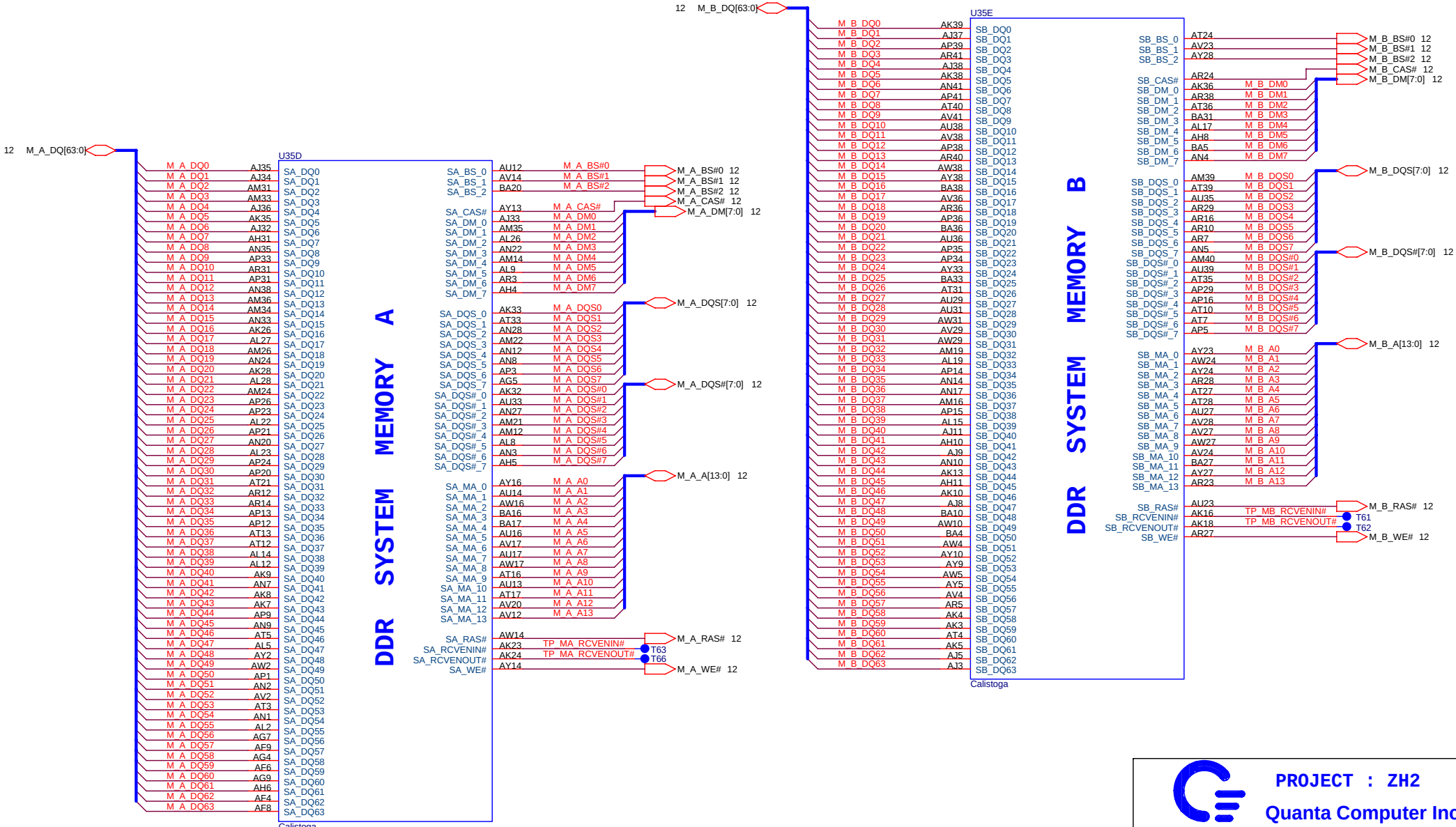

U42D
PZ47903-2741-01
U42C
PZ47903-2741-01
VCC_CORE
+1.05V
+1.5V
reserve_dummy cap--Allen
change to 0805
C570
330U-2.5V_7343
H_VID0 33
H_VID1 33
H_VID2 33
H_VID3 33
H_VID4 33
H_VID5 33
H_VID6 33
VCCSENSE 33
VSSSENSE 33
A1A 7/8 del R11,R12
PROJECT : ZH2
Quanta Computer Inc.
Size
Document Number
CPU(2 OF 2)
Rev
1A
Date: Monday, January 02, 2006
Sheet 4 of 38

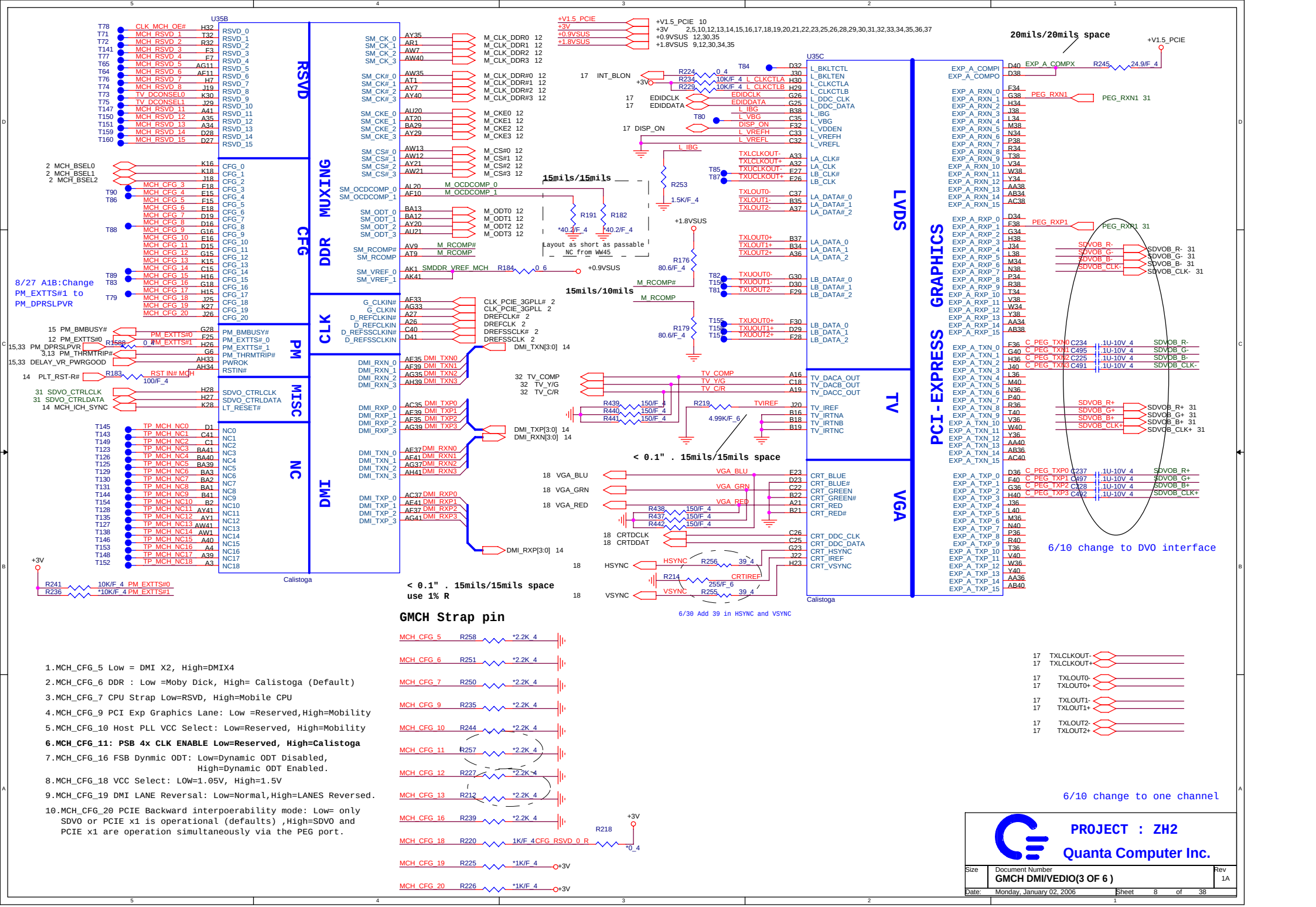


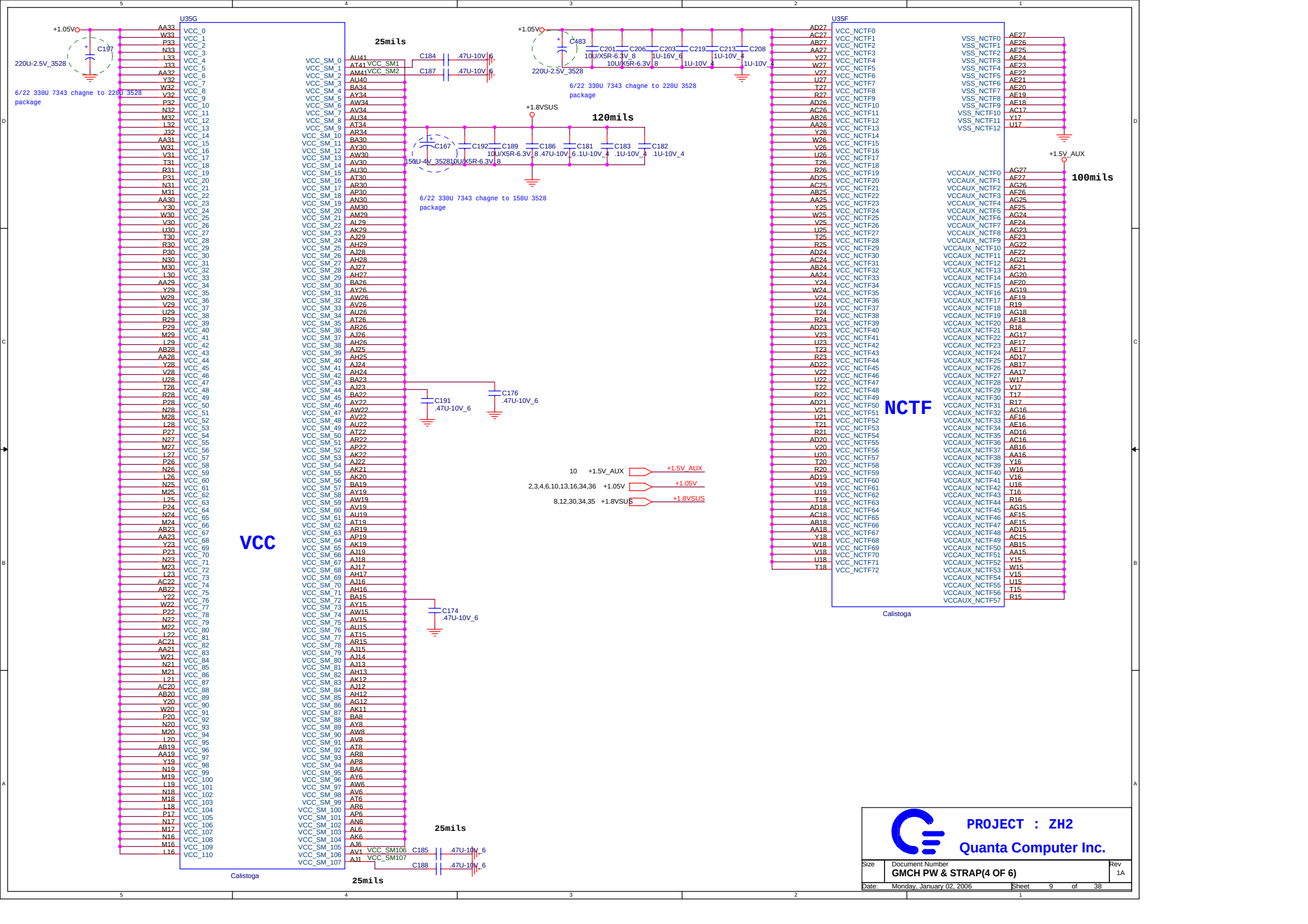


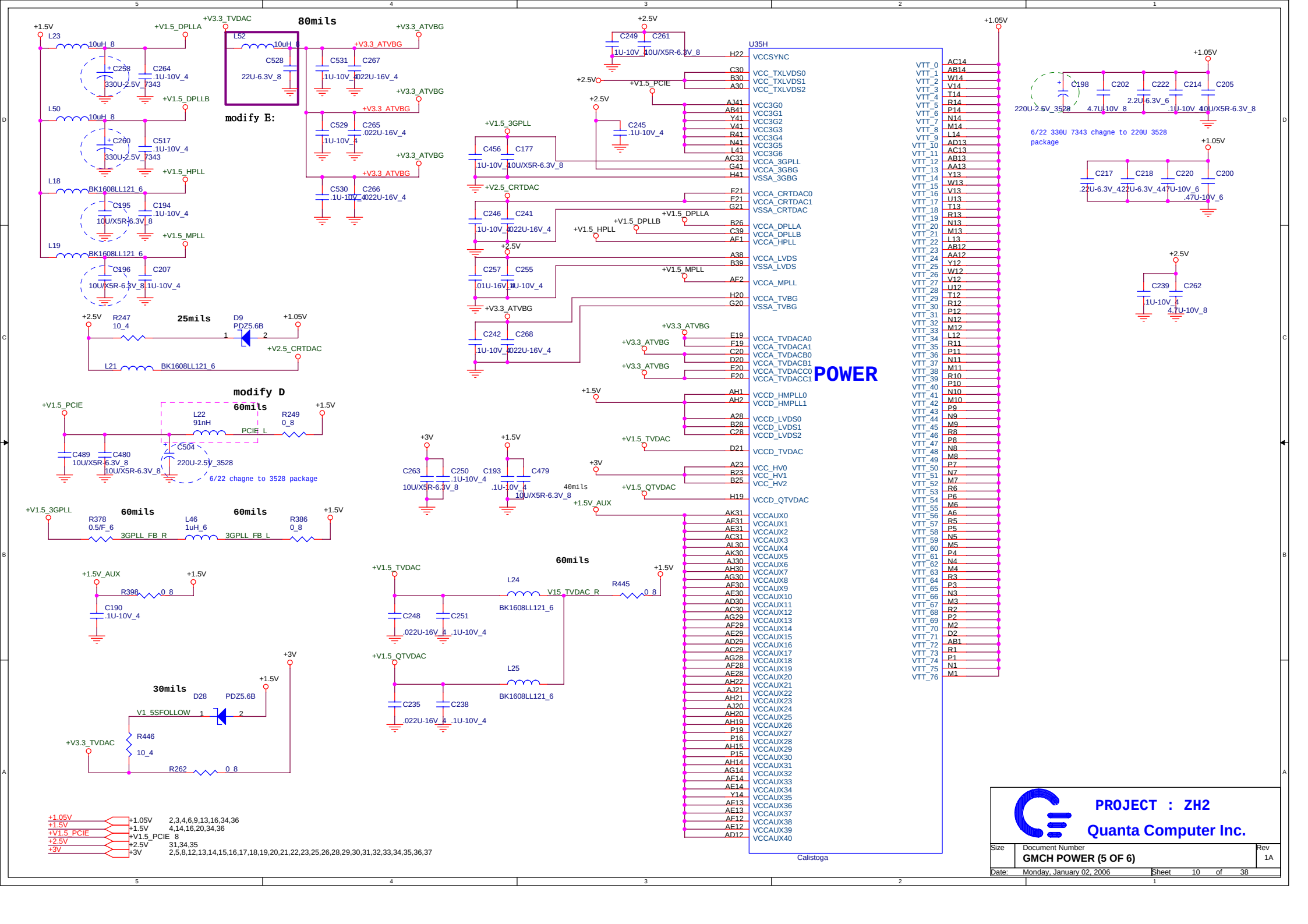
PROJECT : ZH2		
Quanta Computer Inc.		
Size	Document Number: Thermal Sensor LM86	Rev: 1A
Date: Monday, January 02, 2006	Sheet 5 of 38	

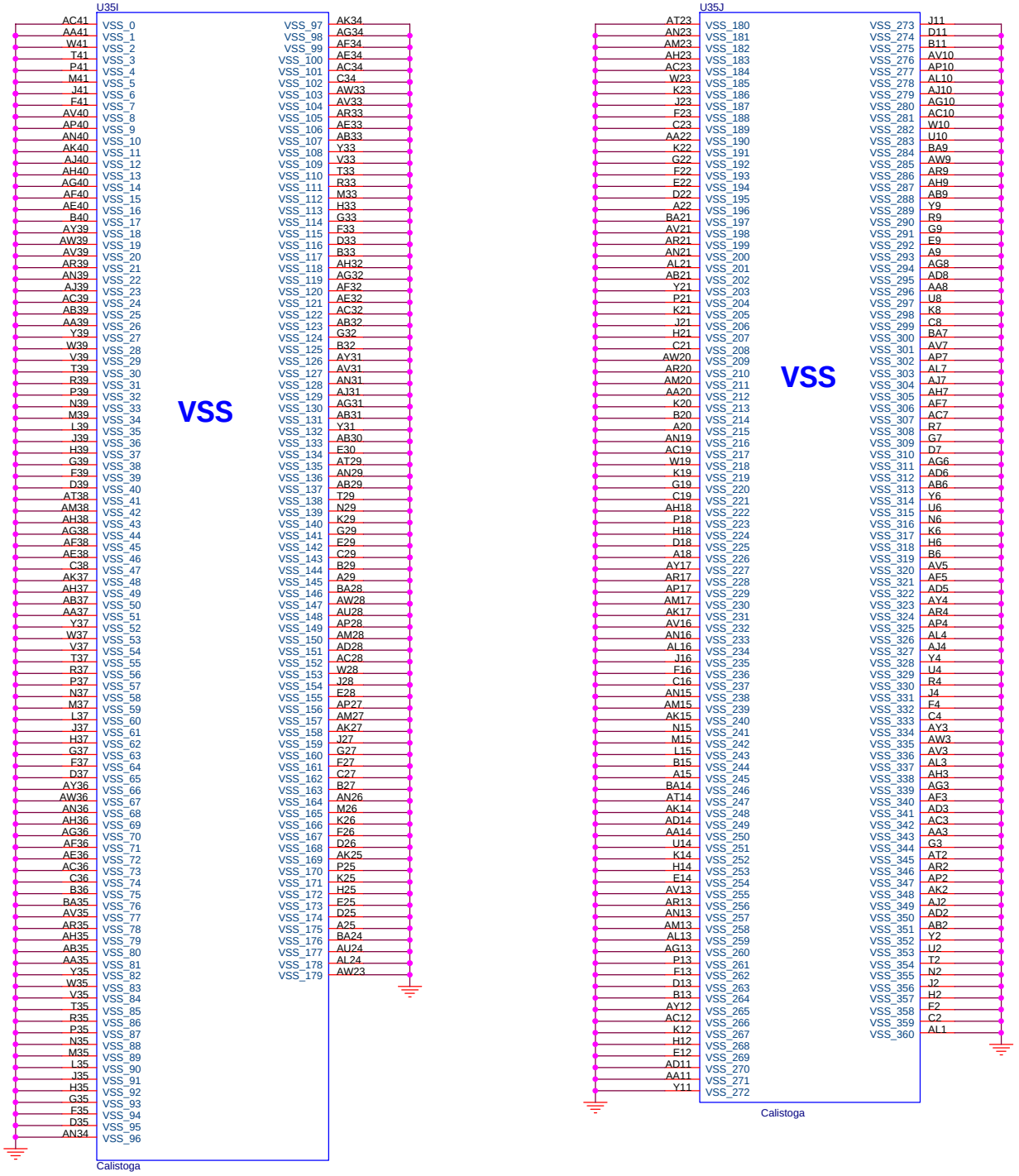

H_XRCOMP
R252
24.9/F_4
15 mils/10mils
+1.05V
R246
54.9/F_4
H_XSCOMP
+1.05V
R261
221/F_4
H_XSWING
R259
100/F_4
C259
.1U-10V_4
+1.05V
R417
54.9/F_4
H_YSCOMP
+1.05V
R416
221/F_4
H_YSWING
R415
100/F_4
C482
.1U-10V_4
H_YRCOMP
R413
24.9/F_4
15 mils/10mils
3 H_D#[63:0]
U35A
HOST
Calistoga
H_D#0 F1
H_D#1 J1
H_D#2 H1
H_D#3 J6
H_D#4 H3
H_D#5 K2
H_D#6 G1
H_D#7 G2
H_D#8 K9
H_D#9 K1
H_D#10 K7
H_D#11 J8
H_D#12 H4
H_D#13 J3
H_D#14 K11
H_D#15 G4
H_D#16 T10
H_D#17 W11
H_D#18 T3
H_D#19 U7
H_D#20 U9
H_D#21 U11
H_D#22 T11
H_D#23 W9
H_D#24 T1
H_D#25 T8
H_D#26 T4
H_D#27 W7
H_D#28 U5
H_D#29 T9
H_D#30 W6
H_D#31 T5
H_D#32 AB7
H_D#33 AA9
H_D#34 W4
H_D#35 W3
H_D#36 Y3
H_D#37 Y7
H_D#38 W5
H_D#39 Y10
H_D#40 AB8
H_D#41 W2
H_D#42 AA4
H_D#43 AA7
H_D#44 AA2
H_D#45 AA6
H_D#46 AA10
H_D#47 Y8
H_D#48 AA1
H_D#49 AB4
H_D#50 AC9
H_D#51 AB11
H_D#52 AC11
H_D#53 AB3
H_D#54 AC2
H_D#55 AD1
H_D#56 AD9
H_D#57 AC1
H_D#58 AD7
H_D#59 AC6
H_D#60 AB5
H_D#61 AD10
H_D#62 AD4
H_D#63 AC8
H_XRCOMP E1
H_XSCOMP E2
H_XSWING E4
H_YRCOMP Y1
H_YSCOMP U1
H_YSWING W1
2 CLK_MCH_BCLK AG2
2 CLK_MCH_BCLK# AG1
H_CLKIN
H_CLKIN#
Short Stub < 100mils
extract from same point
H_A#[31:3] 3
H_A#_3 H9
H_A#_4 C9
H_A#_5 E11
H_A#_6 G11
H_A#_7 F11
H_A#_8 G12
H_A#_9 F9
H_A#_10 H11
H_A#_11 J12
H_A#_12 G14
H_A#_13 D9
H_A#_14 J14
H_A#_15 H13
H_A#_16 J15
H_A#_17 F14
H_A#_18 D12
H_A#_19 A11
H_A#_20 C11
H_A#_21 A12
H_A#_22 A13
H_A#_23 E13
H_A#_24 G13
H_A#_25 F12
H_A#_26 B12
H_A#_27 B14
H_A#_28 C12
H_A#_29 A14
H_A#_30 C14
H_A#_31 D14
H_A#3
H_A#4
H_A#5
H_A#6
H_A#7
H_A#8
H_A#9
H_A#10
H_A#11
H_A#12
H_A#13
H_A#14
H_A#15
H_A#16
H_A#17
H_A#18
H_A#19
H_A#20
H_A#21
H_A#22
H_A#23
H_A#24
H_A#25
H_A#26
H_A#27
H_A#28
H_A#29
H_A#30
H_A#31
+1.05V
+1.05V 2,3,4,9,10,13,16,34,36
H_ADS# E8
H_ADSTB#_0 B9
H_ADSTB#_1 C13
H_VREF_0 J13
H_BNR# C6
H_BPRI# F6
H_BREQ#0 C7
H_CPURST# B7
H_DBSY# A7
H_DEFER# C3
H_DPWR# J9
H_DRDY# H8
H_VREF_1 K13
H_ADS# 3
H_ADSTB0# 3
H_ADSTB1# 3
H_BNR# 3
H_BPRI# 3
H_BREQ#0 3
H_CPURST# 3
H_DBSY# 3
H_DEFER# 3
H_DPWR# 3
H_DRDY# 3
R436 0_4
+1.05V
R213
100/F_4
H_VREF
C230
.1U-10V_4
R215
200/F_4
H_VREF
C229
.1U-10V_4
H_VREF :10 mils/20 mils space
H_DINV#_0 J7
H_DINV#_1 W8
H_DINV#_2 U3
H_DINV#_3 AB10
H_DINV#0
H_DINV#1
H_DINV#2
H_DINV#3
H_DINV#[3:0] 3
H_DSTBN#_0 K4
H_DSTBN#_1 T7
H_DSTBN#_2 Y5
H_DSTBN#_3 AC4
H_DSTBN#0
H_DSTBN#1
H_DSTBN#2
H_DSTBN#3
H_DSTBN#[3:0] 3
H_DSTBP#_0 K3
H_DSTBP#_1 T6
H_DSTBP#_2 AA5
H_DSTBP#_3 AC5
H_DSTBP#0
H_DSTBP#1
H_DSTBP#2
H_DSTBP#3
H_DSTBP#[3:0] 3
H_HIT# D3
H_HITM# D4
H_LOCK# B3
H_HIT# 3
H_HITM# 3
H_LOCK# 3
H_REQ#_0 D8
H_REQ#_1 G8
H_REQ#_2 B8
H_REQ#_3 F8
H_REQ#_4 A8
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
H_REQ#[4:0] 3
H_RS#_0 B4
H_RS#_1 E6
H_RS#_2 D6
H_RS#0
H_RS#1
H_RS#2
H_RS#[2:0] 3
H_SLPCPU# E3
H_TRDY# E7
H_CPUSLP# 3,13
H_TRDY# 3
COMPONENTS
945GM
P/N
AJ009450T04
PROJECT : ZH2
Quanta Computer Inc.
Size
Document Number
GMCH HOST(1 OF 6)
Rev
1A
Date: Monday, January 02, 2006
Sheet 6 of 38


12 M_A_DQ[63:0]
U35D
DDR SYSTEM MEMORY A
Calistoga
12 M_B_DQ[63:0]
U35E
DDR SYSTEM MEMORY B
Calistoga
PROJECT : ZH2
Quanta Computer Inc.
Size
Document Number
GMCH DDR(2 OF 6)
Rev
1A
Date: Monday, January 02, 2006
Sheet 7 of 38


U35B
RSVD
CFG
DDR MUXING
CLK
PM
MISC
NC
DMI
Calistoga
8/27 A1B:Change PM_EXTTS#1 to PM_DPRSLPVR
15mils/15mils
15mils/10mils
Layout as short as passable
NC from WW45
< 0.1" . 15mils/15mils space
use 1% R
< 0.1" . 15mils/15mils space
20mils/20mils space
U35C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
6/10 change to DVO interface
6/30 Add 39 in HSYNC and VSYNC
6/10 change to one channel
GMCH Strap pin
1.MCH_CFG_5 Low = DMI X2, High=DMIX4
2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6.MCH_CFG_11: PSB 4x CLK ENABLE Low=Reserved, High=Calistoga
7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
9.MCH_CFG_19 DMI LANE Reversal: Low=Normal,High=LANES Reversed.
10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.
PROJECT : ZH2
Quanta Computer Inc.
Size
Document Number
GMCH DMI/VEDIO(3 OF 6)
Rev
1A
Date: Monday, January 02, 2006
Sheet 8 of 38

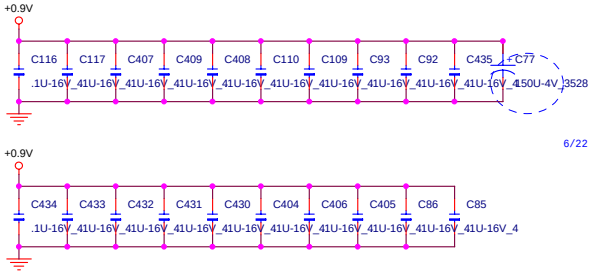

U35G
VCC
Calistoga
U35F
NCTF
Calistoga
+1.05V
C197
220U-2.5V_3528
6/22 330U 7343 chagne to 220U 3528 package
C483
C201
C206
C203
C219
C213
C208
10U/X5R-6.3V_8
1U-16V_6
1U-10V_4
6/22 330U 7343 chagne to 220U 3528 package
+1.8VSUS
120mils
C167
150U-4V_3528
C192
C189
C186
C181
C183
C182
10U/X5R-6.3V_8
.47U-10V_6
.1U-10V_4
6/22 330U 7343 chagne to 150U 3528 package
25mils
C184
C187
.47U-10V_6
C191
C176
C174
C185
C188
VCC_SM106
VCC_SM107
10 +1.5V_AUX
2,3,4,6,10,13,16,34,36 +1.05V
8,12,30,34,35 +1.8VSUS
+1.5V_AUX
+1.05V
+1.8VSUS
+1.5V_AUX
100mils
PROJECT : ZH2
Quanta Computer Inc.
Size
Document Number
GMCH PW & STRAP(4 OF 6)
Rev
1A
Date: Monday, January 02, 2006
Sheet 9 of 38


80mils
modify E:
25mils
modify D
60mils
30mils
40mils
POWER
U35H
Calistoga
PROJECT : ZH2
Quanta Computer Inc.
GMCH POWER (5 OF 6)
Monday, January 02, 2006
Sheet 10 of 38
6/22 330U 7343 chagne to 220U 3528 package
6/22 chagne to 3528 package

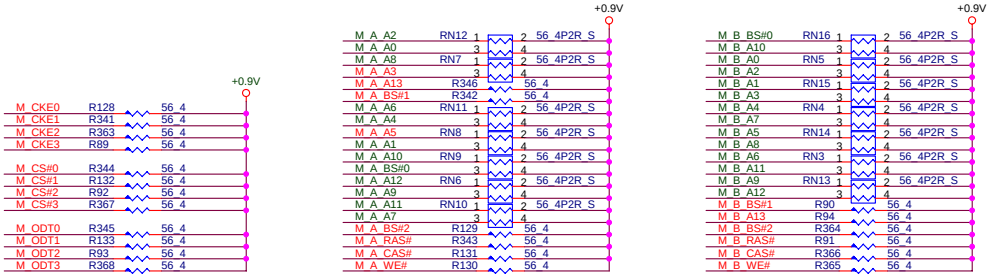


PROJECT : ZH2		
Quanta Computer Inc.		
Size	Document Number: GMCH GND(6 OF 6)	Rev: 1A
Date: Monday, January 02, 2006	Sheet 11 of 38	

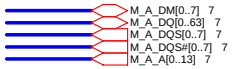
TERMINATOR DECOUPLING CAPACITOR

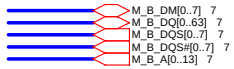


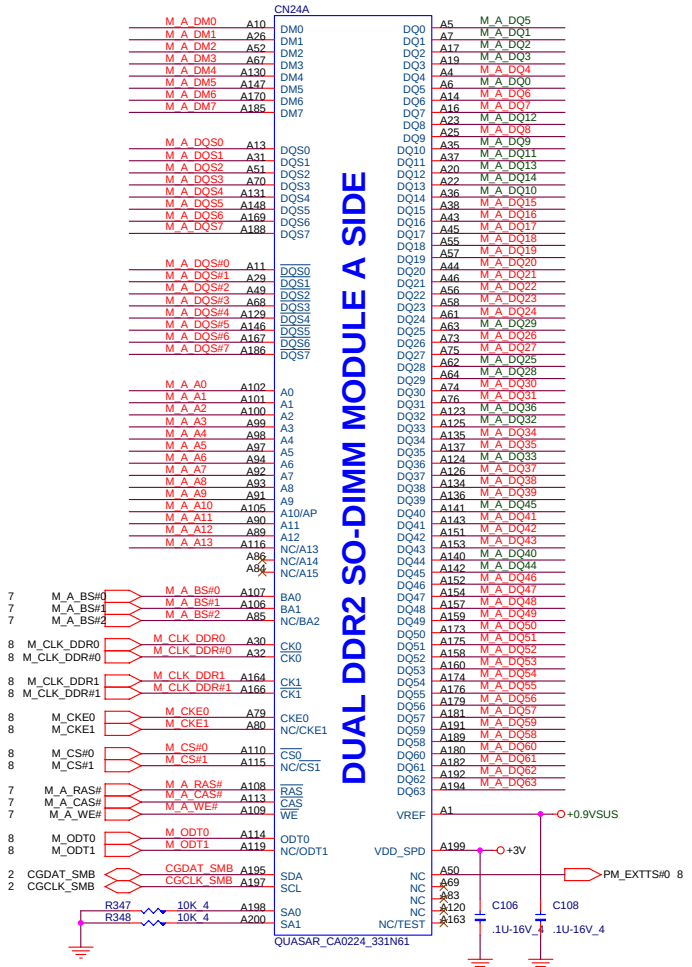
DDR2 TERMINATOR

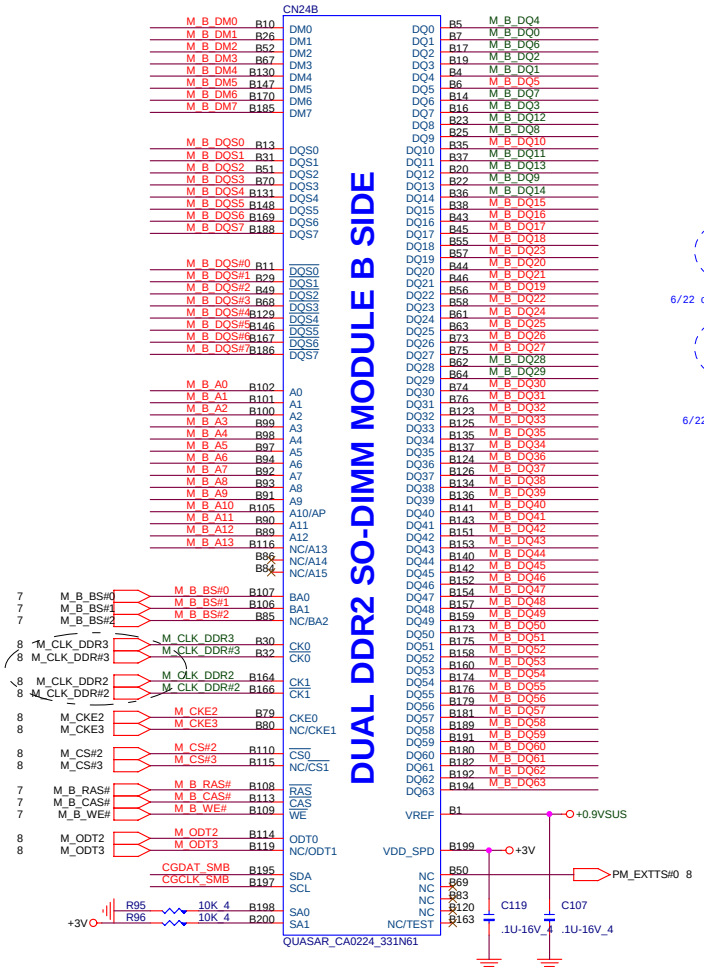


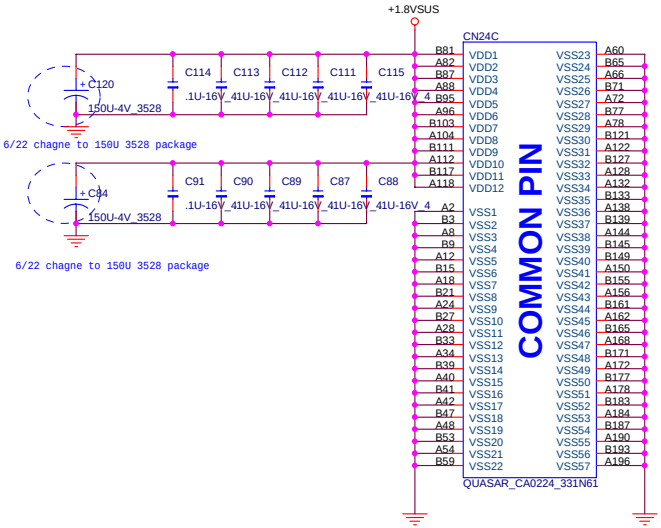
DDR2 SO-DIMM SOCKET

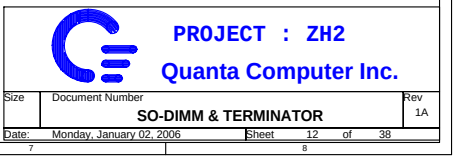


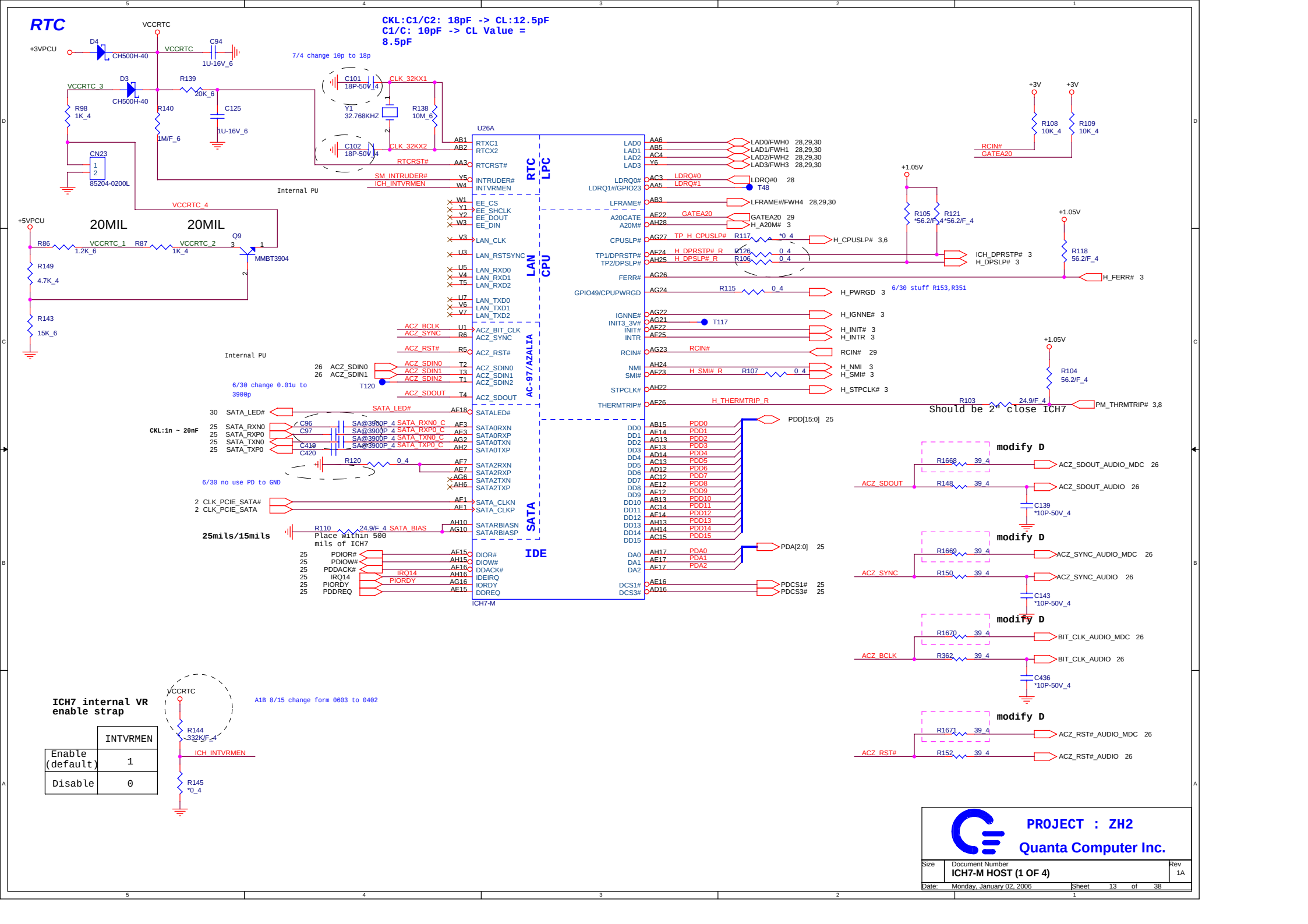











RTC
CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
7/4 change 10p to 18p
U26A
RTC
LPC
LAN
CPU
AC-97/AZALIA
SATA
IDE
ICH7-M
Internal PU
20MIL
20MIL
6/30 change 0.01u to 3900p
6/30 no use PD to GND
25mils/15mils
Place within 500 mils of ICH7
6/30 stuff R153,R351
Should be 2" close ICH7
modify D
ICH7 internal VR enable strap
A1B 8/15 change form 0603 to 0402
PROJECT : ZH2
Quanta Computer Inc.
ICH7-M HOST (1 OF 4)
Monday, January 02, 2006

modify C

MINI CARD PCI-E

5789M

EZ4

EZ4

A1A 8/1 chagne PCI-E signal for different SB use

Place within 500 mils of ICH7

15/15mils

Sys

Sys

Sys

Bluetooth Module

Mini PCI-E modify C

CCD

25mils/15mils

Place within 500 mils of ICH7

modify D

modify D

CKL use 10Kohm

ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7411	AD25	REQ0# / GNT0#	INT E/F/G#

Don't connect to PCI device / Express card

PROJECT : ZH2

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M PCI E (2 OF 4)	1A

Date: Monday, January 02, 2006 Sheet 14 of 38

7/4 change 2.2 to 2.2K

PCLK_SMB R168 2.2K_4
PDAT_SMB R169 2.2K_4
PCIE_WAKE# R159 1K_4

RI# R397 10K_4
SMB_LINK_ALERT# R390 10K_4
SMLINK0 R401 10K_4
SMLINK1 R391 10K_4
EXTSMI# R R404 10K_4
SMB_ALERT# R392 10K_4

DNBSWON# R403 10K_4
SYS_RST# R393 10K_4
PM_BATLOW# R R162 10K_4

CLKRUN# R116 8.2K_4
SERIRQ R101 8.2K_4
RUNTIME_SCI# R R125 10K_4

RSMRST# R141 10K_4

to Clock Gen & DIMM

6/30 no use PU to 3V

R389 *1K/F_4

26 ACZ_SPKR

2,19,20,32 PCLK_SMB
2,19,20,32 PDAT_SMB
T134 T139 T136
21 RI#
21,28,30 LPC_PD#
3 SYS_RST#
R395 *10K_4
R134 0_4
8 PM_BMBUSY#
R114 *10K/F_4
R119 *10K/F_4
No ASF support
2 PM_STPPCI#
2 PM_STPCPU#
R122 0_4
R113 0_4
T132
T137 PAD
T133
T56

U26C

PCLK_SMB C22
PDAT_SMB B22
SMB_LINK_ALERT# A26
SMLINK0 B25
SMLINK1 A25
RI# A28
LPC_PD# A19
SYS_RST# A27
A22
AB18
SMB_ALERT# B23
PM_STPPCI_ICH# AC20
PM_STPCPU_ICH# AF21
A21
B21
E23
CLKRUN# AG18
AC19
U2
PCIE_WAKE# F20
SERIRQ AH21
AF20
VR_PWRGD_CK410 AD22
AC21
AC18
E21

SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
GPIO11/SMBALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8

SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO

GPIO21/SATA0GP AF19
GPIO19/SATA1GP AH18
GPIO36/SATA2GP AH19
GPIO37/SATA3GP AE19
CLK14 AC1
CLK48 B2
SUSCLK C20
SLP_S3# B24
SLP_S4# D23
SLP_S5# F22
PWROK AA4
GPIO16/DPRSLPVR AC22
TP0/BATLOW# C21
PWRBTN# C23
LAN_RST# C19
RSMRST# Y4
GPIO9 E20
GPIO10 A20
GPIO12 E19
GPIO13 E19
GPIO14 R4
GPIO15 E22
GPIO24 R3
GPIO25 D20
GPIO35 AD21
GPIO38 AD20
GPIO39 AE20

ICH7-M

R354 *8.2K_4
R353 33_4
14M_ICH 2
CLKUSB_48 2
PAD T59
R402 100/F_4
R174 100/F_4
SUSB# 21,29
SUSC# 21,29
PAD T54
ICH_PWROK
PM_DPRSLPVR 8,33
PM_BATLOW# R
DNBSWON# 29
R172 *100K_4
R171 0_4
PLTRST# 14,19,20,25,28,29,30,31,32
PM_RSMRST# R
R142 100/F_4 RSMRST#
RSMRST# 29
LOW_G_INT 25,29
HIGHT_G_INT 25,29
EMAIL_LED# 30
LID591# 17,29,37
DOCKIN# 19,26,32
BOARD_ID1
BOARD_ID0
T45
T44
T43

CKL :100Kohm PD

6/30 change RSMRST# to PLTRST#

A1A add G-sense control pin

GPIO25 /Suspend rail is a HW strap , don't pull down .

Note: Connect to EC; Reserve PH/3V

25,21,28,29,30 CLKRUN#
R97 10K/F_4
19,20 PCIE_WAKE#
20,21,28,29,30 SERIRQ
5 THERM_ALERT#
R123 10K_4
18 CRT_SENSE#
29 SCI#
29 KBSMI#
R124 0_4
R396 0_4
RUNTIME_SCI# R
EXTSMI# R

R178 *10K_4
BOARD_ID0
R177 10K_4

R147 *10K_4
BOARD_ID1
R146 10K_4

Board ID	ID1	ID0	
00			PATA,PCMCIA
01			PATA,NEW
10			SATA,PCMCIA
11			PATA,NEW

+3VSUS
C429 .022U-16V_4
U25
8,33 DELAY_VR_PWRGOOD
29 PWROK_EC
ICH_PWROK
TC7SH08FU
R361 10K_4

A1A:Change to inverter for VR_PWRGD_CK410

R127 100K_4
U3
VR_PWRGD_CK410
VR_PWRGD_CK410# 2,33
SN74LVC1G04DCKR

Note: External pull-up 3V

CLKUSB_48
R387 10_4
C467 10P-50V_4
14M_ICH
R136 *33_4
C128 *10P-50V_4

modify D

PROJECT : ZH2

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M GPIO (3 OF 4)	1A
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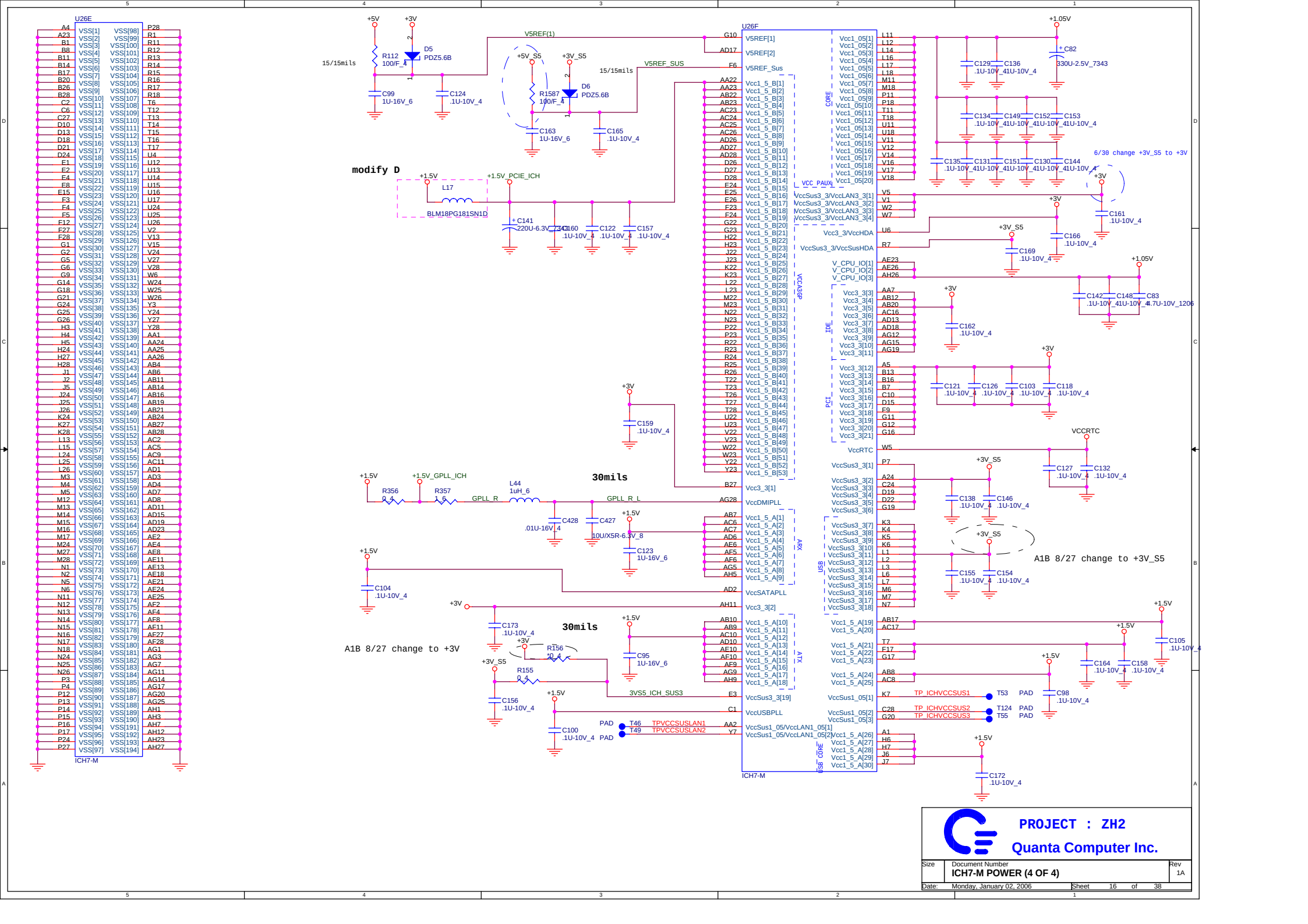
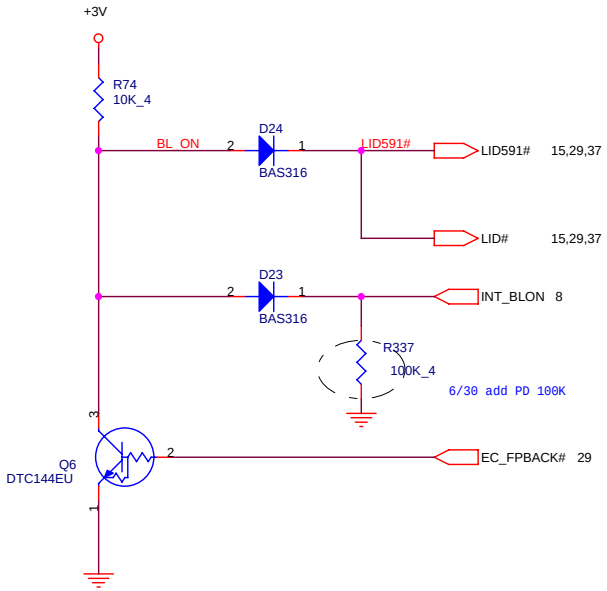
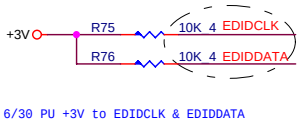
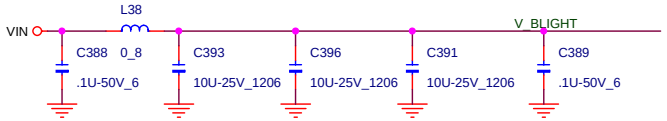
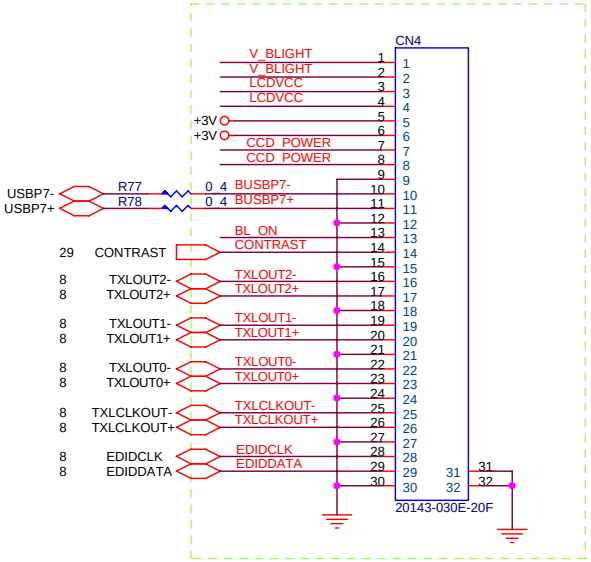
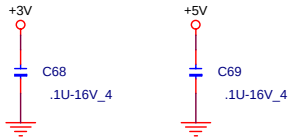

U26E
ICH7-M
U26F
ICH7-M
modify D
L17
BLM18PG181SN1D
30mils
30mils
A1B 8/27 change to +3V
A1B 8/27 change to +3V_S5
6/30 change +3V_S5 to +3V
PROJECT : ZH2
Quanta Computer Inc.
ICH7-M POWER (4 OF 4)
Monday, January 02, 2006
Sheet 16 of 38



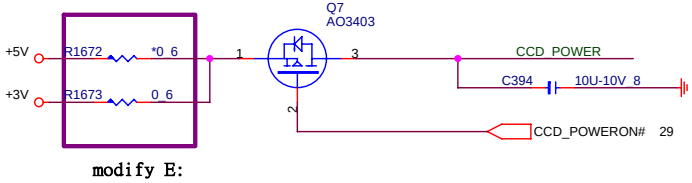






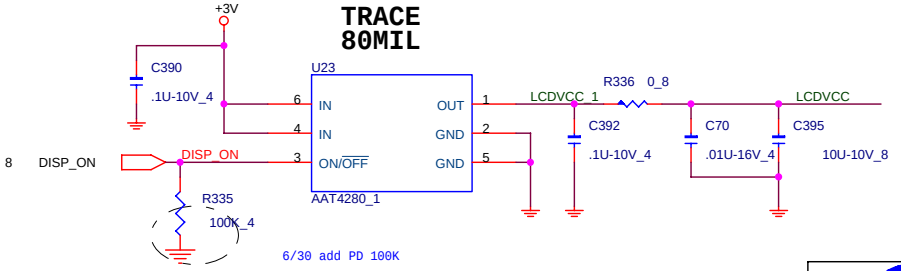


CAMERA MODULE CONNECTOR



modify E:

TRACE 80MIL



PROJECT : ZH2

Quanta Computer Inc.

Size	Document Number	Rev
	LVDS CONNECTOR	1A
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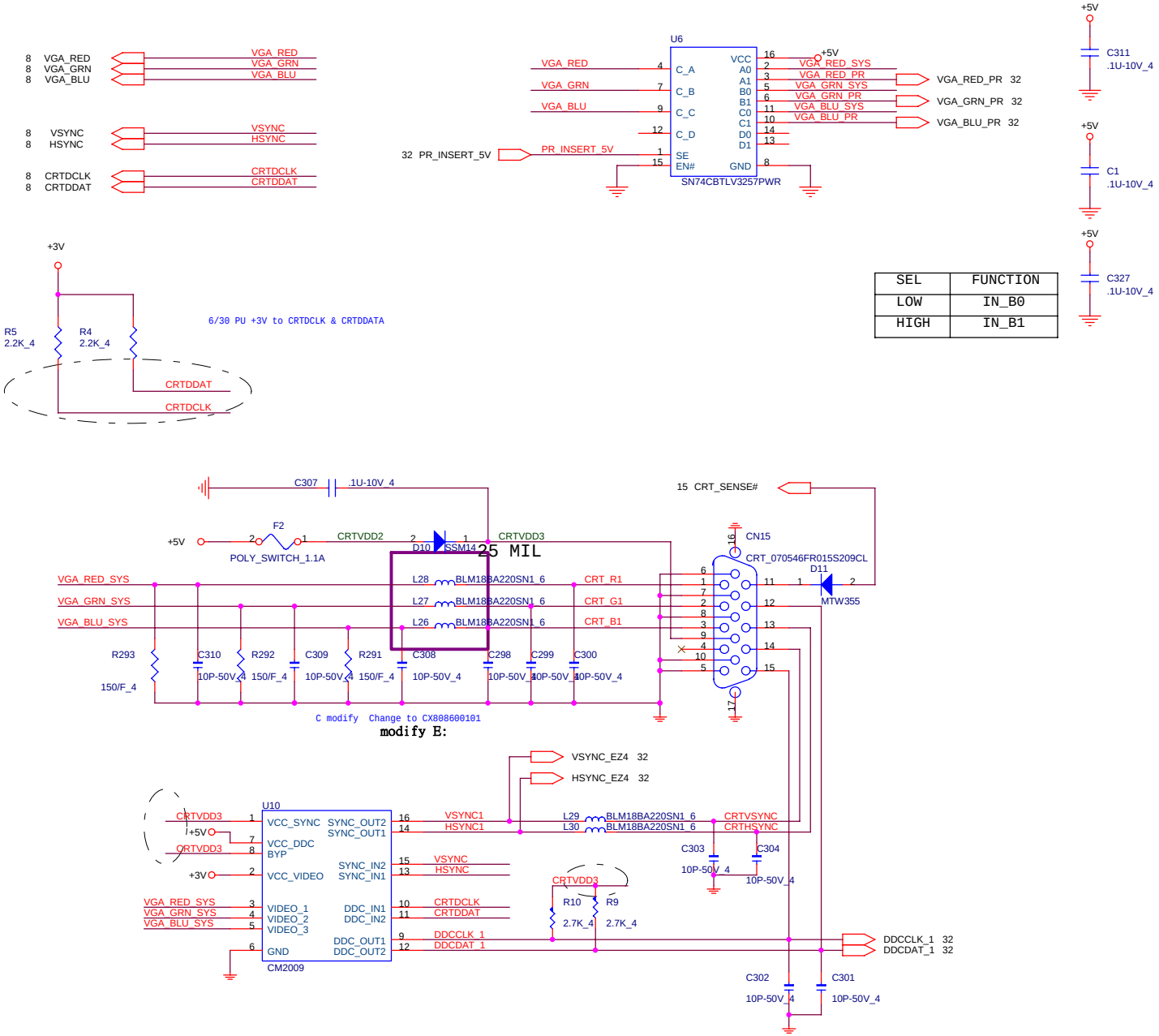

PROJECT : ZH2

Quanta Computer Inc.

Size	Document Number	Rev
	CRT-PORT	1A

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G9@ 5789
G7@ 5789

U14
BCM5789M
15mm x 15mm
BGA196

modify D
modify B:
A1A 7/8 Add Diode to separate
A1A 7/8 change 1.18K to 1.24K Default
A1A 7/8 change to .1u
A1B 8/27 FIX led issue
5787 internal pull up
REV:B MODIFY P/N

SEL	CONNECTION
0	Ax to xB1 : LEDx to xLED1
1	Ax to xB2 : LEDx to xLED2

PROJECT : ZH2
Quanta Computer Inc.
BCM 5789
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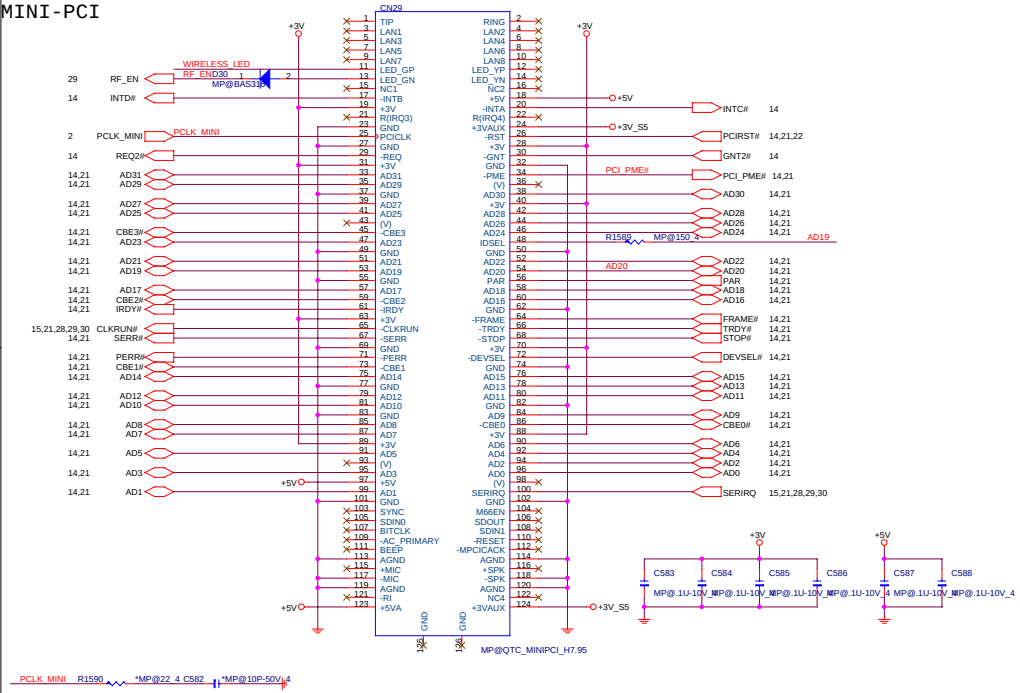
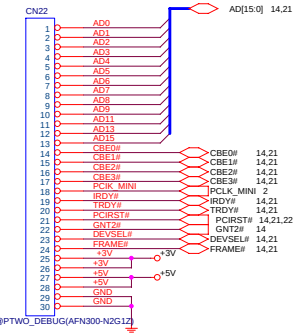
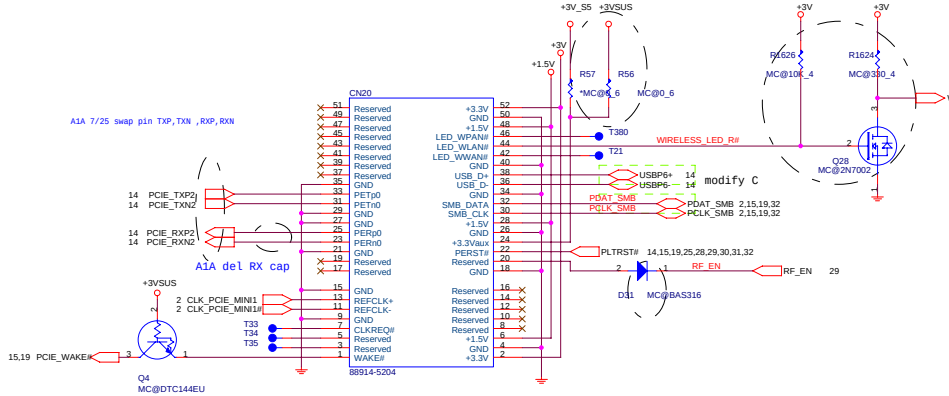
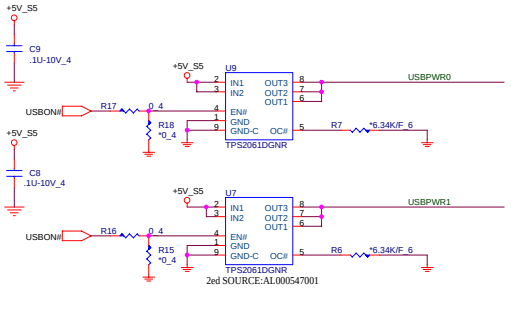
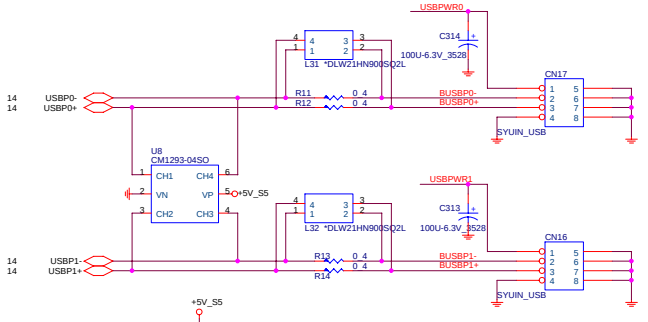
MINI-PCI

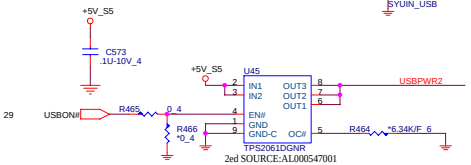


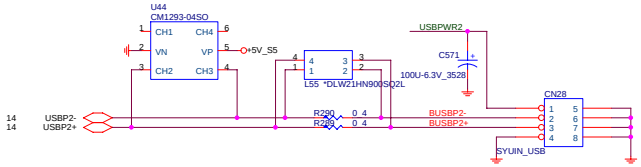




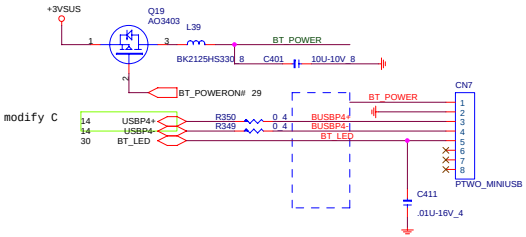








BLUETOOTH MODULE CONNECTOR



PROJECT : ZH2		
Quanta Computer Inc.		
Size	Document Number: MINI PCI,USB	Rev: 1A
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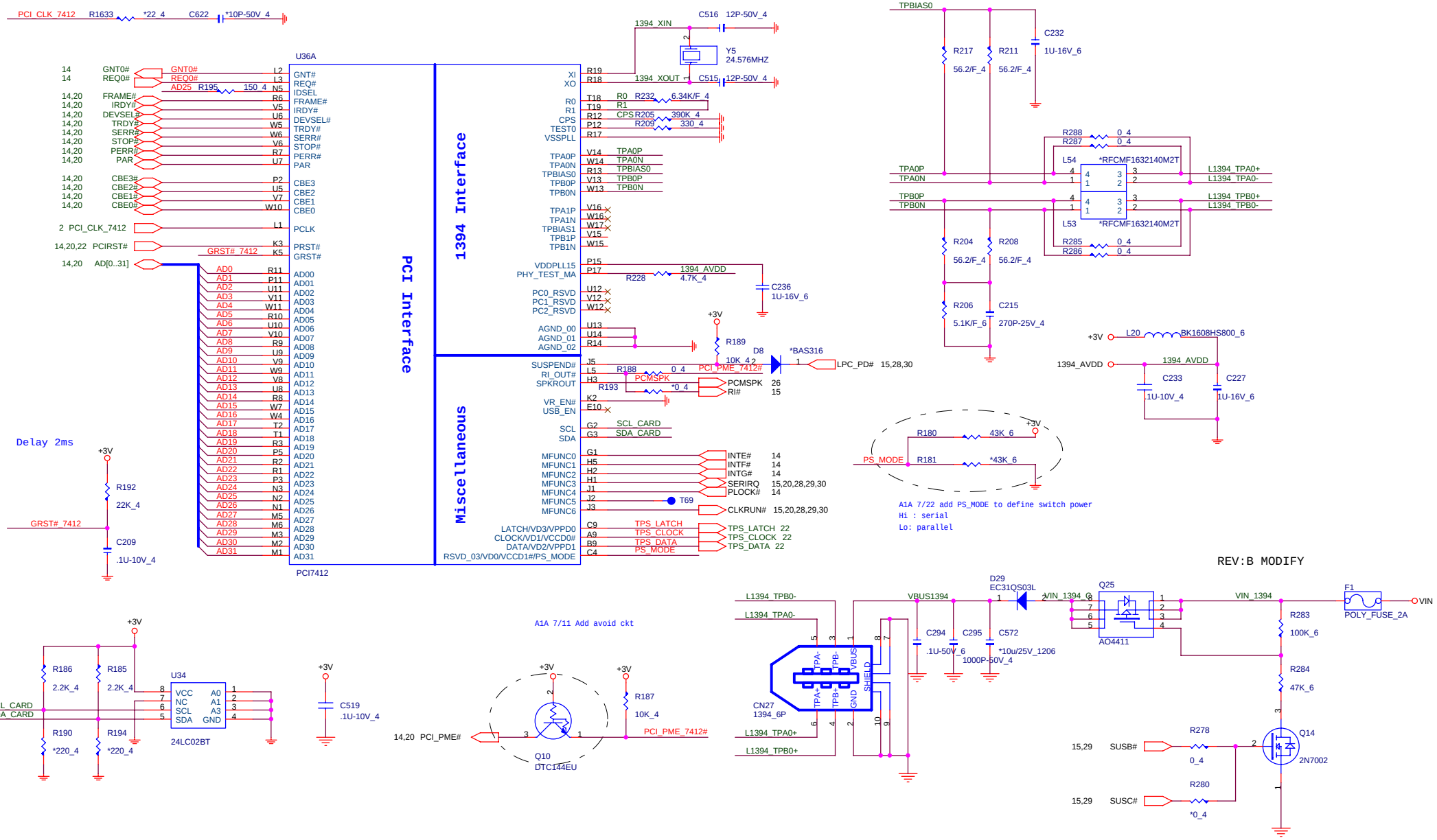

PROJECT : ZH2

Quanta Computer Inc.

Size	Document Number	Rev
	PCI7412-IEEE1394	1A
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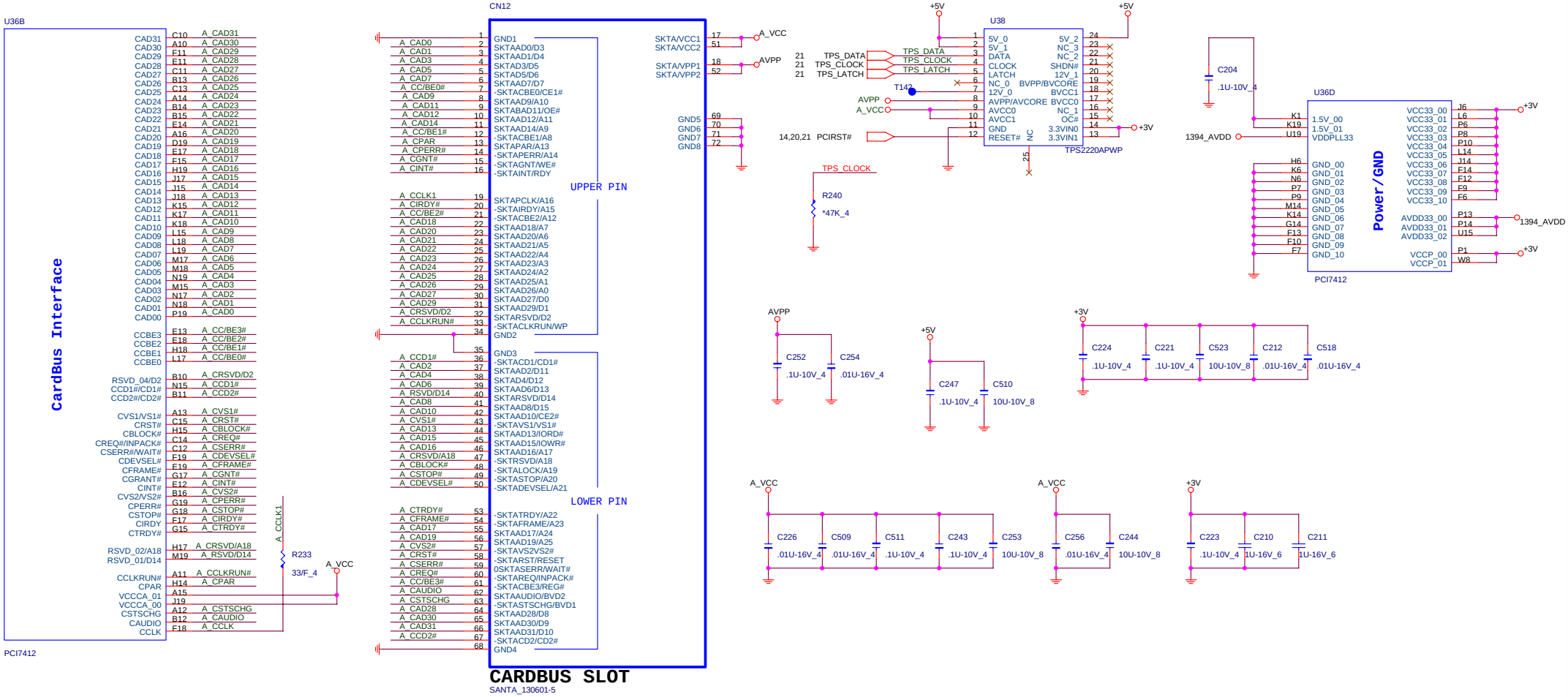

Quanta Computer Inc.	PROJECT : ZH2	
Size	Document Number: PCI7412-PCMCIA	Rev: 1A
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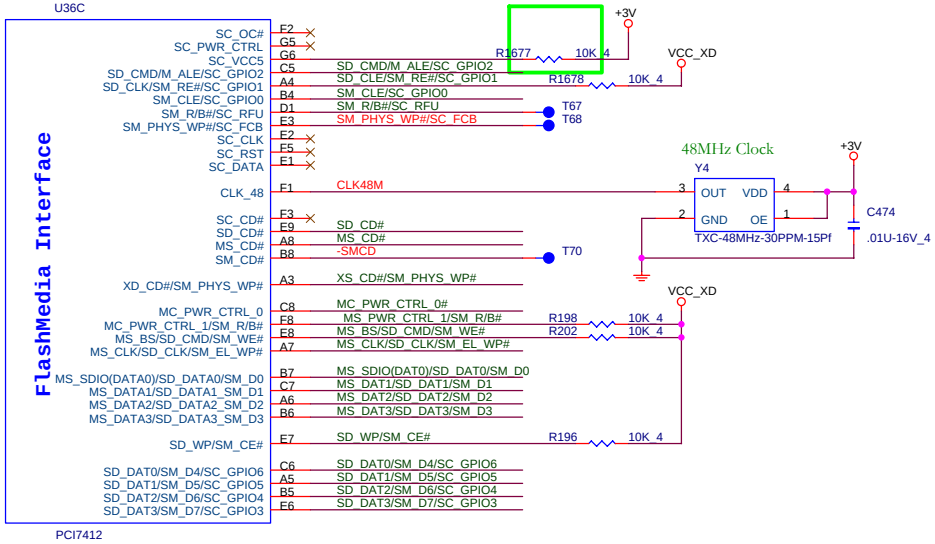
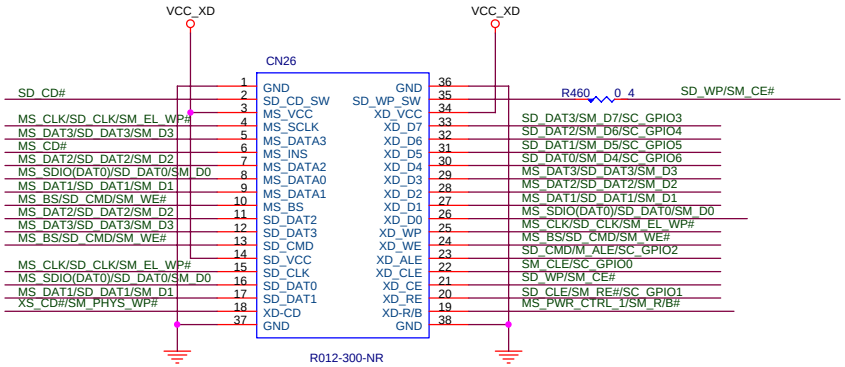
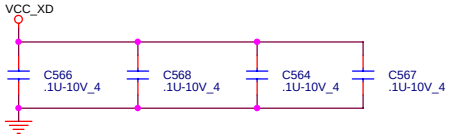
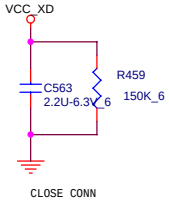
modify F:

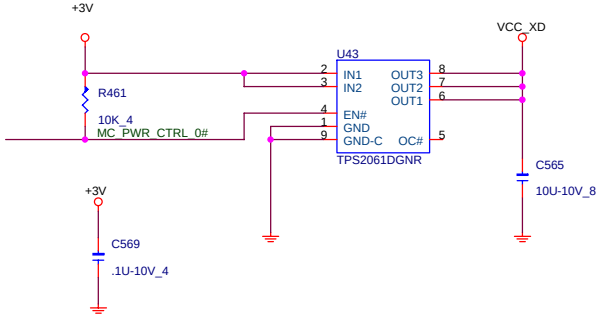


4 IN 1 CARD READER(SD/MMC/MS/MS Pro)





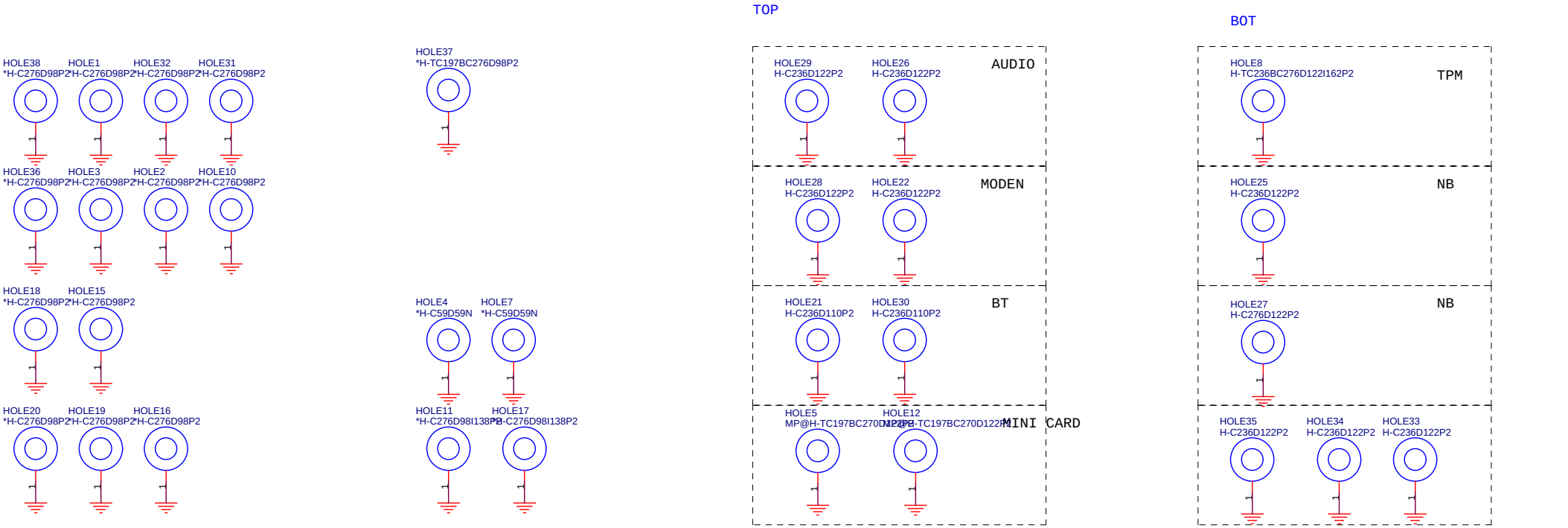




PROJECT : ZH2

Quanta Computer Inc.

Size	Document Number	Rev
	PCI7412-CARD READER	1A
Date: Monday, January 02, 2006	Sheet 23 of 38	



PROJECT : ZH2

Quanta Computer Inc.

Size	Document Number	Rev
	NEW CARD &HOLE	C
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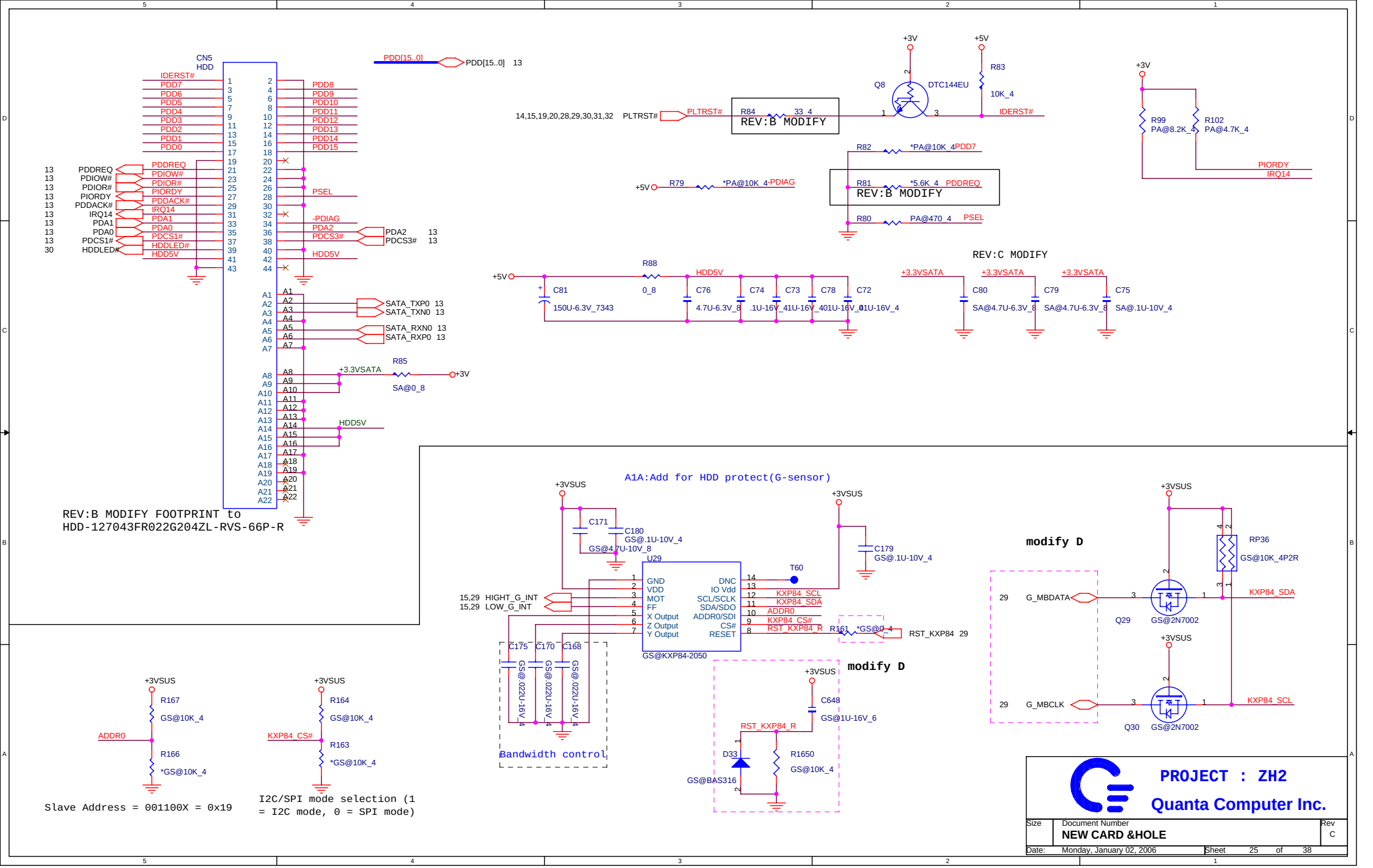
CN5
HDD
IDERST#
PDD7
PDD6
PDD5
PDD4
PDD3
PDD2
PDD1
PDD0
PDD8
PDD9
PDD10
PDD11
PDD12
PDD13
PDD14
PDD15
PDD[15..0]
PDD[15..0] 13
PDDREQ
PDIOW#
PDIOR#
PIORDY
PDDACK#
IRQ14
PDA1
PDA0
PDCS1#
HDDLED#
HDD5V
PSEL
-PDIAG
PDA2
PDCS3#
PDA2 13
PDCS3# 13
SATA_TXP0 13
SATA_TXN0 13
SATA_RXN0 13
SATA_RXP0 13
+3.3VSATA
R85
SA@0_8
+3V
REV:B MODIFY FOOTPRINT to
HDD-127043FR022G204ZL-RVS-66P-R
+3V
+5V
Q8
DTC144EU
R83
10K_4
14,15,19,20,28,29,30,31,32
PLTRST#
R84
33_4
REV:B MODIFY
IDERST#
R82
*PA@10K_4
PDD7
R79
*PA@10K_4
PDIAG
R81
*5.6K_4
PDDREQ
R80
PA@470_4
PSEL
R99
PA@8.2K_4
R102
PA@4.7K_4
PIORDY
IRQ14
REV:C MODIFY
R88
0_8
HDD5V
C81
150U-6.3V_7343
C76
4.7U-6.3V_8
C74
.1U-16V_4
C73
1U-16V_4
C78
01U-16V_4
C72
1U-16V_4
+3.3VSATA
C80
SA@4.7U-6.3V_8
C79
SA@4.7U-6.3V_8
C75
SA@.1U-10V_4
A1A:Add for HDD protect(G-sensor)
+3VSUS
C171
C180
GS@.1U-10V_4
GS@4.7U-10V_8
U29
GND
VDD
MOT
FF
X Output
Z Output
Y Output
DNC
IO Vdd
SCL/SCLK
SDA/SDO
ADDR0/SDI
CS#
RESET
T60
C179
GS@.1U-10V_4
15,29 HIGHT_G_INT
15,29 LOW_G_INT
KXP84_SCL
KXP84_SDA
ADDR0
KXP84_CS#
RST_KXP84_R
R161
*GS@0_4
RST_KXP84 29
GS@KXP84-2050
C175
C170
C168
GS@.022U-16V_4
Bandwidth control
modify D
C648
GS@1U-16V_6
RST_KXP84_R
D33
GS@BAS316
R1650
GS@10K_4
modify D
RP36
GS@10K_4P2R
29 G_MBDATA
29 G_MBCLK
Q29
Q30
GS@2N7002
KXP84_SDA
KXP84_SCL
R167
R166
*GS@10K_4
ADDR0
Slave Address = 001100X = 0x19
R164
R163
*GS@10K_4
KXP84_CS#
I2C/SPI mode selection (1
= I2C mode, 0 = SPI mode)
PROJECT : ZH2
Quanta Computer Inc.
Size
Document Number
NEW CARD &HOLE
Rev
C
Date: Monday, January 02, 2006
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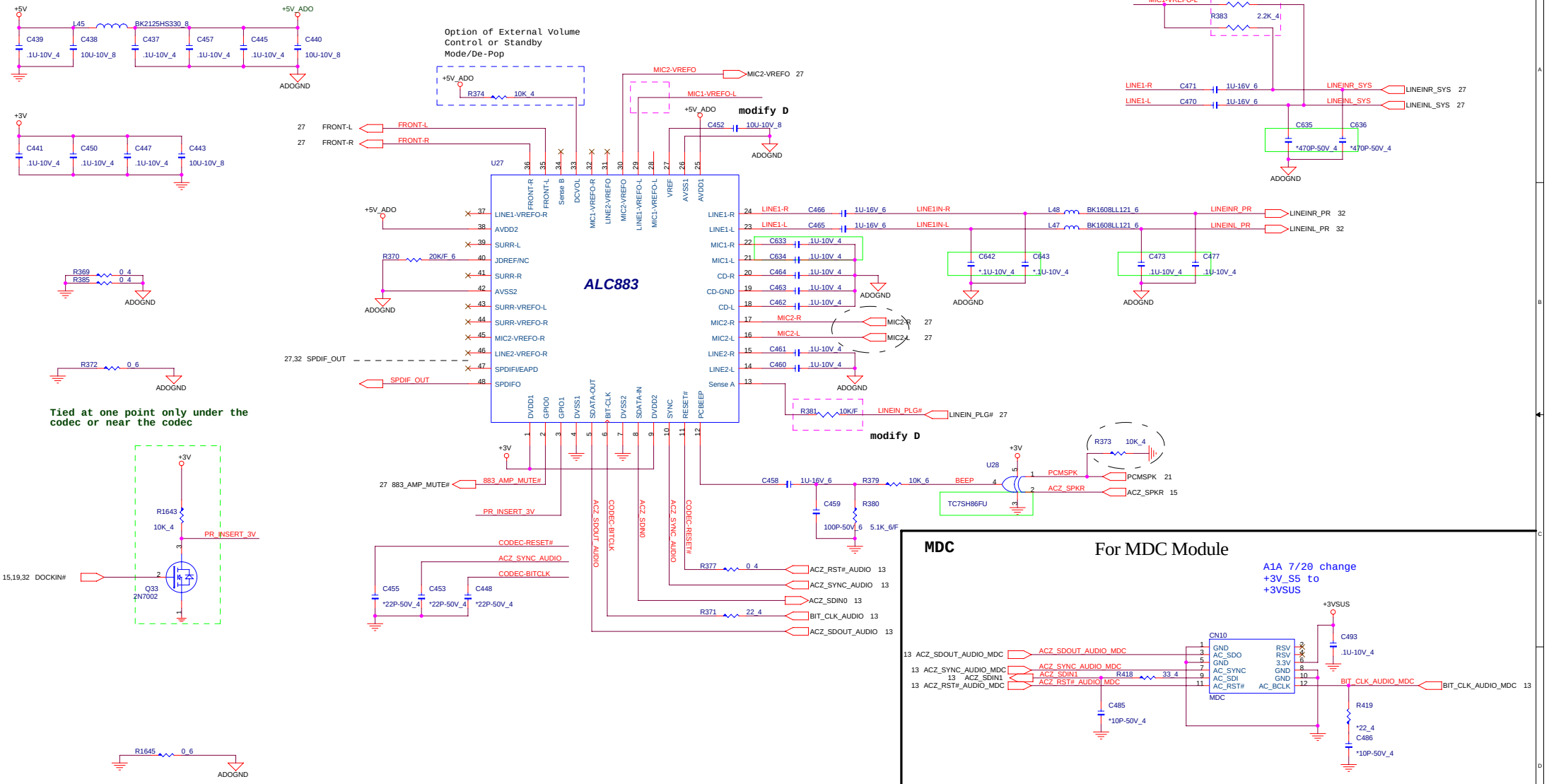
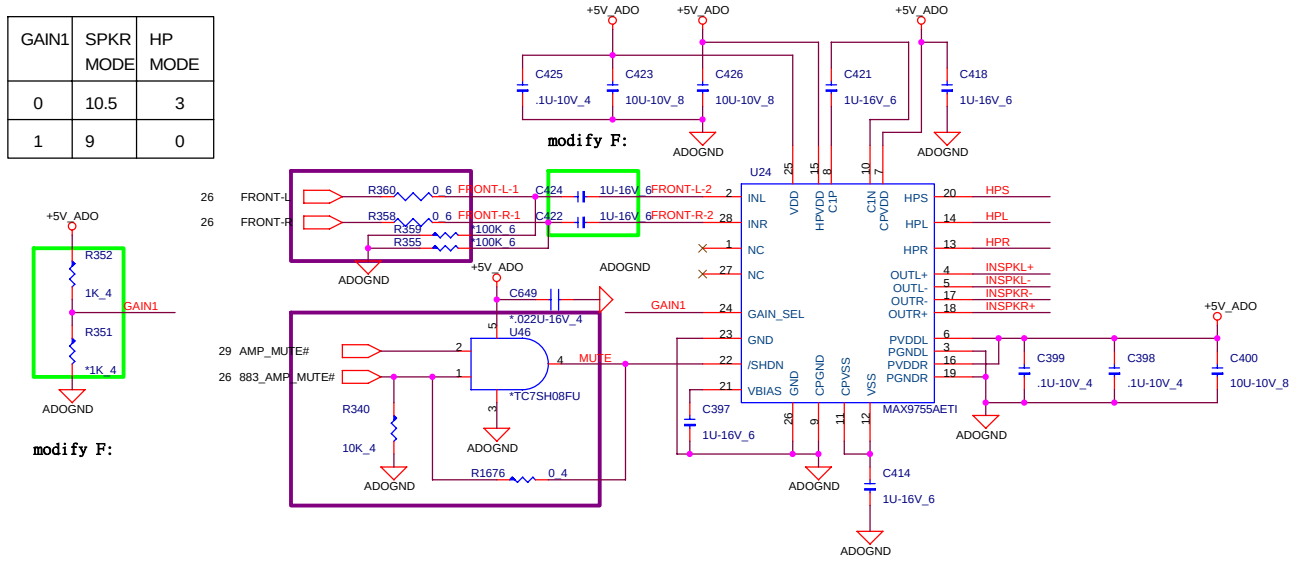
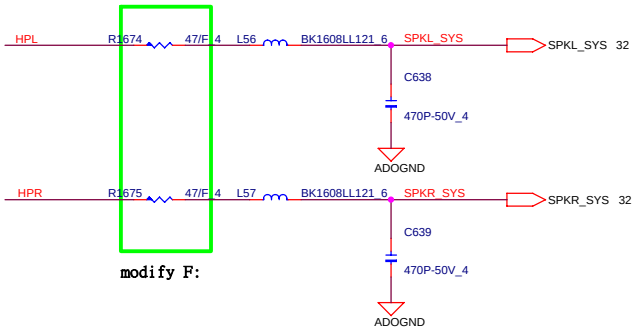
CODEC(ALC883)



GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0



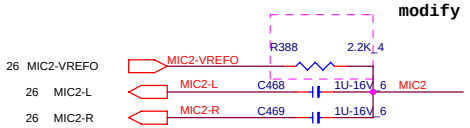
SPKR

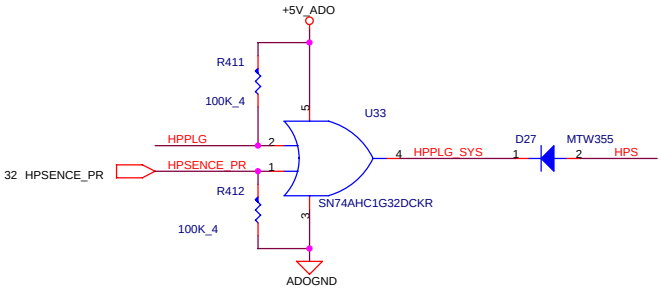


MIC

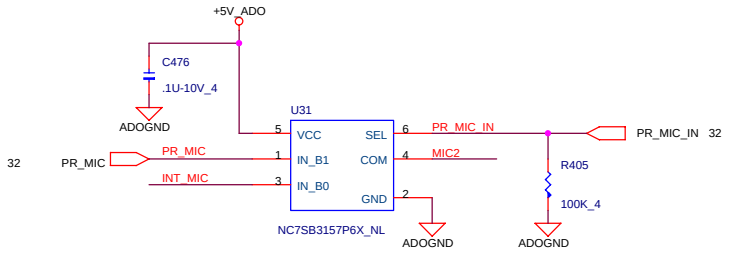
modify D

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

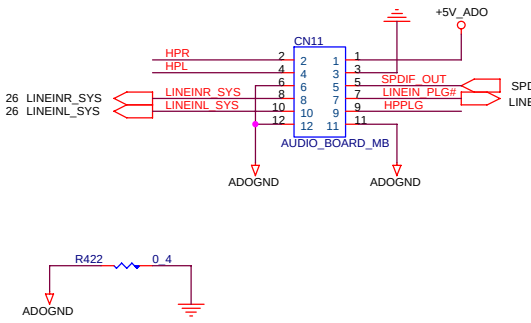




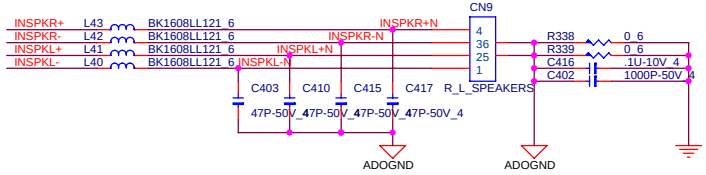
20 MIL

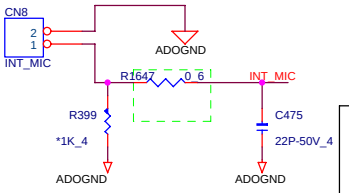


AUDIO BOARD



SPEAKER CONNECTOR



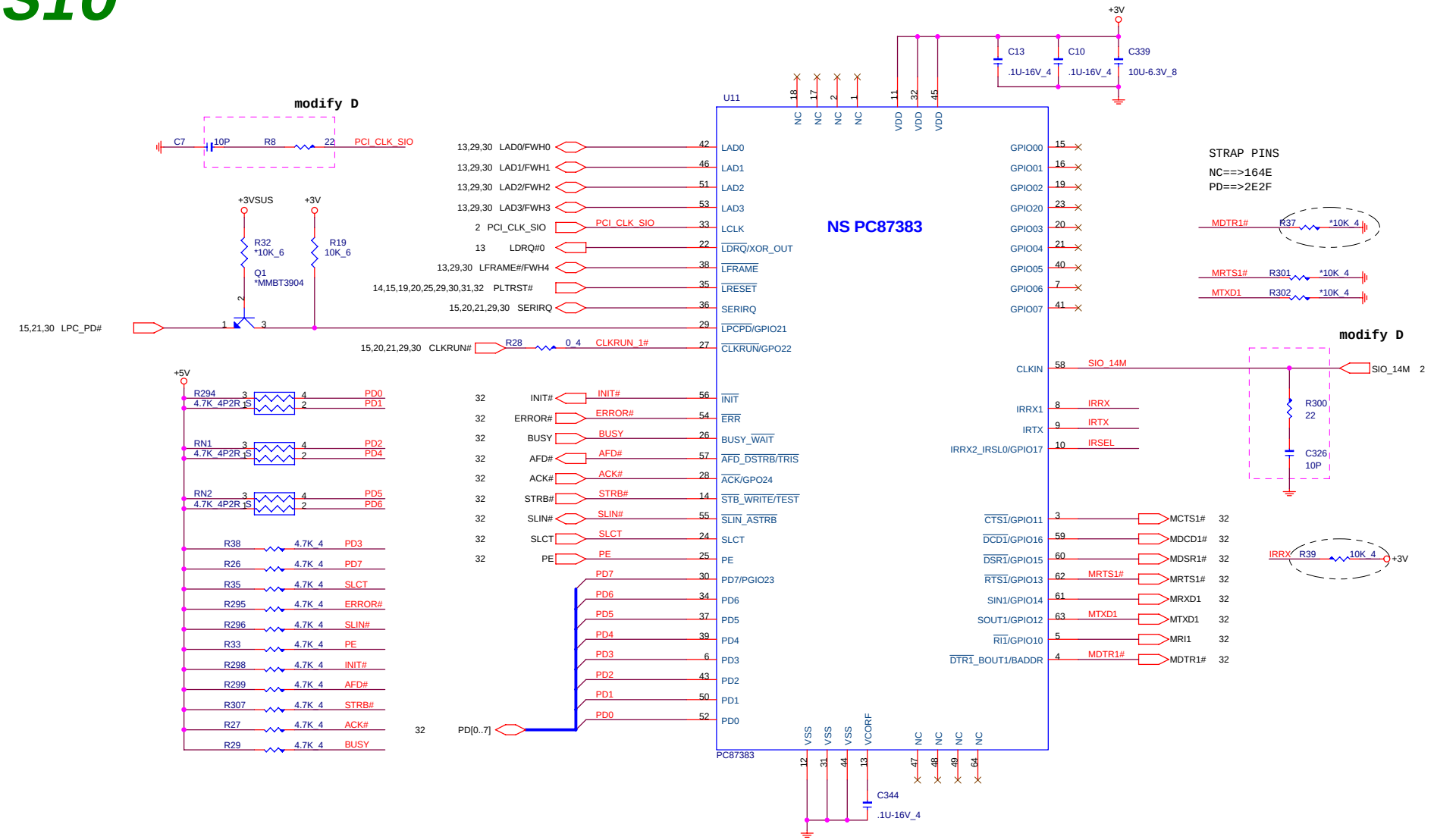


PROJECT : ZH2

Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP(MAX 9755)	1A
Date: Monday, January 02, 2006	Sheet 27 of 38	

SIO



PROJECT : ZH2			
Quanta Computer Inc.			
Size: Custom	Document Number: SIO (87383)		Rev: E2B
Date: Monday, January 02, 2006	Sheet 28 of 38		

LDRQ#(pin 8) internal is no use

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

SHBM=1: Enable shared memory with host BIOS

modify D

modify F:

REV:C MODIFY

If Pin 24 is not pull-high, System will not able to boot.

A1A add HWPG ckt

A1A 7/8 change 121K to 62K

A1B 8/29 pop R327

B1B:Reversed for G sensor buzzer

BIU configuration should match flash speed used

FOR 97551 ONLY

ST Micro M29W008AB/AMD-29LV081B/SST39VF080

modify E:

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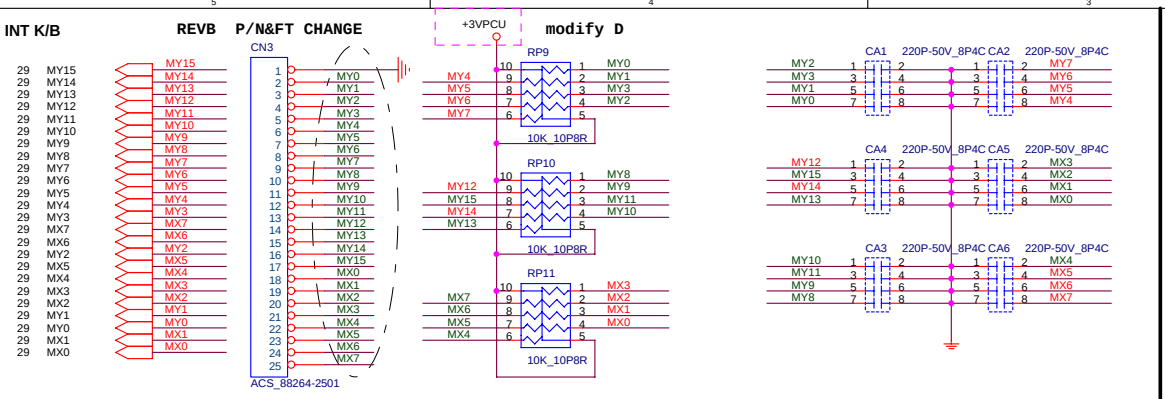
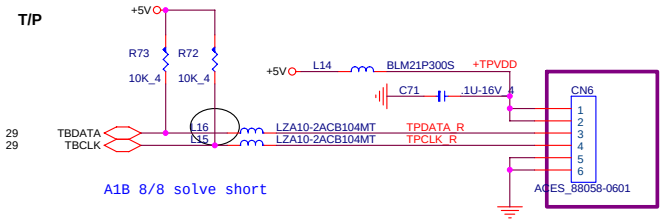
Quanta Computer Inc.	
Size	Document Number: 97551 & FLASH; Rev: 1A
Date: Tuesday, January 03, 2006	Sheet 29 of 38

INT K/B

REVB P/N&FT CHANGE



T/P

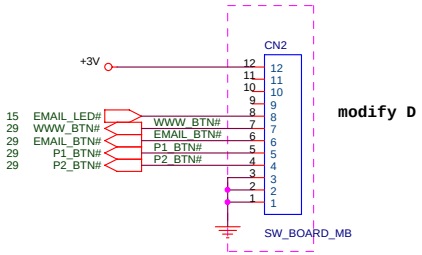


A1B 8/8 solve short

modify E:

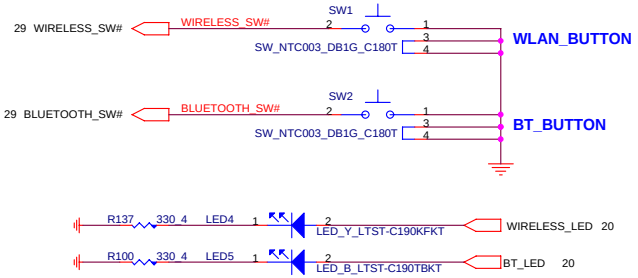
SW BOARD

A1A define keyboard matrix as same as ZH1

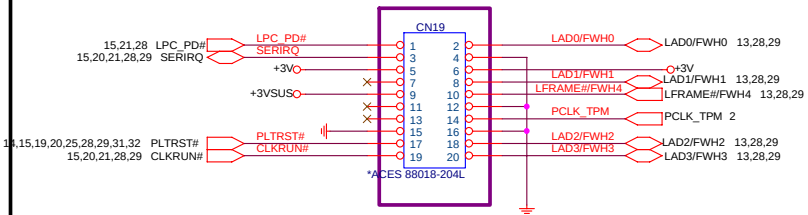


modify D

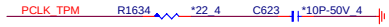
WL/BT



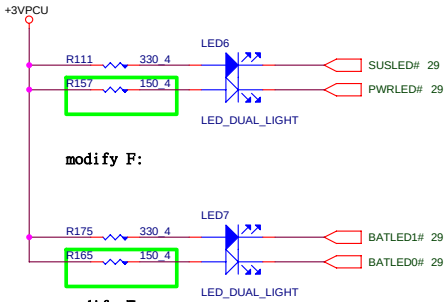
TPM



modify E:

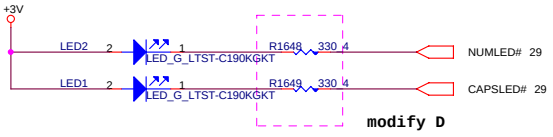


POWER LED/BATT LED

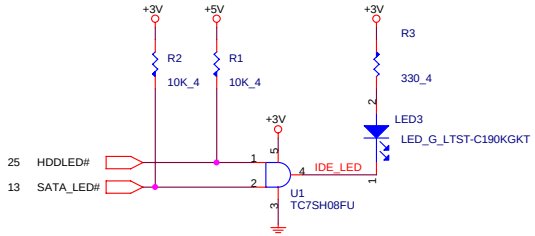


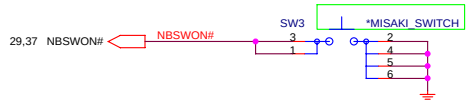
modify F:

modify F:

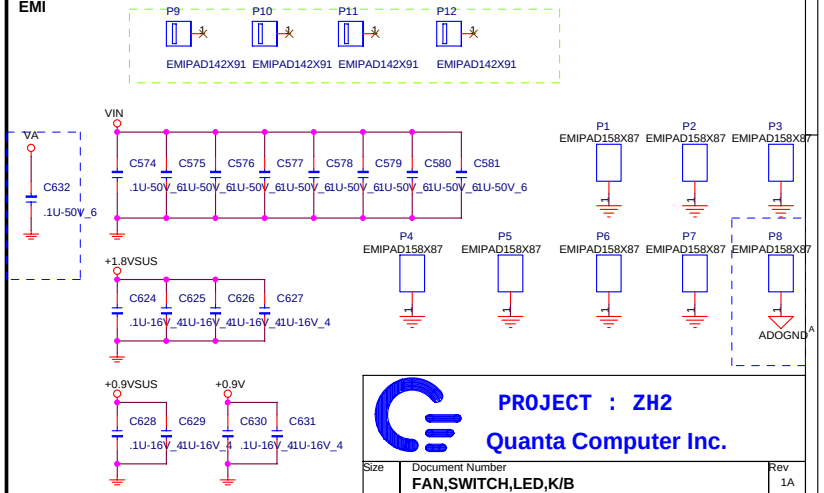


modify D





EMI



PROJECT : ZH2

Quanta Computer Inc.

Size	Document Number	Rev
	FAN,SWITCH,LED,K/B	1A

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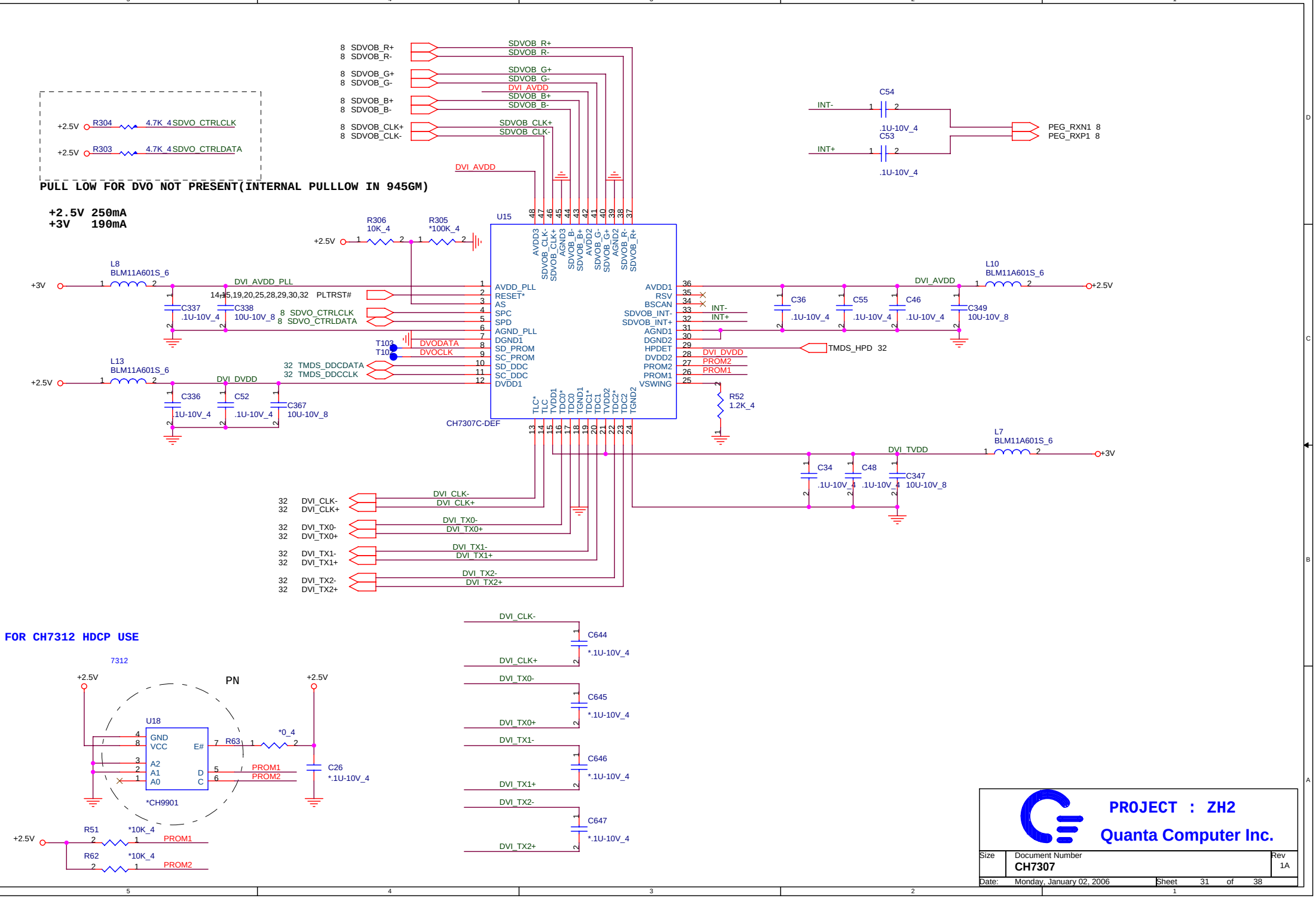
+2.5V R304 4.7K_4 SDVO_CTRLCLK
+2.5V R303 4.7K_4 SDVO_CTRLDATA
PULL LOW FOR DVO NOT PRESENT(INTERNAL PULLLOW IN 945GM)
+2.5V 250mA
+3V 190mA
8 SDVOB_R+
8 SDVOB_R-
8 SDVOB_G+
8 SDVOB_G-
8 SDVOB_B+
8 SDVOB_B-
8 SDVOB_CLK+
8 SDVOB_CLK-
DVI_AVDD
U15
CH7307C-DEF
AVDD_PLL
RESET*
AS
SPC
SPD
AGND_PLL
DGND1
SD_PROM
SC_PROM
SD_DDC
SC_DDC
DVDD1
AVDD1
RSV
BSCAN
SDVOB_INT-
SDVOB_INT+
AGND1
DGND2
HPDET
DVDD2
PROM2
PROM1
VSWING
TLC*
TLC
TVDD1
TDO*
TDO
TGND1
TDC1*
TDC1
TVDD2
TDC2*
TDC2
TGND2
DVI_AVDD_PLL
DVI_DVDD
DVI_TVDD
PLTRST#
DVODATA
DVOCLK
TMDS_DDCDATA
TMDS_DDCCLK
TMDS_HPD 32
INT-
INT+
PEG_RXN1 8
PEG_RXP1 8
DVI_CLK-
DVI_CLK+
DVI_TX0-
DVI_TX0+
DVI_TX1-
DVI_TX1+
DVI_TX2-
DVI_TX2+
FOR CH7312 HDCP USE
7312
PN
U18
GND
VCC
E#
A2
A1
A0
D
C
*CH9901
PROM1
PROM2
PROJECT : ZH2
Quanta Computer Inc.
Document Number
CH7307
Rev
1A
Date: Monday, January 02, 2006
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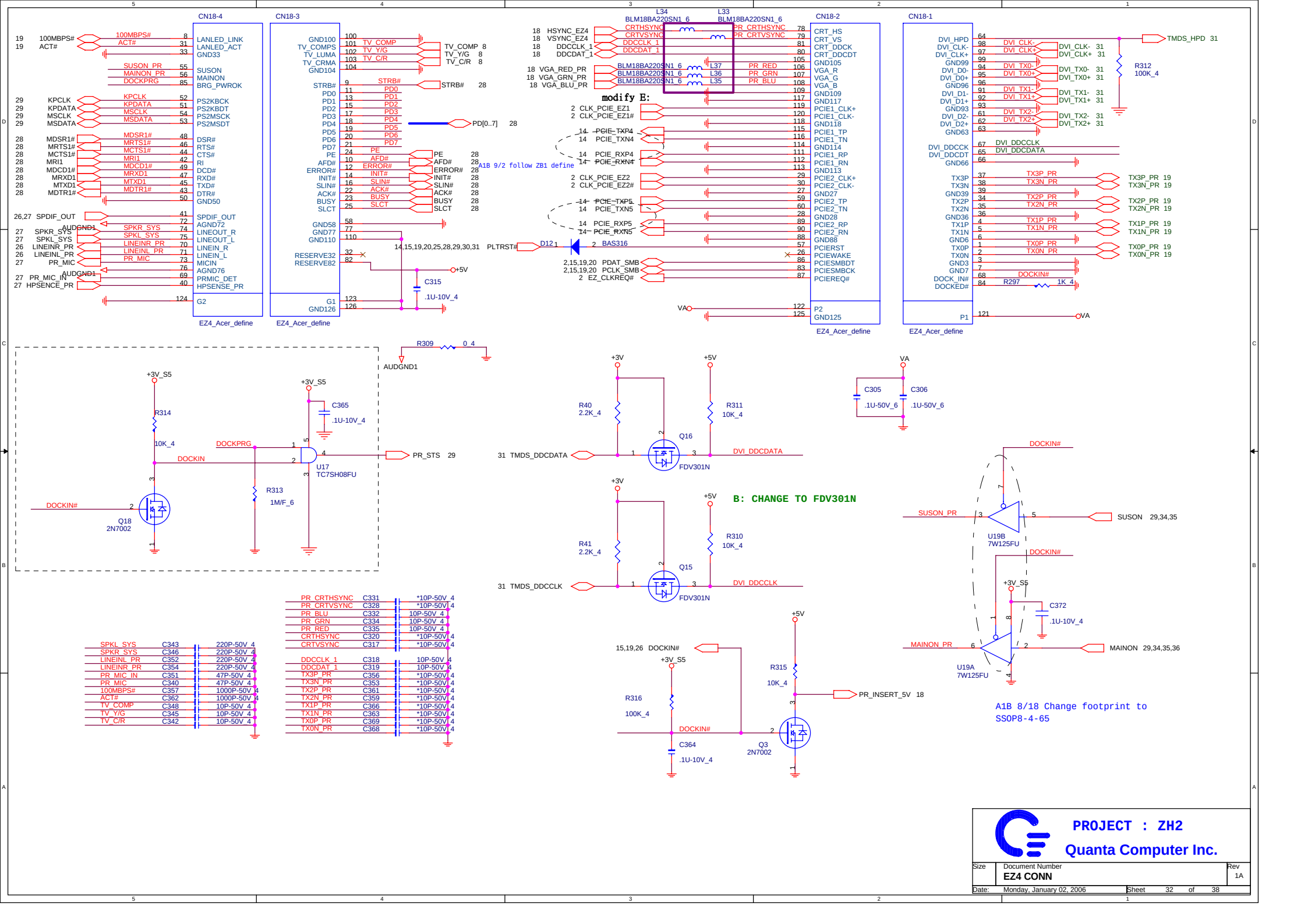
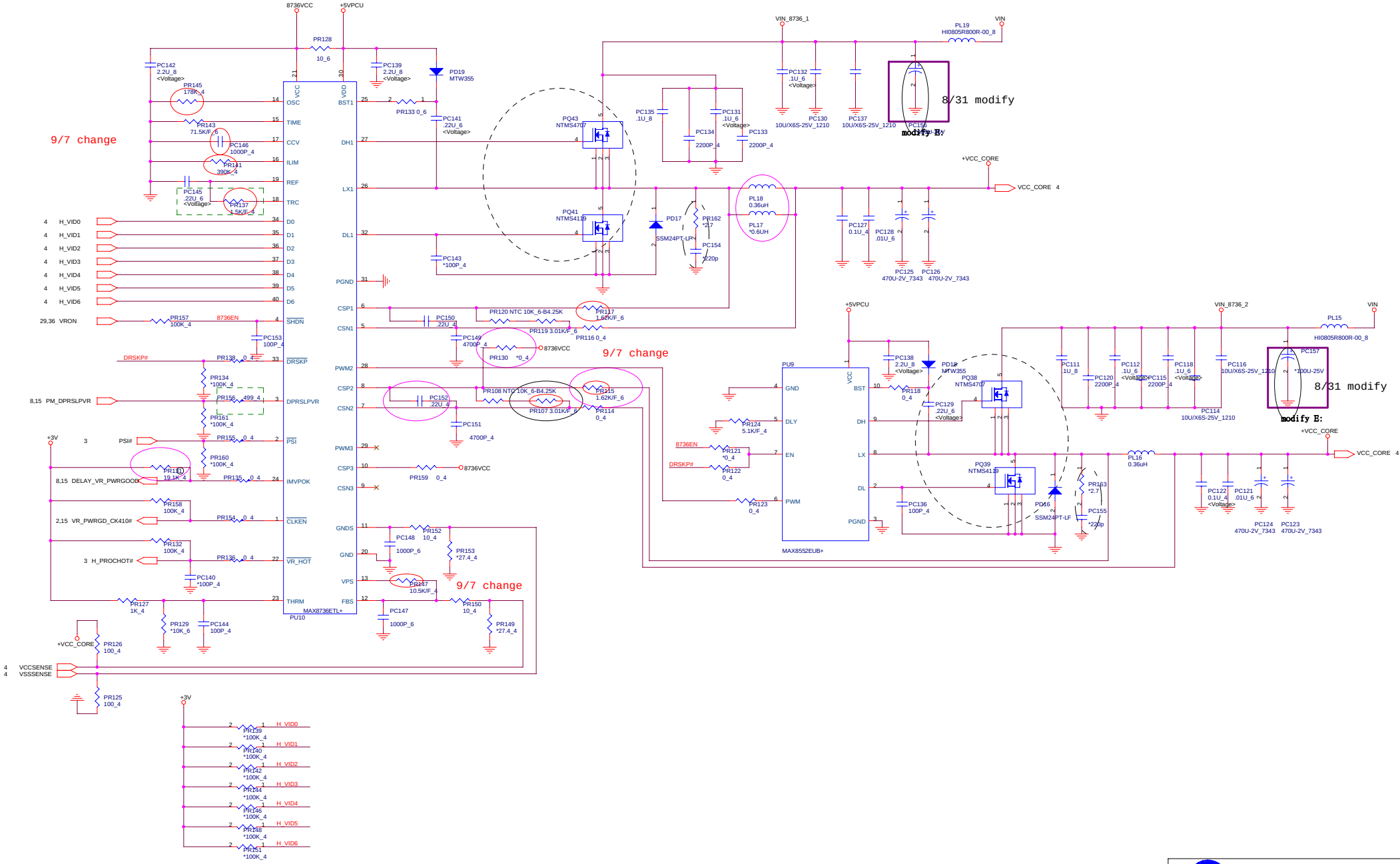

CN18-4
CN18-3
CN18-2
CN18-1
EZ4_Acer_define
modify E:
A1B 9/2 follow ZB1 define
B: CHANGE TO FDV301N
A1B 8/18 Change footprint to SSOP8-4-65
PROJECT : ZH2
Quanta Computer Inc.
EZ4 CONN
Monday, January 02, 2006


8736VCC
+5VPCU
VIN_8736_1
VIN
PL19
HI0805R800R-00_8
8/31 modify
modify B:
9/7 change
+VCC_CORE
VCC_CORE 4
PU10
MAX8736ETL+
PU9
MAX8552EUB+
+5VPCU
VIN_8736_2
VIN
PL15
HI0805R800R-00_8
8/31 modify
modify B:
+VCC_CORE
VCC_CORE 4
9/7 change
9/7 change
4 H_VID0
4 H_VID1
4 H_VID2
4 H_VID3
4 H_VID4
4 H_VID5
4 H_VID6
29,36 VRON
8,15 PM_DPRSLPVR
8,15 DELAY_VR_PWRGOOD
2,15 VR_PWRGD_CK410#
3 H_PROCHOT#
DRSKP#
PSI#
4 VCCSENSE
4 VSSSENSE
+3V
+VCC_CORE
PROJECT : ZH2
Quanta Computer Inc.
CPU CORE (MAX8736)
Monday, January 02, 2006
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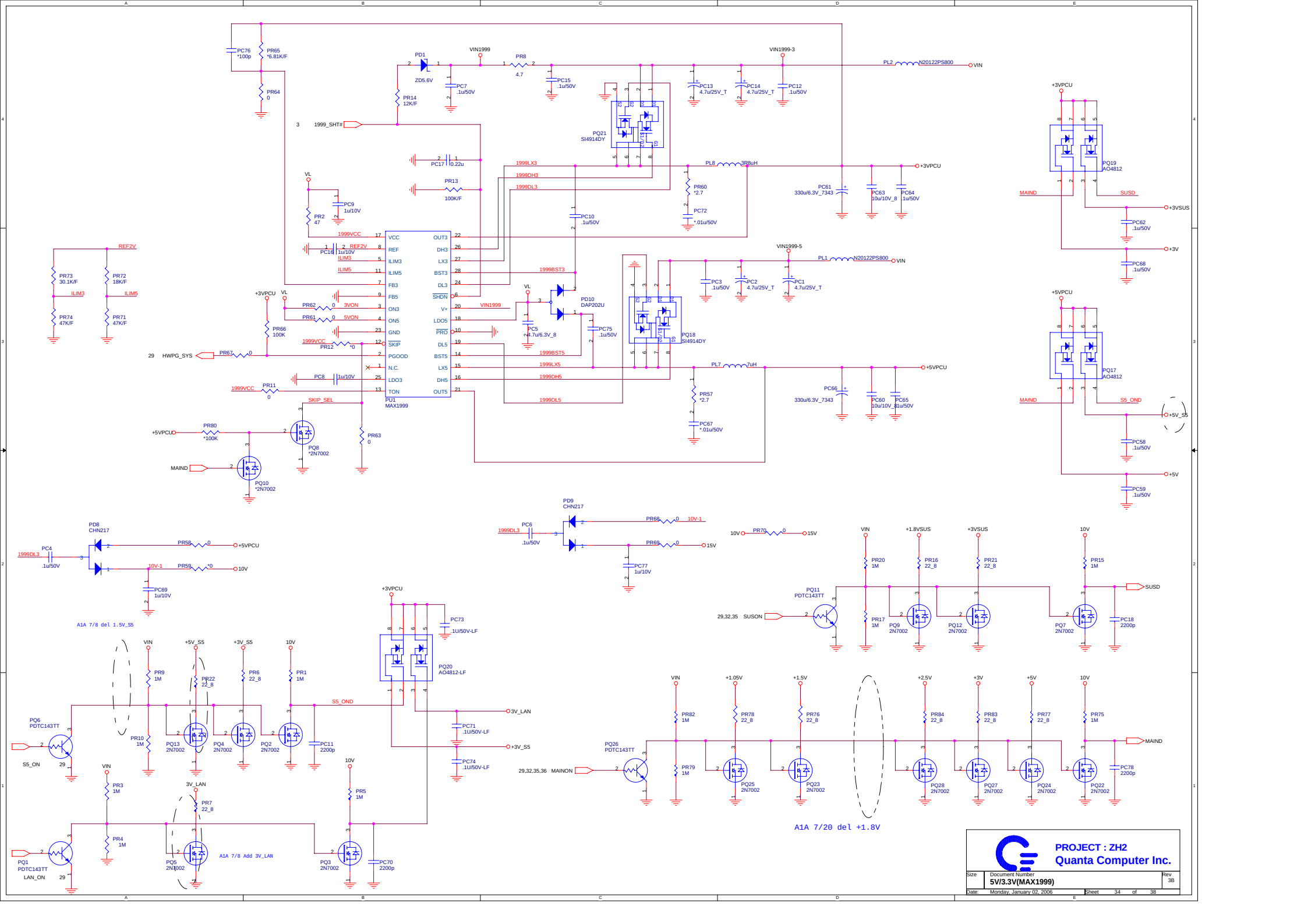
PU1
MAX1999
PQ18
SI4914DY
PQ21
SI4914DY
PQ19
AO4812
PQ17
AO4812
PQ20
AO4812-LF
PD1
ZD5.6
PD10
DAP202U
PD8
CHN217
PD9
CHN217
PROJECT : ZH2
Quanta Computer Inc.
5V/3.3V(MAX1999)
Monday, January 02, 2006
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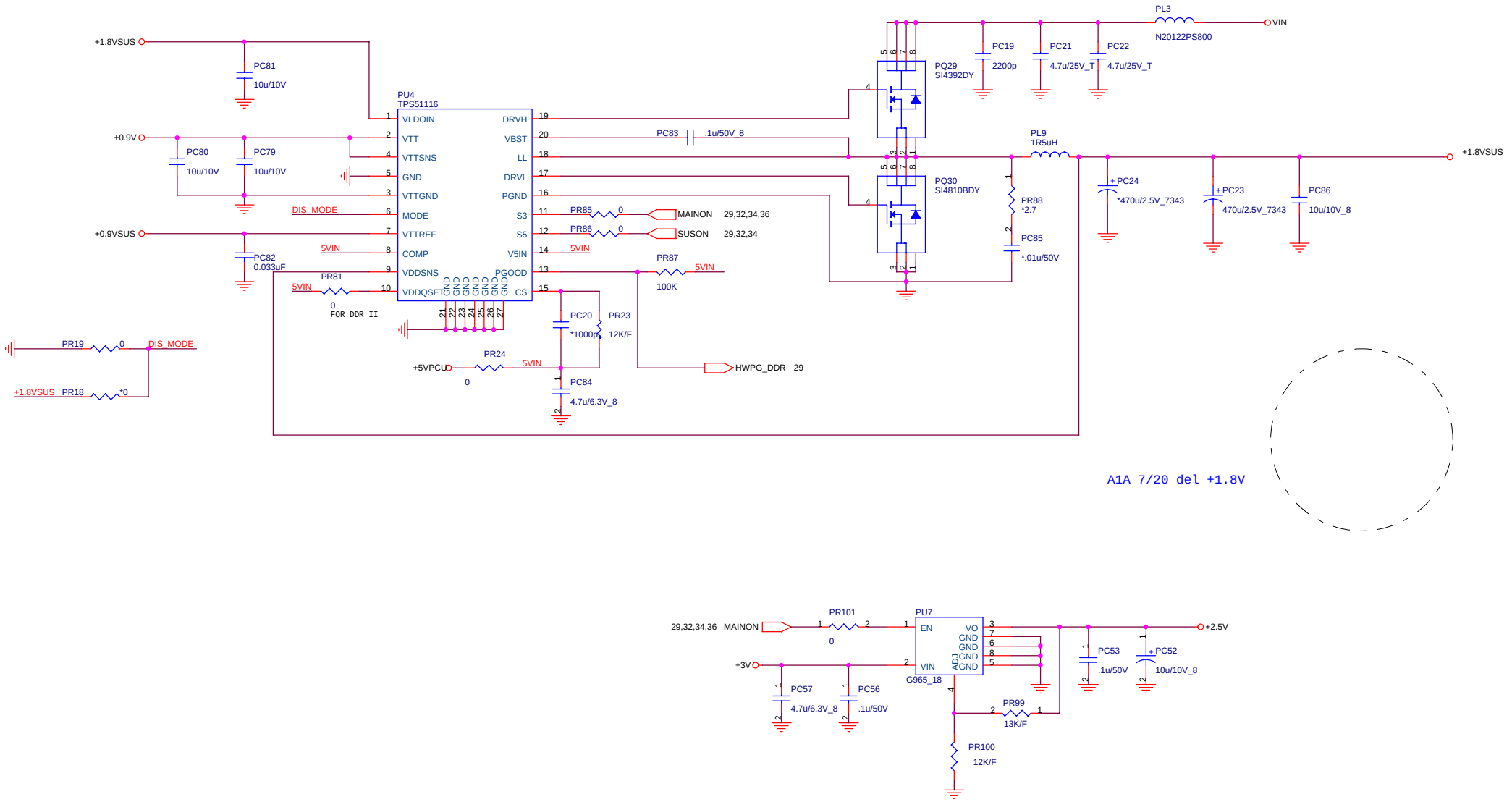
A1A 7/8 del 1.5V_S5
A1A 7/8 Add 3V_LAN
A1A 7/20 del +1.8V



PROJECT : ZH2
Quanta Computer Inc.

Size	Document Number	Rev
	2.5VSUS / 1.25VTERM	3B
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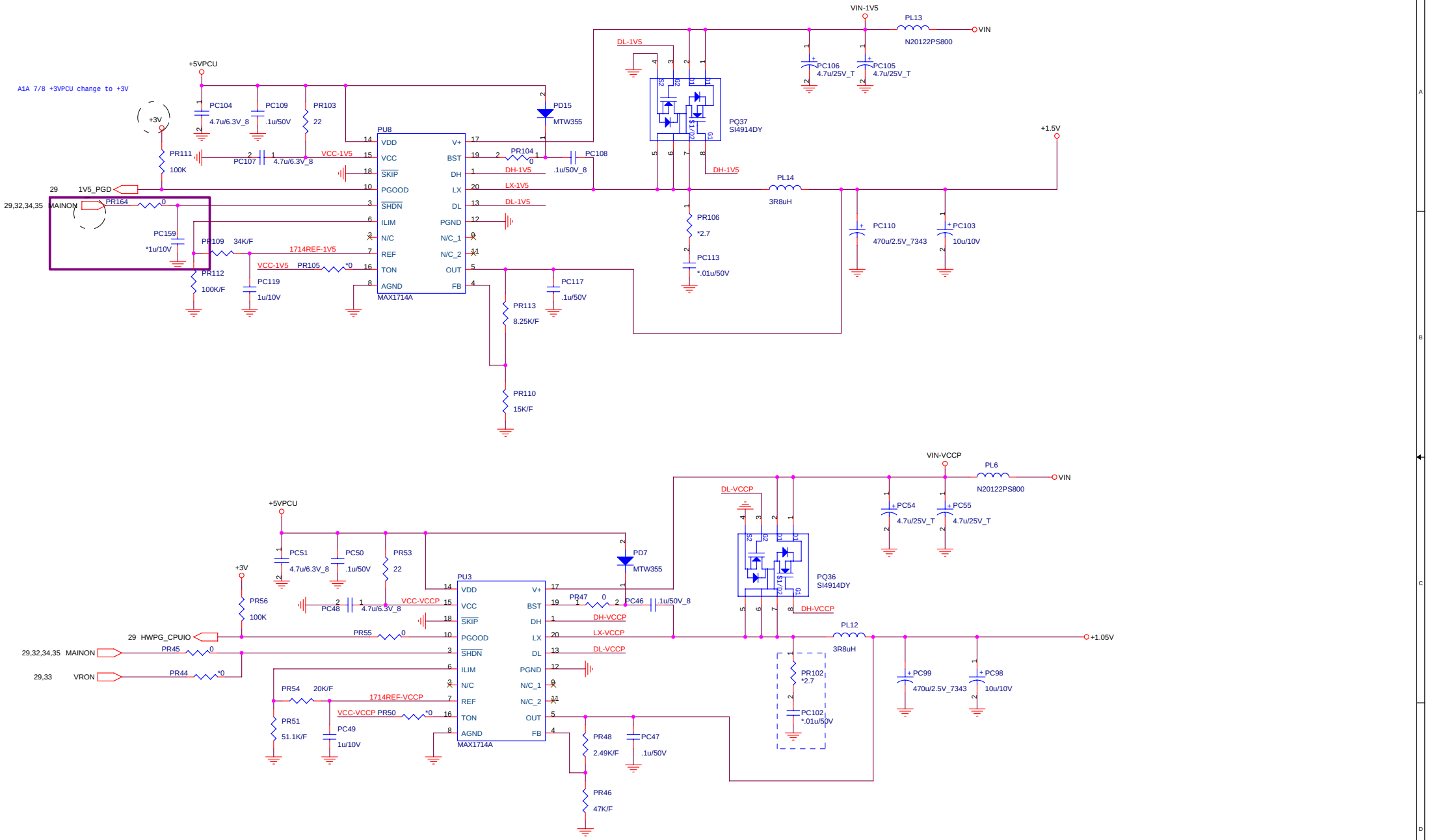

PROJECT : ZH2
Quanta Computer Inc.

Size	Document Number	Rev
	+1.5V / +VCCP	3B
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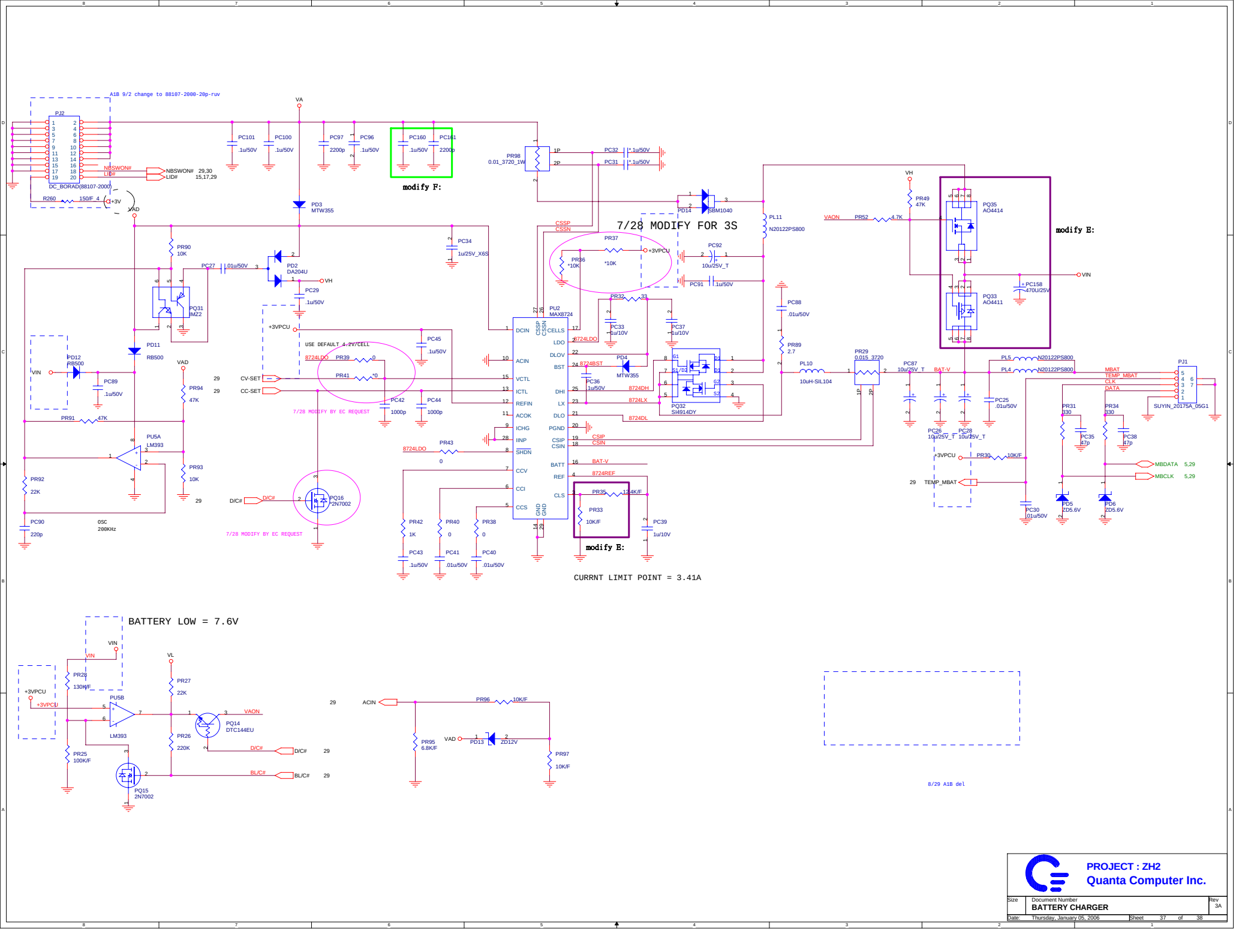
A1B 9/2 change to 88107-2000-20p-ruv
PJ2
DC_BORAD(88107-2000)
NBSWON#
LID#
NBSWON# 29,30
LID# 15,17,29
R260 150/F 4
+3V
VA
VAD
PC101 .1u/50V
PC100 .1u/50V
PC97 2200p
PC96 1u/50V
PC160 .1u/50V
PC161 2200p
modify F:
PR98 0.01_3720_1W
PC32 *.1u/50V
PC31 *.1u/50V
PD3 MTW355
PD14 SBM1040
PL11 N20122PS800
7/28 MODIFY FOR 3S
CSSP
CSSN
PR37 *10K
PR36 *10K
+3VPCU
PC92 10u/25V_T
PC91 .1u/50V
PR32 33
PC34 1u/25V_X6S
PC33 1u/10V
PC37 1u/10V
PR90 10K
PC27 .01u/50V
PD2 DA204U
PC29 .1u/50V
PQ31 IMZ2
PD11 RB500
PD12 RB500
VIN
PC89 .1u/50V
PR94 47K
PR91 47K
PR92 22K
PR93 10K
PU5A LM393
PC90 220p
OSC 200KHz
USE DEFAULT 4.2V/CELL
8724LDO
PR39 0
PR41 *0
PC45 1u/50V
PC42 1000p
PC44 1000p
CV-SET
CC-SET
7/28 MODIFY BY EC REQUEST
D/C#
PQ16 2N7002
PU2 MAX8724
DCIN
CELLS
LDO
DLOV
BST
DHI
LX
DLO
PGND
CSIP
CSIN
BATT
REF
CLS
ACIN
VCTL
ICTL
REFIN
ACOK
ICHG
IINP
SHDN
CCV
CCI
CCS
GND
8724BST
8724DH
8724LX
8724DL
8724REF
BAT-V
PD4 MTW355
PC36 1u/50V
PQ32 SI4914DY
PC88 .01u/50V
PR89 2.7
PL10 10uH-SIL104
PR29 0.015_3720
PC87 10u/25V_T
PC26 10u/25V_T
PC28 10u/25V_T
PC25 .01u/50V
PC30 .01u/50V
PR43 0
PR42 1K
PR40 0
PR38 0
PC43 .1u/50V
PC41 .01u/50V
PC40 .01u/50V
PR35 124K/F
PR33 10K/F
PC39 1u/10V
modify E:
CURRNT LIMIT POINT = 3.41A
VH
PR49 47K
VAON
PR52 4.7K
PQ35 AO4414
PQ33 AO4411
PC158 470U/25V
VIN
PR30 10K/F
PR31 330
PR34 330
PC35 47p
PC38 47p
PD5 ZD5.6V
PD6 ZD5.6V
MBAT
TEMP_MBAT
CLK
DATA
PJ1
SUYIN_20175A_05G1
MBDATA 5,29
MBCLK 5,29
TEMP_MBAT 29
BATTERY LOW = 7.6V
VL
PR28 130K/F
PR27 22K
PU5B LM393
PR26 220K
PQ14 DTC144EU
PR25 100K/F
PQ15 2N7002
BL/C#
PR96 10K/F
PR95 6.8K/F
PD13 ZD12V
PR97 10K/F
8/29 A1B del
PROJECT : ZH2
Quanta Computer Inc.
BATTERY CHARGER
Size
Document Number
Rev 3A
Date: Thursday, January 05, 2006
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Change list

Item	Fixed Issue	Reason for change	Schematic Rev.	PG#	Modify List	BD.Ver#
1	TV flicker	stable TV DAC power	E	10	change L52 to 10mH and C528 to 22U	
2	3D 2005 blue screen	+1.8VSUS plant not enough	E	35	add power plant	
3	LAN test	pass signal issue	E	19	change R58 from 1.24k to 1.2k	
4	CRT	pass signgal issue	E	8	change L33~L37 , L26~L27 to BLM18BA220SN1_6	
5	buzzer sound	too small	E	29	Change +3VSUS to +5V_S5	
6	over adaptor current 3.41A	meet adaptor spec	E	37	change PR35 to 12.4k , PR33 to 10k	
7	Chock noise	low freq noise in C3, C4 mode	E	37	change PQ35, PQ33 and add 470U cap	
8	speaker sound	D-A Full-scale output voltage	E	27	mount R531 , remove R532 chagne R360 , R358 to 4.3K	
9	BO BO sound		E	27	883_MUTE pull down 10k and enable high in DOS mode	
10	audio qality	PassBandRipple	E	27	change C422 & C424 to 2.2U	
11	G-sensor	connect to EC	E	25		
12	G-sensor	connect to EC	E	25		

PROJECT : ZH2
Quanta Computer Inc.

Size	Document Number	Rev
	CHANGE LIST	D
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