

Compal confidential

Schematics Document

Mobile P4 uFCBGA/uFCPGA with SIS 650/961 core logic chip

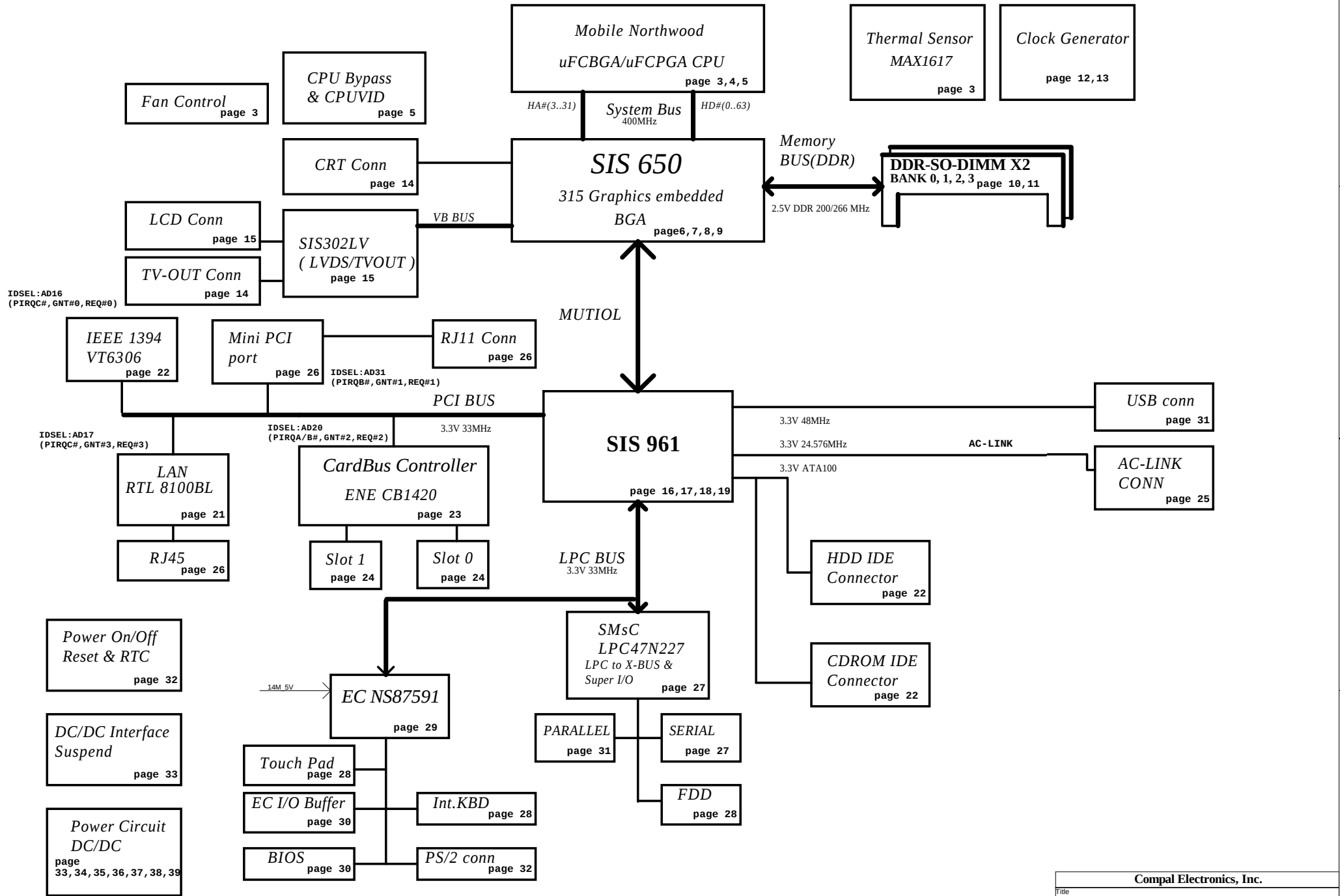
2002-05-13

REV:1.0

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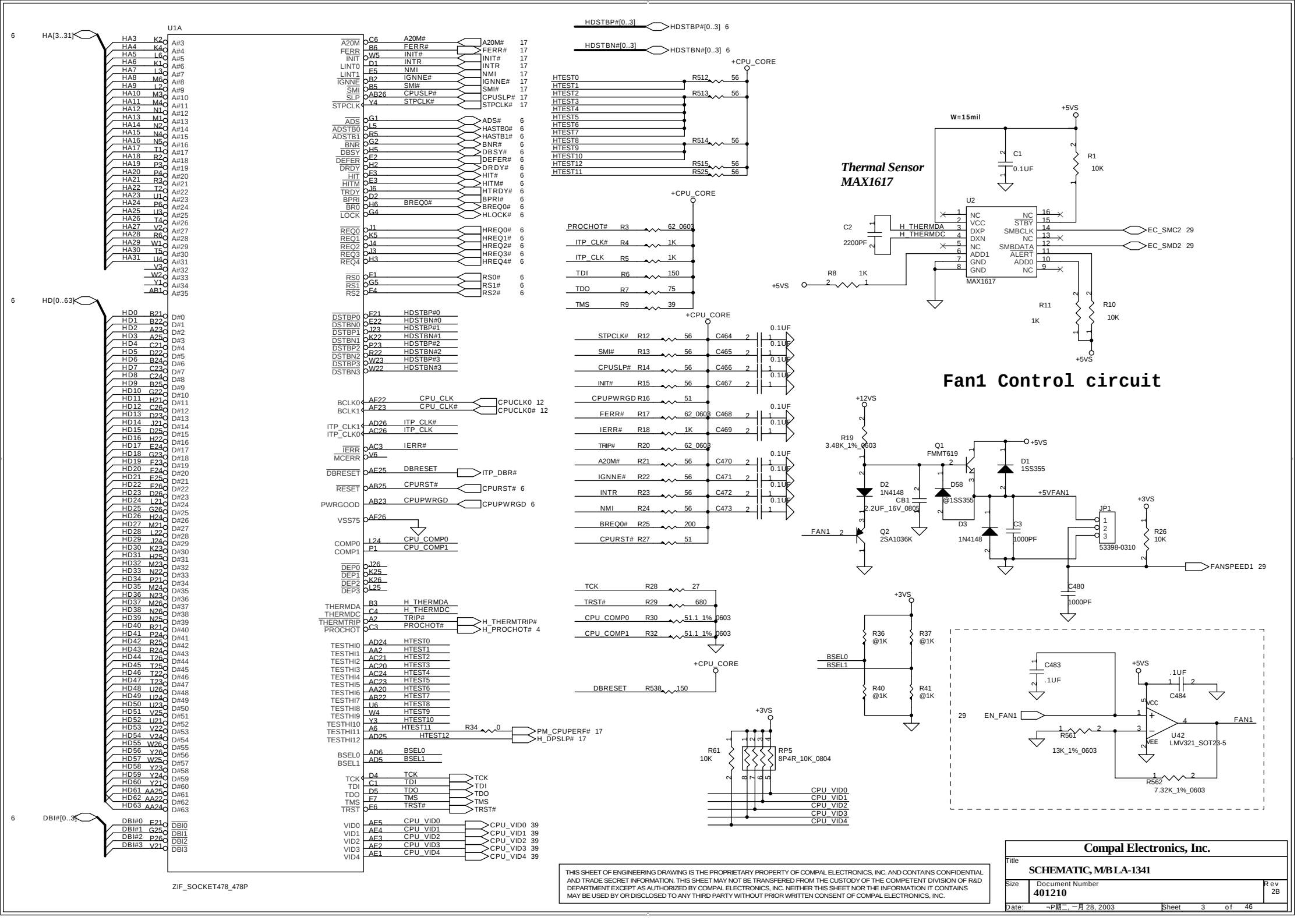
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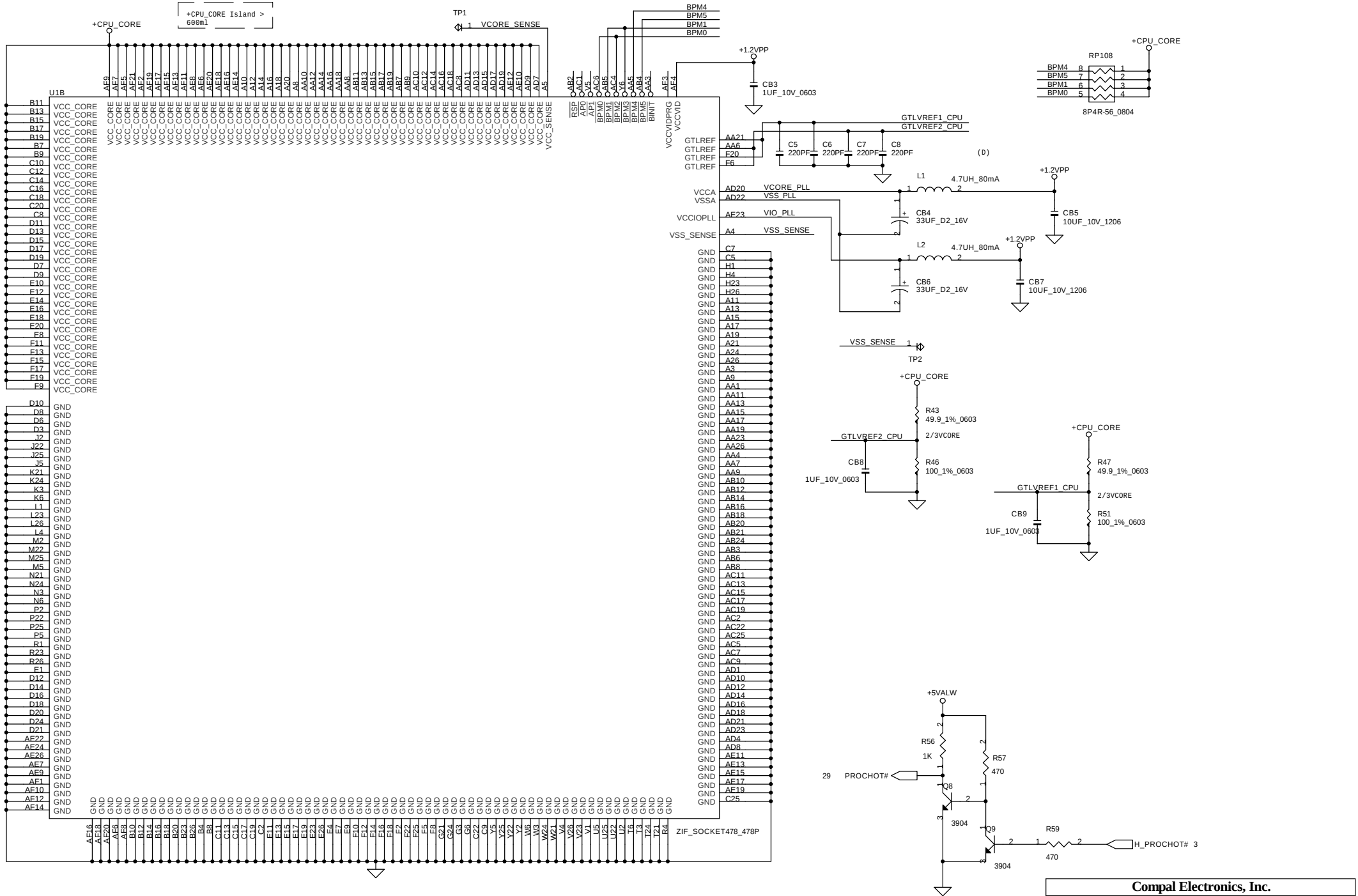
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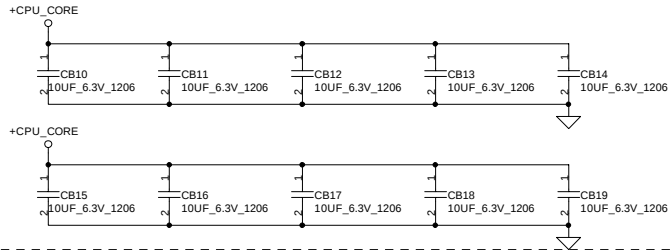


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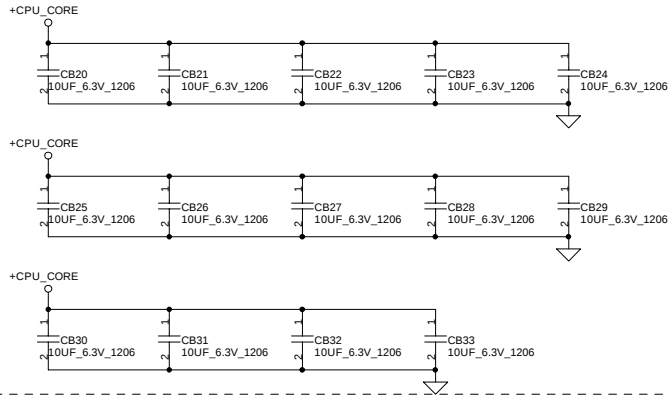
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Layout note :
Place close to CPU. Use 2-3 vias per PAD.
Place 22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2-3 vias per PAD.

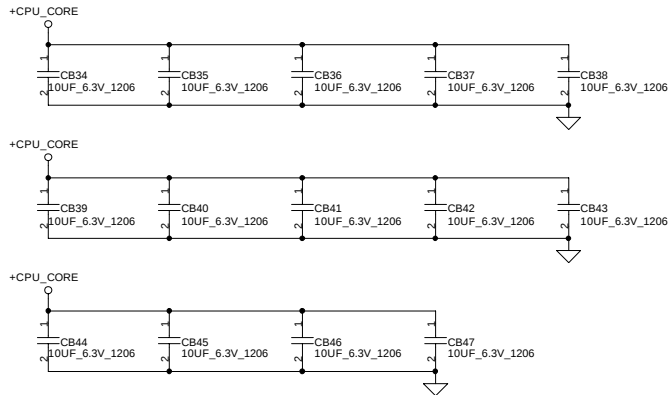
Please place these cap in the socket cavity area



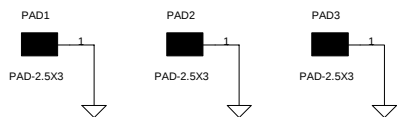
Please place these cap on the socket north side



Please place these cap on the socket south side

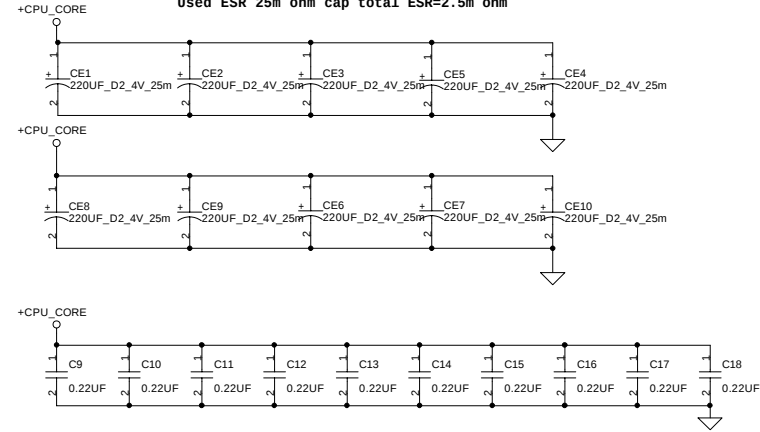


EMI Clip PAD for CPU



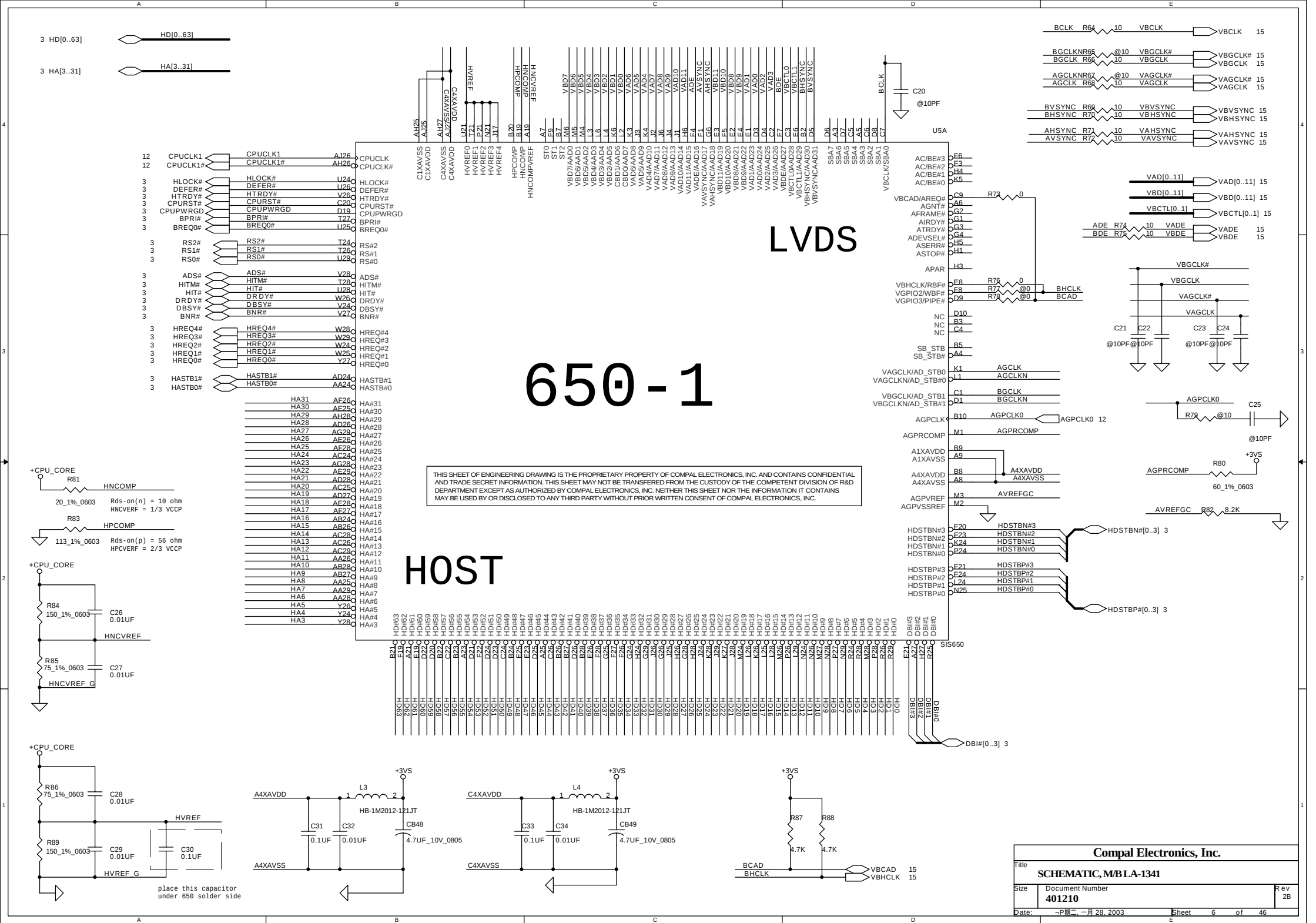
Layout note :
Place close to CPU power and
ground pin as possible
(<1inch)

Used ESR 25m ohm cap total ESR=2.5m ohm

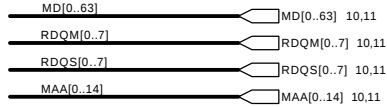


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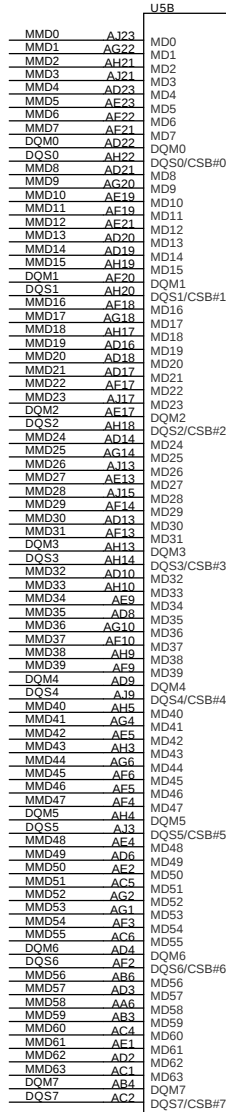
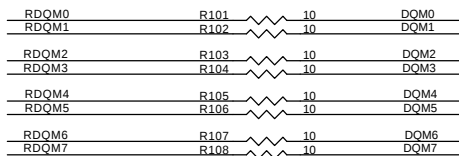
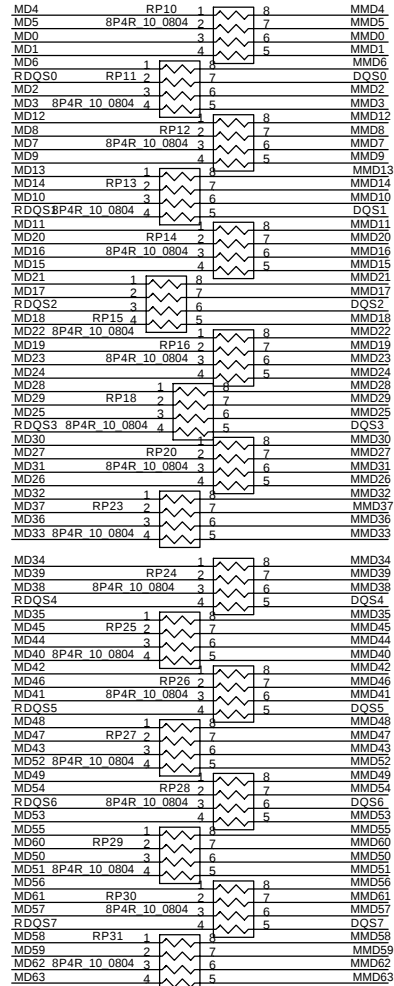
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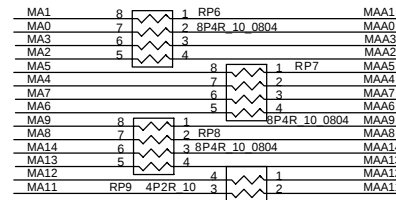
NOTE:This page is for pure DDR SDRAM PCB design



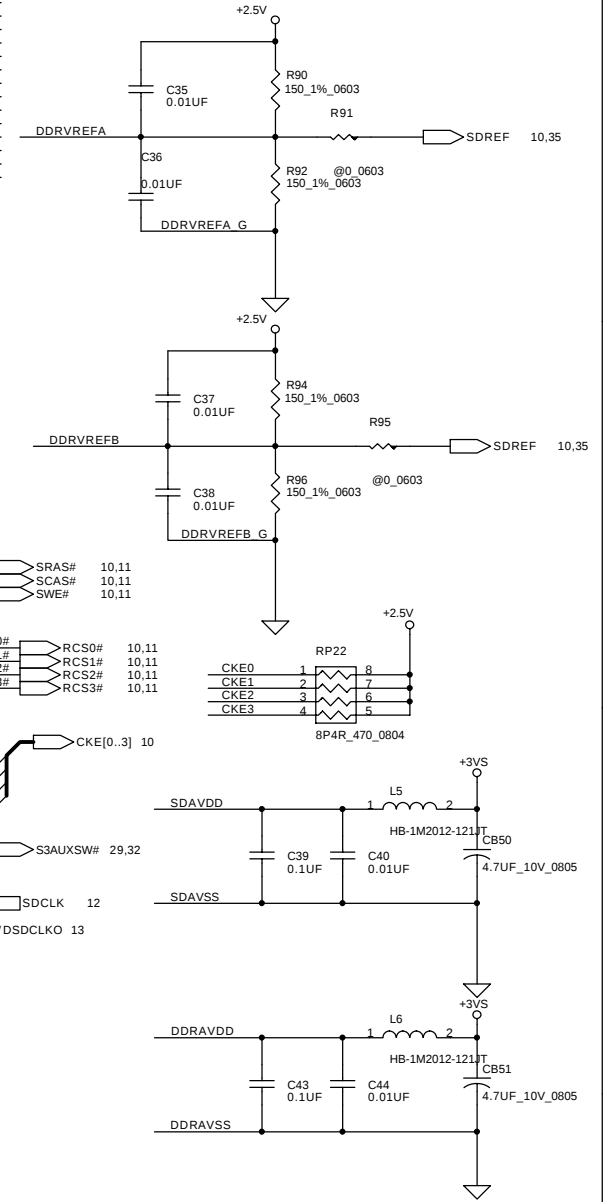
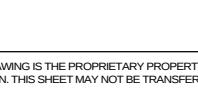
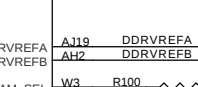
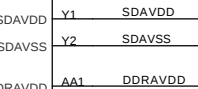
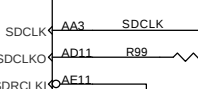
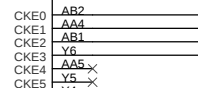
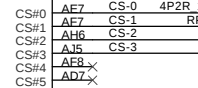
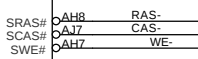
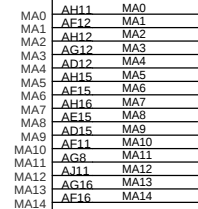
RP* PLACE CLOSE TO DIMM



650-2

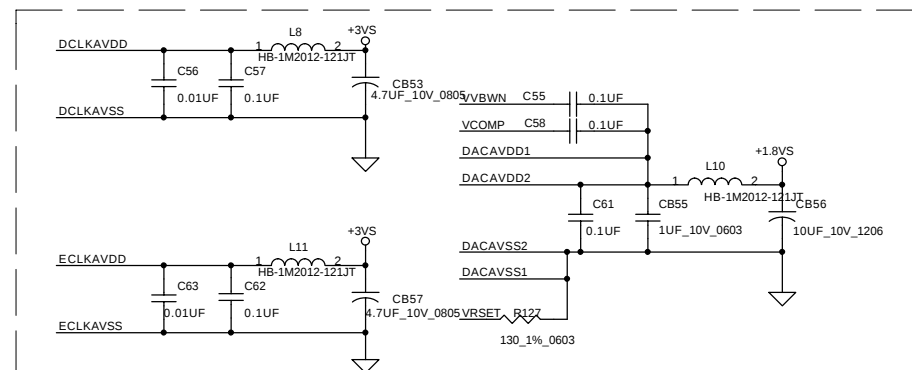
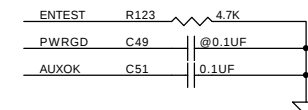
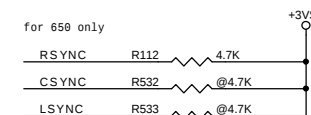
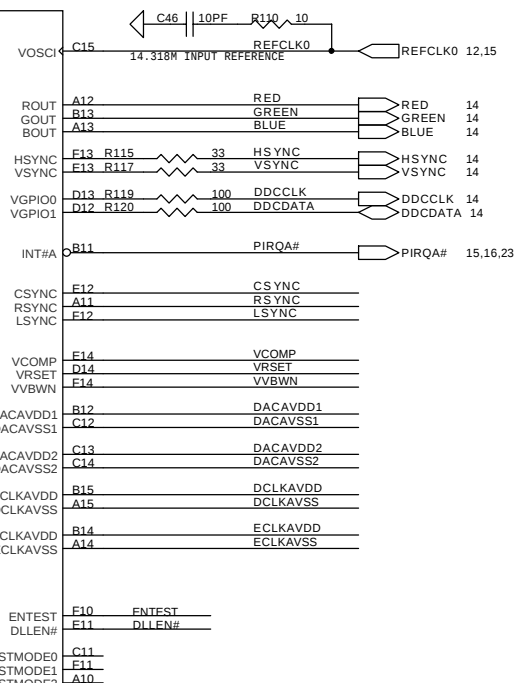
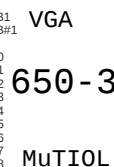
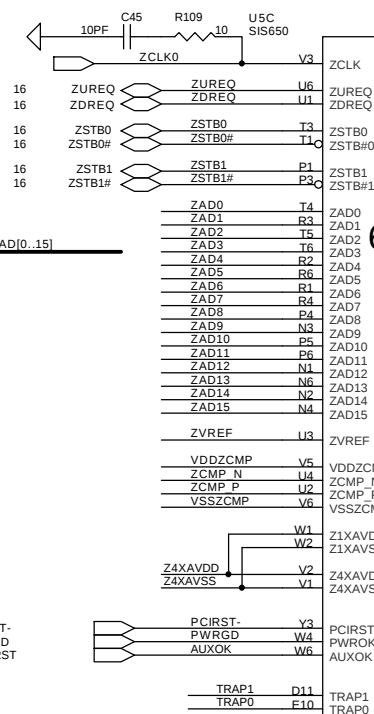
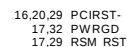
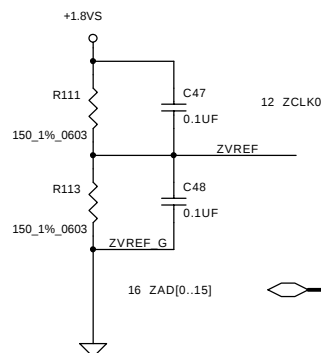


RP* place close to DIMM1

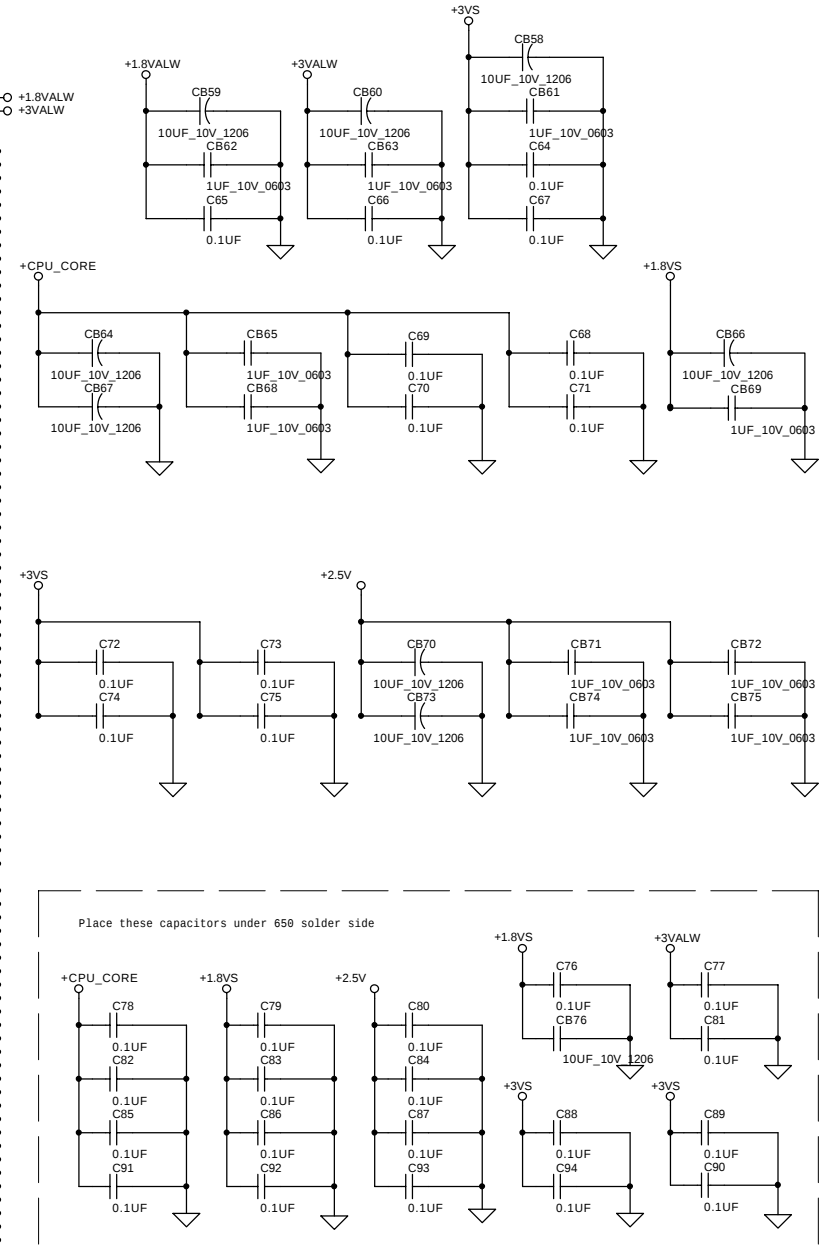
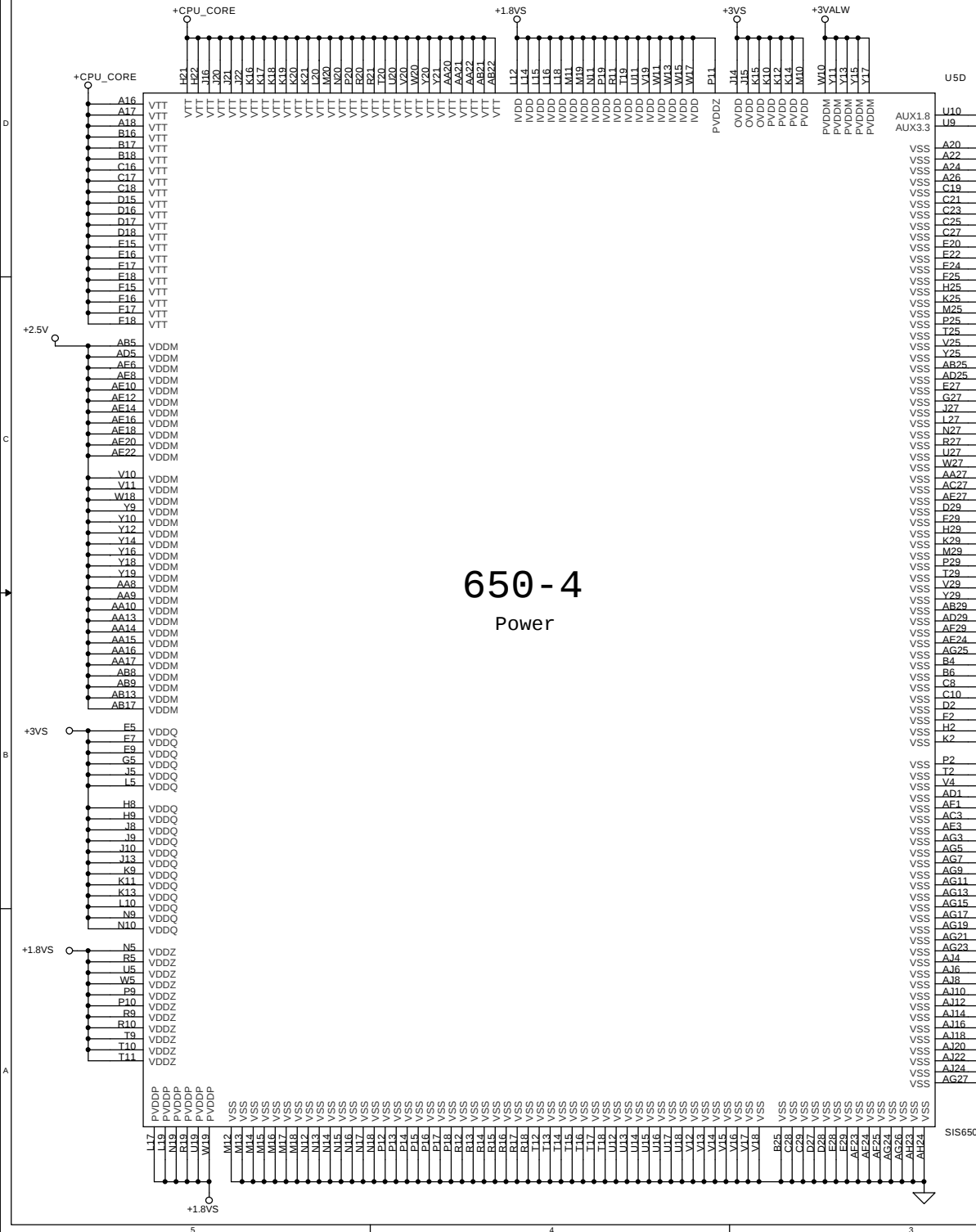


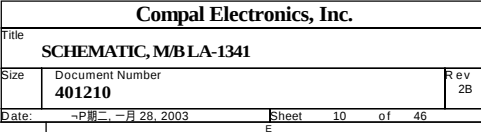
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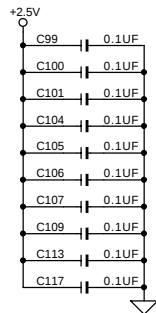
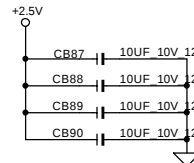
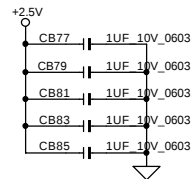


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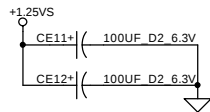
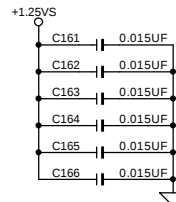
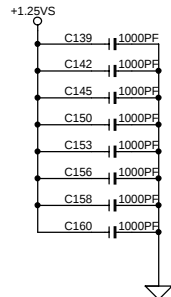
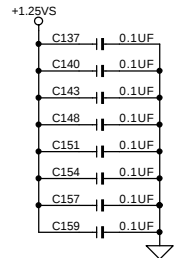




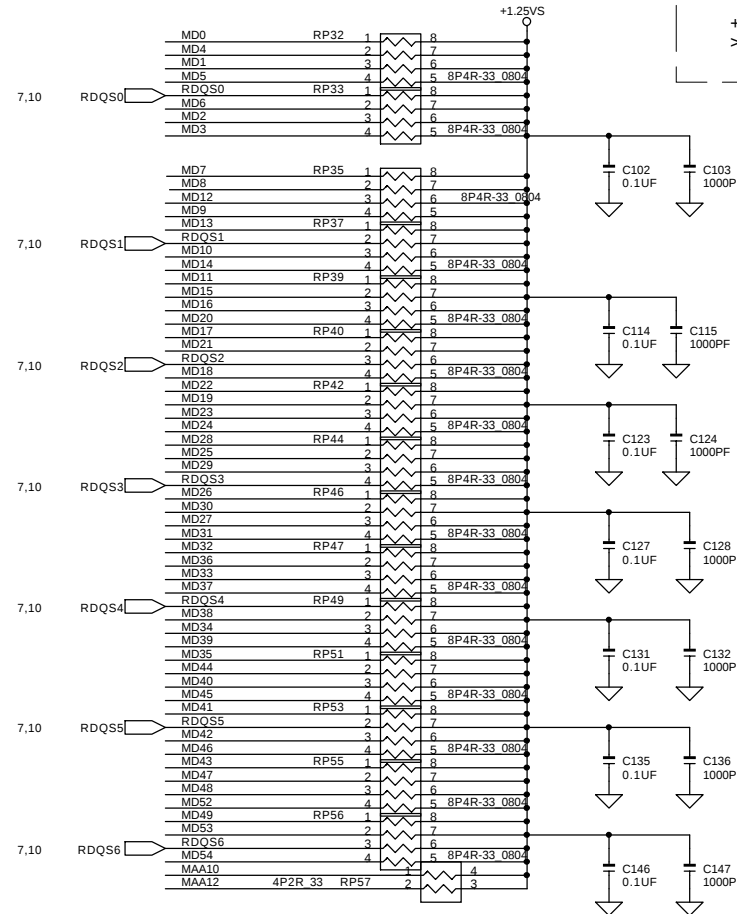
Decoupling capacitors
(Place near DDR SODIMM)



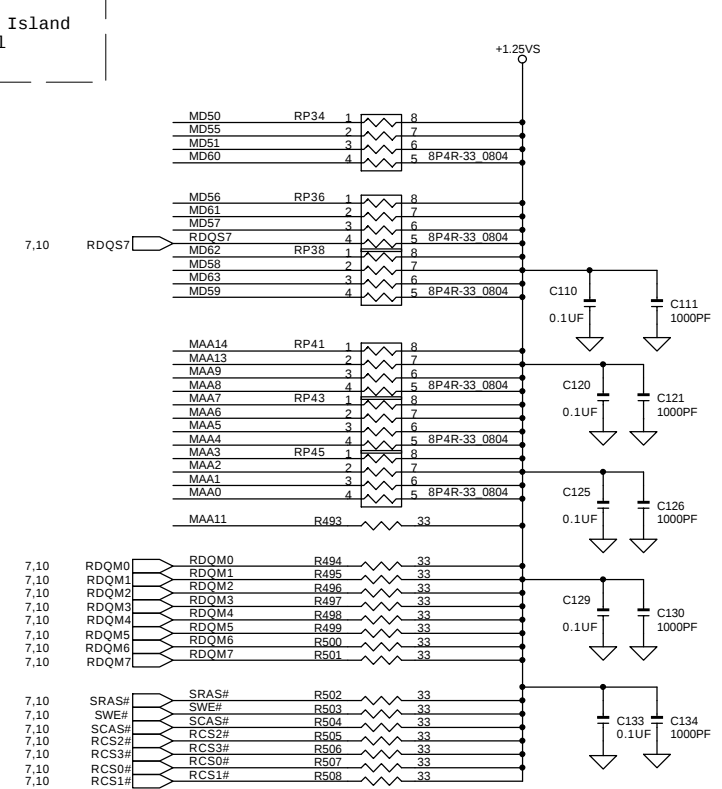
Place these decoupling capacitors close to
VTT_MEM termination resistors.



Termination Network place closely to DIMM



7,10 MD[0..63]
7,10 MAA[0..14]

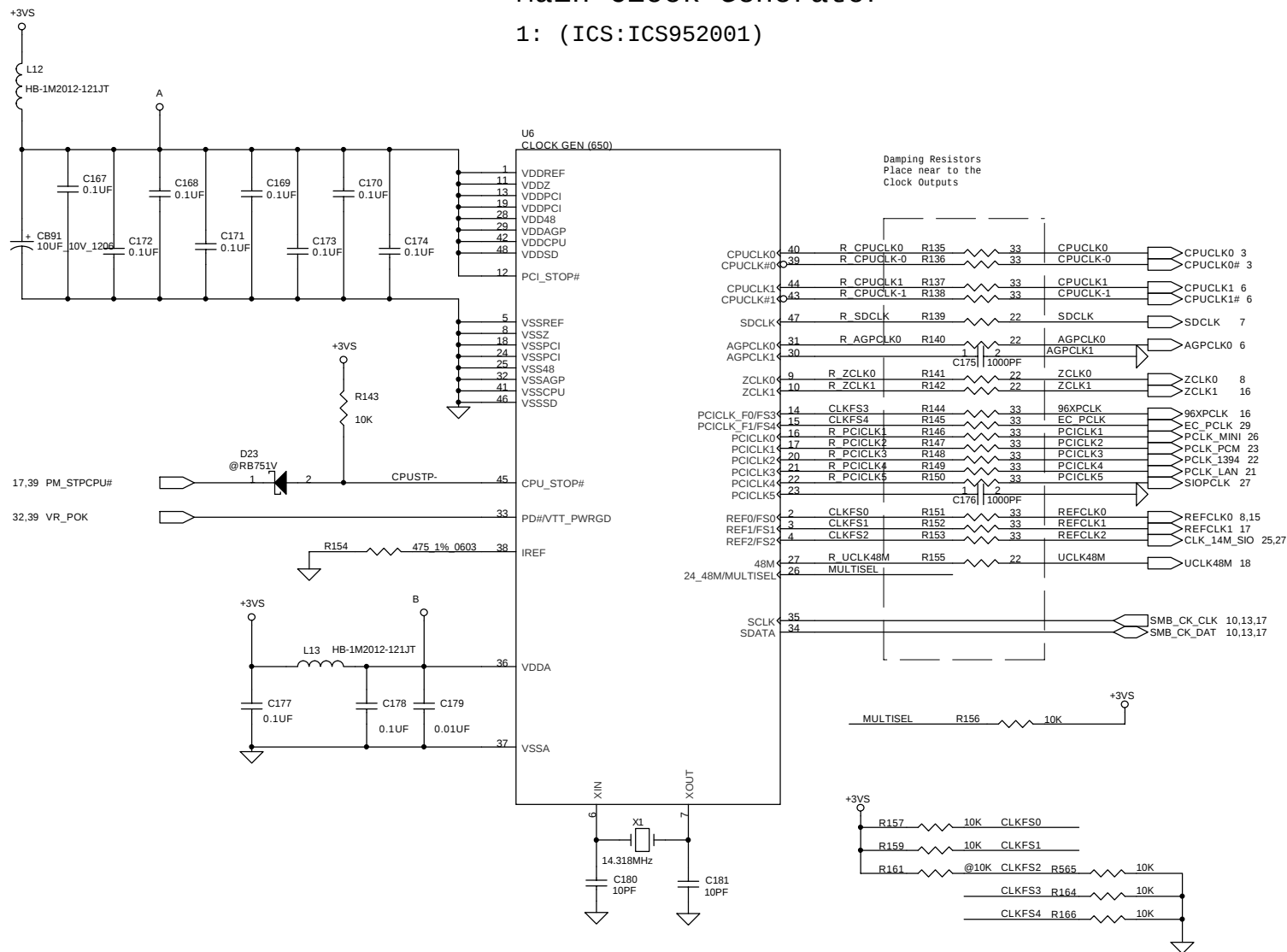


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Main Clock Generator

1: (ICS:ICS952001)



Place near to the Clock Outputs

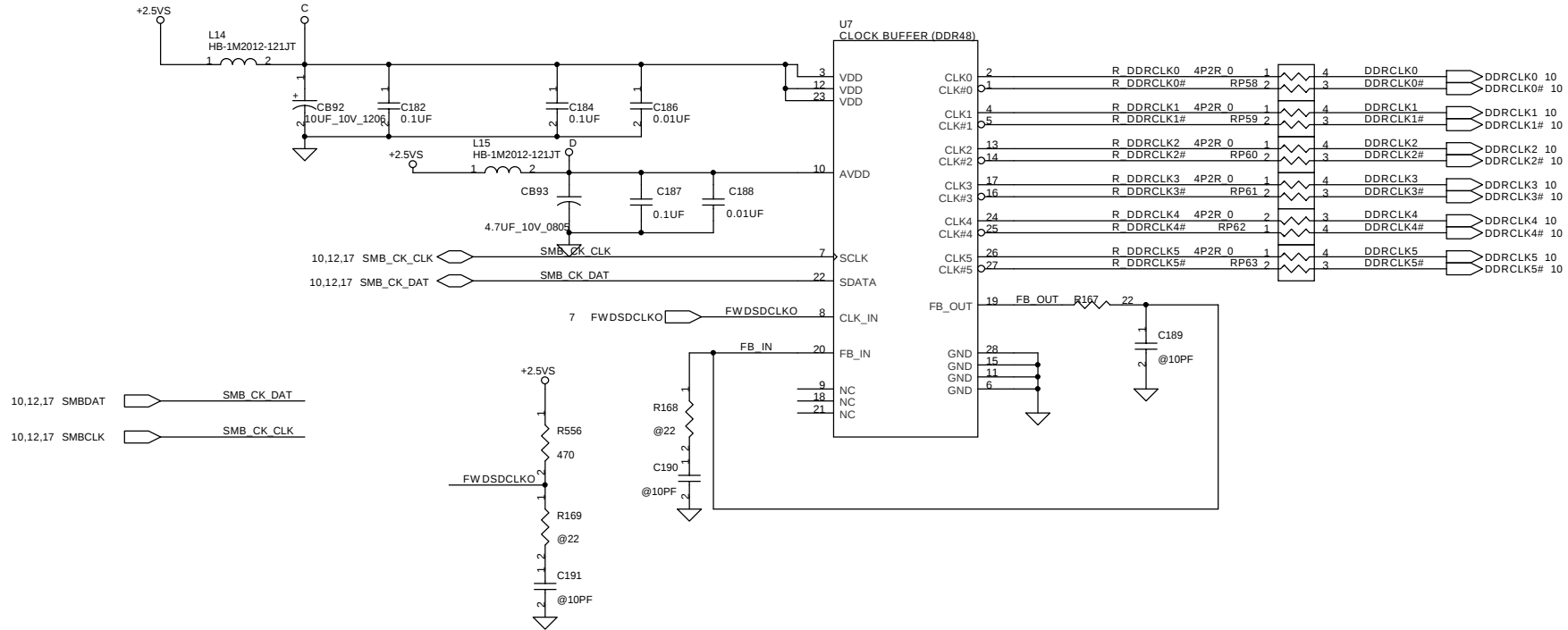
CPUCLK0	R131	49.9 1% 0603
CPUCLK-0	R132	49.9 1% 0603
CPUCLK1	R133	49.9 1% 0603
CPUCLK-1	R134	49.9 1% 0603

FS4	FS3	FS2	FS1	FS0	CPU	DDR	ZCLK	AGP	PCI
1	1	0	0	0	100.0	133.0	80.0	66.7	33.3
1	1	0	0	1	100.0	100.0	80.0	66.7	33.3
* 0	0	1	1	1	100.0	133.3	80.0	66.7	33.3

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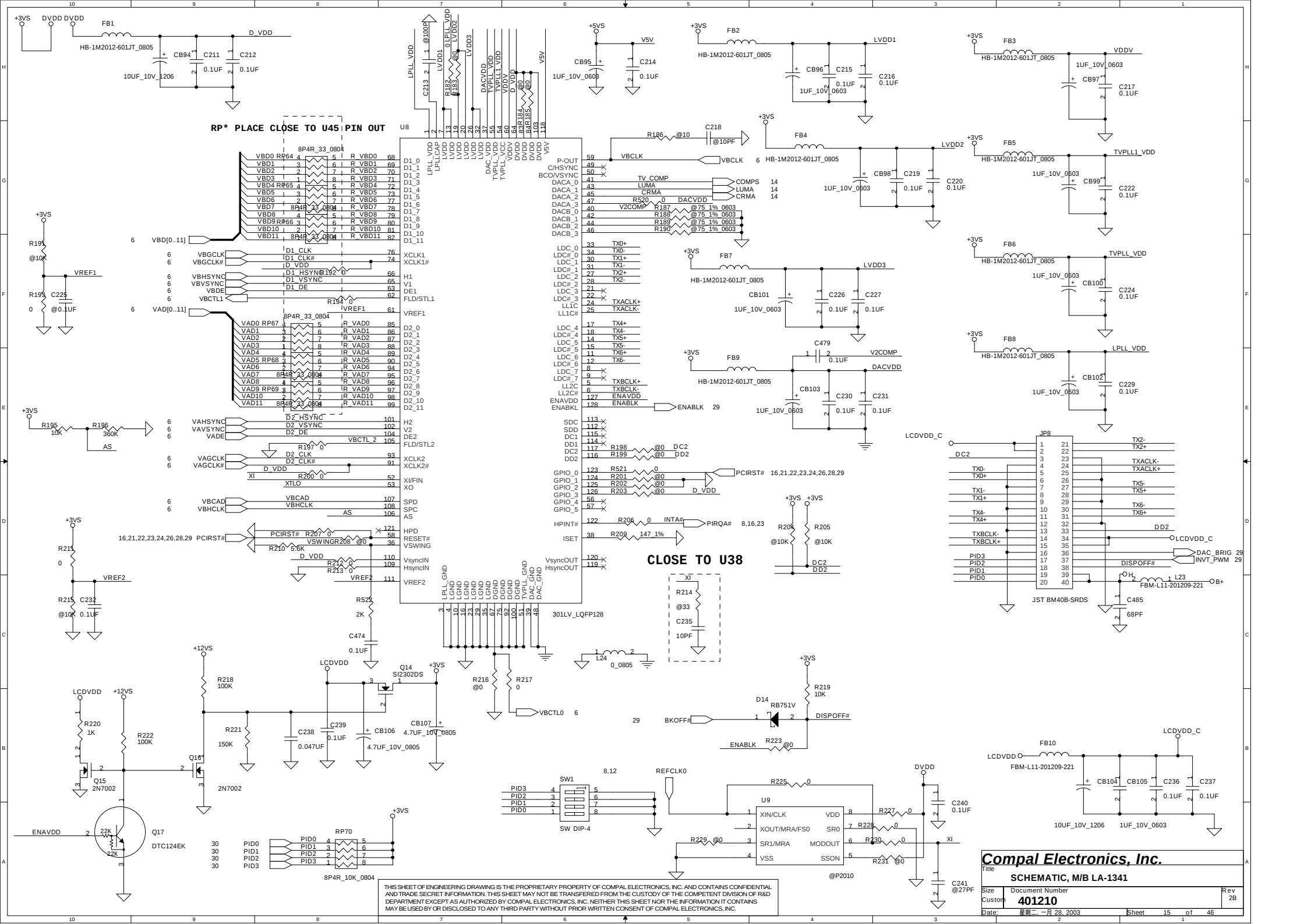
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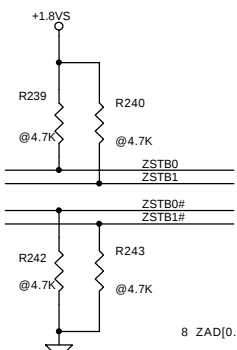
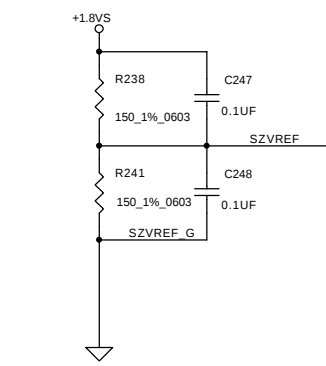
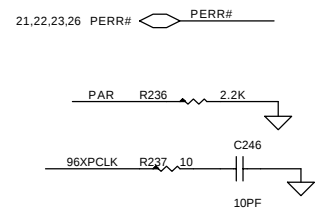
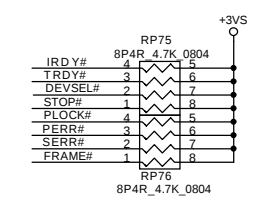
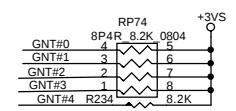
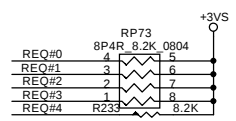
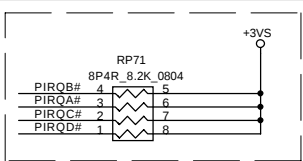
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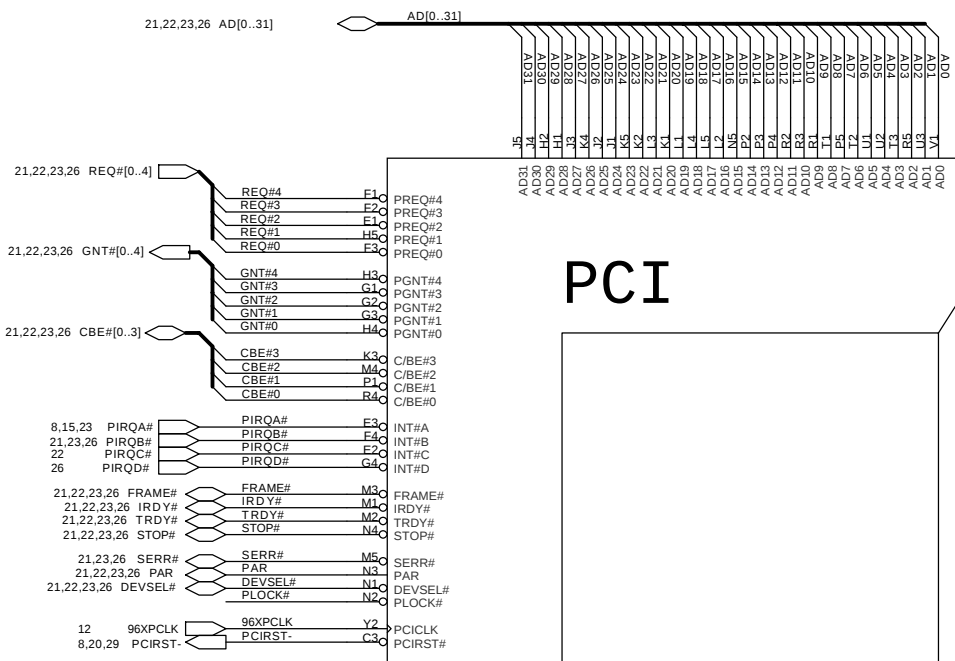
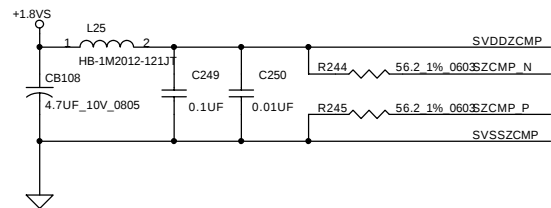
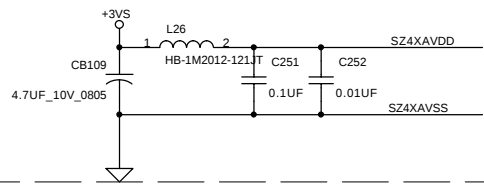
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Analog Power supplies of Transzip function for 961A Chip.



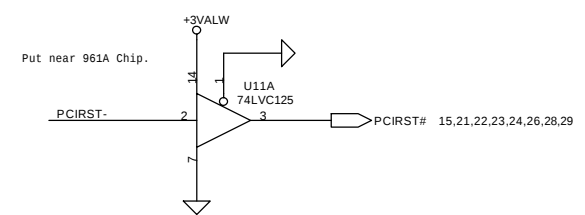
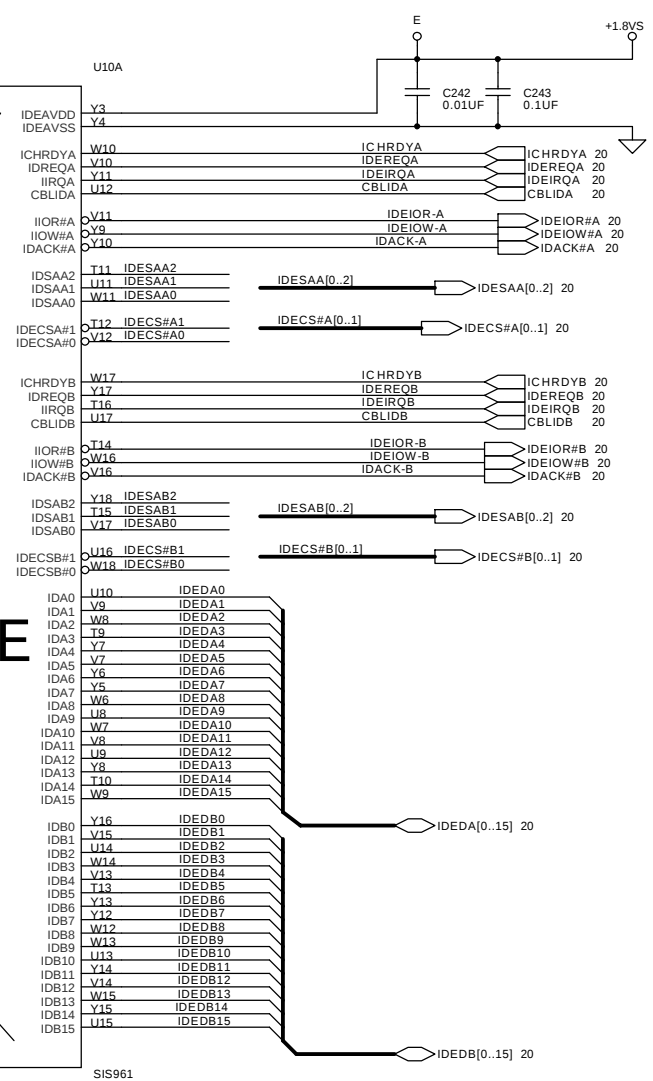
PCI

961-1

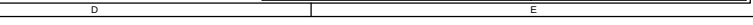
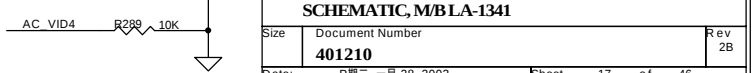
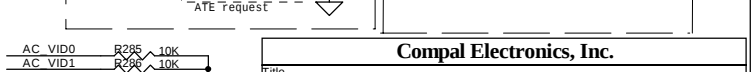
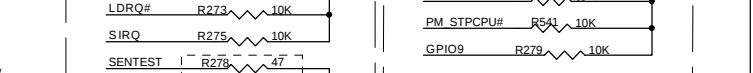
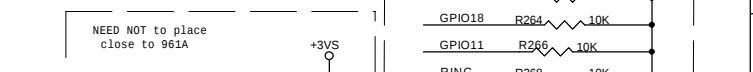
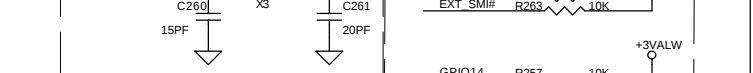
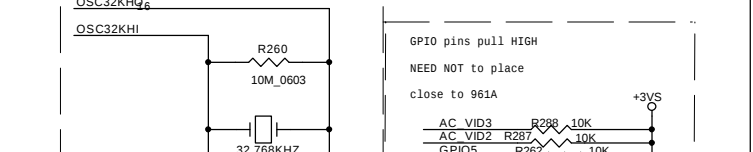
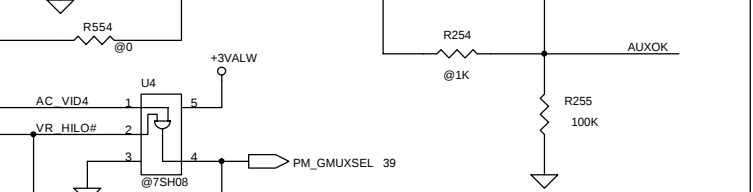
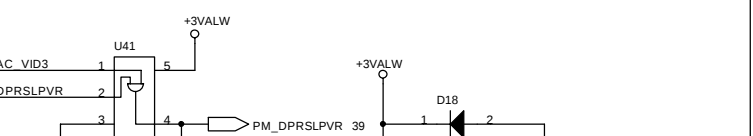
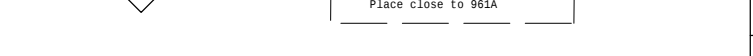
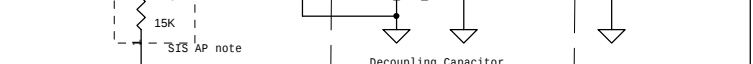
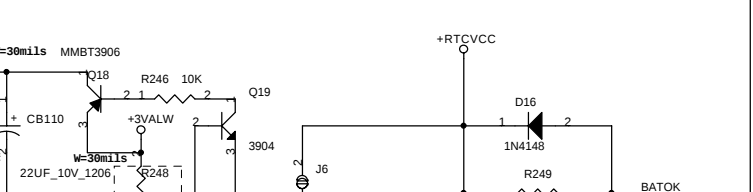
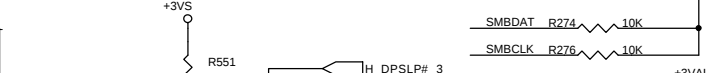
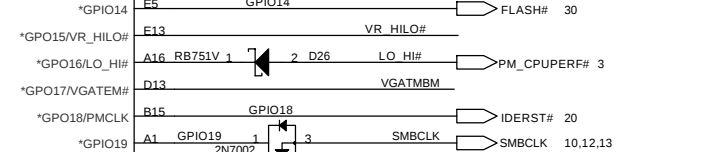
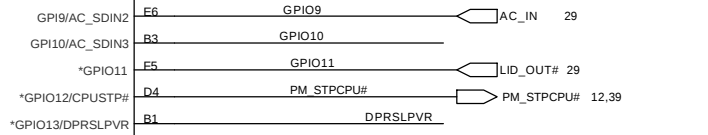
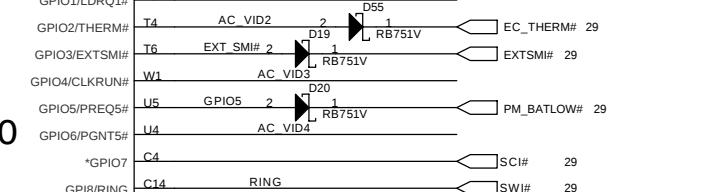
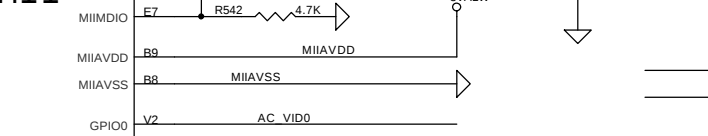
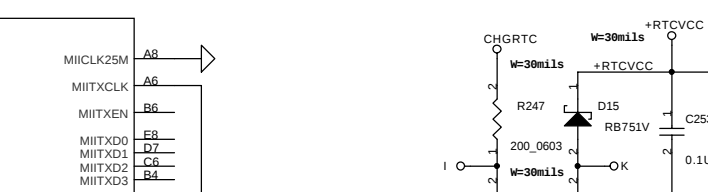
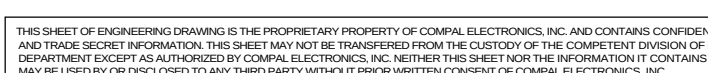
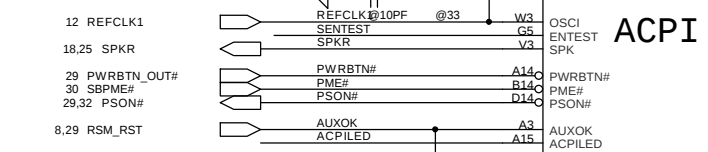
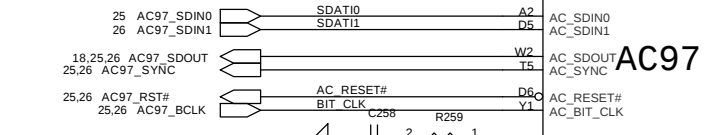
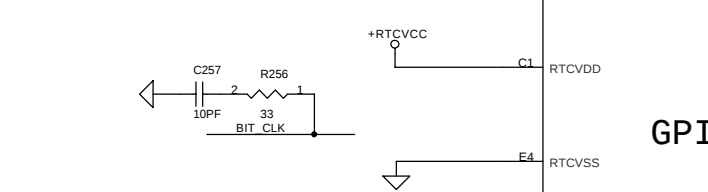
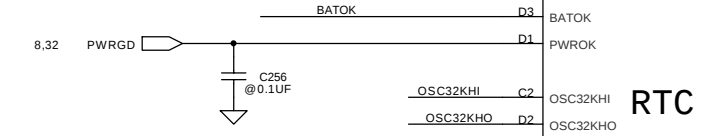
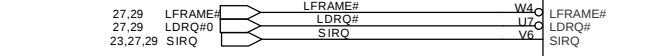
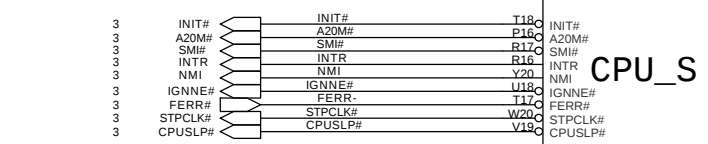
IDE

MULTIO

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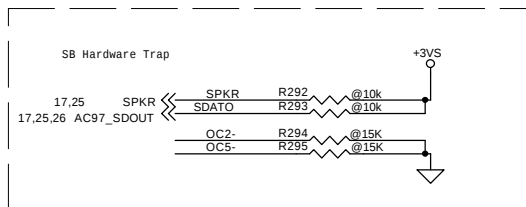
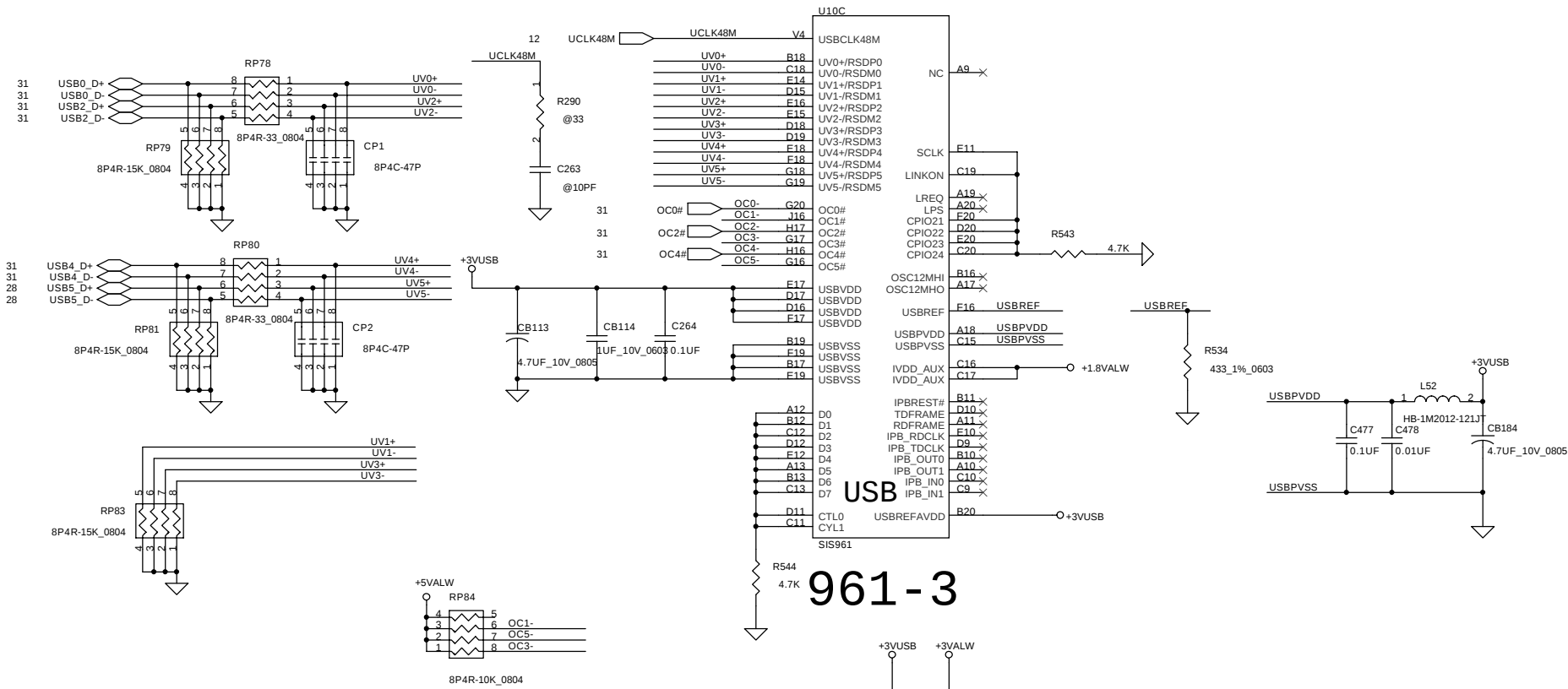


Programable on-die pull-high strength for CPU_S:
(Infinite, 150, 110, 56 Ohm)



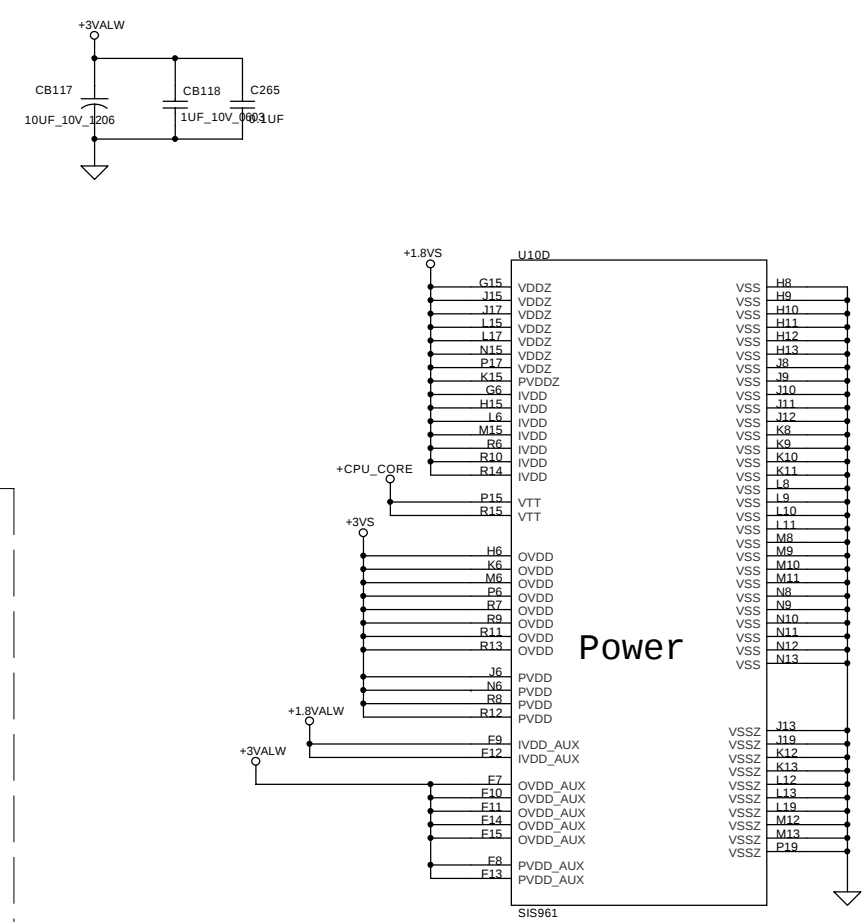
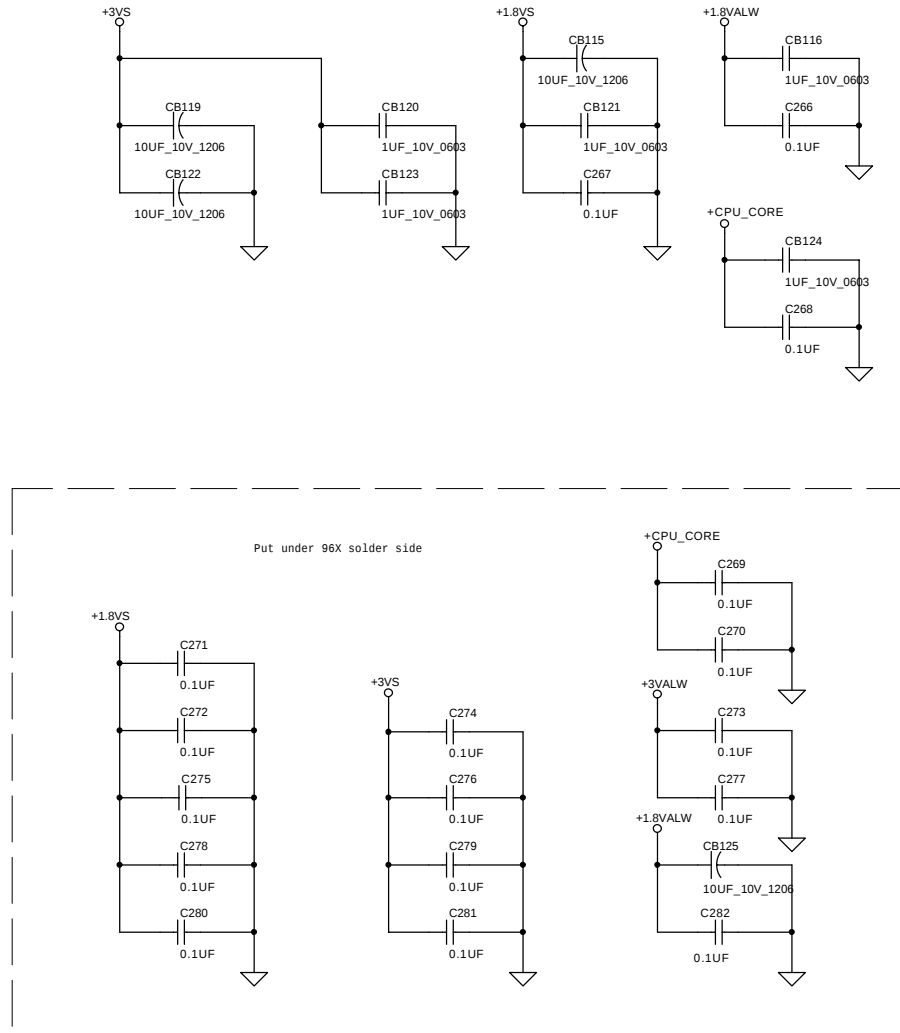
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	0	1	Default
SPKR(LPC addr mapping)	disable	enable	0
SDATO(PCICLK PLL)	enable	disable	0
OC2-(SB debug mode)	enable	disable	1
OC5-(Trap mode)	PCI AD	ROM	1

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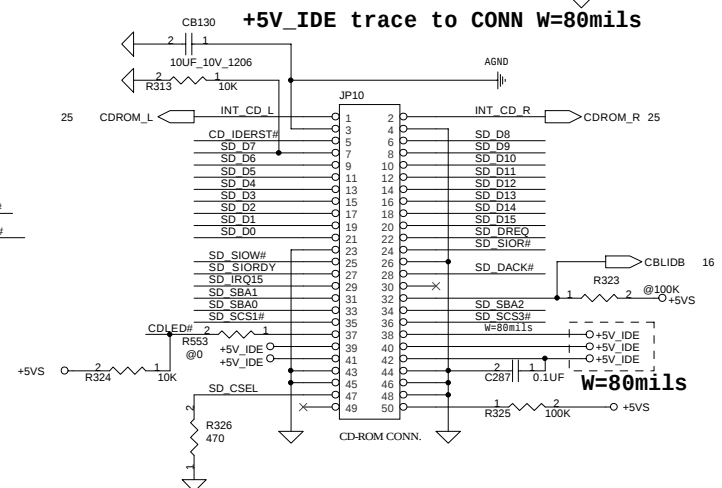
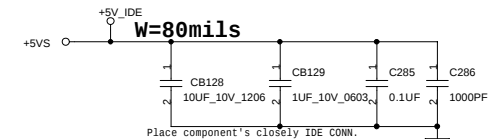
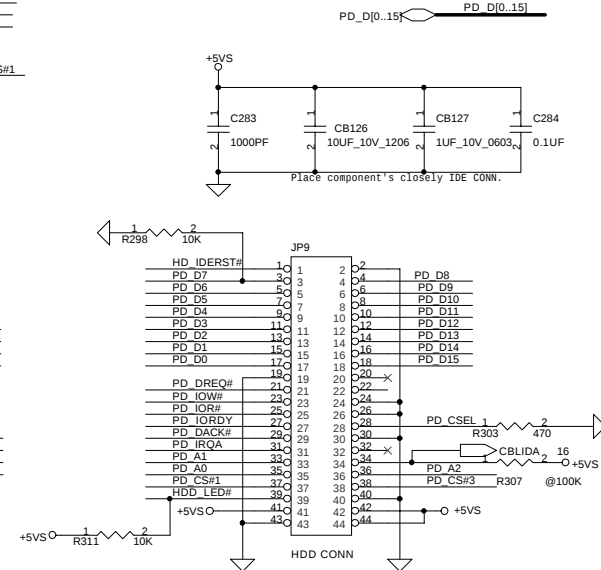
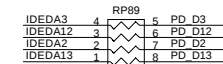
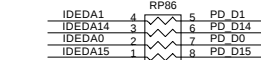
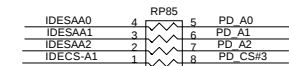
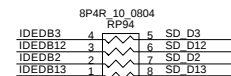
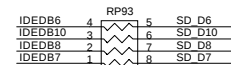
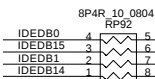
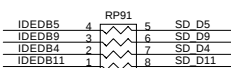
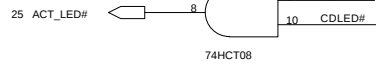
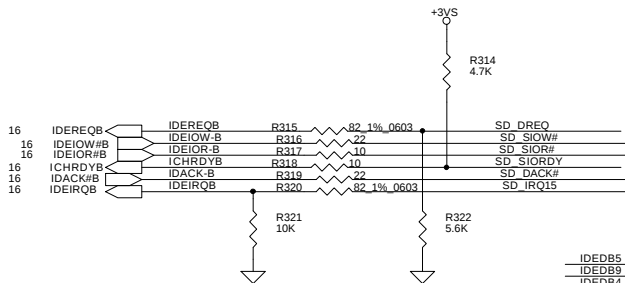
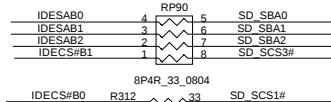
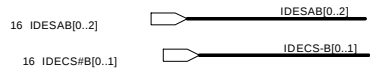
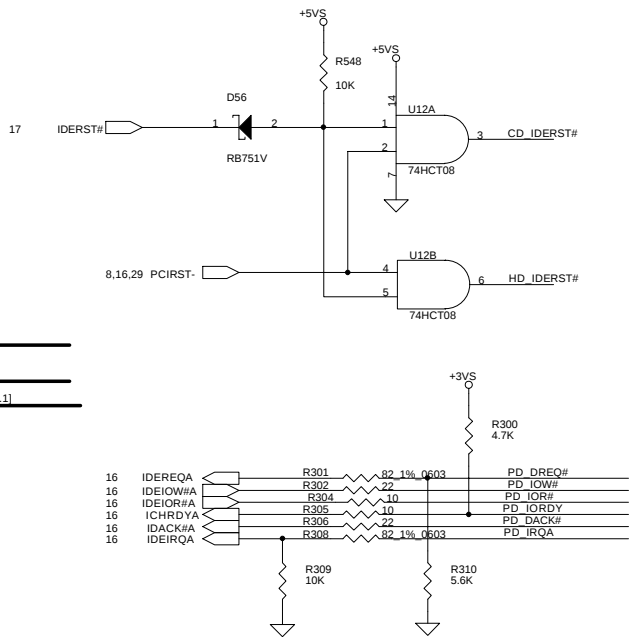


961-4

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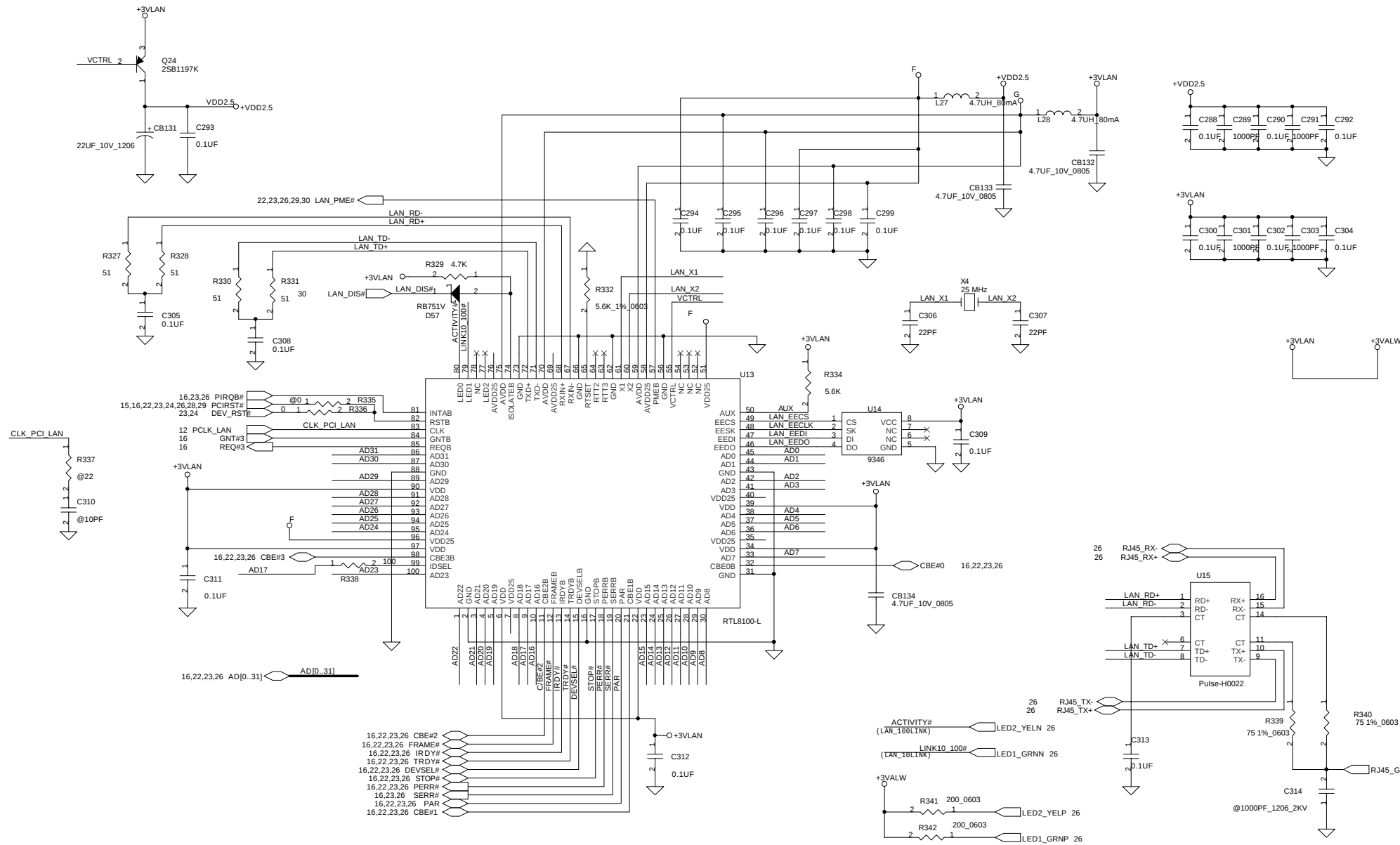
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HDD/CD-ROM Module



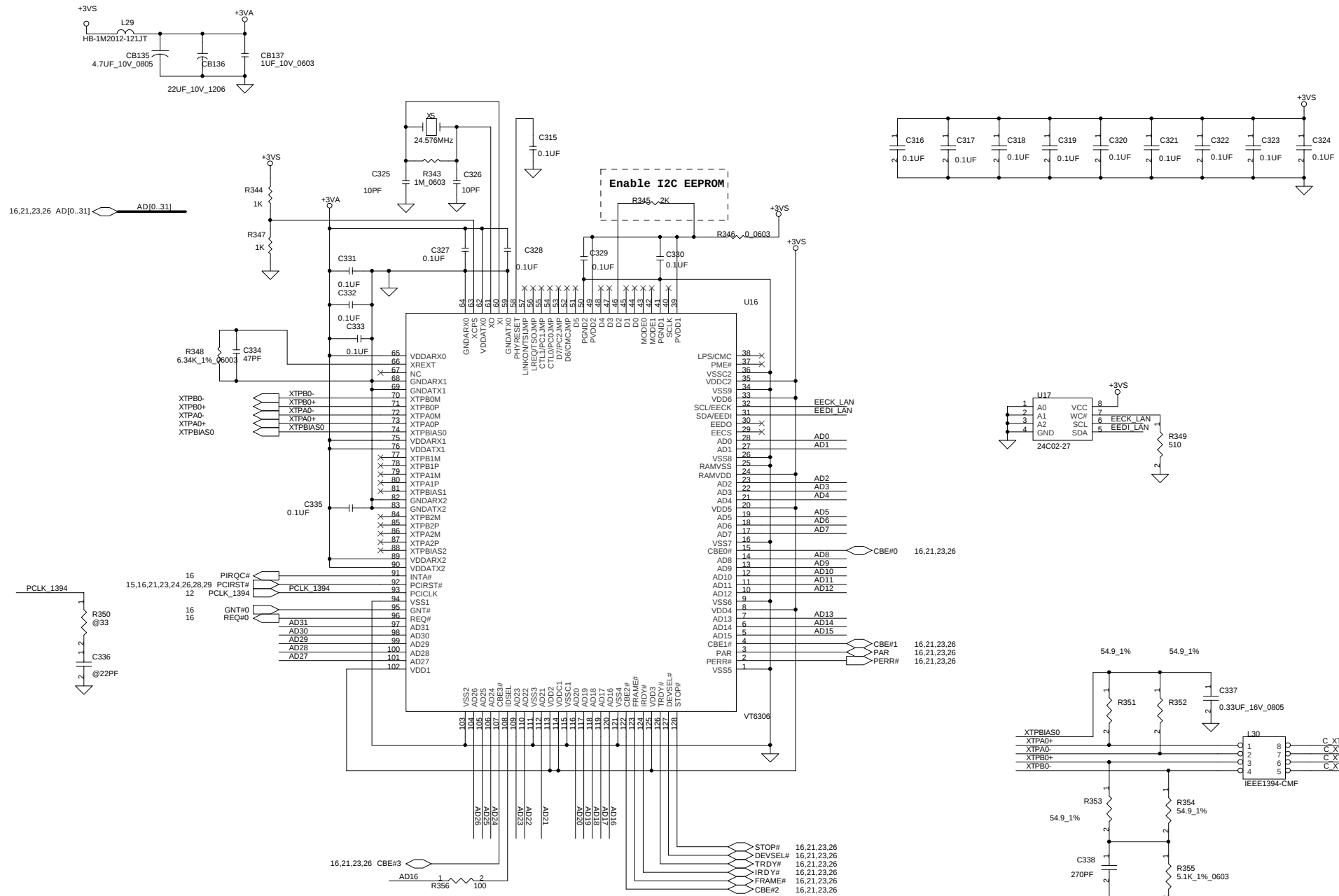
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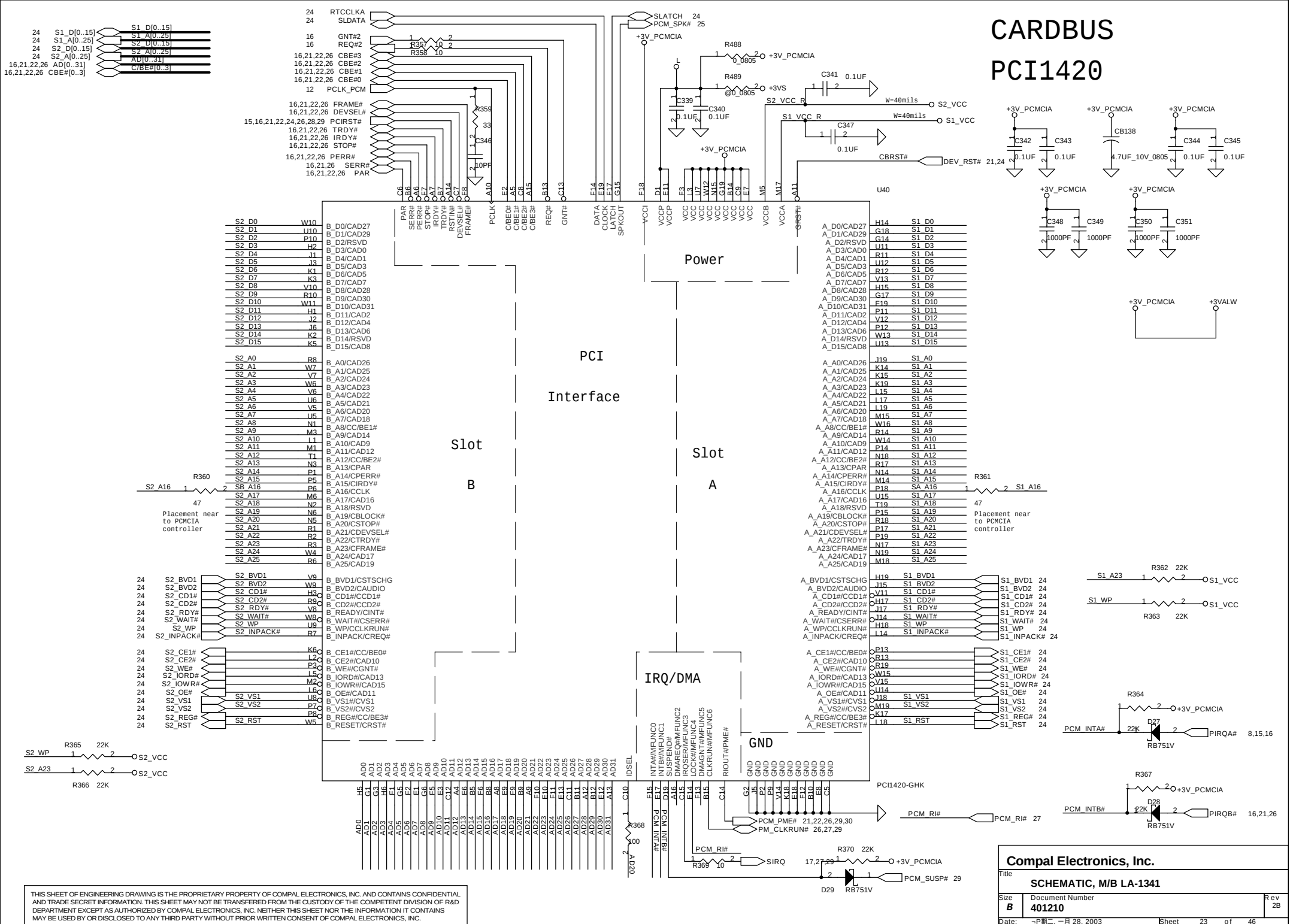


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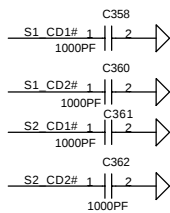
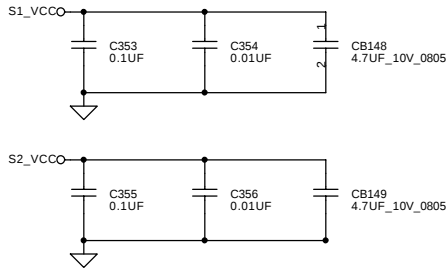
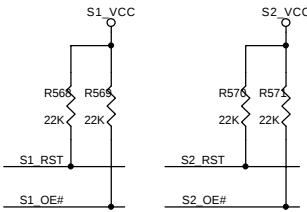
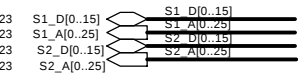
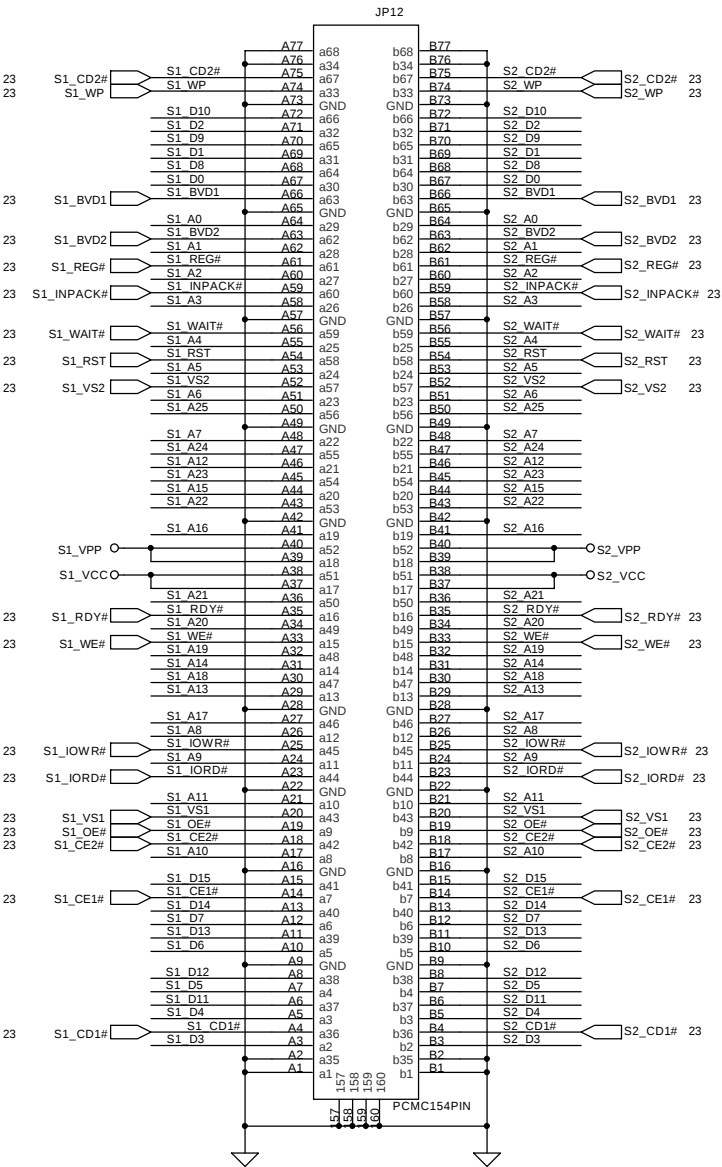
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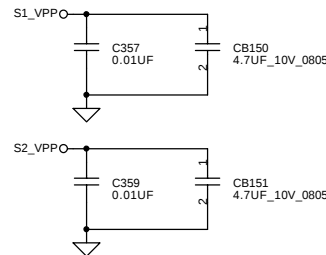
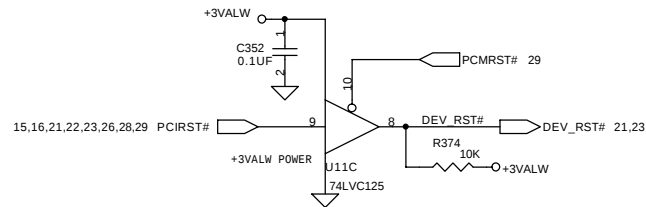
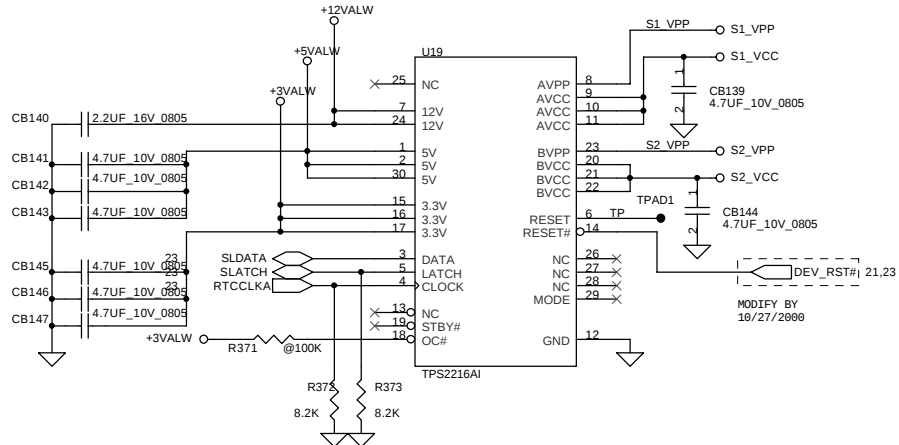
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CARDBUS SOCKET

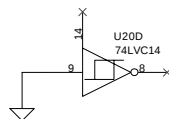
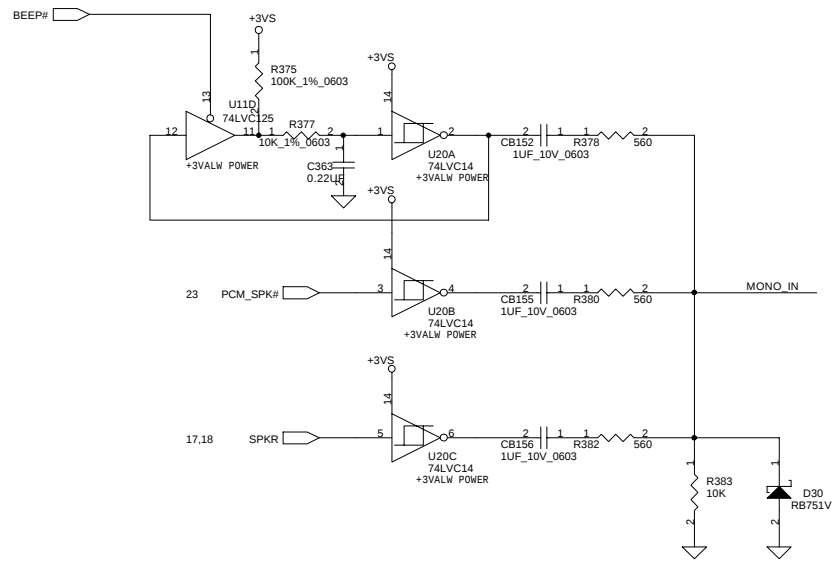


PCMCIA POWER CTRL.

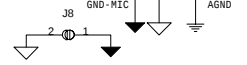
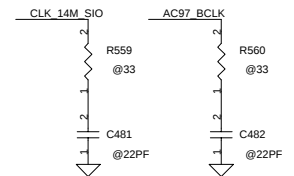
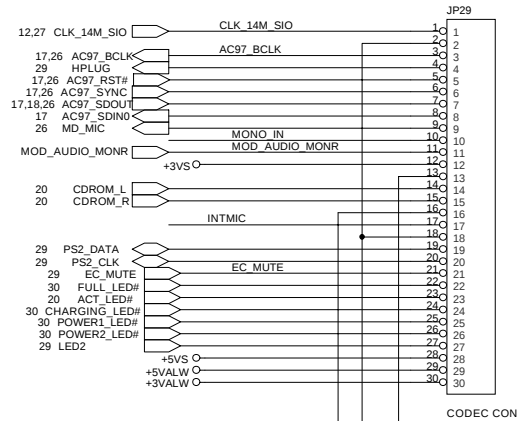
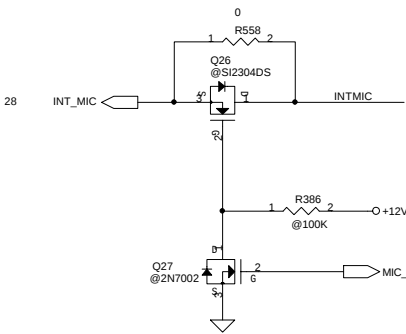
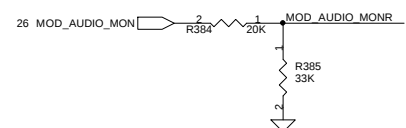


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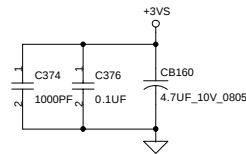
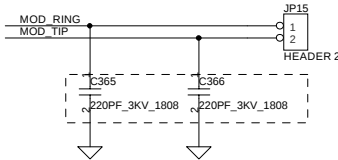
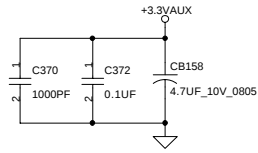
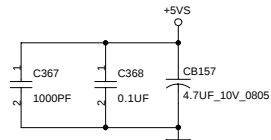
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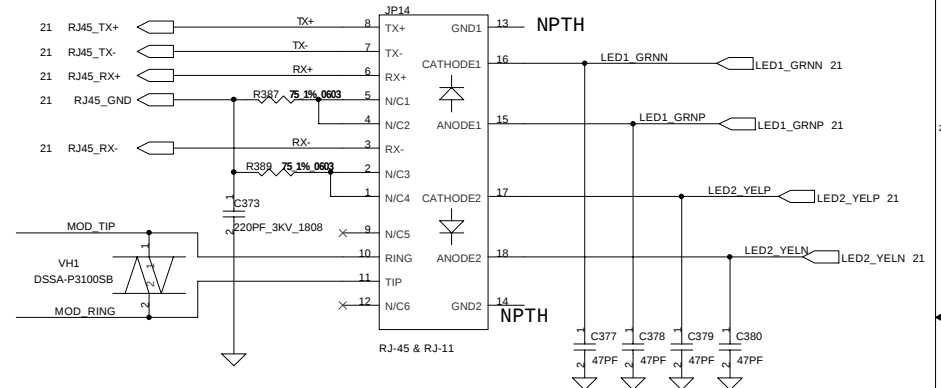
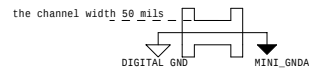
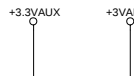
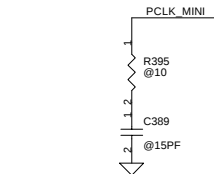
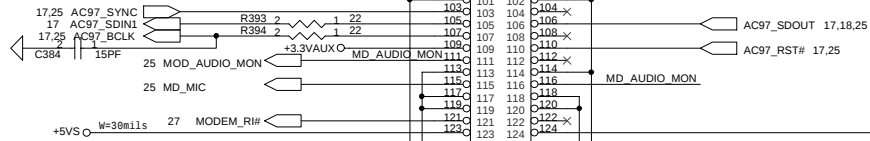
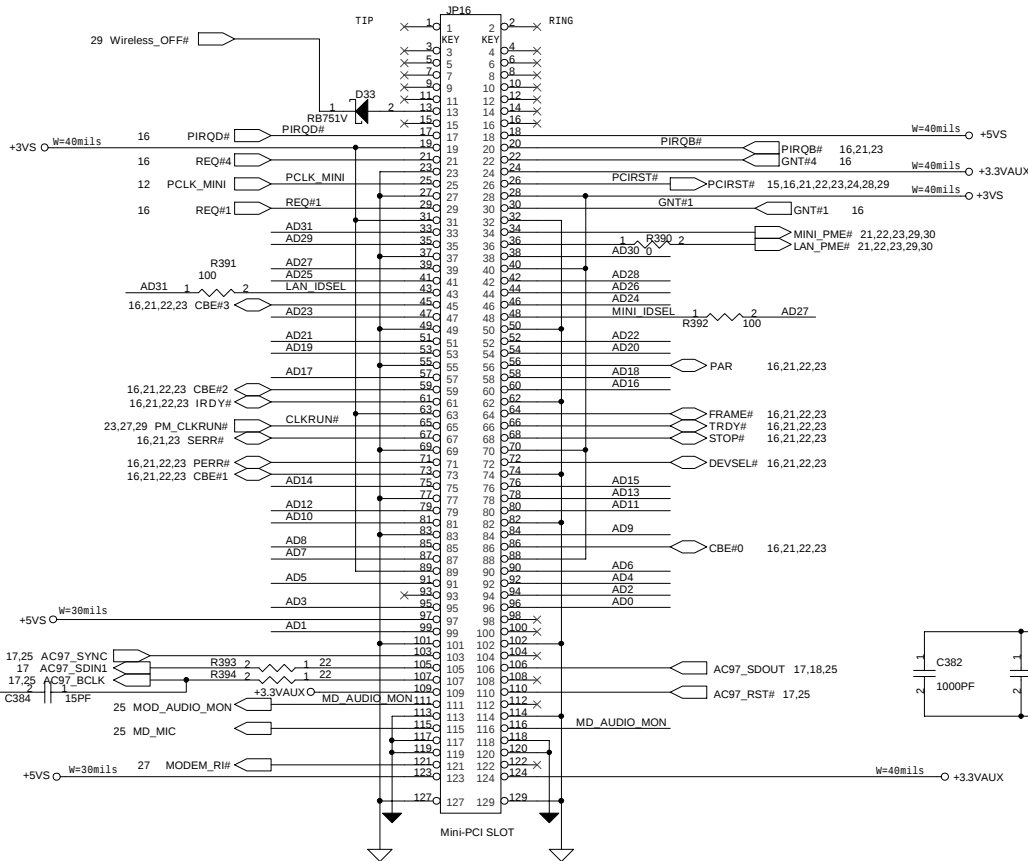
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Mini-PCI Slot



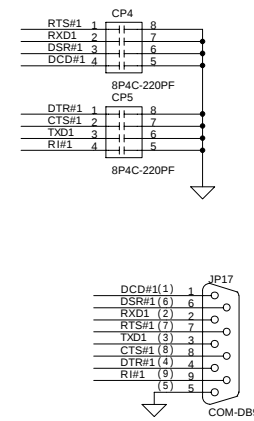
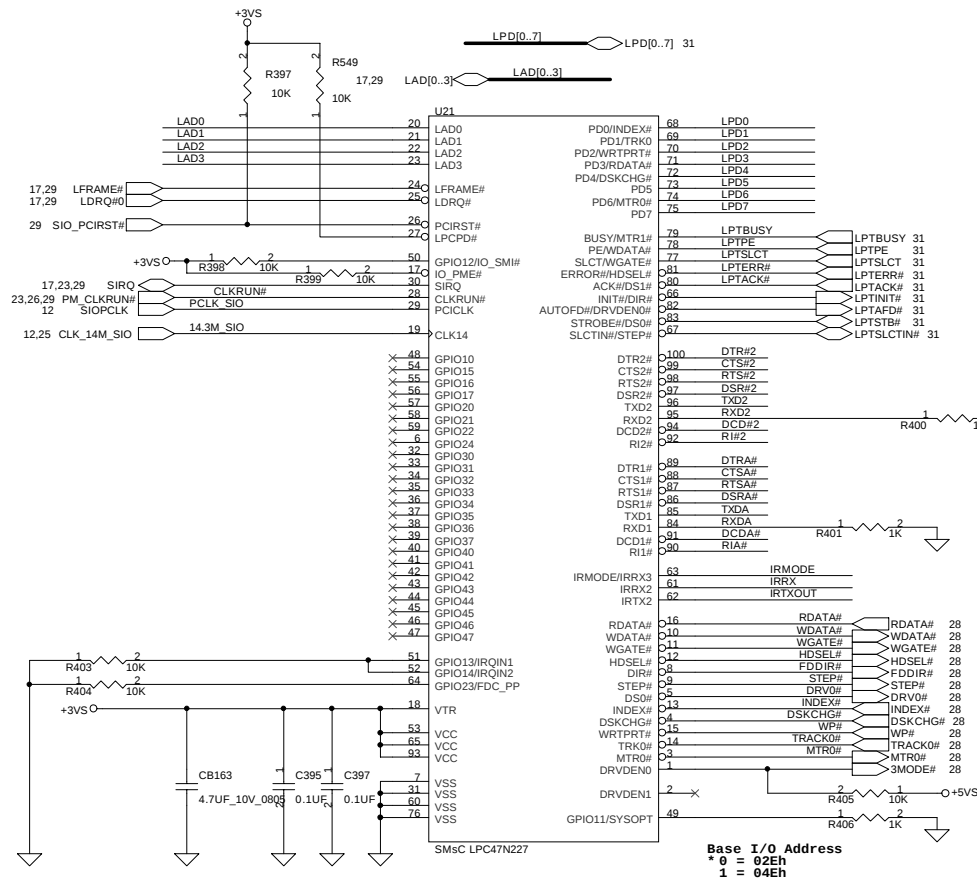
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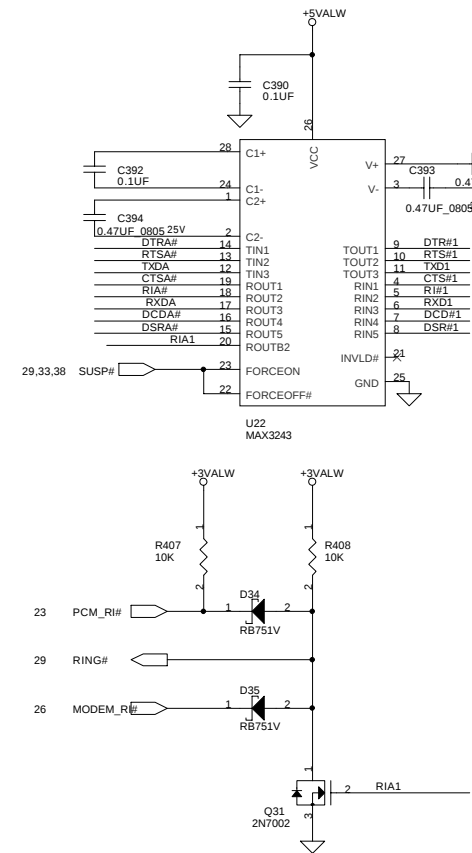
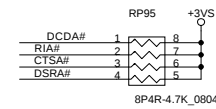
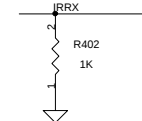
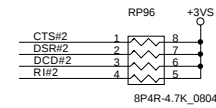
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SUPER I/O SMsC LPC47N227



SERIAL PORT



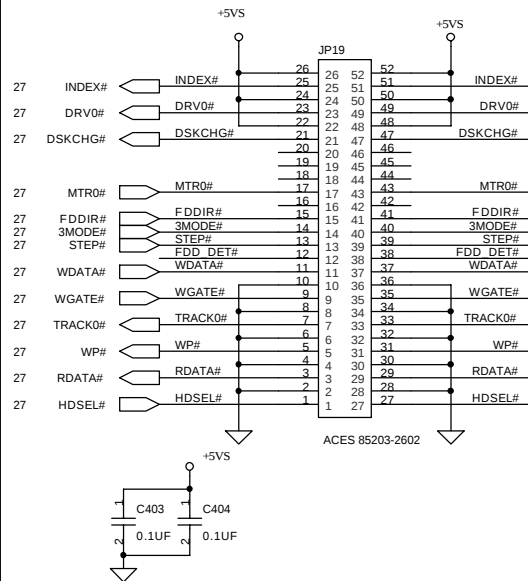
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SCHEMATIC, M/B LA-1341

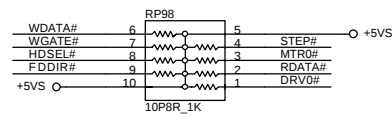
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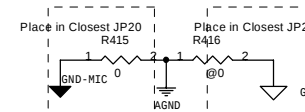
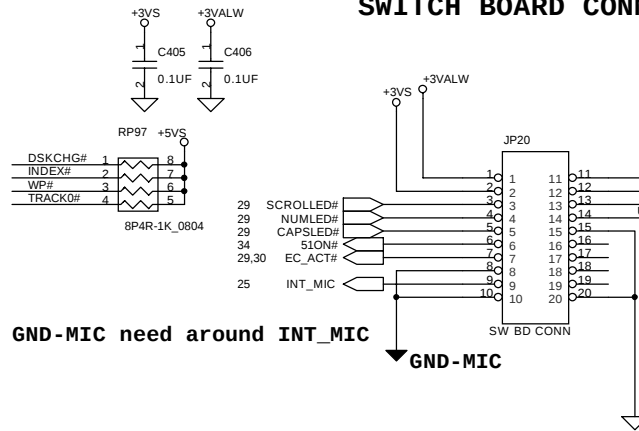
FDD CONN.



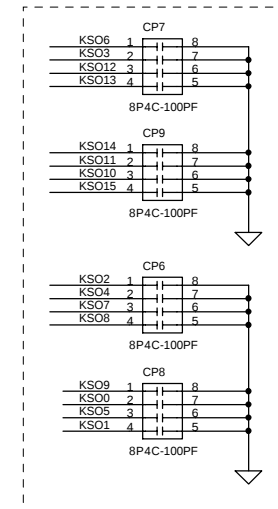
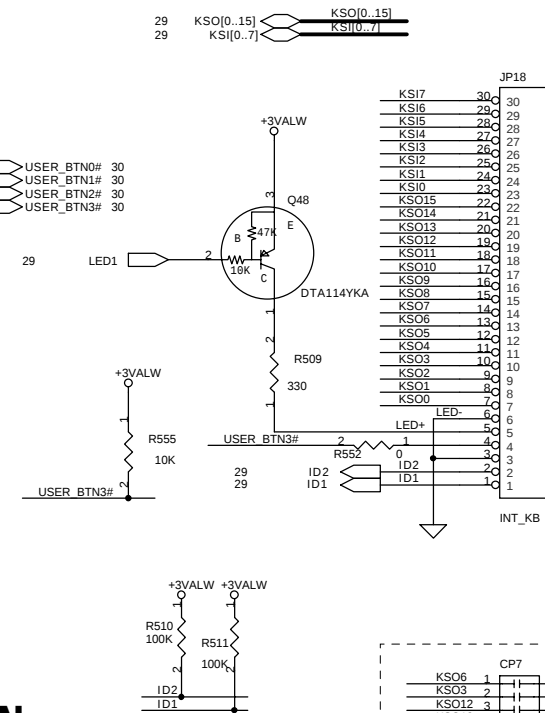
GND-MIC need around INT_MIC



SWITCH BOARD CONN.

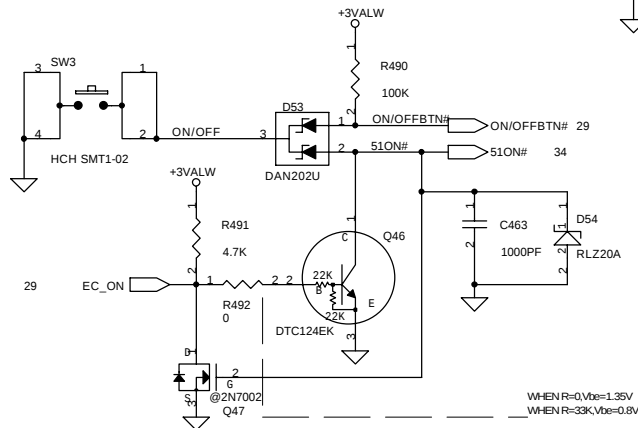


INT_KBD CONN.

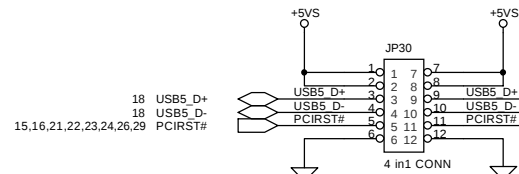


NEED CLOSEST JP18 ADD BY EMI REQUEST

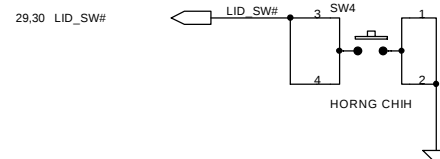
ON/OFF BUTTON



4 IN 1 CONN

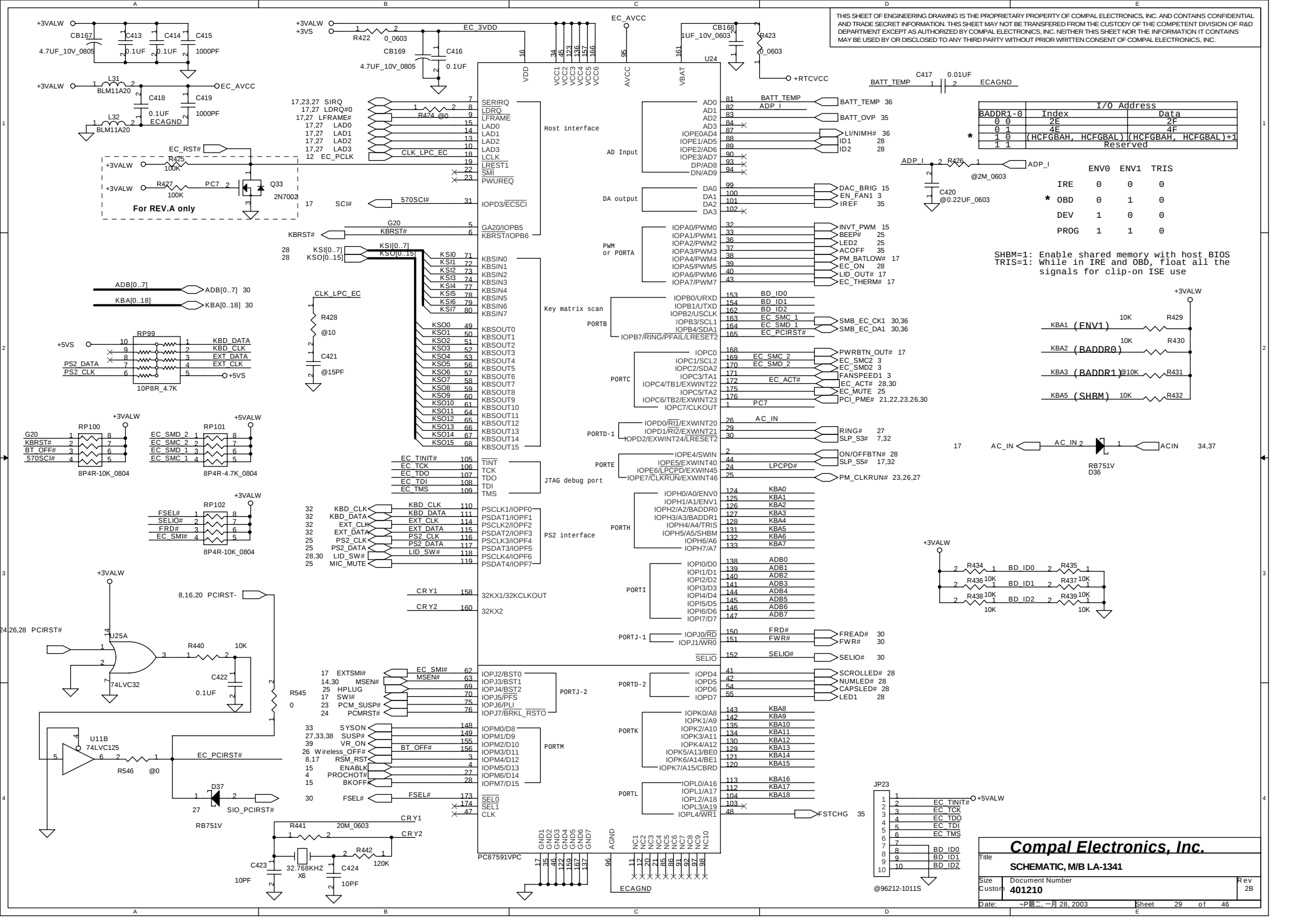


LID SW



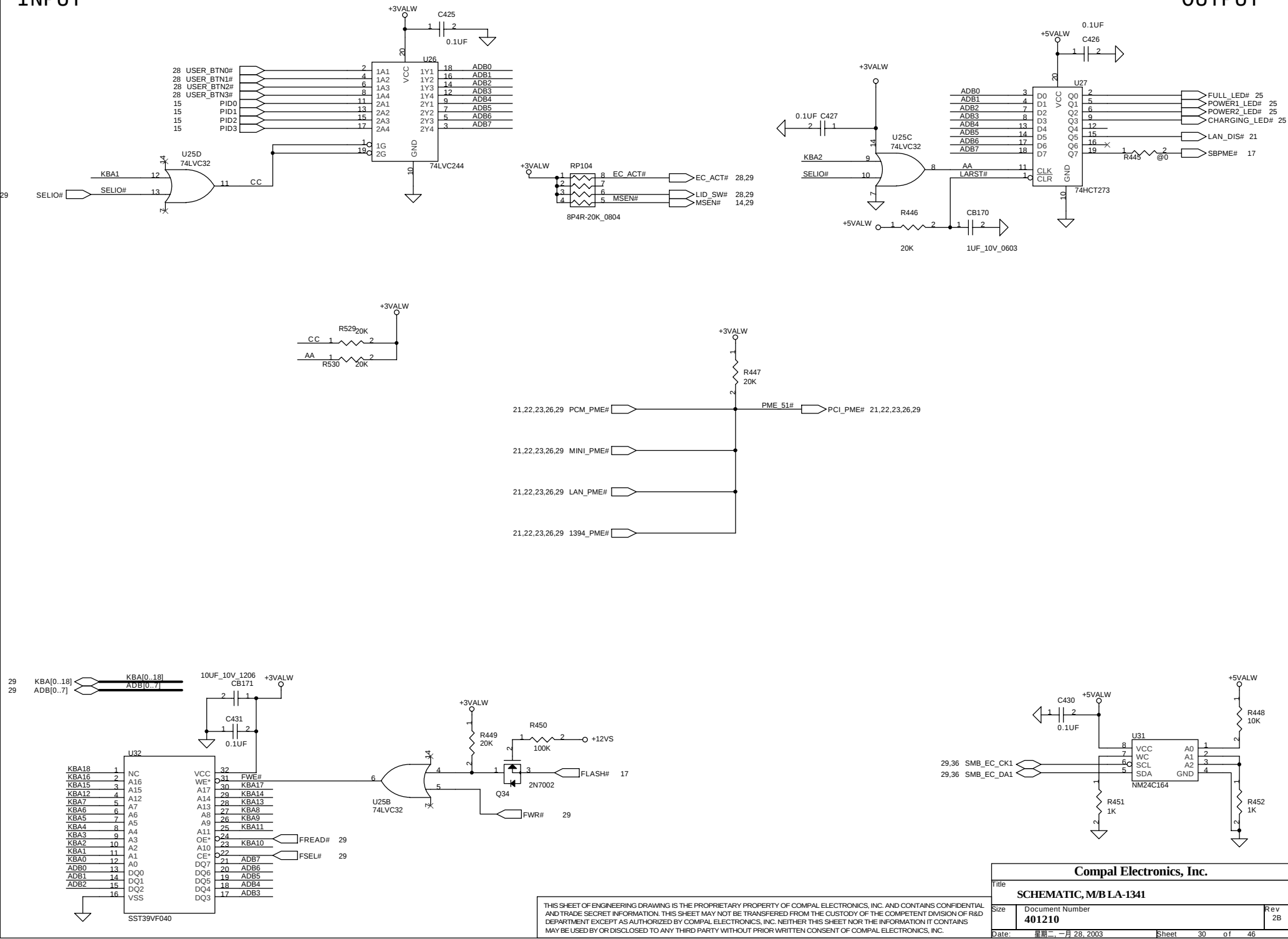
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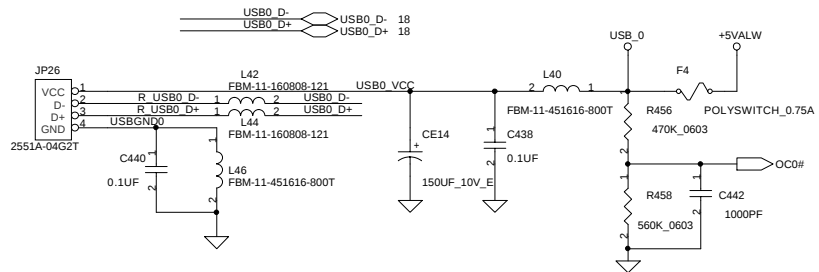


INPUT

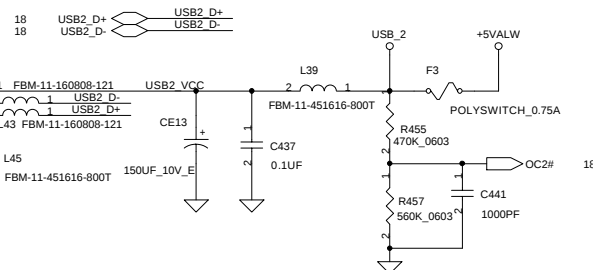
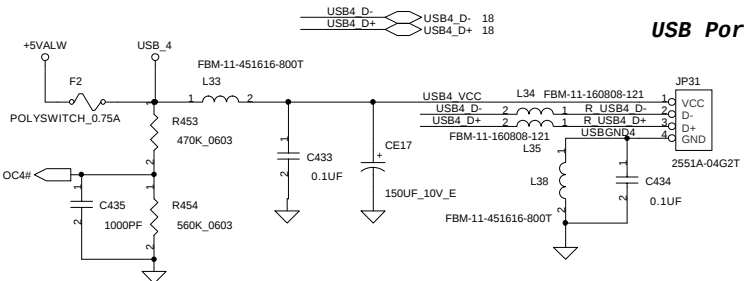
OUTPUT



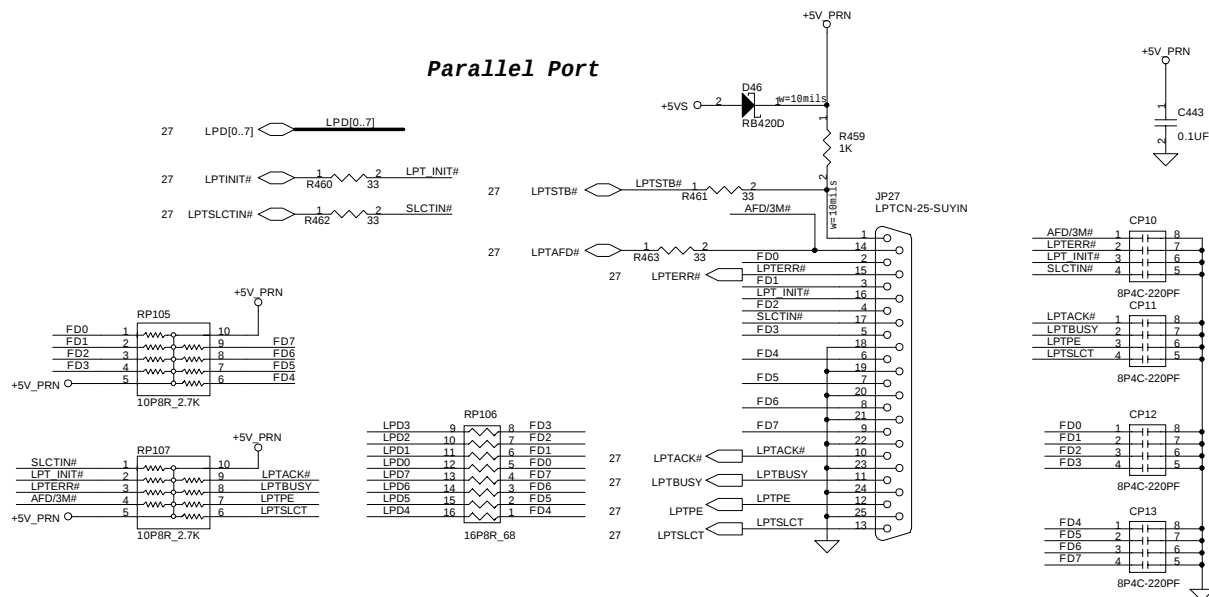
Printer Port/USB



USB Port

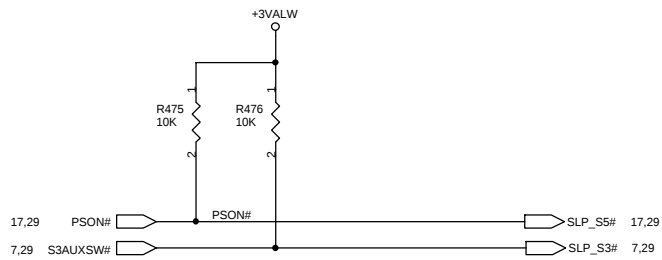
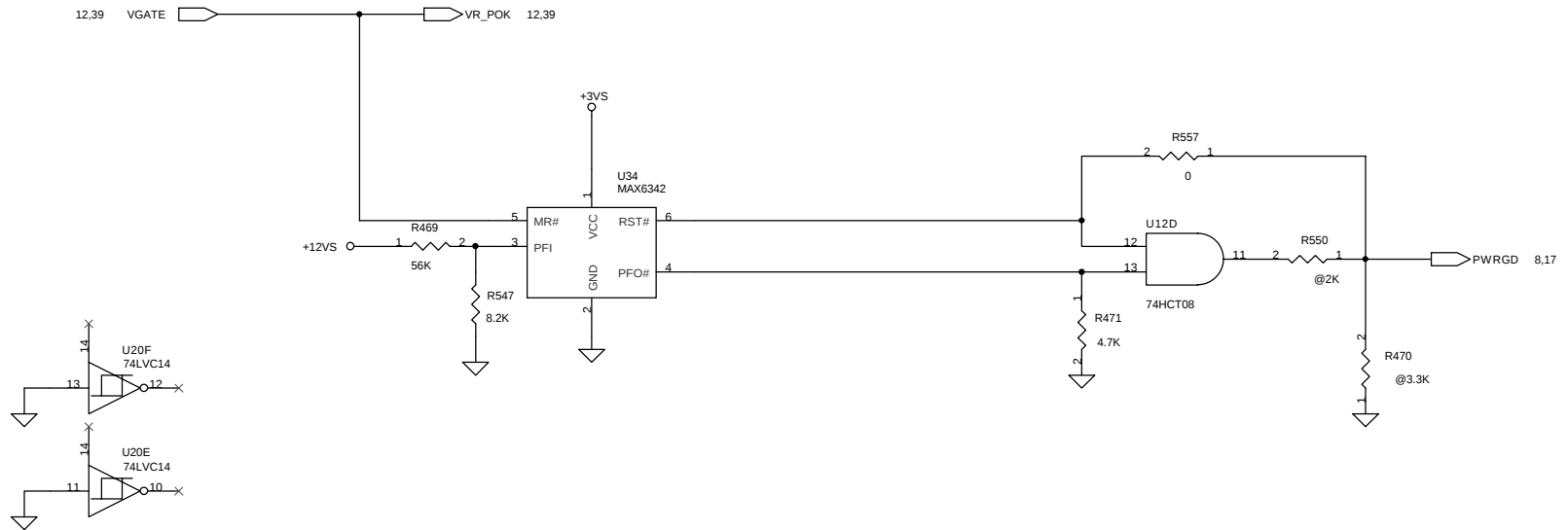


Parallel Port

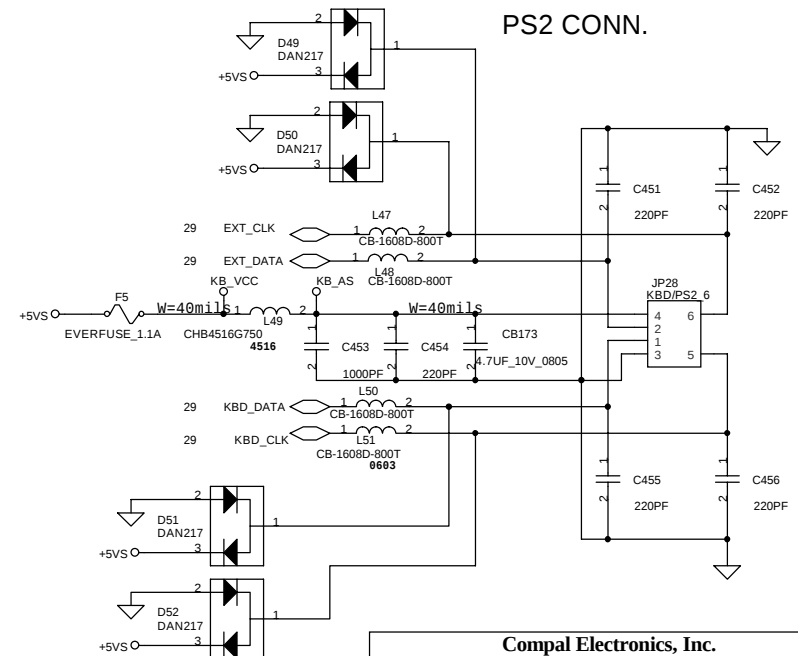


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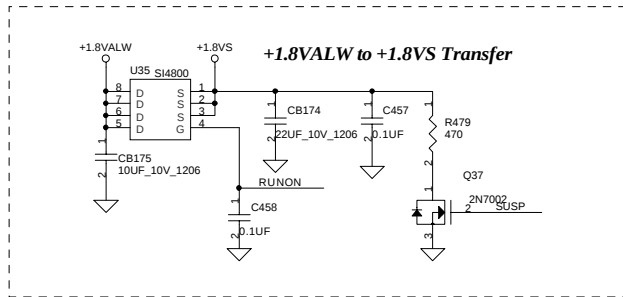


	S1	S3	S5
S3AUXSW#	1	0	1
PSON#	0	1	1
SLP_S3#	1	0	0
SLP_S5#	1	1	0

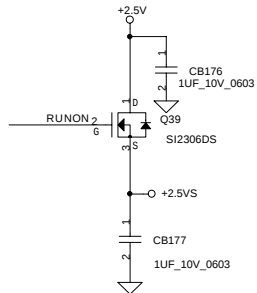


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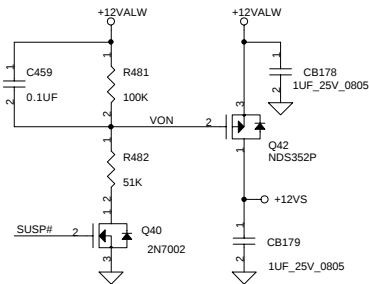


+2.5V to +2.5VS Transfer

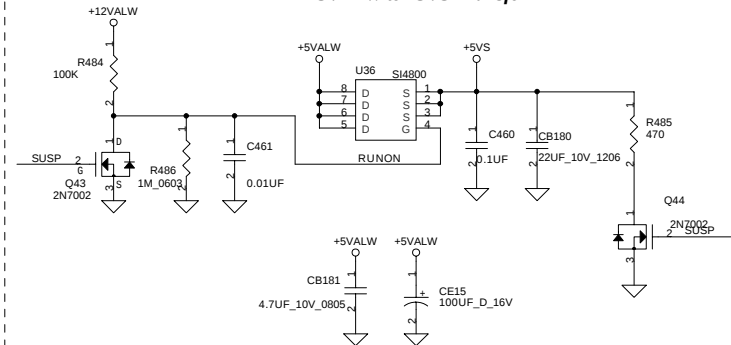


1.8VALW/+1.5VS Power direct provide

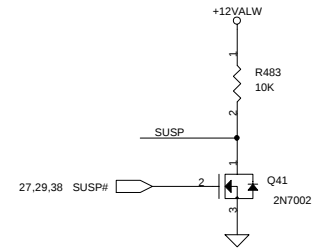
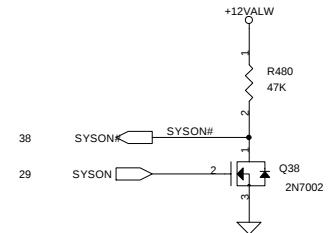
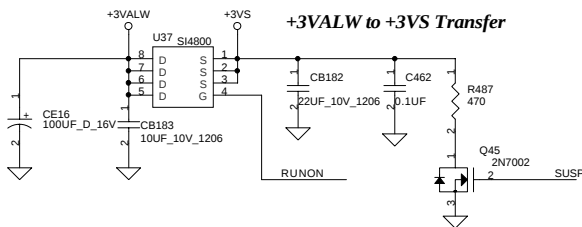
+12VALW TO +12VS Transfer



+5VALW to +5VS Transfer

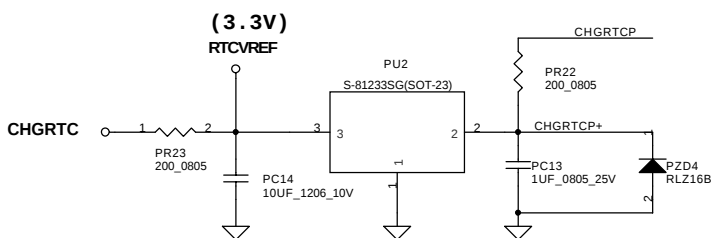
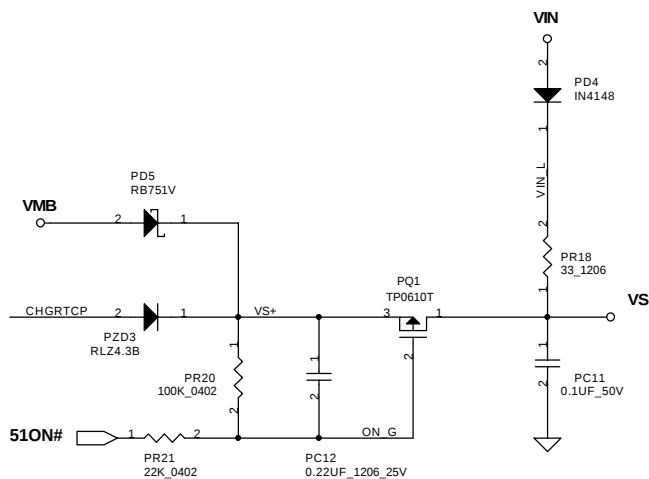
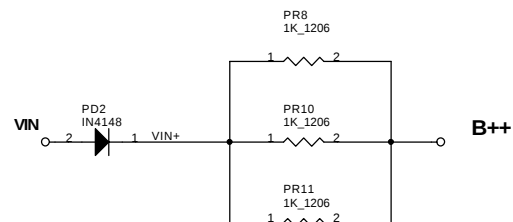
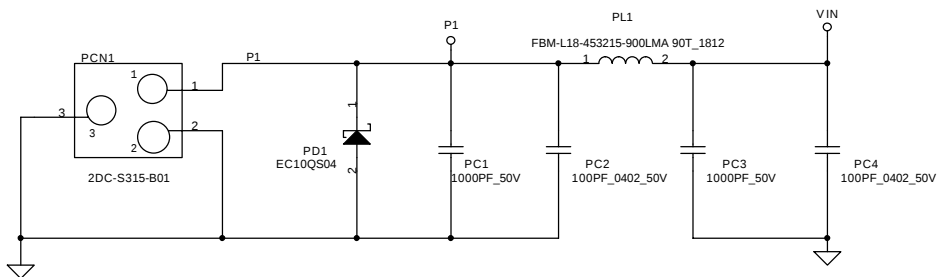


+3VALW to +3VS Transfer



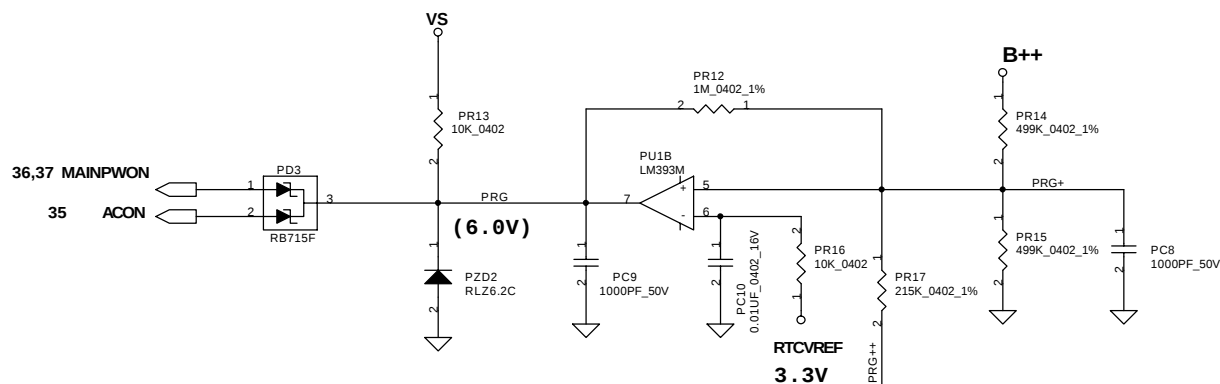
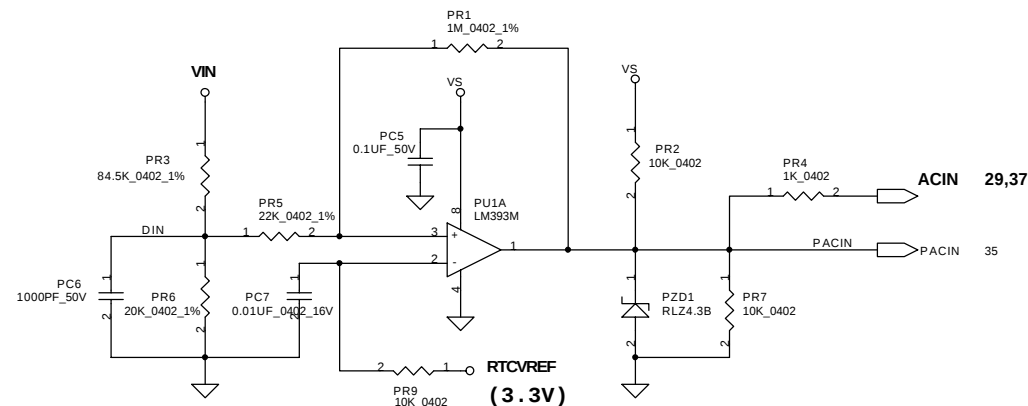
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Vin Detector

High 18.784 17.901 17.077 V
Low 17.877 17.043 16.195 V

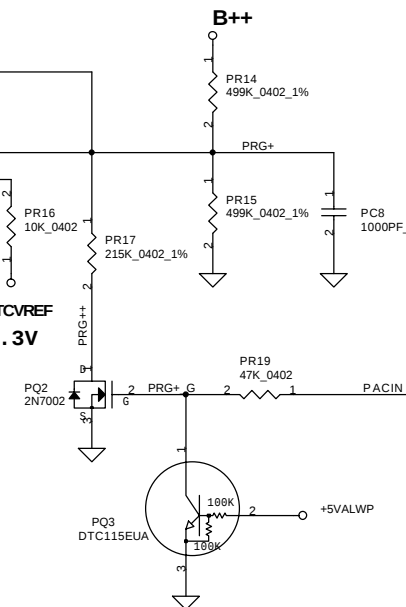


ACIN

Precharge detector
16.6 15.9 15.2
13.48 12.93 12.09

BAT ONLY

Precharge detector
8.597 8.247 7.904
6.310 6.101 5.683

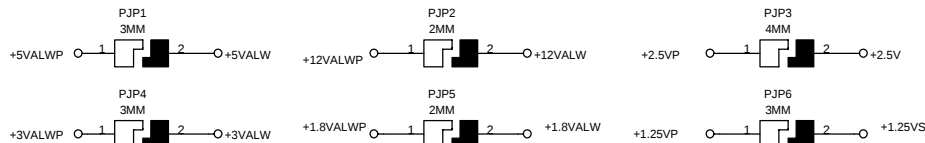


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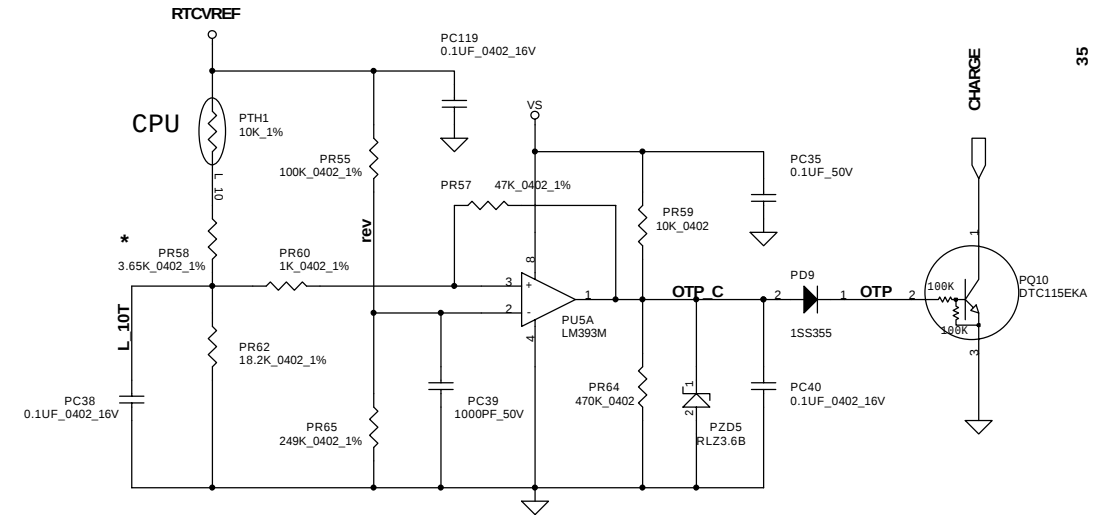
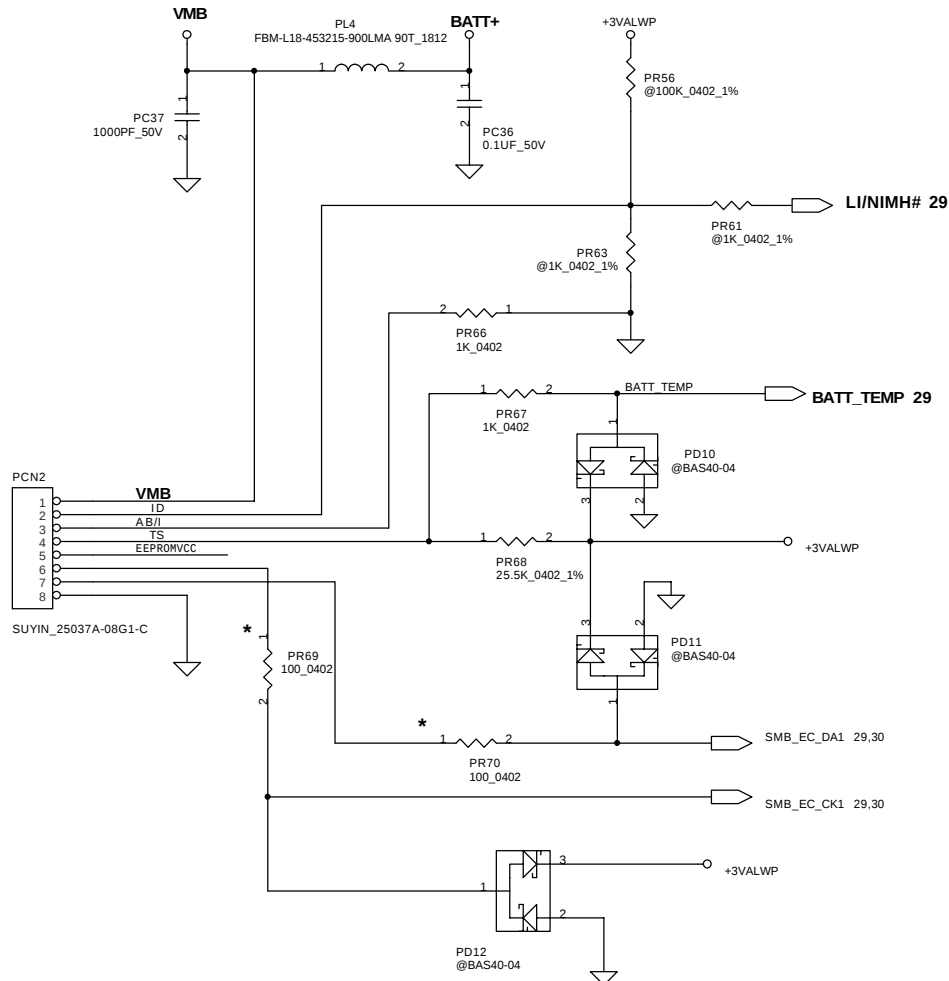
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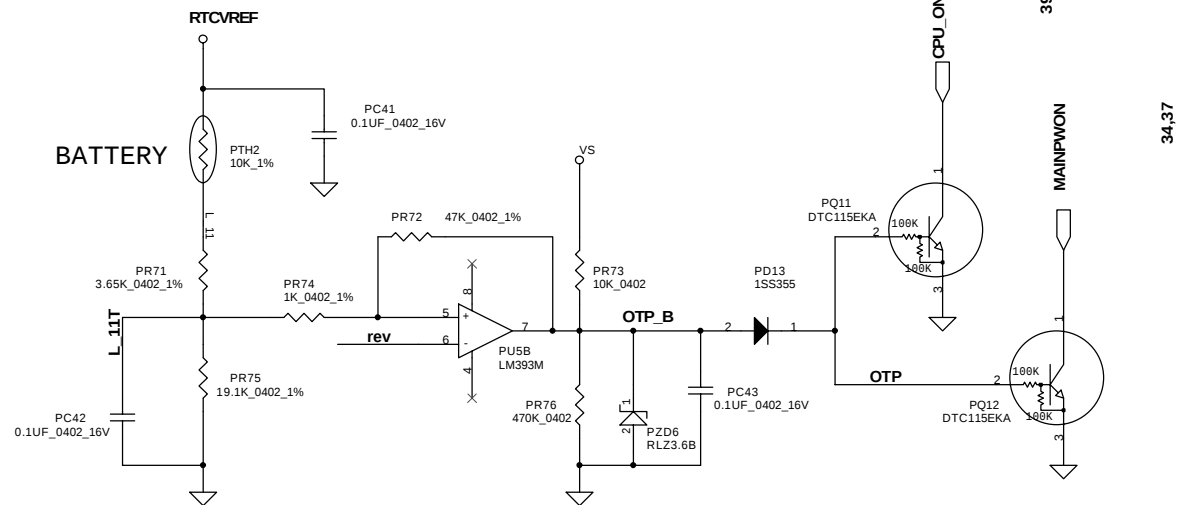
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PH1 under CPU botten side :
 CPU thermal protection at 90(91)+-3 degree C
 Recovery at 50(51)+-3 degree C



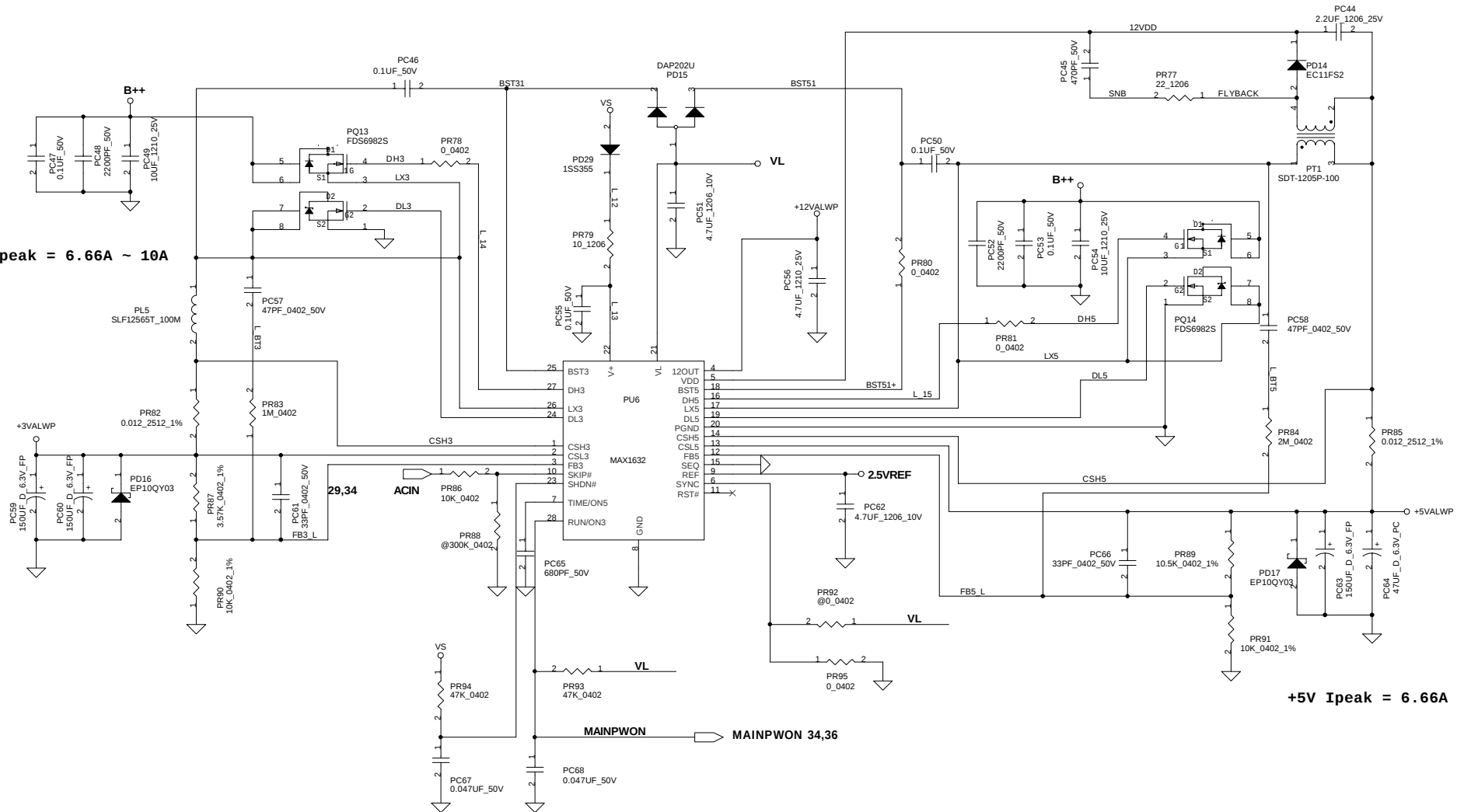
PH2 near main Battery CONN :
 BAT. thermal protection at 85(86)+-3 degree C
 Recovery at 50(51) degree C



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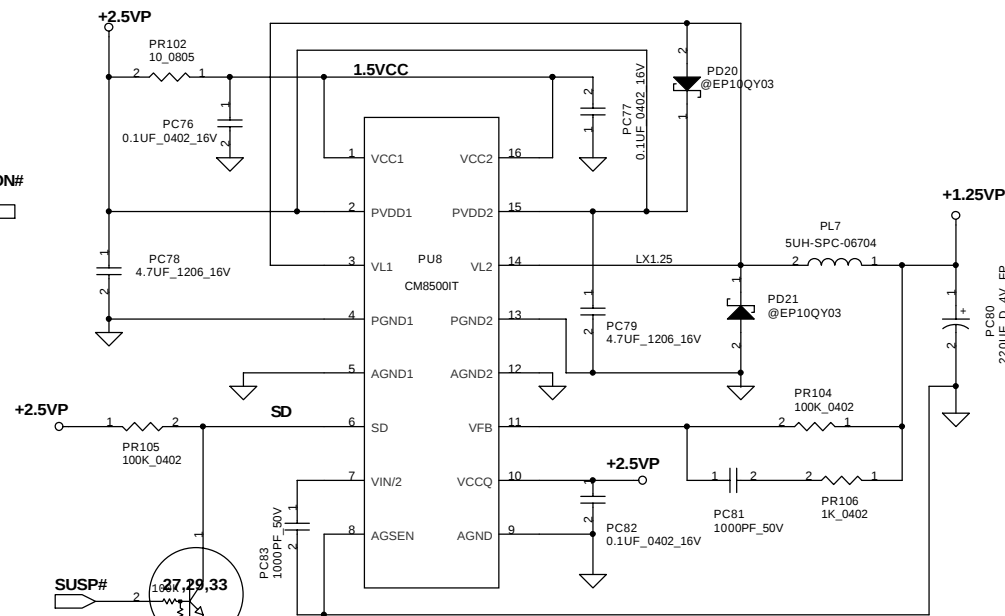
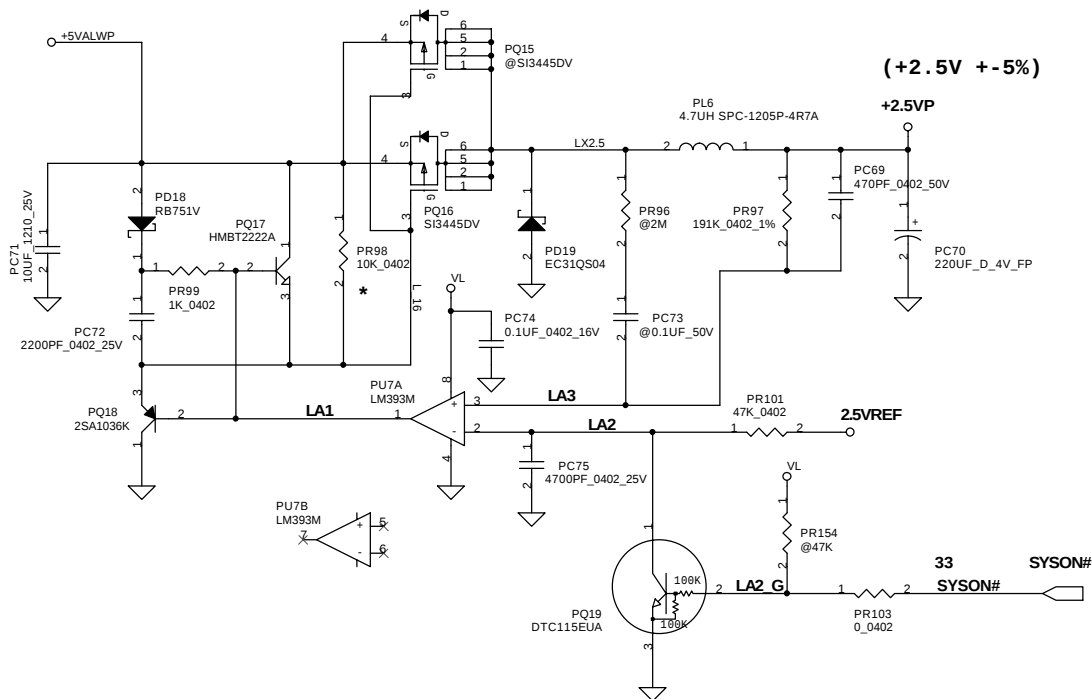
+3.3V Ipeak = 6.66A ~ 10A



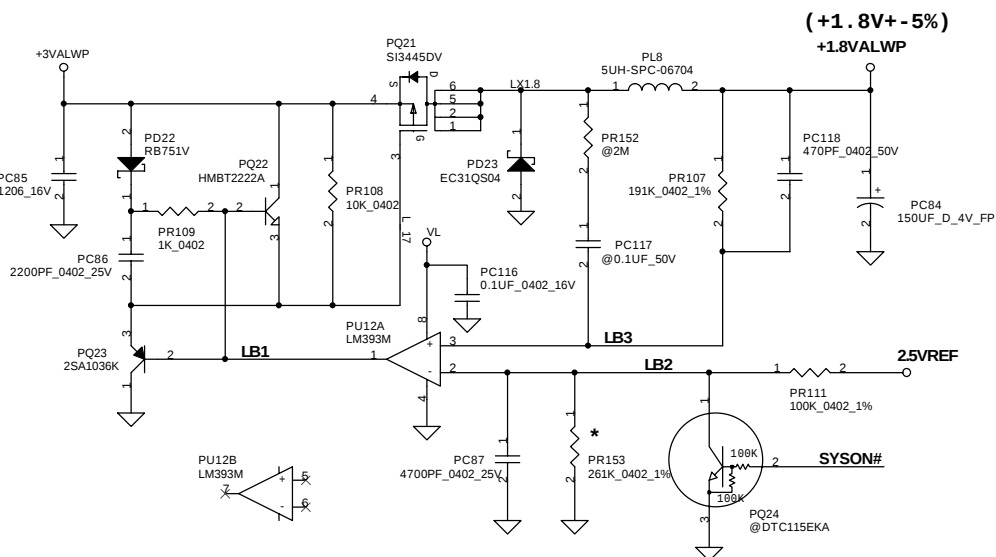
+5V Ipeak = 6.66A ~ 10A

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Layout : "Compensation network close to FB pin"

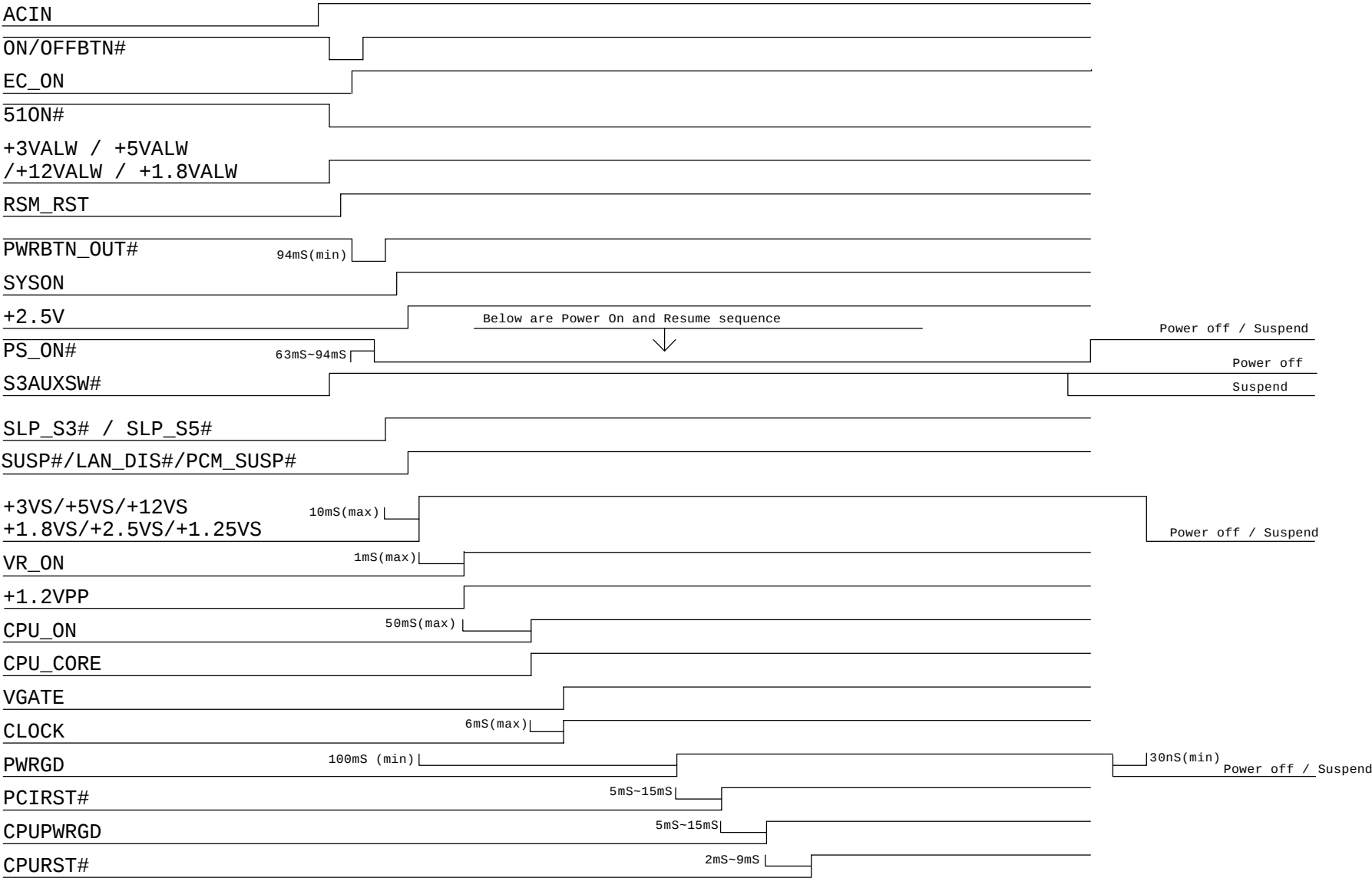


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Power ON sequence

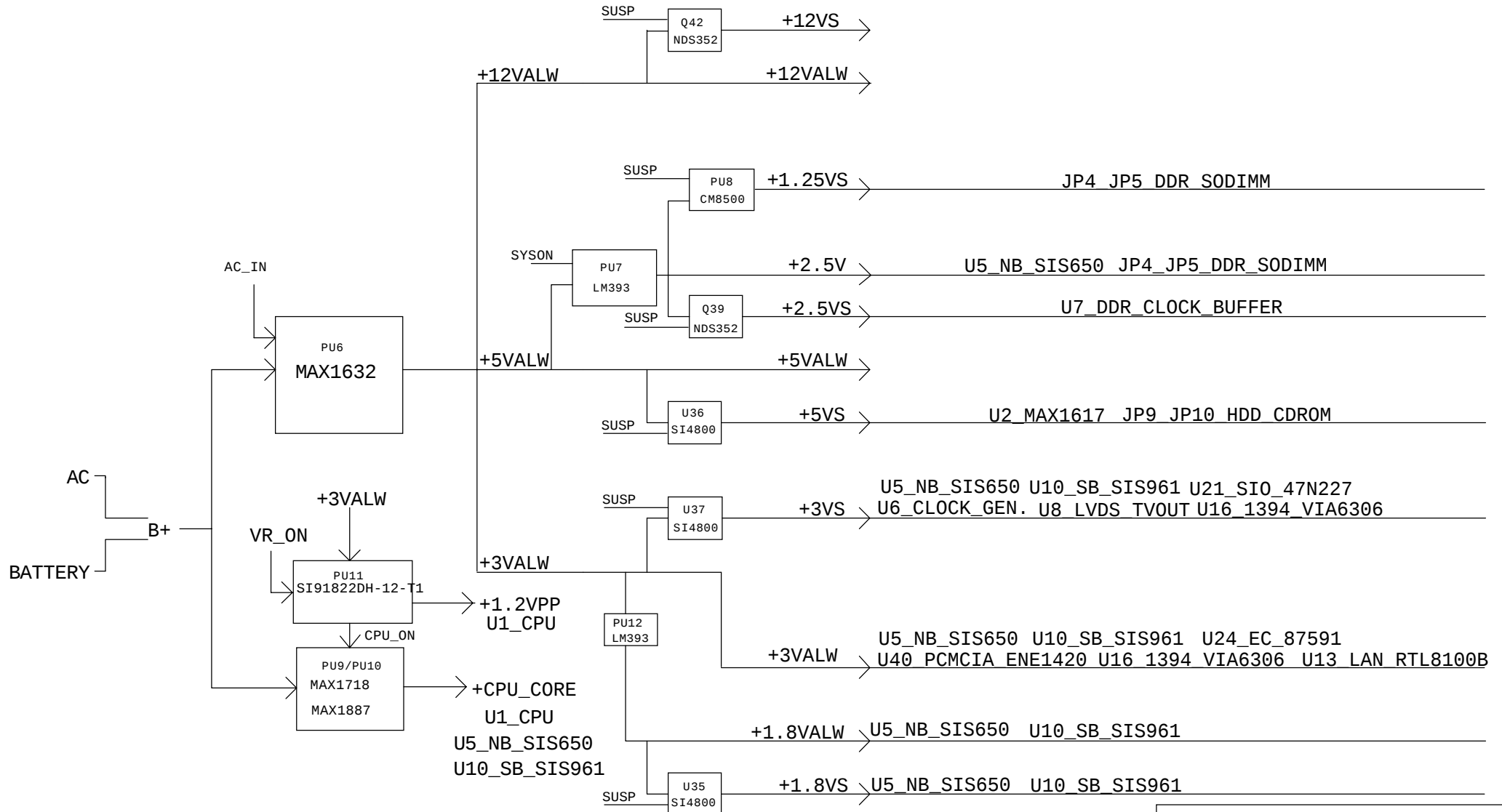
Power Off sequence



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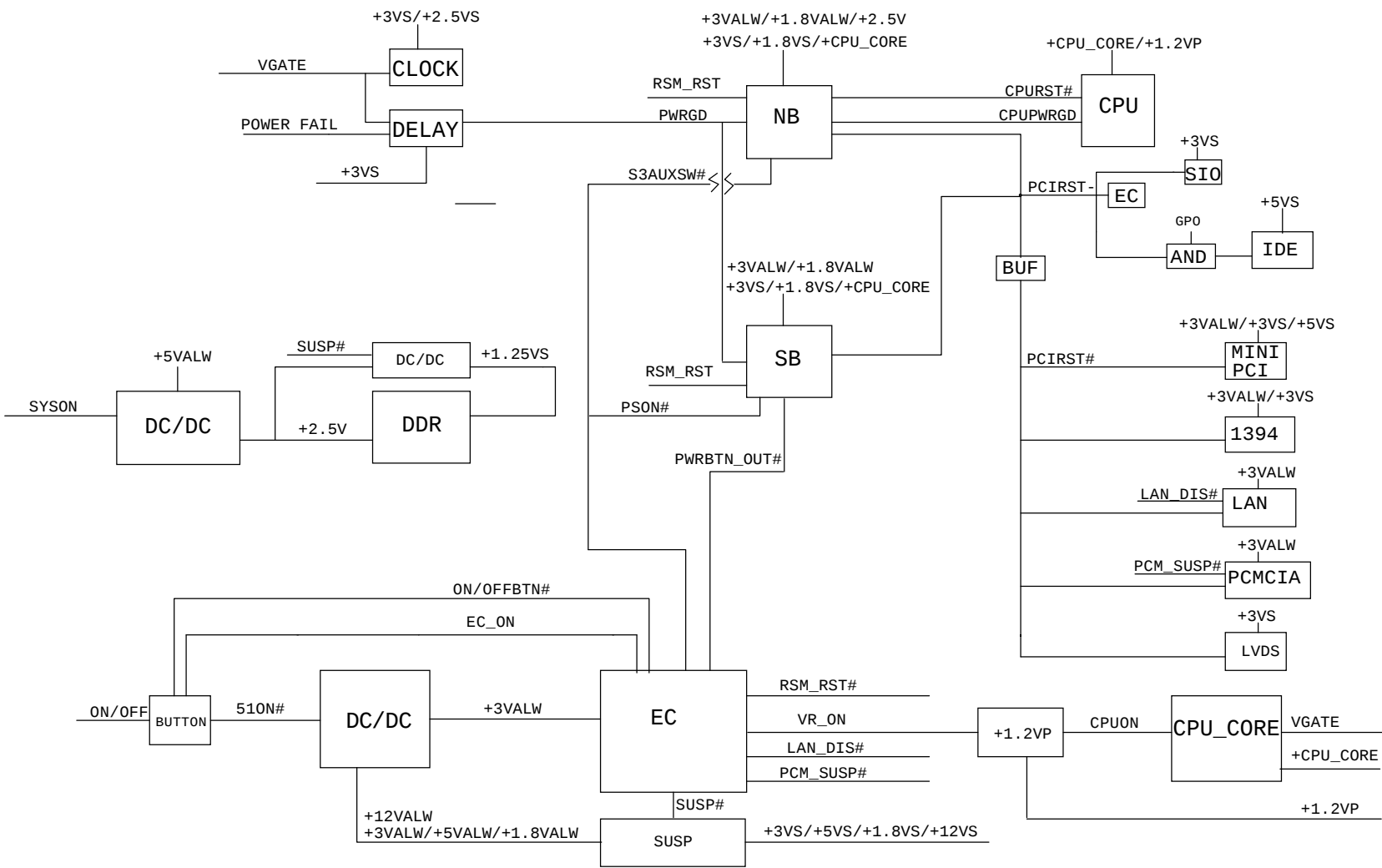
POWER SOURCE BLOCK DIAGRAM



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ACY25 RESET MAP DIAGRAM



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Power PIR							
Item	Fixed Issue	Reason for change	Page	Modify item	MB_Ver.	Phase	
1	NO	Improve CPU_CORE voltage regulator.	39		0.3	C test	
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
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UNIT	IDSEL	IRQ	GNT	REQ
1394	U16	AD16	PIRQC#	GNT#0 REQ#0
MINIPCI	JP16	AD31	PIRQB#	GNT#1 REQ#1
LAN	U13	AD17	PIRQB#	GNT#3 REQ#3
CARDBUS	U40	AD20	PIRQA/B#	GNT#2 REQ#2

SMBUS from EC

EC_SMD2,EC_SMC2 : U2 (MAX1617) AD : 1001 110
SMB_EC_CK1,SMB_EC_DA1: U31(EEPROM) , PCN2 (BATT CONN)

SMBUS from SIS961

SMBCLK , SMBDAT: JP5 , JP4 , CLK GEN (U6) , CLK BUF(U7).

ACY25 A-TEST Modify

Change to 310LV : Add R64,R73,R76. Del R77,R78,Q49,Q50,R539

Add DPSLP# : Add Q49 ,R551

DPRSLPVR : Change to pull Low =Del R536 Add R284 ; Add U41 ,R554.

AUXOK : Del CB112

IDERST# : Add D56 , R548

LAN : VDD2.5 add L27,C294,C297,C299

1394 : +3VA change to +3VS power , R351,R352,R353,R3354 change to 54.9_1% , R355
change to 5.1K_1% , C337 change to .33UF , C338 change to 270PF

KB : Add R552 to disconnect ON/OFF

PSON# : Connect to SLP_S5# directly. Del U33

S3AUXSW# : Connect to SLP_S3# directly

PWRGD : Add R550 transfer 5V to 3V

+2.5V : Q39 using SI2306 to transfer +2.5VS

H_DPSLP# : Add Q49 , R551 to connect with PM_STPCPU#

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CDLED# : Add R553 to disconnect with JP10

USER_BTN3# : Add R552 to disconnect with JP18,R555 pull high to +3VALW

DDR termination : RP32~RP57 , R494~R508 chanage to 33 ohm

PWRGD : Del C42 , C256

SUSP# : R487 change to 75 ohm

FOR C TEST

LED1 : Q48 PIN3 CHANGE TO +3VALW

FWSDCLK0 : Add pull high resistor R556

PWRGD : Add pass through resistor R557

CRTVDD : R170,R171 change from 2.2K to 1K

GPI019,20 : Add pull high resistor R566,R567 , del R269

EC_ON : Del Q47. R492 change to 0 ohm

EN_FAN1 : Add U42 , C483 , C484 , R561 ,R562

CLKFS2 :Del R161 , Add R565

AUXOK : Del D18 , R254

For MP

+5VFAN1 : Add D58 for reserve

S1_RST# ,S2_OE# , S2_RST# , S2_OE# :Add R568,R569,R570,R571 for reserve

LAN_DIS# : Del R333 , add D57 for reserve

MINI PCI : Change to REQ#4 & GNT#4

For MP 5/3

R248 change to 47K , R251 change to 15K

For MP 6/6

R278 change from 0 to 47 ohm

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