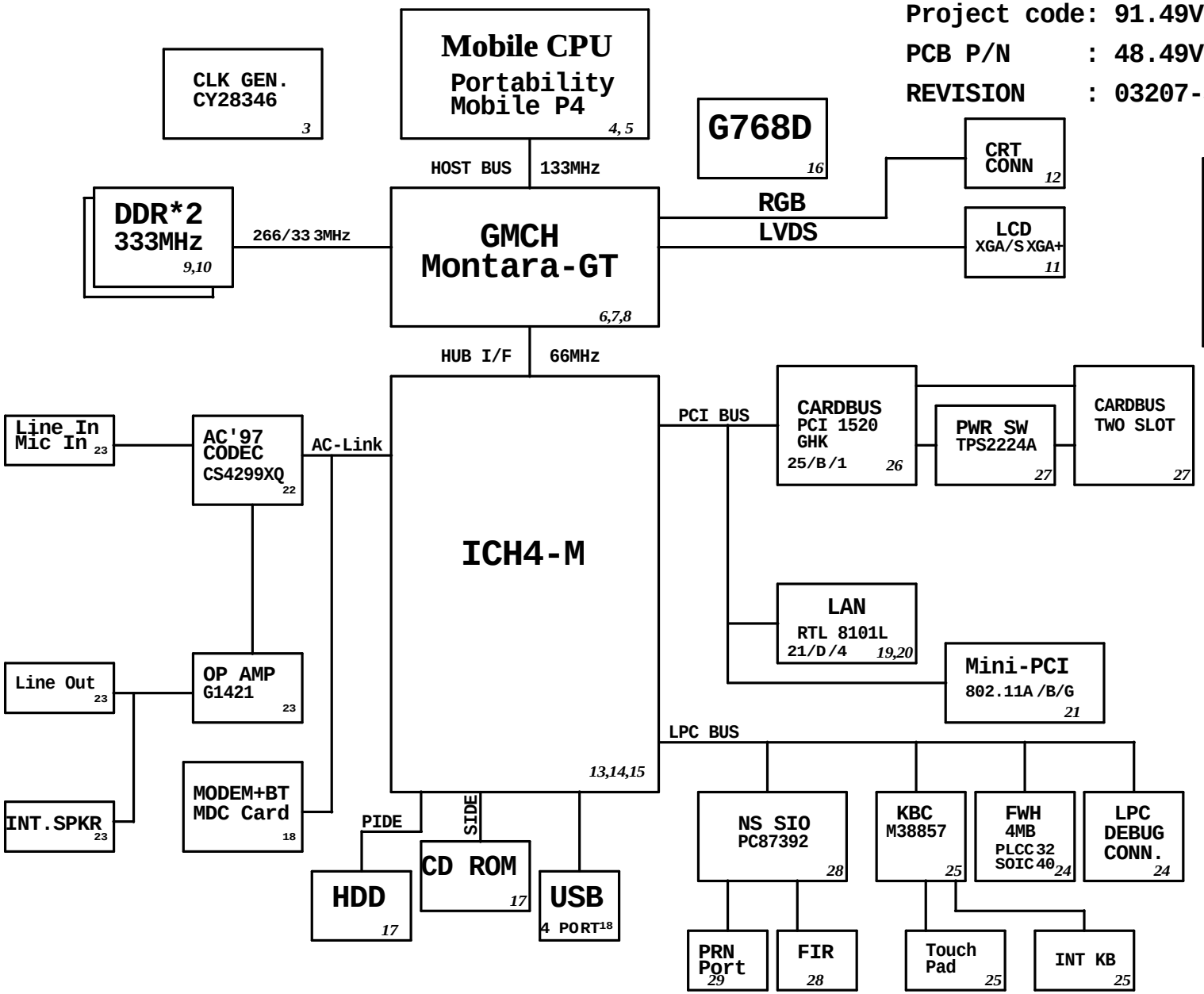
YUHINA Block Diagram

Project code: 91.49V01.001
PCB P/N : 48.49V01.0SC
REVISION : 03207-SC



SYSTEM DC/DC MAX1999 33	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 5V_S3 5V_S0 3D3V_S5 3D3V_S3 3D3V_S0 3D3V_LAN AC

SYSTEM DC/DC MAX1715 30	
INPUTS	OUTPUTS
DCBATOUT	2D5V_S3 1D5V_S0

LP2996 30	
2D5V_S3	1D25V_S0

CPU DC/DC MAX1546ETL 31,32 CM2843ACIM25 31	
INPUTS	OUTPUTS
DCBATOUT	+VCC_CORE 1.3V 44A +VID 1.2V 0.3A

MAXIM CHARGER MAX1645 34	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

PCB LAYER
L1: Signal 1
L2: VCC/GND
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

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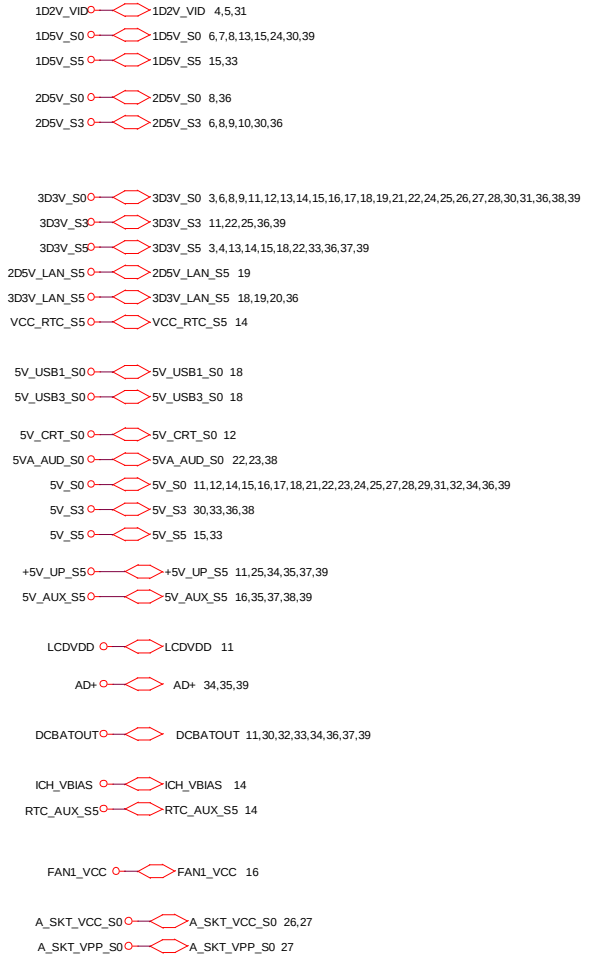
Title: BLOCK DIAGRAM

Size: Custom | Document Number: YUHINA | Rev: SC

Date: Monday, April 28, 2003 | Sheet 1 of 39



PCI DEVICE RESOURCE ASSIGNMENT

	BUS	DEVICE	IDSEL	PCI_REQ#	PCI_GNT#	INT_IRQ#
LAN	1	5	PCI_AD26	REQ#4	GNT#4	IRQD#
CardBus	1	9	PCI_AD20	REQ#1	GNT#1	IRQB#/IRQA#
MiniPCI	1	6	PCI_AD21	REQ#2	GNT#2	IRQE#

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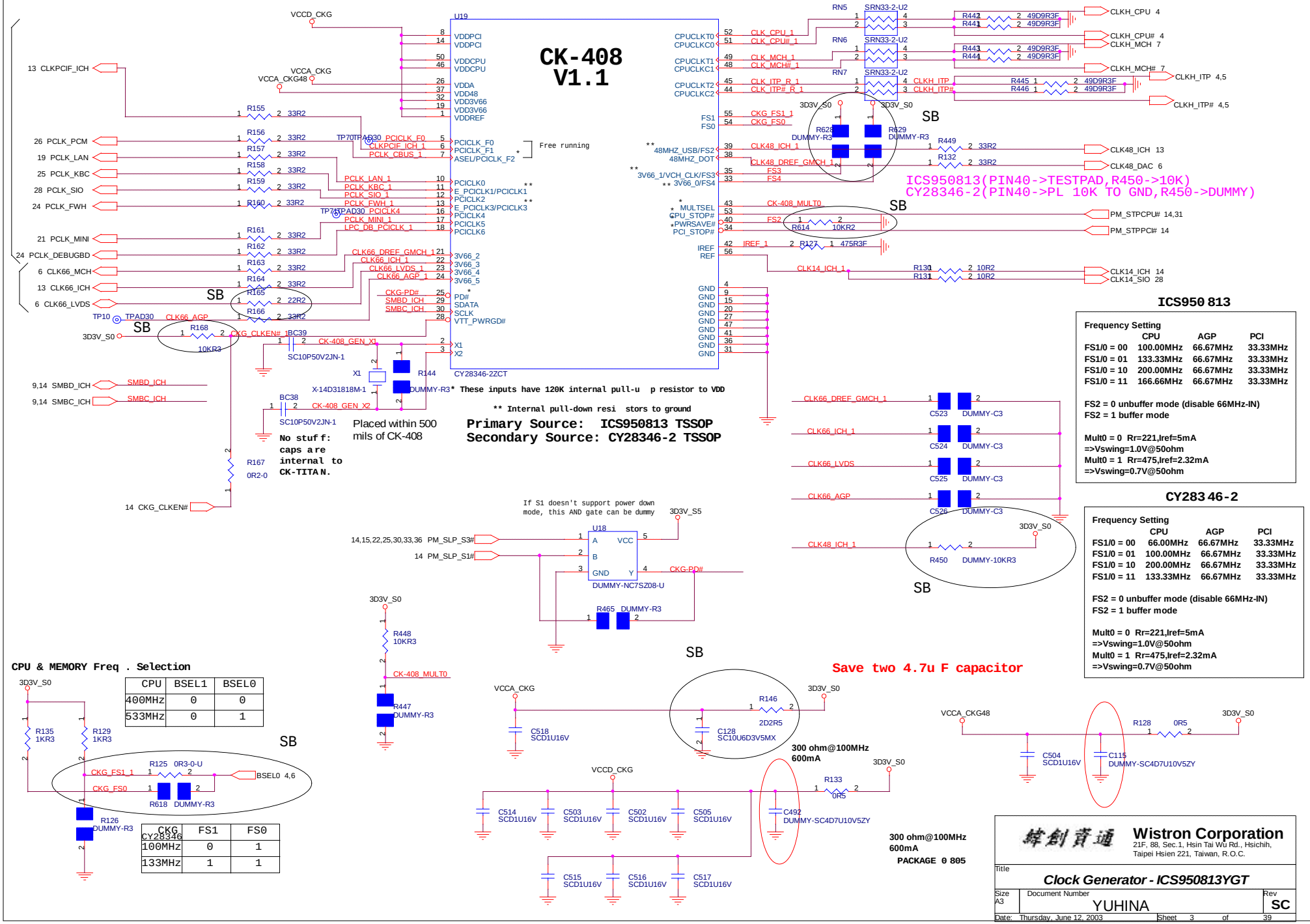
Title: *Table of Content / HISTORY*

Size: A3 | Document Number: YUHINA | Rev: SC

Date: Thursday, May 29, 2003 | Sheet 2 of 39


CK-408
V1.1
CY28346-2ZCT
Free running
SB
ICS950813(PIN40->TESTPAD,R450->10K)
CY28346-2(PIN40->PL 10K TO GND,R450->DUMMY)
ICS950 813
Frequency Setting
CPU AGP PCI
FS1/0 = 00 100.00MHz 66.67MHz 33.33MHz
FS1/0 = 01 133.33MHz 66.67MHz 33.33MHz
FS1/0 = 10 200.00MHz 66.67MHz 33.33MHz
FS1/0 = 11 166.66MHz 66.67MHz 33.33MHz
FS2 = 0 unbuffer mode (disable 66MHz-IN)
FS2 = 1 buffer mode
Mult0 = 0 Rr=221,Iref=5mA
=>Vswing=1.0V@50ohm
Mult0 = 1 Rr=475,Iref=2.32mA
=>Vswing=0.7V@50ohm
CY283 46-2
Frequency Setting
CPU AGP PCI
FS1/0 = 00 66.00MHz 66.67MHz 33.33MHz
FS1/0 = 01 100.00MHz 66.67MHz 33.33MHz
FS1/0 = 10 200.00MHz 66.67MHz 33.33MHz
FS1/0 = 11 133.33MHz 66.67MHz 33.33MHz
FS2 = 0 unbuffer mode (disable 66MHz-IN)
FS2 = 1 buffer mode
Mult0 = 0 Rr=221,Iref=5mA
=>Vswing=1.0V@50ohm
Mult0 = 1 Rr=475,Iref=2.32mA
=>Vswing=0.7V@50ohm
* These inputs have 120K internal pull-u p resistor to VDD
** Internal pull-down resi stors to ground
Primary Source: ICS950813 TSSOP
Secondary Source: CY28346-2 TSSOP
Placed within 500 mils of CK-408
No stuff: caps are internal to CK-TITAN.
If S1 doesn't support power down mode, this AND gate can be dummy
DUMMY-NC7SZ08-U
CPU & MEMORY Freq . Selection
CPU BSEL1 BSEL0
400MHz 0 0
533MHz 0 1
CKG CY28346 FS1 FS0
100MHz 0 1
133MHz 1 1
Save two 4.7u F capacitor
300 ohm@100MHz
600mA
300 ohm@100MHz
600mA
PACKAGE 0 805
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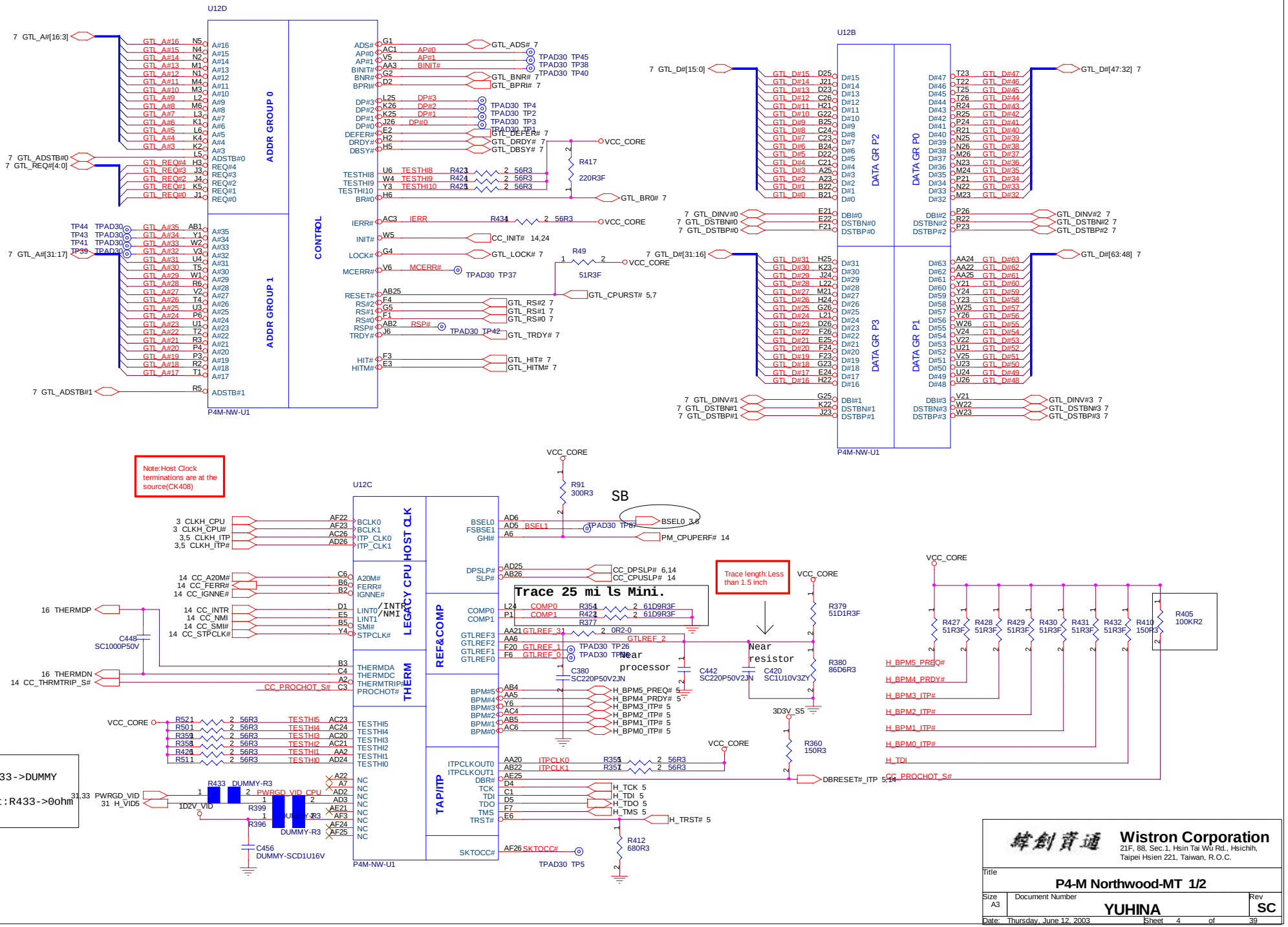
Title
Clock Generator - ICS950813YGT
Size A3
Document Number YUHINA
Rev SC
Date: Thursday, June 12, 2003
Sheet 3 of 39


U12D
ADDR GROUP 0
ADDR GROUP 1
CONTROL
P4M-NW-U1
U12B
DATA GR P0
DATA GR P1
DATA GR P2
DATA GR P3
P4M-NW-U1
U12C
HOST CLK
LEGACY CPU
REF&COMP
THERM
TAP/ITP
P4M-NW-U1
SB
Note:Host Clock terminations are at the source(CK408)
Trace 25 mi ls Mini.
Trace length:Less than 1.5 inch
Near processor
Near resistor
P4:R433->DUMMY
Prescott:R433->0ohm
Wistron Corporation
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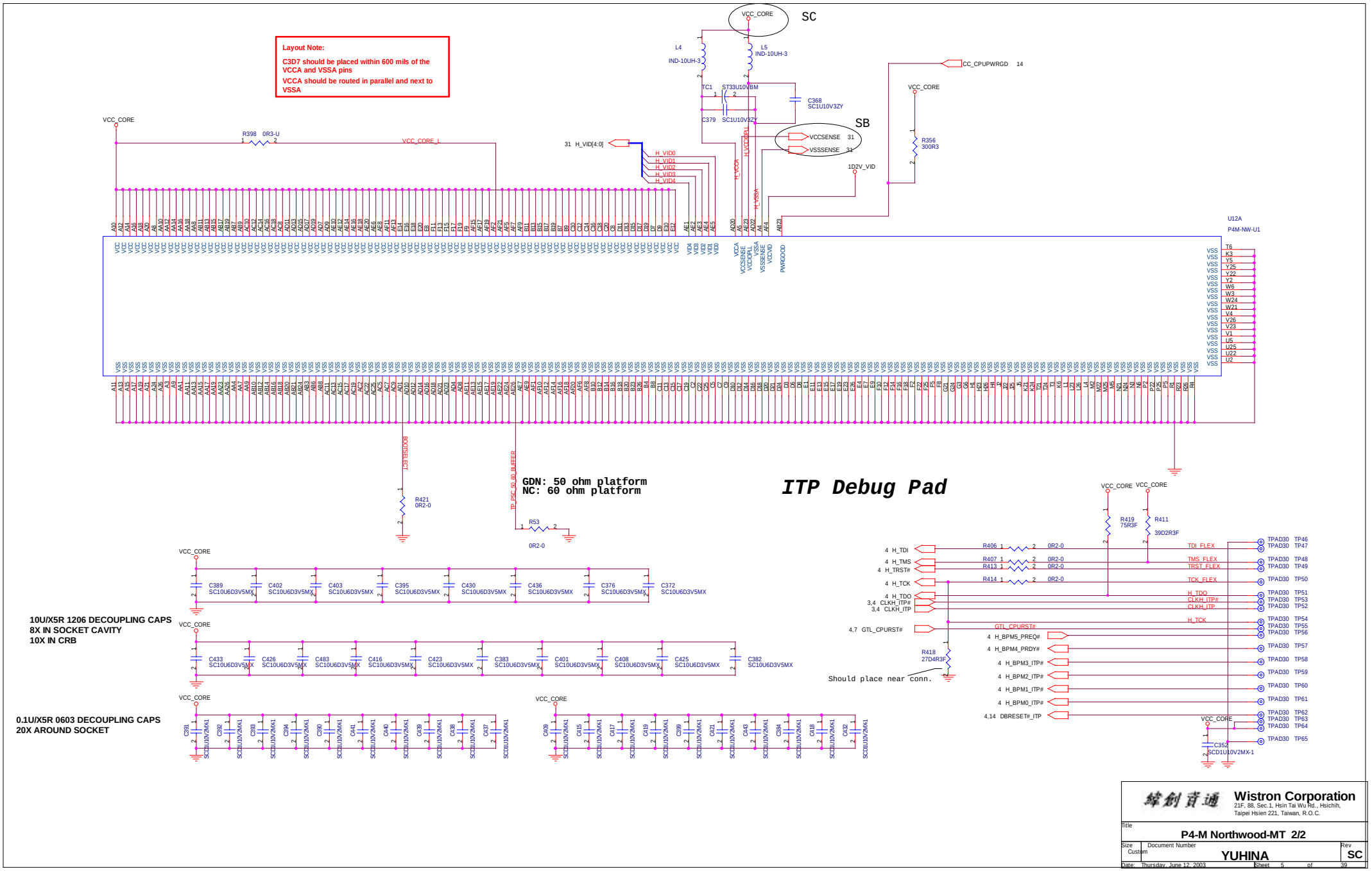
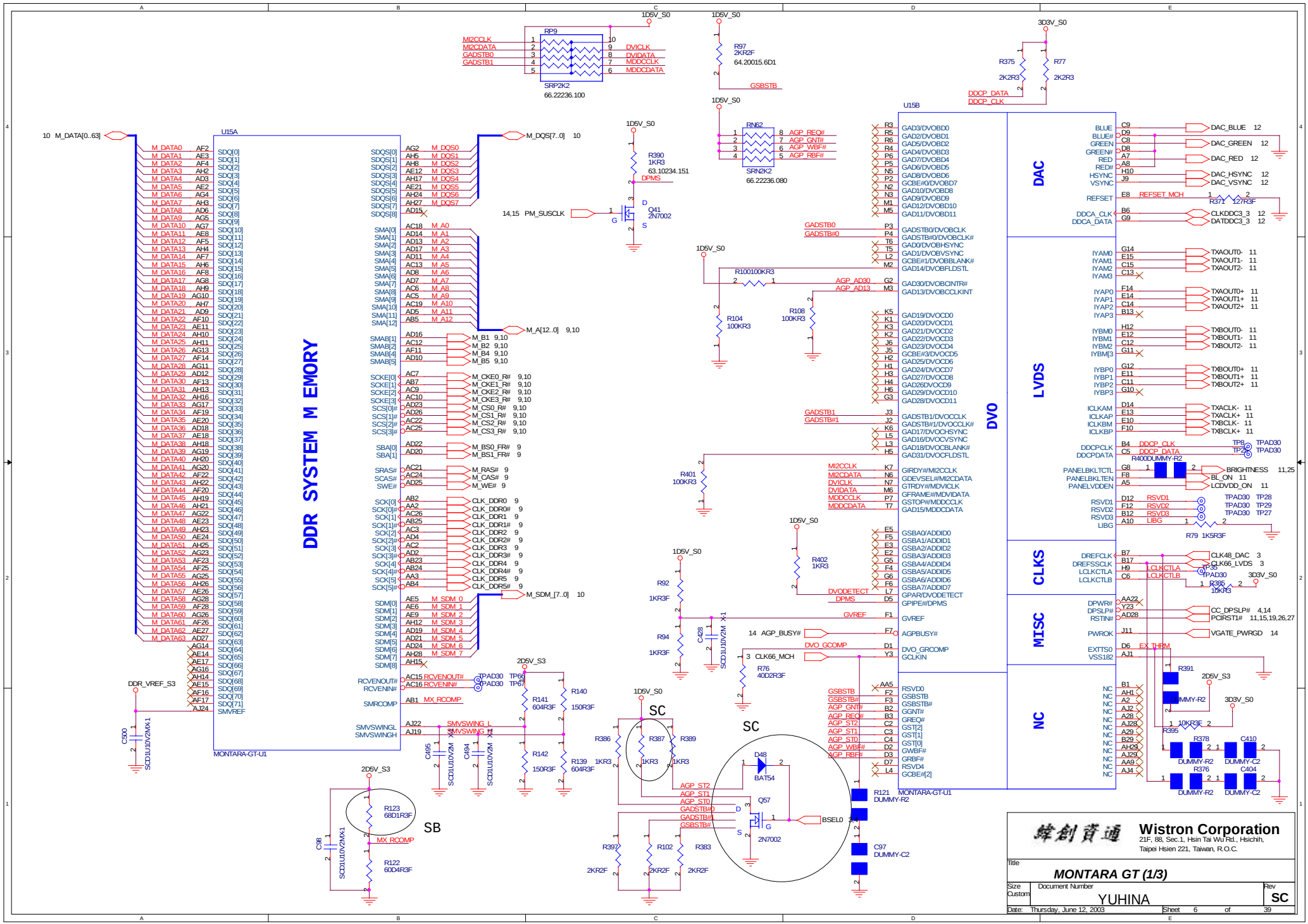
Title
P4-M Northwood-MT 1/2
Size A3
Document Number YUHINA
Rev SC
Date: Thursday, June 12, 2003
Sheet 4 of 39



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	P4-M Northwood-MT 2/2		
Size: Custom	Document Number: YUHINA	Rev: SC	
Date: Thursday, June 12, 2003	Sheet 5 of 39		


DDR SYSTEM MEMORY
U15A
MONTARA-GT-U1
U15B
DVO
DAC
LVDS
CLKS
MISC
NC
SB
SC
SC
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
MONTARA GT (1/3)
YUHINA
Size Custom
Document Number
Rev SC
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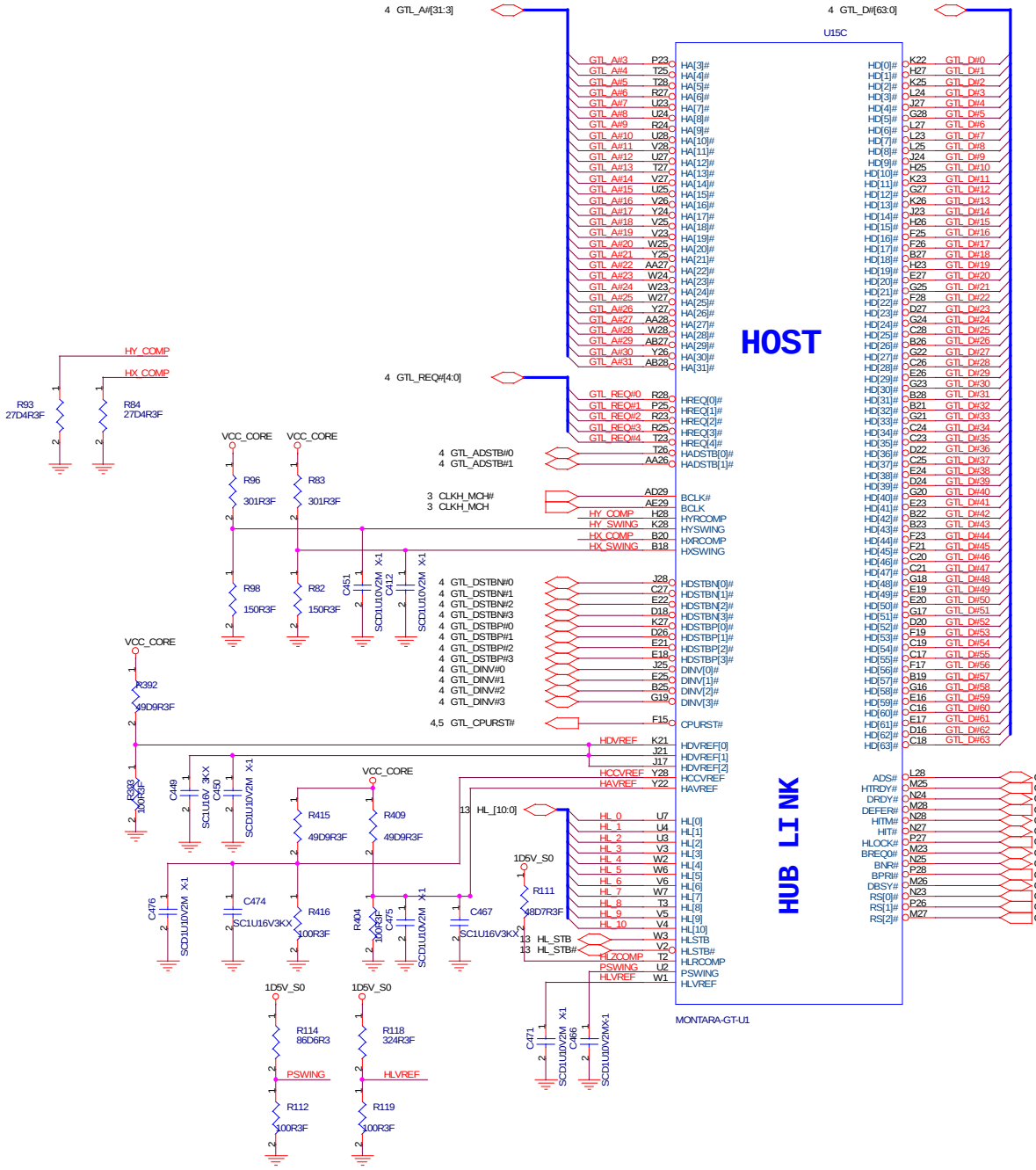

GMCH Strapping Options

	Function	Board Default	Optional Override
LCLKCTB	PSB Voltage Select	Shunt for 1.2V	No shunt for 1.05V
AGPDETCT	DVO/AGP Strap	No shunt for DVO	Shunt for AGP

GMCH Frequency Starpping

ST2	ST1	ST0	PSB Freq	SM Freq	GFX Freq Range
0	0	0	400	267	133-200
0	0	1	400	200	100-200
0	1	0	400	200	100-133
0	1	1	400	267	133-267
1	0	0	533	267	133-200
1*	0*	1*	533	267	133-267
1	1	0	533	333	167-267
1	1	1	400	333	167-250

0 = No Shunt
1 = Shunt
* Default

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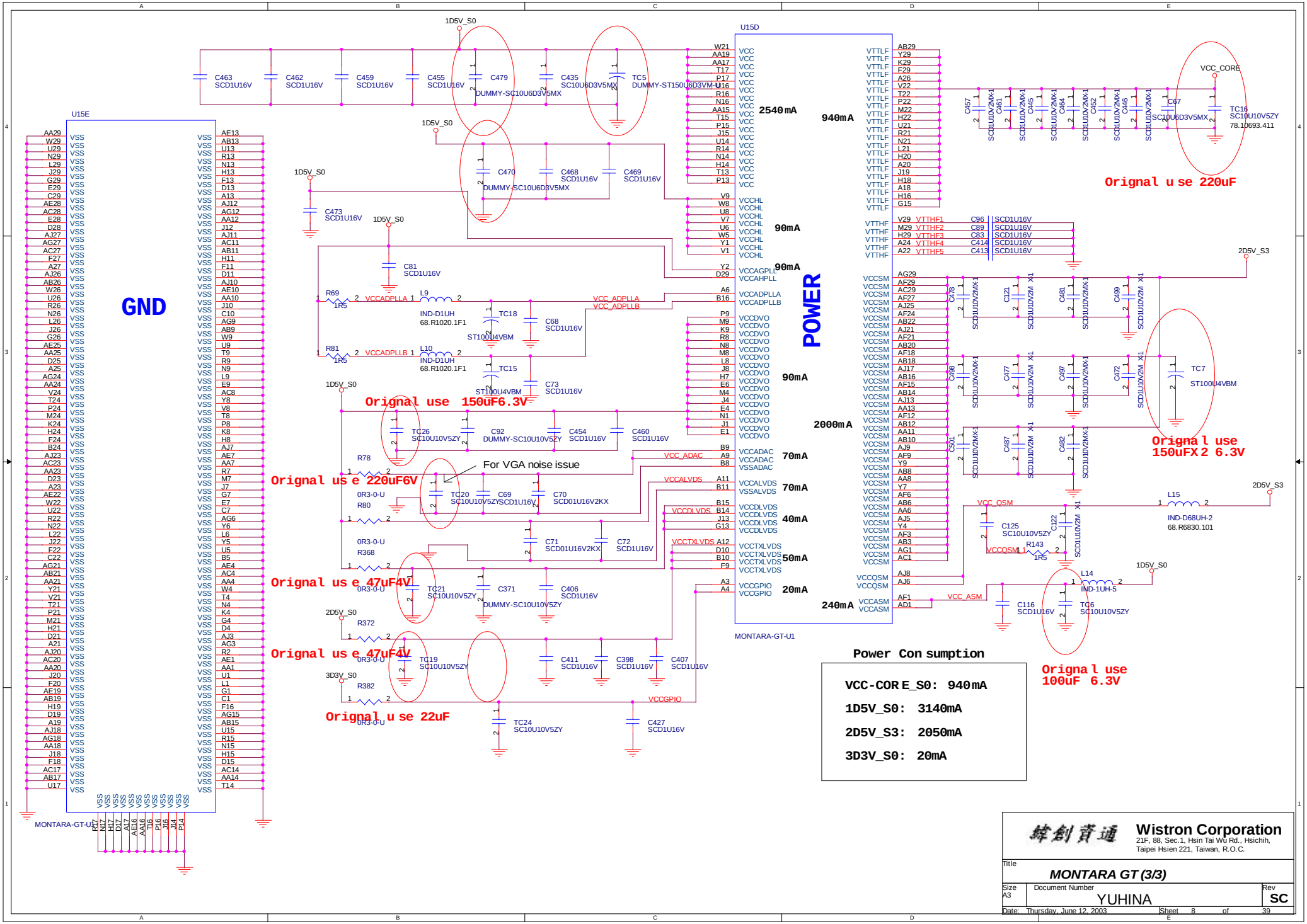
Title: MONTARA GT (2/3)

Size: Custom | Document Number: YUHINA | Rev: SC

Date: Thursday, June 12, 2003 | Sheet 7 of 39


GND
POWER
U15E
U15D
MONTARA-GT-U1
1D5V_S0
2D5V_S0
3D3V_S0
2D5V_S3
VCC_CORE
2540mA
940mA
90mA
90mA
90mA
2000mA
70mA
70mA
40mA
50mA
20mA
240mA
Orignal use 150uF6.3V
Orignal use 220uF6V
Orignal use 47uF4V
Orignal use 47uF4V
Orignal use 22uF
Orignal use 220uF
Orignal use 150uFX2 6.3V
Orignal use 100uF 6.3V
For VGA noise issue
Power Consumption
VCC-CORE_S0: 940mA
1D5V_S0: 3140mA
2D5V_S3: 2050mA
3D3V_S0: 20mA
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MONTARA GT (3/3)
YUHINA
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Thursday, June 12, 2003
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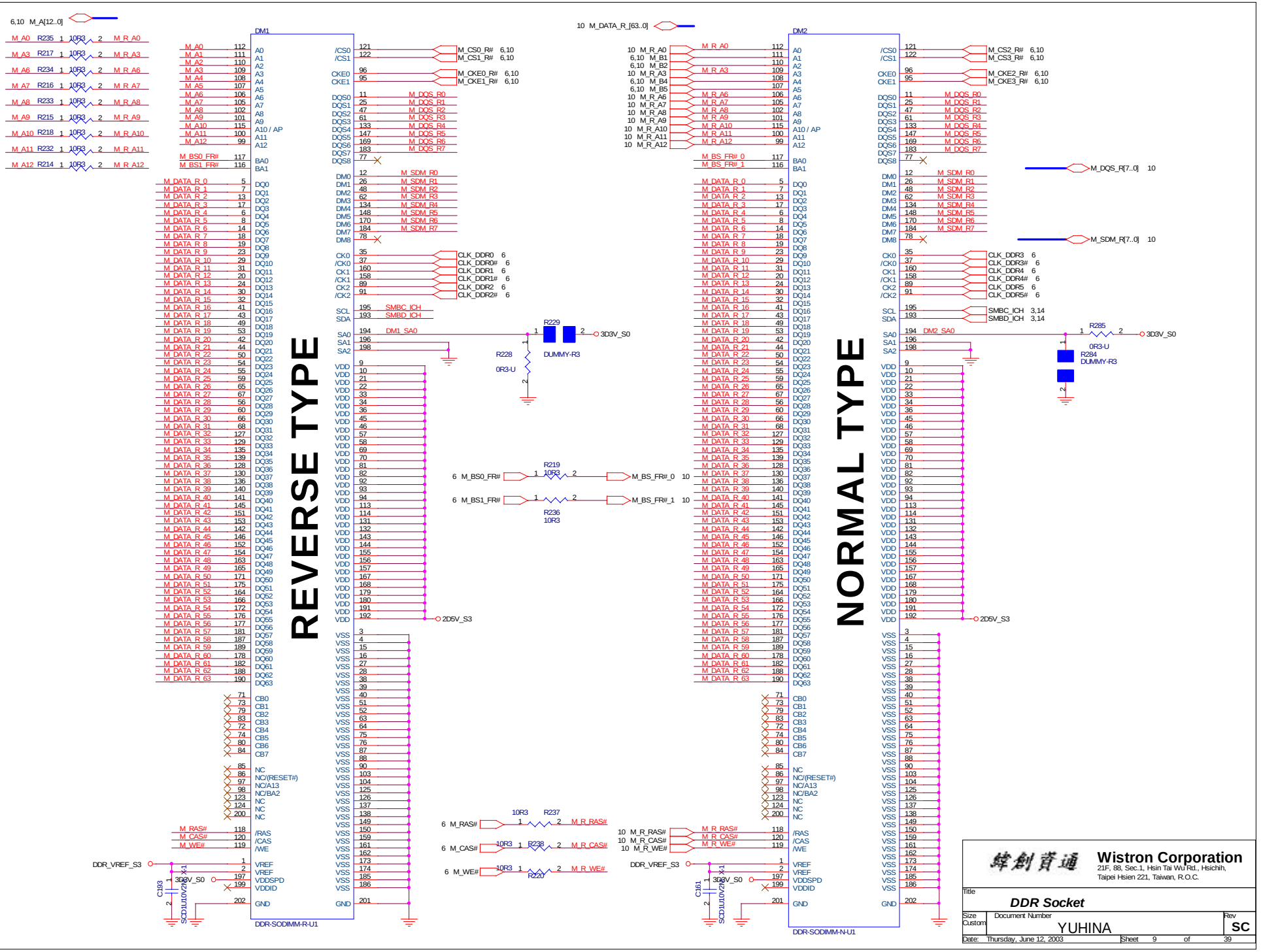
REVERSE TYPE
NORMAL TYPE
DM1
DM2
DDR-SODIMM-R-U1
DDR-SODIMM-N-U1
6,10 M_A[12..0]
10 M_DATA_R_[63..0]
M_DQS_R[7..0] 10
M_SDM_R[7..0] 10
M_A0 R235 10R3 M_R_A0
M_A3 R217 10R3 M_R_A3
M_A6 R234 10R3 M_R_A6
M_A7 R216 10R3 M_R_A7
M_A8 R233 10R3 M_R_A8
M_A9 R215 10R3 M_R_A9
M_A10 R218 10R3 M_R_A10
M_A11 R232 10R3 M_R_A11
M_A12 R214 10R3 M_R_A12
M_CS0_R# 6,10
M_CS1_R# 6,10
M_CKE0_R# 6,10
M_CKE1_R# 6,10
M_CS2_R# 6,10
M_CS3_R# 6,10
M_CKE2_R# 6,10
M_CKE3_R# 6,10
CLK_DDR0 6
CLK_DDR0# 6
CLK_DDR1 6
CLK_DDR1# 6
CLK_DDR2 6
CLK_DDR2# 6
CLK_DDR3 6
CLK_DDR3# 6
CLK_DDR4 6
CLK_DDR4# 6
CLK_DDR5 6
CLK_DDR5# 6
SMBC_ICH 3,14
SMBD_ICH 3,14
R229 DUMMY-R3
R228 0R3-U
R285 0R3-U
R284 DUMMY-R3
DM1_SA0
DM2_SA0
3D3V_S0
2D5V_S3
R219 10R3
R236 10R3
6 M_BS0_FR#
6 M_BS1_FR#
M_BS_FR#_0 10
M_BS_FR#_1 10
R237 10R3
R238 10R3
R220 10R3
6 M_RAS#
6 M_CAS#
6 M_WE#
M_R_RAS# 10
M_R_CAS# 10
M_R_WE# 10
DDR_VREF_S3
C193 SCD1U10V2KX-1
C161 SCD1U10V2KX-1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR Socket
Size Custom
Document Number YUHINA
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Date: Thursday, June 12, 2003
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SERIES DAMPING

RN28 SRN10: M_DATA60 M_DATA_R_60; M_DATA55 M_DATA_R_55; M_DATA54 M_DATA_R_54; M_SDM_6 M_SDM_R6

RN29 SRN10: M_DATA63 M_DATA_R_63; M_DATA62 M_DATA_R_62; M_SDM_7 M_SDM_R7; M_DATA61 M_DATA_R_61

RN20 SRN10: M_DATA_6 M_DATA_R_6; M_SDM_0 M_SDM_R0; M_DATA4 M_DATA_R_4; M_DATA5 M_DATA_R_5

RN21 SRN10: M_SDM_1 M_SDM_R1; M_DATA13 M_DATA_R_13; M_DATA12 M_DATA_R_12; M_DATA7 M_DATA_R_7

RN13 SRN10: M_DATA24 M_DATA_R_24; M_DATA19 M_DATA_R_19; M_DATA18 M_DATA_R_18; M_DQS2 M_DQS_R2

RN14 SRN10: M_DATA27 M_DATA_R_27; M_DATA26 M_DATA_R_26; M_DQS3 M_DQS_R3; M_DATA25 M_DATA_R_25

RN15 SRN10: M_DATA34 M_DATA_R_34; M_DQS4 M_DQS_R4; M_DATA33 M_DATA_R_33; M_DATA32 M_DATA_R_32

RN16 SRN10: M_DQS5 M_DQS_R5; M_DATA41 M_DATA_R_41; M_DATA40 M_DATA_R_40; M_DATA35 M_DATA_R_35

RN10 SRN10: M_DATA2 M_DATA_R_2; M_DQS0 M_DQS_R0; M_DATA1 M_DATA_R_1; M_DATA0 M_DATA_R_0

RN11 SRN10: M_DQS1 M_DQS_R1; M_DATA9 M_DATA_R_9; M_DATA8 M_DATA_R_8; M_DATA3 M_DATA_R_3

RN25 SRN10: M_DATA38 M_DATA_R_38; M_SDM_4 M_SDM_R4; M_DATA37 M_DATA_R_37; M_DATA36 M_DATA_R_36

RN26 SRN10: M_SDM_5 M_SDM_R5; M_DATA45 M_DATA_R_45; M_DATA44 M_DATA_R_44; M_DATA39 M_DATA_R_39

RN17 SRN10: M_DATA49 M_DATA_R_49; M_DATA48 M_DATA_R_48; M_DATA42 M_DATA_R_42; M_DATA43 M_DATA_R_43

RN22 SRN10: M_DATA20 M_DATA_R_20; M_DATA21 M_DATA_R_21; M_DATA15 M_DATA_R_15; M_DATA14 M_DATA_R_14

RN12 SRN10: M_DATA16 M_DATA_R_16; M_DATA17 M_DATA_R_17; M_DATA10 M_DATA_R_10; M_DATA11 M_DATA_R_11

RN27 SRN10: M_DATA53 M_DATA_R_53; M_DATA52 M_DATA_R_52; M_DATA47 M_DATA_R_47; M_DATA46 M_DATA_R_46

RN18 SRN10: M_DATA56 M_DATA_R_56; M_DATA51 M_DATA_R_51; M_DATA50 M_DATA_R_50; M_DQS6 M_DQS_R6

RN19 SRN10: M_DATA59 M_DATA_R_59; M_DATA58 M_DATA_R_58; M_DQS7 M_DQS_R7; M_DATA57 M_DATA_R_57

RN23 SRN10: M_DATA28 M_DATA_R_28; M_DATA23 M_DATA_R_23; M_DATA22 M_DATA_R_22; M_SDM_2 M_SDM_R2

RN24 SRN10: M_DATA31 M_DATA_R_31; M_DATA30 M_DATA_R_30; M_SDM_3 M_SDM_R3; M_DATA29 M_DATA_R_29

PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER PIN

2D5V_S3

C197 C186 C167 C164 C165 C185 C184 C241 SCD1U16V

C183 C242 C162 C163 C166 C203 C245 C244 SCD1U16V

SB FOR EMI

C246 SC10U6D3V5MX C243 SC10U6D3V5MX C187

C663 C664 C665 C666 SCD1U16V

1D25V_S0

RN45 SRN56: M_SDM_R0 M_DATA_R_6 M_DATA_R_4 M_DATA_R_5 — C199 SCD1U16V; C255 SCD01U16V2KX
RN46 SRN56: M_SDM_R1 M_DATA_R_13 M_DATA_R_12 M_DATA_R_7 — C200 SCD1U16V
RN31 SRN56: M_DATA_R_2 M_DQS_R0 M_DATA_R_1 M_DATA_R_0 — C202 SCD1U16V; C214 SCD01U16V2KX
RN32 SRN56: M_DQS_R1 M_DATA_R_9 M_DATA_R_8 M_DATA_R_3 — C218 SCD1U16V
RN34 SRN56: M_DATA_R_24 M_DATA_R_19 M_DQS_R2 M_DATA_R_18 — C273 SCD1U16V; C217 SCD01U16V2KX
RN35 SRN56: M_DATA_R_27 M_DATA_R_26 M_DQS_R3 M_DATA_R_25 — C269 SCD1U16V
RN47 SRN56: M_DATA_R_20 M_DATA_R_21 M_DATA_R_15 M_DATA_R_14 — C225 SCD1U16V; C215 SCD01U16V2KX
RN33 SRN56: M_DATA_R_16 M_DATA_R_17 M_DATA_R_10 M_DATA_R_11 — C227 SCD1U16V
RN48 SRN56: M_DATA_R_28 M_DATA_R_23 M_DATA_R_22 M_SDM_R2 — C204 SCD1U16V; C259 SCD01U16V2KX
RN49 SRN56: M_DATA_R_31 M_DATA_R_30 M_SDM_R3 M_DATA_R_29 — C229 SCD1U16V
RN55 SRN56: M_DATA_R_53 M_DATA_R_52 M_DATA_R_47 M_DATA_R_46 — C231 SCD1U16V; C228 SCD01U16V2KX
RN42 SRN56: M_DATA_R_49 M_DATA_R_48 M_DATA_R_42 M_DATA_R_43 — C248 SCD1U16V
RN53 SRN56: M_SDM_R4 M_DATA_R_38 M_DATA_R_37 M_DATA_R_36 — C201 SCD1U16V; C268 SCD01U16V2KX
RN54 SRN56: M_DATA_R_45 M_SDM_R5 M_DATA_R_44 M_DATA_R_39 — C267 SCD1U16V
RN40 SRN56: M_DATA_R_34 M_DATA_R_33 M_DQS_R4 M_DATA_R_32 — C254 SCD1U16V; C226 SCD01U16V2KX
RN41 SRN56: M_DQS_R5 M_DATA_R_40 M_DATA_R_41 M_DATA_R_35 — C249 SCD1U16V
RN56 SRN56: M_DATA_R_60 M_DATA_R_55 M_SDM_R6 M_DATA_R_54 — C258 SCD1U16V; C256 SCD01U16V2KX
RN57 SRN56: M_DATA_R_62 M_DATA_R_63 M_SDM_R7 M_DATA_R_61 — C260 SCD1U16V
RN43 SRN56: M_DATA_R_56 M_DATA_R_50 M_DATA_R_51 M_DQS_R6 — C270 SCD1U16V; C230 SCD01U16V2KX
RN44 SRN56: M_DATA_R_58 M_DATA_R_59 M_DQS_R7 M_DATA_R_57 — C271 SCD1U16V

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO DM2
NO EQUAL LENGTH LIMITATION

M_DATA[63..0] 6
M_DATA_R_[63..0] 9
M_DQS[7..0] 6
M_DQS_R[7..0] 9
M_SDM_[7..0] 6
M_SDM_R[7..0] 9

CPC Address

1D25V_S0

RN39 SRN56: 6,9 M_CS0_R# 6,9 M_CS2_R# 9 M_R_WE# 9 M_BS_FR#_0 — C223 SCD01U16V2KX; C224 SCD1U16V

RN51 SRN56: 9 M_BS_FR#_1 9 M_R_A0 6,9 M_B2 6,9 M_A2 — M_R_A0 M_A2 — C264 SCD1U16V; C265 SCD01U16V2KX

66.56036.080

Address / Command

1D25V_S0

RN50 SRN56: 6,9 M_A4 6,9 M_B4 9 M_R_A6 9 M_R_A8 — M_A4 M_R_A6 M_R_A8 — C262 SCD1U16V; C263 SCD01U16V2KX

RN52 SRN56: 6,9 M_CS3_R# 9 M_R_CAS# 6,9 M_CS1_R# 9 M_R_RAS# — C266 SCD1U16V; C257 SCD01U16V2KX

RN36 SRN56: 6,9 M_A5 9 M_R_A3 9 M_R_A12 9 M_R_A11 — M_A5 M_R_A3 M_R_A12 M_R_A11 — C261 SCD1U16V; C220 SCD01U16V2KX

RN38 SRN56: 9 M_R_A10 6,9 M_B1 6,9 M_A1 6,9 M_B5 — M_R_A10 M_A1 — C181 SCD1U16V; C222 SCD01U16V2KX

66.56036.080

Control

SB

1D25V_S0

6,9 M_CKE2_R# 6,9 M_CKE3_R# — R283 56R2J; R255 56R2J — C216 SCD1U16V

6,9 M_CKE1_R# 6,9 M_CKE0_R# — R221 56R2J; R231 56R2J — C219 SCD1U16V

RN37 SRN560J: 9 M_R_A7 9 M_R_A9 — M_R_A7 M_R_A9 — C221 SCD1U16V; C272 SCD01U16V2KX

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR Serial/Terminator Resistor

Size: A3 | Document Number: YUHINA | Rev: SC

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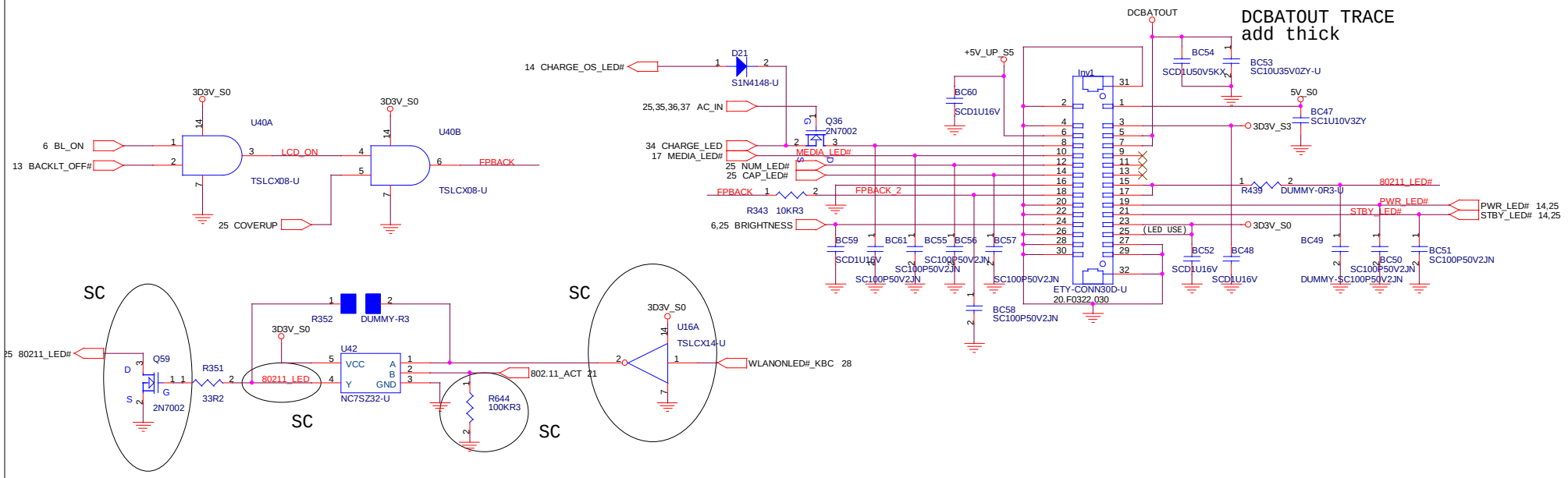
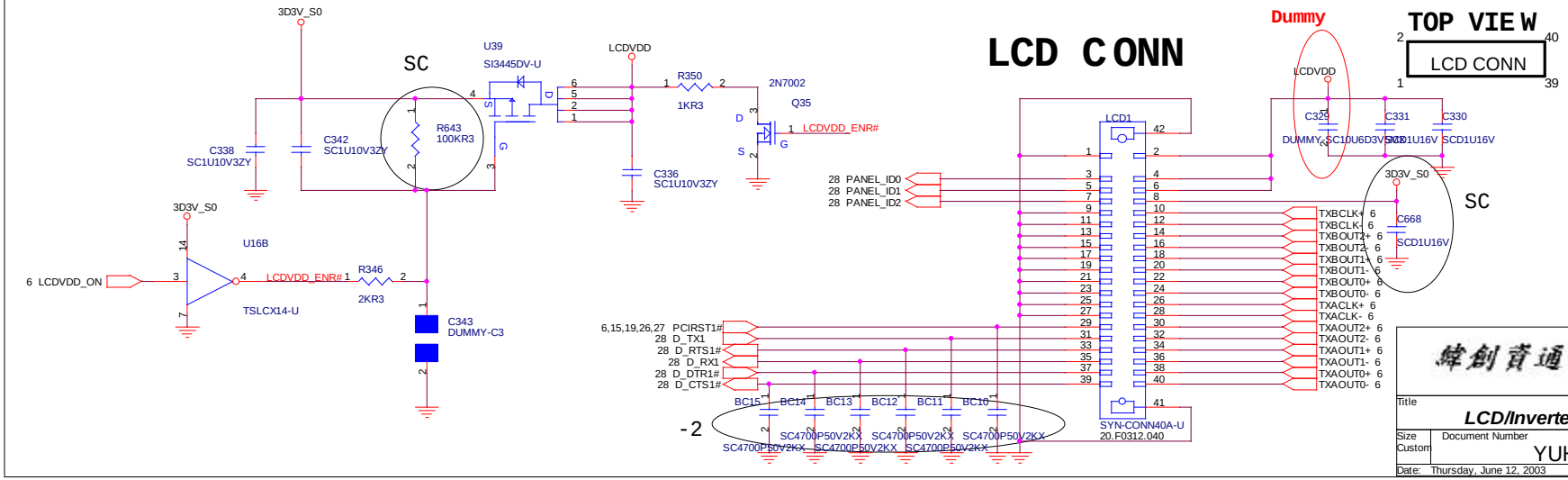
LCD / INVERTER INTERFACE





Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LCD/Inverter Connector*

Size	Document Number	Rev
Custom	YUHINA	SC

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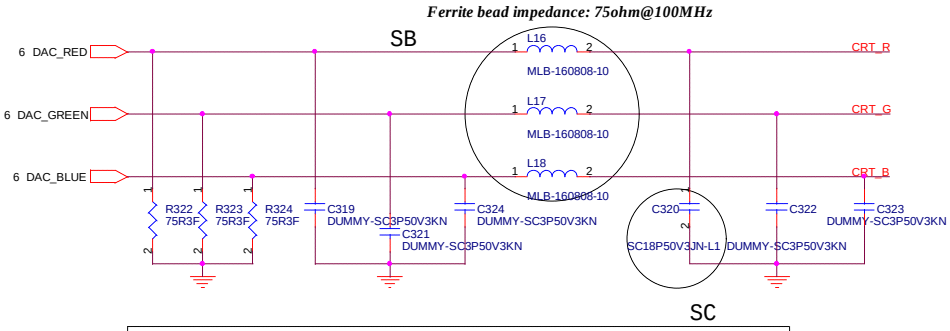
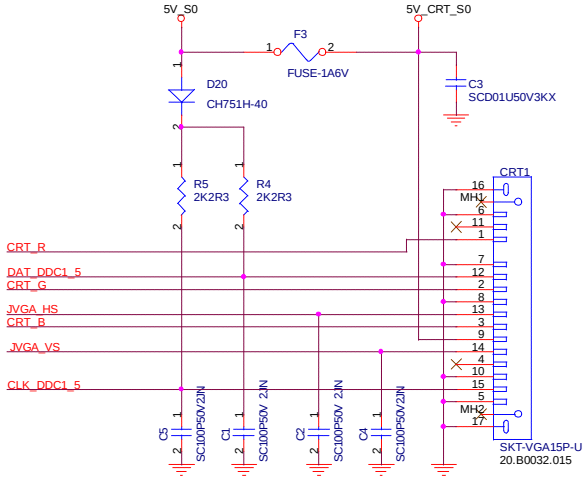
CRT I/F & CONNECTOR



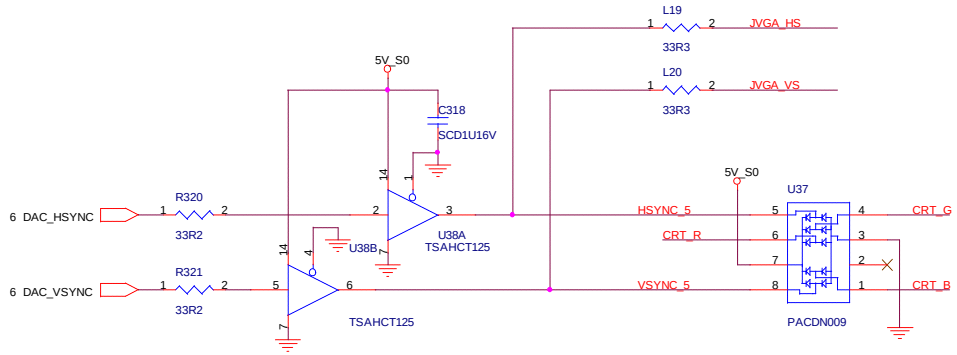
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
**** 37.4_1% resistors must be placed at the same place as the RGB 75 Ohm pull-down resistors.***

Pi-filter & 75 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

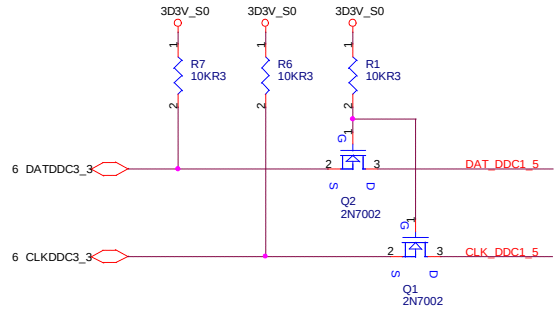
RDDP 1.0



Hsync & Vsync level shift



DDC_CLK & DATA level shift



5V @ ext. CRT side

緯創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***CRT Connector***		
Size: A3	Document Number: YUHINA	Rev: **SC**
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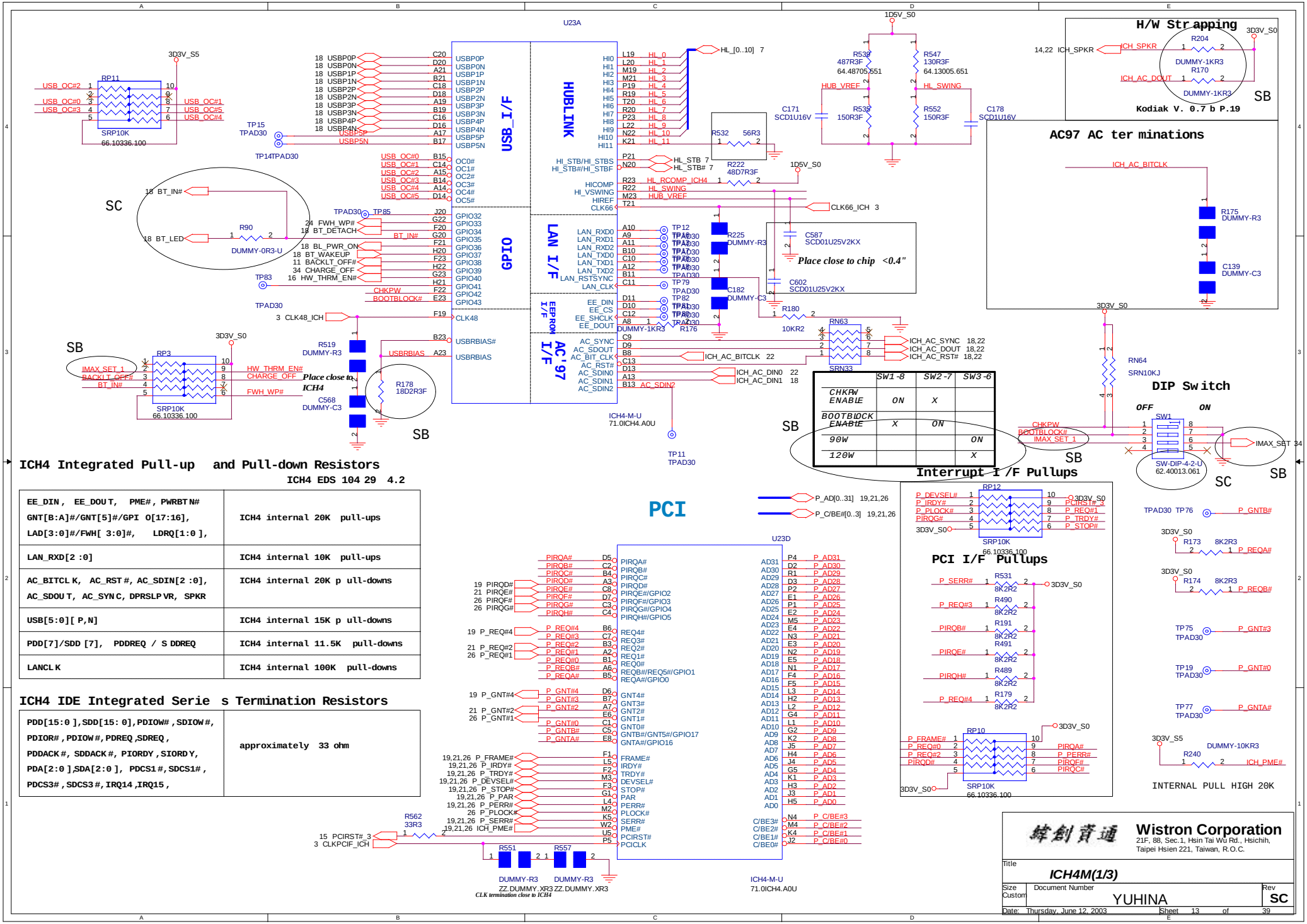
U23A
USB_I/F
HUBLINK
GPIO
LAN I/F
EEPROM I/F
AC '97 I/F
USBP0P
USBP0N
USBP1P
USBP1N
USBP2P
USBP2N
USBP3P
USBP3N
USBP4P
USBP4N
USBP5P
USBP5N
OC0#
OC1#
OC2#
OC3#
OC4#
OC5#
HI0
HI1
HI2
HI3
HI4
HI5
HI6
HI7
HI8
HI9
HI10
HI11
HI_STB/HI_STBS
HI_STB#/HI_STBF
HICOMP
HI_VSWING
HIREF
CLK66
GPIO32
GPIO33
GPIO34
GPIO35
GPIO36
GPIO37
GPIO38
GPIO39
GPIO40
GPIO41
GPIO42
GPIO43
CLK48
USBRBIAS#
USBRBIAS
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_RSTSYNC
LAN_CLK
EE_DIN
EE_CS
EE_SHCLK
EE_DOUT
AC_SYNC
AC_SDOUT
AC_BIT_CLK
AC_RST#
AC_SDIN0
AC_SDIN1
AC_SDIN2
HL_[0..10] 7
HL_0
HL_1
HL_2
HL_3
HL_4
HL_5
HL_6
HL_7
HL_8
HL_9
HL_10
HL_11
HL_STB 7
HL_STB# 7
HL_RCOMP_ICH4
HL_SWING
HUB_VREF
CLK66_ICH 3
ICH_AC_BITCLK 22
ICH_AC_DIN0 22
ICH_AC_DIN1 18
AC_SDIN2
ICH4-M-U
71.0ICH4.A0U
USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
TP15 TPAD30
TP14TPAD30
SC
18 BT_IN#
18 BT_LED
R90
DUMMY-0R3-U
TPAD30 TP85
24 FWH_WP#
18 BT_DETACH
BT_IN#
18 BL_PWR_ON
18 BT_WAKEUP
11 BACKLT_OFF#
34 CHARGE_OFF
16 HW_THRM_EN#
TP83
CHKPW
BOOTBLOCK#
TPAD30
3 CLK48_ICH
R519
DUMMY-R3
USBRBIAS
R178
18D2R3F
SB
3D3V_S0
RP3
IMAX_SET_1
BACKLT_OFF#
BT_IN#
HW_THRM_EN#
CHARGE_OFF
FWH_WP#
SRP10K
66.10336.100
Place close to ICH4
C568
DUMMY-C3
R532 56R3
R222 48D7R3F
1D5V_S0
R225
DUMMY-R3
C182
DUMMY-C3
C587
SCD01U25V2KX
C602
SCD01U25V2KX
Place close to chip <0.4"
R180
10KR2
RN63
ICH_AC_SYNC 18,22
ICH_AC_DOUT 18,22
ICH_AC_RST# 18,22
SRN33
R176
DUMMY-1KR3
TP11
TPAD30
R539
487R3F
64.48705.551
R547
130R3F
64.13005.651
HUB_VREF
HL_SWING
R538
150R3F
R552
150R3F
C171
SCD1U16V
C178
SCD1U16V
H/W Strapping
14,22 ICH_SPKR
ICH_SPKR
R204
DUMMY-1KR3
R170
ICH_AC_DOUT
DUMMY-1KR3
SB
Kodiak V. 0.7 b P.19
AC97 AC ter minations
ICH_AC_BITCLK
R175
DUMMY-R3
C139
DUMMY-C3
3D3V_S0
RN64
SRN10KJ
DIP Switch
OFF ON
SW1
CHKPW
BOOTBLOCK#
IMAX_SET_1
IMAX_SET 34
SW-DIP-4-2-U
62.40013.061
SC
SB
SW1-8 SW2-7 SW3-6
CHKPW ENABLE ON X
BOOTBLOCK ENABLE X ON
90W ON
120W X
Interrupt I/F Pullups
RP12
P_DEVSEL#
P_IRDY#
P_PLOCK#
PIRQG#
PCIRST#_3
P_REQ#1
P_TRDY#
P_STOP#
SRP10K
66.10336.100
PCI
U23D
P_AD[0..31] 19,21,26
P_C/BE#[0..3] 19,21,26
PIRQA#
PIRQB#
PIRQC#
PIRQD#
PIRQE#/GPIO2
PIRQF#/GPIO3
PIRQG#/GPIO4
PIRQH#/GPIO5
REQ4#
REQ3#
REQ2#
REQ1#
REQ0#
REQB#/REQ5#/GPIO1
REQA#/GPIO0
GNT4#
GNT3#
GNT2#
GNT1#
GNT0#
GNTB#/GNT5#/GPIO17
GNTA#/GPIO16
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PAR
PERR#
PLOCK#
SERR#
PME#
PCIRST#
PCICLK
AD31 P_AD31
AD30 P_AD30
AD29 P_AD29
AD28 P_AD28
AD27 P_AD27
AD26 P_AD26
AD25 P_AD25
AD24 P_AD24
AD23 P_AD23
AD22 P_AD22
AD21 P_AD21
AD20 P_AD20
AD19 P_AD19
AD18 P_AD18
AD17 P_AD17
AD16 P_AD16
AD15 P_AD15
AD14 P_AD14
AD13 P_AD13
AD12 P_AD12
AD11 P_AD11
AD10 P_AD10
AD9 P_AD9
AD8 P_AD8
AD7 P_AD7
AD6 P_AD6
AD5 P_AD5
AD4 P_AD4
AD3 P_AD3
AD2 P_AD2
AD1 P_AD1
AD0 P_AD0
C/BE3# P_C/BE#3
C/BE2# P_C/BE#2
C/BE1# P_C/BE#1
C/BE0# P_C/BE#0
PCI I/F Pullups
P_SERR#
P_REQ#3
PIRQB#
PIRQE#
PIRQH#
P_REQ#4
R531
R490
R191
R491
R489
R179
8K2R2
RP10
P_FRAME#
P_REQ#0
P_REQ#2
PIRQD#
PIRQA#
P_PERR#
PIRQF#
PIRQC#
SRP10K
66.10336.100
TPAD30 TP76
P_GNTB#
R173 8K2R3
P_REQA#
R174 8K2R3
P_REQB#
TP75 TPAD30
P_GNT#3
TP19 TPAD30
P_GNT#0
TP77 TPAD30
P_GNTA#
DUMMY-10KR3
R240
ICH_PME#
INTERNAL PULL HIGH 20K
R562
33R3
15 PCIRST#_3
3 CLKPCIF_ICH
R551
R557
DUMMY-R3
ZZ.DUMMY.XR3
CLK termination close to ICH4
ICH4 Integrated Pull-up and Pull-down Resistors
ICH4 EDS 104 29 4.2
EE_DIN, EE_DOUT, PME#, PWRBTN#
GNT[B:A]#/GNT[5]#/GPIO[17:16],
LAD[3:0]#/FWH[3:0]#, LDRQ[1:0],
ICH4 internal 20K pull-ups
LAN_RXD[2:0]
ICH4 internal 10K pull-ups
AC_BITCLK, AC_RST#, AC_SDIN[2:0],
AC_SDOUT, AC_SYNC, DPRSLPVR, SPKR
ICH4 internal 20K pull-downs
USB[5:0]P,N]
ICH4 internal 15K pull-downs
PDD[7]/SDD[7], PDDREQ / SDDREQ
ICH4 internal 11.5K pull-downs
LANCLK
ICH4 internal 100K pull-downs
ICH4 IDE Integrated Series Termination Resistors
PDD[15:0],SDD[15:0],PDIOW#,SDIOW#,
PDIOR#,PDIOW#,PDREQ,SDREQ,
PDDACK#, SDDACK#, PIORDY, SIORDY,
PDA[2:0],SDA[2:0], PDCS1#,SDCS1#,
PDCS3#,SDCS3#,IRQ14,IRQ15,
approximately 33 ohm
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH4M(1/3)
Size Custom
Document Number
YUHINA
Rev
SC
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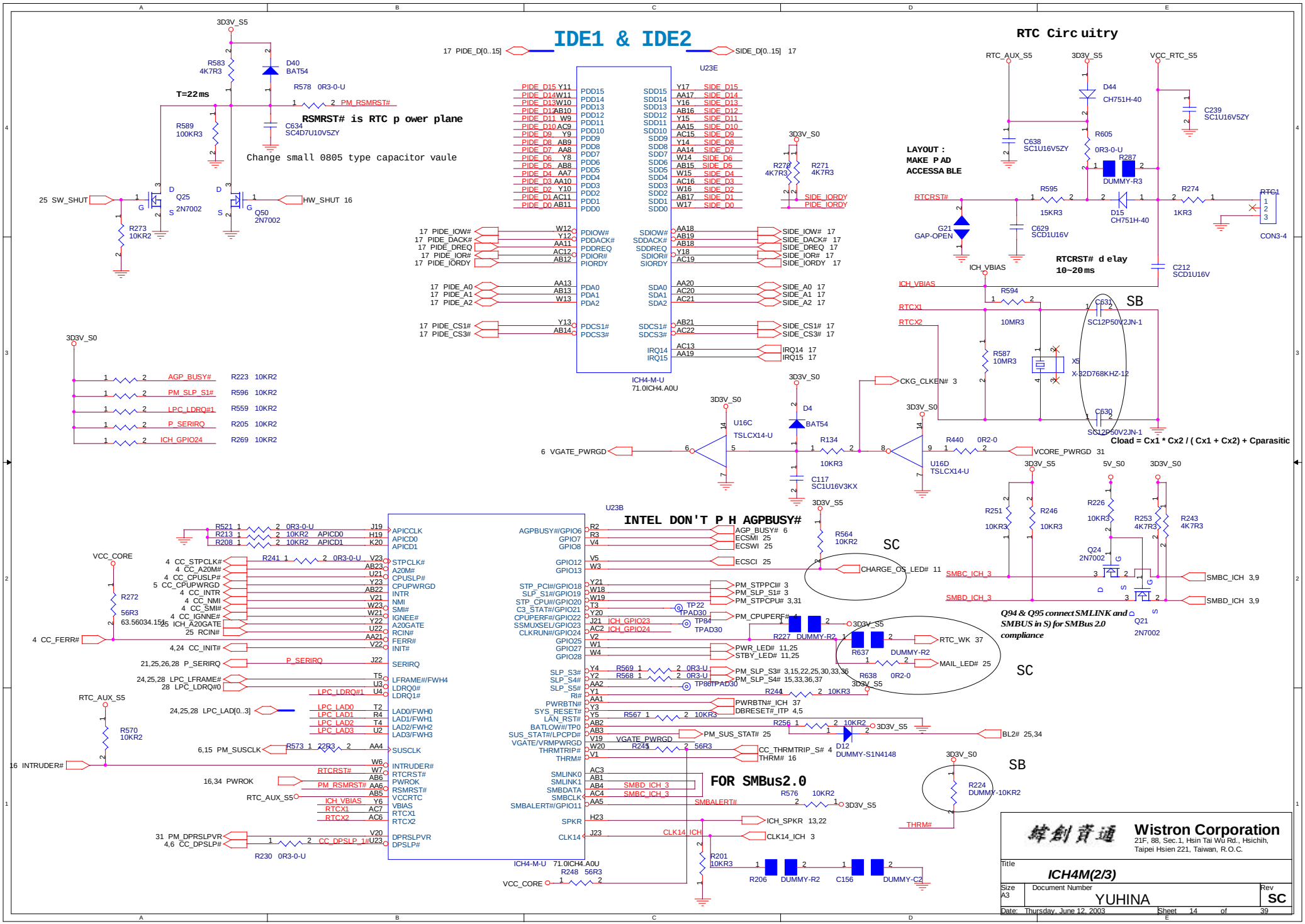
IDE1 & IDE2
RTC Circuitry
INTEL DON'T PASS AGPBUSY#
FOR SMBus2.0
T=22ms
RSMRST# is RTC power plane
Change small 0805 type capacitor vaule
LAYOUT : MAKE PAD ACCESSABLE
RTCRST# delay 10~20ms
Cload = Cx1 * Cx2 / (Cx1 + Cx2) + Cparasitic
Q94 & Q95 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance
ICH4-M-U 71.0ICH4.A0U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH4M(2/3)
Size A3
Document Number YUHINA
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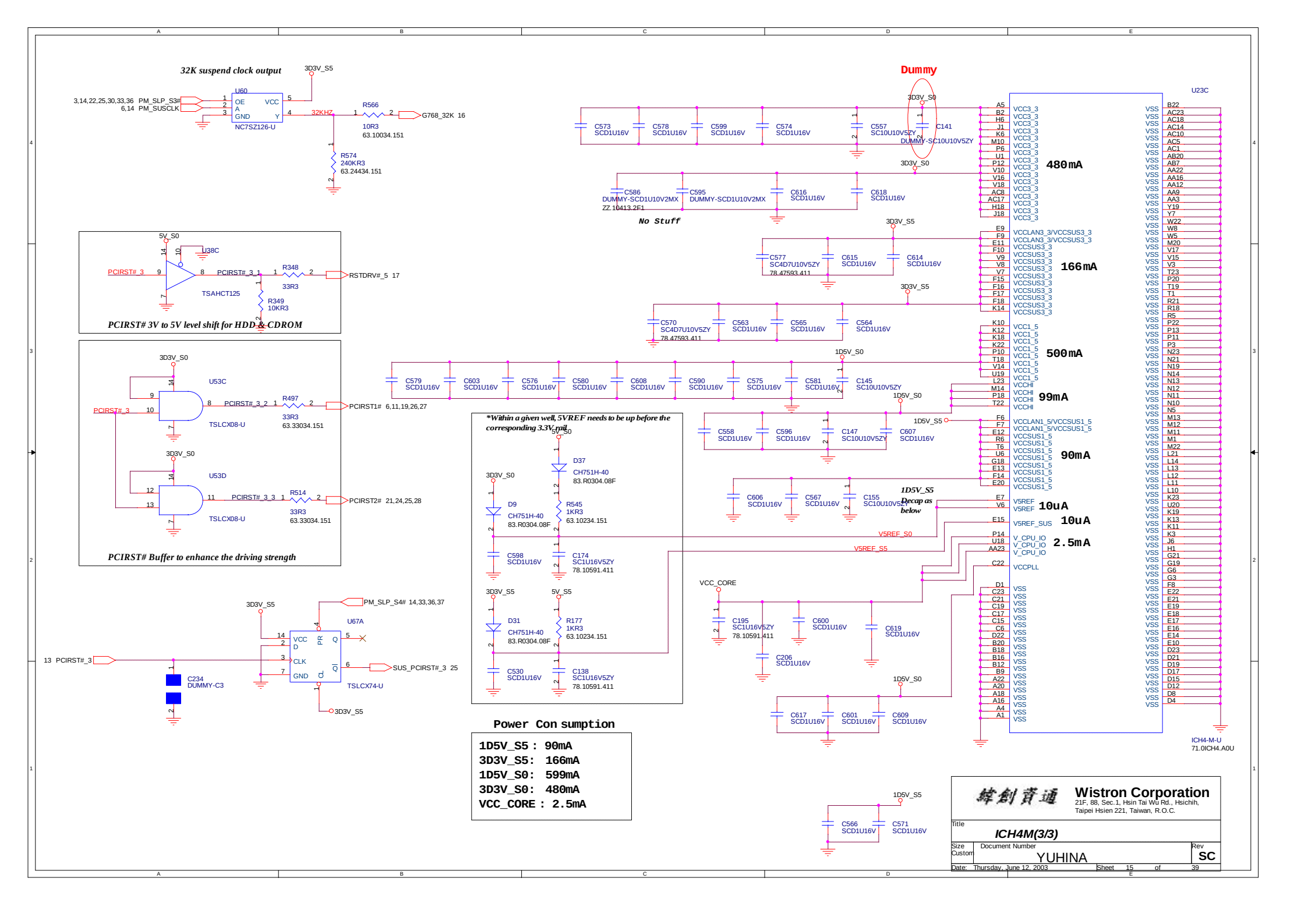
32K suspend clock output
3D3V_S5
U60
NC7SZ126-U
3,14,22,25,30,33,36 PM_SLP_S3#
6,14 PM_SUSCLK
32KHZ
R566
10R3
63.10034.151
G768_32K 16
R574
240KR3
63.24434.151
PCIRST# 3V to 5V level shift for HDD & CDROM
5V_S0
U38C
TSAHCT125
PCIRST# 3
PCIRST#_3_1
R348
33R3
R349
10KR3
RSTDRV#_5 17
PCIRST# Buffer to enhance the driving strength
3D3V_S0
U53C
U53D
TSLCX08-U
PCIRST#_3
PCIRST#_3_2
PCIRST#_3_3
R497
R514
PCIRST1# 6,11,19,26,27
PCIRST2# 21,24,25,28
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail.
D37
CH751H-40
83.R0304.08F
D9
R545
1KR3
63.10234.151
C598
SCD1U16V
C174
SC1U16V5ZY
78.10591.411
D31
R177
C530
C138
Dummy
U23C
C573
C578
C599
C574
C557
SC10U10V5ZY
C141
DUMMY-SC10U10V5ZY
C586
DUMMY-SCD1U10V2MX
ZZ.10413.2F1
C595
DUMMY-SCD1U10V2MX
C616
C618
No Stuff
C577
SC4D7U10V5ZY
78.47593.411
C615
C614
C570
C563
C565
C564
C579
C603
C576
C580
C608
C590
C575
C581
C145
SC10U10V5ZY
C558
C596
C147
C607
C606
C567
C155
1D5V_S5
Decap as below
V5REF_S0
V5REF_S5
VCC_CORE
C195
C600
C619
C206
C617
C601
C609
C566
C571
480mA
166mA
500mA
99mA
90mA
10uA
10uA
2.5mA
VCC3_3
VCCLAN3_3/VCCSUS3_3
VCCSUS3_3
VCC1_5
VCCHI
VCCLAN1_5/VCCSUS1_5
VCCSUS1_5
V5REF
V5REF_SUS
V_CPU_IO
VCCPLL
VSS
ICH4-M-U
71.0ICH4.A0U
PM_SLP_S4# 14,33,36,37
U67A
TSLCX74-U
C234
DUMMY-C3
13 PCIRST#_3
SUS_PCIRST#_3 25
Power Con sumption
1D5V_S5 : 90mA
3D3V_S5: 166mA
1D5V_S0: 599mA
3D3V_S0: 480mA
VCC_CORE : 2.5mA
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Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH4M(3/3)
Size Custom
Document Number
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SC
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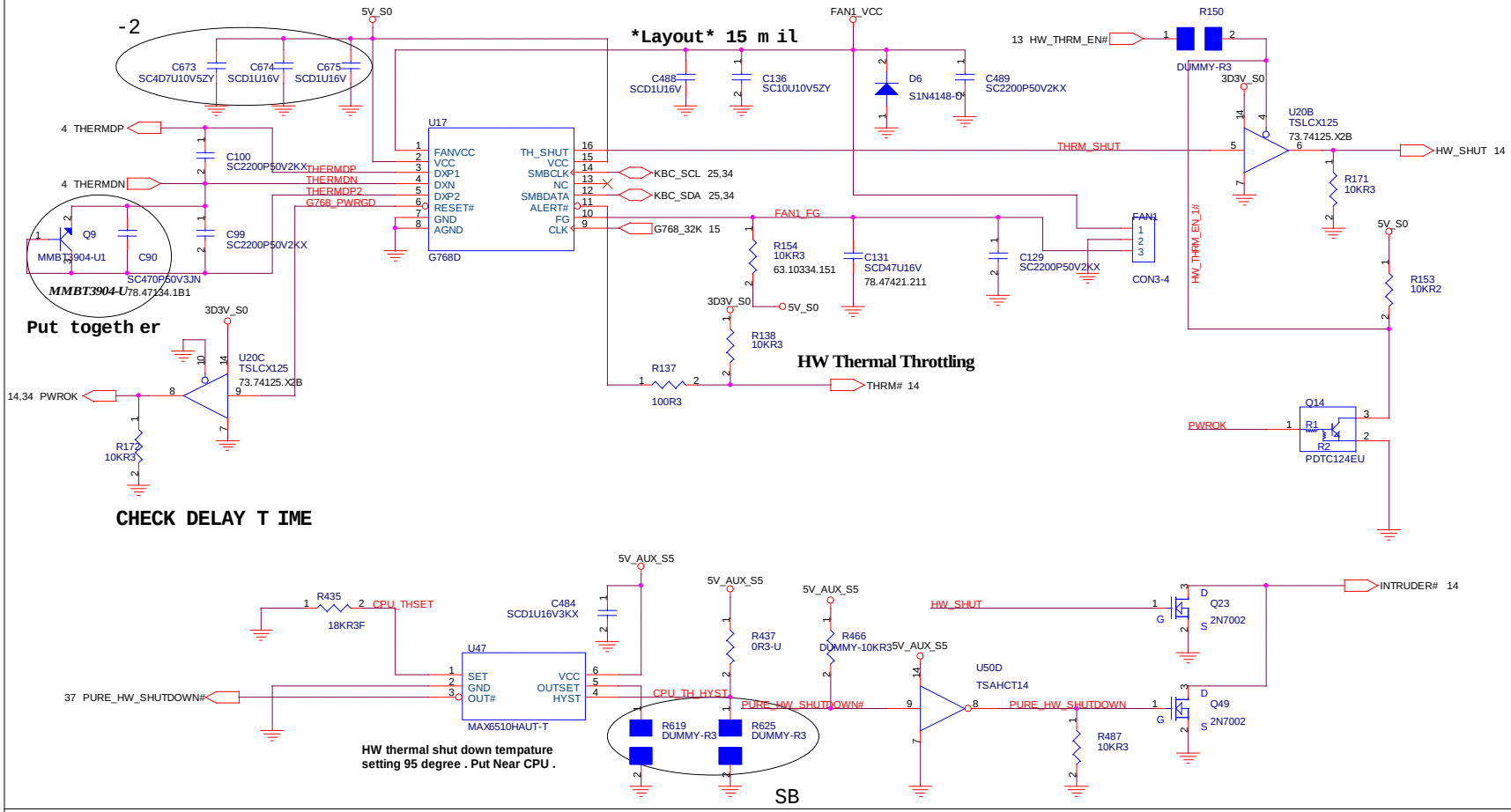
G768D thermal sensor & Fan controller



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Thermal/Fan Controllor***	
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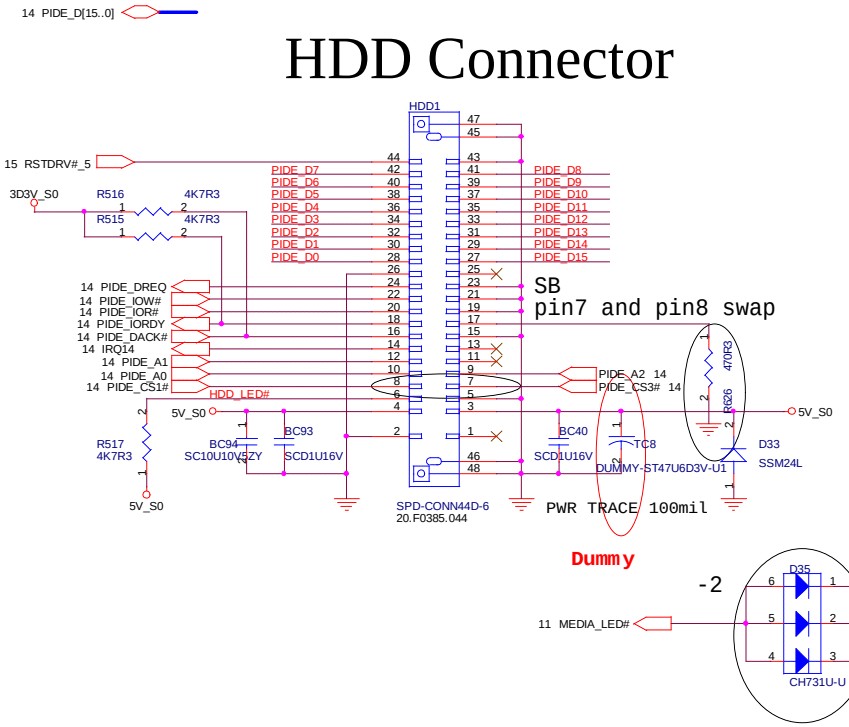
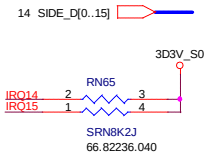
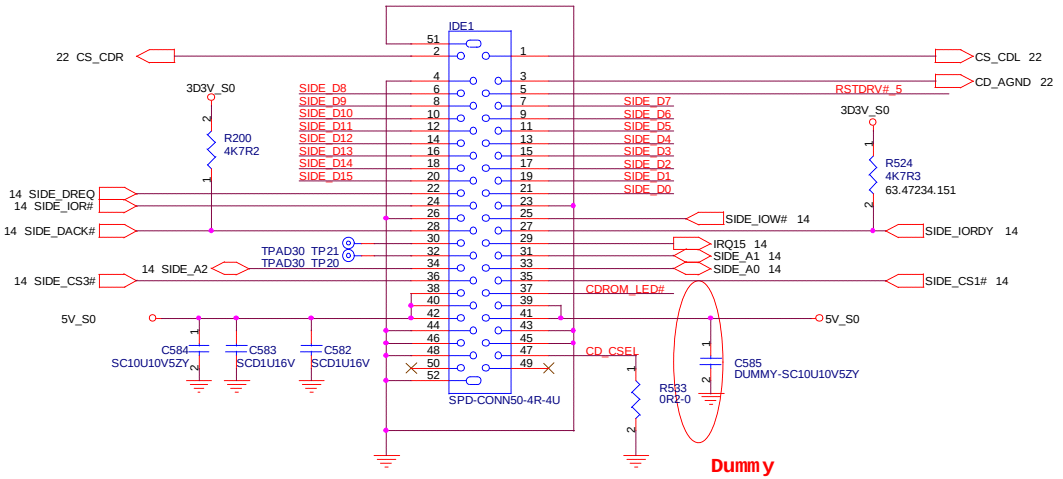
HDD Connector



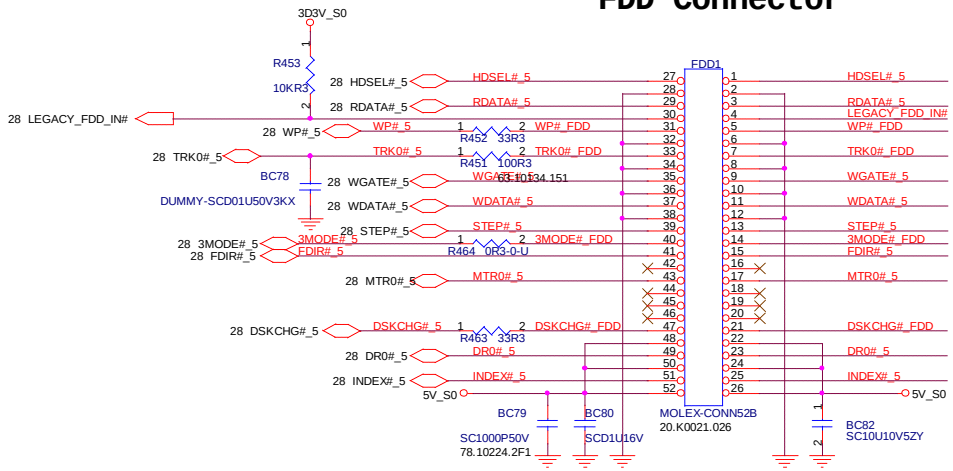


CD-ROM CONN



CHECK PIDE/SIDE DIAG# PIN

FDD Connector



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD and CDROM and FDD CONN**

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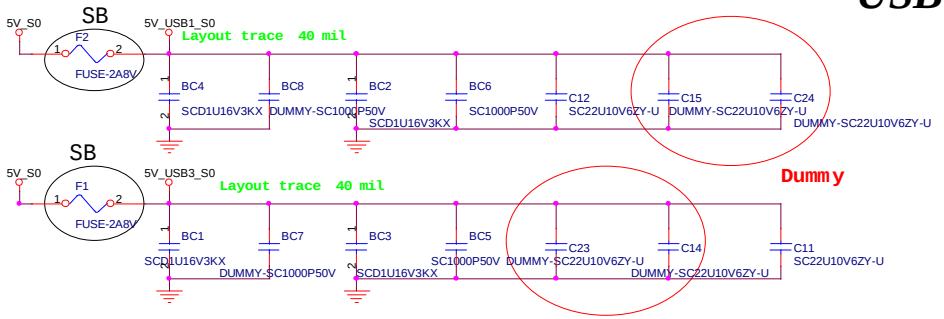
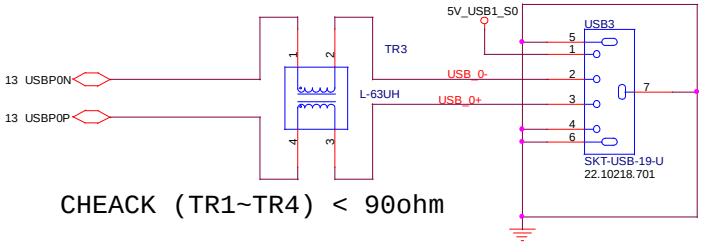
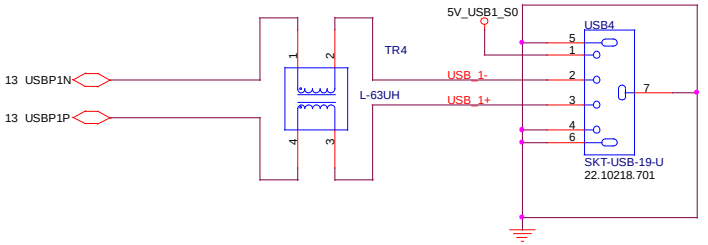
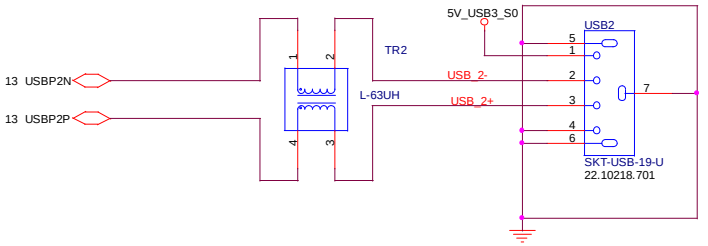
USB PORT

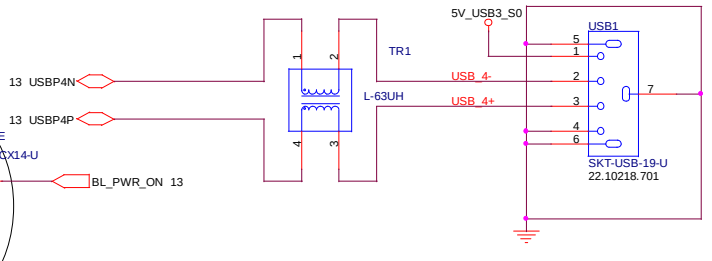


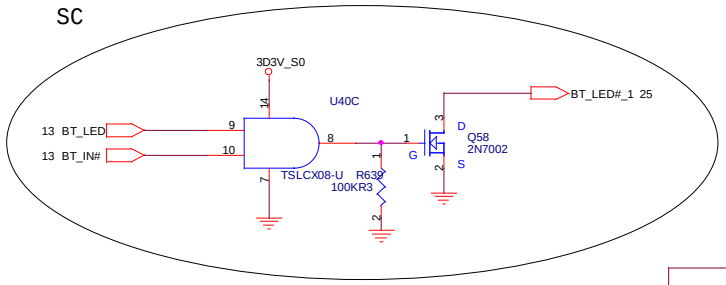


CHEACK (TR1~TR4) < 90ohm

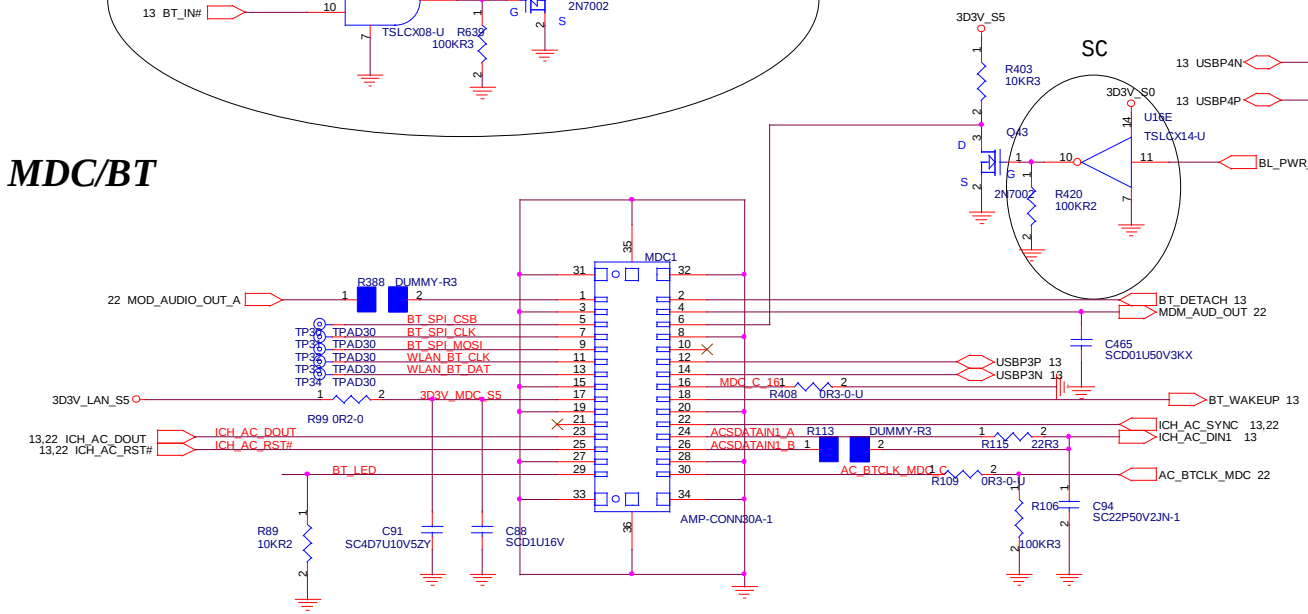


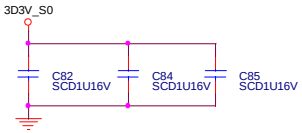






MDC/BT





緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***USB and MDC I/F and LAN***	
Size A3	Document Number YUHINA	Rev **SC**
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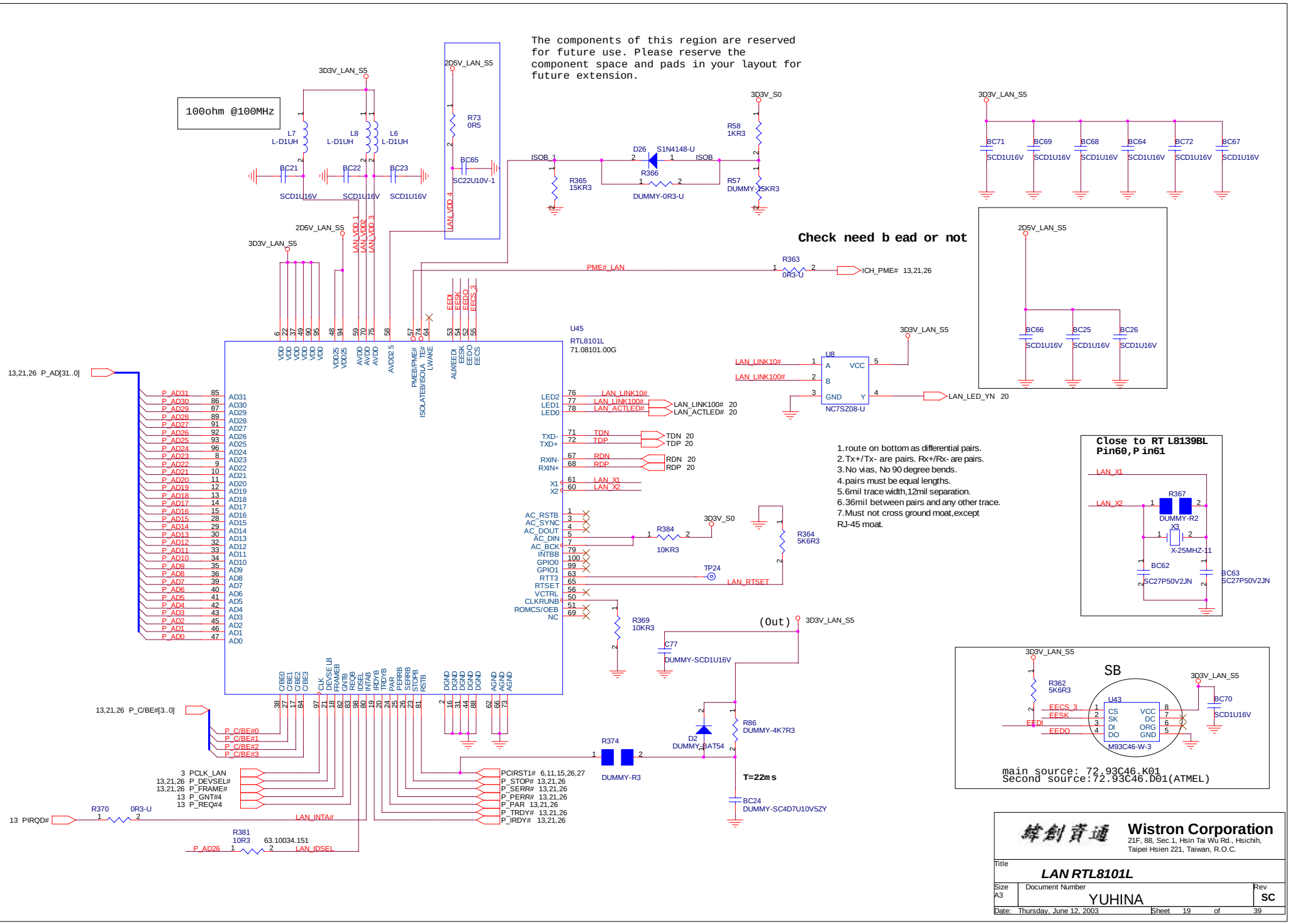
The components of this region are reserved for future use. Please reserve the component space and pads in your layout for future extension.
100ohm @100MHz
Check need b ead or not
Close to RT L8139BL Pin60,Pin61
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width,12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat,except RJ-45 moat.
SB
main source: 72.93C46.K01
Second source:72.93C46.D01(ATMEL)
T=22ms
U45
RTL8101L
71.08101.00G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
LAN RTL8101L
YUHINA
Date: Thursday, June 12, 2003
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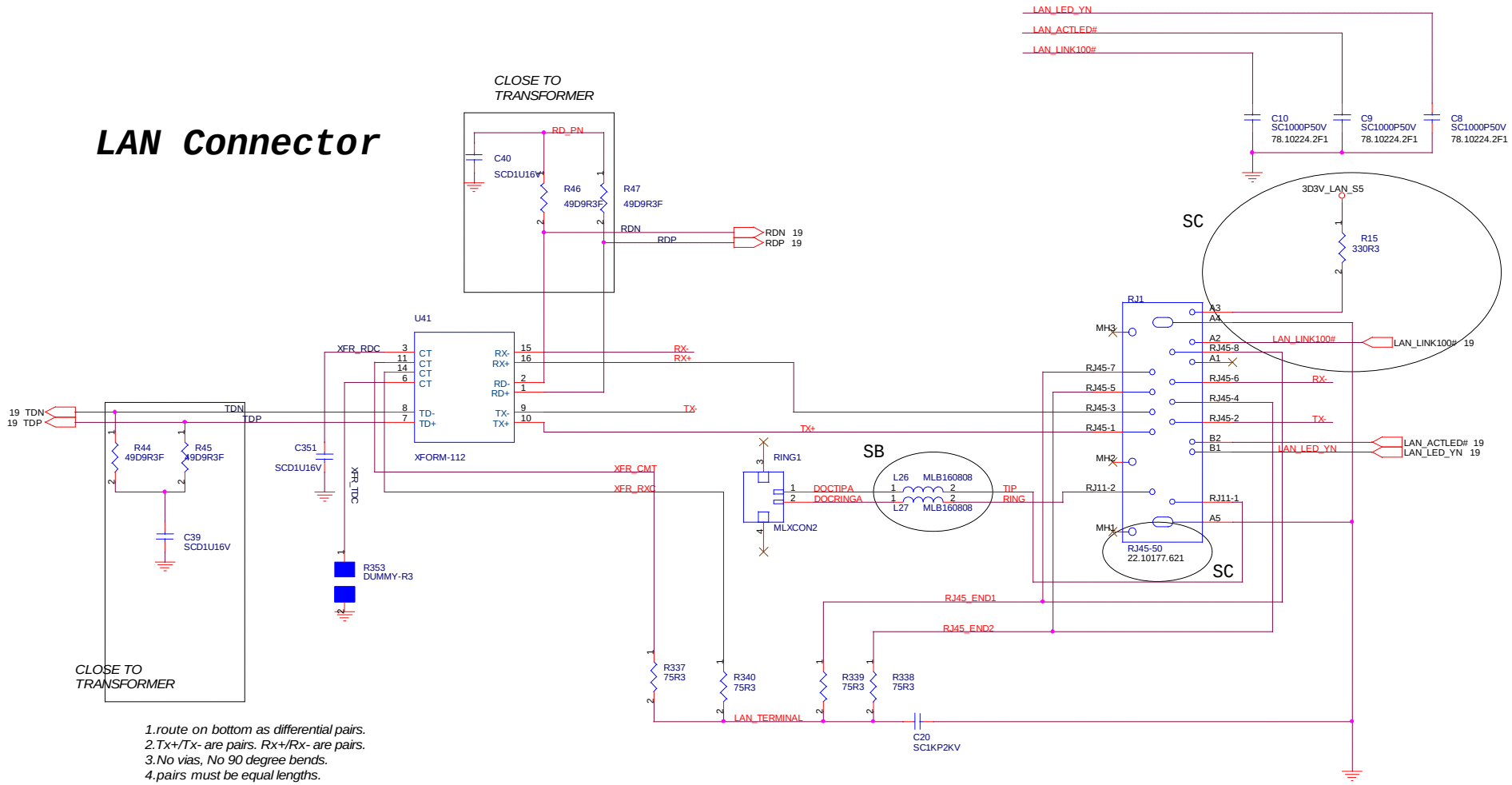
LAN Connector



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

Green LED---Speed100:O N/Speed10:OFF
Yellow LED---Link:ON ,TX/RX:Flash

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN Connector

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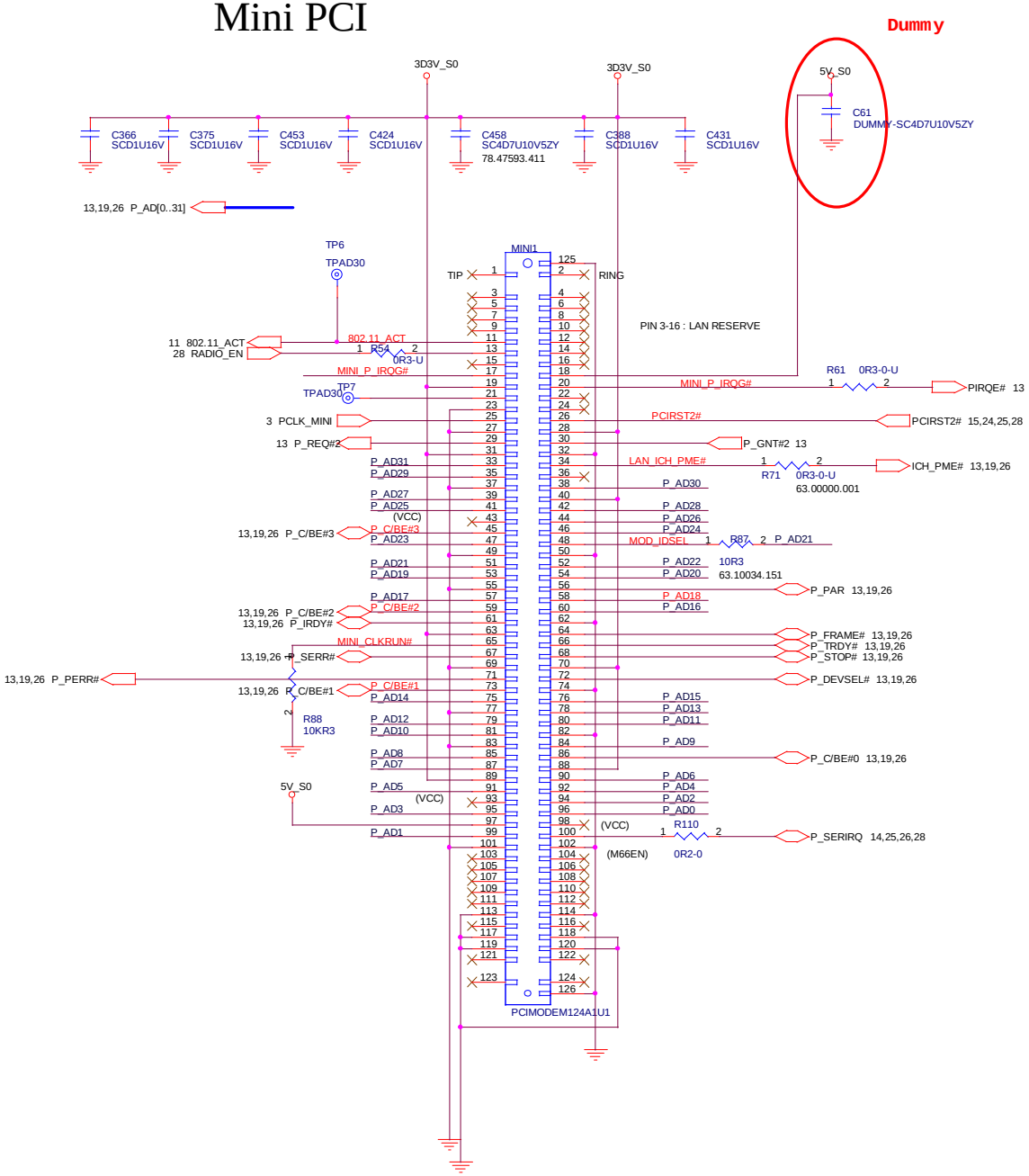
Mini PCI



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI-PCI***	
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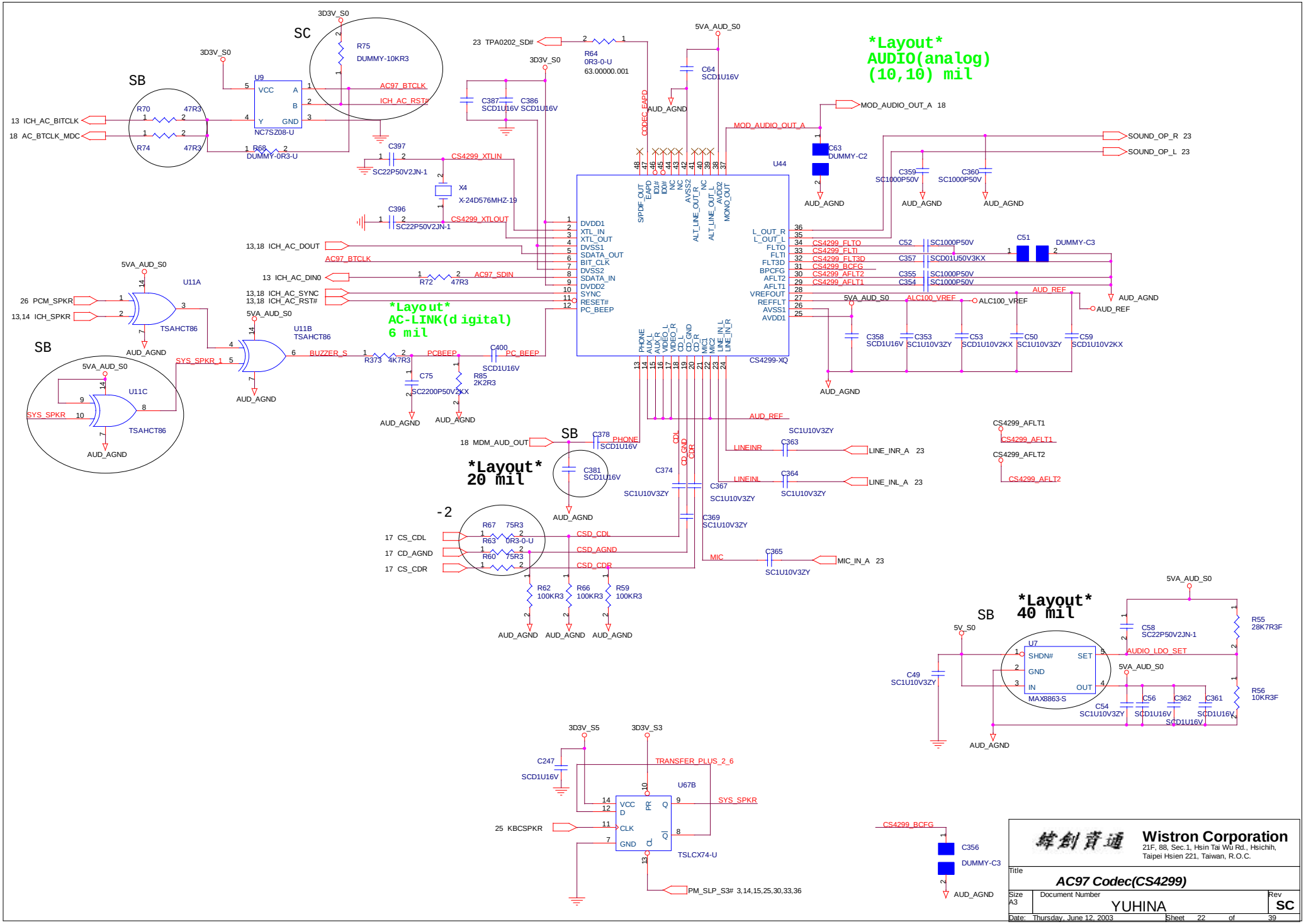
Layout
AUDIO(analog)
(10,10) mil
Layout
AC-LINK(digital)
6 mil
Layout
20 mil
Layout
40 mil
SC
SB
-2
U44
CS4299-XQ
U9
NC7SZ08-U
U11A
U11B
U11C
TSAHCT86
U7
MAX8863-S
U67B
TSLCX74-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
AC97 Codec(CS4299)
Size A3
Document Number
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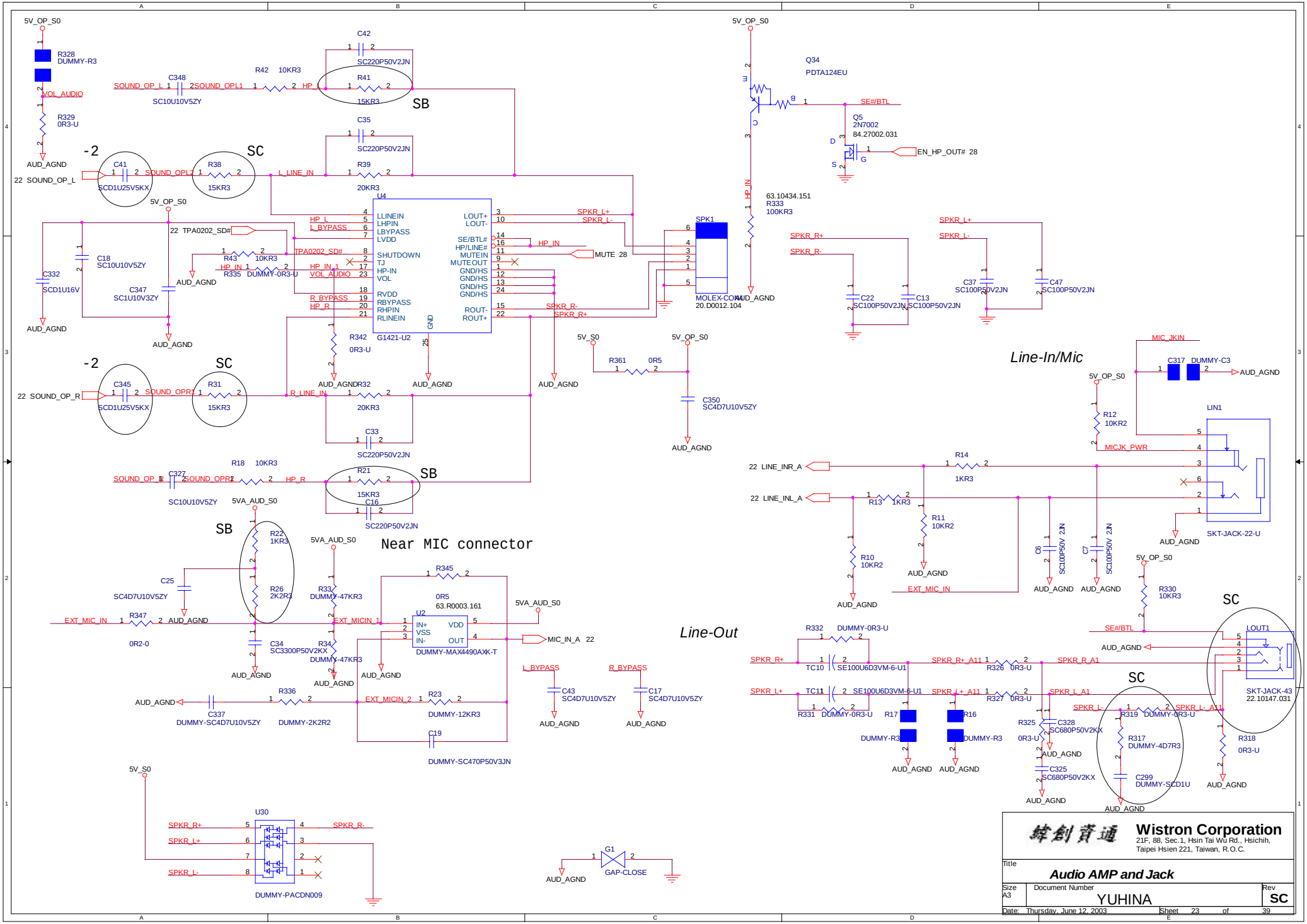
Near MIC connector
Line-Out
Line-In/Mic
SB
SC
-2
U4
G1421-U2
U2
DUMMY-MAX4490AXK-T
U30
DUMMY-PACDN009
SPK1
MOLEX-CONN
20.D0012.104
Q34
PDTA124EU
Q5
2N7002
84.27002.031
63.10434.151
R333
100KR3
SKT-JACK-22-U
SKT-JACK-43
22.10147.031
GAP-CLOSE
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Audio AMP and Jack
YUHINA
SC
Thursday, June 12, 2003
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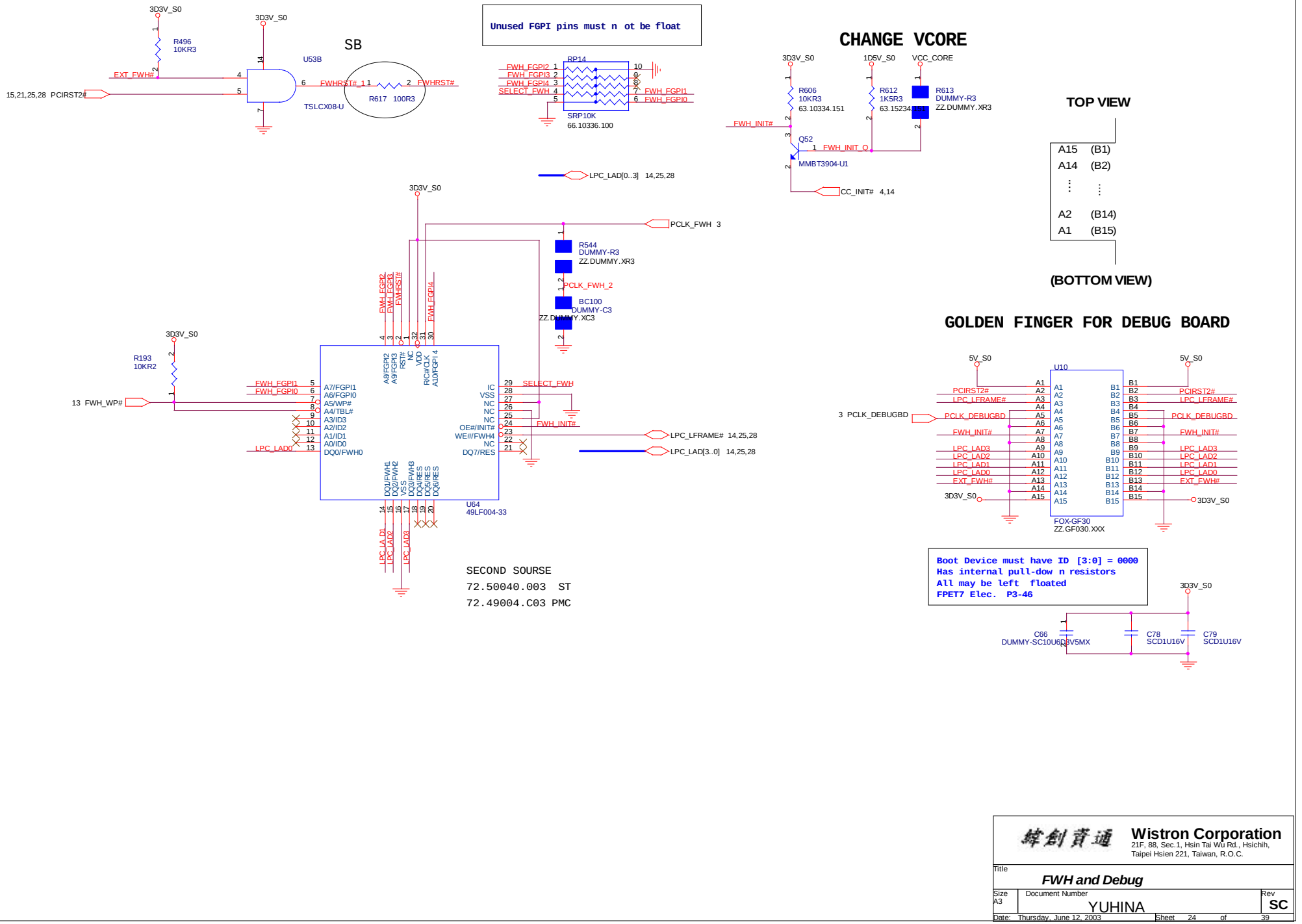
39



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*FWH and Debug*
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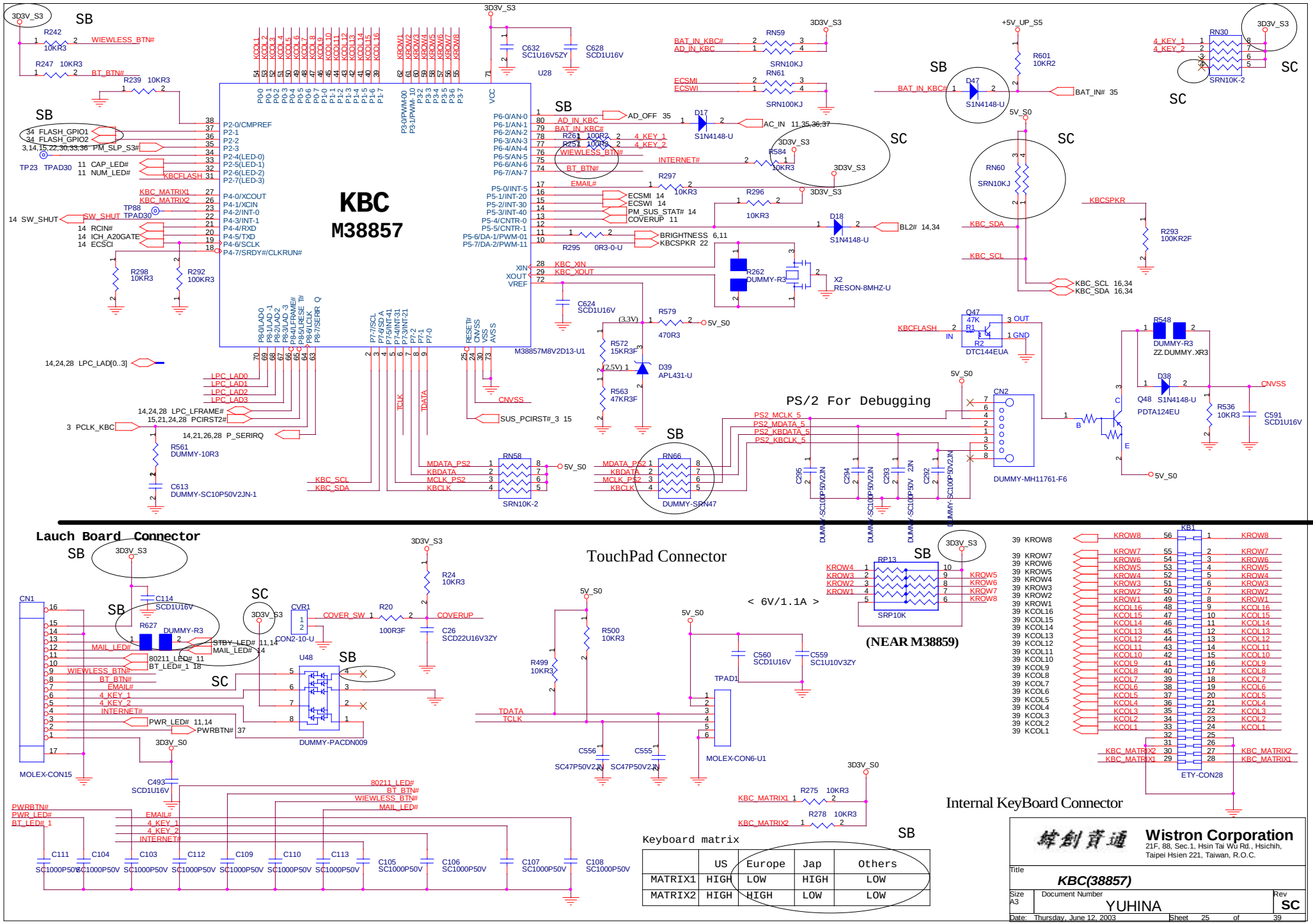
KBC
M38857
PS/2 For Debugging
Lauch Board Connector
TouchPad Connector
< 6V/1.1A >
(NEAR M38859)
Internal KeyBoard Connector
Keyboard matrix
US
Europe
Jap
Others
MATRIX1
HIGH
LOW
HIGH
LOW
MATRIX2
HIGH
HIGH
LOW
LOW
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
KBC(38857)
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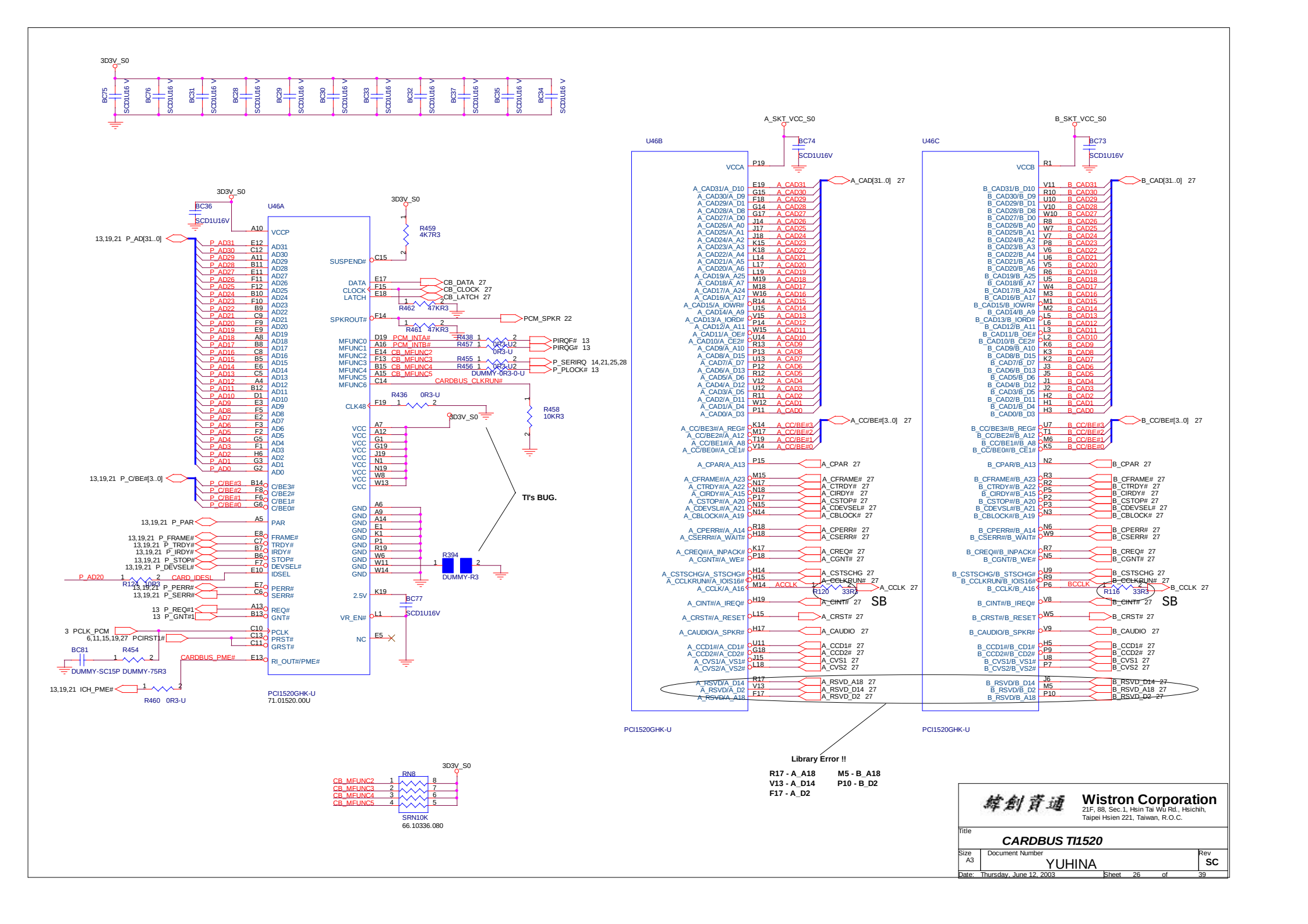
3D3V_S0
BC75 SCD1U16V
BC76 SCD1U16V
BC31 SCD1U16V
BC28 SCD1U16V
BC29 SCD1U16V
BC30 SCD1U16V
BC33 SCD1U16V
BC32 SCD1U16V
BC37 SCD1U16V
BC35 SCD1U16V
BC34 SCD1U16V
U46A
PCI1520GHK-U
71.01520.00U
U46B
U46C
A_SKT_VCC_S0
B_SKT_VCC_S0
BC74 SCD1U16V
BC73 SCD1U16V
TI's BUG.
Library Error !!
R17 - A_A18
V13 - A_D14
F17 - A_D2
M5 - B_A18
P10 - B_D2
SB
SRN10K
66.10336.080
Wistron Corporation
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Title
CARDBUS TI1520
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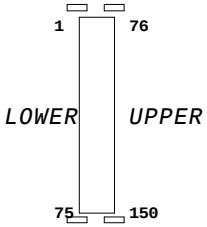
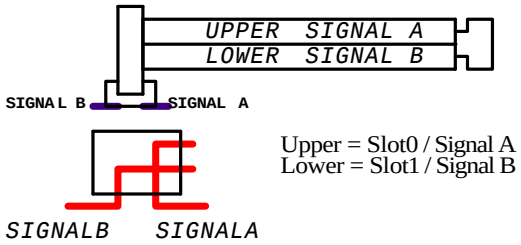
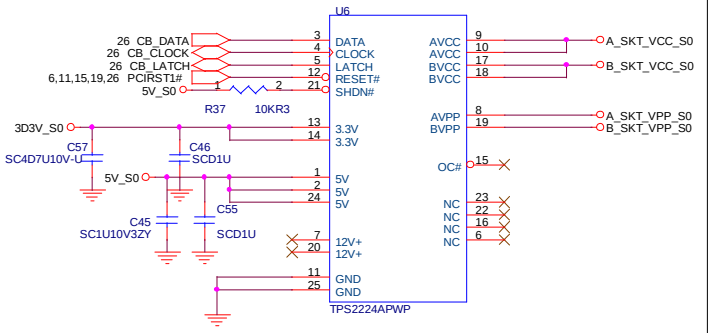
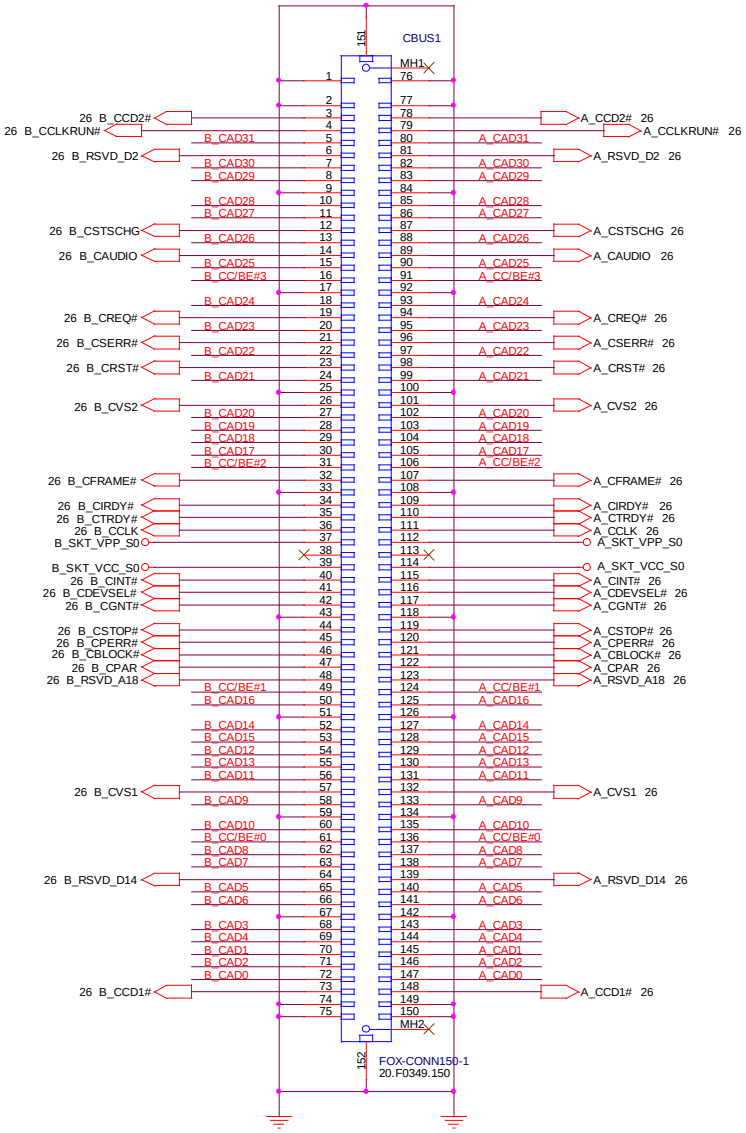
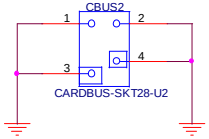


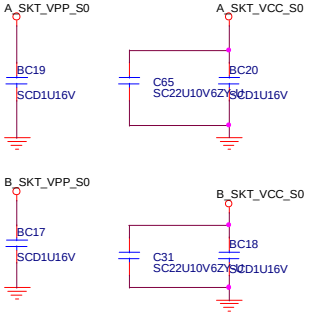


Upper = Slot0 / Signal A = Conn B
Lower = Slot1 / Signal B = Conn A









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Title	***CARDBUS CONN / PWR SW***	
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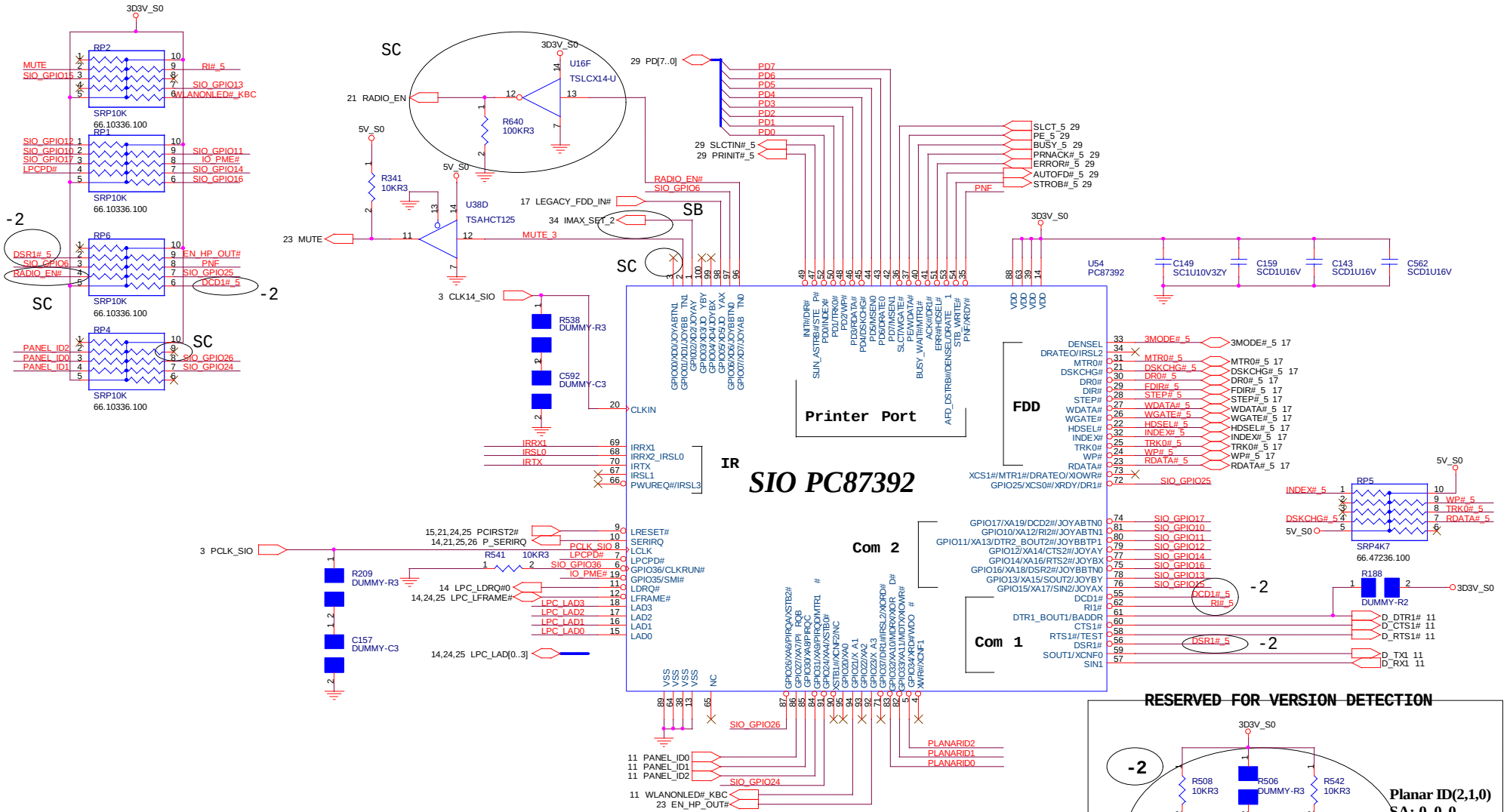
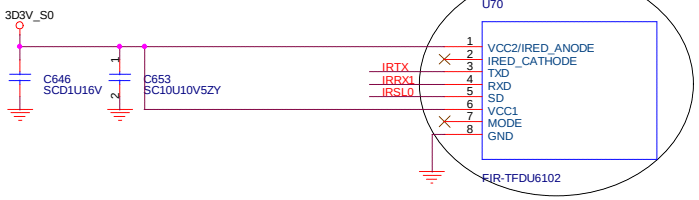


Infineon FIR Module

SB

Layout Guide:
(1) FIR_5V : 30 mils



PANEL ID DEFINE			
PANEL_ID2	PANEL_ID1	PANEL_ID0	VENDORS
1	1	1	No Panel
0	1	1	Hitachi (15")
0	1	1	AU (15")
0	1	1	CMO(15")
1	0	0	CMO(14")
1	0	1	AU (14")
1	1	0	AU (14")**

Note : AU (¤ ¹),CMO(© ¬),** : With Digitizer

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Title: *SIO(87392)*

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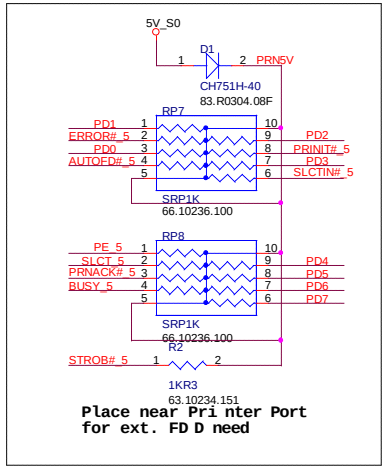
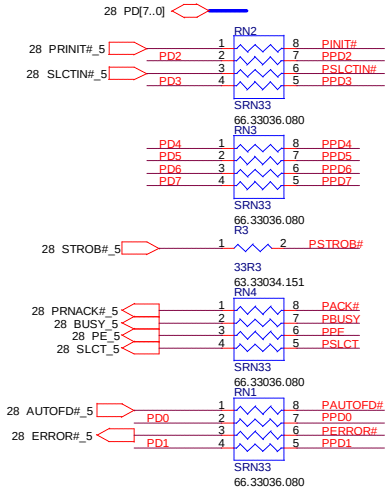
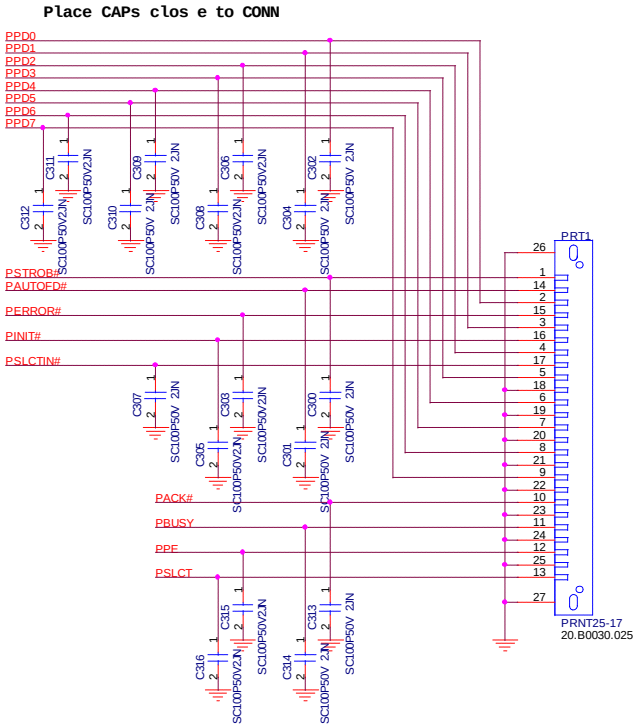
PRINTER PORT







鋒創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Parallel Port***	
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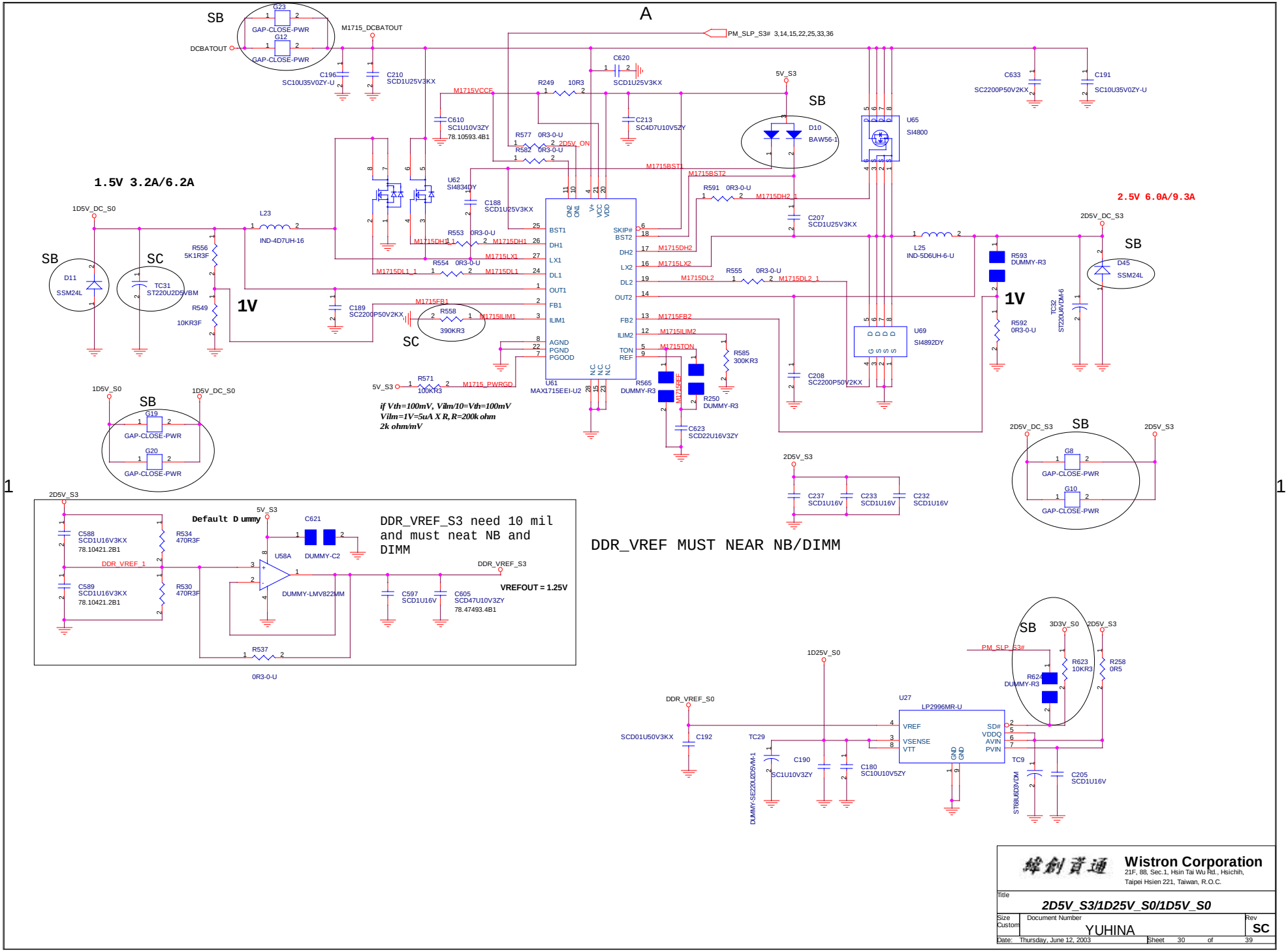
1.5V 3.2A/6.2A
2.5V 6.0A/9.3A
1V
1V
SB
SC
DDR_VREF_S3 need 10 mil and must neat NB and DIMM
DDR_VREF MUST NEAR NB/DIMM
if Vth=100mV, Vilm/10=Vth=100mV
Vilm=1V=5uA X R, R=200k ohm
2k ohm/mV
Default Dummy
VREFOUT = 1.25V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
2D5V_S3/1D25V_S0/1D5V_S0
Size Custom
Document Number
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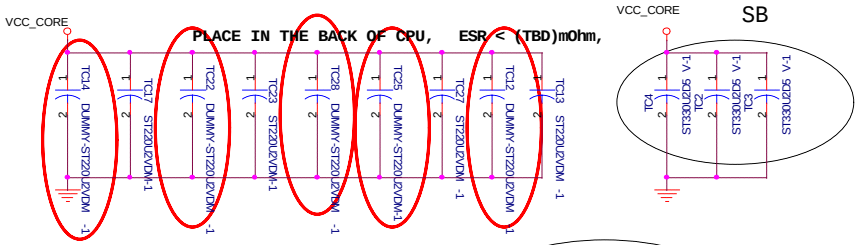
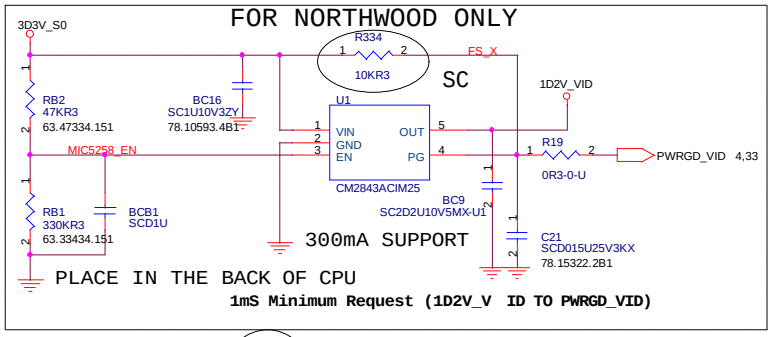
CPU_Vcore IMVP5_FMS0(1/2)

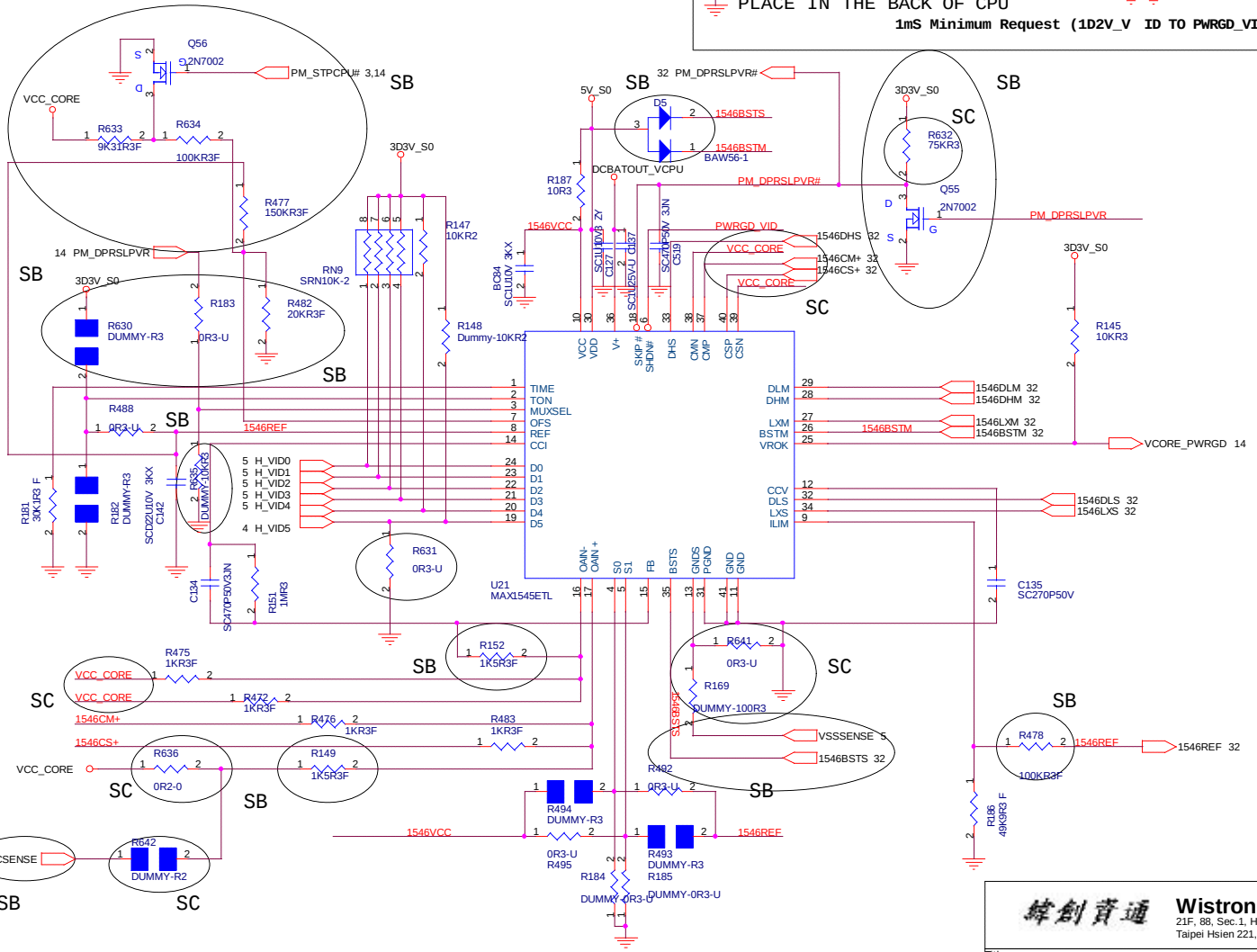


Dummy

Voltage Identica tion Codes

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
	1	1	1	1	1	OFF
	1	1	1	1	0	1.100
	1	1	1	0	1	1.125
	1	1	1	0	0	1.150
	1	1	0	1	1	1.175
	1	1	0	1	0	1.200
	1	1	0	0	1	1.225
	1	1	0	0	0	1.250
	1	0	1	1	1	1.275
	1	0	1	1	0	1.300
	1	0	1	0	1	1.325
	1	0	1	0	0	1.350
	1	0	0	1	1	1.375
	1	0	0	1	0	1.400
	1	0	0	0	1	1.425
	1	0	0	0	0	1.450
	0	1	1	1	1	1.475
	0	1	1	1	0	1.500
	0	1	1	0	1	1.525
	0	1	1	0	0	1.550
	0	1	0	1	1	1.575
	0	1	0	1	0	1.600
	0	1	0	0	1	1.625
	0	1	0	0	0	1.650
	0	0	1	1	1	1.675
	0	0	1	1	0	1.700
	0	0	1	0	1	1.725
	0	0	1	0	0	1.750
	0	0	0	1	1	1.775
	0	0	0	1	0	1.800
	0	0	0	0	1	1.825
	0	0	0	0	0	1.850





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Title	CPU_Vcore IMVP5_FMS0(1/2)	
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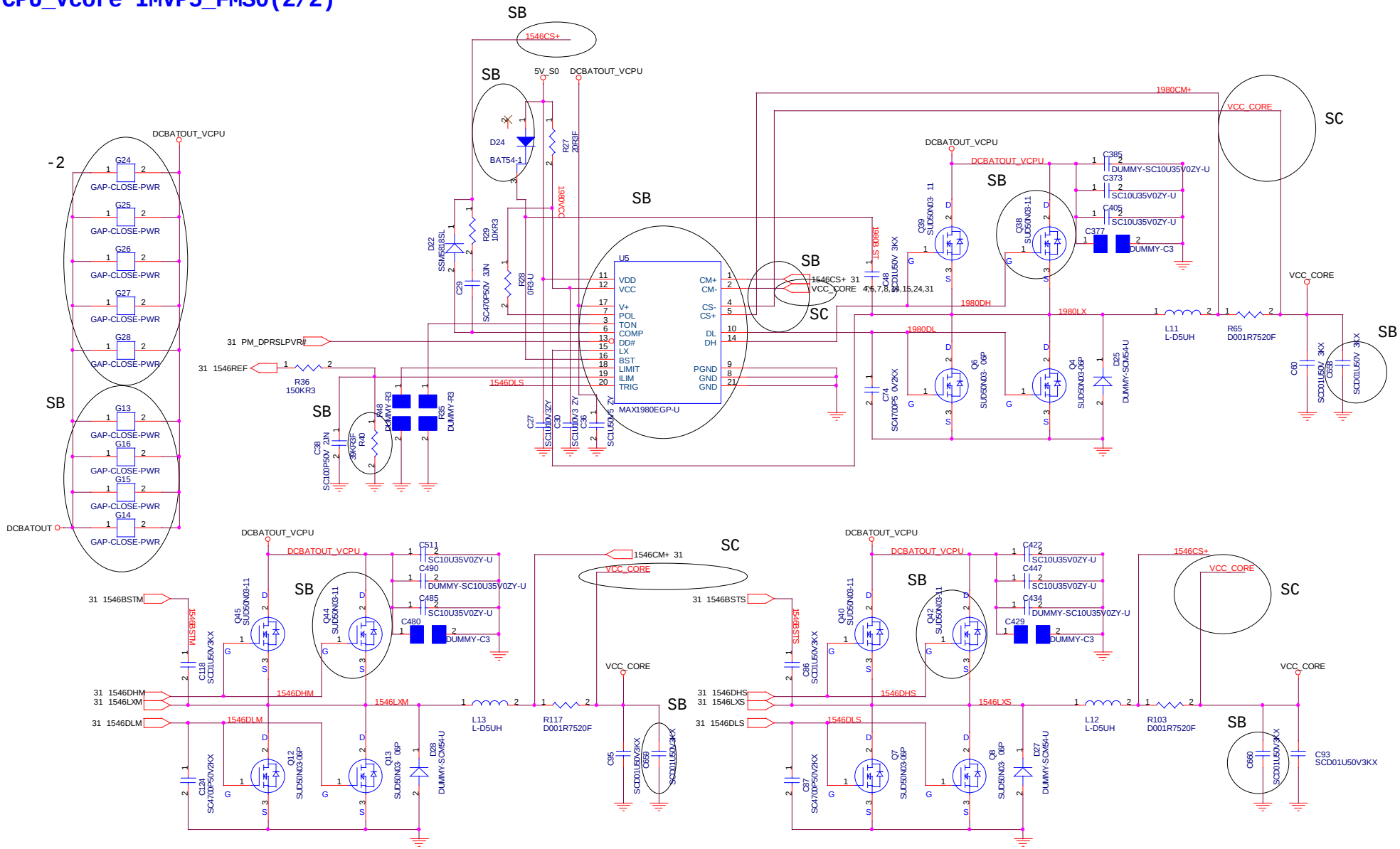
CPU_Vcore IMVP5_FMS0(2/2)



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*CPU_Vcore IMVP5_FMS0(2/2)*	
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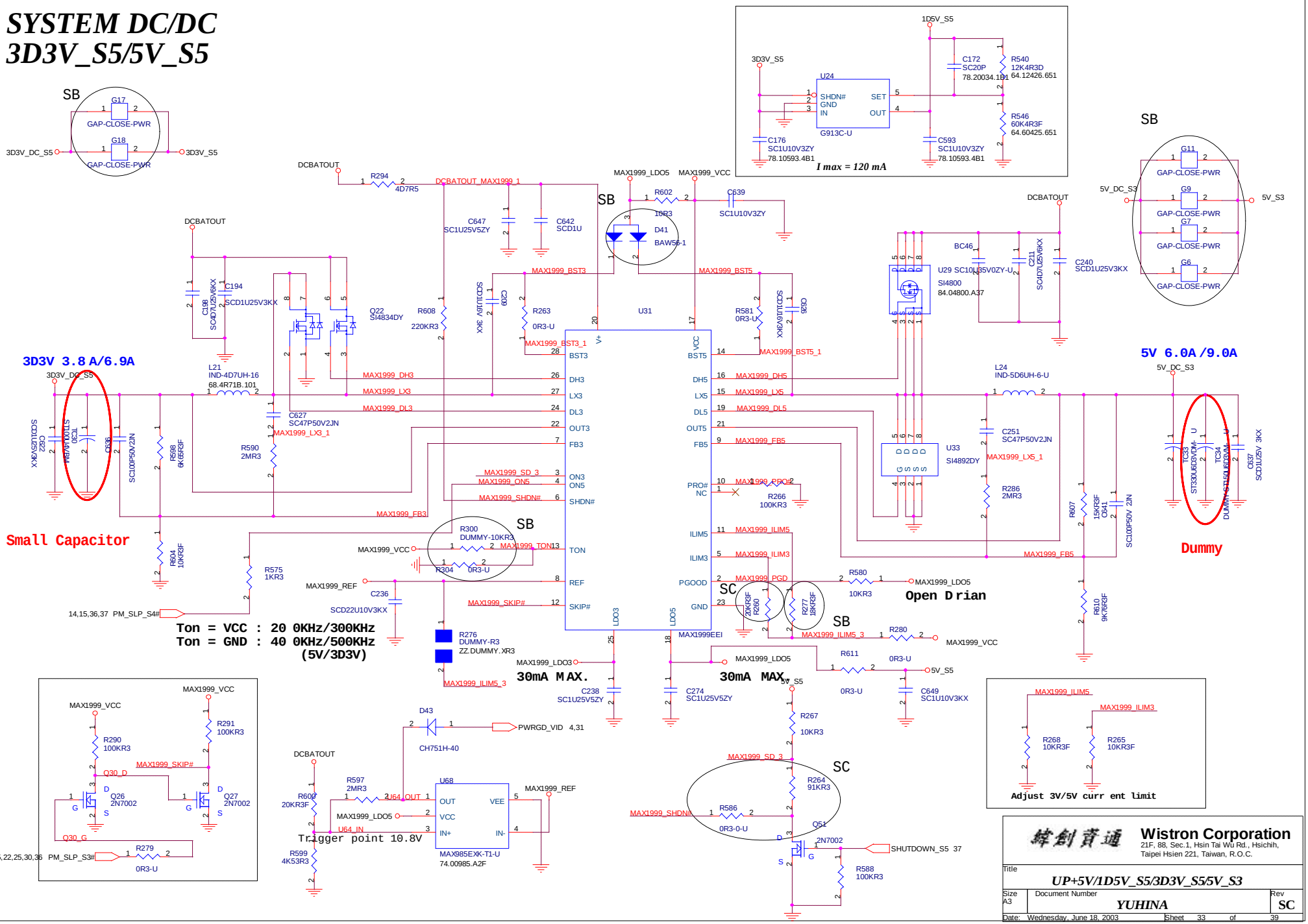
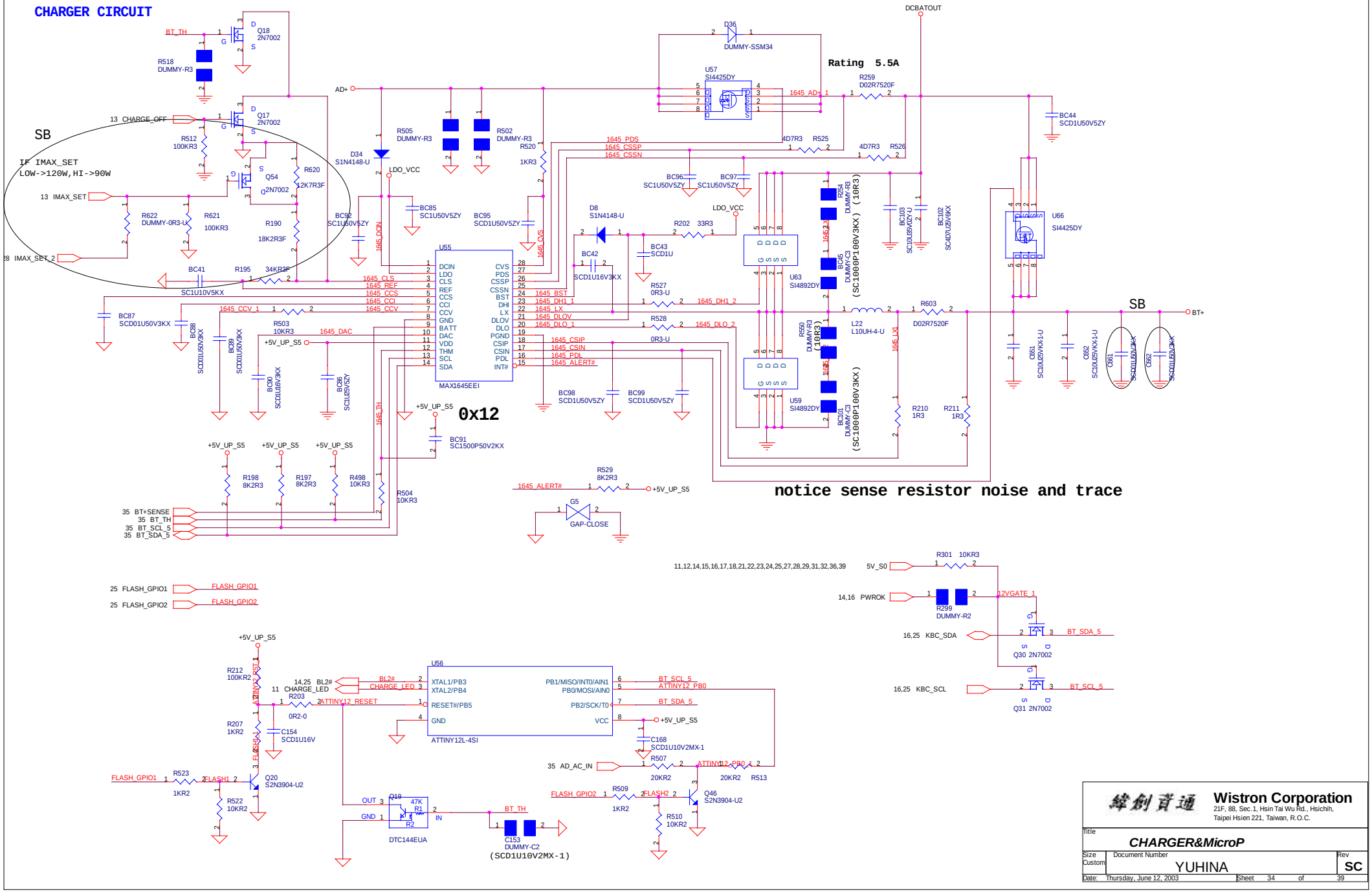
SYSTEM DC/DC
3D3V_S5/5V_S5




CHARGER CIRCUIT
SB
IF IMAX_SET
LOW->120W,HI->90W
13 IMAX_SET
28 IMAX_SET_2
13 CHARGE_OFF
BT_TH
Q18 2N7002
Q17 2N7002
Q54 2N7002
R518 DUMMY-R3
R512 100KR3
R620 12K7R3F
R622 DUMMY-0R3-U
R621 100KR3
R190 18K2R3F
R195 34K2R3F
BC41 SC1U10V5KX
AD+
D34 S1N4148-U
LDO_VCC
R505 DUMMY-R3
R502 DUMMY-R3
R520 1KR3
BC85 SC1U50V5ZY
BC90 SC1U50V5ZY
BC95 SCD1U50V5ZY
1645_DCIN
1645_CVS
U55
MAX1645EEI
DCIN
LDO
CLS
REF
CCS
CCI
CCV
GND
BATT
DAC
VDD
THM
SCL
SDA
CVS
PDS
CSSP
CSSN
BST
DHI
LX
DLOV
DLO
PGND
CSIP
CSIN
PDL
INT#
1645_CLS
1645_REF
1645_CCS
1645_CCI
1645_CCV
1645_CCV_1
1645_DAC
1645_BST
1645_DH1_1
1645_LX
1645_DLOV
1645_DLO_1
1645_CSIP
1645_CSIN
1645_PDL
1645_ALERT#
BC87 SCD01U50V3KX
BC88 SCD01U50V3KX
BC89 SCD01U50V3KX
BC90 SCD1U16V3KX
BC86 SC1U25V5ZY
R503 10KR3
+5V_UP_S5
0x12
BC91 SC1500P50V2KX
1645_TH
R198 8K2R3
R197 8K2R3
R498 10KR3
R504 10KR3
35 BT+SENSE
35 BT_TH
35 BT_SCL_5
35 BT_SDA_5
D36 DUMMY-SSM34
U57 SI4425DY
1645_AD+_1
Rating 5.5A
R259 D02R7520F
DCBATOUT
BC44 SCD1U50V5ZY
1645_PDS
1645_CSSP
1645_CSSN
4D7R3 R525
4D7R3 R526
BC96 SC1U50V5ZY
BC97 SC1U50V5ZY
D8 S1N4148-U
R202 33R3
BC42 SCD1U16V3KX
BC43 SCD1U
R527 0R3-U
R528 0R3-U
1645_DH1_2
1645_DLO_2
1645_LX
BC98 SCD1U50V5ZY
BC99 SCD1U50V5ZY
U63 SI4892DY
U59 SI4892DY
R550 DUMMY-R3 (10R3)
R254 DUMMY-R3
BC45 DUMMY-C3
BC101 DUMMY-C3
(SC1000P100V3KX) (10R3)
(SC1000P100V3KX)
BC103 SC10U06V0Z-U
BC102 SC4D7U25V9KX
U66 SI4425DY
L22 L10UH-4-U
R603 D02R7520F
BT+
SB
C061 SC10U25VKX1-U
C062 SC10U25VKX1-U
R210 1R3
R211 1R3
R529 8K2R3
G5 GAP-CLOSE
GAP-CLOSE
notice sense resistor noise and trace
11,12,14,15,16,17,18,21,22,23,24,25,27,28,29,31,32,36,39
5V_S0
R301 10KR3
14,16 PWROK
R299 DUMMY-R2
12VGATE_1
16,25 KBC_SDA
16,25 KBC_SCL
Q30 2N7002
Q31 2N7002
BT_SDA_5
BT_SCL_5
25 FLASH_GPIO1
25 FLASH_GPIO2
FLASH_GPIO1
FLASH_GPIO2
U56
ATTINY12L-4SI
XTAL1/PB3
XTAL2/PB4
RESET#/PB5
GND
PB1/MISO/INT0/AIN1
PB0/MOSI/AIN0
PB2/SCK/T0
VCC
ATTINY12_RESET
ATTINY12_PB0
BL2#
CHARGE_LED
14,25 BL2#
11 CHARGE_LED
R212 100KR2
R203 0R2-0
R207 1KR2
C154 SCD1U16V
C168 SCD1U10V2MX-1
R523 1KR2
R522 10KR2
Q20 S2N3904-U2
35 AD_AC_IN
R507 20KR2
R513 20KR2
R509 1KR2
R510 10KR2
Q46 S2N3904-U2
Q19 DTC144EUA
47K R1
R2
OUT
GND
IN
C153 DUMMY-C2
(SCD1U10V2MX-1)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER&MicroP
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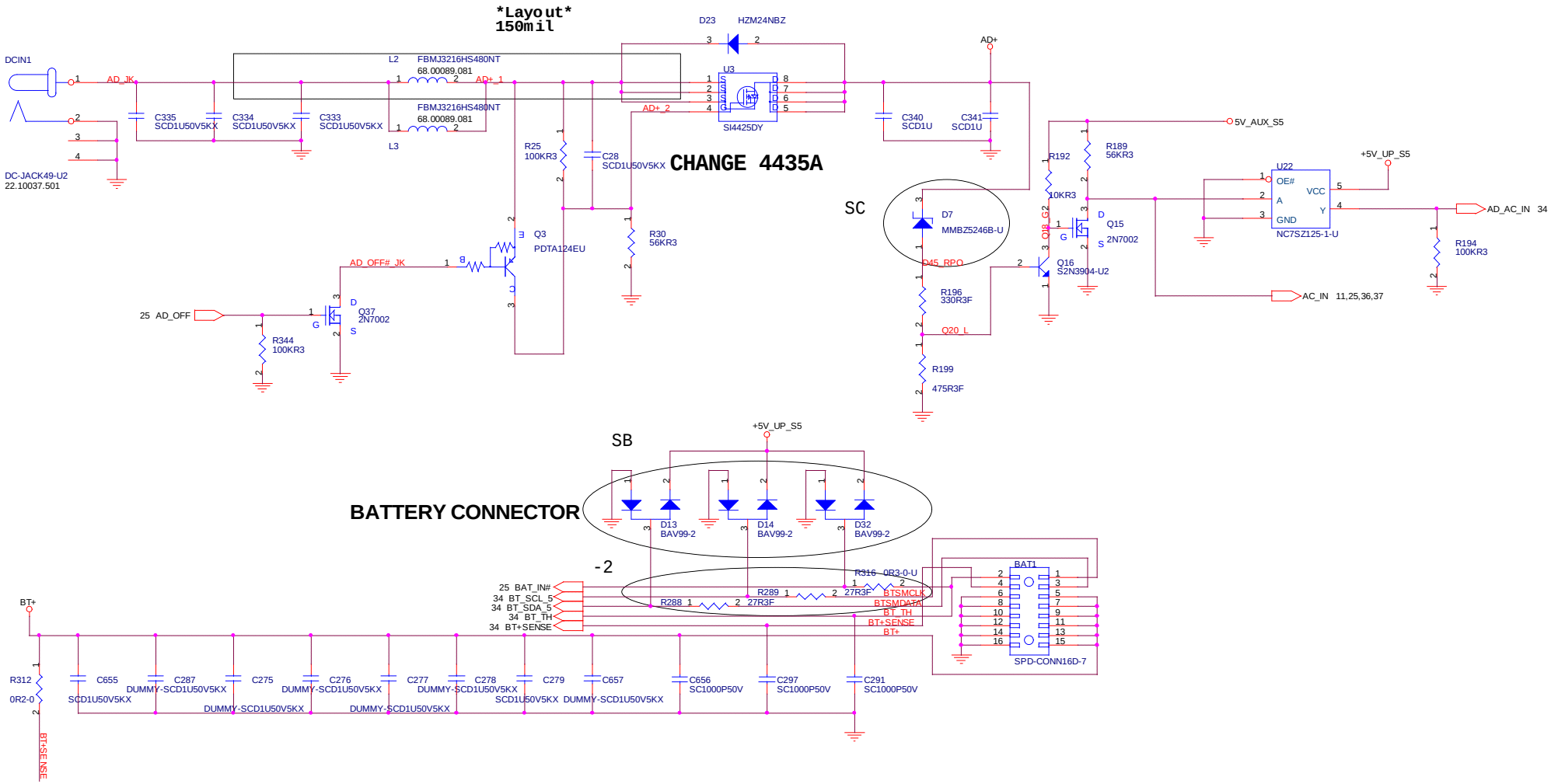
Adaptor in to generate DCBATOUT



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

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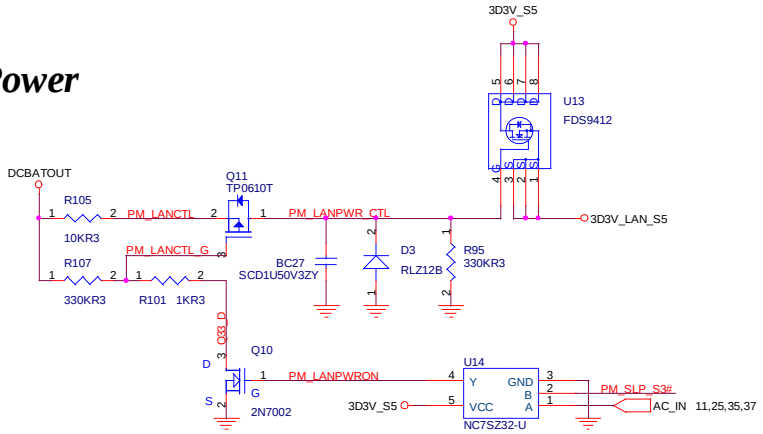
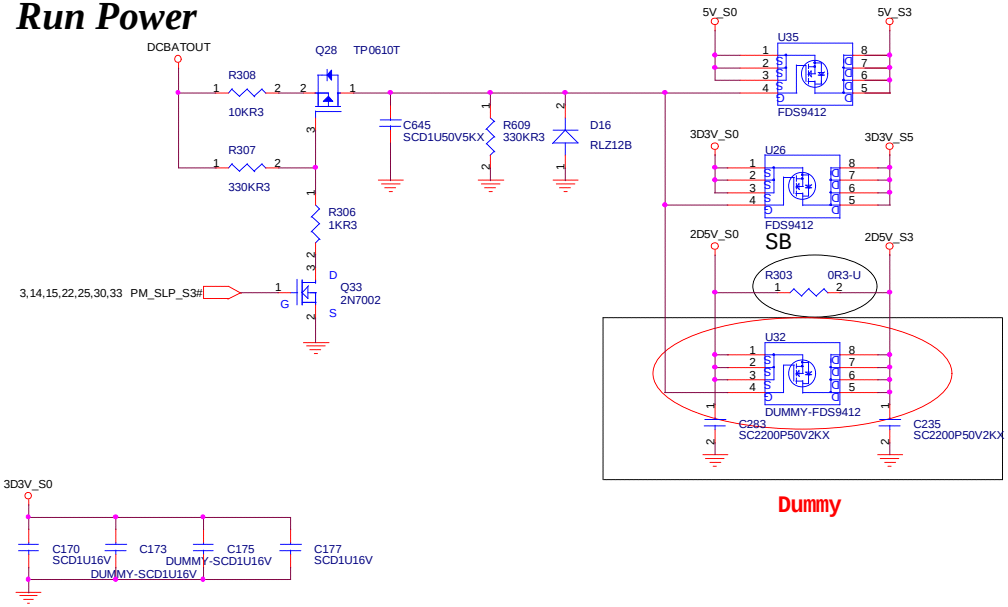
LAN Power

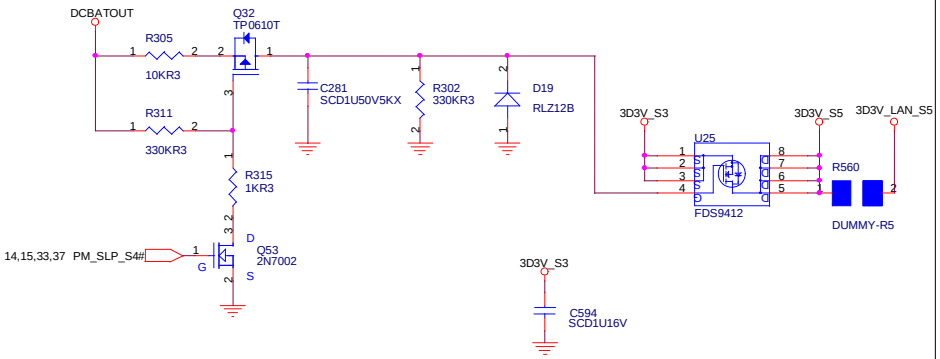


Run Power



Suspend Power

Support standby wakeup LAN only



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PWRPLANE&RESETLOGIC***	
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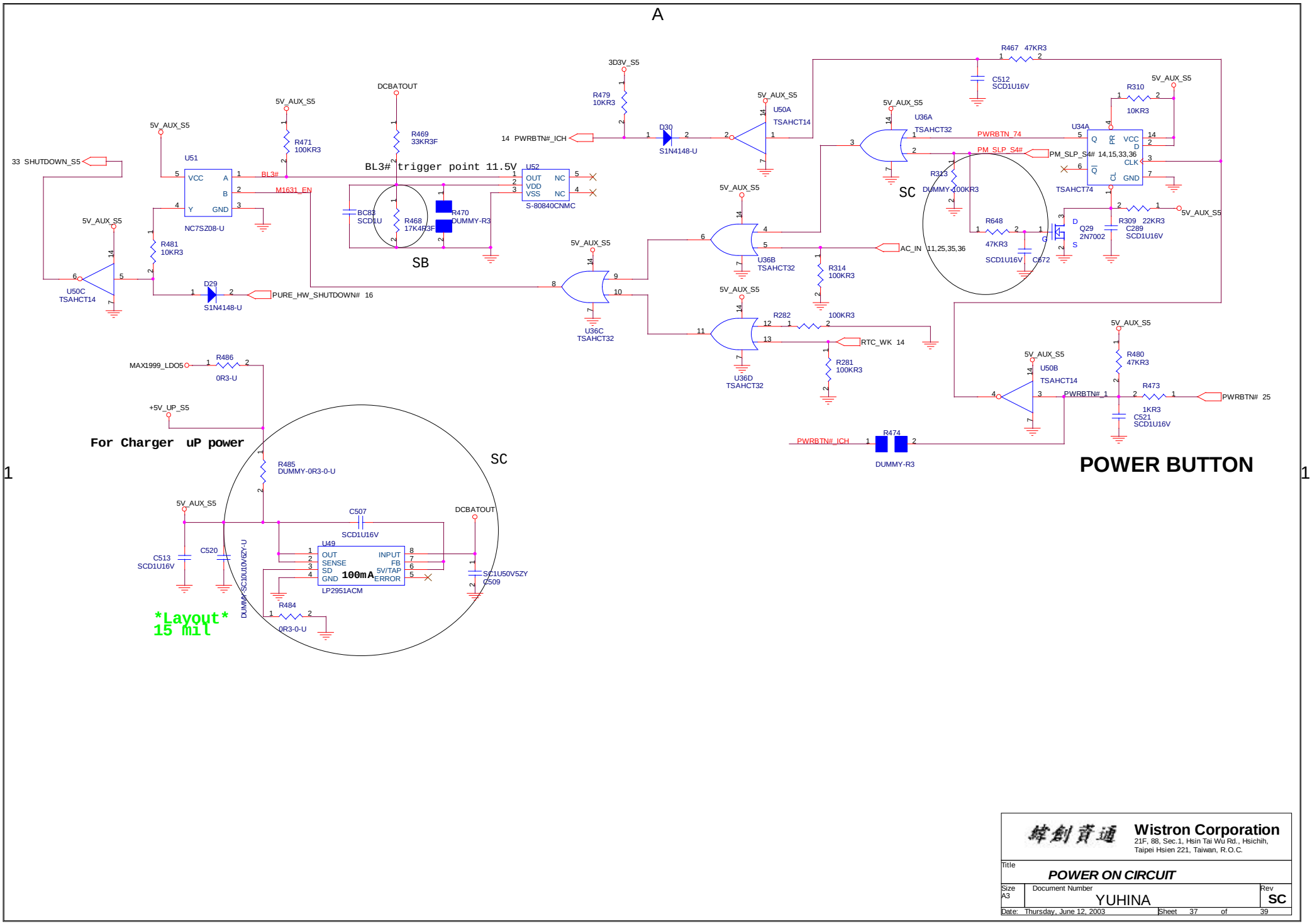
POWER BUTTON
SB
SC
SC
BL3# trigger point 11.5V
For Charger uP power
Layout
15 mil
100mA
33 SHUTDOWN_S5
14 PWRBTN#_ICH
PURE_HW_SHUTDOWN# 16
AC_IN 11,25,35,36
RTC_WK 14
PWRBTN# 25
PWRBTN_74
PM_SLP_S4#
PM_SLP_S4# 14,15,33,36
MAX1999_LDO5
+5V_UP_S5
PWRBTN#_ICH
5V_AUX_S5
3D3V_S5
DCBATOUT
U51
NC7SZ08-U
U52
S-80840CNMC
U50A
U50B
U50C
U36A
U36B
U36C
U36D
TSAHCT14
TSAHCT32
TSAHCT74
U49
LP2951ACM
U34A
D30
S1N4148-U
D29
S1N4148-U
Q29
2N7002
R467 47KR3
C512 SCD1U16V
R479 10KR3
R471 100KR3
R469 33KR3F
R481 10KR3
R468 17K4R3F
R470 DUMMY-R3
BC83 SCD1U
R310 10KR3
R313 DUMMY-100KR3
R648 47KR3
SCD1U16V C672
R309 22KR3
C289 SCD1U16V
R314 100KR3
R282 100KR3
R281 100KR3
R480 47KR3
R473 1KR3
C521 SCD1U16V
R474 DUMMY-R3
R486 0R3-U
R485 DUMMY-0R3-0-U
C507 SCD1U16V
C513 SCD1U16V
C520
DUMMY-SC10U10V6ZY-U
C509 SC1U50V5ZY
R484 0R3-0-U
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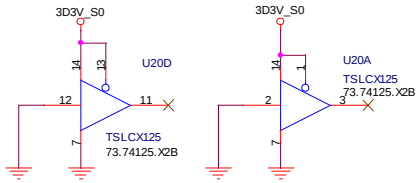
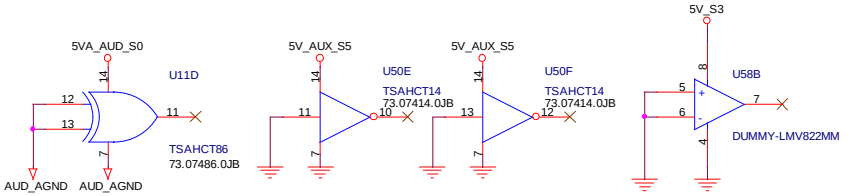
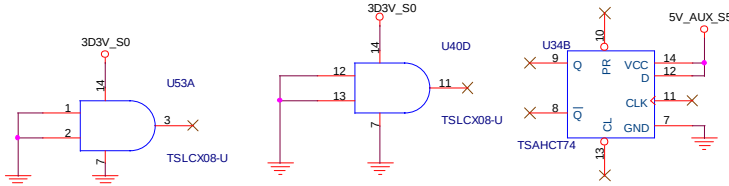
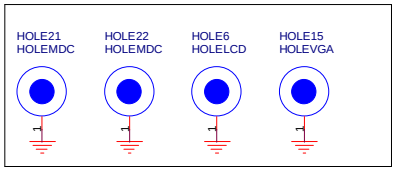
NO USE LOGIC

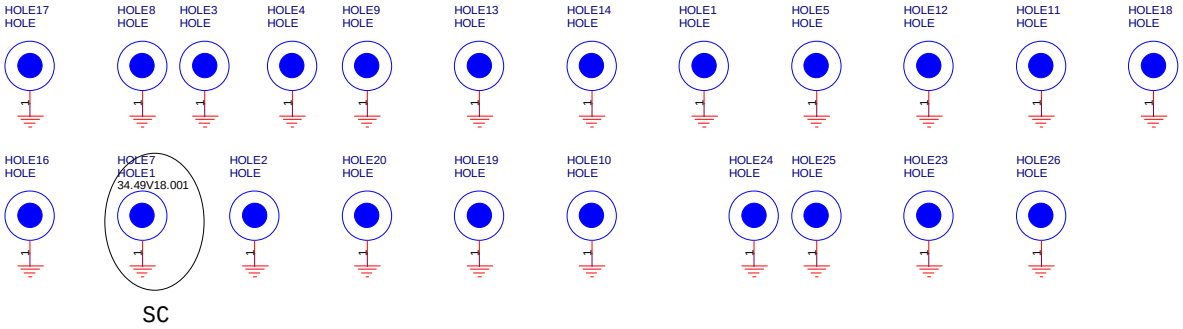


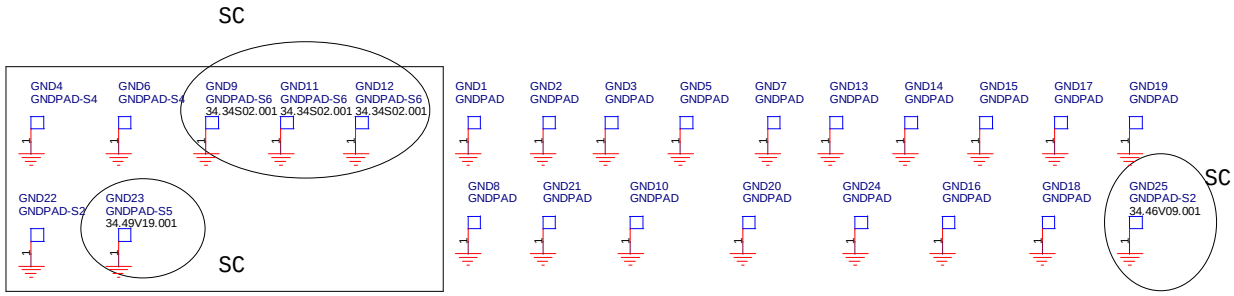






SPARE GATES





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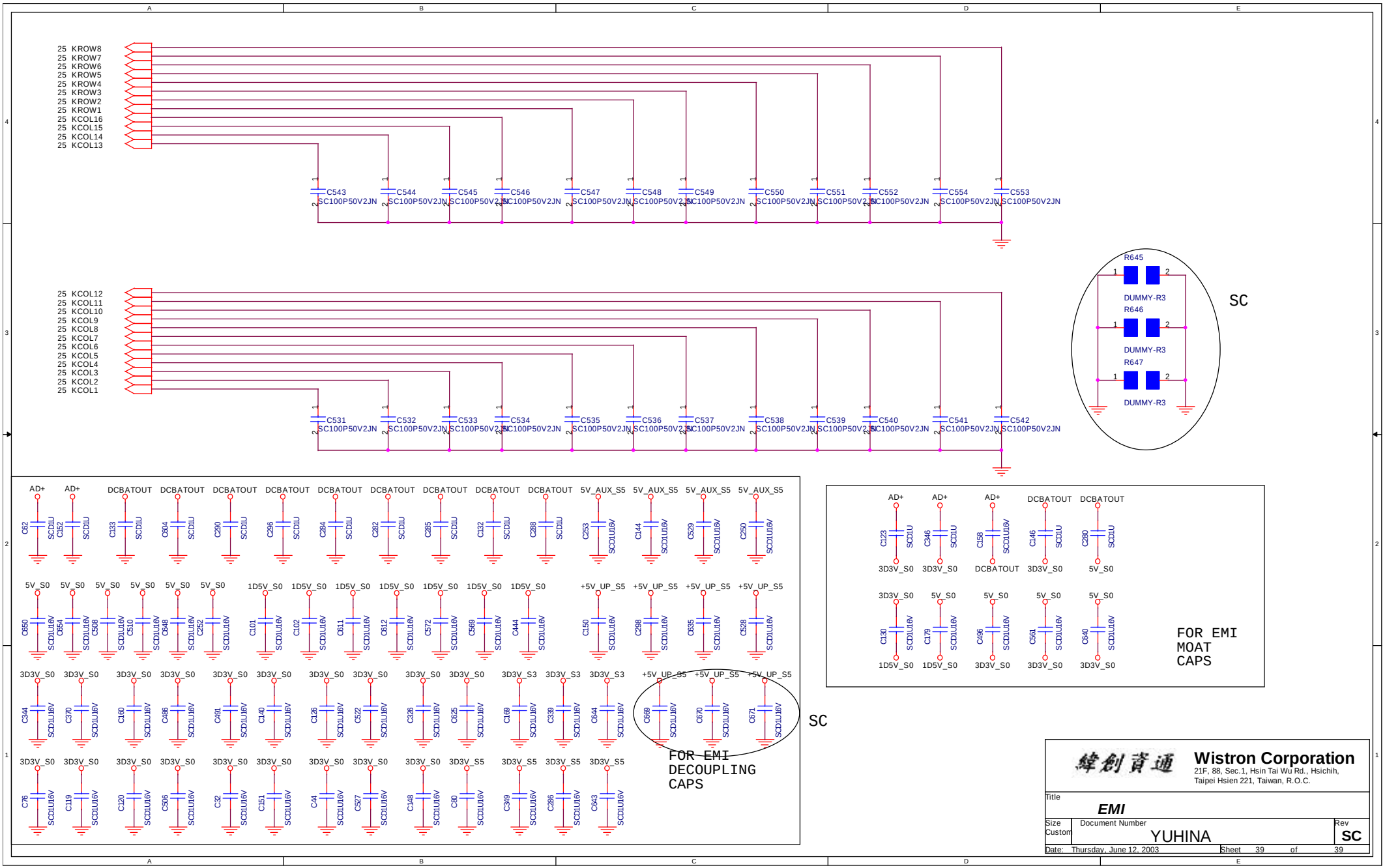
25 KROW8
25 KROW7
25 KROW6
25 KROW5
25 KROW4
25 KROW3
25 KROW2
25 KROW1
25 KCOL16
25 KCOL15
25 KCOL14
25 KCOL13
C543 SC100P50V2JN
C544 SC100P50V2JN
C545 SC100P50V2JN
C546 SC100P50V2JN
C547 SC100P50V2JN
C548 SC100P50V2JN
C549 SC100P50V2JN
C550 SC100P50V2JN
C551 SC100P50V2JN
C552 SC100P50V2JN
C554 SC100P50V2JN
C553 SC100P50V2JN
25 KCOL12
25 KCOL11
25 KCOL10
25 KCOL9
25 KCOL8
25 KCOL7
25 KCOL6
25 KCOL5
25 KCOL4
25 KCOL3
25 KCOL2
25 KCOL1
C531 SC100P50V2JN
C532 SC100P50V2JN
C533 SC100P50V2JN
C534 SC100P50V2JN
C535 SC100P50V2JN
C536 SC100P50V2JN
C537 SC100P50V2JN
C538 SC100P50V2JN
C539 SC100P50V2JN
C540 SC100P50V2JN
C541 SC100P50V2JN
C542 SC100P50V2JN
R645 DUMMY-R3
R646 DUMMY-R3
R647 DUMMY-R3
SC
AD+ AD+ DCBATOUT DCBATOUT DCBATOUT DCBATOUT DCBATOUT DCBATOUT DCBATOUT DCBATOUT DCBATOUT 5V_AUX_S5 5V_AUX_S5 5V_AUX_S5 5V_AUX_S5
C62 SCD1U C152 SCD1U C133 SCD1U C304 SCD1U C290 SCD1U C296 SCD1U C284 SCD1U C282 SCD1U C285 SCD1U C132 SCD1U C288 SCD1U C253 SCD1U16V C144 SCD1U16V C529 SCD1U16V C250 SCD1U16V
5V_S0 5V_S0 5V_S0 5V_S0 5V_S0 5V_S0 1D5V_S0 1D5V_S0 1D5V_S0 1D5V_S0 1D5V_S0 1D5V_S0 1D5V_S0 +5V_UP_S5 +5V_UP_S5 +5V_UP_S5 +5V_UP_S5
C650 SCD1U16V C654 SCD1U16V C508 SCD1U16V C510 SCD1U16V C648 SCD1U16V C252 SCD1U16V C101 SCD1U16V C102 SCD1U16V C611 SCD1U16V C612 SCD1U16V C572 SCD1U16V C569 SCD1U16V C444 SCD1U16V C150 SCD1U16V C298 SCD1U16V C635 SCD1U16V C528 SCD1U16V
3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S3 3D3V_S3 3D3V_S3 +5V_UP_S5 +5V_UP_S5 +5V_UP_S5
C344 SCD1U16V C370 SCD1U16V C100 SCD1U16V C486 SCD1U16V C491 SCD1U16V C140 SCD1U16V C126 SCD1U16V C522 SCD1U16V C326 SCD1U16V C625 SCD1U16V C169 SCD1U16V C339 SCD1U16V C644 SCD1U16V C669 SCD1U16V C670 SCD1U16V C671 SCD1U16V
3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S0 3D3V_S5 3D3V_S5 3D3V_S5
C76 SCD1U16V C119 SCD1U16V C120 SCD1U16V C506 SCD1U16V C32 SCD1U16V C151 SCD1U16V C44 SCD1U16V C527 SCD1U16V C148 SCD1U16V C90 SCD1U16V C349 SCD1U16V C286 SCD1U16V C643 SCD1U16V
FOR EMI DECOUPLING CAPS
SC
AD+ AD+ AD+ DCBATOUT DCBATOUT
C123 SCD1U 3D3V_S0
C346 SCD1U 3D3V_S0
C158 SCD1U16V DCBATOUT
C146 SCD1U 3D3V_S0
C290 SCD1U 5V_S0
3D3V_S0 5V_S0 5V_S0 5V_S0 5V_S0
C130 SCD1U16V 1D5V_S0
C179 SCD1U16V 1D5V_S0
C496 SCD1U16V 3D3V_S0
C561 SCD1U16V 3D3V_S0
C640 SCD1U16V 3D3V_S0
FOR EMI MOAT CAPS
Wistron Corporation
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