

Compal Confidential

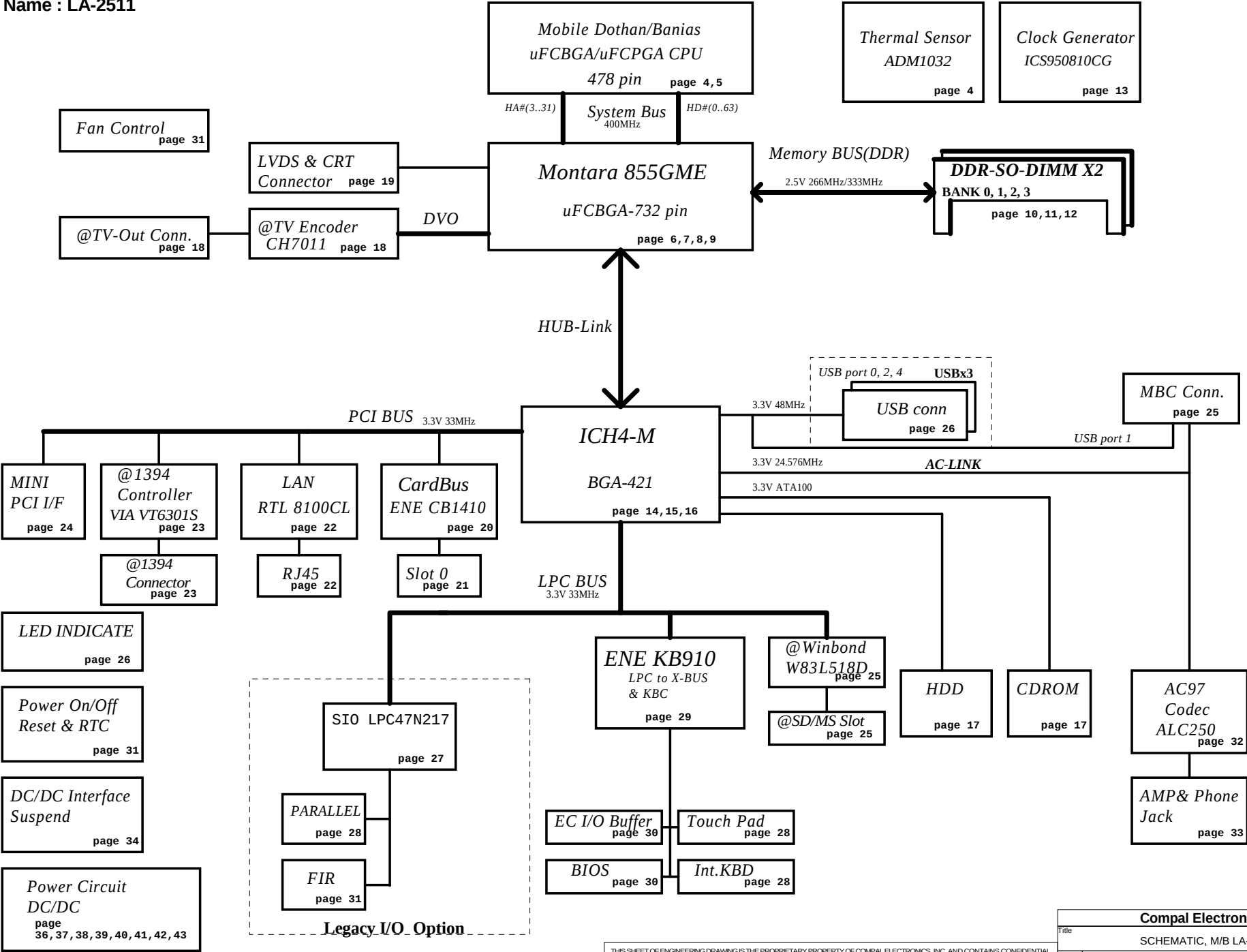
Schematics Document

Dothan/ Bantias uFCBGA/uFCPGA
Package
with Montara-GME Core Logic
REV: 0.1

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Title		
SCHEMATIC, M/B LA-2511		
Size	Document Number	Rev
	401313	A
Date:	~P期五, 九月 10, 2004	Sheet 1 of 45
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File Name : LA-2511



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Title			
SCHEMATIC, M/B LA-2511			
Size	Document Number	Rev	
	401313	A	
Date:	星期五, 九月 10, 2004	Sheet	2 of 45

Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2VS switched power rail for GMCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	1.5V power rail for GMCH	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
R368	100K +/- 5%			
Board ID	R361	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

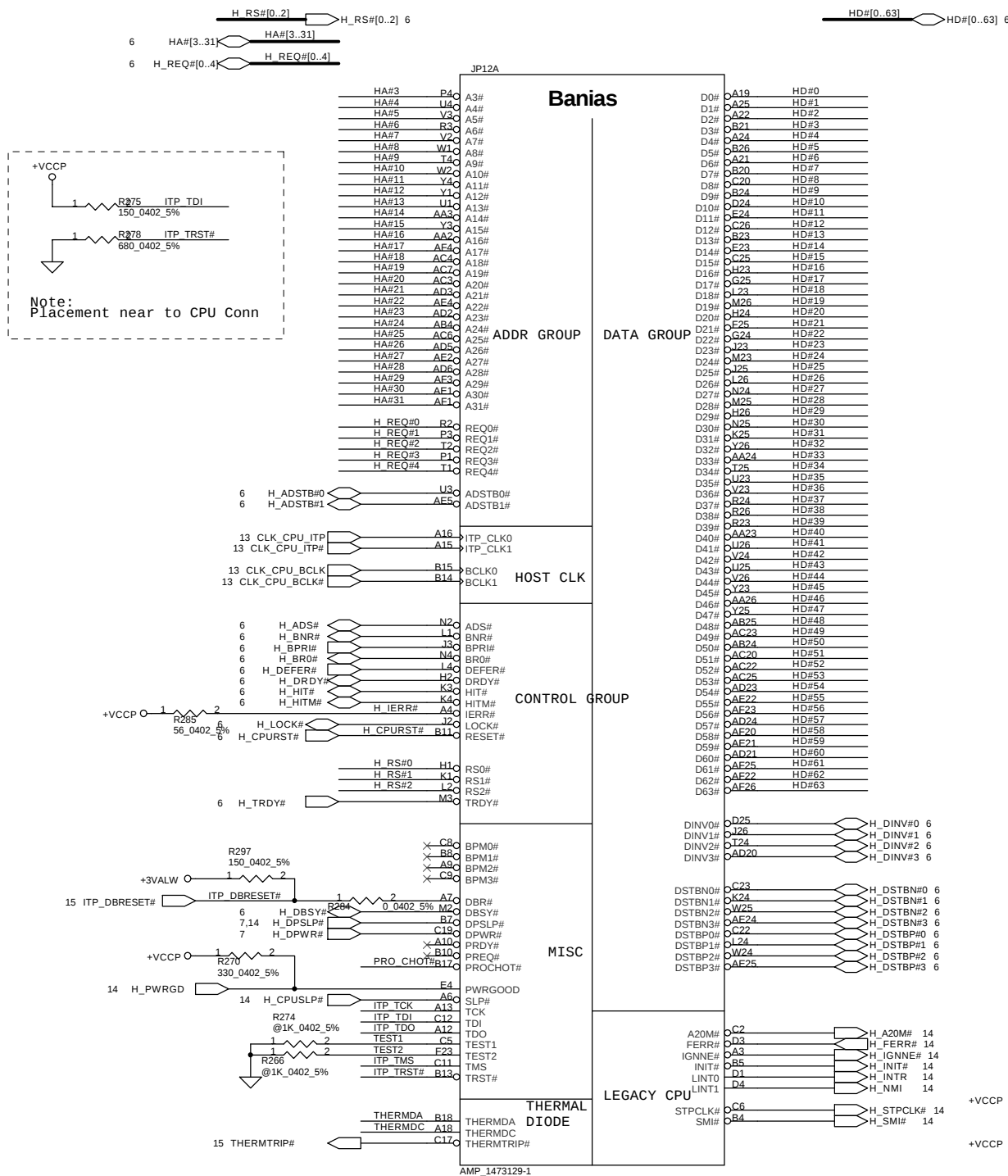
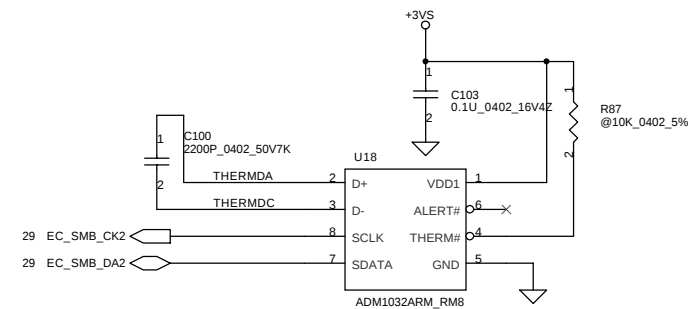
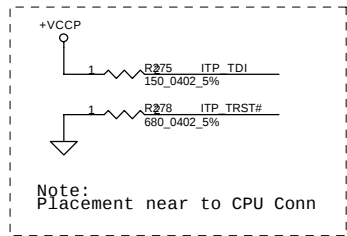
Board ID	PCB Revision
0	
1	0.1
2	0.2
3	1.0
4	
5	
6	
7	

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
CardBus	AD20	2	PIRQA
LAN	AD17	3	PIRQF
Mini-PCI	AD18/AD20	1/4	PIRQG/PIRQH
1394	AD16	0	PIRQE

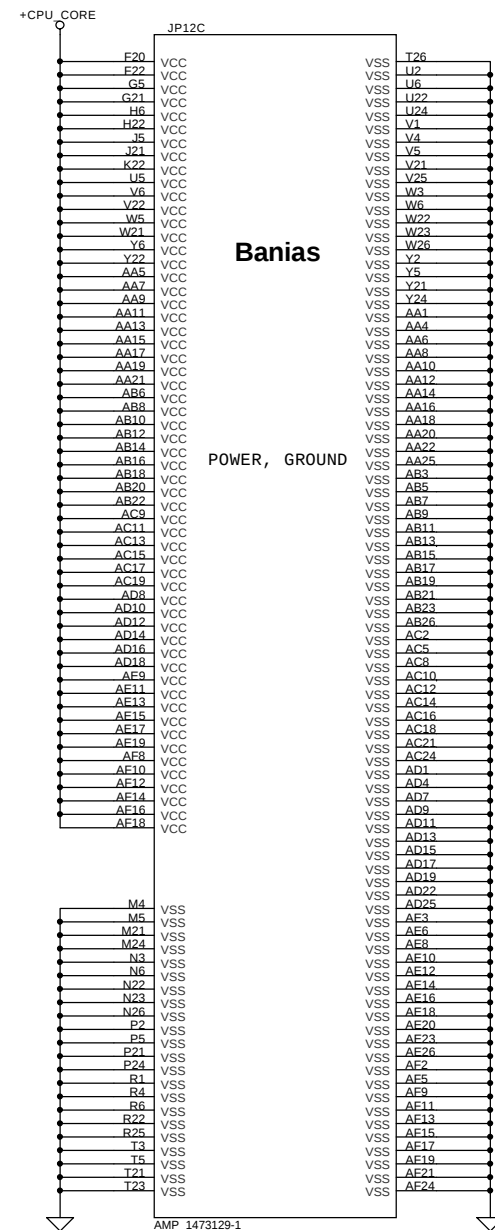
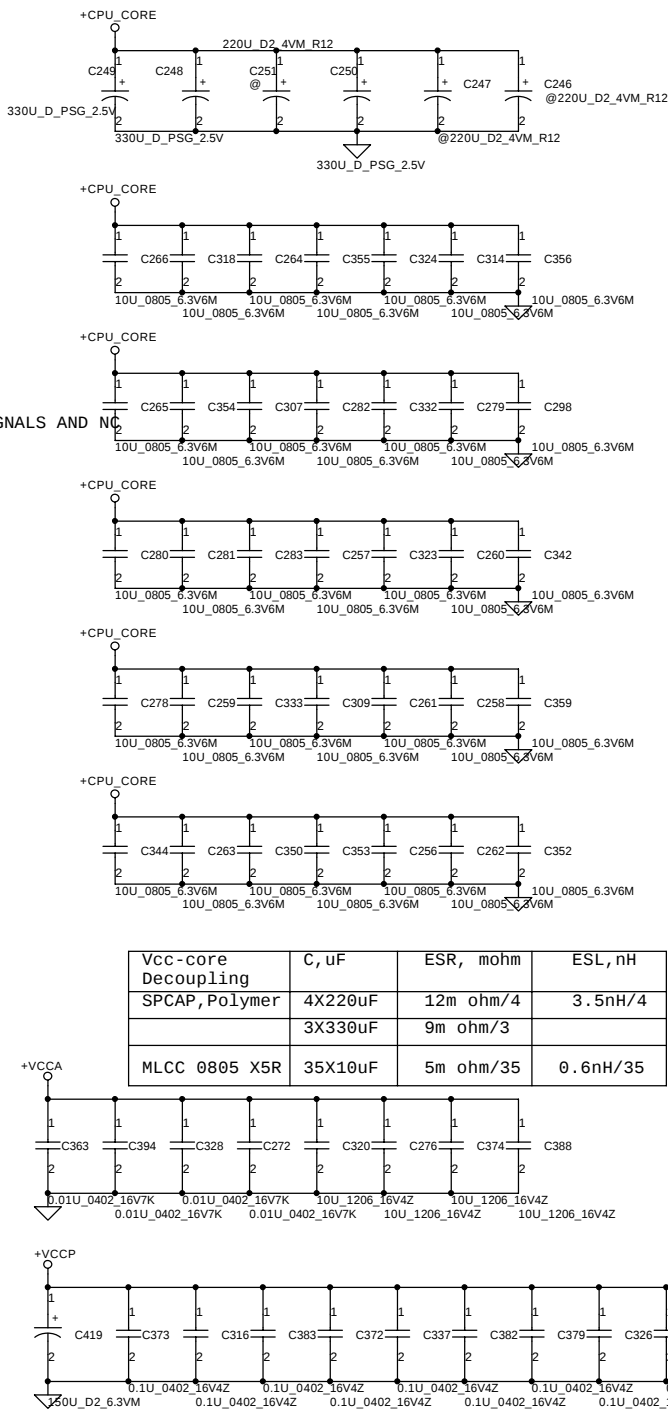
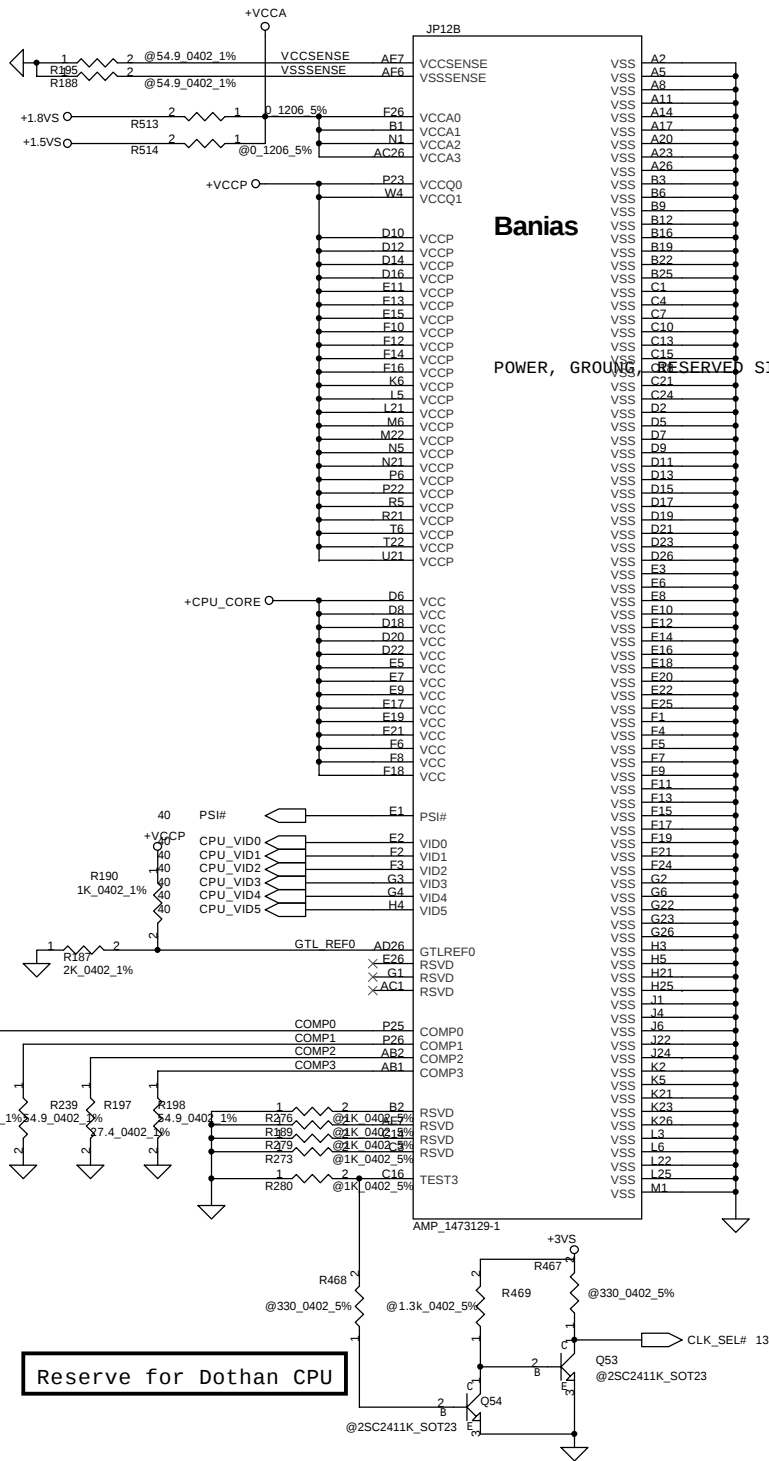
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Title		SCHEMATIC, M/B LA-2511	
Size B	Document Number	Rev A	
401313			
Date:	~P期五, 九月 10, 2004	Sheet 3	of 45



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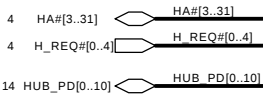
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Size	Document Number	Rev
A3	401313	A
Date:	~P版五, 九月 10, 2004	Sheet 4 of 45



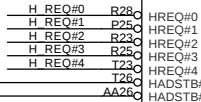
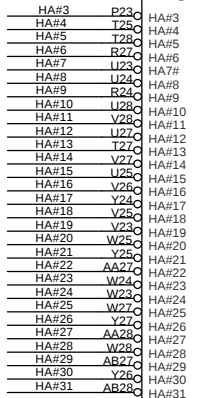
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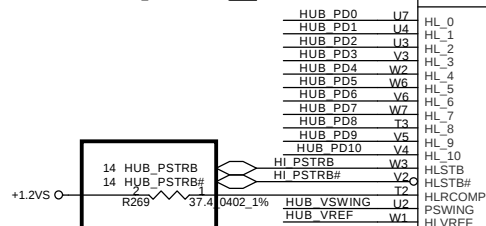
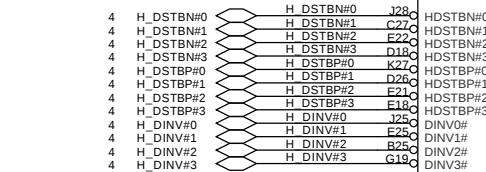
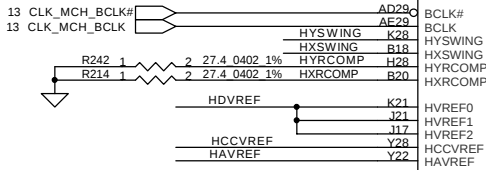
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Montara-GM(L)



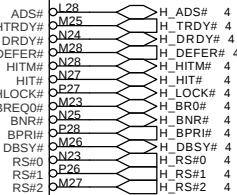
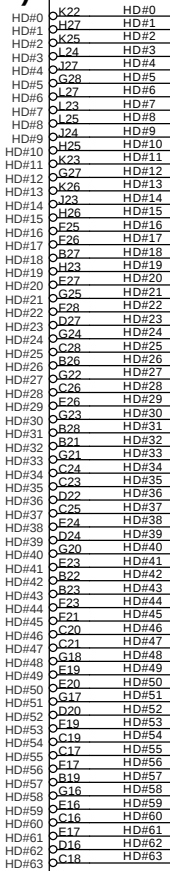
HOST



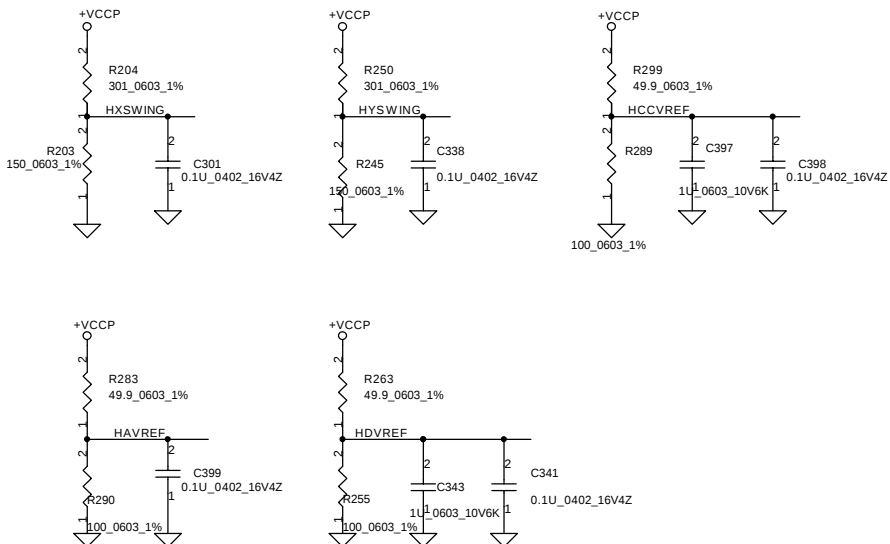
27.4 Ohm For GM
37.4 Ohm For GM+

RG82G4350M_uFCBGA732

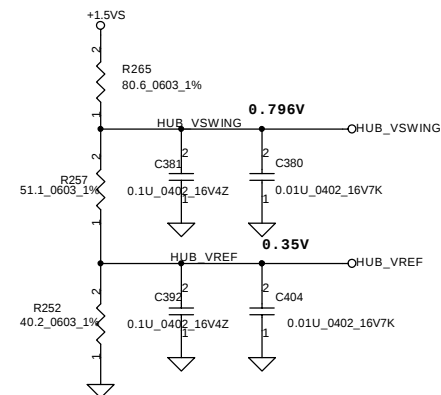
HUB I/F



HOST REF VOLTAGE



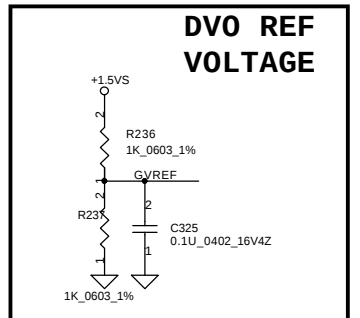
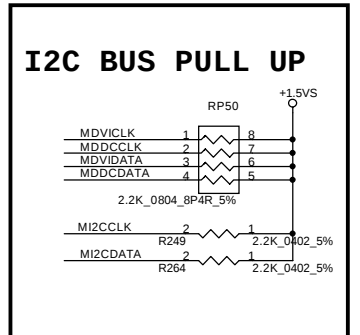
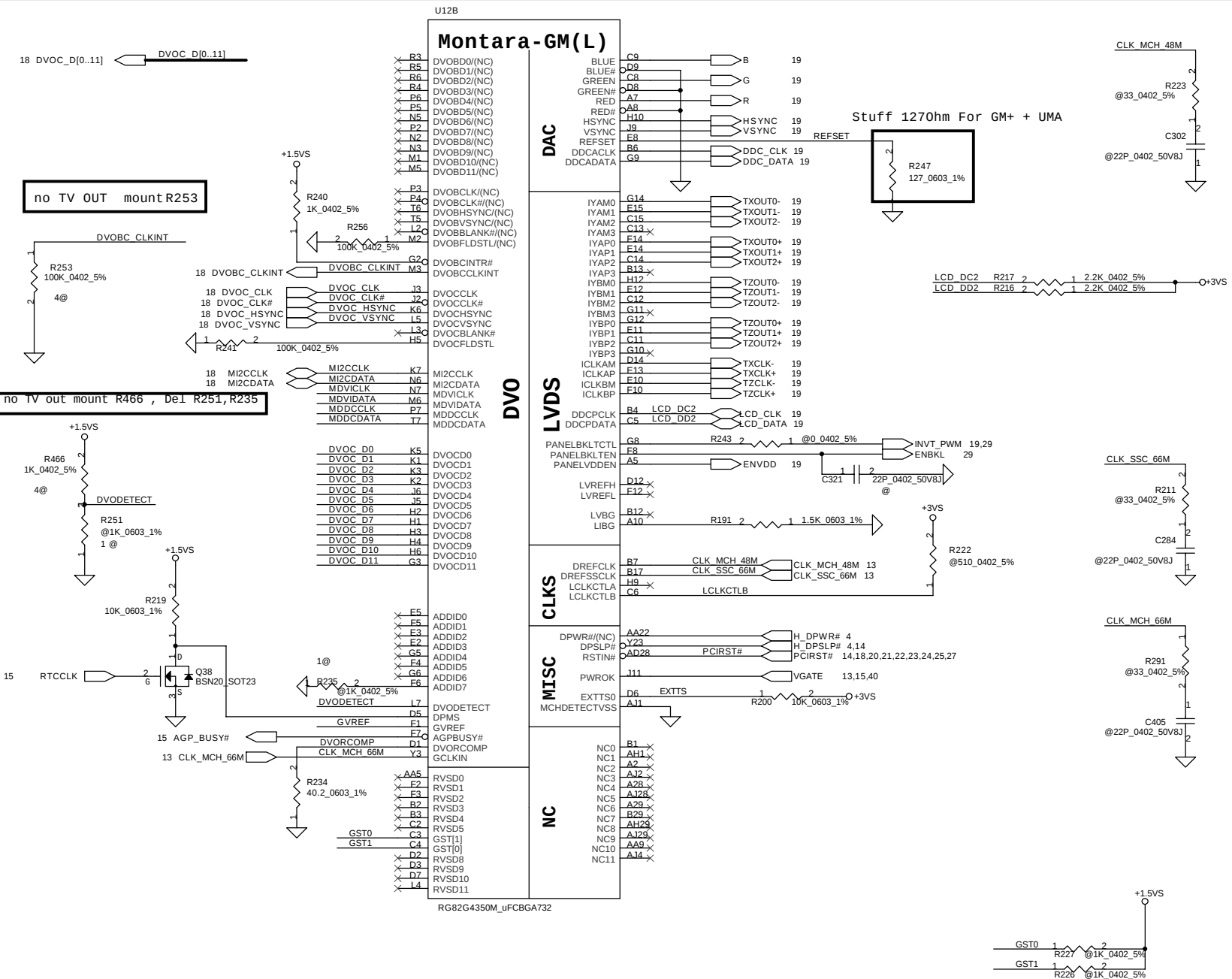
HUB I/F REF VOLTAGE



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		401313								A	
Date:		~P期五, 九月 10, 2004				Sheet		6		of 45	

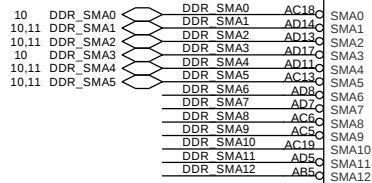
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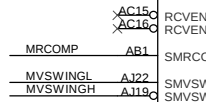
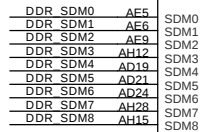
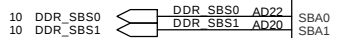
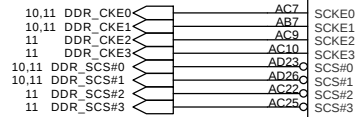
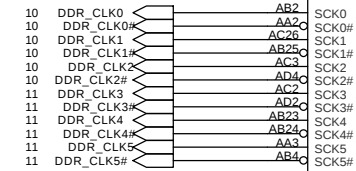
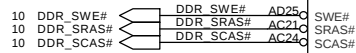
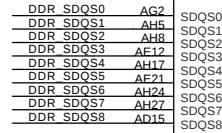
Starp pin list			
LCLKCTLB: High for P4 N.C. for Banias(default low) DVO DETECT: Low to enable DVO High to disable DVO			
GST0	GST1	PSB/Sys Mem/ GFX Core	
0	0	400/266/200 (default)	
0	1	400/200/200	
1	0	400/200/133	

U12C

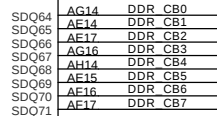
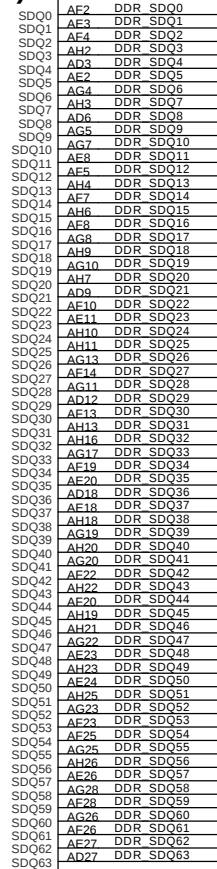
Montara-GM(L)



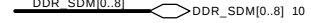
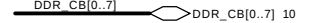
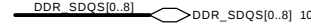
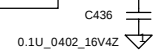
MEMORY



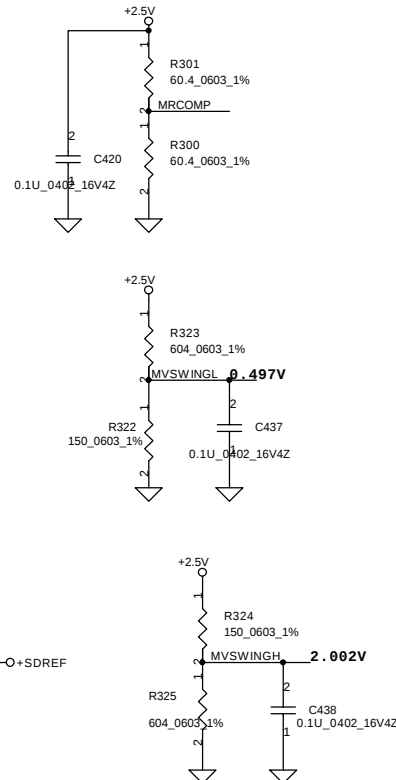
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SMVREF0 AJ24



DDR REF & SWING VOLTAGE



U12D

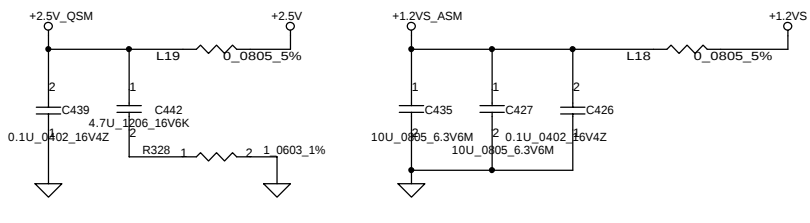
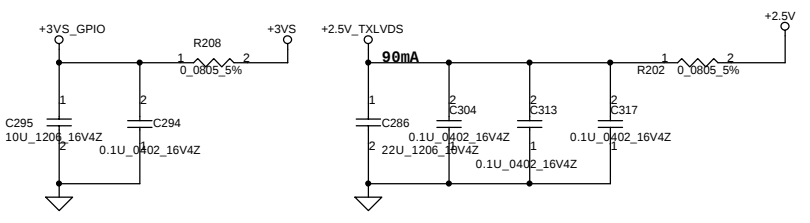
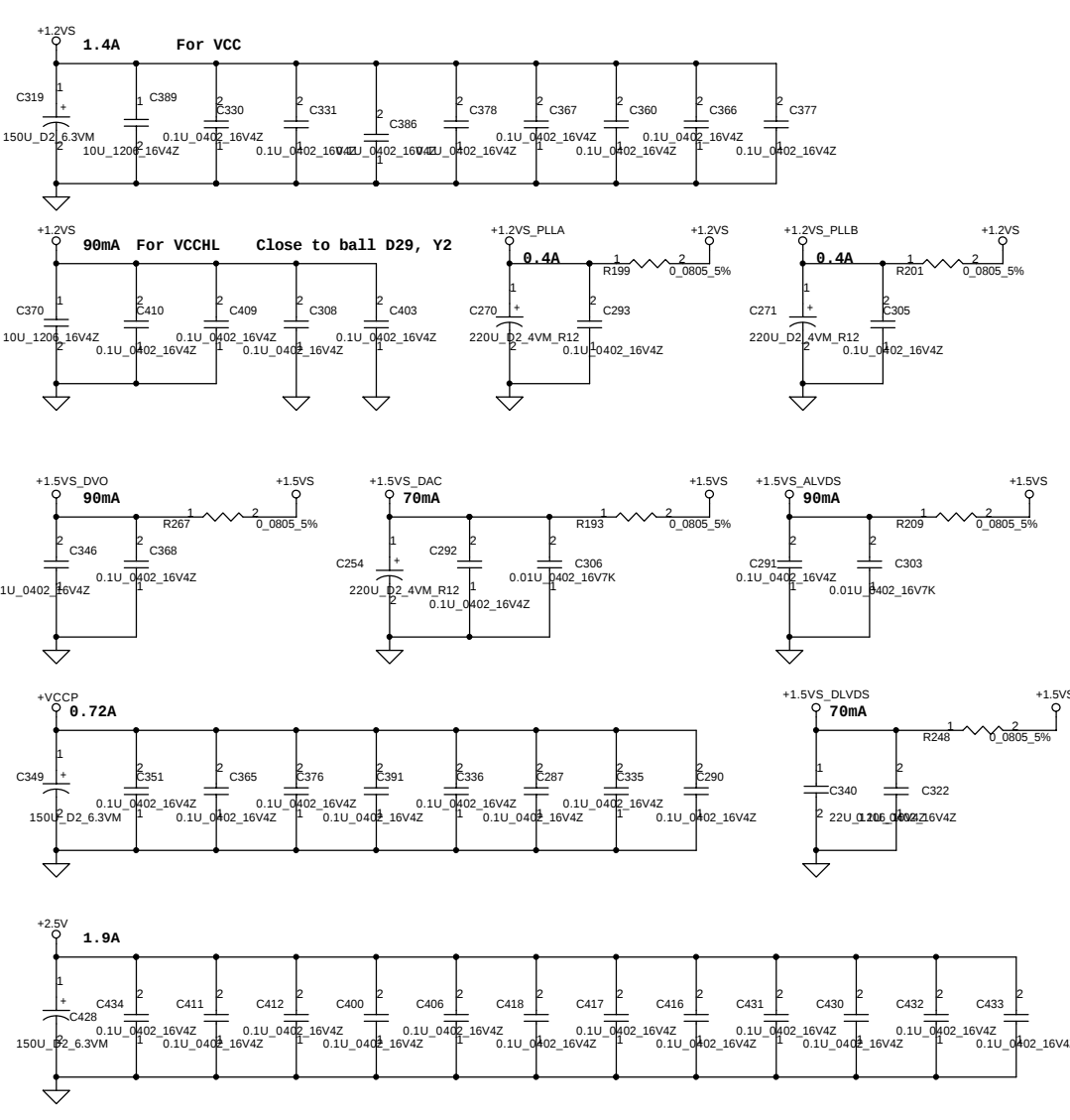
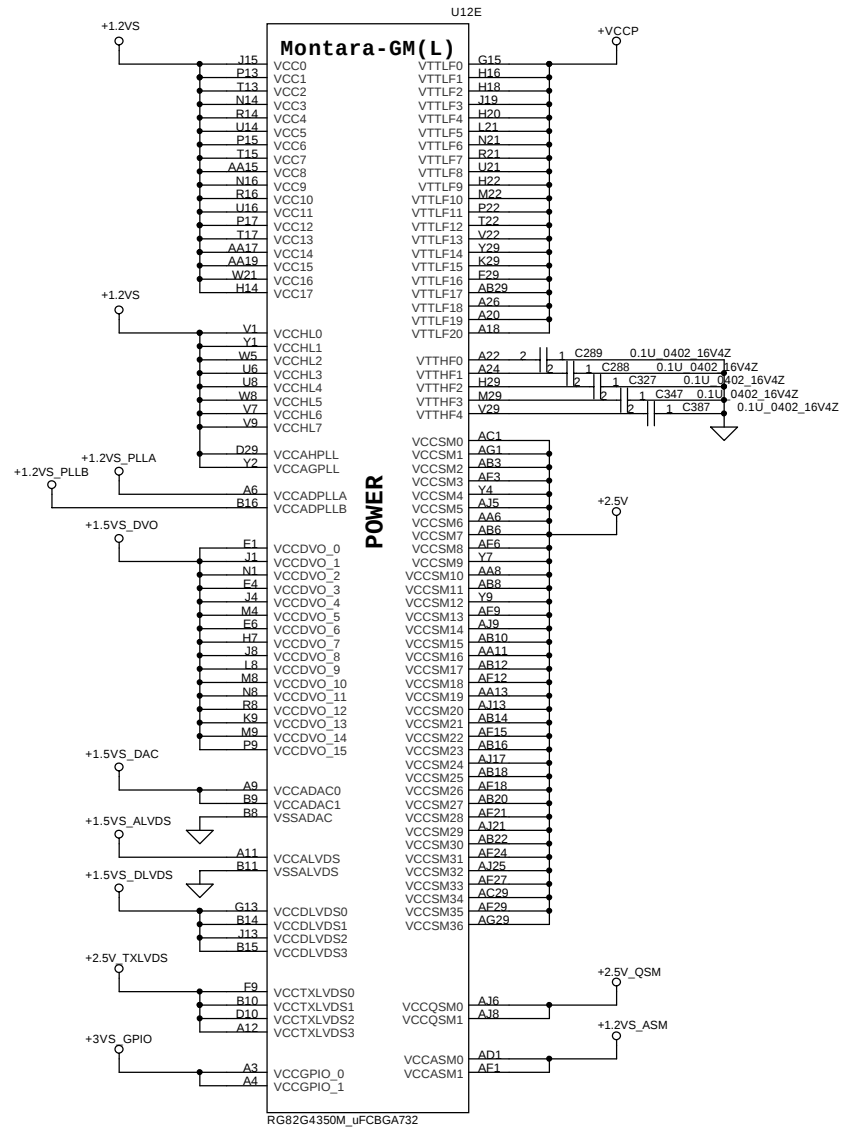


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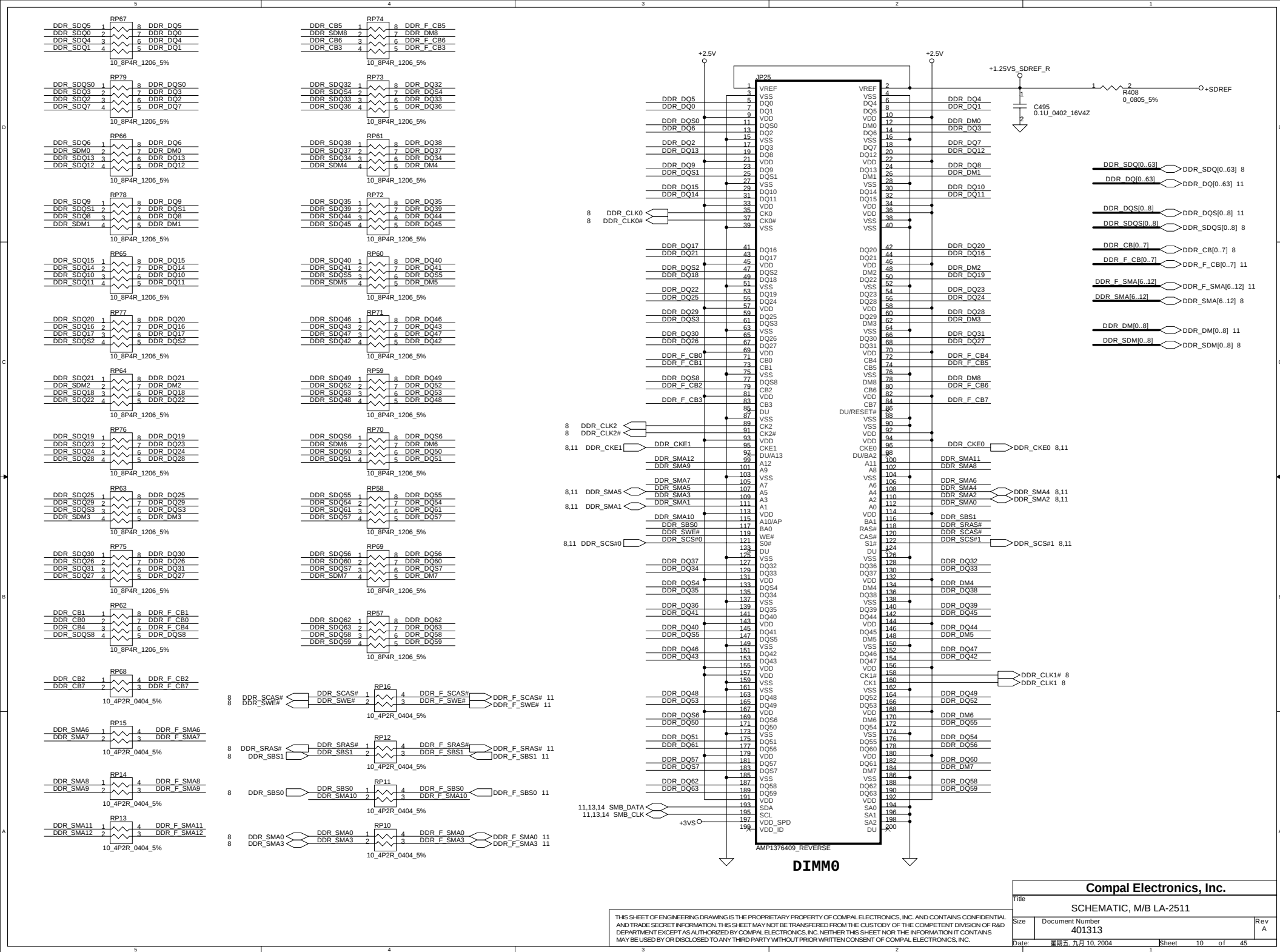
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	401313		A		
Date:	~P期五, 九月 10, 2004		Sheet	8	of 45

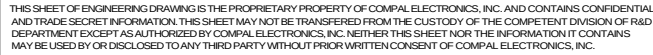
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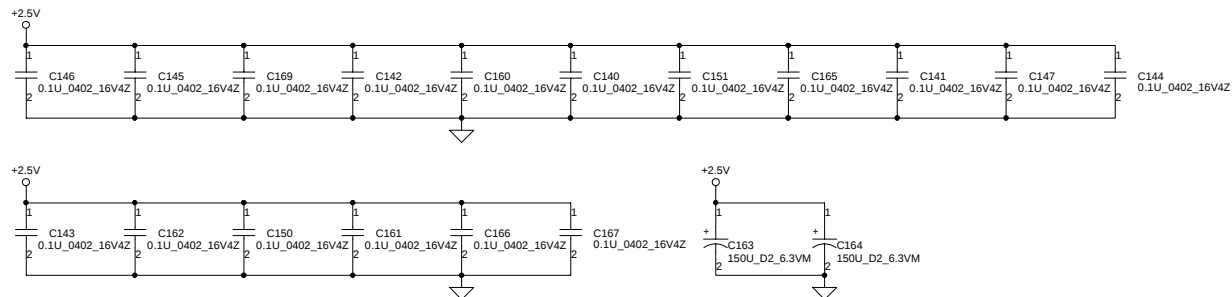
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Sheet		
9 of 45		
Rev		
A		

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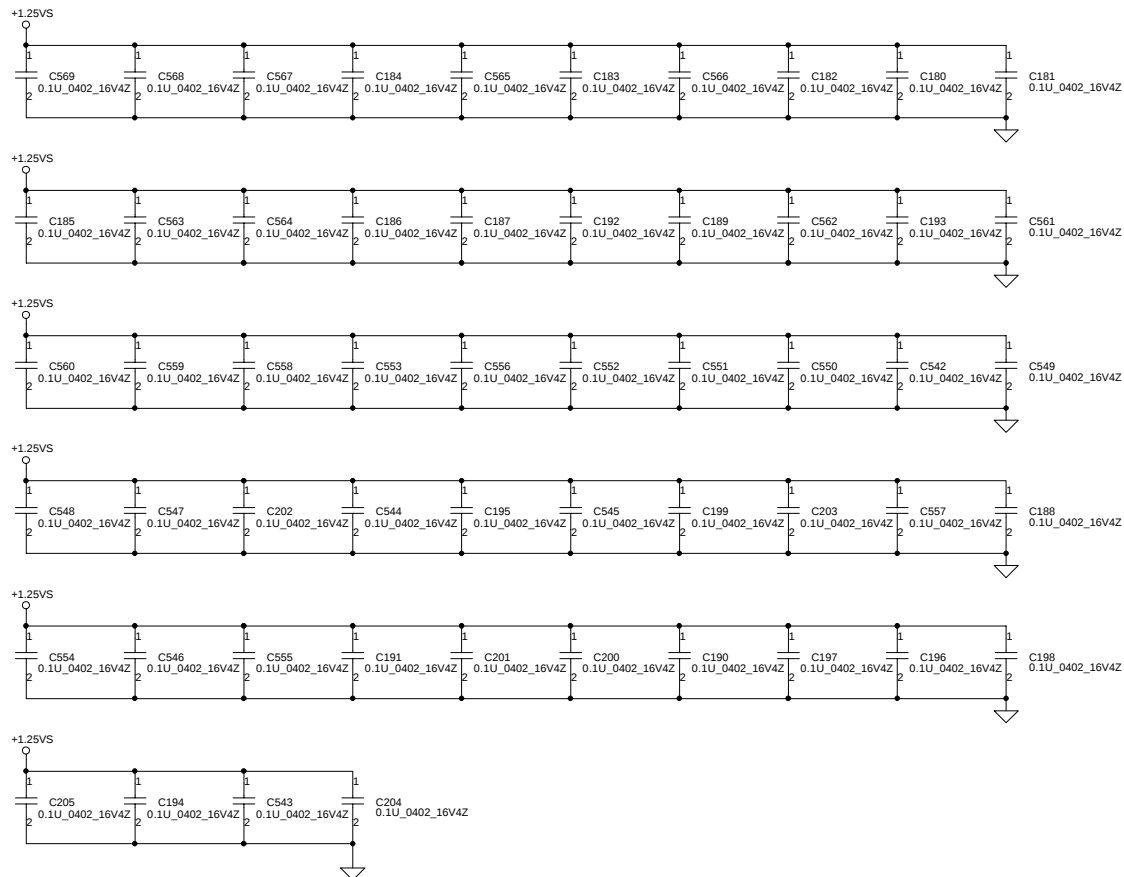




Layout note :
Distribute as close as possible
to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



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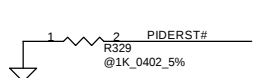
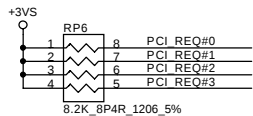
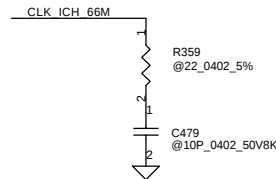
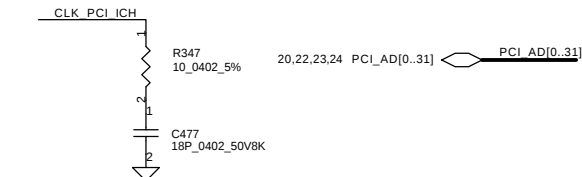
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Date:	星期五, 九月 10, 2004		Sheet 12 of 45

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

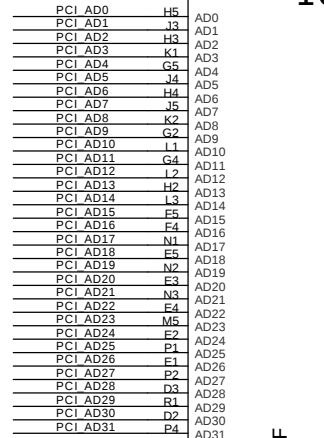
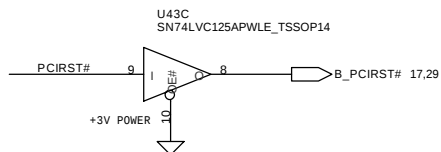
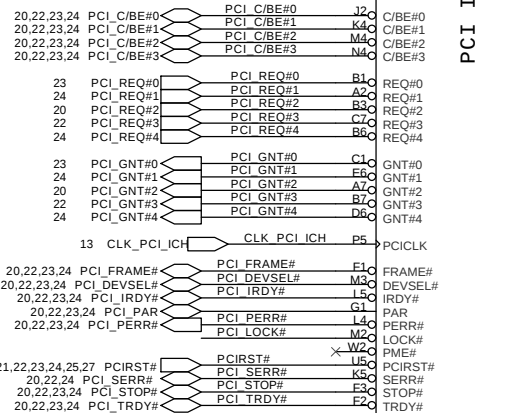
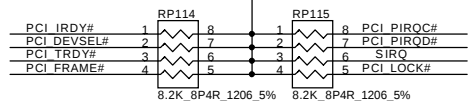
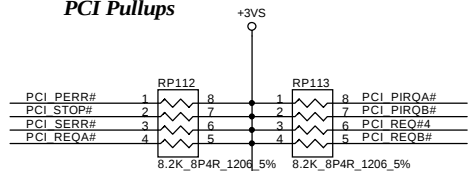
SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	66.67	66.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33



Compal Electronics, Inc.			
Title			
SCHEMATIC, M/B LA-2511			
Size B	Document Number 401313		Rev A
Date	星期五, 九月 10, 2004	Sheet	13 of 45

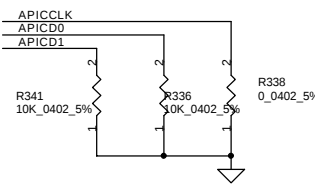
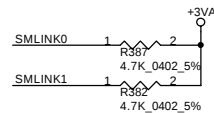
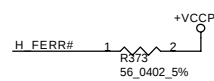
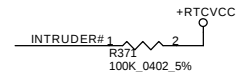
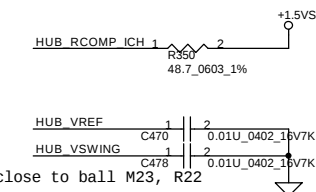
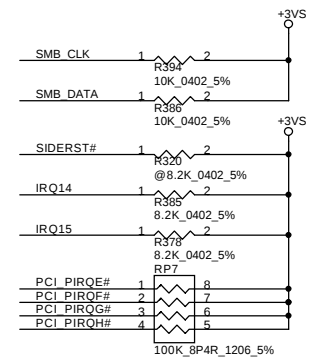
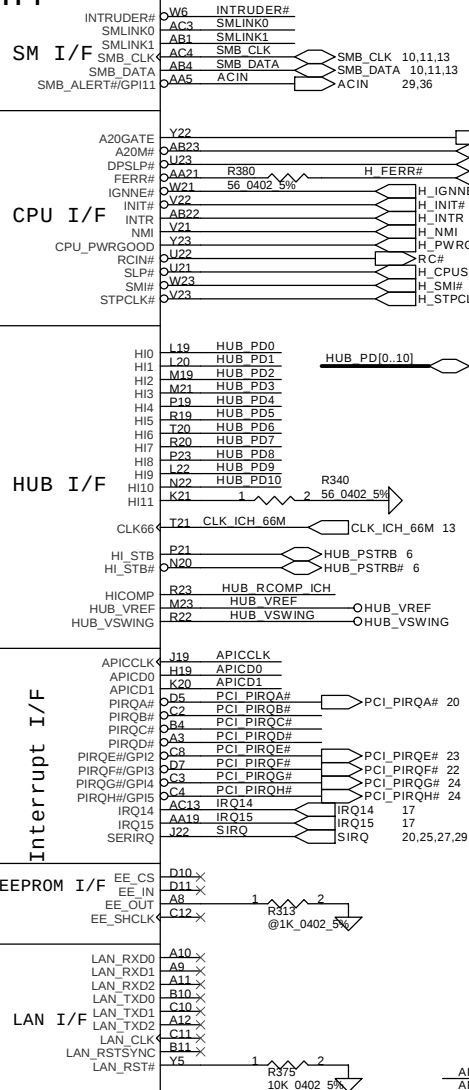


PCI Pullups



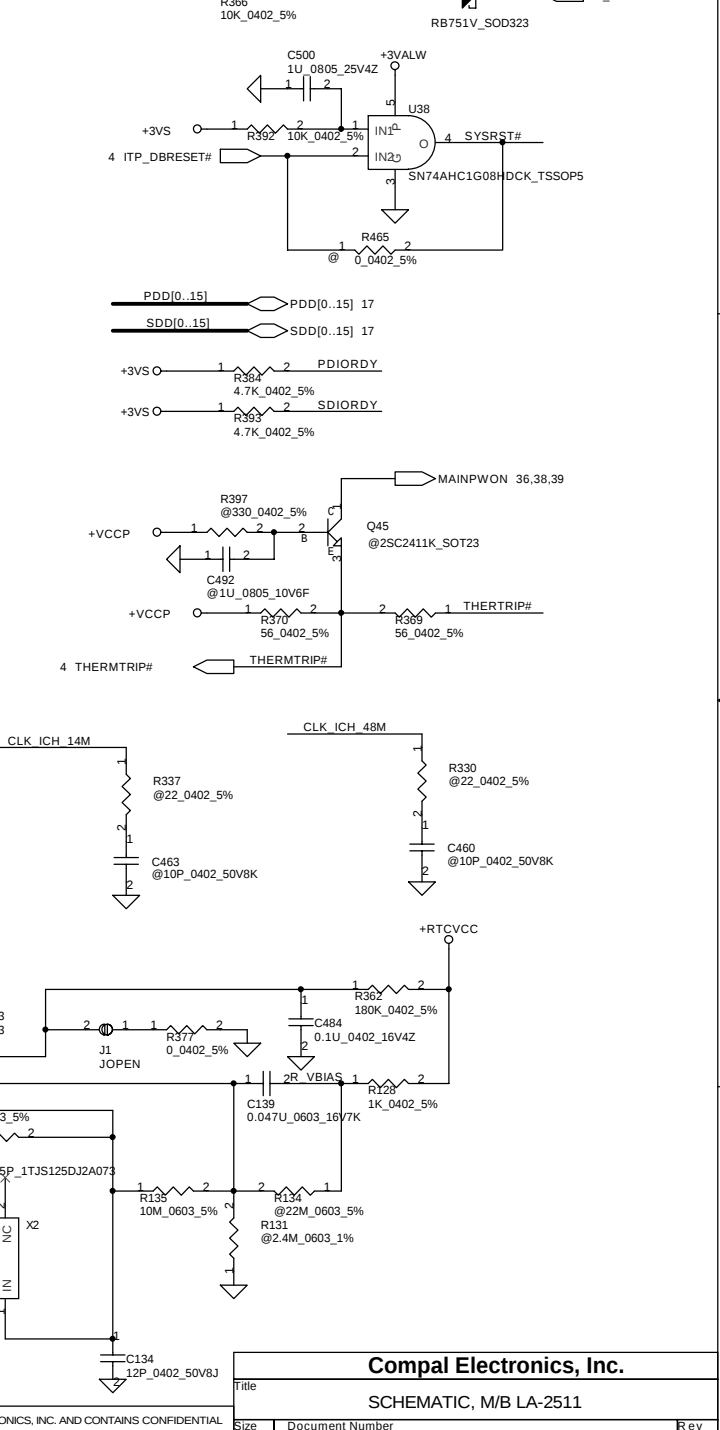
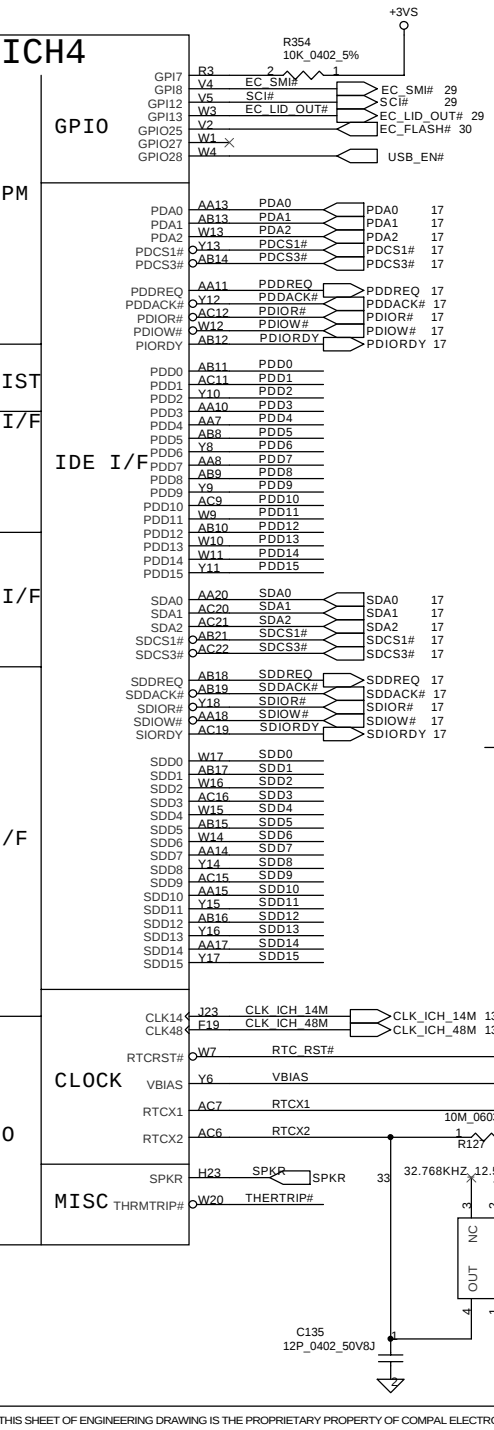
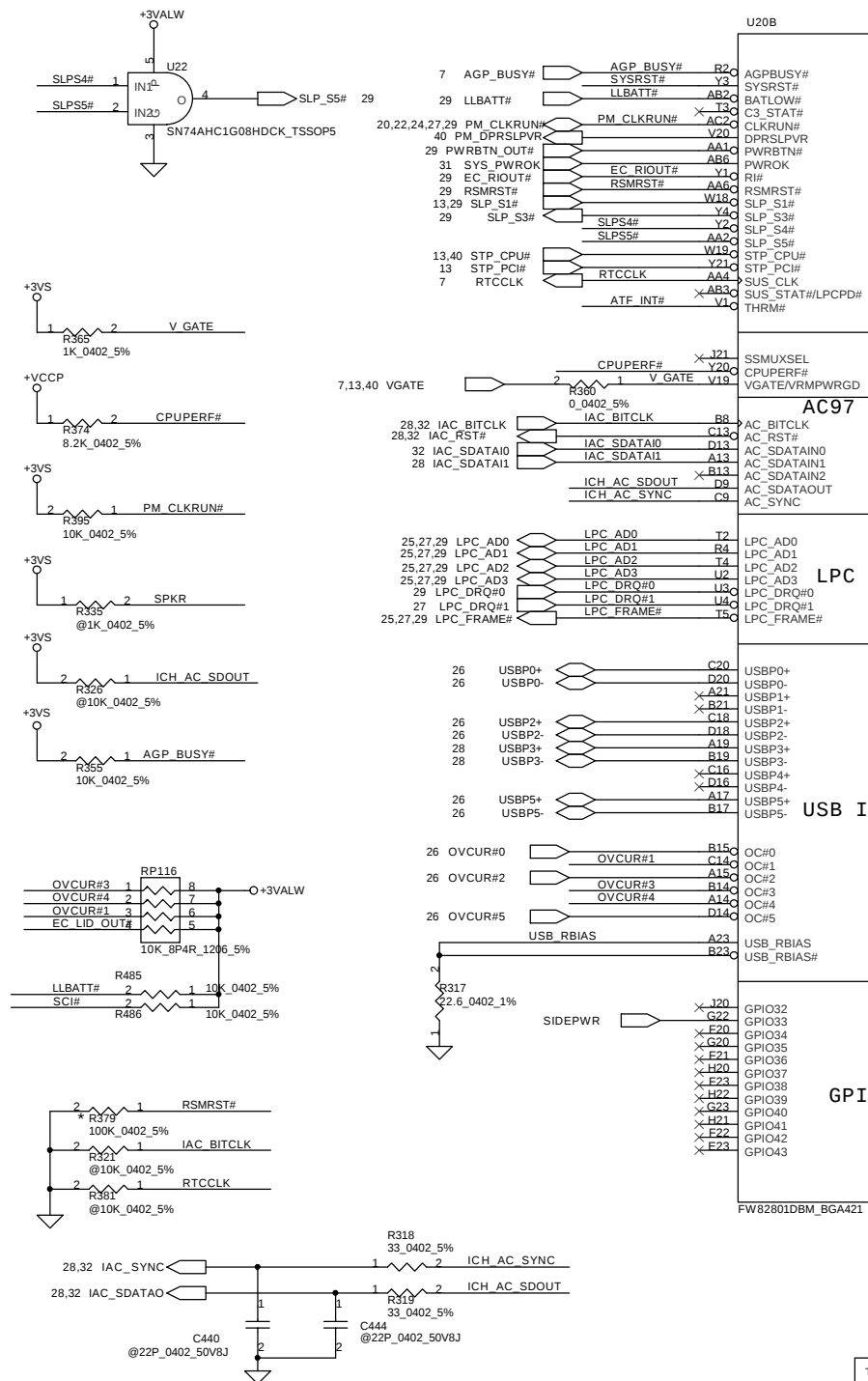
PCI I/F

ICH4



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Size	Document Number		Rev
	401313		A
Date:	~P 期五, 九月 10, 2004		Sheet 14 of 45



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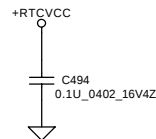
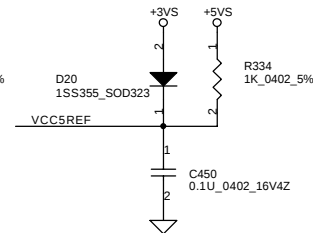
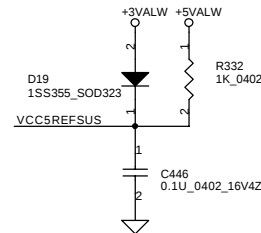
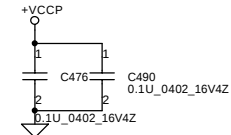
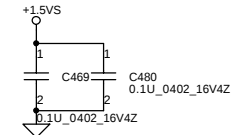
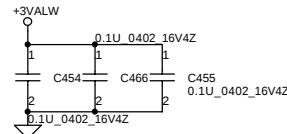
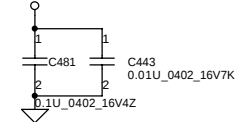
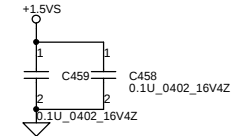
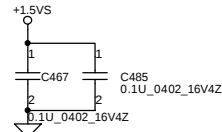
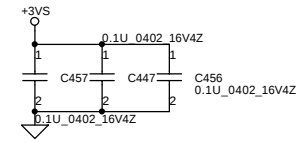
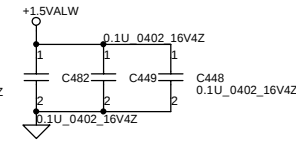
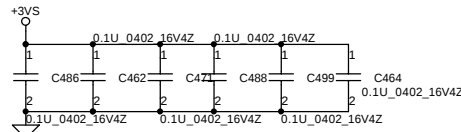
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Title			
SCHEMATIC, M/B LA-2511			
Size			
Document Number			
401313			
Rev			
A			
Date: ~P 周五, 九月 10, 2004			
Sheet 15 of 45			

U20C

ICH4

GND POWER

FW82801DBM_BGA421



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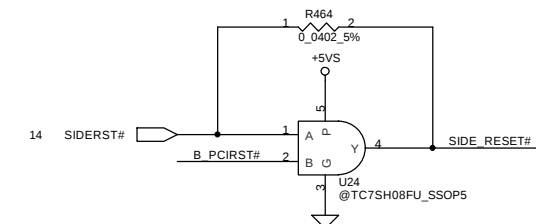
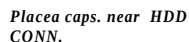
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Date: ~P期五, 九月 10, 2004

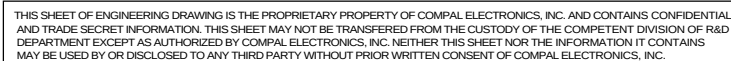
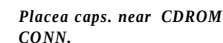
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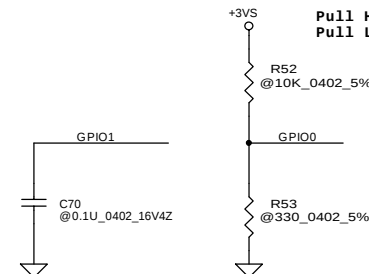
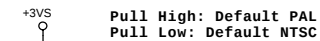
15 PDD[0..15] PDD[0..15]



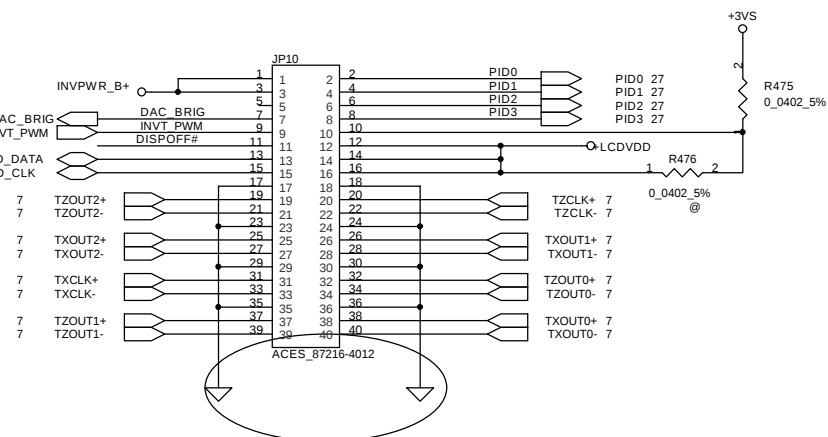
SDD[0..15] SDD[0..15] 15



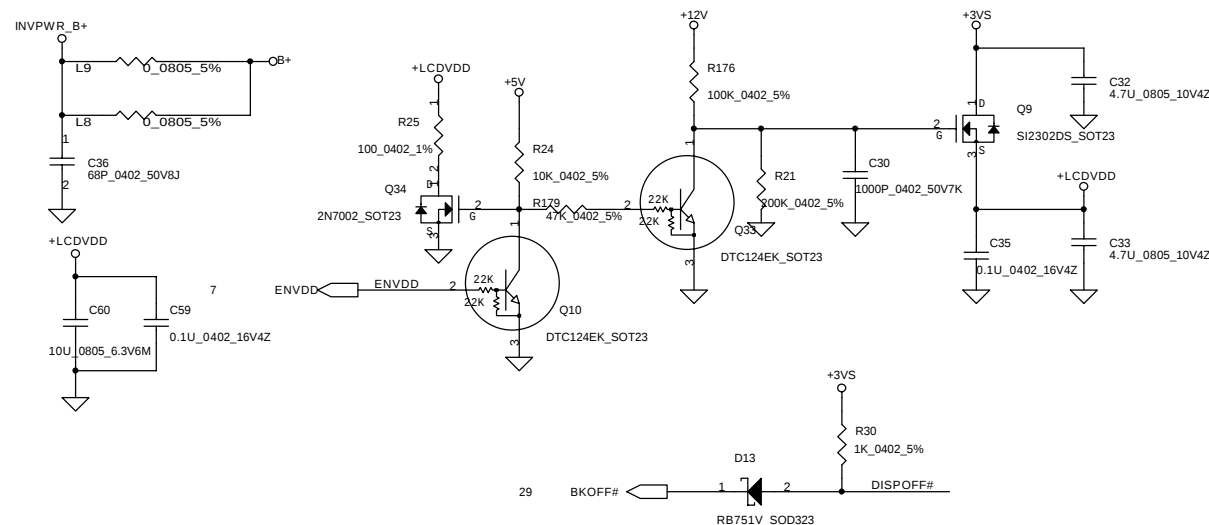
TV Encoder



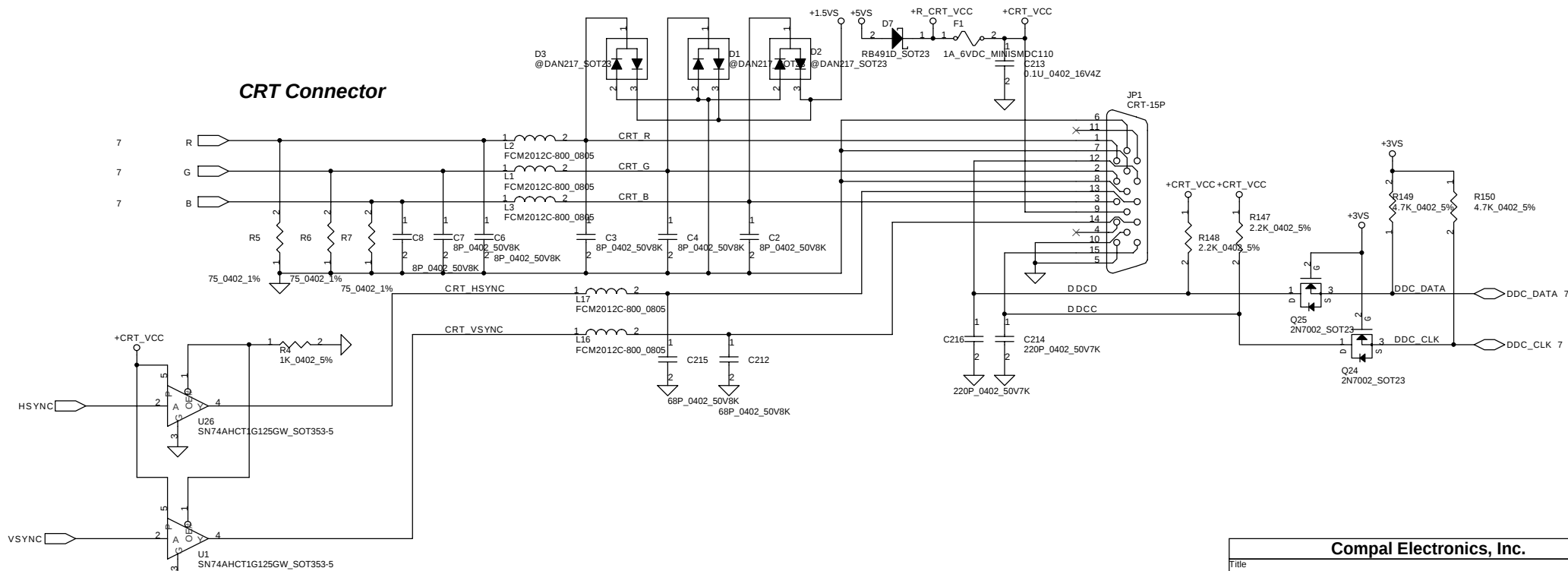
LVDS Connector



Change to Wire to board conn



CRT Connector



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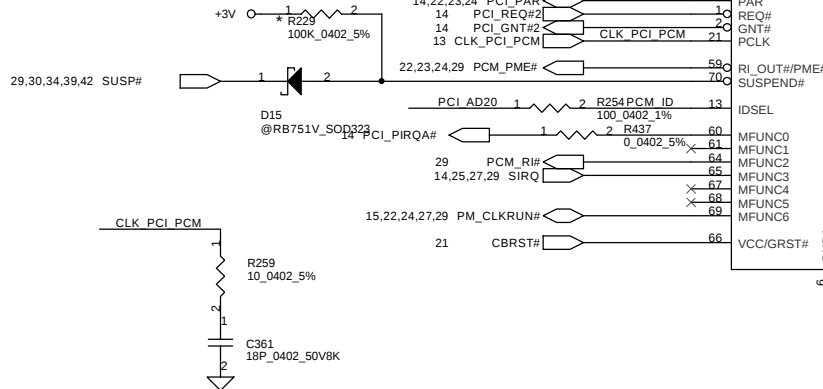
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Title			
SCHEMATIC, M/B LA-2511			
Size	Document Number		Rev
	401313		A
Date:	~P陽五, 九月 10, 2004		Sheet 19 of 45

14,22,23,24 PCI_AD[0..31] PCI_AD[0..31]

PCI_AD31	3	AD31
PCI_AD30	4	AD30
PCI_AD29	5	AD29
PCI_AD28	7	AD28
PCI_AD27	8	AD27
PCI_AD26	9	AD26
PCI_AD25	10	AD25
PCI_AD24	11	AD24
PCI_AD23	15	AD23
PCI_AD22	16	AD22
PCI_AD21	17	AD21
PCI_AD20	19	AD20
PCI_AD19	23	AD19
PCI_AD18	24	AD18
PCI_AD17	25	AD17
PCI_AD16	26	AD16
PCI_AD15	38	AD15
PCI_AD14	39	AD14
PCI_AD13	40	AD13
PCI_AD12	41	AD12
PCI_AD11	42	AD11
PCI_AD10	45	AD10
PCI_AD9	46	AD9
PCI_AD8	47	AD8
PCI_AD7	49	AD7
PCI_AD6	51	AD6
PCI_AD5	52	AD5
PCI_AD4	53	AD4
PCI_AD3	54	AD3
PCI_AD2	55	AD2
PCI_AD1	56	AD1
PCI_AD0	57	AD0

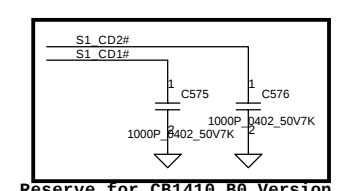
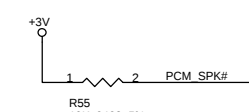
PQFP 144
22.2 X 22.2 X 1.60

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14,22,23,24 PCI_C/BE#2	27	C/BE#2
14,22,23,24 PCI_C/BE#1	37	C/BE#1
14,22,23,24 PCI_C/BE#0	48	C/BE#0
7,14,18,21,22,23,24,25,27 PCIRST#	20	RST#
14,22,23,24 PCI_FRAME#	28	FRAME#
14,22,23,24 PCI_IRDY#	29	IRDY#
14,22,23,24 PCI_TRDY#	31	TRDY#
14,22,23,24 PCI_DEVSEL#	32	DEVSEL#
14,22,23,24 PCI_STOP#	33	STOP#
14,22,23,24 PCI_PERR#	34	PERR#
14,22,24 PCI_SERR#	35	SERR#
14,22,23,24 PCI_PAR#	36	PAR#
14 PCI_REQ#2	1	REQ#
14 PCI_GNT#2	2	GNT#
13 CLK_PCI_PCM	21	CLK



CAD31/D10	144	S1_D10
CAD30/D9	142	S1_D9
CAD29/D1	141	S1_D1
CAD28/D8	140	S1_D8
CAD27/D0	139	S1_D0
CAD26/A0	129	S1_A0
CAD25/A1	128	S1_A1
CAD24/A2	127	S1_A2
CAD23/A3	124	S1_A3
CAD22/A4	121	S1_A4
CAD21/A5	120	S1_A5
CAD20/A6	118	S1_A6
CAD19/A25	116	S1_A25
CAD18/A7	115	S1_A7
CAD17/A24	113	S1_A24
CAD16/A17	98	S1_A17
CAD15/IOWR#	96	S1_IOWR#
CAD14/A9	97	S1_A9
CAD13/IORD#	93	S1_IORD#
CAD12/A11	95	S1_A11
CAD11/OE#	92	S1_OE#
CAD10/CE2#	91	S1_CE2#
CAD9/A10	89	S1_A10
CAD8/D15	87	S1_D15
CAD7/D7	85	S1_D7
CAD6/D13	82	S1_D13
CAD5/D6	83	S1_D6
CAD4/D12	80	S1_D12
CAD3/D5	81	S1_D5
CAD2/D11	77	S1_D11
CAD1/D4	79	S1_D4
CAD0/D3	76	S1_D3
CC/BE3#/REG#	125	S1_REG#
CC/BE2#/A12	112	S1_A12
CC/BE1#/A8	99	S1_A8
CC/BE0#/CE1#	88	S1_CE1#
CRST#/RESET	119	S1_RST
CFRAME#/A23	111	S1_A23
CIRDY#/A15	109	S1_A15
CTRDRY#/A22	107	S1_A22
CDEVSEL#/A21	105	S1_A21
CSTOP#/A20	104	S1_A20
CPERR#/A14	103	S1_A14
CSERR#/WAIT#	133	S1_WAIT#
CPAR/A13	101	S1_A13
CREQ#/INPACK#	123	S1_INPACK#
CGNT#/WE#	106	S1_WE#
CLK/A16	108	A16_CLK
CSTSCHG/BVD1	135	S1_BVD1
CLKRUN#/WP	136	S1_WP
CBLOCK#/A19	103	S1_A19
CINT#/READY	132	S1_RDY#
SPKOUT	62	PCM_SPK#
CAUDIO/BVD2	134	S1_BVD2
CCD2#/CD2#	137	S1_CD2#
CCD1#/CD1#	125	S1_CD1#
CVS2/VS2#	117	S1_VS2
CVS1/VS1#	131	S1_VS1

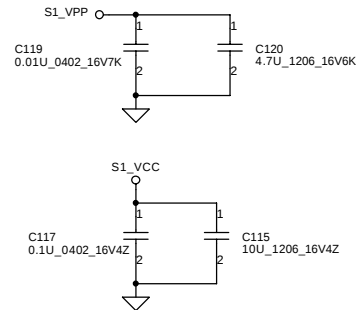
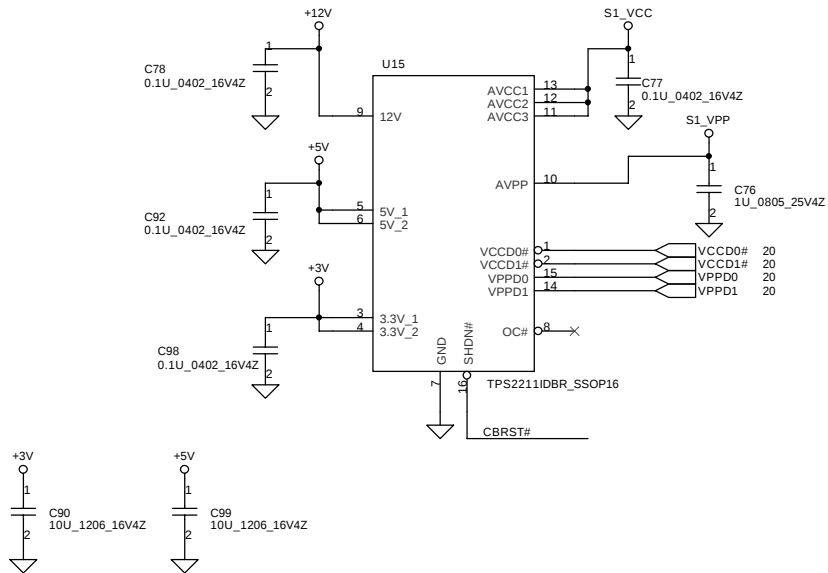
S1_A[0..25] S1_A[0..25] 21
S1_D[0..15] S1_D[0..15] 21



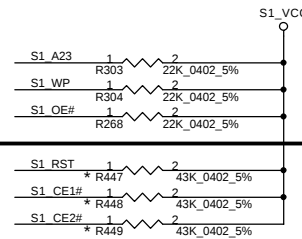
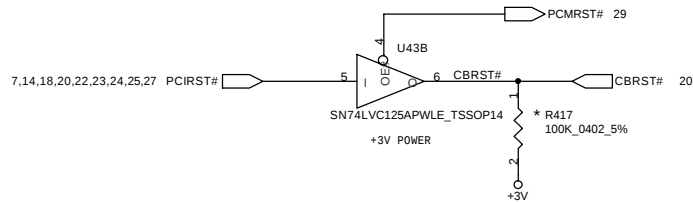
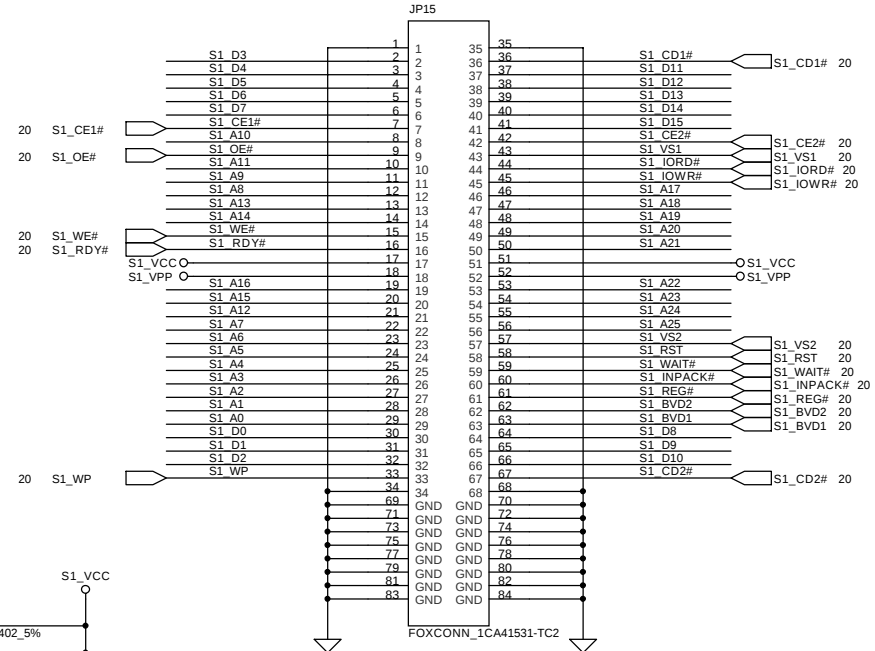
Reserve for CB1410 B0 Version

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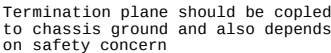
PCMCIA Power Controller

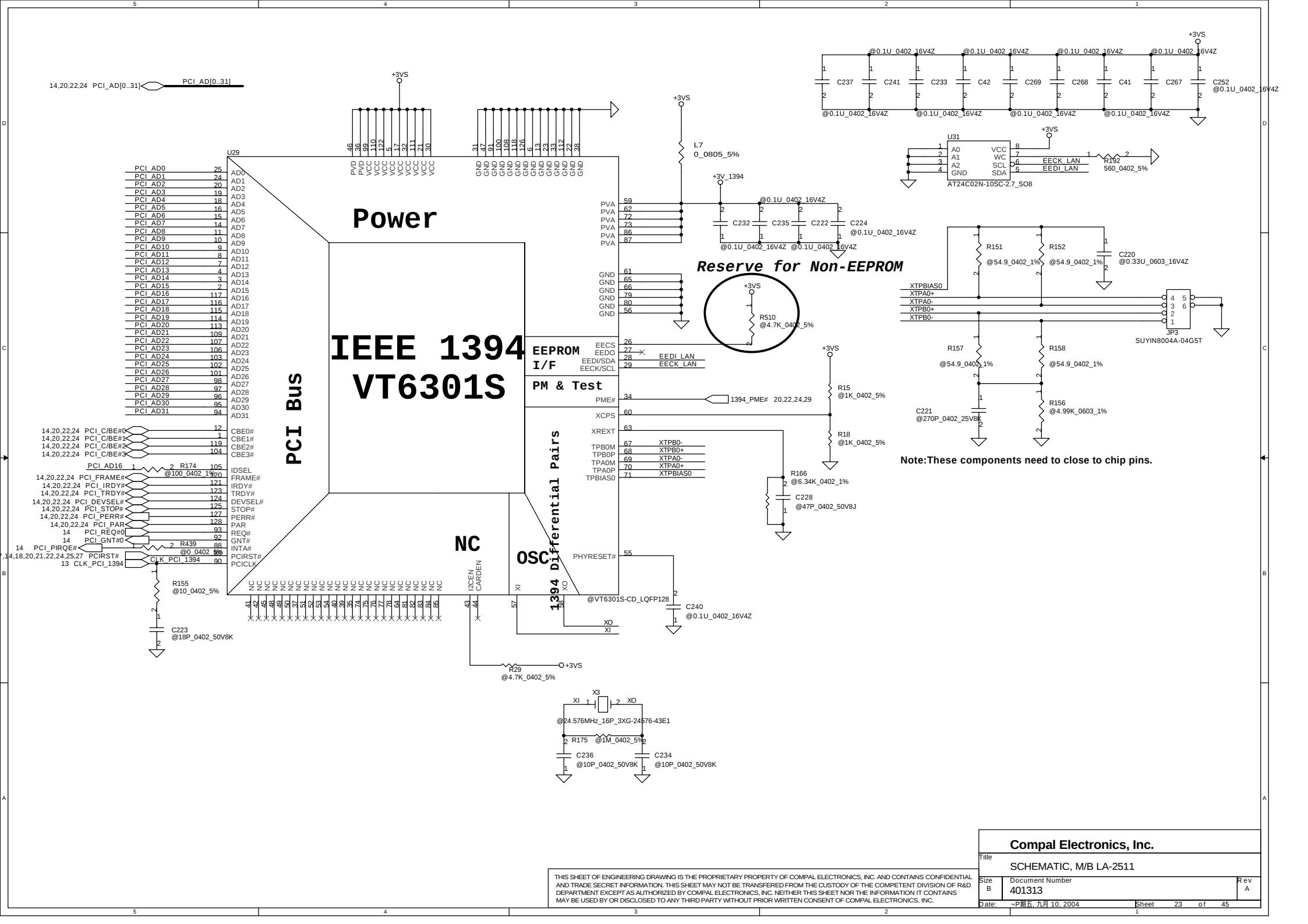


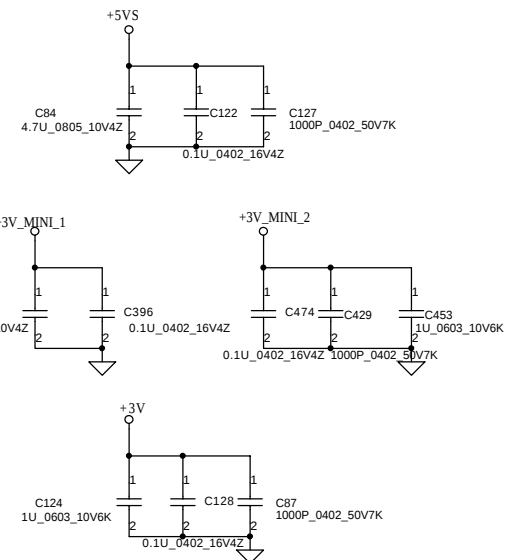
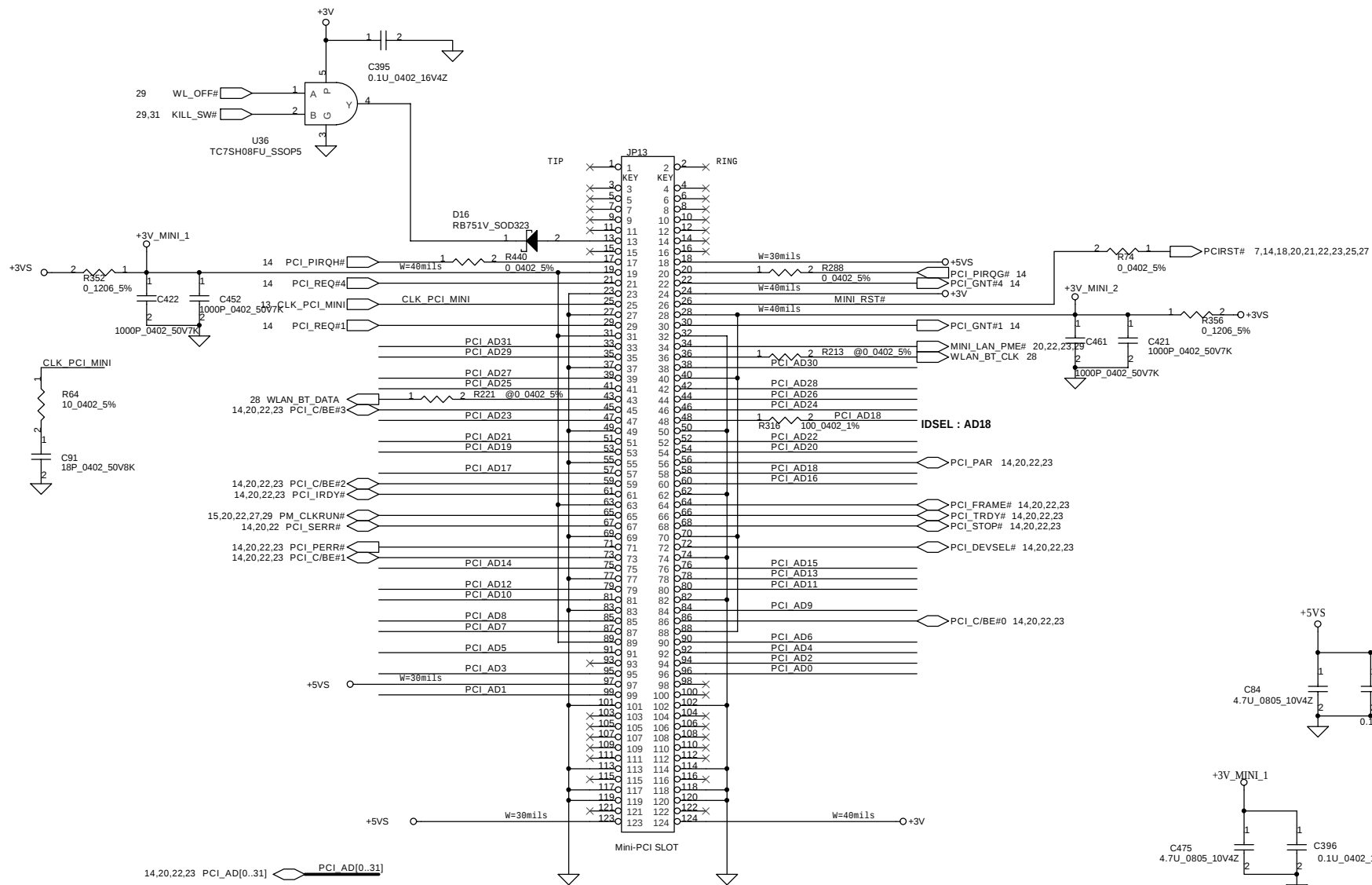
CardBus Socket



Reserve for CB1410 B0 Version





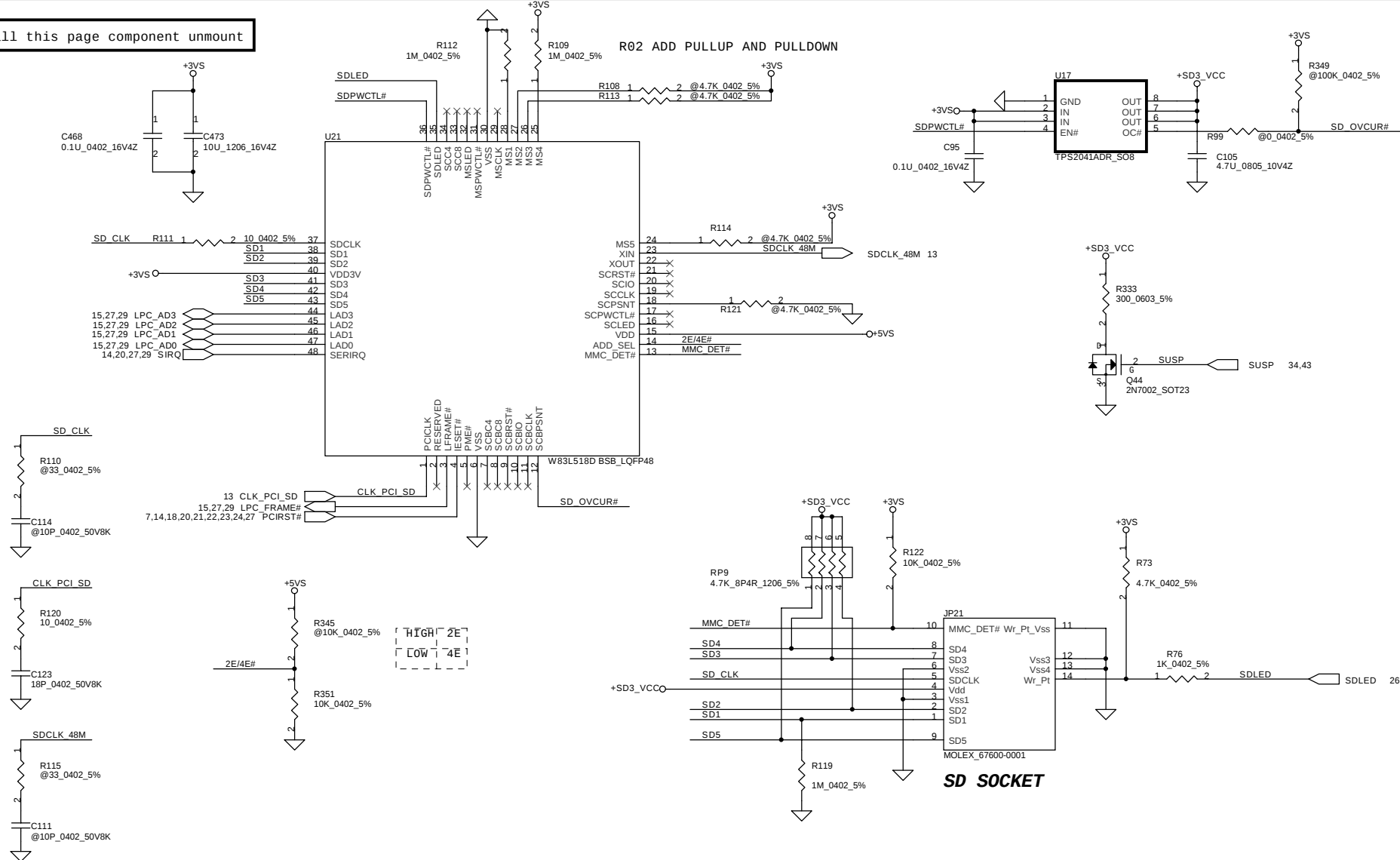


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Title		SCHEMATIC, M/B LA-2511	
Size	Document Number	Rev	
B	401313	A	
Date:	~P期五, 九月 10, 2004	Sheet	24 of 45

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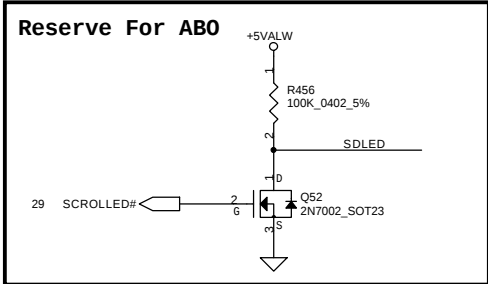
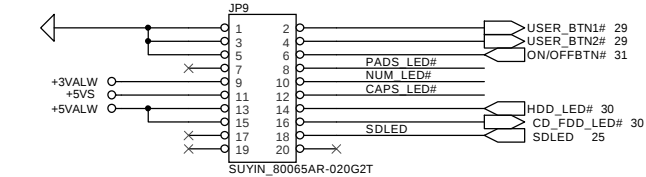
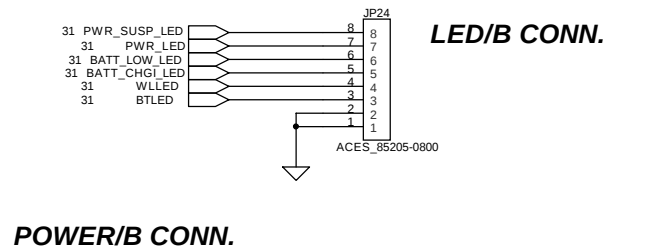
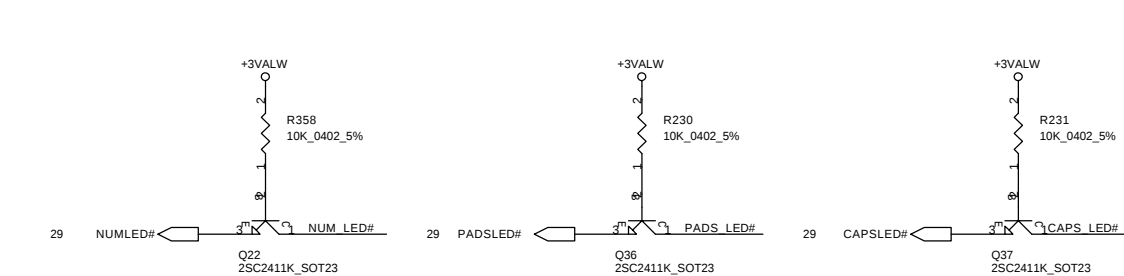
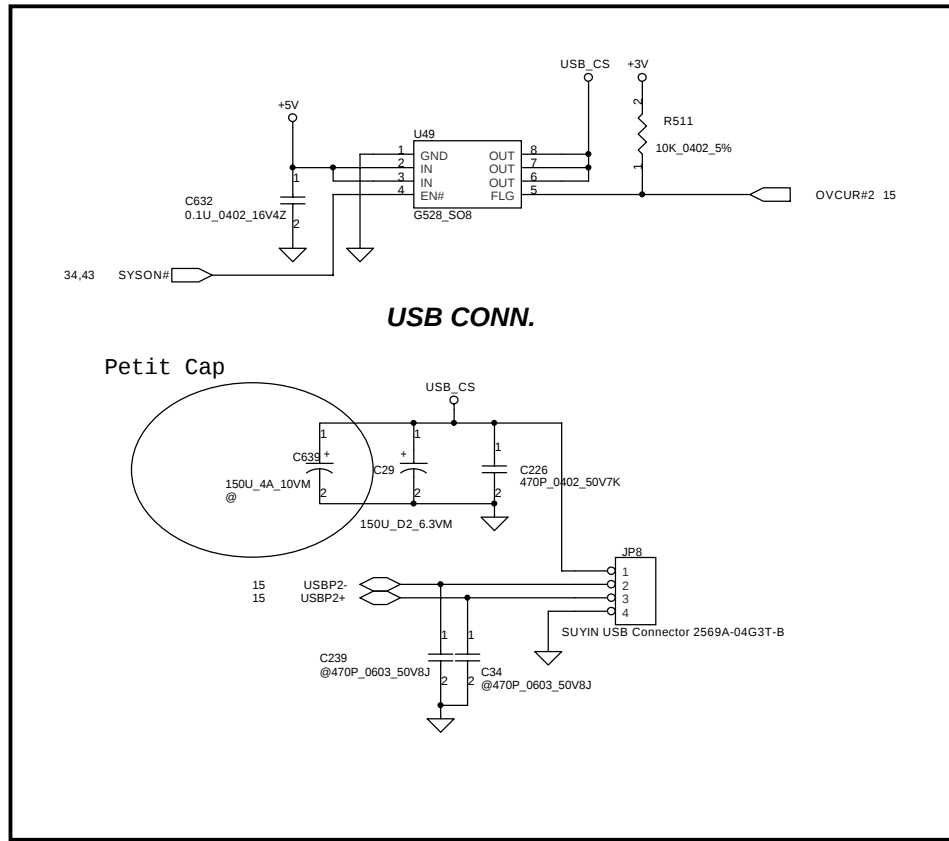
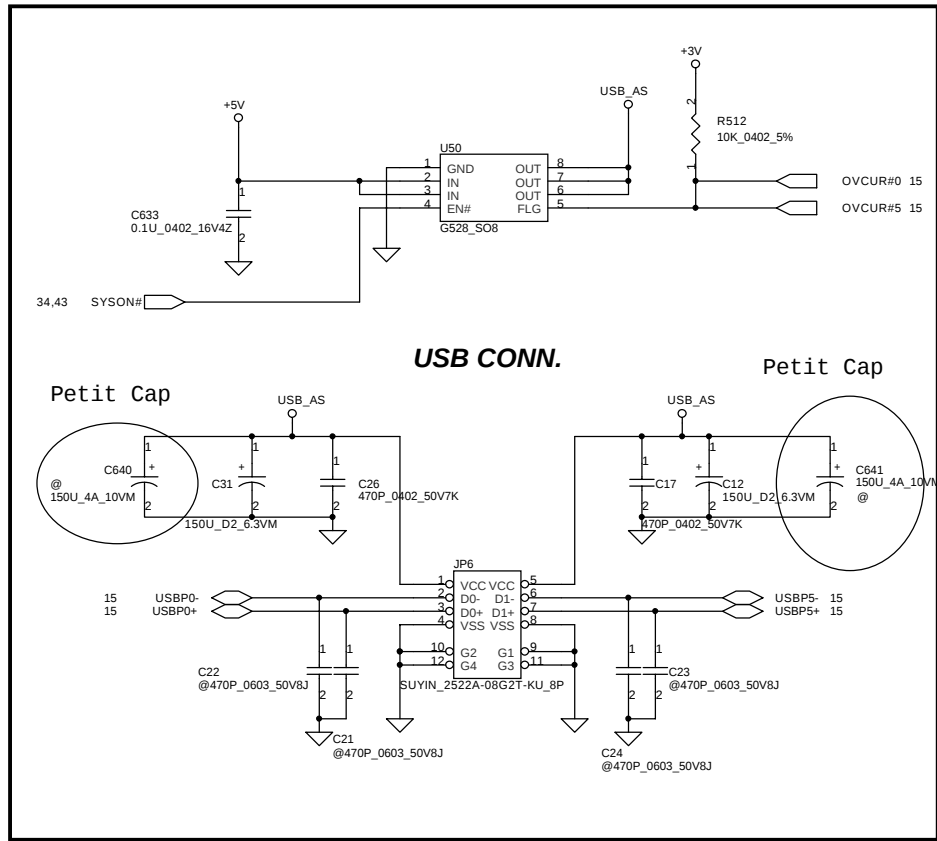
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Title	SCHEMATIC, M/B LA-2511
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Size B	Document Number 401313	Rev A
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Date: 一P期五, 九月 10, 2004 Sheet 25 of 45

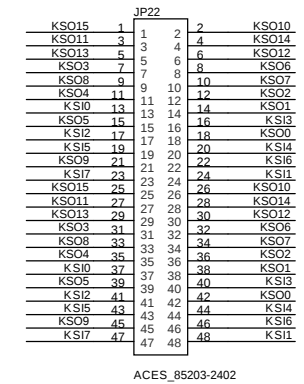
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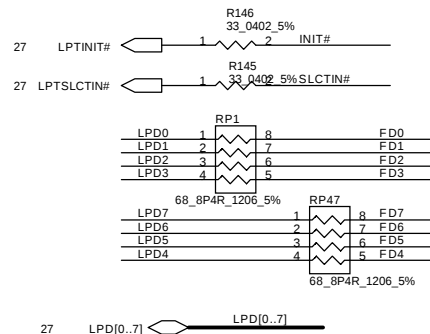
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Title	SCHEMATIC, M/B LA-2511	
Size	Document Number	Rev
B	401313	A
Date:	~P期五, 九月 10, 2004	Sheet 26 of 45

INT_KBD CONN.



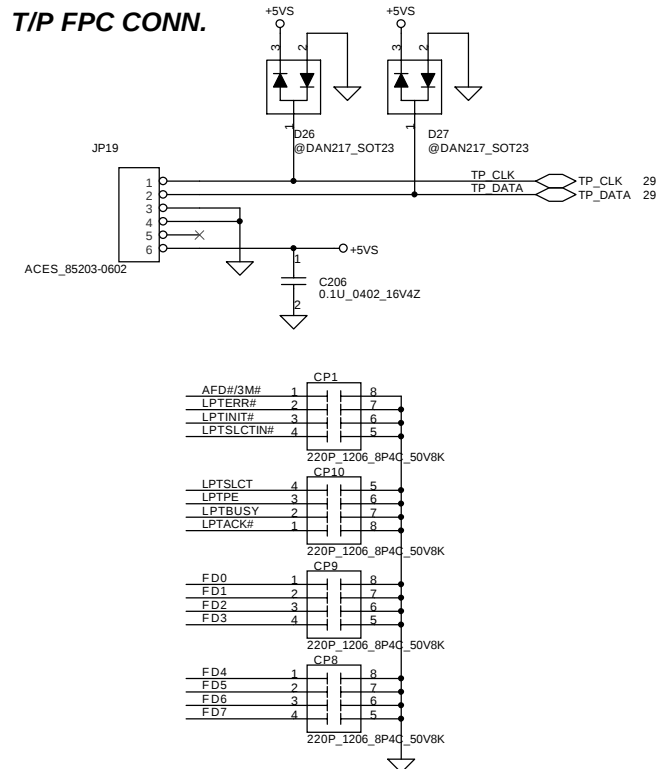
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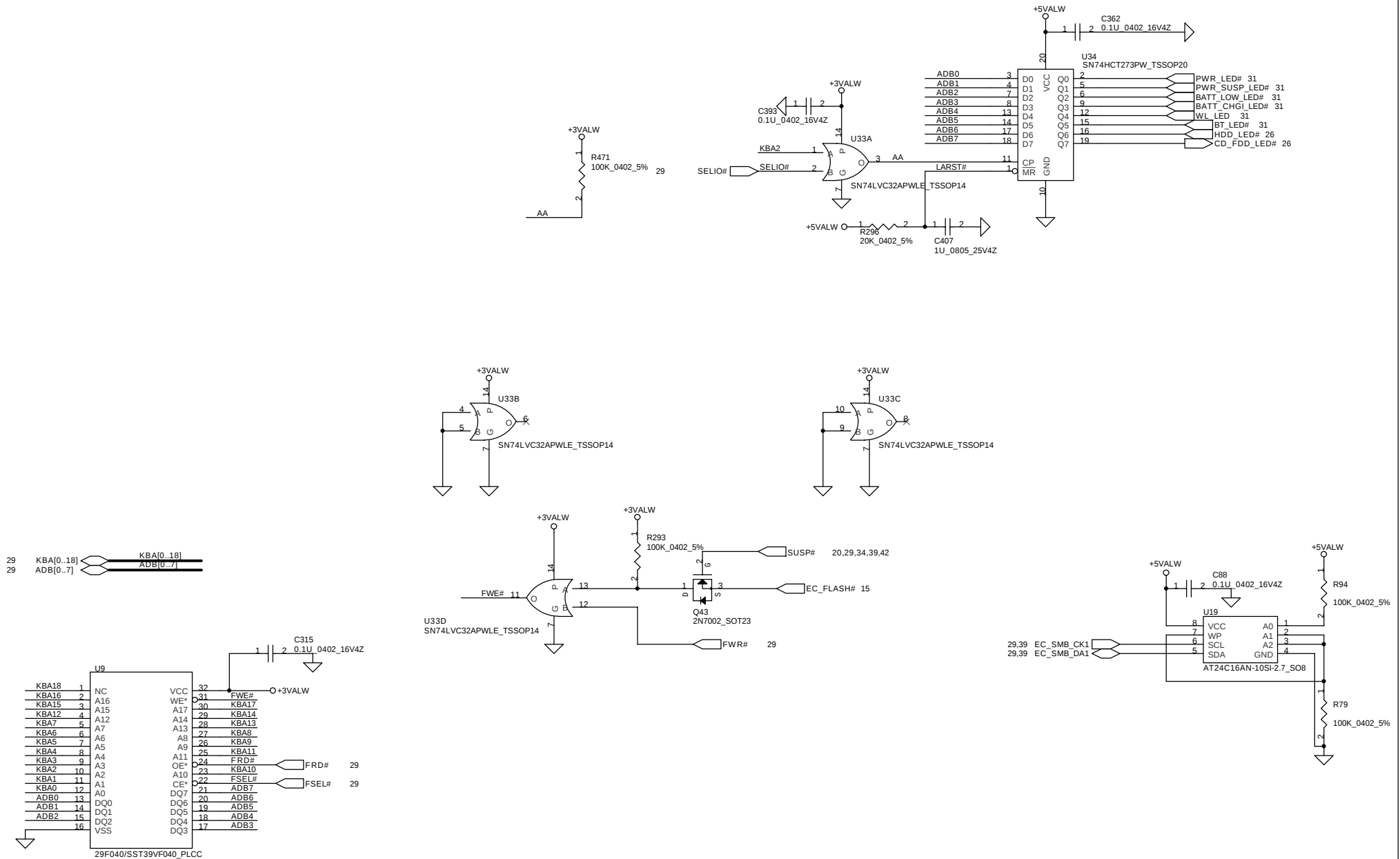
The schematic diagram illustrates the LPTCN-25 connector interface. It features a 25-pin connector (JP2) with the following connections:

- Pin 1:** Connected to +5V through a diode (D4, RB420D_SOT23) and a resistor (R1, 2.2K_0402_5%).
- Pin 2:** Connected to +5V.
- Pin 3:** Connected to LPTSTB# through a resistor (R2, 33 0402 5%).
- Pin 4:** Connected to LPTAFD# through a resistor (R3, 33 0402 5%).
- Pin 5:** Connected to LPTERR#.
- Pins 6-13:** Connected to FD0-FD7.
- Pins 14-25:** Connected to LPTACK#, LPTBUSY, LPTPE, and LPTSLCT.

A capacitor (C1, 220P_0402_50V7K) is connected between pins 1 and 2.



AL ID	Title			
	SCHEMATIC, M/B LA-2511			
	Size	Document Number		Rev
		401313		A
	Date:	~P 期五, 九月 10, 2004		Sheet 28 of 45

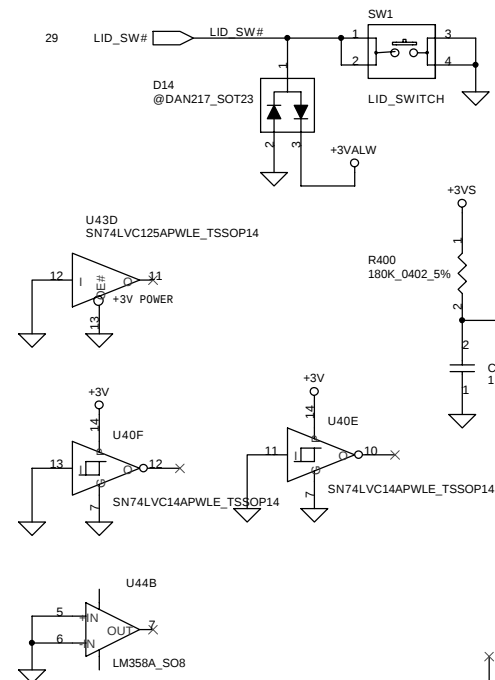


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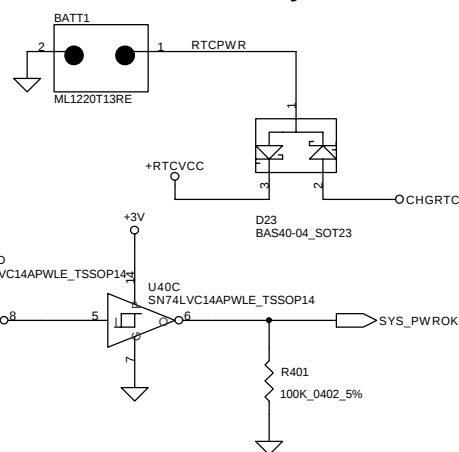
Title			SCHEMATIC, M/B LA-2511
Size	Document Number	Rev	
B	401313	A	
Date:	~P 期五, 九月 10, 2004	Sheet	30 of 45

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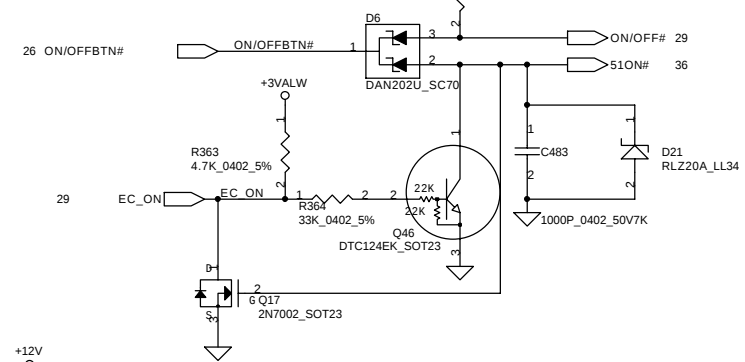
Power ON Circuit



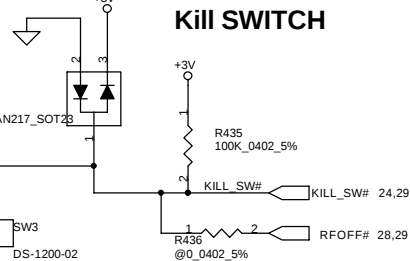
RTC Battery



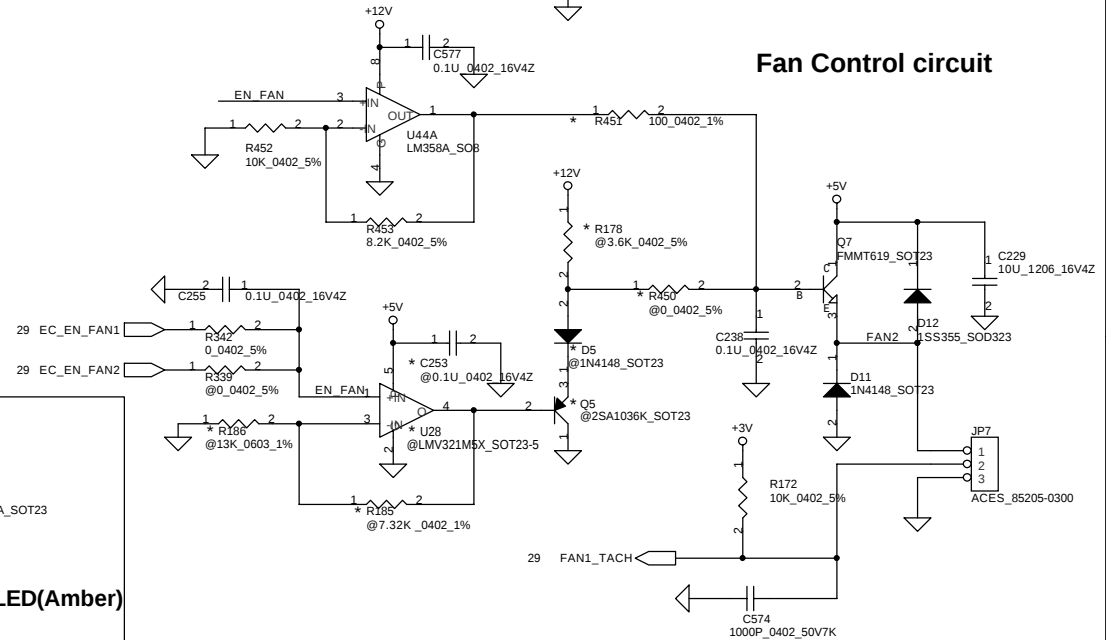
Power BTN



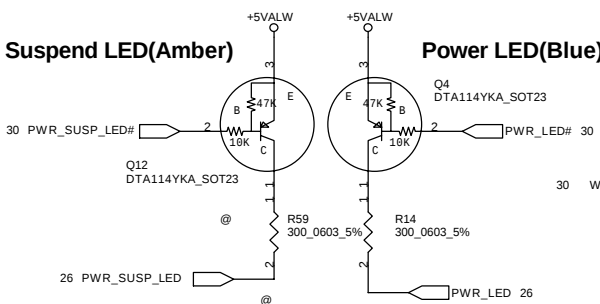
Kill SWITCH



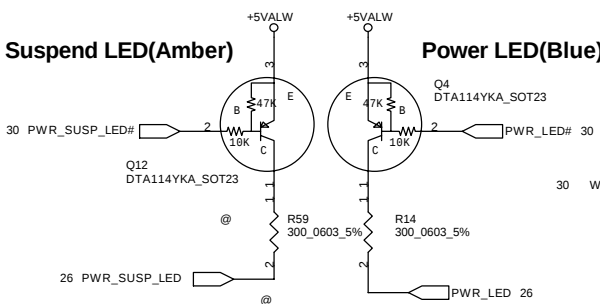
Fan Control circuit



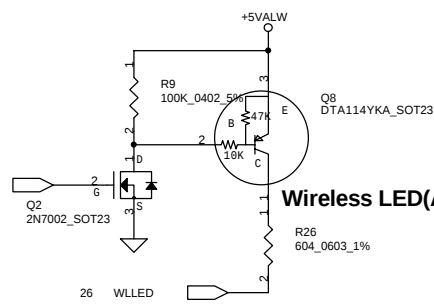
Suspend LED(Amber)



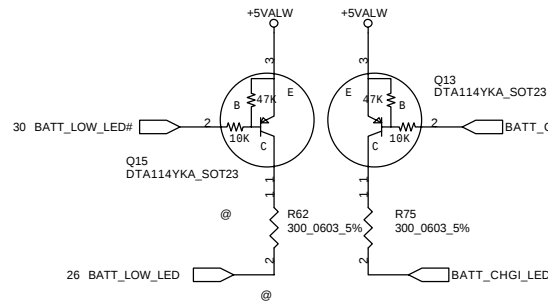
Power LED(Blue)



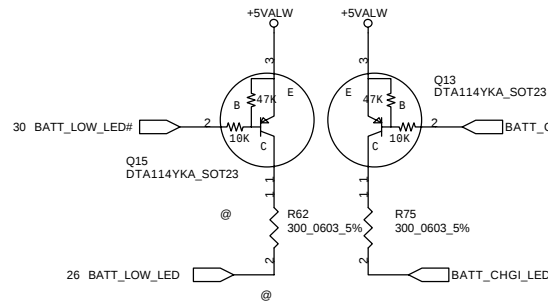
Wireless LED(Amber)



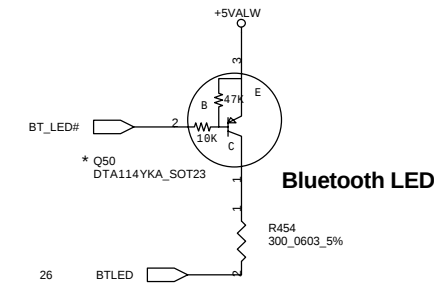
BATT Low LED(Amber)



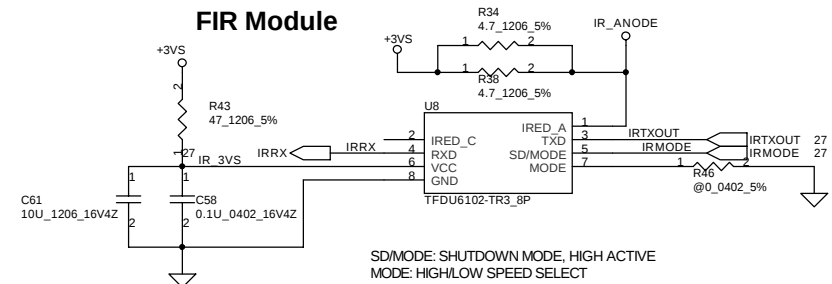
BATT Charge LED(Blue)



Bluetooth LED(Blue)



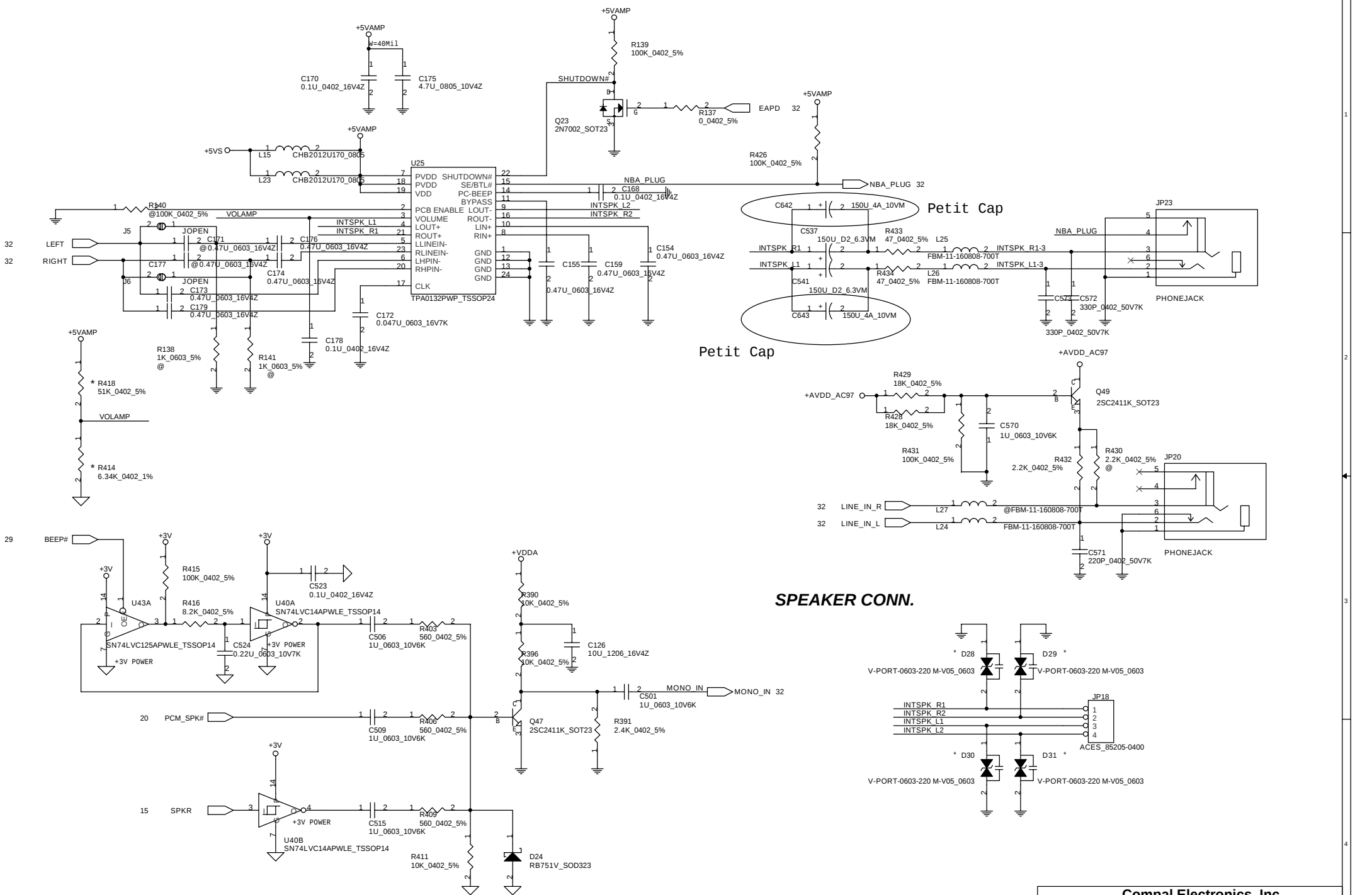
FIR Module



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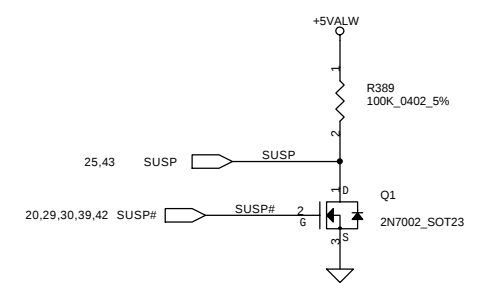
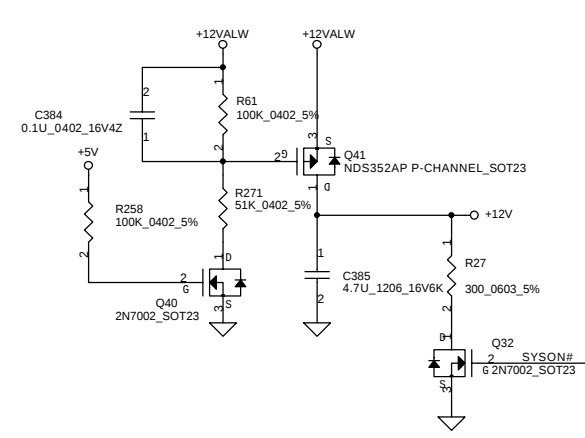
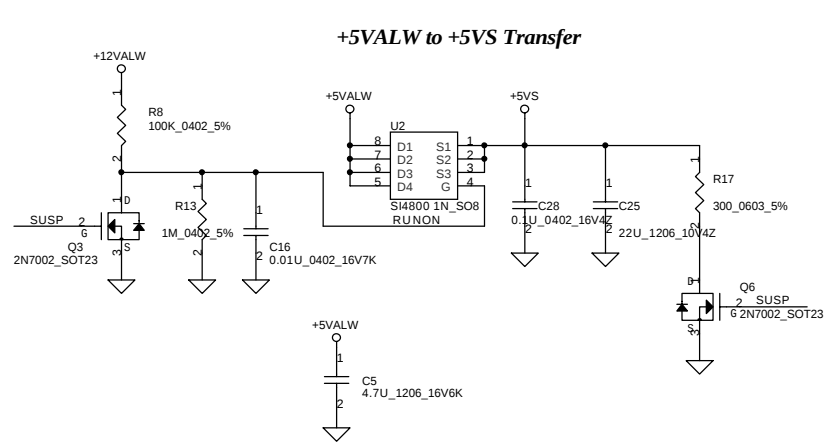
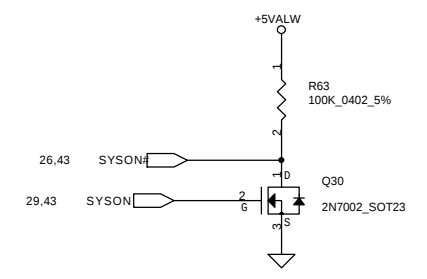
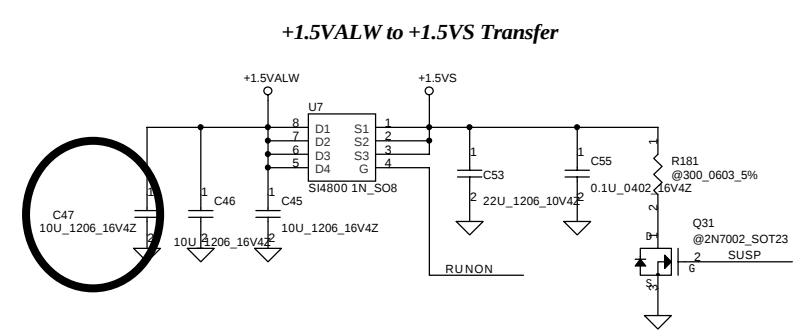
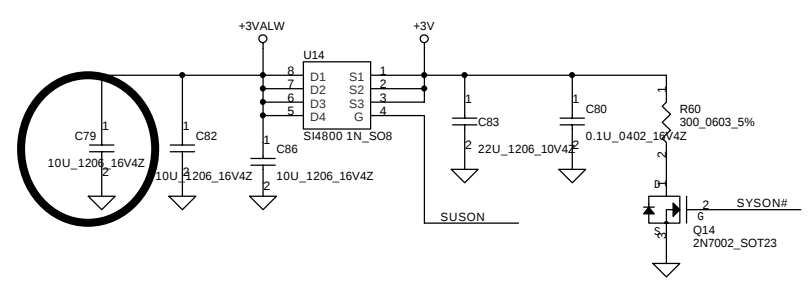
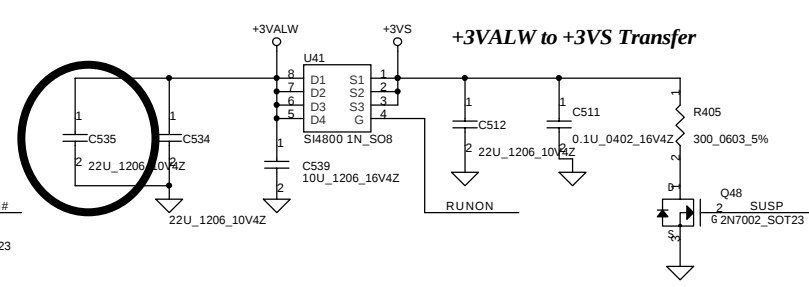
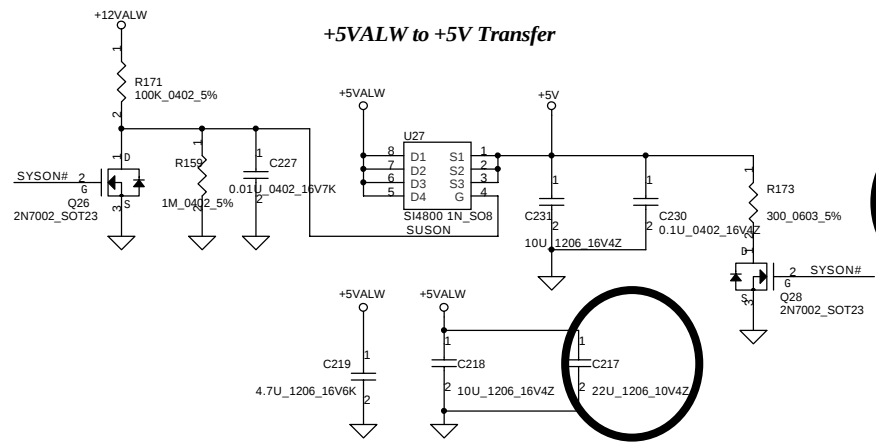
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Title			SCHEMATIC, M/B LA-2511	
Size	Document Number		401313	
Date:	~P 周五, 九月 10, 2004		Sheet	31 of 45
		Rev		A



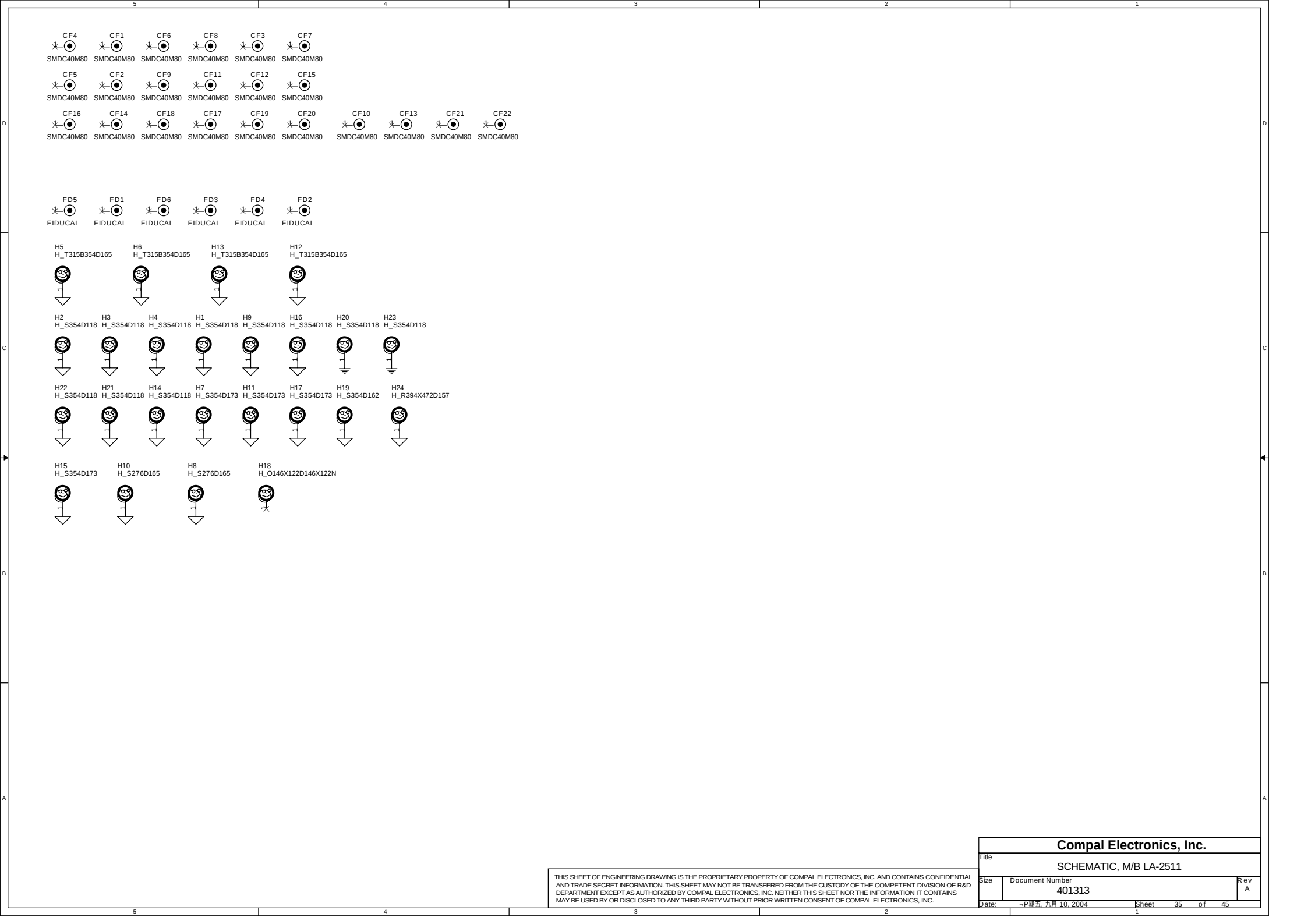
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Title			
SCHEMATIC, M/B LA-2511			
Size	Document Number		Rev
	401313		A
Date:	~P期五, 九月 10, 2004		Sheet 33 of 45



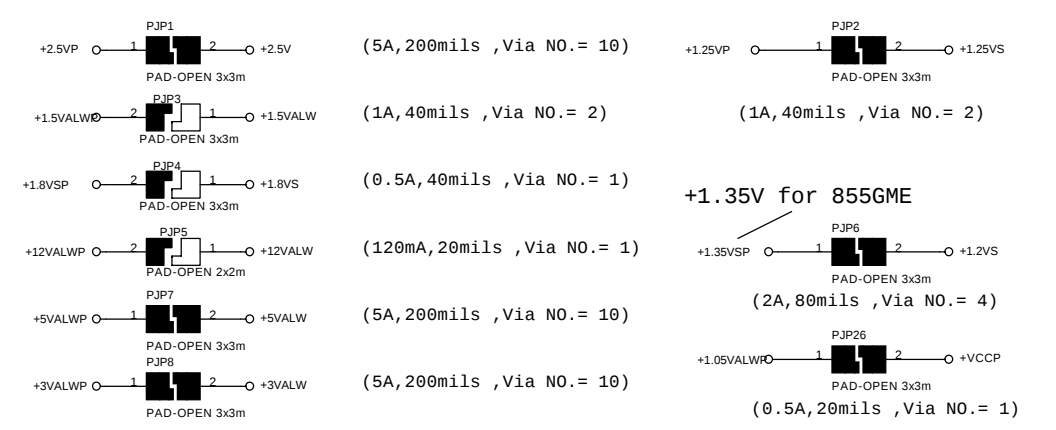
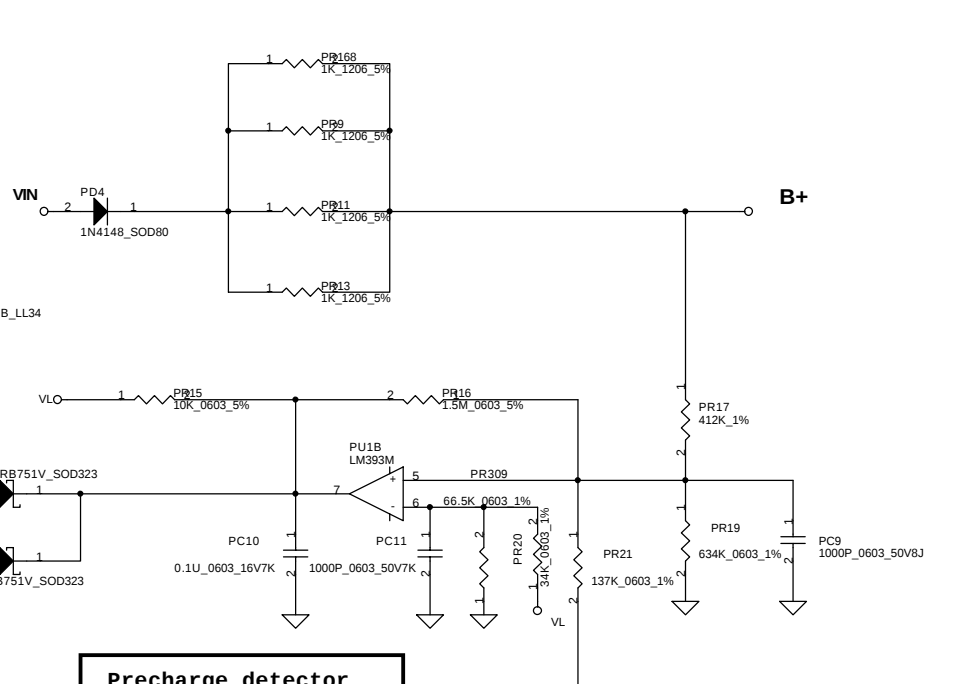
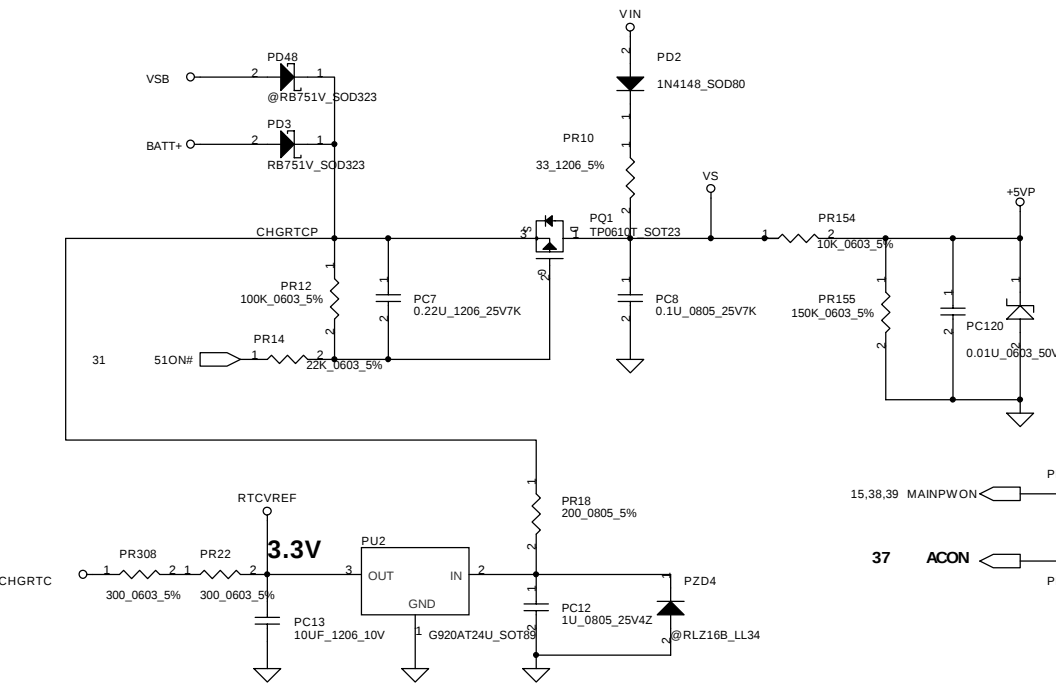
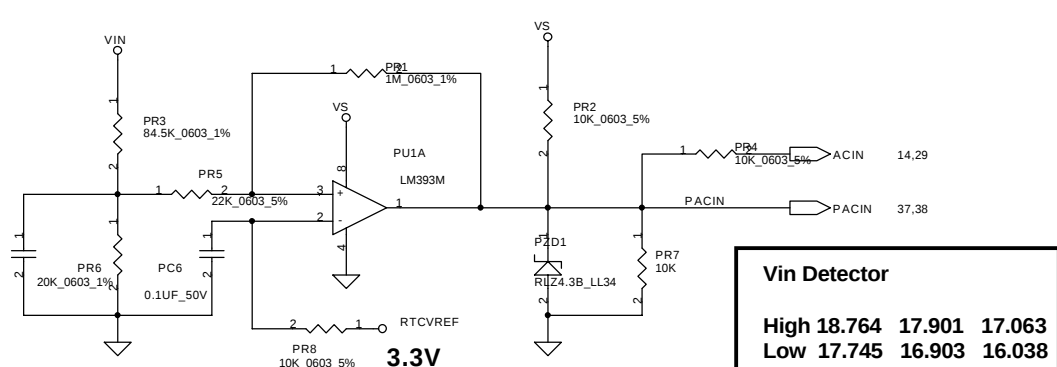
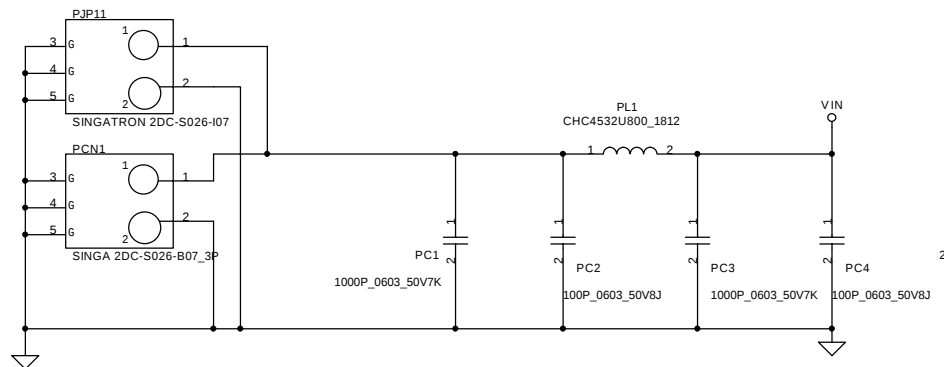
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Title			
SCHEMATIC, M/B LA-2511			
Size	Document Number		Rev
	401313		A
Date:	~P期五, 九月 10, 2004		Sheet 34 of 45



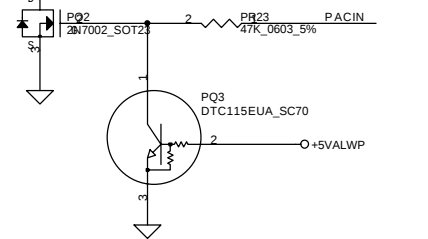
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Title		SCHEMATIC, M/B LA-2511	
Size	Document Number		Rev
	401313		A
Date:	~P期五, 九月 10, 2004		Sheet 35 of 45

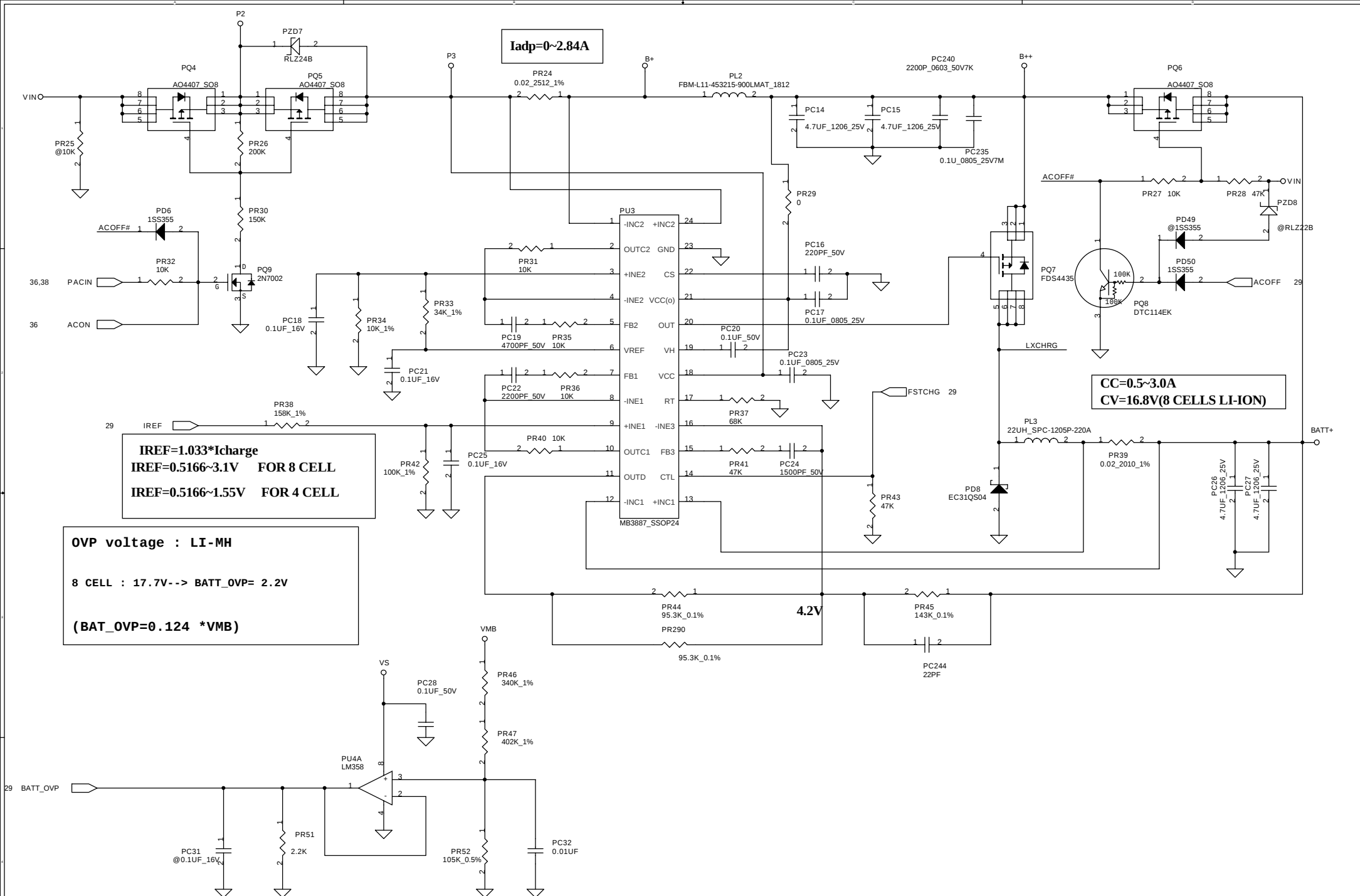


Precharge detector AC ADAPTOR		
16.69	16.05	15.42
15.6	15.02	14.35

Precharge detector AC ADAPTOR		
6.33	6.12	5.92
5.227	5.09	4.85



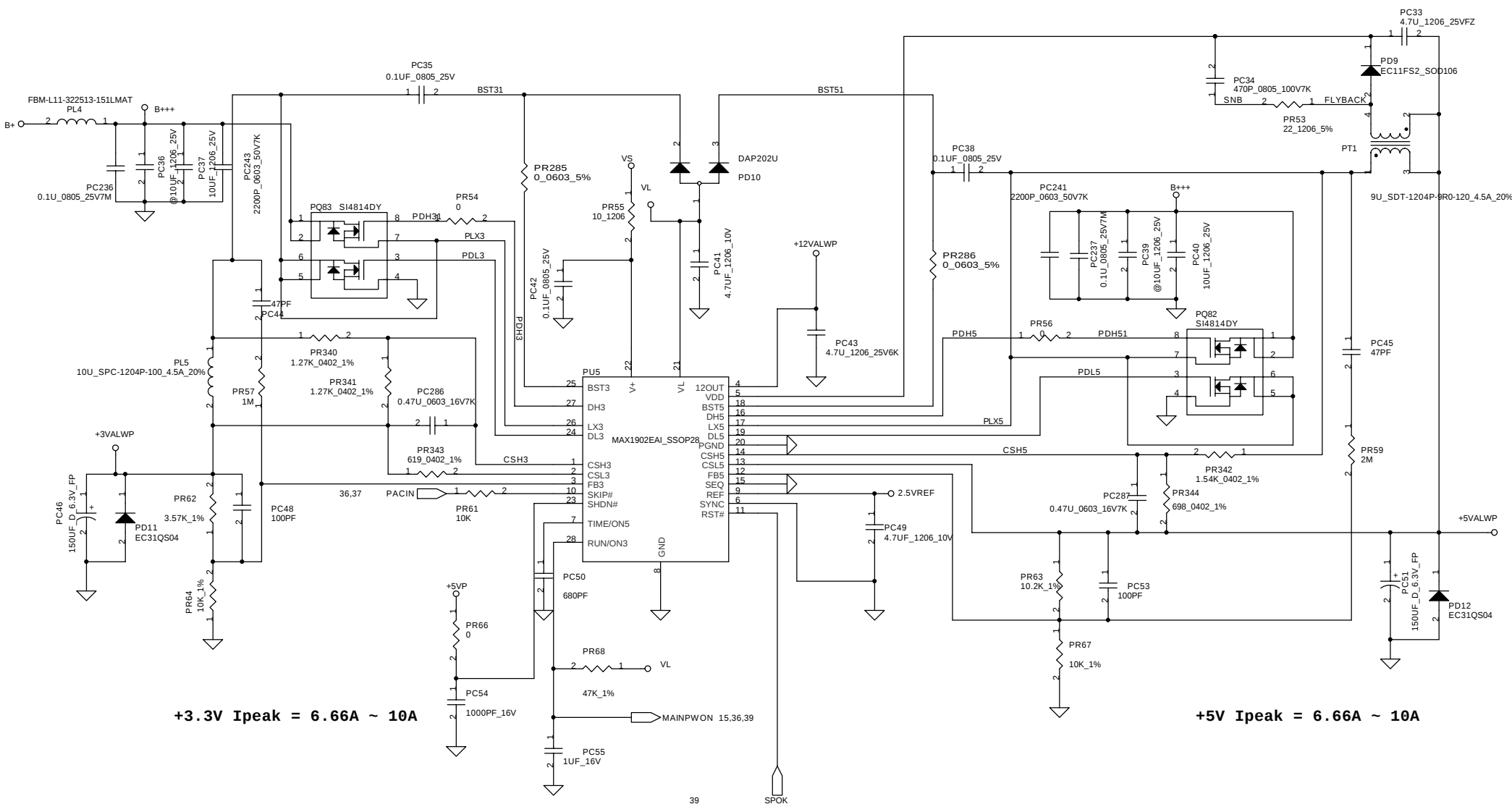
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Title		SCHEMATIC, M/B LA-2511	
Size	Document Number	401313	
B		A	
Date:	-P 期五 九月 10, 2004	Sheet	37 of 45

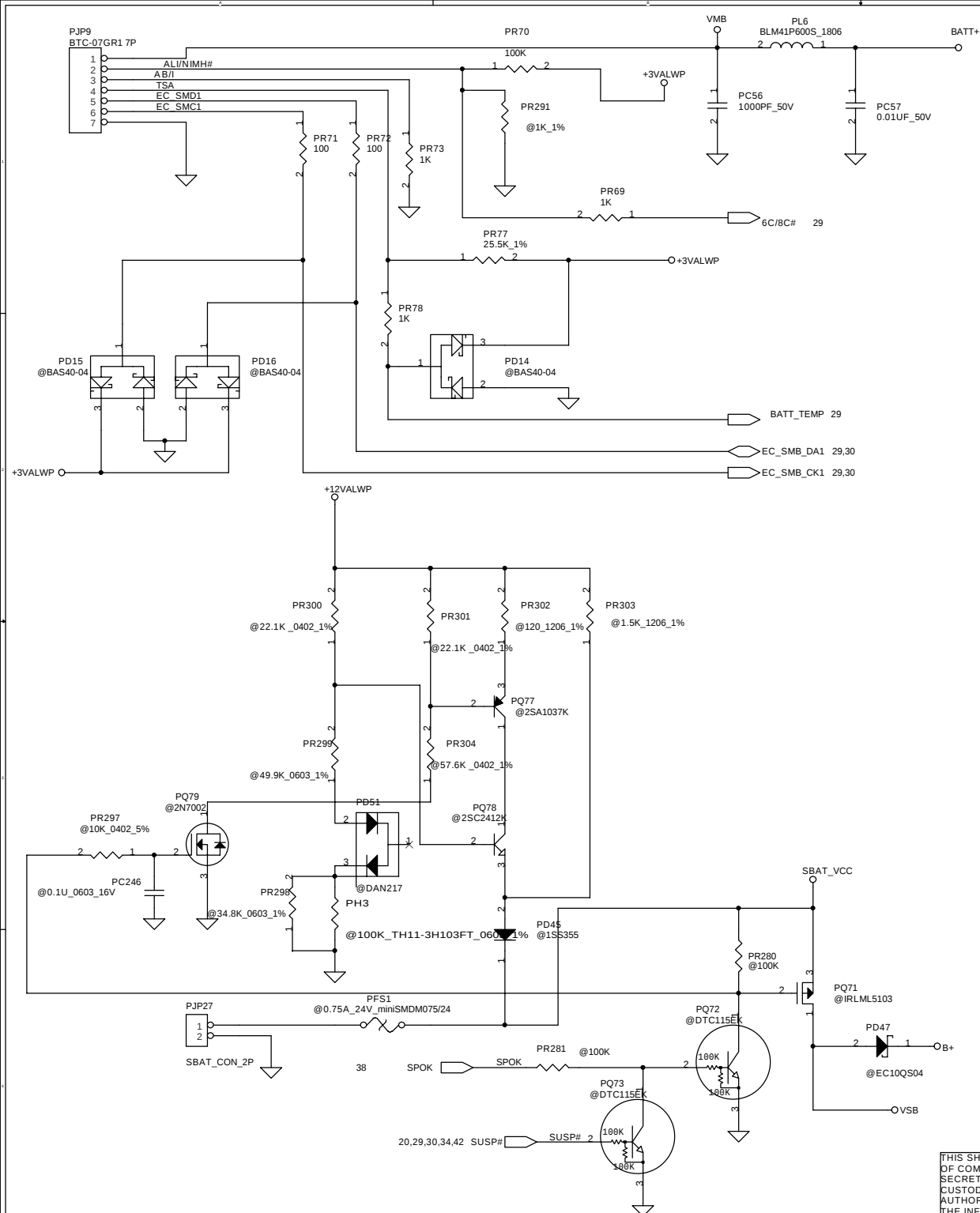


+3.3V Ipeak = 6.66A ~ 10A

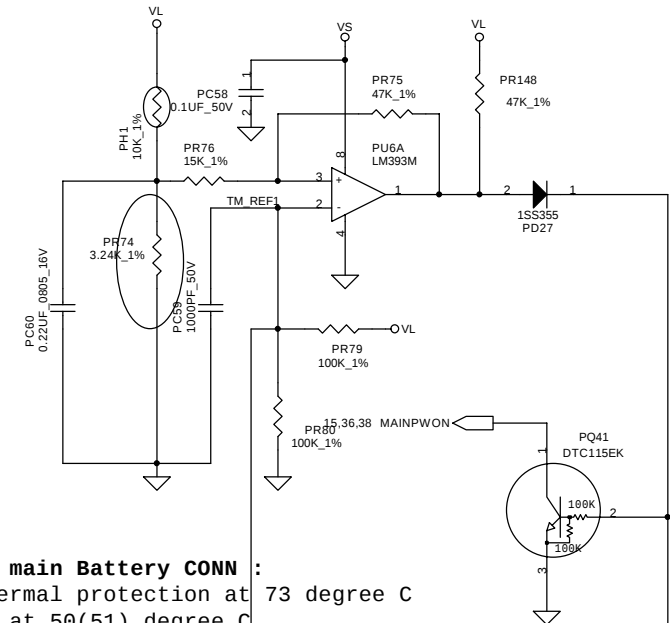
+5V Ipeak = 6.66A ~ 10A

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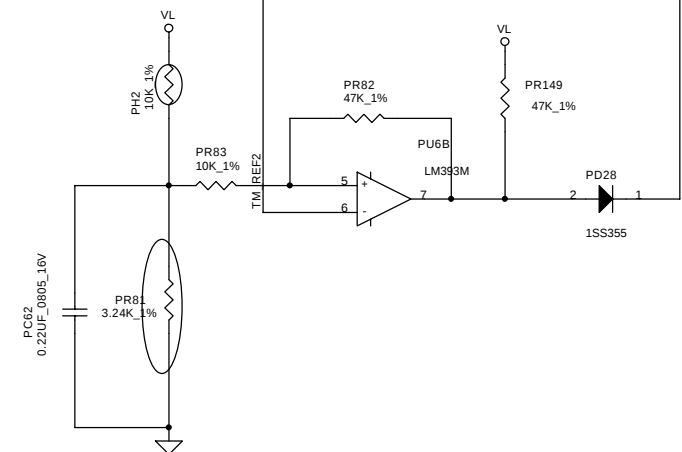
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Title		SCHEMATIC, M/B LA-2511	
Size	Document Number	Rev	
B	401313	A	
Date: -P 期五, 九月 10, 2004		Sheet	38 of 45



PH1 under CPU botten side :
CPU thermal protection at 82 degree C
Recovery at 48 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 73 degree C
Recovery at 50(51) degree C



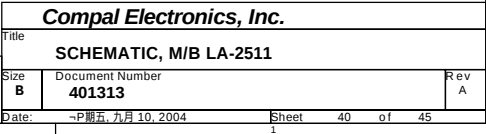
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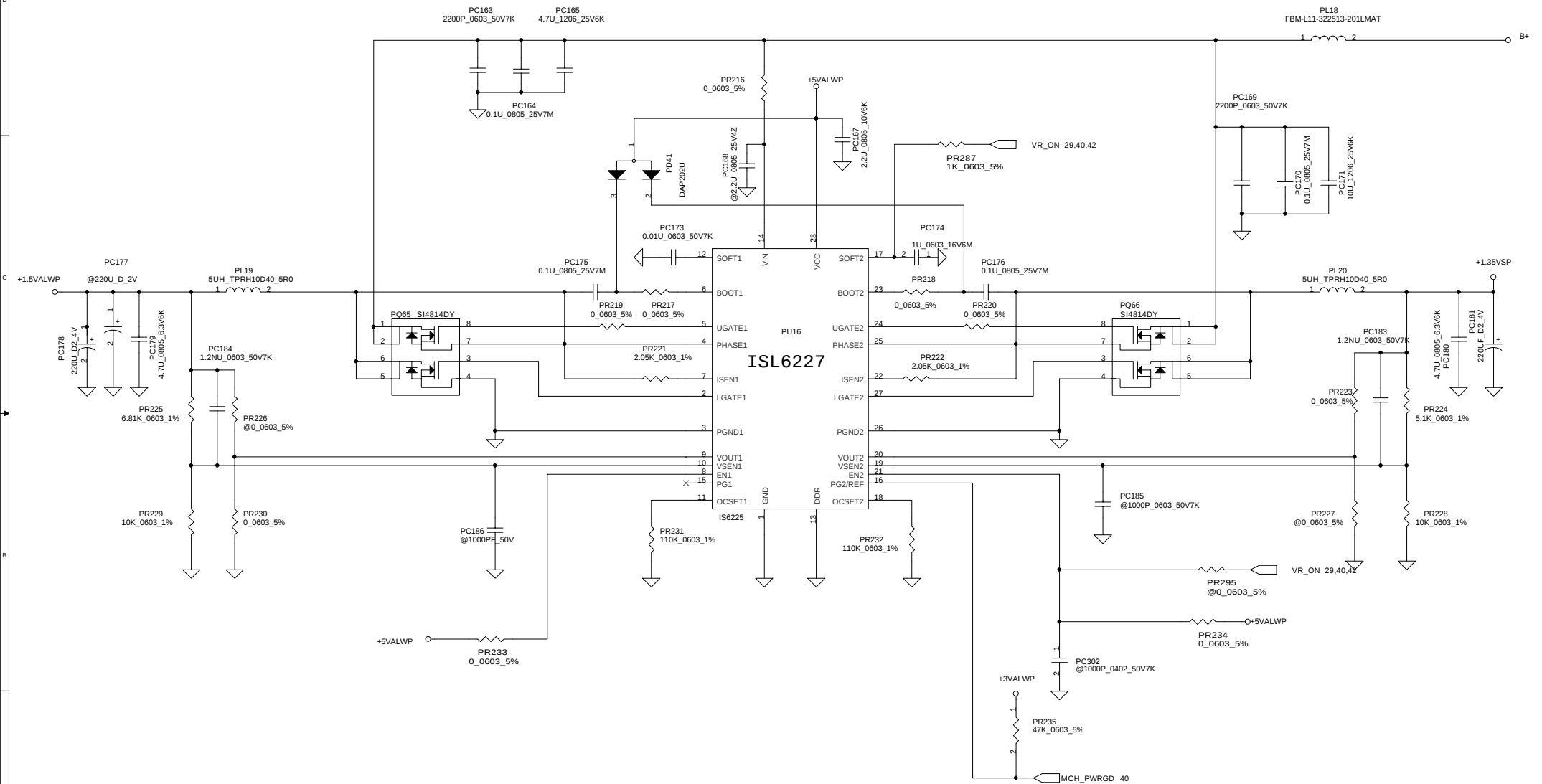
SCHEMATIC, M/B LA-2511

Size	Document Number	Rev
B	401313	A

Date: -P 期五, 九月 10, 2004 Sheet 39 of 45



+1.5VALWPV/+1.35VSP

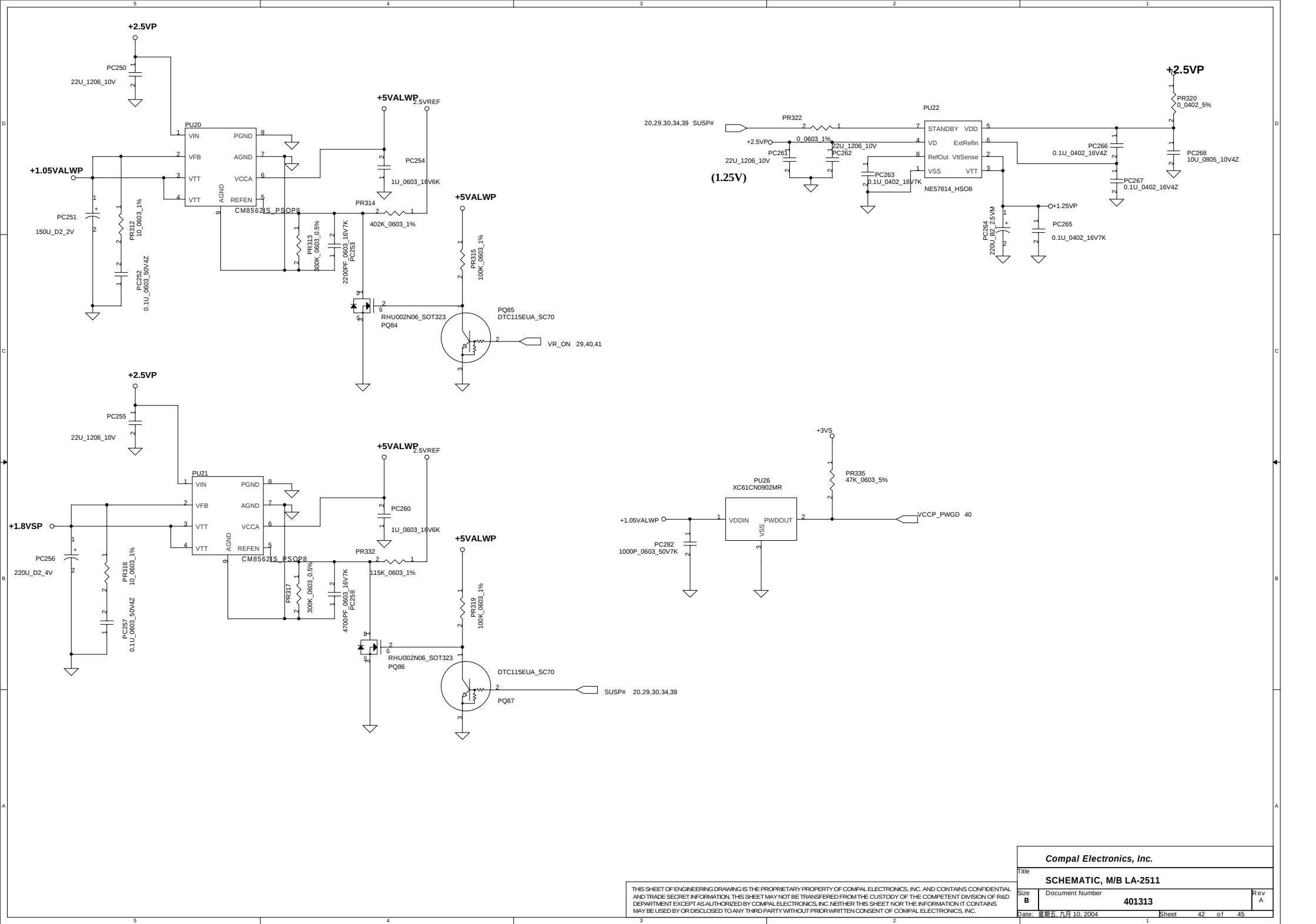


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Title	SCHEMATIC, M/B LA-2511
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Size B	Document Number	Rev A
	401313	
Date: 星期五, 九月 10, 2004		Sheet 41 of 45

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Title			
SCHEMATIC, M/B LA-2511			
Size	Document Number	Rev	
B	401313	A	
Date:	星期五, 九月 10, 2004	Sheet	42 of 45

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
1		Modify 1.05VP voltage level		42	1. change PR314 to 402k		DVT
2		Change PU16(ISL6227) 135VSP power build from softstart build to enable build		41	1.delete PR287; change PC174 from 1u 0805 to 0.01u 0603;add PR295:0		
3		To leave PC302 for 1.35VSP soft start time		41			
4		Change PU16(ISL6227) 135VSP power build from enable build to softstart build due to the sequence		41	1.add PR287:1k ; change PC174 from 0.01u 0603 to 1u 0603;delete PR295:0;add PR234:0		
5		change PU2 from S-81233SG(sot89) to G920AT24U(sot89)		36	1.delete PZD2;PZD4		
6							
7							
8							
9							

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Title			
SCHEMATIC, M/B LA-2511			
Size	Document Number		Rev
	401313		A
Date:	星期五, 九月 10, 2004		Sheet 44 of 45

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	VER	Phase
1	Delete R45,R47	EMI cost down	0.2	28			
2	Add R505,C627	Improve signal quality					
3							
4							
5							
6							
7							
8							
9							

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TitleSCHEMATIC, M/B LA-2511

SizeDocument Number401313

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Date~P期五, 九月 10, 2004Sheet45 of 45