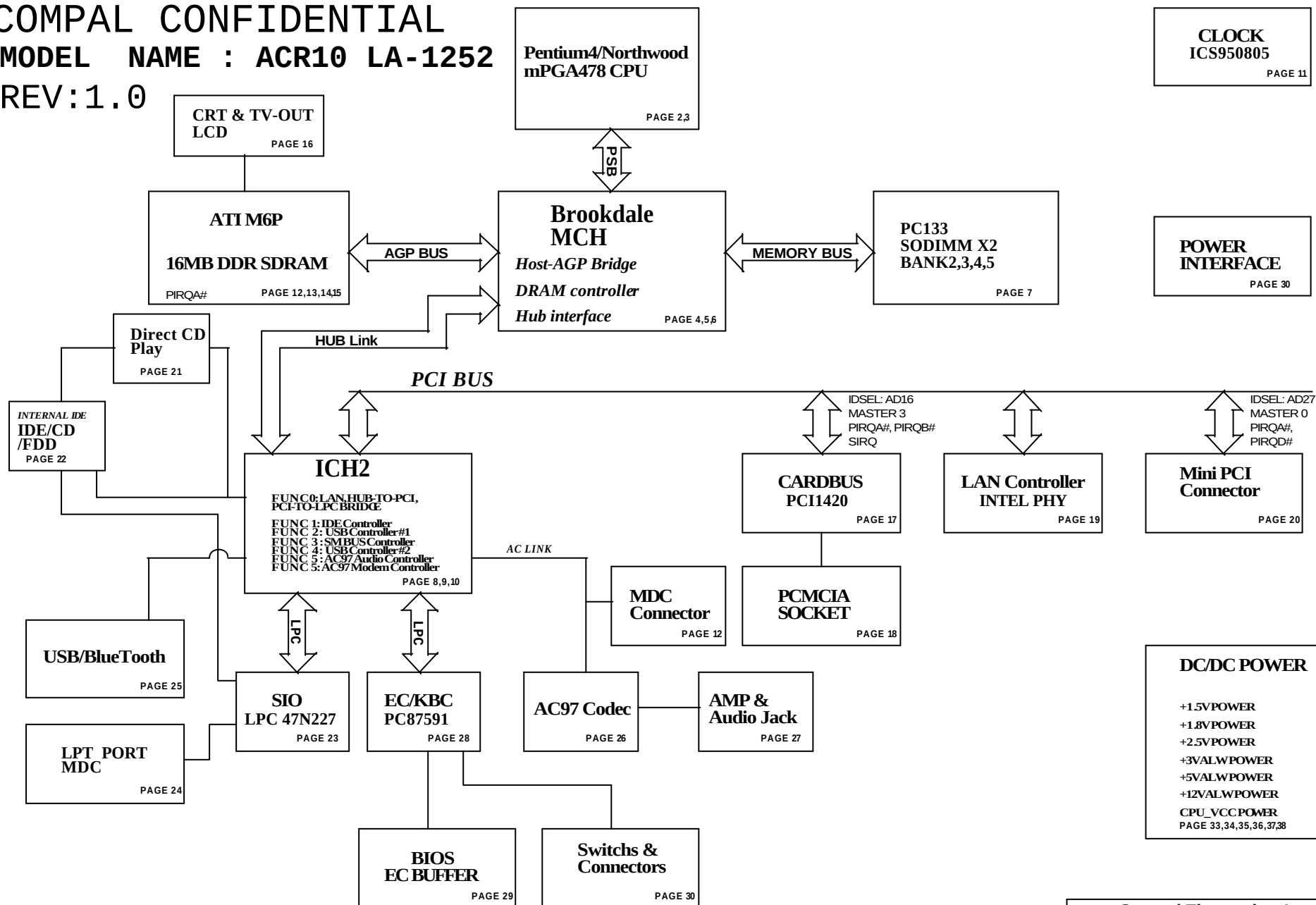
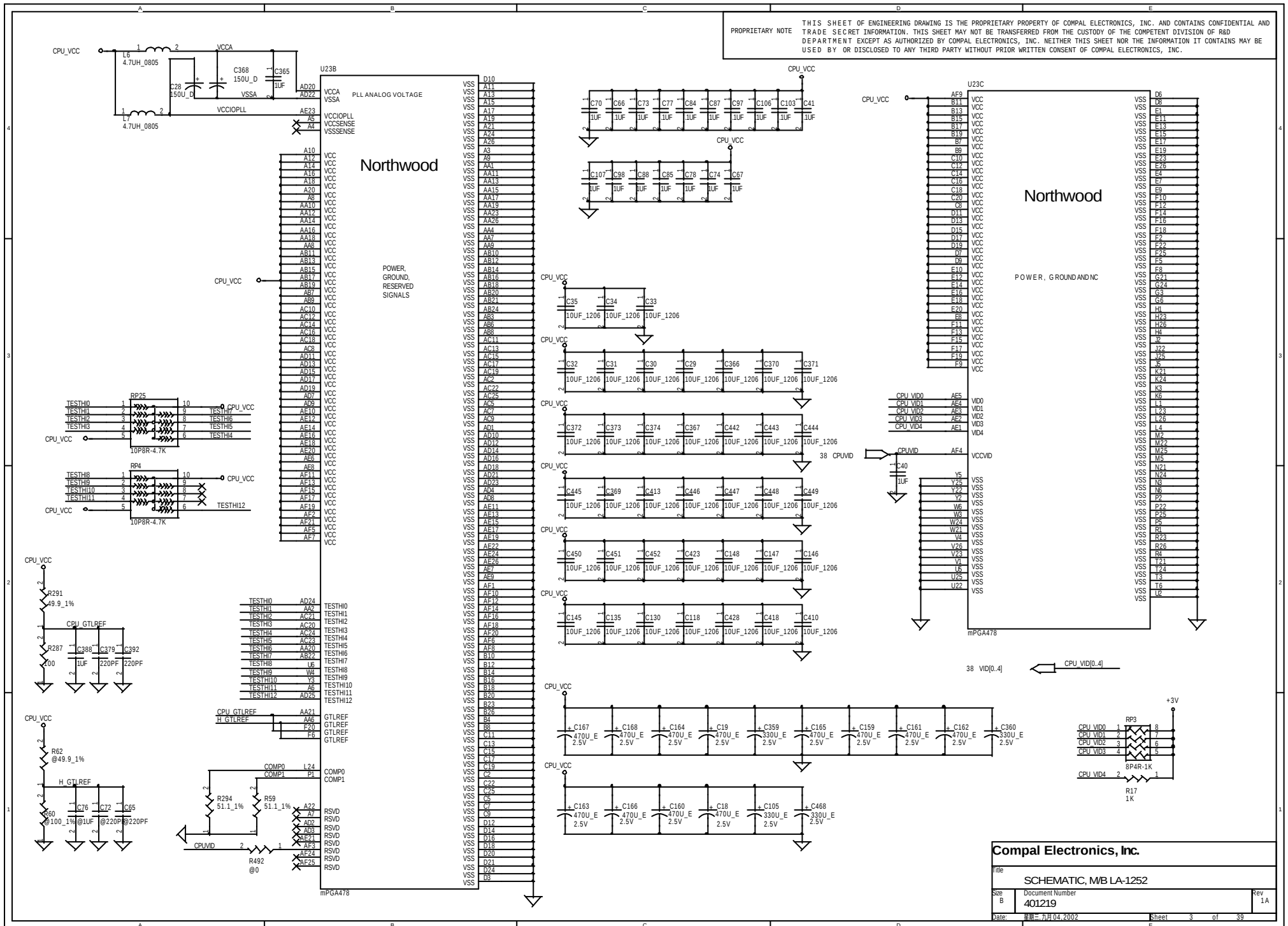


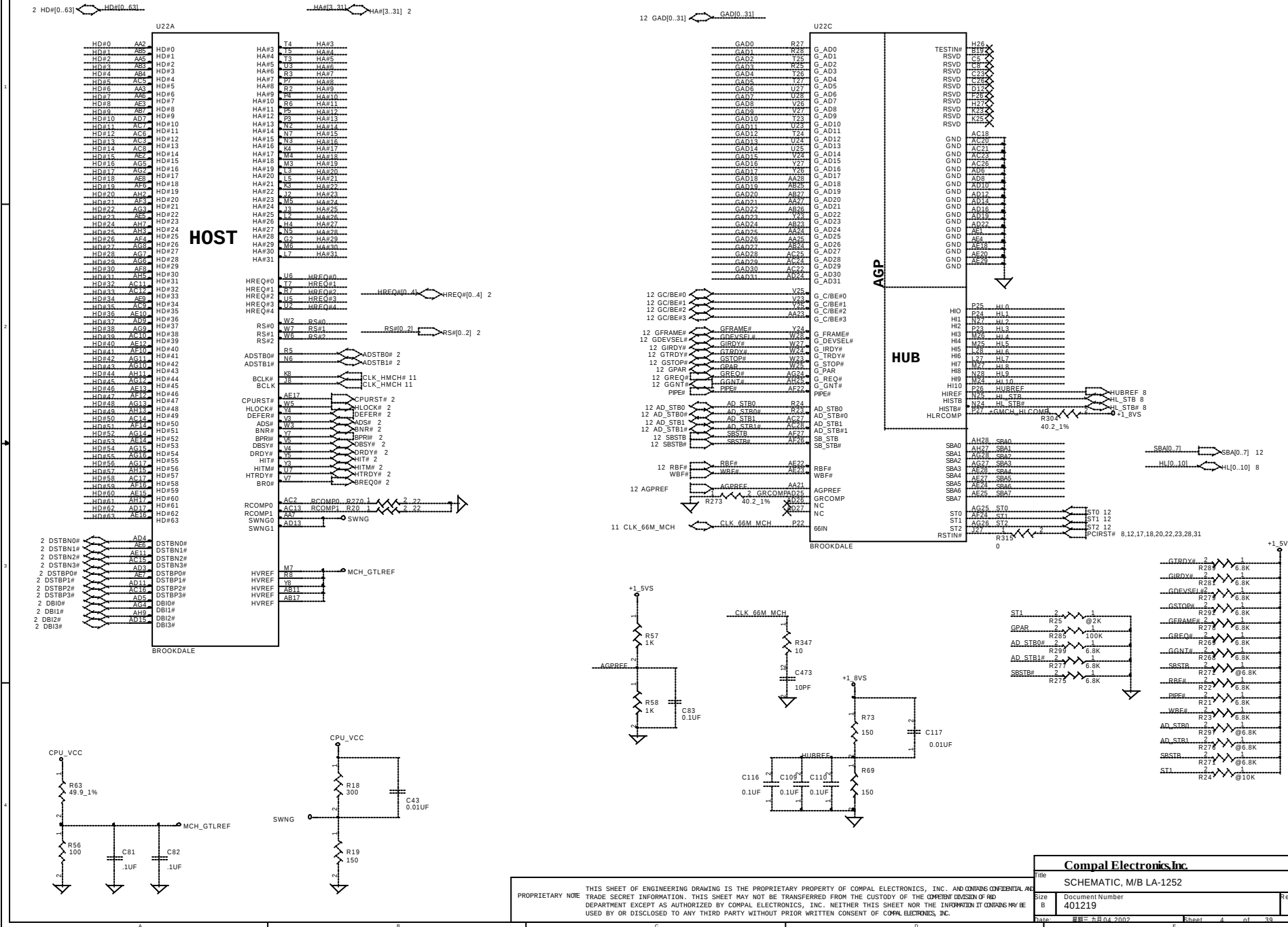
COMPAL CONFIDENTIAL
MODEL NAME : ACR10 LA-1252
REV:1.0



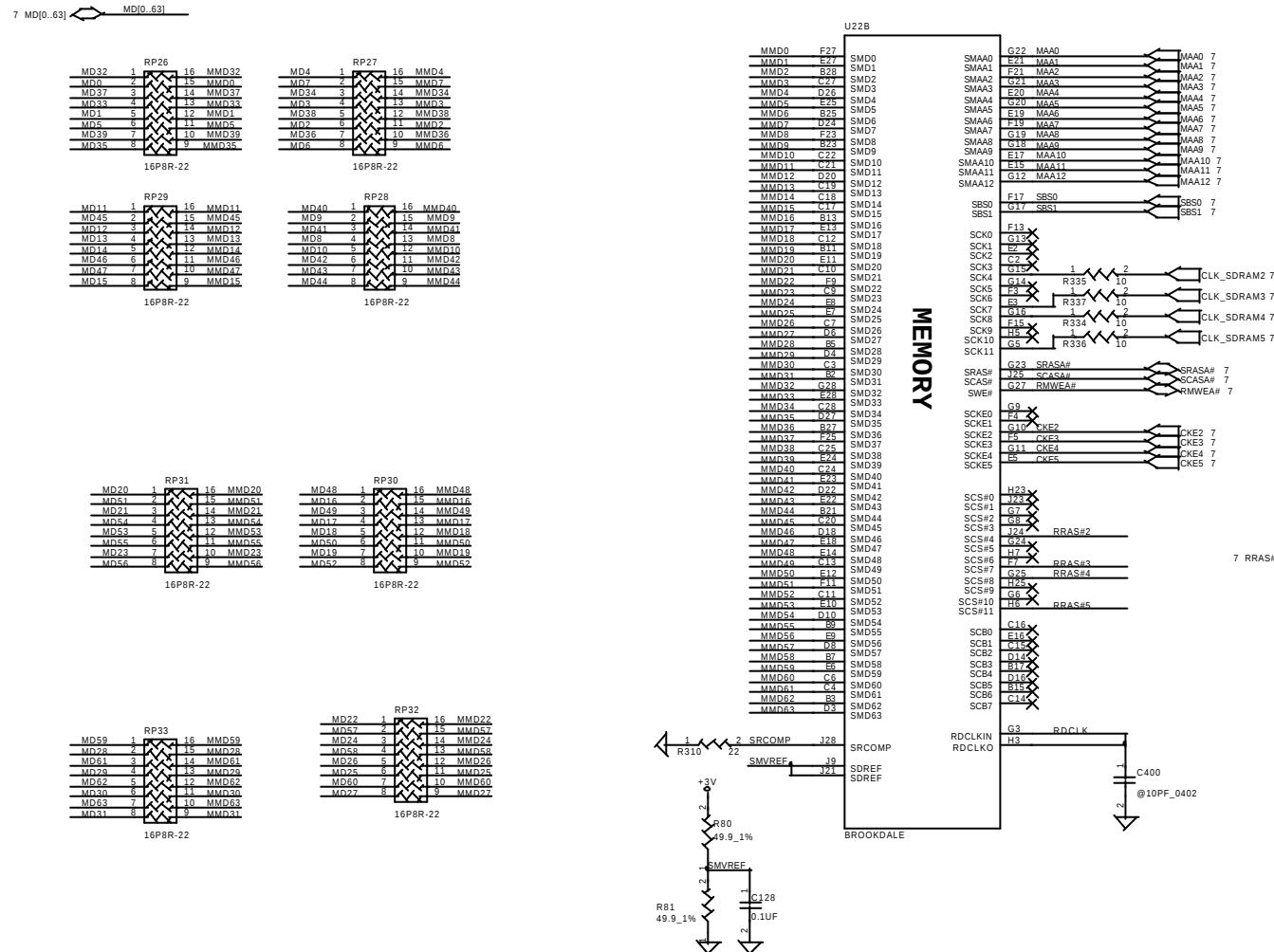
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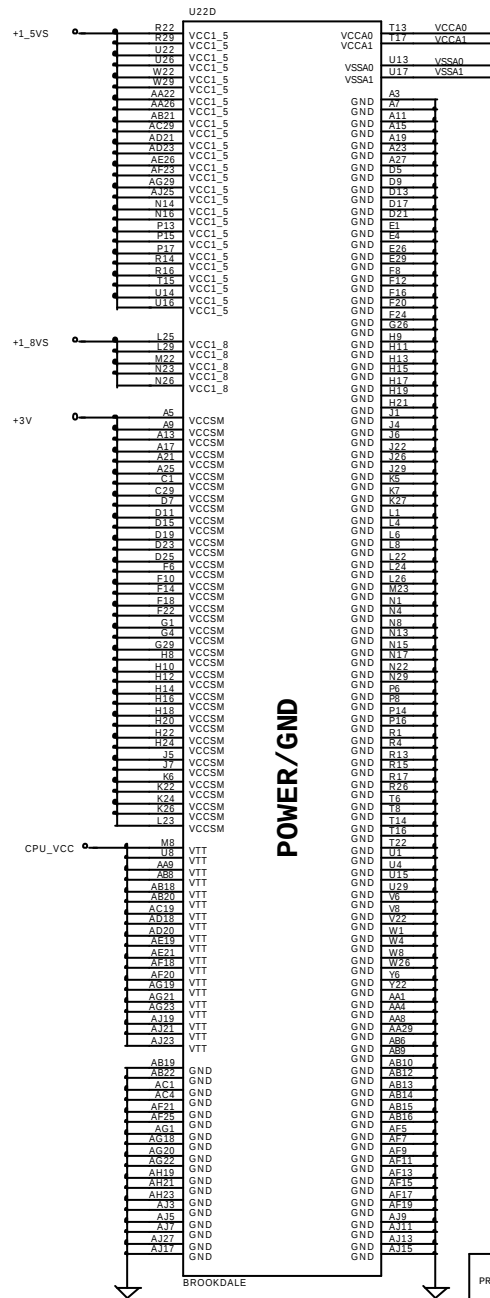
MC-1/3(GTL+,AGP,HUB)



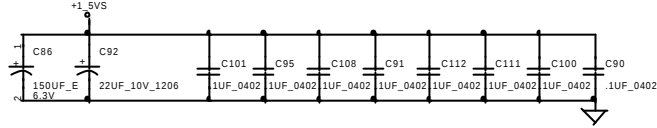
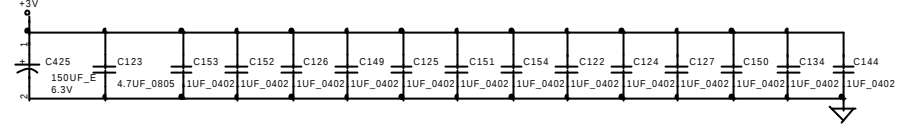
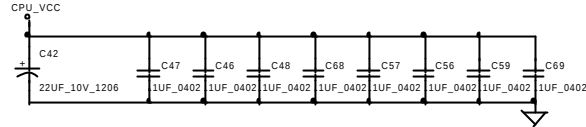
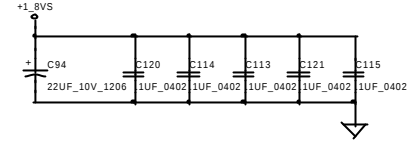
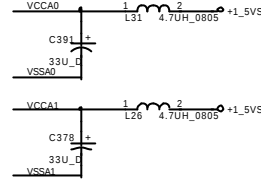
MCH-2/3(SDRAM)



MCH-3/3(Power)



POWER/GND



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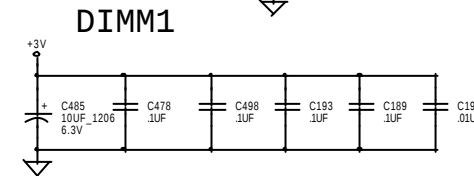
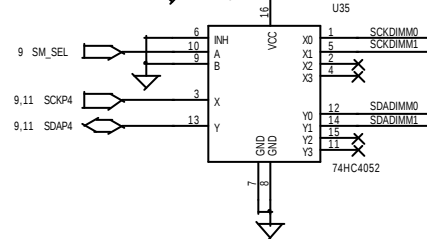
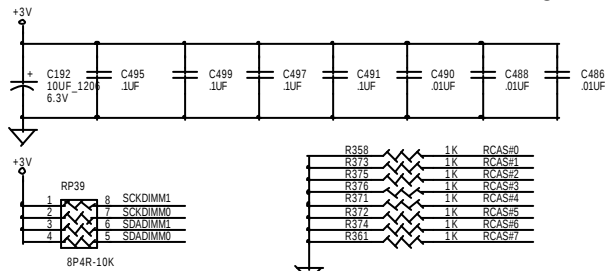
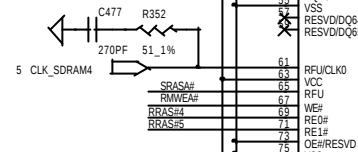
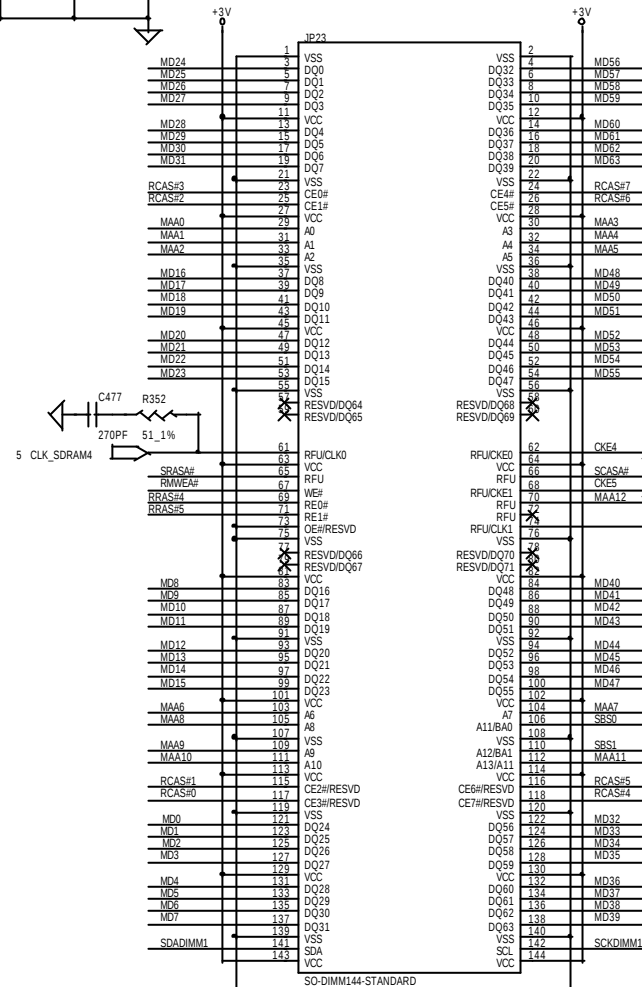
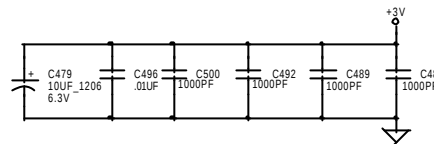
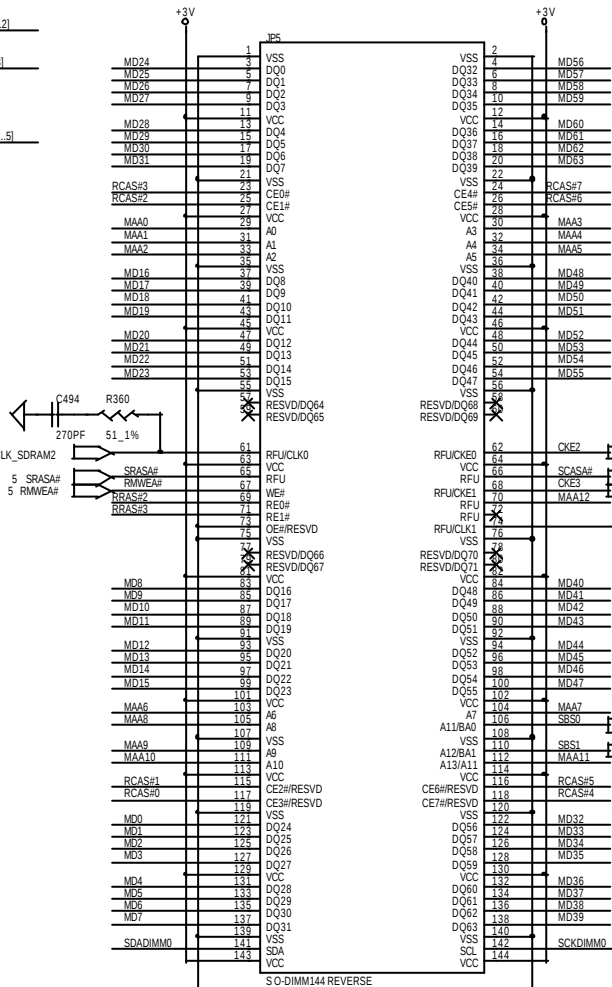
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SO-DIMM 144 PINS
RAM MODULE CONN.

BANK2/3

BANK4/5

5 MAA[0..12] → MAA[0..12]
5 MD[0..63] → MD[0..63]
5 RRAS#[2..5] → RRAS#[2..5]



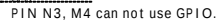
Compal Electronics, Inc.

SCHEMATIC, M/B LA-1252

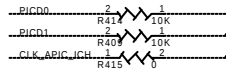
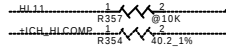
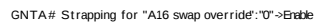
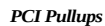
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(FW82801BA)

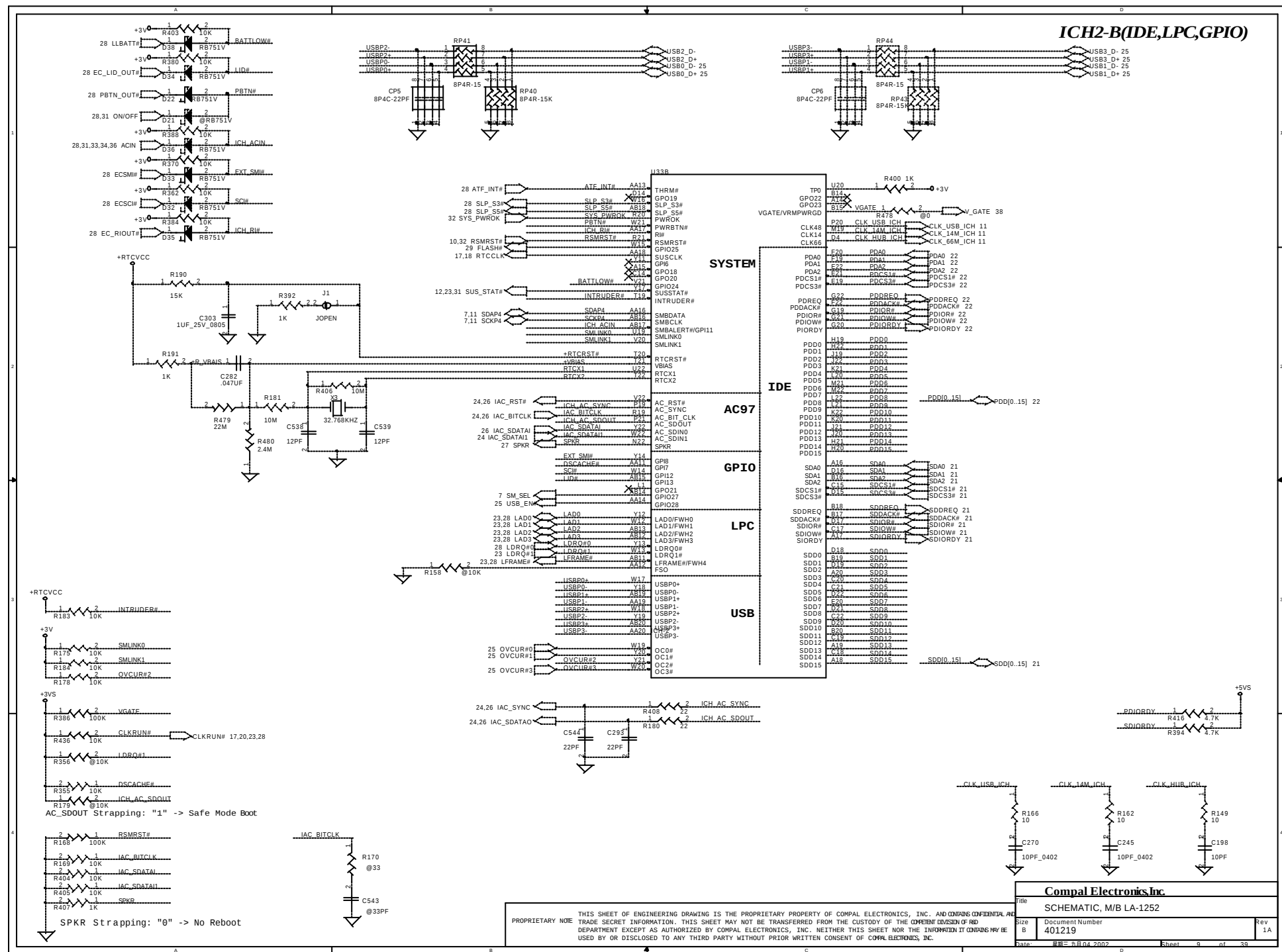


PCI REQ ASSIGNMENT	
REQ#0	WLAN
REQ#1	NC
REQ#2	NC
REQ#3	PCMCIA CONTROLLER
REQ#4	NC

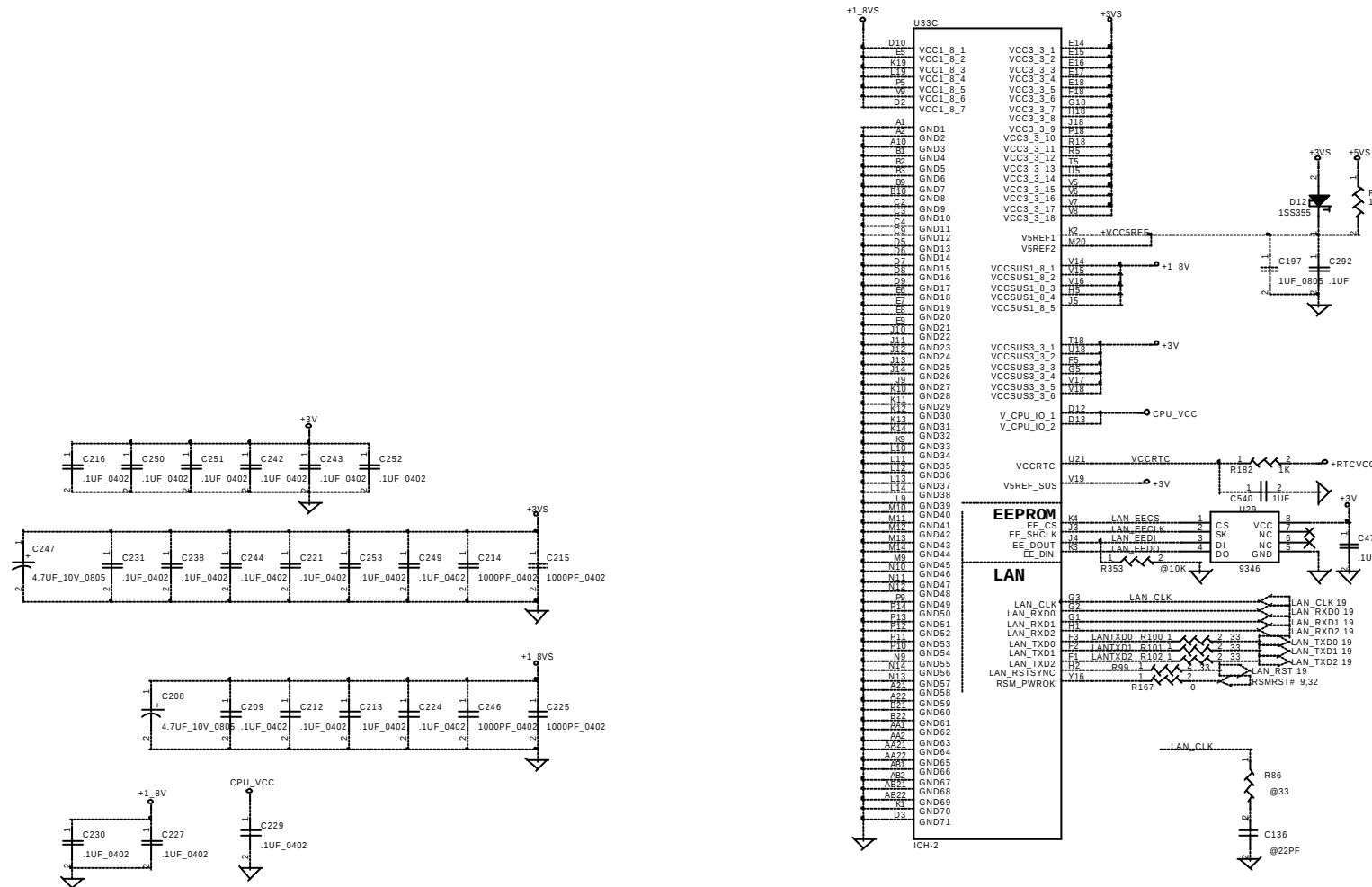


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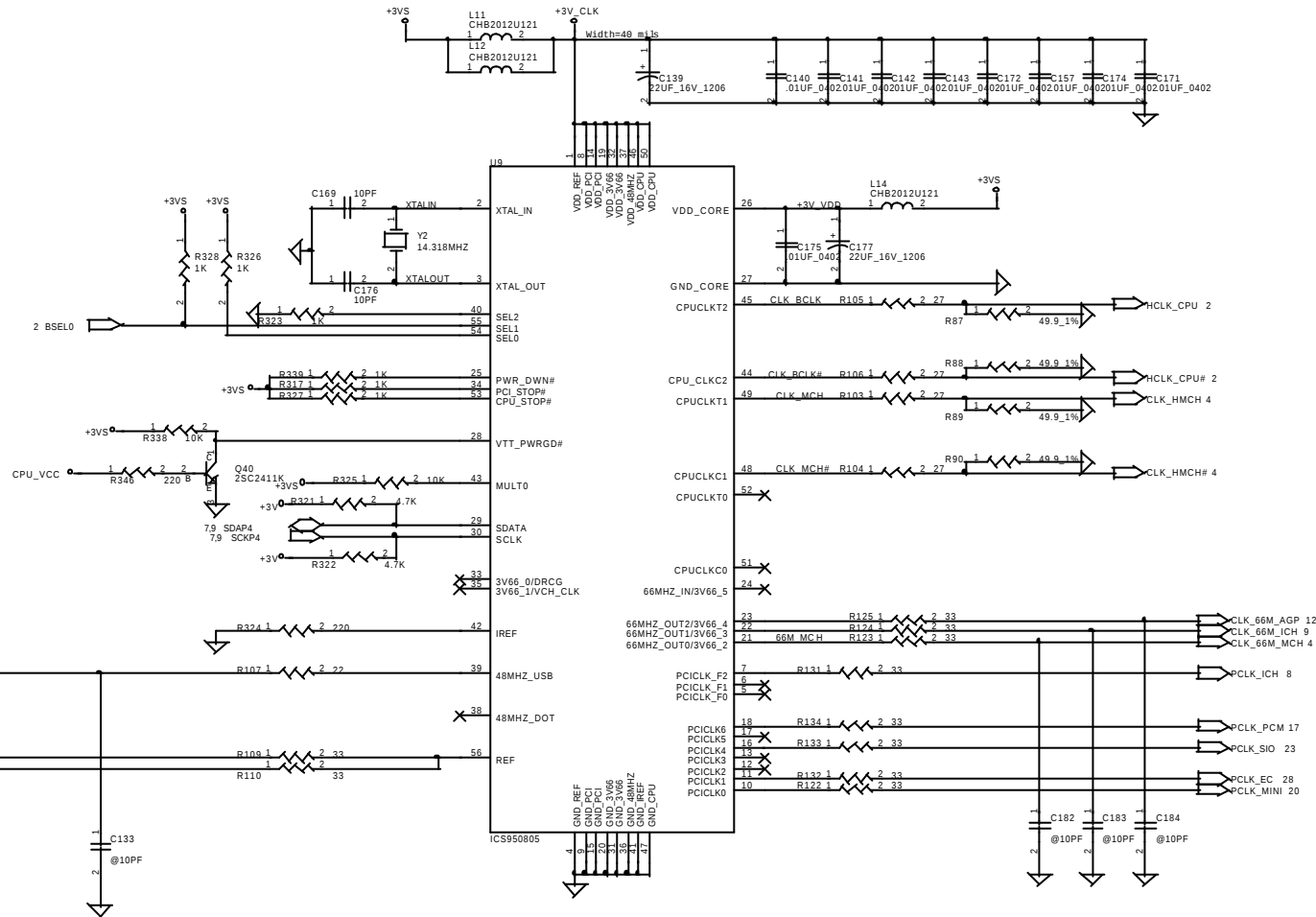
ICH2-C(LAN,Power)



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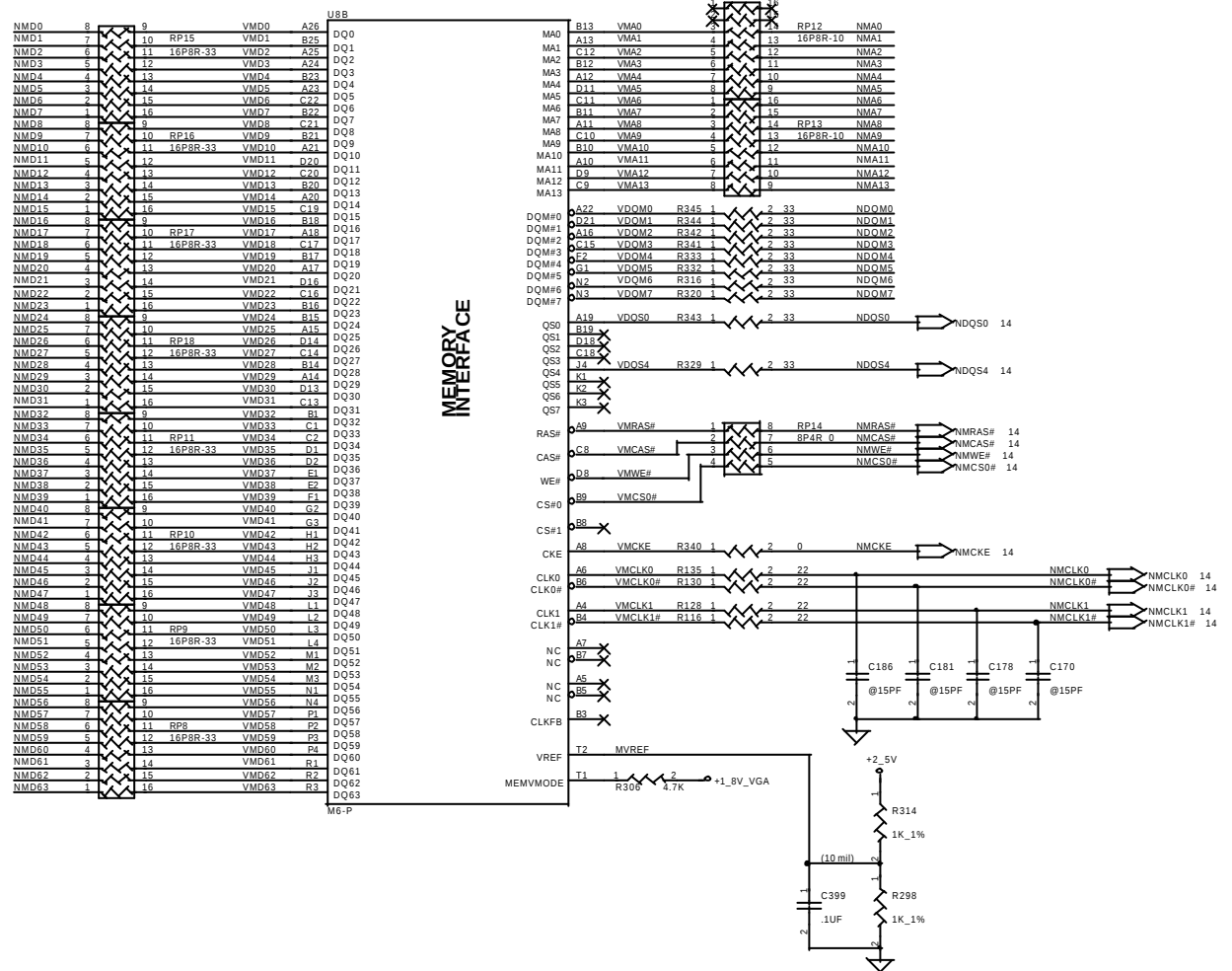
Clock Generator



SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	66.67	66.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

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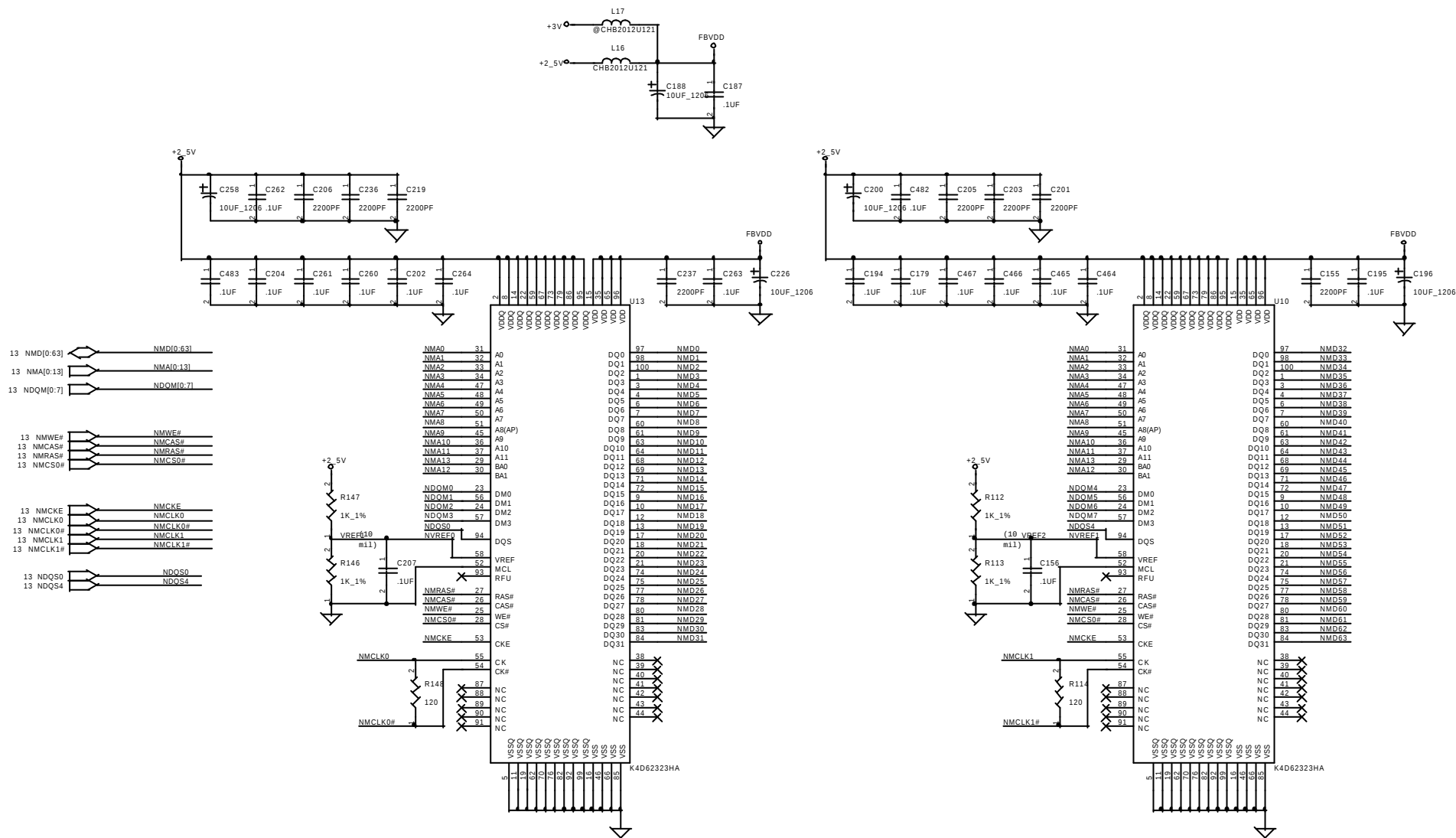
MEMORY INTERFACE



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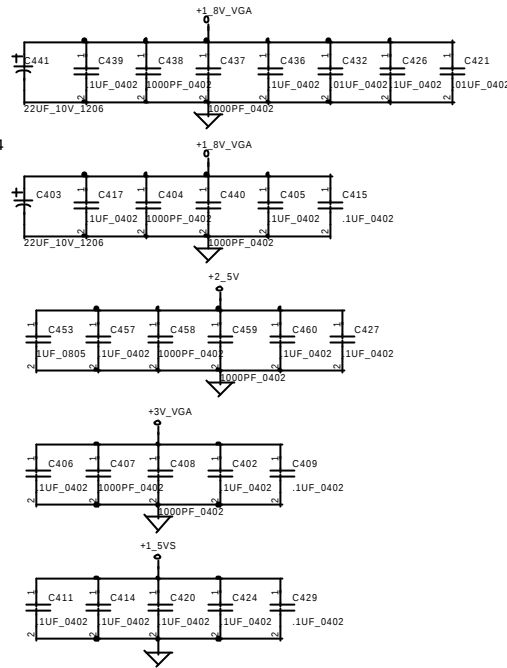
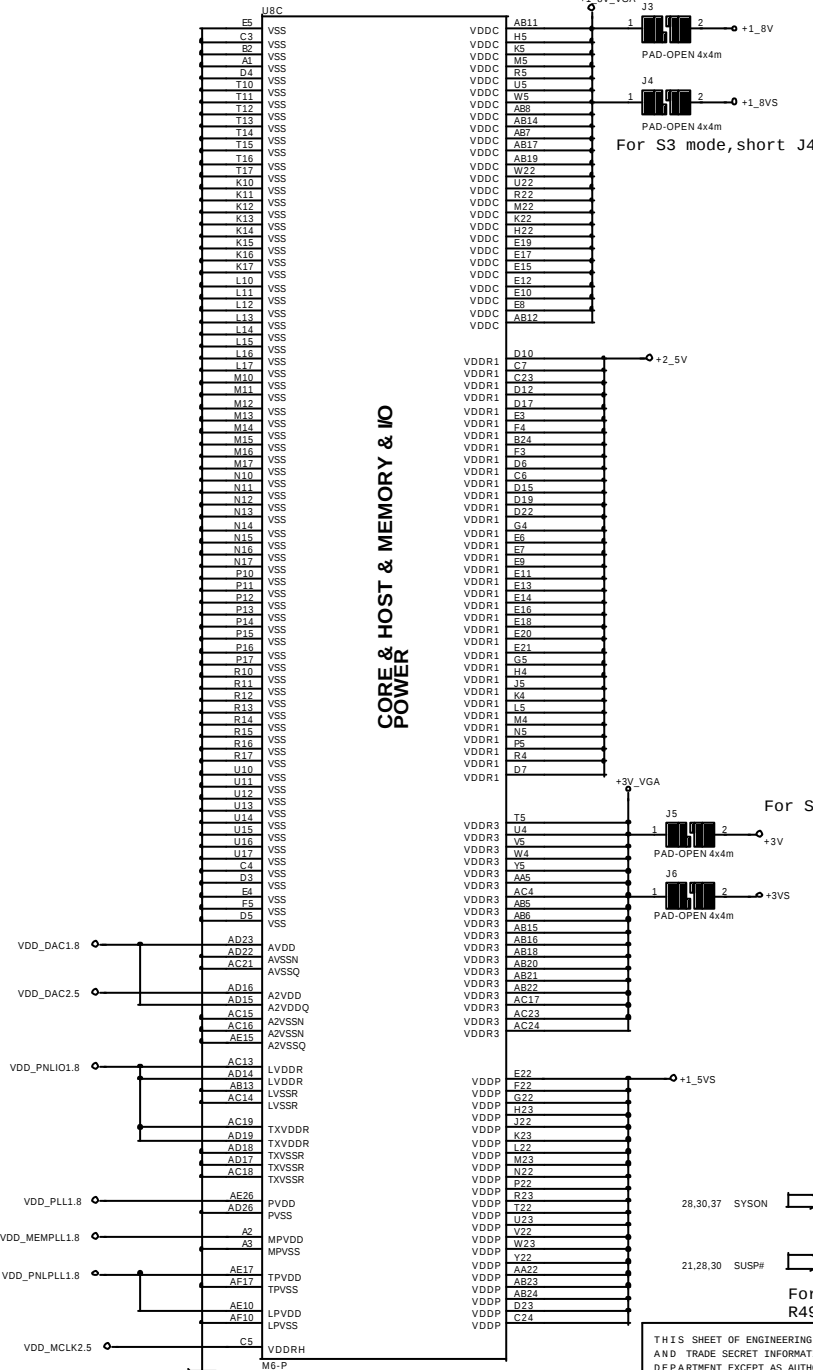
DDR SDRAM



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CORE & HOST & MEMORY & IO POWER

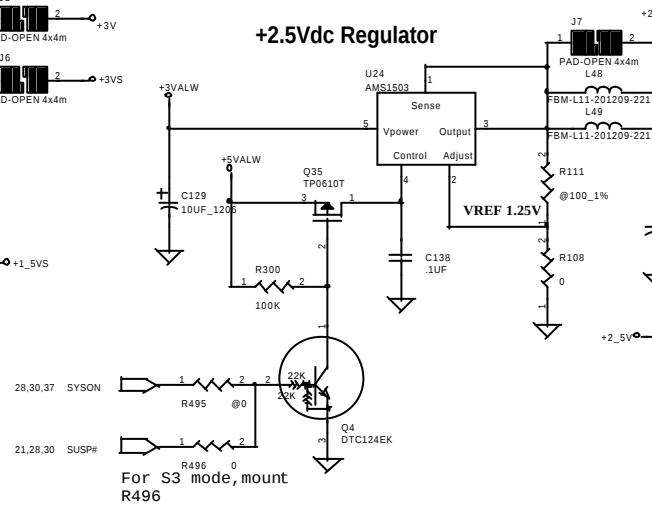


POWER INTERFACE

For S3 mode, short J4

For S3 mode, short J6

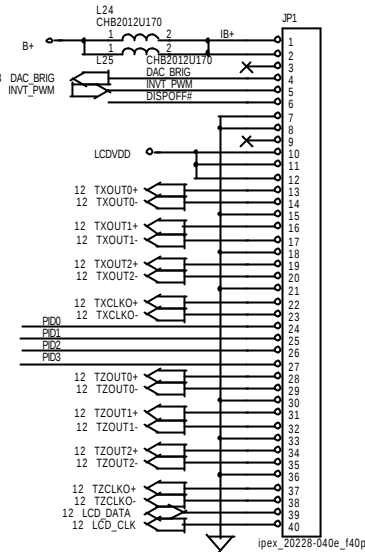
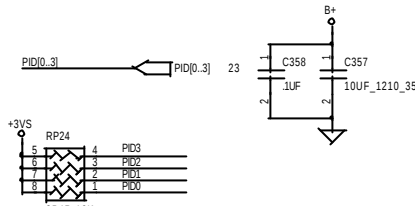
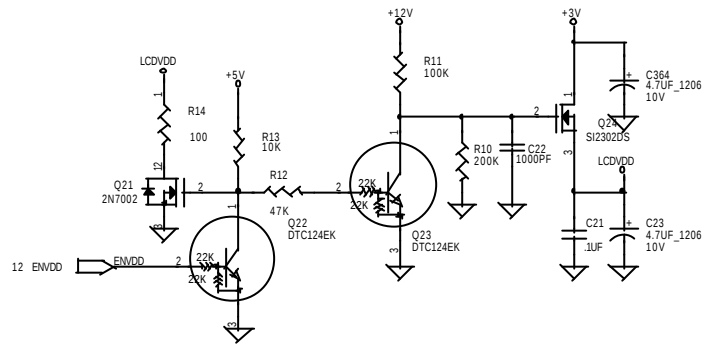
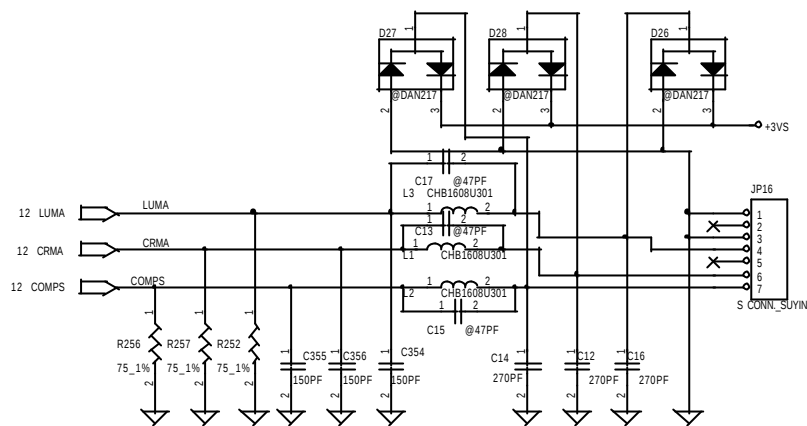
+2.5Vdc Regulator



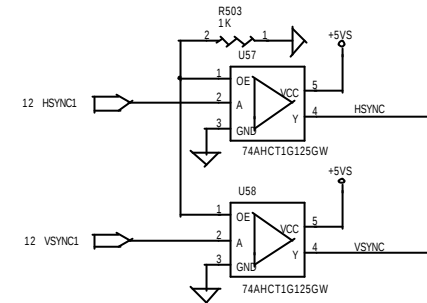
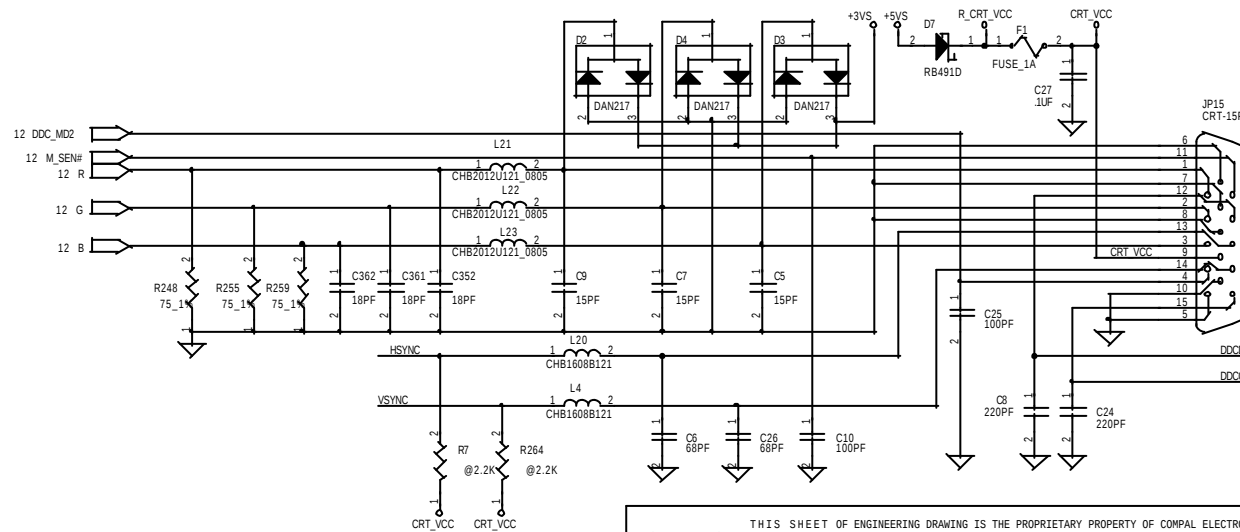
For S3 mode, mount
R496

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CRT Connector



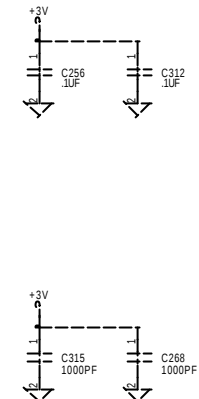
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CARDBUS PCI1420



Power

PCI Interface

Slot B

Slot A

IRQ/DMA

GND

Compal Electronics, Inc.

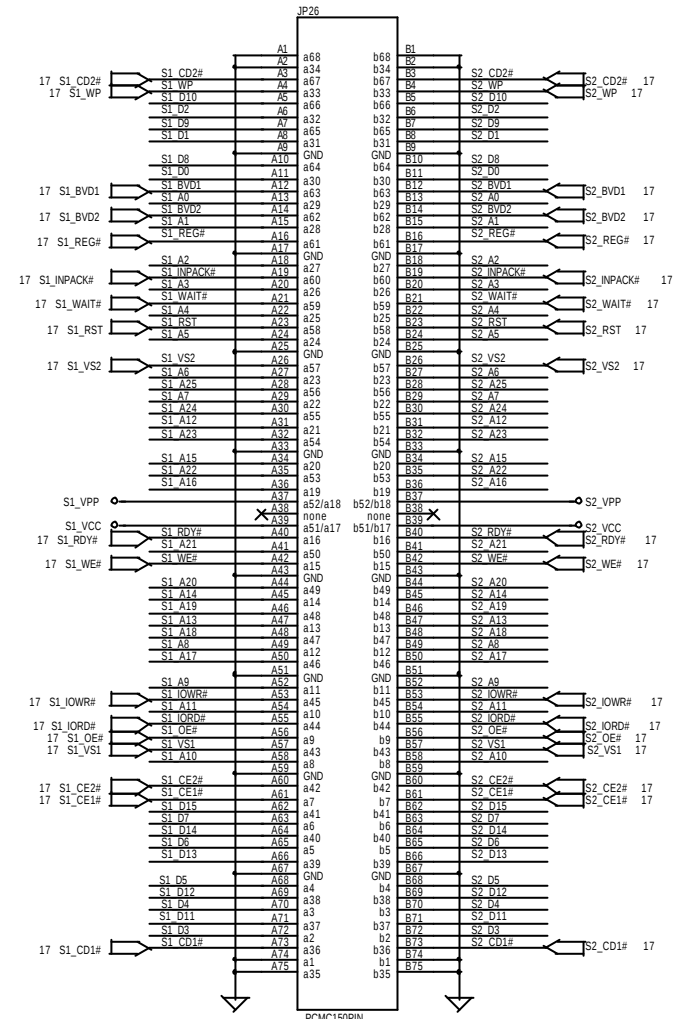
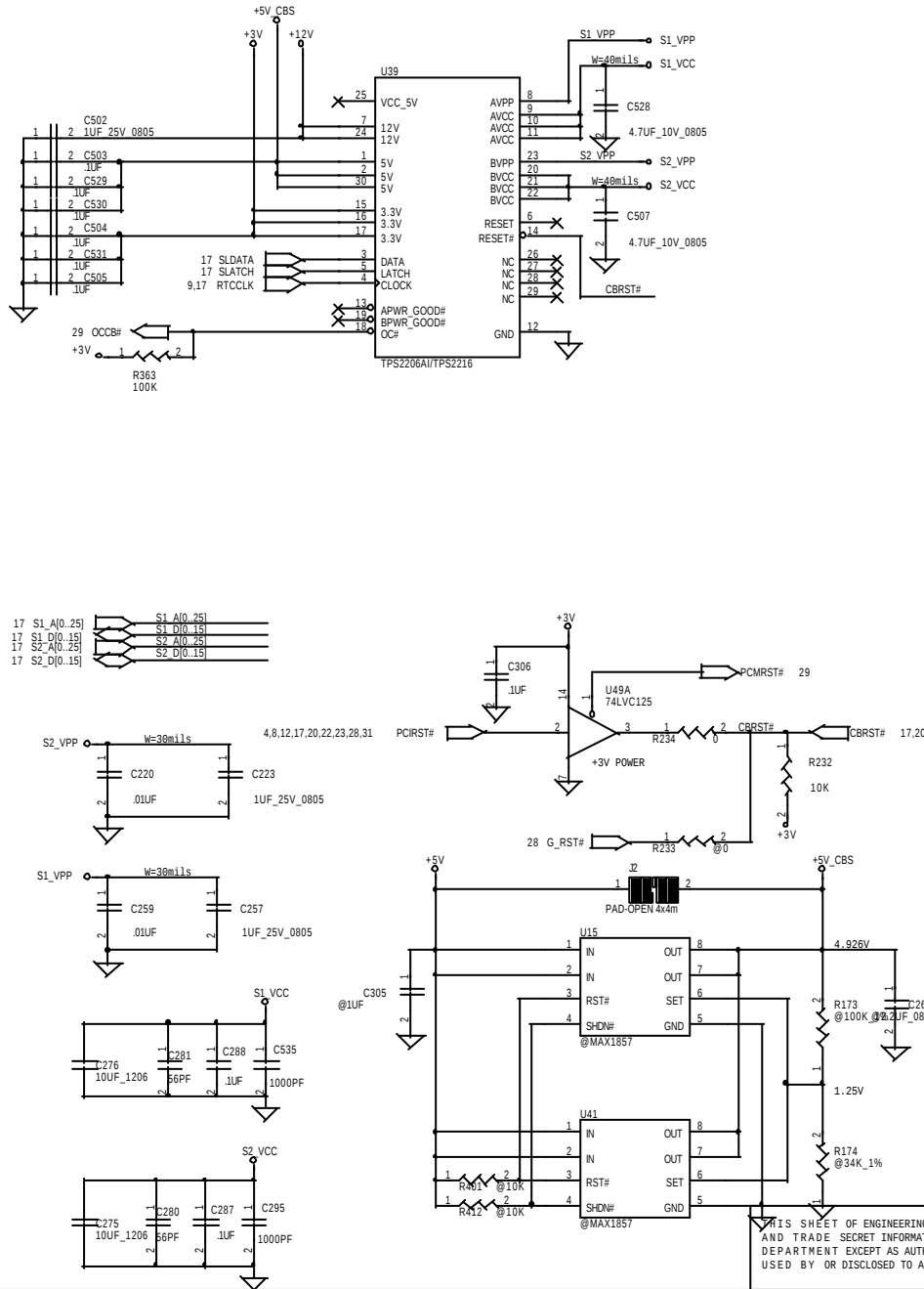
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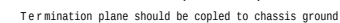
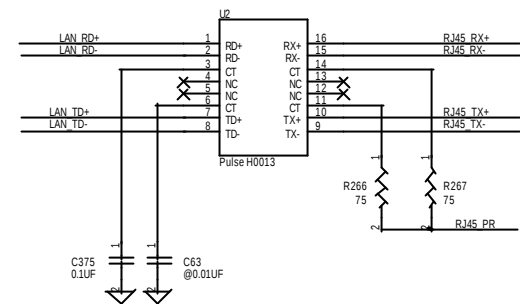
PCMCIA POWER CTRL.

CARDBUS SOCKET

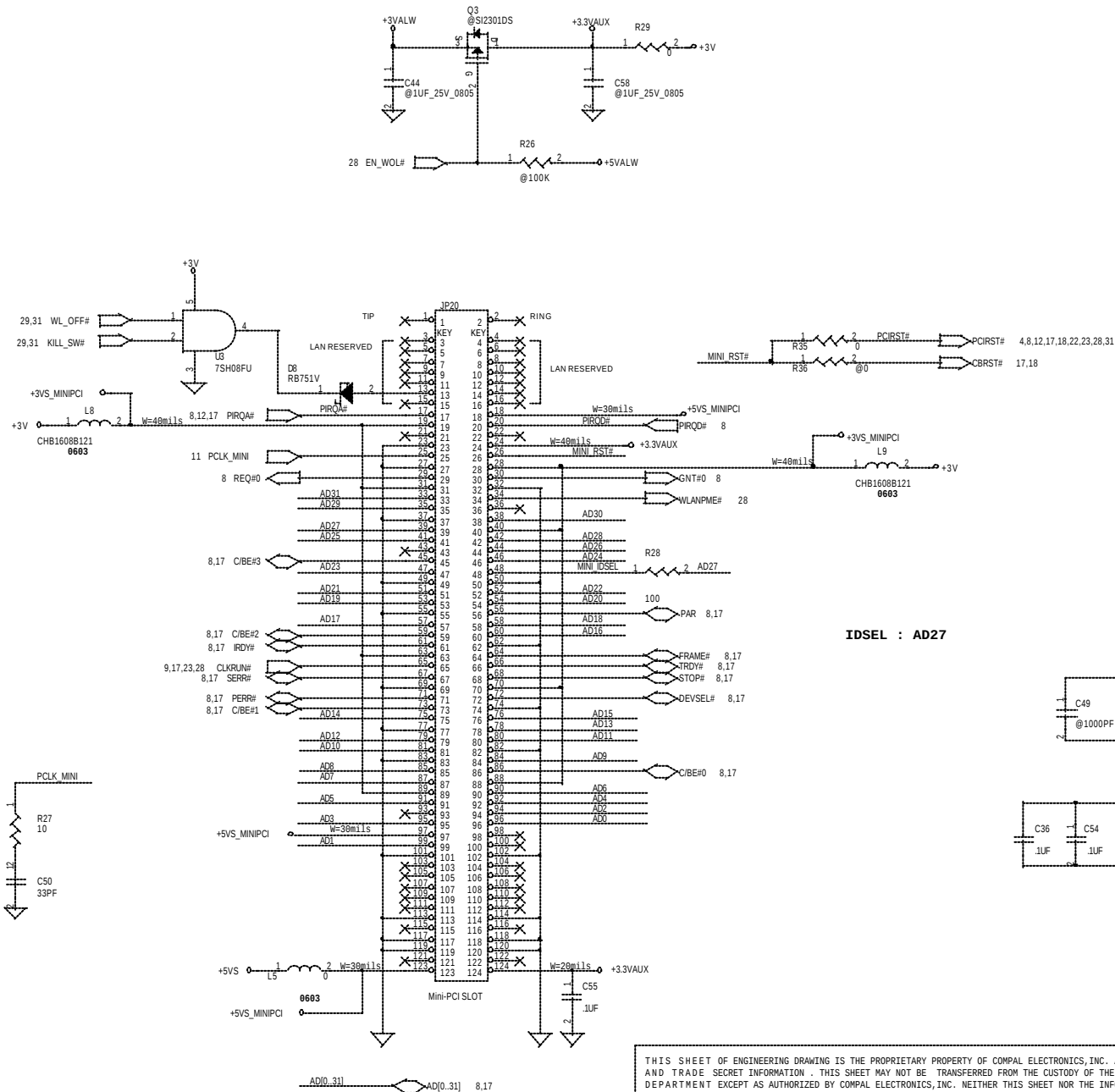


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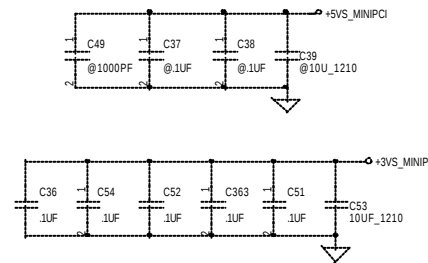
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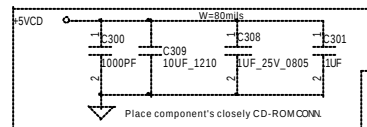
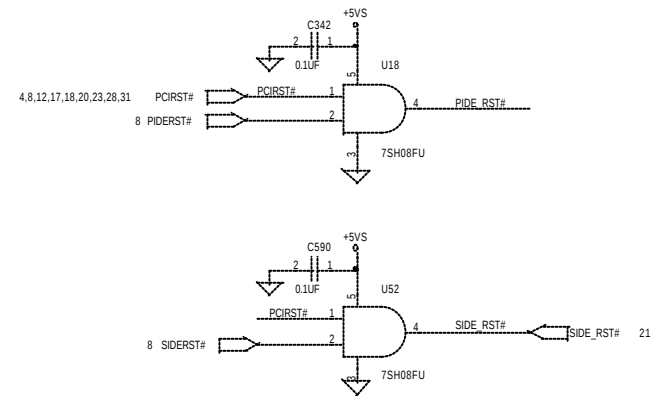
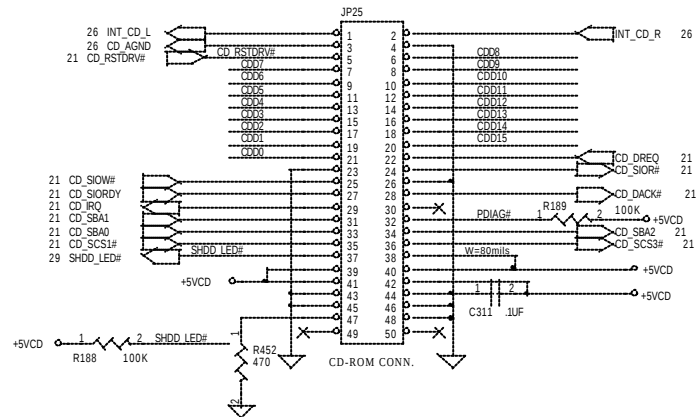
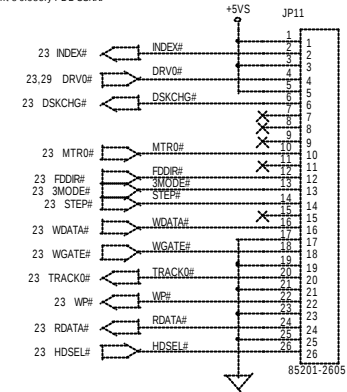
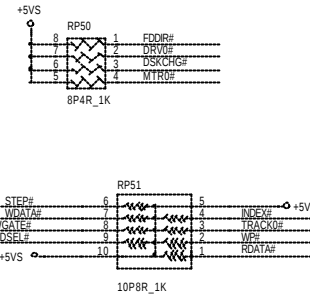
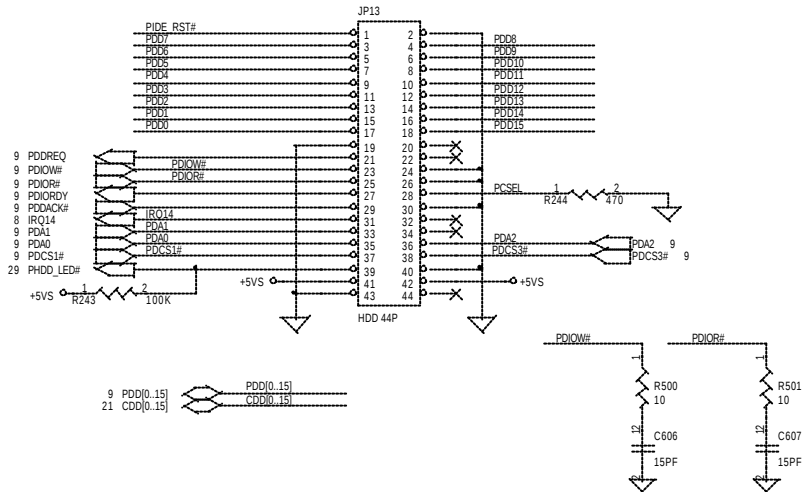
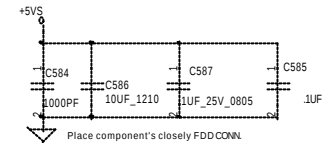
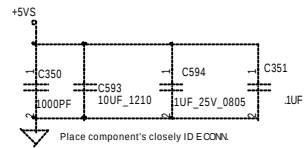
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IDE,CD-ROM Module CONN.



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Compal Electronics, Inc.

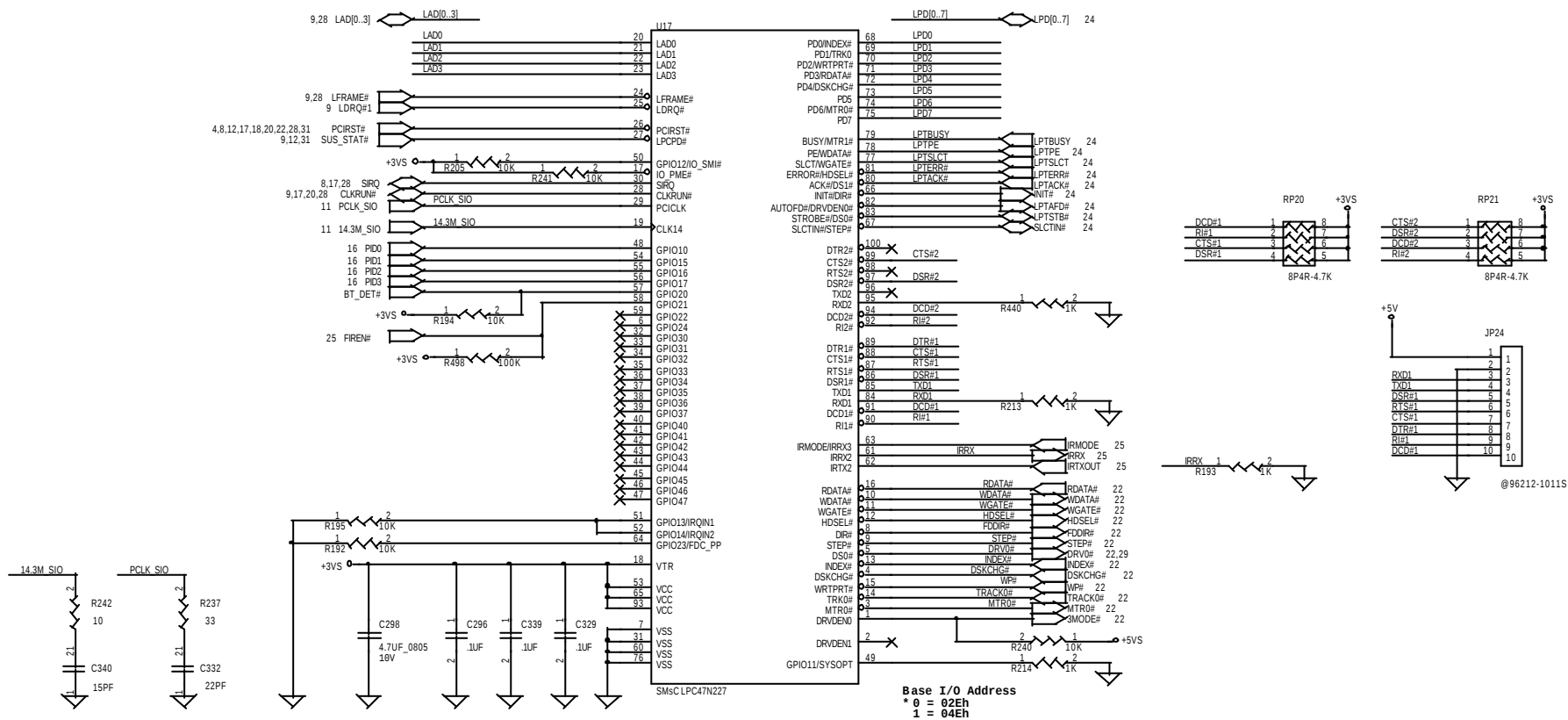
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SUPER I/O SMsC FDC47N227



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Compal Electronics, Inc.

SCHEMATIC, M/B LA-1252

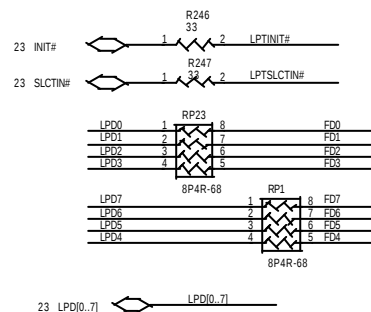
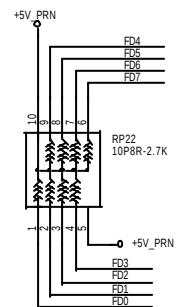
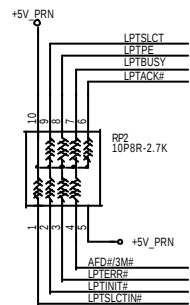
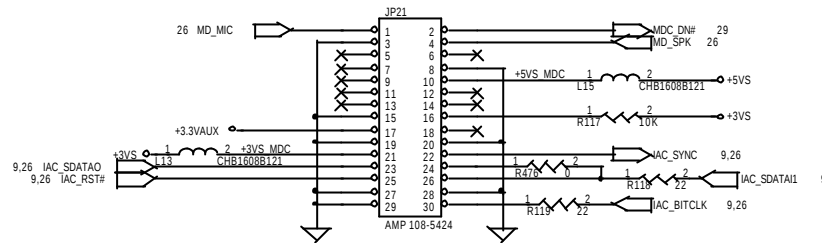
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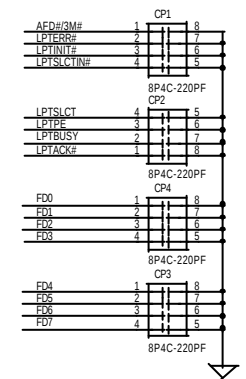
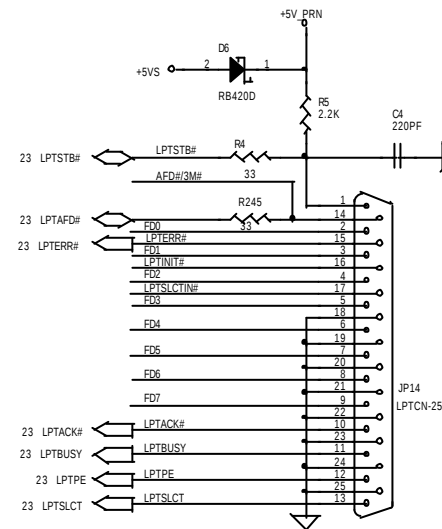
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PARALLEL PORT



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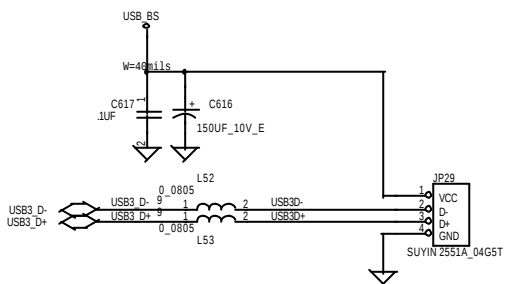
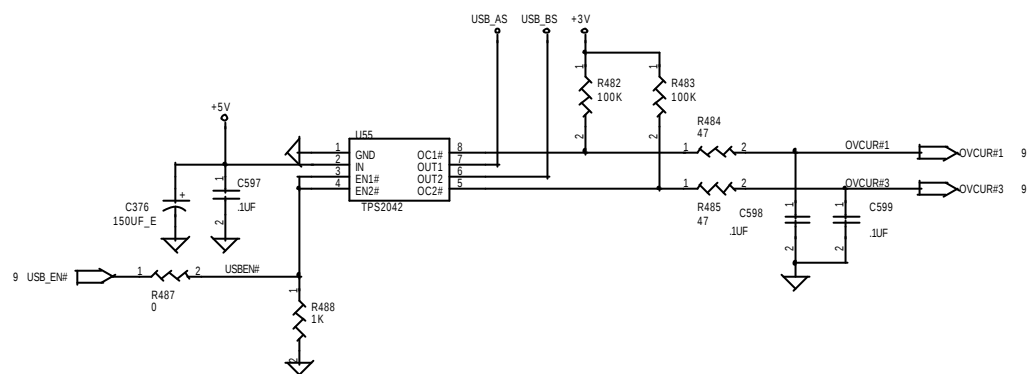
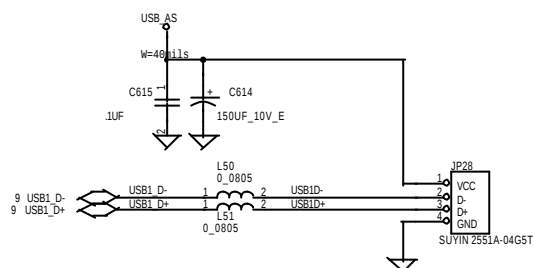
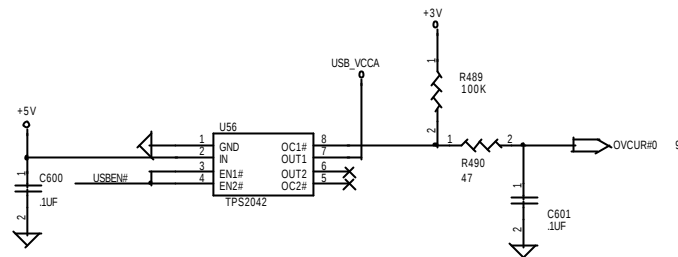
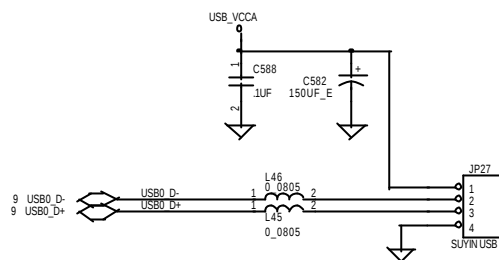
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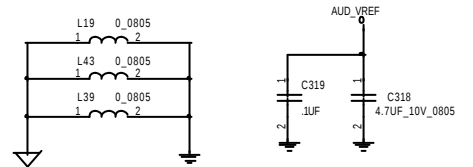
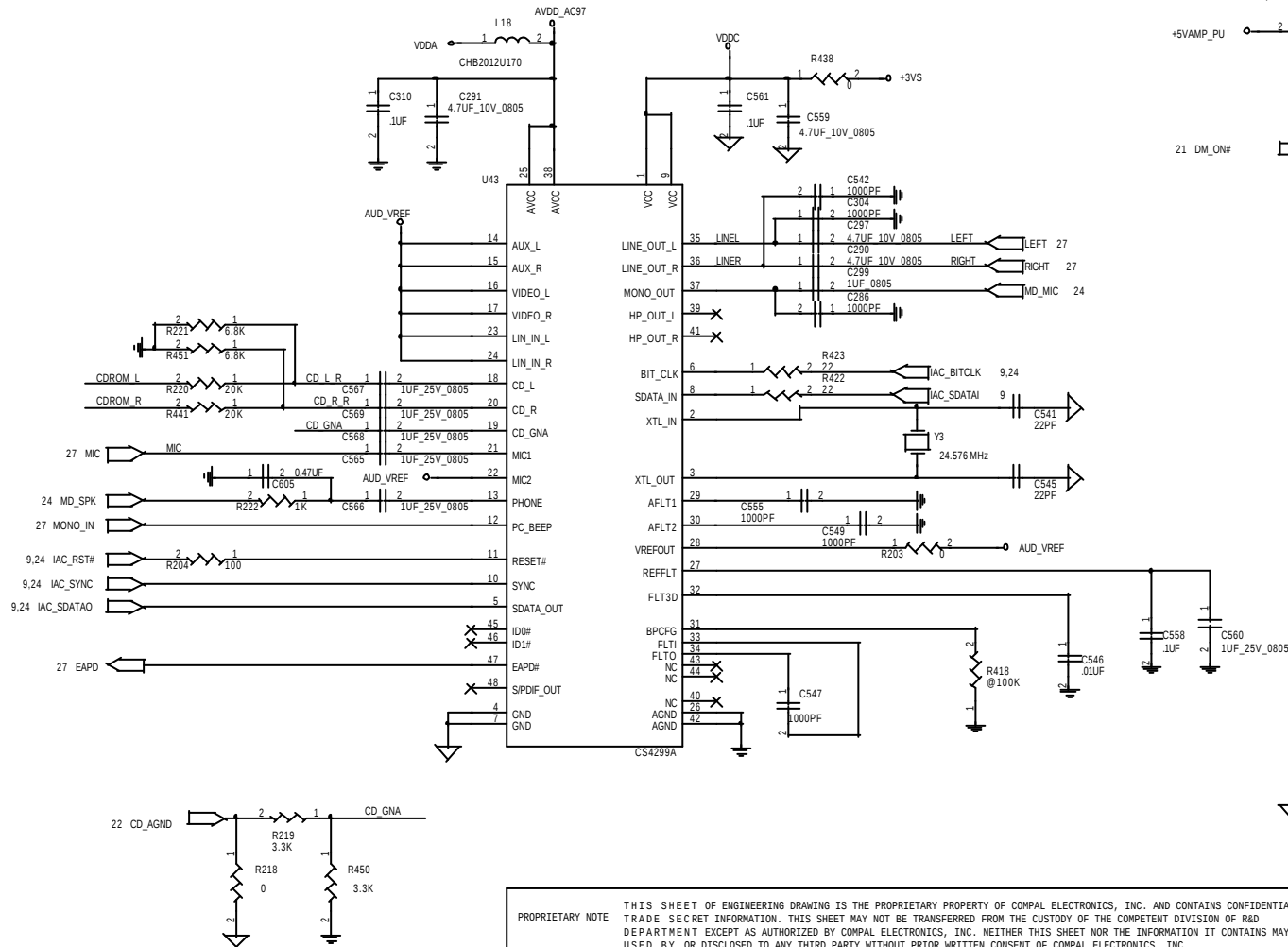
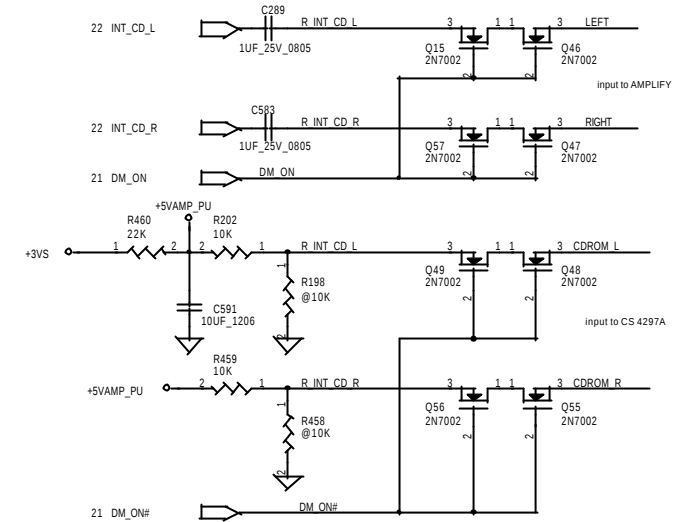
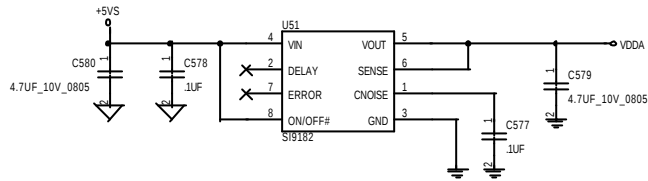


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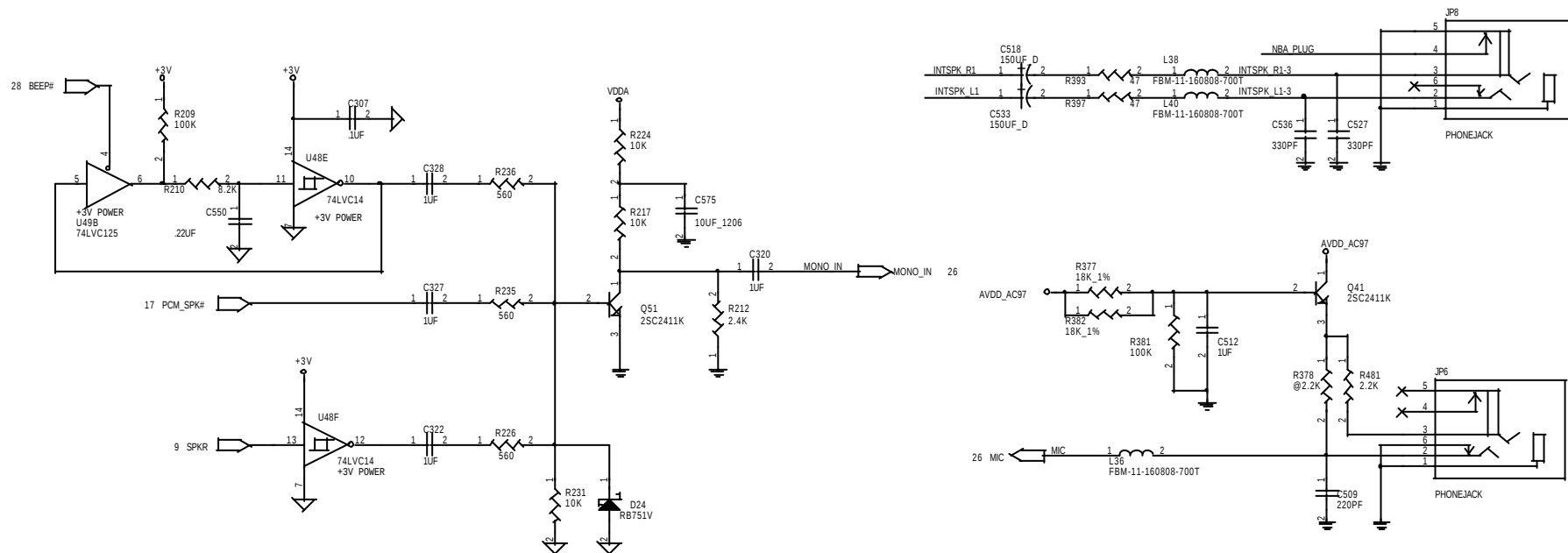
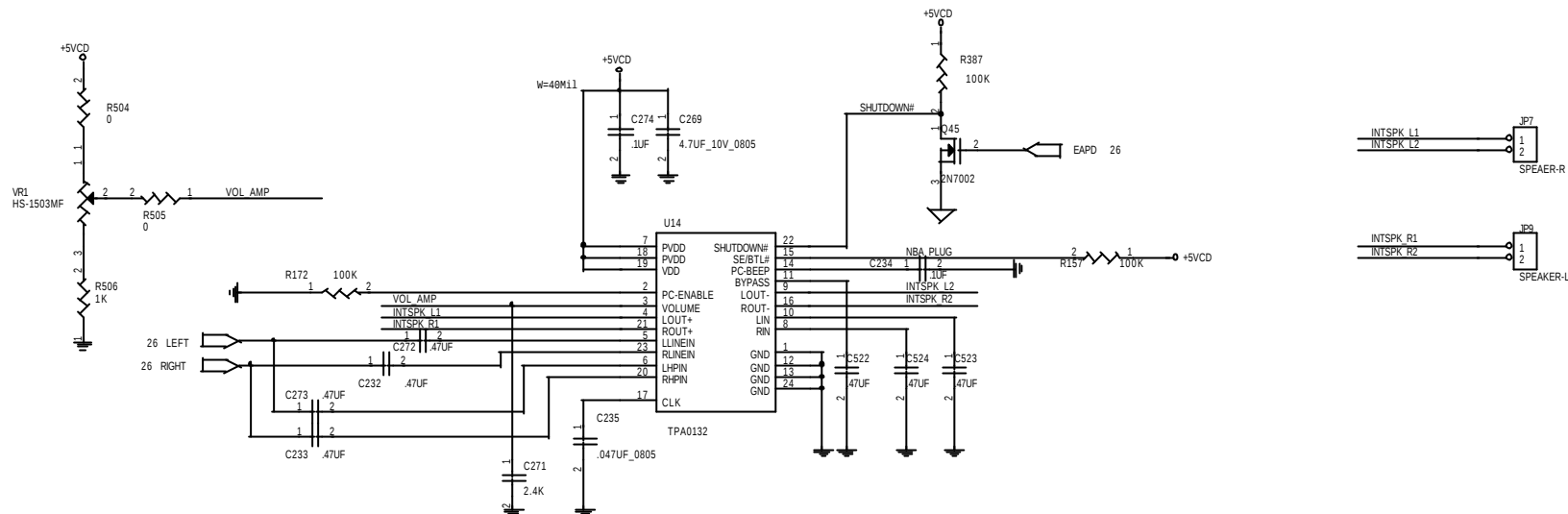
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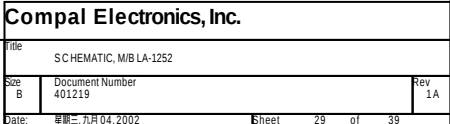
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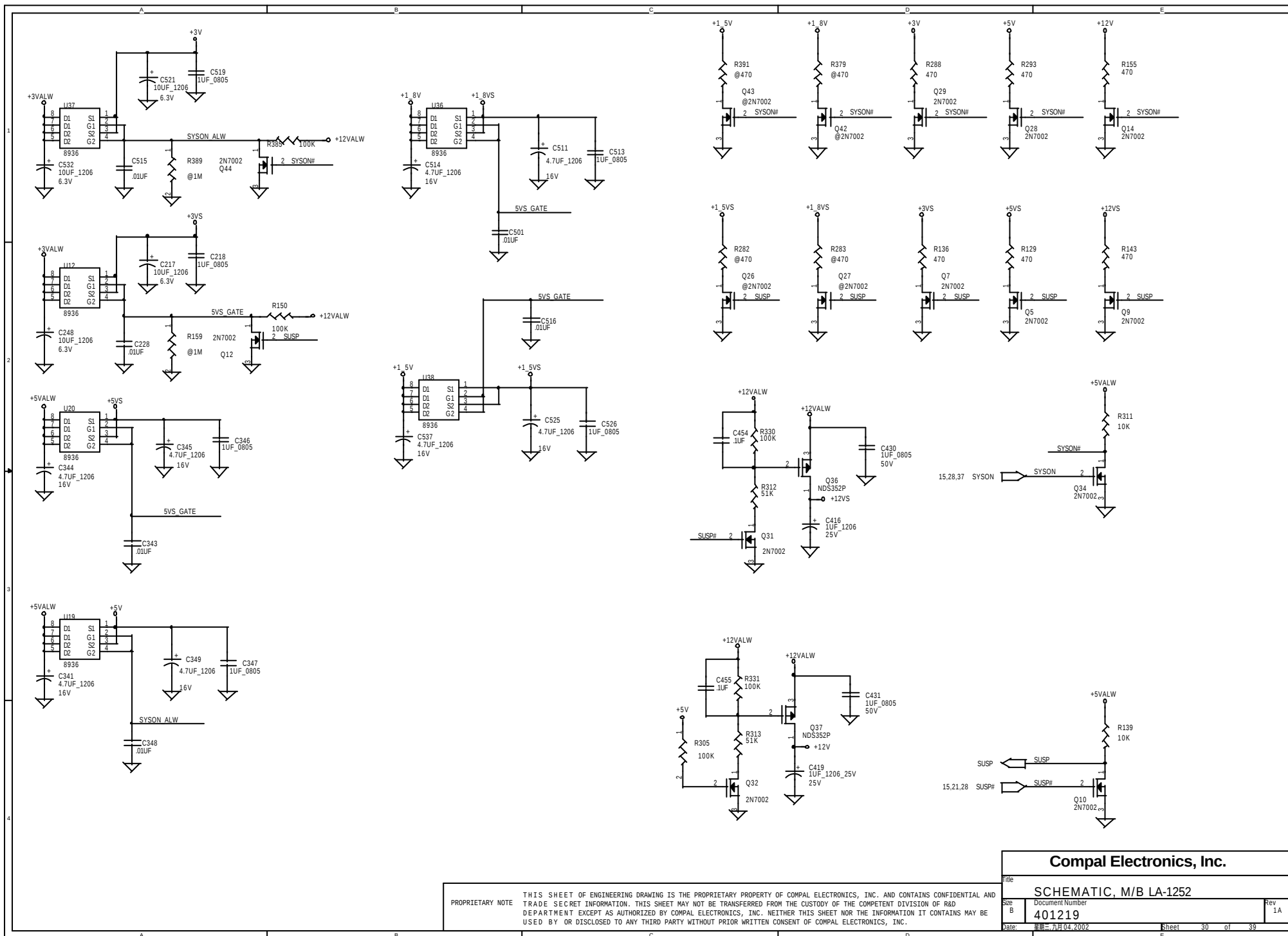


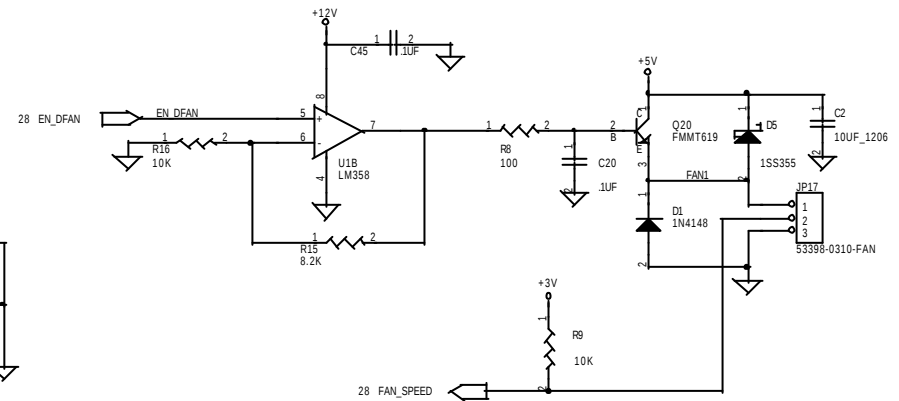
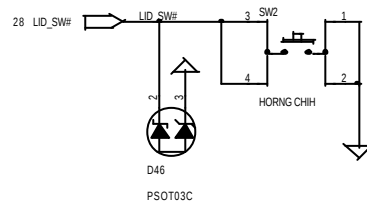
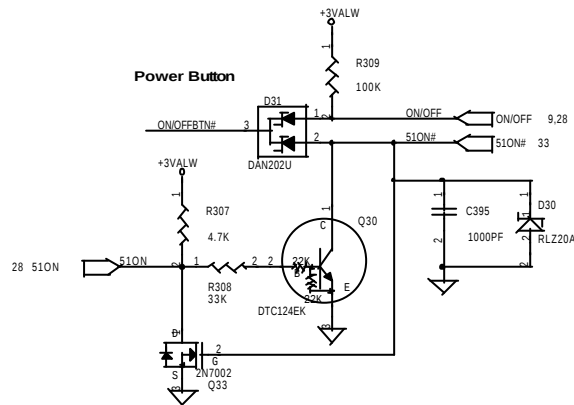
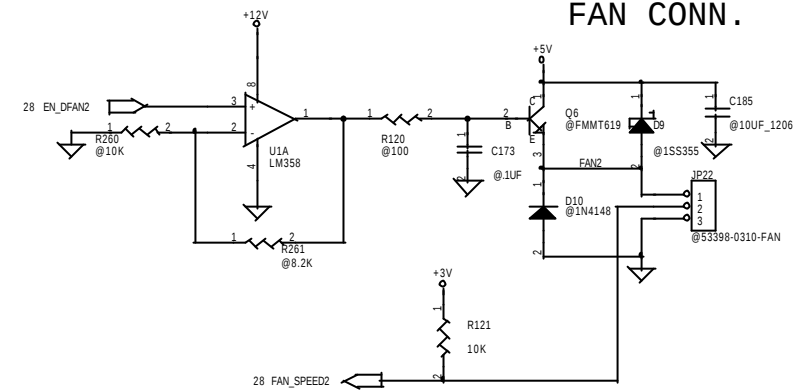
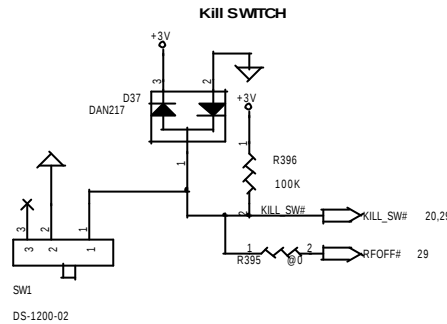
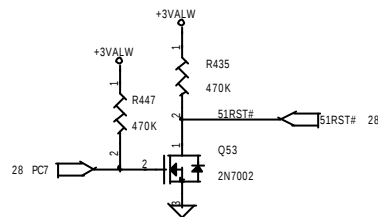
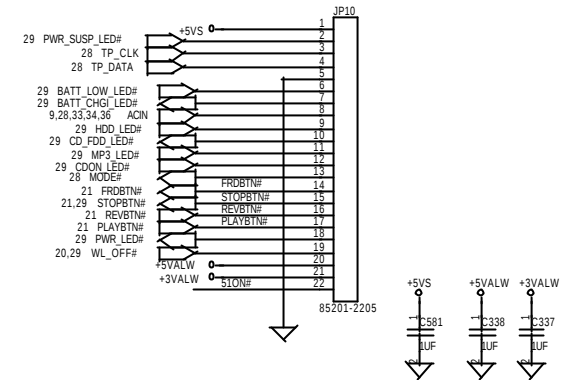
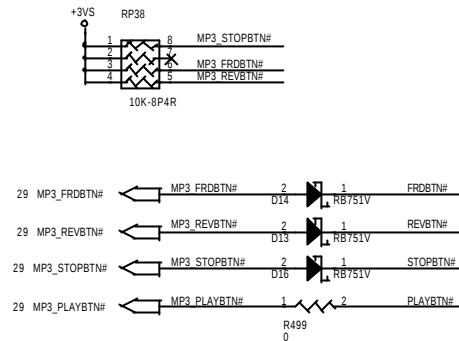
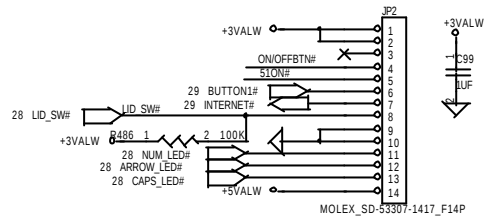
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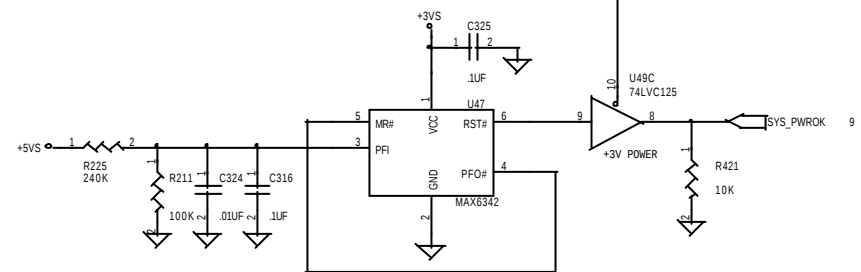
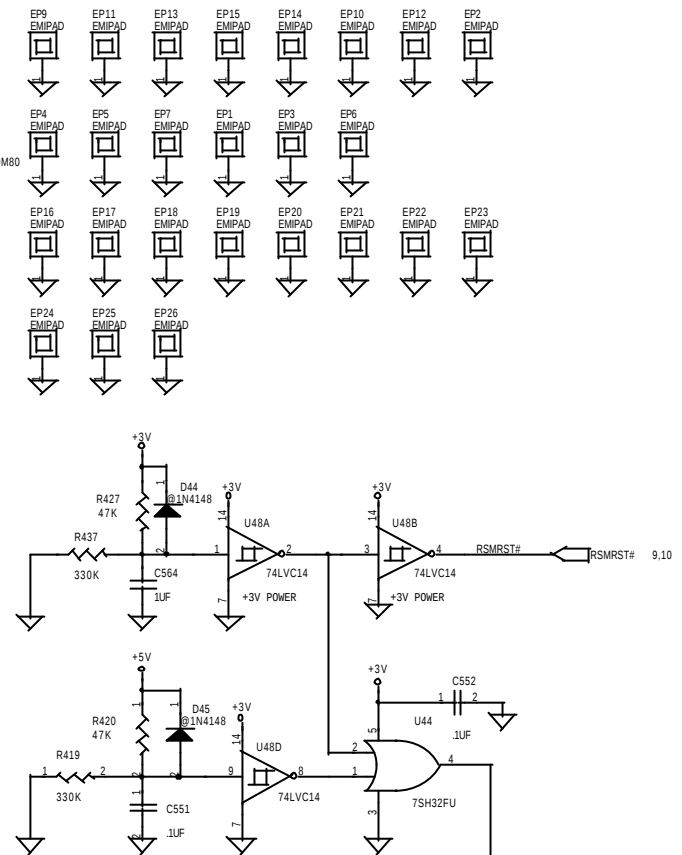
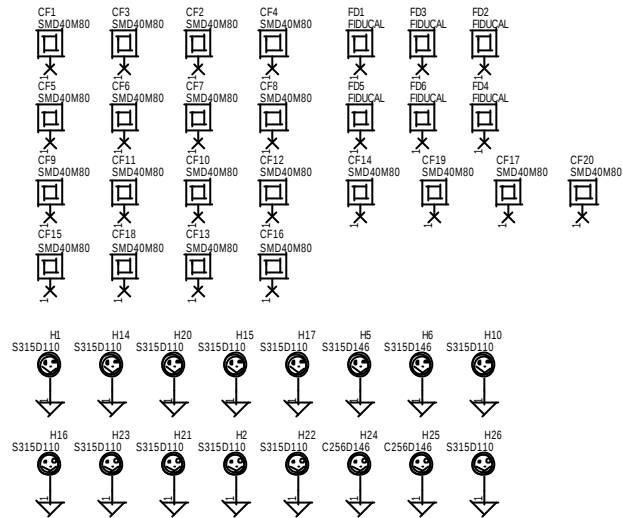
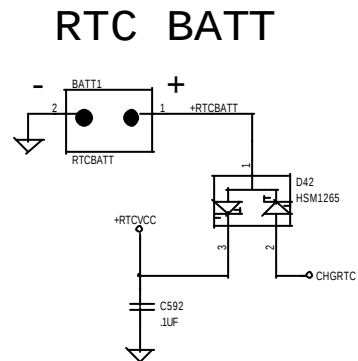


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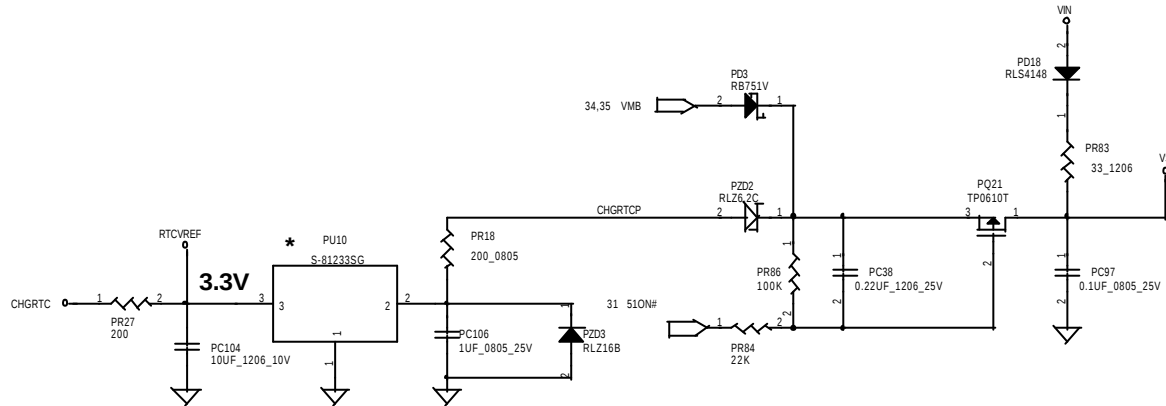
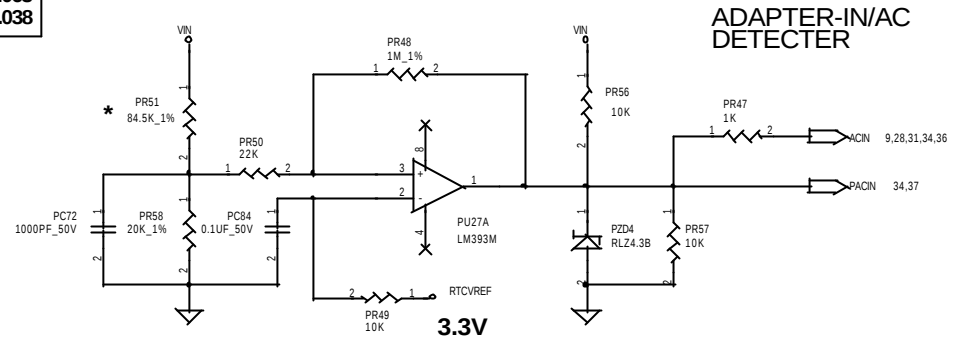
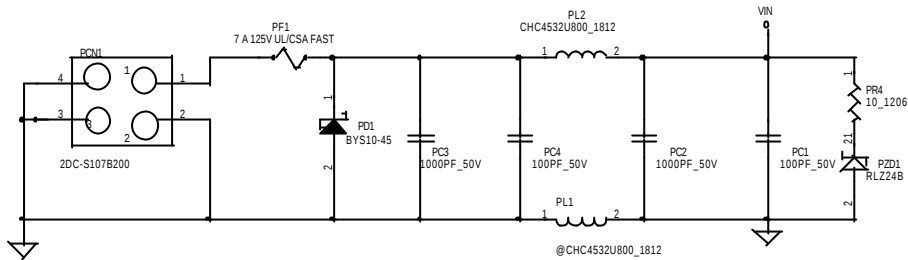
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Vin Detector

High 18.764 17.901 17.063
Low 17.745 16.903 16.038



+1.8VP 1 2 (3A,120mils ,Via NO.= 6)

+12VALWP 2 1 (120mA,20mils ,Via NO.= 1)

+5VALWP 1 2 (5A,200mils ,Via NO.= 10)

+3VALWP 1 2 (5A,200mils ,Via NO.= 10)

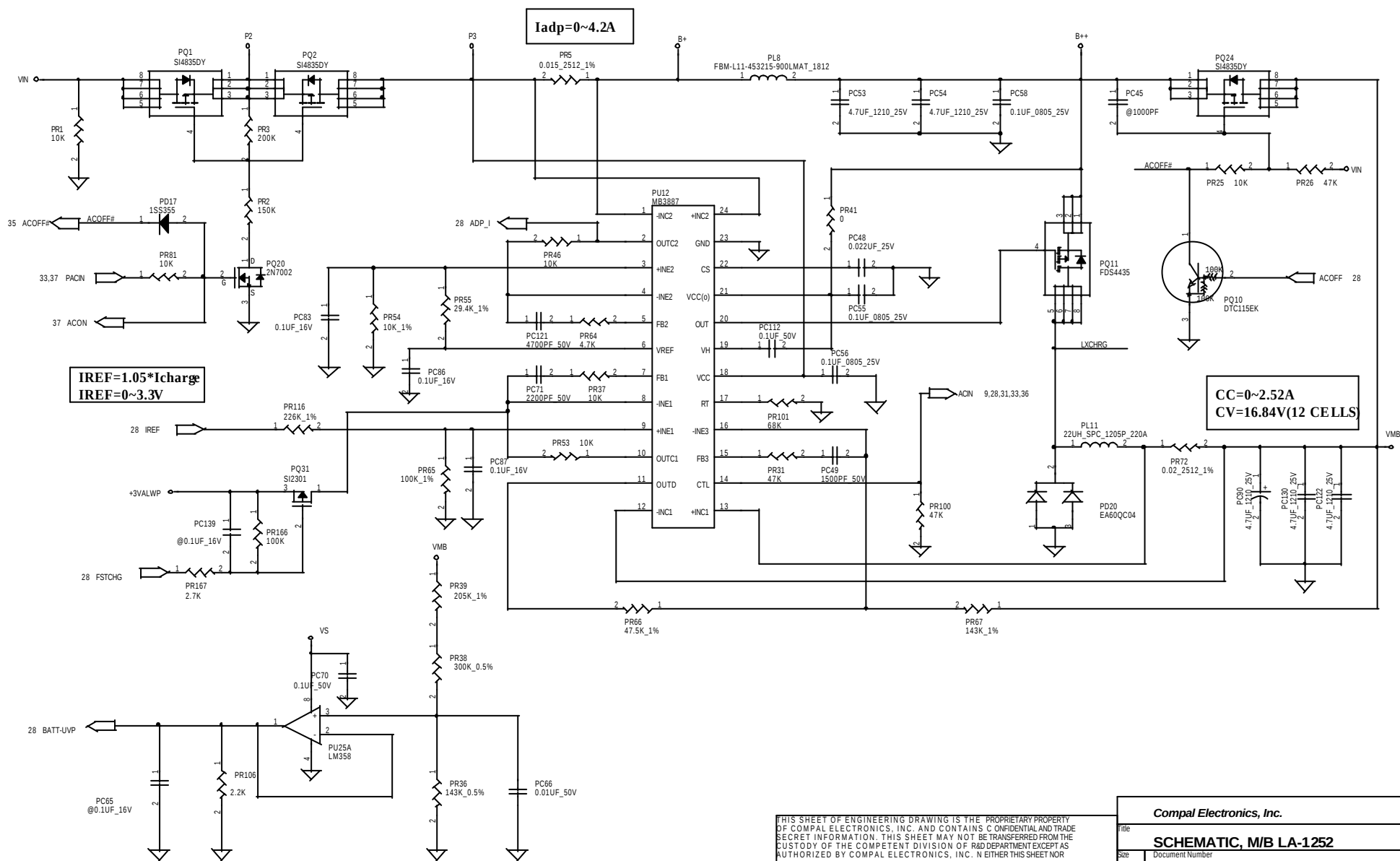
+1.5VP 2 1 (3A,120mils ,Via NO.= 6)

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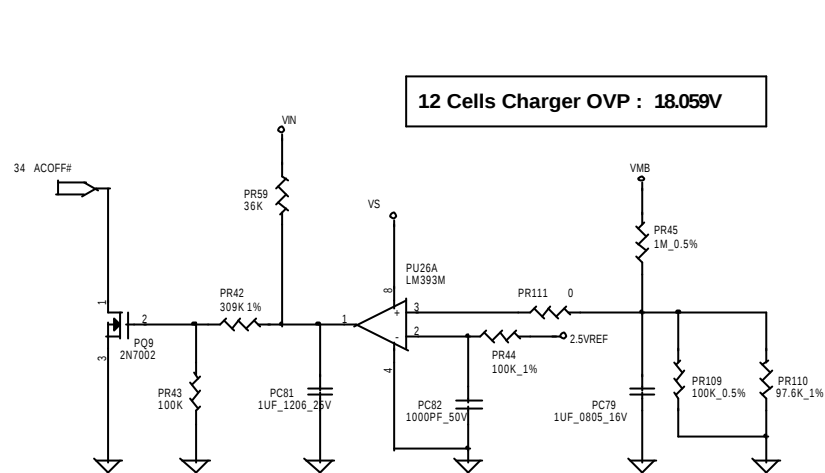
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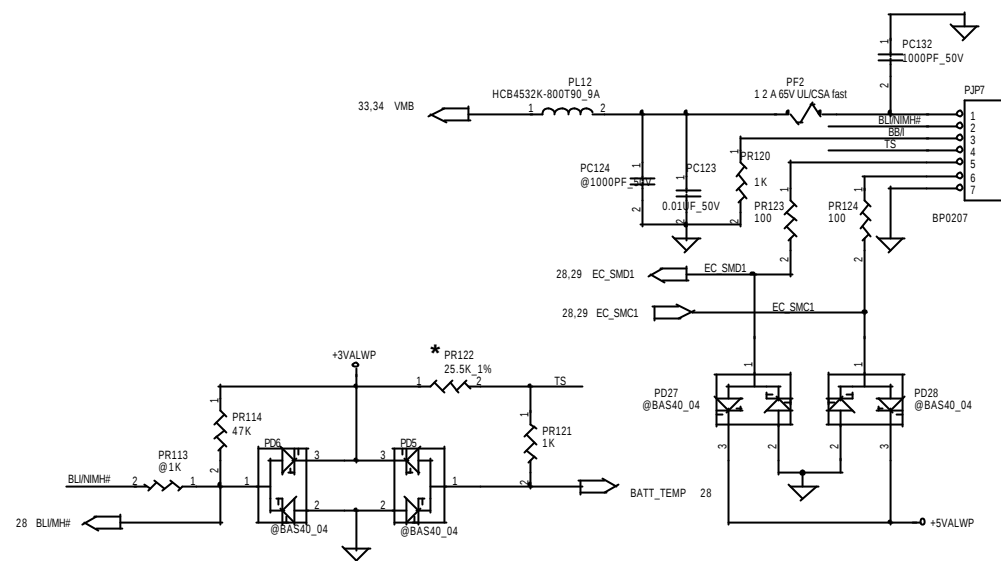
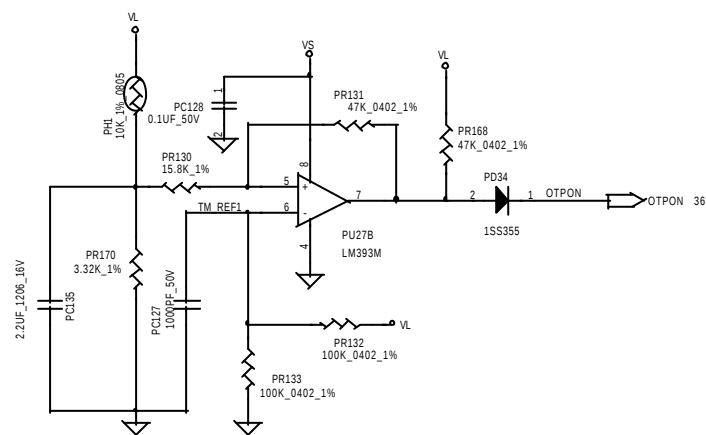
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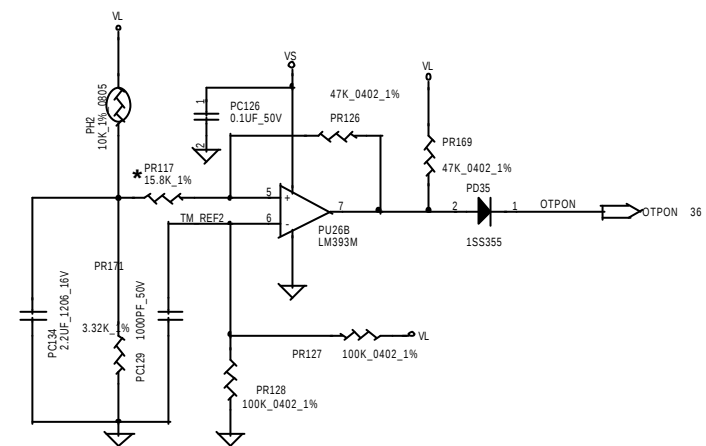
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PH1 under CPU bottom side :
CPU thermal protection at 82 degree C
Recovery at 50 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 82 degree C
Recovery at 50 degree C



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+3.3V/+5V/+12V

+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

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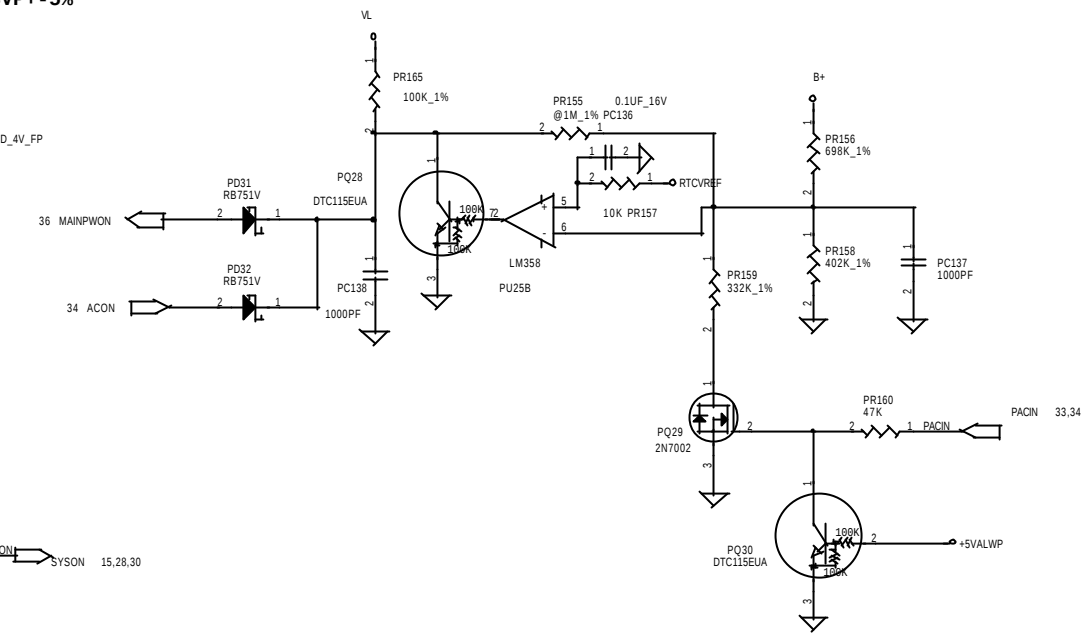
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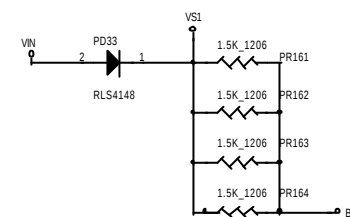
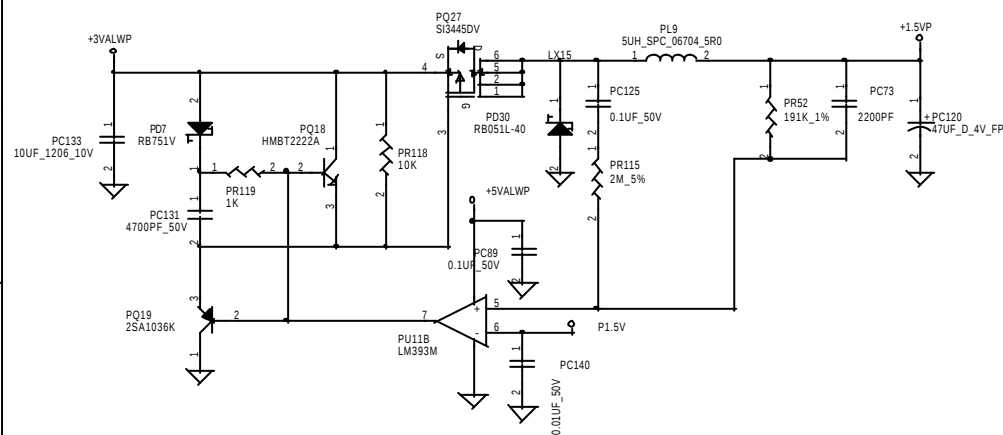
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1.8V/1.5V

+1.8VP+-5%



+1.5VP+-5%

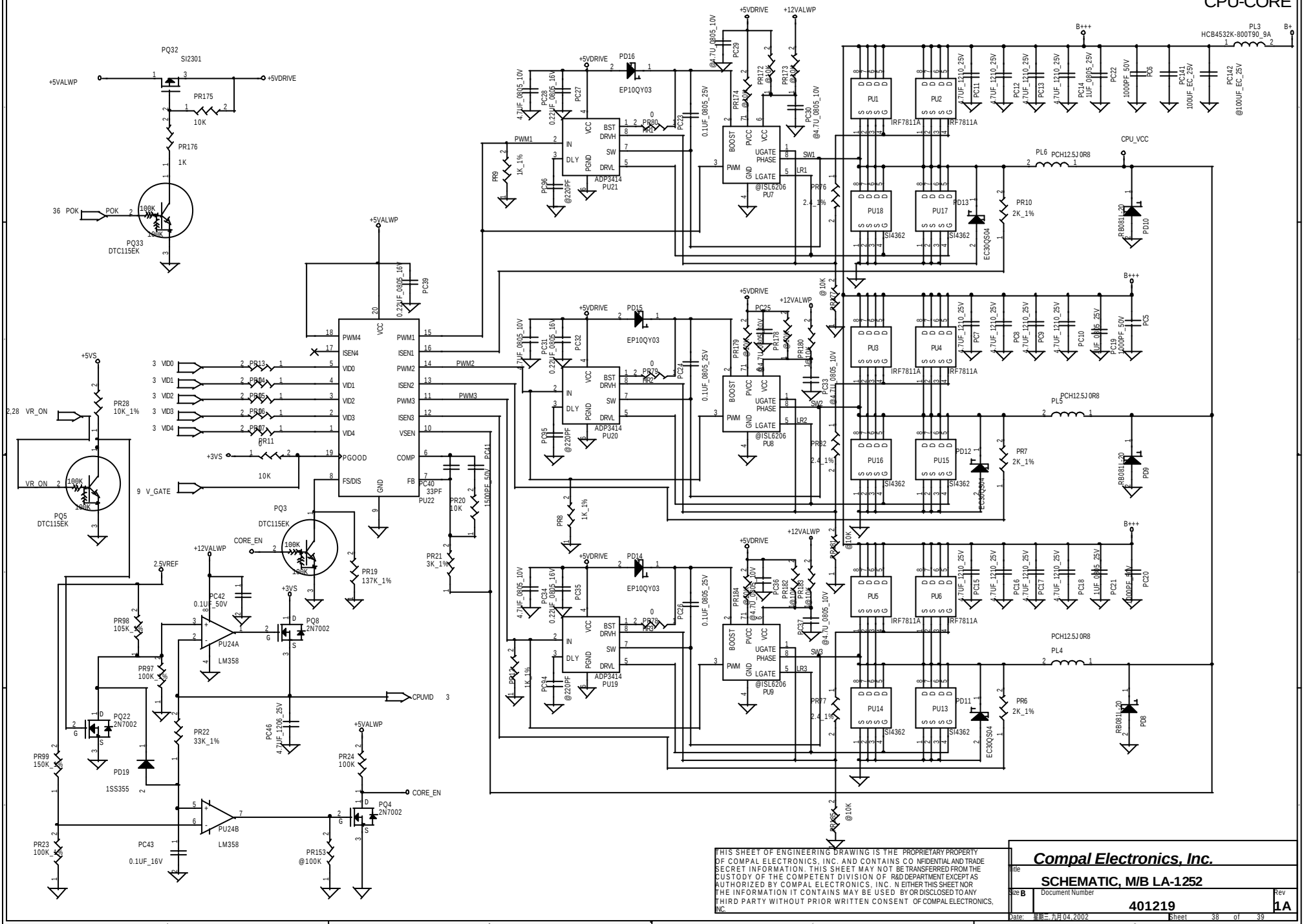


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CPU-CORE



ACR10 PIR LIST

HW PIR LIST

PWR PIR LIST

ATEST 9/6~

1	+2.5V LEVEL ERROR	Remove R111 100ohm Change R108 from 100 to 0 ohm	P15
2	SDRAM BANK select error	Change CLK_SDRAM3 from U22.F3 to U22.E3 Change CLK_SDRAM5 from U22.H5 to U22.G5 Change RRAS#3 from U22.H7 to U22.F7 Change RRAS#5 from U22.G6 to U22.H6	P5
3	Add CPU VCCVID pin	Add R492 connect to U23.AF3	P3
4	TV OUT output error	Change CRMA from U8.AF15 to U8.AF16 Change LUMA from U8.AF16 to U8.AF15	P12
5	Add MK1787 output terminate	Add R494 22 ohm	P12
6	Add low pass filter for MK1787 power pin	Add L47	P12
7	Change VGA option resistor to jumper	Change R284 to J3 Change R286 to J4 Change R295 to J5 Change R296 to J6	P15
8	Reserve +2.5V option control	Add R495 for SYSON control Add R496 for SUSP control	P15
9	Change LCD connector type	Change JP1	P16
10	Add TI TPS2042 for USB protect circuit	Add U56(TPS2042)	P25

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