ZC3 BLOCK DIAGRAM

AMD K8/RX485/SB460 REV:B

BOM
VRAM@ ->(Samsung,Infineon,Hynix)
UC@ ->(ATMEL,SST)
MEMID@ ->(Samsung,Infineon,Hynix)
2@ ->Add second source

SYSTEM POWER MAX1999 Page 44
CPU CORE(MAX8774) Page 41
+1.2V/+1.5V/+2.5V Page 42
+1.8V / VGA_CORE Page 43,46
DISCHARGE CIRCUIT Page 44

CPU THERMAL SENSOR Page 13

AMD S1 Turion 64
(638 S1g1 socket)
Page 3,4,5,6

DDR II 533,667MHz

DDR II-SODIMM1 Page 7,8
DDR II-SODIMM2 Page 7,8

Clock GEN
ICS951462
Page 2

HOST 133/166MHz
PCIE 100MHz
VGA 96MHz
USB 48MHz
PCI 33MHz
REF 14MHz

HyperThansport I/O BUS
LINK 16X16

NORTH BRIDGE
RX485
465 FCBGA
Page 9,10,11,12

PCIE 16X

ATI M56-P
Page 18,19,20,21,22,24

VRAM X4
(GDDR3 500MHZ)
Page 23

R,G,B — CRT port Page 26
LCD — LCD CONN Page 25
TV-OUT — S-VIDEO Page 25
TMDS — HDMI Page 34

DOCKING PORT Page 32 — 2X PCI-E 0,1
Mini Card/WLAN Page 29 — 1X PCI-E 3
New Card Page 33 — 1X PCI-E 2
USB 2.0 * 1(USB5)

A-LINK

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLOCK
TI 7412	AD25	REQ0# / GNT0#	INTE#,F#,G#	PCICLK2
BCM5788M	AD20	REQ2# / GNT2#	INTH#	PCICLK5

USB PORT X4 Page 29 — USB 2.0 * 4(USB0 ~ 3)
BLUETOOTH Page 29 — USB 2.0 * 1(USB6)
1.3M Camera Module Page 25 — USB 2.0 * 1(USB7)

USB0: M/B IO
USB1: M/B IO
USB2: D/B IO
USB3: D/B IO
USB4:
USB5: NEW CARD
USB6: BLUETOOTH
USB7: CAMERA

SOUTH BRIDGE
SB460
549 BGA
Page 14,15,16,17

PCI/33MHz
Azalia

AUDIO CODEC ALC883 Page 36
MDC1.5 MODEM Page 36
CARDBUS/1394/Card reade TI 7412 Page 30,31
Giga LAN Broadcom BCM5788MG Page 27

HP AMP Page 37
SPK AMP Page 37
RJ11 Page 45
PCMCIA Page 31
1394 Page 30
6 in 1 Cardreader Page 31
RJ45 Page 28

HP/ SPDIF Page 37
INT SPK Page 37
Line-in & MIC Page 37

Primary IDE HDD Page 35 — SATA
Media bay CDROM Page 35 — ATA 66/100

RTC Battery Page 14

LPC/33MHZ

EZ4 Docking Connector
PCIE1~2 , Lan
Ser & Par Port
PS2 , VGA, DVI
SPDIF,SM BUS
Page 32

PCI-Express X 2
TV out / CRT — Switch Page 25,26
Audio — Switch Page 37
DVI — Switch Page 34
10/100/1G — Switch Page 28

SUPER I/O
PC87383
Page 38

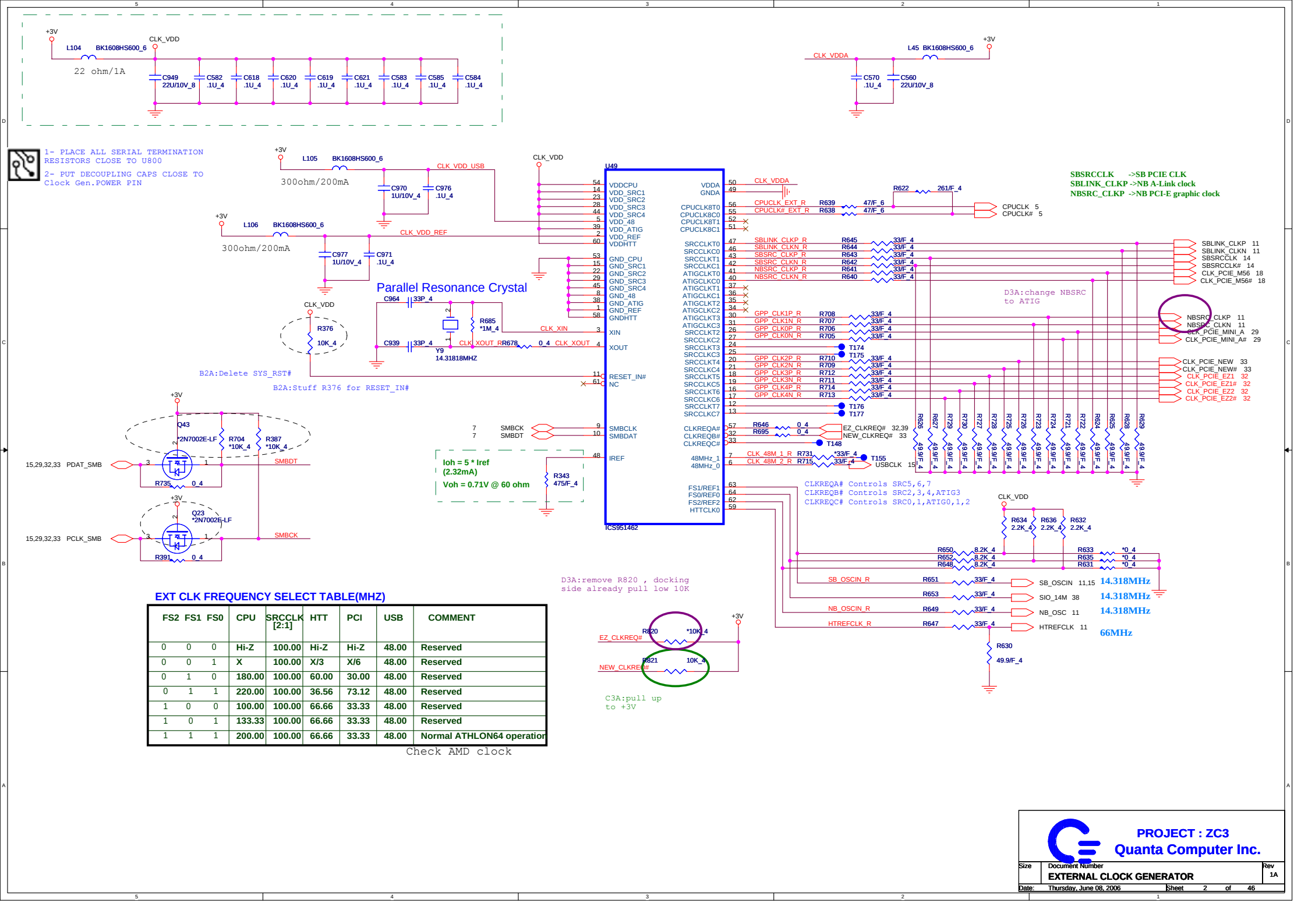
Embedded Controller
NS 551
Page 39

FIR Page 38
BIOS Page 39
Keyboard Page 40
Touchpad Page 40
SWITCH & LED Page 40
FAN Page 13

PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	B2A

Date: Thursday, June 08, 2006 Sheet 1 of 46



EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock

PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
	EXTERNAL CLOCK GENERATOR	1A
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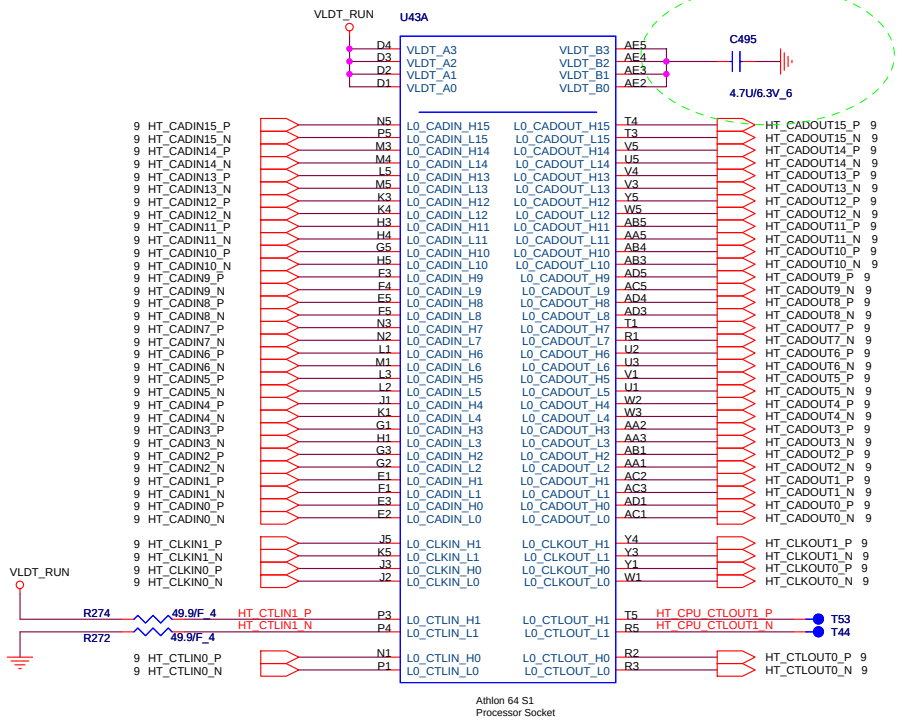
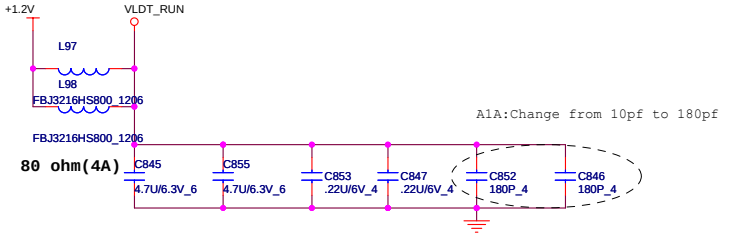
PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE





LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 HT I/F	1A
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Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

PLACE THEM CLOSE TO CPU WITHIN 1"

+1.8VSUS

R279 2K/F_4

CPU_M_VREF

C488 .1U_4

C503 1000p/50V_4

R282 2K/F_4

R574 39.2F_4

R573 39.2F_4

T56

VTT_SENSE

M_ZN

M_ZP

+0.9V_VTER

U43B

MEMVREF W17
VTT_SENSE Y10
MEMZN AE10
MEMZP AF10

VTT1 D10
VTT2 C10
VTT3 B10
VTT4 AD10
VTT5 W10
VTT6 AC10
VTT7 AB10
VTT8 AA10
VTT9 A10

MA0_CS_L3 V19
MA0_CS_L2 J22
MA0_CS_L1 V22
MA0_CS_L0 T19

MB0_CS_L3 Y26
MB0_CS_L2 J24
MB0_CS_L1 W24
MB0_CS_L0 U23

MA0_CLK_H2 Y16
MA0_CLK_L2 AA16
MA0_CLK_H1 E16
MA0_CLK_L1 E16

MB0_CLK_H2 AF18
MB0_CLK_L2 AF17
MB0_CLK_H1 A17
MB0_CLK_L1 A18

M_CLKOUT1 7
M_CLKOUT1# 7
M_CLKOUT0 7
M_CLKOUT0# 7
M_CLKOUT4 7
M_CLKOUT4# 7
M_CLKOUT3 7
M_CLKOUT3# 7

MB_CKE1 H26
MB_CKE0 J23
MA_CKE1 J20
MA_CKE0 J21

MB0_ODT1 W23
MB0_ODT0 W26
MA0_ODT1 V20
MA0_ODT0 U19

M_ODT3 7,8
M_ODT2 7,8
M_ODT1 7,8
M_ODT0 7,8

MA_ADD15 K19
MA_ADD14 K20
MA_ADD13 V24
MA_ADD12 K24
MA_ADD11 L20
MA_ADD10 R19
MA_ADD9 L19
MA_ADD8 L22
MA_ADD7 L21
MA_ADD6 M19
MA_ADD5 M20
MA_ADD4 M24
MA_ADD3 M22
MA_ADD2 N22
MA_ADD1 N21
MA_ADD0 R21

MB_ADD15 J25
MB_ADD14 J26
MB_ADD13 W25
MB_ADD12 L23
MB_ADD11 L25
MB_ADD10 U25
MB_ADD9 L24
MB_ADD8 M26
MB_ADD7 L26
MB_ADD6 N23
MB_ADD5 N24
MB_ADD4 N25
MB_ADD3 N26
MB_ADD2 P24
MB_ADD1 P26
MB_ADD0 T24

M_B_A[0..15] 7,8

MA_BANK2 K22
MA_BANK1 R20
MA_BANK0 T22

MB_BANK2 K26
MB_BANK1 T26
MB_BANK0 U26

M_B_BS#2 7,8
M_B_BS#1 7,8
M_B_BS#0 7,8

MA_RAS_L T20
MA_CAS_L U20
MA_WE_L U21

MB_RAS_L U24
MB_CAS_L V26
MB_WE_L U22

M_B_RAS# 7,8
M_B_CAS# 7,8
M_B_WE# 7,8

DDR II: CMD/CTRL/CLK

Athlon 64 S1
Processor Socket

+0.9V_VTER VTT decoupling capacitor,place near CPU

C517 4.7U/6.3V_6
C332 4.7U/6.3V_6
C512 4.7U/6.3V_6
C330 4.7U/6.3V_6
C350 .22U/6V_4
C485 .22U/6V_4
C487 .22U/6V_4
C338 .22U/6V_4
C504 1000p/50V_4
C335 1000p/50V_4
C509 1000p/50V_4
C352 1000p/50V_4
C339 180P_4
C344 180P_4
C475 180P_4
C496 180P_4

To SODIMM socket B (Far)

To SODIMM socket A (near)

U43C

7 M_B_DQ[0..63]

M_B_DQ63 AD11
M_B_DQ62 AF11
M_B_DQ61 AF14
M_B_DQ60 AE14
M_B_DQ59 Y11
M_B_DQ58 AB11
M_B_DQ57 AC12
M_B_DQ56 AF13
M_B_DQ55 AF15
M_B_DQ54 AE16
M_B_DQ53 AC18
M_B_DQ52 AF19
M_B_DQ51 AD14
M_B_DQ50 AC14
M_B_DQ49 AE18
M_B_DQ48 AD18
M_B_DQ47 AD20
M_B_DQ46 AC20
M_B_DQ45 AF23
M_B_DQ44 AF24
M_B_DQ43 AF20
M_B_DQ42 AE20
M_B_DQ41 AD22
M_B_DQ40 AC22
M_B_DQ39 AE25
M_B_DQ38 AD26
M_B_DQ37 AA25
M_B_DQ36 AA26
M_B_DQ35 AE24
M_B_DQ34 AD24
M_B_DQ33 AA23
M_B_DQ32 AA24
M_B_DQ31 G24
M_B_DQ30 G23
M_B_DQ29 D26
M_B_DQ28 C26
M_B_DQ27 G26
M_B_DQ26 G25
M_B_DQ25 E24
M_B_DQ24 E23
M_B_DQ23 C24
M_B_DQ22 B24
M_B_DQ21 C20
M_B_DQ20 B20
M_B_DQ19 C25
M_B_DQ18 D24
M_B_DQ17 A21
M_B_DQ16 D20
M_B_DQ15 D18
M_B_DQ14 C18
M_B_DQ13 D14
M_B_DQ12 C14
M_B_DQ11 A20
M_B_DQ10 A19
M_B_DQ9 A16
M_B_DQ8 A15
M_B_DQ7 A13
M_B_DQ6 D12
M_B_DQ5 E11
M_B_DQ4 G11
M_B_DQ3 B14
M_B_DQ2 A14
M_B_DQ1 A11
M_B_DQ0 C11

MB_DATA63 AA12
MB_DATA62 AB12
MB_DATA61 AA14
MB_DATA60 AB14
MB_DATA59 W11
MB_DATA58 Y12
MB_DATA57 AD13
MB_DATA56 AB13
MB_DATA55 AD15
MB_DATA54 AB15
MB_DATA53 AB17
MB_DATA52 Y17
MB_DATA51 Y14
MB_DATA50 W14
MB_DATA49 W16
MB_DATA48 AD17
MB_DATA47 Y18
MB_DATA46 AD19
MB_DATA45 AD21
MB_DATA44 AB21
MB_DATA43 AB18
MB_DATA42 AA18
MB_DATA41 AA20
MB_DATA40 Y20
MB_DATA39 AA22
MB_DATA38 Y22
MB_DATA37 W21
MB_DATA36 W22
MB_DATA35 AA21
MB_DATA34 AB22
MB_DATA33 AB24
MB_DATA32 Y24
MB_DATA31 H22
MB_DATA30 H20
MB_DATA29 F22
MB_DATA28 E21
MB_DATA27 J19
MB_DATA26 H24
MB_DATA25 F22
MB_DATA24 F20
MB_DATA23 C23
MB_DATA22 B22
MB_DATA21 E18
MB_DATA20 E20
MB_DATA19 D22
MB_DATA18 C19
MB_DATA17 G18
MB_DATA16 G17
MB_DATA15 C17
MB_DATA14 E14
MB_DATA13 E14
MB_DATA12 H17
MB_DATA11 E17
MB_DATA10 E15
MA_DATA9 H15
MA_DATA8 E13
MA_DATA7 C13
MA_DATA6 H12
MA_DATA5 H11
MA_DATA4 G14
MA_DATA3 H14
MA_DATA2 F12
MA_DATA1 G12
MA_DATA0 G12

M_A_DQ63 AA12
M_A_DQ62 AB12
M_A_DQ61 AA14
M_A_DQ60 AB14
M_A_DQ59 W11
M_A_DQ58 Y12
M_A_DQ57 AD13
M_A_DQ56 AB13
M_A_DQ55 AD15
M_A_DQ54 AB15
M_A_DQ53 AB17
M_A_DQ52 Y17
M_A_DQ51 Y14
M_A_DQ50 W14
M_A_DQ49 W16
M_A_DQ48 AD17
M_A_DQ47 Y18
M_A_DQ46 AD19
M_A_DQ45 AD21
M_A_DQ44 AB21
M_A_DQ43 AB18
M_A_DQ42 AA18
M_A_DQ41 AA20
M_A_DQ40 Y20
M_A_DQ39 AA22
M_A_DQ38 Y22
M_A_DQ37 W21
M_A_DQ36 W22
M_A_DQ35 AA21
M_A_DQ34 AB22
M_A_DQ33 AB24
M_A_DQ32 Y24
M_A_DQ31 H22
M_A_DQ30 H20
M_A_DQ29 F22
M_A_DQ28 E21
M_A_DQ27 J19
M_A_DQ26 H24
M_A_DQ25 F22
M_A_DQ24 F20
M_A_DQ23 C23
M_A_DQ22 B22
M_A_DQ21 E18
M_A_DQ20 E20
M_A_DQ19 D22
M_A_DQ18 C19
M_A_DQ17 G18
M_A_DQ16 G17
M_A_DQ15 C17
M_A_DQ14 E14
M_A_DQ13 E14
M_A_DQ12 H17
M_A_DQ11 E17
M_A_DQ10 E15
M_A_DQ9 H15
M_A_DQ8 E13
M_A_DQ7 C13
M_A_DQ6 H12
M_A_DQ5 H11
M_A_DQ4 G14
M_A_DQ3 H14
M_A_DQ2 F12
M_A_DQ1 G12
M_A_DQ0 G12

M_A_DQ[0..63] 7

7 M_B_DM[0..7]

M_B_DM7 AD12
M_B_DM6 AC16
M_B_DM5 AE22
M_B_DM4 AB26
M_B_DM3 E25
M_B_DM2 A22
M_B_DM1 B16
M_B_DM0 A12

MB_DM7
MB_DM6
MB_DM5
MB_DM4
MB_DM3
MB_DM2
MB_DM1
MB_DM0

MA_DM7 Y13
MA_DM6 AB16
MA_DM5 Y19
MA_DM4 AC24
MA_DM3 F24
MA_DM2 E19
MA_DM1 C15
MA_DM0 E12

M_A_DM7
M_A_DM6
M_A_DM5
M_A_DM4
M_A_DM3
M_A_DM2
M_A_DM1
M_A_DM0

M_A_DM[0..7] 7

M_B_DQS7 AE12
M_B_DQS#7 AE13
M_B_DQS6 AE16
M_B_DQS#6 AD16
M_B_DQS5 AF21
M_B_DQS#5 AF22
M_B_DQS4 AC25
M_B_DQS#4 AC26
M_B_DQS3 F26
M_B_DQS#3 E26
M_B_DQS2 A24
M_B_DQS#2 A23
M_B_DQS1 D16
M_B_DQS#1 C16
M_B_DQS0 C12
M_B_DQS#0 B12

MB_DQS_H7
MB_DQS_L7
MB_DQS_H6
MB_DQS_L6
MB_DQS_H5
MB_DQS_L5
MB_DQS_H4
MB_DQS_L4
MB_DQS_H3
MB_DQS_L3
MB_DQS_H2
MB_DQS_L2
MB_DQS_H1
MB_DQS_L1
MB_DQS_H0
MB_DQS_L0

MA_DQS_H7 W12
MA_DQS_L7 W13
MA_DQS_H6 Y15
MA_DQS_L6 W15
MA_DQS_H5 AB19
MA_DQS_L5 AB20
MA_DQS_H4 AD23
MA_DQS_L4 AC23
MA_DQS_H3 G22
MA_DQS_L3 G21
MA_DQS_H2 C22
MA_DQS_L2 C21
MA_DQS_H1 G16
MA_DQS_L1 G15
MA_DQS_H0 G13
MA_DQS_L0 H13

M_A_DQS7
M_A_DQS#7
M_A_DQS6
M_A_DQS#6
M_A_DQS5
M_A_DQS#5
M_A_DQS4
M_A_DQS#4
M_A_DQS3
M_A_DQS#3
M_A_DQS2
M_A_DQS#2
M_A_DQS1
M_A_DQS#1
M_A_DQS0
M_A_DQS#0

7 M_B_DQS[0..7]

M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7

7 M_B_DQS#[0..7]

M_B_DQS#0
M_B_DQS#1
M_B_DQS#2
M_B_DQS#3
M_B_DQS#4
M_B_DQS#5
M_B_DQS#6
M_B_DQS#7

7 M_A_DQS[0..7]

M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7

7 M_A_DQS#[0..7]

M_A_DQS#0
M_A_DQS#1
M_A_DQS#2
M_A_DQS#3
M_A_DQS#4
M_A_DQS#5
M_A_DQS#6
M_A_DQS#7

DDR: DATA

Athlon 64 S1
Processor Socket

PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 DDRII MEMORY I/F	1A
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ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

CPU_VDDA_RUN

50 mil
33 ohm(3000mA)
CPU_VDDA_RUN
L29 BLM18PG330SN1D
+2.5V
C336 4.7U/6.3V_6
C351 .22U/6V
C345 3300p/25V_4
C839 100U/6.3V_3528

A1A:Change from 3900pf to 3300pf

2 CPUCLK C837 3900p/25V_4 CPU_CLKIN_SC_P
R563 169F_6
2 CPUCLK# C838 3900p/25V_4 CPU_CLKIN_SC_N

SB460 only

B2A:ati suggestion to avoid hynix rev issue
stuff R558,R560 del R561

+1.8V +3V +1.8VSUS
R557 300_4
R558 4.7K/F_4
C840 .1U_4
14,15 CPU_PWRGD
U41 NC7S208P5X_NL
CPU_ALL_PWROK

+1.8V +1.8VSUS
R556 300_4
C331 .1U_4
11,14,15 LDT_STOP#
U21 NC7SZ08P5X_NL
CPU_LDTSTOP#

+1.8V +1.8VSUS
R559 300_4
C841 .1U_4
14 LDT_RST#
14,15,39 EC_PWRGD
11,39 NB_PWRGD
R560 *0_4
R561 *0_4
U42 NC7SZ08P5X_NL
CPU_HT_RESET#

+1.8V +1.8VSUS
R304 330_4
Q19 MMBT3904
R295 300_4
R300 *0_4
H_PROCHOT#
CPU_EC_PROCHOT# 39
CPU_PROCHOT# 15

SB_THERMTRIP# 15
separated input voltage
0104
R310
EC_PWRGD
+1.8V R305 *330_4
Q21 *MMBT3904
R309 4.7K/F_4
1.8VSUS 300_4 R303
H_THERMTRIP#
Q20 MMBT3904
THERM_SYS_PWR 44

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.

+1.8V R583 *300_4 R584 *300_4 R585 300_4
CPU_SIC_R
CPU_SID_R

B2A:Add LEVEL-SHIFT circuit(R806,R807,Q47) on PSI# that between CPU and POWER.

+1.8VSUS +3V
R806 10K_4
R807 10K_4
Q47 MMBT3904
PSI_L# PSI# PSI# 41

VLDT_RUN
place them to CPU within 1"
10/5/5/5/10
R276 44.2F_4
R277 44.2F_4
41 COREFB+V
41 COREFB-
To Power

+1.8VSUS
R215 300_4
Only VID1 need pullup to VDDIO

U43D

CPU_VDDA_RUN F8 F9 VDDA2 VDDA1
CPU_HT_RESET# T10 B7 RESET_L
CPU_ALL_PWROK T10 A7 PWROK
CPU_LDTSTOP# T31 F10 LDTSTOP_L
CPU_SIC_R AF4 SIC
CPU_SID_R AF5 SID
CPU_HTREF1 P6 HT_REF1
CPU_HTREF0 R6 HT_REF0
T22 F6 VDD_FB_H
F6 VDD_FB_L
T23 W9
CPU_VDDIO_SUS_FB_H T58 Y9 VDDIO_FB_H
CPU_VDDIO_SUS_FB_L T57 VDDIO_FB_L
CPU_CLKIN_SC_P A9 CLKIN_H
CPU_CLKIN_SC_N A8 CLKIN_L
CPU_DBRDY G10 DBRDY
CPU_TMS AA9 TMS
CPU_TCK AC9 TCK
CPU_TRST# AD9 TRST_L
CPU_TDI AF9 TDI
THERMTRIP_L AF6 H_THERMTRIP#
PROCHOT_L AC7 H_PROCHOT#
VID5 A5 VID4 C6 VID3 A6 VID2 A4 VID1 C5 VID0 B5
CPU_PRESENT_L AC6 CPU_PRESENT#
PSI_L A3 PSI_L#
T19
DBREQ_L E10 CPU_DBREQ#
TDO AF9 CPU_TDO
TEST29_H C9 CPU_TEST29_H
TEST29_L C8 CPU_TEST29_L
R220 80.6F_4
FBCLKOUT_P
FBCLKOUT_N
ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"
CPU_TEST25_H_BYPASSCLK_H E9
CPU_TEST25_L_BYPASSCLK_L E8
CPU_TEST19_PLLTEST0 G9
CPU_TEST18_PLLTEST1 H10
AA7
C2
CPU_TEST17_BP3 T21 D7
CPU_TEST16_BP2 T32 E7
CPU_TEST15_BP1 F7
CPU_TEST14_BP0 C7
CPU_TEST12_SCANSHIFTENB AC8
CPU_TEST07_ANALOG_T C3
CPU_TEST6_DIECRACKMON T27 AA6
CPU_TEST5_THERMDC T60 W7
CPU_TEST4_THERMDA W8
CPU_TEST3_GATE0 T59 Y6
CPU_TEST2_DRAIN0 T64 AB6
13 CPU_TEST5_THERMDC
13 CPU_TEST4_THERMDA
CPU_TEST24_SCANCLK1 AE7
CPU_TEST23_TSTUPD AD7 T137
CPU_TEST22_SCANSHIFTEN AE8
CPU_TEST21_SCANEN AB8
CPU_TEST20_SCANCLK2 AE7
CPU_TEST28_H_PLLCHRZ_P J7 T54
CPU_TEST28_L_PLLCHRZ_N H8 T55
CPU_TEST27_SINGLECHAIN AF8
CPU_TEST26_BURNIN# AE6
CPU_TEST10_ANALOGOUT K8 T52
CPU_TEST08_DIG_T C4 T20
CPU_RSVD_MA0_CLK3_P T49 P20 RSVD0
CPU_RSVD_MA0_CLK3_N T51 P19 RSVD1
CPU_RSVD_MA0_CLK0_P T42 N20 RSVD2
CPU_RSVD_MA0_CLK0_N T43 N19 RSVD3
CPU_RSVD_MB0_CLK3_P T46 R26 RSVD4
CPU_RSVD_MB0_CLK3_N T47 R25 RSVD5
CPU_RSVD_MB0_CLK0_P T48 P22 RSVD6
CPU_RSVD_MB0_CLK0_N T50 R22 RSVD7
RSVD8 H16 CPU_MA_RESET# T25
RSVD9 B18 CPU_MB_RESET# T26
RSVD10 B3 CPU_RSVD_VIDSTRB1 T18
RSVD11 C1 CPU_RSVD_VIDSTRB0 T29
RSVD12 H6 CPU_RSVD_VDDNB_FB_P T40
RSVD13 G6 CPU_RSVD_VDDNB_FB_N T45
RSVD14 D5 CPU_RSVD_CORE_TYPE T24
RSVD15 R24
RSVD16 W18
RSVD17 R23
RSVD18 AA8
RSVD19 R18
RSVD20 R19
MISC

AMD NPT S1 SOCKET
Processor Socket

Power Status Indicator for the VDD Power Supply regulator. This signal may be used by the regulator to improve effeciency when the processor is in low power states.

B2A:AMD suggestion not stuff
R577,R580,R581,R579,R292,R213,R209

+1.8VSUS
CPU_TEST27_SINGLECHAIN R577 *300_4
CPU_TEST26_BURNIN# R580 300_4
CPU_PRESENT# R294 1K/F_4
CPU_TEST25_H_BYPASSCLK_H R210 510/F_4
CPU_TEST21_SCANEN R293 300_4
CPU_TEST20_SCANCLK2 R580 *300_4
CPU_TEST24_SCANCLK1 R581 *300_4
CPU_TEST22_SCANSHIFTEN R579 *300_4
CPU_TEST12_SCANSHIFTENB R292 *300_4
CPU_TEST15_BP1 R213 *300_4
CPU_TEST14_BP0 R209 *300_4
CPU_TEST25_L_BYPASSCLK_L R214 510/F_4
CPU_TEST19_PLLTEST0 R208 300_4
CPU_TEST18_PLLTEST1 R212 300_4

IF no use which Net need pull-up or down

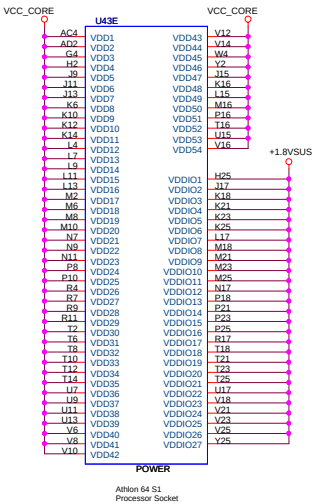
+1.8VSUS
R576 *220_4
R575 *220_4
R296 *220_4
R570 *220_4
R211 *220_4

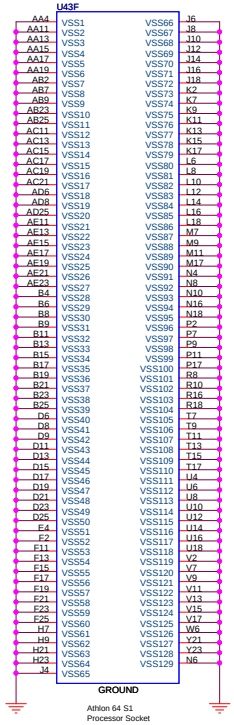
HDT CONNECTOR
CPU_DBREQ# T28
CPU_DBRDY T30
CPU_TCK T136
CPU_TMS T65
CPU_TDI T133
CPU_TRST# T135
CPU_TDO T134
LDT_RST# T105
PUT CLOSE ON LAYOUT

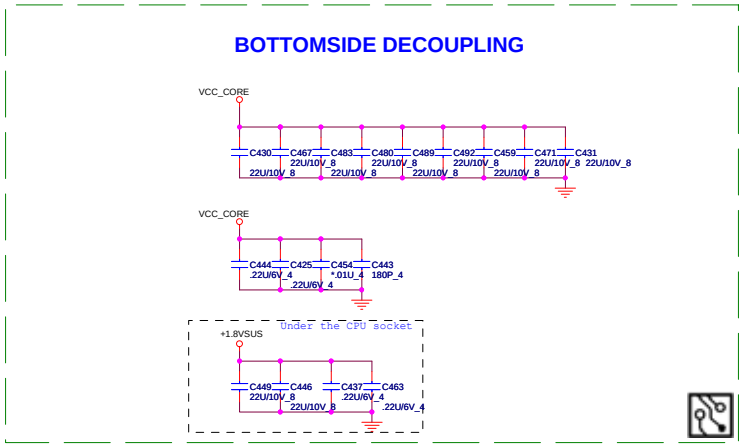
NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

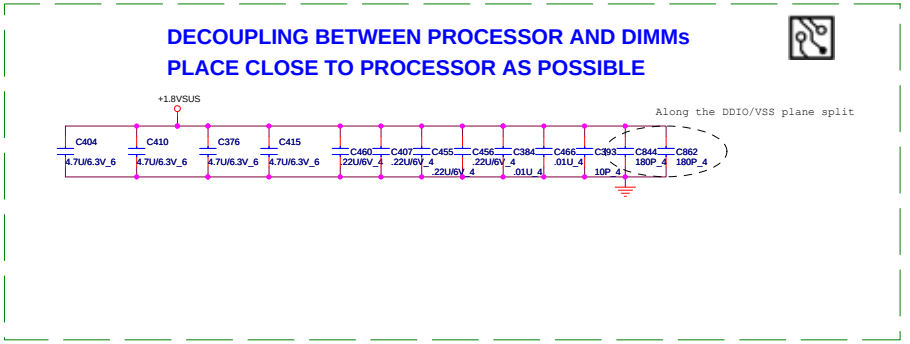
PROJECT : ZC3
Quanta Computer Inc.

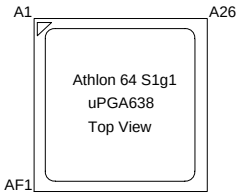
Size	Document Number	Rev
	ATHLON64 CTRL & DEBUG	1A
Date: Thursday, June 08, 2006	Sheet 5 of 46	





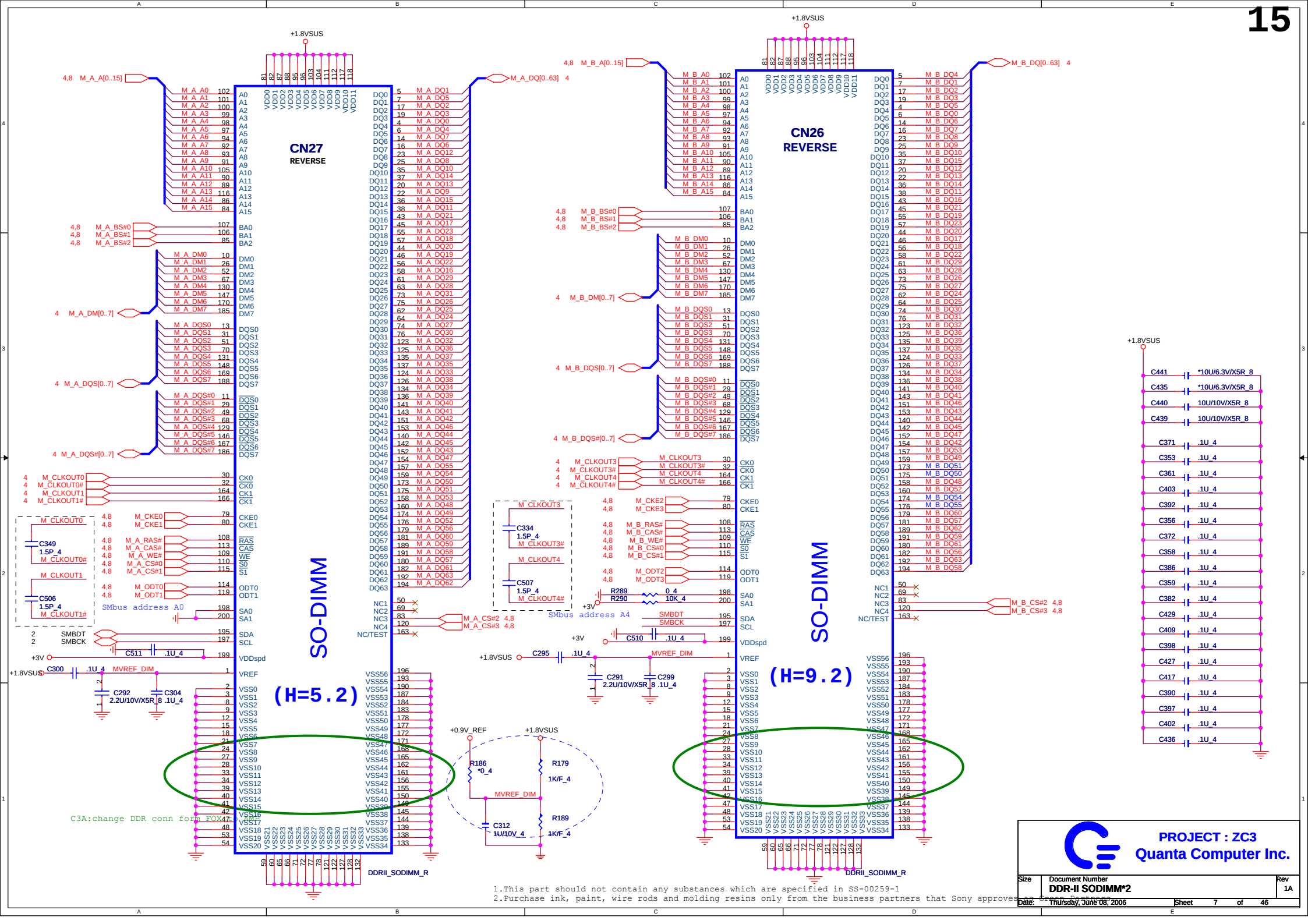






PROCESSOR POWER AND GROUND

PROJECT : ZC3		
Quanta Computer Inc.		
Size	Document Number	Rev
	ATHLON64 PWR & GND	1A
Date: Thursday, June 08, 2006	Sheet 6 of 46	

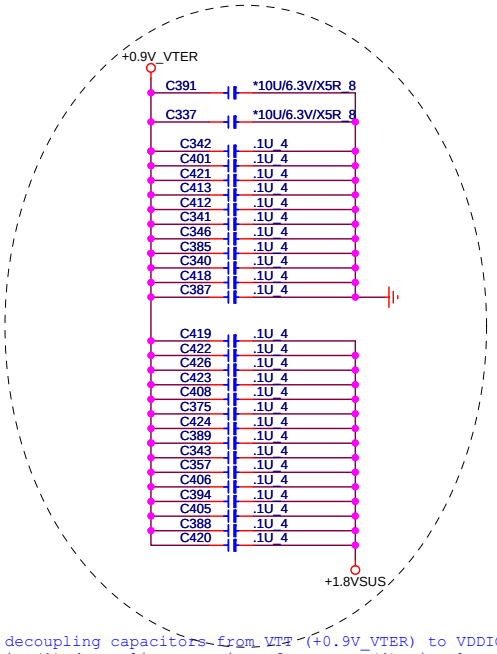


PROJECT : ZC3
Quanta Computer Inc.

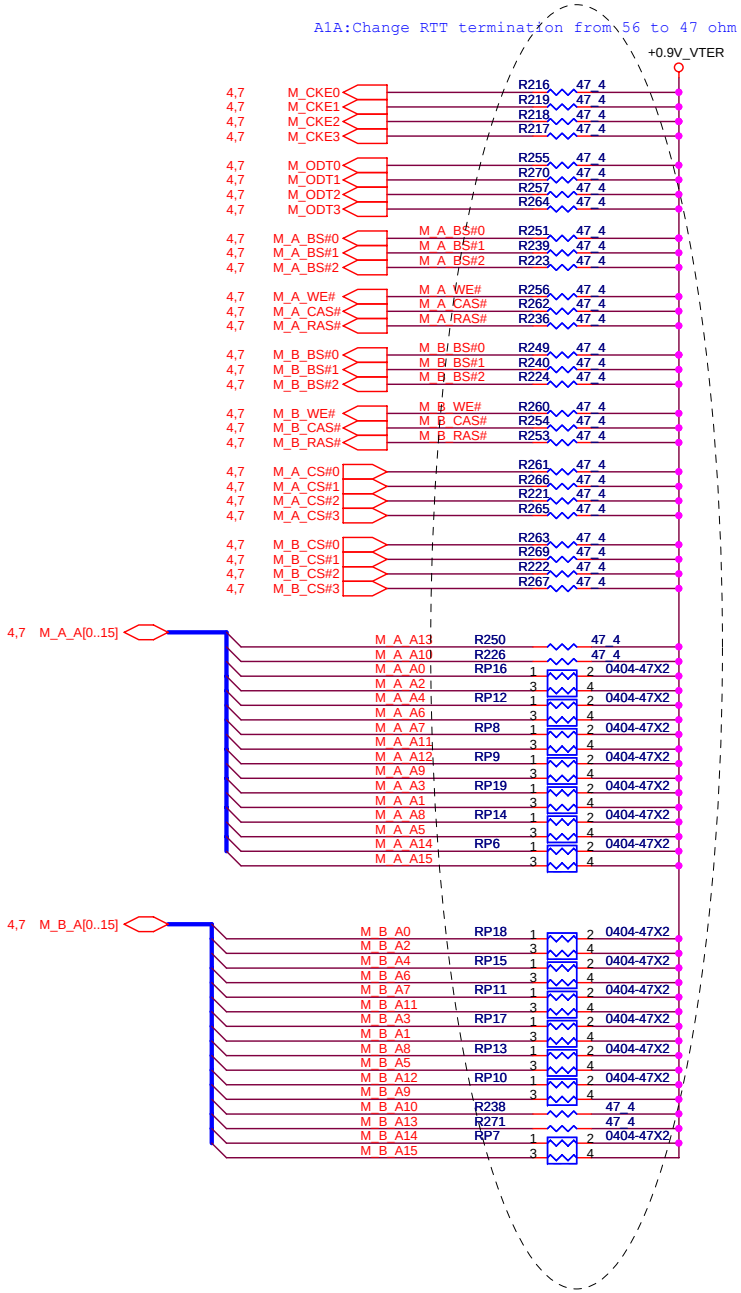
Size	Document Number	Rev
	DDR-II SODIMM*2	1A
Date: Thursday, June 08, 2006	Sheet 7 of 46	

A1A:Change RTT termination from 56 to 47 ohm

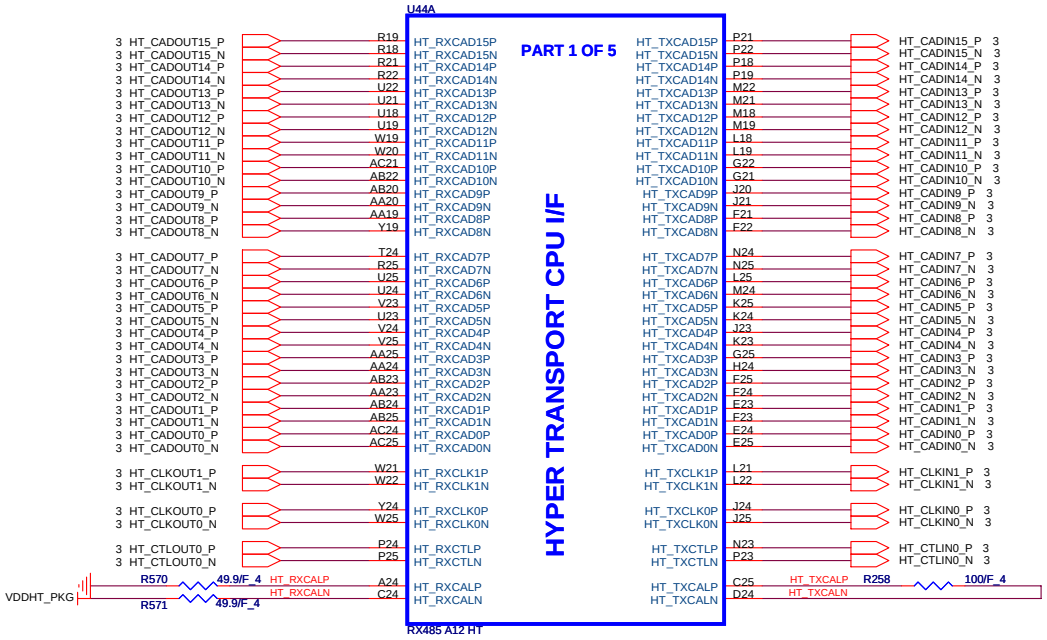
VTT is decoupled to VDDIO,VTT is decoupled to VSS



decoupling capacitors from VTT (+0.9V_VTER) to VDDIO (+1.8VSUS). Which is (1) decoupling capacitor for every (4) signals terminated to VTT



PROJECT : ZC3		
Quanta Computer Inc.		
Size	Document Number	Rev
	DDR-II TERMINATION	1A
Date: Thursday, June 08, 2006	Sheet 8 of 46	



PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-HT LINK0 I/F	1A
Date: Thursday, June 08, 2006	Sheet 9 of 46	

Stiching capacitor

VA: C146 .1U_4, C159 .1U_4 — VIN / +1.8V

+3V: C134 .1U_4 — VIN

+1.8V: C206 .1U_4 — VIN

VIN: C147 .1U_4, C322 .1U_4 — +1.8V / +3V

VIN: C959 .1U_4 — +3V

+3V: C311 .1U_4 — VIN

+1.8V: C822 .1U_4 — +1.2V

VCC_CORE: C360 .1U_4 — +1.2V

VCC_NB: C461 .1U_4 — VCC_CORE

+3V: C494 .1U_4 — VCC_CORE

+1.8VSUS: C505 .1U_4 — VCC_CORE

+1.8VSUS: C908 .1U_4 — +3V

+1.8VSUS: C289 .1U_4 — VIN

+5V: C47 .1U_4 — +3V

+5V: C919 .1U_4 — +3V

+5V: C518 .1U_4 — VIN

+1.8VSUS: C468 .1U_4 — +0.9V_VTER

+5V: C1039 .1U_4 — +3V

+5V: C921 .1U_4 — +3V

+5V: C26 .1U_4 — +3V

+5V: C662 .1U_4 — +3V

+5V: C751 .1U_4 — VIN

+3V: C70 .1U_4 — VIN

+3V: C842 .1U_4 — VIN

+3V: C400 .1U_4 — VIN

+5V: C1044 .1U_4 — VIN

+5V: C553 .1U_4 — VIN

+1.2V_VPCIE: C784 .1U_4 — +1.1V_VGA

+1.2V_VPCIE: C103 .1U_4 — +3V

+5V: C60 .1U_4 — +1.1V_VGA

+1.2V_VPCIE: C843 .1U_4 — +1.8V

+3V: C333 .1U_4 — +1.2V

+3V: C514 .1U_4 — VCC_CORE

+3V: C895 .1U_4 — VCC_CORE

+3V: C906 .1U_4 — VCC_CORE

+1.8VSUS: C907 .1U_4 — +3VPCU

+3V: C554 .1U_4 — +3VPCU

+3V: C526 .1U_4 — +3VPCU

+3V: C637 .1U_4 — VDDQ_3V

+3V: C612 .1U_4 — VDDQ_3V

U44B

PART 2 OF 5

PCIE I/F GFX

PEG_RXN[15:0] 18

PEG_RXN0 PEG_RXN1 PEG_RXN2 PEG_RXN3 PEG_RXN4 PEG_RXN5 PEG_RXN6 PEG_RXN7 PEG_RXN8 PEG_RXN9 PEG_RXN10 PEG_RXN11 PEG_RXN12 PEG_RXN13 PEG_RXN14 PEG_RXN15

PEG_RXP[15:0] 18

PEG_RXP0 PEG_RXP1 PEG_RXP2 PEG_RXP3 PEG_RXP4 PEG_RXP5 PEG_RXP6 PEG_RXP7 PEG_RXP8 PEG_RXP9 PEG_RXP10 PEG_RXP11 PEG_RXP12 PEG_RXP13 PEG_RXP14 PEG_RXP15

PEG_RXP0 G5, PEG_RXN0 G4, PEG_RXP1 J3, PEG_RXN1 J2, PEG_RXP2 J4, PEG_RXN2 J5, PEG_RXP3 L3, PEG_RXN3 L2, PEG_RXP4 L4, PEG_RXN4 L5, PEG_RXP5 M3, PEG_RXN5 M2, PEG_RXP6 M4, PEG_RXN6 M5, PEG_RXP7 P3, PEG_RXN7 P2, PEG_RXP8 P4, PEG_RXN8 P5, PEG_RXP9 R4, PEG_RXN9 R5, PEG_RXP10 R7, PEG_RXN10 R8, PEG_RXP11 U4, PEG_RXN11 U5, PEG_RXP12 W4, PEG_RXN12 W5, PEG_RXP13 Y4, PEG_RXN13 Y5, PEG_RXP14 V9, PEG_RXN14 W9, PEG_RXP15 AB7, PEG_RXN15 AB6

GFX_RX0P GFX_RX0N GFX_RX1P GFX_RX1N GFX_RX2P GFX_RX2N GFX_RX3P GFX_RX3N GFX_RX4P GFX_RX4N GFX_RX5P GFX_RX5N GFX_RX6P GFX_RX6N GFX_RX7P GFX_RX7N GFX_RX8P GFX_RX8N GFX_RX9P GFX_RX9N GFX_RX10P GFX_RX10N GFX_RX11P GFX_RX11N GFX_RX12P GFX_RX12N GFX_RX13P GFX_RX13N GFX_RX14P GFX_RX14N GFX_RX15P GFX_RX15N

GFX_TX0P GFX_TX0N GFX_TX1P GFX_TX1N GFX_TX2P GFX_TX2N GFX_TX3P GFX_TX3N GFX_TX4P GFX_TX4N GFX_TX5P GFX_TX5N GFX_TX6P GFX_TX6N GFX_TX7P GFX_TX7N GFX_TX8P GFX_TX8N GFX_TX9P GFX_TX9N GFX_TX10P GFX_TX10N GFX_TX11P GFX_TX11N GFX_TX12P GFX_TX12N GFX_TX13P GFX_TX13N GFX_TX14P GFX_TX14N GFX_TX15P GFX_TX15N

J1 C_PEG_TXP0 C866 .1U-10V_4 PEG_TXP0
H2 C_PEG_TXN0 C863 .1U-10V_4 PEG_TXN0
K2 C_PEG_TXP1 C865 .1U-10V_4 PEG_TXP1
K1 C_PEG_TXN1 C864 .1U-10V_4 PEG_TXN1
K3 C_PEG_TXP2 C867 .1U-10V_4 PEG_TXP2
L3 C_PEG_TXN2 C869 .1U-10V_4 PEG_TXN2
L1 C_PEG_TXP3 C870 .1U-10V_4 PEG_TXP3
L2 C_PEG_TXN3 C868 .1U-10V_4 PEG_TXN3
N2 C_PEG_TXP4 C871 .1U-10V_4 PEG_TXP4
N1 C_PEG_TXN4 C873 .1U-10V_4 PEG_TXN4
P2 C_PEG_TXP5 C874 .1U-10V_4 PEG_TXP5
P1 C_PEG_TXN5 C872 .1U-10V_4 PEG_TXN5
P3 C_PEG_TXP6 C875 .1U-10V_4 PEG_TXP6
R3 C_PEG_TXN6 C877 .1U-10V_4 PEG_TXN6
R1 C_PEG_TXP7 C878 .1U-10V_4 PEG_TXP7
R2 C_PEG_TXN7 C876 .1U-10V_4 PEG_TXN7
T2 C_PEG_TXP8 C879 .1U-10V_4 PEG_TXP8
U1 C_PEG_TXN8 C881 .1U-10V_4 PEG_TXN8
V2 C_PEG_TXP9 C882 .1U-10V_4 PEG_TXP9
V1 C_PEG_TXN9 C880 .1U-10V_4 PEG_TXN9
V3 C_PEG_TXP10 C883 .1U-10V_4 PEG_TXP10
W3 C_PEG_TXN10 C885 .1U-10V_4 PEG_TXN10
W1 C_PEG_TXP11 C886 .1U-10V_4 PEG_TXP11
W2 C_PEG_TXN11 C884 .1U-10V_4 PEG_TXN11
Y2 C_PEG_TXP12 C887 .1U-10V_4 PEG_TXP12
AA1 C_PEG_TXN12 C889 .1U-10V_4 PEG_TXN12
AA2 C_PEG_TXP13 C890 .1U-10V_4 PEG_TXP13
AB2 C_PEG_TXN13 C888 .1U-10V_4 PEG_TXN13
AB1 C_PEG_TXP14 C891 .1U-10V_4 PEG_TXP14
AC1 C_PEG_TXN14 C893 .1U-10V_4 PEG_TXN14
AE3 C_PEG_TXP15 C894 .1U-10V_4 PEG_TXP15
AE4 C_PEG_TXN15 C892 .1U-10V_4 PEG_TXN15

EZ4
32 PCIE_RXP0
32 PCIE_RXN0
W11 W12

EZ4
32 PCIE_RXP1
32 PCIE_RXN1
AA11 AB11

New card
33 PCIE_RXP2
33 PCIE_RXN2
Y7 AA7

WLAN
29 PCIE_RXP3
29 PCIE_RXN3
AB9 AA9

PCIE I/F GPP

GPP_RX0P GPP_RX0N GPP_RX1P GPP_RX1N GPP_RX2P GPP_RX2N GPP_RX3P GPP_RX3N

GPP_TX0P GPP_TX0N GPP_TX1P GPP_TX1N GPP_TX2P GPP_TX2N GPP_TX3P GPP_TX3N

AD8 GPP_TX0P_C C497 .1U_4 PCIE_TXP0 32 EZ4
AE8 GPP_TX0N_C C491 .1U_4 PCIE_TXN0 32 EZ4
AD7 GPP_TX1P_C C478 .1U_4 PCIE_TXP1 32 EZ4
AE7 GPP_TX1N_C C479 .1U_4 PCIE_TXN1 32 EZ4
AD4 GPP_TX2P_C C902 .1U_4 PCIE_TXP2 33 New card
AE5 GPP_TX2N_C C901 .1U_4 PCIE_TXN2 33 New card
AD5 GPP_TX3P_C C477 .1U_4 PCIE_TXP3 29 WLAN
AD6 GPP_TX3N_C C476 .1U_4 PCIE_TXN3 29 WLAN

PCIE I/F SB

SB_RX0P SB_RX0N SB_RX1P SB_RX1N

SB_TX0P SB_TX0N SB_TX1P SB_TX1N

AE9 A_TX0P_C C898 .1U_4 A_TX0P 14
AD10 A_TX0N_C C897 .1U_4 A_TX0N 14
AC8 A_TX1P_C C900 .1U_4 A_TX1P 14
AD9 A_TX1N_C C899 .1U_4 A_TX1N 14

14 A_RX0P
14 A_RX0N
W14 W15

14 A_RX1P
14 A_RX1N
AB12 AA12

R278 10K_4 AA14
R281 8.25K/F_6 AB14

PCE_ISET(PCE_CALI) PCE_PCAL(PCE_CALRP)
PCE_TXISET(NC) PCE_NCAL(PCE_CALRN)

AD11 R572 150/F_4 VDDA12_PKG2
AE11 R280 100/F_4

RX485 A12 HT

C3A:change footprint form c0402-c to c0402

R214: 10KOhm FOR RS485
1.47KOhm FOR RS690
R213: 8.25KOhm FOR RS485
DNI FOR RS690

R216: 150 Ohm FOR RS485
562 Ohm FOR RS690
Ward update to 100 Ohm FOR RS485
2KOhm FOR RS690
R215:

PEG_TXN[15:0] 18

PEG_TXN0 PEG_TXN1 PEG_TXN2 PEG_TXN3 PEG_TXN4 PEG_TXN5 PEG_TXN6 PEG_TXN7 PEG_TXN8 PEG_TXN9 PEG_TXN10 PEG_TXN11 PEG_TXN12 PEG_TXN13 PEG_TXN14 PEG_TXN15

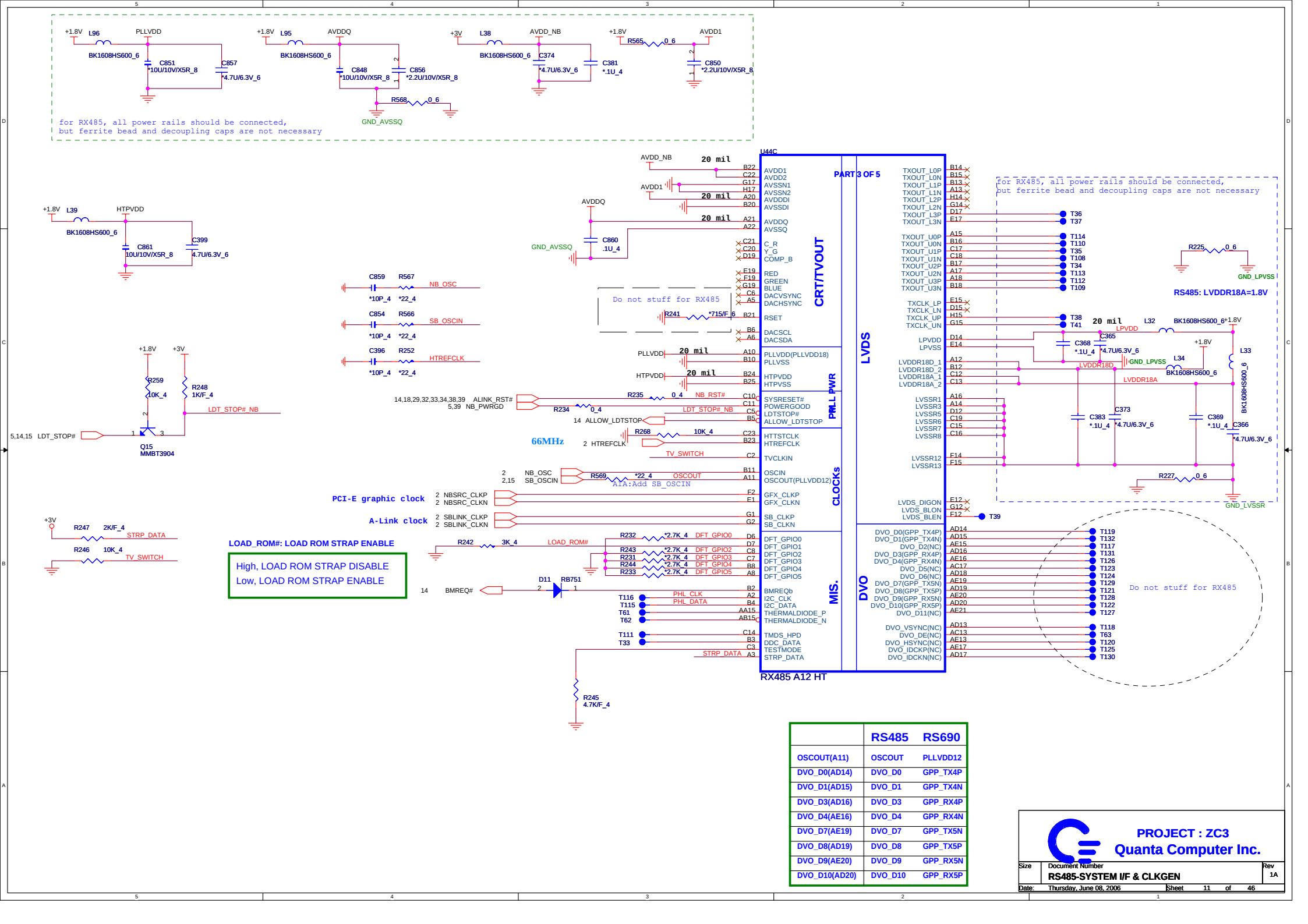
PEG_TXP[15:0] 18

PEG_TXP0 PEG_TXP1 PEG_TXP2 PEG_TXP3 PEG_TXP4 PEG_TXP5 PEG_TXP6 PEG_TXP7 PEG_TXP8 PEG_TXP9 PEG_TXP10 PEG_TXP11 PEG_TXP12 PEG_TXP13 PEG_TXP14 PEG_TXP15

Place these caps close to connector

PROJECT : ZC3
Quanta Computer Inc.

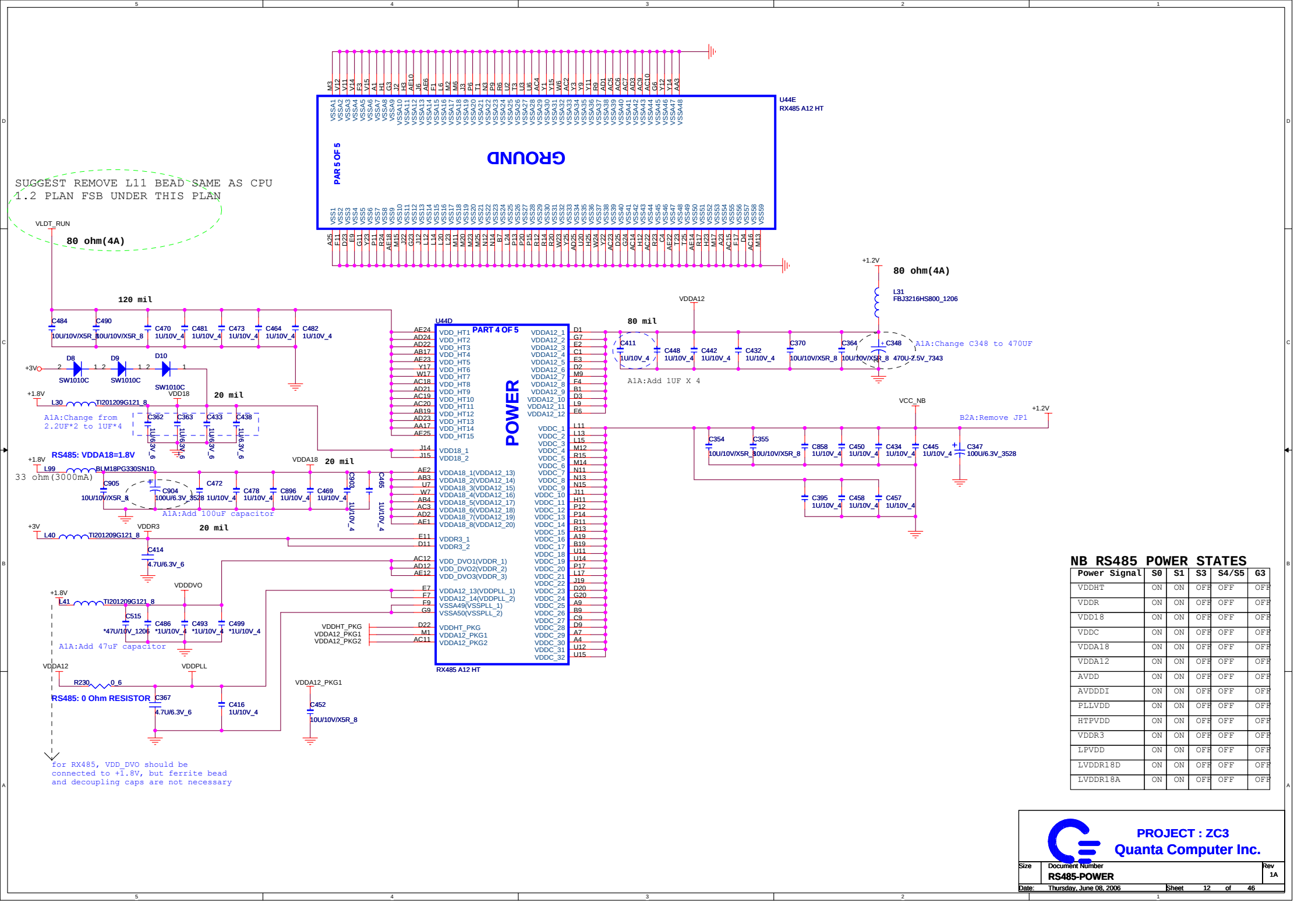
Size	Document Number	Rev
	RS485-PCIE LINK I/F	1A
Date: Thursday, June 08, 2006	Sheet 10 of 46	



	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-SYSTEM I/F & CLKGEN	1A
Date: Thursday, June 08, 2006	Sheet 11 of 46	

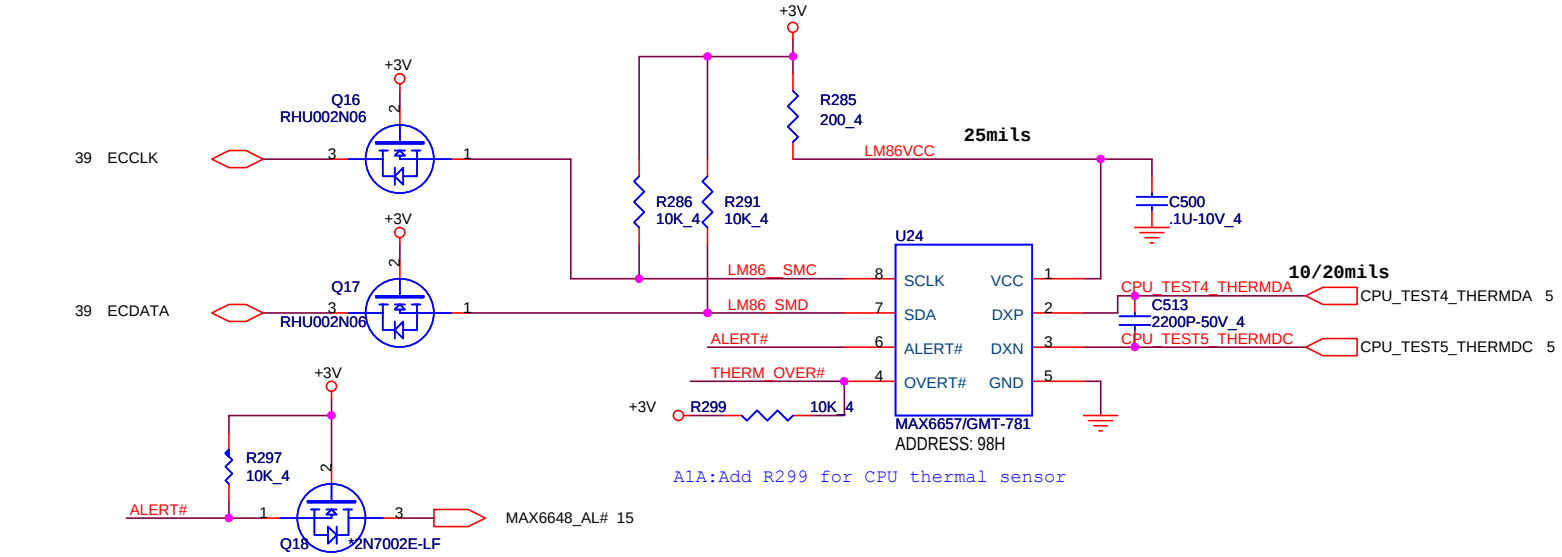


NB RS485 POWER STATES

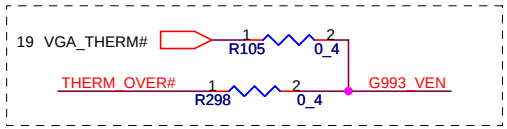
Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-POWER	1A
Date: Thursday, June 08, 2006	Sheet 12 of 46	

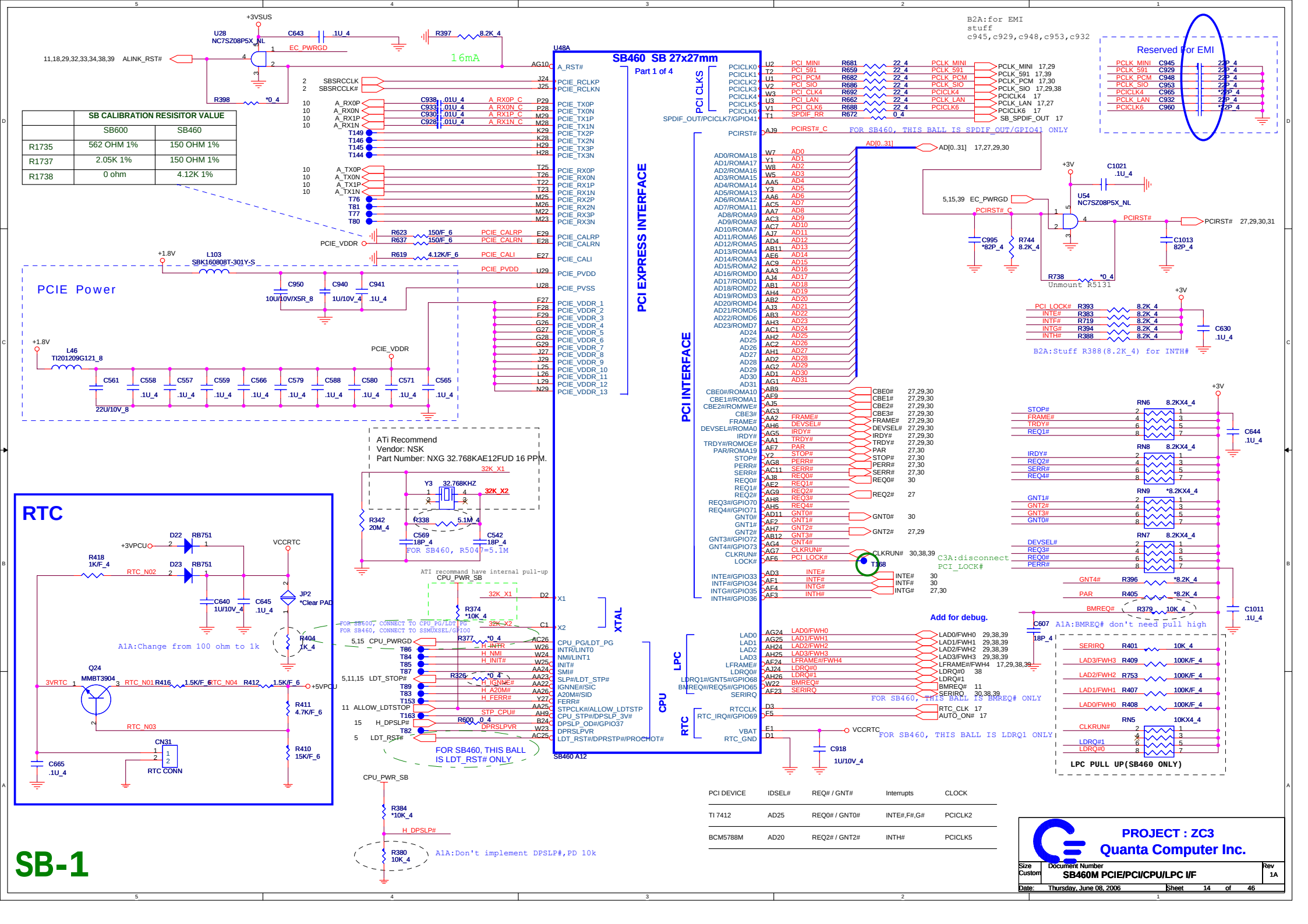


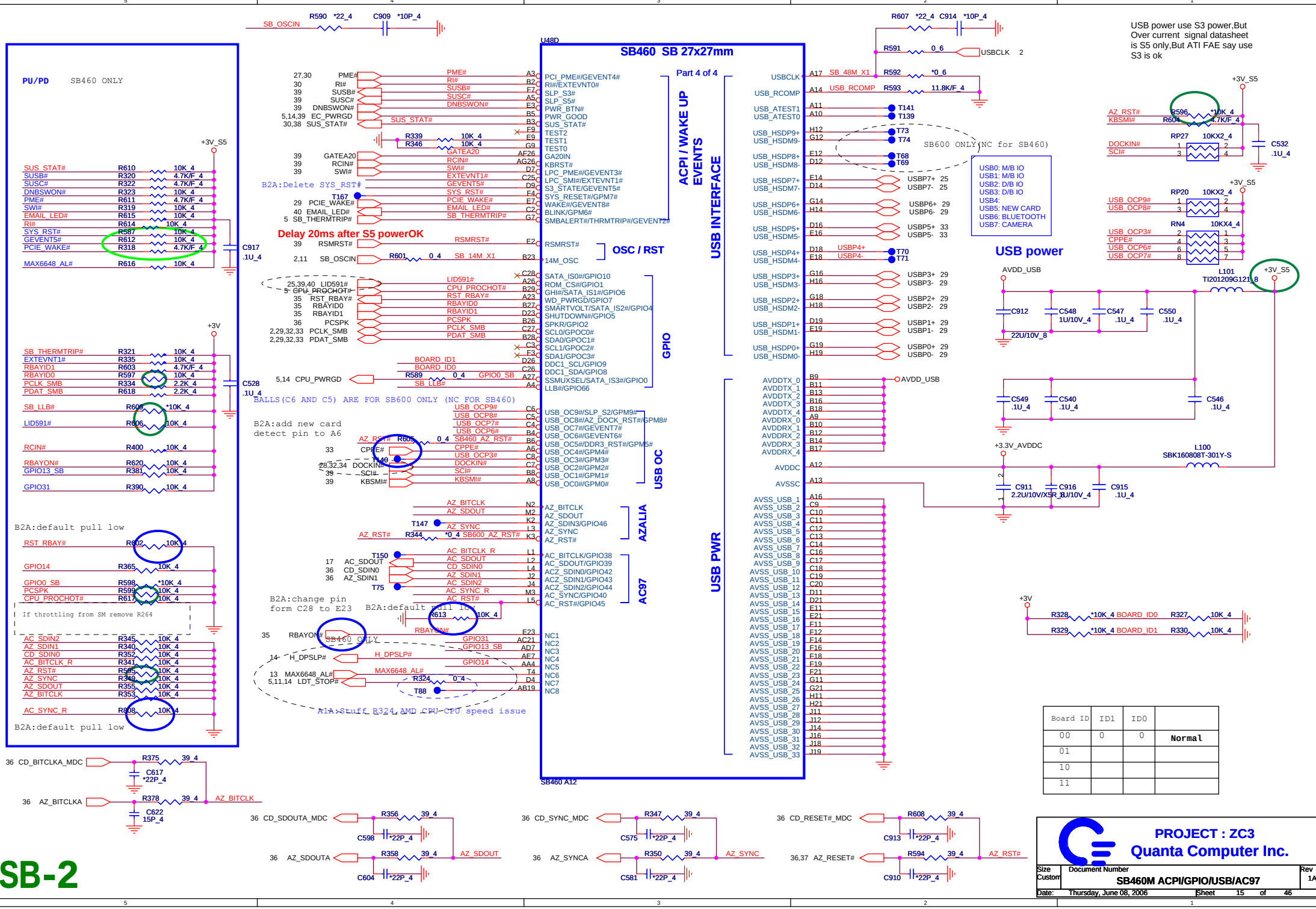
A1A:Add R105 for VGA thermal sensor

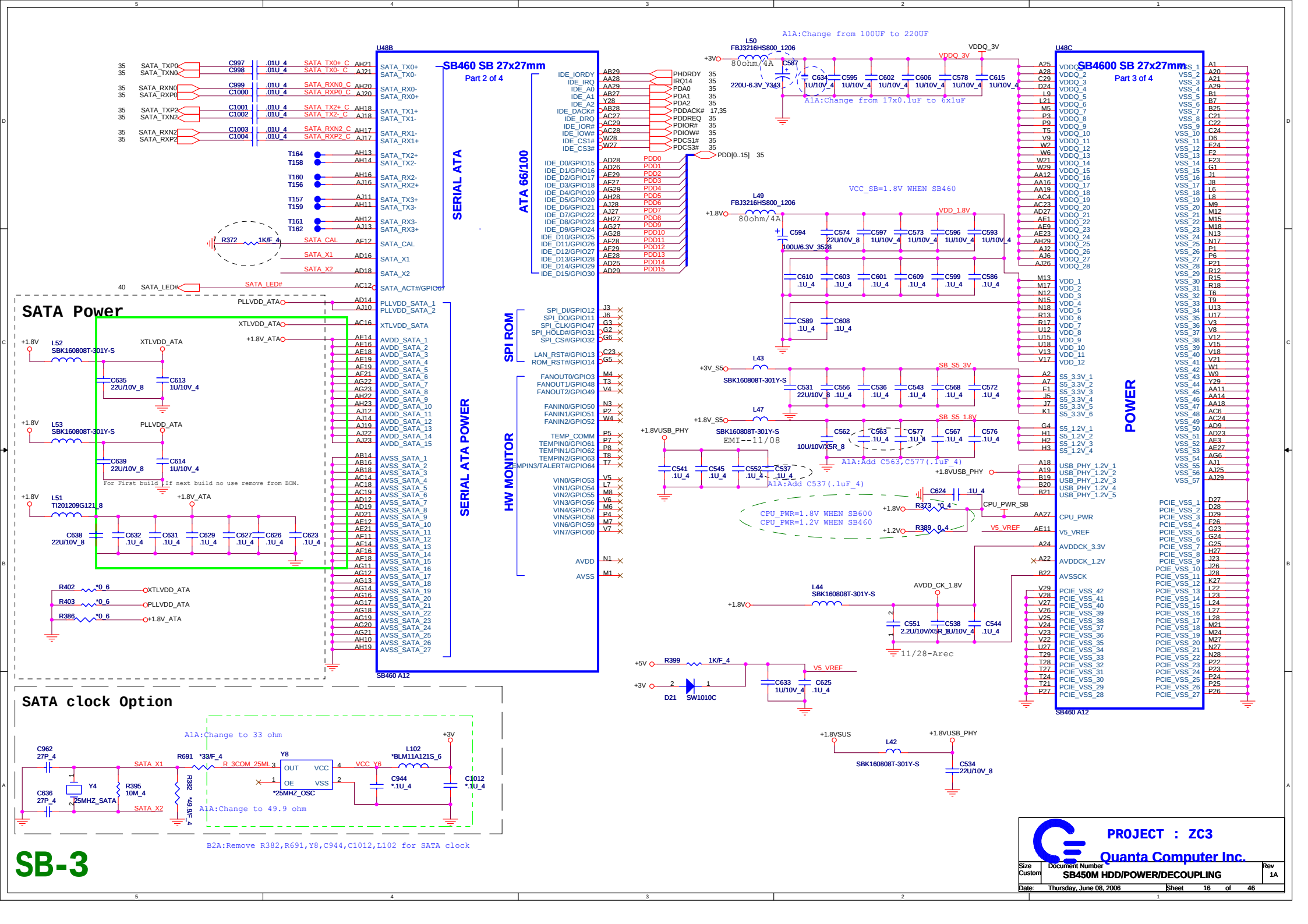


CPU FAN

	PROJECT : ZC3 Quanta Computer Inc.	
Size	Document Number Thermal Sensor,FAN	Rev 1A
Date: Thursday, June 08, 2006	Sheet 13 of 46	


SB460 SB 27x27mm
Part 1 of 4
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
CPU
LPC
RTC
SB460 A12
PCIE Power
RTC
SB-1
B2A:for EMI stuff
c945,c929,c948,c953,c932
Reserved For EMI
16mA
SB CALIBRATION RESISITOR VALUE
SB600
SB460
R1735 562 OHM 1% 150 OHM 1%
R1737 2.05K 1% 150 OHM 1%
R1738 0 ohm 4.12K 1%
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
FOR SB460, R5047=5.1M
ATI recommand have internal pull-up
FOR SB600, CONNECT TO CPU_PG/LDT_PG
FOR SB460, CONNECT TO SSMUXSEL/GPIO0
FOR SB460, THIS BALL IS LDT_RST# ONLY
FOR SB460, THIS BALL IS SPDIF_OUT/GPIO41 ONLY
FOR SB460, THIS BALL IS LDRQ1 ONLY
FOR SB460, THIS BALL IS BMREQ# ONLY
A1A:Change from 100 ohm to 1k
A1A:Don't implement DPSLP#,PD 10k
B2A:Stuff R388(8.2K_4) for INTH#
C3A:disconnect PCI_LOCK#
Add for debug.
A1A:BMREQ# don't need pull high
Unmount R5131
LPC PULL UP(SB460 ONLY)
PCI DEVICE IDSEL# REQ# / GNT# Interrupts CLOCK
TI 7412 AD25 REQ0# / GNT0# INTE#,F#,G# PCICLK2
BCM5788M AD20 REQ2# / GNT2# INTH# PCICLK5
PROJECT : ZC3
Quanta Computer Inc.
SB460M PCIE/PCI/CPU/LPC I/F
Size Custom
Rev 1A
Date: Thursday, June 08, 2006
Sheet 14 of 46


SB460 SB 27x27mm
Part 4 of 4
U48D
SB460 A12
PU/PD SB460 ONLY
ACPI / WAKE UP EVENTS
USB INTERFACE
OSC / RST
GPIO
USB OC
AZALIA
AC97
USB PWR
Delay 20ms after S5 powerOK
BALLS(C6 AND C5) ARE FOR SB600 ONLY (NC FOR SB460)
B2A:add new card detect pin to A6
B2A:Delete SYS_RST#
B2A:change pin form C28 to E23
B2A:default pull low
If throttling from SM remove R264
SB460 ONLY
A1A:Stuff R324 AMD CPU-CPU speed issue
SB600 ONLY(NC for SB460)
USB0: M/B IO
USB1: M/B IO
USB2: D/B IO
USB3: D/B IO
USB4:
USB5: NEW CARD
USB6: BLUETOOTH
USB7: CAMERA
USB power
USB power use S3 power,But Over current signal datasheet is S5 only,But ATI FAE say use S3 is ok
Board ID | ID1 | ID0
00 | 0 | 0 | Normal
01
10
11
PROJECT : ZC3
Quanta Computer Inc.
SB460M ACPI/GPIO/USB/AC97
Size Custom
Rev 1A
Date: Thursday, June 08, 2006
Sheet 15 of 46
SB-2


SB460 SB 27x27mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
SATA Power
SATA clock Option
SB460 A12
SB4600 SB 27x27mm
Part 3 of 4
POWER
A1A:Change from 100UF to 220UF
A1A:Change from 17x0.1uF to 6x1uF
VCC_SB=1.8V WHEN SB460
A1A:Add C563,C577(.1uF_4)
A1A:Add C537(.1uF_4)
CPU_PWR=1.8V WHEN SB600
CPU_PWR=1.2V WHEN SB460
11/28-Arec
A1A:Change to 33 ohm
A1A:Change to 49.9 ohm
B2A:Remove R382,R691,Y8,C944,C1012,L102 for SATA clock
For First build If next build no use remove from BOM.
SB-3
PROJECT : ZC3
Quanta Computer Inc.
SB450M HDD/POWER/DECOUPLING
Thursday, June 08, 2006
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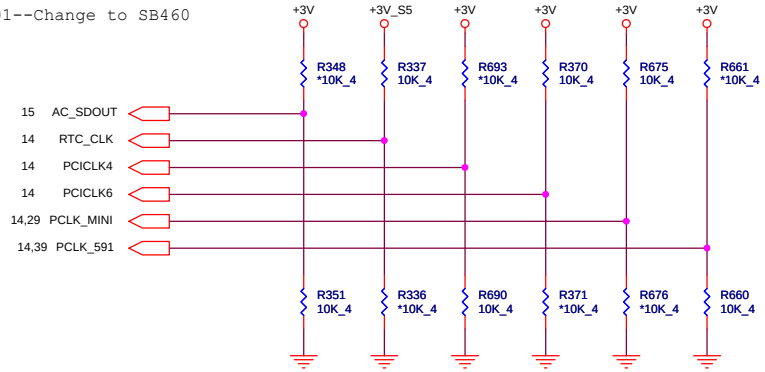
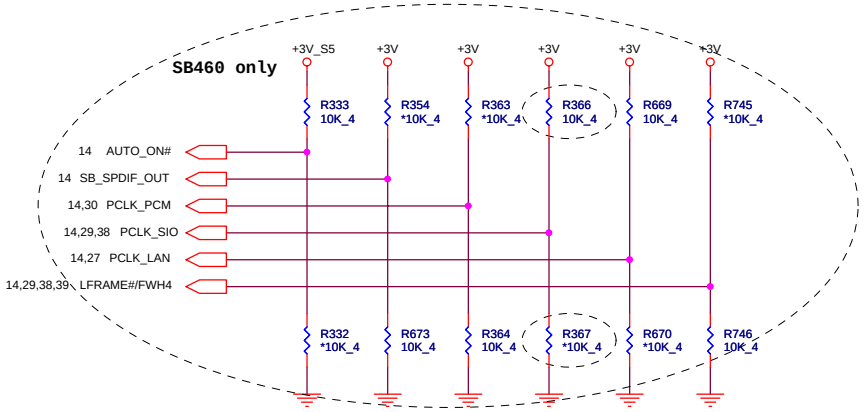
Edison-11/01--Change to SB460





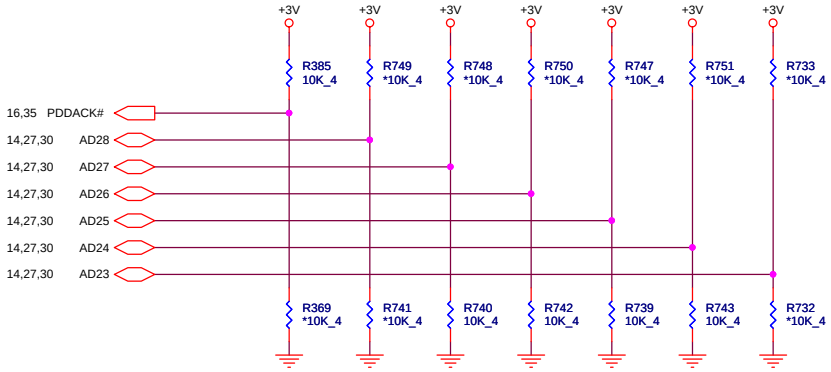
A1A:USB PHY POWERDOWN DISABLE

REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCLK_591
					PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM L, H = LPC TYPE II ROM DEFAULT L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]

	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET LOW DEFAULT	ENABLE THERMTRIP# DEFAULT
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HIGH	DISABLE THERMTRIP#

BIOS ENABLE AFTER STARTUP



10K IF USED FOR SB460

DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

SB460 only SB600 only

SB-4

PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB460M STRAPS	1A
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PCIE TEST PADS
PCIE TEST POINTS MUST BE WITHIN 250 MILS
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE
SIGNALS THE SAME DISTANCE

10 PEG_RXP[15:0]
10 PEG_RXN[15:0]
10 PEG_TXP[15:0]
10 PEG_TXN[15:0]

A1A:PCI-E 16X LAN are Swap

U38A

PART 1 OF 7

PEG_TXP15	AJ31	PCIE_RX0P	AK27	PCIE_TX0P	V_GMCHEXP_RXP15	C123	EV@.1U-10V_4	PEG_RXP15
PEG_TXN15	AH31	PCIE_RX0N	AJ27	PCIE_TX0N	V_GMCHEXP_RXN15	C130	EV@.1U-10V_4	PEG_RXN15
PEG_TXP14	AH30	PCIE_RX1P	AJ25	PCIE_TX1P	V_GMCHEXP_RXP14	C127	EV@.1U-10V_4	PEG_RXP14
PEG_TXN14	AG30	PCIE_RX1N	AH25	PCIE_TX1N	V_GMCHEXP_RXN14	C132	EV@.1U-10V_4	PEG_RXN14
PEG_TXP13	AG32	PCIE_RX2P	AH28	PCIE_TX2P	V_GMCHEXP_RXP13	C133	EV@.1U-10V_4	PEG_RXP13
PEG_TXN13	AF32	PCIE_RX2N	AG28	PCIE_TX2N	V_GMCHEXP_RXN13	C138	EV@.1U-10V_4	PEG_RXN13
PEG_TXP12	AF31	PCIE_RX3P	AG27	PCIE_TX3P	V_GMCHEXP_RXP12	C137	EV@.1U-10V_4	PEG_RXP12
PEG_TXN12	AE31	PCIE_RX3N	AF27	PCIE_TX3N	V_GMCHEXP_RXN12	C143	EV@.1U-10V_4	PEG_RXN12
PEG_TXP11	AE30	PCIE_RX4P	AF25	PCIE_TX4P	V_GMCHEXP_RXP11	C145	EV@.1U-10V_4	PEG_RXP11
PEG_TXN11	AD30	PCIE_RX4N	AE25	PCIE_TX4N	V_GMCHEXP_RXN11	C151	EV@.1U-10V_4	PEG_RXN11
PEG_TXP10	AD32	PCIE_RX5P	AE28	PCIE_TX5P	V_GMCHEXP_RXP10	C155	EV@.1U-10V_4	PEG_RXP10
PEG_TXN10	AC32	PCIE_RX5N	AD28	PCIE_TX5N	V_GMCHEXP_RXN10	C167	EV@.1U-10V_4	PEG_RXN10
PEG_TXP9	AC31	PCIE_RX6P	AD27	PCIE_TX6P	V_GMCHEXP_RXP9	C160	EV@.1U-10V_4	PEG_RXP9
PEG_TXN9	AB31	PCIE_RX6N	AC27	PCIE_TX6N	V_GMCHEXP_RXN9	C174	EV@.1U-10V_4	PEG_RXN9
PEG_TXP8	AB30	PCIE_RX7P	AC25	PCIE_TX7P	V_GMCHEXP_RXP8	C180	EV@.1U-10V_4	PEG_RXP8
PEG_TXN8	AA30	PCIE_RX7N	AB25	PCIE_TX7N	V_GMCHEXP_RXN8	C188	EV@.1U-10V_4	PEG_RXN8
PEG_TXP7	AA32	PCIE_RX8P	AB28	PCIE_TX8P	V_GMCHEXP_RXP7	C181	EV@.1U-10V_4	PEG_RXP7
PEG_TXN7	Y32	PCIE_RX8N	AA28	PCIE_TX8N	V_GMCHEXP_RXN7	C190	EV@.1U-10V_4	PEG_RXN7
PEG_TXP6	Y31	PCIE_RX9P	AA27	PCIE_TX9P	V_GMCHEXP_RXP6	C192	EV@.1U-10V_4	PEG_RXP6
PEG_TXN6	W31	PCIE_RX9N	Y27	PCIE_TX9N	V_GMCHEXP_RXN6	C199	EV@.1U-10V_4	PEG_RXN6
PEG_TXP5	W30	PCIE_RX10P	Y25	PCIE_TX10P	V_GMCHEXP_RXP5	C197	EV@.1U-10V_4	PEG_RXP5
PEG_TXN5	V30	PCIE_RX10N	W25	PCIE_TX10N	V_GMCHEXP_RXN5	C203	EV@.1U-10V_4	PEG_RXN5
PEG_TXP4	V32	PCIE_RX11P	W28	PCIE_TX11P	V_GMCHEXP_RXP4	C211	EV@.1U-10V_4	PEG_RXP4
PEG_TXN4	U32	PCIE_RX11N	V28	PCIE_TX11N	V_GMCHEXP_RXN4	C219	EV@.1U-10V_4	PEG_RXN4
PEG_TXP3	U31	PCIE_RX12P	V27	PCIE_TX12P	V_GMCHEXP_RXP3	C214	EV@.1U-10V_4	PEG_RXP3
PEG_TXN3	T31	PCIE_RX12N	U27	PCIE_TX12N	V_GMCHEXP_RXN3	C223	EV@.1U-10V_4	PEG_RXN3
PEG_TXP2	T30	PCIE_RX13P	U25	PCIE_TX13P	V_GMCHEXP_RXP2	C230	EV@.1U-10V_4	PEG_RXP2
PEG_TXN2	R30	PCIE_RX13N	T25	PCIE_TX13N	V_GMCHEXP_RXN2	C241	EV@.1U-10V_4	PEG_RXN2
PEG_TXP1	R32	PCIE_RX14P	T28	PCIE_TX14P	V_GMCHEXP_RXP1	C236	EV@.1U-10V_4	PEG_RXP1
PEG_TXN1	P32	PCIE_RX14N	R28	PCIE_TX14N	V_GMCHEXP_RXN1	C243	EV@.1U-10V_4	PEG_RXN1
PEG_TXP0	P31	PCIE_RX15P	R27	PCIE_TX15P	V_GMCHEXP_RXP0	C253	EV@.1U-10V_4	PEG_RXP0
PEG_TXN0	N31	PCIE_RX15N	P27	PCIE_TX15N	V_GMCHEXP_RXN0	C256	EV@.1U-10V_4	PEG_RXN0

P C I - E X P R E S S I N T E R F A C E

Clock

2 CLK_PCIE_M56 → AL28 PCIE_REFCLKP
2 CLK_PCIE_M56# → AK28 PCIE_REFCLKN

Calibration

PCIE_CALRN: AE24 — R155 EV@2K/F_4 — +1.2V_VPCIE
PCIE_CALRP: AD24 — R135 EV@562/F_4
PCIE_CALI: AB24 — R144 EV@1.47K/F_4

A1A:PCIE_CALRN(ball AE24) need change to +1.2V_VPCIE

11,14,29,32,33,34,38,39 ALINK_RST# → ALINK_RST# R562 0_4 → PLTRST# M56 → AG24 PERSTB

T15 → PCIE_TEST → AA24 PCIE_TEST

AF24 PERSTB_MASK — Tie To VSS

EV@M56-P B26

FOR M52P,M54P,M56P
PCIE_CALRN = 2K
PCIE_CALRP = 562R
PCIE_CALI = 1.47K

Change M56 to B26 version

PROJECT : ZC3

Quanta Computer Inc.

Size	Document Number	Rev
	M56P 1 OF 7	1A
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MEMORY CLOCK SPREAD SPECTRUM

ANY UNUSED GPIO CAN OPTIONALLY BE MEMORY TYPE CONFIG STRAPS

For HDMI use

A1A:Change memory type straps to DVPDATA[3:0]

B2A:remove R90,R101,R102,R103

A1A:Change R103,R90,R101,R102 from 330 to 180 for TMDS

Voltage divider resistor values R181 and R551 to ensure XTALIN/XTALOUT voltage level matches vddc

A1A:Reversed LVDSCLK,LVDSDATA pull high to LVDS side

A1A:Change LVDS_DAT/LVDS_CLK to DVPDATA18/DVPDATA19

A1A:Add pull low 10k GPIO15 HI = 1.0V VDDC GPIO15 LO = 1.1V VDDC

V_PWRCNTL DRIVEN HI SELECT 1.0V VDDC
V_PWRCNTL DRIVEN LO SELECT 1.1V VDDC

For m26x,m52p,m54p,m56p thermal interrupt is low edge and connects to gpio17

A1A:Reserved for VREFG

FOR M52P,M54P,M56P CONNECT TO +2.5V

1.2V OR 1.0V @ 20MA ASIC MPVDD CONNECT TO VDDC

FOR M52P,M54P,M56P CONNECT TO +2.5V

FOR M52P,M54P,M56P A2VDDQ IT IS NO CONNECT

FOR M52P,M54P,M56P CONNECT TO +2.5V

PLACE CLOSE TO ASIC

A1A:Add R124,R83,R104,R118,R119,R126 (150 ohm) for CRT/TV can't detect issue

HDMI hot plug

The DDC2 is for DVI (TMDS) reading EDID data, which cannot be shared with other I2C devices.

HDMI upgrade f/w

FOR M52P,M54P,M56P GENERICC IT IS GPIO

10 mil trace / 10 mil space

Close to pin ASIC

SLAVE ADDRESS: 9A

A1A:Connect U18 OVERT to fan driver

A1A:Reserve for VGA thermal sensor

A1A:Change R81,R91 to 10K to resolve Battery can't learning issue

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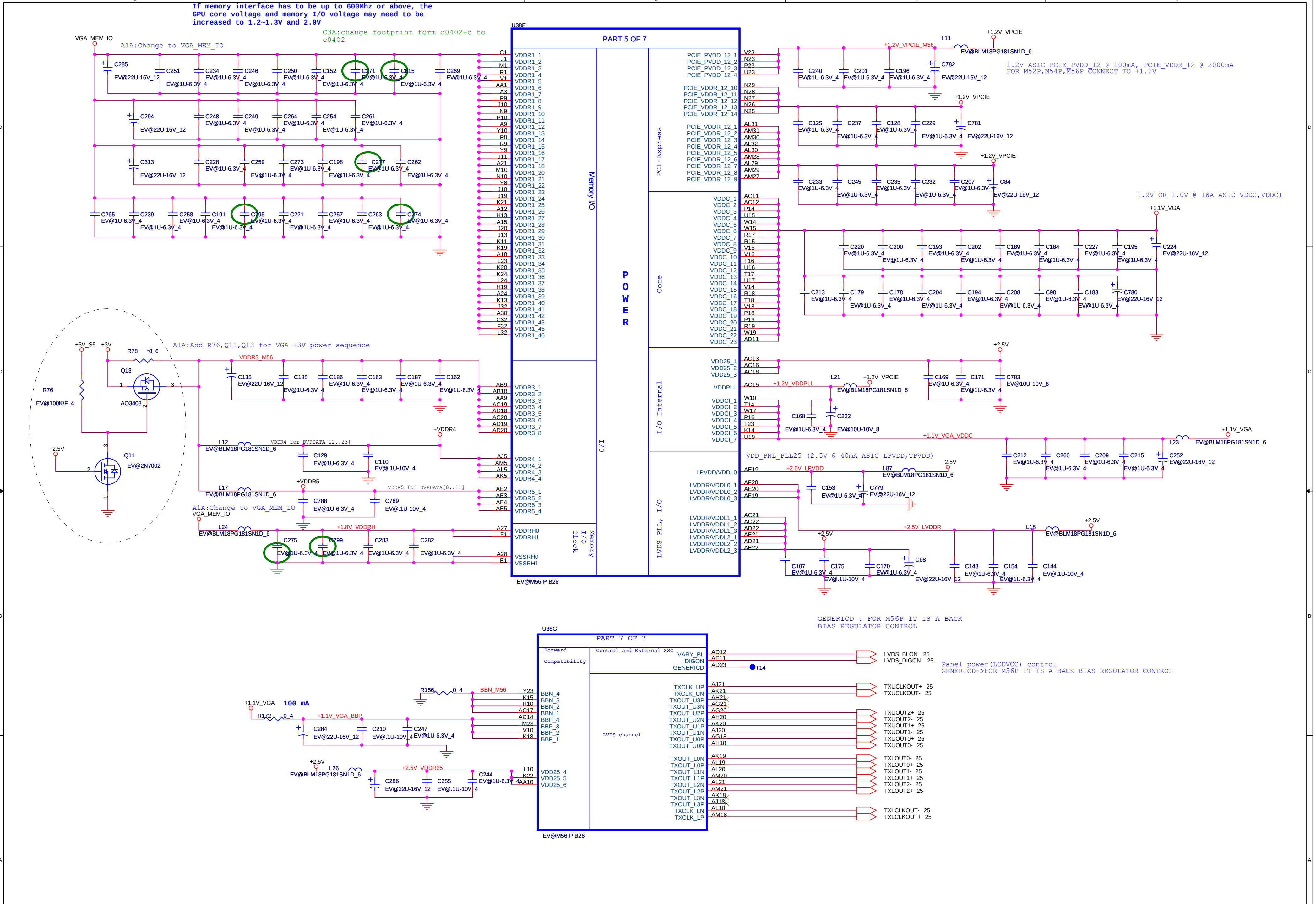
Quanta Computer Inc.



PROJECT : ZC3

Quanta Computer Inc.

Size	Document Number	Rev
	M56P POWER	1A

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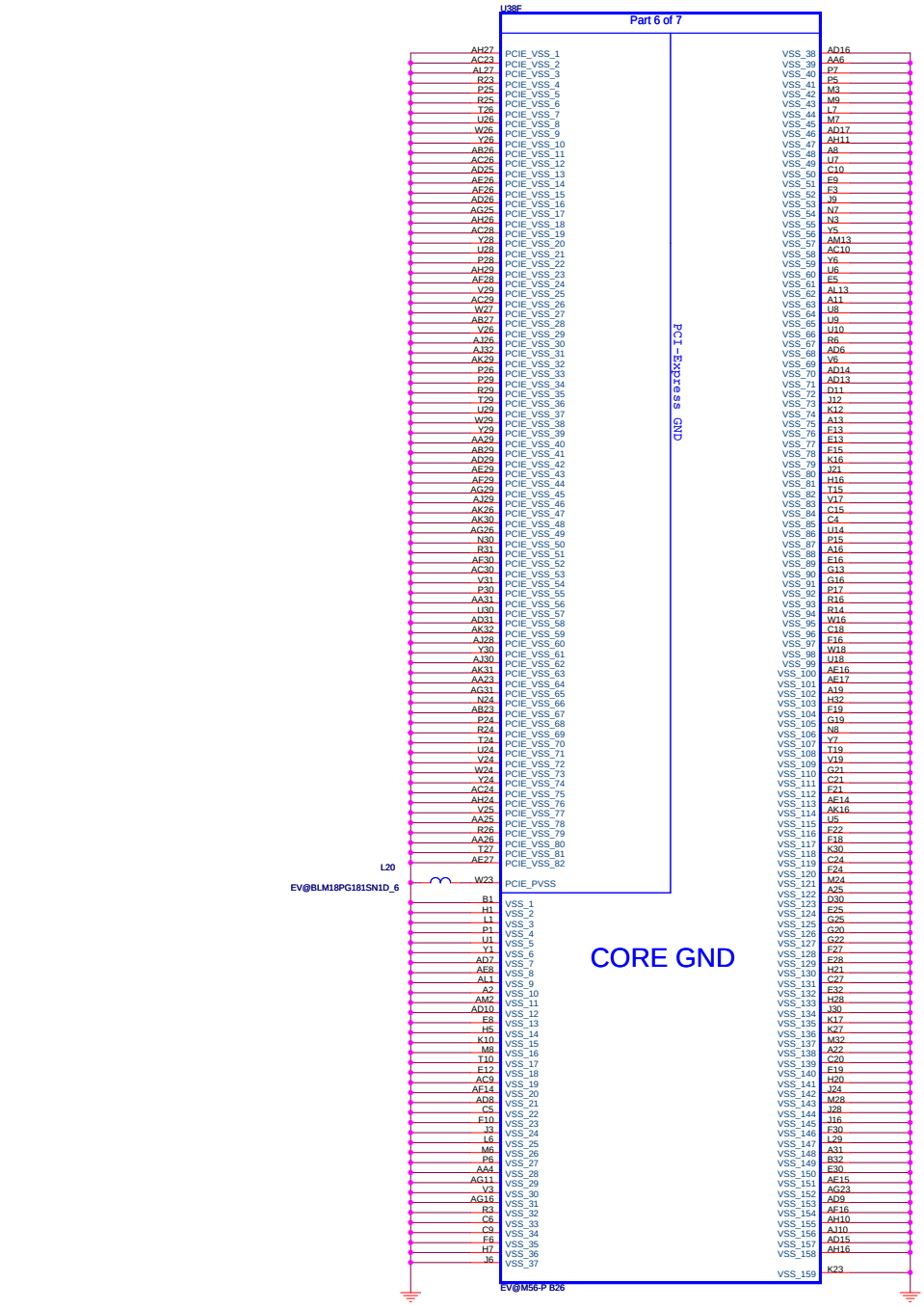

PROJECT : ZC3		
Quanta Computer Inc.		
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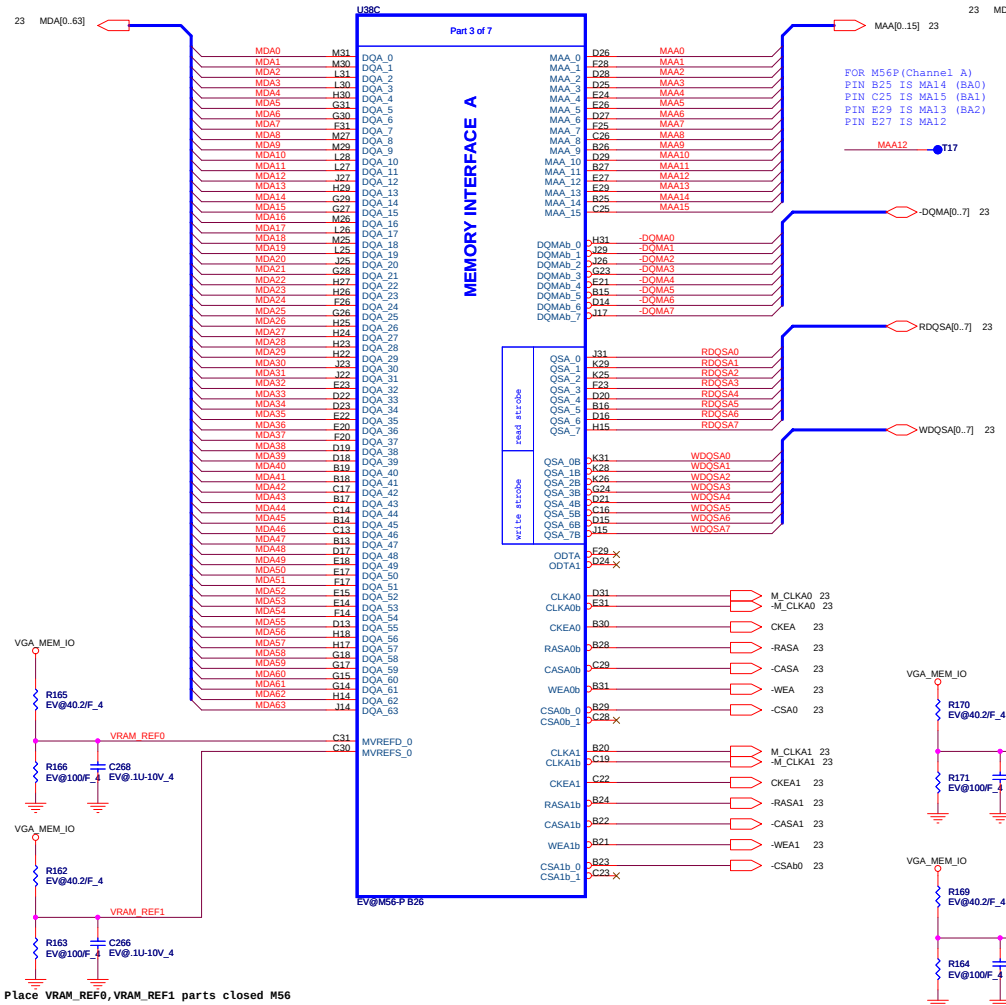
RV410 MEMORY CHANNELS A and B

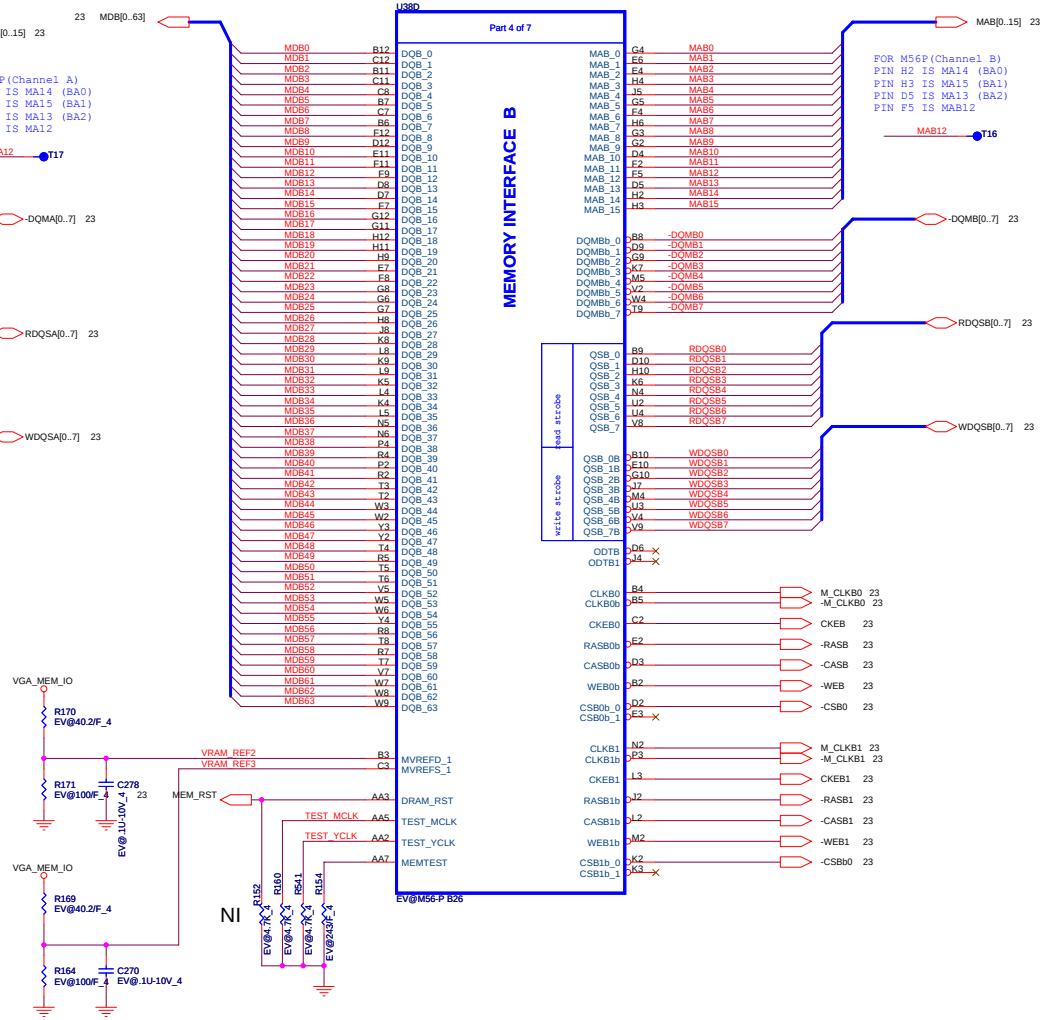
Channel A



Place VRAM_REF0,VRAM_REF1 parts closed M56

Reference voltage per channel (memory data/strobe)
MVREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVREFS_[0:1] (0.7 * VDDR1) (for GDDR3)

Channel B



Reference voltage per channel (memory data/strobe)
MVREFD_[0:1] (0.7 * VDDR1) (for GDDR3)
MVREFS_[0:1] (0.7 * VDDR1) (for GDDR3)

PROJECT : ZC3
Quanta Computer Inc.

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	M56P 3/4 OF 7	1A

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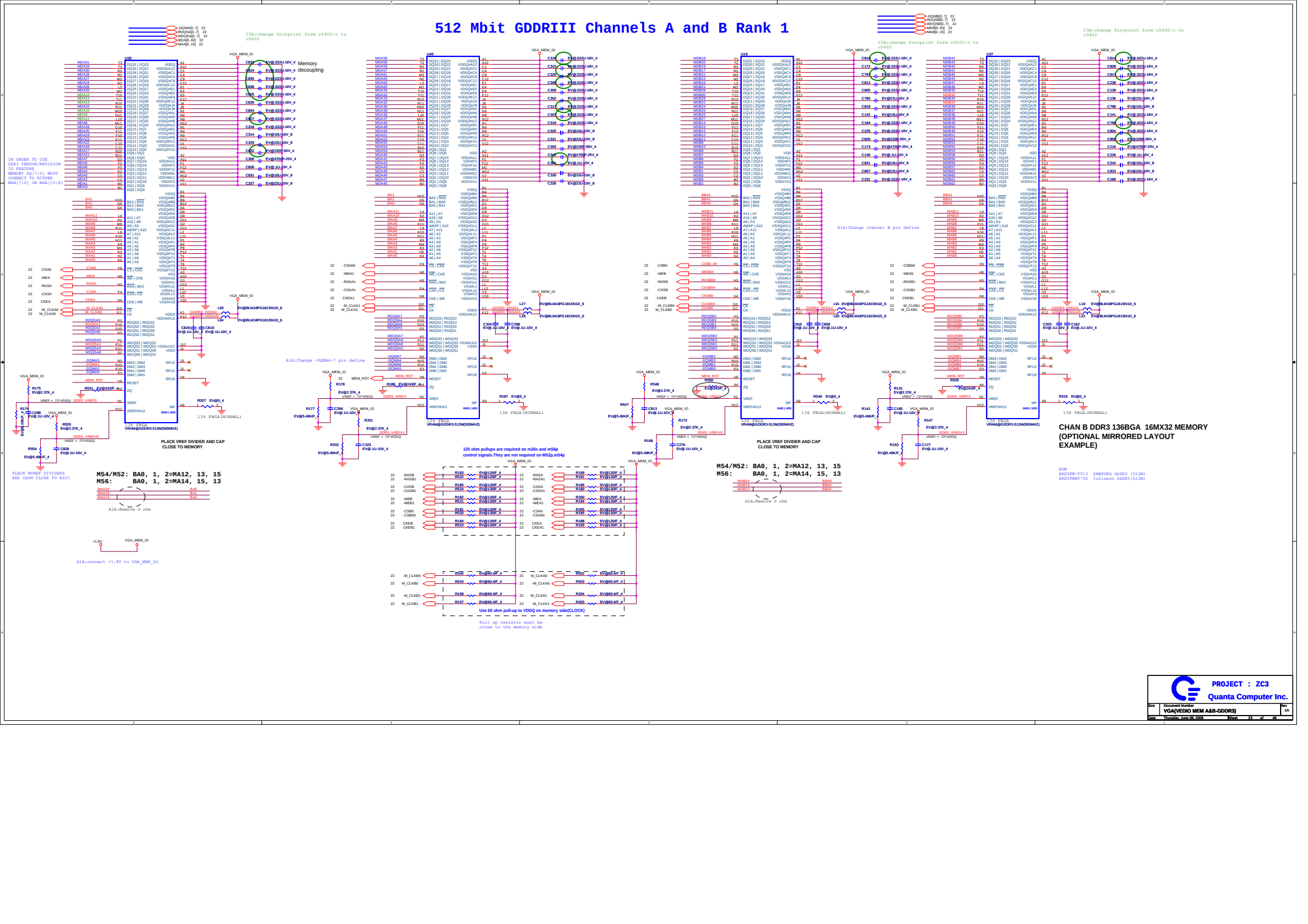
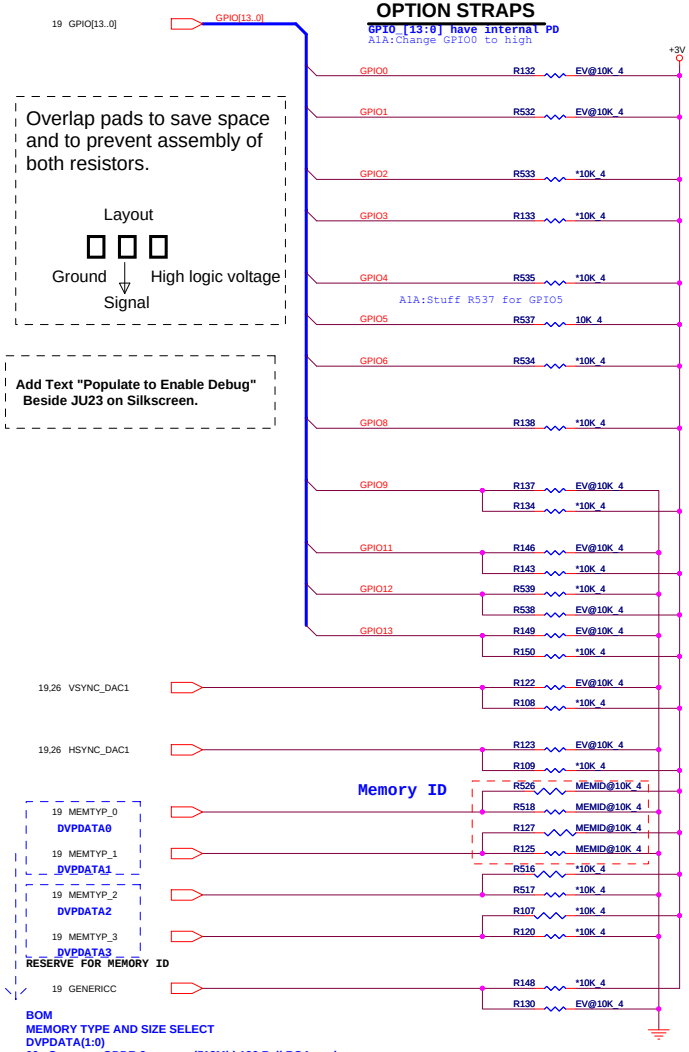
512 Mbit GDDRIII Channels A and B Rank 1



OPTION STRAPS

GPIO_[13:0] have internal PD
A1A:Change GPIO0 to high



Overlap pads to save space and to prevent assembly of both resistors.

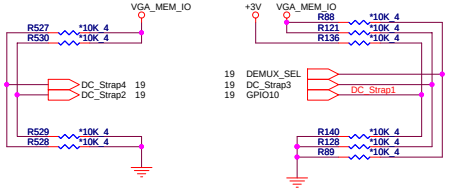
Layout

Ground — High logic voltage

Signal

Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.

BOM
MEMORY TYPE AND SIZE SELECT
DVPDATA(1:0)
00 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package
01 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package
10 - Hynix GDDR 3 memory(512Mb) 136 Ball BGA package
11 - Reserved



A1A:change video capture enable setting

M56-P Strap

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE FOR M26X,M50P: INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS DO NOT INSTALL WITH INTEL 915PM CHIPSET FOR M5X - INSTALL	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE RSVD	GPIO5	sets the desired PCIE PLL bandwidth for M5x parts	DO NOT INSTALL 10K RESISTOR
COMMON MODE RANGE	GPIO6	NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO(9,13:11)	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE 000x - No ROM, MEM_AP_SIZE=00(128MB) 001x - No ROM,MEM_AP_SIZE=01(256MB) 010x - No Rom, MEM_AP_SIZE=10(64MB) 011x - No ROM,MEM_AP_SIZE=11(Reserved) 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	A1A:change ROMIDCFG(3:0) to 0010
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	No default
NO STRAP FUNCTION	H2SYNC, V2SYNC,GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

Board Straps REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	DVPDATA(1:0)	MEMORY TYPE AND SIZE SELECT->DVPDATA(1:0) 00 - Samsung GDDR 3 memory(512Mb) 136 Ball BGA package 01 - Infineon GDDR 3 memory(512Mb) 136 Ball BGA package 10 - Hynix GDDR 3 memory(512Mb) 136 Ball BGA package 11 - Reserved	00
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Enabled	1
DC_Strap3	LCDDATA(14)	HDTV out detect 0 - Detected **1 - Not detected**	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT **10 - DAC2 On as TVOUT** 11 - DAC2 On as TVOUT and CRT	10
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1

MEMORY TYPE AND SPEED SELECT

PROJECT : ZC3
Quanta Computer Inc.

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	M56P OPTION STRAPS	1A

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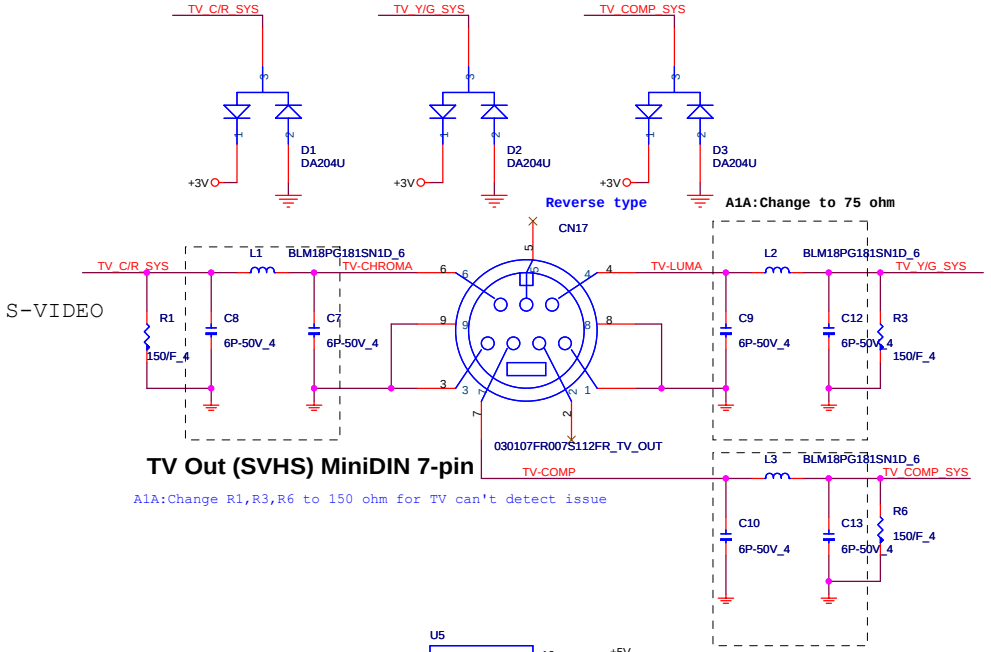
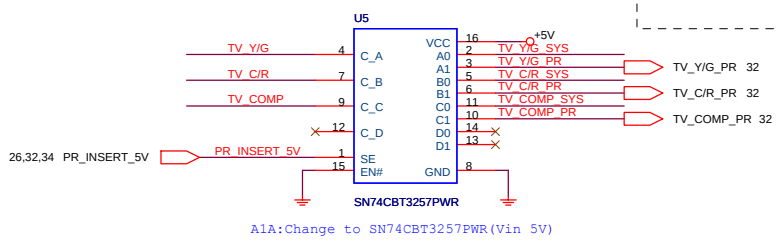
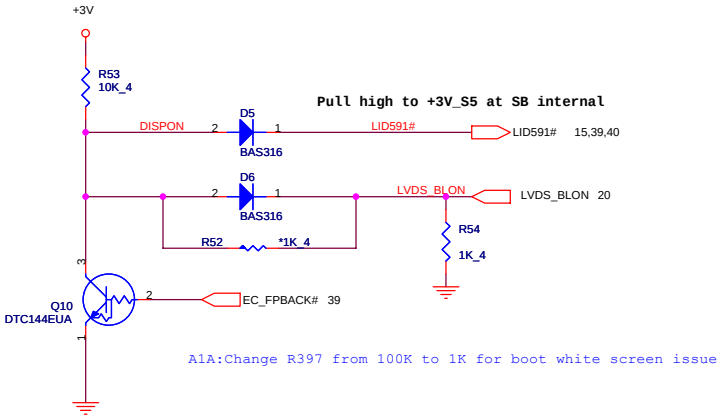
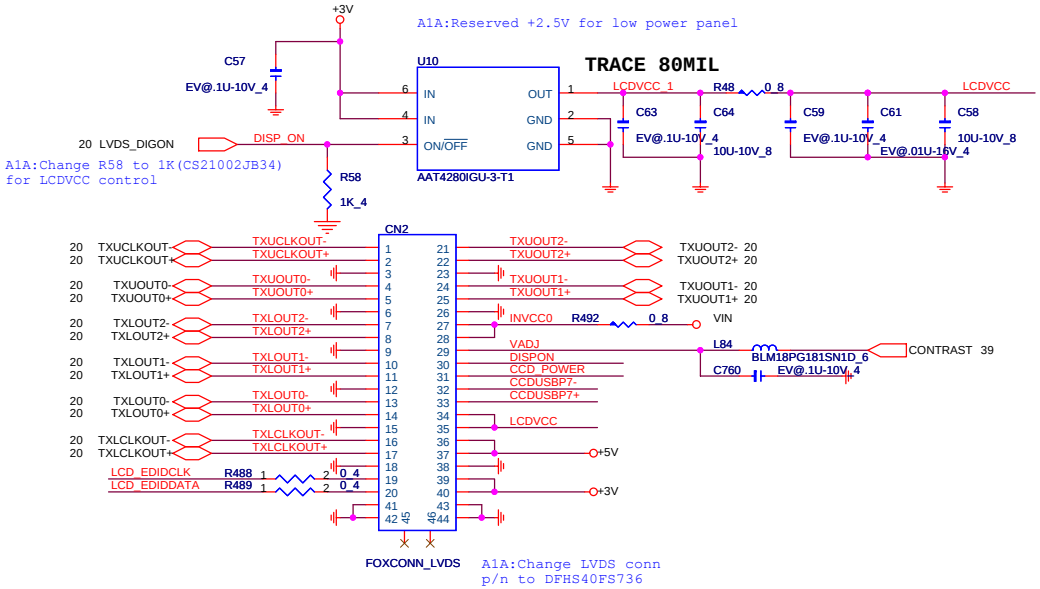
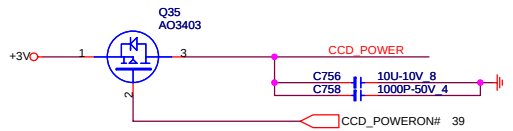
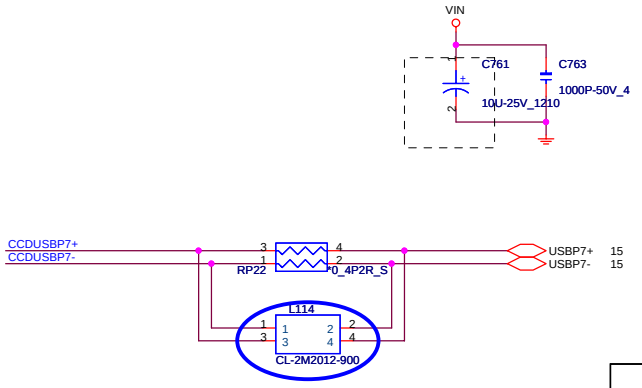


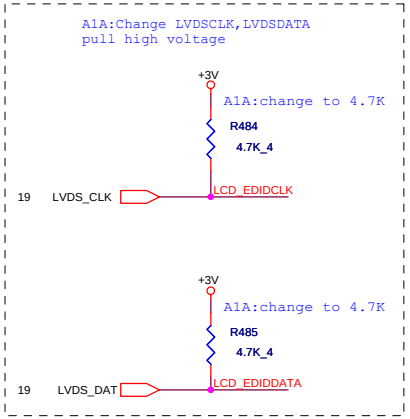








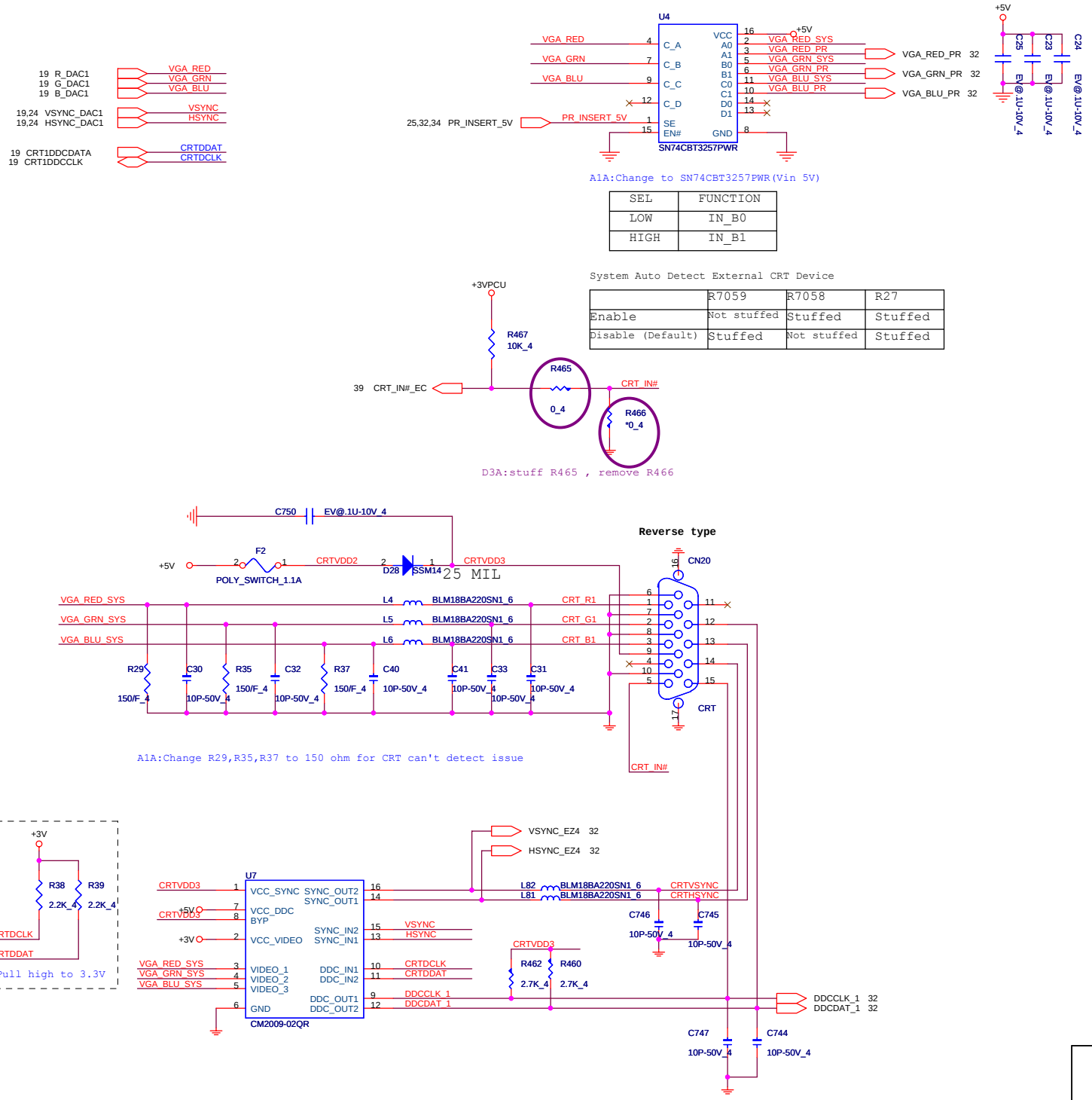




PROJECT : ZC3

Quanta Computer Inc.

Size	Document Number	Rev
	LVDS/TV-OUT CONNECTOR	1A
Date: Thursday, June 08, 2006	Sheet 25 of 46	



PROJECT :	ZC3
Quanta Computer Inc.	
Size	Document Number: CRT-PORT
Rev	1A
Date:	Thursday, June 08, 2006
Sheet	26 of 46

Voltage Rail	BCM5788MG
VDDIO_PCI	+3VRUN(PCI SW)
2.5V_LAN	2.5V
1.2V_LAN	1.2V

LAN
BCM5787MKFBG :
AD20 REQ2#
GNT2# INTF#

BCM5788MG

15mm x 15mm
BGA196

BCM 5788M LAN Power

LAN EEPROM

Stuff for 5705E&5788E&5787&5789

A1A:Change to AT24C128

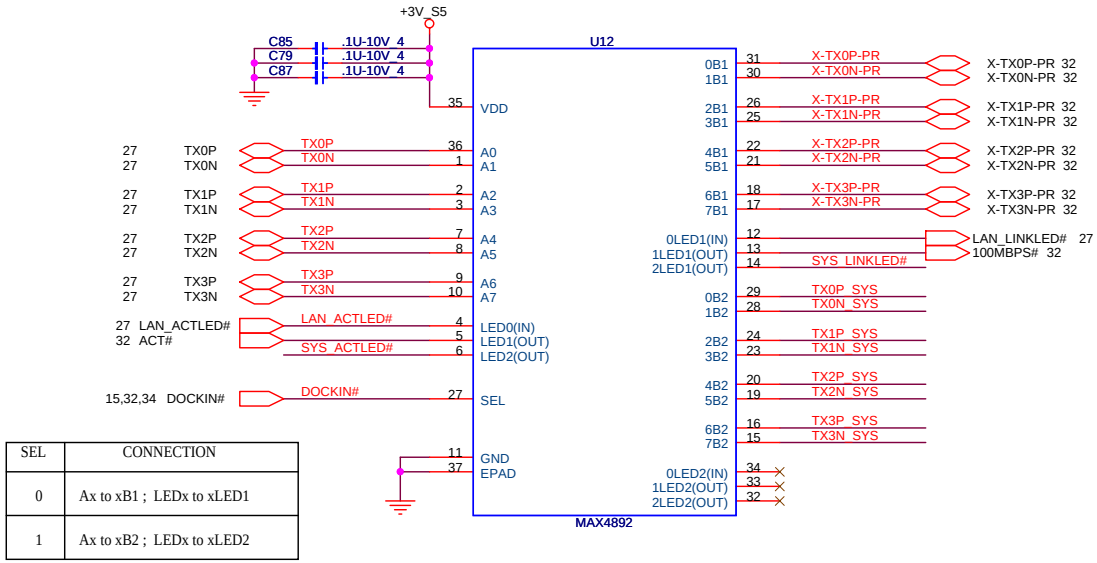
LAN PME

D3A:change form 1.24K to 1.18K

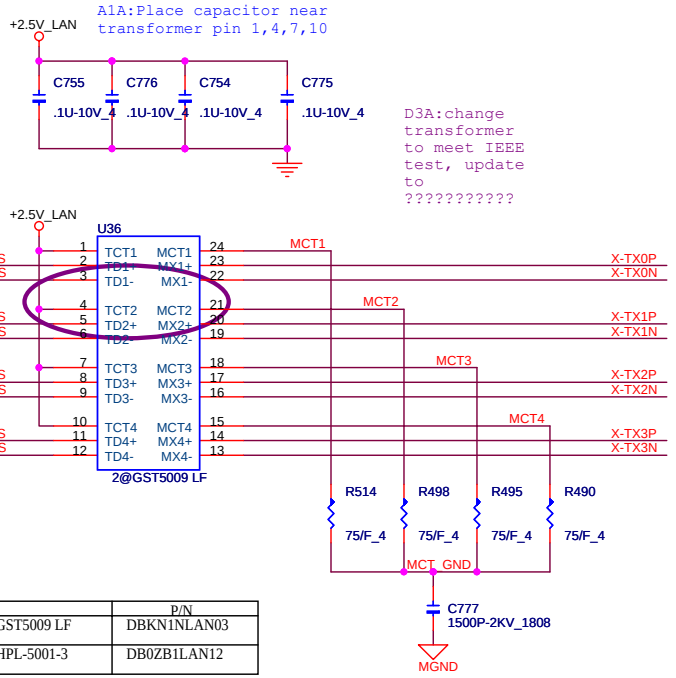
B2A:change to INTG#

A1A:Add C691,C1046,C689,C1007,C658 for +3V_S5

PROJECT : ZC3			
Quanta Computer Inc.			
Size	Document Number: BCM5788MG LAN		Rev: 1A
Date: Thursday, June 08, 2006	Sheet 27 of 46		



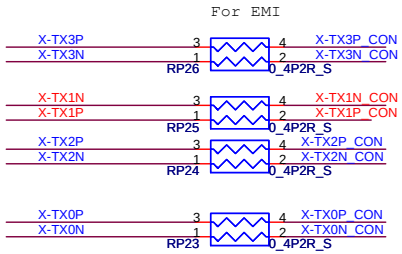
SEL	CONNECTION
0	Ax to xB1 ; LEDx to xLED1
1	Ax to xB2 ; LEDx to xLED2

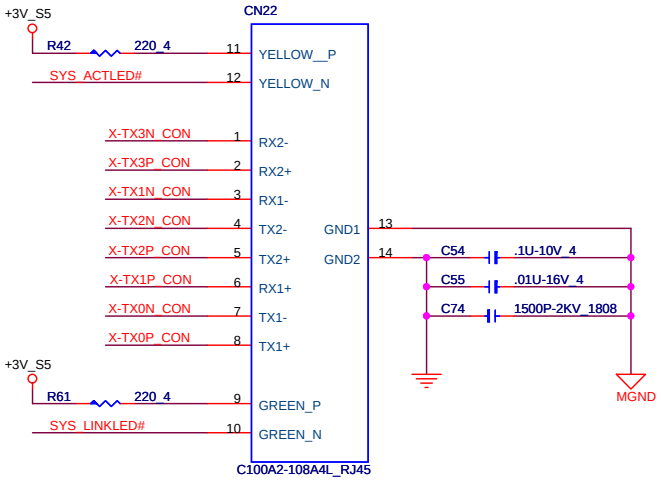


BOM

		P/N
帛漢	GST5009 LF	DBKN1NLAN03
瀚荻	HPL-5001-3	DB0ZB1LAN12

A1A:Change RJ45 CONN to C100A2-108A4L
A1A:Change RJ45 TX,RX pin define





LED1	A1(+) A2(-)	ACT (Tx/Rx)	YELLOW BLINKING
LED2	B1(+) B2(-)	LINK 10/100/1000	GREEN

A1A:Add diode for 10/100M & 1000M led control

PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
	TRANSFORMER/RJ45	1A
Date: Thursday, June 08, 2006	Sheet 28 of 46	

Debug card interface

BOT contact

CN29

AD[15:0] 14,27,30

AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD11 AD13 AD15

CBE0# 14,27,30
CBE1# 14,27,30
CBE2# 14,27,30
CBE3# 14,27,30
PCIK_MINI PCLK_MINI 14,17
IRDY# IRDY# 14,27,30
TRDY# TRDY# 14,27,30
PCIRST# PCIRST# 14,27,30,31
GNT2# GNT2# 14,27
DEVSEL# DEVSEL# 14,27,30
FRAME# FRAME# 14,27,30

+3V +3V
+5V +5V
+5V
GND
GND

*AFHJ300-N2G1Z_DEBUG

C3A:remove PCI debug conn

B1A:These signals of reserve have be used by wileless module of Foxconn BG. These signals impact LPC. I remove signal line in order to solve the WLAN issue.

+3.3V:1000mA
3.3Vaux:330mA
+1.5V:500mA

A1A:Change mini card +3.3Vaux to +3VSUS

D3A:for acer request

L115 BLM18PG181SN1D_6

+3V_MINI +3V

C1077 10U-10V_8

+1.5V +3VSUS

Reserved for debug only

14,27,30,31 PCIRST# PCIRST# R811 *0_4
14,17,38 PCLK_SIO PCLK_SIO R812 *0_4

MiniCard/WLAN

CN21

51	Reserved	+3.3V	52
49	Reserved	GND	50
47	Reserved	+1.5V	48
45	Reserved	LED_WPAN#	46
43	Reserved	LED_WLAN#	44
41	Reserved	LED_WWAN#	42
39	Reserved	GND	40
37	Reserved	USB_D+	38
35	GND	USB_D-	36
33	PETp0	GND	34
31	PETn0	SMB_DATA	32
29	GND	SMB_CLK	30
27	GND	+1.5V	28
25	PERp0	GND	26
23	PERn0	+3.3Vaux	24
21	GND	PERST#	22
19	Reserved	Reserved	20
17	Reserved	GND	18
15	GND	Reserved	16
13	REFCLK+	Reserved	14
11	REFCLK-	Reserved	12
9	GND	Reserved	10
7	CLKREQ#	Reserved	8
5	Reserved	+1.5V	6
3	Reserved	GND	4
1	WAKE#	+3.3V	2

AS0B226-S80N-7F_MINI CARD(H=8.0)

A1A:Mini card WLAN LED low active

WIRELESS_LED 40

T100

PDAT_SMB 2,15,32,33
PCLK_SMB 2,15,32,33

ALINK_RST# 11,14,18,32,33,34,38,39
RF_EN 39

10 PCIE_TXP3
10 PCIE_TXN3
10 PCIE_RXP3
10 PCIE_RXN3

B1A: Stuff R243 for debug

2 CLK_PCIE_MINI_A
2 CLK_PCIE_MINI_A#
CLKREQ# WLAN

*0_4 R813 LFRAME#/FWH4 14,17,38,39
*0_4 R814 LAD3/FWH3 14,38,39
*0_4 R815 LAD2/FWH2 14,38,39
*0_4 R816 LAD1/FWH1 14,38,39
*0_4 R817 LAD0/FWH0 14,38,39

Reserved for debug only

B2A:Add R799,R800,R801,R802,R803,R804,R805 for debug port,place on uder CN21(BOT)

+3VSUS

R446 4.7K_4

15 PCIE_WAKE#

Q30 DTC144EUA

Pull up to +3V_S5 on ICH7

+3V

R805 *10K_4

CLKREQ# WLAN

CLKREQ# and WAKE# are open drain signal

BLUETOOTH MODULE CONNECTOR

A1A:Change BT CONN to 5 pin

+3VSUS

Q31 AO3403

L70 BK2125HS330_8

BT_POWER

C717 10U-10V_8
C716 1000P-50V_4

BT_POWERON# 39

CN32

15 USBP6+
15 USBP6-
40 BT_LED

R441 0_4
R440 0_4

BUSBP4+
BUSBP4-
BT_LED

BT CONN(EIC 3702-E05C)

A1A:Reserve for EMI

USBP3- CON
USBP3+ CON
USBP2- CON
USBP2+ CON

C801 C800 C803 C802
*22P_4 *22P_4 *22P_4 *22P_4

B2A: for EMI stuff c707,c708

C707 10P_4
C708 10P_4

C1051 *.01U-16V_4

A1A:Change CN32 footprint to 3703-05-1-5p-1-zc1

A1A:In adapter mode, should be powered during S0~S5.
In battery only mode, should be powered during S0 and S3, and not powered during S5

80mil

+5V_S5

C811 .1U-10V_4

USBON# R546 0_4

U39 G528P1U

GND OUT 8
IN OUT 7
IN OUT 6
EN# OUTNC 5

80mil

USBPWR3

R544 *0_4

D3A:change to GMT , del MAX1930

MB USB PORT(REAR)

A1A:Change CN3 pin 4 to +5V_S5

C267 .1U-10V_4

CN3

RP2 0_4P2R_S +5V_S5

15 USBP3-
15 USBP3+
15 USBP2-
15 USBP2+

USBP3- CON
USBP3+ CON
USBP2- CON
USBP2+ CON

RP1 0_4P2R_S

88231-10001_USB/B

+5V_S5

C462 .1U-10V_4

USBON# R301 0_4

U25 G528P1U

GND OUT 8
IN OUT 7
IN OUT 6
EN# OUTNC 5

80mil

USBPWR1

R302 *0_4

MB USB PORT(RIGHT)

USBPWR1

C521 100U-6.3V_3528
C520 1000P-50V_4

CN8

15 USBP0-
15 USBP0+

R287 0_6
R283 0_6

BUSBP0-
BUSBP0+

C516 *22P_4
C508 *22P_4

020133MB004S557ZL_USB

U23 2@CM1293-04SO

CH1 CH4 6
VN VP 5 +5V_S5
CH2 CH3 4

USBPWR1

C451 100U-6.3V_3528
C453 1000P-50V_4

CN6

15 USBP1-
15 USBP1+

R275 0_6
R273 0_6

BUSBP1-
BUSBP1+

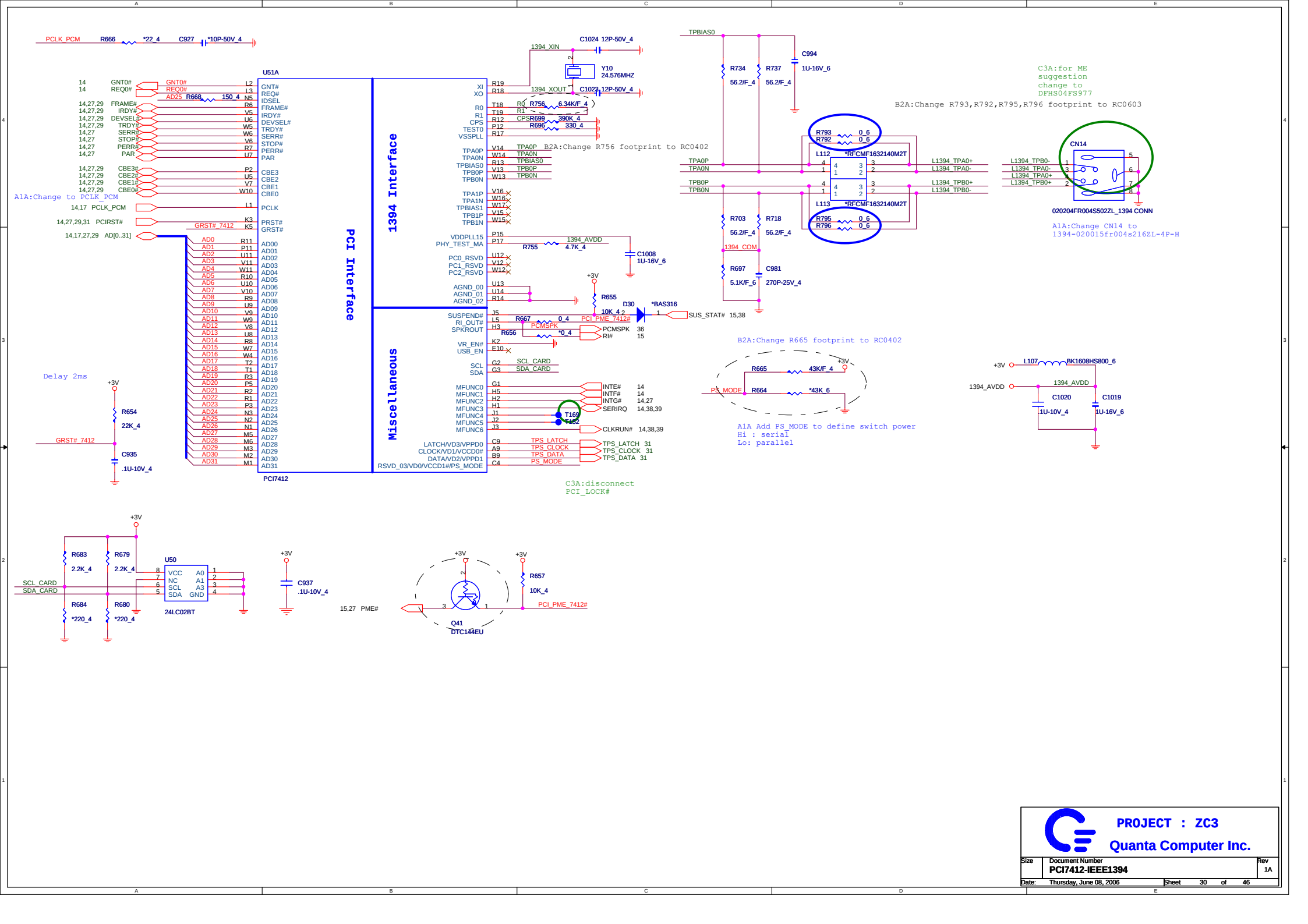
C428 *22P_4
C447 *22P_4

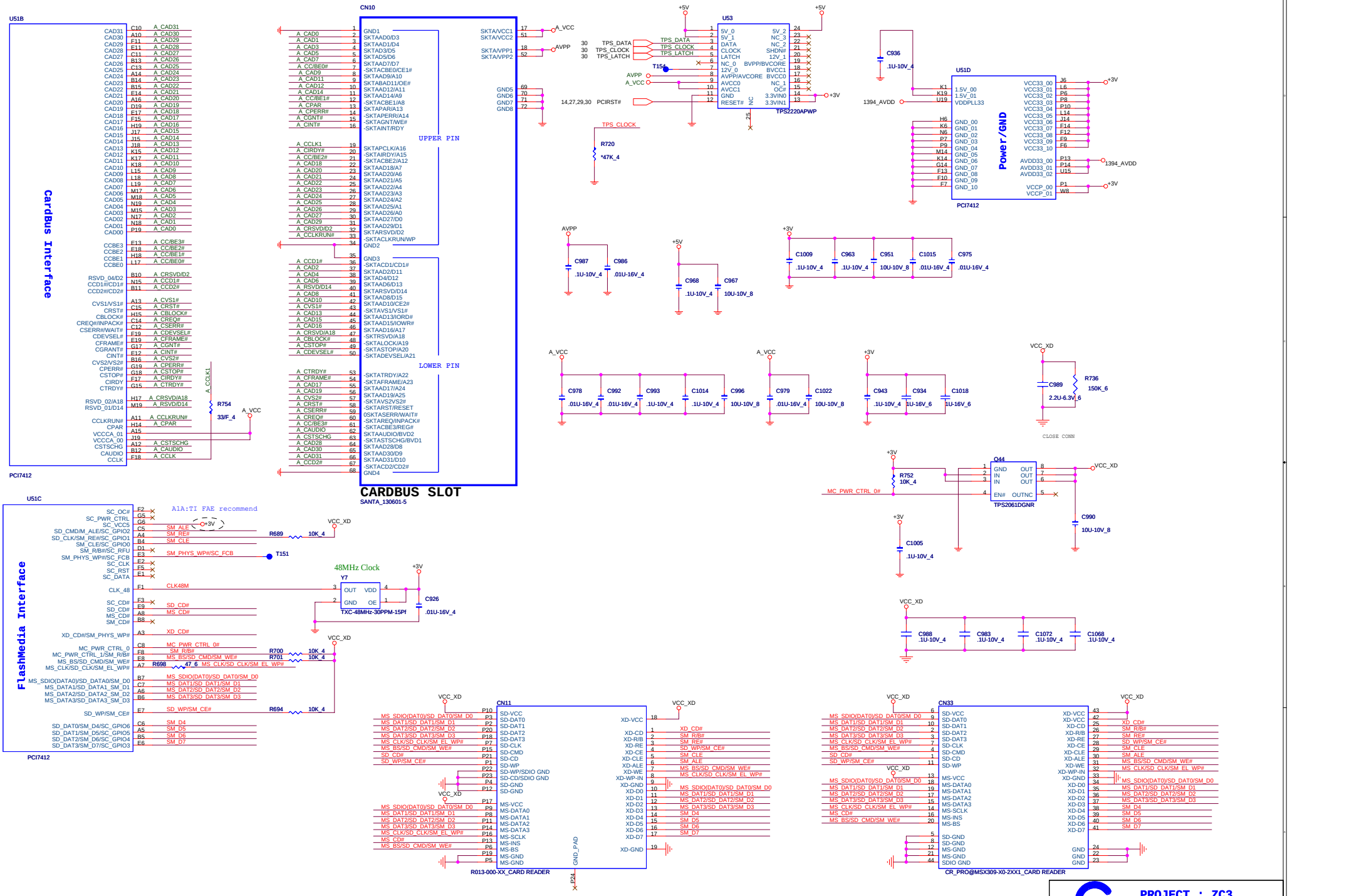
020133MB004S557ZL_USB

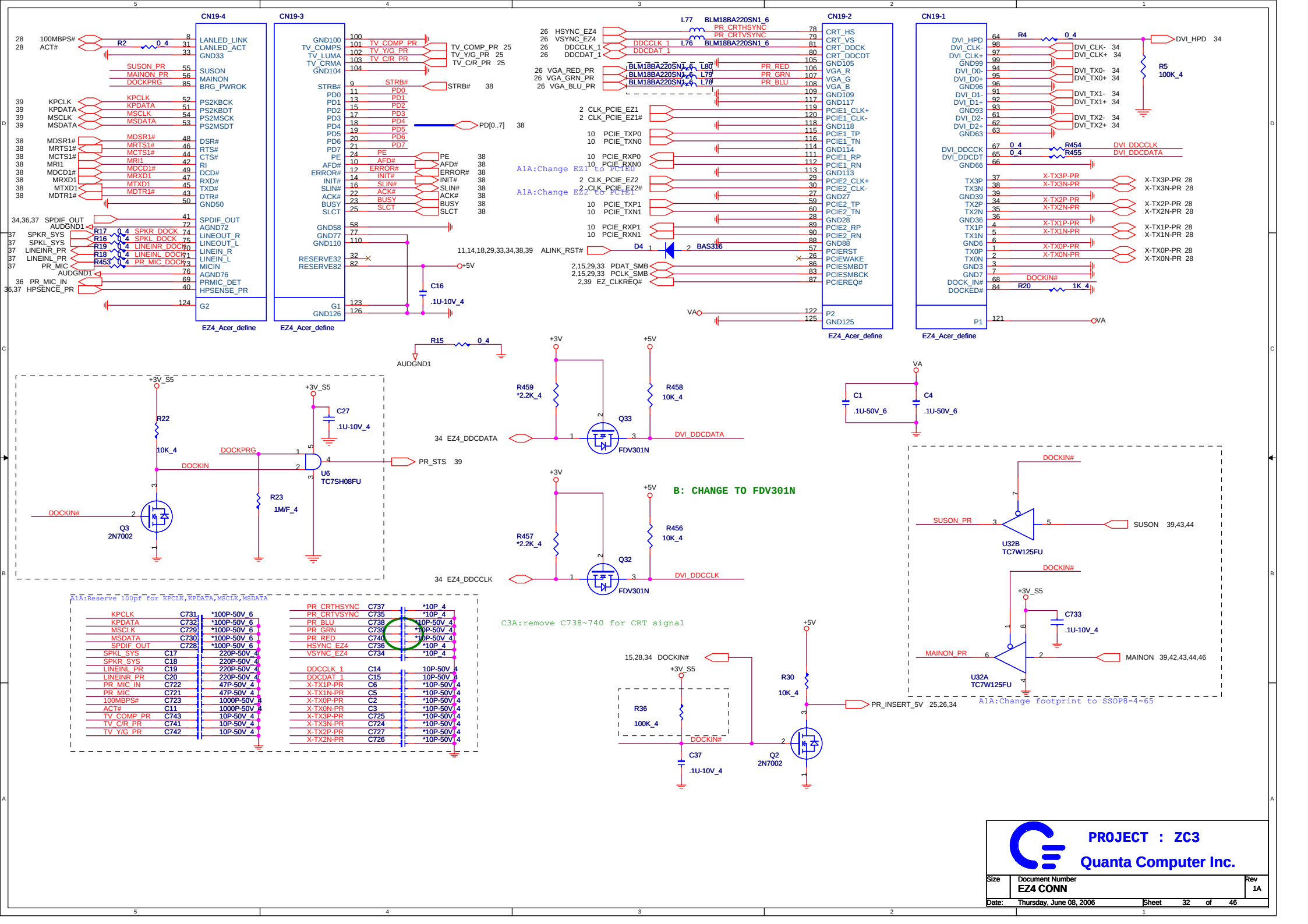
PROJECT : ZC3

Quanta Computer Inc.

Size	Document Number	Rev
	DEBUG CARD&PCI-E card&USB	1A
Date: Thursday, June 08, 2006	Sheet 29 of 46	


PCLK_PCM R666 *22_4 C927 *10P-50V_4
U51A
PCI Interface
1394 Interface
Miscellaneous
PCI7412
GNT0# REQ0# AD25 R668 150_4
FRAME# IRDY# DEVSEL# TRDY# SERR# STOP# PERR# PAR
CBE3# CBE2# CBE1# CBE0#
A1A:Change to PCLK_PCM
PCLK
PCIRST# GRST# 7412
AD[0..31]
1394_XIN C1024 12P-50V_4
Y10 24.576MHZ
1394_XOUT C1023 12P-50V_4
R0 R756 6.34K/F_4
CPS R699 390K_4
R696 330_4
B2A:Change R756 footprint to RC0402
TPA0P TPA0N TPBIAS0 TPB0P TPB0N
TPA1P TPA1N TPBIAS1 TPB1P TPB1N
VDDPLL15 PHY_TEST_MA
R755 1394_AVDD 4.7K_4
C1008 1U-16V_6
PC0_RSVD PC1_RSVD PC2_RSVD
AGND_00 AGND_01 AGND_02
R655 10K_4 D30 *BAS316
SUSPEND# RI_OUT# SPKROUT
R667 0_4 PCI_PME_7412#
R656 *0_4 PCMSPK RI#
SUS_STAT# 15,38
VR_EN# USB_EN
SCL SDA SCL_CARD SDA_CARD
MFUNC0 MFUNC1 MFUNC2 MFUNC3 MFUNC4 MFUNC5 MFUNC6
INTE# INTF# INTG# SERIRQ CLKRUN#
LATCH/VD3/VPPD0 CLOCK/VD1/VCCD0# DATA/VD2/VPPD1 RSVD_03/VD0/VCCD1#/PS_MODE
TPS_LATCH TPS_CLOCK TPS_DATA PS_MODE
C3A:disconnect PCI_LOCK#
TPBIAS0
R734 56.2/F_4 R737 56.2/F_4 C994 1U-16V_6
R793 0_6 R792 0_6
L112 *RFCMF1632140M2T
L113 *RFCMF1632140M2T
R703 56.2/F_4 R718 56.2/F_4
1394_COM
R697 5.1K/F_6 C981 270P-25V_4
R795 0_6 R796 0_6
L1394_TPA0+ L1394_TPA0- L1394_TPB0+ L1394_TPB0-
C3A:for ME suggestion change to DFHS04FS977
B2A:Change R793,R792,R795,R796 footprint to RC0603
CN14
020204FR004S502ZL_1394 CONN
A1A:Change CN14 to 1394-020015fr004s2162L-4P-H
Delay 2ms
R654 22K_4 C935 .1U-10V_4
B2A:Change R665 footprint to RC0402
R665 43K/F_4 R664 *43K_6 PS_MODE
A1A Add PS_MODE to define switch power
Hi : serial
Lo: parallel
L107 BK1608HS800_6
C1020 1U-10V_4 C1019 1U-16V_6
R683 2.2K_4 R679 2.2K_4 R684 *220_4 R680 *220_4
U50 24LC02BT
C937 .1U-10V_4
15,27 PME#
Q41 DTC144EU
R657 10K_4 PCI_PME_7412#
PROJECT : ZC3
Quanta Computer Inc.
Document Number PCI7412-IEEE1394
Rev 1A
Date: Thursday, June 08, 2006
Sheet 30 of 46


U51B
CardBus Interface
PCI7412
CN10
UPPER PIN
LOWER PIN
CARDBUS SLOT
SANTA_130601-5
U53
TPS2220APWP
U51D
Power/GND
PCI7412
U51C
FlashMedia Interface
PCI7412
A1A:TI FAE recommend
48MHz Clock
TXC-48MHz-30PPM-15Pf
Q44
TPS2061DGNR
CN11
R013-000-XX_CARD READER
CN33
CR_PRO@MSX309-X0-2XX1_CARD READER
PROJECT : ZC3
Quanta Computer Inc.
5 IN1 CARD READER
PCI(TI7412)-PCMCIA
Thursday, June 08, 2006


CN19-4
CN19-3
CN19-2
CN19-1
EZ4_Acer_define
EZ4_Acer_define
EZ4_Acer_define
EZ4_Acer_define
LANLED_LINK
LANLED_ACT
GND33
SUSON
MAINON
BRG_PWROK
PS2KBCK
PS2KBDT
PS2MSCK
PS2MSDT
DSR#
RTS#
CTS#
RI
DCD#
RXD#
TXD#
DTR#
GND50
SPDIF_OUT
AGND72
LINEOUT_R
LINEOUT_L
LINEIN_R
LINEIN_L
MICIN
AGND76
PRMIC_DET
HPSENSE_PR
G2
GND100
TV_COMPS
TV_LUMA
TV_CRMA
GND104
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
AFD#
ERROR#
INIT#
SLIN#
ACK#
BUSY
SLCT
GND58
GND77
GND110
RESERVE32
RESERVE82
G1
GND126
CRT_HS
CRT_VS
CRT_DDCK
CRT_DDCDT
GND105
VGA_R
VGA_G
VGA_B
GND109
GND117
PCIE1_CLK+
PCIE1_CLK-
GND118
PCIE1_TP
PCIE1_TN
GND114
PCIE1_RP
PCIE1_RN
GND113
PCIE2_CLK+
PCIE2_CLK-
GND27
PCIE2_TP
PCIE2_TN
GND28
PCIE2_RP
PCIE2_RN
GND88
PCIERST
PCIEWAKE
PCIESMBDT
PCIESMBCK
PCIEREQ#
P2
GND125
DVI_HPD
DVI_CLK-
DVI_CLK+
GND99
DVI_D0-
DVI_D0+
GND96
DVI_D1-
DVI_D1+
GND93
DVI_D2-
DVI_D2+
GND63
DVI_DDCCK
DVI_DDCDT
GND66
TX3P
TX3N
GND39
TX2P
TX2N
GND36
TX1P
TX1N
GND6
TX0P
TX0N
GND3
GND7
DOCK_IN#
DOCKED#
P1
R2 0_4
R4 0_4
R5 100K_4
R454 DVI_DDCCLK
R455 DVI_DDCDATA
R20 1K_4
R17 0_4 SPKR_DOCK
R16 0_4 SPKL_DOCK
R19 0_4 LINEINR_DOCK
R18 0_4 LINEINL_DOCK
R453 0_4 PR_MIC_DOCK
R15 0_4
AUDGND1
D4 BAS316
L77 BLM18BA220SN1_6
L76 BLM18BA220SN1_6
L80 BLM18BA220SN1_6
L79 BLM18BA220SN1_6
L78 BLM18BA220SN1_6
A1A:Change EZ1 to PCIE0
A1A:Change EZ2 to PCIE1
C16 .1U-10V_4
C27 .1U-10V_4
C1 .1U-50V_6
C4 .1U-50V_6
R22 10K_4
R23 1M/F_4
U6 TC7SH08FU
Q3 2N7002
R459 *2.2K_4
R458 10K_4
Q33 FDV301N
R457 *2.2K_4
R456 10K_4
Q32 FDV301N
B: CHANGE TO FDV301N
U32B TC7W125FU
U32A TC7W125FU
C733 .1U-10V_4
A1A:Change footprint to SSOP8-4-65
A1A:Reserve 100pf for KPCLK,KPDATA,MSCLK,MSDATA
C3A:remove C738~740 for CRT signal
R30 10K_4
R36 100K_4
C37 .1U-10V_4
Q2 2N7002
PROJECT : ZC3
Quanta Computer Inc.
EZ4 CONN
Thursday, June 08, 2006
Sheet 32 of 46

+NEW_1.5V Max. 650mA, Average 500mA.
+NEW_3V Max. 1300mA, Average 1000mA.

A1A:Change New card power sw to Oz27c10

A1A:Change New card to small type(130832-1)

Reverse

U47

ExpressSwitch

2@R5538D001-TR-F/OZ27C10LN

R671 100K_4

B2A:remove R677, R674

Place near U20

B2A:update footprint to h-c236d146p2

B2A:update footprint to H-C236D146I186P2

Q42 2N7002

Q40 2N7002

RP29 10K_4P2R

RP28 0_4P2R_S

CN30

130832-1_NEW CARD

Place near CN35

A1A:Reserve for EMI

B2A:MB-IR-SUP-BKT-ZC1

HOLE14 *H-C236BC276D98I138P2
HOLE5 h-c236d146p2
HOLE11 H-C236D146I186P2
HOLE4 *h-c236d142p2
HOLE15 H-C236D146I186P2
HOLE9 h-c236d146p2
HOLE8 h-c236d146p2
HOLE12 *H-C276BC315D118P2
HOLE22 *h-c276bc315d118p2
HOLE23 *h-c276bc315d118p2
HOLE6 *h-c276bc315d118p2
HOLE24 *h-c276bc315d118p2
HOLE13 *h-c276d118p2
HOLE21 *h-c276d118p2
HOLE17 *h-c276d118p2
HOLE1 *h-c276d118p2
HOLE7 *h-c276d142p2
HOLE16 h-c276d146p2
HOLE10 *H-C276D98I138P2
HOLE18 h-c276d146p2
HOLE3 H-C236D146I226A226P2
HOLE2 H-C236D146I226A226P2
HOLE19 h-c276d118p2
HOLE20 *h-c276d118p2

PAD31 *EMIPAD
PAD32 *EMIPAD
PAD33 *EMIPAD

PAD20 *EMIPAD
PAD21 *EMIPAD
PAD8 *EMIPAD
PAD10 *EMIPAD
PAD11 *EMIPAD
PAD13 *EMIPAD
PAD1 *EMIPAD
PAD16 *EMIPAD
PAD17 *EMIPAD
PAD15 *EMIPAD
PAD3 *EMIPAD
PAD19 *EMIPAD
PAD14 *EMIPAD
PAD27 *EMIPAD
PAD26 *EMIPAD
PAD29 *EMIPAD
PAD30 *EMIPAD
PAD18 *EMIPAD
PAD6 *EMIPAD
PAD5 *EMIPAD
PAD9 *EMIPAD
PAD22 *EMIPAD
PAD28 *EMIPAD
PAD7 *EMIPAD
PAD25 *EMIPAD
PAD24 *EMIPAD
PAD23 *EMIPAD
PAD12 *EMIPAD
PAD4 *EMIPAD
PAD2 *EMIPAD

ADOGND

PROJECT : ZC3

Quanta Computer Inc.

Size	Document Number	Rev
	NEW CARD &HOLE	1A
Date: Thursday, June 08, 2006	Sheet 33 of 46	

PVCC1 67mA
PVCC2 13.5mA
SPVCC 30mA
SVCC 323mA
VCC 133mA

Sil1930

Sil1930 TQFP or QFN package

B2A:change R500~R503 from 300 to 175 for HDMI

Improve signal swing

B2A:remove L72~L75 for HDMI signal

DB "short" and reserve common mode choke pads for EMI final tune

B2A:Mirror CN18(HDMI connector) pin define to meet cable define

C-CD012A1D

HDMI PORT

C3A:change R44 to 10K to meet HDMI plug spec

Place close to the connector

ESD4,ESD5 may be removed if can pass the ESD test w/o these 2 chips.

Layout note:Place close to HDMI Conn

TO docking DVI

TO SYSTEM HDMI

Change from 1.8K to 4.7K

TS3DV520RHUR

SEL	FUN
H	B2
L	B1

Mount R7086, keep R7087 NC at the beginning
Remove R7086, mount R7087 after VBIOS add SW_RST# function.

I2C ADDRESS = 20h

AK4113VF

SN74CBTD3305C

SN74LV1G00DCK

UC@AT89C51IC2-RLTIL
VQFP44

uC
ATMEL(AT89C51IC2-RLTIL)
SST(SST89V54RD2-33-C-TQJE)

BOM
ATMEL open
SST stuff

Open if use Atmel uC

P1.2,P1.3 : Software I2C (SST)
P4.1,P4.3 : Hardware I2C (ATMEL)

C3A:change footprint form c0402-c to c0402

HDMI_SDA & HDMI_SCL capacitance MUST less than 50PF

D3A:stuff R483 for HDMI update F/W

SEL	FUNCTION
LOW	IN_B0
HIGH	IN_B1

NC7SB3157P6X

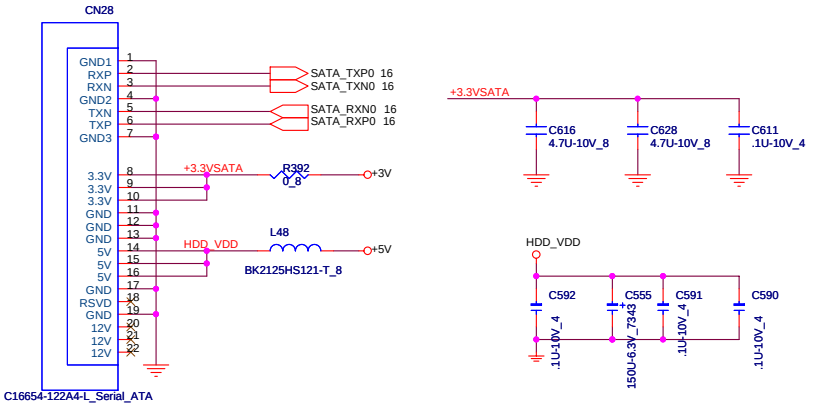
DOCKING
HDMI connector

PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AK4113-Sil1930-uP(HDMI)	1A

Date: Thursday, June 08, 2006 Sheet 34 of 46

SATA HDD



From SB

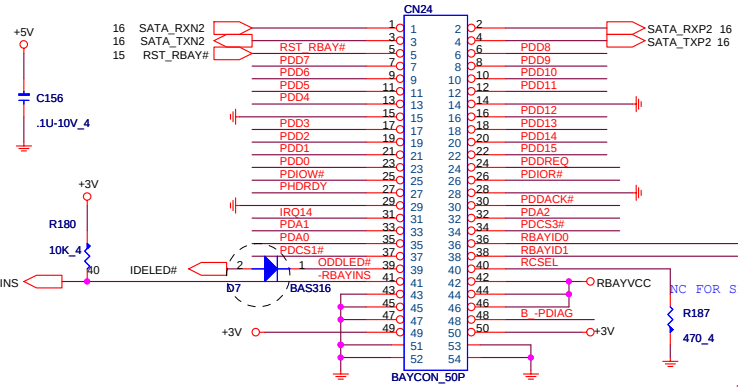
PDD0
PDD1
PDD2
PDD3
PDD4
PDD5
PDD6
PDD7
PDD8
PDD9
PDD10
PDD11
PDD12
PDD13
PDD14
PDD15
PDD[0..15] 16

PDIOR#
PDIOW#
PDDACK#
IRQ14
PHDRDY
PDDREQ
PDIOR# 16
PDIOW# 16
PDDACK# 16,17
IRQ14 16
PHDRDY 16
PDDREQ 16 39

PDA0
PDA1
PDA2
PDA[2:0] 16

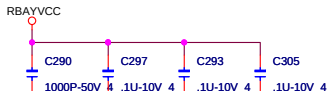
PDCS1#
PDCS3#
PDCS1# 16
PDCS3# 16

Media Bay Connector



BAY ID STATUS

RBAYID0/ LBAYID0	RBAYID1/ LBAYID1	STATUS
0	0	FDD
0	1	HDD
1	0	CD/DVD



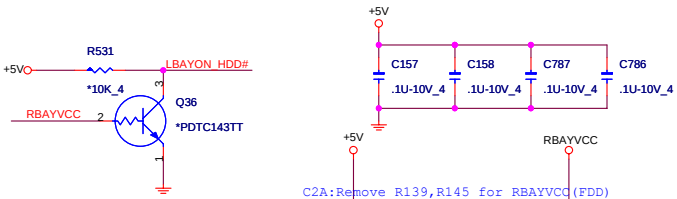
RBAYID0 15
RBAYID1 15

NC FOR SLAVE
R187
470_4
R192
*0_4

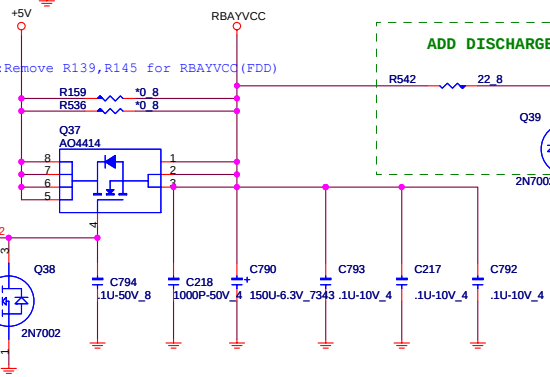
A1A:Remove R192 for RBAYID

B_-PDIAG R167 10K_4 +5V

C2A:Stuff R1266,set ODD to Master



C2A:Remove R139,R145 for RBAYVCC(FDD)



ADD DISCHARGE CIRCUIT

PROJECT : ZC3		
Quanta Computer Inc.		
Size	Document Number: HDD & MEDIA BAY	Rev: 1A
Date: Thursday, June 08, 2006	Sheet 35 of 46	

B2A: for audio noise
del
L55,C657,C661,C1063,C675,C679,C1064
stuff U29,R414,R423,R425,C664

Option of External Volume
Control or Standby
Mode/De-Pop

System MIC
Docking MIC
INT MIC

MIC1-VREFO-R 37
MIC3-VREFO-L 37
MIC2-VREFO-L 37

MIC1-VREFO-L 37

+5V_ADO
R439 10K_4

C685 10U-25V_1206
ADOGND

TO Headphone AMP

FRONT-L
FRONT-R
SENSEB

U57

55mA(AVDD=5.0V)

+5V_ADO

37 SURR-L
SURR-L
R790 20K/F_6
37 SURR-R
SURR-R
ADOGND

TO SPEAKER AMP

ALC883

LINE1-VREFO-R
AVDD2
SURR-L
JDREF/NC
SURR-R
AVSS2
SURR-VREFO-L
SURR-VREFO-R
MIC2-VREFO-R
LINE2-VREFO-R
SPDIFI/EAPD
SPDIFO

FRONT-R
FRONT-L
Sense B
DCVOL
MIC1-VREFO-R
LINE2-VREFO
MIC2-VREFO
LINE1-VREFO-L
MIC1-VREFO-L
VREF
AVSS1
AVDD1

LINE1-R
LINE1-L
MIC1-R
MIC1-L
CD-R
CD-GND
CD-L
MIC2-R
MIC2-L
LINE2-R
LINE2-L
Sense A

C1034 .1U-10V_4
C1033 .1U-10V_4
C1032 .1U-10V_4
ADOGND

LINE1-R 37
LINE1-L 37
MIC1-R 37
MIC1-L 37

SYSTEM AND DOCKING
LINE IN

SYSTEM MIC

MIC2_INT_R 37
MIC2_INT_L 37

INT MIC

MIC3-R 37
MIC3-L 37

Docking MIC

SENSEA R760 20K/F_6
R759 10K/F-6
MIC1_JD 37
LINEIN_JD 37

DVDD1
GPIO0
GPIO1
DVSS1
SDATA-OUT
BIT-CLK
DVSS2
SDATA-IN
DVDD2
SYNC
RESET#
PCBEEP

32,34,37 SPDIF_OUT
R789
SPDIF_OUT 0_4 SPDIF_OUT_883
CX5LL121007

+3V
C1059 10U-10V_8
37 883_AMP_MUTE#
883_AMP_MUTE#
R784 *10K_4
ADOGND

CODEC-RESET#
AZ_SYNCA
CODEC-BITCLK

C683 *22P_4
C1048 *22P_4
C1052 10P_4

AZ_SDOUTA
CODEC-BITCLK
AZ2_SDIN0
AZ_SYNCA
CODEC_RESET#

R773 0_4 AZ_RESET# 15,37
AZ_SYNCA 15
R779 22_4 AZ_SDIN1 15
R782 0_4 AZ_BITCLKA 15
AZ_SDOUTA 15

A1A:Change AZ_SDIN1 series resistor from 33 to 22 ohm

SENSEB
R428 39.2K/F_6
Change to 39.2K/F

Q25 2N7002
32 PR_MIC_IN
R427 100K_4
ADOGND

SENSEA
R432 5.1K/F_6
Change to 5.1K/F
LINE_JD 37

Q26 2N7002
32,37 HPSENCE_PR
R431 100K_4
ADOGND

Change to SENSEA,when docking HP
insert,system speaker can be mute

Sense A	5.1k	1%	Front out(pin35.36)
Sense A	10k	1%	Line1(pin23.24)
Sense A	20k	1%	Mic1(pin21.22)
Sense A	39.2k	1%	Surr out(pin39.41)
Sense B	5.1k	1%	Side out(pin45.46)
Sense B	10k	1%	Cen/Lfe out(pin43.44)
Sense B	20k	1%	Mic2(pin16.17)
Sense B	39.2k	1%	Line2(pin14.15)

+5V
R414 0_8
U29
VEN VOUT
VIN GND ADJ
G961-18ADJTEU(SOT89-5)
R423 36K_4
R425 12K_4
C664 10U-25V_1206
+5V_ADO
ADOGND

Reserved only

Vo=1.2*(R371+R372)/R371= 4.8V

+3V
C694 .1U-10V_4
C710 .1U-10V_4
C687 .1U-10V_4
C709 10U-25V_1206

C1060 *100P_6
C1036 *100P_6
R764 *0_6
R791 *0_6
R765 *0_6
ADOGND

Tied at one point only
under the codec or near
the codec

D3A:remove R791

PCBEEP
C1043 1U-16V_6
BEEP_1
R767 10K_4
BEEP
C1040 .1U-10V_4
R771 1K_4
ADOGND

D3A:change
to .1u

D3A:change
to ADOGND

U56
SN74LVC1G86DCKR

R775 10K_4
PCMSPK 30
PCSPK 15

For MDC Module

CN9
MDC

15 CD_SDOUTA_MDC
CD_SDOUTA_MDC
15 CD_SYNC_MDC
CD_SYNC_MDC
15 CD_SDIN0
CD_SDIN0
15 CD_RESET#_MDC
CD_RESET#_MDC

R687 22_4 CD_SDIN1

GND RSV
AC_SDO RSV
GND 3.3V
AC_SYNC GND
AC_SDI GND
AC_RST# AC_BCLK

CD_BITCLKA_MDC 15

+3V_S5
C973 .1U-10V_4
C958 *10P_4
R716 *22_4
C972 *10P_4

Change from 1UF to 4.7UF to meet
vista performance requirement

C3A:change 0 to 4.7k to avoid noise

Headphone Amplifier

U30 MAX4411ETP+

FRONT-L
FRONT-R
C672 1U/16V_6
C686 1U/16V_6
AOUTR_L_HP
AOUTR_R_HP
R426 4.7K_4
R429 4.7K_4
INL_4411
INR_4411

37 MUTE#
R437 0_4
D3A:change to 1U

C678 1U/10V_4
C1P_4411
C1N_4411
PVSS_4411
C673 1U/10V_4

INL
INR
SHDNR
SHDNL
C1P
C1N
PVSS
SVSS

EP EP EP EP EP
OUTL OUTR
NC1 NC2 NC3 NC4 NC5 NC6
SVDD PVDD
PGND SGND

QFN20-4X4-5-25P

A1A:Per FAE recommend,keep exposed pad floating

HPL 37
HPR 37

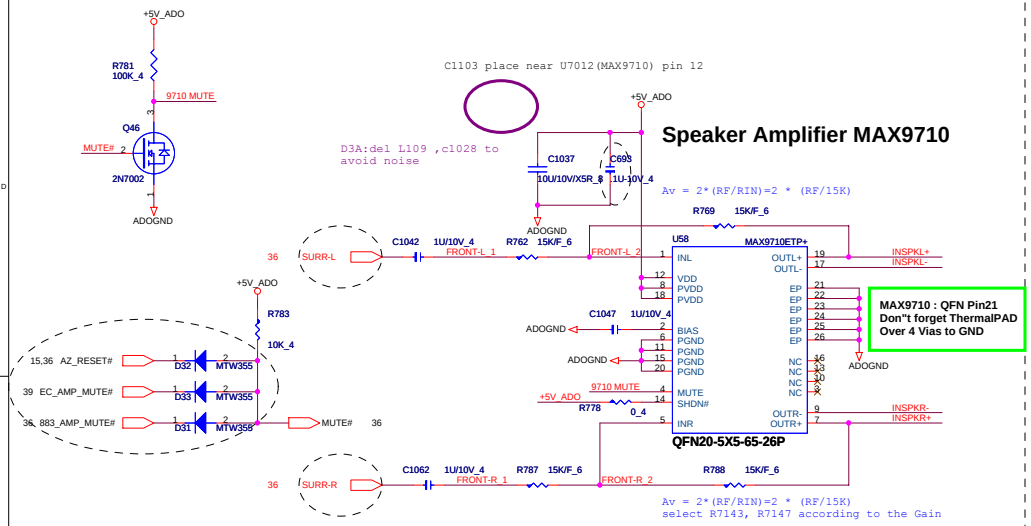
D3A:change form BLM11A601S to
BLM18PG181SN1D

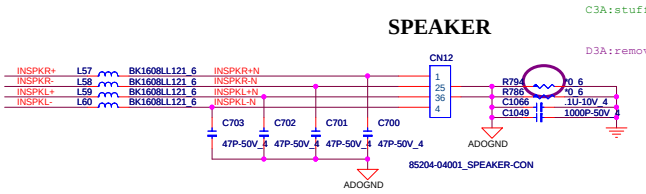
L54
BLM18PG181SN1D_6
VCC3_4411
C666 1U/10V_4
C663 10U-10V_8

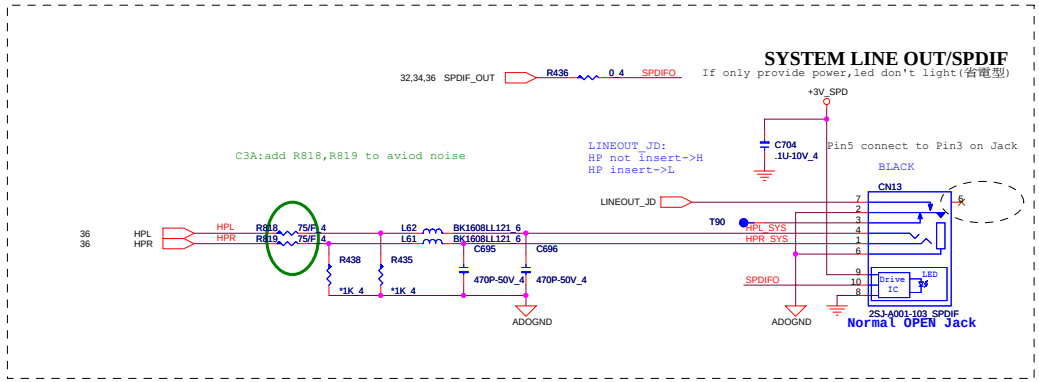
ADOGND ADOGND

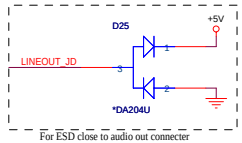
PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ALC883 & MDC & HP AMP	1A
Date: Thursday, June 08, 2006	Sheet 36 of 46	

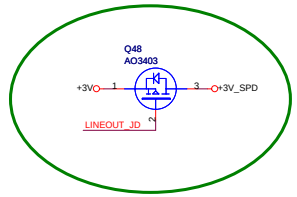


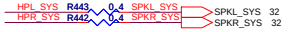


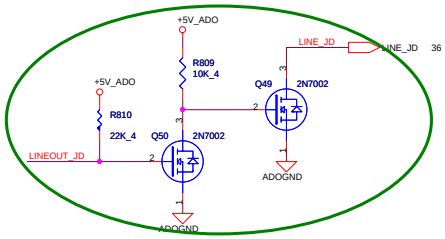


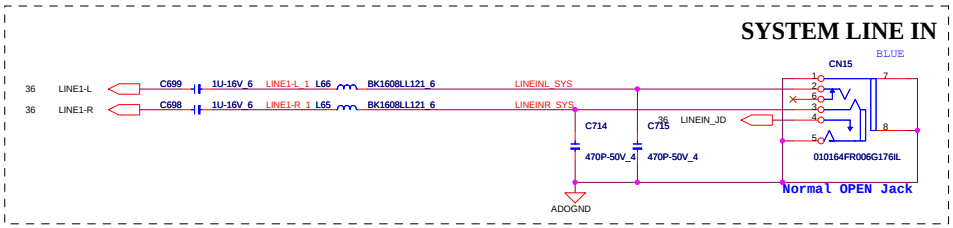


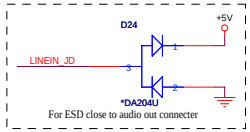
Reserved only,when performance can meet vista requirement,pls delete it.

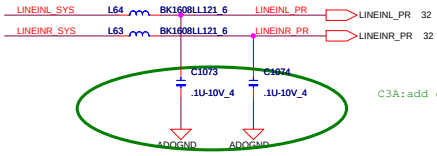


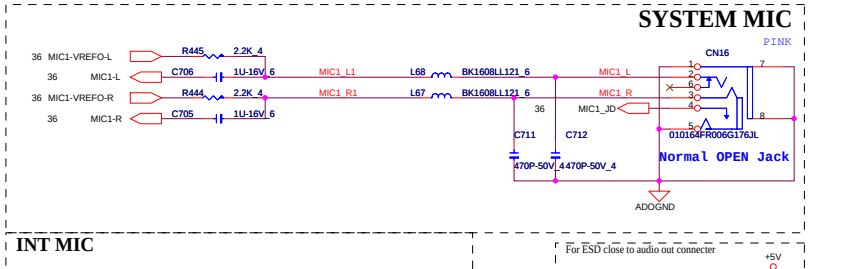


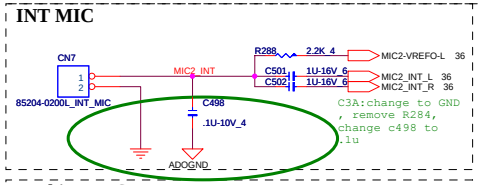


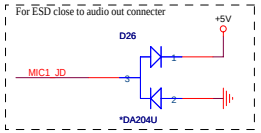


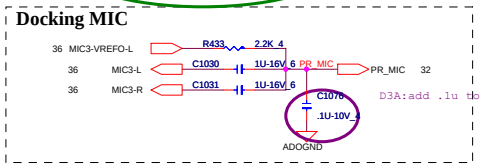












PROJECT : ZC3
Quanta Computer Inc.

Size	Document Number	Rev
C	SPEAKER AMP / JACK	1A

Date: Thursday, June 08, 2006 Sheet 37 of 46

MDTR1# (PC87383's BADDR)

BADDR:0 ->Index-Data pair at 2Eh~2Fh(ZC3 setting)

BADDR:1 ->Index-Data pair at 164Eh-164Fh(default)

B2A:Stuff R27,set PC87383 I/O to 2E/2F

STRAP PINS

MDTR1# R27 10K_4

MRTS1# R32 *10K_4

MTXD1 R31 *10K_4

U8

NS PC87383

PC87383-VS

+3V

C28 .1U-10V_4

C45 .1U-10V_4

C48 10U-10V_8

C52 *10P_4

R40 *22_4

PCLK_SIO

R474 10K_4

D29 *BAS316

15,30 SUS_STAT#

+5V

RN1 4.7K_4P2R_S

RN2 4.7K_4P2R_S

RN3 4.7K_4P2R_S

R26 4.7K_4 PD3

R475 4.7K_4 PD7

R34 4.7K_4 SLCT

R473 4.7K_4 ERROR#

R472 4.7K_4 SLIN#

R464 4.7K_4 PE

R468 4.7K_4 INIT#

R461 4.7K_4 AFD#

R24 4.7K_4 STRB#

R471 4.7K_4 ACK#

R470 4.7K_4 Bbusy

32 PD[0..7]

14,29,39	LAD0/FWH0	LAD0/FWH0	42	LAD0	
14,29,39	LAD1/FWH1	LAD1/FWH1	46	LAD1	
14,29,39	LAD2/FWH2	LAD2/FWH2	51	LAD2	
14,29,39	LAD3/FWH3	LAD3/FWH3	53	LAD3	
14,17,29	PCLK_SIO	PCLK_SIO	33	LCLK	
14	LDRQ#0	LDRQ#0	22	LDRQ/XOR_OUT	
14,17,29,39	LFRAME#/FWH4	LFRAME#/FWH4	38	LFRAME	
11,14,18,29,32,33,34,39	ALINK_RST#	ALINK_RST#	35	LRESET	
14,30,39	SERIRQ	SERIRQ	36	SERIRQ	
		SUS_STAT_3V#	29	LPCPD/GPIO21	
14,30,39	CLKRUN#	CLKRUN#	27	CLKRUN/GPO22	
32	INIT#	INIT#	56	INIT	
32	ERROR#	ERROR#	54	ERR	
32	BUSY	BUSY	26	BUSY_WAIT	
32	AFD#	AFD#	57	AFD_DSTRB/TRIS	
32	ACK#	ACK#	28	ACK/GPO24	
32	STRB#	STRB#	14	STB_WRITE/TEST	
32	SLIN#	SLIN#	55	SLIN_ASTRB	
32	SLCT	SLCT	24	SLCT	
32	PE	PE	25	PE	
		PD7	30	PD7/PGIO23	
		PD6	34	PD6	
		PD5	37	PD5	
		PD4	39	PD4	
		PD3	6	PD3	
		PD2	43	PD2	
		PD1	50	PD1	
		PD0	52	PD0	

GPIO00	15	C43 *180P_4 PD0
GPIO01	16	C46 *180P_4 PD1
GPIO02	19	C51 *180P_4 PD2
GPIO20	23	C29 *180P_4 PD3
GPIO03	20	C50 *180P_4 PD4
GPIO04	21	C49 *180P_4 PD5
GPIO05	40	C53 *180P_4 PD6
GPIO06	7	C44 *180P_4 PD7
GPIO07	41	C35 *180P_4 SLCT
		C752 *180P_4 ERROR#
		C39 *180P_4 SLIN#
		C749 *180P_4 PE
		C36 *180P_4 INIT#
		C34 *180P_4 AFD#
		C21 *180P_4 STRB#
		C42 *180P_4 ACK#
		C38 *180P_4 BUSY

CLKIN 58 SIO_14M → SIO_14M 2

R469 *22_4

C748 *10P_4

IRRX1 8 IRRX

R25 10K_4 +3V

IRTX 9 IRTXOUT

IRRX2_IRSL0/GPIO17 10 IRMODE

CTSI/GPIO11	3	MCTS1#	32
DCD1/GPIO16	59	MDCD1#	32
DSR1/GPIO15	60	MDSR1#	32
RTS1/GPIO13	62	MRTS1#	32
SIN1/GPIO14	61	MRXD1	32
SOUT1/GPIO12	63	MTXD1	32
RI1/GPIO10	5	MRI1	32
DTR1_BOUT1/BADDR	4	MDTR1#	32

VSS 12, 31, 44; VCORF 13; NC 47, 48, 49, 64

C22 .1U-10V_4

FIR

U31 VISHAY_TFDU6102_8P

IRTXOUT 3 TXD

IRRX 4 RXD

IRMODE 5 SD

8 GND

VCC 6

MODE 7

LED_C 2

LED_A 1

+3V

T = 20mil

C1067 .1U-10V_4

C1071 10U-10V_8

C1069 10U-10V_8

+5V_FIR

T = 20mil

R447 5.6_1206

R452 5.6_1206

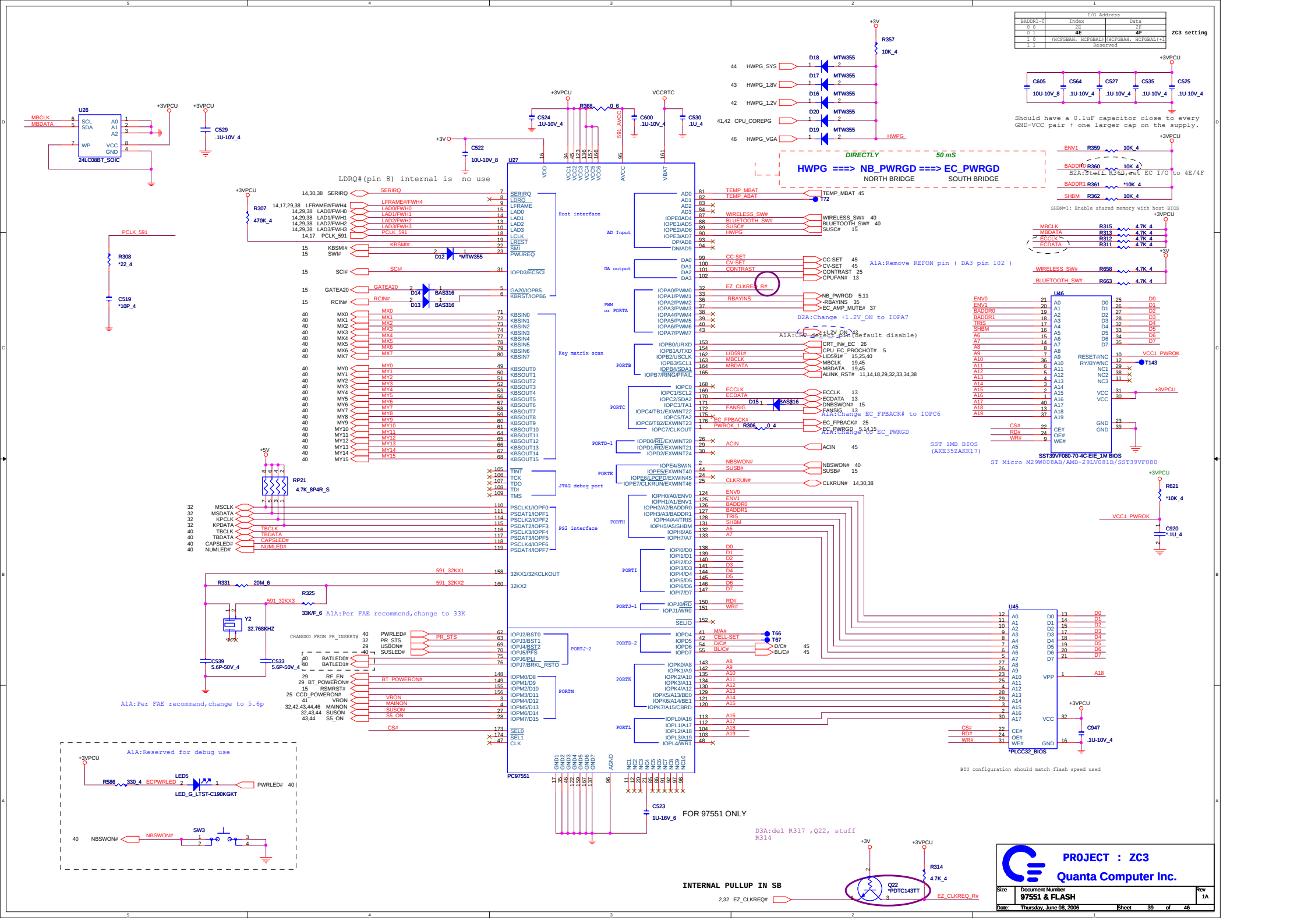
C1070 10U-10V_8

A1A:Change to +3v,prevent FIR noise impact audio quality

PROJECT : ZC3

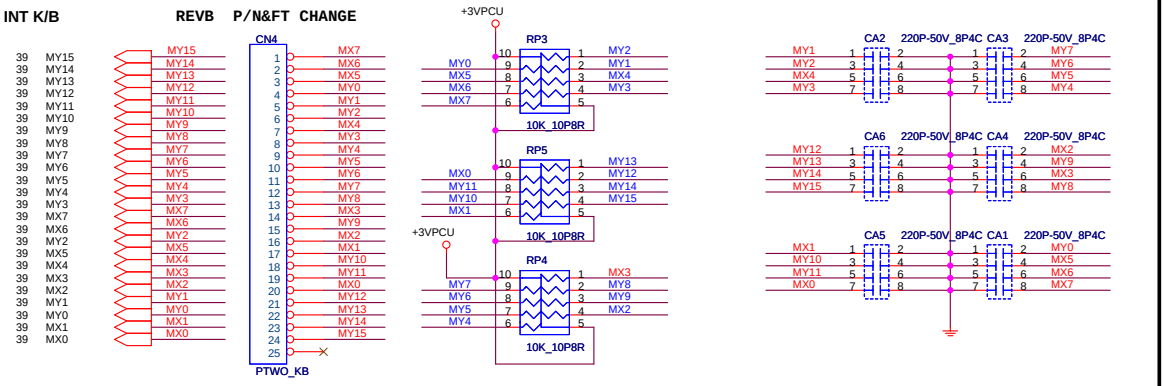
Quanta Computer Inc.

Size	Document Number	Rev
	SIO (87383)	1A
Date: Thursday, June 08, 2006	Sheet 38 of 46	

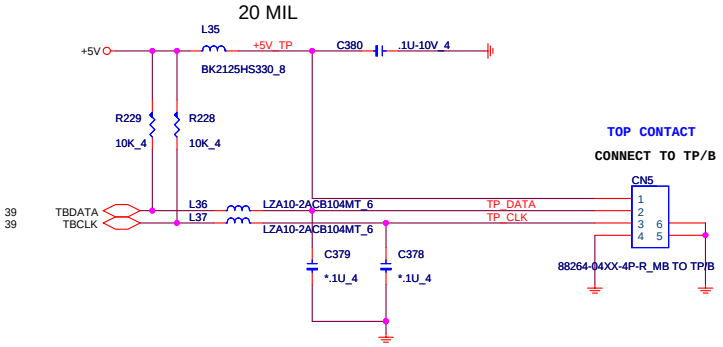

I/O Address
BADDR1-0 | Index | Data
0 0 | 2E | 2F
0 1 | 4E | 4F
1 0 | (HCFGBAH, HCFGBAL) | (HCFGBAH, HCFGBAL)+1
1 1 | Reserved
ZC3 setting
Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.
HWPG ===> NB_PWRGD ===> EC_PWRGD
DIRECTLY
50 mS
NORTH BRIDGE
SOUTH BRIDGE
LDRQ#(pin 8) internal is no use
B2A:Stuff R360,set EC I/O to 4E/4F
SHBM=1: Enable shared memory with host BIOS
A1A:Remove REFON pin (DA3 pin 102)
A1A:Change EC_FPBACK# to IOPC6
A1A:Change to EC_PWRGD
SST 1MB BIOS (AKE35ZAKK17)
ST Micro M29W008AB/AMD-29LV081B/SST39VF080
A1A:Per FAE recommend,change to 33K
A1A:Per FAE recommend,change to 5.6p
A1A:Reserved for debug use
FOR 97551 ONLY
D3A:del R317 ,Q22, stuff R314
INTERNAL PULLUP IN SB
BIU configuration should match flash speed used
PROJECT : ZC3
Quanta Computer Inc.
Size
Document Number
97551 & FLASH
Rev
1A
Date: Thursday, June 08, 2006
Sheet 39 of 46

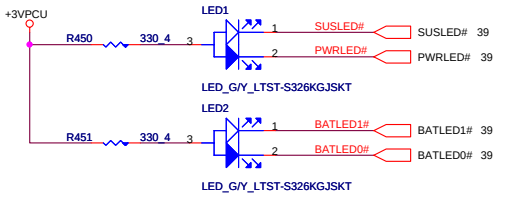
INT K/B

REVB P/N&FT CHANGE

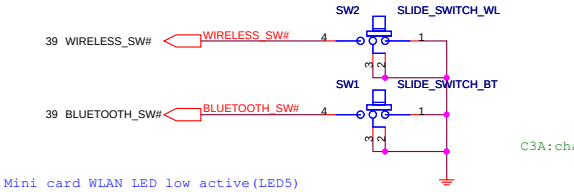


TOUCH PAD

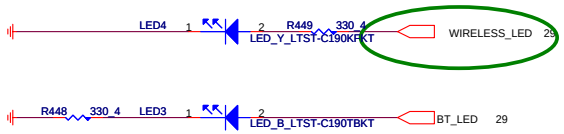




A1A:Change LED footprint to ledltst-s326kgjskt-3p-zc1

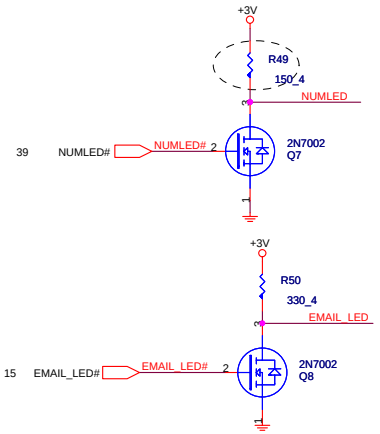


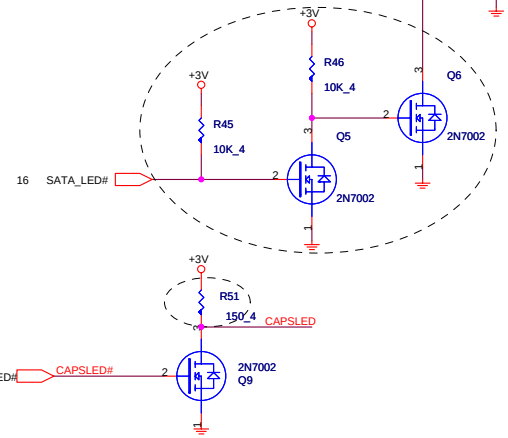
Mini card WLAN LED low active(LED5)

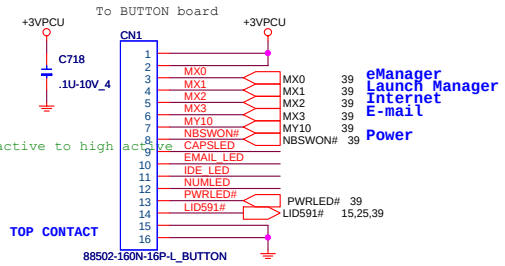


A1A:Change footprint to LEDLTST-C190TGKT

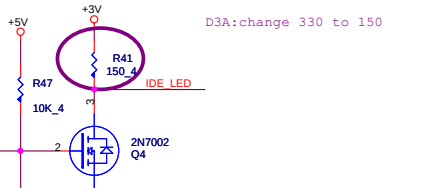
A1A:Change R49,R51from 220 to 150 increase LED brightness







C3A:change form low active to high active



D3A:change 330 to 150

PROJECT : ZC3	
Quanta Computer Inc.	
Size	Document Number: SWITCH,LED,K/B,TP — Rev: 1A
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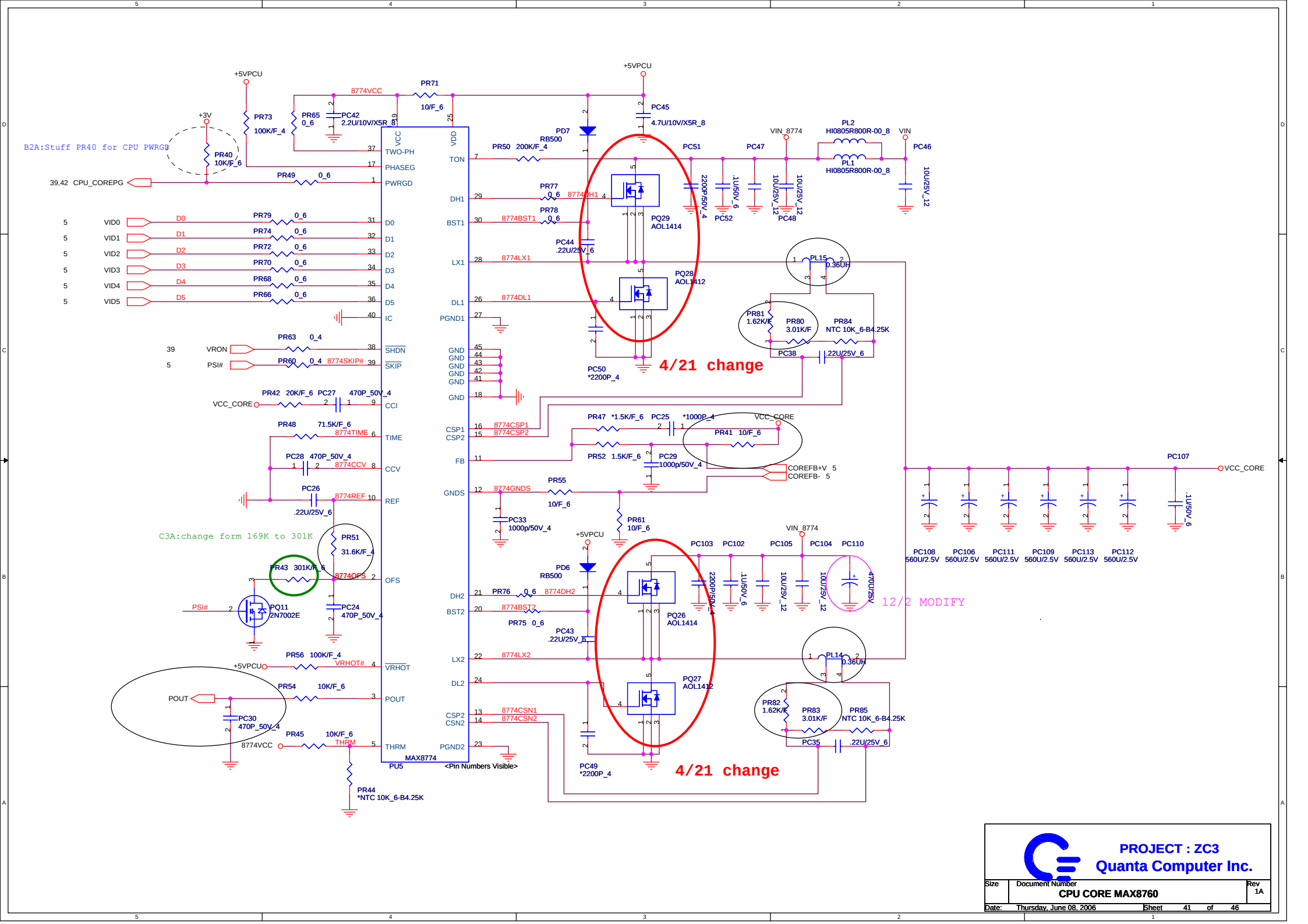
B2A:Stuff PR40 for CPU PWRGD
C3A:change form 169K to 301K
4/21 change
4/21 change
12/2 MODIFY
MAX8774
PU5
<Pin Numbers Visible>
PROJECT : ZC3
Quanta Computer Inc.
CPU CORE MAX8760
Rev 1A
Thursday, June 08, 2006
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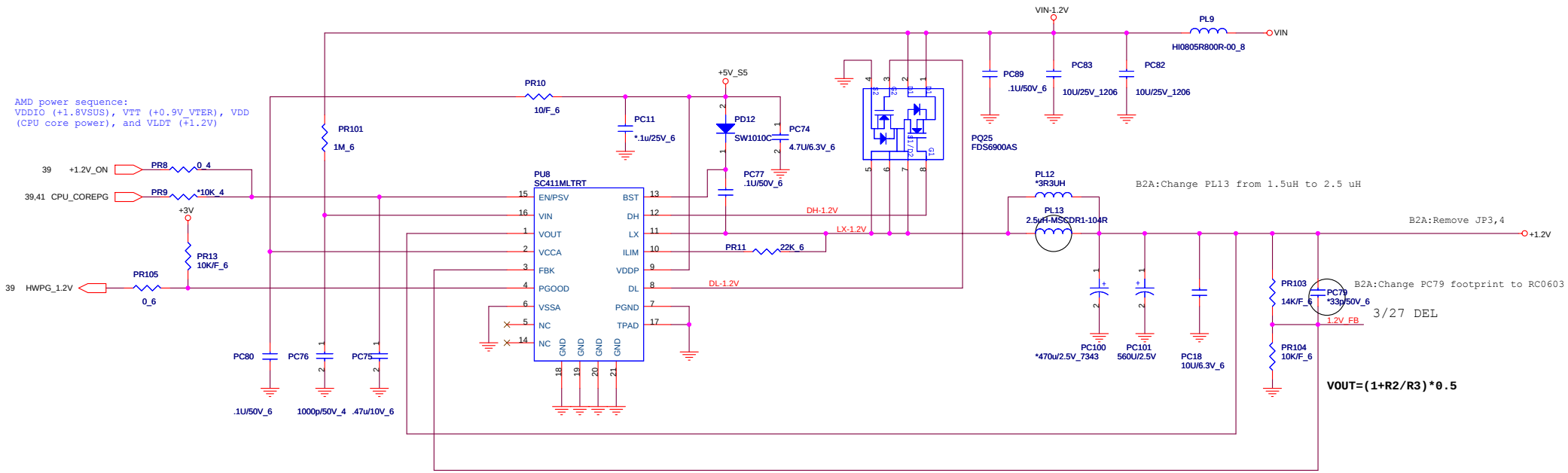
AMD power sequence:
VDDIO (+1.8VSUS), VTT (+0.9V_VTER), VDD
(CPU core power), and VLDT (+1.2V)
VIN-1.2V
VIN
PL9
HI0805R800R-00_8
PC89 .1U/50V_6
PC83 10U/25V_1206
PC82 10U/25V_1206
PQ25 FDS6900AS
+5V_S5
PR10 10/F_6
PC11 *.1u/25V_6
PD12 SW1010C
PC74 4.7U/6.3V_6
PC77 .1U/50V_6
PR101 1M_6
39 +1.2V_ON
PR8 0_4
39,41 CPU_COREPG
PR9 *10K_4
+3V
PR13 10K/F_6
39 HWPG_1.2V
PR105 0_6
PU8 SC411MLTRT
EN/PSV
VIN
VOUT
VCCA
FBK
PGOOD
VSSA
NC
NC
BST
DH
LX
ILIM
VDDP
DL
PGND
TPAD
GND
DH-1.2V
LX-1.2V
DL-1.2V
PR11 22K_6
PL12 *3R3UH
PL13 2.5uH-MSCDR1-104R
B2A:Change PL13 from 1.5uH to 2.5 uH
B2A:Remove JP3,4
+1.2V
PR103 14K/F_6
PC79 *33p/50V_6
B2A:Change PC79 footprint to RC0603
1.2V_FB
3/27 DEL
PR104 10K/F_6
PC100 *470u/2.5V_7343
PC101 560U/2.5V
PC18 10U/6.3V_6
PC80 .1U/50V_6
PC76 1000p/50V_4
PC75 .47u/10V_6
VOUT=(1+R2/R3)*0.5
VIN
+1.2V
PR20 1M/F_4
PR35 22_8
1.2V_ON_G
39 +1.2V_ON
PQ3 DTC144EUA
PR21 1M/F_4
PQ9 2N7002E
+3V
+1.8VSUS
A1A:Add PR69 for G966_VIN,change source to +1.8VSUS
PR57 100K/F_4
PR69 0_6
+5V
PU4
G966_VIN
46 VDDCPG
32,39,43,44,46 MAINON
PCIEVDDRPG
PR59 0_4
PR62 *0_4
VPP
VIN
VEN
POK
VO
ADJ
GND
NC
GGND
G966
+1.2V_VPCIE
PR64 45.3K/F_4
PR58 91K_4
PC41 10U-10V_8
PC40 .1U-10V_4
PC36 *.1U-10V_4
PC37 10U-10V_8
PC39 .1U-10V_4
Max Power Consumption 1.6W
PCIEVDDRPG
32,39,43,44,46 MAINON
R206 10K_4
PR53 *0_6
PU3
GND0
EN
VIN
VIN
VO
VO
GND1
GND2
ADJ
AT815
+3VSUS
PC31 .1U_6
PC32 10U-10V_8
PC34 .1U-50V_6
PC22 22U/6.3V_8
PC21 .1U-50V_6
+2.5V
A1A:Remove JP2 for +2.5V
0.8V
VTT-ADJ
R1
PR38 10.2K/F_4
PR37 10K/F_4
R2
3/27 Change P/N
Vout=1.24*[1+(R1/R2)]
A1A:Change PU3 p/n CS33242FB19
3/27 Change to +3V
MAINON PR91 10K_6
PU7
+3V
PC58 .1U/50V_6
PC59 .1U/50V_6
PC60 10U/10V/X5R_8
VPCIE-ADJ
R1
PR90 10K/F_6
R2
PR92 2.15K/F_6
3/27 Change P/N
+1.5V
PC61 22U/6.3V_8
PC63 .1U/50V_6
Vout=1.24*[1+(R1/R2)]
PROJECT : ZC3
Quanta Computer Inc.
Size Custom
Document Number
+1.2V/+1.5V/+2.5V
Rev A1A
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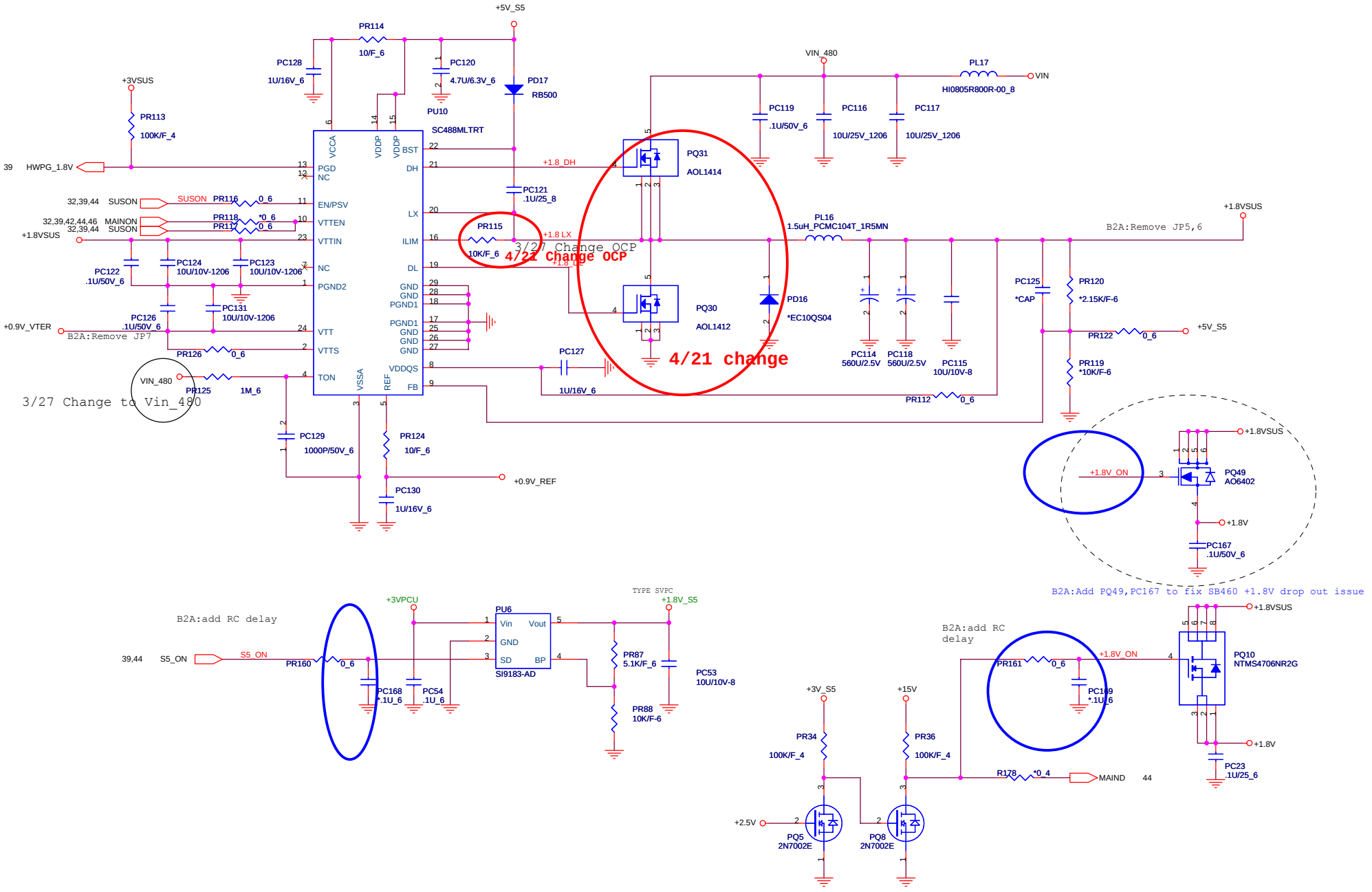

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.8V&DDRII	1A
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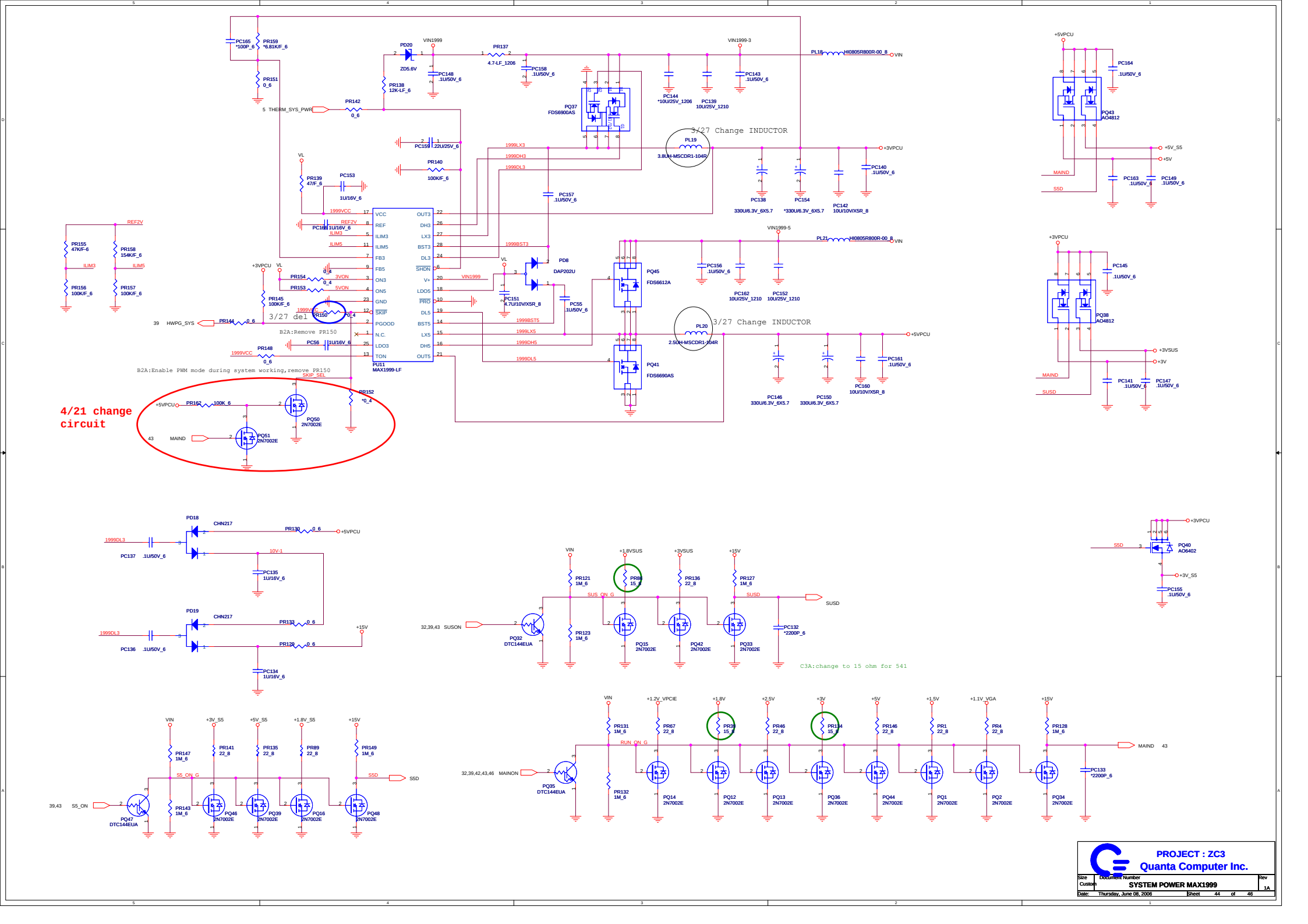
PU11
MAX1999-LF
PQ37
FDS6900AS
PQ45
FDS6612A
PQ41
FDS6690AS
PL19
3.8UH-MSCDR1-104R
PL20
2.5UH-MSCDR1-104R
PL16
PL21
HI0805R800R-00_8
PD20
ZD5.6V
PD8
DAP202U
PQ43
AO4812
PQ38
AO4812
PQ40
AO6402
PQ50
2N7002E
PQ51
2N7002E
PQ32
DTC144EUA
PQ35
DTC144EUA
PQ47
DTC144EUA
3/27 Change INDUCTOR
3/27 del
B2A:Remove PR150
B2A:Enable PWM mode during system working,remove PR150
4/21 change circuit
C3A:change to 15 ohm for 541
PROJECT : ZC3
Quanta Computer Inc.
SYSTEM POWER MAX1999
Size: Custom
Document Number
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A1A:Change PJ1 footprint to 4 pin

D3A:change from BCPL1040218 to BCSBM104219 (EOL issue)

PJ1
20277-044L_POWER_CONN
PC98 .1U/25_8
PC92 .1U/25_8
HI0805R800R-00_8 PL10
PL11 HI0805R800R-00_8
VA
2200P/50V_4
PC13 .1U/25_8
PC15
PC14 .1U/25_8
PD14 SPL1040PT
PR107 0.01_3720_1W
PC93 *.1u/50V_6
PC91 *.1u/50V_6
+3VPCU
PR106 100K/F_6
CELLR-SET
PR16 0_6
8724CELLS
PR15 100K/F_6
PD2 SW1010C
VAD
PR33 10K/F_6
PC19 .01U/50V_6
PD5 DA204U
PC94 1U/16V_6
PQ7 IMZ2 IMD
PC16 .1U/25_8
VH
PD3 RB500
PD15 RB500
VIN
PC20 .1U/25_8
PR111 47K_6
PR26 47K_6
PR25 10K/F_6
PU2A LM393
PR31 22K_6
PC17 220p_4
OSC 200KHz
CSSP
CSSN
PC81 10U/25V_12
PC10 .1U/25_8
PL8 HI0805R800R-00_8
VAON
PR12 4.7K/F_6
PR14 47K_6
PQ24 AO4414L
PC84 .1U/25_8
PQ22 FDS4435
PQ23 FDS6612A
PQ21 FDS6690AS
PL7 3.8uH-MSCDR1-104R
PR102 0.01
PC73 10U/25V_1206
PC9 10U/25V_1206
PC78 10U/25V_1206
PC72 .01U/50V_6
BAT-V
MBAT
4/28 for meet acer request 0.8c , change 0.15 to 0.01
FOR 4S
CELLR-SET
PU9 MAX8724
DCIN
CSSP
CSSN
CELLS
LDO
DLOV
BST
DHI
LX
DLO
PGND
CSIP
CSIN
BATT
REF
CLS
GND
ACIN
VCTL
ICTL
REFIN
ACOK
ICHG
IINP
SHDN
CCV
CCI
CCS
8724LDO
8724BST
8724DH
8724LX
8724DL
8724REF
PR108 33_6
PC97 1U/16V_6
PC85 1U/16V_6
PD13 SW1010C
PC88 .1U/25_8
PR108 0_6
PR19 8.25K/F_6
PR22 14K/F_6
PC12 1U/16V_6
PR110 1K/F_6
PC99 .1U/50V_6
PC95 .01U/50V_6
PC96 .01U/50V_6
+3VPCU
PC90 1U/50V_6
USE DEFAULT 4.2V/CELL
PR18 0_6
PR17 *0_6
CV-SET
CC-SET
PC86 1000p/50V_4
PC87 1000p/50V_4
CURRNT LIMIT POINT = 4.74A
CN23
SUYIN_BATTERY
MBAT+
TEMP_MBAT
TEMP_MBAT 39
HI0805R800R-00_8 PL5
PL6 HI0805R800R-00_8
MBAT
+3VPCU
PC6 47P_4
PC7 47P_4
PC71 .1U/50V_6
PR5 10K/F_6
PR6 330_4
PR7 330_4
MBCLK 19,39
MBDATA 19,39
TEMP_MBAT
PD10 ZD5.6V
PD11 ZD5.6V
PC8 .01U/50V_6
VIN
PR23 220K_6
+3VPCU
PU2B LM393
PR24 180K/F_6
VL
PR27 22K_6
PR28 220K_6
PQ6 DTC144EU
VAON
D/C#
BL/C#
PQ4 2N7002E
39 ACIN
PR29 10K/F_6
PR32 6.8K/F_6
VAD
PD4 ZD12V
PR30 10K/F_6

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Quanta Computer Inc.
Size C
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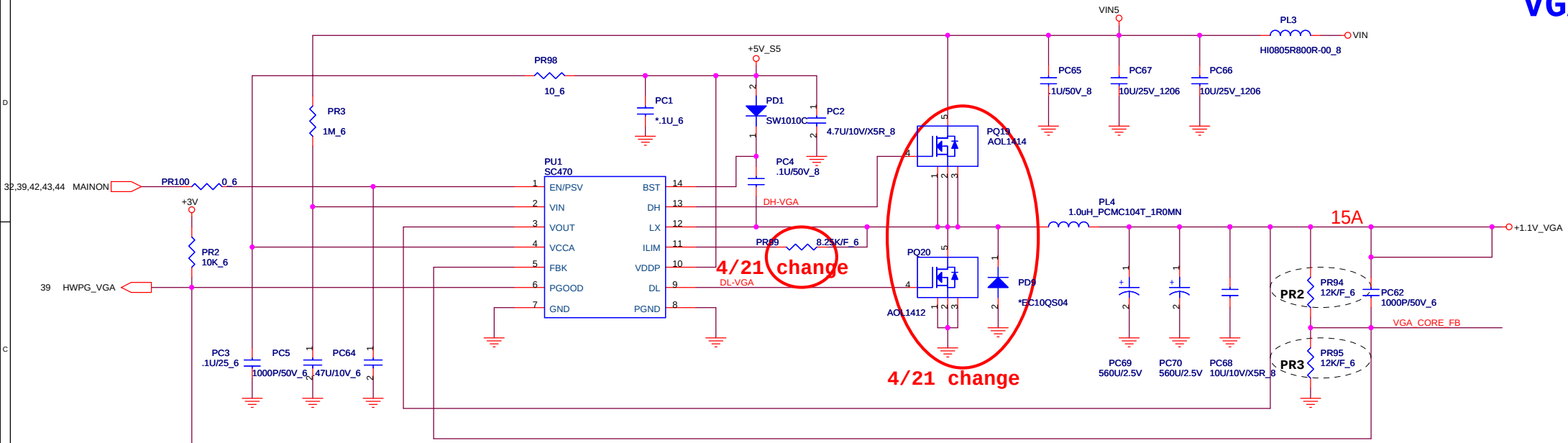
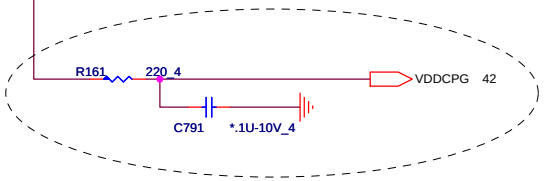
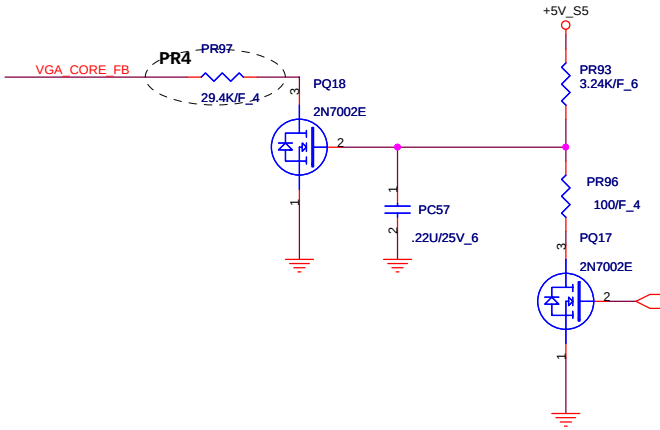
VGA





AlA:Add for M56 power sequence



HI-->VOUT=(1+R2/R3)*0.5

LO-->VOUT=(1+R2/(R3//R4))*0.5

M52P(G)

PR2 : 10K
PR3 : 11K
PR4 : 110K

M54P

PR2 : 12K
PR3 : 12K
PR4 : 60.4K

M56P

PR2 : 12K
PR3 : 12K
PR4 : 29.4K

Power Play Mode

VGA_PWR_SW	VGA_CORE
HI	0.95V--M52P(G) 1.0V --M54P 1.0V --M56P
Default LO	1.0V--M52P(G) 1.1V--M54P 1.2V--M56P

PROJECT : ZC3

Quanta Computer Inc.

Size	Document Number	Rev
	VGA CORE	1A

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