Olan (TM15") Block Diagram

Project code: 91.4Z701.001
PCB P/N : 48.4Z701.0SA
REVISION : 07249-SA

DDR2 667/800 MHz 8,9
DDR2 667/800 MHz 8,9
667/800MHz
667/800MHz
AMD Giffin CPU S1G2 (35W)
638-Pin uFCPGA638
4,5,6,7
OUT
IN
16X16
G792 25
CLK GEN.
SILEGO SLG8SP628 3
North Bridge
AMD RS780M
CPU I/F LVDS, CRT I/F
INTEGRATED GRAHPICS
11,12,13
A-Link 4X4
PCIex16
CRT 18
LCD 16
HDMI 19
VGA Borad 37
45,46
CRT
DVI
RJ45
Port Replicator
USBX4
HP OUT
MIC IN
LINE IN
LAN
Giga LAN BCM5764M 35
TXFM 36
RJ45 36
New card 38
PWR SW TPS2231 38
Mini Card Kedron a/b/g/n 39
PCIex1
Line In 42
Codec CX20561 40
AZALIA
MIC In 42
42
Line Out (No-SPDIF)
42
OP AMP APA2031 41
INT.SPKR
RJ11
MODEM MDC Card 29
South Bridge
AMD SB700
USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
ATA 66/100
ACPI 1.1
LPC I/F
PCI/PCI BRIDGE
20,21,22,23,24
PCI
Cardbus OZ711MZ 32
MS/MS Pro/xD /MMC/SD/SD IO 5 in 1 33
PCMCIA SLOT 34
LPC BUS
USB
SATA
HDD SATA 27
ODD SATA 26
Mini USB Blue Tooth 28
Finger Printer 31
Camera
USB 4 Port 30
KBC Winbond WPC775 43
BIOS Winbond W25X80 44
Launch Buttom 15
Touch Pad 43
INT. KB 43
LPC DEBUG CONN. 44

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC TPS51125 51	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)

SYSTEM DC/DC TPS51124 52	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(9A) 1D2V_S0(5A)

SYSTEM DC/DC TPS51117 53	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(10A)

RT9026PFP 54	
5V_S5	DDR_VREF_S3 0D9V_S3

RT9166 54	
3D3V_S0	2D5V_S0 (300mA)

G957 54	
3D3V_S0	1D5V_S0 (1A)

G9161 54	
3D3V_S5	1D2V_S5 (400mA)

CHARGER BQ24745 55	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 50	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

DIS

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Title: BLOCK DIAGRAM
Size: A3 | Document Number: Olan | Rev: SA
Date: Monday, November 19, 2007 | Sheet 1 of 57

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
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DIS

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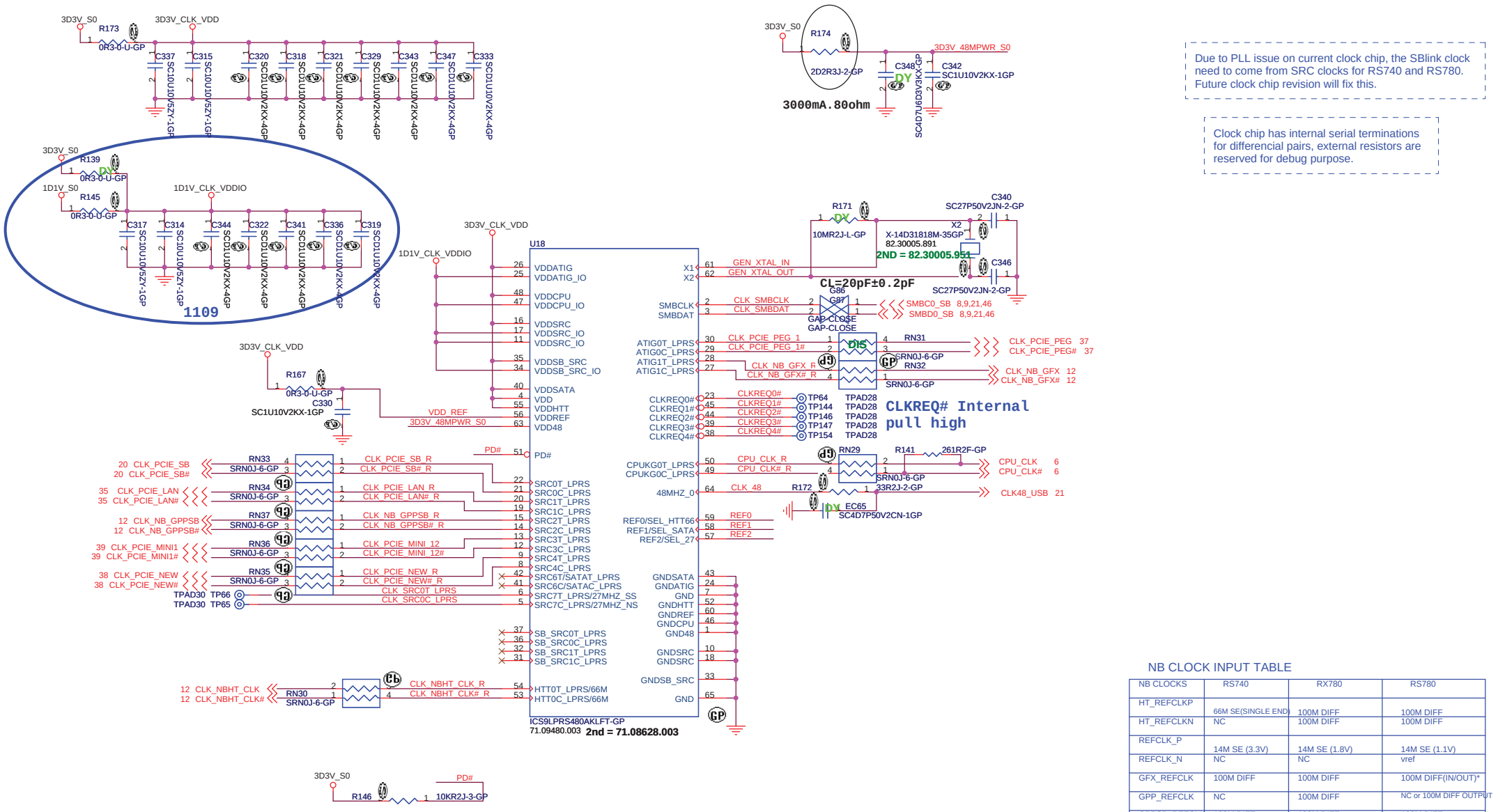
Title: ***HISTORY***

Size: A3 | Document Number: **Olan** | Rev: SA

Date: Monday, November 19, 2007 | Sheet 2 of 57



Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

DIS

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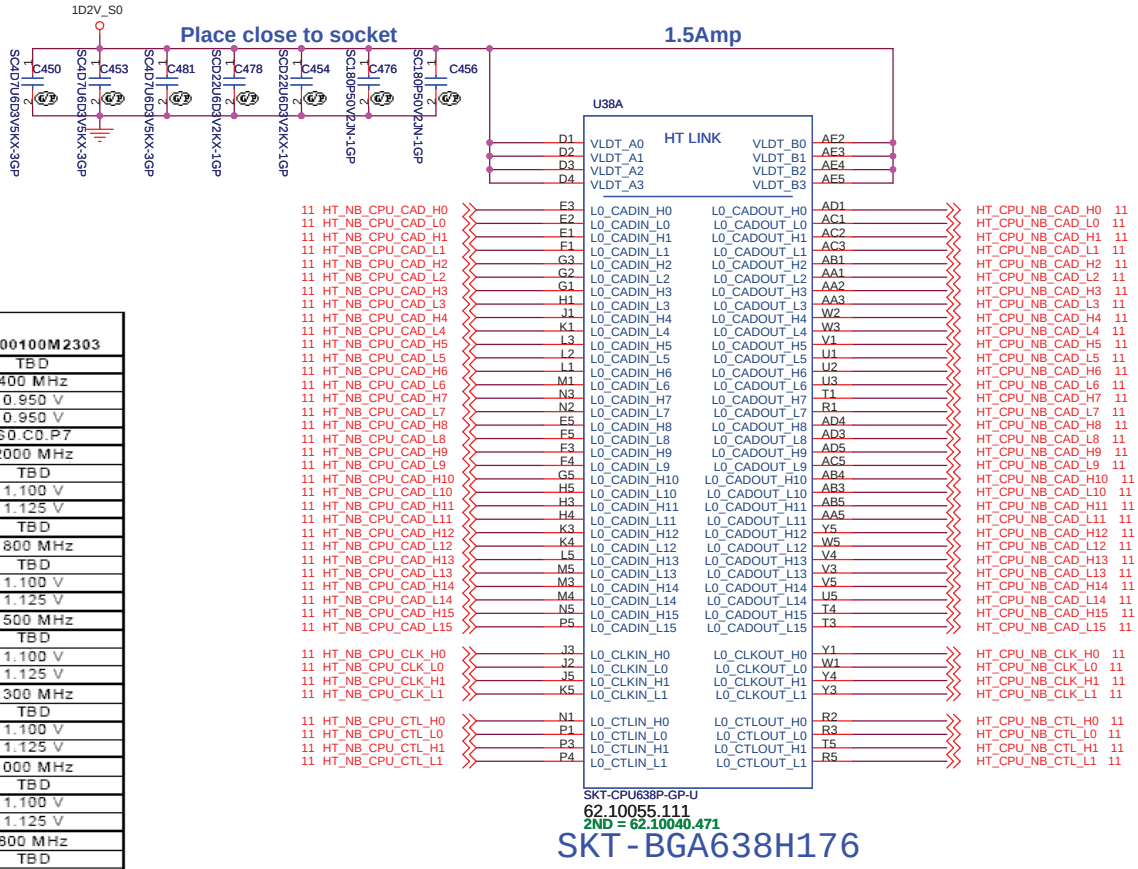
Title: CLKGEN_ICS9LPRS473

Size	Document Number	Rev
A3	Olan	SA

Date: Monday, November 19, 2007 Sheet 3 of 57



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

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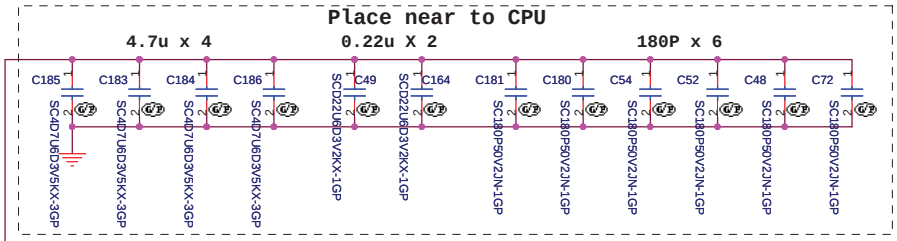
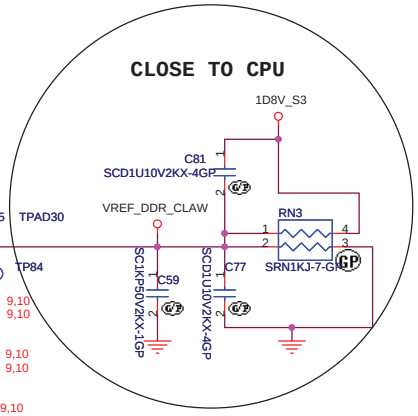
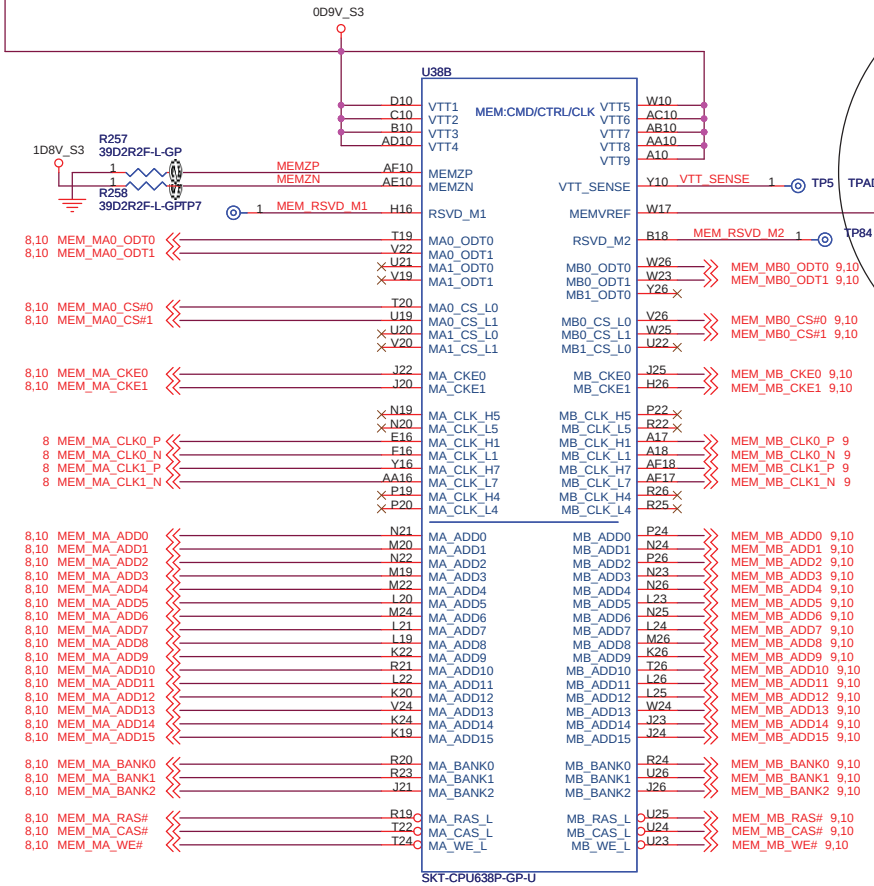
Title: ***CPU_HT_LINK I/F_(1/4)***

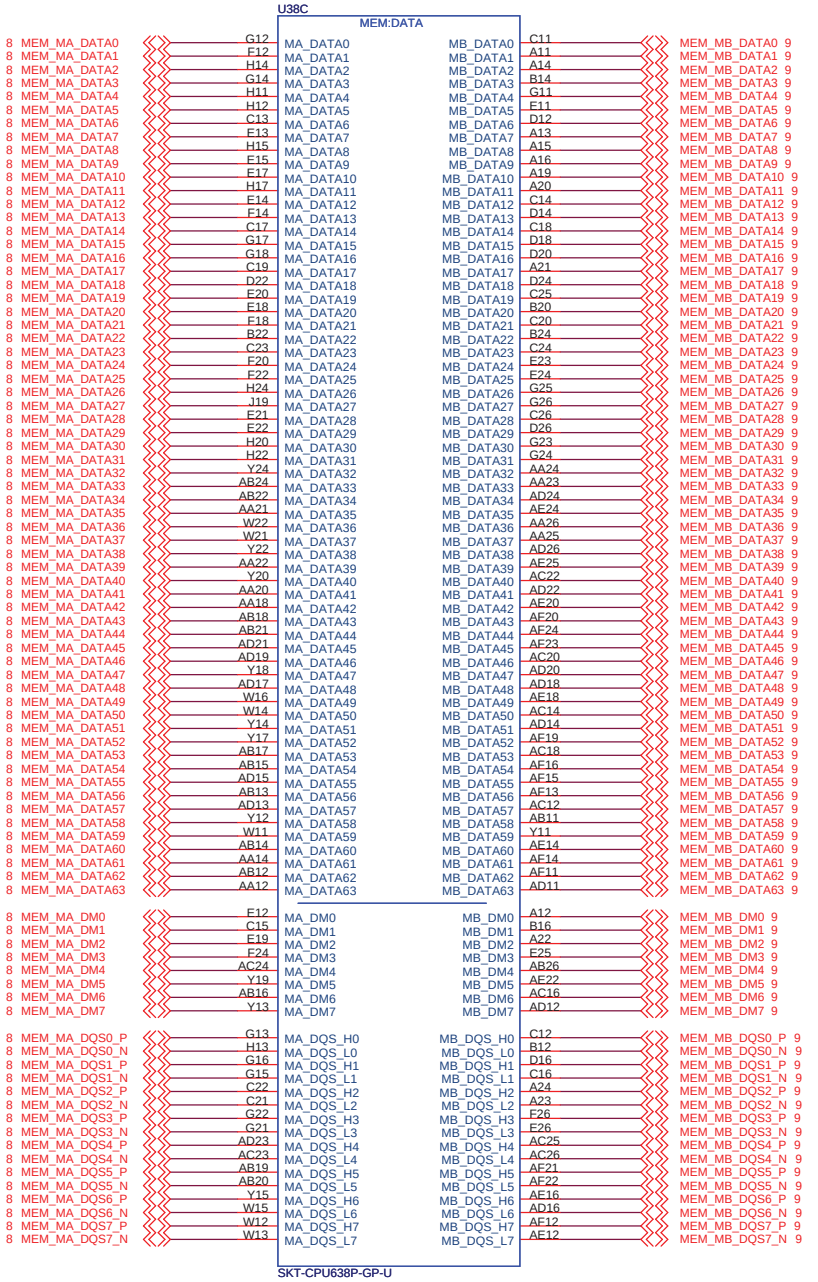
Size	Document Number	Rev
A3	Olan	SA

Date: Monday, November 19, 2007 Sheet 4 of 57









DIS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU_DDR_(2/4)***	
Size: A3	Document Number: **Olan**	Rev: SA
Date: Monday, November 19, 2007	Sheet 5 of 57	

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

SA Short

Near CPU PIN

CPU exceeds 125℃

SKT-CPU638P-GP-U

HDT Connectors

SMC-CONN26A-FP

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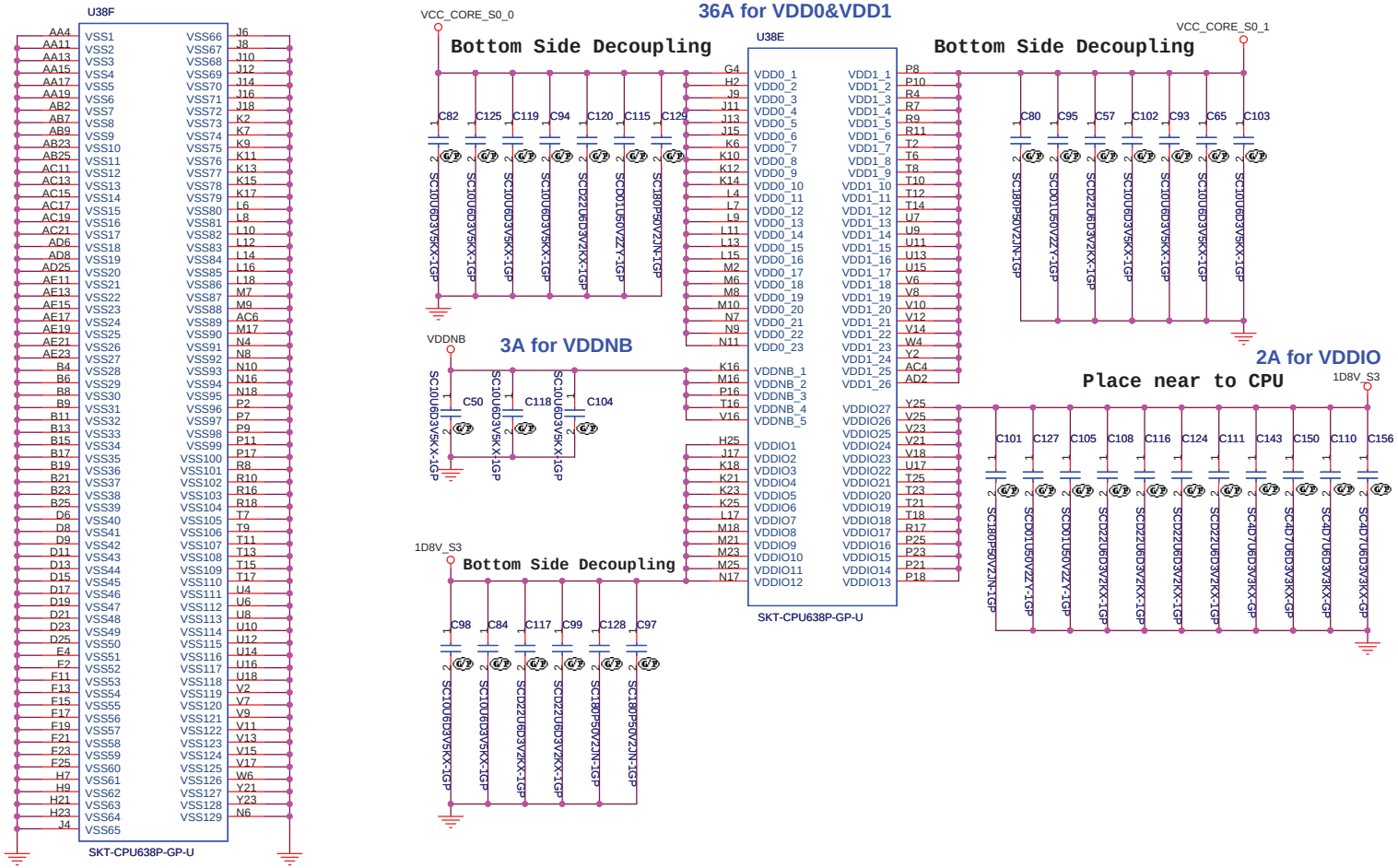
Title: CPU_Control&Debug_(3/4)

Size	Document Number	Rev
A3	Olan	SA

Date: Monday, November 19, 2007 Sheet 6 of 57



DIS

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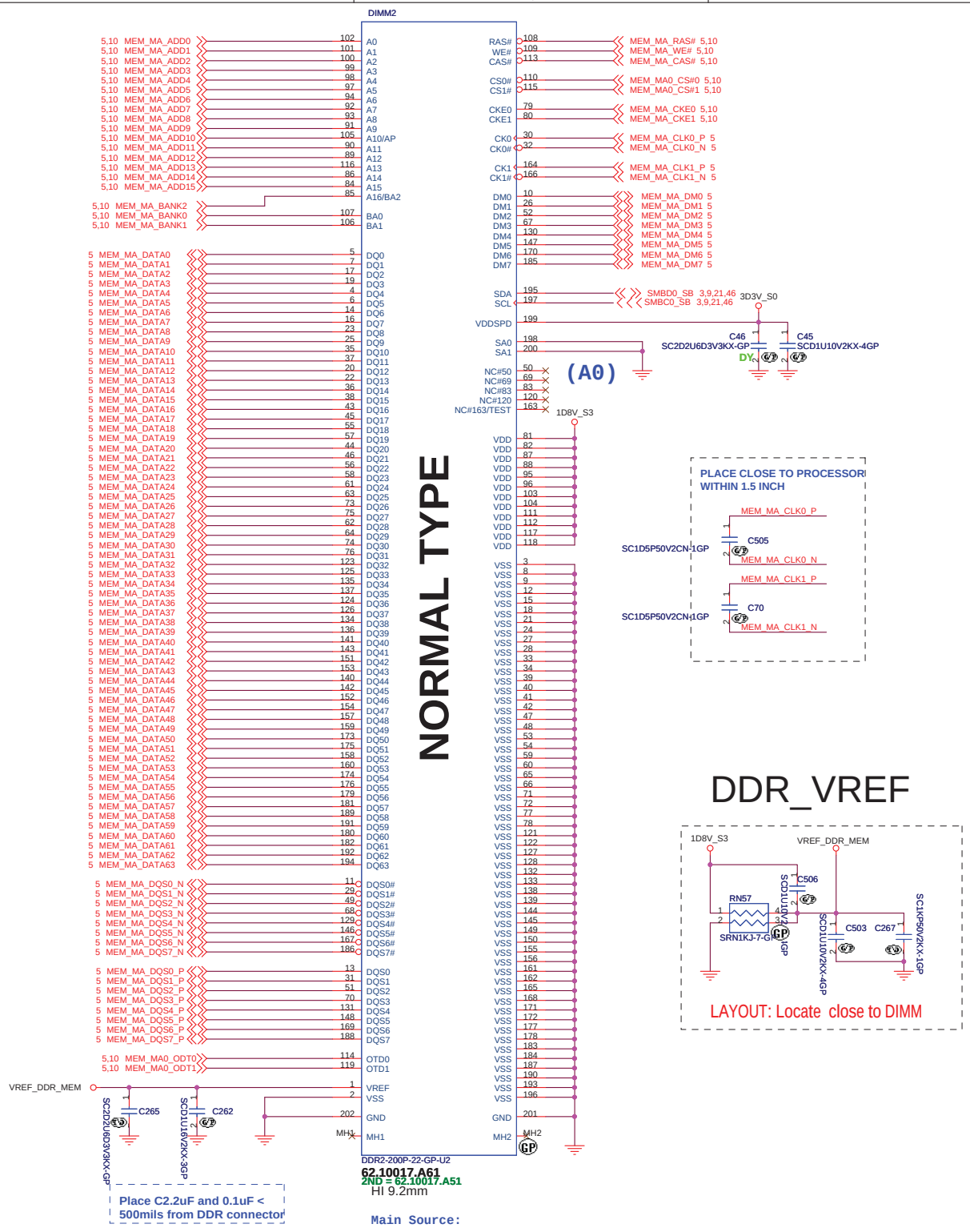
Title: ***CPU_Power_(4/4)***

Size	Document Number	Rev
A3	Olan	SA

Date: Monday, November 19, 2007 Sheet 7 of 57



DIS

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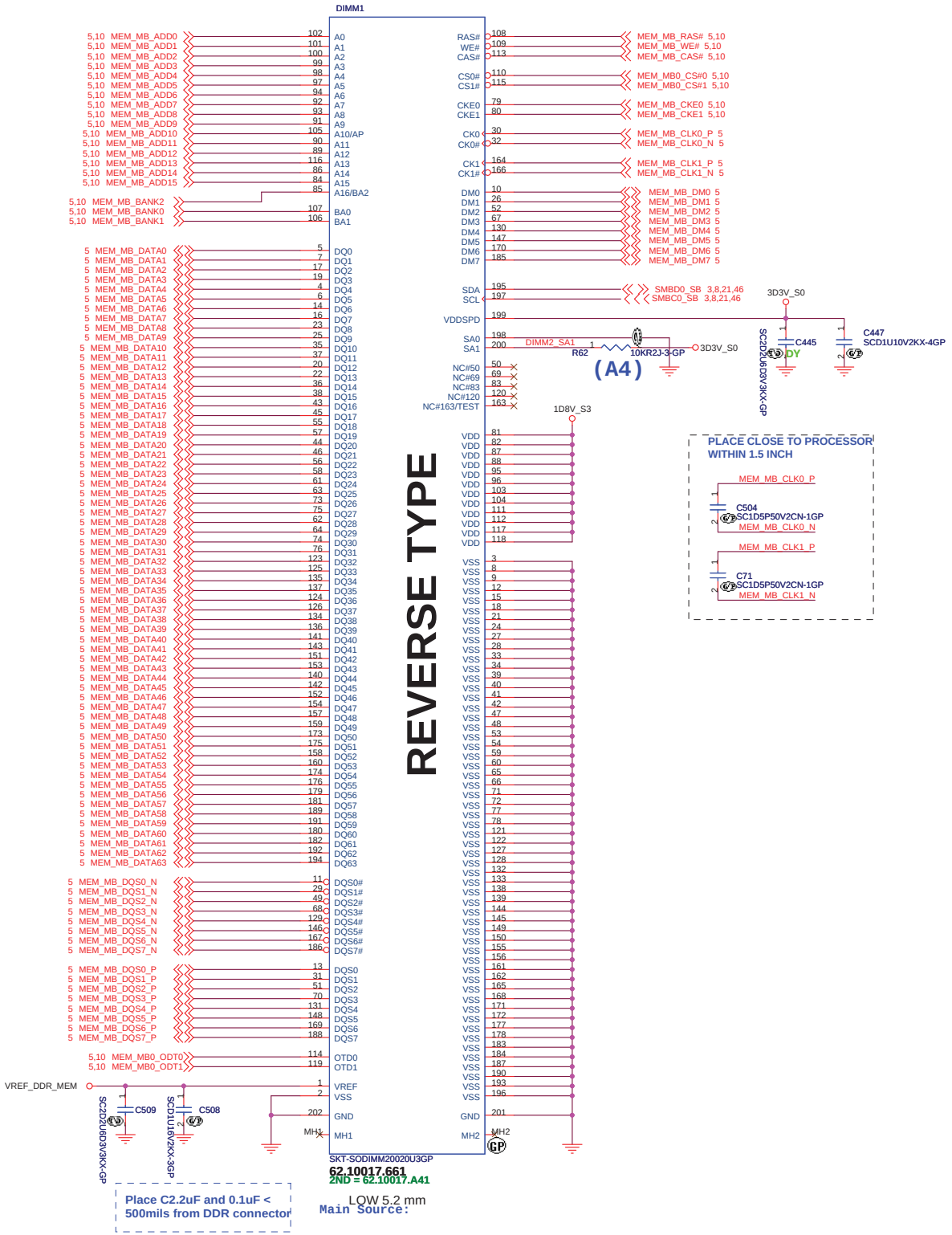
Title: DDR_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	Olan	SA

Date: Monday, November 19, 2007 Sheet 8 of 57



DIS

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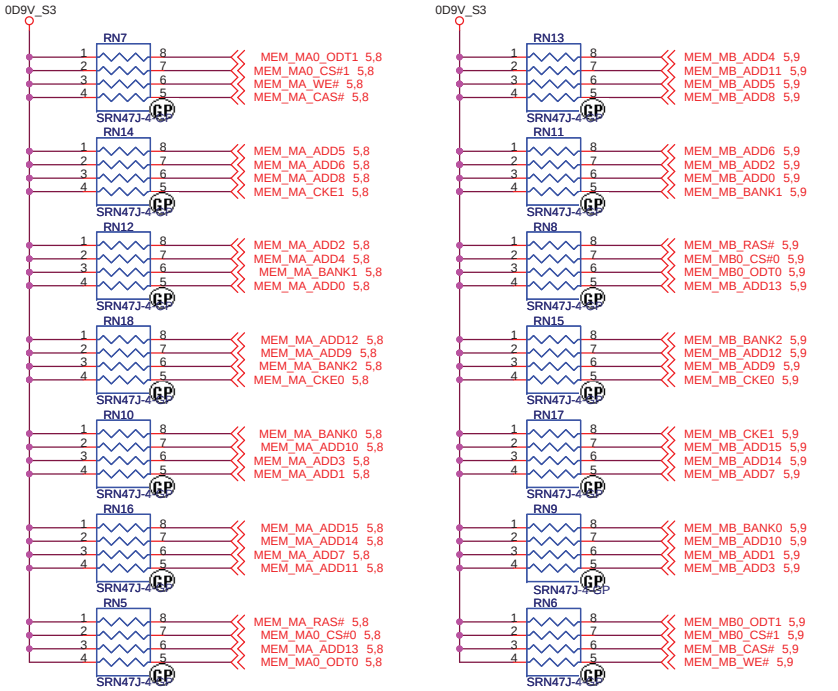
Title: DDR_SO-DIMM SKT_2

Size: Custom | Document Number: Olan | Rev: SA

Date: Monday, November 19, 2007 | Sheet 9 of 57

PARALLEL TERMINATION

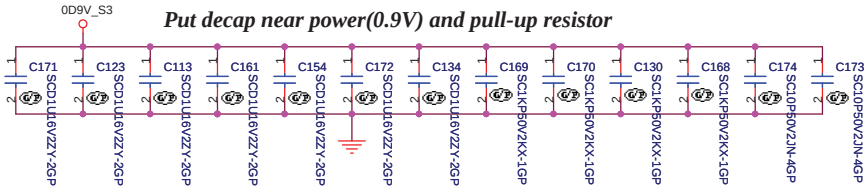
Put decap near power(0.9V) and pull-up resistor



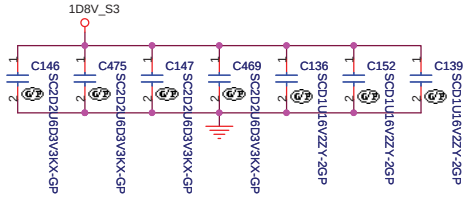
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

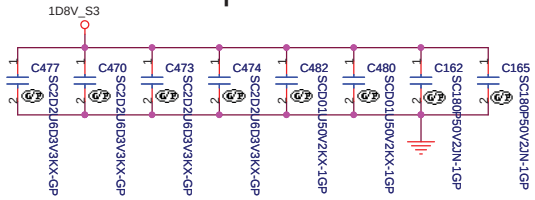


Place these Caps near DM1



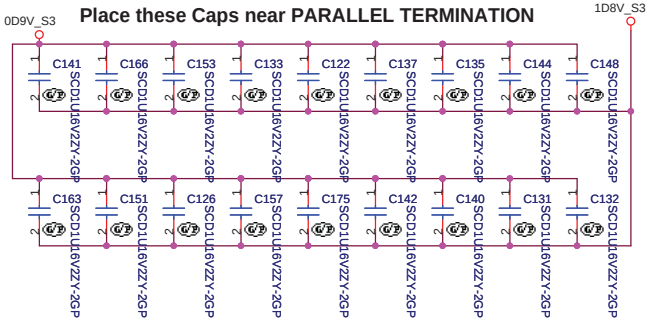
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



DIS

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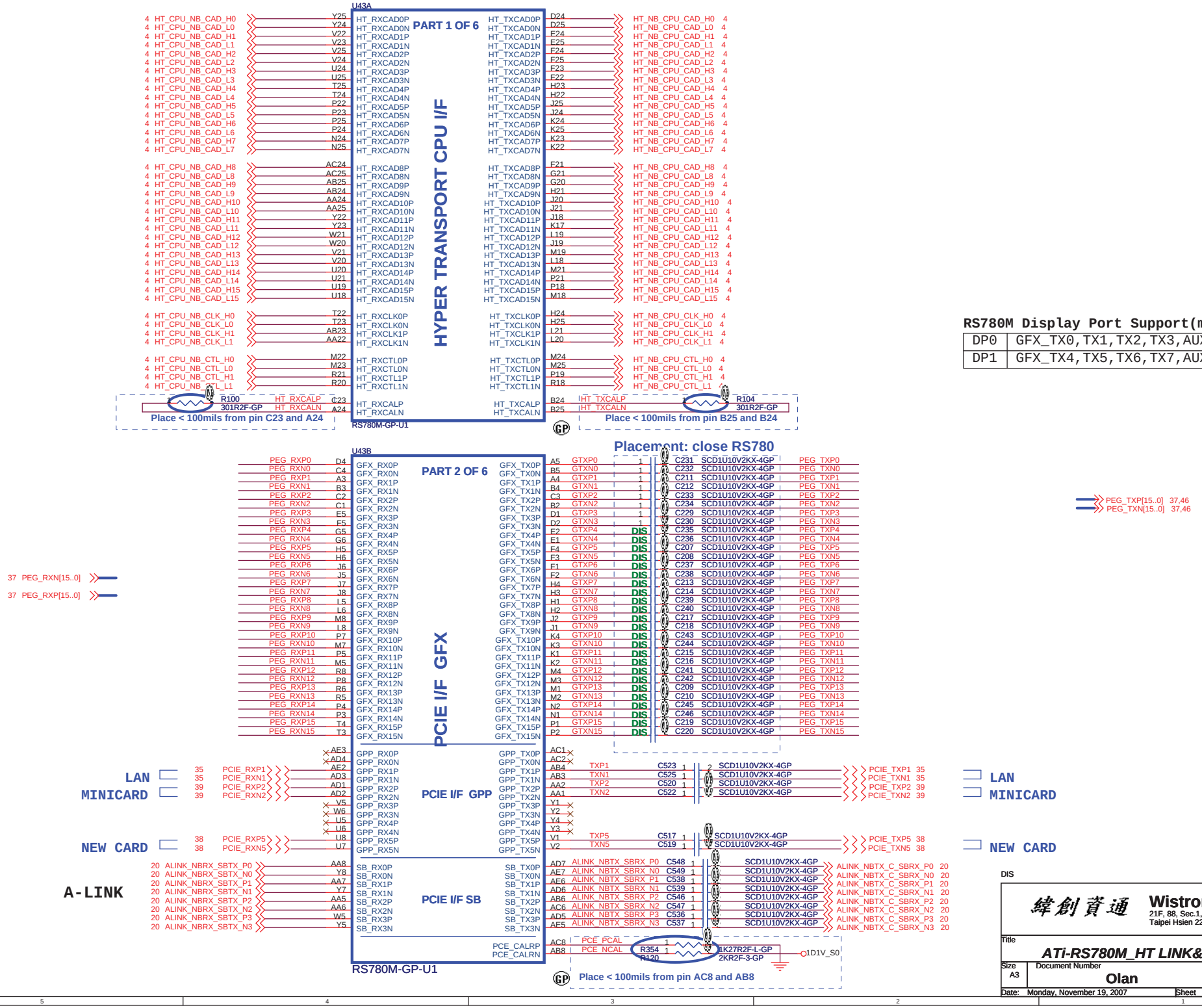
Title: ***DDR_DAMPING & TERMINATION***

Size	Document Number	Rev
A3	Olan	SA

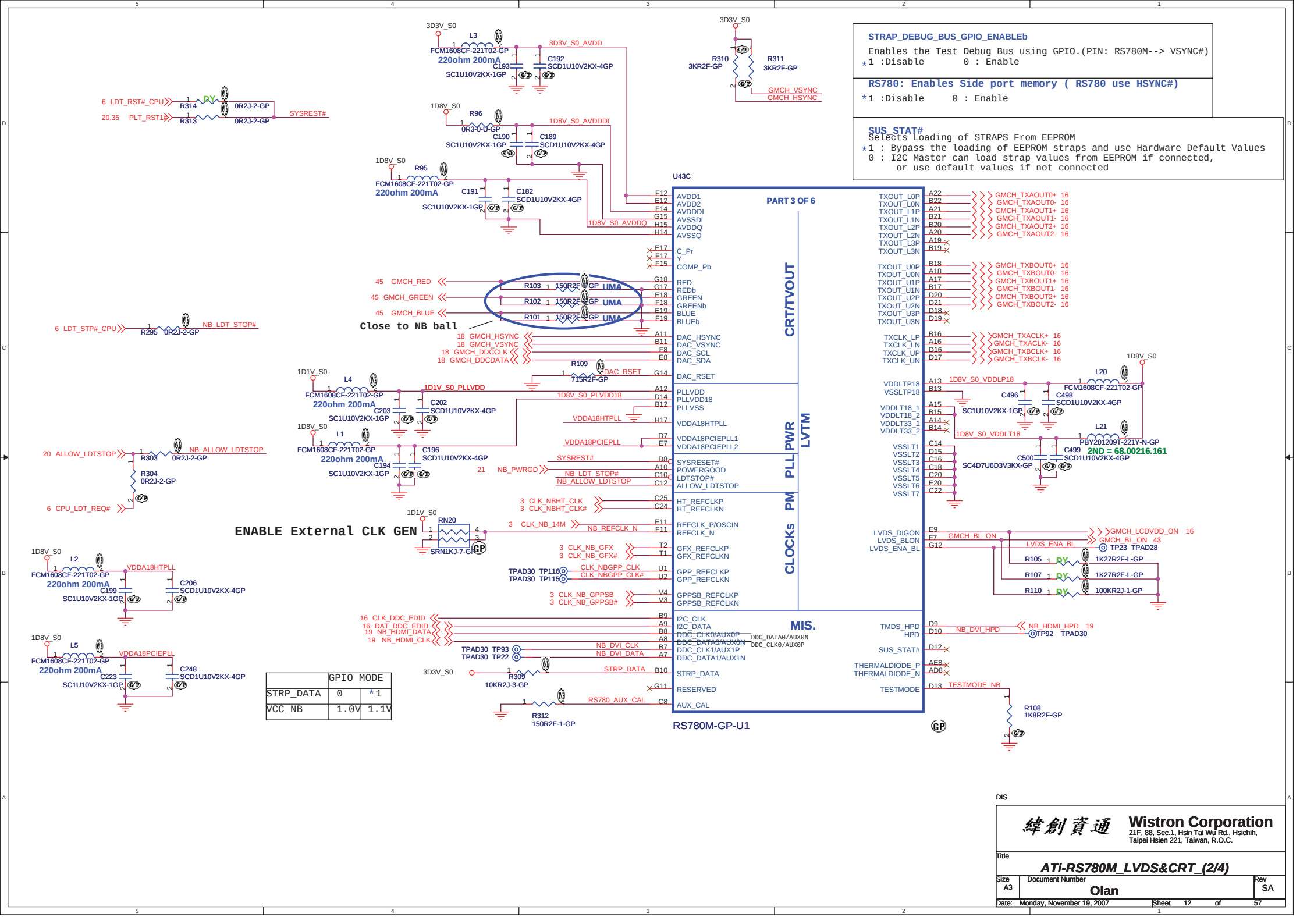
Date: Monday, November 19, 2007 Sheet 10 of 57



RS780M Display Port Support(muxed on GFX)

DP0	GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1	GFX_TX4,TX5,TX6,TX7,AUX1,HPD1

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***ATi-RS780M_HT LINK&PCIe(1/3)***		
Size: A3	Document Number: **Olan**		Rev: SA
Date: Monday, November 19, 2007	Sheet 11 of 57		


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
U43C
PART 3 OF 6
CRT/TVOUT
PWR
LVTM
PLL
PM
CLOCKs
MIS.
RS780M-GP-U1
Close to NB ball
ENABLE External CLK GEN
GPIO MODE
STRP_DATA 0 *1
VCC_NB 1.0V 1.1V
Wistron Corporation
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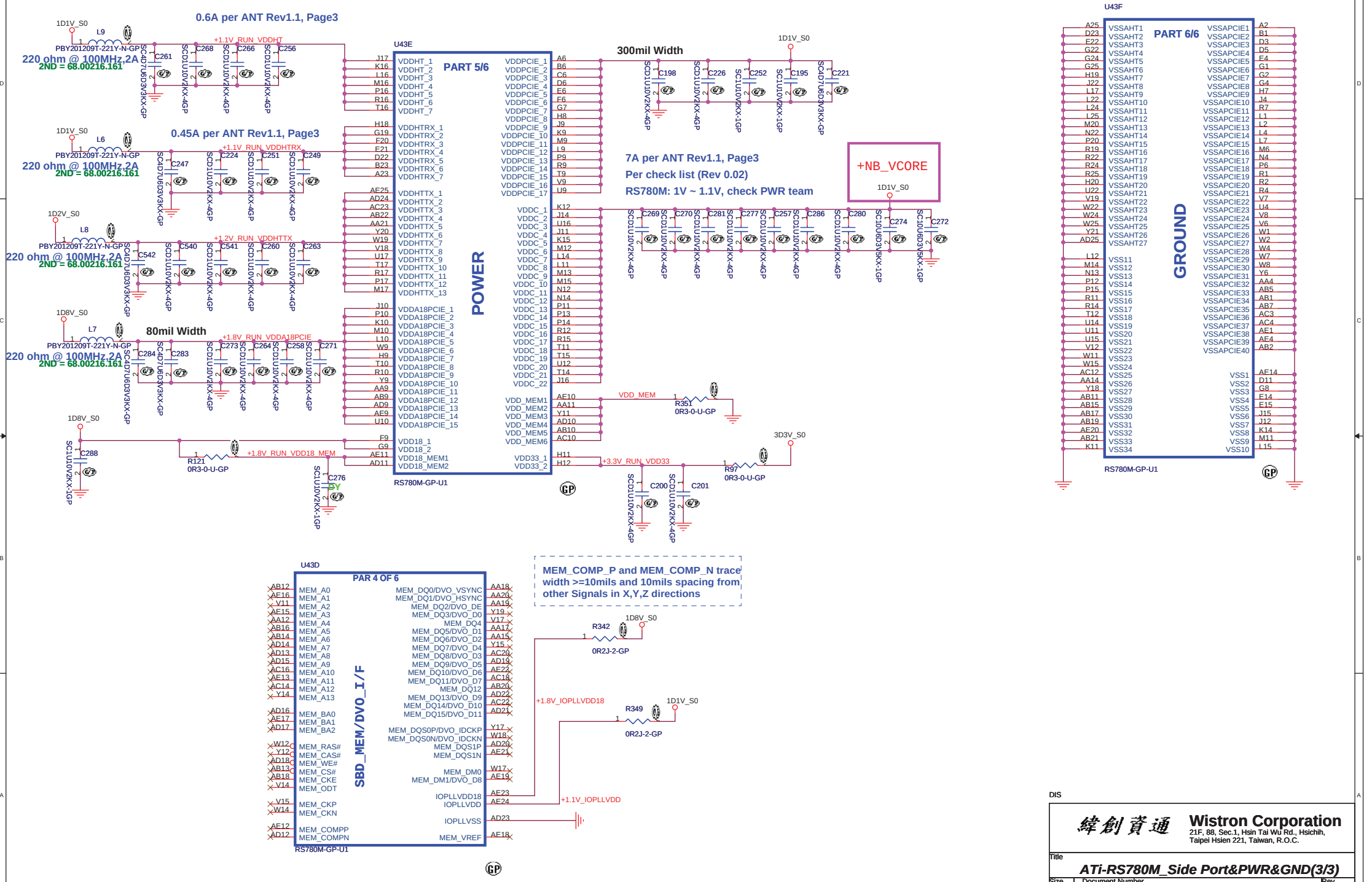
Title
ATi-RS780M_LVDS&CRT_(2/4)
Size A3
Document Number Olan
Rev SA
Date: Monday, November 19, 2007
Sheet 12 of 57


0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
7A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
220 ohm @ 100MHz,2A
2ND = 68.00216.161
U43E
PART 5/6
POWER
RS780M-GP-U1
U43F
PART 6/6
GROUND
U43D
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
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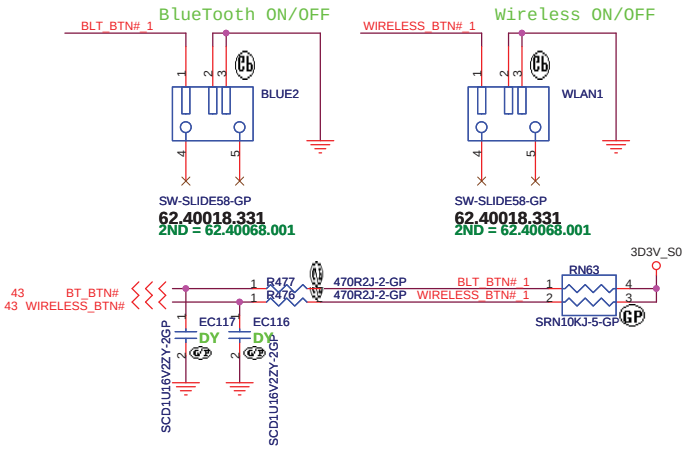
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_Side Port&PWR&GND(3/3)
Olan
Monday, November 19, 2007
Sheet 13 of 57



DIS

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Title: ***SWITCH***

Size	Document Number	Rev
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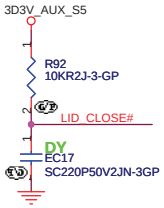
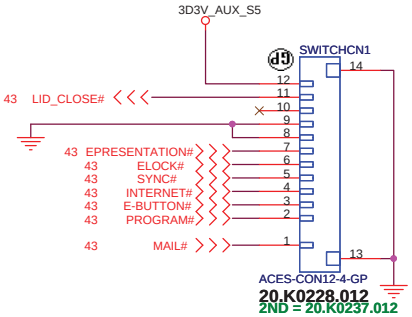
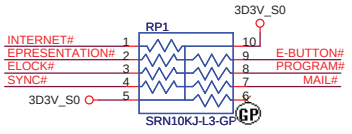
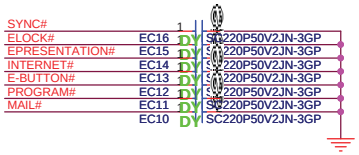
Date: Monday, November 19, 2007 Sheet 14 of 57

LAUNCH









DIS

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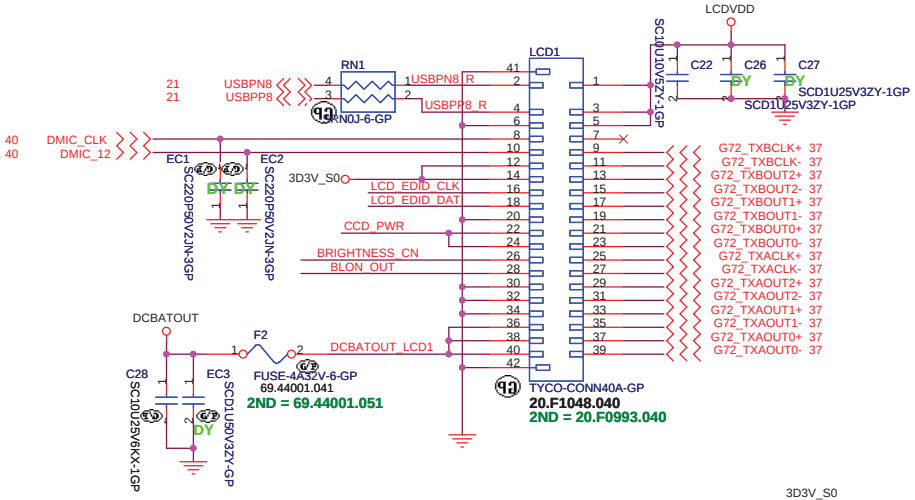
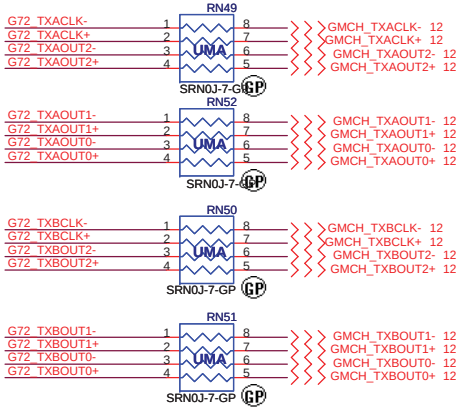
Title: LAUNCH

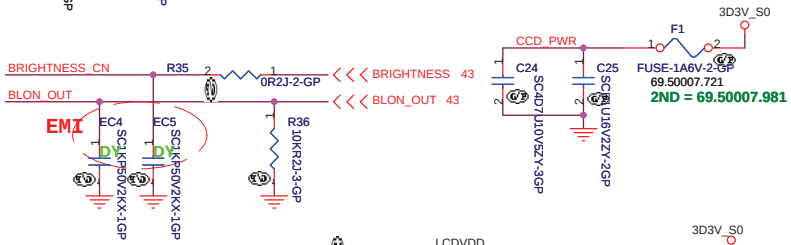
Size	Document Number	Rev
A3	Olan	SA

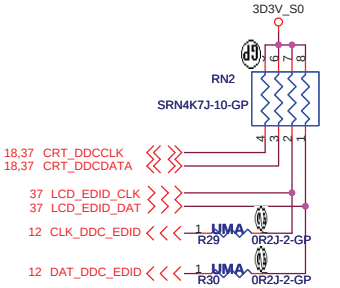
Date: Monday, November 19, 2007 Sheet 15 of 57

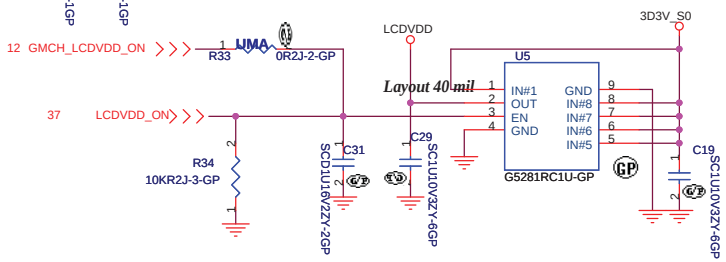
LCD/INVERTER/CCD CONN











DIS

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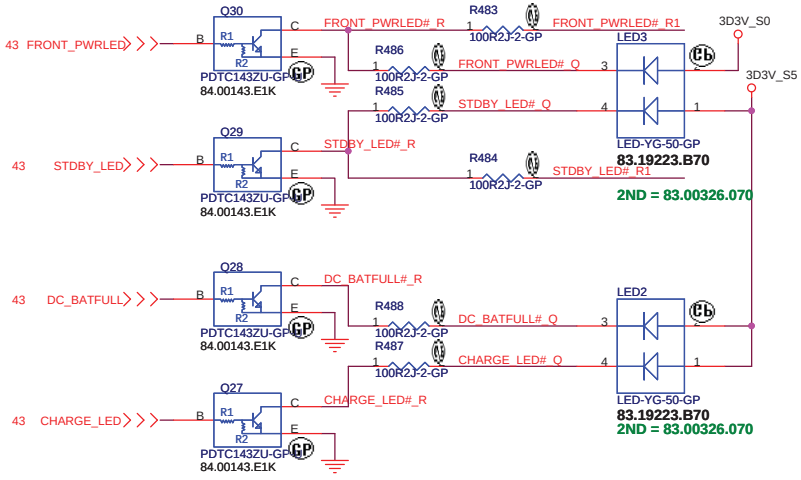
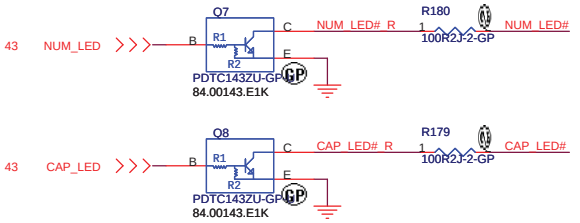
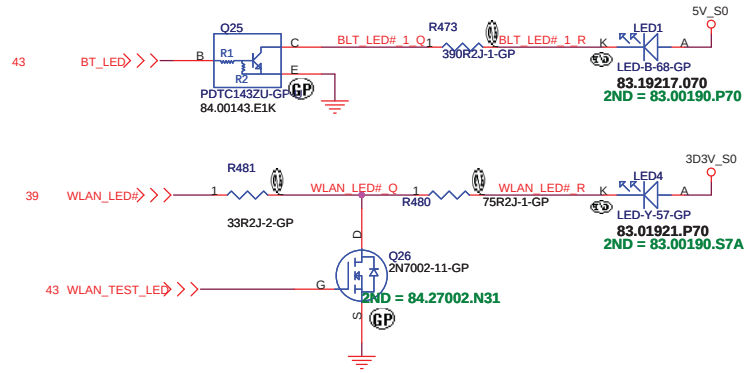
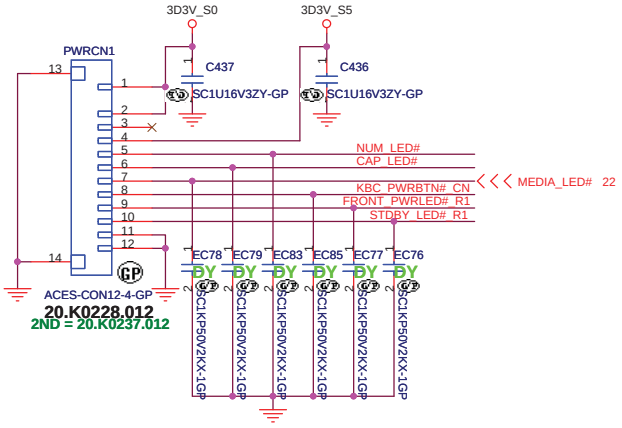
Title		
LCD CONN		
Size: A3	Document Number: Olan	Rev: SA
Date: Monday, November 19, 2007	Sheet 16 of 57	

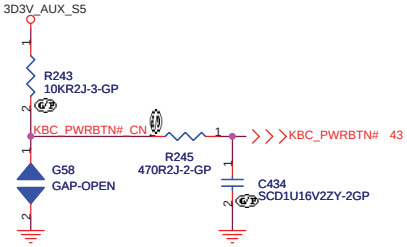
LED











緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LED & LAUNCH		
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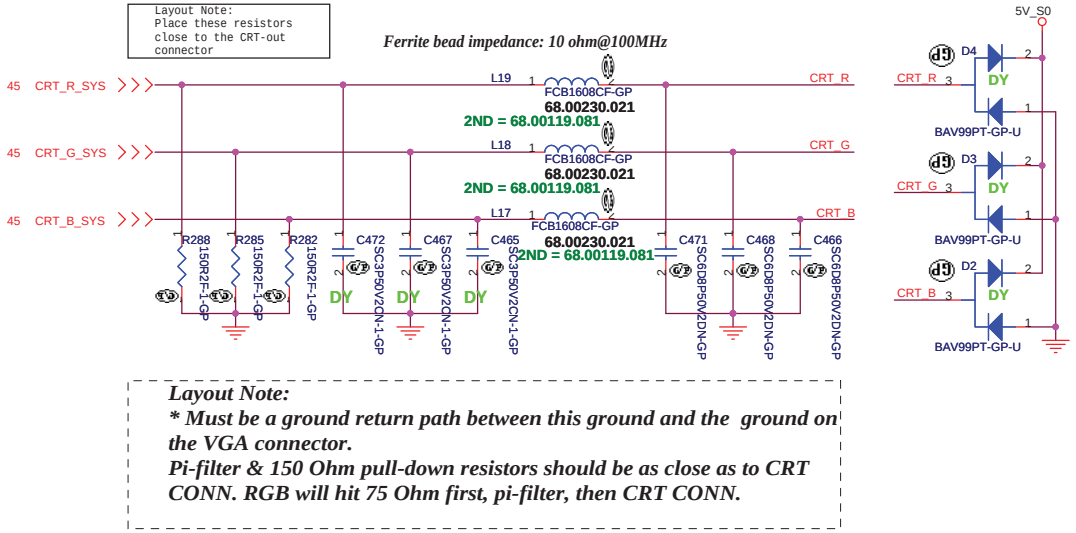
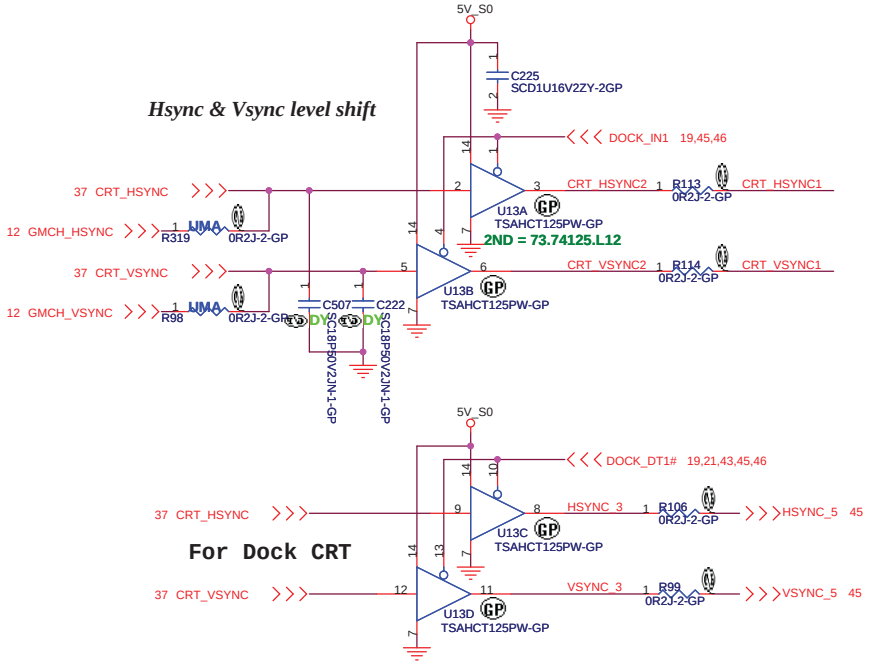
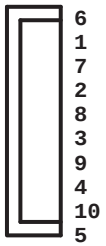
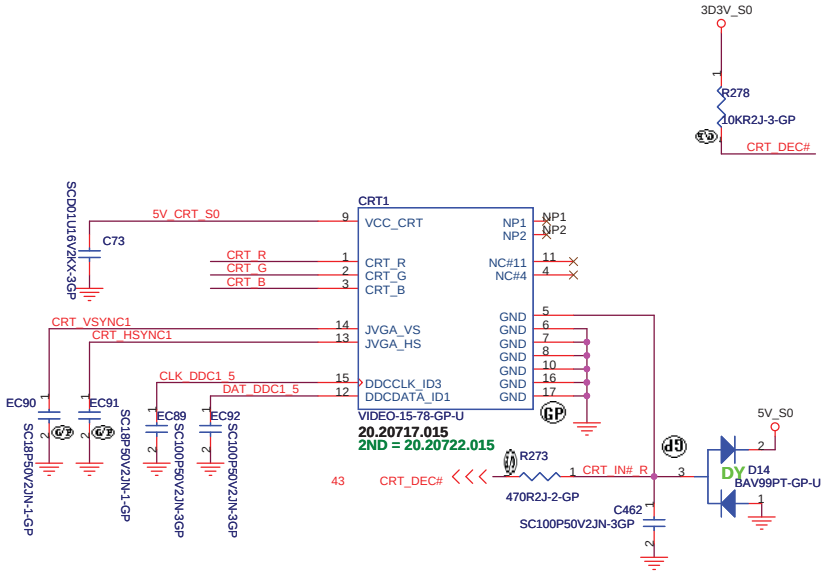


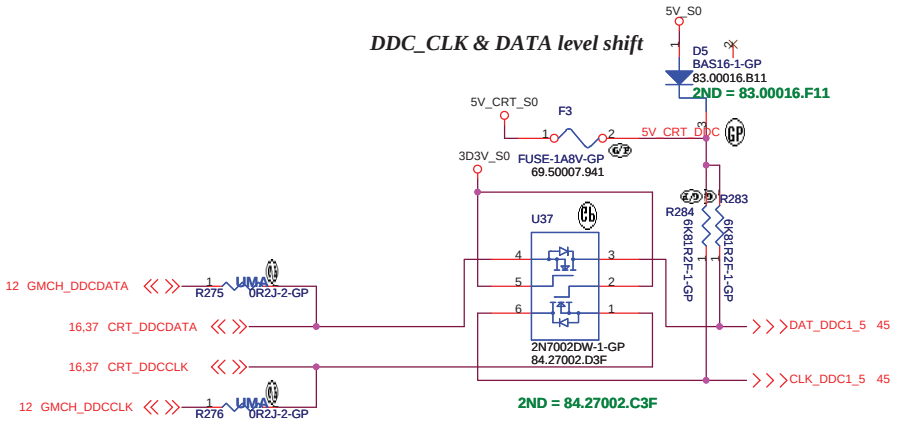
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



CRT I/F & CONNECTOR







DIS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT Connector***	
Size	Document Number **Olan**	Rev SA
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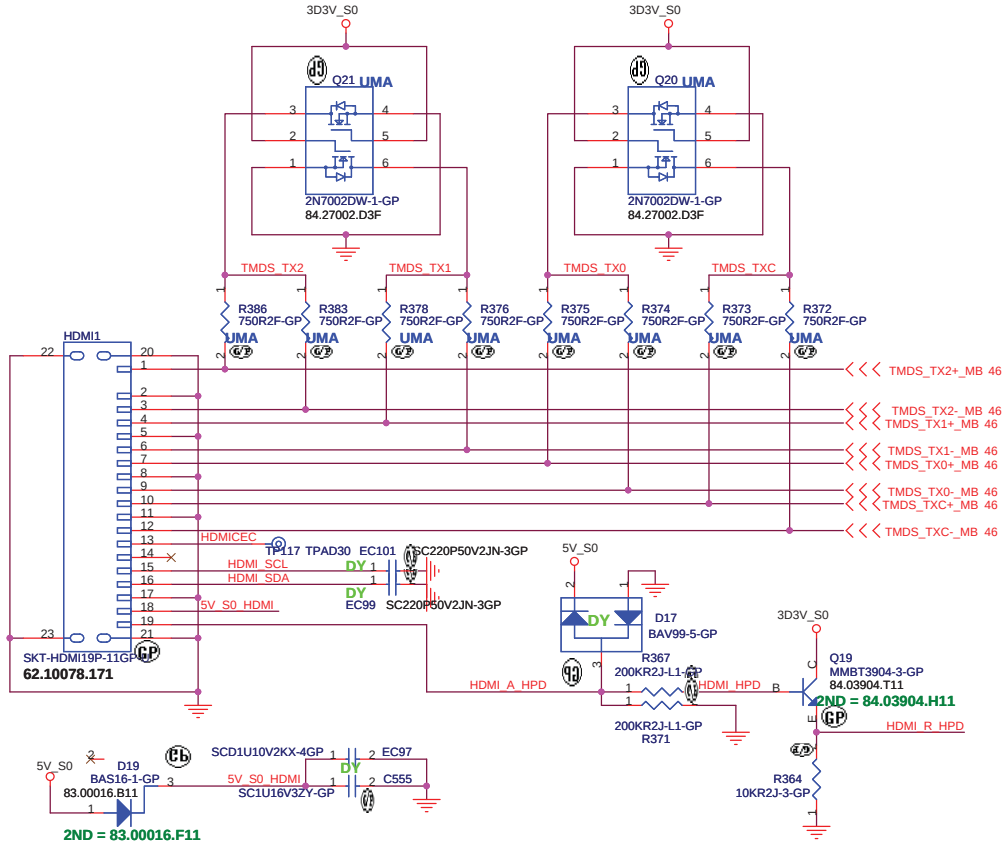
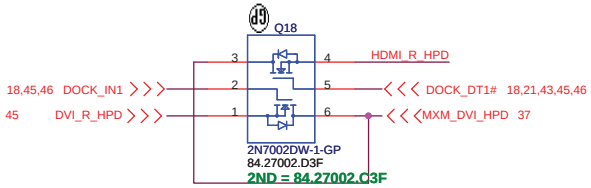
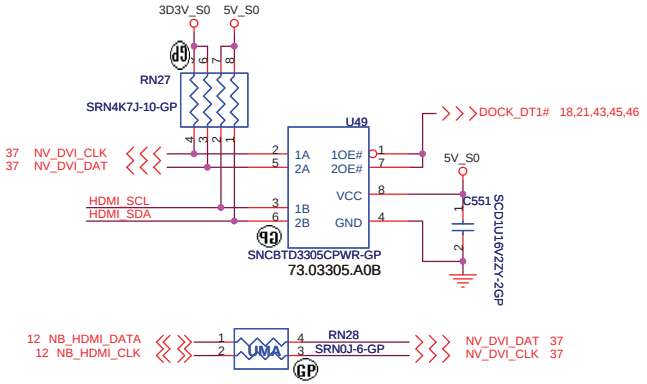
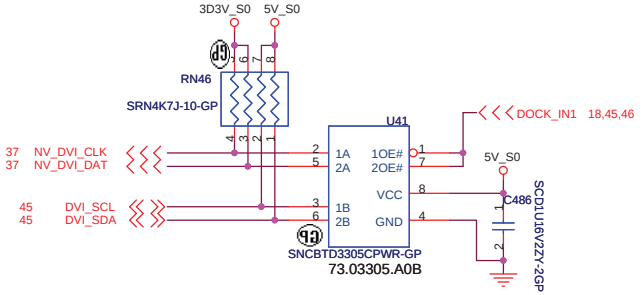




HDMI LEVEL shifter



DVI LEVEL shifter



DIS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI CONNECTOR**

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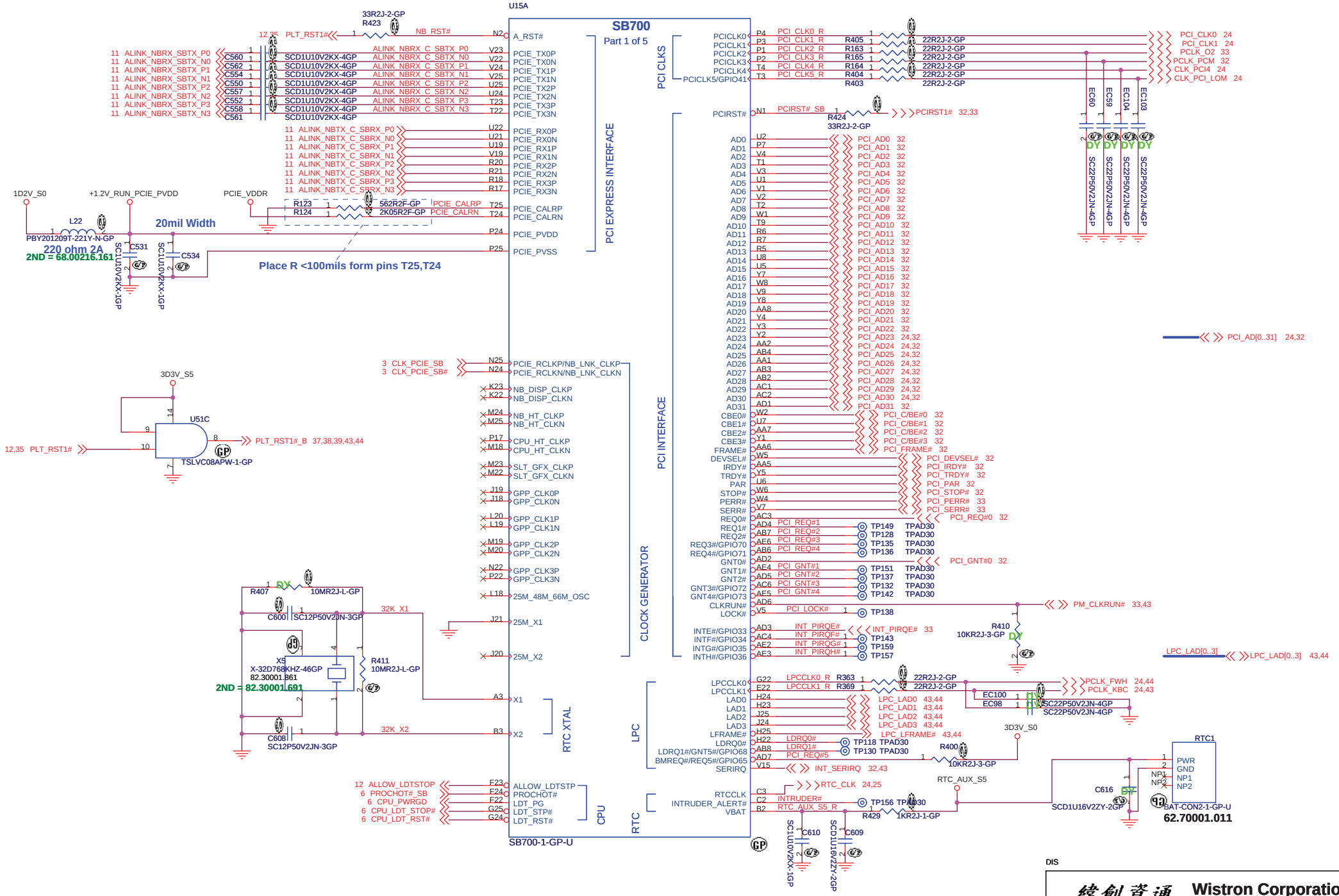
U15A
SB700
Part 1 of 5
SB700-1-GP-U
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
RTC
CPU
33R2J-2-GP
R423
PLT_RST1#
NB_RST#
ALINK_NBRX_SBTX_P0
ALINK_NBRX_SBTX_N0
ALINK_NBRX_SBTX_P1
ALINK_NBRX_SBTX_N1
ALINK_NBRX_SBTX_P2
ALINK_NBRX_SBTX_N2
ALINK_NBRX_SBTX_P3
ALINK_NBRX_SBTX_N3
SCD1U10V2KX-4GP
ALINK_NBRX_C_SBTX_P0
ALINK_NBRX_C_SBTX_N0
ALINK_NBRX_C_SBTX_P1
ALINK_NBRX_C_SBTX_N1
ALINK_NBRX_C_SBTX_P2
ALINK_NBRX_C_SBTX_N2
ALINK_NBRX_C_SBTX_P3
ALINK_NBRX_C_SBTX_N3
ALINK_NBTX_C_SBRX_P0
ALINK_NBTX_C_SBRX_N0
ALINK_NBTX_C_SBRX_P1
ALINK_NBTX_C_SBRX_N1
ALINK_NBTX_C_SBRX_P2
ALINK_NBTX_C_SBRX_N2
ALINK_NBTX_C_SBRX_P3
ALINK_NBTX_C_SBRX_N3
1D2V_S0
+1.2V_RUN_PCIE_PVDD
PCIE_VDDR
L22
PBY201209T-221Y-N-GP
220 ohm 2A
2ND = 68.00216.161
20mil Width
C531
C534
SC1U10V2KX-1GP
R123
R124
562R2F-GP
2K05R2F-GP
PCIE_CALRP
PCIE_CALRN
Place R <100mils form pins T25,T24
3D3V_S5
U51C
TSLVC08APW-1-GP
PLT_RST1#_B 37,38,39,43,44
CLK_PCIE_SB
CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
25M_48M_66M_OSC
25M_X1
25M_X2
32K_X1
32K_X2
R407
10MR2J-L-GP
C600
SC12P50V2JN-3GP
X5
X-32D768KHZ-46GP
82.30001.861
2ND = 82.30001.691
R411
10MR2J-L-GP
C608
SC12P50V2JN-3GP
ALLOW_LDTSTOP
PROCHOT#_SB
CPU_PWRGD
CPU_LDT_STOP#
CPU_LDT_RST#
ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCI_CLK0_R
PCI_CLK1_R
PCI_CLK2_R
PCI_CLK3_R
PCI_CLK4_R
PCI_CLK5_R
R405
R163
R165
R164
R404
R403
22R2J-2-GP
PCI_CLK0 24
PCI_CLK1 24
PCLK_O2 33
PCLK_PCM 32
CLK_PCI4 24
CLK_PCI_LOM 24
EC60
EC59
EC104
EC103
SC22P50V2JN-4GP
PCIRST#
PCIRST_SB
R424
33R2J-2-GP
PCIRST1# 32,33
PCI_AD0 32
PCI_AD1 32
PCI_AD2 32
PCI_AD3 32
PCI_AD4 32
PCI_AD5 32
PCI_AD6 32
PCI_AD7 32
PCI_AD8 32
PCI_AD9 32
PCI_AD10 32
PCI_AD11 32
PCI_AD12 32
PCI_AD13 32
PCI_AD14 32
PCI_AD15 32
PCI_AD16 32
PCI_AD17 32
PCI_AD18 32
PCI_AD19 32
PCI_AD20 32
PCI_AD21 32
PCI_AD22 32
PCI_AD23 24,32
PCI_AD24 24,32
PCI_AD25 24,32
PCI_AD26 24,32
PCI_AD27 24,32
PCI_AD28 24,32
PCI_AD29 24,32
PCI_AD30 24,32
PCI_AD31 32
PCI_AD[0..31] 24,32
PCI_C/BE#0 32
PCI_C/BE#1 32
PCI_C/BE#2 32
PCI_C/BE#3 32
PCI_FRAME# 32
PCI_DEVSEL# 32
PCI_IRDY# 32
PCI_TRDY# 32
PCI_PAR 32
PCI_STOP# 32
PCI_PERR# 33
PCI_SERR# 33
PCI_REQ#0 32
PCI_GNT#0 32
TP149 TPAD30
TP128 TPAD30
TP135 TPAD30
TP136 TPAD30
TP151 TPAD30
TP137 TPAD30
TP132 TPAD30
TP142 TPAD30
TP138
PM_CLKRUN# 33,43
R410
10KR2J-3-GP
INT_PIRQE# 33
INT_PIRQF#
INT_PIRQG#
INT_PIRQH#
TP143
TP159
TP157
LPC_LAD[0..3]
LPC_LAD[0..3] 43,44
LPCCLK0_R
LPCCLK1_R
R363
R369
PCLK_FWH 24,44
PCLK_KBC 24,43
EC100
EC98
LPC_LAD0 43,44
LPC_LAD1 43,44
LPC_LAD2 43,44
LPC_LAD3 43,44
LPC_LFRAME# 43,44
LDRQ0#
LDRQ1#
TP118 TPAD30
TP130 TPAD30
PCI_REQ#5
R400
10KR2J-3-GP
3D3V_S0
INT_SERIRQ 32,43
RTC_CLK 24,25
INTRUDER#
TP156 TPAD30
RTC_AUX_S5_R
R429
1KR2J-1-GP
RTC_AUX_S5
C610
C609
SC1U10V2KX-1GP
SCD1U16V2ZY-2GP
C616
SCD1U16V2ZY-2GP
RTC1
BAT-CON2-1-GP-U
62.70001.011
PWR
GND
NP1
NP2
DIS
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_PCIE&PCI_(1/5)
Size
A3
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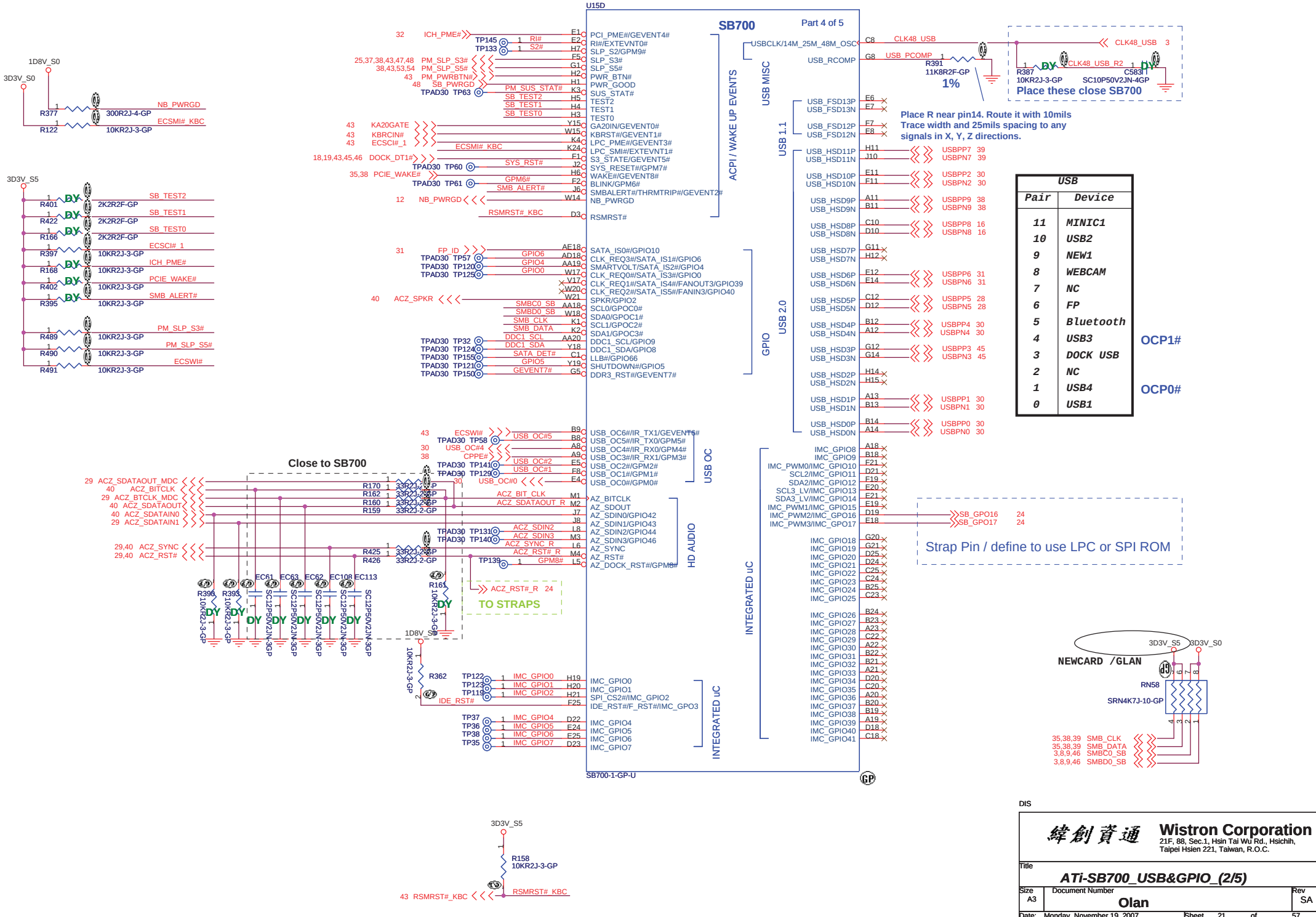
U15D
SB700
Part 4 of 5
SB700-1-GP-U
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB MISC
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB 1.1
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
USB 2.0
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
GPIO
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
USB OC
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
HD AUDIO
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
INTEGRATED uC
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
INTEGRATED uC
CLK48_USB
USB_PCOMP
R391 11K8R2F-GP 1%
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
R387 10KR2J-3-GP
C583 SC10P50V2JN-4GP
Place these close SB700
USB
Pair | Device
11 MINIC1
10 USB2
9 NEW1
8 WEBCAM
7 NC
6 FP
5 Bluetooth
4 USB3 OCP1#
3 DOCK USB
2 NC
1 USB4 OCP0#
0 USB1
Strap Pin / define to use LPC or SPI ROM
SB_GPO16
SB_GPO17
Close to SB700
TO STRAPS
ACZ_RST#_R
NEWCARD /GLAN
RN58
SRN4K7J-10-GP
R158 10KR2J-3-GP
RSMRST#_KBC
1D8V_S0
3D3V_S0
3D3V_S5
R377 300R2J-4-GP
R122 10KR2J-3-GP
NB_PWRGD
ECSMI#_KBC
R401 2K2R2F-GP
R422 2K2R2F-GP
R166 2K2R2F-GP
R397 10KR2J-3-GP
R168 10KR2J-3-GP
R402 10KR2J-3-GP
R395 10KR2J-3-GP
SB_TEST2
SB_TEST1
SB_TEST0
ECSCI#_1
ICH_PME#
PCIE_WAKE#
SMB_ALERT#
R489 10KR2J-3-GP
R490 10KR2J-3-GP
R491 10KR2J-3-GP
PM_SLP_S3#
PM_SLP_S5#
ECSWI#
R170 33R2J-2-GP
R162 33R2J-2-GP
R160 33R2J-2-GP
R159 33R2J-2-GP
R425 33R2J-2-GP
R426 33R2J-2-GP
R396 10KR2J-3-GP
R393 10KR2J-3-GP
R161 10KR2J-3-GP
R362 10KR2J-3-GP
EC61 SC12P50V2JN-3GP
EC63 SC12P50V2JN-3GP
EC62 SC12P50V2JN-3GP
EC108 SC12P50V2JN-3GP
EC113 SC12P50V2JN-3GP
ACZ_BIT_CLK
ACZ_SDATAOUT_R
ACZ_SDIN2
ACZ_SDIN3
ACZ_SYNC_R
ACZ_RST#_R
GPM8#
IDE_RST#
SMB_CLK
SMB_DATA
SMBC0_SB
SMBD0_SB
ACZ_SDATAOUT_MDC
ACZ_BITCLK
ACZ_BTCLK_MDC
ACZ_SDATAOUT
ACZ_SDATAIN0
ACZ_SDATAIN1
ACZ_SYNC
ACZ_RST#
KA20GATE
KBRCIN#
ECSCI#_1
ECSMI#_KBC
DOCK_DT1#
SYS_RST#
PCIE_WAKE#
GPM6#
SMB_ALERT#
NB_PWRGD
RSMRST#_KBC
FP_ID
GPIO6
GPIO4
GPIO0
ACZ_SPKR
SMBC0_SB
SMBD0_SB
SMB_CLK
SMB_DATA
DDC1_SCL
DDC1_SDA
SATA_DET#
GPIO5
GEVENT7#
ECSWI#
USB_OC#5
USB_OC#4
CPPE#
USB_OC#2
USB_OC#1
USB_OC#0
PM_SLP_S3#
PM_SLP_S5#
KBRST#
IMC_GPIO0
IMC_GPIO1
IMC_GPIO2
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
TP145
TP133
TP63
TP60
TP61
TP57
TP120
TP125
TP58
TP141
TP129
TP131
TP140
TP139
TP32
TP124
TP155
TP121
TP150
TP122
TP123
TP119
TP37
TP36
TP38
TP35
DIS
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_USB&GPIO_(2/5)
Size A3
Document Number Olan
Rev SA
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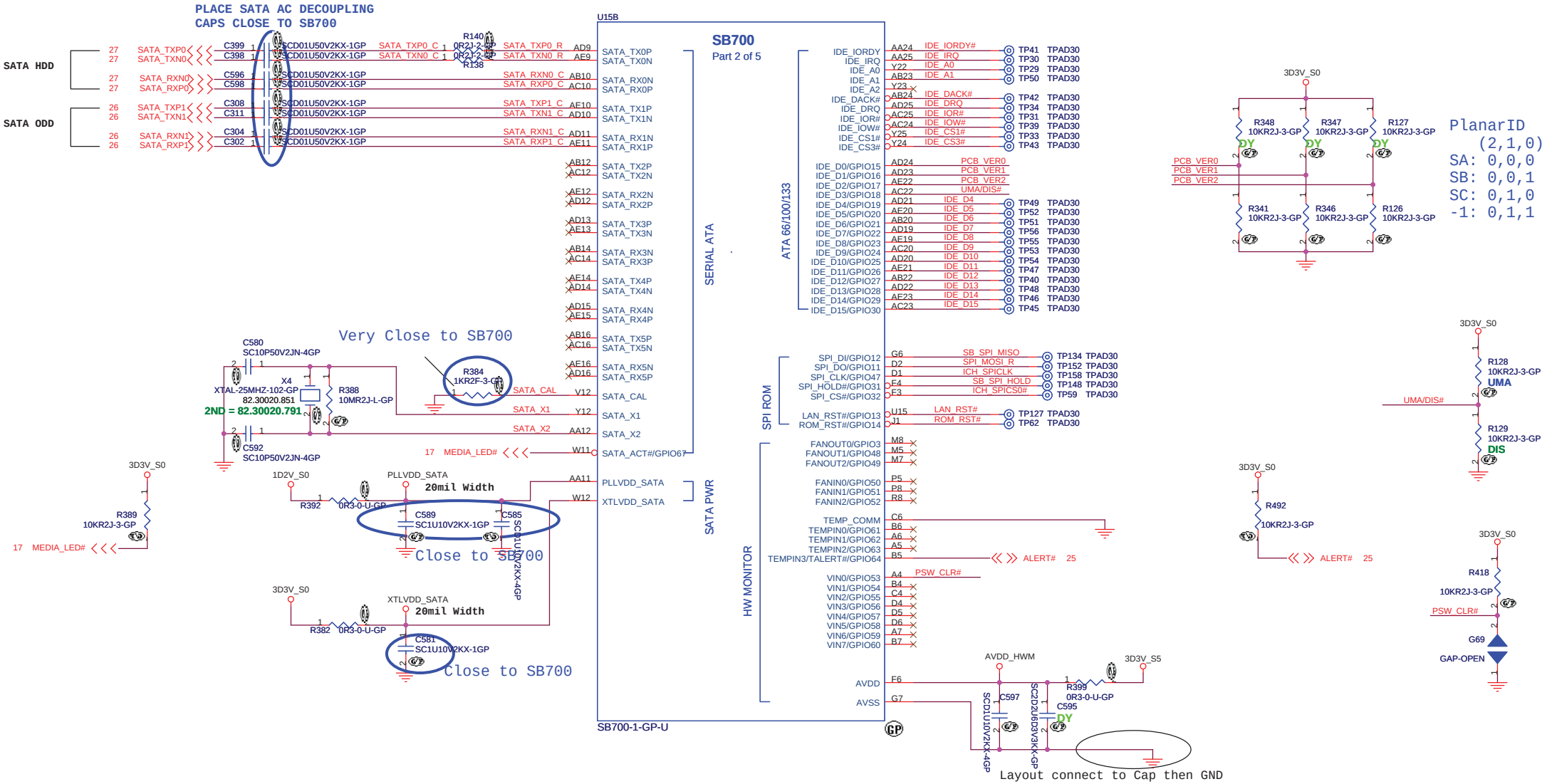

DIS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***ATi-SB700_SATA-IDE_(3/5)***
Size: A3	Document Number: Olan
Rev: SA	
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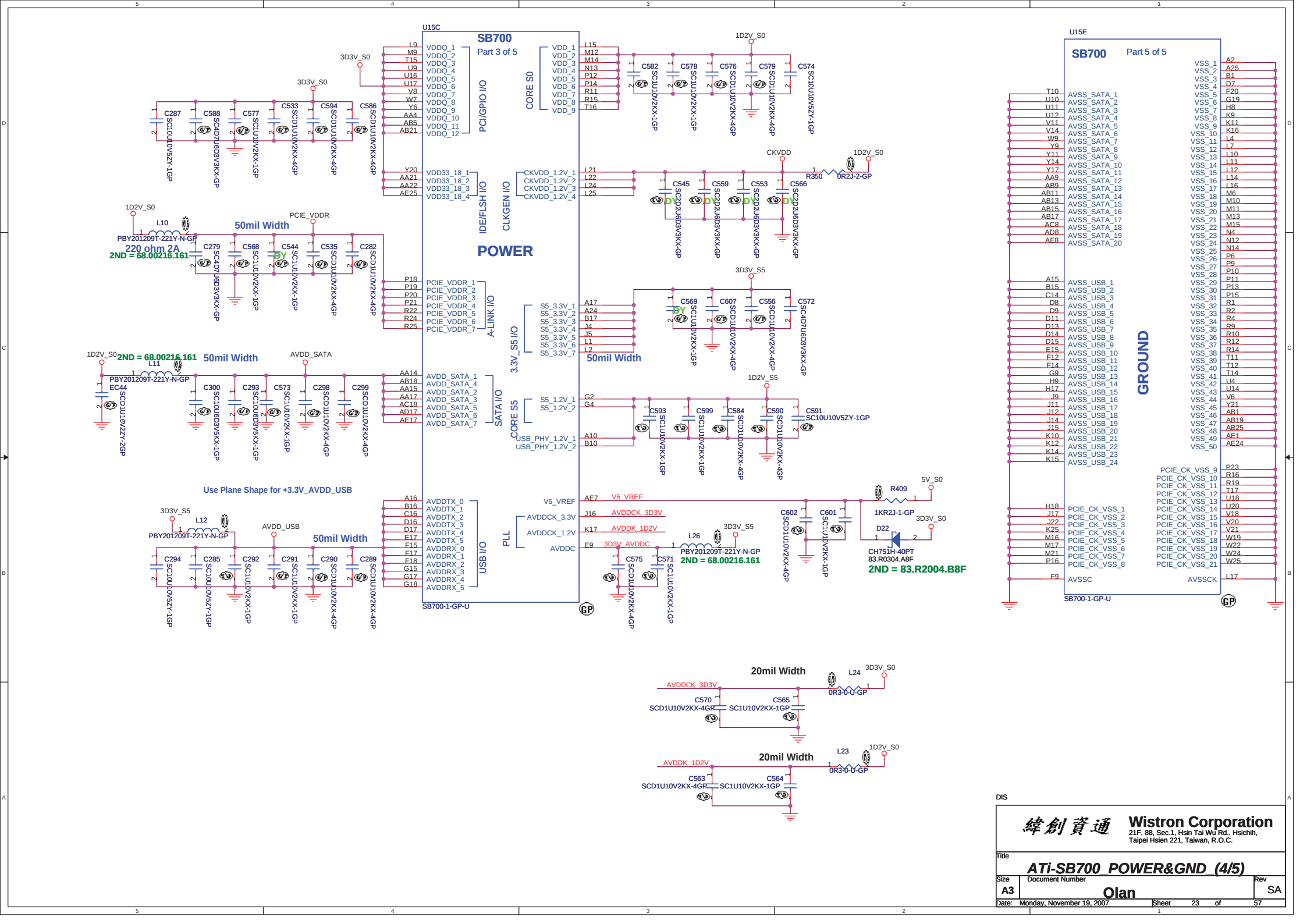
U15C
SB700
Part 3 of 5
POWER
PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
CORE S5
USB I/O
PLL
SB700-1-GP-U
U15E
SB700
Part 5 of 5
GROUND
SB700-1-GP-U
50mil Width
220 ohm 2A
2ND = 68.00216.161
Use Plane Shape for +3.3V_AVDD_USB
20mil Width
2ND = 83.R2004.B8F
DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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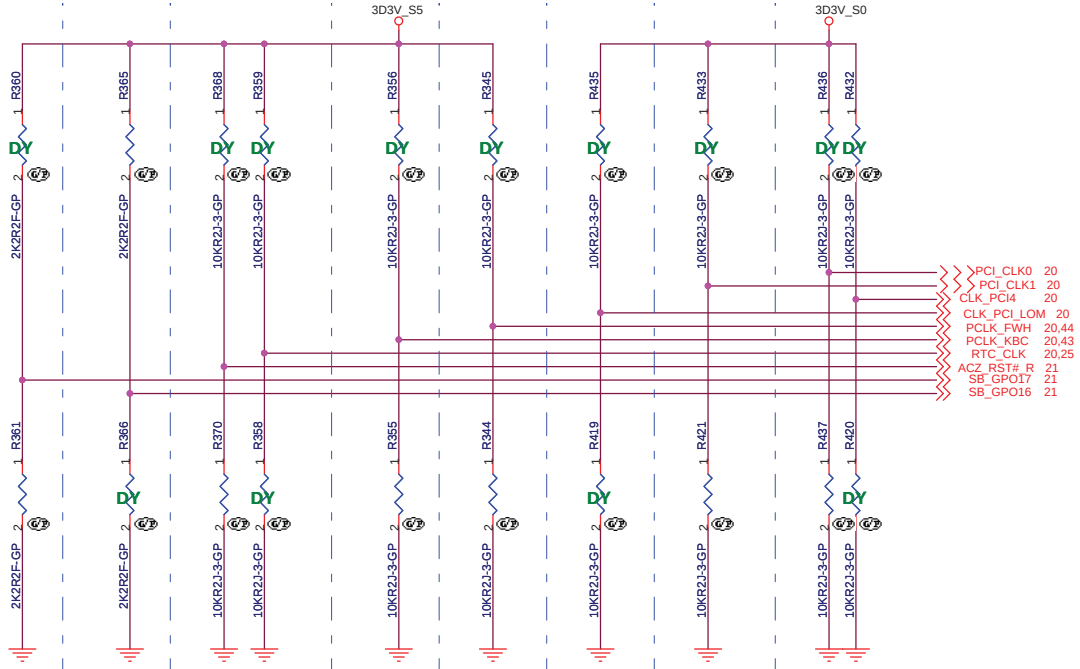
REQUIRED STRAPS

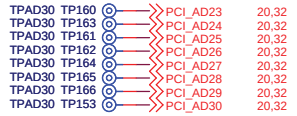
REQUIRED SYSTEM STRAPS



	PCI_CLK0	PCI_CLK1	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

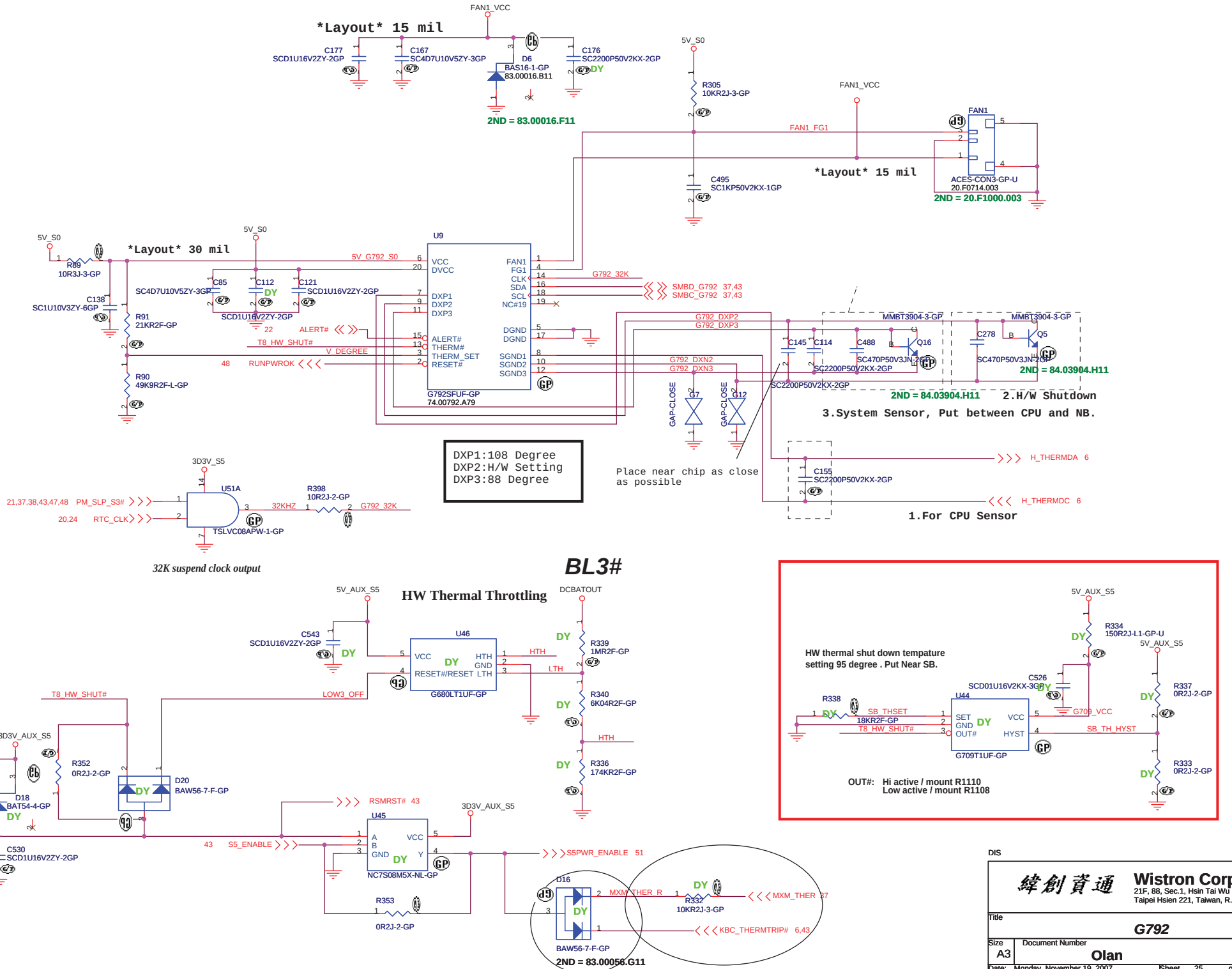
DIS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: Olan | Rev: SA

Date: Monday, November 19, 2007 | Sheet 24 of 57



DIS

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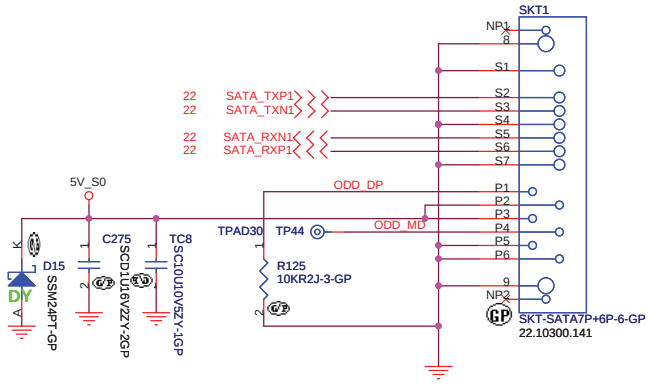
Taipei Hsien 221, Taiwan, R.O.C.

Title			
	G792		
Size	Document Number		Rev
A3	Olan		SA
Date: Monday, November 19, 2007	Sheet 25	of	57

ODD Connector



DIS

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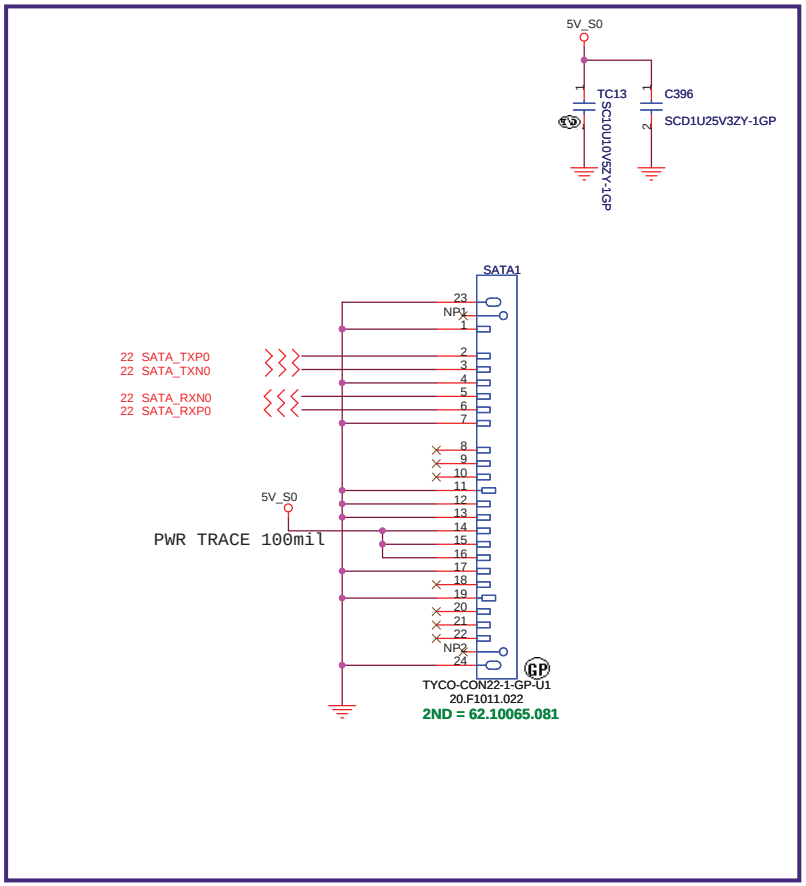
Taipei Hsien 221, Taiwan, R.O.C.

Title: CDROM

Size | Document Number: Olan | Rev: SA

Date: Monday, November 19, 2007 | Sheet 26 of 57

SATA HDD Connector



DIS

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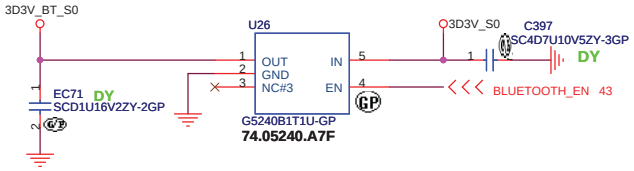
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD

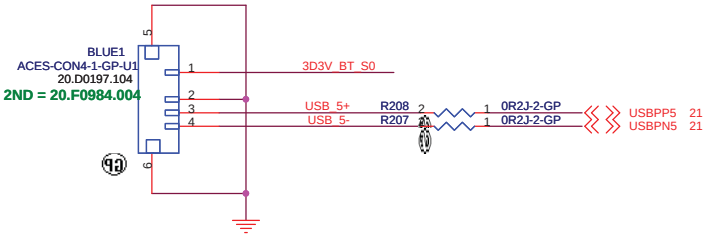
Size | Document Number: Olan | Rev: SA

Date: Monday, November 19, 2007 Sheet 27 of 57

BLUETOOTH MODULE



EC40 put near BLUE1 / all USB put one choke near connector by EMI request



DIS

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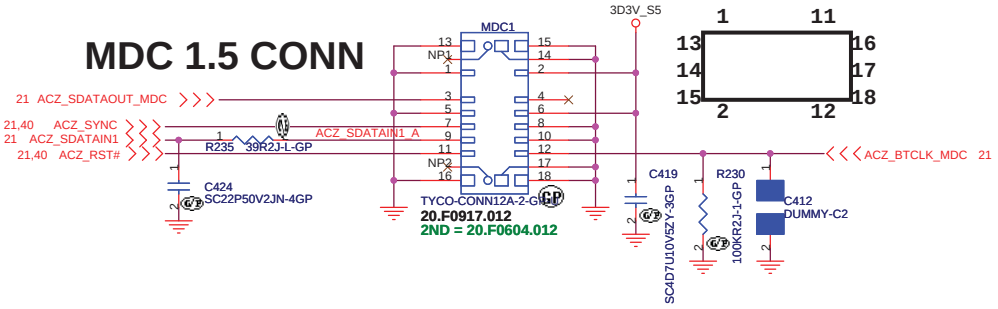
Title: ***BLUETOOTH***

Size | Document Number: **Olan** | Rev: SA

Date: Monday, November 19, 2007 | Sheet 28 of 57

MDC 1.5 CONN



DIS

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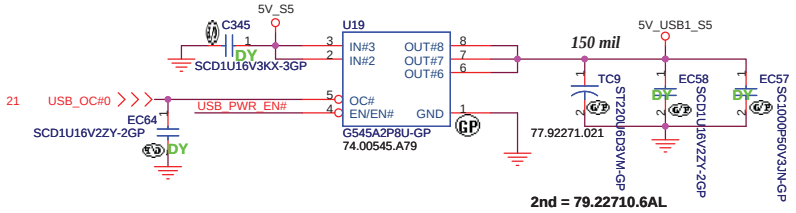
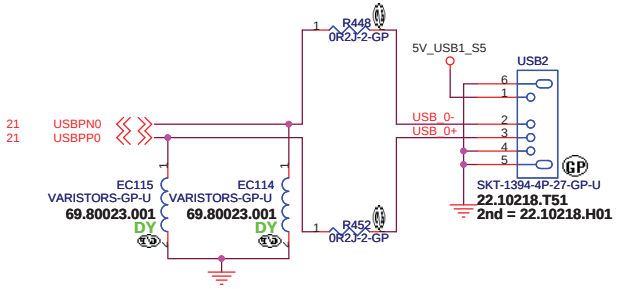
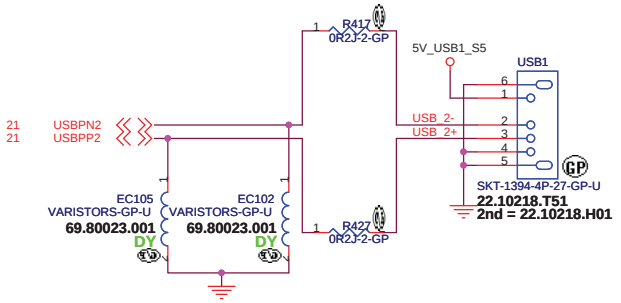
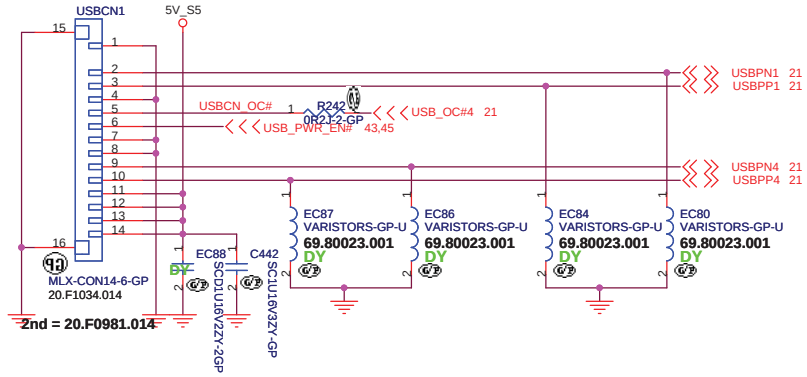
Taipei Hsien 221, Taiwan, R.O.C.

Title		
MDC		
Size	Document Number	Rev
	Olan	SA
Date: Monday, November 19, 2007	Sheet 29 of 57	









DIS

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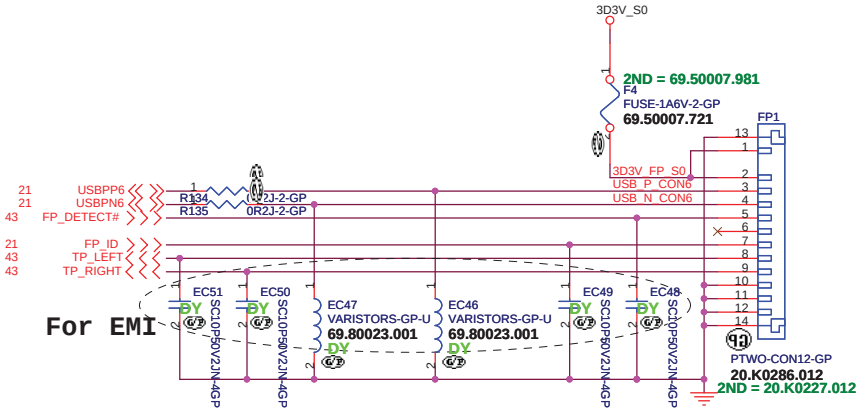
Taipei Hsien 221, Taiwan, R.O.C.

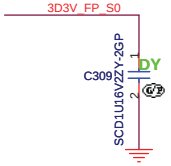
Title: **USB**

Size	Document Number	Rev
	Olan	SA

Date: Monday, November 19, 2007 Sheet 30 of 57

Finger printer





For EMI

DIS

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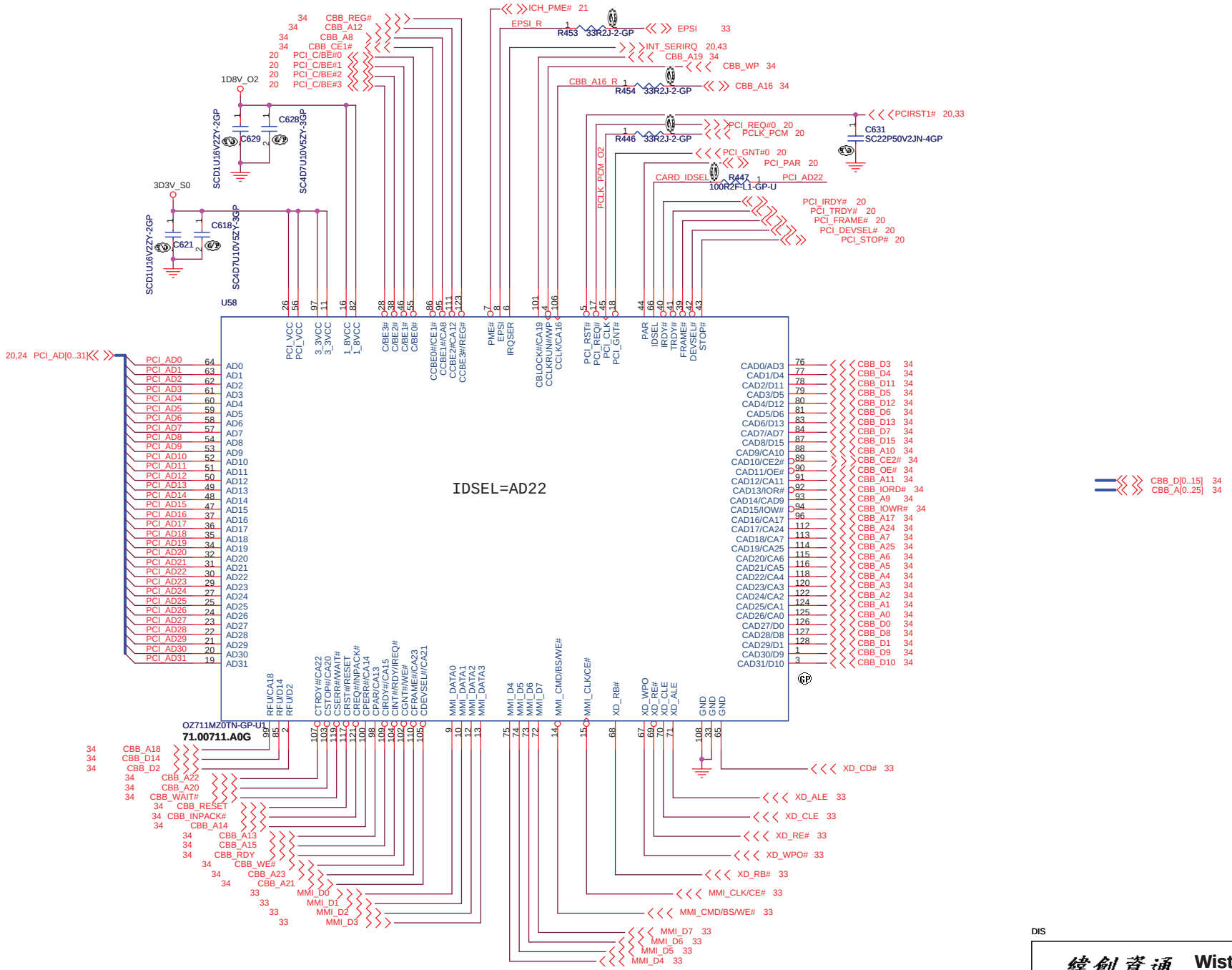
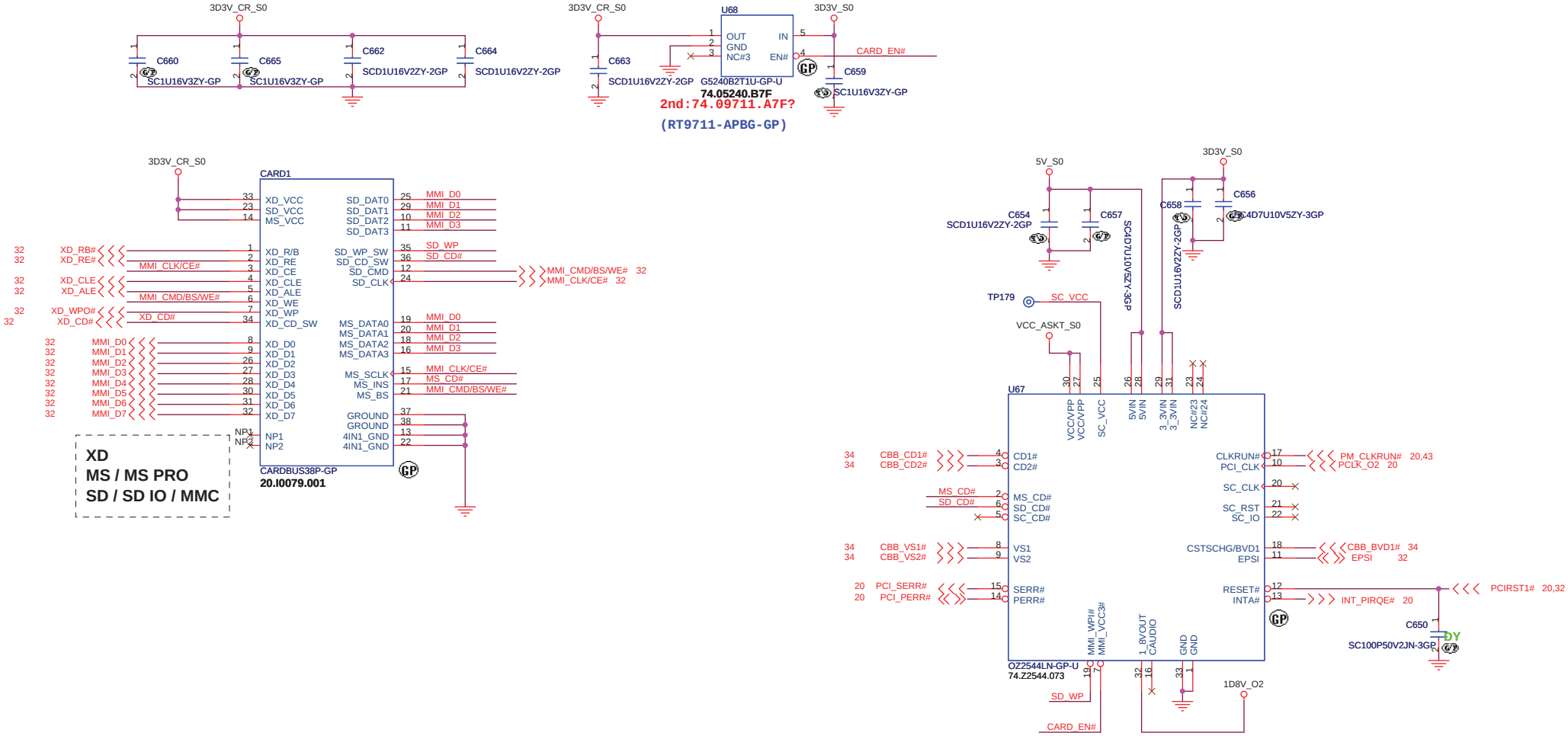
Title: *Finger Printer*		
Size	Document Number: Olan	Rev: SA
Date: Monday, November 19, 2007	Sheet 31 of 57	



DIS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*OZ711MZ0*	
Size: A3	Document Number: Olan	Rev: SA
Date: Monday, November 19, 2007	Sheet 32 of 57	



DIS

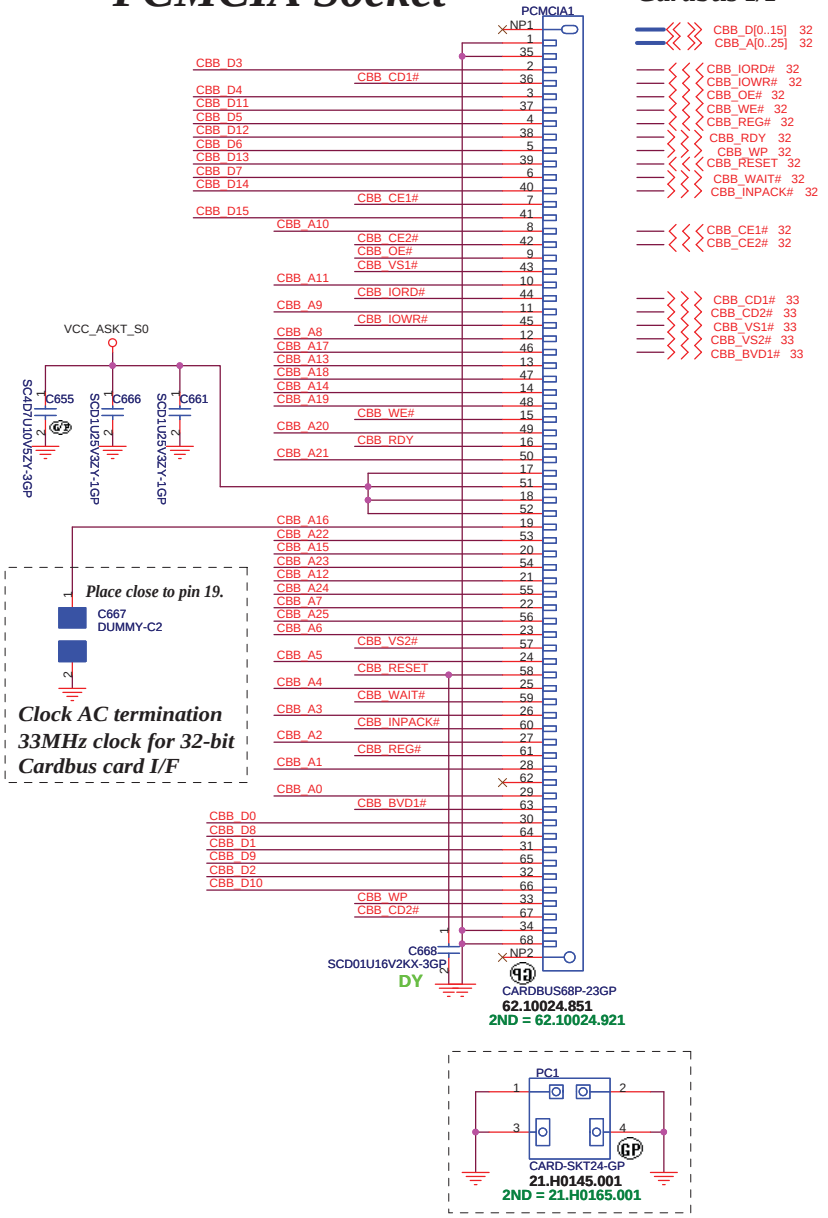
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Card Reader Connector*

Size	Document Number	Rev
A3	Olan	SA

Date: Monday, November 19, 2007 Sheet 33 of 57

PCMCIA Socket



Cardbus I/F

CBB_D[0..15] 32
CBB_A[0..25] 32
CBB_IORD# 32
CBB_IOWR# 32
CBB_OE# 32
CBB_WE# 32
CBB_REG# 32
CBB_RDY 32
CBB_WP 32
CBB_RESET 32
CBB_WAIT# 32
CBB_INPACK# 32
CBB_CE1# 32
CBB_CE2# 32
CBB_CD1# 33
CBB_CD2# 33
CBB_VS1# 33
CBB_VS2# 33
CBB_BVD1# 33

DIS

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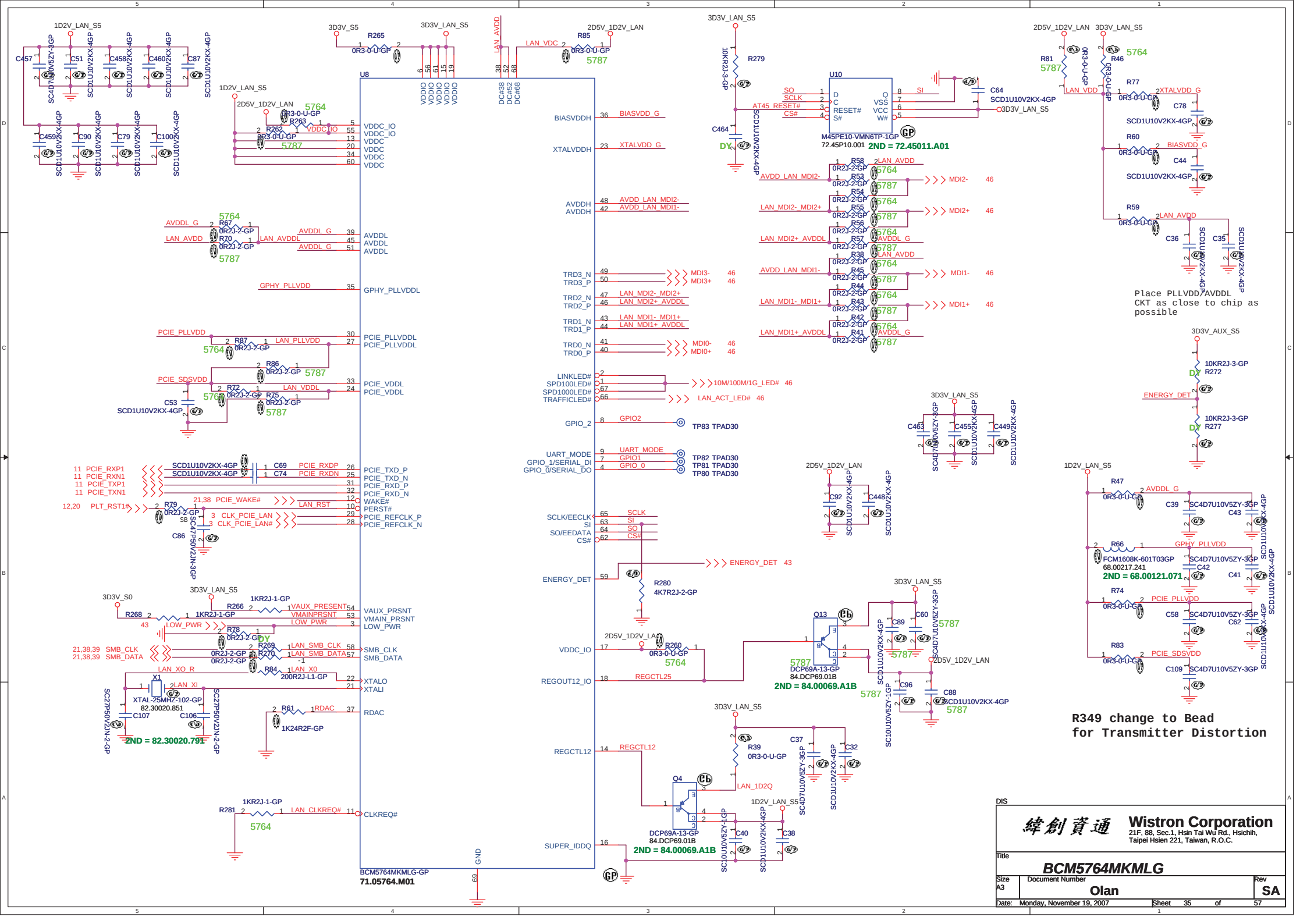
Title		
PCMCIA		
Size: A3	Document Number: Olan	Rev: SA
Date: Monday, November 19, 2007	Sheet 34 of 57	


U8
BCM5764MKMLG-GP
71.05764.M01
U10
M45PE10-VMN6TP-1GP
72.45P10.001
2ND = 72.45011.A01
Q13
DCP69A-13-GP
84.DCP69.01B
2ND = 84.00069.A1B
Q4
DCP69A-13-GP
84.DCP69.01B
2ND = 84.00069.A1B
XTAL-25MHZ-102-GP
82.30020.851
2ND = 82.30020.791
FCM1608K-601T03GP
68.00217.241
2ND = 68.00121.071
Place PLLVDD/AVDDL CKT as close to chip as possible
R349 change to Bead for Transmitter Distortion
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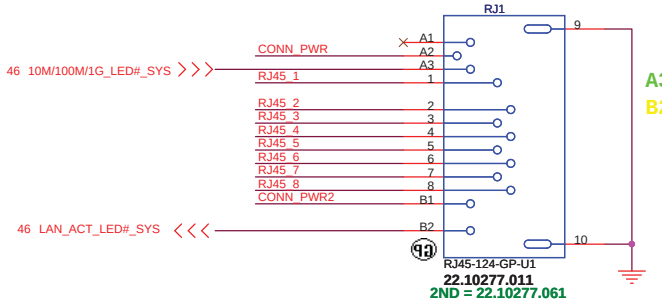
Title
BCM5764MKMLG
Size A3
Document Number
Olan
Rev SA
Date: Monday, November 19, 2007
Sheet 35 of 57

LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

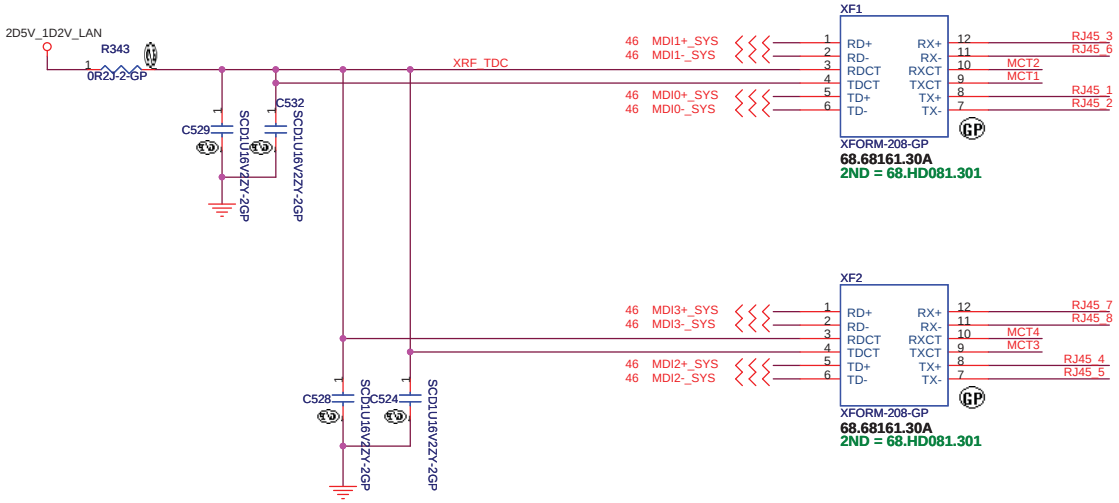


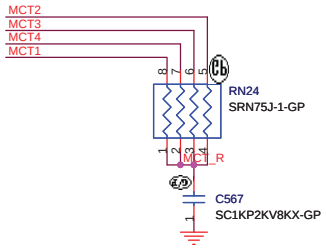
A3:GREEN
B2:Orange

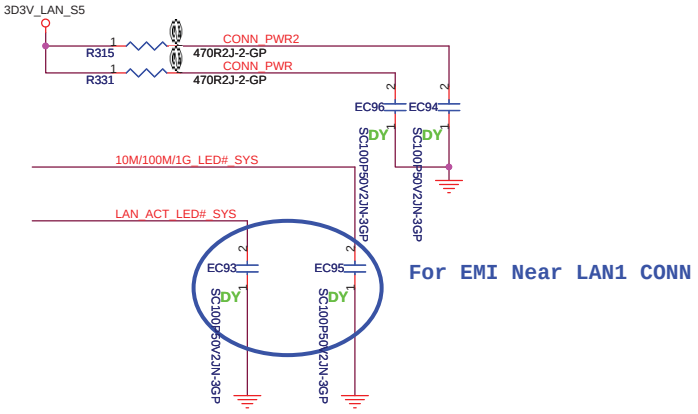
LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

GIGA Lan Transformer







For EMI Near LAN1 CONN

DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

Size	Document Number	Rev
A3	Olan	SA

Date: Monday, November 19, 2007 Sheet 36 of 57

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

? CHECK ATI NEED?

MXM1
SPD-CONN230A-4-GP-U1

20.F1031.230

DCBATOUT_MXM

DCBATOUT DCBATOUT_MXM
G24 GAP-OPEN-PWR
G22 GAP-OPEN-PWR
G23 GAP-OPEN-PWR
G25 GAP-OPEN-PWR

DIS

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Title: Graphic MXM CONN

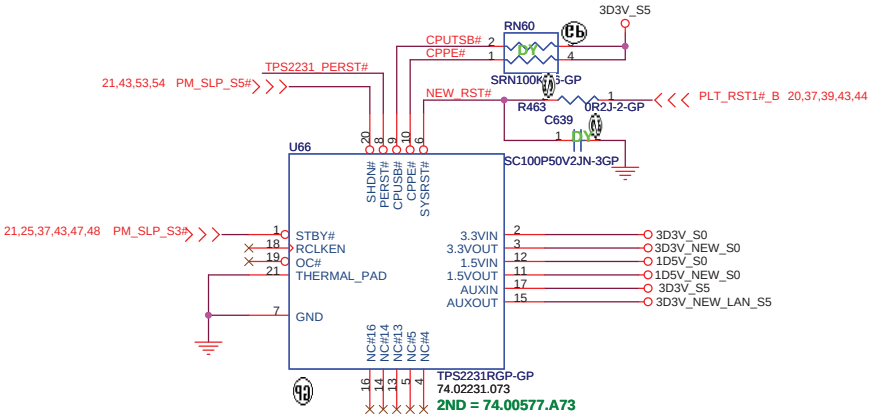
Size: A3 | Document Number: Olan | Rev: SA

Date: Monday, November 19, 2007 | Sheet 37 of 57

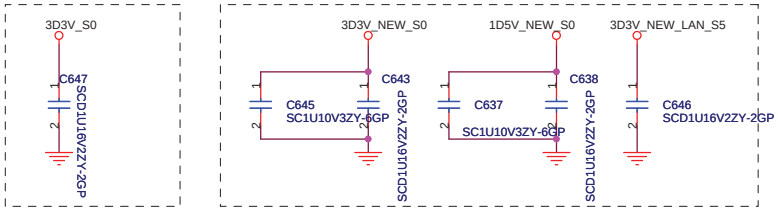
NEWCARD Connector

Reserve the symbol
for bottom side
connector

TOP VIEW



Place them Near to ChipPlace them Near to Connector



DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: NEW CARD

Size	Document Number	Rev
A3	Olan	SA

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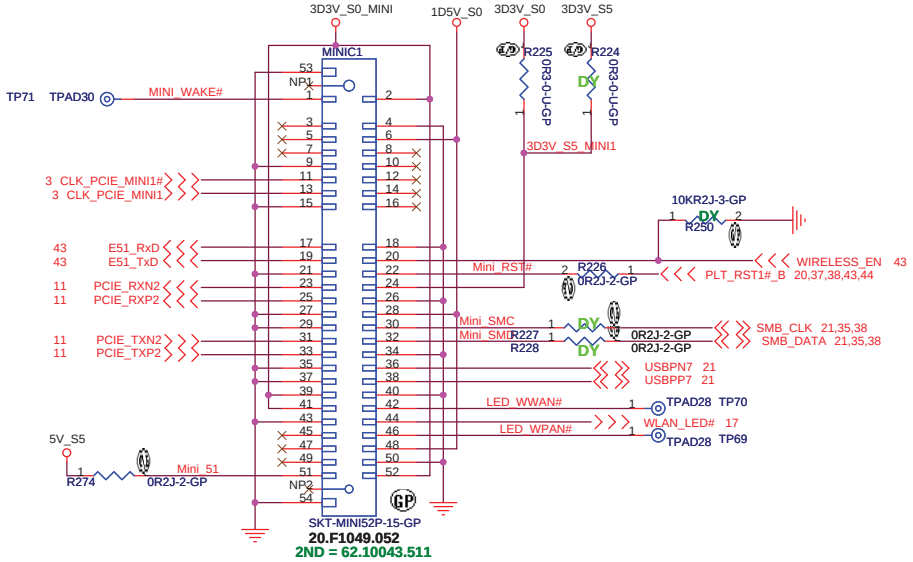
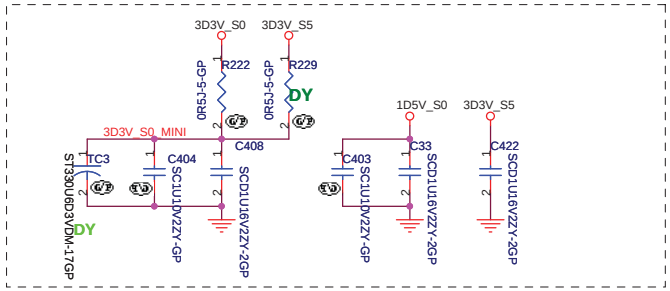
Mini Card Connector(WLAN)



Place near MINIC1



DIS

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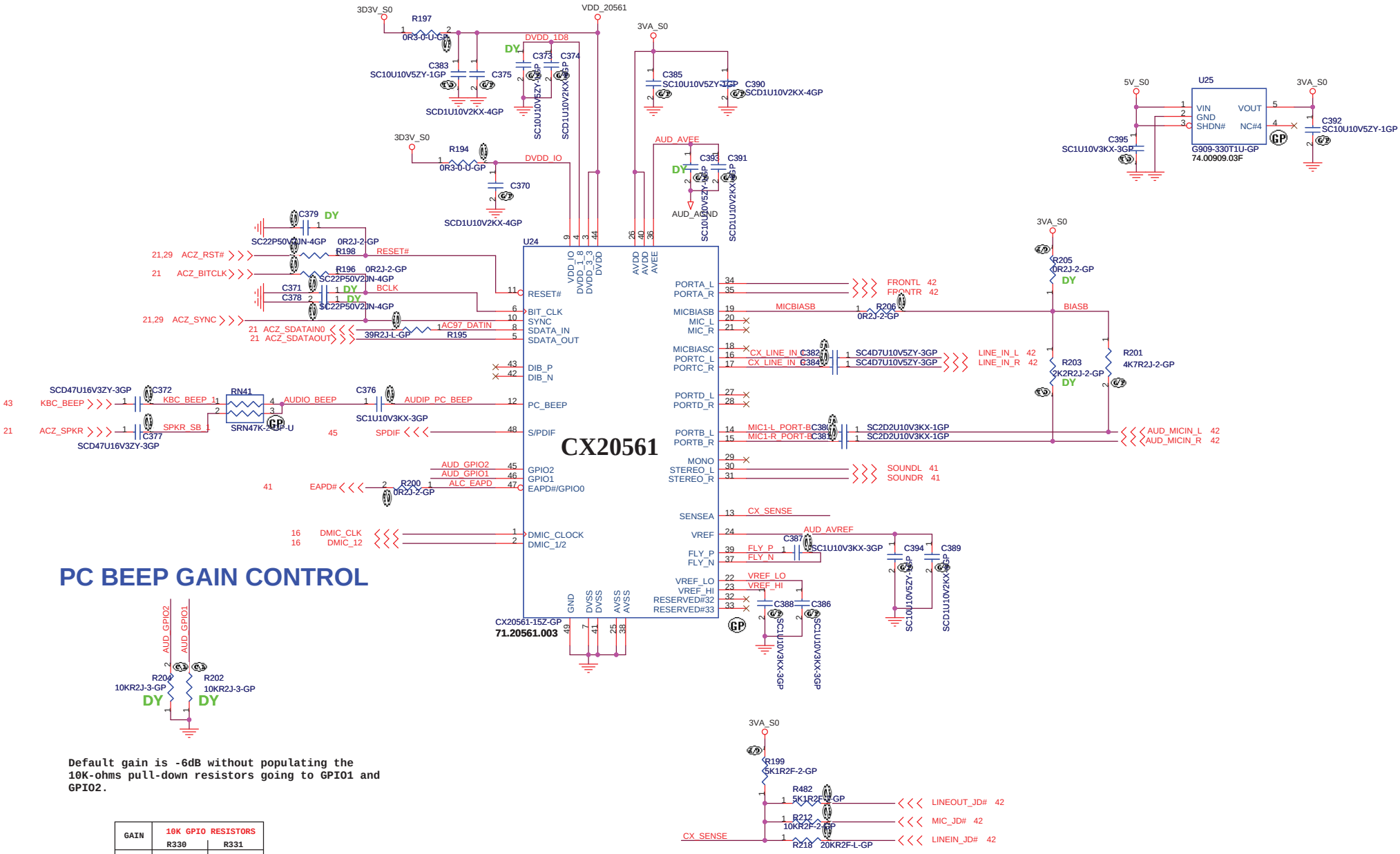
Title: Mini Card		
Size: A3	Document Number: Olan	Rev: SA
Date: Monday, November 19, 2007	Sheet 39 of 57	



PC BEEP GAIN CONTROL

Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.

GAIN	10K GPIO RESISTORS	
	R330	R331
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-18dB	Omit	Populate

DIS

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Title: Azalia codec CX20561

Size: A3 | Document Number: Olan | Rev: SA

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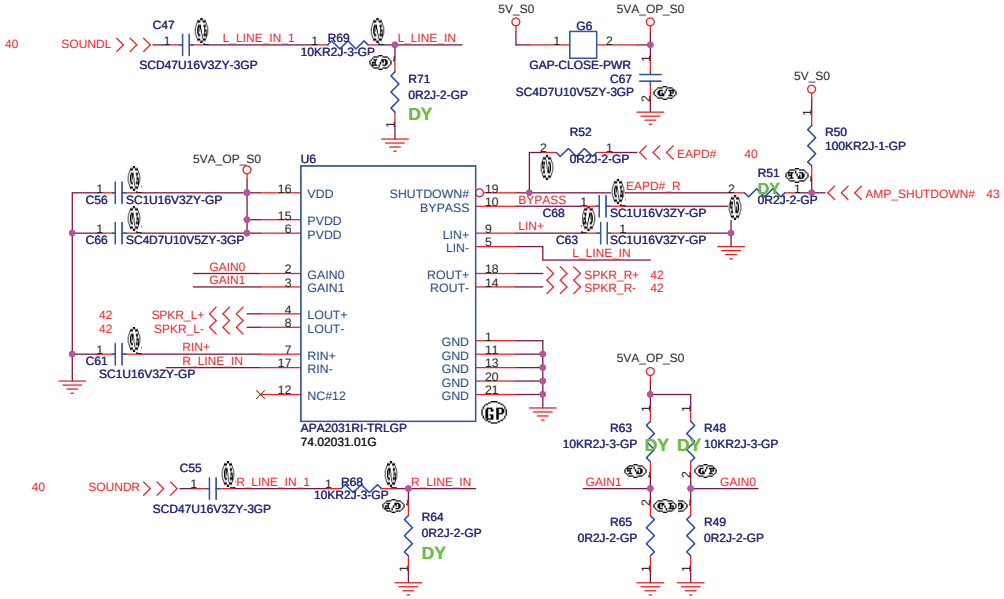
AUDIO OP AMPLIFIER



DIS

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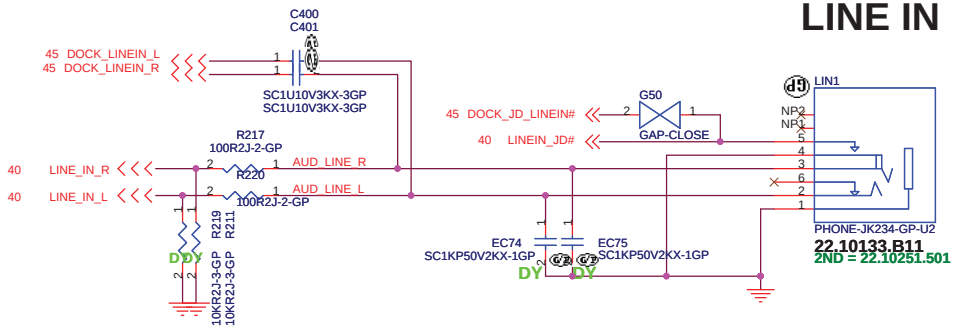
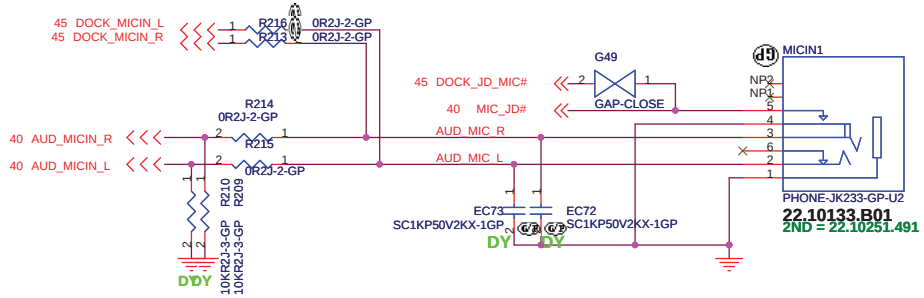
Title	AUDIO AMP	
Size	Document Number: Olan	Rev: SA
Date: Monday, November 19, 2007	Sheet 41 of 57	

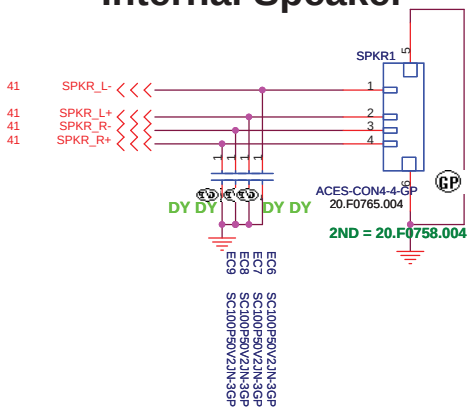
LINE IN



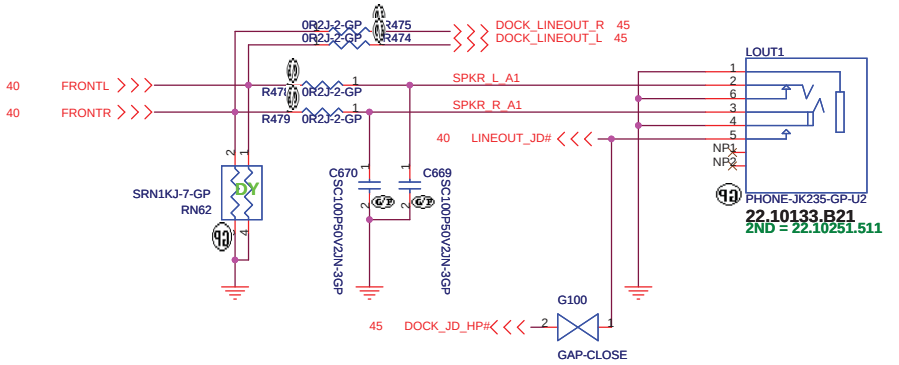
MIC IN



Internal Speaker



LINE OUT



DIS

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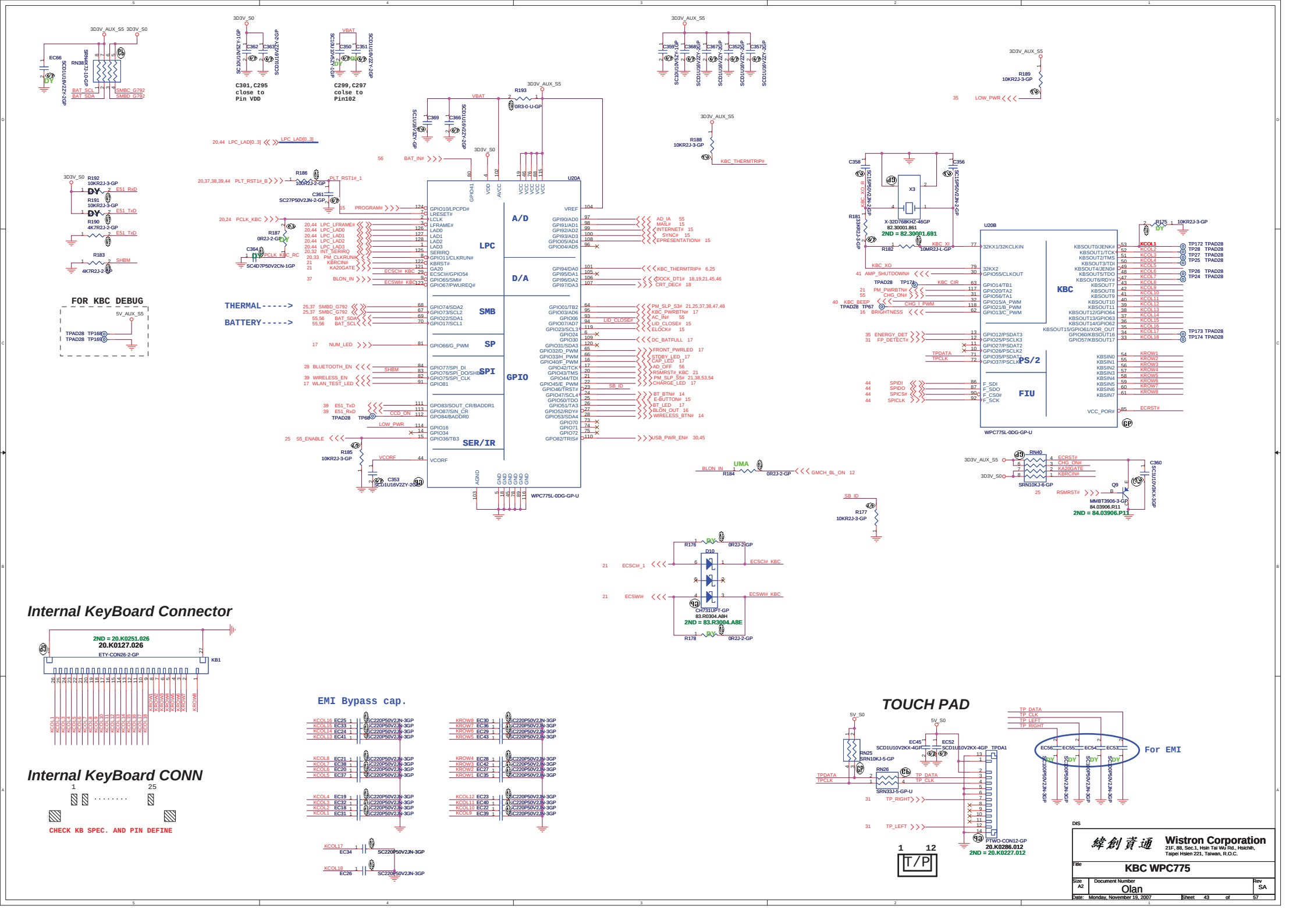
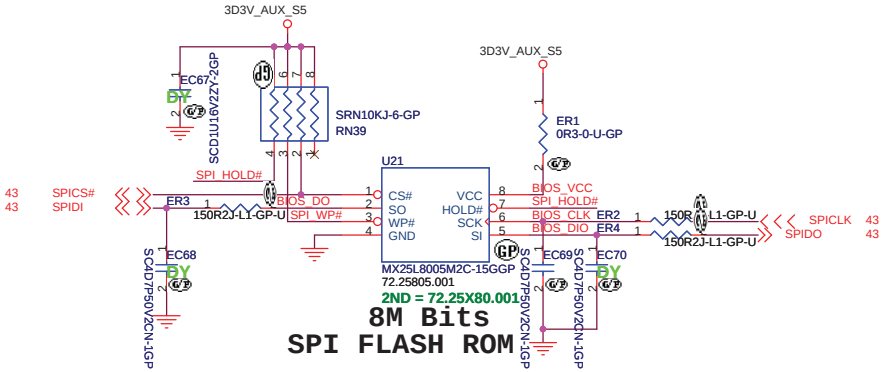
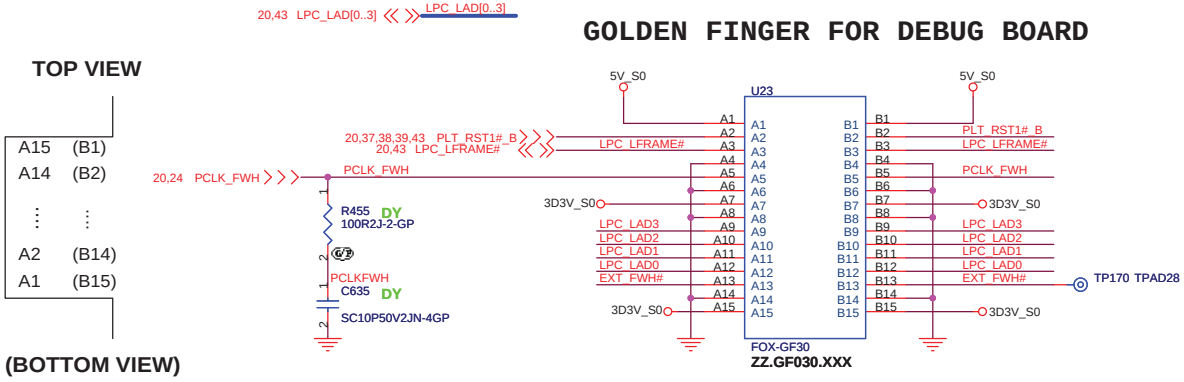
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO JACK	
Size	Document Number: Olan	Rev: SA
Date: Monday, November 19, 2007	Sheet 42 of 57	


C301,C295
close to
Pin VDD
C299,C297
colse to
Pin102
FOR KBC DEBUG
THERMAL----->
BATTERY----->
U20A
LPC
SMB
SP
SPI
SER/IR
GPIO
A/D
D/A
WPC775L-0DG-GP-U
U20B
KBC
PS/2
FIU
WPC775L-0DG-GP-U
Internal KeyBoard Connector
2ND = 20.K0251.026
20.K0127.026
ETY-CON26-2-GP
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
EMI Bypass cap.
TOUCH PAD
For EMI
PTWO-CON12-GP
20.K0286.012
2ND = 20.K0227.012
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775
Olan
Monday, November 19, 2007





DIS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BIOS***

Size	Document Number	Rev
A3	Olan	SA

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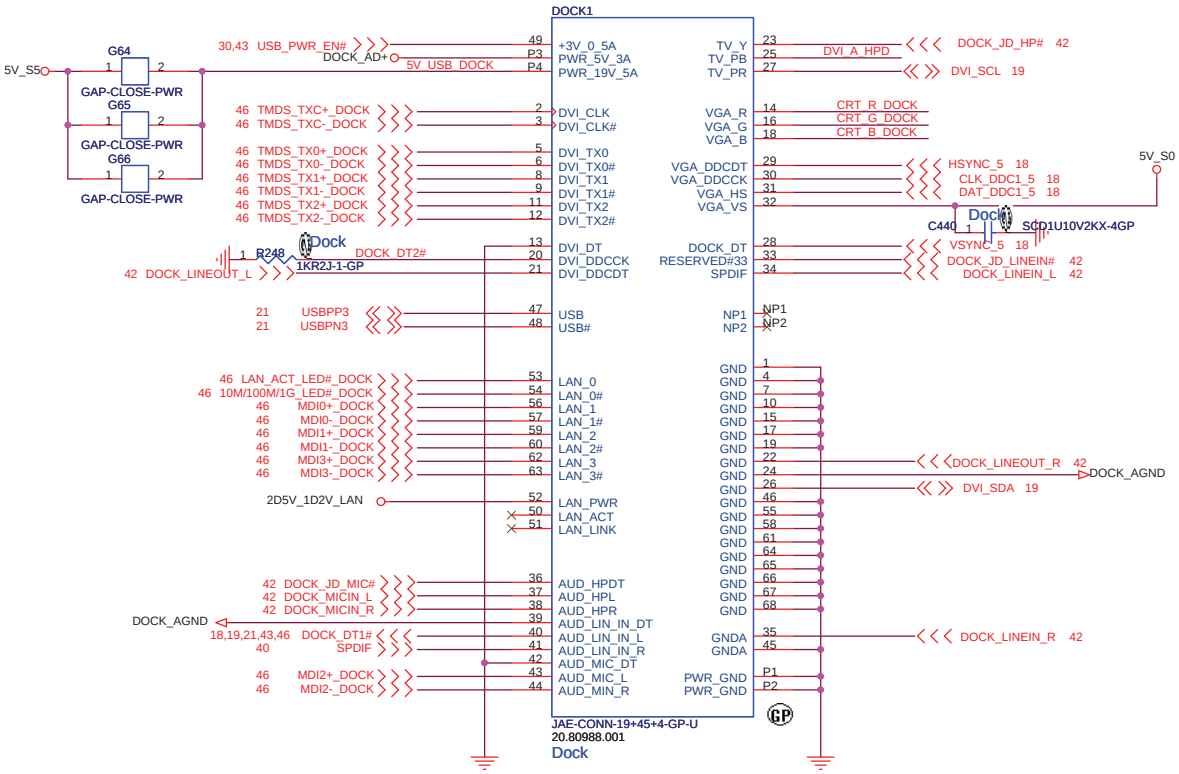
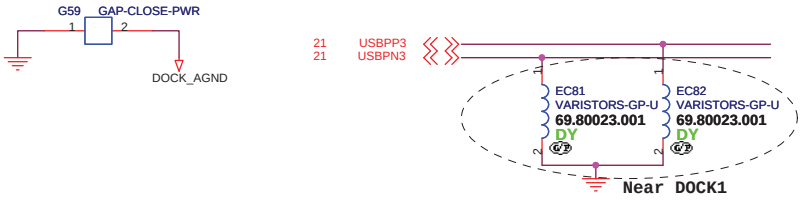
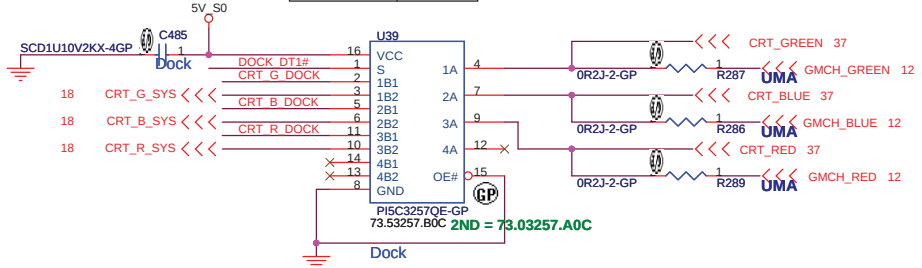
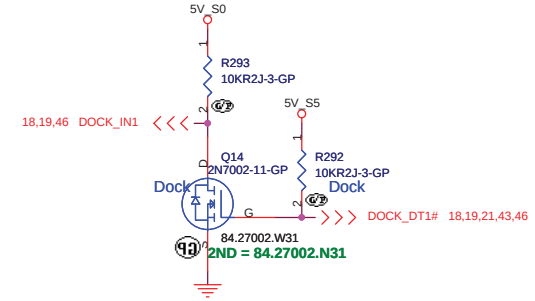
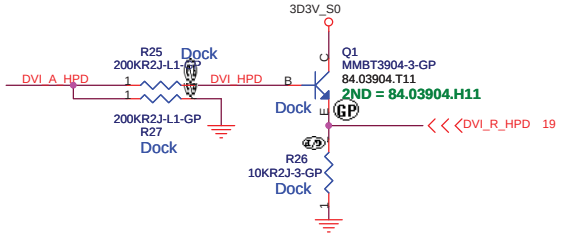


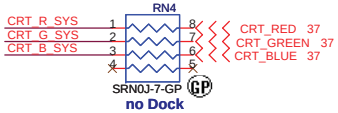


Function	CRT
SYSTEM	H
DOCK	L









DIS

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **EASY PORT4**

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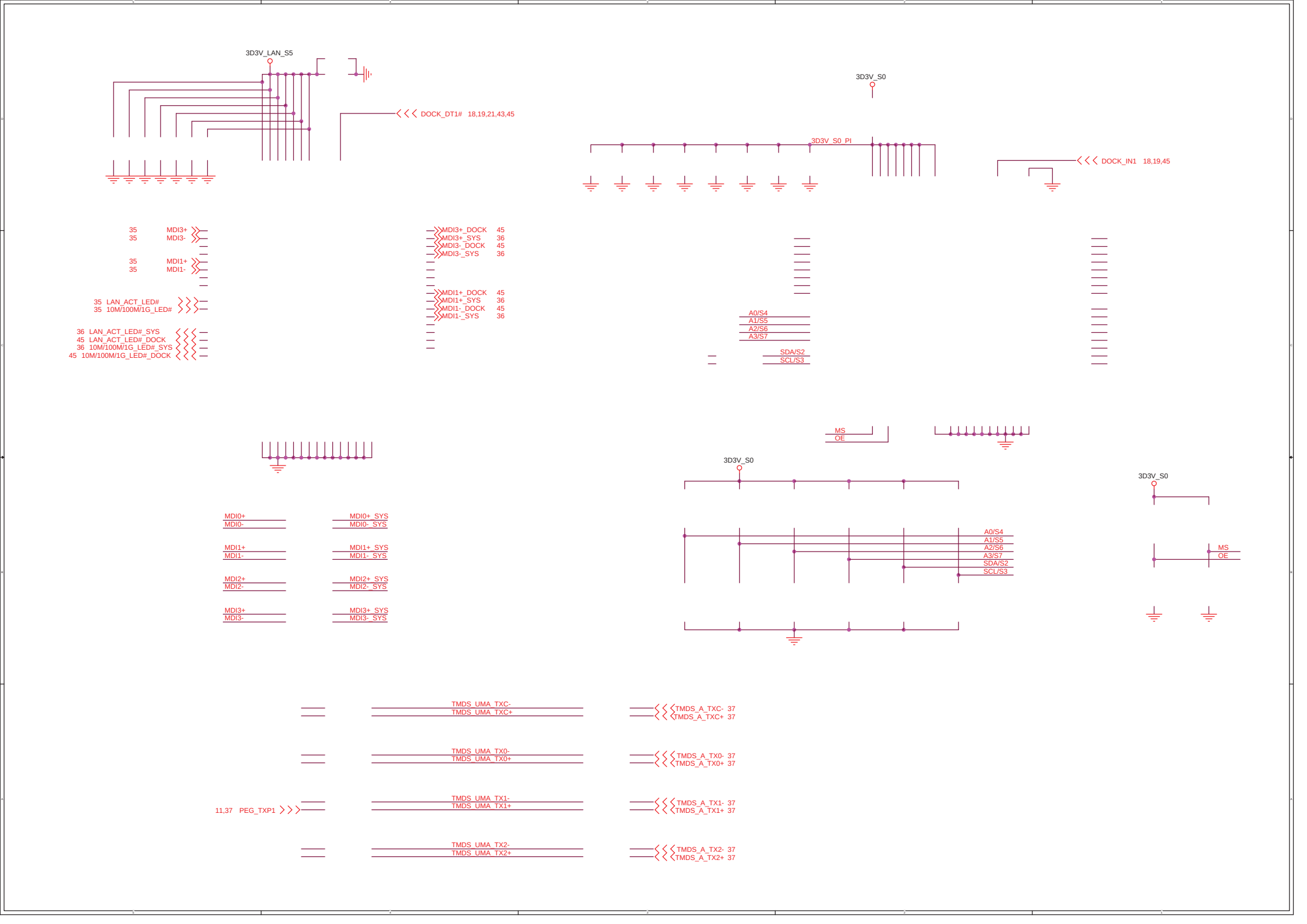
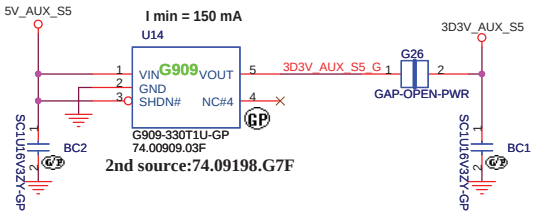
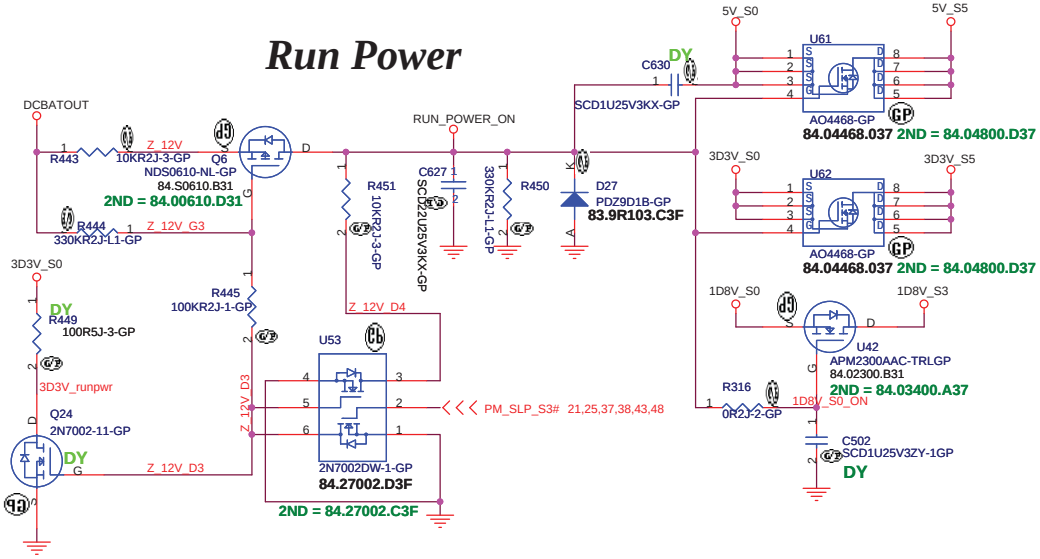

3D3V_LAN_S5
DOCK_DT1# 18,19,21,43,45
3D3V_S0
3D3V_S0_PI
DOCK_IN1 18,19,45
35 MDI3+
35 MDI3-
35 MDI1+
35 MDI1-
35 LAN_ACT_LED#
35 10M/100M/1G_LED#
36 LAN_ACT_LED#_SYS
45 LAN_ACT_LED#_DOCK
36 10M/100M/1G_LED#_SYS
45 10M/100M/1G_LED#_DOCK
MDI3+_DOCK 45
MDI3+_SYS 36
MDI3-_DOCK 45
MDI3-_SYS 36
MDI1+_DOCK 45
MDI1+_SYS 36
MDI1-_DOCK 45
MDI1-_SYS 36
A0/S4
A1/S5
A2/S6
A3/S7
SDA/S2
SCL/S3
MS
OE
3D3V_S0
3D3V_S0
MDI0+
MDI0-
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
MDI0+_SYS
MDI0-_SYS
MDI1+_SYS
MDI1-_SYS
MDI2+_SYS
MDI2-_SYS
MDI3+_SYS
MDI3-_SYS
A0/S4
A1/S5
A2/S6
A3/S7
SDA/S2
SCL/S3
MS
OE
TMDS_UMA_TXC-
TMDS_UMA_TXC+
TMDS_A_TXC- 37
TMDS_A_TXC+ 37
TMDS_UMA_TX0-
TMDS_UMA_TX0+
TMDS_A_TX0- 37
TMDS_A_TX0+ 37
11,37 PEG_TXP1
TMDS_UMA_TX1-
TMDS_UMA_TX1+
TMDS_A_TX1- 37
TMDS_A_TX1+ 37
TMDS_UMA_TX2-
TMDS_UMA_TX2+
TMDS_A_TX2- 37
TMDS_A_TX2+ 37

Aux Power 3D3V_AUX_S5



Run Power



DIS

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Title: RUN POWER and 3D3V_AUX_S5		
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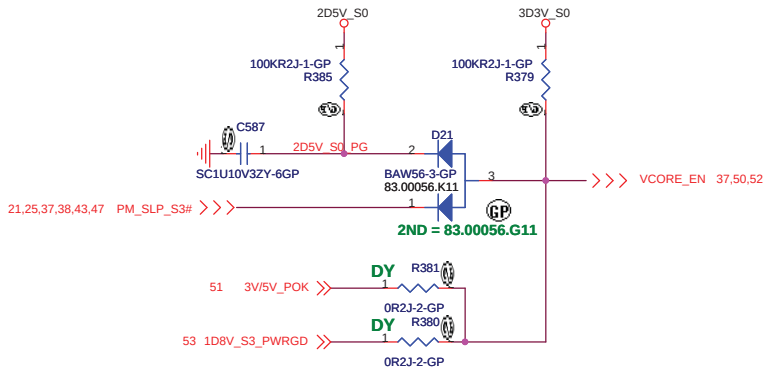
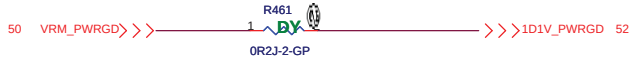
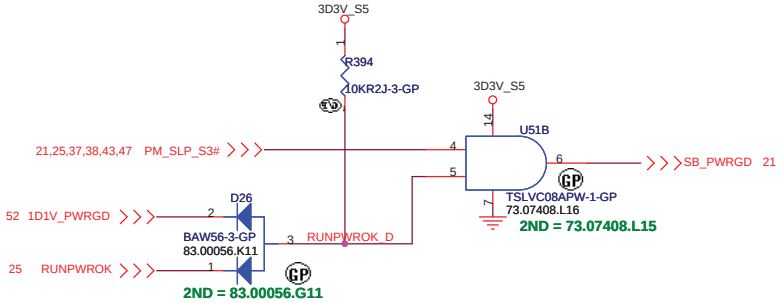


P/H @ 1D8V_S3 PAGE





DIS

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Title: ***POWER ON LOGIC***

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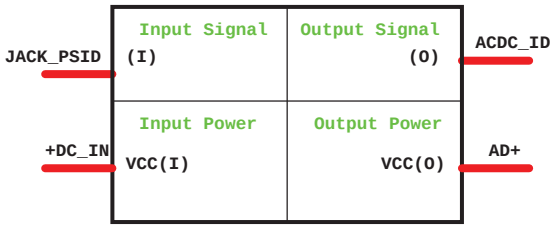
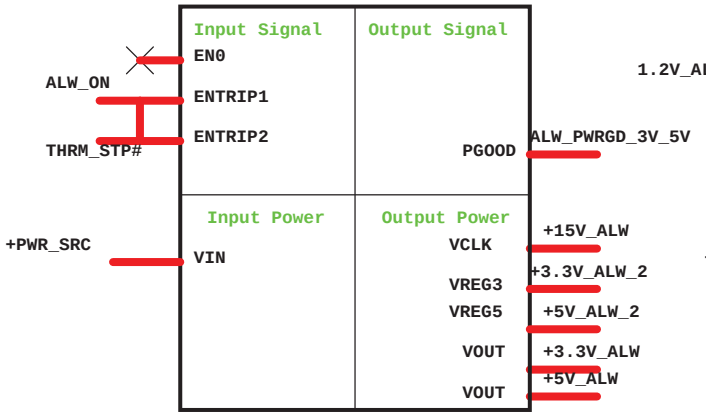
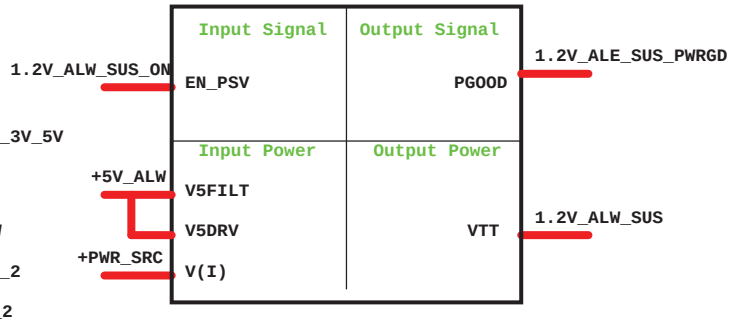
Adapter



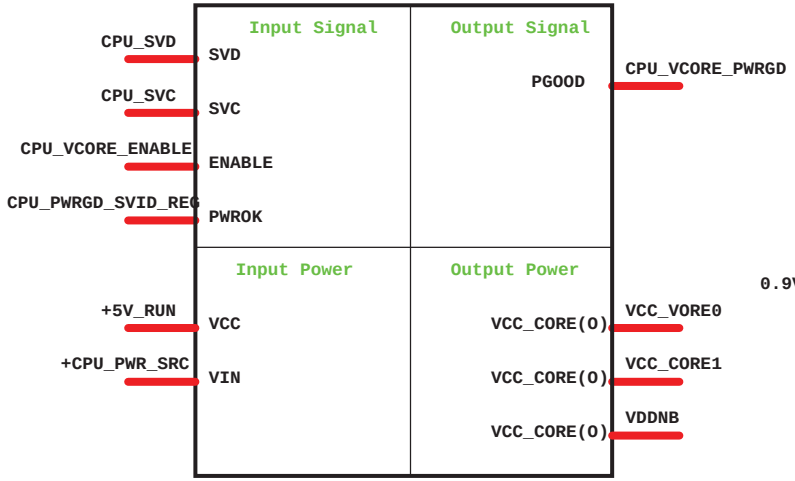
SN0608098



DCDC 1D2V(TPS5117)

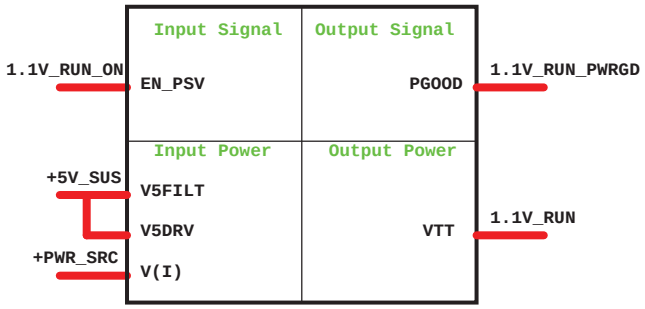


CPU_CORE
ISL6265HRTZ

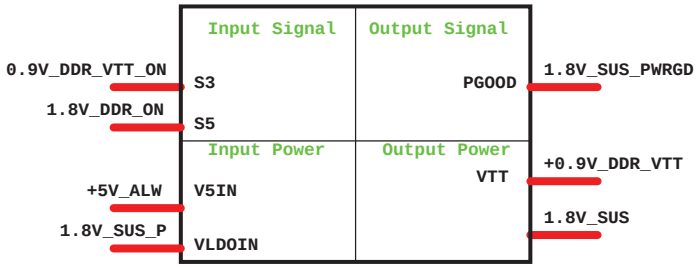


	S3	S5	VDDQ	VTTREF	VTT
S0 S3	1	1	1	1	1
S4 S5	0	0	0	0	0

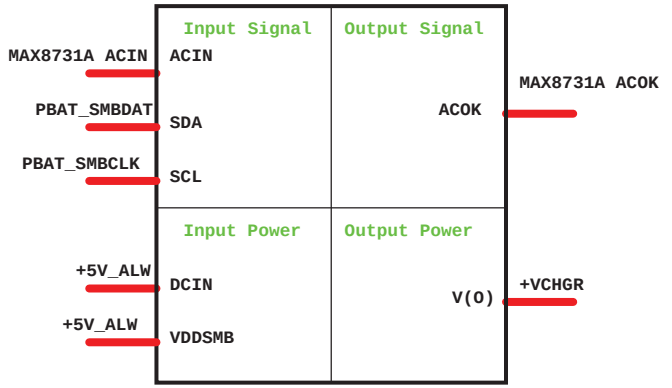
1D1V(TPS5117)



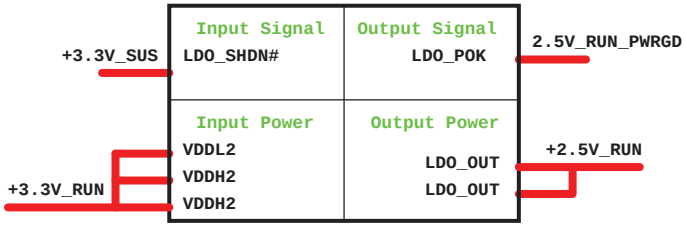
1D8V/0D9V(TPS5116)



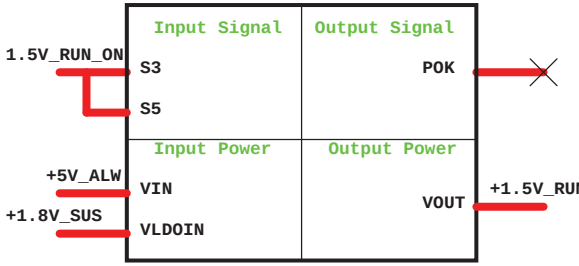
CHARGER BQ24745



2.5V LDO
EMC4002



1.5V_LDO



DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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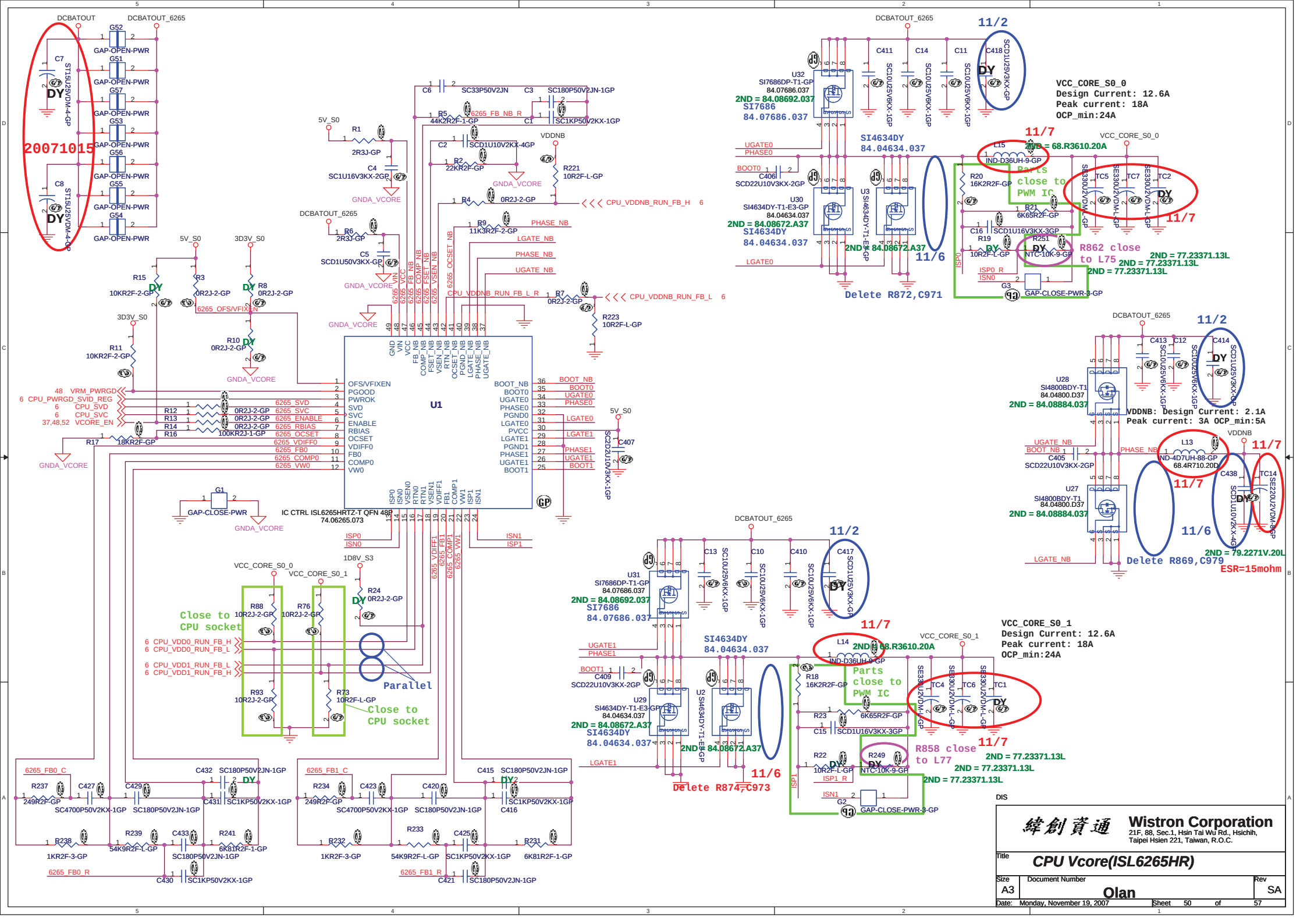
20071015
U1
IC CTRL ISL6265HRTZ-T QFN 48P
74.06265.073
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
SI7686DP-T1-GP
84.07686.037
2ND = 84.08692.037
SI7686
84.07686.037
SI4634DY
84.04634.037
SI4634DY-T1-E3-GP
84.04634.037
2ND = 84.08672.A37
SI4634DY
84.04634.037
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
IND-D36UH-9-GP
2ND = 68.R3610.20A
IND-4D7UH-88-GP
68.4R710.20D
2ND = 79.2271V.20L
ESR=15mohm
Parts close to PWM IC
R862 close to L75
R858 close to L77
2ND = 77.23371.13L
Delete R872,C971
Delete R869,C979
Delete R874,C973
Close to CPU socket
Parallel
11/2
11/7
11/6
DCBATOUT
DCBATOUT_6265
5V_S0
3D3V_S0
1D8V_S3
VDDNB
GNDA_VCORE
CPU_VDDNB_RUN_FB_H 6
CPU_VDDNB_RUN_FB_L 6
CPU_VDDNB_RUN_FB_L_R
6265_OFS/VFIXEN
6265_SVD
6265_SVC
6265_ENABLE
6265_RBIAS
6265_OCSET
6265_VDIFF0
6265_FB0
6265_COMP0
6265_VW0
6265_FB0_C
6265_FB0_R
6265_FB1_C
6265_FB1_R
PHASE_NB
LGATE_NB
UGATE_NB
BOOT_NB
ISP0
ISN0
ISP1
ISN1
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
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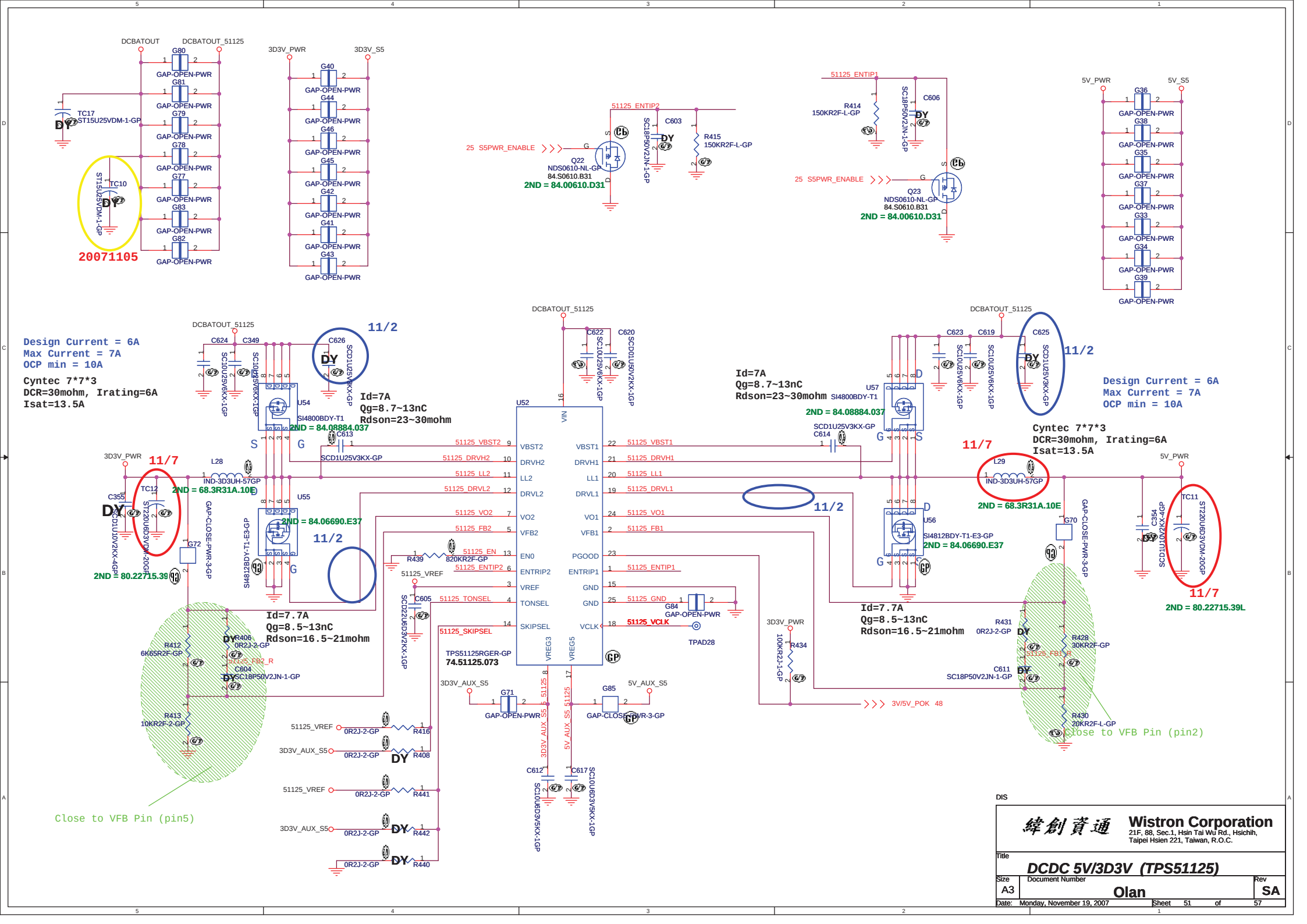
DCBATOUT
DCBATOUT_51125
TC17
ST15U25VDM-1-GP
TC10
20071105
3D3V_PWR
3D3V_S5
GAP-OPEN-PWR
51125_ENTIP2
25 S5PWR_ENABLE
Q22
NDS0610-NL-GP
84.S0610.B31
2ND = 84.00610.D31
C603
R415
150KR2F-L-GP
SC18P50V2JN-1-GP
51125_ENTIP1
R414
C606
Q23
5V_PWR
5V_S5
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
11/2
11/7
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
U54
SI4800BDY-T1
2ND = 84.08884.037
U55
SI4812BDY-T1-E3-GP
2ND = 84.06690.E37
U56
U57
L28
L29
IND-3D3UH-57GP
2ND = 68.3R31A.10E
TC12
ST220U6D3VDM-20GP
2ND = 80.22715.39L
TC11
U52
TPS51125RGER-GP
74.51125.073
VIN
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
ENTRIP1
GND
VCLK
VREG3
VREG5
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_GND
51125_VCLK
TPAD28
3V/5V_POK 48
3D3V_AUX_S5
5V_AUX_S5
51125_VREF
R439
820KR2F-GP
R431
0R2J-2-GP
R428
30KR2F-GP
R430
20KR2F-L-GP
R434
100KR2J-1-GP
C611
SC18P50V2JN-1-GP
R406
R412
6K65R2F-GP
R413
10KR2F-2-GP
C604
R416
R408
R441
R442
R440
C612
C617
SCD22U6D3V2KX-1GP
SCD10U6D3V5KX-1GP
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
DIS
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (TPS51125)
Size
A3
Document Number
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Rev
SA
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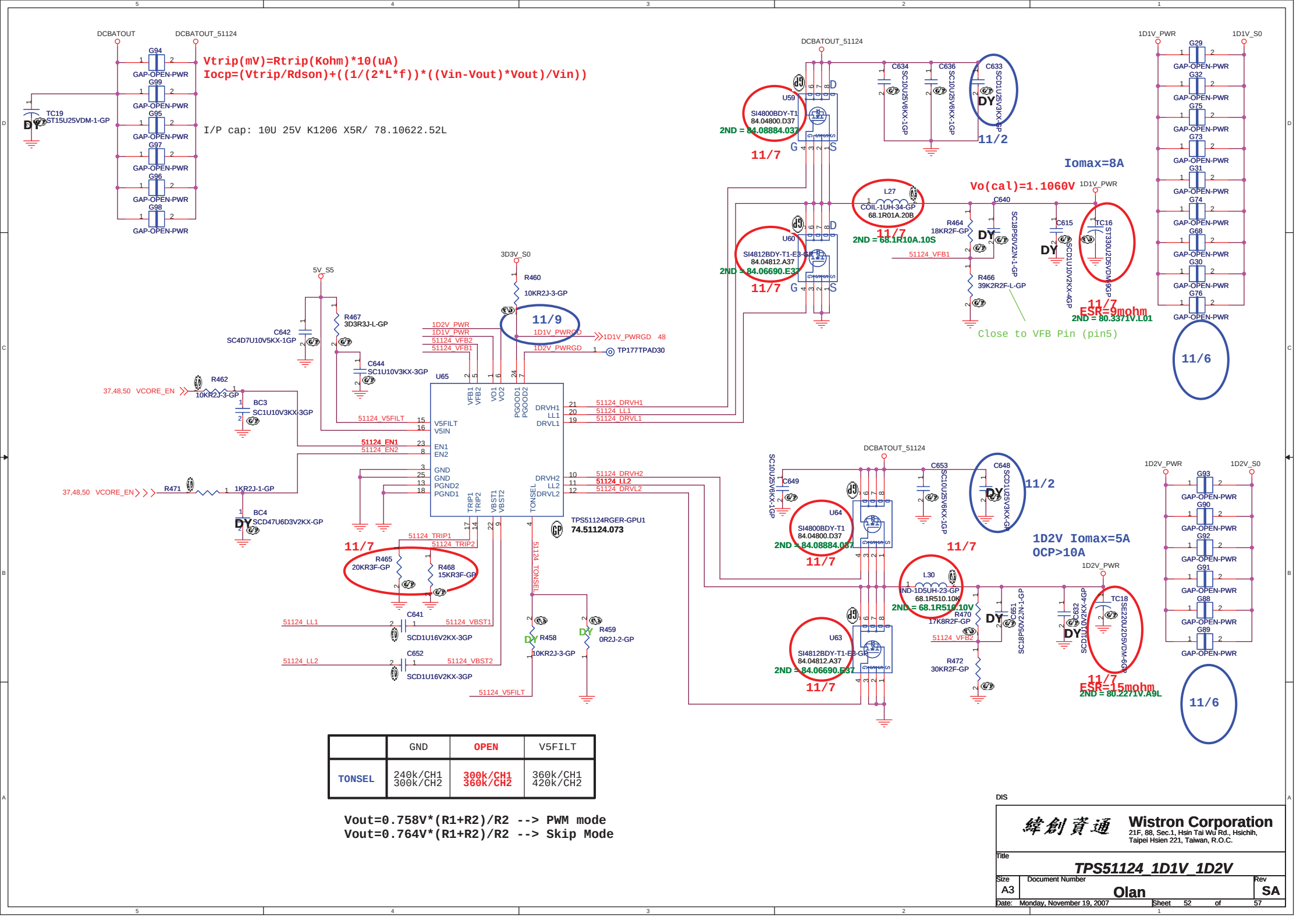
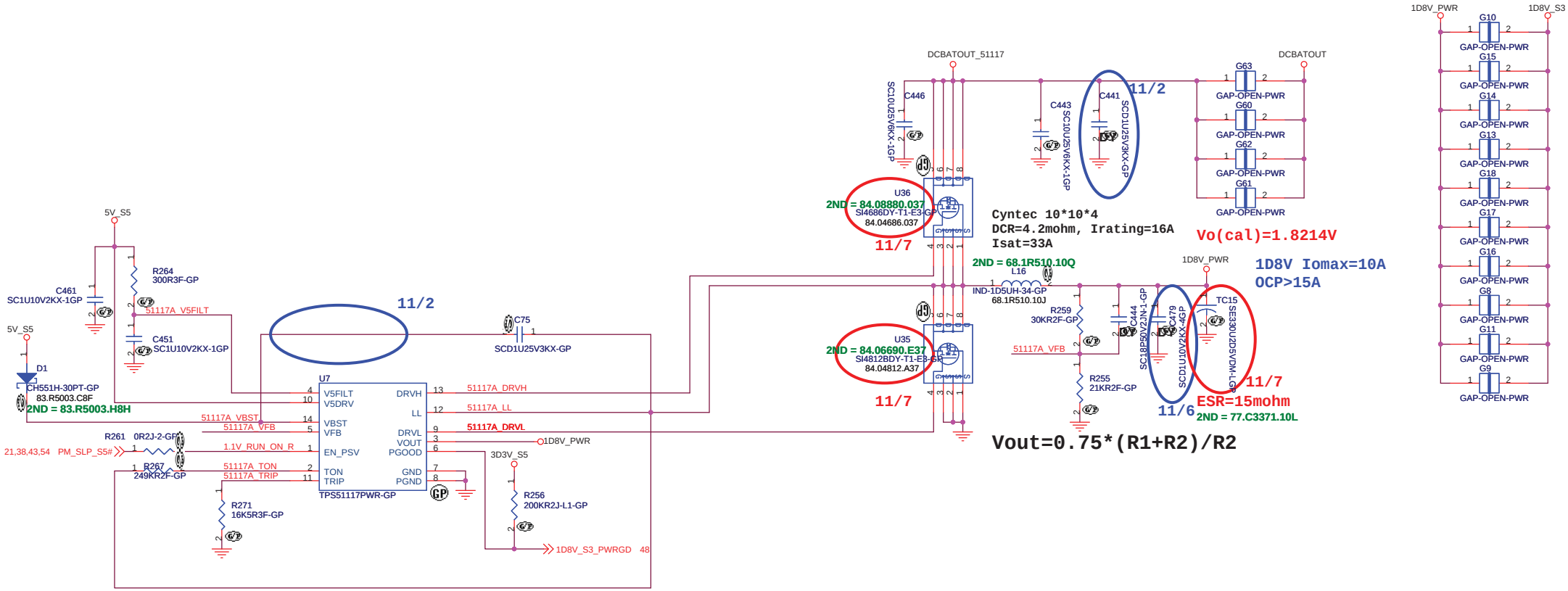


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2



DIS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***1D8V(TPS5117)***	
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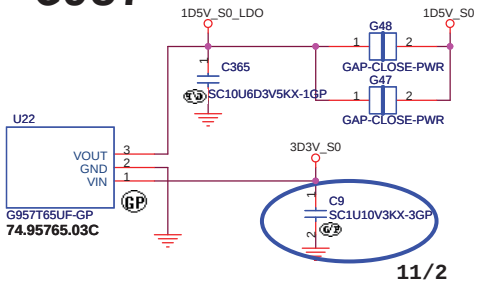
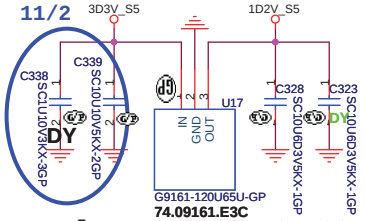
1D5V_S0
Iomax=1A

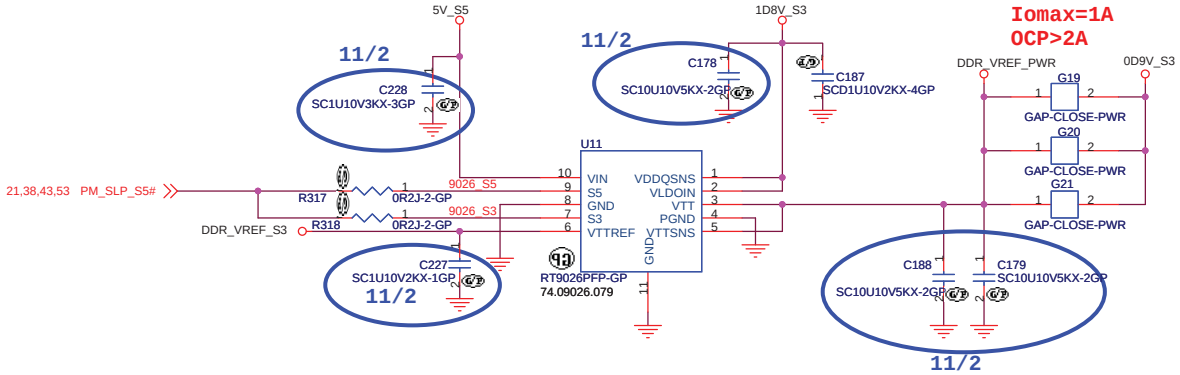
G957



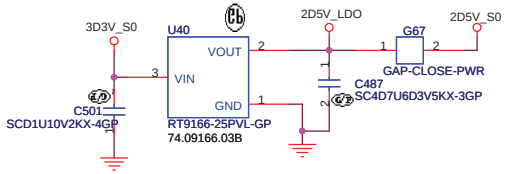
1D2V_S5
Iomax=400mA



Place near to SB700



2D5V_S0
Iomax=0.3A 2D5V/300mA



DIS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *0D9V&2D5V&1D25V&1D5V*

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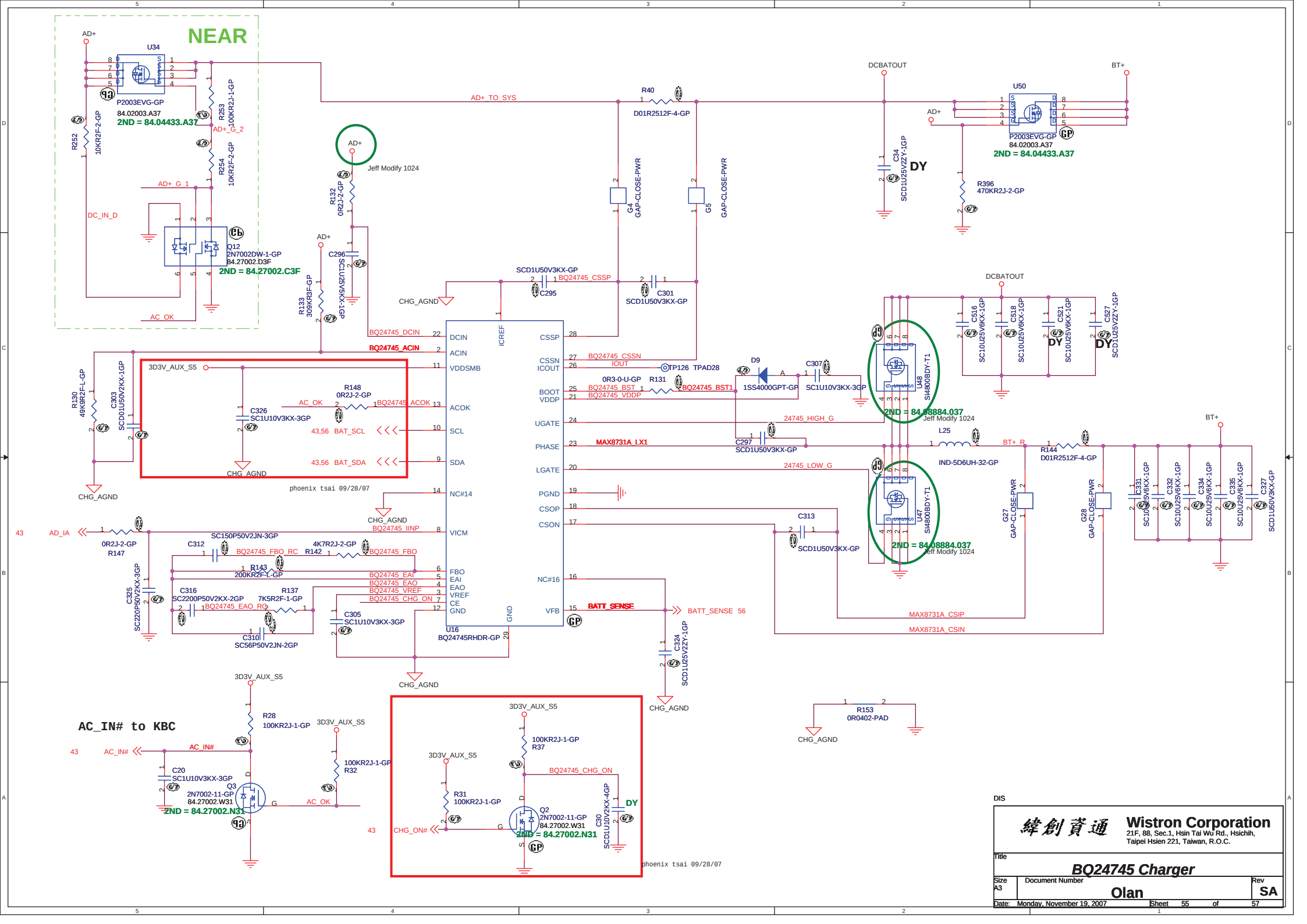
NEAR
AD+
U34
P2003EVG-GP
84.02003.A37
2ND = 84.04433.A37
R253 100KR2J-1-GP
R252 10KR2F-2-GP
R254 10KR2F-2-GP
AD+_G_2
AD+_G_1
DC_IN_D
Q12
2N7002DW-1-GP
84.27002.D3F
2ND = 84.27002.C3F
AC_OK
Jeff Modify 1024
R132 0R2J-2-GP
C296 SCD1U25V3KX-1GP
R133 309KR3F-GP
AD+ TO SYS
R40
D01R2512F-4-GP
G4 GAP-CLOSE-PWR
G5 GAP-CLOSE-PWR
SCD1U50V3KX-GP
C295
BQ24745_CSSP
C301 SCD1U50V3KX-GP
CHG_AGND
DCBATOUT
BT+
U50
P2003EVG-GP
84.02003.A37
2ND = 84.04433.A37
C34 SCD1U25V2Z-1GP
DY
R396 470KR2J-2-GP
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
R130 49K9R2F-L-GP
C303 SCD01U50V2KX-1GP
R148 0R2J-2-GP
AC_OK
BQ24745_ACOK
C326 SC1U10V3KX-3GP
43,56 BAT_SCL
43,56 BAT_SDA
phoenix tsai 09/28/07
ICREF
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
U16
BQ24745RHDR-GP
BQ24745_CSSN
IOUT
TP126 TPAD28
D9
1SS4000GPT-GP
C307 SC1U10V3KX-3GP
0R3-0-U-GP R131
BQ24745_BST
BQ24745_BST1
BQ24745_VDDP
24745_HIGH_G
MAX8731A_LX1
C297 SCD1U50V3KX-GP
24745_LOW_G
U48 SI4800BDY-T1
U47 SI4800BDY-T1
2ND = 84.08884.037
Jeff Modify 1024
L25 IND-5D6UH-32-GP
BT+_R
R144 D01R2512F-4-GP
C516 SC10U25V6KX-1GP
C518 SC10U25V6KX-1GP
C521 SC10U25V6KX-1GP
C527 SCD1U25V2Z-1GP
C331 SC10U25V6KX-1GP
C332 SC10U25V6KX-1GP
C334 SC10U25V6KX-1GP
C335 SC10U25V6KX-1GP
C327 SCD1U50V3KX-GP
G27 GAP-CLOSE-PWR
G28 GAP-CLOSE-PWR
C313 SCD1U50V3KX-GP
MAX8731A_CSIP
MAX8731A_CSIN
BATT_SENSE
BATT_SENSE 56
C324 SCD1U25V2Z-1GP
R153 0R0402-PAD
AD_IA
0R2J-2-GP R147
SC150P50V2JN-3GP
C312
BQ24745_FBO_RC
R142 4K7R2J-2-GP
BQ24745_FBO
R143 200KR2F-L-GP
C325 SC220P50V2KX-3GP
C316 SC2200P50V2KX-2GP
BQ24745_EAO_RC
R137 7K5R2F-1-GP
C310 SC56P50V2JN-2GP
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
C305 SC1U10V3KX-3GP
AC_IN# to KBC
R28 100KR2J-1-GP
AC_IN#
C20 SC1U10V3KX-3GP
Q3
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
R32 100KR2J-1-GP
R37 100KR2J-1-GP
R31 100KR2J-1-GP
Q2
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
C30 SCD1U10V2KX-4GP
CHG_ON#
DIS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size A3
Document Number
Olan
Rev SA
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Adaptor in to generate DCBATOUT

Jeff modify 20071031

DC1
ACES-CON5-7-GP-U1
20.F1002.005
2ND = 20.F1170.005

AD_JK

D12
S10P40PT-GP-U
83.10R04.F87
2ND = 83.10R10.080

C426
SCD1U50V3ZY-GP

AD_DOCK

C402
SCD1U50V3ZY-GP

D13
P4SSMJ24PT-GP
2ND = 83.00022.0AM

U33
P2003EVG-GP
2ND = 84.04433.A37

AD+
AD+_2

R236
200KR2J-1-GP

C428
SC1U50V5ZY-1-GP

Q10
PDTA124EU-1-GP
84.00124.K1K
2ND = 84.00124.N1K

AD_OFF#_JK

R240
100KR2J-1-GP

DOCK_AD+

D11
S10P40PT-GP-U
83.10R04.F87
2ND = 83.10R10.080

43

AD_OFF

Q11
MMBT2222A-3-GP
84.02222.V11

R247
1KR2J-1-GP

Jeff modify 20071031

BATTERY CONNECTOR

3D3V_AUX_S5

R438
100KR2J-1-GP

D23
BAV99PT-GP-U

D24
BAV99PT-GP-U

D25
BAV99PT-GP-U

DY

RN59
SRN33J-5-GP-U

43,55 BAT_SCL
43,55 BAT_SDA
43 BAT_IN#

BATA_SCL_1
BATA_SDA_1

BAT1
SYN-CON7-25-GP
20.80896.007
2ND = 20.80877.007

BT+

Jeff Modify it 1015
55 BATT_SENSE

R169
0R0402-PAD

EC106
SCD1U50V3ZY-GP

EC107
SCD1U50V3ZY-GP

EC109
SC1KP50V2KX-1GP

EC110
SC1KP50V2KX-1GP

EC111
SC10P50V2JN-4GP

EC112
SC10P50V2JN-4GP

DIS

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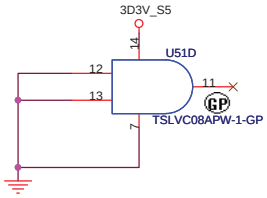
Title	***AD/BATT CONN***	
Size **A4**	Document Number **Olan**	Rev SA
Date: Monday, November 19, 2007	Sheet 56 of 57	



STAND OFF ON TOP

MDC

H4 HOLE H3 HOLE

34.42Y01.001

STAND OFF ON BOTTOM

CPU & NB

H8 HOLE H7 HOLE H16 HOLE H5 HOLE H11 HOLE H12 HOLE H32 HOLE

34.42Y01.001

Mini Card

H29 HOLE H6 HOLE

34.4G502.001

MXM

H18 HOLE H14 HOLE H17 HOLE H13 HOLE

34.4G805.001

MXM

H20 HOLE H19 HOLE

34.4z401.001

H1 HOLE H22 HOLE H25 HOLE H15 HOLE H21 HOLE H33 HOLE H27 HOLE H31 HOLE H30 HOLE H2 HOLE H10 HOLE H9 HOLE H24 HOLE H23 HOLE H28 HOLE H26 HOLE

DIS

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size | Document Number: **Olan** | Rev: SA

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