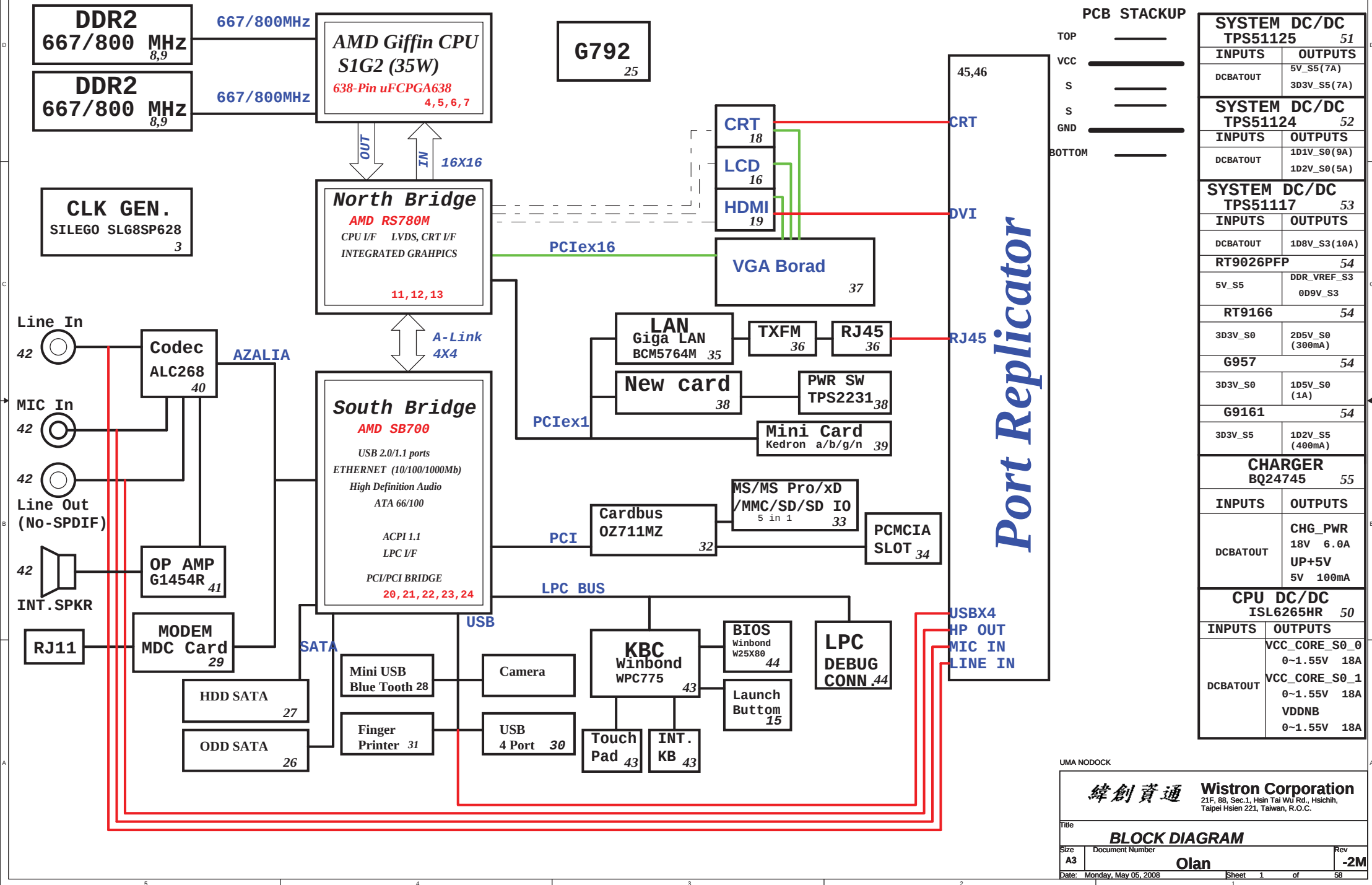
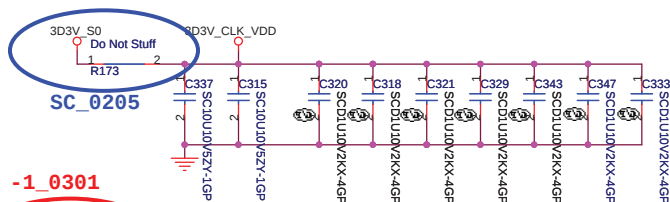


Olan (TM15") Block Diagram

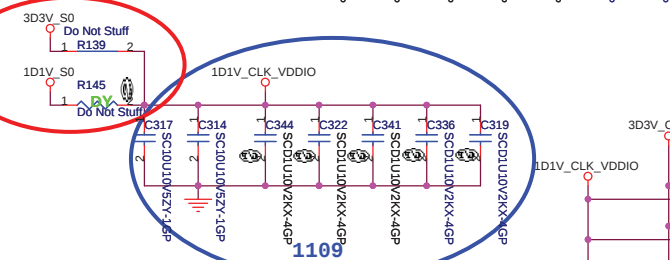
Project code: 91.4Z701.001
PCB P/N : 48.4Z701.001
REVISION : 07249-2M



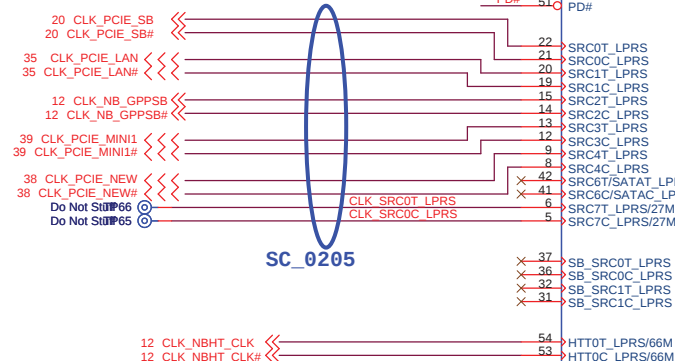
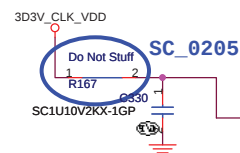
UMA NODOCK			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
N34" to "SRN47J-7-GP"; UNdummy "EC61" "EC61"			
Title			
HISTORY			
Size	Document Number	Rev	
A3	Olán	-1	
Date:	Friday, April 18, 2008	Sheet	2 of 58



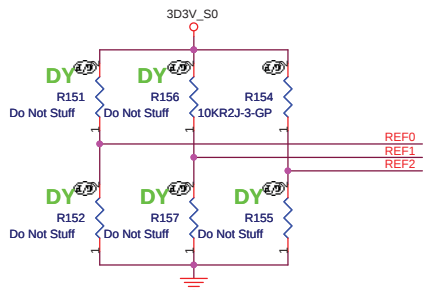
-1_0301



1109



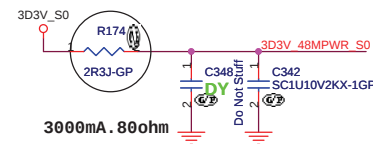
SC_0205



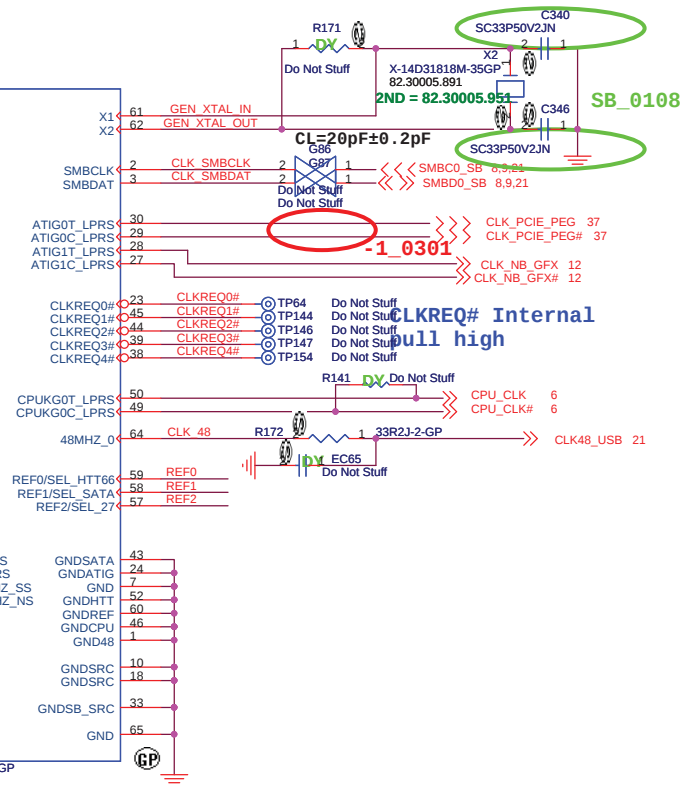
SEL_SATA	1	100 MHz non-spreading differential SRC clock
REF1	0*	100 MHz spreading differential SRC clock
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
REF0	0*	100 MHz differential HTT clock

* default

CPU_CLK(200MHz)



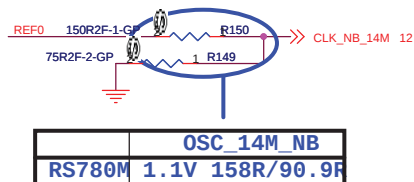
3000mA.800ohm



-1_0301

CLKREQ# Internal Pull high

ICS9LPRS480BKLFT-GP
71.09480.A03
2nd = SLG:71.08628.003
-1_0310 change to 71.09480.A03



OSC_14M_NB
RS780M 1.1V 158R/90.9F

Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

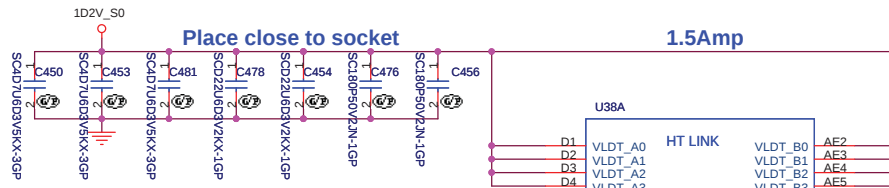
NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

UMA NODOCK

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title			CLKGEN_ICS9LPRS480
Size	Document Number	Rev	
A3	Olan	-2M	
Date:	Monday, May 05, 2008	Sheet	3 of 58



11 HT_NB_CPU_CAD_H0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	HT_CPU_NB_CAD_H0	11
11 HT_NB_CPU_CAD_L0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	HT_CPU_NB_CAD_L0	11
11 HT_NB_CPU_CAD_H1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	HT_CPU_NB_CAD_H1	11
11 HT_NB_CPU_CAD_L1	G1	L0_CADIN_L1	L0_CADOUT_L1	AC3	HT_CPU_NB_CAD_L1	11
11 HT_NB_CPU_CAD_H2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	HT_CPU_NB_CAD_H2	11
11 HT_NB_CPU_CAD_L2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	HT_CPU_NB_CAD_L2	11
11 HT_NB_CPU_CAD_H3	H1	L0_CADIN_H3	L0_CADOUT_H3	AA2	HT_CPU_NB_CAD_H3	11
11 HT_NB_CPU_CAD_L3	J1	L0_CADIN_L3	L0_CADOUT_L3	W2	HT_CPU_NB_CAD_L3	11
11 HT_NB_CPU_CAD_H4	K1	L0_CADIN_H4	L0_CADOUT_H4	AA3	HT_CPU_NB_CAD_H4	11
11 HT_NB_CPU_CAD_L4	L3	L0_CADIN_L4	L0_CADOUT_L4	W3	HT_CPU_NB_CAD_L4	11
11 HT_NB_CPU_CAD_H5	L2	L0_CADIN_H5	L0_CADOUT_H5	V1	HT_CPU_NB_CAD_H5	11
11 HT_NB_CPU_CAD_L5	L1	L0_CADIN_L5	L0_CADOUT_L5	U2	HT_CPU_NB_CAD_L5	11
11 HT_NB_CPU_CAD_H6	M1	L0_CADIN_H6	L0_CADOUT_H6	U3	HT_CPU_NB_CAD_H6	11
11 HT_NB_CPU_CAD_L6	N3	L0_CADIN_L6	L0_CADOUT_L6	T1	HT_CPU_NB_CAD_L6	11
11 HT_NB_CPU_CAD_H7	N2	L0_CADIN_H7	L0_CADOUT_H7	R1	HT_CPU_NB_CAD_H7	11
11 HT_NB_CPU_CAD_L7	E5	L0_CADIN_L7	L0_CADOUT_L7	AD4	HT_CPU_NB_CAD_L7	11
11 HT_NB_CPU_CAD_H8	F5	L0_CADIN_H8	L0_CADOUT_H8	AD3	HT_CPU_NB_CAD_H8	11
11 HT_NB_CPU_CAD_L8	F3	L0_CADIN_L8	L0_CADOUT_L8	AD5	HT_CPU_NB_CAD_L8	11
11 HT_NB_CPU_CAD_H9	F4	L0_CADIN_H9	L0_CADOUT_H9	AC5	HT_CPU_NB_CAD_H9	11
11 HT_NB_CPU_CAD_L9	G5	L0_CADIN_L9	L0_CADOUT_L9	AB4	HT_CPU_NB_CAD_L9	11
11 HT_NB_CPU_CAD_H10	H5	L0_CADIN_H10	L0_CADOUT_H10	AB3	HT_CPU_NB_CAD_H10	11
11 HT_NB_CPU_CAD_L10	H3	L0_CADIN_L10	L0_CADOUT_L10	AB5	HT_CPU_NB_CAD_L10	11
11 HT_NB_CPU_CAD_H11	H4	L0_CADIN_H11	L0_CADOUT_H11	AA5	HT_CPU_NB_CAD_H11	11
11 HT_NB_CPU_CAD_L11	K4	L0_CADIN_L11	L0_CADOUT_L11	V5	HT_CPU_NB_CAD_L11	11
11 HT_NB_CPU_CAD_H12	L5	L0_CADIN_H12	L0_CADOUT_H12	W5	HT_CPU_NB_CAD_H12	11
11 HT_NB_CPU_CAD_L12	K3	L0_CADIN_L12	L0_CADOUT_L12	V4	HT_CPU_NB_CAD_L12	11
11 HT_NB_CPU_CAD_H13	M5	L0_CADIN_H13	L0_CADOUT_H13	V3	HT_CPU_NB_CAD_H13	11
11 HT_NB_CPU_CAD_L13	M3	L0_CADIN_L13	L0_CADOUT_L13	V5	HT_CPU_NB_CAD_L13	11
11 HT_NB_CPU_CAD_H14	M4	L0_CADIN_H14	L0_CADOUT_H14	U5	HT_CPU_NB_CAD_H14	11
11 HT_NB_CPU_CAD_L14	N5	L0_CADIN_L14	L0_CADOUT_L14	T4	HT_CPU_NB_CAD_L14	11
11 HT_NB_CPU_CAD_H15	P5	L0_CADIN_H15	L0_CADOUT_H15	T3	HT_CPU_NB_CAD_H15	11
11 HT_NB_CPU_CAD_L15	P3	L0_CADIN_L15	L0_CADOUT_L15	T1	HT_CPU_NB_CAD_L15	11
11 HT_NB_CPU_CLK_H0	J2	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	HT_CPU_NB_CLK_H0	11
11 HT_NB_CPU_CLK_L0	J1	L0_CLKIN_L0	L0_CLKOUT_L0	W1	HT_CPU_NB_CLK_L0	11
11 HT_NB_CPU_CLK_H1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	HT_CPU_NB_CLK_H1	11
11 HT_NB_CPU_CLK_L1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	HT_CPU_NB_CLK_L1	11
11 HT_NB_CPU_CTL_H0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	HT_CPU_NB_CTL_H0	11
11 HT_NB_CPU_CTL_L0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	HT_CPU_NB_CTL_L0	11
11 HT_NB_CPU_CTL_H1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	HT_CPU_NB_CTL_H1	11
11 HT_NB_CPU_CTL_L1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	HT_CPU_NB_CTL_L1	11

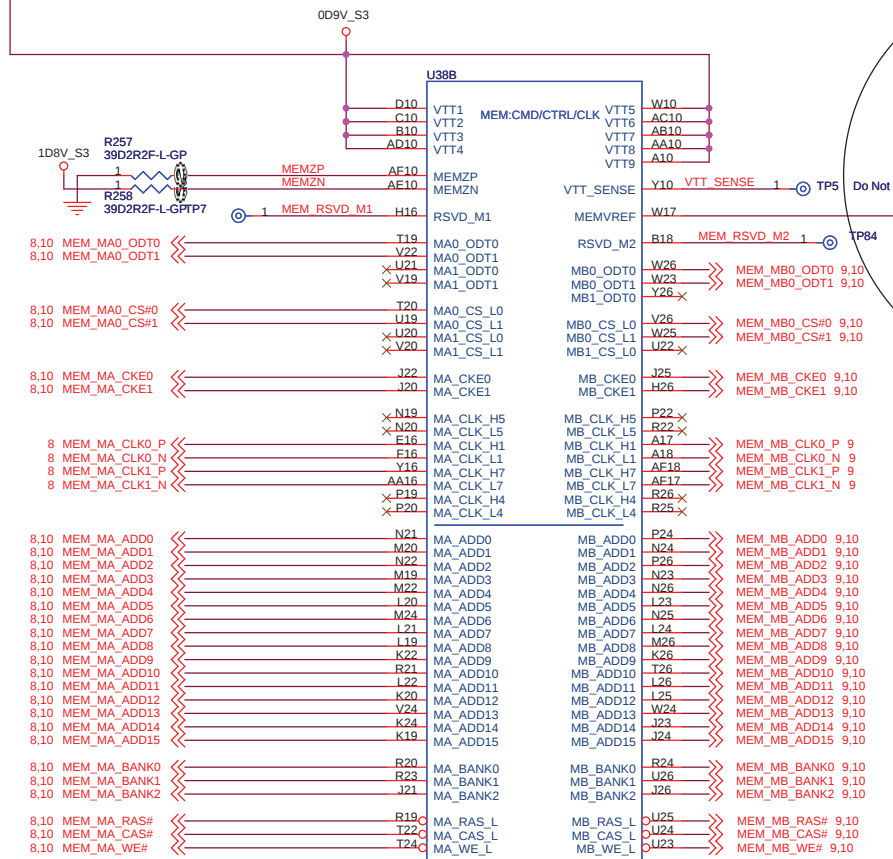
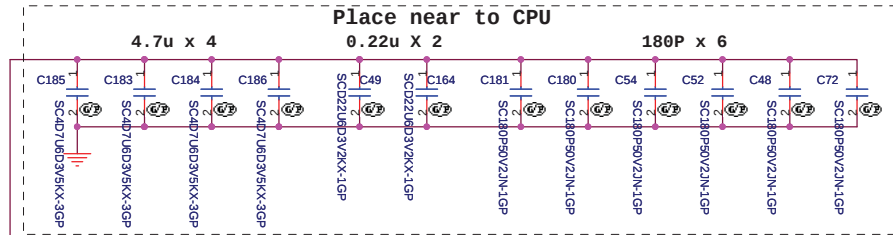
SKT-CPU638P-GP-U1
62 10055 111
2ND = 62.10040.471

SKT - BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V

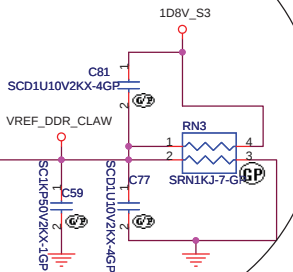
UMA NODOCK

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU_HT_LINK I/F (1/4)		
Size A3	Document Number	Rev -1
Olan		
Date: Friday, April 18, 2008	Sheet 4	of 58



SKT-CPU638P-GP-U1

CLOSE TO CPU



8	MEM_MA_DATA0
8	MEM_MA_DATA1
8	MEM_MA_DATA2
8	MEM_MA_DATA3
8	MEM_MA_DATA4
8	MEM_MA_DATA5
8	MEM_MA_DATA6
8	MEM_MA_DATA7
8	MEM_MA_DATA8
8	MEM_MA_DATA9
8	MEM_MA_DATA10
8	MEM_MA_DATA11
8	MEM_MA_DATA12
8	MEM_MA_DATA13
8	MEM_MA_DATA14
8	MEM_MA_DATA15
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8	MEM_MA_DATA58
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8	MEM_MA_DATA60
8	MEM_MA_DATA61
8	MEM_MA_DATA62
8	MEM_MA_DATA63

8	MEM_MA_DM0
8	MEM_MA_DM1
8	MEM_MA_DM2
8	MEM_MA_DM3
8	MEM_MA_DM4
8	MEM_MA_DM5
8	MEM_MA_DM6
8	MEM_MA_DM7

8	MEM_MA_DQS0_P
8	MEM_MA_DQS0_N
8	MEM_MA_DQS1_P
8	MEM_MA_DQS1_N
8	MEM_MA_DQS2_P
8	MEM_MA_DQS2_N
8	MEM_MA_DQS3_P
8	MEM_MA_DQS3_N
8	MEM_MA_DQS4_P
8	MEM_MA_DQS4_N
8	MEM_MA_DQS5_P
8	MEM_MA_DQS5_N
8	MEM_MA_DQS6_P
8	MEM_MA_DQS6_N
8	MEM_MA_DQS7_P
8	MEM_MA_DQS7_N

U38C	
MEM-DATA	
G12	MA_DATA0
F12	MA_DATA1
H14	MA_DATA2
G14	MA_DATA3
H11	MA_DATA4
C13	MA_DATA5
E13	MA_DATA6
H15	MA_DATA7
E15	MA_DATA8
E17	MA_DATA9
E17	MA_DATA10
E17	MA_DATA11
F14	MA_DATA12
C17	MA_DATA13
G17	MA_DATA14
G18	MA_DATA15
C19	MA_DATA16
D22	MA_DATA17
E18	MA_DATA18
F18	MA_DATA19
B22	MA_DATA20
C23	MA_DATA21
F20	MA_DATA22
E22	MA_DATA23
H24	MA_DATA24
.119	MA_DATA25
E21	MA_DATA26
E22	MA_DATA27
H20	MA_DATA28
H22	MA_DATA29
MA_DATA30	MA_DATA30
MA_DATA31	MA_DATA31
AB24	MA_DATA32
AB22	MA_DATA33
AA21	MA_DATA34
W21	MA_DATA35
W21	MA_DATA36
Y22	MA_DATA37
AA22	MA_DATA38
Y20	MA_DATA39
MA_DATA40	MA_DATA40
AA20	MA_DATA41
AA18	MA_DATA42
AB18	MA_DATA43
AB21	MA_DATA44
AD19	MA_DATA45
Y18	MA_DATA46
AD17	MA_DATA47
W16	MA_DATA48
Y14	MA_DATA49
MA_DATA50	MA_DATA50
Y17	MA_DATA51
MA_DATA52	MA_DATA52
AB17	MA_DATA53
AB15	MA_DATA54
AD15	MA_DATA55
AB13	MA_DATA56
AD13	MA_DATA57
Y12	MA_DATA58
W11	MA_DATA59
AB14	MA_DATA60
AA14	MA_DATA61
AB12	MA_DATA62
AA12	MA_DATA63

MA_DM0	MA_DM0
MA_DM1	MA_DM1
MA_DM2	MA_DM2
MA_DM3	MA_DM3
MA_DM4	MA_DM4
MA_DM5	MA_DM5
MA_DM6	MA_DM6
MA_DM7	MA_DM7

G13	MA_DQS_H0
H13	MA_DQS_L0
G16	MA_DQS_H1
G15	MA_DQS_L1
C22	MA_DQS_H2
C21	MA_DQS_L2
G22	MA_DQS_H3
G21	MA_DQS_L3
AD23	MA_DQS_H4
AC23	MA_DQS_L4
AB19	MA_DQS_H5
AB20	MA_DQS_L5
Y15	MA_DQS_H6
W15	MA_DQS_L6
W12	MA_DQS_H7
W13	MA_DQS_L7

MB_DATA0	MB_DATA0
MB_DATA1	MB_DATA1
MB_DATA2	MB_DATA2
MB_DATA3	MB_DATA3
MB_DATA4	MB_DATA4
MB_DATA5	MB_DATA5
MB_DATA6	MB_DATA6
MB_DATA7	MB_DATA7
MB_DATA8	MB_DATA8
MB_DATA9	MB_DATA9
MB_DATA10	MB_DATA10
MB_DATA11	MB_DATA11
MB_DATA12	MB_DATA12
MB_DATA13	MB_DATA13
MB_DATA14	MB_DATA14
MB_DATA15	MB_DATA15
MB_DATA16	MB_DATA16
MB_DATA17	MB_DATA17
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MB_DATA20	MB_DATA20
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MB_DATA49	MB_DATA49
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MB_DATA52	MB_DATA52
MB_DATA53	MB_DATA53
MB_DATA54	MB_DATA54
MB_DATA55	MB_DATA55
MB_DATA56	MB_DATA56
MB_DATA57	MB_DATA57
MB_DATA58	MB_DATA58
MB_DATA59	MB_DATA59
MB_DATA60	MB_DATA60
MB_DATA61	MB_DATA61
MB_DATA62	MB_DATA62
MB_DATA63	MB_DATA63

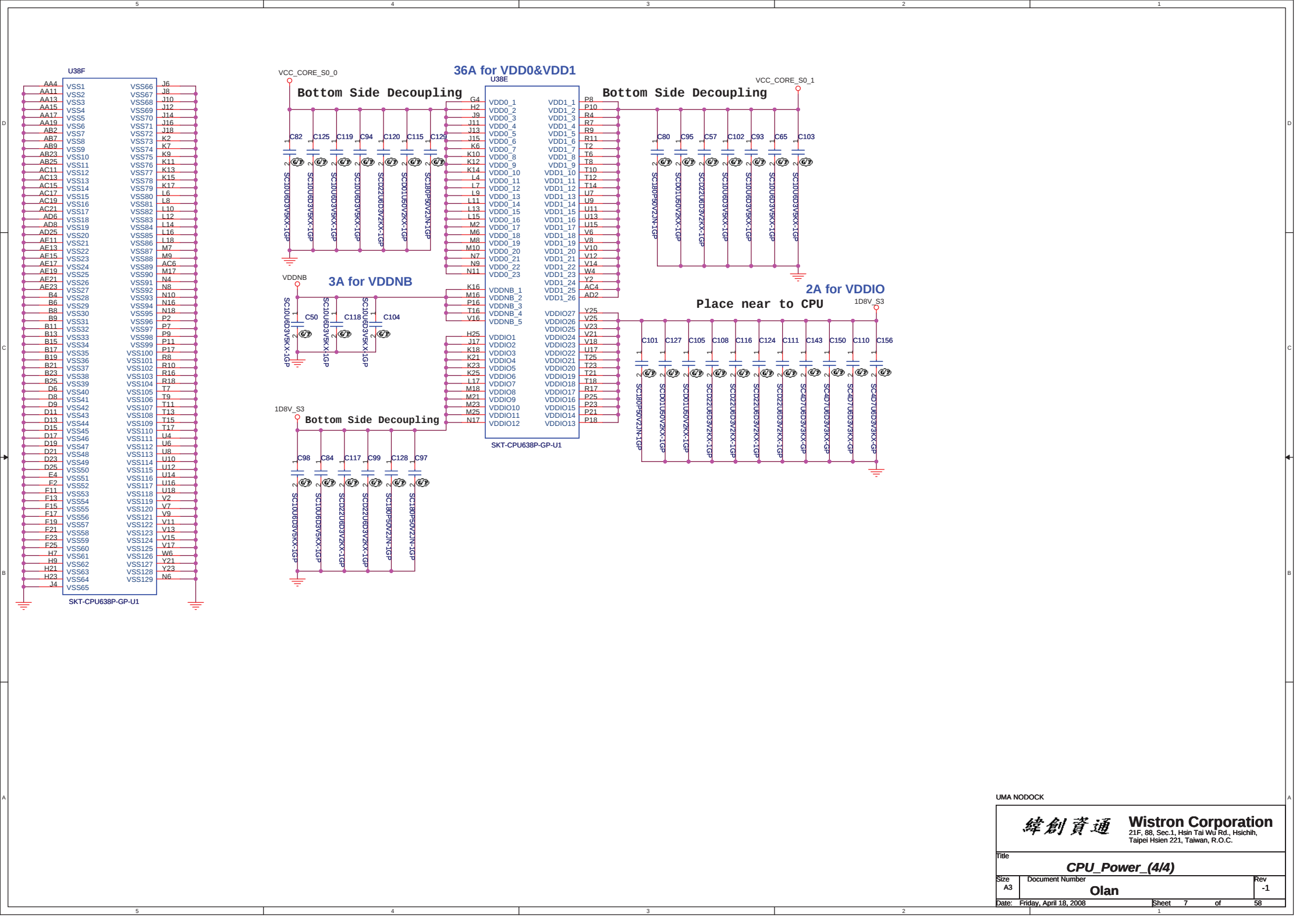
MB_DM0	MB_DM0
MB_DM1	MB_DM1
MB_DM2	MB_DM2
MB_DM3	MB_DM3
MB_DM4	MB_DM4
MB_DM5	MB_DM5
MB_DM6	MB_DM6
MB_DM7	MB_DM7

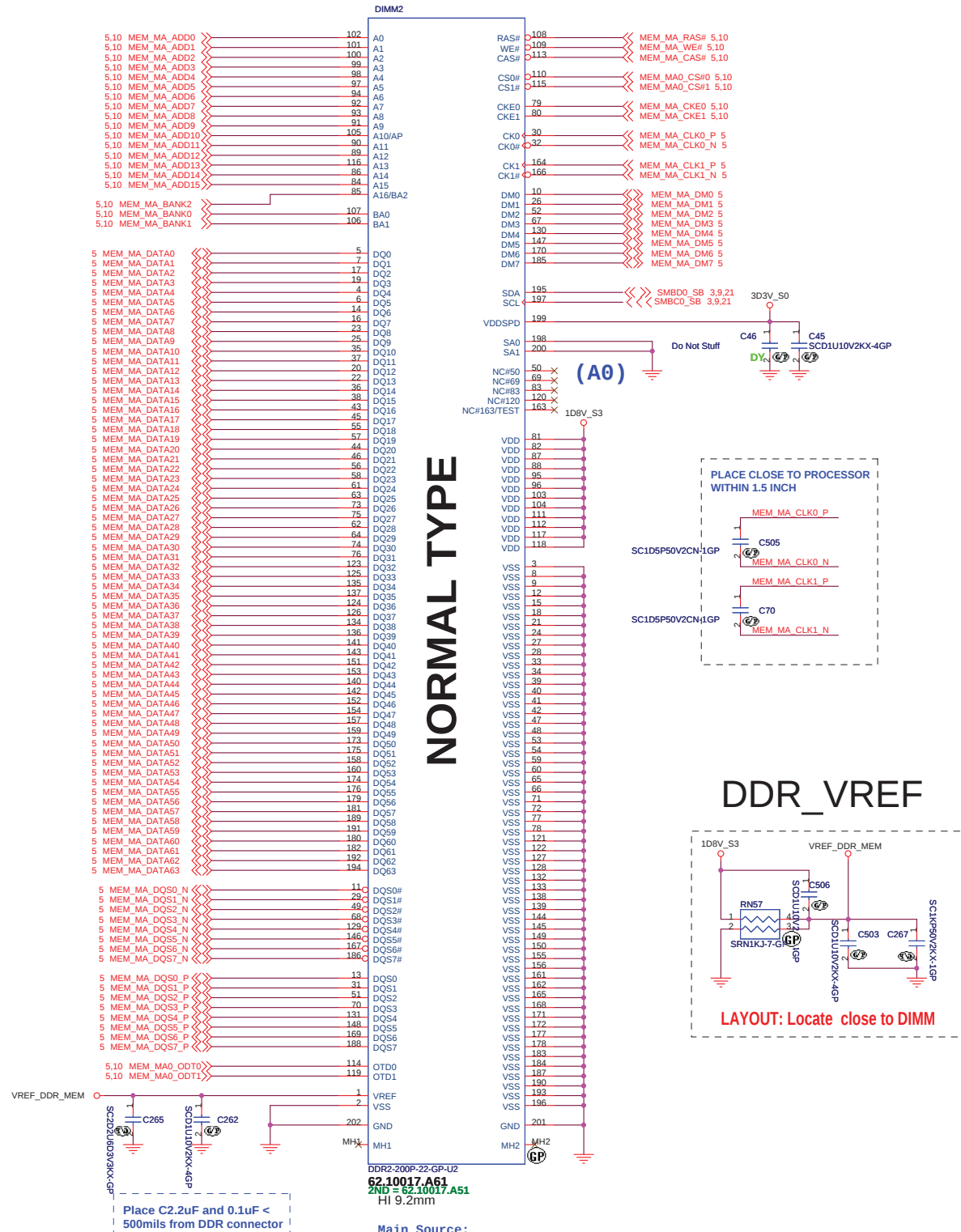
MB_DQS_H0	MB_DQS_H0
MB_DQS_L0	MB_DQS_L0
MB_DQS_H1	MB_DQS_H1
MB_DQS_L1	MB_DQS_L1
MB_DQS_H2	MB_DQS_H2
MB_DQS_L2	MB_DQS_L2
MB_DQS_H3	MB_DQS_H3
MB_DQS_L3	MB_DQS_L3
MB_DQS_H4	MB_DQS_H4
MB_DQS_L4	MB_DQS_L4
MB_DQS_H5	MB_DQS_H5
MB_DQS_L5	MB_DQS_L5
MB_DQS_H6	MB_DQS_H6
MB_DQS_L6	MB_DQS_L6
MB_DQS_H7	MB_DQS_H7
MB_DQS_L7	MB_DQS_L7

UMA NODOCK

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU_DDR (2/4)		
Size	Document Number	Rev
A3	Olan	-1
Date:	Friday, April 18, 2008	Sheet 5 of 58



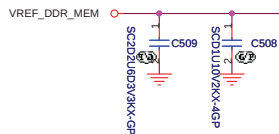


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5.10 MEM_MB_ADD1 >>> 101 A1
5.10 MEM_MB_ADD2 >>> 100 A2
5.10 MEM_MB_ADD3 >>> 99 A3
5.10 MEM_MB_ADD4 >>> 98 A4
5.10 MEM_MB_ADD5 >>> 97 A5
5.10 MEM_MB_ADD6 >>> 96 A6
5.10 MEM_MB_ADD7 >>> 95 A7
5.10 MEM_MB_ADD8 >>> 94 A8
5.10 MEM_MB_ADD9 >>> 93 A9
5.10 MEM_MB_ADD10 >>> 108 A10/AP
5.10 MEM_MB_ADD11 >>> 90 A11
5.10 MEM_MB_ADD12 >>> 89 A12
5.10 MEM_MB_ADD13 >>> 116 A13
5.10 MEM_MB_ADD14 >>> 86 A14
5.10 MEM_MB_ADD15 >>> 84 A15
5.10 MEM_MB_BANK2 >>> 107 BA0
5.10 MEM_MB_BANK0 >>> 106 BA1
5.10 MEM_MB_BANK1 >>> 106 BA1

5 MEM_MB_DATA0 >>> 5 DQ0
5 MEM_MB_DATA1 >>> 7 DQ1
5 MEM_MB_DATA2 >>> 17 DQ2
5 MEM_MB_DATA3 >>> 19 DQ3
5 MEM_MB_DATA4 >>> 4 DQ4
5 MEM_MB_DATA5 >>> 6 DQ5
5 MEM_MB_DATA6 >>> 14 DQ6
5 MEM_MB_DATA7 >>> 16 DQ7
5 MEM_MB_DATA8 >>> 23 DQ8
5 MEM_MB_DATA9 >>> 25 DQ9
5 MEM_MB_DATA10 >>> 35 DQ10
5 MEM_MB_DATA11 >>> 37 DQ11
5 MEM_MB_DATA12 >>> 20 DQ12
5 MEM_MB_DATA13 >>> 22 DQ13
5 MEM_MB_DATA14 >>> 36 DQ14
5 MEM_MB_DATA15 >>> 38 DQ15
5 MEM_MB_DATA16 >>> 43 DQ16
5 MEM_MB_DATA17 >>> 45 DQ17
5 MEM_MB_DATA18 >>> 55 DQ18
5 MEM_MB_DATA19 >>> 57 DQ19
5 MEM_MB_DATA20 >>> 44 DQ20
5 MEM_MB_DATA21 >>> 46 DQ21
5 MEM_MB_DATA22 >>> 58 DQ22
5 MEM_MB_DATA23 >>> 61 DQ23
5 MEM_MB_DATA24 >>> 58 DQ24
5 MEM_MB_DATA25 >>> 63 DQ25
5 MEM_MB_DATA26 >>> 73 DQ26
5 MEM_MB_DATA27 >>> 75 DQ27
5 MEM_MB_DATA28 >>> 62 DQ28
5 MEM_MB_DATA29 >>> 64 DQ29
5 MEM_MB_DATA30 >>> 74 DQ30
5 MEM_MB_DATA31 >>> 76 DQ31
5 MEM_MB_DATA32 >>> 123 DQ32
5 MEM_MB_DATA33 >>> 125 DQ33
5 MEM_MB_DATA34 >>> 135 DQ34
5 MEM_MB_DATA35 >>> 137 DQ35
5 MEM_MB_DATA36 >>> 124 DQ36
5 MEM_MB_DATA37 >>> 126 DQ37
5 MEM_MB_DATA38 >>> 134 DQ38
5 MEM_MB_DATA39 >>> 136 DQ39
5 MEM_MB_DATA40 >>> 141 DQ40
5 MEM_MB_DATA41 >>> 143 DQ41
5 MEM_MB_DATA42 >>> 151 DQ42
5 MEM_MB_DATA43 >>> 153 DQ43
5 MEM_MB_DATA44 >>> 140 DQ44
5 MEM_MB_DATA45 >>> 142 DQ45
5 MEM_MB_DATA46 >>> 152 DQ46
5 MEM_MB_DATA47 >>> 154 DQ47
5 MEM_MB_DATA48 >>> 157 DQ48
5 MEM_MB_DATA49 >>> 159 DQ49
5 MEM_MB_DATA50 >>> 173 DQ50
5 MEM_MB_DATA51 >>> 175 DQ51
5 MEM_MB_DATA52 >>> 158 DQ52
5 MEM_MB_DATA53 >>> 160 DQ53
5 MEM_MB_DATA54 >>> 174 DQ54
5 MEM_MB_DATA55 >>> 176 DQ55
5 MEM_MB_DATA56 >>> 179 DQ56
5 MEM_MB_DATA57 >>> 181 DQ57
5 MEM_MB_DATA58 >>> 189 DQ58
5 MEM_MB_DATA59 >>> 191 DQ59
5 MEM_MB_DATA60 >>> 180 DQ60
5 MEM_MB_DATA61 >>> 182 DQ61
5 MEM_MB_DATA62 >>> 192 DQ62
5 MEM_MB_DATA63 >>> 194 DQ63

5 MEM_MB_DQS0_N >>> 11C DQS0#
5 MEM_MB_DQS1_N >>> 29C DQS1#
5 MEM_MB_DQS2_N >>> 49C DQS2#
5 MEM_MB_DQS3_N >>> 68C DQS3#
5 MEM_MB_DQS4_N >>> 129C DQS4#
5 MEM_MB_DQS5_N >>> 146C DQS5#
5 MEM_MB_DQS6_N >>> 167C DQS6#
5 MEM_MB_DQS7_N >>> 186C DQS7#
5 MEM_MB_DQS0_P >>> 13 DQS0
5 MEM_MB_DQS1_P >>> 31 DQS1
5 MEM_MB_DQS2_P >>> 51 DQS2
5 MEM_MB_DQS3_P >>> 70 DQS3
5 MEM_MB_DQS4_P >>> 131 DQS4
5 MEM_MB_DQS5_P >>> 148 DQS5
5 MEM_MB_DQS6_P >>> 169 DQS6
5 MEM_MB_DQS7_P >>> 188 DQS7

5.10 MEM_MB0_ODT0 >>> 114 OTD0
5.10 MEM_MB0_ODT1 >>> 119 OTD1

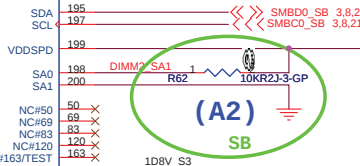


Place C2.2uF and 0.1uF < 500mils from DDR connector

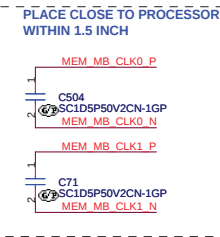
LOW 5.2 mm Main Source:

REVERSE TYPE

RAS# 108 A0
WE# 109 A1
CAS# 113 A2
CS0# 110 A3
CS1# 115 A4
CKE0 79 A5
CKE1 80 A6
CK0 30 A7
CK0# 32 A8
CK1 164 A9
CK1# 166 A10
DM0 10 A11
DM1 26 A12
DM2 52 A13
DM3 130 A14
DM4 147 A15
DM5 170 A16/BA2
DM6 185 A17
DM7 185 A18



VDD 81
VDD 82
VDD 87
VDD 88
VDD 95
VDD 96
VDD 103
VDD 104
VDD 111
VDD 112
VDD 117
VDD 118
VSS 3
VSS 8
VSS 9
VSS 12
VSS 15
VSS 18
VSS 21
VSS 24
VSS 27
VSS 28
VSS 33
VSS 34
VSS 38
VSS 40
VSS 41
VSS 42
VSS 47
VSS 48
VSS 49
VSS 53
VSS 54
VSS 59
VSS 60
VSS 65
VSS 66
VSS 71
VSS 72
VSS 77
VSS 78
VSS 121
VSS 122
VSS 127
VSS 128
VSS 132
VSS 133
VSS 138
VSS 139
VSS 144
VSS 145
VSS 149
VSS 150
VSS 155
VSS 156
VSS 161
VSS 162
VSS 165
VSS 168
VSS 171
VSS 172
VSS 177
VSS 178
VSS 183
VSS 184
VSS 187
VSS 190
VSS 193
VSS 196
VSS 201
GND 201
MH2 GP



PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

MEM_MB_CLK0_P
C504
SC1D5P50V2CN-1GP
MEM_MB_CLK0_N
C71
SC1D5P50V2CN-1GP
MEM_MB_CLK1_N

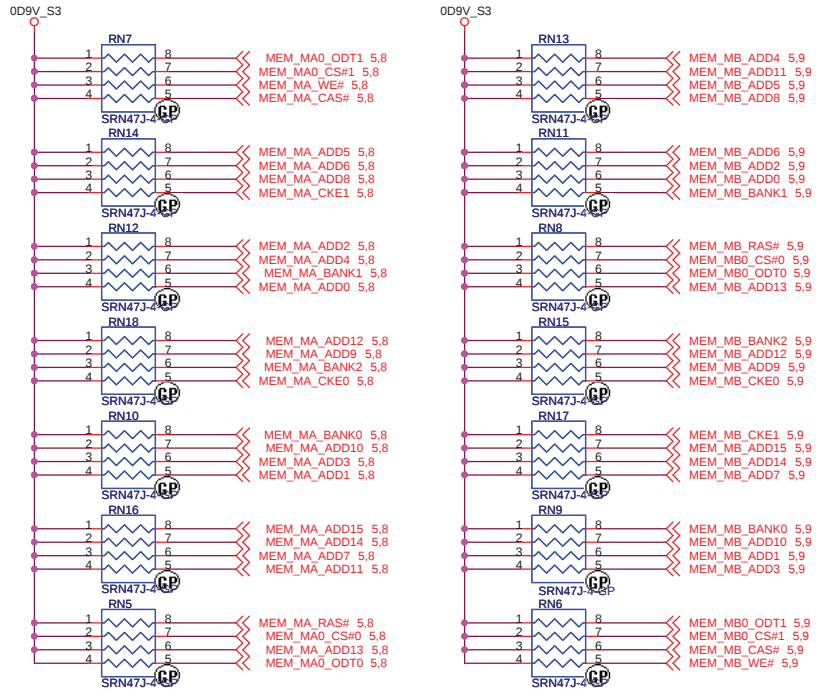
UMA NODOCK

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

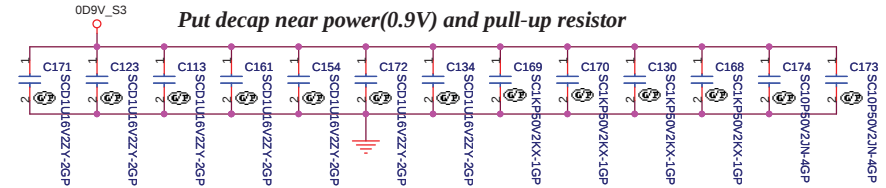
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

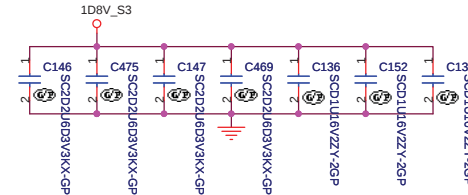


Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

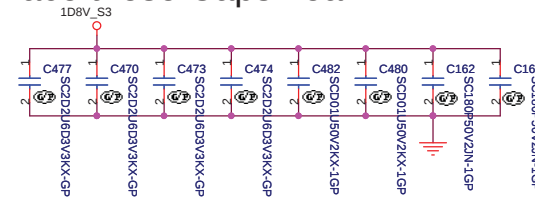


Place these Caps near DM1

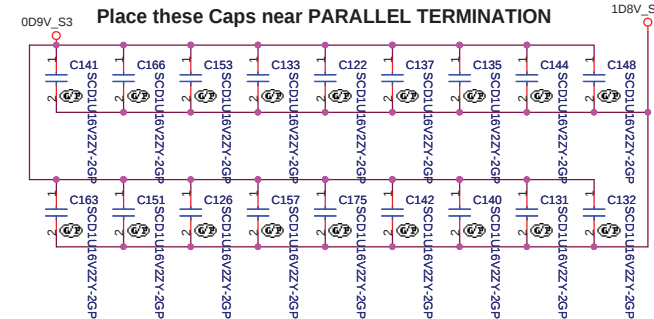


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



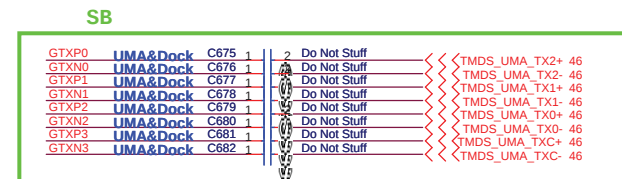
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

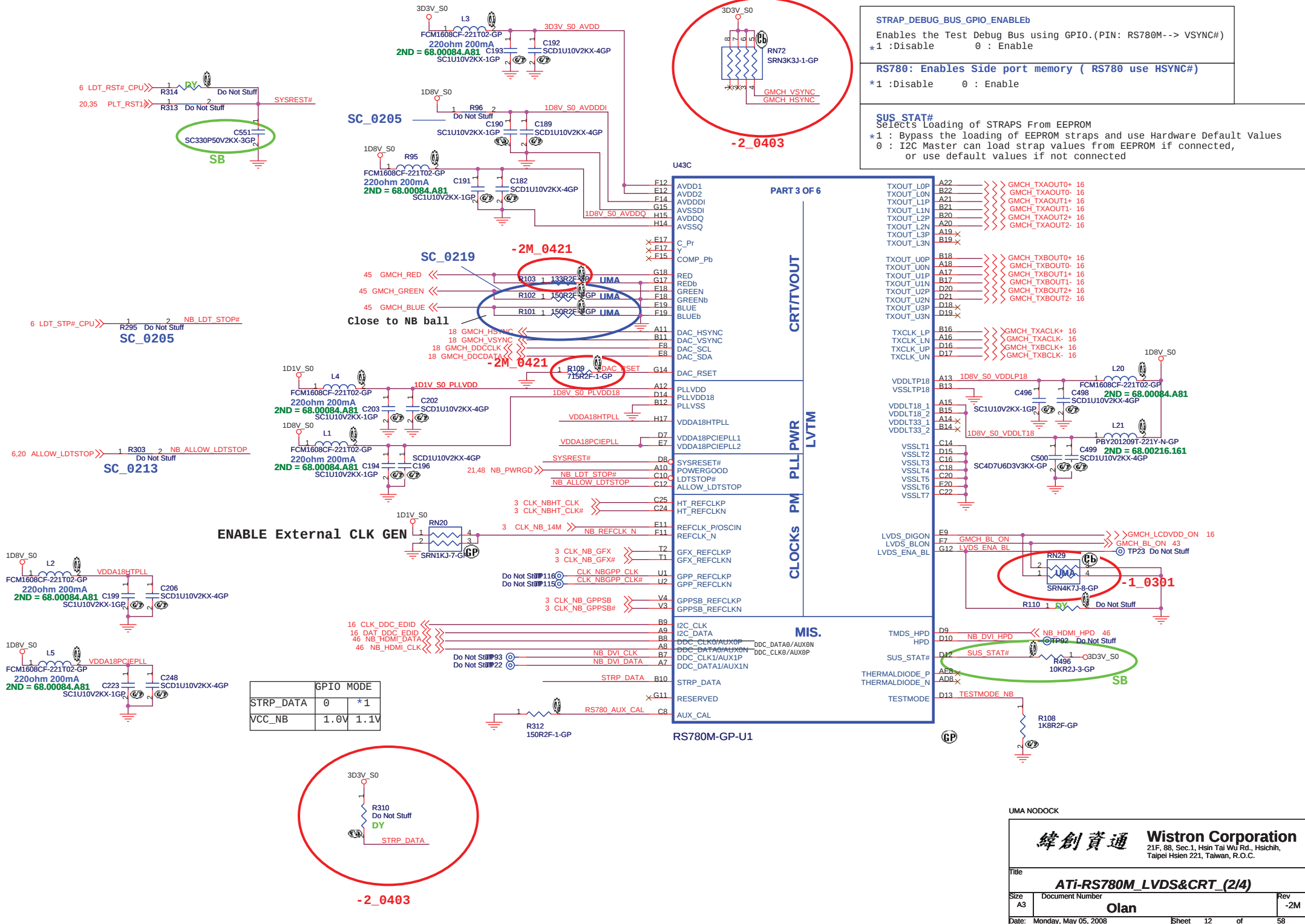


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Title		
DDR DAMPING & TERMINATION		
Size	Document Number	Rev
A3	Olan	-1
Date:	Friday, April 18, 2008	Sheet 10 of 58



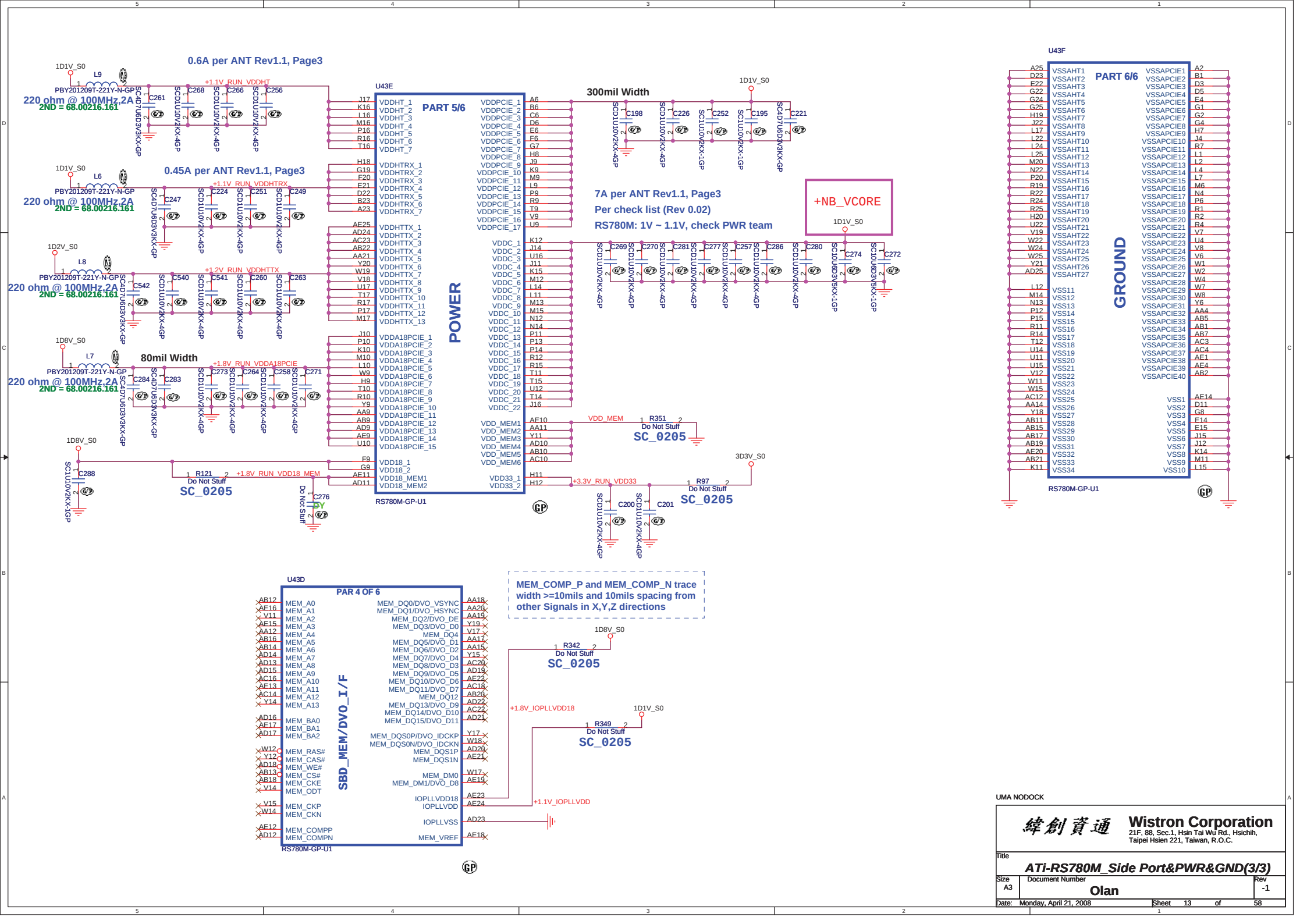


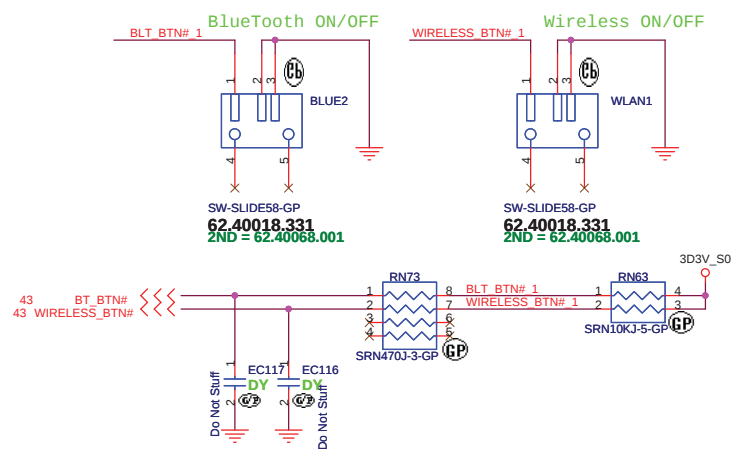
STRAP_DEBUG_BUS_GPIO_ENABLEB
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

GPIO MODE		
STRP_DATA	0	*1
VCC_NB	1.0V	1.1V





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Title

SWITCH

Size
A3

Document Number

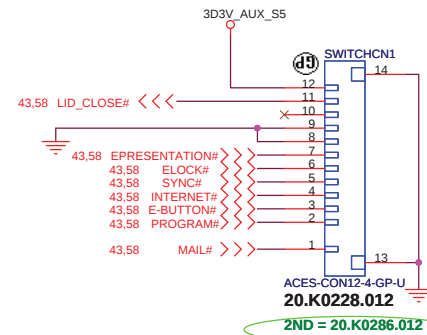
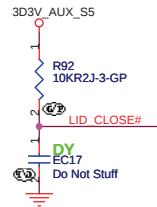
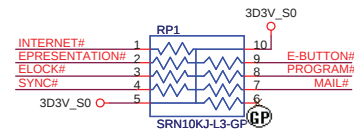
Olan

Rev
-1

Date: Friday, April 18, 2008

Sheet 14 of 58

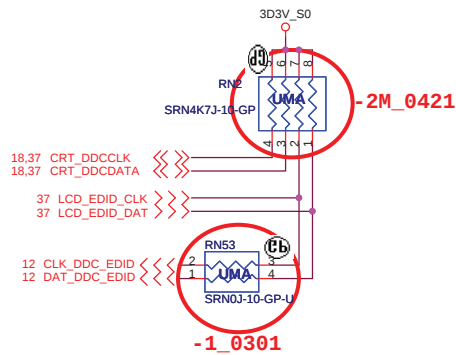
LAUNCH



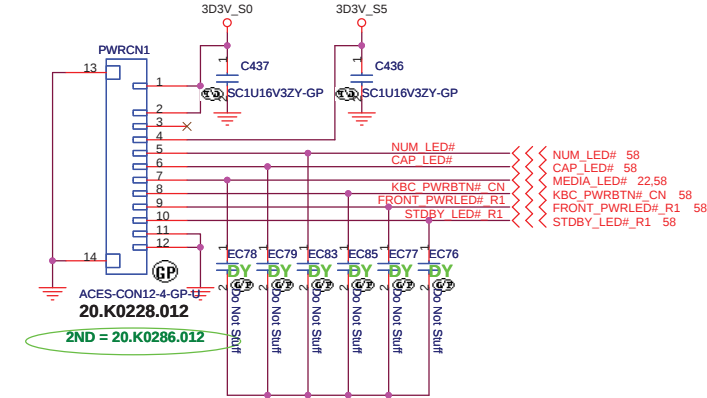
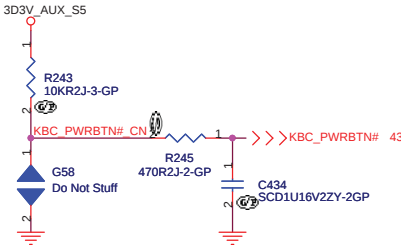
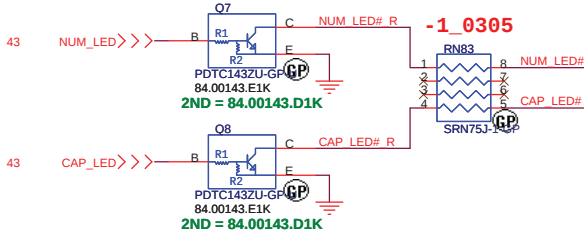
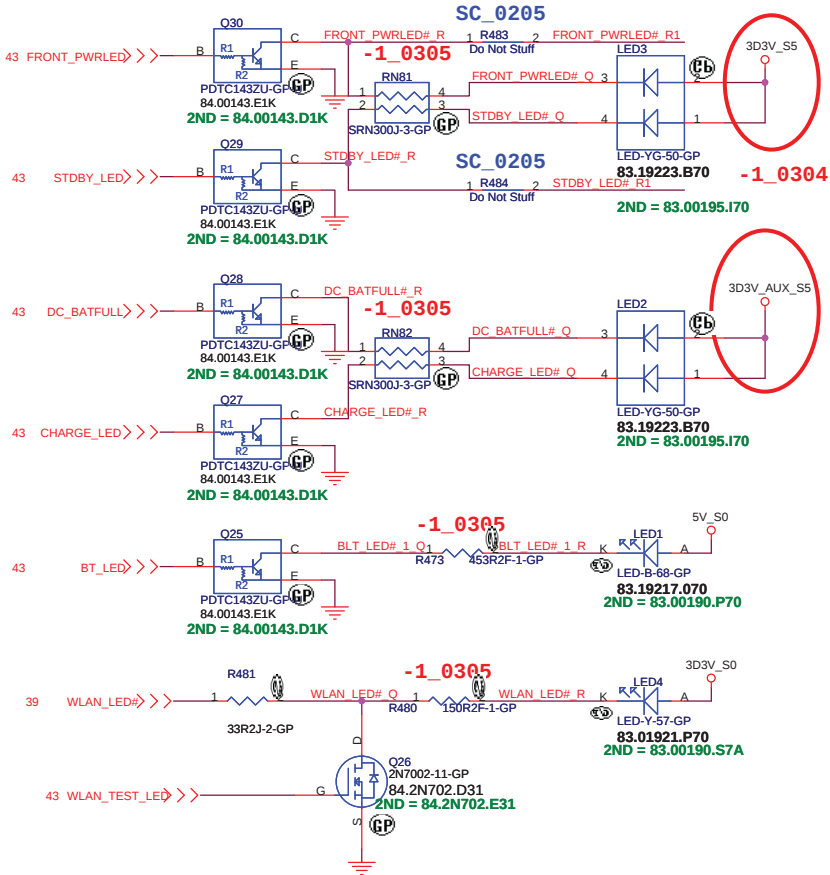
2ND = 20.K0286.012
SB_0108_change 2nd source



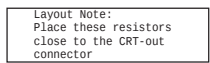
LCD/INVERTER/CCD CONN



LED



SB_0108_change 2nd source

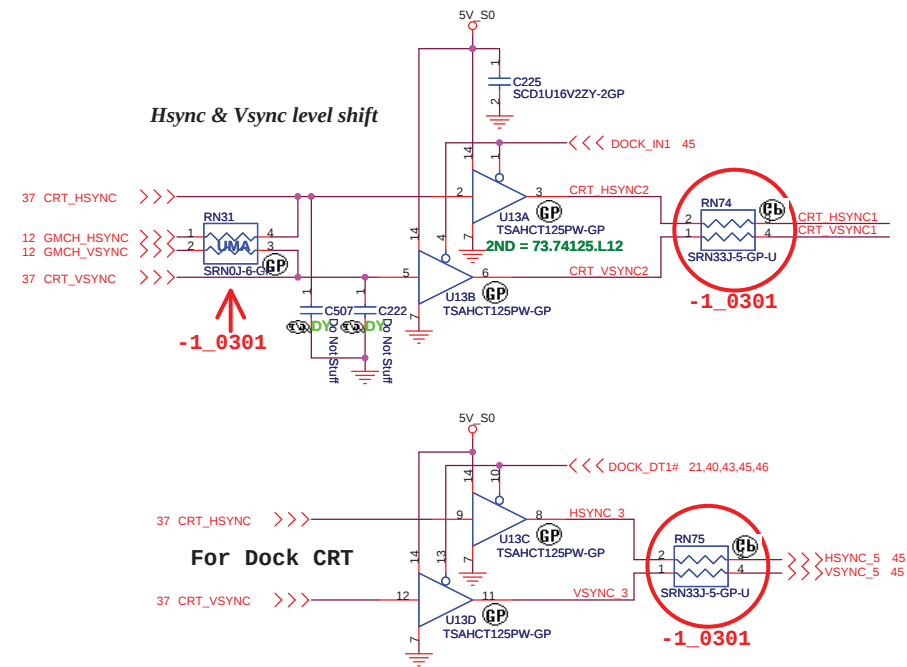


2ND = 68.00119.081

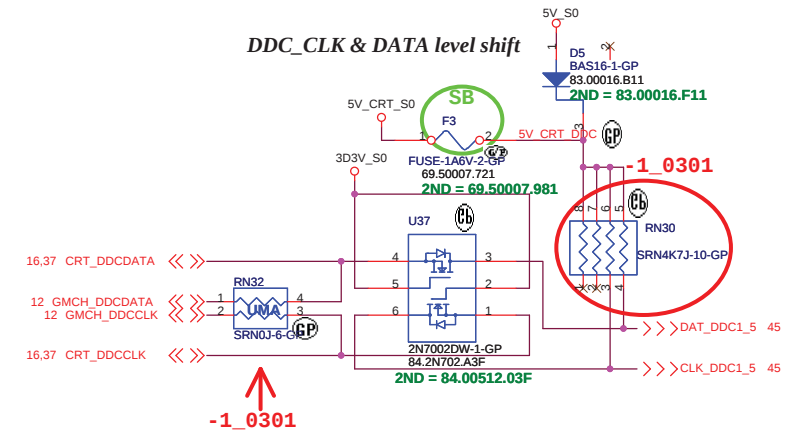
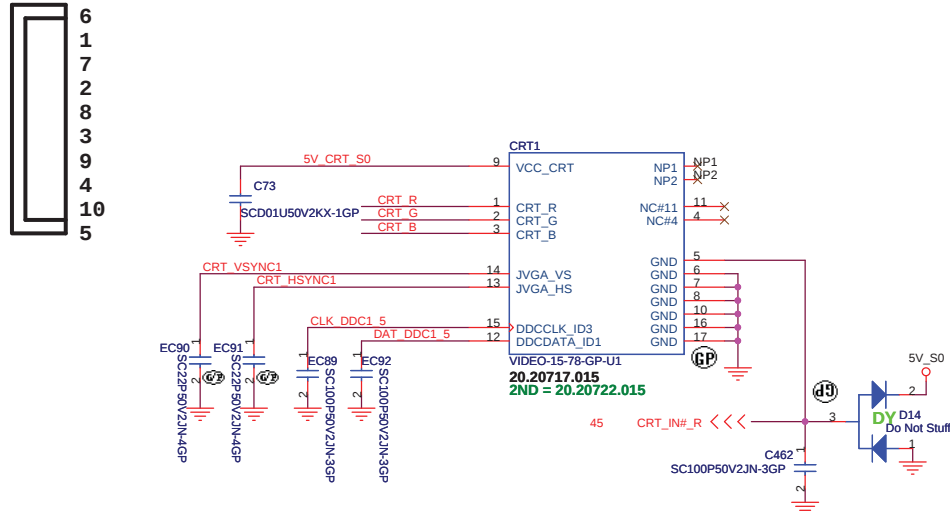
2ND = 68.00119.081

$2ND = 68.001$

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT
CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.*



CRT I/F & CONNECTOR



UMA NODOCK

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Connector

Size

Document Number

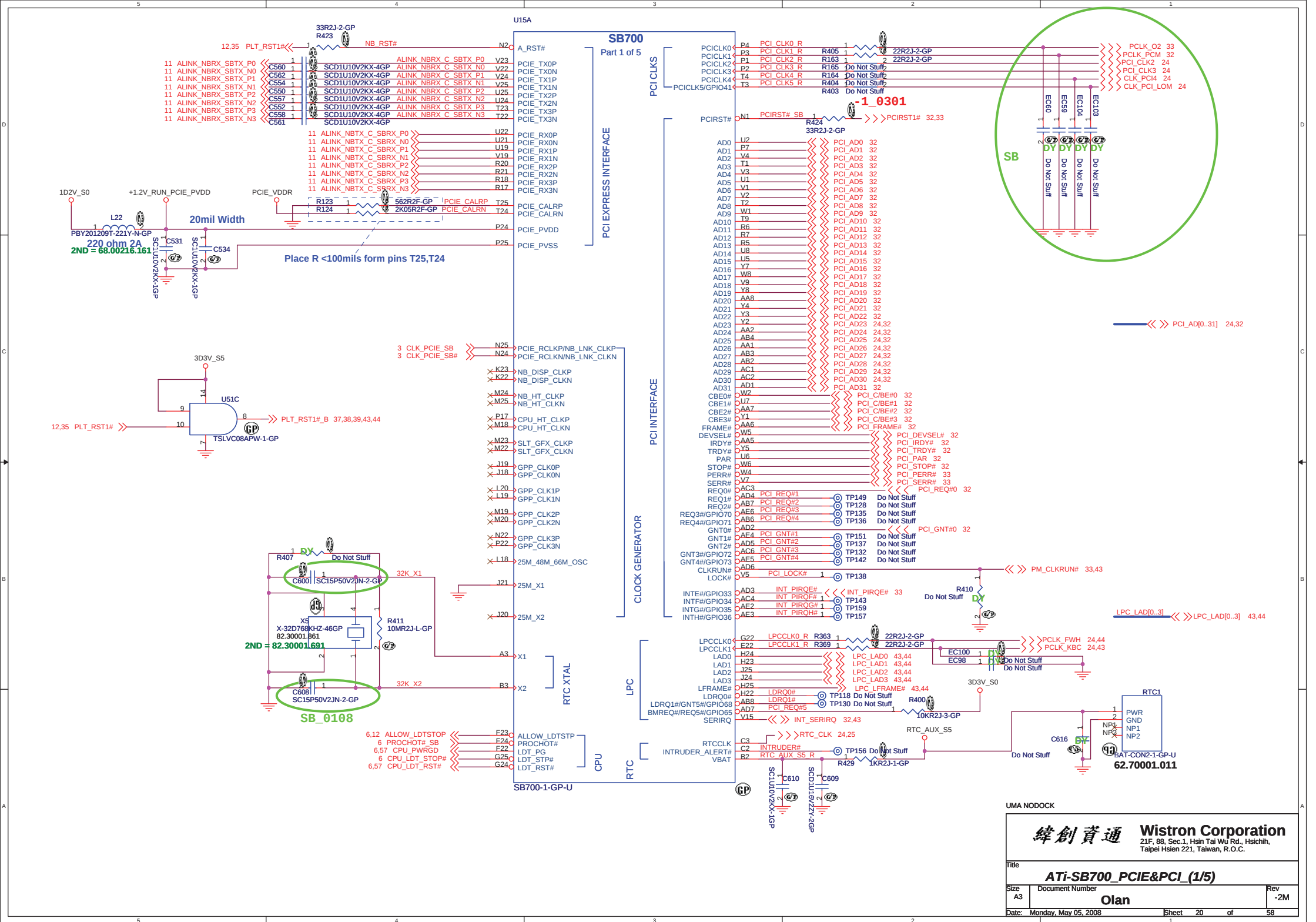
Olan

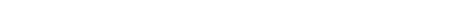
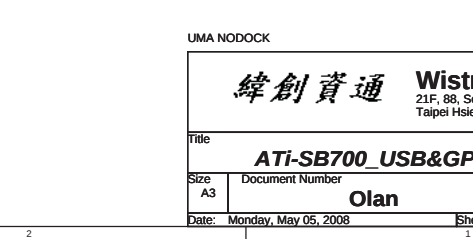
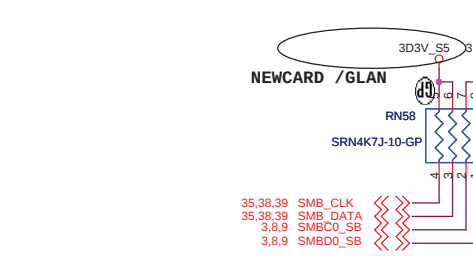
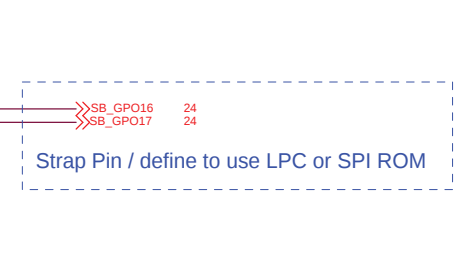
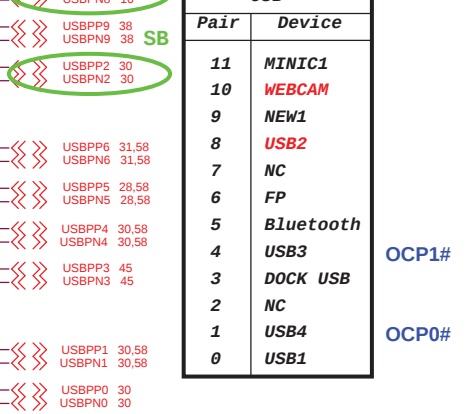
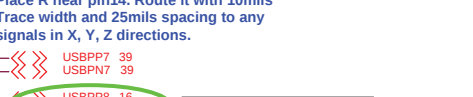
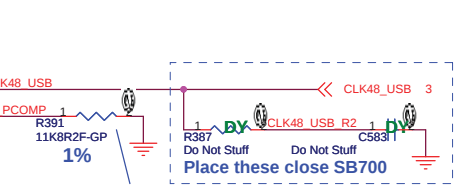
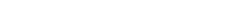
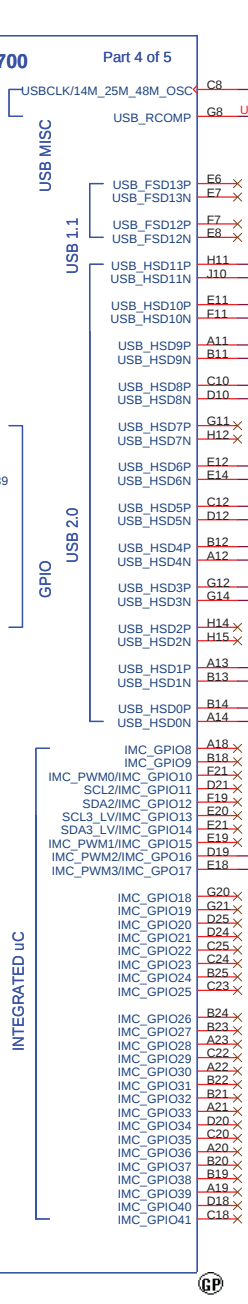
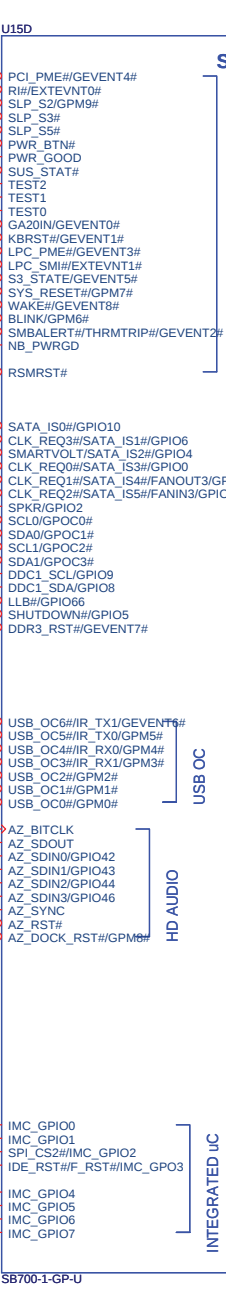
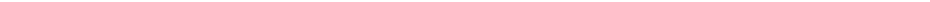
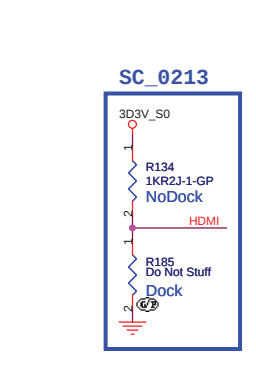
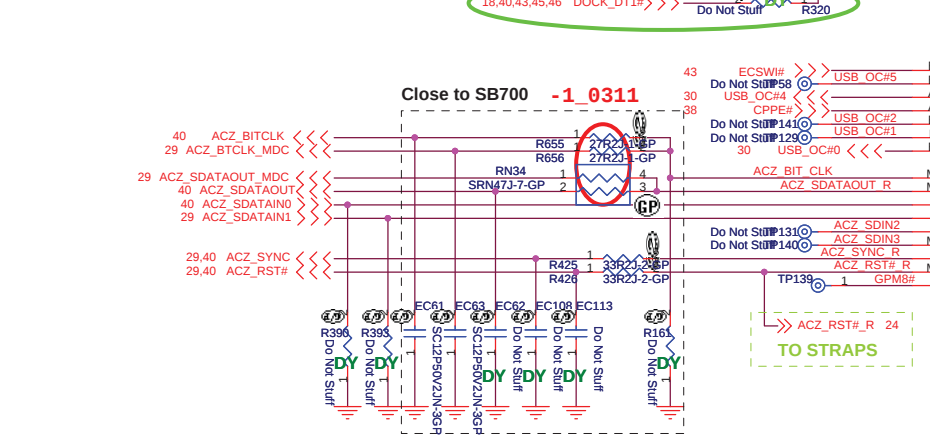
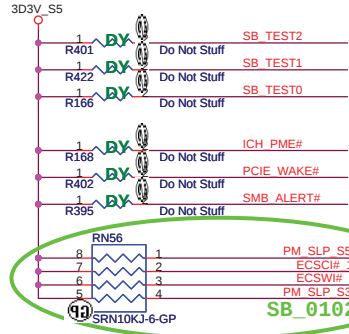
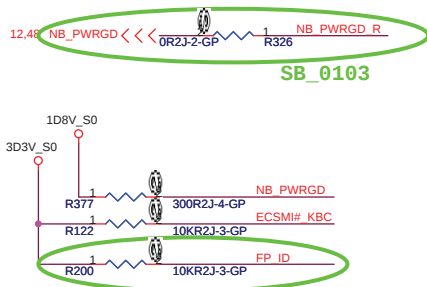
Date: Monday, May 05, 2008

Sheet 18 of 58

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-2M





USB	
Pair	Device
11	MINIC1
10	WEBCAM
9	NEW1
8	USB2
7	NC
6	FP
5	Bluetooth
4	USB3
3	DOCK USB
2	NC
1	USB4
0	USB1

UMA NODOCK	
Pair	Device
11	MINIC1
10	WEBCAM
9	NEW1
8	USB2
7	NC
6	FP
5	Bluetooth
4	USB3
3	DOCK USB
2	NC
1	USB4
0	USB1

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2	NC
1	USB4
0	USB1

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

ATi-SB700_USB&GPIO (2/5)

Size

A3

Document Number

Olan

Date

Monday, May 05, 2008

Sheet

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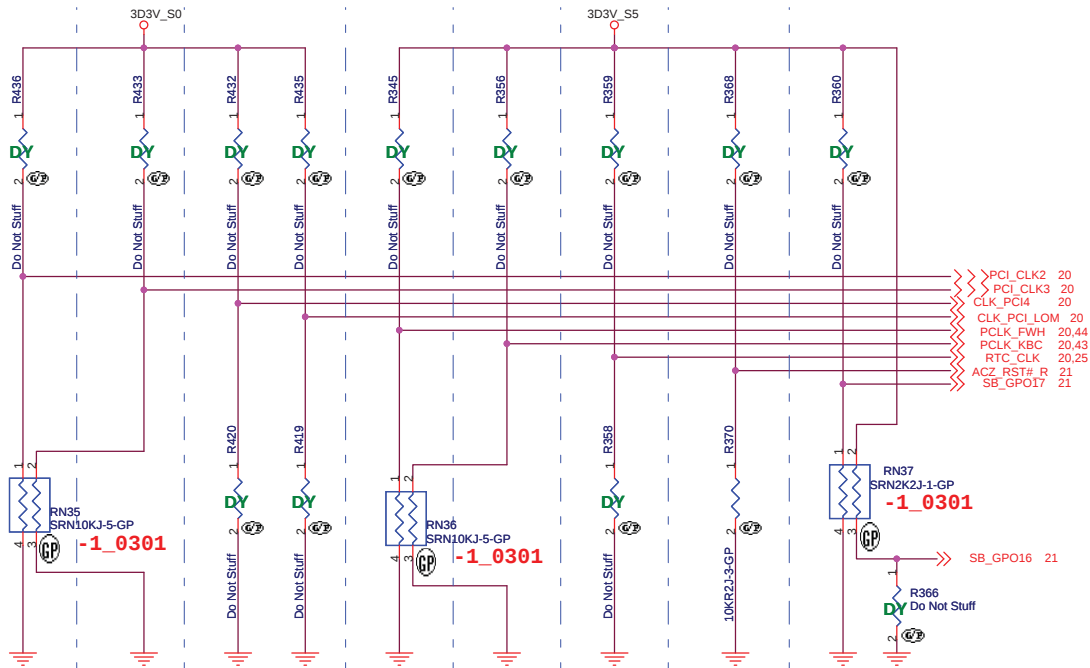
of

58

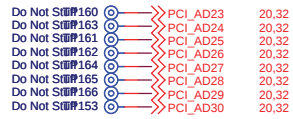
Rev

-2M

REQUIRED STRAPS
REQUIRED SYSTEM STRAPS



DEBUG STRAPS

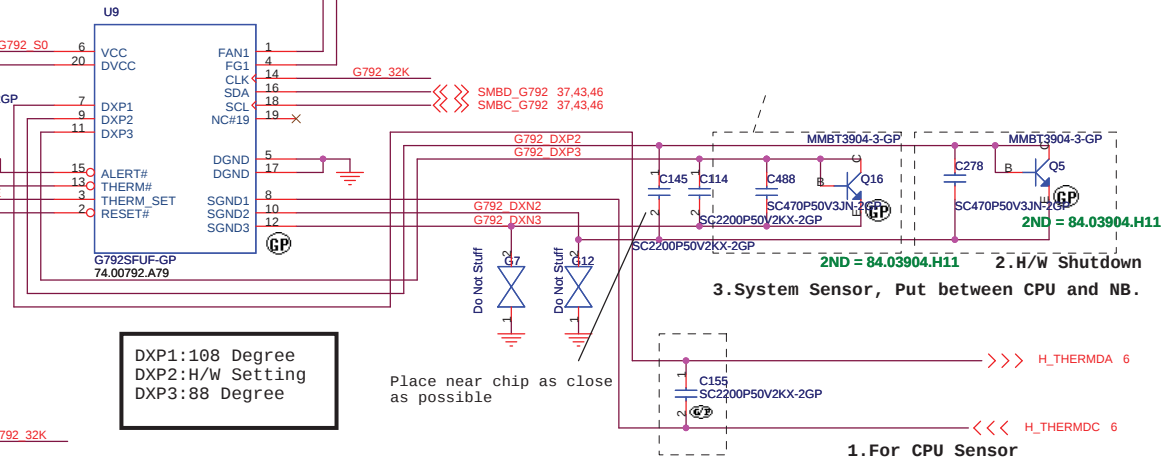
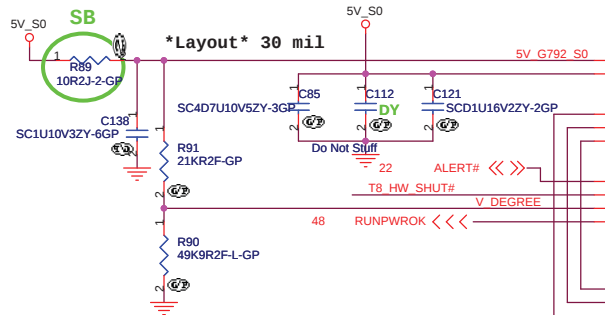
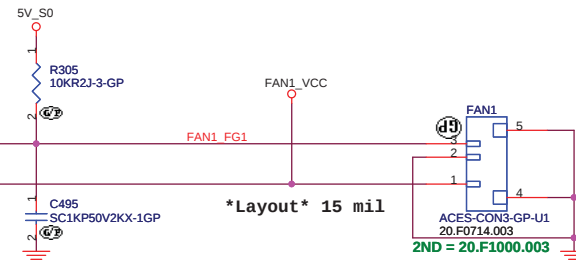
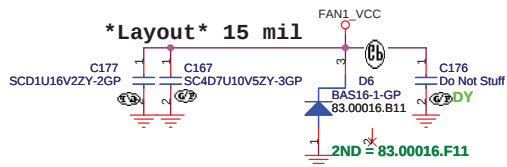


	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

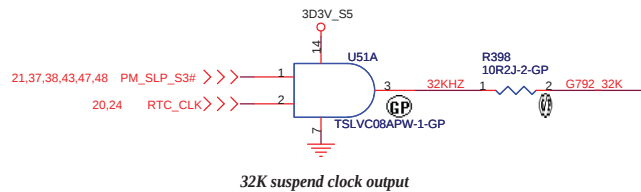
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]



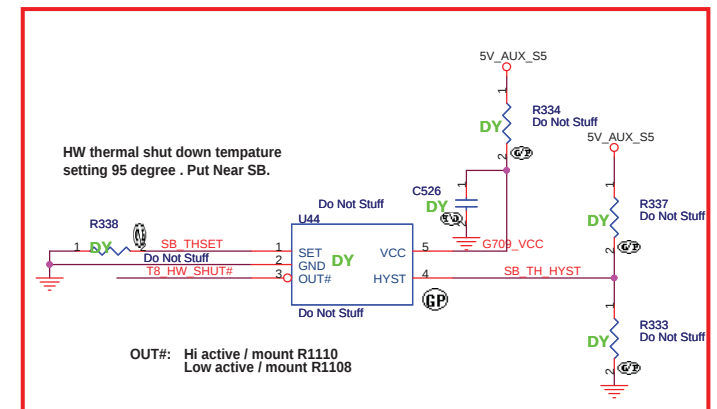
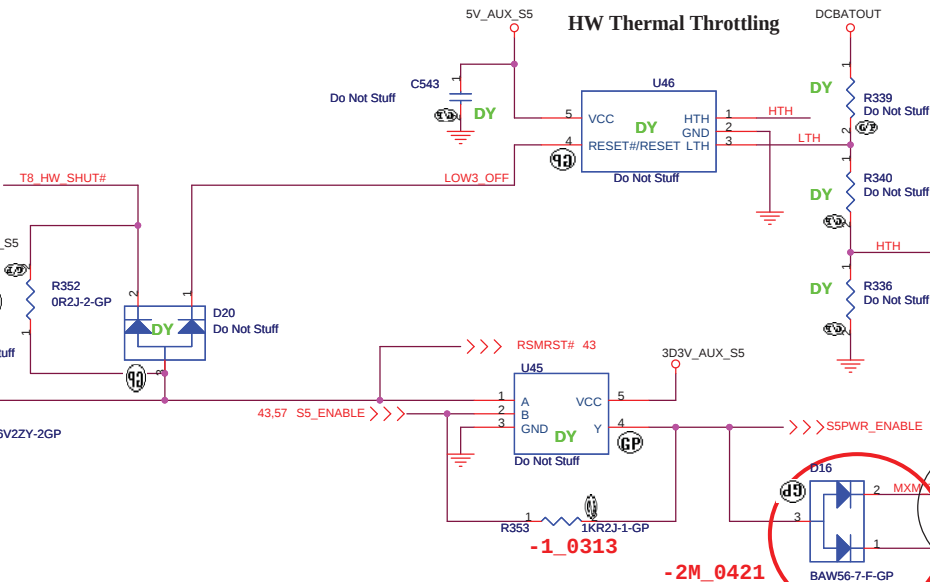
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Place near chip as close as possible



32K suspend clock output

BL3#

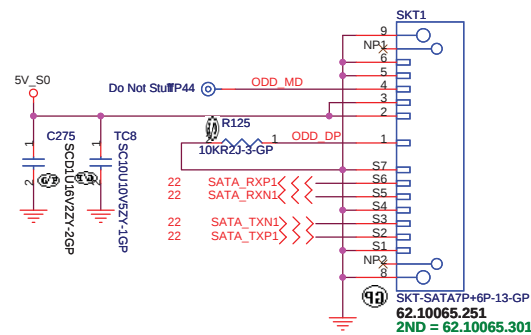


UMA NODOCK

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

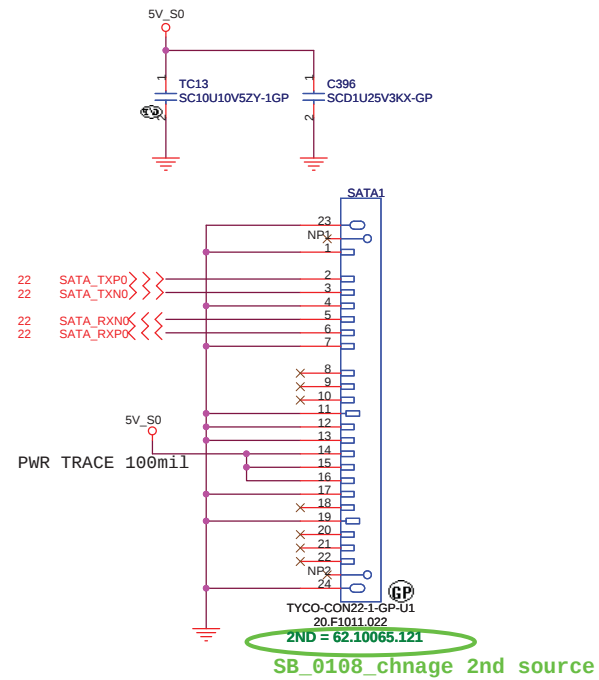
Title			G792	
Size	Document Number	Olan		Rev
A3				-2M
Date: Monday, May 05, 2008		Sheet 25 of 58		

ODD Connector



-1_0305

SATA HDD Connector

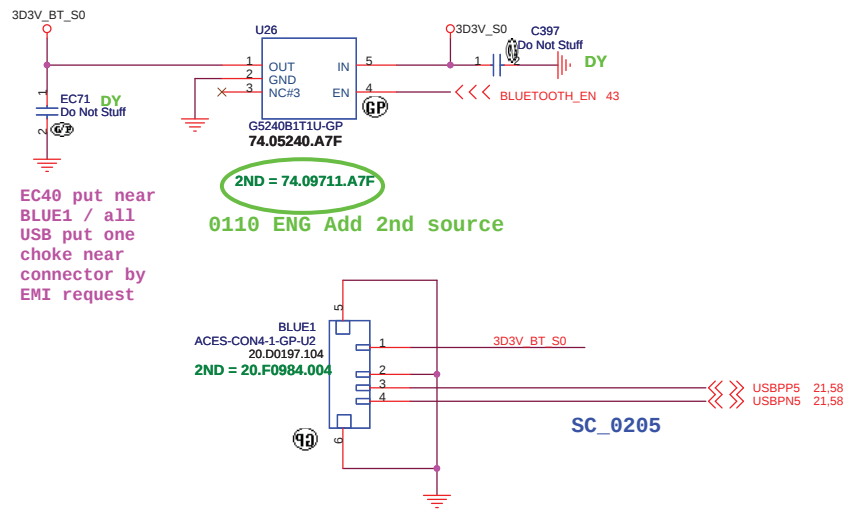


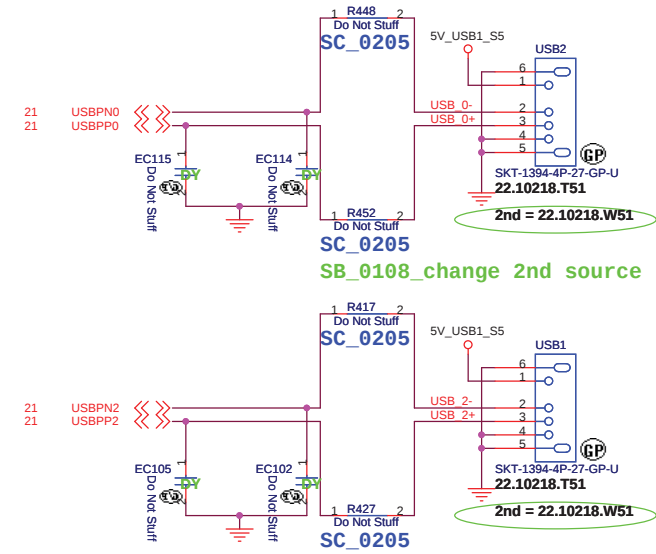
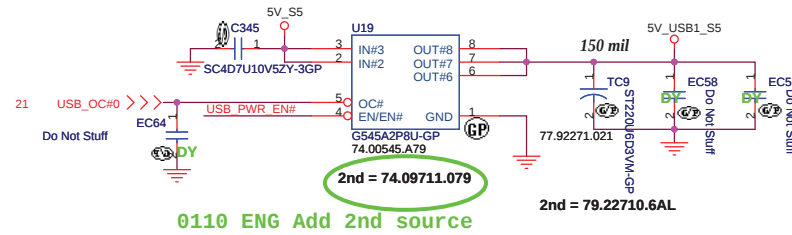
UMA NODOCK

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Taipei Hsien 221, Taiwan, R.O.C.

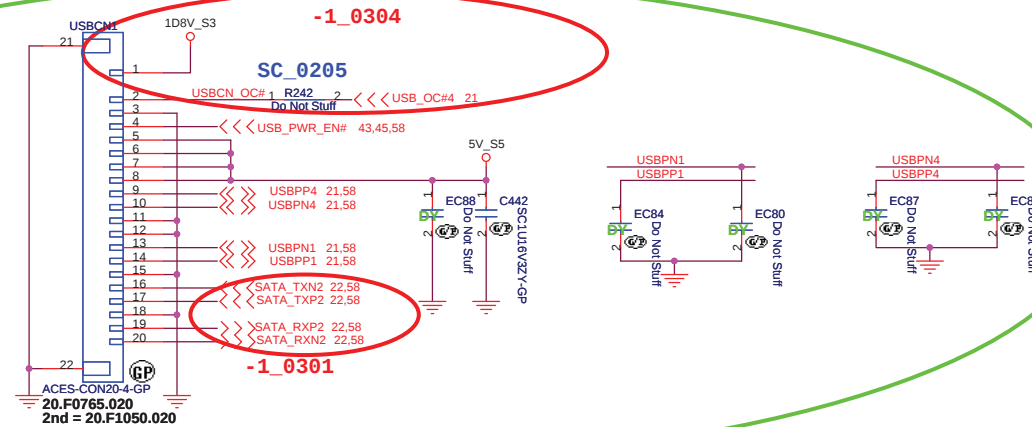
Title		
HDD		
Size	Document Number	Rev
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Date:	Friday, April 18, 2008	Sheet 27 of 58

BLUETOOTH MODULE





SB_0102



58 USB_OC# <<< USB_OC#

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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB

Size

Document Number

Olan

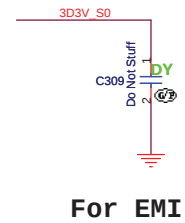
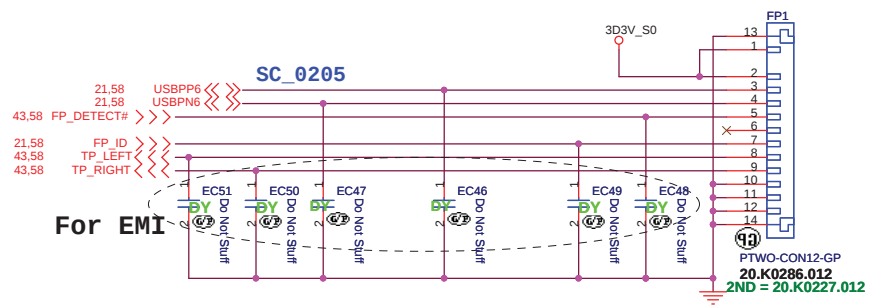
Rev

-2M

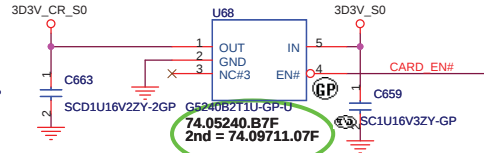
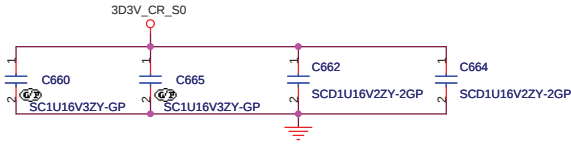
Date: Monday, May 05, 2008

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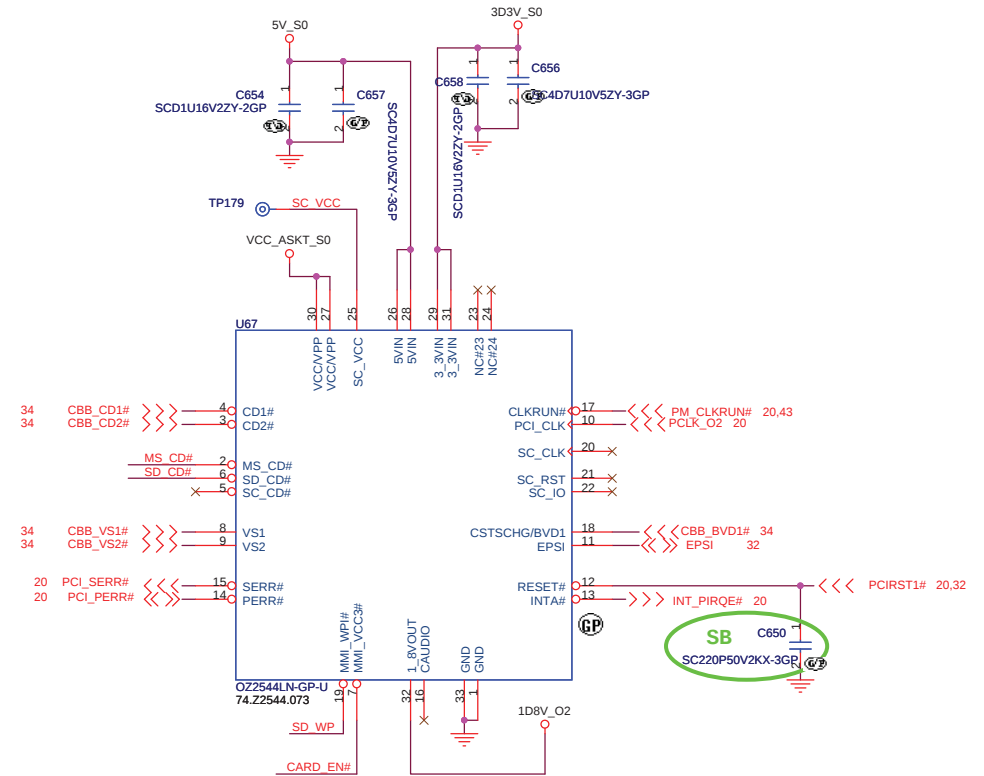
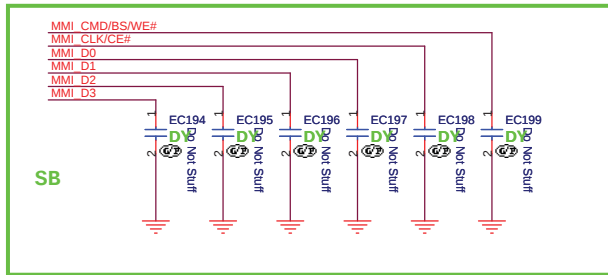
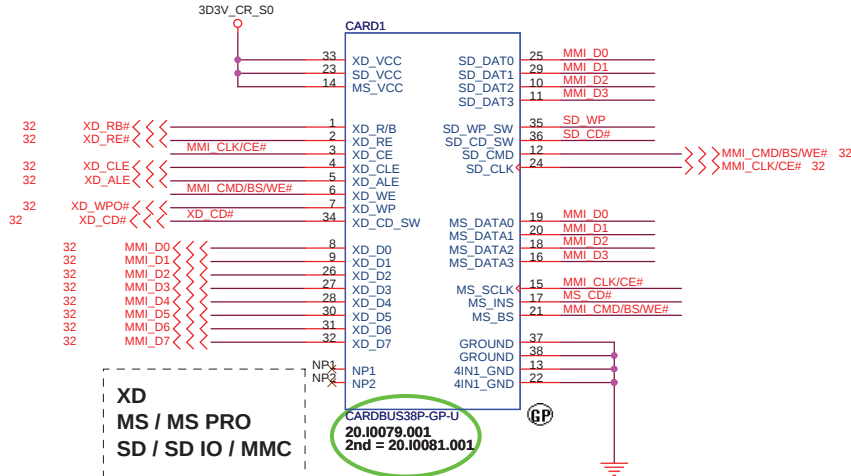
Finger printer







ENG Add 2nd source



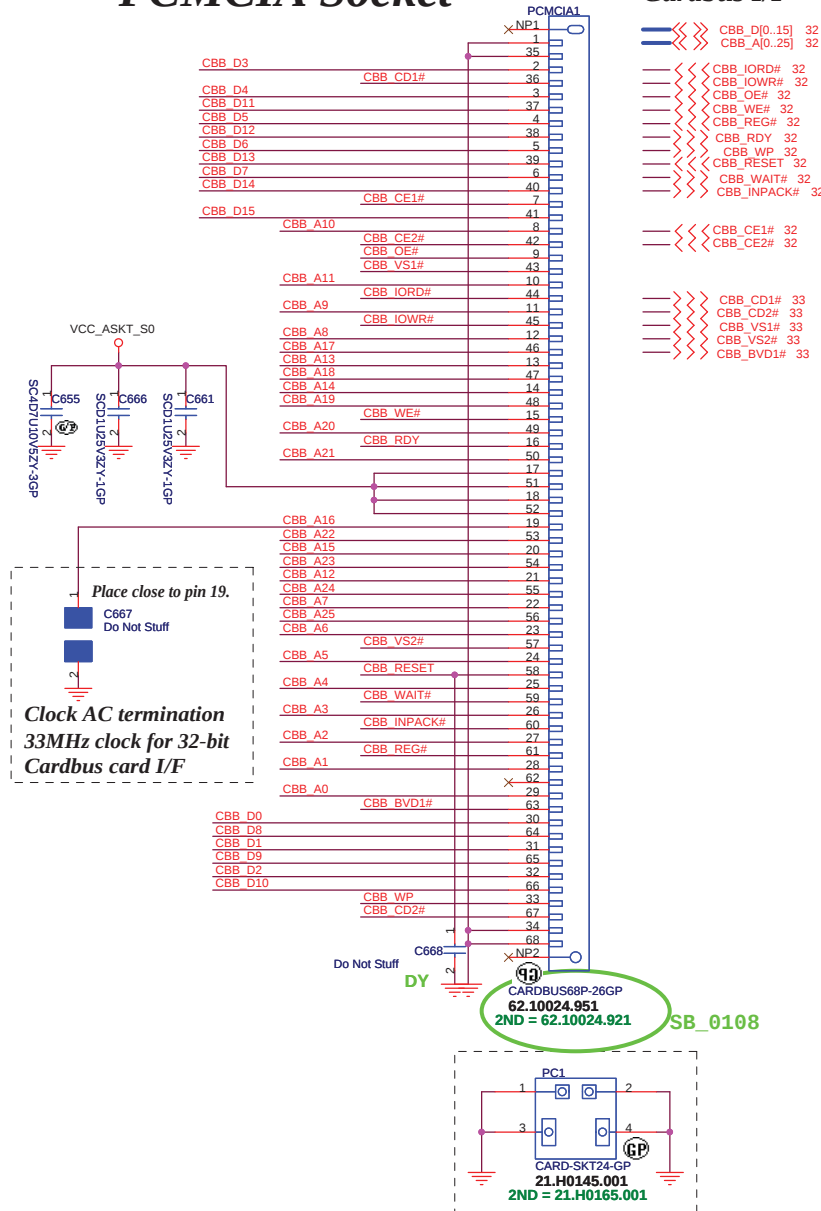
UMA NODOCK

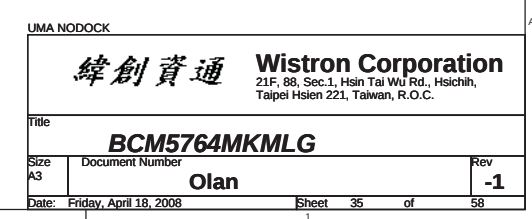
緯創資通 Wistron Corporation
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Title		
Card Reader Connector		
Size	Document Number	Rev
A3		-1
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PCMCIA Socket

Cardbus I/F





- A

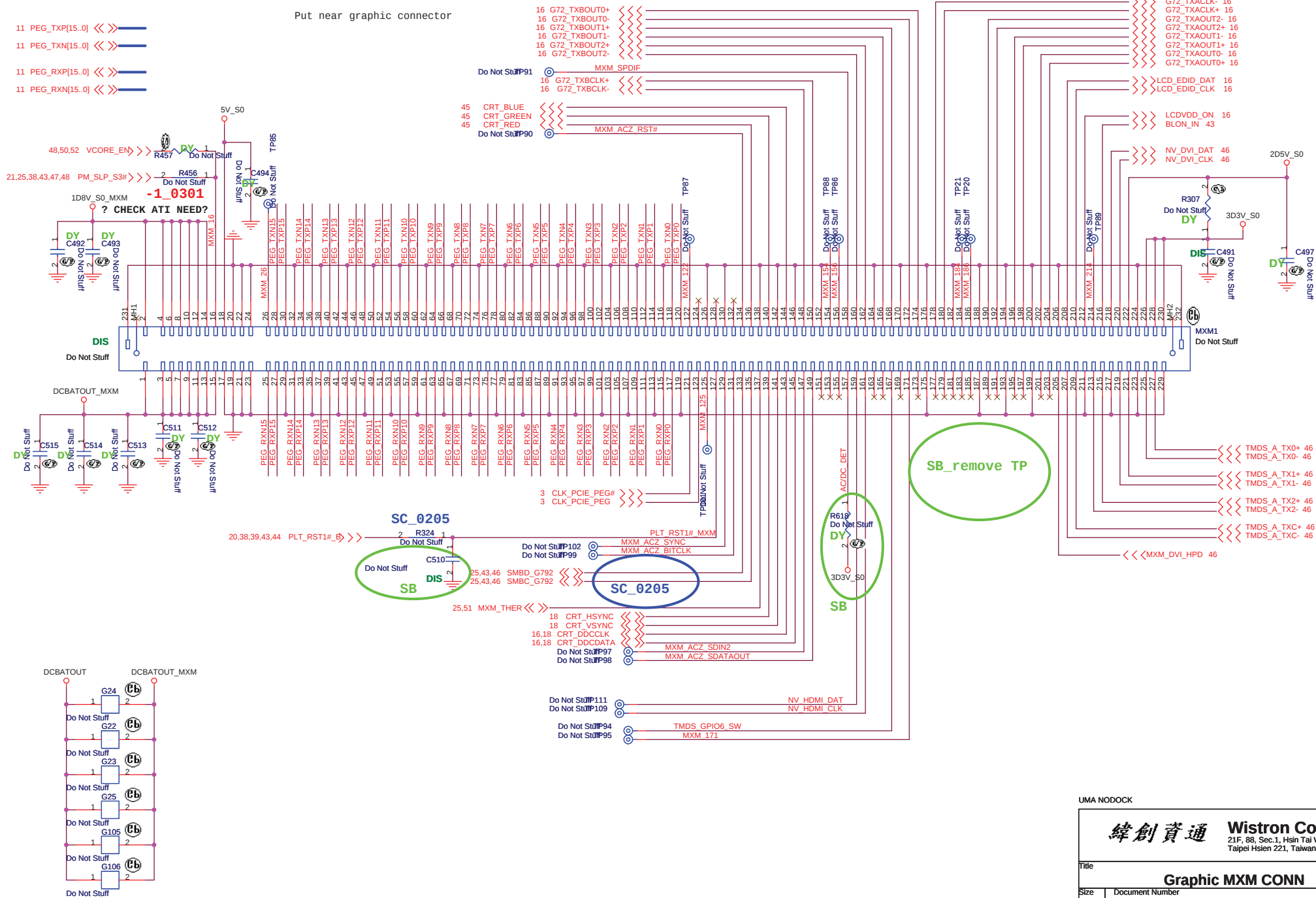
1



1



NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS



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Title

Graphic MXM CONN

Size

Document Number	
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Olan

Date: Friday, April 18, 2008

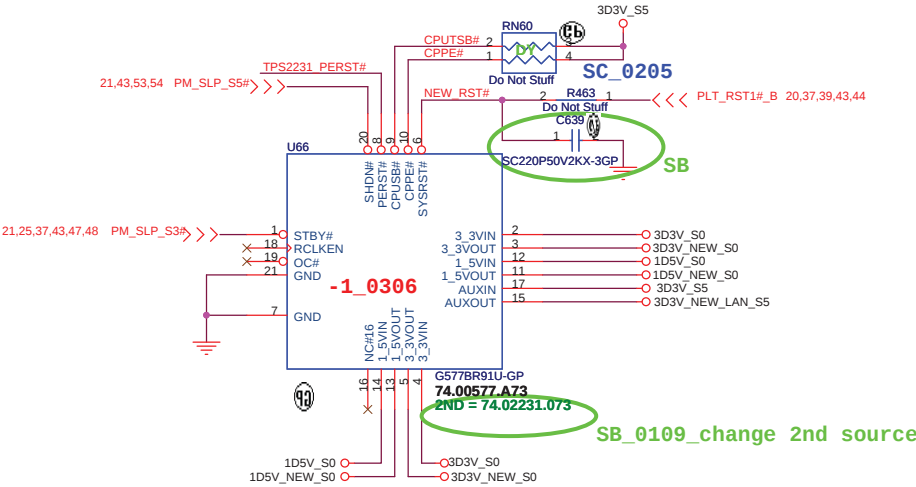
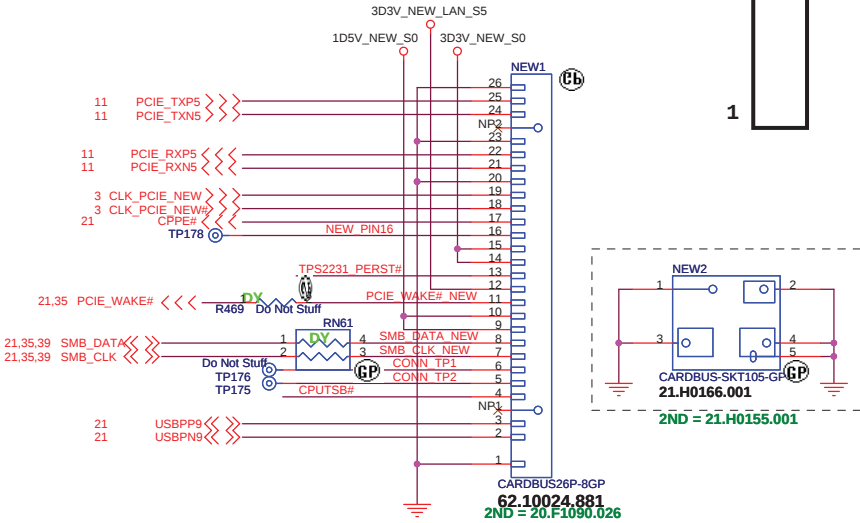
Sheet 37 of 58

Rev

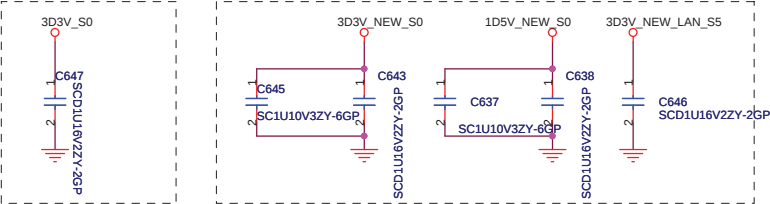
NEWCARD Connector

Reserve the symbol
for bottom side
connector

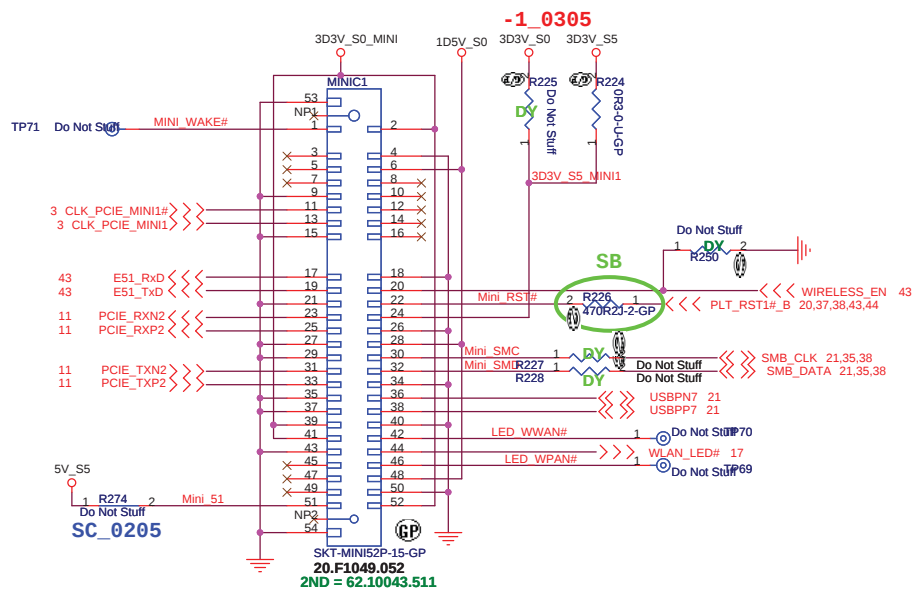
TOP VIEW



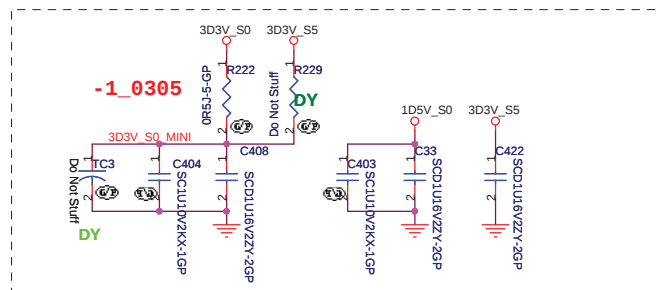
Place them Near to ChipPlace them Near to Connector



Mini Card Connector(WLAN)



Place near MINIC1



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Title

Mini Card

Size
A3

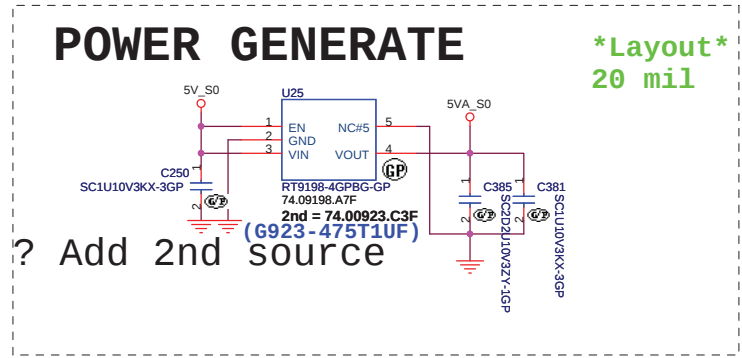
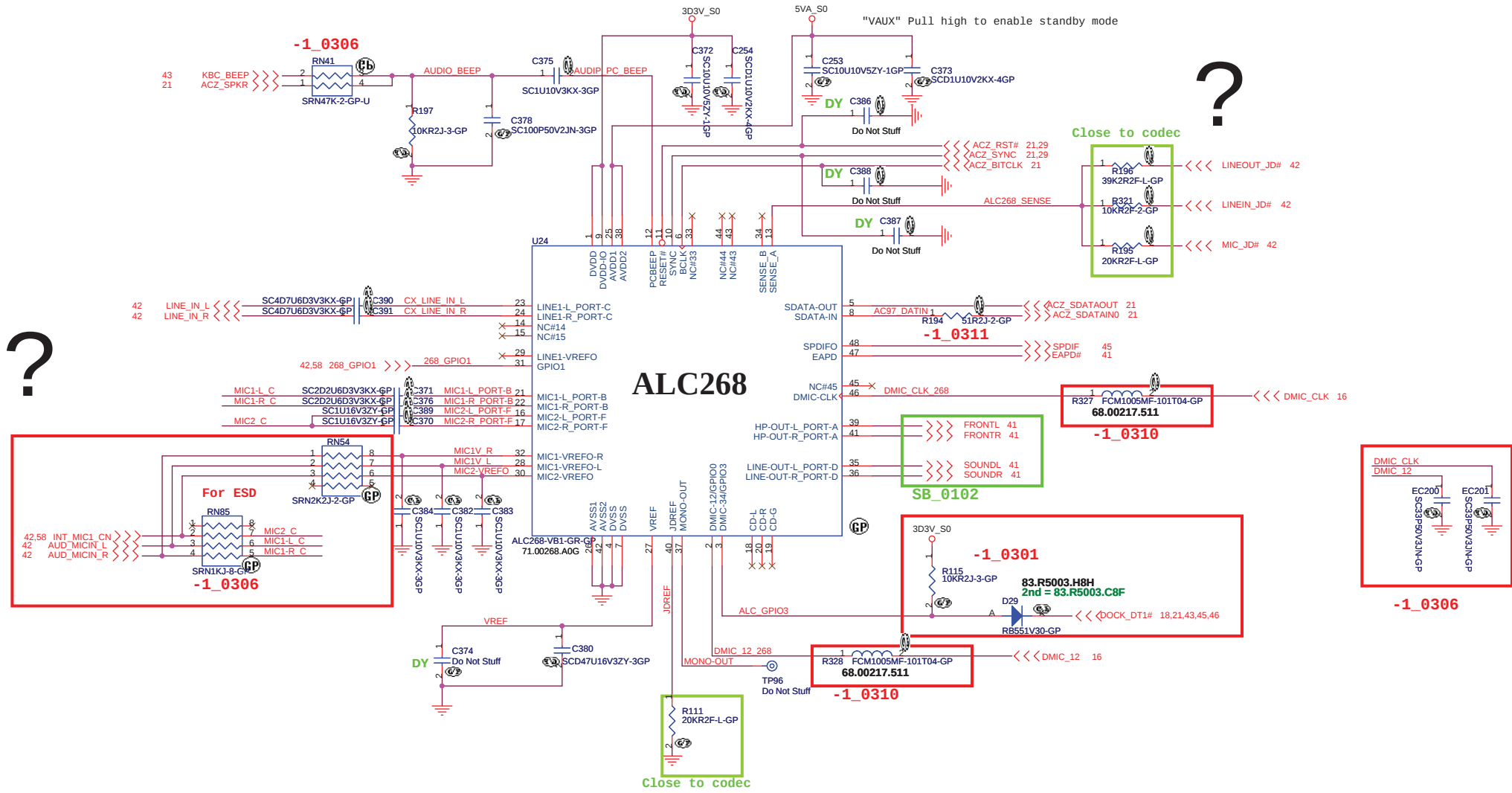
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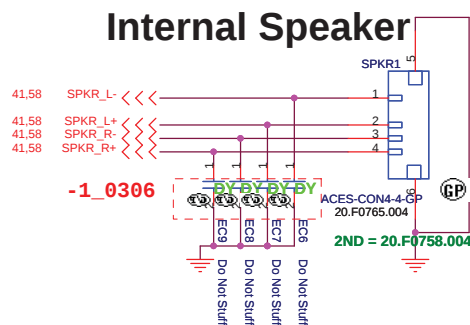
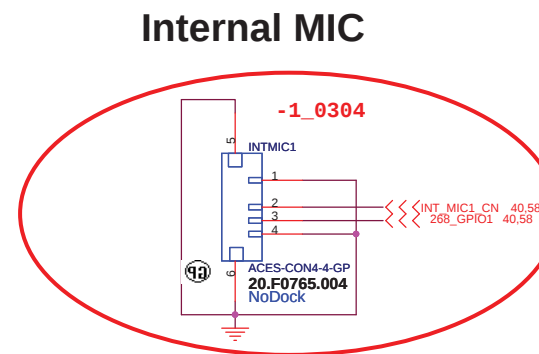
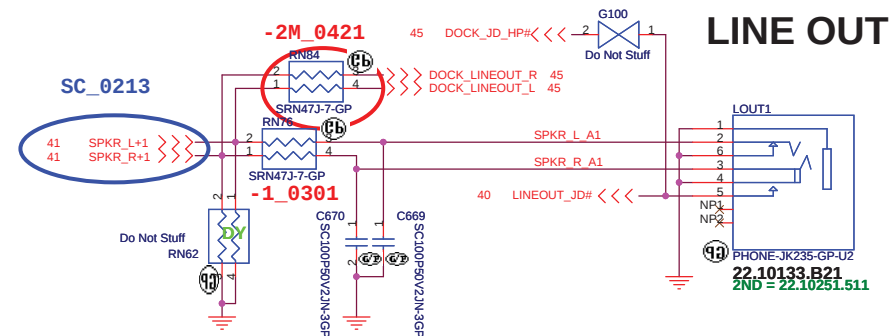
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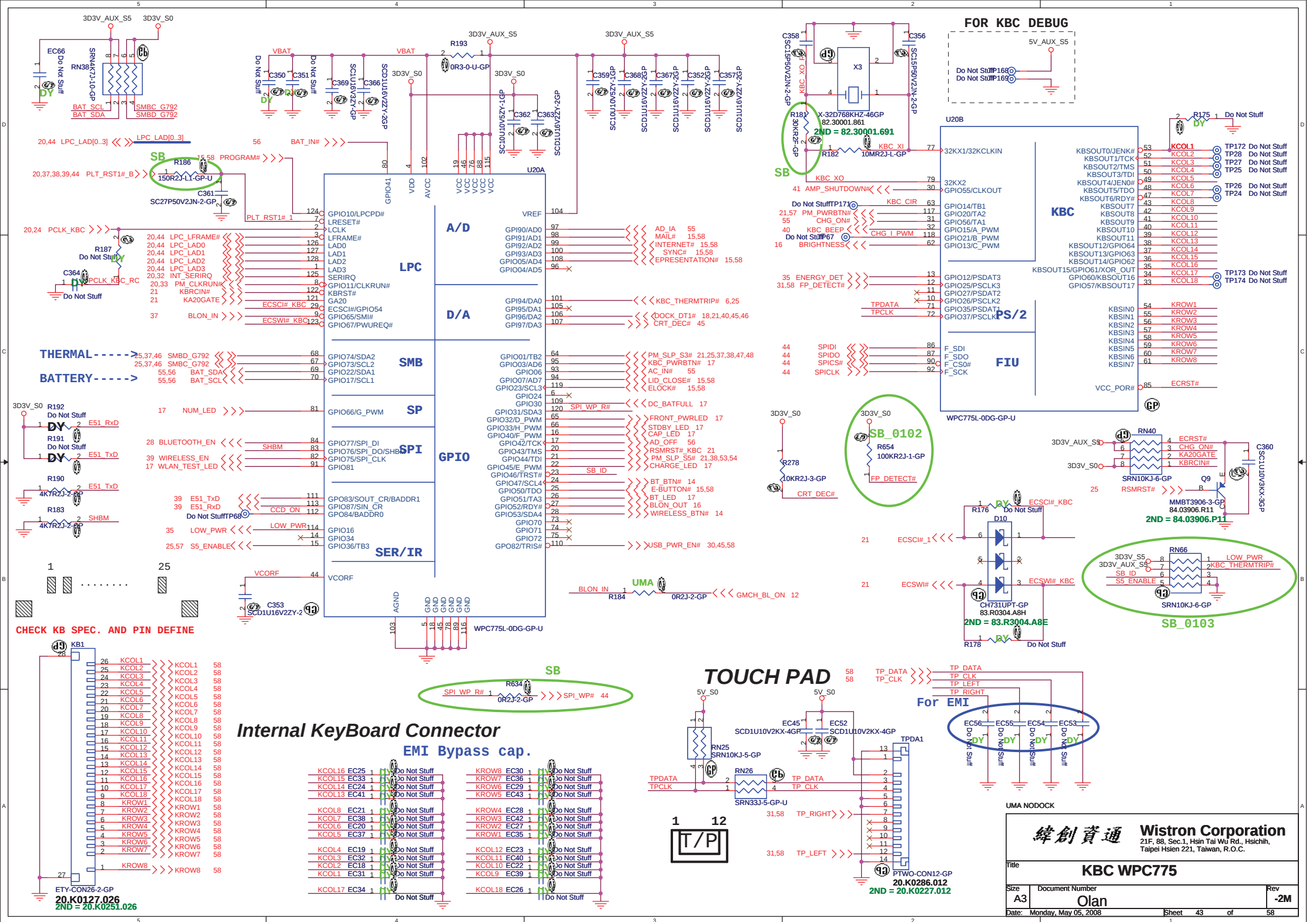
Rev	-1
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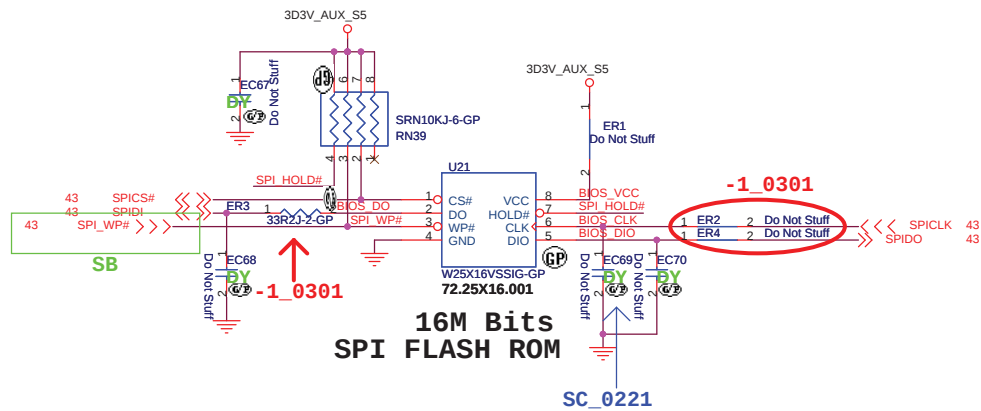
Date: Friday, April 18, 2008

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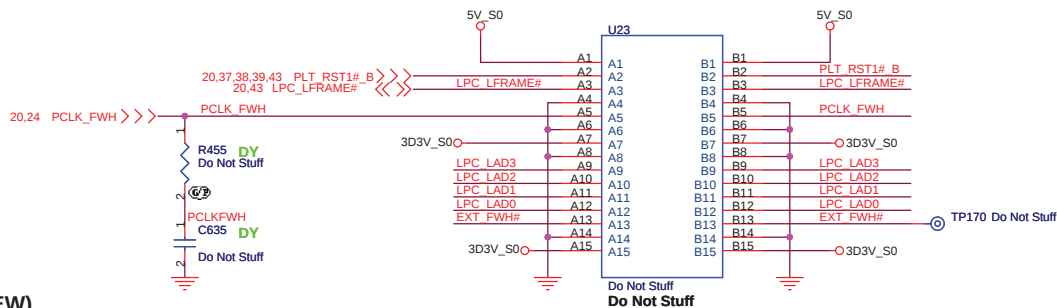
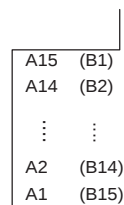




20,43 LPC_LAD[0..3] <<>> LPC_LAD[0..3]

GOLDEN FINGER FOR DEBUG BOARD

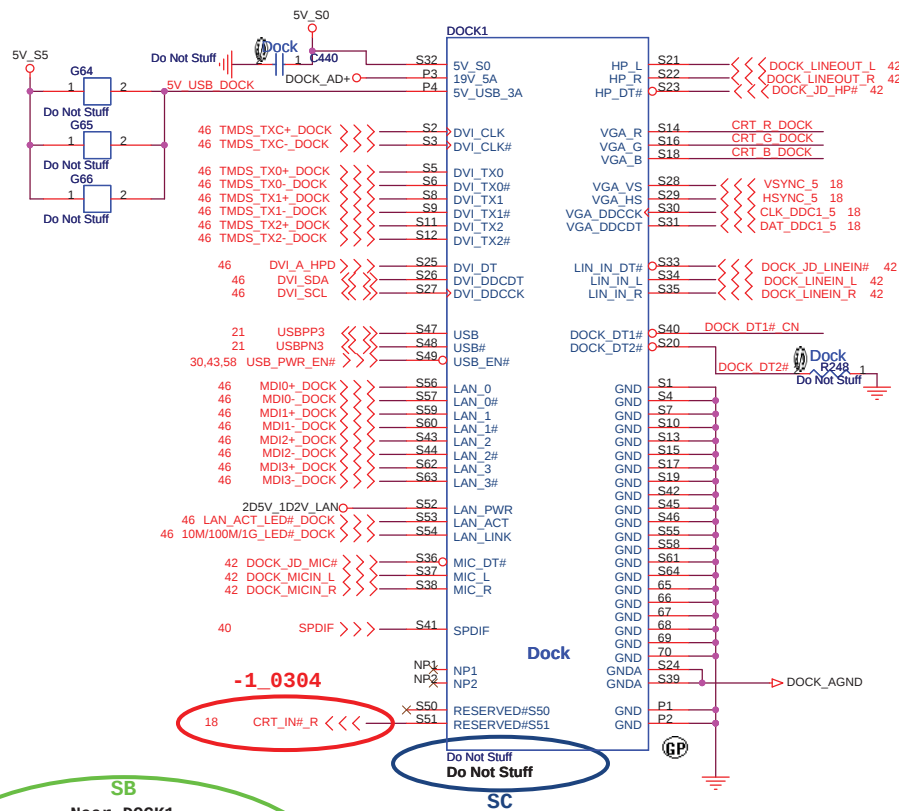
TOP VIEW



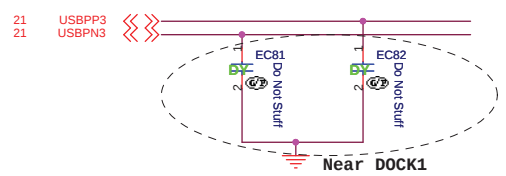
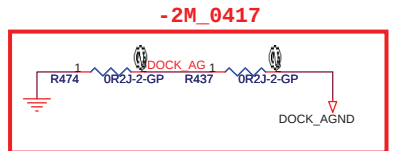
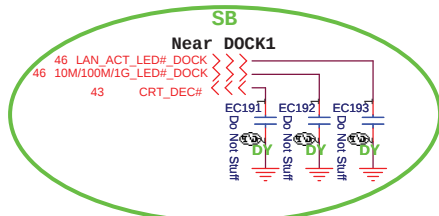
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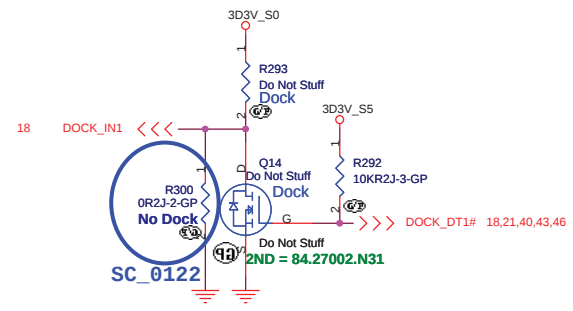
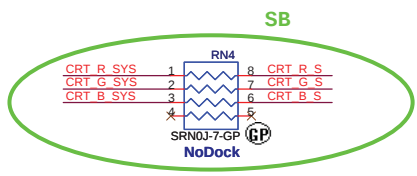
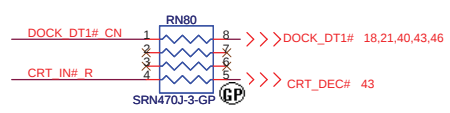
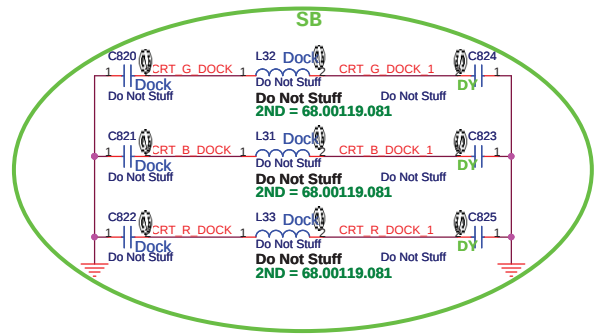
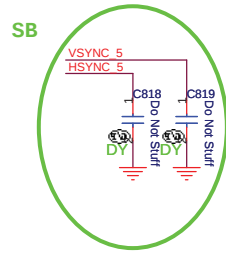
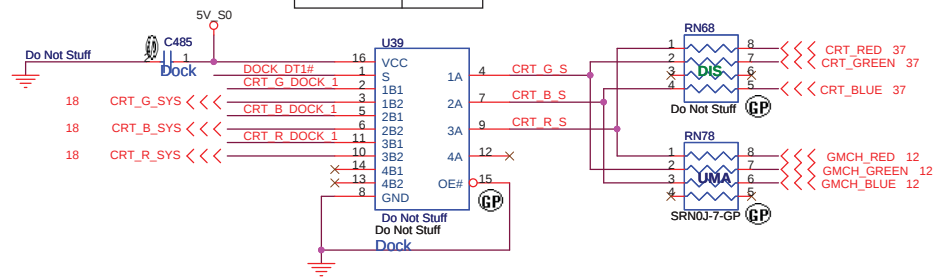
Title			BIOS	
Size	Document Number	Rev		
A3		Olan		-2M
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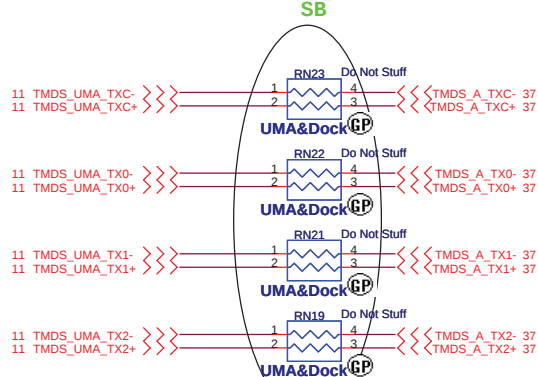
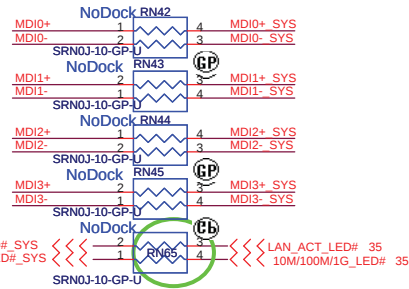
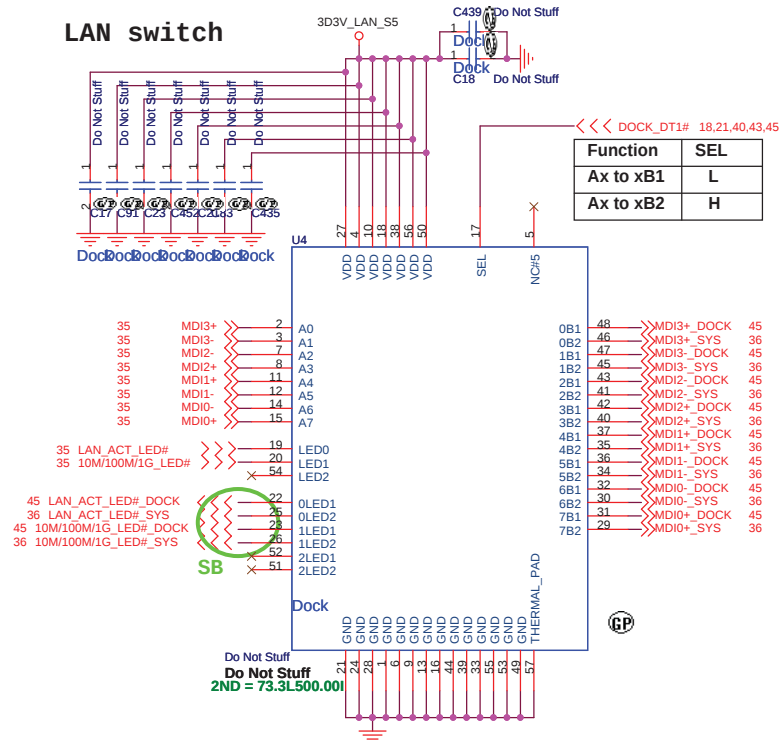
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18 CRT_IN#_R <<<



Function	CRT
SYSTEM	H
DOCK	L

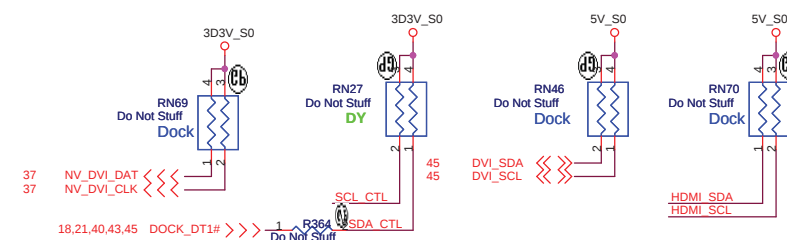
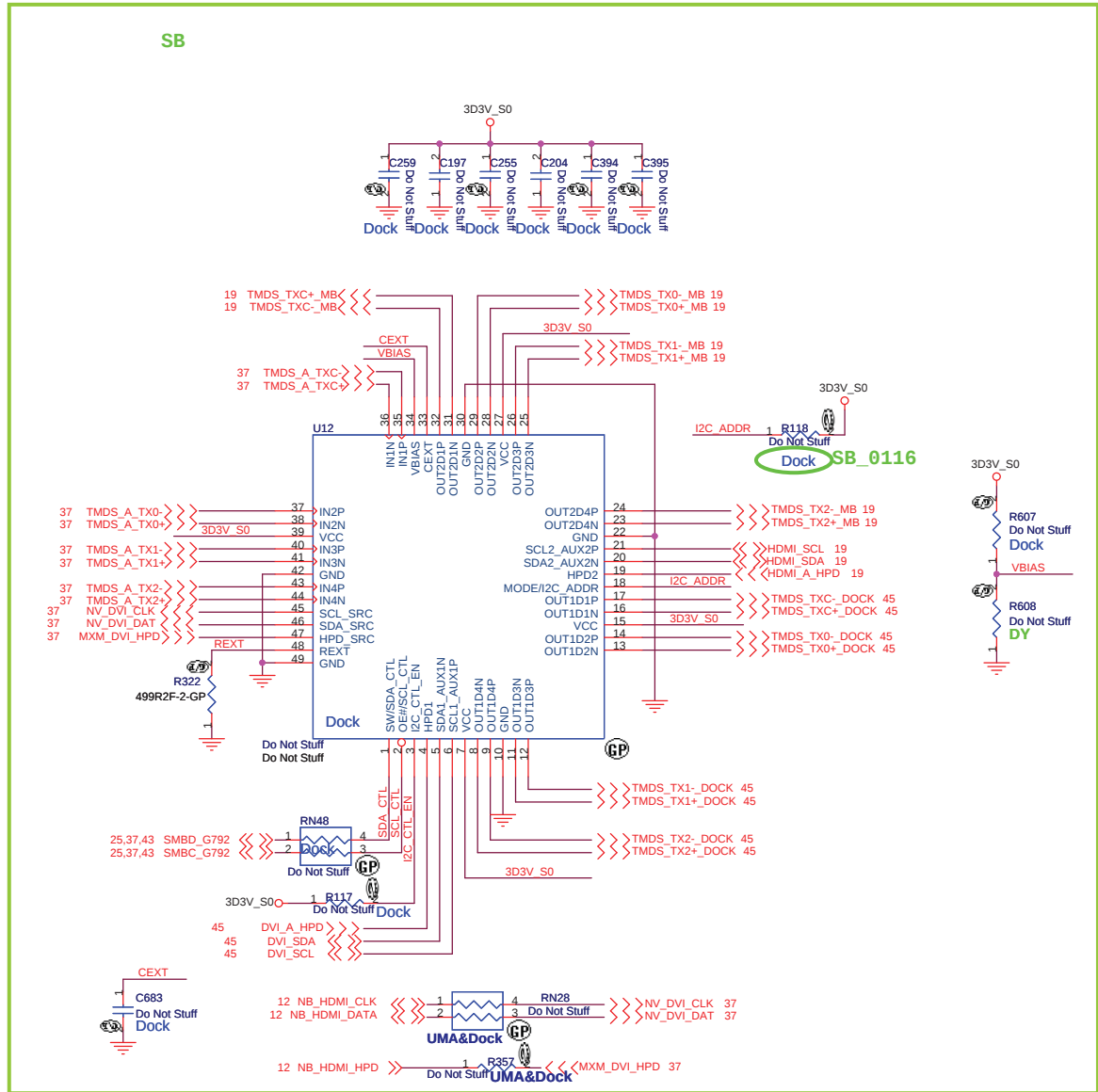


LAN switch



Place Near Switch

SB



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Title

EASY PORT4(2/2)

Size

Document Number

Olan

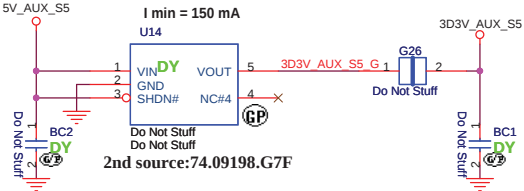
Rev

-1

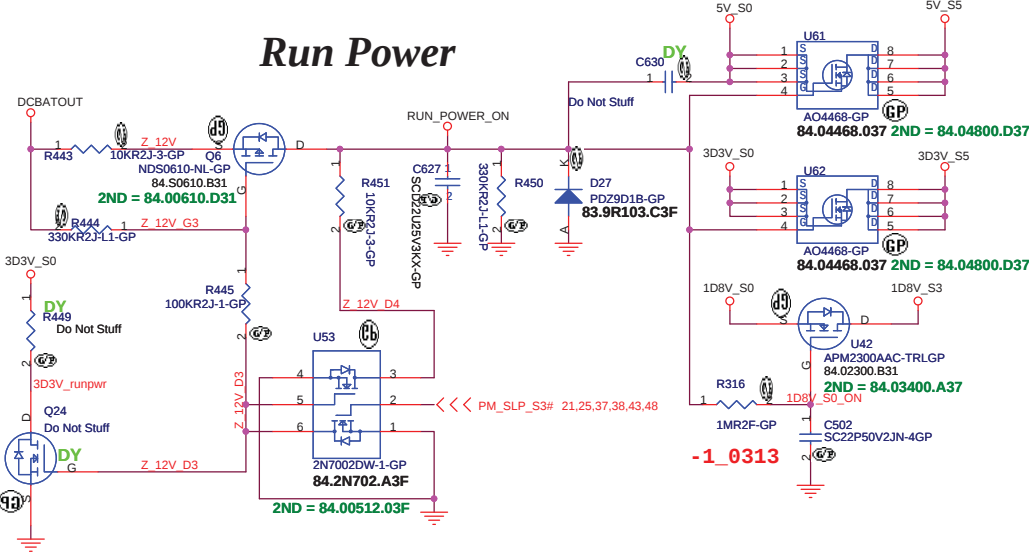
Date: Monday, April 21, 2008

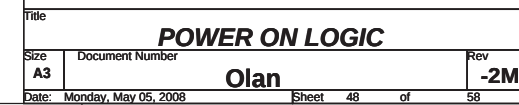
Sheet 46 of 58

Aux Power 3D3V_AUX_S5

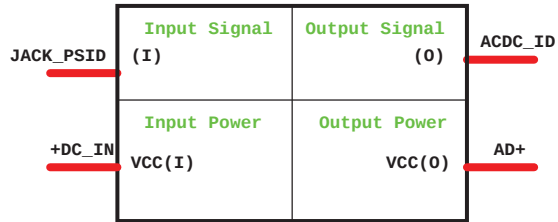


Run Power

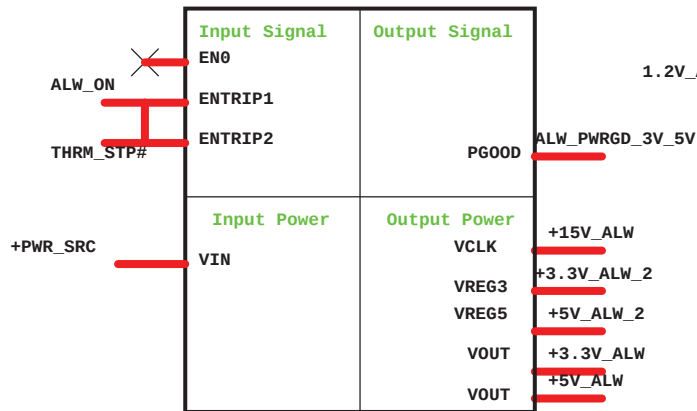




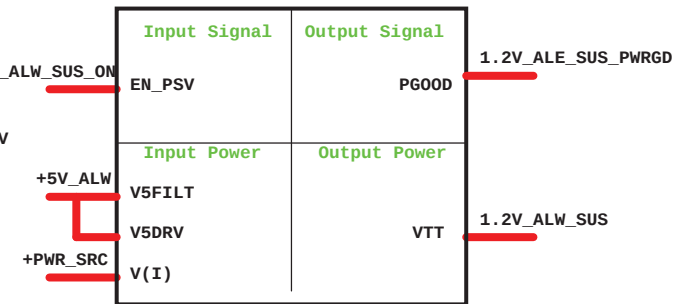
Adapter



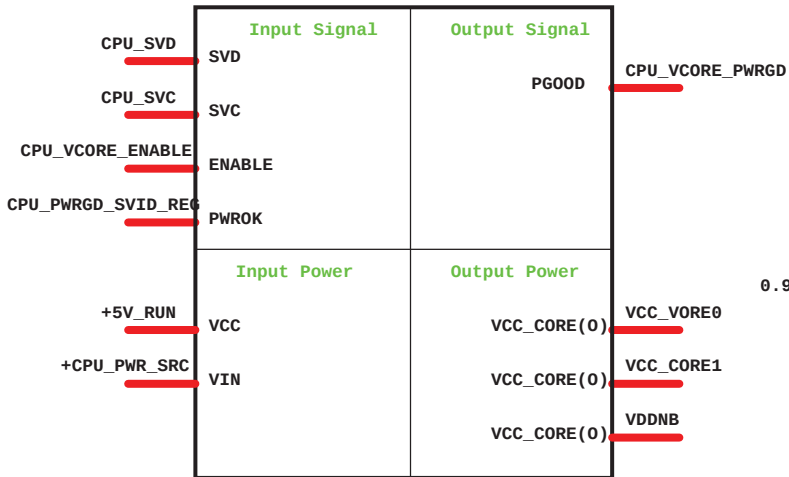
SN0608098



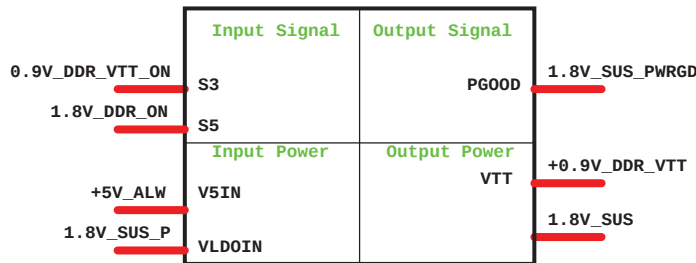
DCDC 1D2V(TPS5117)



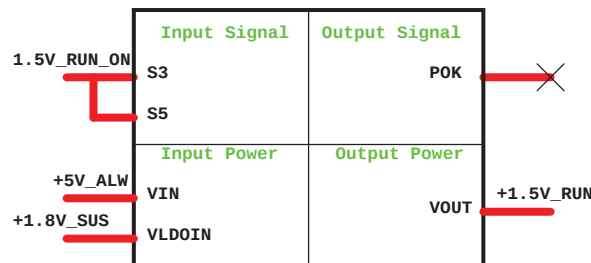
CPU_CORE ISL6265HRTZ



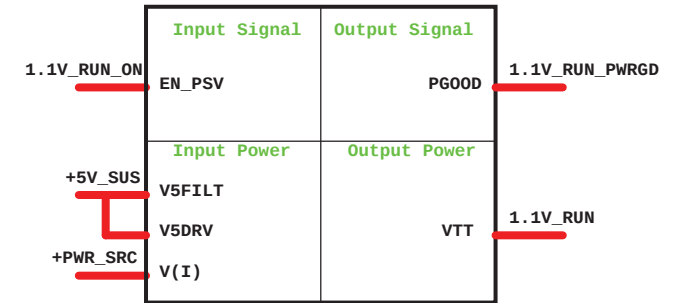
1D8V/0D9V(TPS5116)



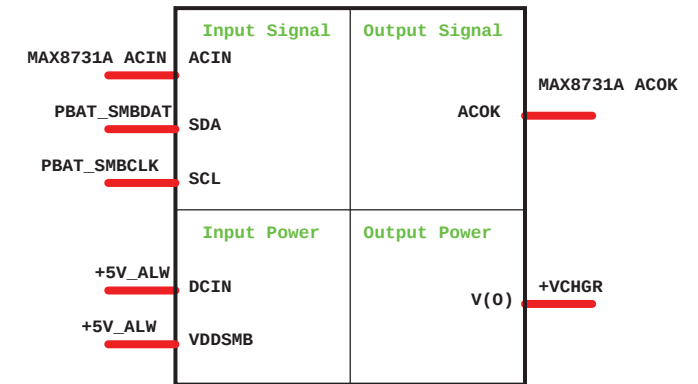
1.5V_LDO



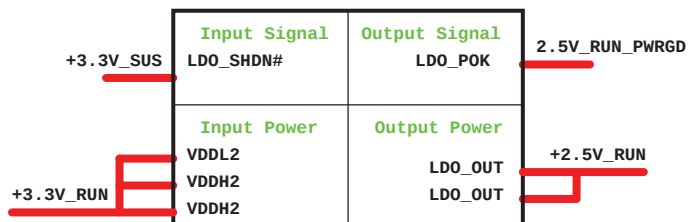
1D1V(TPS5117)



CHARGER BQ24745



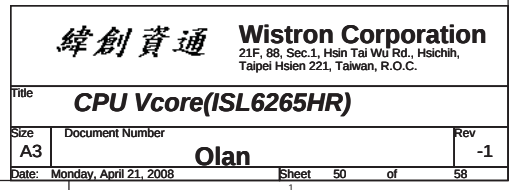
2.5V LDO EMC4002



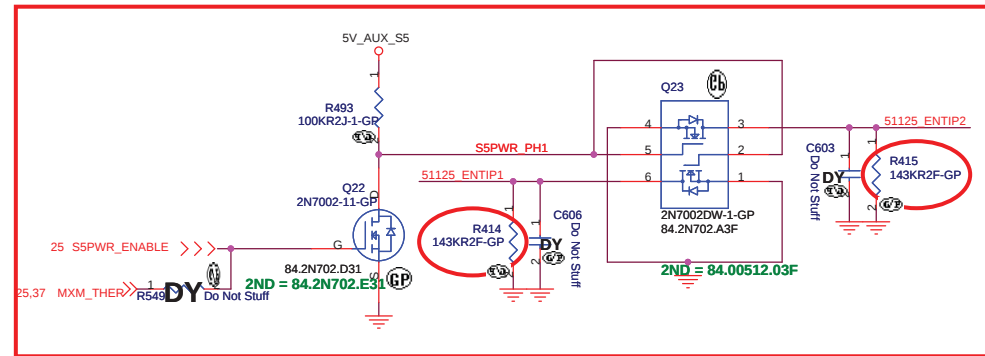
UMA NODOCK

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Taipei Hsien 221, Taiwan, R.O.C.

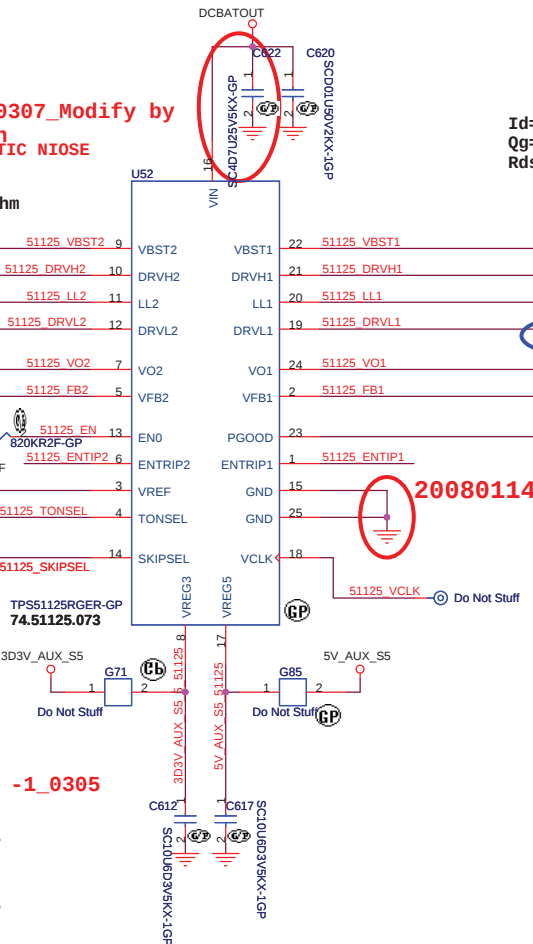
Title Power Block Diagram		
Size A3	Document Number Olan	Rev -1
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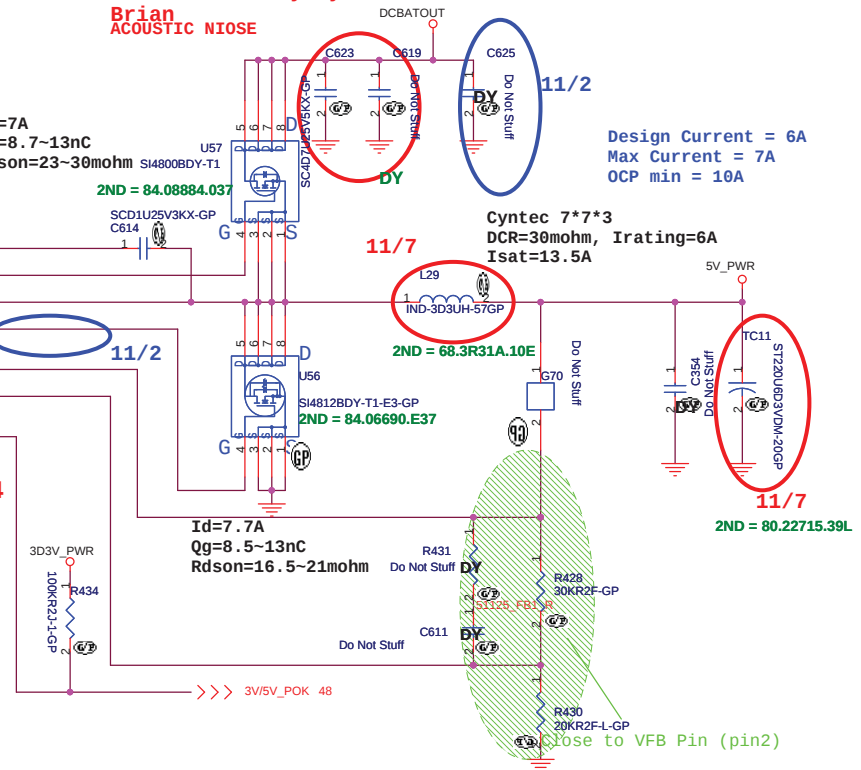
Brian
ACOUSTIC NIOSE



Id=7A
Qg=8.7~13nC
Rdson=23~30mohm



2ND = 84.08884.037



Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A

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Title			
DCDC 5V/3D3V (TPS51125)			
Size	Document Number		Rev
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Date:	Monday, May 05, 2008	Sheet 51 of 58	

20080307_Modify by

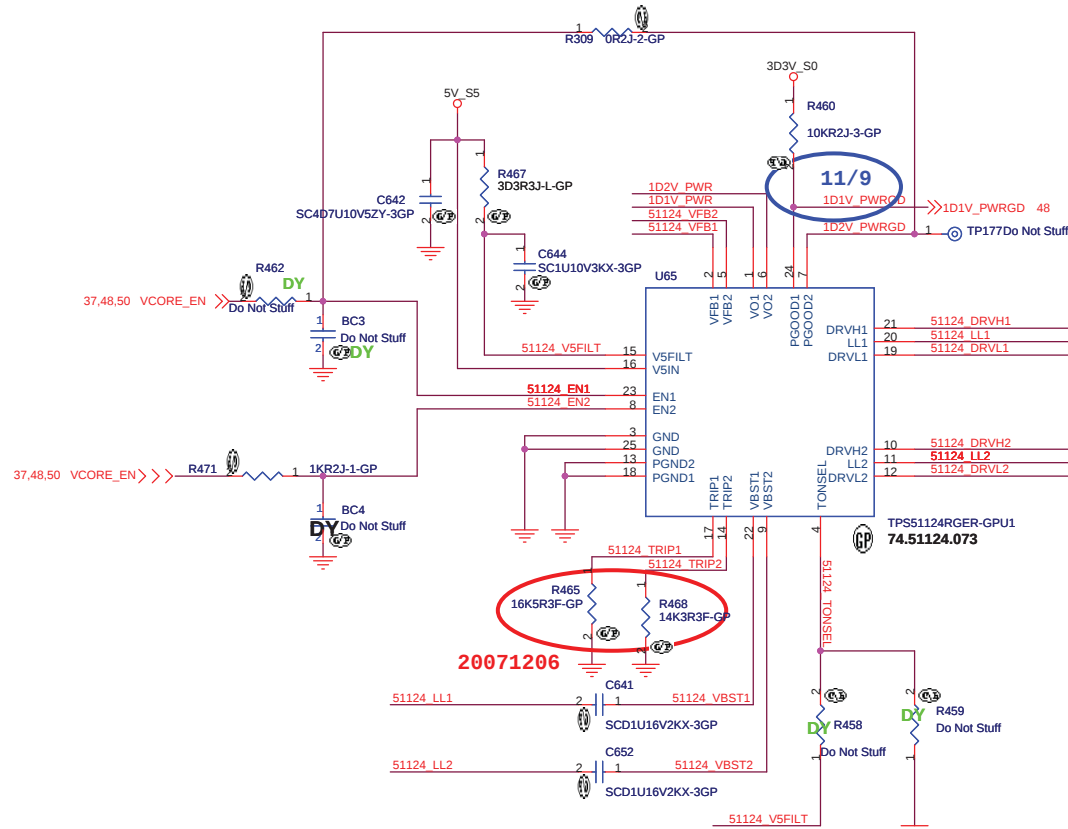
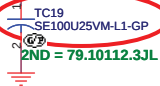
Brian
ACOUSTIC NIOSE

$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out})/V_{in}))$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

-1_0306

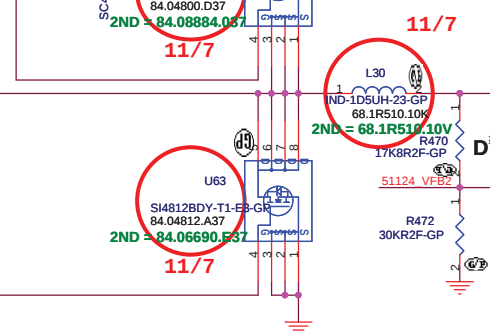
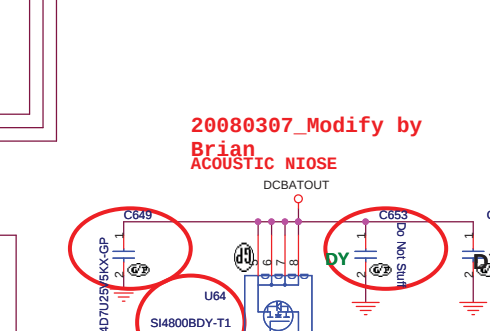
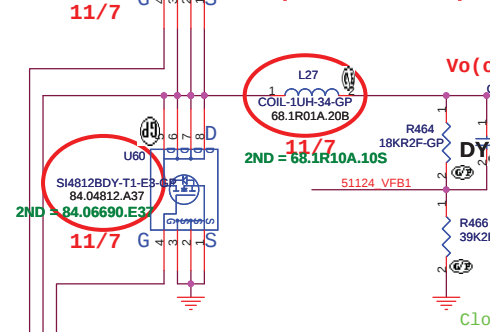
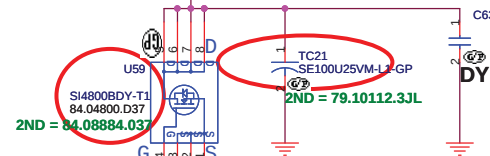


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2)/R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2)/R2$ --> Skip Mode

20080307_Modify by

Brian
ACOUSTIC NIOSE



Iomax=8A

Vo(cal)=1.1060V

11/7

2N2 = 84.08884.037

2N2 = 84.06690.537

2N2 = 84.08884.037

2N2 = 84.06690.537

2N2 = 84.08884.037

2N2 = 84.06690.537

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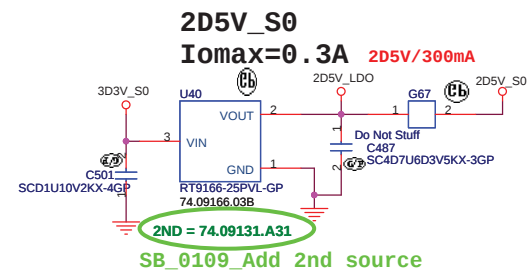
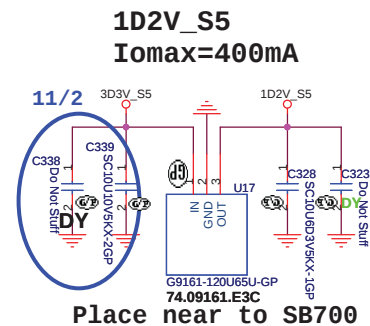
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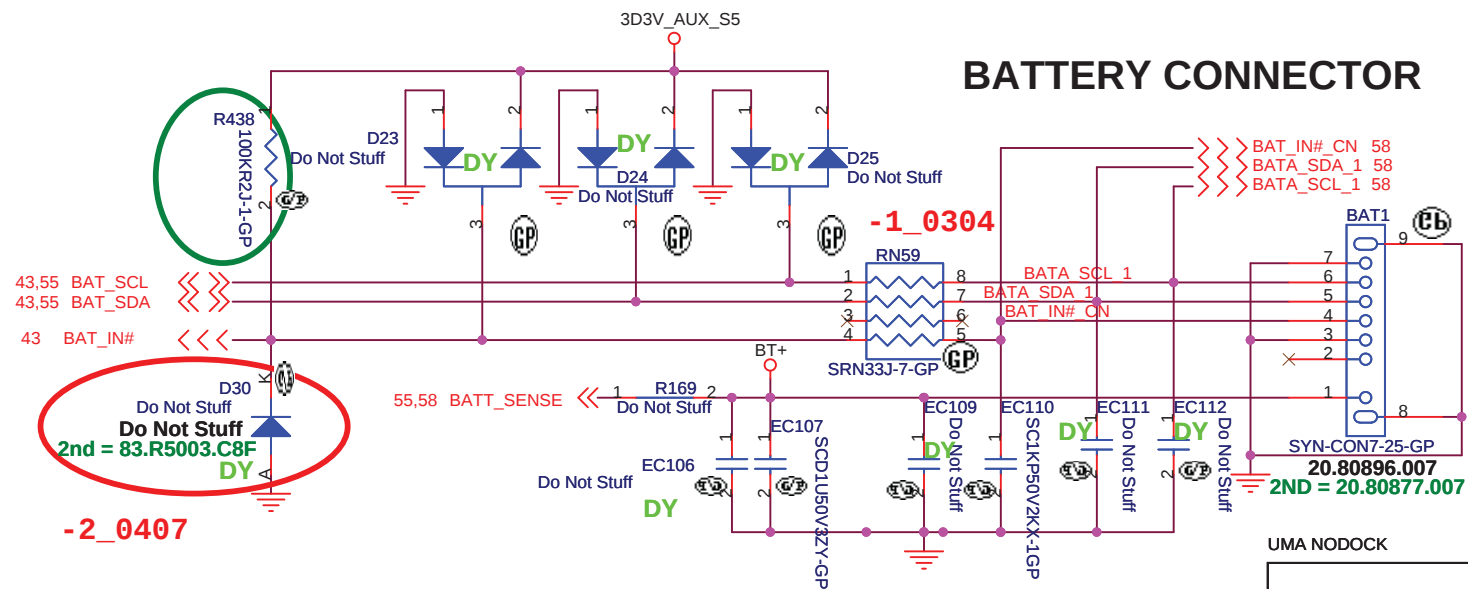
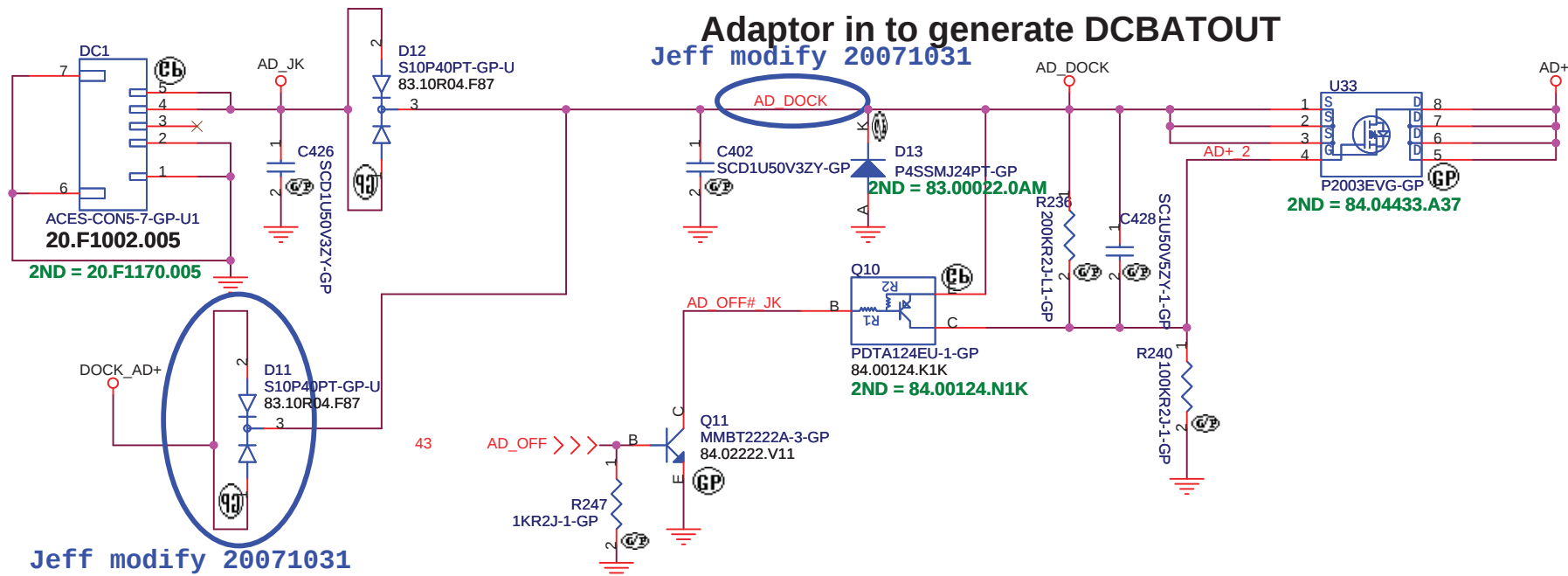
緯創資通

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Title		TPS51124 1D1V 1D2V	
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A3		-1	
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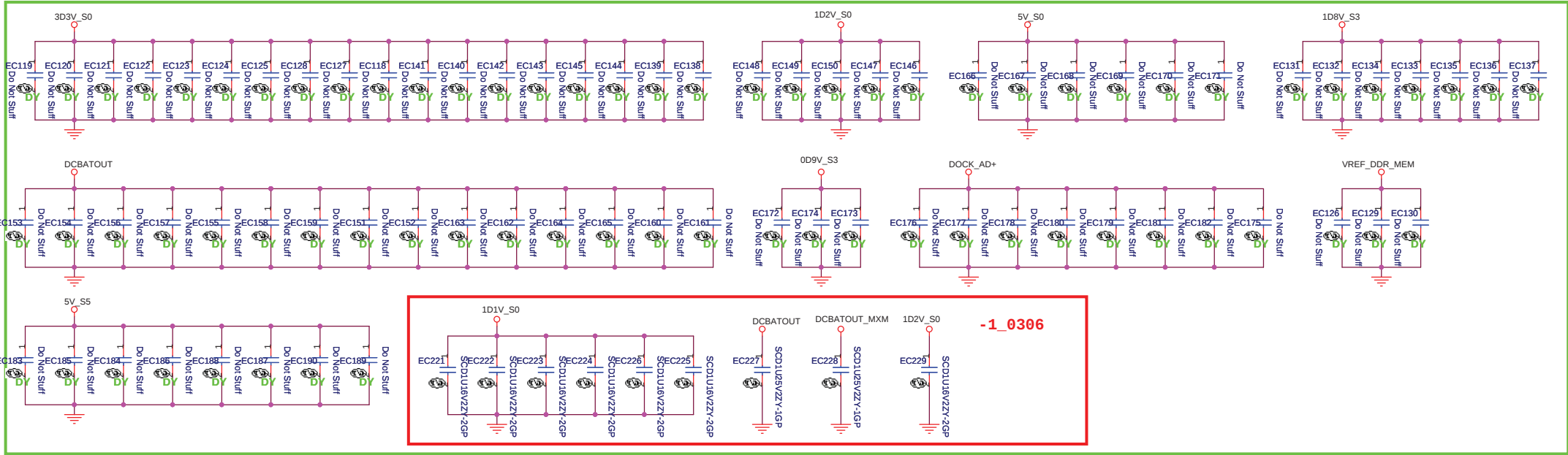
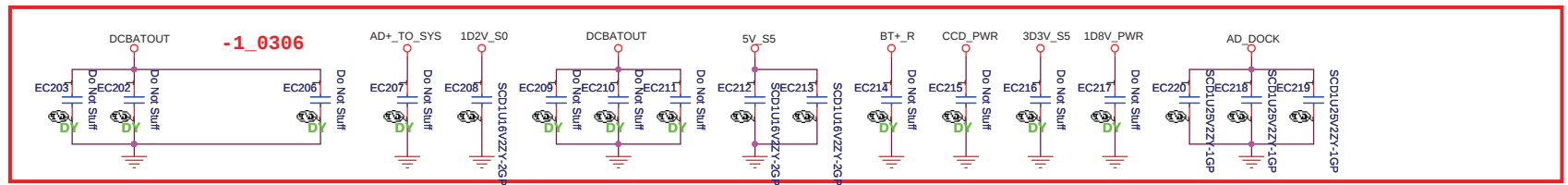
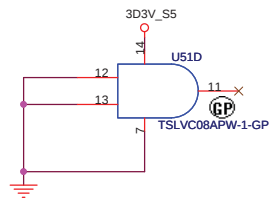




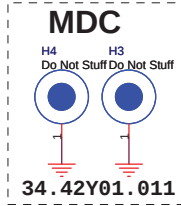


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

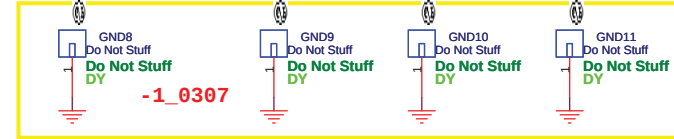
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A4	Olan	-1
Date: Tuesday, April 29, 2008	Sheet 56 of 58	



STAND OFF ON TOP



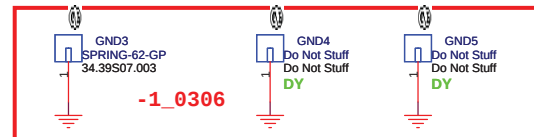
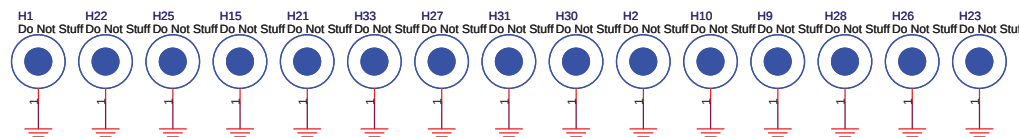
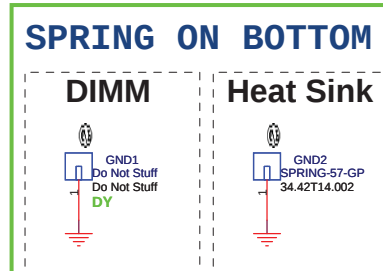
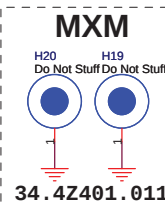
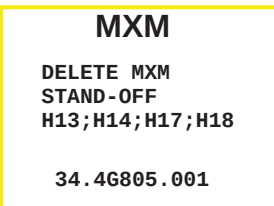
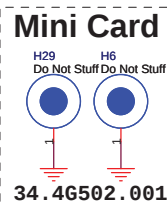
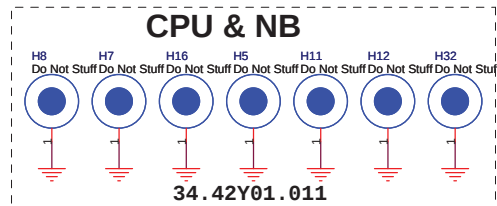
MXM SPRING -1 20080307



Check test point

STAND OFF ON BOTTOM

20080307_Modify by
Brian



- 3D3V_S0 TP180 Do Not Stuff
- 3D3V_AUX_S5 TP4 Do Not Stuff
- 3D3V_S5 TP183 Do Not Stuff
- 5V_S5 TP186 Do Not Stuff
- 21.43 PM_PWRBTN# TP185 Do Not Stuff
- 6.20 CPU_PWRGD TP184 Do Not Stuff
- 25.43 SS_ENABLE TP181 Do Not Stuff
- 6.20 CPU_LDT_RST# TP182 Do Not Stuff

Test Point放在Dimm Door打開可量測處

INTMIC1



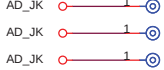
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SPKR1



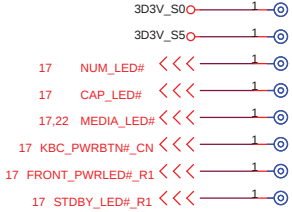
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DC1



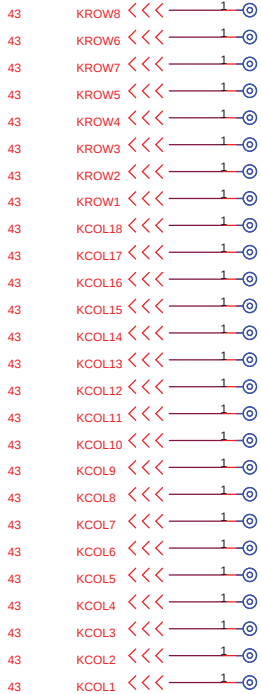
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PWRCN1



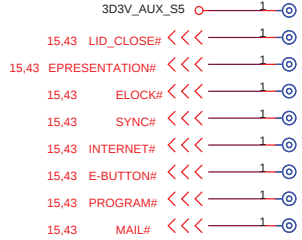
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KB1



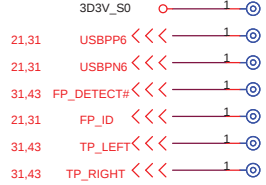
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TP224 Do Not Stuff
TP228 Do Not Stuff
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TP227 Do Not Stuff
TP222 Do Not Stuff
TP223 Do Not Stuff

SWITCHCN1



TP221 Do Not Stuff
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TP238 Do Not Stuff
TP243 Do Not Stuff

FP1



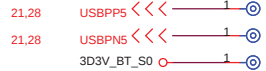
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TPDA1



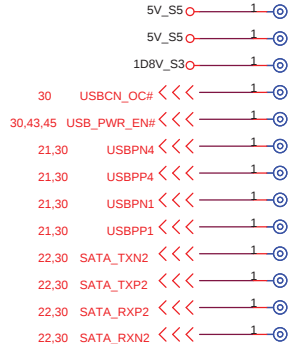
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BLUE1



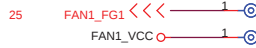
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USBCN1



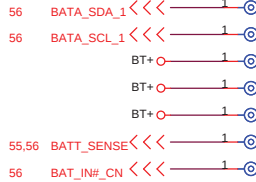
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TP261 Do Not Stuff
TP258 Do Not Stuff
TP259 Do Not Stuff
TP253 Do Not Stuff

FAN1



TP257 Do Not Stuff
TP256 Do Not Stuff

BAT1



TP254 Do Not Stuff
TP255 Do Not Stuff
TP251 Do Not Stuff
TP276 Do Not Stuff
TP279 Do Not Stuff
TP249 Do Not Stuff
TP248 Do Not Stuff

UMA NODOCK

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

AFTE TP

Size
A3

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Date: Monday, May 05, 2008

Sheet 1

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Rev
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