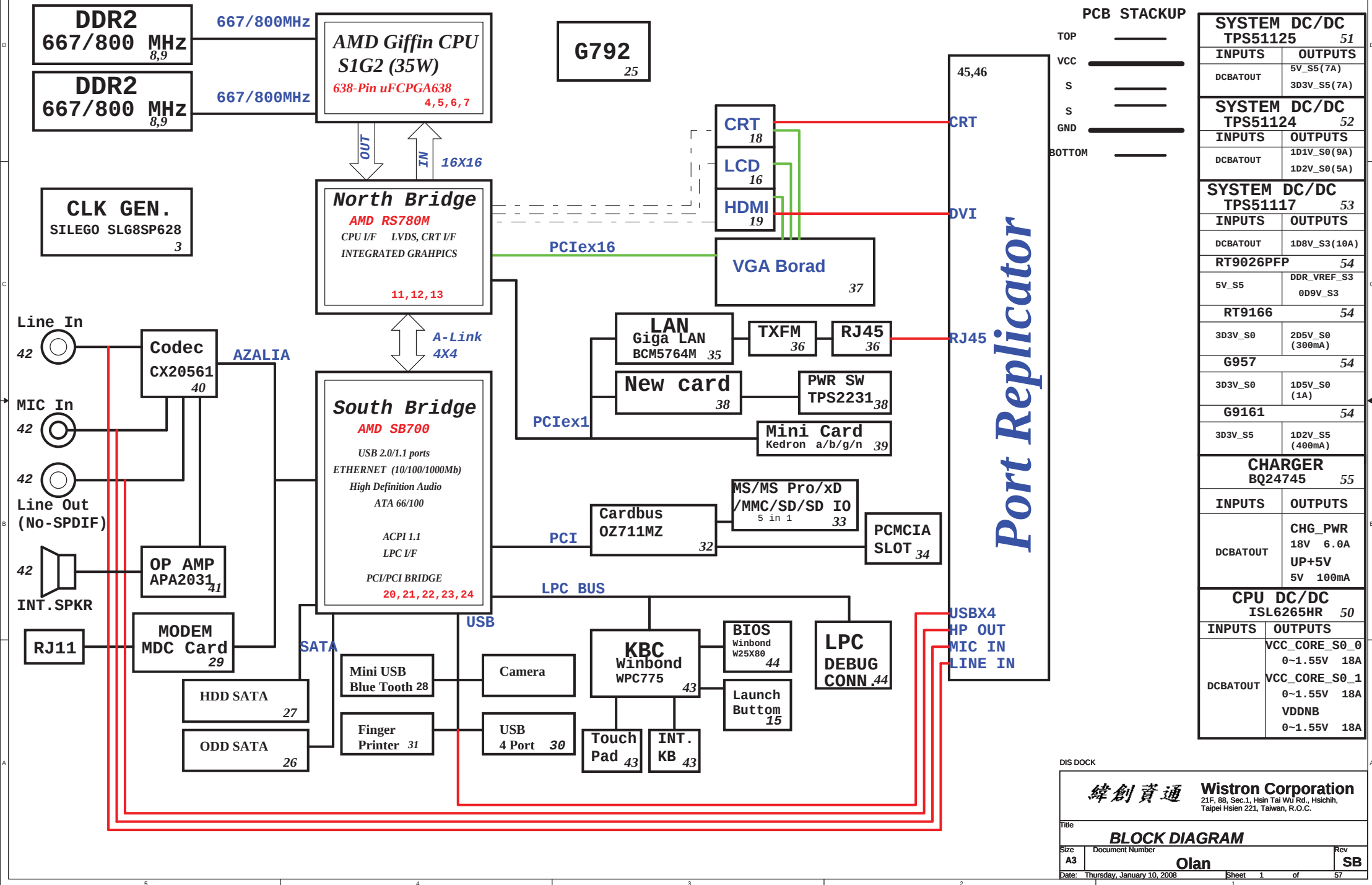


Olan (TM15") Block Diagram

Project code: 91.4Z701.001
PCB P/N : 48.4Z701.0SB
REVISION : 07249-SB



DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
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緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY

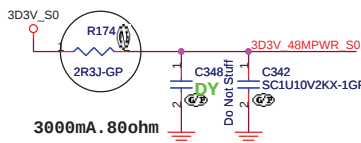
SizeA3

Document Number

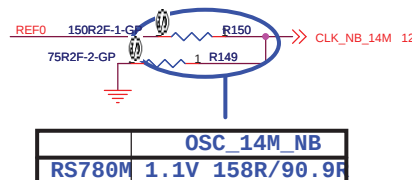
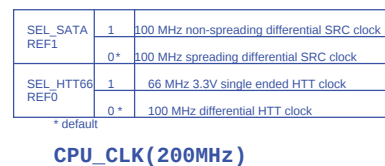
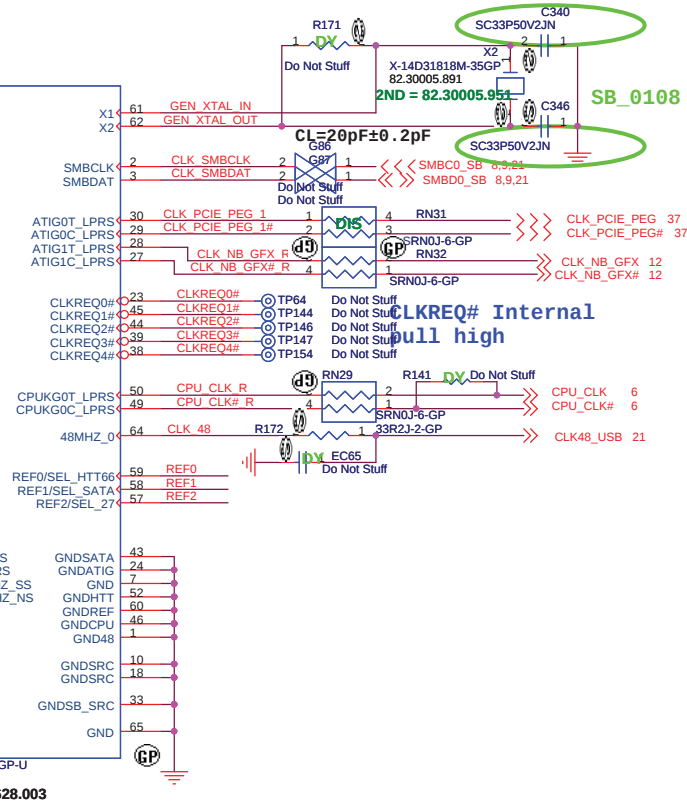
RevSA

Date: Thursday, January 10, 2008

Sheet2of57



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF

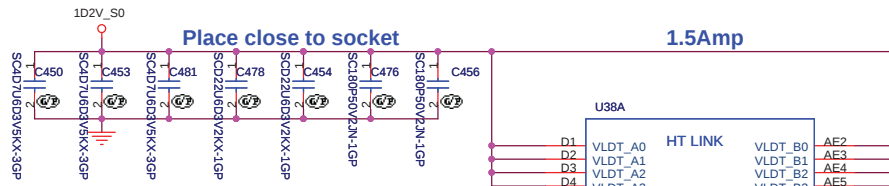
* RS780 can be used as clock buffer to output two PCIE reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

DIS DOCK

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Taipei Hsien 221, Taiwan, R.O.C.

Title	CLKGEN_ICS9LPRS480
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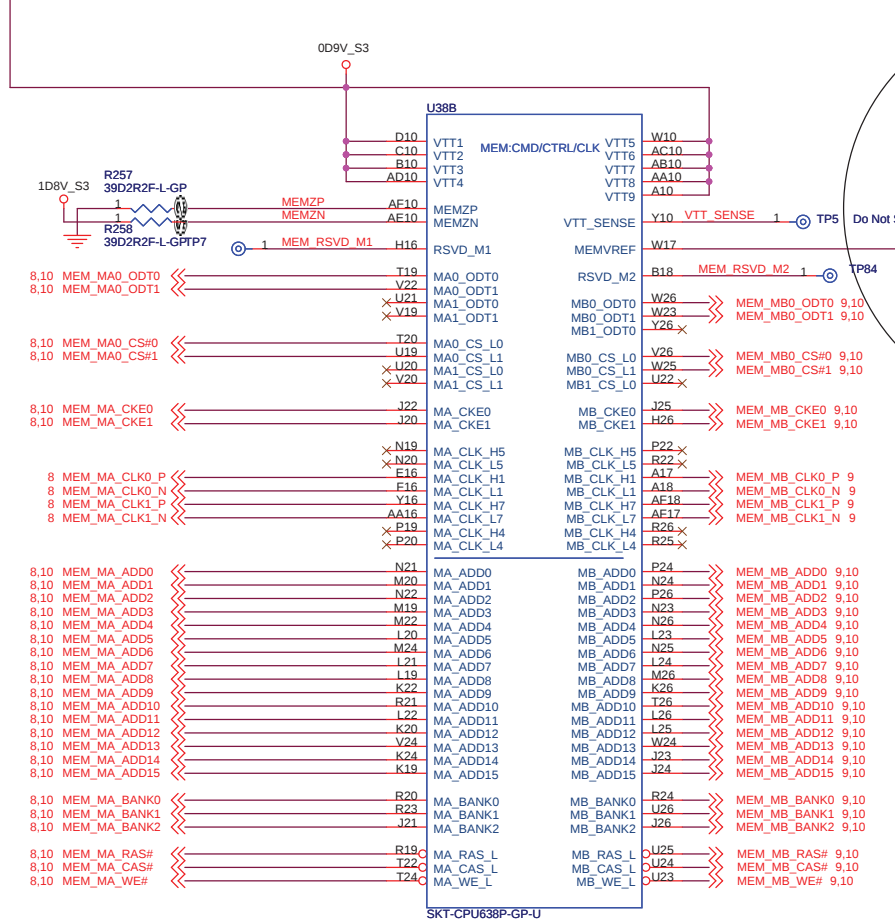
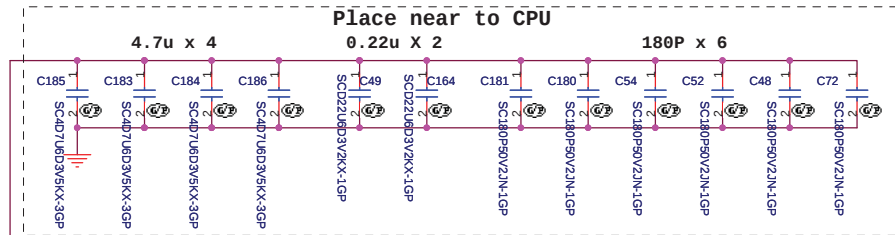
Size A3	Document Number Olan	Rev SA
Date: Thursday, January 10, 2008	Sheet 3 of	57



11 HT_NB_CPU_CAD_H0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	HT_CPU_NB_CAD_H0	11
11 HT_NB_CPU_CAD_L0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	HT_CPU_NB_CAD_L0	11
11 HT_NB_CPU_CAD_H1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	HT_CPU_NB_CAD_H1	11
11 HT_NB_CPU_CAD_L1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	HT_CPU_NB_CAD_L1	11
11 HT_NB_CPU_CAD_H2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	HT_CPU_NB_CAD_H2	11
11 HT_NB_CPU_CAD_L2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	HT_CPU_NB_CAD_L2	11
11 HT_NB_CPU_CAD_H3	H1	L0_CADIN_H3	L0_CADOUT_H3	AA2	HT_CPU_NB_CAD_H3	11
11 HT_NB_CPU_CAD_L3	J1	L0_CADIN_L3	L0_CADOUT_L3	W2	HT_CPU_NB_CAD_L3	11
11 HT_NB_CPU_CAD_H4	K1	L0_CADIN_H4	L0_CADOUT_H4	AA3	HT_CPU_NB_CAD_H4	11
11 HT_NB_CPU_CAD_L4	L3	L0_CADIN_L4	L0_CADOUT_L4	W3	HT_CPU_NB_CAD_L4	11
11 HT_NB_CPU_CAD_H5	L2	L0_CADIN_H5	L0_CADOUT_H5	V1	HT_CPU_NB_CAD_H5	11
11 HT_NB_CPU_CAD_L5	L1	L0_CADIN_L5	L0_CADOUT_L5	U1	HT_CPU_NB_CAD_L5	11
11 HT_NB_CPU_CAD_H6	M1	L0_CADIN_H6	L0_CADOUT_H6	U2	HT_CPU_NB_CAD_H6	11
11 HT_NB_CPU_CAD_L6	N3	L0_CADIN_L6	L0_CADOUT_L6	T1	HT_CPU_NB_CAD_L6	11
11 HT_NB_CPU_CAD_H7	N2	L0_CADIN_H7	L0_CADOUT_H7	R1	HT_CPU_NB_CAD_H7	11
11 HT_NB_CPU_CAD_L7	E5	L0_CADIN_L7	L0_CADOUT_L7	AD4	HT_CPU_NB_CAD_L7	11
11 HT_NB_CPU_CAD_H8	F5	L0_CADIN_H8	L0_CADOUT_H8	AD3	HT_CPU_NB_CAD_H8	11
11 HT_NB_CPU_CAD_L8	F3	L0_CADIN_L8	L0_CADOUT_L8	AD5	HT_CPU_NB_CAD_L8	11
11 HT_NB_CPU_CAD_H9	F4	L0_CADIN_H9	L0_CADOUT_H9	AC5	HT_CPU_NB_CAD_H9	11
11 HT_NB_CPU_CAD_L9	G5	L0_CADIN_L9	L0_CADOUT_L9	AB4	HT_CPU_NB_CAD_L9	11
11 HT_NB_CPU_CAD_H10	H5	L0_CADIN_H10	L0_CADOUT_H10	AB3	HT_CPU_NB_CAD_H10	11
11 HT_NB_CPU_CAD_L10	H3	L0_CADIN_L10	L0_CADOUT_L10	AB5	HT_CPU_NB_CAD_L10	11
11 HT_NB_CPU_CAD_H11	H4	L0_CADIN_H11	L0_CADOUT_H11	AA5	HT_CPU_NB_CAD_H11	11
11 HT_NB_CPU_CAD_L11	K4	L0_CADIN_L11	L0_CADOUT_L11	V5	HT_CPU_NB_CAD_L11	11
11 HT_NB_CPU_CAD_H12	L5	L0_CADIN_H12	L0_CADOUT_H12	W5	HT_CPU_NB_CAD_H12	11
11 HT_NB_CPU_CAD_L12	M5	L0_CADIN_L12	L0_CADOUT_L12	V4	HT_CPU_NB_CAD_L12	11
11 HT_NB_CPU_CAD_H13	M3	L0_CADIN_H13	L0_CADOUT_H13	V3	HT_CPU_NB_CAD_H13	11
11 HT_NB_CPU_CAD_L13	M4	L0_CADIN_L13	L0_CADOUT_L13	V5	HT_CPU_NB_CAD_L13	11
11 HT_NB_CPU_CAD_H14	M4	L0_CADIN_H14	L0_CADOUT_H14	U5	HT_CPU_NB_CAD_H14	11
11 HT_NB_CPU_CAD_L14	N5	L0_CADIN_L14	L0_CADOUT_L14	T4	HT_CPU_NB_CAD_L14	11
11 HT_NB_CPU_CAD_H15	P5	L0_CADIN_H15	L0_CADOUT_H15	T3	HT_CPU_NB_CAD_H15	11
11 HT_NB_CPU_CAD_L15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	HT_CPU_NB_CAD_L15	11
11 HT_NB_CPU_CLK_H0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	HT_CPU_NB_CLK_H0	11
11 HT_NB_CPU_CLK_L0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	HT_CPU_NB_CLK_L0	11
11 HT_NB_CPU_CLK_H1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	HT_CPU_NB_CLK_H1	11
11 HT_NB_CPU_CLK_L1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	HT_CPU_NB_CLK_L1	11
11 HT_NB_CPU_CTL_H0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	HT_CPU_NB_CTL_H0	11
11 HT_NB_CPU_CTL_L0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	HT_CPU_NB_CTL_L0	11
11 HT_NB_CPU_CTL_H1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	HT_CPU_NB_CTL_H1	11
11 HT_NB_CPU_CTL_L1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	HT_CPU_NB_CTL_L1	11

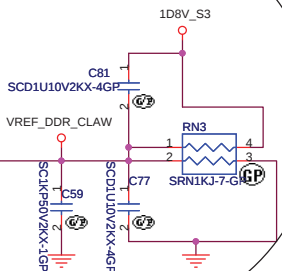
SKT-CPU638P-GP-U
62.10055.111
2ND = 62.10040.471
SKT - BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V



SKT-CPU638P-GP-U

CLOSE TO CPU



8	MEM_MA_DATA0	
8	MEM_MA_DATA1	
8	MEM_MA_DATA2	
8	MEM_MA_DATA3	
8	MEM_MA_DATA4	
8	MEM_MA_DATA5	
8	MEM_MA_DATA6	
8	MEM_MA_DATA7	
8	MEM_MA_DATA8	
8	MEM_MA_DATA9	
8	MEM_MA_DATA10	
8	MEM_MA_DATA11	
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8	MEM_MA_DATA61	
8	MEM_MA_DATA62	
8	MEM_MA_DATA63	

8	MEM_MA_DM0	
8	MEM_MA_DM1	
8	MEM_MA_DM2	
8	MEM_MA_DM3	
8	MEM_MA_DM4	
8	MEM_MA_DM5	
8	MEM_MA_DM6	
8	MEM_MA_DM7	

8	MEM_MA_DQS0_P	
8	MEM_MA_DQS0_N	
8	MEM_MA_DQS1_P	
8	MEM_MA_DQS1_N	
8	MEM_MA_DQS2_P	
8	MEM_MA_DQS2_N	
8	MEM_MA_DQS3_P	
8	MEM_MA_DQS3_N	
8	MEM_MA_DQS4_P	
8	MEM_MA_DQS4_N	
8	MEM_MA_DQS5_P	
8	MEM_MA_DQS5_N	
8	MEM_MA_DQS6_P	
8	MEM_MA_DQS6_N	
8	MEM_MA_DQS7_P	
8	MEM_MA_DQS7_N	

U38C		MEM-DATA	
G12	MA_DATA0	MB_DATA0	C11
F12	MA_DATA1	MB_DATA1	A11
H14	MA_DATA2	MB_DATA2	A14
G14	MA_DATA3	MB_DATA3	B14
H11	MA_DATA4	MB_DATA4	G11
C13	MA_DATA5	MB_DATA5	D12
E13	MA_DATA6	MB_DATA6	A13
H15	MA_DATA7	MB_DATA7	A15
E15	MA_DATA8	MB_DATA8	A16
E17	MA_DATA9	MB_DATA9	A19
E17	MA_DATA10	MB_DATA10	A20
E17	MA_DATA11	MB_DATA11	A21
F14	MA_DATA12	MB_DATA12	D14
C17	MA_DATA13	MB_DATA13	C18
G17	MA_DATA14	MB_DATA14	D18
G18	MA_DATA15	MB_DATA15	D20
C19	MA_DATA16	MB_DATA16	A21
D22	MA_DATA17	MB_DATA17	D24
E18	MA_DATA18	MB_DATA18	C25
F18	MA_DATA19	MB_DATA19	B20
B22	MA_DATA20	MB_DATA20	C20
C23	MA_DATA21	MB_DATA21	B24
F20	MA_DATA22	MB_DATA22	C24
E22	MA_DATA23	MB_DATA23	E23
H24	MA_DATA24	MB_DATA24	G25
.119	MA_DATA25	MB_DATA25	G26
E21	MA_DATA26	MB_DATA26	C26
E22	MA_DATA27	MB_DATA27	D26
H20	MA_DATA28	MB_DATA28	G23
H22	MA_DATA29	MB_DATA29	G24
AB24	MA_DATA30	MB_DATA30	AA24
AB22	MA_DATA31	MB_DATA31	AA23
AA21	MA_DATA32	MB_DATA32	AD24
W21	MA_DATA33	MB_DATA33	AE24
Y22	MA_DATA34	MB_DATA34	AE26
AA20	MA_DATA35	MB_DATA35	AE25
AA18	MA_DATA36	MB_DATA36	AC22
AB18	MA_DATA37	MB_DATA37	AD22
AB21	MA_DATA38	MB_DATA38	AE20
AD19	MA_DATA39	MB_DATA39	AE20
Y18	MA_DATA40	MB_DATA40	AD14
AD17	MA_DATA41	MB_DATA41	AE19
W16	MA_DATA42	MB_DATA42	AC18
Y14	MA_DATA43	MB_DATA43	AE16
AB17	MA_DATA44	MB_DATA44	AE15
AB15	MA_DATA45	MB_DATA45	AE13
AD15	MA_DATA46	MB_DATA46	AC12
AB13	MA_DATA47	MB_DATA47	AE11
AD13	MA_DATA48	MB_DATA48	AE10
Y12	MA_DATA49	MB_DATA49	AE09
W11	MA_DATA50	MB_DATA50	AE08
AB14	MA_DATA51	MB_DATA51	AE07
AA14	MA_DATA52	MB_DATA52	AE06
AB12	MA_DATA53	MB_DATA53	AE05
AA12	MA_DATA54	MB_DATA54	AE04
	MA_DATA55	MB_DATA55	AE03
	MA_DATA56	MB_DATA56	AE02
	MA_DATA57	MB_DATA57	AE01
	MA_DATA58	MB_DATA58	AE00
	MA_DATA59	MB_DATA59	AE00
	MA_DATA60	MB_DATA60	AE00
	MA_DATA61	MB_DATA61	AE00
	MA_DATA62	MB_DATA62	AE00
	MA_DATA63	MB_DATA63	AE00

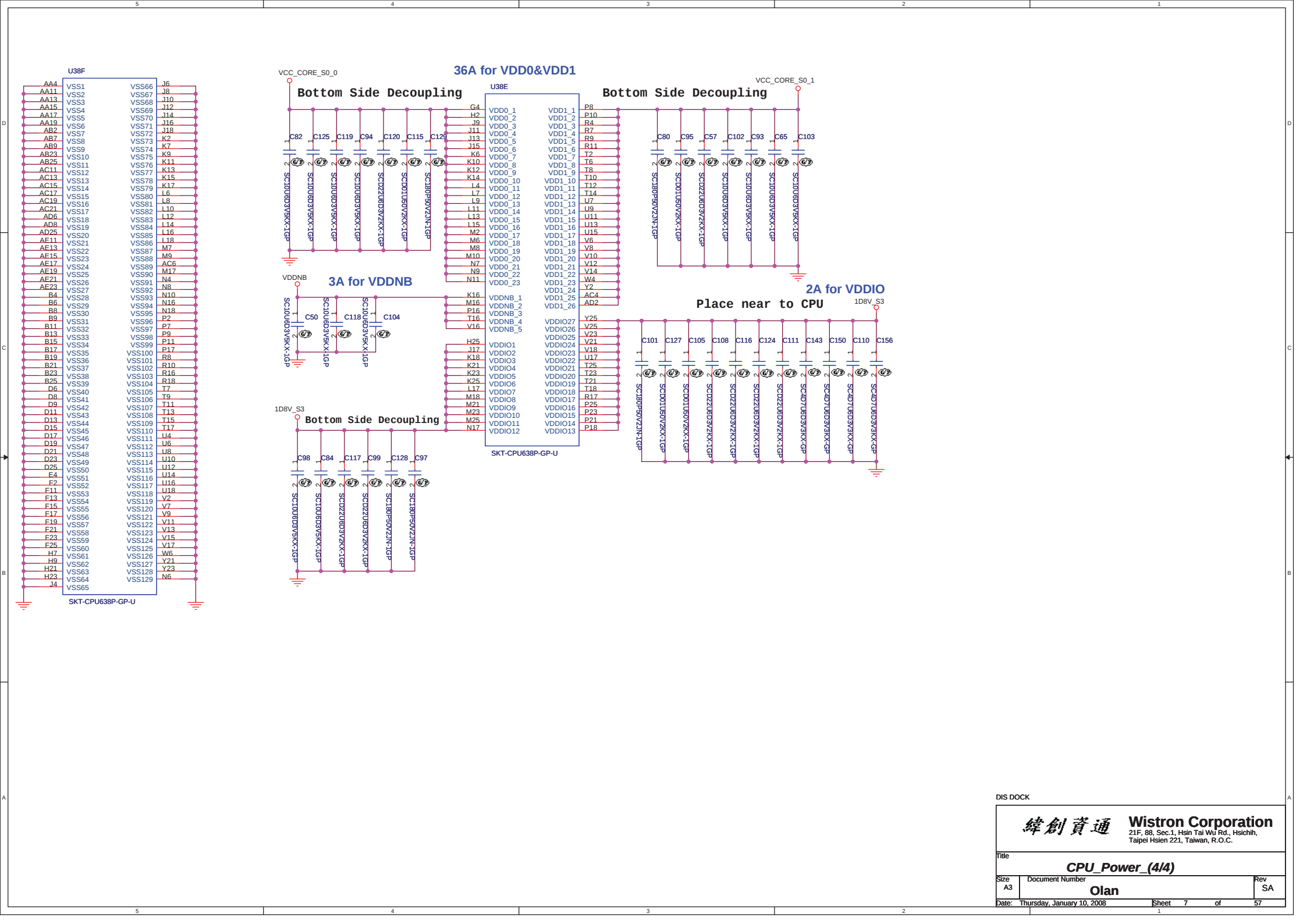
MA_DM0	MB_DM0	C12
MA_DM1	MB_DM1	B12
MA_DM2	MB_DM2	A22
MA_DM3	MB_DM3	E25
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MA_DM5	MB_DM5	AE22
MA_DM6	MB_DM6	AC16
MA_DM7	MB_DM7	AD12

MA_DQS_H0	MB_DQS_H0	C12
MA_DQS_L0	MB_DQS_L0	B12
MA_DQS_H1	MB_DQS_H1	D12
MA_DQS_L1	MB_DQS_L1	C15
MA_DQS_H2	MB_DQS_H2	A24
MA_DQS_L2	MB_DQS_L2	A23
MA_DQS_H3	MB_DQS_H3	F26
MA_DQS_L3	MB_DQS_L3	E26
MA_DQS_H4	MB_DQS_H4	AC25
MA_DQS_L4	MB_DQS_L4	AC26
MA_DQS_H5	MB_DQS_H5	AE21
MA_DQS_L5	MB_DQS_L5	AE22
MA_DQS_H6	MB_DQS_H6	AE16
MA_DQS_L6	MB_DQS_L6	AD16
MA_DQS_H7	MB_DQS_H7	AE12
MA_DQS_L7	MB_DQS_L7	AE12

DIS DOCK

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU_DDR (2/4)		
Size	Document Number	Rev
A3	Olan	SA
Date:	Thursday, January 10, 2008	Sheet 5 of 57

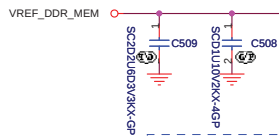


5.10 MEM_MB_ADD0 >> 102 A0
5.10 MEM_MB_ADD1 >> 101 A1
5.10 MEM_MB_ADD2 >> 100 A2
5.10 MEM_MB_ADD3 >> 99 A3
5.10 MEM_MB_ADD4 >> 98 A4
5.10 MEM_MB_ADD5 >> 97 A5
5.10 MEM_MB_ADD6 >> 96 A6
5.10 MEM_MB_ADD7 >> 95 A7
5.10 MEM_MB_ADD8 >> 94 A8
5.10 MEM_MB_ADD9 >> 93 A9
5.10 MEM_MB_ADD10 >> 92 A10/AP
5.10 MEM_MB_ADD11 >> 91 A11
5.10 MEM_MB_ADD12 >> 90 A12
5.10 MEM_MB_ADD13 >> 89 A13
5.10 MEM_MB_ADD14 >> 88 A14
5.10 MEM_MB_ADD15 >> 87 A15
5.10 MEM_MB_BANK2 >> 107 BA0
5.10 MEM_MB_BANK0 >> 106 BA1
5.10 MEM_MB_BANK1 >> 105 BA2

5 MEM_MB_DATA0 >> 5 DQ0
5 MEM_MB_DATA1 >> 7 DQ1
5 MEM_MB_DATA2 >> 17 DQ2
5 MEM_MB_DATA3 >> 19 DQ3
5 MEM_MB_DATA4 >> 4 DQ4
5 MEM_MB_DATA5 >> 6 DQ5
5 MEM_MB_DATA6 >> 14 DQ6
5 MEM_MB_DATA7 >> 16 DQ7
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5 MEM_MB_DATA57 >> 181 DQ57
5 MEM_MB_DATA58 >> 189 DQ58
5 MEM_MB_DATA59 >> 191 DQ59
5 MEM_MB_DATA60 >> 180 DQ60
5 MEM_MB_DATA61 >> 182 DQ61
5 MEM_MB_DATA62 >> 192 DQ62
5 MEM_MB_DATA63 >> 194 DQ63

5 MEM_MB_DQS0_N >> 110 DQS0#
5 MEM_MB_DQS1_N >> 29 DQS1#
5 MEM_MB_DQS2_N >> 49 DQS2#
5 MEM_MB_DQS3_N >> 69 DQS3#
5 MEM_MB_DQS4_N >> 129 DQS4#
5 MEM_MB_DQS5_N >> 149 DQS5#
5 MEM_MB_DQS6_N >> 169 DQS6#
5 MEM_MB_DQS7_N >> 189 DQS7#
5 MEM_MB_DQS0_P >> 13 DQS0
5 MEM_MB_DQS1_P >> 31 DQS1
5 MEM_MB_DQS2_P >> 51 DQS2
5 MEM_MB_DQS3_P >> 70 DQS3
5 MEM_MB_DQS4_P >> 131 DQS4
5 MEM_MB_DQS5_P >> 148 DQS5
5 MEM_MB_DQS6_P >> 169 DQS6
5 MEM_MB_DQS7_P >> 188 DQS7

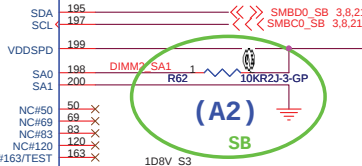
5.10 MEM_MB_ODT0 >> 114 OTD0
5.10 MEM_MB_ODT1 >> 119 OTD1



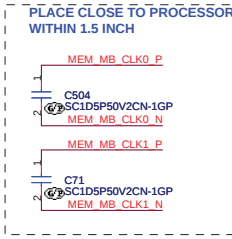
LOW 5.2 mm
Main Source:

REVERSE TYPE

RAS# 108 A0
WE# 109 A1
CAS# 113 A2
CS0# 110 A3
CS1# 115 A4
CKE0 79 A5
CKE1 80 A6
CK0 30 A7
CK0# 32 A8
CK1 164 A9
CK1# 166 A10/AP
DM0 10 A11
DM1 26 A12
DM2 52 A13
DM3 130 A14
DM4 147 A15
DM5 170 A16/BA2
DM6 185 BA0
DM7 185 BA1



VDD 81 DQ0
VDD 82 DQ1
VDD 87 DQ2
VDD 88 DQ3
VDD 95 DQ4
VDD 96 DQ5
VDD 103 DQ6
VDD 104 DQ7
VDD 111 DQ8
VDD 112 DQ9
VDD 117 DQ10
VDD 118 DQ11
VSS 3 DQ12
VSS 8 DQ13
VSS 9 DQ14
VSS 15 DQ15
VSS 18 DQ16
VSS 21 DQ17
VSS 24 DQ18
VSS 27 DQ19
VSS 28 DQ20
VSS 33 DQ21
VSS 34 DQ22
VSS 38 DQ23
VSS 40 DQ24
VSS 41 DQ25
VSS 42 DQ26
VSS 47 DQ27
VSS 48 DQ28
VSS 53 DQ29
VSS 54 DQ30
VSS 59 DQ31
VSS 60 DQ32
VSS 65 DQ33
VSS 66 DQ34
VSS 71 DQ35
VSS 72 DQ36
VSS 77 DQ37
VSS 78 DQ38
VSS 121 DQ39
VSS 122 DQ40
VSS 127 DQ41
VSS 128 DQ42
VSS 132 DQ43
VSS 133 DQ44
VSS 138 DQ45
VSS 139 DQ46
VSS 144 DQ47
VSS 145 DQ48
VSS 149 DQ49
VSS 150 DQ50
VSS 155 DQ51
VSS 156 DQ52
VSS 161 DQ53
VSS 162 DQ54
VSS 165 DQ55
VSS 168 DQ56
VSS 171 DQ57
VSS 172 DQ58
VSS 177 DQ59
VSS 178 DQ60
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VSS 190 DQ64
VSS 193 DQ65
VSS 196 DQ66
GND 201 DQ67
MH2 202 DQ68



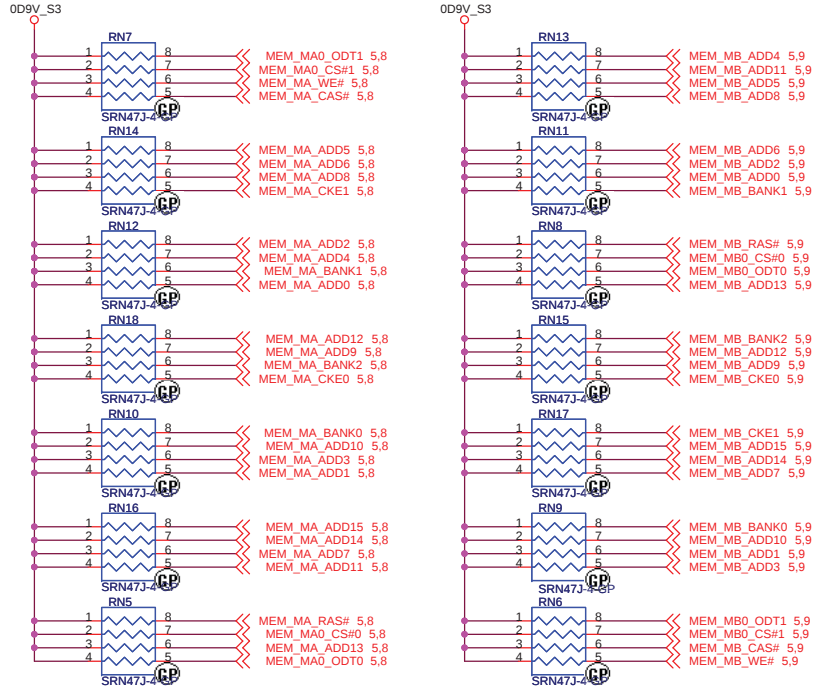
DIS DOCK

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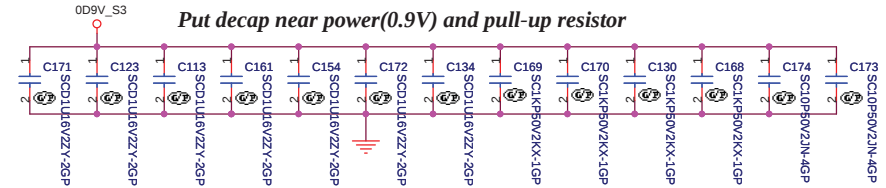
Title			DDR_SO-DIMM SKT_2
Size	Document Number	Rev	
Custom	Olan	SA	
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PARALLEL TERMINATION

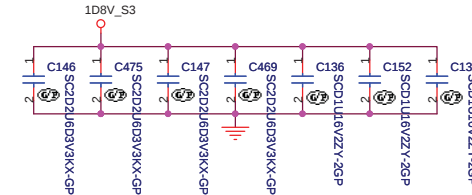
Put decap near power(0.9V) and pull-up resistor



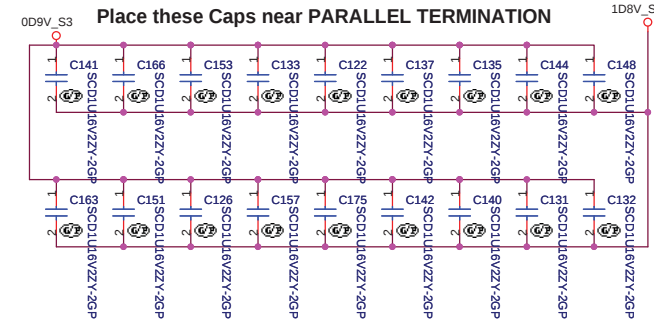
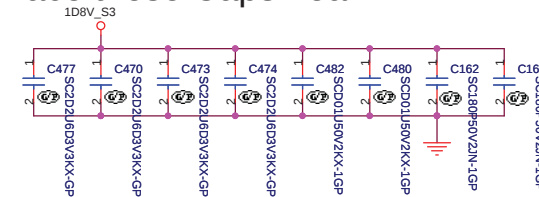
Decoupling Capacitor



Place these Caps near DM1



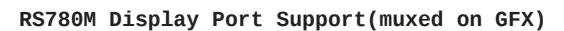
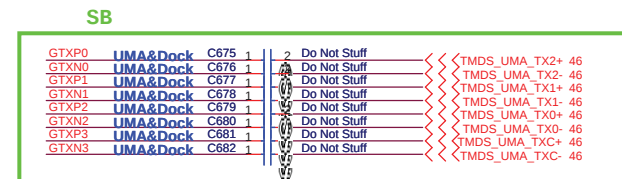
Place these Caps near DM2



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Title		
DDR DAMPING & TERMINATION		
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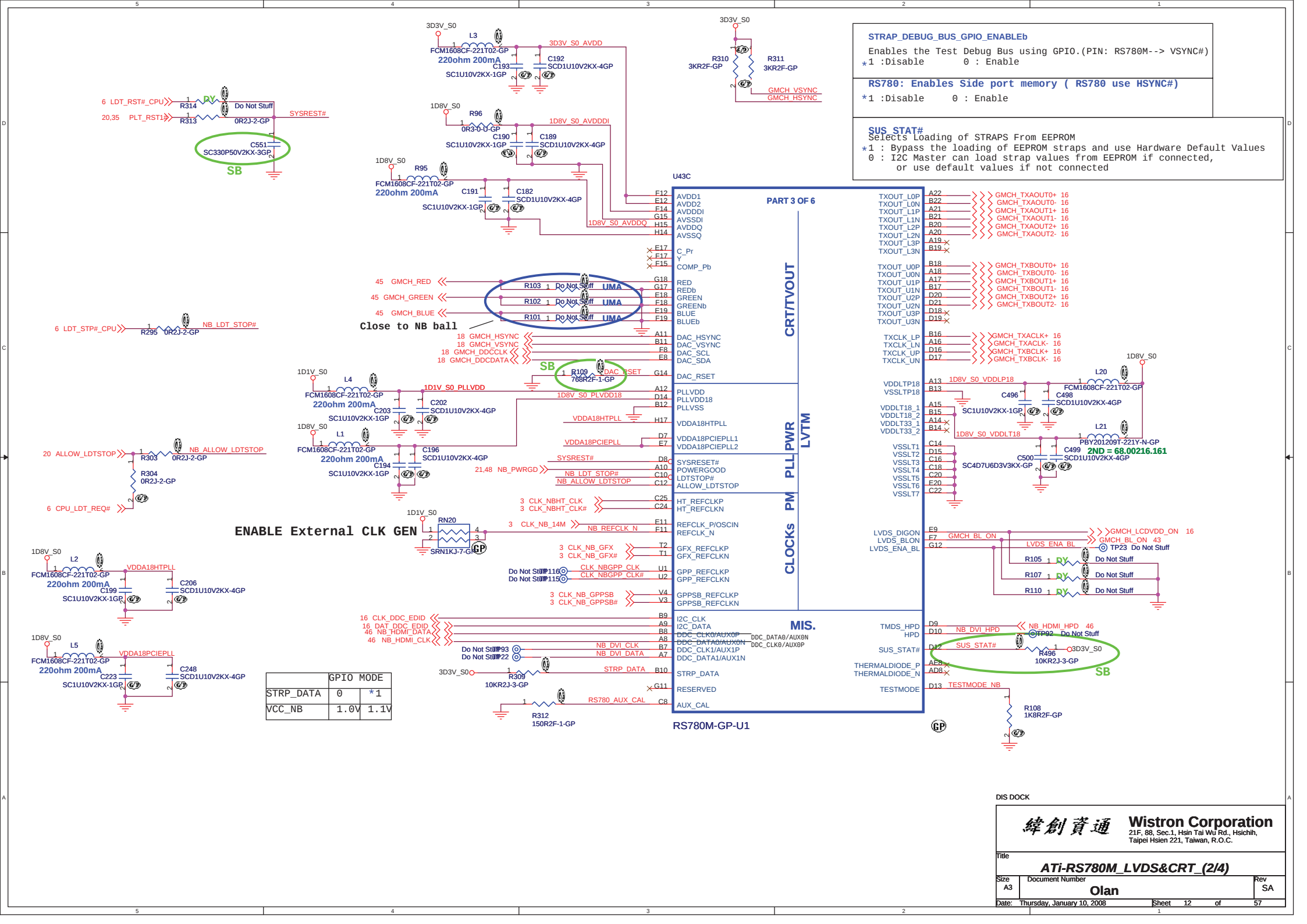


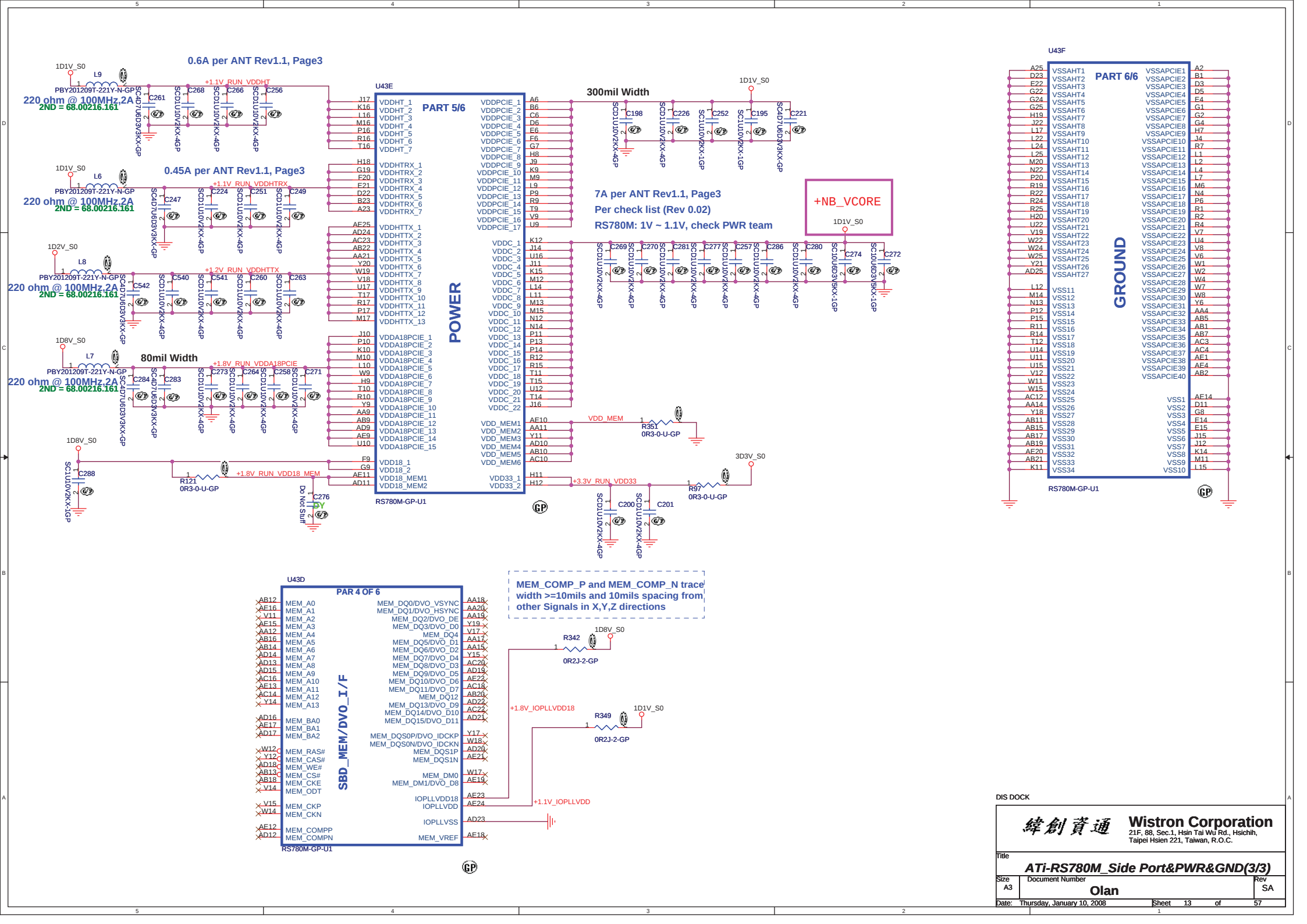
The diagram shows the pin assignment for the NEW CARD connector, which is a 38-pin connector. The pins are organized into four main sections: LAN, MINICARD, SB, and A-LINK. The LAN section includes pins 35 (RJ45), 36 (RJ45), 37 (RJ45), 38 (RJ45), and 39 (RJ45). The MINICARD section includes pins 40 (RJ45), 41 (RJ45), 42 (RJ45), 43 (RJ45), 44 (RJ45), 45 (RJ45), 46 (RJ45), 47 (RJ45), 48 (RJ45), 49 (RJ45), 50 (RJ45), 51 (RJ45), 52 (RJ45), 53 (RJ45), 54 (RJ45), 55 (RJ45), 56 (RJ45), 57 (RJ45), 58 (RJ45), 59 (RJ45), 60 (RJ45), 61 (RJ45), 62 (RJ45), 63 (RJ45), 64 (RJ45), 65 (RJ45), 66 (RJ45), 67 (RJ45), 68 (RJ45), 69 (RJ45), 70 (RJ45), 71 (RJ45), 72 (RJ45), 73 (RJ45), 74 (RJ45), 75 (RJ45), 76 (RJ45), 77 (RJ45), 78 (RJ45), 79 (RJ45), 80 (RJ45), 81 (RJ45), 82 (RJ45), 83 (RJ45), 84 (RJ45), 85 (RJ45), 86 (RJ45), 87 (RJ45), 88 (RJ45), 89 (RJ45), 90 (RJ45), 91 (RJ45), 92 (RJ45), 93 (RJ45), 94 (RJ45), 95 (RJ45), 96 (RJ45), 97 (RJ45), 98 (RJ45), 99 (RJ45), 100 (RJ45). The SB section includes pins 101 (RJ45), 102 (RJ45), 103 (RJ45), 104 (RJ45), 105 (RJ45), 106 (RJ45), 107 (RJ45), 108 (RJ45), 109 (RJ45), 110 (RJ45), 111 (RJ45), 112 (RJ45), 113 (RJ45), 114 (RJ45), 115 (RJ45), 116 (RJ45), 117 (RJ45), 118 (RJ45), 119 (RJ45), 120 (RJ45), 121 (RJ45), 122 (RJ45), 123 (RJ45), 124 (RJ45), 125 (RJ45), 126 (RJ45), 127 (RJ45), 128 (RJ45), 129 (RJ45), 130 (RJ45), 131 (RJ45), 132 (RJ45), 133 (RJ45), 134 (RJ45), 135 (RJ45), 136 (RJ45), 137 (RJ45), 138 (RJ45), 139 (RJ45), 140 (RJ45), 141 (RJ45), 142 (RJ45), 143 (RJ45), 144 (RJ45), 145 (RJ45), 146 (RJ45), 147 (RJ45), 148 (RJ45), 149 (RJ45), 150 (RJ45), 151 (RJ45), 152 (RJ45), 153 (RJ45), 154 (RJ45), 155 (RJ45), 156 (RJ45), 157 (RJ45), 158 (RJ45), 159 (RJ45), 160 (RJ45), 161 (RJ45), 162 (RJ45), 163 (RJ45), 164 (RJ45), 165 (RJ45), 166 (RJ45), 167 (RJ45), 168 (RJ45), 169 (RJ45), 170 (RJ45), 171 (RJ45), 172 (RJ45), 173 (RJ45), 174 (RJ45), 175 (RJ45), 176 (RJ45), 177 (RJ45), 178 (RJ45), 179 (RJ45), 180 (RJ45), 181 (RJ45), 182 (RJ45), 183 (RJ45), 184 (RJ45), 185 (RJ45), 186 (RJ45), 187 (RJ45), 188 (RJ45), 189 (RJ45), 190 (RJ45), 191 (RJ45), 192 (RJ45), 193 (RJ45), 194 (RJ45), 195 (RJ45), 196 (RJ45), 197 (RJ45), 198 (RJ45), 199 (RJ45), 200 (RJ45). The A-LINK section includes pins 201 (RJ45), 202 (RJ45), 203 (RJ45), 204 (RJ45), 205 (RJ45), 206 (RJ45), 207 (RJ45), 208 (RJ45), 209 (RJ45), 210 (RJ45), 211 (RJ45), 212 (RJ45), 213 (RJ45), 214 (RJ45), 215 (RJ45), 216 (RJ45), 217 (RJ45), 218 (RJ45), 219 (RJ45), 220 (RJ45), 221 (RJ45), 222 (RJ45), 223 (RJ45), 224 (RJ45), 225 (RJ45), 226 (RJ45), 227 (RJ45), 228 (RJ45), 229 (RJ45), 230 (RJ45), 231 (RJ45), 232 (RJ45), 233 (RJ45), 234 (RJ45), 235 (RJ45), 236 (RJ45), 237 (RJ45), 238 (RJ45), 239 (RJ45), 240 (RJ45), 241 (RJ45), 242 (RJ45), 243 (RJ45), 244 (RJ45), 245 (RJ45), 246 (RJ45), 247 (RJ45), 248 (RJ45), 249 (RJ45), 250 (RJ45), 251 (RJ45), 252 (RJ45), 253 (RJ45), 254 (RJ45), 255 (RJ45), 256 (RJ45), 257 (RJ45), 258 (RJ45), 259 (RJ45), 260 (RJ45), 261 (RJ45), 262 (RJ45), 263 (RJ45), 264 (RJ45), 265 (RJ45), 266 (RJ45), 267 (RJ45), 268 (RJ45), 269 (RJ45), 270 (RJ45), 271 (RJ45), 272 (RJ45), 273 (RJ45), 274 (RJ45), 275 (RJ45), 276 (RJ45), 277 (RJ45), 278 (RJ45), 279 (RJ45), 280 (RJ45), 281 (RJ45), 282 (RJ45), 283 (RJ45), 284 (RJ45), 285 (RJ45), 286 (RJ45), 287 (RJ45), 288 (RJ45), 289 (RJ45), 290 (RJ45), 291 (RJ45), 292 (RJ45), 293 (RJ45), 294 (RJ45), 295 (RJ45), 296 (RJ45), 297 (RJ45), 298 (RJ45), 299 (RJ45), 300 (RJ45).

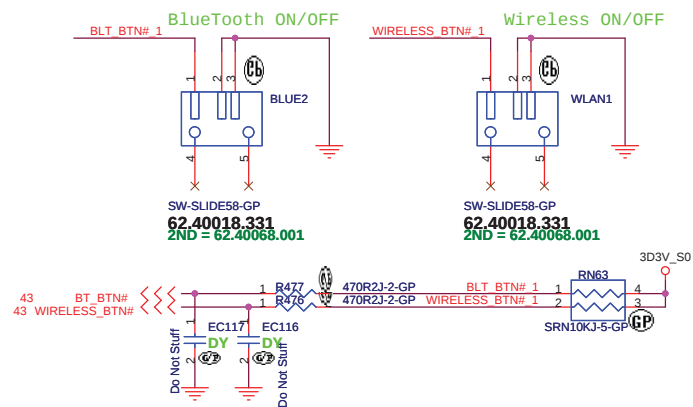


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ATI-RS780M_HT LINK&PCle(1/3)			
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DIS DOCK

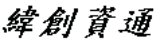
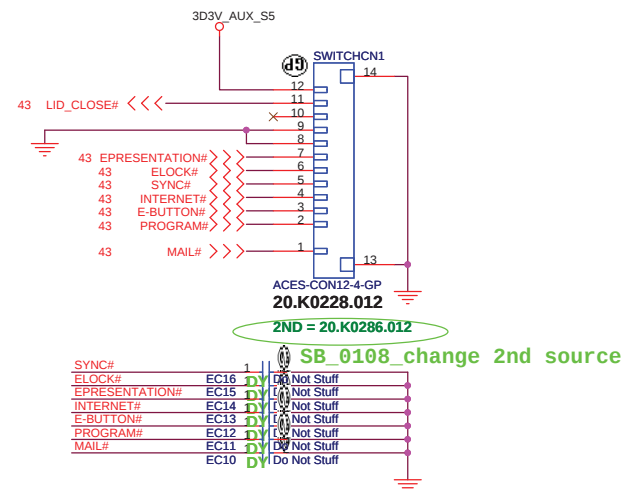
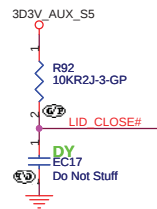
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Title	
SWITCH	
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Diagram illustrating the pin configuration for the SRN10KJ-L3-GP component. The component is a square package with pins numbered 1 through 10. The connections are as follows:

- Pin 1: INTERNET#
- Pin 2: EPRESENTATION#
- Pin 3: ELOCK#
- Pin 4: SYNC#
- Pin 5: 3D3V_S0
- Pin 6: MAIL#
- Pin 7: PROGRAM#
- Pin 8: E-BUTTON#
- Pin 9: 3D3V_S0
- Pin 10: 3D3V_S0

The component is labeled SRN10KJ-L3-GP and GP.



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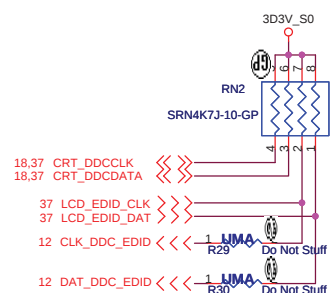
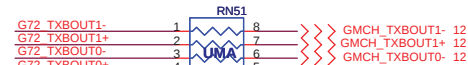
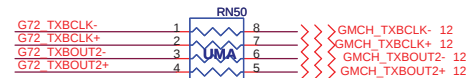
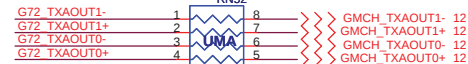
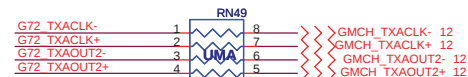
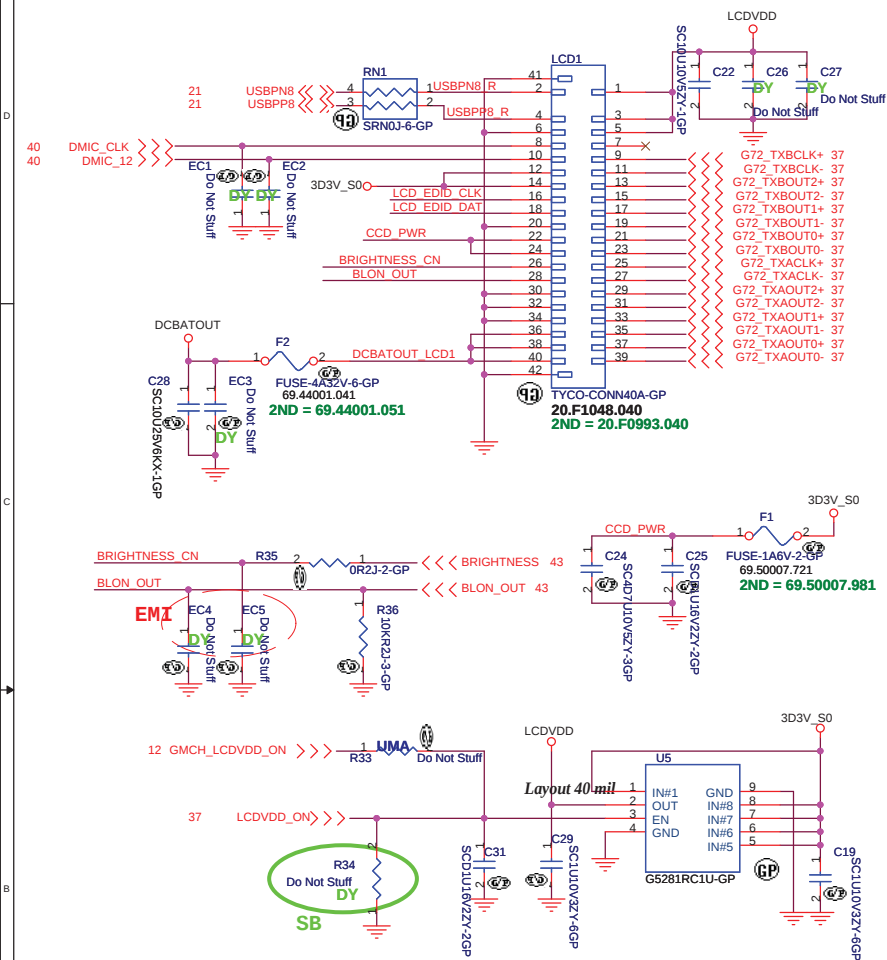
LAUNCH

Olan

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LCD/INVERTER/CCD CONN

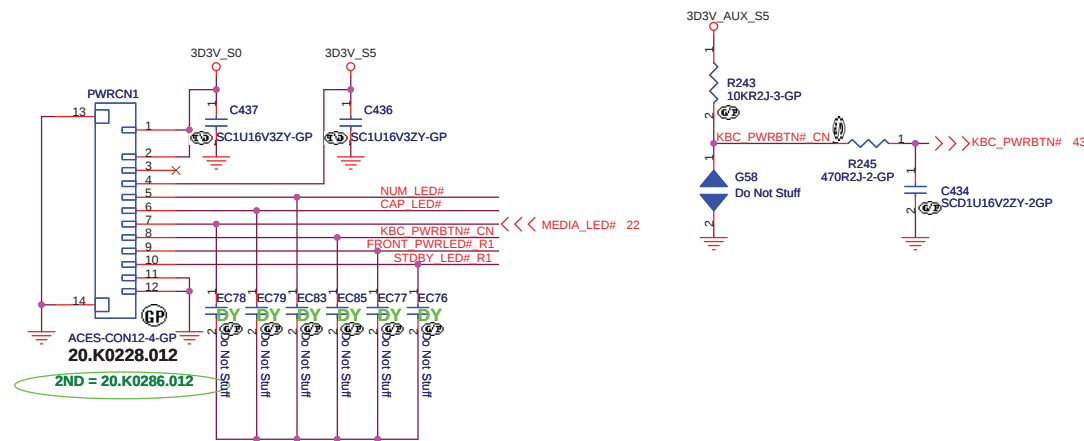
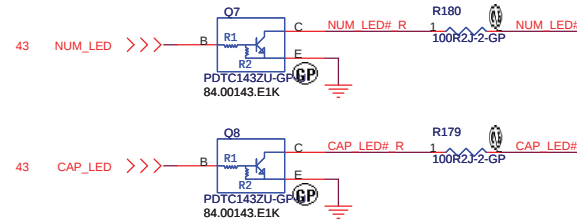
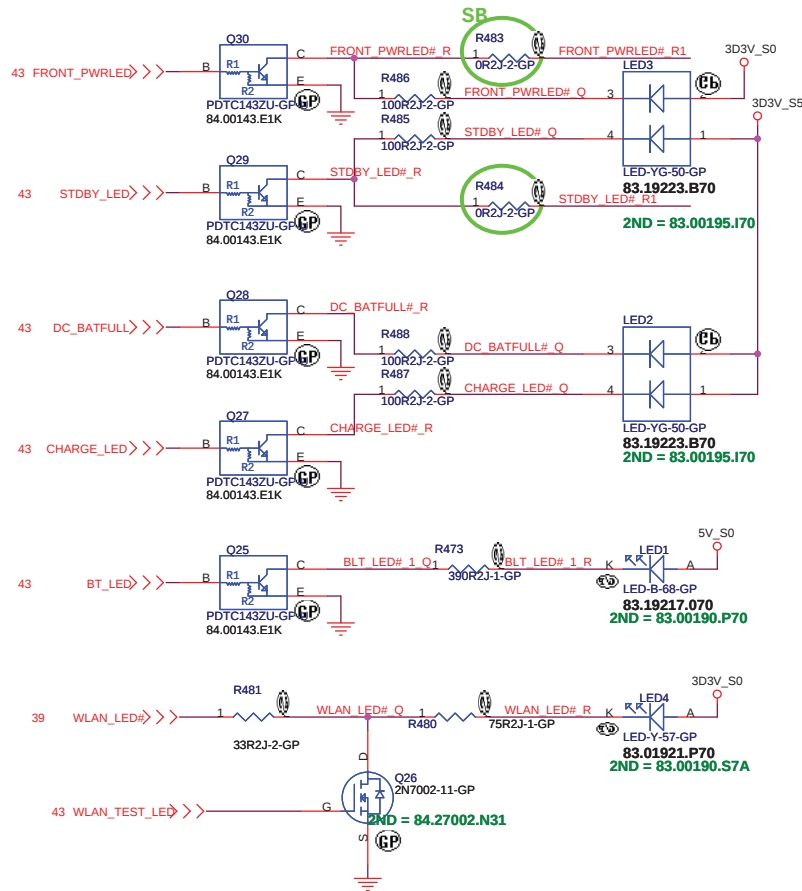


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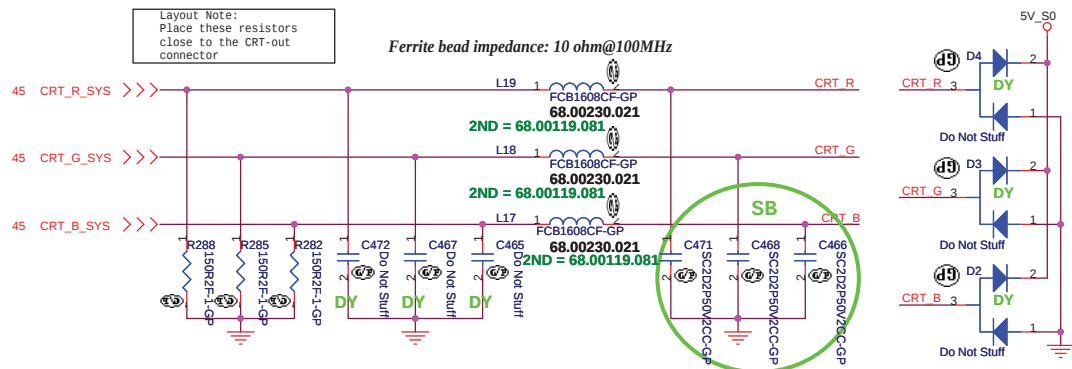
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LCD CONN				
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LED



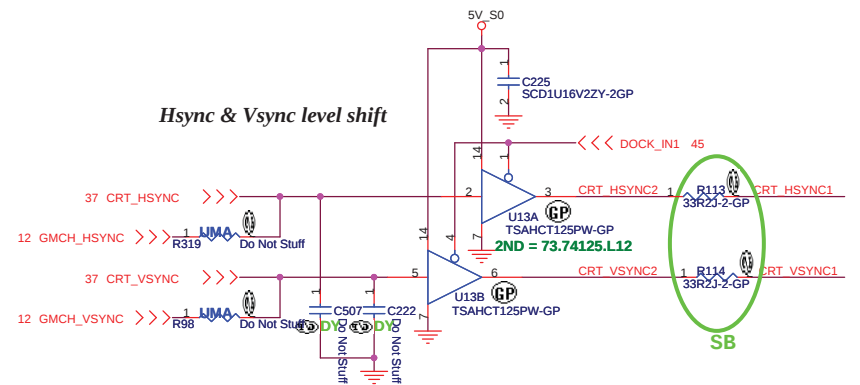
SB_0108_change 2nd source



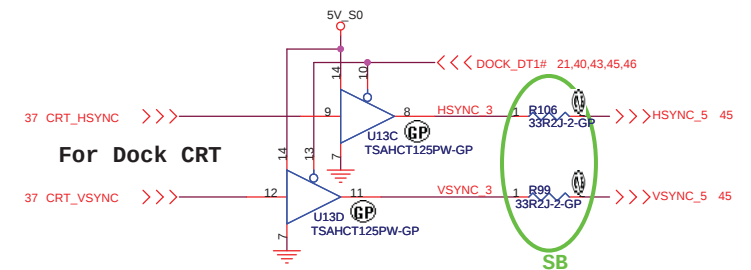
Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

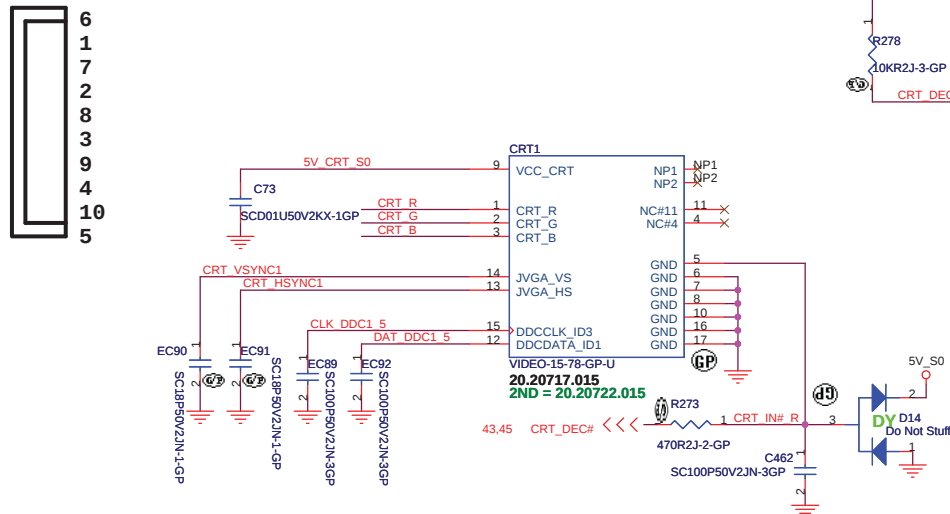
Hsync & Vsync level shift



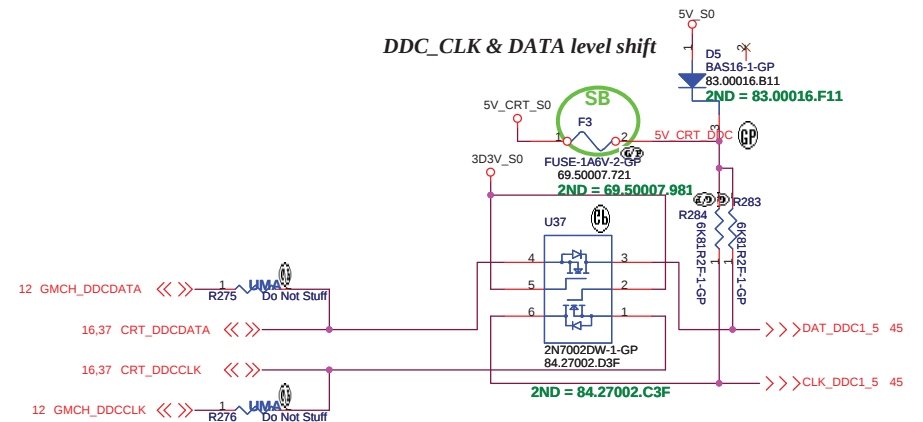
For Dock CRT



CRT I/F & CONNECTOR



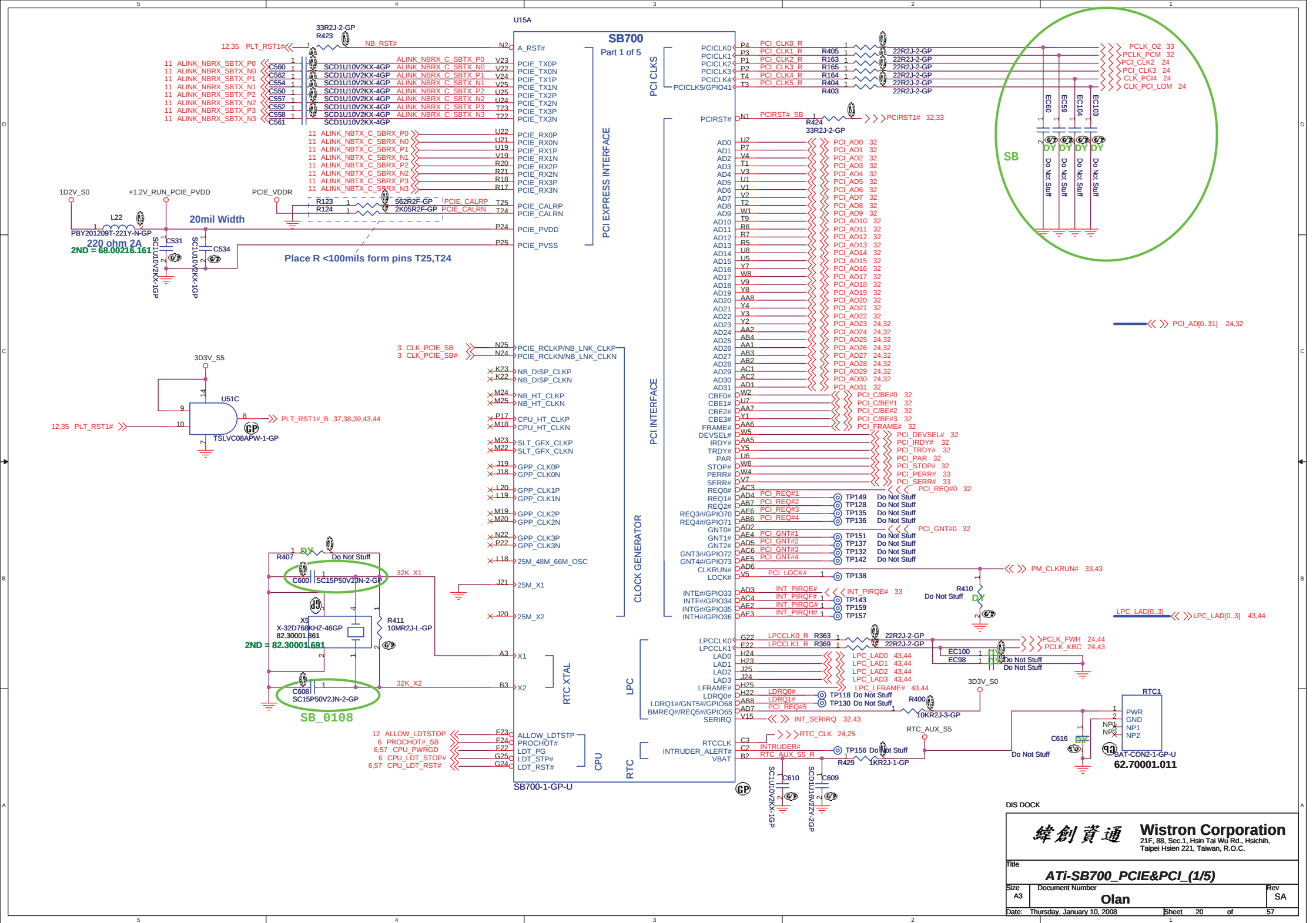
DDC_CLK & DATA level shift

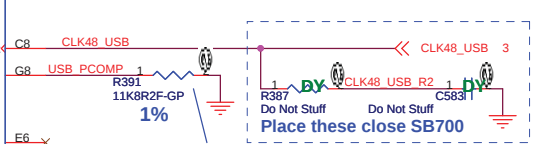
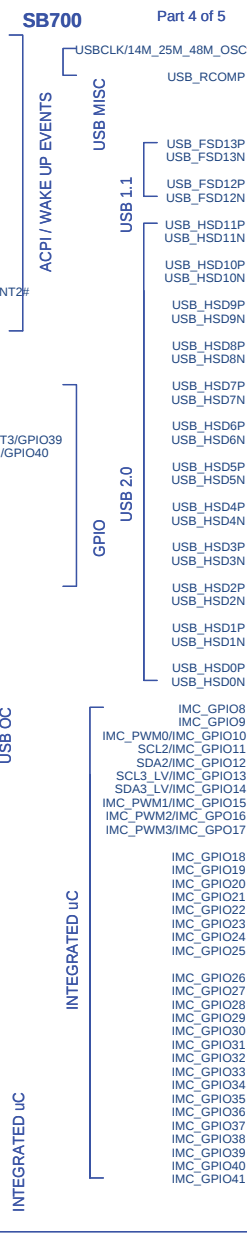


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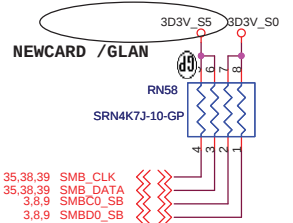
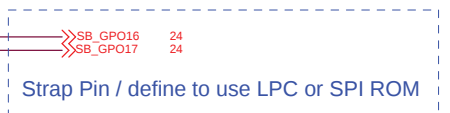
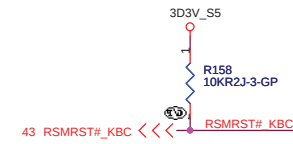
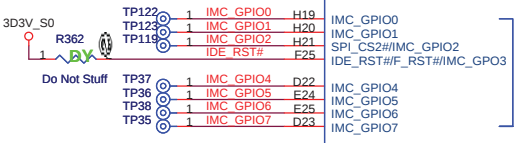
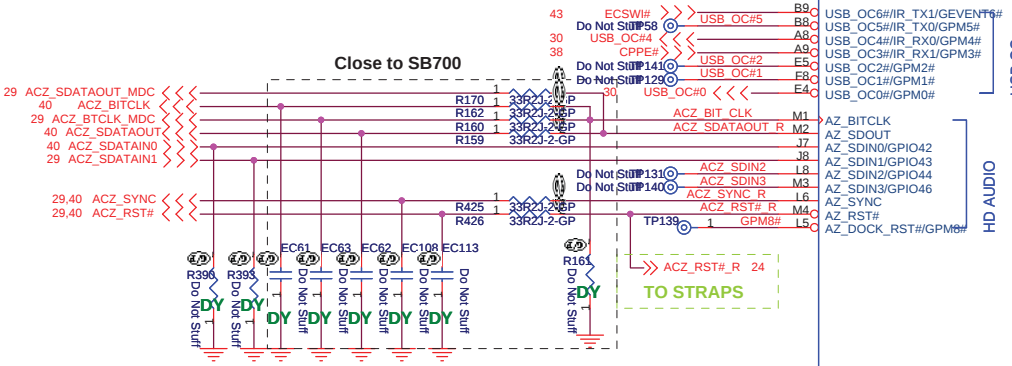
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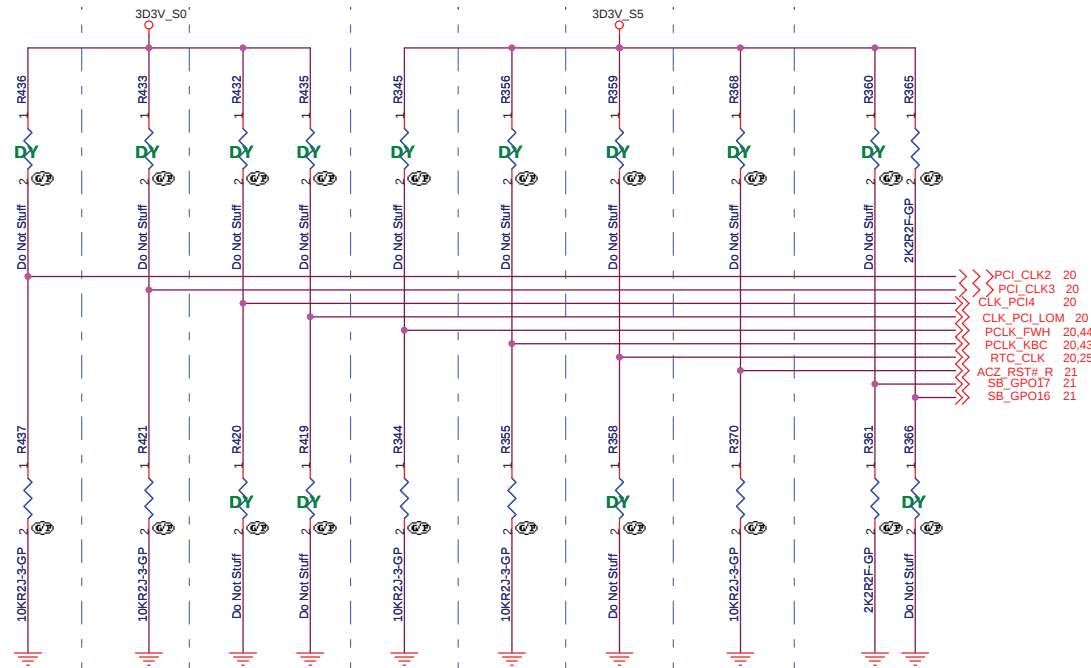


USB	
Pair	Device
11	MINIC1
10	WEBCAM
9	NEW1
8	USB2
7	NC
6	FP
5	Bluetooth
4	USB3
3	DOCK USB
2	NC
1	USB4
0	USB1

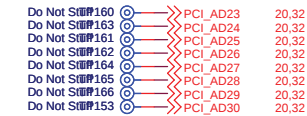


REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



DEBUG STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17, SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

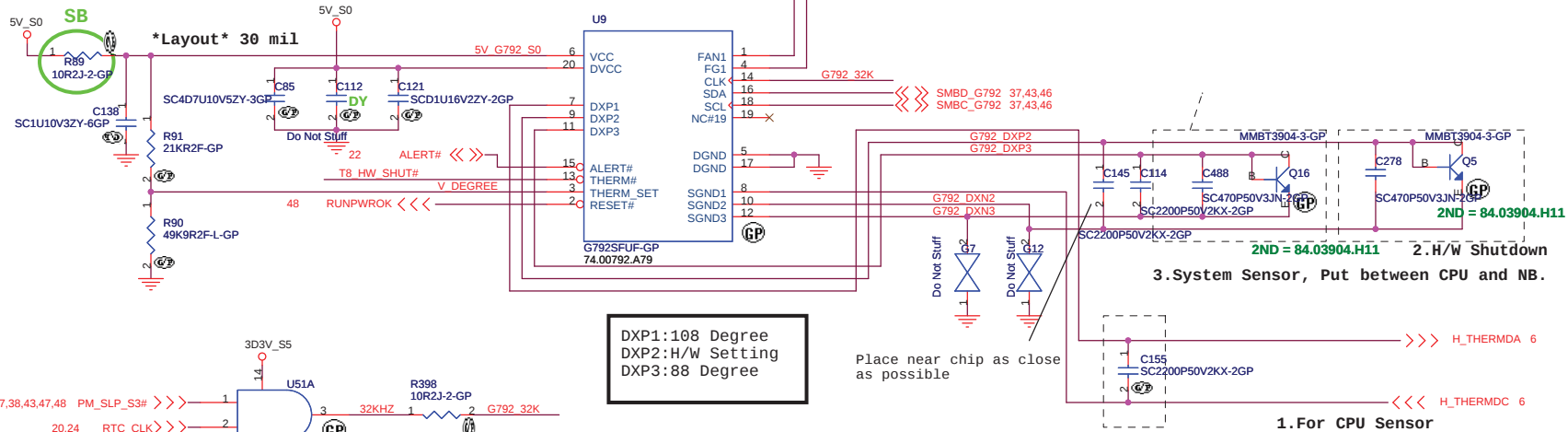
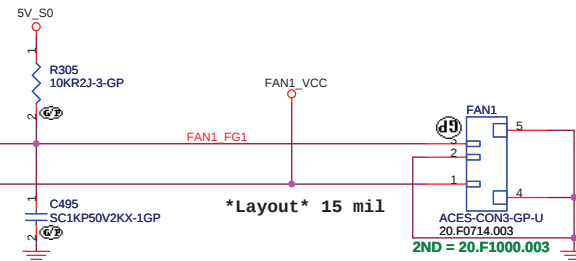
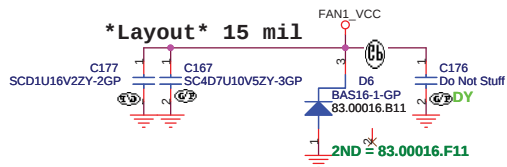
NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

DIS DOCK

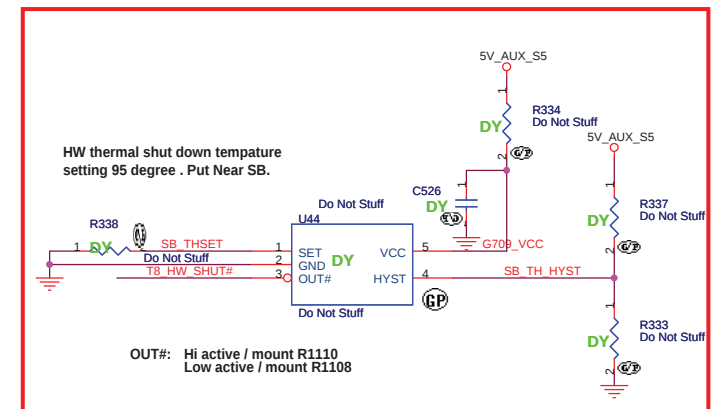
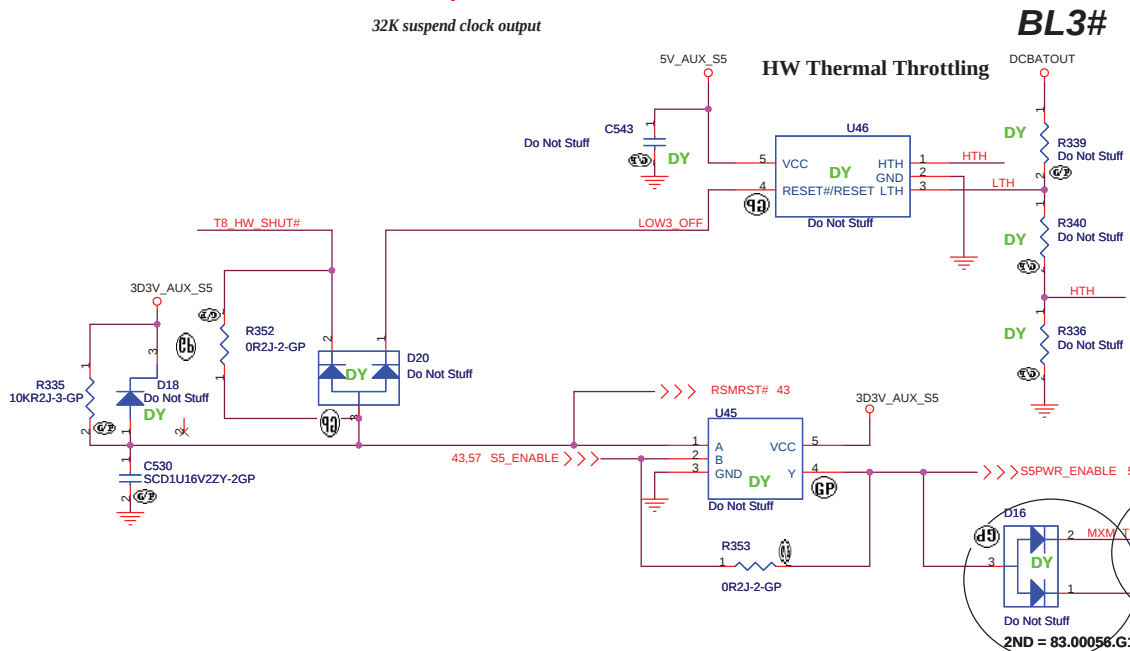
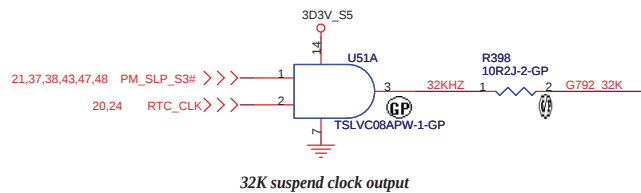
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
ATi-SB700 STRAPPING (5/5)			
Size	Document Number	Rev	SA
A3		Olan	
Date:	Thursday, January 10, 2008	Sheet	24 of 57



DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Place near chip as close as possible

1.For CPU Sensor

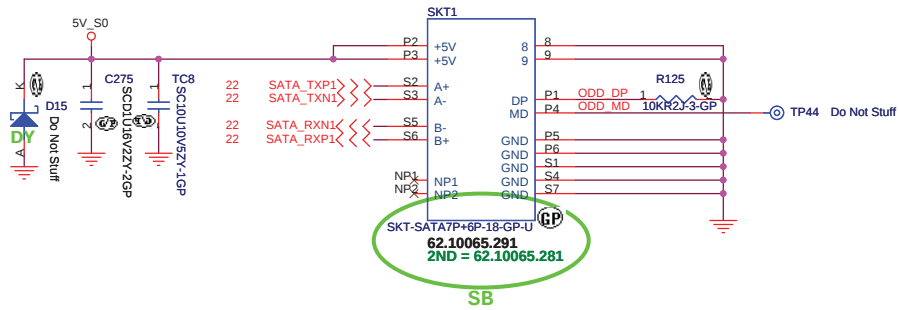


DIS DOCK

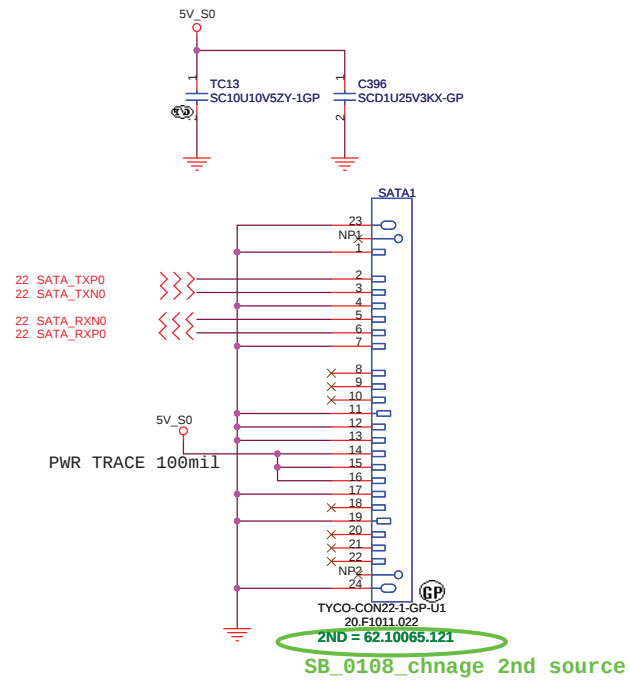
緯創資通 Wistron Corporation
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Title			
G792			
Size	Document Number	Rev	
A3	Olan	SA	
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ODD Connector



SATA HDD Connector



DIS DOCK

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

HDD

Size

Document Number

Olan

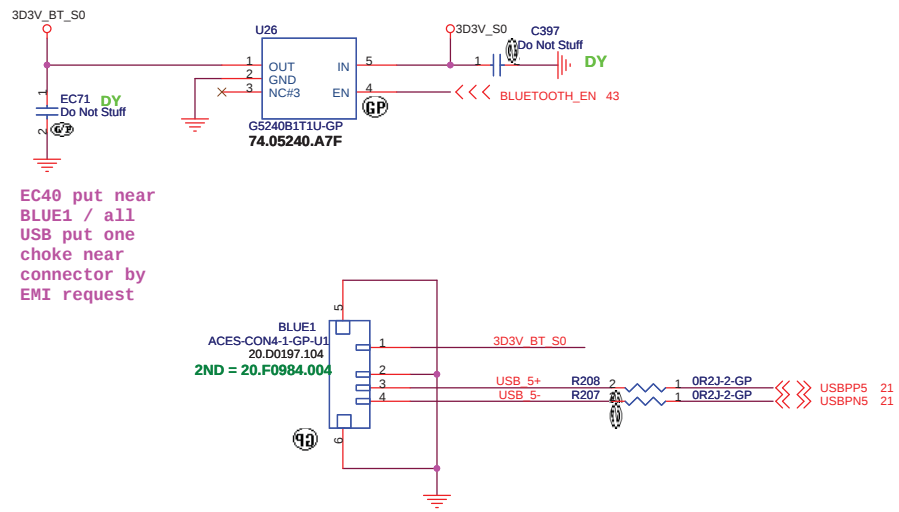
Rev

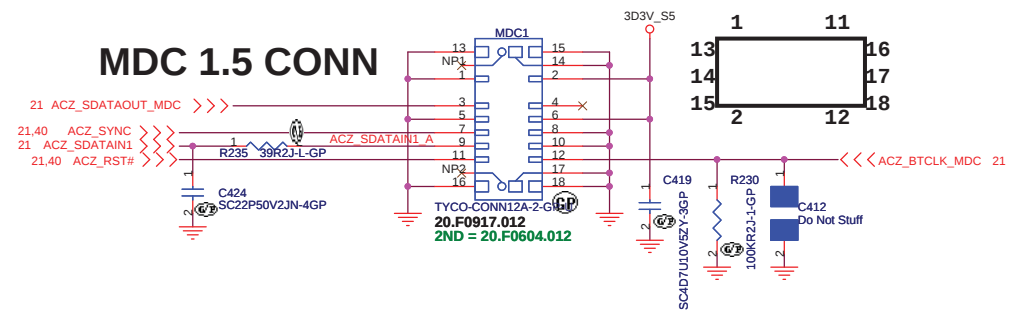
SA

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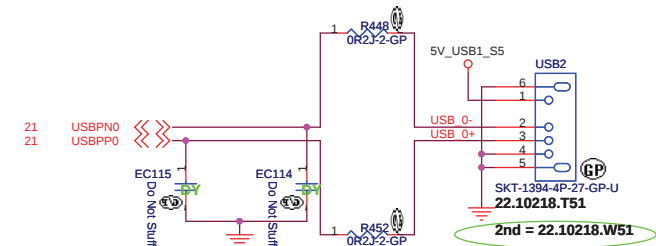
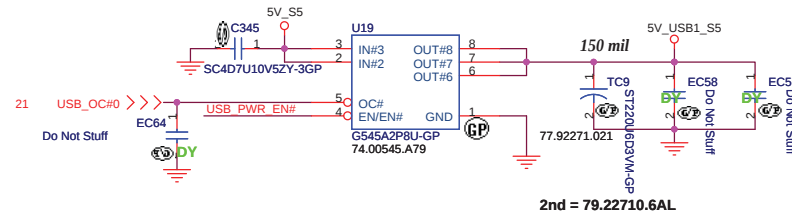
BLUETOOTH MODULE



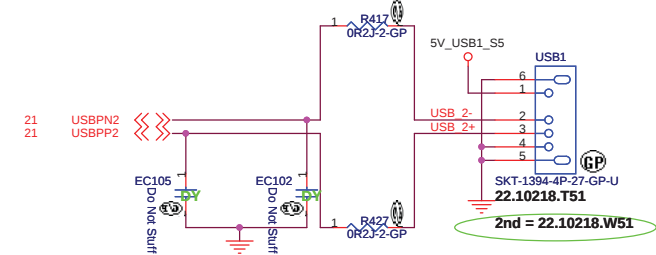


DIS DOCK

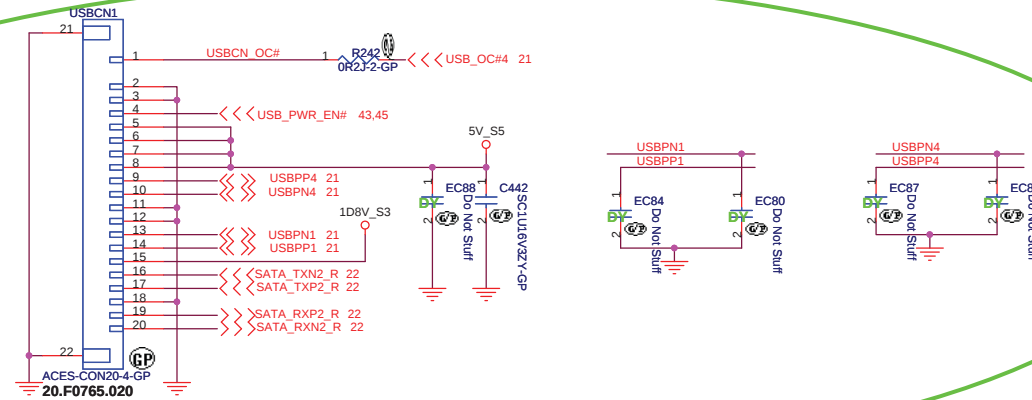
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
MDC			
Size	Document Number		Rev
	Olan		SA
Date:	Thursday, January 10, 2008		Sheet 29 of 57



SB_0108_change 2nd source



SB_0102

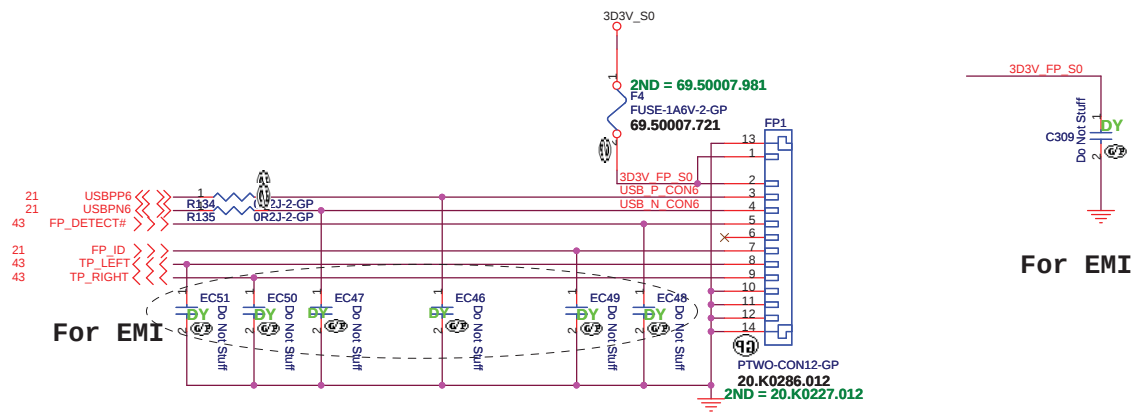


DIS DOCK

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Title			USB
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Finger printer



For EMI

DIS DOCK

緯創資通

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Title

Finger Printer

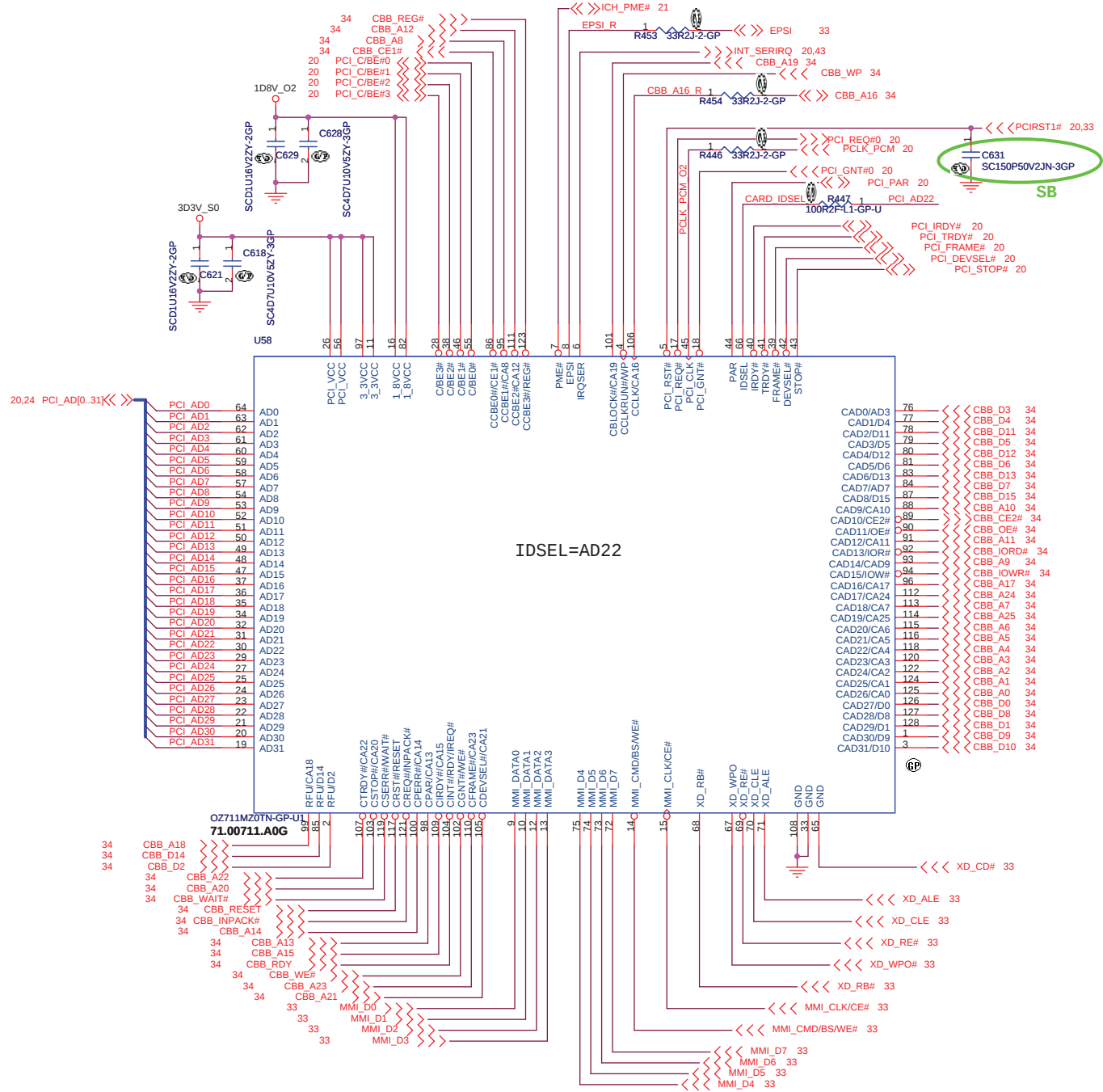
Size	Document Number
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Olan

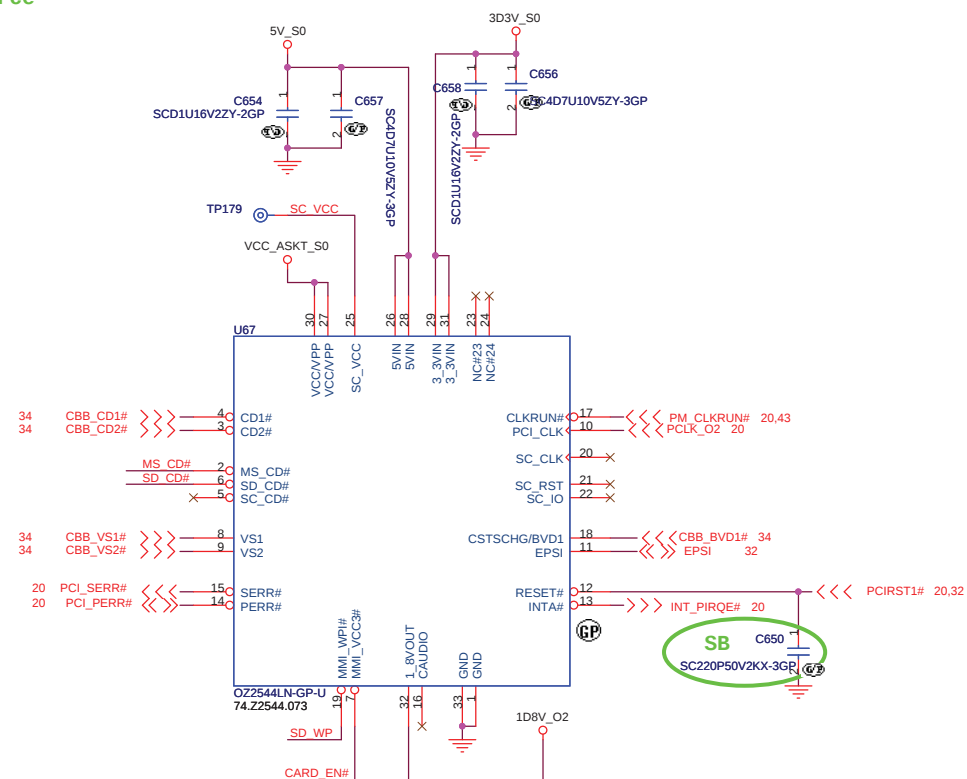
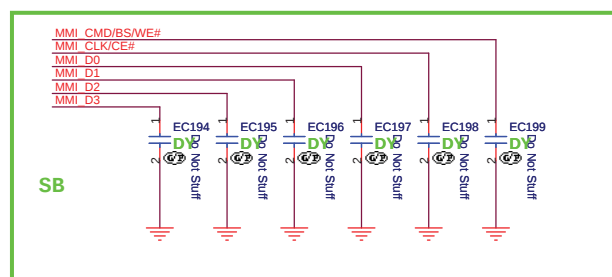
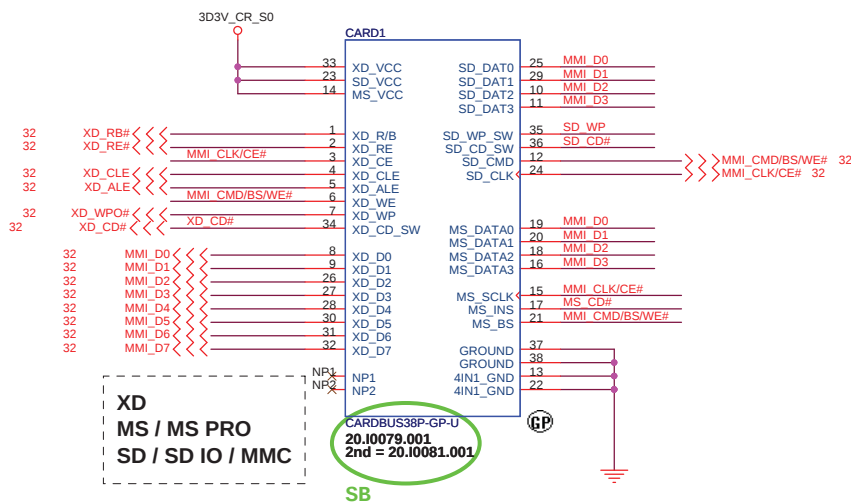
Rev	
SA	

Date: Thursday, January 10, 2008

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ENG Add 2nd source



DIS DOCK

緯創資通 **Wistron Corporation**
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Title	Author	Date	Page	Page	Page	Page	Page	Page	Page
Title	Author	Date	Page	Page	Page	Page	Page	Page	Page

Card Reader Connector

Size
A3

Document Number

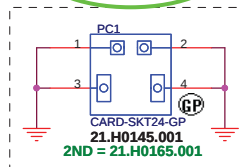
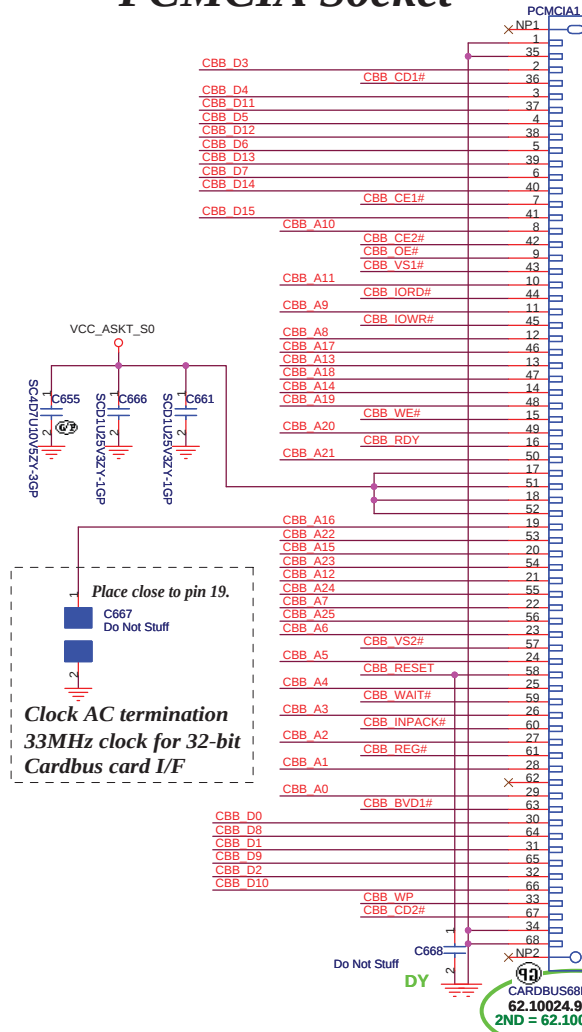
Olan

Rev	SA
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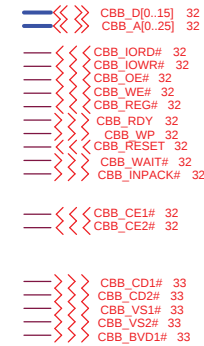
Date: Thursday, January 10, 2008

Sheet 33 of 57

PCMCIA Socket



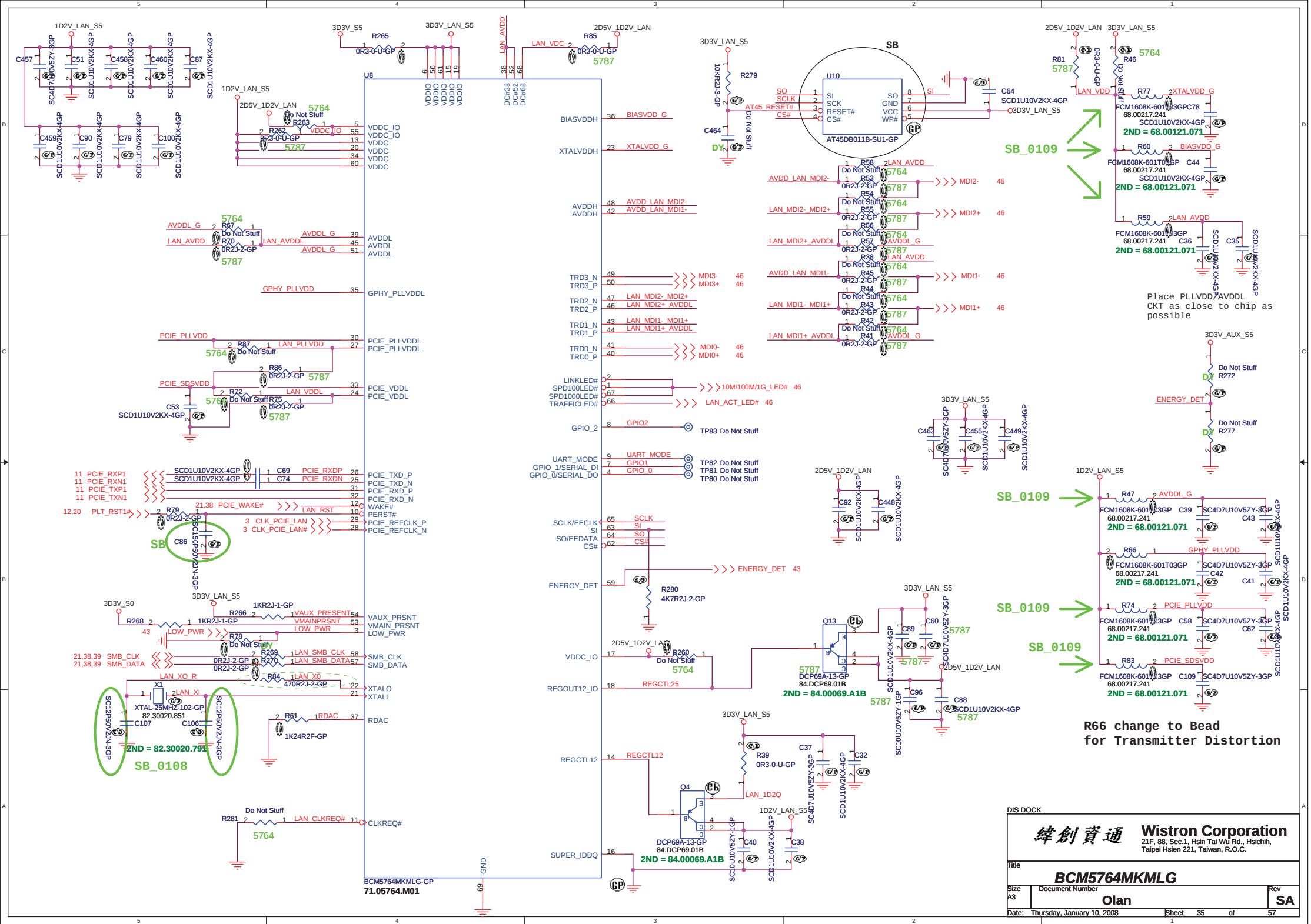
Cardbus I/F



DIS DOCK

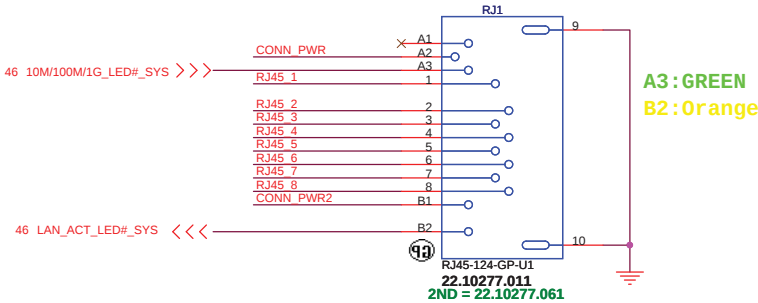
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCMCIA			
Size	Document Number		Rev
A3	Olan		SA
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- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

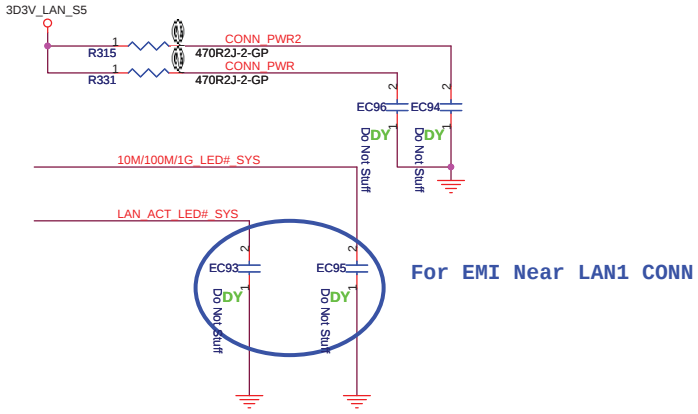
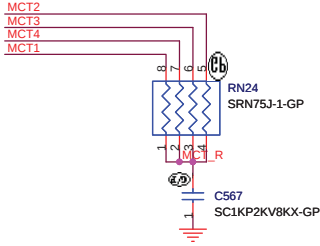
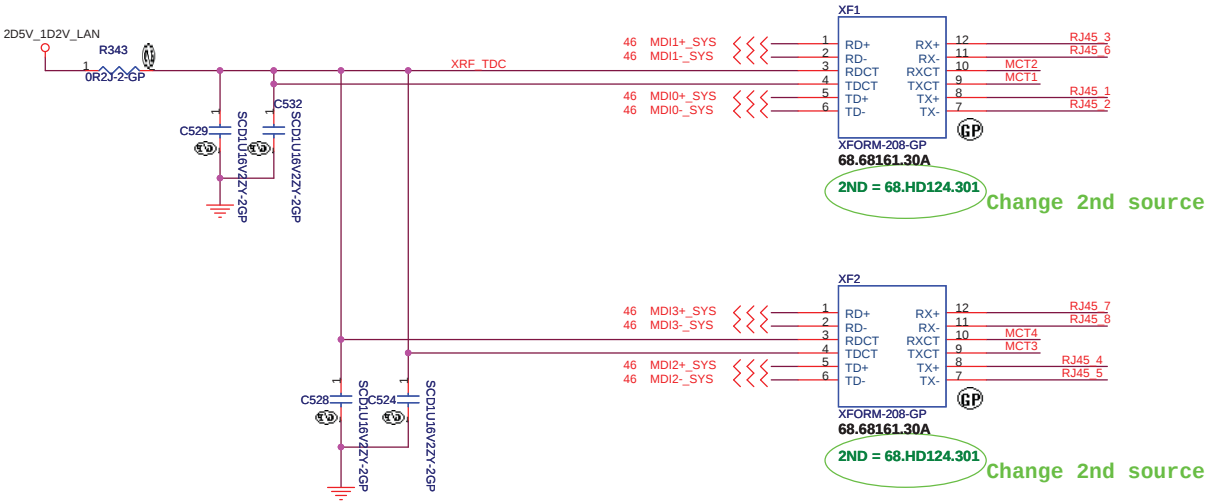
LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transferring data.

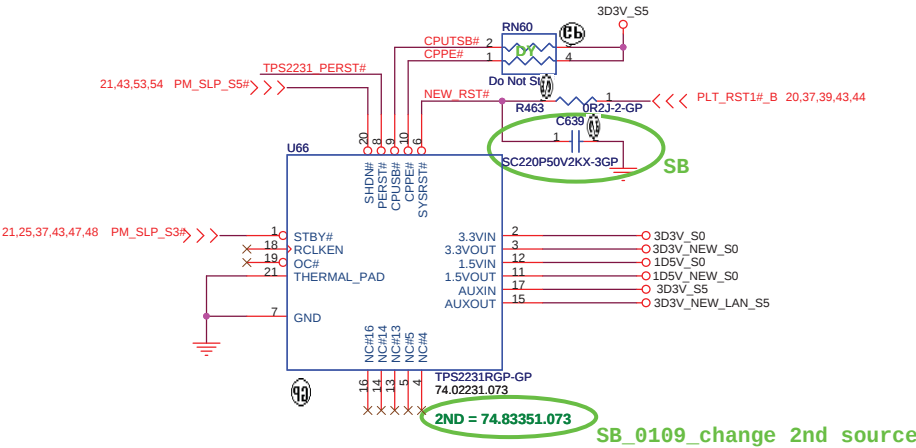
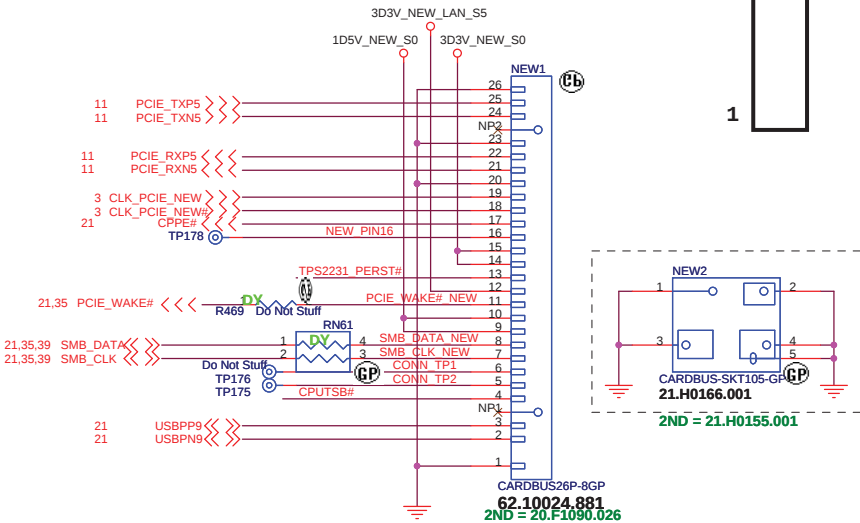
GIGA Lan Transformer



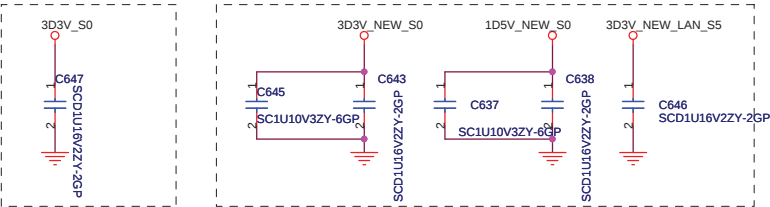
NEWCARD Connector

Reserve the symbol
for bottom side
connector

TOP VIEW

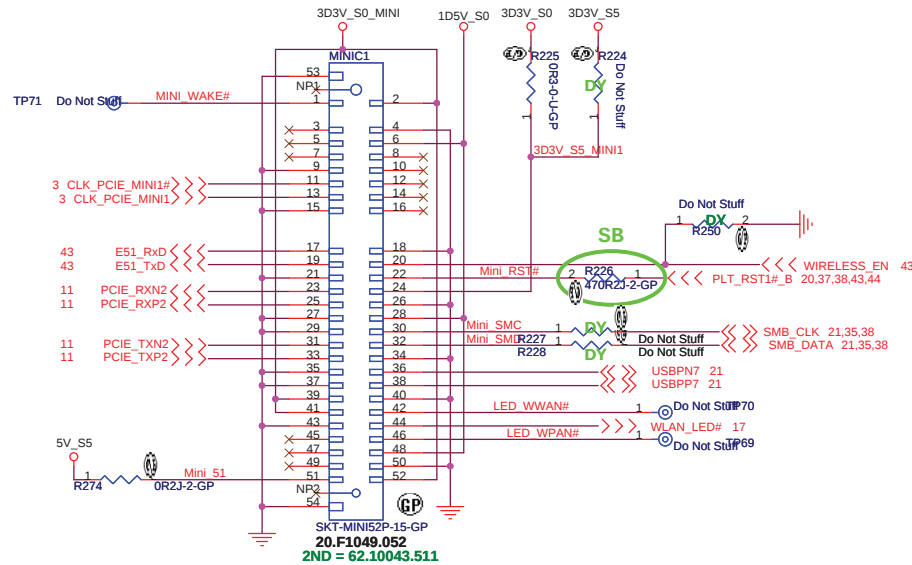


Place them Near to ChipPlace them Near to Connector

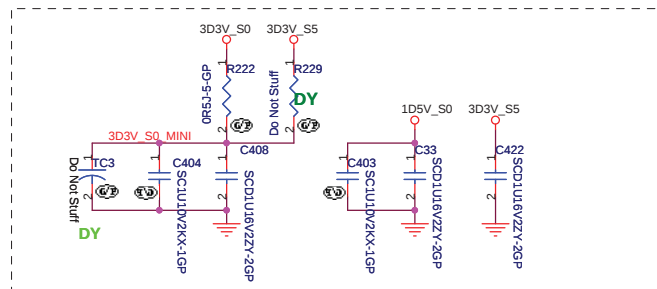


DIS DOCK		Wistron Corporation	
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Title		NEW CARD	
Size	Document Number	Rev	SA
A3		Olan	
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Mini Card Connector(WLAN)



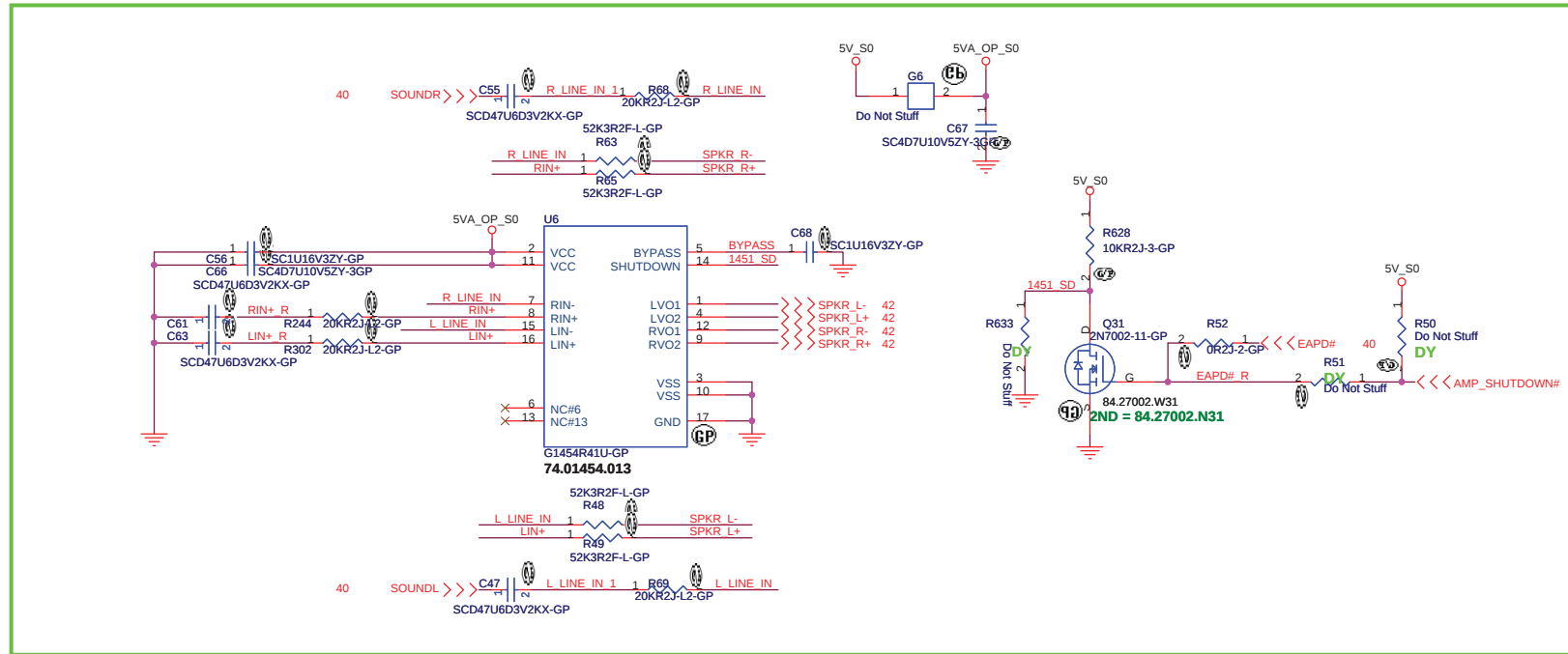
Place near MINIC1



DIS DOCK

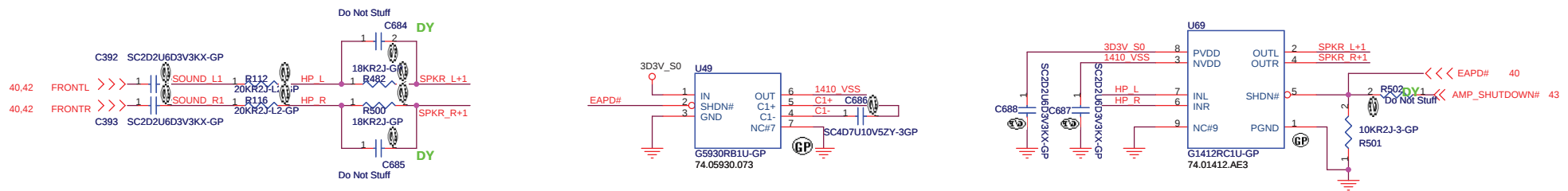
AUDIO OP AMPLIFIER

SB

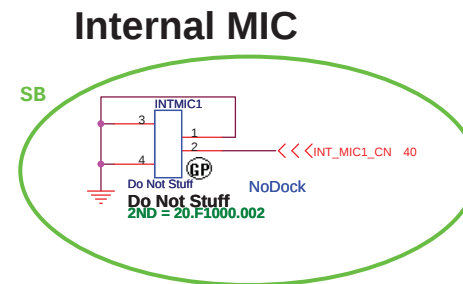
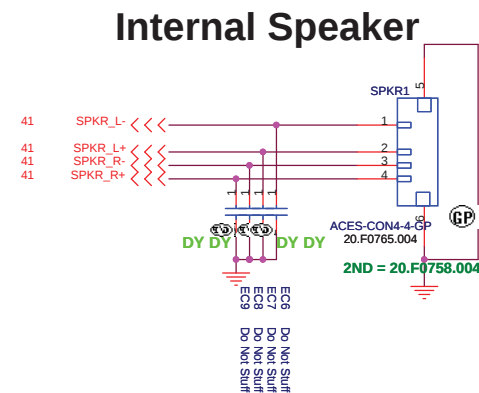
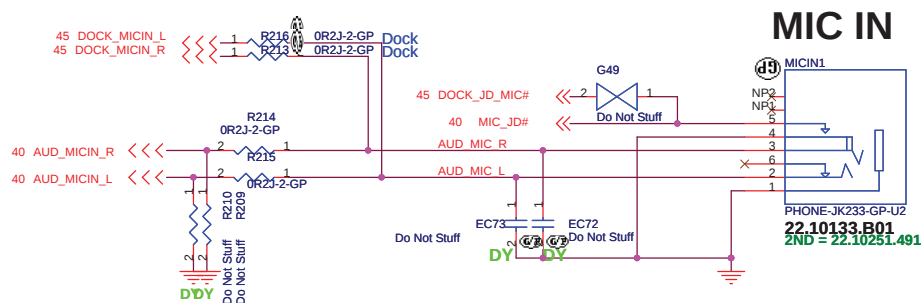
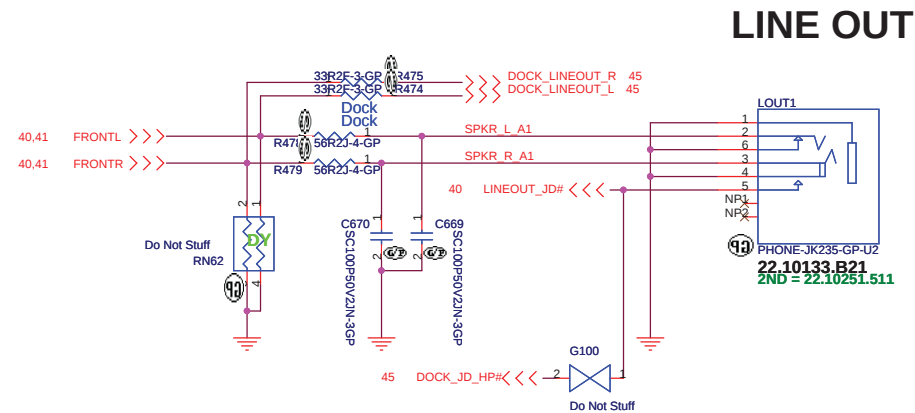
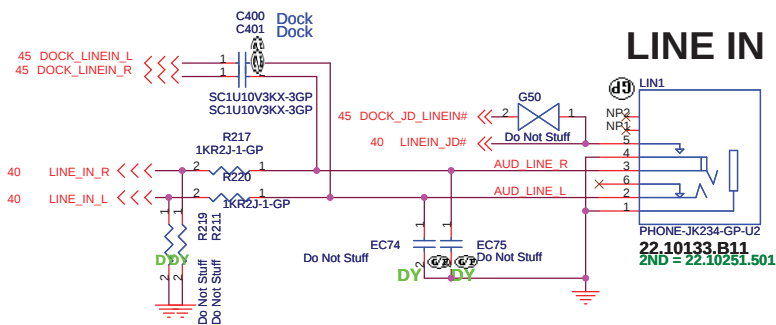


SB

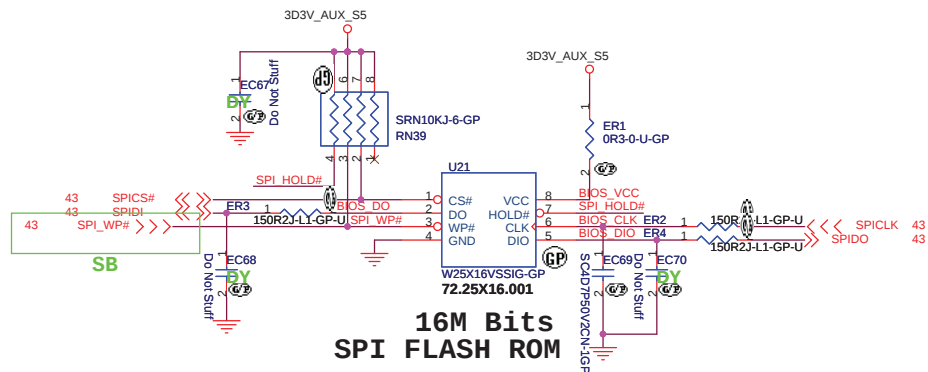
KBC_MUTE_GPI08



DIS DOCK



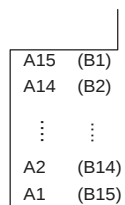
DIS DOCK



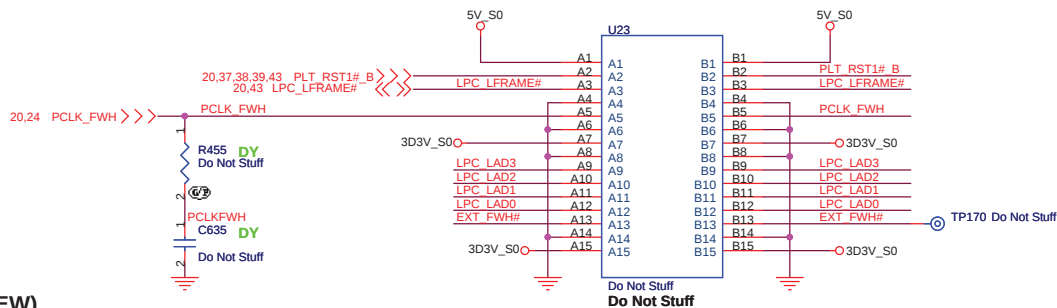
20,43 LPC_LAD[0..3] <<>> LPC_LAD[0..3]

GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW



(BOTTOM VIEW)

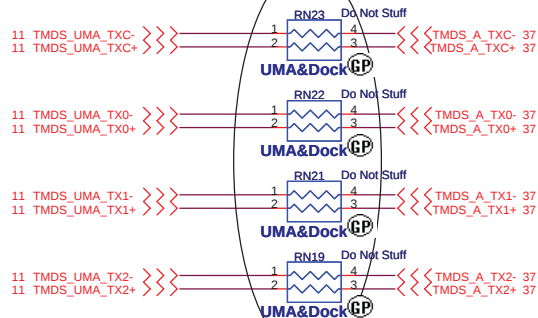
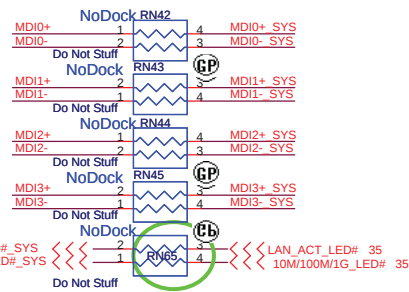
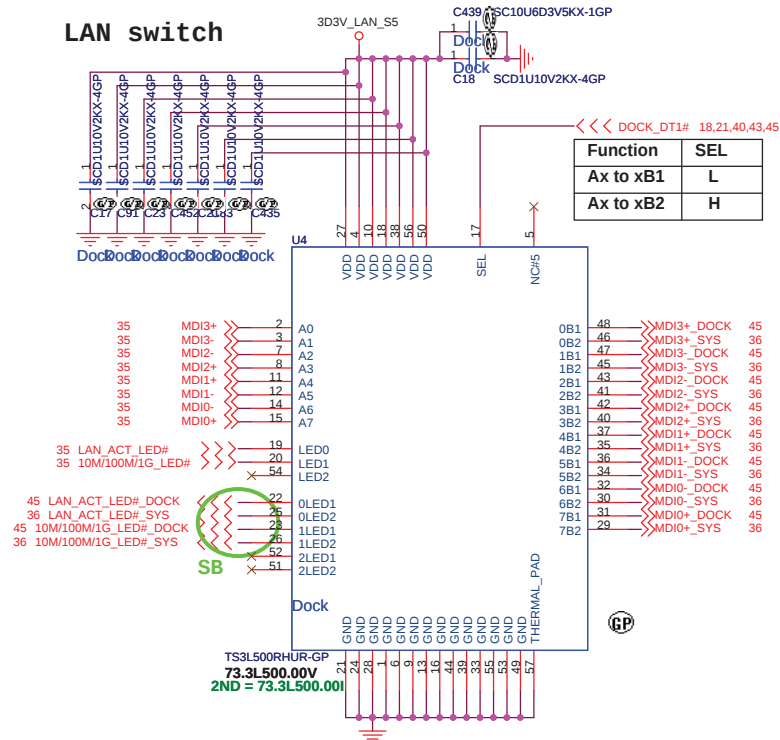


DIS DOCK

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

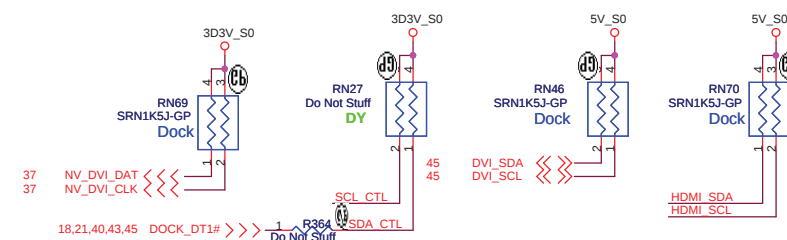
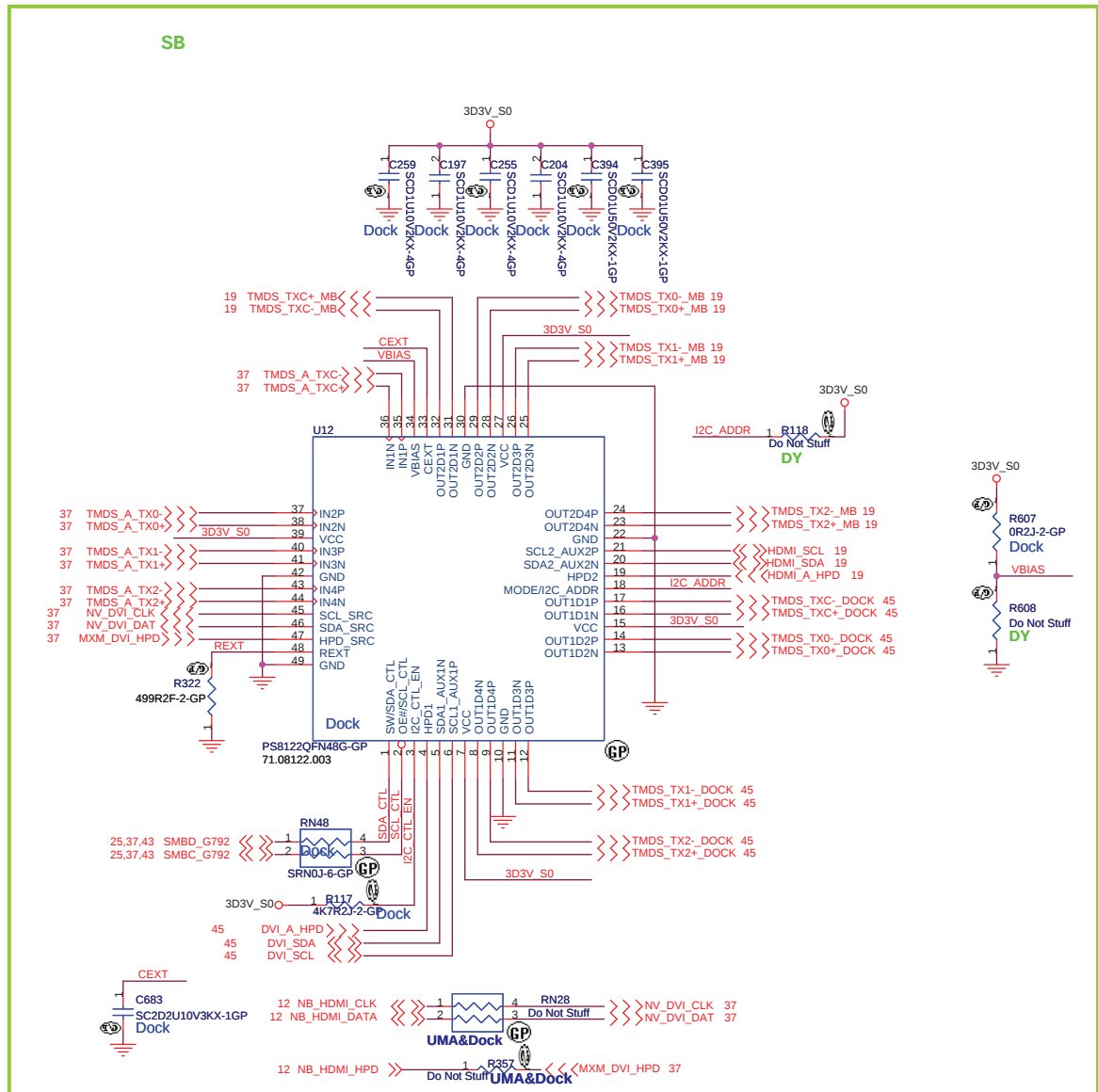
Title			BIOS	
Size	Document Number	Rev		SA
A3		Olan		
Date:	Thursday, January 10, 2008	Sheet	44	of 57

LAN switch



Place Near Switch

SB

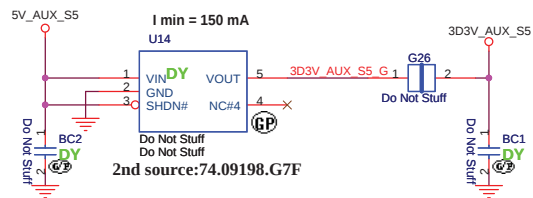


DIS DOCK

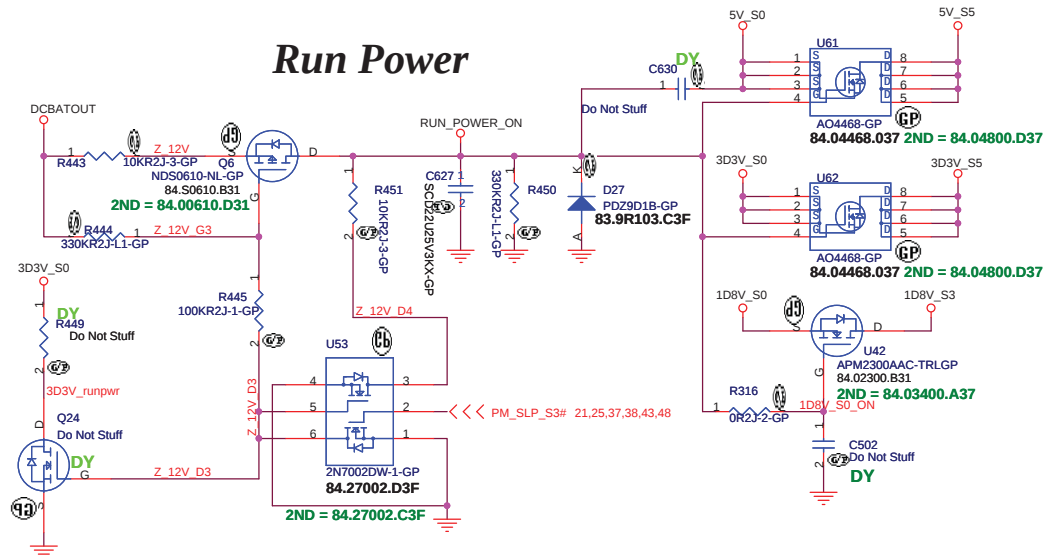
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			EASY PORT4(2/2)	
Size	Document Number	Rev		SA
A3	Olan			
Date:	Thursday, January 10, 2008	Sheet	46	of 57

Aux Power 3D3V_AUX_S5



Run Power

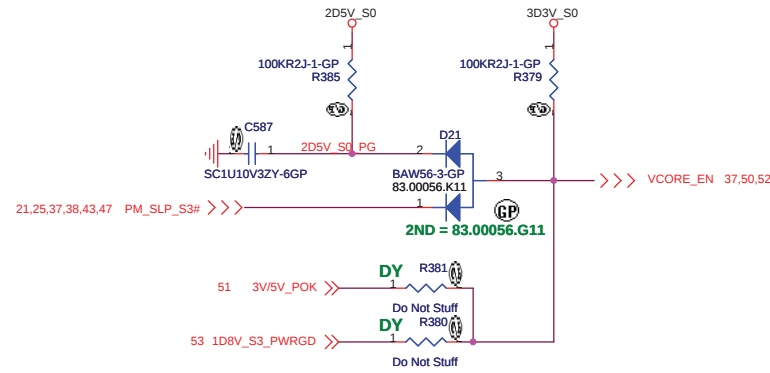


DIS DOCK

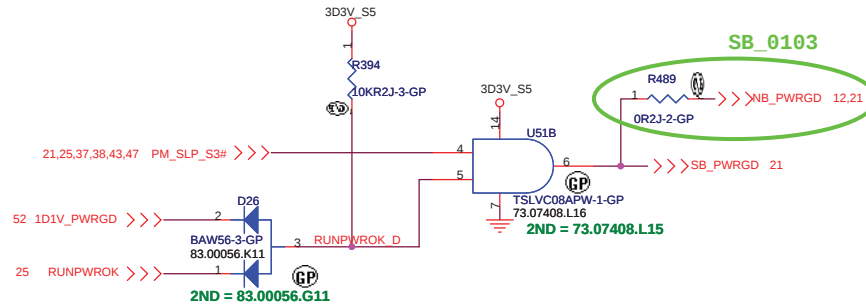
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	<i>RUN POWER and 3D3V_AUX_S5</i>
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Size A3	Document Number Olan	Rev SA
Date: Thursday, January 10, 2008		Sheet 47 of 57



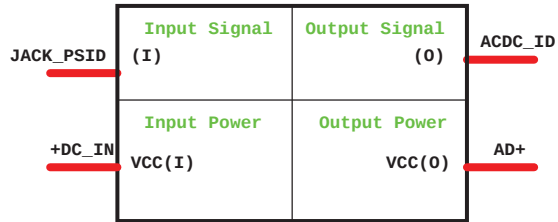
P/H @ 1D8V_S3 PAGE



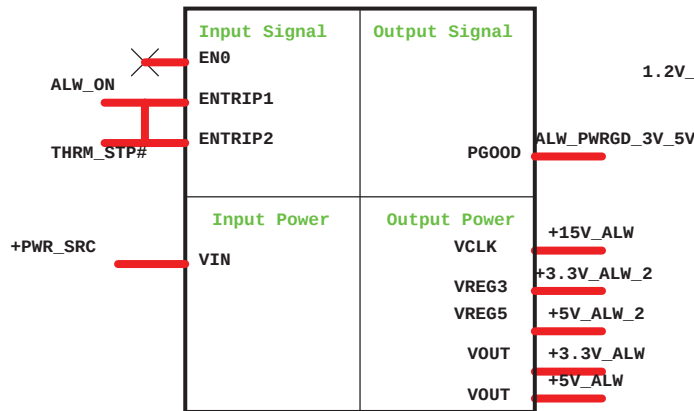
DIS DOCK

緯創資通		Wistron Corporation	
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POWER ON LOGIC			
Title	Document Number		Rev
Size A3	Date: Thursday, January 10, 2008		SA
Sheet 48 of 57			

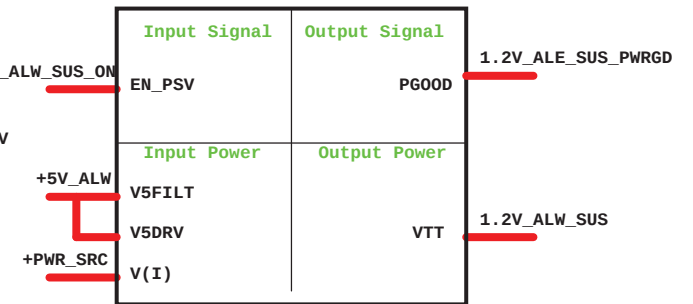
Adapter



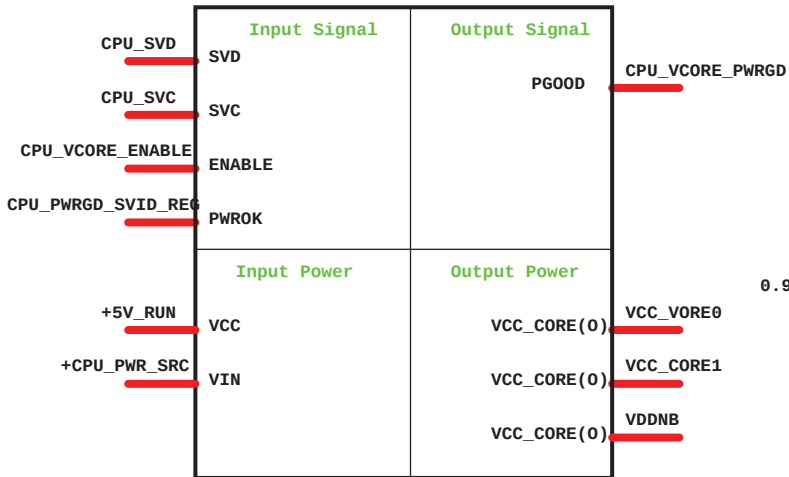
SN0608098



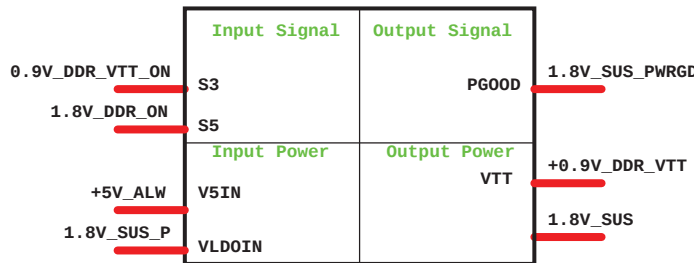
DCDC 1D2V(TPS5117)



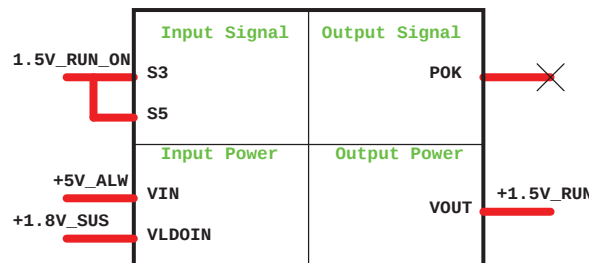
CPU_CORE ISL6265HRTZ



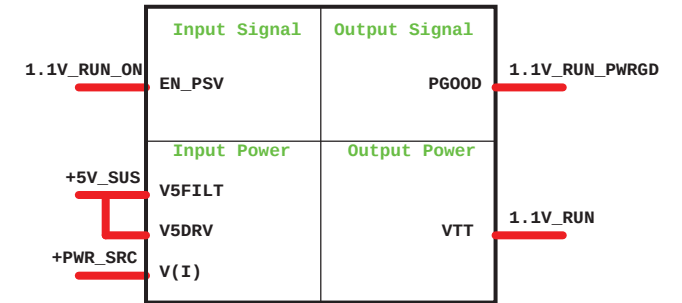
1D8V/0D9V(TPS5116)



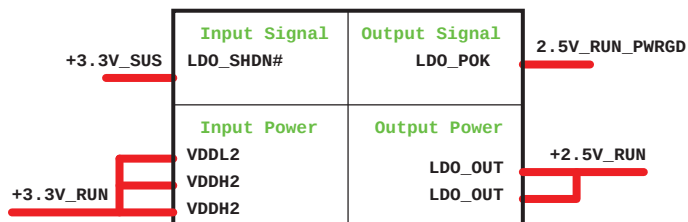
1.5V_LDO



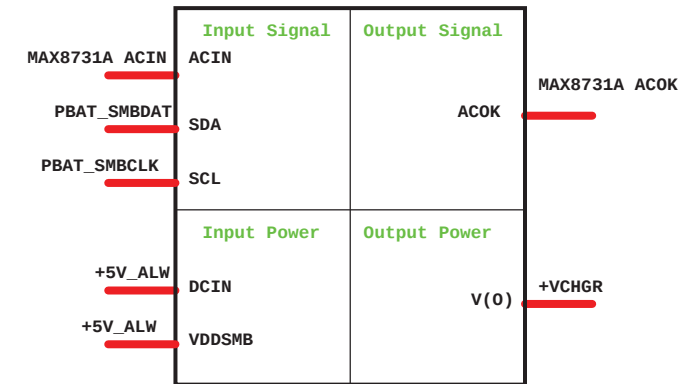
1D1V(TPS5117)



2.5V LDO EMC4002



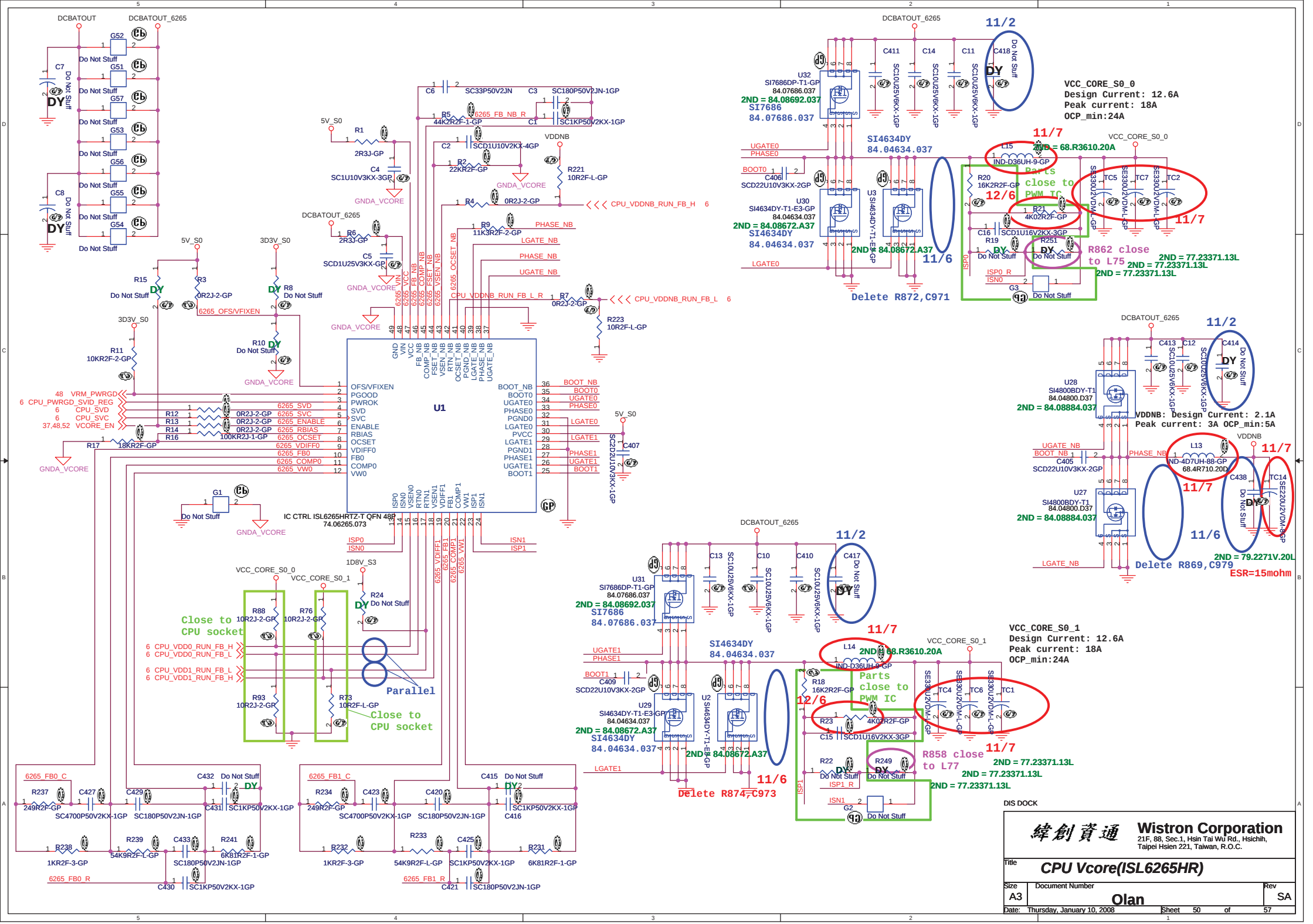
CHARGER BQ24745

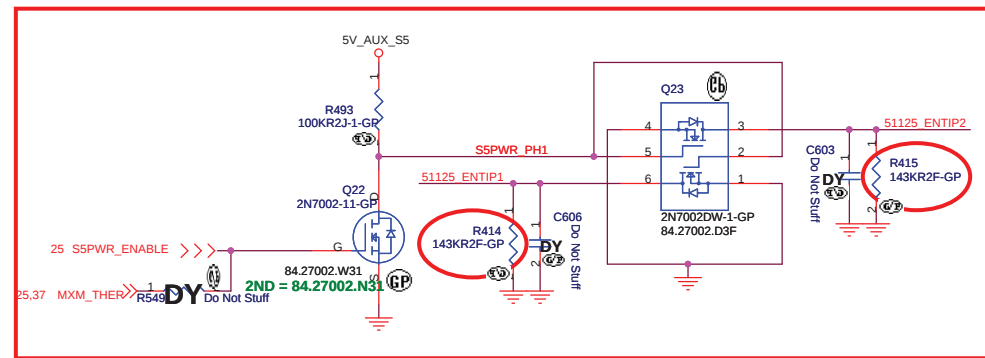


DIS DOCK

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title Power Block Diagram		
Size A3	Document Number Olan	Rev SA
Date: Thursday, January 10, 2008	Sheet 49 of 57	



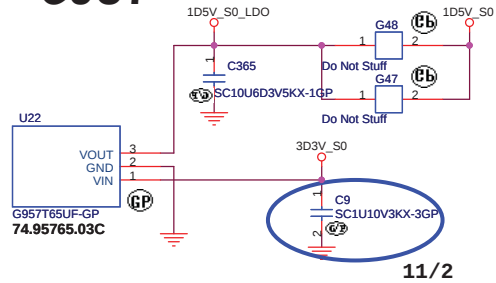
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Design Current = 6A
Max Current = 7A
OCP min = 10A

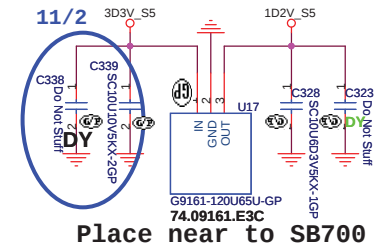


57

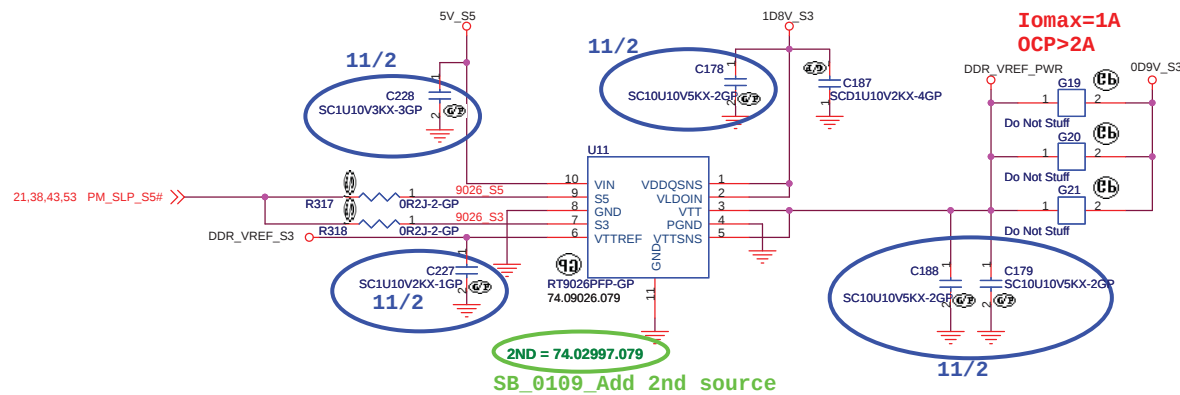
G957
1D5V_S0
Iomax=1A



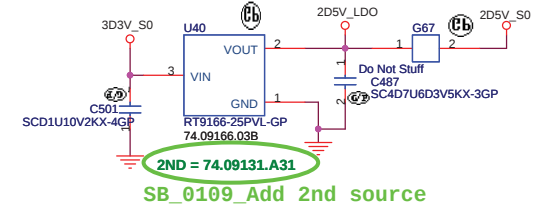
1D2V_S5
Iomax=400mA



Place near to SB700



2D5V_S0
Iomax=0.3A **2D5V/300mA**



DIS DOCK

緯創資通 **Wistron Corporation**
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Title			0D9V&2D5V&1D25V&1D5V	
Size	Document Number		Rev	
A3			SA	
Date:	Thursday, January 10, 2008		Sheet	54 of 57



Adaptor in to generate DCBATOUT

Jeff modify 20071031



BATTERY CONNECTOR



緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

AD/BATT CONN

Size
A4

Document Number

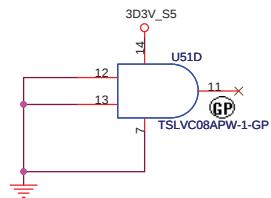
Olan

Rev
SA

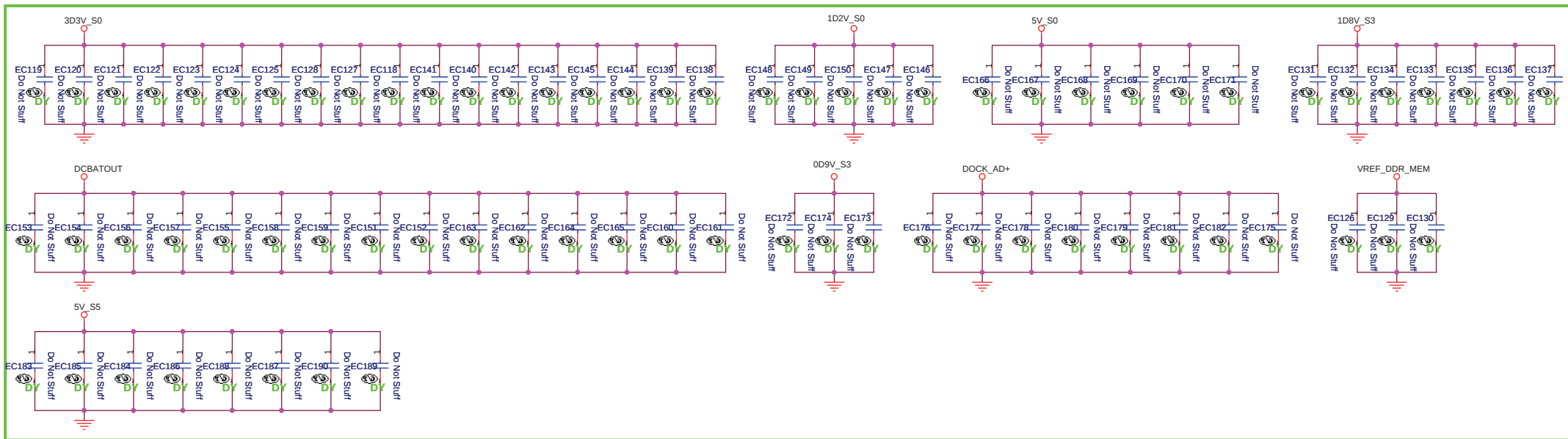
Date: Thursday, January 10, 2008

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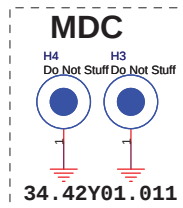
57



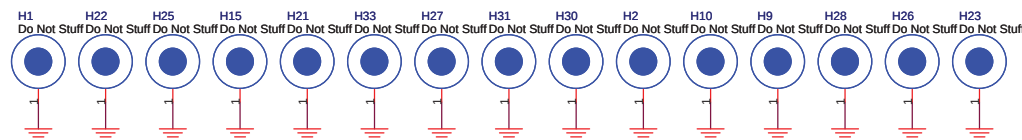
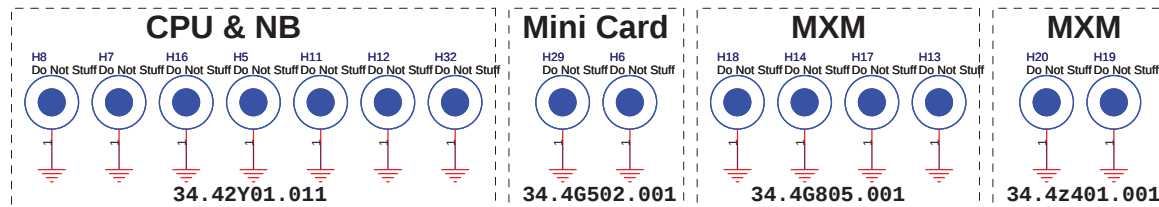
SB



STAND OFF ON TOP

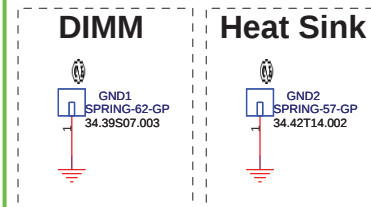


STAND OFF ON BOTTOM



SB

SPRING ON BOTTOM



Check test point

- 3D3V_S0 TP180 Do Not Stuff
- 3D3V_AUX_S5 TP4 Do Not Stuff
- 3D3V_S5 TP183 Do Not Stuff
- 5V_S5 TP186 Do Not Stuff
- 21.43 PM_PWRBTN# TP185 Do Not Stuff
- 6.20 CPU_PWRGD TP184 Do Not Stuff
- 25.43 SS_ENABLE TP181 Do Not Stuff
- 6.20 CPU_LDT_RST# TP182 Do Not Stuff

Test Point放在Dimm Door打開可量測處

DIS DOCK

緯創資通 Wistron Corporation		
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Title		
EMI/Spring/Boss		
Size A3	Document Number	Rev SB
Date: Thursday, January 10, 2008		
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