ZR6E SYSTEM BLOCK DIAGRAM

BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA

REV:A

X'TAL 14.318MHz
CLOCK GENERATOR
ICS:
SELGO: SLG8SP512TTR
P2

Penryn 479
uFCPGA
P3, P4

Thermal Sensor
(G780-1P81U) P3

Fan Driver
(G991) P24

FSB
667/800 MHz

DDR2 PWR TPS51116 P35
CHARGER ISL6251 P31
THERMAL PROTECTION P38
3/5V SYS PWR ISL6237 P32
DISCHARGER P37
CPU CORE PWR OZ8116LN P34
VGA CORE OZ8118 P36
+1.05V UP6111AQDD P33

NVIDIA N10M-GE1
VRAM DDRII 1GB P17-P23

PCIE 16X
EXT_LVDS
EXT_CRT

SWITCH CIRCUIT P23

CRT P23
LVDS P23

DDRII
SO-DIMM 0
SO-DIMM 1
P16

Dual Channel DDR2
667/800 MHz

NB Cantiga
(GM45/ PM45/ GL40)
P5, P6, P7, P8, P9, P10, P11

LVDS
RGB
INT_LVDS
INT_CRT

X4 DMI interface

HDD (SATA) *1 P24

ODD (SATA) P24

SATA0
SATA1

SB ICH9M
P12,P13,P14,P15

X'TAL 32.768KHz

PCI-Express
PCIE-1

Mini Card WLAN P25

USB 2.0
USB8

Ext USB Port x 2 USB 0,1 P25
Int USB Port x 1 USB 7 P25
Bluetooth USB5 P25
CCD USB11 P23

Azalia

PCIE-6
X'TAL 25MHz

Media Cardreader (RTS5159) USB2 P29

Atheros Giga-LAN (AR8131) P27

LPC

Audio CODEC (CX20561) P26

EC (WPC775LDG) P30
X'TAL 32.768KHz

Card Reader Connector P29

Transformer P28

RJ45 P28

SPI ROM P30

Touch Pad P24

K/B COON. P30

Audio Amplifier G1453L P26
MIC Jack P26
Int. MIC P26

Int. Speaker P26

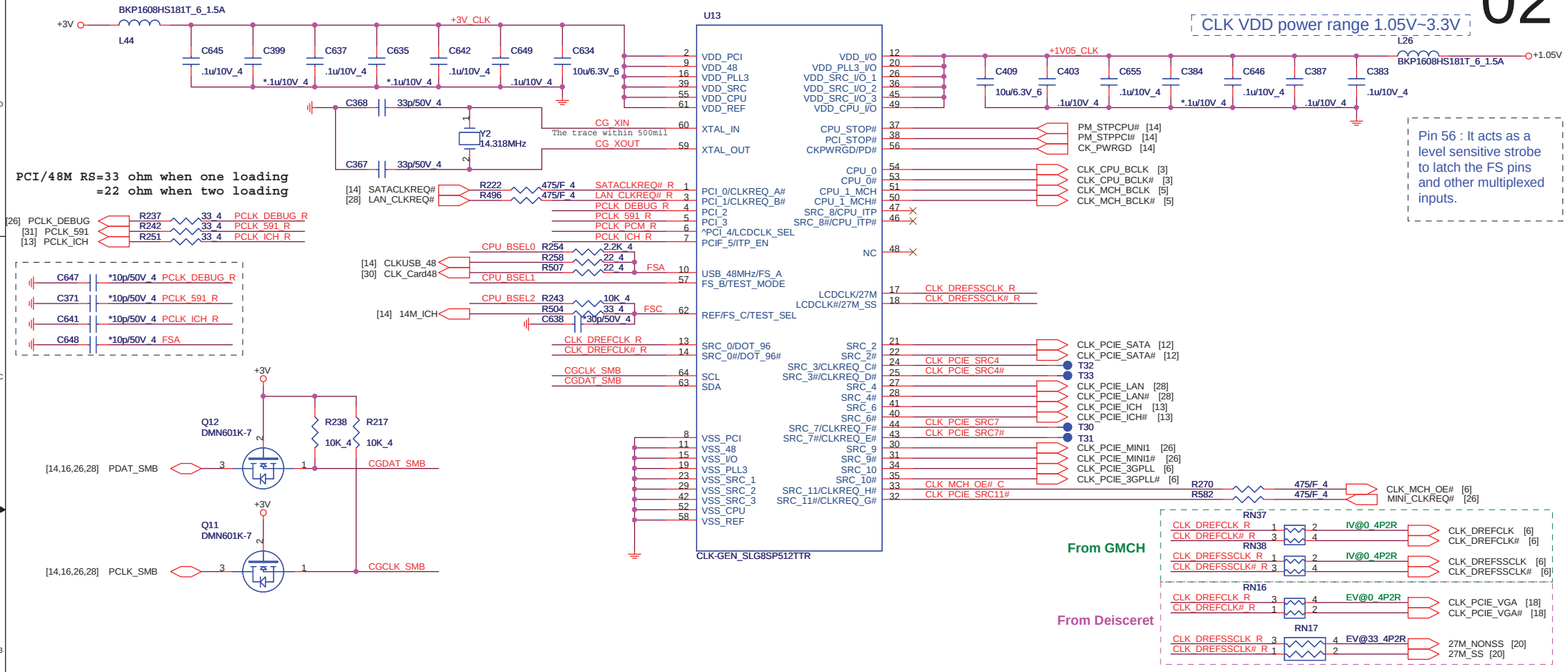
Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	Block Diagram	1A
Date: Tuesday, May 19, 2009	Sheet 1 of 39	

Clock Generator (CLK)

02

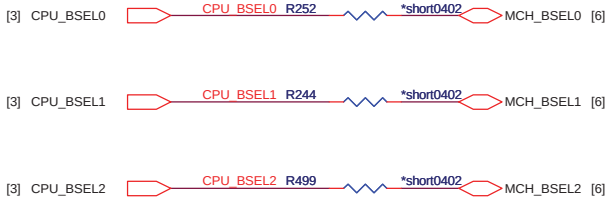
CLK VDD power range 1.05V~3.3V



Pin 56 : It acts as a level sensitive strobe to latch the FS pins and other multiplexed inputs.

CPU Clock select

Pin 10/57/62 : For Pin CPU frequency selection



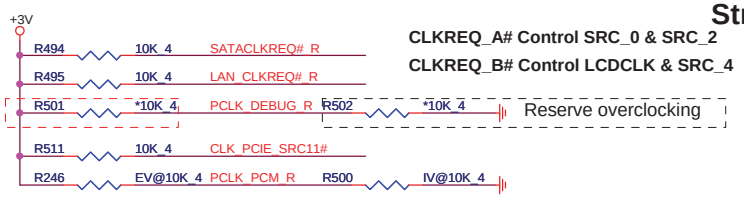
BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

Strap table

CLKREQ_A# Control SRC_0 & SRC_2

CLKREQ_B# Control LCDCLK & SRC_4



Pin 6 : For Pin 13/14 and 17/18 selection
0 = LCDCLK & DOT96 for internal graphic controller support
1 = 27M & 27M_SS &SRC_0 for external graphic controller support

PCLK_ICH_R R503 10K_4

Pin 7 : For Pin 46/47 selection
1 = CPU_ITP
0 = SRC_8

CLOCK GENERATOR

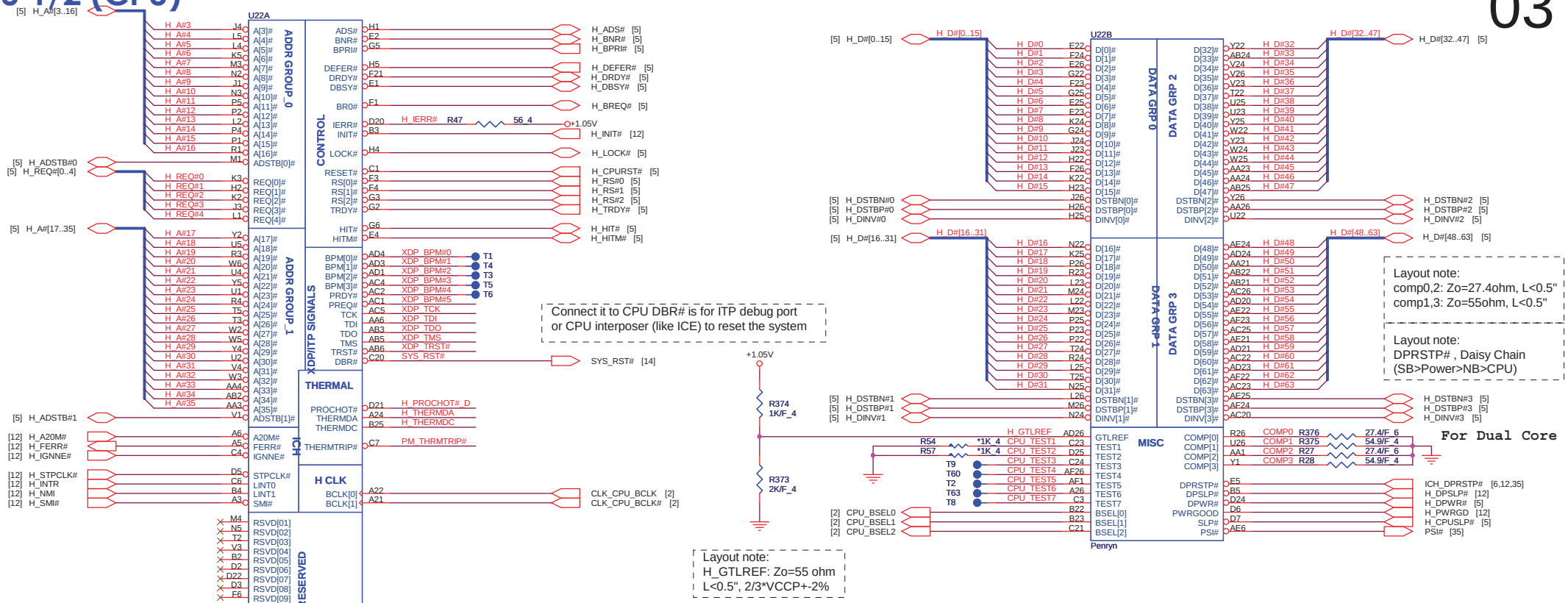
Quanta Computer Inc.

PROJECT : ZR6E

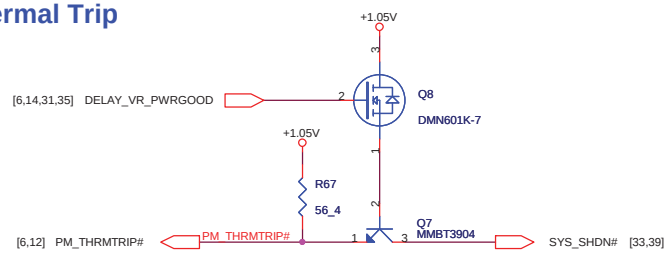
Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date: Tuesday, May 19, 2009	Sheet 2 of 39	

CPU 1/2 (CPU)

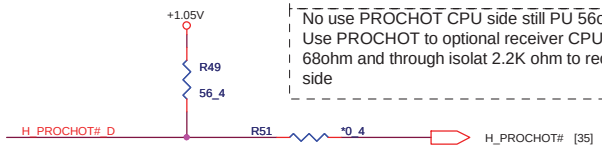
03



Thermal Trip



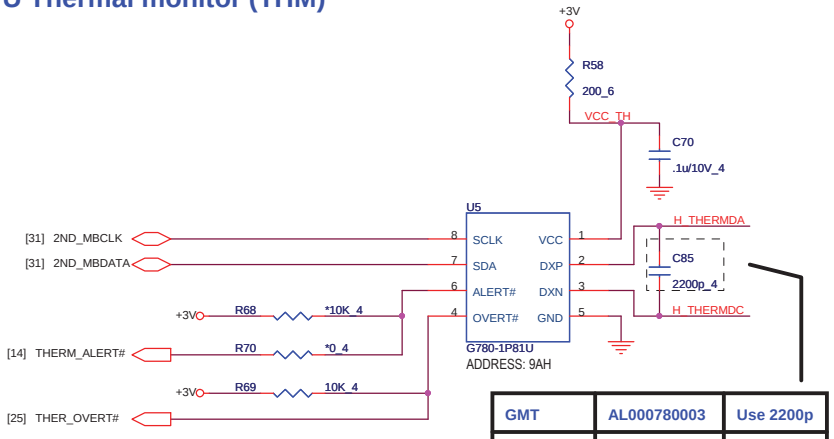
Processor hot



No use Thermal trip CPU side still PU 56ohm. Use Thermal trip can share PU at SB side

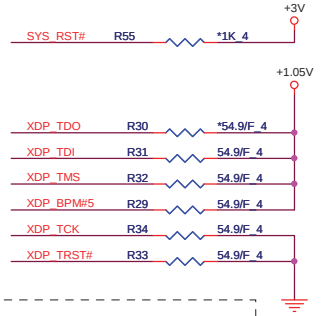
No use PROCHOT CPU side still PU 56ohm. Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side

CPU Thermal monitor (THM)



GMT	AL000780003	Use 2200p
WINDBOND	AL83L771001	Check

XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

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PROJECT : ZR6E

Size	Document Number	Rev
	CPU Host Bus	1A
Date: Tuesday, May 19, 2009	Sheet 3 of 39	

CPU 2/2 (CPU)

04

U22D

Penryn

U22C

Penryn

VCC_CORE

VCC_CORE

VCC:38A (Low power type)
VCC:47A (Standard type)

Layout Note:
Inside CPU center cavity in 2 rows

VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)

Layout Note:
Place these parts reference to Intel demo board.

+1.05V

+1.5V

VCCA:130mA

Layout Note:
Z0=27.4,PU/PD L<1"

Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2

Quanta Computer Inc.

PROJECT : ZR6E

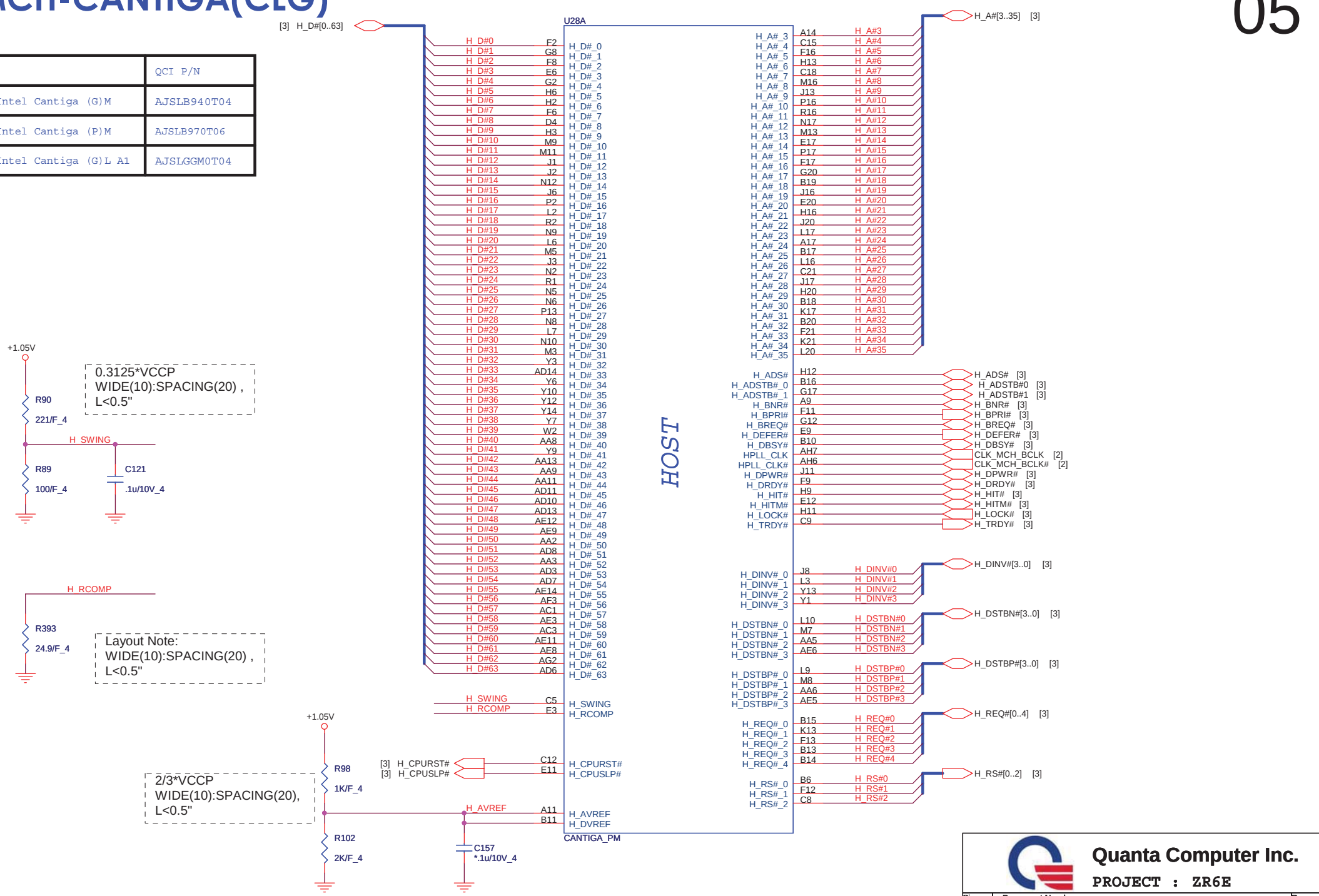
Size	Document Number	Rev
	CPU Power	1A

Date: Tuesday, May 19, 2009 Sheet 4 of 39

GMCH-CANTIGA(CLG)

05

	QCI P/N
Intel Cantiga (G)M	AJSLB940T04
Intel Cantiga (P)M	AJSLB970T06
Intel Cantiga (G)L A1	AJSLGGM0T04



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	GMCH HOST	1A

Date: Tuesday, May 19, 2009 Sheet 5 of 39

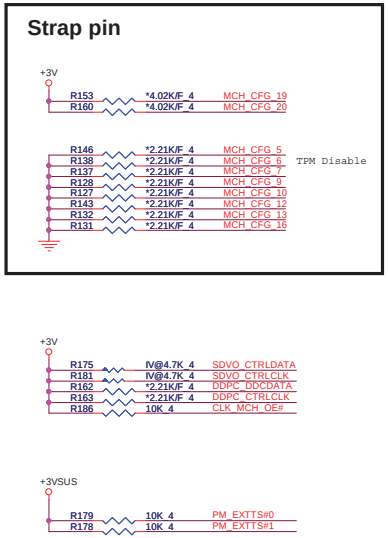
GMCH-CANTIGA(CLG)

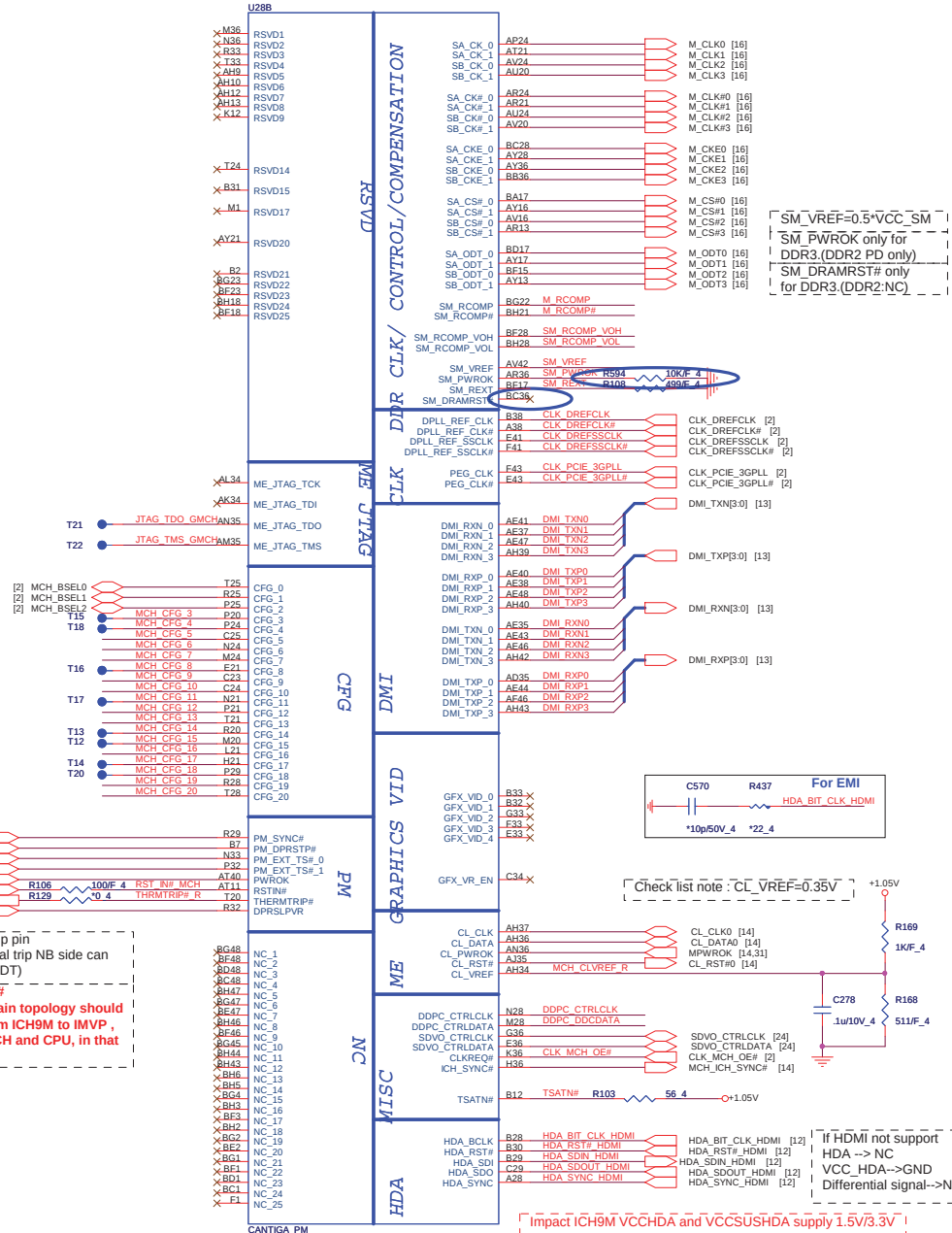
IV@
EV@

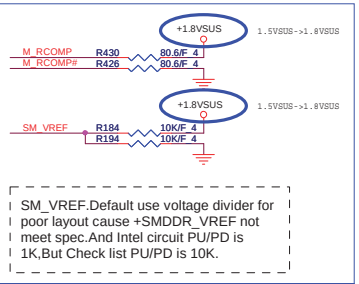
Strap table

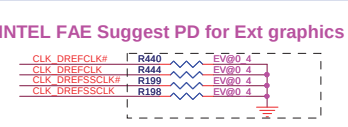
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

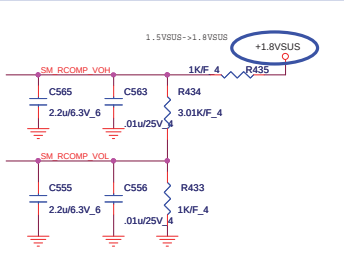
Strap pin

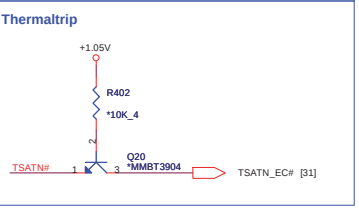












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PROJECT : ZR6E			
Size	Document Number		Rev
	GMCH DMI		1A
Date: Tuesday, May 19, 2009		Sheet 6 of 39	

GMCH-CANTIGA(CLG)

07

IV@
EV@
SP@

IV&EV Dis/Enable setting

If LVDS no use,all signal can NC

U28C

[24] L_BKLT_CTRL
[24] INT_LVDS_BLON
R171 IV@10K_4 L_CTRL_CLK
+3V
R172 IV@10K_4 L_CTRL_DATA
[24] INT_LVDS_EDIDCLK
[24] INT_LVDS_EDIDDATA
[24] INT_LVDS_DIGON
R195 IV@2.4K/F_4 LVDS_IBG
[24] INT_TXLCLKOUT-
[24] INT_TXLCLKOUT+
[24] INT_TXLOUT0-
[24] INT_TXLOUT1-
[24] INT_TXLOUT2-
[24] INT_TXLOUT0+
[24] INT_TXLOUT1+
[24] INT_TXLOUT2+

L_BKLT_CTRL
L_BKLT_EN
L_CTRL_CLK
L_CTRL_DATA
L_DDC_CLK
L_DDC_DATA
L_VDD_EN
LVDS_IBG
LVDS_VBG
LVDS_VREFH
LVDS_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSB_CLK#
LVDSB_CLK
LVDSA_DATA#_0
LVDSA_DATA#_1
LVDSA_DATA#_2
LVDSA_DATA#_3
LVDSA_DATA_0
LVDSA_DATA_1
LVDSA_DATA_2
LVDSA_DATA_3
LVDSB_DATA#_0
LVDSB_DATA#_1
LVDSB_DATA#_2
LVDSB_DATA#_3
LVDSB_DATA_0
LVDSB_DATA_1
LVDSB_DATA_2
LVDSB_DATA_3

SDVT

SP@ TV_A/B/C
For IV: 75ohm
For EV:0ohm

R147 SP@75_4 INT_TV_COMP
R136 SP@75_4 INT_TV_Y/G
R151 SP@75_4 INT_TV_C/R

TVA_DAC
TVB_DAC
TVC_DAC
TV_RTN
TV_DCONSEL_0
TV_DCONSEL_1

[24] INT_CRT_BLU
[24] INT_CRT_GRN
[24] INT_CRT_RED
[24] INT_CRT_DDCCLK
[24] INT_CRT_DDCDAT
[24] INT_HSYNC
R158 IV@30.1_4 HSYNC_G
CRTIREF
[24] INT_VSYNC
R165 IV@30.1_4 VSYNC_G

CRT_BLUE
CRT_GREEN
CRT_RED
CRT_IRTN
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_TVO_IREF
CRT_VSYNC

HSYNC/VSYNC serial R place close to NB

CANTIGA_PM

PCI-EXPRESS GRAPHICS

VGA

L<0.5" , If PCIE not support still connect to +VCC_PEG

+1.05V

PEG_COMPI
PEG_COMPO
T37 EXP_A_COMPX R176 49.9/F_4
T36

PEG_RX#_0 ... PEG_RX#_15
H44 PEG_RXN0
J46 PEG_RXN1
L44 PEG_RXN2
L40 PEG_RXN3
N41 PEG_RXN4
P48 PEG_RXN5
N44 PEG_RXN6
T43 PEG_RXN7
U43 PEG_RXN8
Y43 PEG_RXN9
Y48 PEG_RXN10
Y36 PEG_RXN11
AA43 PEG_RXN12
AD37 PEG_RXN13
AC47 PEG_RXN14
AD39 PEG_RXN15
PEG_RXN[15:0] [18]

PEG_RX_0 ... PEG_RX_15
H43 PEG_RXP0
J44 PEG_RXP1
L43 PEG_RXP2
L41 PEG_RXP3
N40 PEG_RXP4
P47 PEG_RXP5
N43 PEG_RXP6
T42 PEG_RXP7
U42 PEG_RXP8
Y42 PEG_RXP9
W47 PEG_RXP10
Y37 PEG_RXP11
AA42 PEG_RXP12
AD36 PEG_RXP13
AC48 PEG_RXP14
AD40 PEG_RXP15
PEG_RXP[15:0] [18,24]

Can support reversal routing.If CFG9=1, PCI Express is normal operation. If CFG9=0, then PEG_TXP0 becomes PEG_TXP15, PEG_TXP1 becomes PEG_TXP14, PEG_TXP2 becomes PEG_TXP13, etc. similarly for PEG_RXP[15:0] and PEG_RXN[15:0]

PEG_TX#_0 ... PEG_TX#_15
J41 C_PEG_TXN0 C583 .1u/10V_4 PEG_TXN0
M46 C_PEG_TXN1 C587 .1u/10V_4 PEG_TXN1
M47 C_PEG_TXN2 C591 .1u/10V_4 PEG_TXN2
M40 C_PEG_TXN3 C596 .1u/10V_4 PEG_TXN3
M42 C_PEG_TXN4 C618 EV@.1U/10V_4 PEG_TXN4
R48 C_PEG_TXN5 C588 EV@.1U/10V_4 PEG_TXN5
N38 C_PEG_TXN6 C600 EV@.1U/10V_4 PEG_TXN6
T40 C_PEG_TXN7 C598 EV@.1U/10V_4 PEG_TXN7
U37 C_PEG_TXN8 C604 EV@.1U/10V_4 PEG_TXN8
U40 C_PEG_TXN9 C603 EV@.1U/10V_4 PEG_TXN9
Y40 C_PEG_TXN10 C608 EV@.1U/10V_4 PEG_TXN10
AA46 C_PEG_TXN11 C594 EV@.1U/10V_4 PEG_TXN11
AA37 C_PEG_TXN12 C616 EV@.1U/10V_4 PEG_TXN12
AA40 C_PEG_TXN13 C619 EV@.1U/10V_4 PEG_TXN13
AD43 C_PEG_TXN14 C614 EV@.1U/10V_4 PEG_TXN14
AC46 C_PEG_TXN15 C593 EV@.1U/10V_4 PEG_TXN15
PEG_TXN[15:0] [18,24]

PEG_TX_0 ... PEG_TX_15
J42 C_PEG_TXP0 C580 .1u/10V_4 PEG_TXP0
L46 C_PEG_TXP1 C585 .1u/10V_4 PEG_TXP1
M48 C_PEG_TXP2 C590 .1u/10V_4 PEG_TXP2
M39 C_PEG_TXP3 C597 .1u/10V_4 PEG_TXP3
M43 C_PEG_TXP4 C611 EV@.1U/10V_4 PEG_TXP4
R47 C_PEG_TXP5 C586 EV@.1U/10V_4 PEG_TXP5
N37 C_PEG_TXP6 C601 EV@.1U/10V_4 PEG_TXP6
T39 C_PEG_TXP7 C599 EV@.1U/10V_4 PEG_TXP7
U36 C_PEG_TXP8 C605 EV@.1U/10V_4 PEG_TXP8
U39 C_PEG_TXP9 C602 EV@.1U/10V_4 PEG_TXP9
Y39 C_PEG_TXP10 C609 EV@.1U/10V_4 PEG_TXP10
Y46 C_PEG_TXP11 C595 EV@.1U/10V_4 PEG_TXP11
AA36 C_PEG_TXP12 C617 EV@.1U/10V_4 PEG_TXP12
AA39 C_PEG_TXP13 C620 EV@.1U/10V_4 PEG_TXP13
AD42 C_PEG_TXP14 C615 EV@.1U/10V_4 PEG_TXP14
AD46 C_PEG_TXP15 C592 EV@.1U/10V_4 PEG_TXP15
PEG_TXP[15:0] [18,24]

IV&EV Dis/Enable setting

<5/31>Montevina_Schematics_Checklist_Rev0_8
a)For TVOUT Disabled, TV_DCONSEL[1:0] Connect to GND. But design guide Rev0.7 show NC.What is correct.
b)For CRT DAC Disable, CRT_DDC_CLK, CRT_DDC_DATA . CRT_HSYNC, CRT_VSYNCThese signals should be connected to GND. But design guide Rev0.7 show NC, Intel suggest follow Design guide.

<check list>	<check list>
For EV@	For IV@
CRT R/G/B 0ohm to GND	CRT R/G/B 150ohm to GND
CRTIREF 0ohm to GND	CRTIREF 1Kohm to GND

For topology without the analog switch - if the total motherboard route length is less than 12", the recommended reference resistor value is 1 kΩ ±1%

CRTIREF
For IV: 1Kohm
For EV:0ohm

R161 SP@1K/F_4 CRTIREF

SP@

CRT_R/G/B
For IV: 150ohm
For EV:0ohm

R155 SP@150/F_4 INT_CRT_BLU
R154 SP@150/F_4 INT_CRT_GRN
R150 SP@150/F_4 INT_CRT_RED

Discrete Stuffed. (CRT)

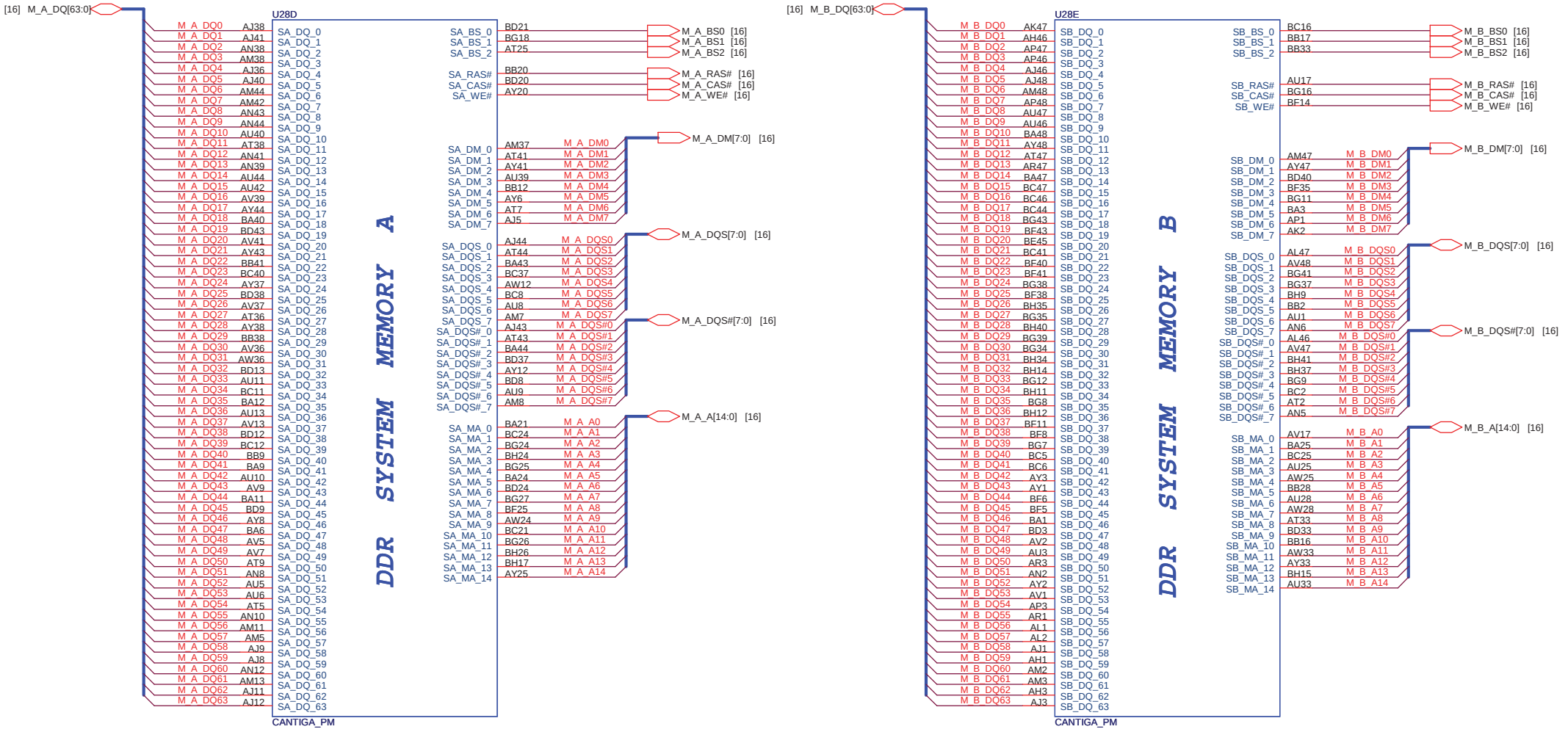
HSYNC_G
VSYNC_G
R159 EV@0_4
R166 EV@0_4

CRTIREF pull down for IV cantiga 1.02k ohm/F

Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	GMCH VGA	1A
Date: Tuesday, May 19, 2009	Sheet 7 of 39	

GMCH-CANTIGA(CLG)



Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	GMCH DDRII	1A

Date: Tuesday, May 19, 2009 Sheet 8 of 39

GMCH-CANTIGA(CLG)

IV@

SP@

Power consumption reference to Intel
644135 Cantiga chipset EDS Volume1.
Section 10

GM TDP 10.5~12W
GS TDP 7~8W
PM TDP 7W

Intel check list(Rev 0.8)
No description for VCC_SM bulk CAP
Intel CRB(Rev 0.7)
330U*1 Reserve near to power
330U*1 near to NB

Intel check list(Rev 0.8)
270U*1 near to power(+V1.05M).
270U*2 near to NB
Intel CRB(Rev 0.7)
270U*3 near to power(+V1.05M).
270U*1 near to NB
ESR=12m ohm

+1.8VSUS

+1.5VSUS to +1.8VSUS

C606 22u/6.3V_8 | C612 *22u/6.3V_8 | C264 .1u/10V_4 | C624 330u/2V_7343

VCC_SM(1.8V) DDR2

U28G

VCC_SM_1 … VCC_SM_42 — POWER — VCC SM

VCC_SM_36/NC … VCC_SM_42/NC

VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60 — VCC GFX NCTF

+1.05V_AXG

VCC_AXG_1 … VCC_AXG_42 — VCC GFX

VCC_AXG_SENSE
VSS_AXG_SENSE

VCC_SM_LF1 … VCC_SM_LF7 — VCC SM LF

1.05V
Graphics core
VCC_AXG
VCC_AXG_NCTF
6326.84mA

Voltage regulator is shared between the Graphics Core Rail, VCCA_HPLL,VCCA_MPLL,VCCA_PEG_PLL,VCCD_PEG_PLL, VCCA_SM_CK, VCCA_DPLLA, VCCA_DPLLB, VCCD_HPLL, VCCA_SM, VCC_AXF

1.8V
Internal connect to power

C163 .1u/10V_4 | C151 .1u/10V_4 | C142 .22u/6.3V_4 | C211 .22u/6.3V_4 | C292 .47u/6.3V_4 | C290 1u/10V_4 | C319 1u/10V_4

IV@ R112 IV@/10/F_4 | R110 IV@/10/F_4

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

CANTIGA_PM

+1.05V

C267 .1u/10V_4 | C283 *.22u/6.3V_4 | C266 .22u/6.3V_4 | C286 22u/6.3V_8 | C610 330u/2V_7343

Place close to the GMCH

U28F

VCC_1 … VCC_35 — VCC CORE

IV@ R156 IV@ 8 | R83 IV@ 8 | R80 IV@ 8

IV&EV Dis/Enable setting
Design guide(Table 72)
For INT VGA diasble.VCC_AXG power can connect to GND

+1.05V_AXG

+C505 IV@330u/2V_7343 | +C501 IV@330u/2V_7343 | C219 IV@.47u/6.3V_4 | SP@ C168 SP@1u/10V_6 | C149 IV@10u/6.3V_8 | C187 IV@22u/6.3V_8 | C223 IV@.1u/10V_4 | C107 IV@.1u/10V_4 | C166 IV@.1u/10V_4

Place close to the GMCH

SP@/IV Sutff 1uf
EVstuff 0 ohm

Cavity Capacitors

Intel check list(Rev 0.8)
220U*2 near to NB(ESR=15m ohm)
Intel CRB(Rev 0.7)
270U*4 near to power(+V1.05S).
330U*2 near to NB

VCC_NCTF_1 … VCC_NCTF_44 — POWER — VCC NCTF

CANTIGA_PM

VCC
VCC_NCTF
1210.34mA_EV
1930.4mA_IV
ME Engine
508.12mA
Total Max=2438.52mA

NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)
(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	GMCH VCC,NCTF	1A

Date: Tuesday, May 19, 2009 Sheet 9 of 39

GMCH-CANTIGA(CLG)

Power consumption reference to Intel Cantiga_chipset EDS Volume1. Section 10

IV@
EV@
SP@

If CRT have Flicker issue
STUFF 5.6 ohm

IV&EV Dis/Enable setting

SP@:INT use 0.01U
EXT use 0 ohm

SP@:INT use 0.1U
EXT use 0 ohm

1210 10UH, 10%
0.45A DCR_max = 0.39

1.05V
64.8mA for DPLL_A/B

3.3V
73mA

3.3V
5mA

USE same GND plane

VCCA_DPLLA/B always keep to +1.05V
(If no use IV dynamic core power)

1.8V
13.2mA

1.5V
414uA

1.05V
24mA

1.05V
139.2mA

1.05V
DDR2-800
720mA

1.05V
50mA

VCCA_PEG_PLL
+1.25V for Teenah use(100mA)

3.9 nH, 0.2 nH, 1A
DCR_max=32 m

1210 0.1uH, 20%, 1A,
DCR_max=0.078Ω

1.05V
DDR2-800
26mA

CRB : 0 ohm
Check list : 2.2nH

3.3V
24.15mA for VCCA_TVA_DAC
39.48mA for VCCA_TVB_DAC
24.15mA for VCCA_TVC_DAC
Total 87.78mA

FB 180@100 MHz, 25% 1.5A
DCR_max=90 m

3.3V
79mA

CRB no 10U
Check list need min 10U~100U for VCCA_TV_DAC

1.5V
50mA

VCCD_TVDAC always keep 0.1U/0.022U/10U to +1.5V

1.5V
35mA

VCCD_QDAC share to TV and CRT

1.5V
48.363mA for CRT
5mA for TV

1.5V
0.5mA

CRB no 10U
Check list need min 10U~100U
for VCCA_QDAC

MODIFY

FB 220 @100 MHz, 25%, 2A

1.05V
50mA

ESR=60m ohm

1.8V
60.31mA

SP@:INT use 1 U
EXT use 0 ohm

1.05V
FSB-1067
852mA

1.05V
321.35mA

1.8V
DDR2-800
124mA

0805 1UH , Rdc = 0.14 - 0.26.
Max rated current = 220 mA

1.8V
118.8mA

3.3V
105.3mA

1.05V
1782mA

1.05V
456mA

1.05V
Internal connect to power

External Graphics
(GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TVDAC	GND
VCCD_QDAC	GND
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

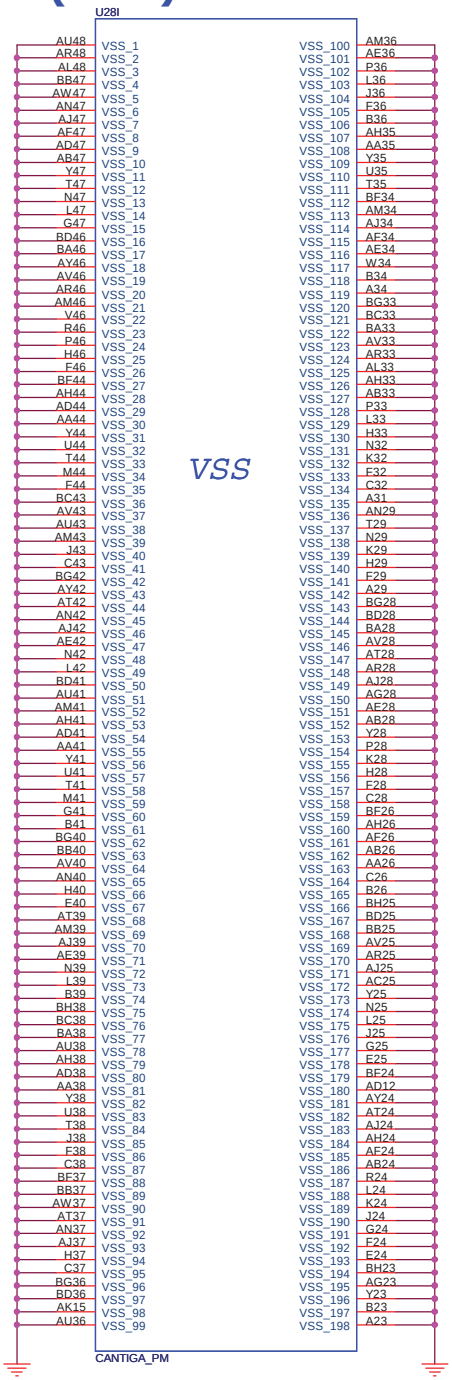
Power Net Name	Cantiga(V)
VCC_AXG_# VCC_AXG_NCTF_#	1.05V
VCCA_PEG_BG	1.5V
VCCA_DPLLA	1.05V
VCCA_DPLLB	1.05V
VCCA_SM_#	1.05V
VCCA_HPLL	1.05V
VCCA_MPLL	1.05V
VCCA_SM_CK_#	1.05V
VCCA_PEG_PLL	1.05V
VCC_AXF_#	1.05V
VCCD_HPLL	1.05V
VCCD_PEG_PLL	1.05V

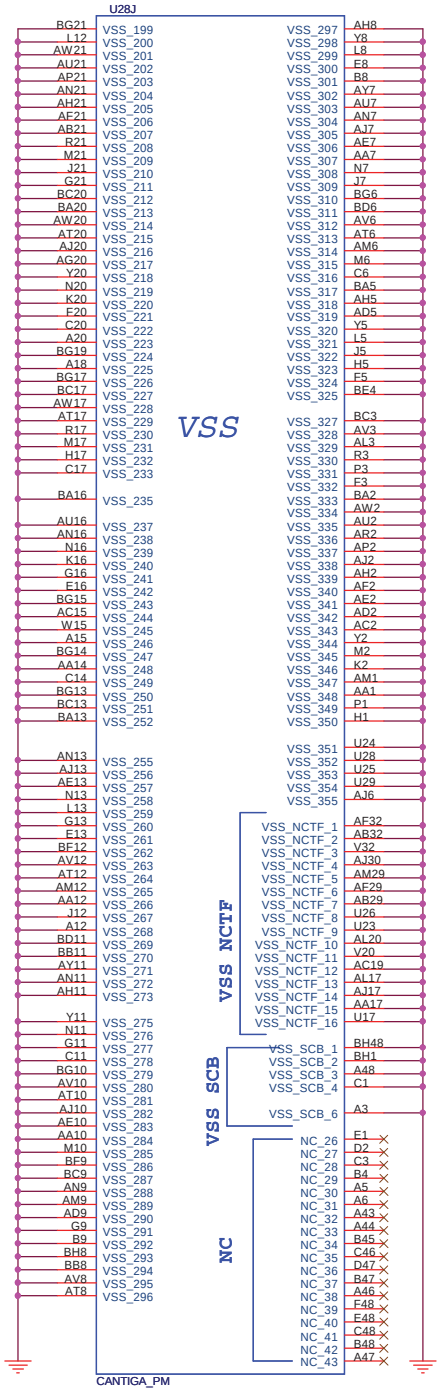
Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	GMCH POWER	1A

Date: Tuesday, May 19, 2009 Sheet 10 of 39

GMCH-CANTIGA(CLG)





Quanta Computer Inc.

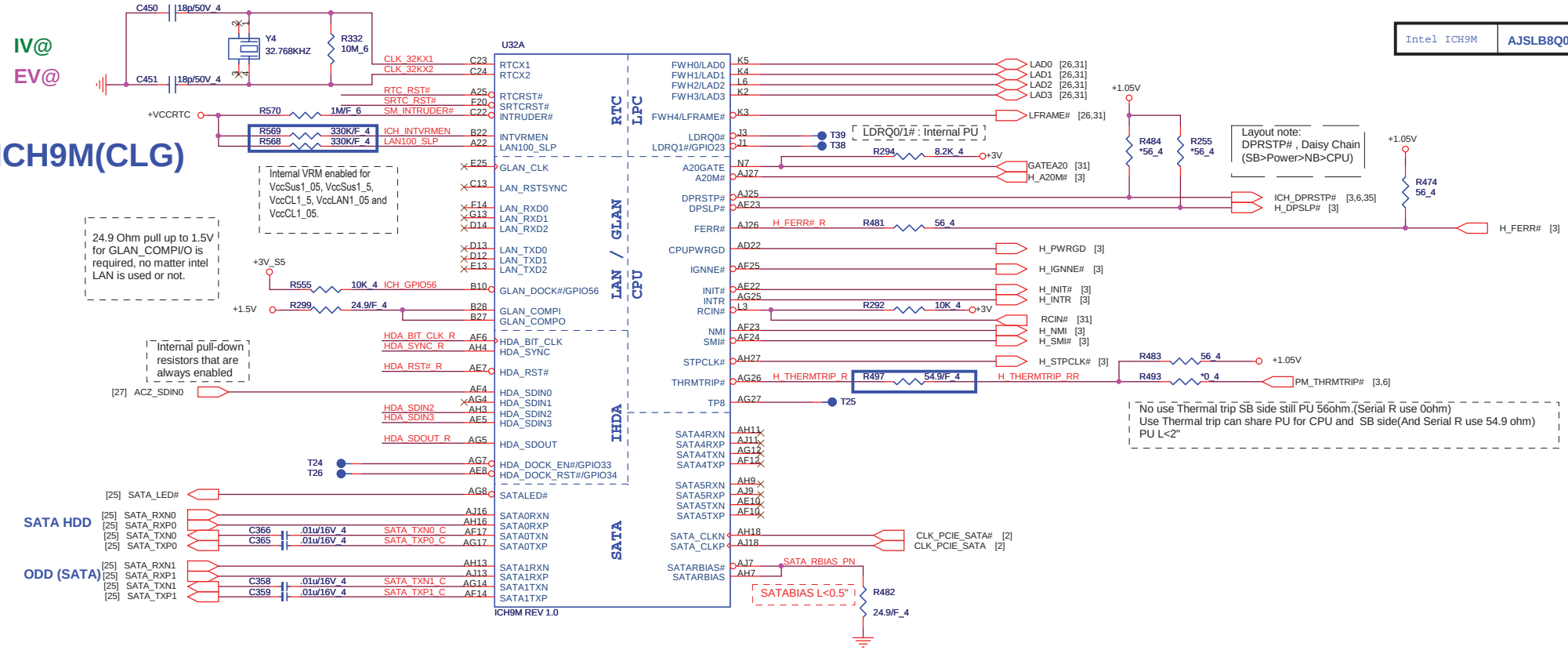
PROJECT : ZR6E

Size	Document Number	Rev
	GMCH VSS	1A
Date: Tuesday, May 19, 2009	Sheet 11 of 39	

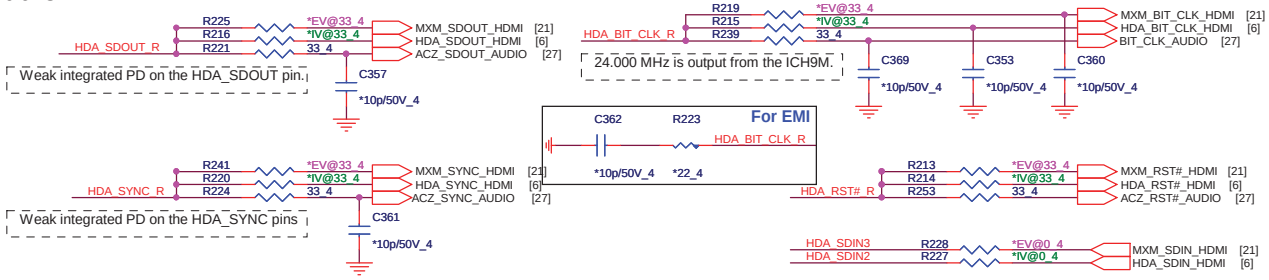
IV@

EV@

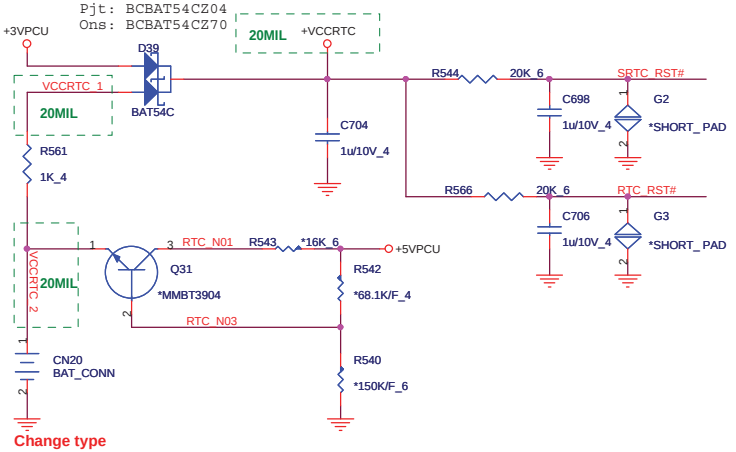
ICH9M(CLG)



HD Audio



RTC



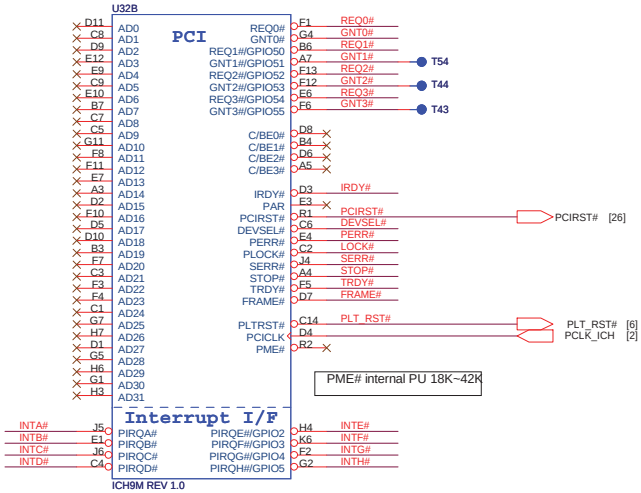
South Bridge Strap Pin (1/3)

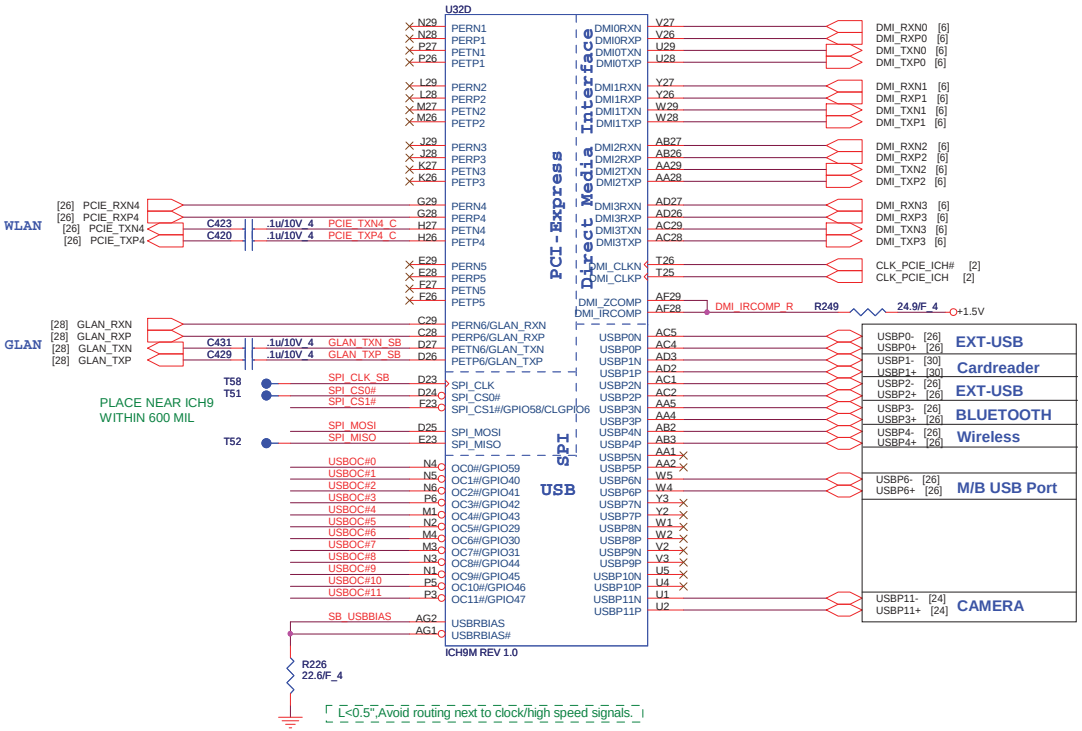
Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
TP3	XOR Chain Entrance	PWROK	ICH_TP3 / HDA_SDOUT: 0/0 RSVD; 0/1 Enter XOR Chain; 1/0 Normal opration(Default); 1/1 Set PCIE port config bit 1	[14] ICH_TP3 — ICH_TP3 — R545 — *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_SDOUT_R — R240 — *1K_4 — +3V

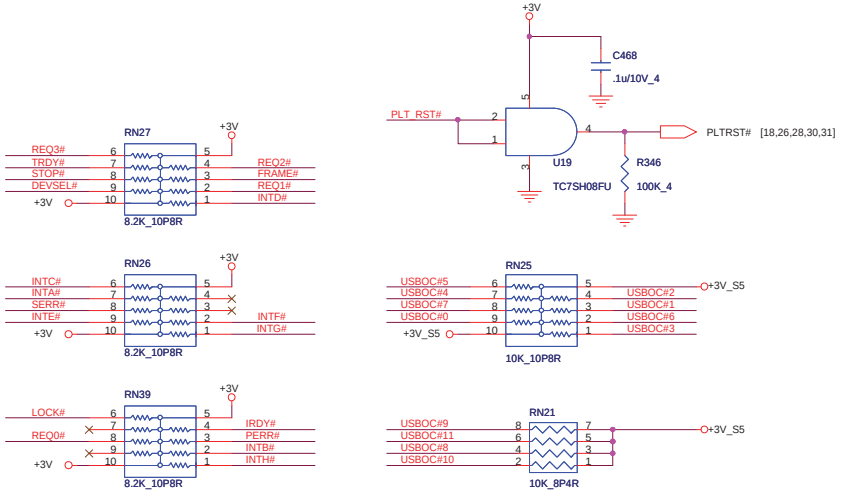
Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	ICH9M HOST	1A
Date: Tuesday, May 19, 2009	Sheet 12 of 39	







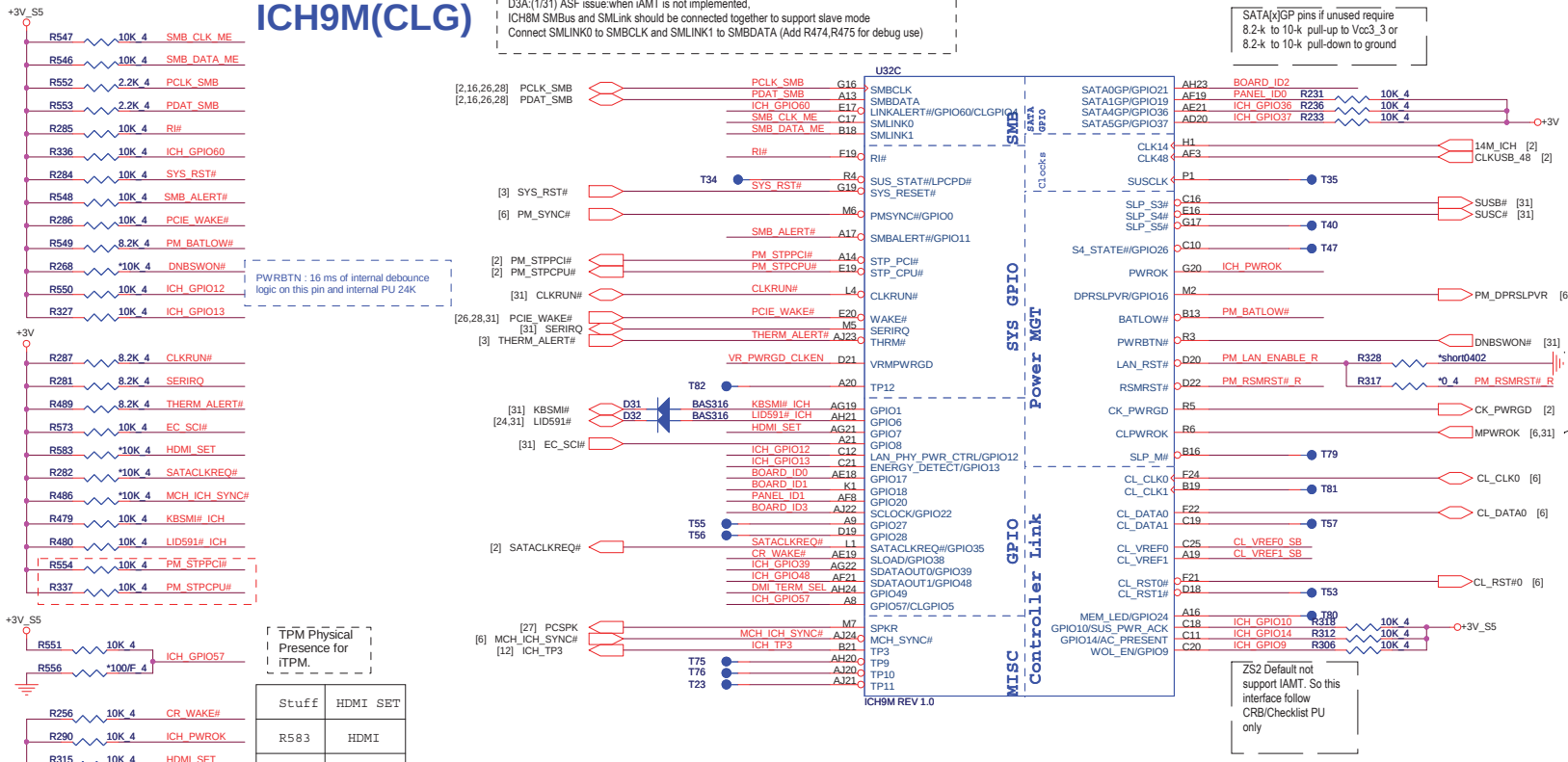
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R309 *1K_4
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R277 *10K_4 +3V_S5
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI 1 / 0 / PCI 1 / 1 / **LPC(Default)**	GNT0# R293 *1K_4
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# R274 *1K_4

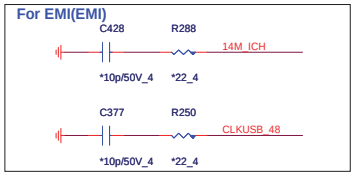
ICH9M(CLG)

D3A:(1/31) ASF issue:when iAMT is not implemented,
ICH8M SMBus and SMLink should be connected together to support slave mode
Connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA (Add R474,R475 for debug use)

SATA[x]GP pins if unused require
8.2-k to 10-k pull-up to Vcc3_3 or
8.2-k to 10-k pull-down to ground



For EMI(EMI)



<Checklist ver0.8>
If integrated LAN is not used LAN_RST# tie it to GND.NC serial R from RSMRST#.
If Intel LAN is used with Wake On LAN, tie LAN_RST# to RSMRST# and NC 0ohm.

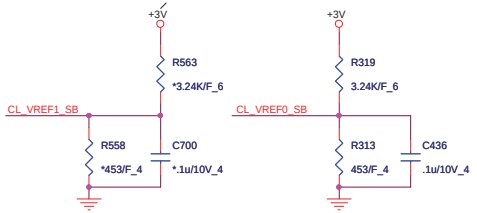
CL_PWROK must not assert after PWROK asserts for IAMT.
CL_PWROK to the NB and SB should be connected to existing PWROK inputs on the NB and SB on a platform with no IAMT

Stuff	HDMI SET
R583	HDMI
R315	No HDMI

CL VREF

VREF1 CRB connect to +3V_S5
Checklist connect to +3V(iAMT reserve)

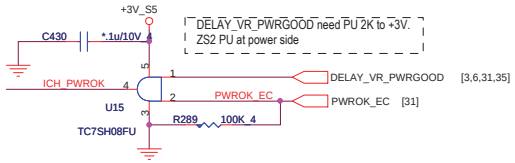
<Checklist ver0.8>
The ICH9M Controller Link 1 VREF circuit is required only if Intel AMT is to be supported.



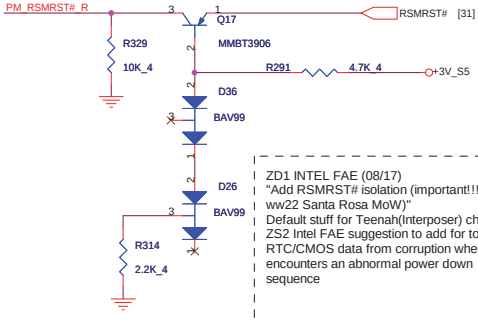
+3V_S5
R571 *10K_4 EC_SCI#
+3V
R245 10K_4 PANEL_ID1
R490 10K_4 ICH_GPIO39
R232 10K_4 ICH_GPIO48

Follow CHECK LIST V1.5

ICH PWROK



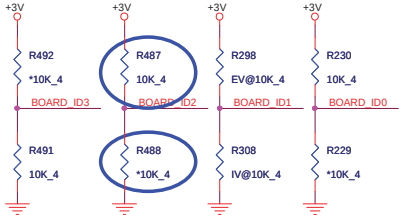
Resume RST



ZD1 INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"
Default stuff for Teenah(Interposer) chipset
ZS2 Intel FAE suggestion to add for to protect RTC/CMOS data from corruption when system encounters an abnormal power down sequence

M/B ID

ID0=0 -->ZK6 ,ID0=1 -->ZR6
ID1=0 -->UMA ,ID1=1 -->Discrete

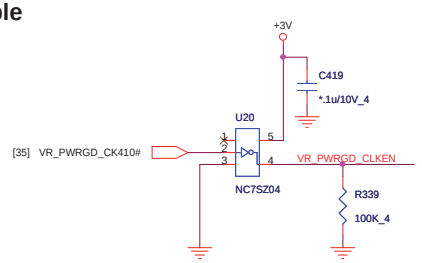


Board ID	ID3	ID2	ID1	ID0
A-SMT,ID1=0 -->UMA ,ID1=1 -->Discrete	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1
	0	0	0/1	1

South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R271 *1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R485 *1K_4

CLK Enable



Quanta Computer Inc.
PROJECT : ZR6E
Size | Document Number | ICH9M GPIO | Rev 1A
Date: Tuesday, May 19, 2009 | Sheet 14 of 39

ICH9M(CLG)

IV@

EV@

Power consumption reference to Intel ICH9 Family EDS Rev 1.6

PER INTEL SUGGESTION: CHANGE TO 100OHM & 1UF

MODIFY

MODIFY

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

VCCSUS1_05 power by VCC1_05 in S0 / VCCSUS3_3 in S3/S4/S5
VCCSUS1_5 power by VCC1_5_A in S0 / VCCSUS3_3 in S3/S4/S5

VCCCL1_05 power by VCC1_05_A in S0
VCCCL1_5 power by VCC1_5_A in S0

1.05V , Powered by VCC1_05 in S0

If use SB MAC for LAN function. And support wake up need connect to relation power.

If use SB MAC for LAN function. And support wake up need connect to relation power.

U32F

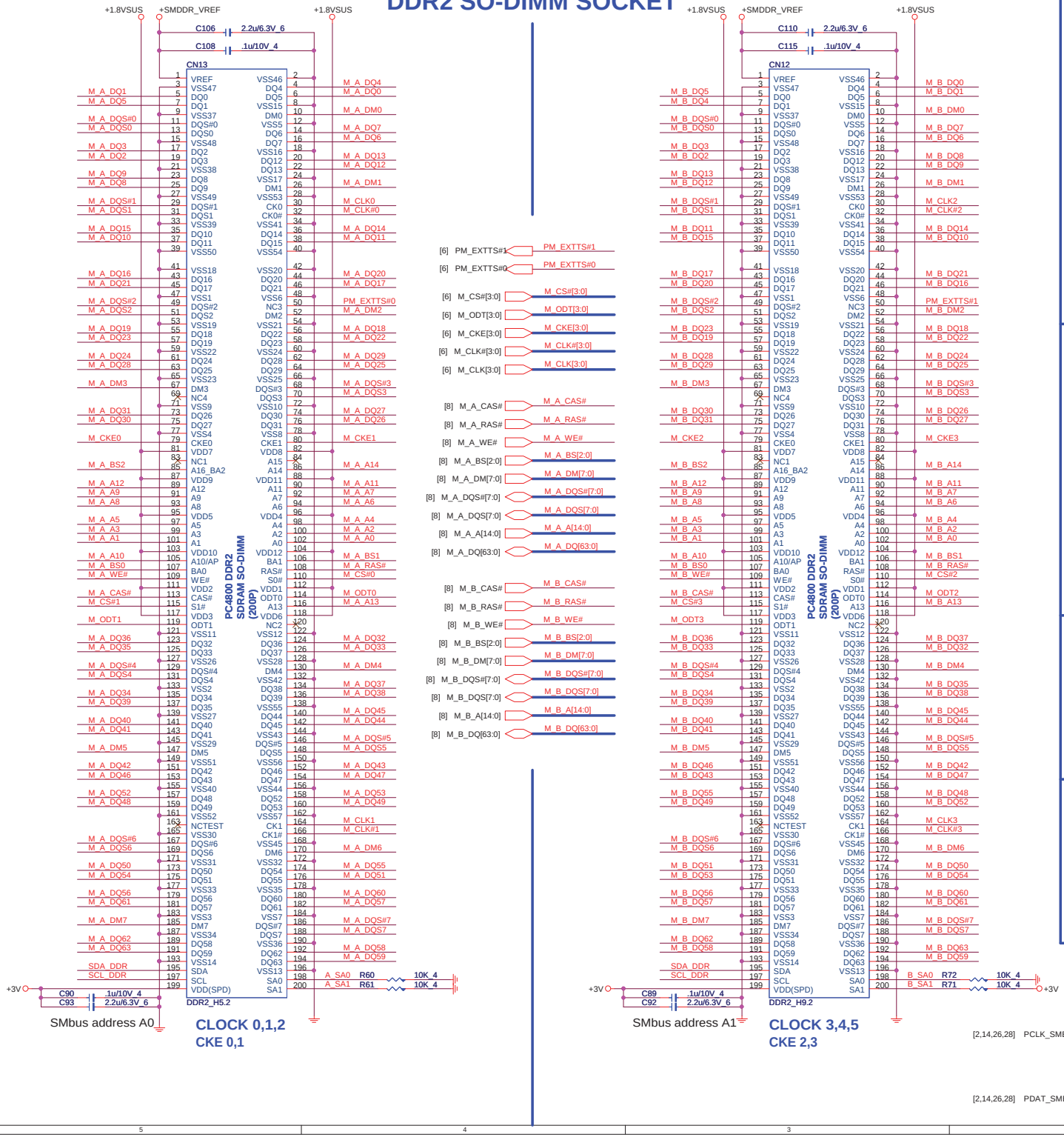
ICH9M REV 1.0

U32E

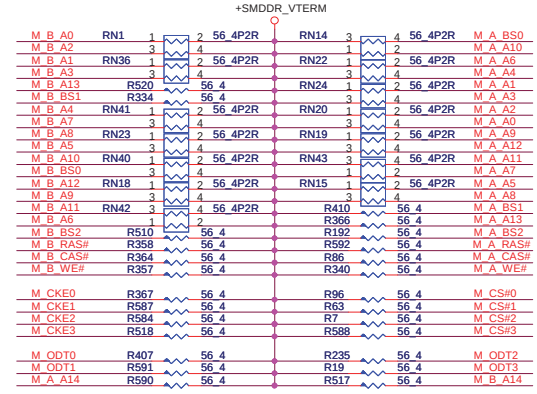
ICH9M REV 1.0

Quanta Computer Inc.	
PROJECT : ZR6E	
Size	Document Number: ICH9 POWER — Rev 1A
Date: Tuesday, May 19, 2009	Sheet 15 of 39

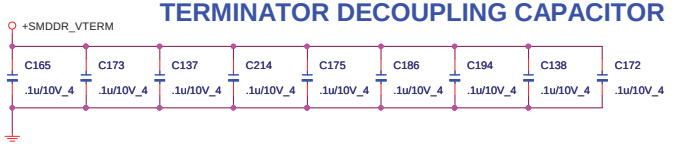
DDR2 SO-DIMM SOCKET



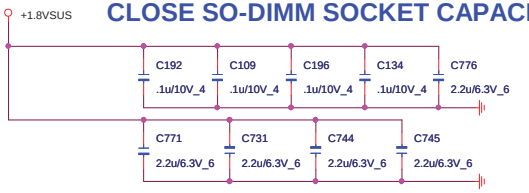
DDR2 TERMINATOR



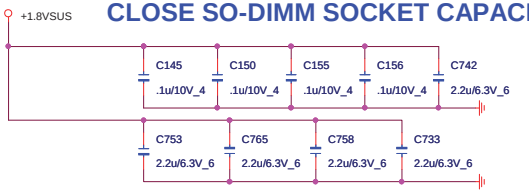
TERMINATOR DECOUPLING CAPACITOR

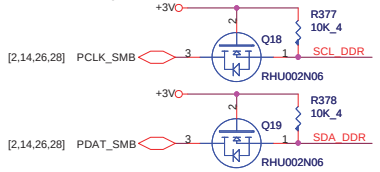


CLOSE SO-DIMM SOCKET CAPACITORS



CLOSE SO-DIMM SOCKET CAPACITORS





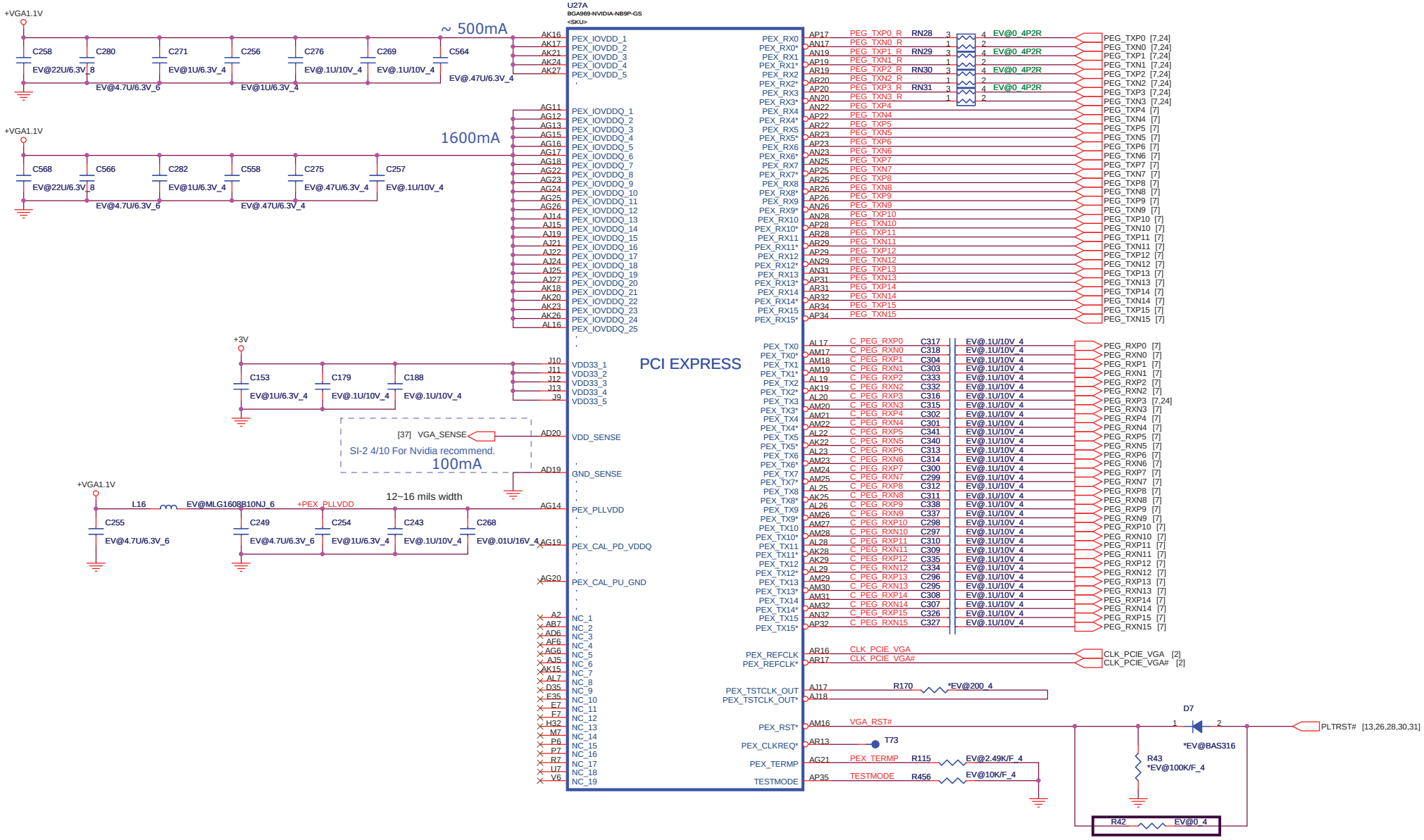
Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	DDRII SO-DIMM	1A

Date: Tuesday, May 19, 2009 Sheet 16 of 39

NV10M (VGA)



Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	NV10X (PCIE I/F) 1/5	1A

Date: Tuesday, May 19, 2009 Sheet 17 of 39

NV10M (VGA)

U27B
BGA969-NVIDIA-NB9P-GS
<SKU>

MEMORY I/F A

U27C
BGA969-NVIDIA-NB9P-GS
<SKU>

MEMORY I/F B

Add for 64x16 vram

for DDR2 need use
CMD11(CKE) and
CMD12(ODT)

use internal Vref, ext
divider no stuff

15mils width

For Debug only

R91 Install for DDR3

R86 no stuff

G96 only

Quanta Computer Inc.	
PROJECT : ZR6E	
Size	Document Number: NV10X (MEMORY I/F) 2/5 — Rev 1A
Date: Tuesday, May 19, 2009	Sheet 18 of 39

NV10M (VGA)

U27D

BGA969-NVIDIA-N89P-GS
<SKU>

IFPAB(LVDS)

+1.8V
L41 EV@HCB1608KF-181T15_6 +IFPAB_PLLVDD
C578 EV@4.7U/6.3V_6
C575 EV@4700P/25V_4
C279 EV@470P/50V_4
100 mA
IFPAB_PLLVDD AK9
IFPAB_RSET AJ11
R173 *EV@1K/F_4

L14 EV@HCB1608KF-181T15_6 +IFPAB_IOVDD
C247 EV@4.7U/6.3V_6
C246 EV@4.7U/6.3V_6
C251 EV@4700P/25V_4
C265 EV@4700P/25V_4
C250 EV@470P/50V_4
C259 EV@470P/50V_4
50 mA
IFPA_IOVDD AG9
50 mA
IFPB_IOVDD AG10

IFPA_TXC+ AM11
IFPA_TXC- AM12
IFPA_TXD0+ AM8
IFPA_TXD0- AL8
IFPA_TXD1+ AM10
IFPA_TXD1- AM9
IFPA_TXD2+ AK10
IFPA_TXD2- AL10
IFPA_TXD3+ AK11
IFPA_TXD3- AL11
IFPB_TXC+ AP13
IFPB_TXC- AN13
IFPB_TXD4+ AN8
IFPB_TXD4- AP8
IFPB_TXD5+ AP10
IFPB_TXD5- AN10
IFPB_TXD6+ AR11
IFPB_TXD6- AR10
IFPB_TXD7+ AN11
IFPB_TXD7- AP11

EV_TXLCLKOUT+ [24]
EV_TXLCLKOUT- [24]
EV_TXLOUT0+ [24]
EV_TXLOUT0- [24]
EV_TXLOUT1+ [24]
EV_TXLOUT1- [24]
EV_TXLOUT2+ [24]
EV_TXLOUT2- [24]

IFPCD

+1.8V
L40 EV@HCB1608KF-181T15_6 +IFPCD_PLLVDD
C132 EV@1U/6.3V_4
C572 EV@4.7U/6.3V_6
C260 EV@4700P/25V_4
C261 EV@470P/50V_4
IFPCD_PLLVDD AJ9
IFPCD_RSET AK7
R432 EV@1K/F_4

+VGA1.1V
L42 EV@HCB1608KF-181T15_6 +IFPCD_IOVDD
C579 EV@4.7U/6.3V_6
C581 EV@1U/6.3V_4
C576 EV@1U/6.3V_4
C584 EV@4700P/25V_4
C287 EV@470P/50V_4
C274 EV@470P/50V_4
IFPC_IOVDD AJ8
IFPD_IOVDD AK8

IFPC

AUX+ AN3
AUX- AP2
DPL3_TXC+ AR2 HDMI_CLK-_R C293 EV@.1U/10V_4 HDMI_CLK- [24]
DPL3_TXC- AP1 HDMI_CLK+_R C294 EV@.1U/10V_4 HDMI_CLK+ [24]
DPL2_TXD0+ AN4 HDMI_TX0N_R C305 EV@.1U/10V_4 HDMI_TX0N [24]
DPL2_TXD0- AM3 HDMI_TX0P_R C306 EV@.1U/10V_4 HDMI_TX0P [24]
DPL1_TXD1+ AM5 HDMI_TX1N_R C323 EV@.1U/10V_4 HDMI_TX1N [24]
DPL1_TXD1- AL5 HDMI_TX1P_R C324 EV@.1U/10V_4 HDMI_TX1P [24]
DPL0_TXD2+ AM6 HDMI_TX2N_R C322 EV@.1U/10V_4 HDMI_TX2N [24]
DPL0_TXD2- AM7 HDMI_TX2P_R C321 EV@.1U/10V_4 HDMI_TX2P [24]

Fix Ball out and Pin Name

IFPD

AUX+ AN4
AUX- AP4
DPL3_TXC+ AR4
DPL3_TXC- AR5
DPL2_TXD0+ AP5
DPL2_TXD0- AN5
DPL1_TXD1+ AM7
DPL1_TXD1- AP7
DPL0_TXD2+ AR7
DPL0_TXD2- AR8

TMDS channel two

IFPEF

IFPEF_PLLVDD AJ6
T72
IFPEF_PLLVDD AL1
R164 EV@10K/F_4
IFPEF_IOVDD AE7
IFPE_IOVDD
IFPF_IOVDD AD7
R425 EV@10K/F_4

IFPE_AUX+ AE4
IFPE_AUX- AD4
IFPE_L0+ AH6
IFPE_L0- AH5
IFPE_L1+ AH4
IFPE_L1- AG4
IFPE_L2+ AF4
IFPE_L2- AF5
IFPE_L3+ AE6
IFPE_L3- AE5
IFPF_AUX+ AF3
IFPF_AUX- AE3
IFPF_L0+ AE2
IFPF_L0- AL2
IFPF_L1+ AL3
IFPF_L1- AJ3
IFPF_L2+ AJ2
IFPF_L2- AJ1
IFPF_L3+ AH1
IFPF_L3- AH2
AH3

Display port output

DACA(CRT)

+3V
L17 EV@HCB1608KF-181T15_6 +DACA_VDD
C285 EV@4.7U/6.3V_6
C270 EV@4700P/25V_4
C284 EV@470P/50V_4
C281 EV@.1U/10V_4
R454 EV@124/F_4
DACA_VDD AJ12
DACA_VREF AK12
DACA_RSET AK13

DACA_RED AM15 EV_VGA_RED [24]
DACA_GREEN AM14 EV_VGA_GRN [24]
DACA_BLUE AL14 EV_VGA_BLU [24]
DACA_HSYNC AM13 CRT_HSYNC R190 EV@33_4 EV_HSYNC [24]
DACA_VSYNC AL13 CRT_VSYNC R191 EV@33_4 EV_VSYNC [24]
I2CA_SCL G1 EV_CRTDCLK [24]
I2CA_SDA G4 EV_CRTDDAT [24]

EV_VGA_RED R187 EV@150/F_4
EV_VGA_GRN R188 EV@150/F_4
EV_VGA_BLU R189 EV@150/F_4
Close to GPU

DACC(CRT2)

+DACB_VDD AG7
R431 EV@10K/F_4
T71 AK6
T70 AH7
DACC_VDD
DACC_VREF
DACC_RSET

DACC_RED AK4
DACC_GREEN AL4
DACC_BLUE AJ4
DACC_HSYNC AM1
DACC_VSYNC AM2
I2CB_SCL G3 I2CB_SCL R404 EV@2.2K_4 +3V
I2CB_SDA G2 I2CB_SDA R405 EV@2.2K_4 +3V

DACB(TV)

+DACC_VD AC6
R145 EV@10K/F_4
T68 AC5
T67 AB6
DACB_VDD
DACB_VREF
DACB_RSET

DACB_RED AA4
DACB_GREEN AB4
DACB_BLUE Y4
DACB_CSYNC AB5 T69

SI Build

XTAL_PLL

+VGA1.1V
L13 EV@HCB1608KF-181T15_6 +NV_PLLVDD
C227 EV@1U/6.3V_4
C224 EV@1U/6.3V_4
C238 EV@1U/6.3V_4
C241 EV@.1U/10V_4
C245 EV@.1U/10V_4
65mA
50mA
25mA
PLLVDD AE9
VID_PLLVDD AD9
SP_PLLVDD AF9

XTAL_SSIN D2 27M_SS [2]
XTAL_OUTBUFF D1 BXTALOUT
XTAL_IN B1 27M_NONSS [2]
XTAL_OUT B2

NVidia suggest:
10 kΩ pull-down only if
no spread chip used.

27M_SS
BXTALOUT
R391 EV@10K/F_4
R396 EV@10K/F_4

SPREAD SPECTRUM

+3V
R379 *EV@10K/F_4
R392 *EV@10K/F_4
SI Build
R395 *EV@22_4 27M_SS
C520 *EV@10P/50V_4
GFX27M_L
U23
ICSS_PD
BXTALOUT
PD# VDD
CLKIN CLKOUT
REFOUT
ICSS_RFO
SCL
SDA GND
*EV@ICS91730AMLF-T
+3V_SSC
R394 *EV@4.7_6 +3V
R397 *EV@10K/F_4
C506 *EV@470P/50V_4
C503 *EV@.1U/10V_4
C514 *EV@4.7U/6.3V_6
C513 *EV@4.7U/6.3V_6
EV_LVDS_DDCCLK
EV_LVDS_DDCDAT

I2C ADDRESS: 0xD4H

Quanta Computer Inc.			
PROJECT : ZR6E			
Size	Document Number	NV10X (DISPLAY) 3/5	Rev 1A
Date: Tuesday, May 19, 2009		Sheet 19 of 39	

NV10M (VGA)

N10P-GE1 (G96) Straps
N10M-GE1 (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL

PCI_DEVID[4]/SUBVENDOR

SEE Datasheet for details on G10x Straps!

NVidia Propose Remove C3134,C3681,R3092,R3402,R3063,R3064,C3076

Delete T31

HD Audio Level :3V

SI Build

PCI_DEVID: STRAP2

NB9M-GE	0x06E	8	1000
NB9M-GS	0x06E	9	1001
NB9P-GE2	0x064	8	1000
NB9P-GS	0x064	9	1001
N10P-GE1	0x065	2	0010
N10M-GE1	0x06E	C	1100 default

Logical Strap Bit Mapping

R414 PU-VDD	PD
5K 1000	0000
10K 1001	0001
15K 1010	0010
20K 1011	0011
25K 1100	0100
30K 1101	0101
35K 1110	0110
45K 1111	0111

R386	Config	Definitions	Die
CS25102FB02 5K	64Mx16 DDR2	Hynix	E
CS31002FB26 10K	64Mx16 DDR2	Samsung	Q
CS32002FB29 20K	64Mx16 DDR2	Samsung	E

I2C ADDRESS: 0x98H

VGA THERMAIL CIRCUIT Use 10MIL Guard(GND) Trace around THERMDC and THERMDA

HDCP ROM

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

SI Build

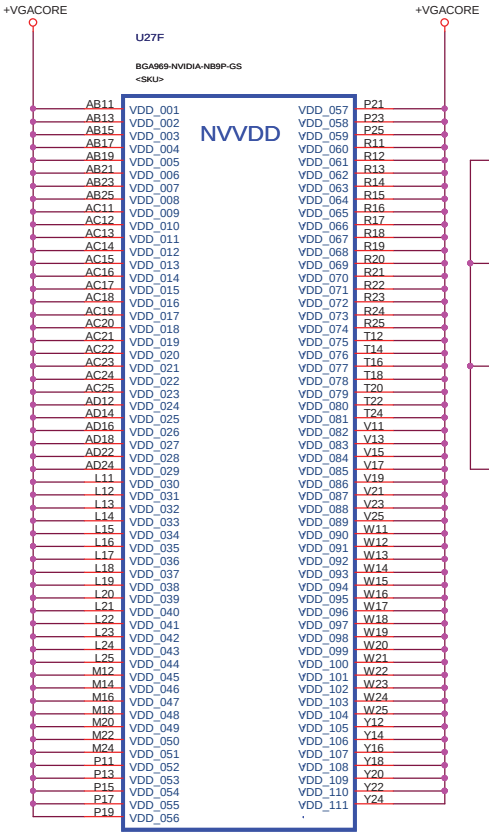
Waiting Confirm from Nvidia

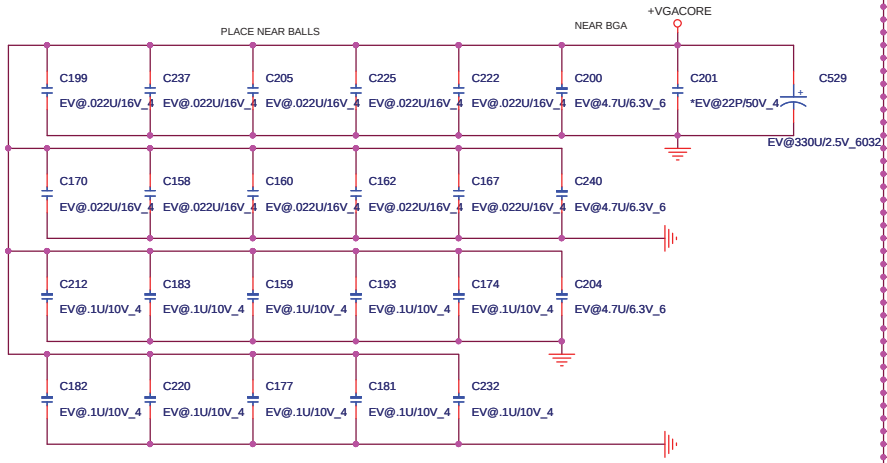
NVidia Request

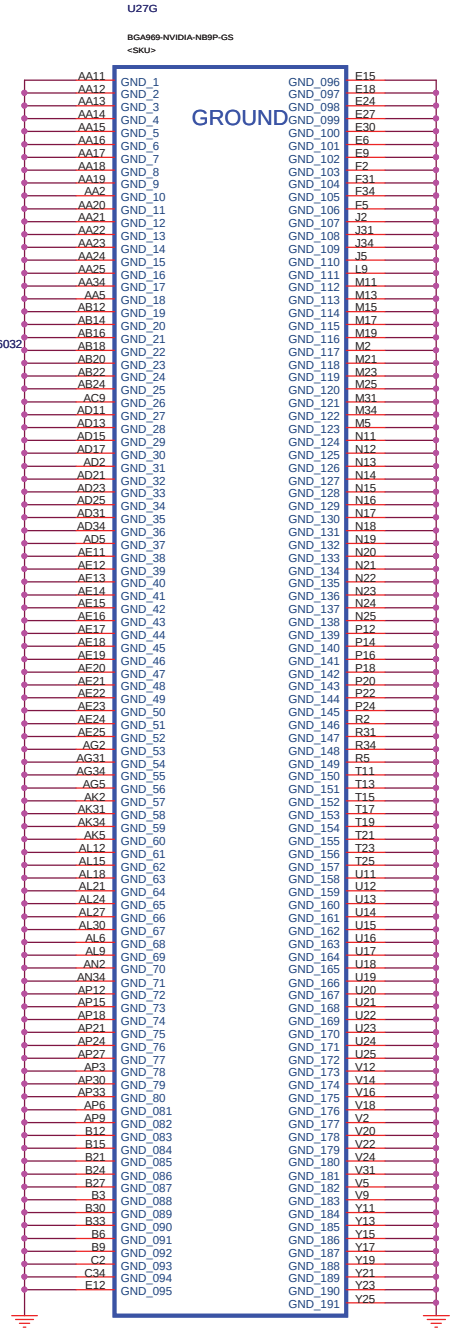
CLOSE U38 EMI

Quanta Computer Inc.	PROJECT : ZR6E	
Size	Document Number: NV10X (GPIO & STRRAPS) 4/5	Rev 1A
Date: Tuesday, May 19, 2009	Sheet 20 of 39	

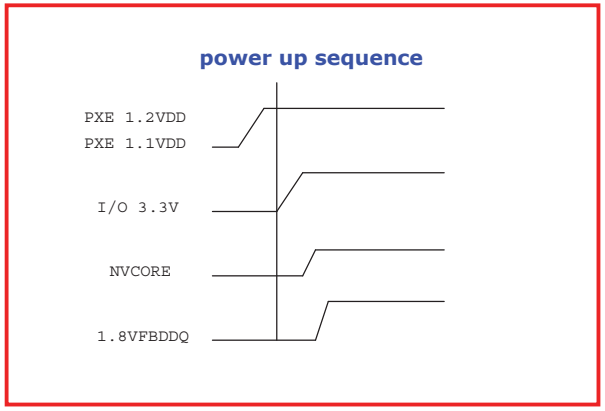
NVVDD Decoupling







Follow Design Guide DG-03276-001 4.7uFx3 and 0.22x10 uF instead of 0.1uF x10

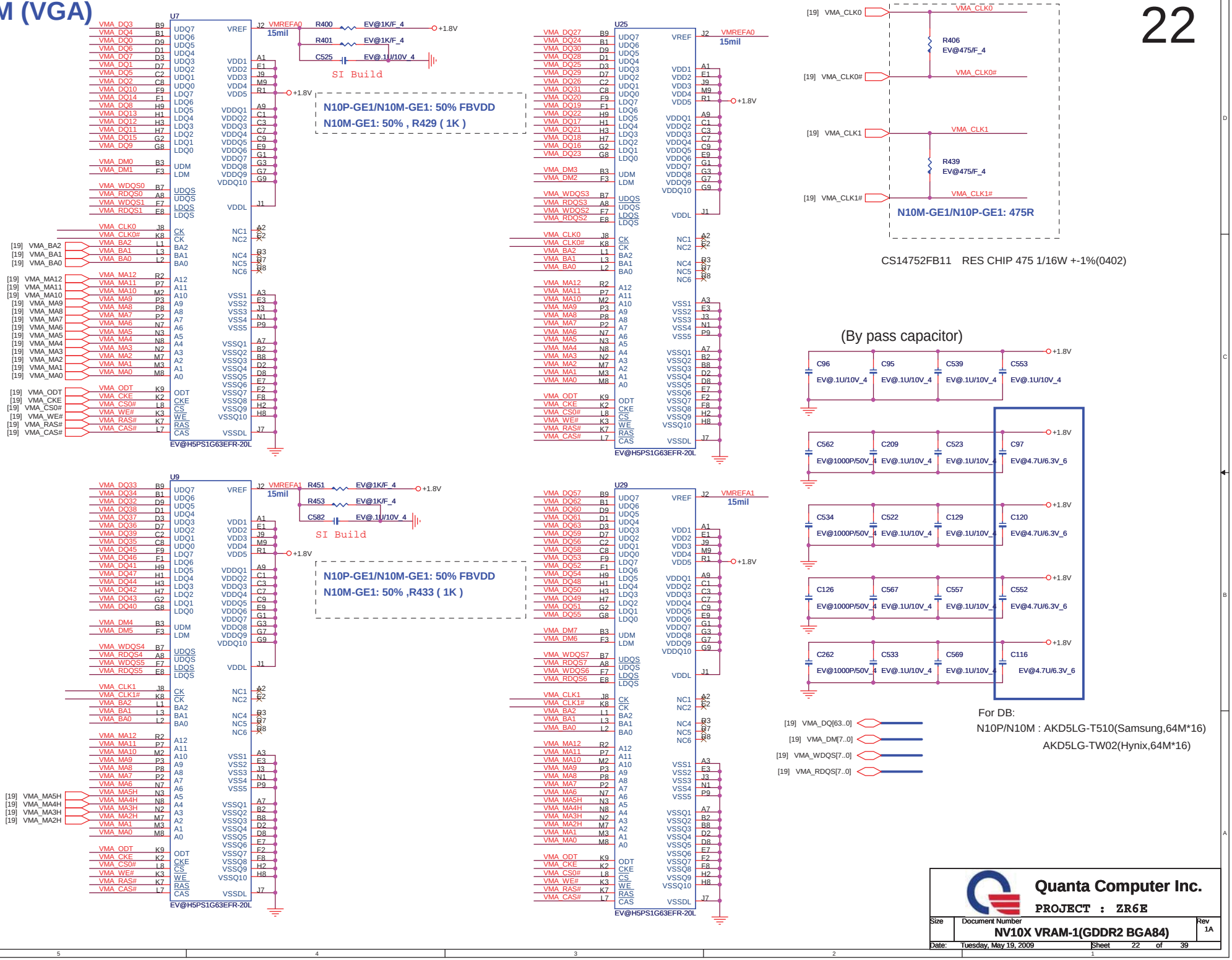


Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	NV10X (POWER & GND) 5/5	1A
Date: Tuesday, May 19, 2009	Sheet 21 of 39	

NV10M (VGA)

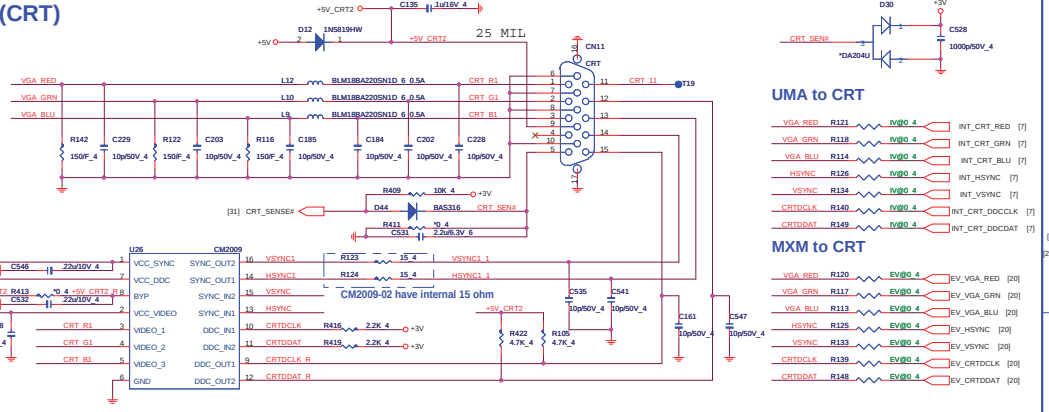


Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	NV10X VRAM-1(GDDR2 BGA84)	1A
Date: Tuesday, May 19, 2009	Sheet 22 of 39	

CRT(CRT)



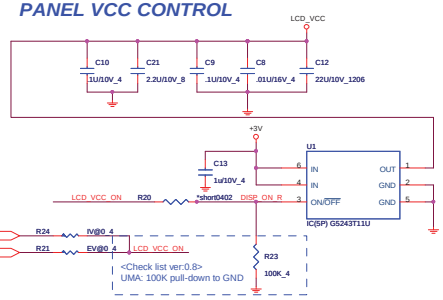
UMA to CRT

VGA_RED	R121 IV@0_4	INT_CRT_RED [7]	
VGA_GRN	R118 IV@0_4	INT_CRT_GRN [7]	
VGA_BLU	R114 IV@0_4	INT_CRT_BLU [7]	
HSYNC	R126 IV@0_4	INT_HSYNC [7]	
VSYNC	R134 IV@0_4	INT_VSYNC [7]	
CRTDCLK	R140 IV@0_4	INT_CRT_DDCCLK [7]	
CRTDDAT	R149 IV@0_4	INT_CRT_DDCDAT [7]	

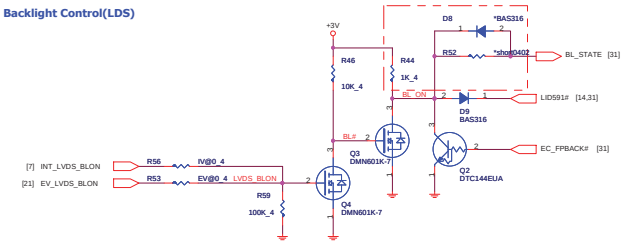
MXM to CRT

VGA_RED	R120 EV@0_4	EV_VGA_RED [20]	
VGA_GRN	R117 EV@0_4	EV_VGA_GRN [20]	
VGA_BLU	R113 EV@0_4	EV_VGA_BLU [20]	
HSYNC	R125 EV@0_4	EV_HSYNC [20]	
VSYNC	R133 EV@0_4	EV_VSYNC [20]	
CRTDCLK	R139 EV@0_4	EV_CRTDCLK [20]	
CRTDDAT	R148 EV@0_4	EV_CRTDDAT [20]	

LCD_ON(LDS) PANEL VCC CONTROL

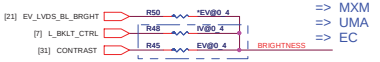


Backlight Control(LDS)



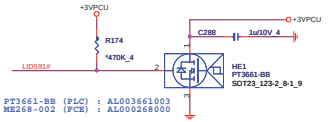
LVDS(LDS)

BRIGHTNESS
DPST



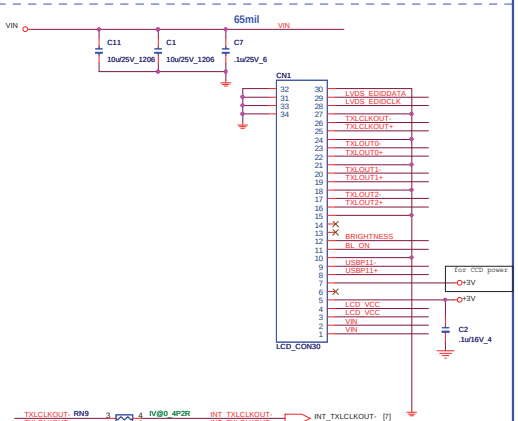
=> MXM
=> UMA
=> EC

Lid Switch (HSR)



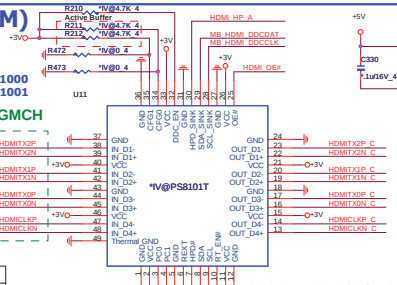
PT3661-BB (PLC) : AL003661003
MS268-002 (PCB) : AL000268000

LCD EDID SMBus PU

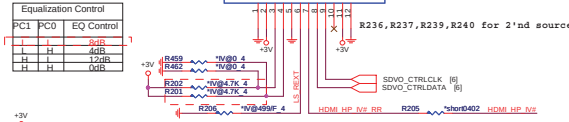


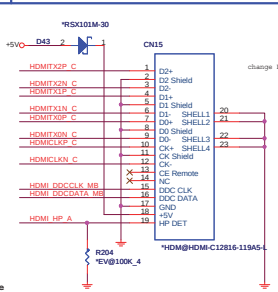
HDMI(HDM)

PS8101 : AL008101000
PS8101T : AL008101001



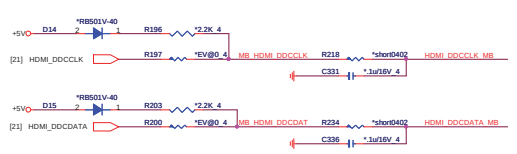
R236,R237,R239,R240 for 2'nd source



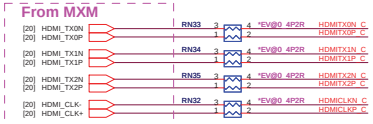


FOR UMA iHDMI HPD

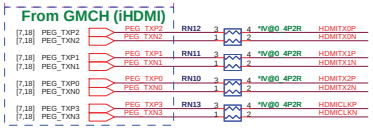
SDVO I2C Control



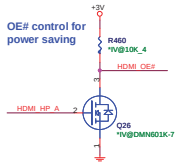
From MXM



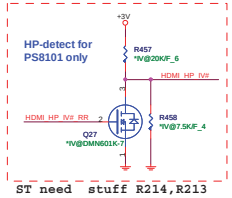
From GMCH (iHDMI)



OE# control for power saving

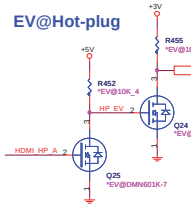


HP-detect for PS8101 only



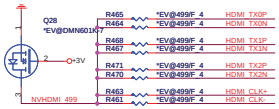
ST need stuff R214,R213

EV@Hot-plug

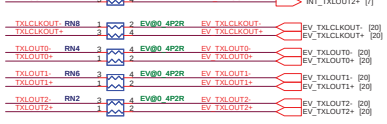


FOR NV HDMI

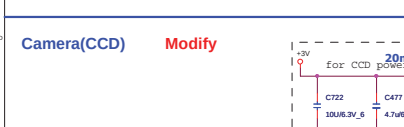
NV suggestion near HDMI connector



UMA to LVDS

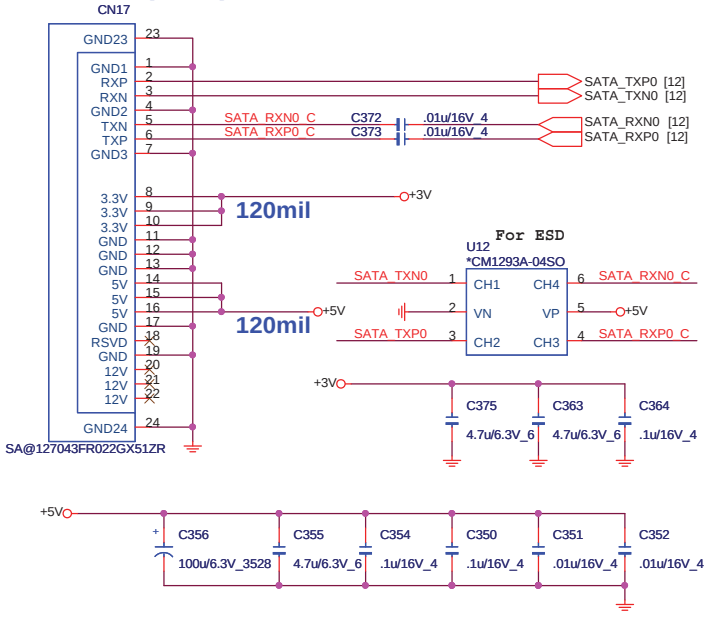


MXM to LVDS

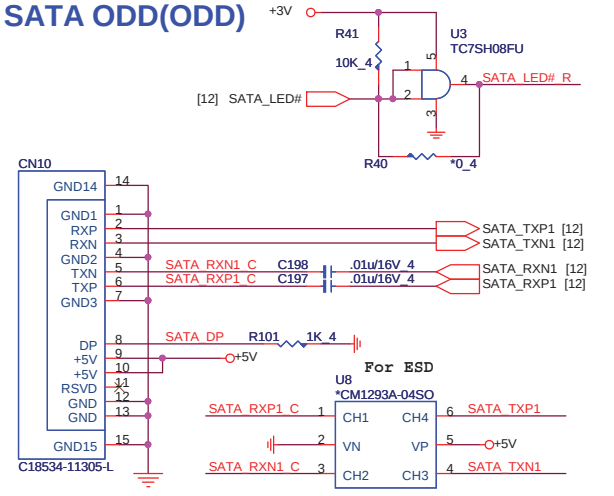


Camera(CCD) Modify

SATA HDD(HDD)

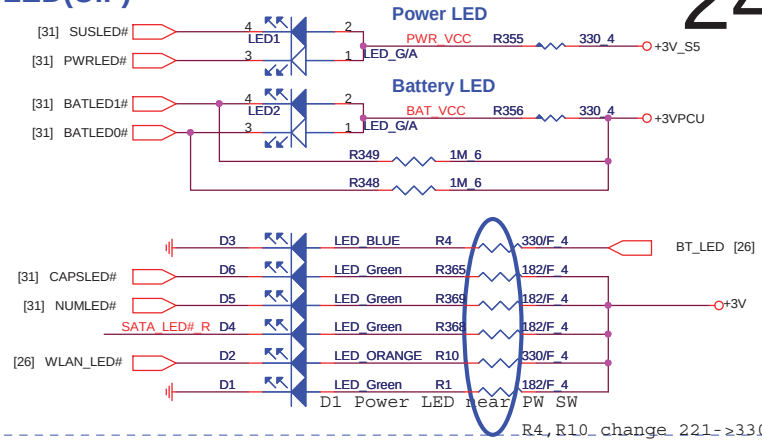


SATA ODD(ODD)



LED(UIF)

Power/Suspend: Green/Amber

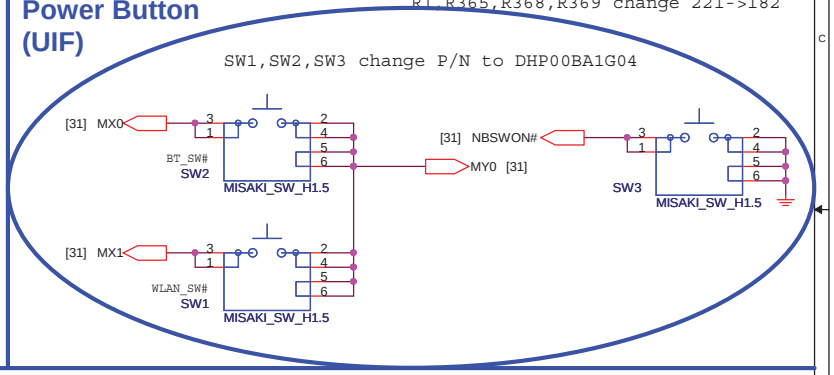


R4,R10 change 221->330

R1,R365,R368,R369 change 221->182

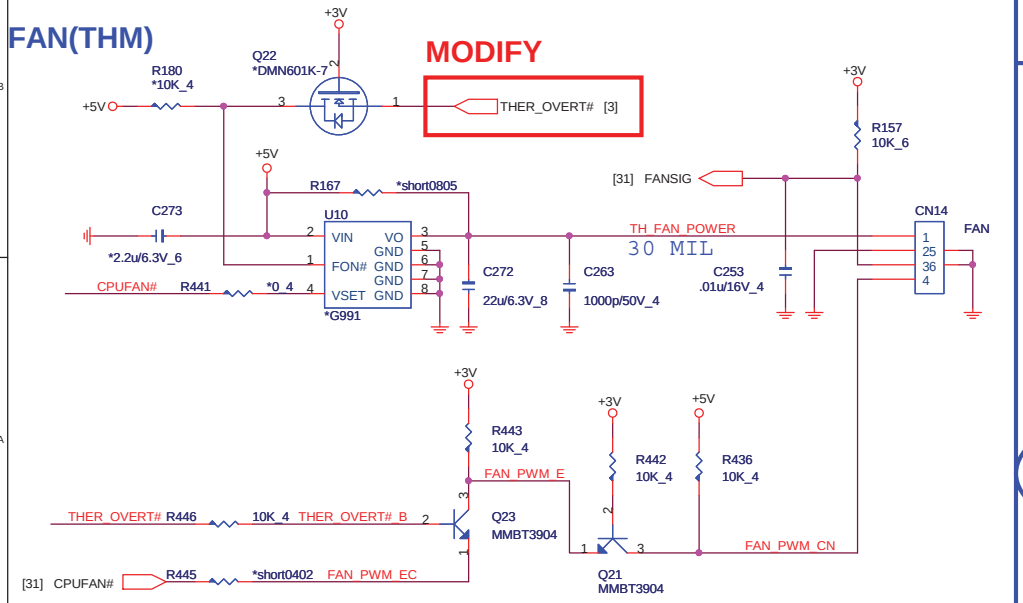
Power Button (UIF)

SW1,SW2,SW3 change P/N to DHP00BA1G04



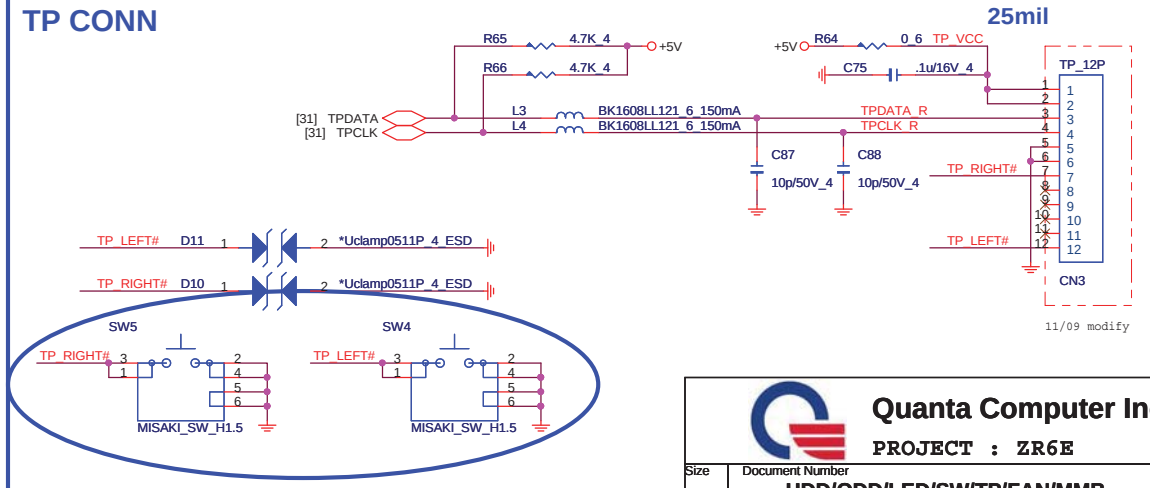
FAN(THM)

MODIFY



TP CONN

25mil



11/09 modify

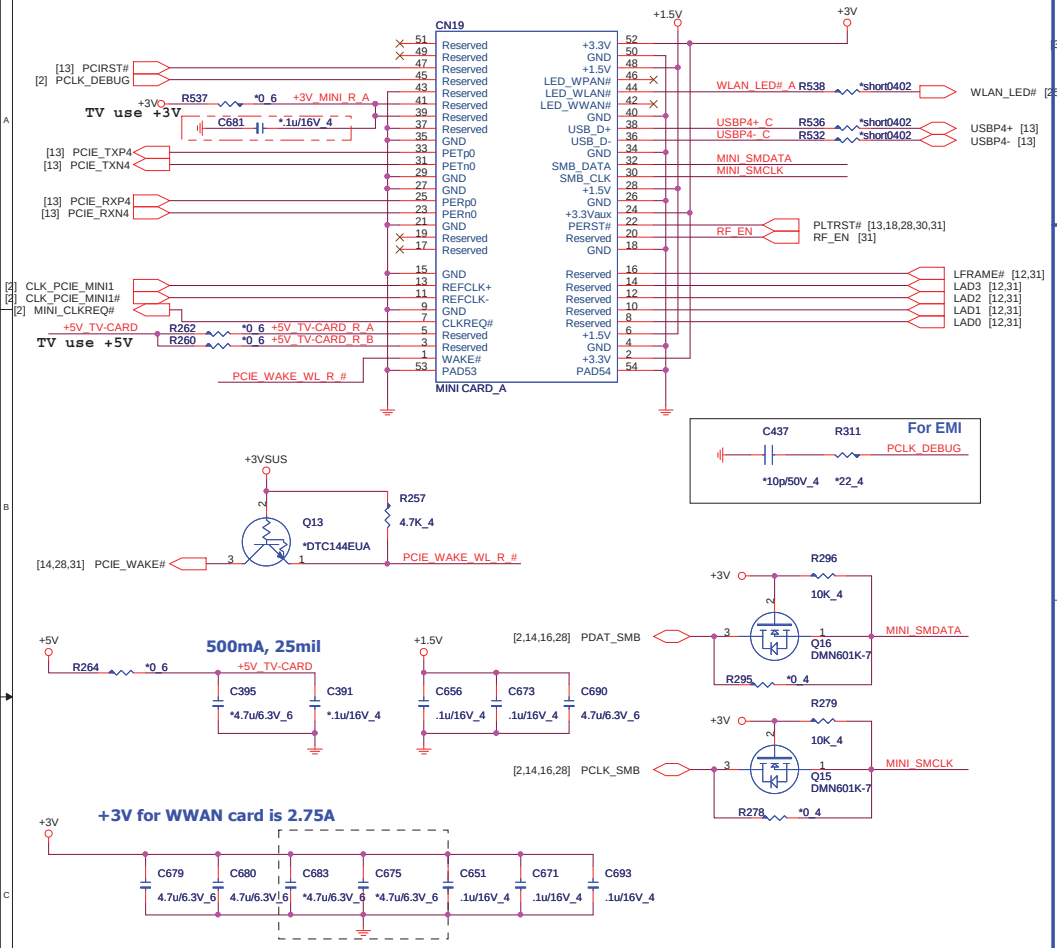
SW4,SW5 change P/N to DHP00BA1G04

Quanta Computer Inc.

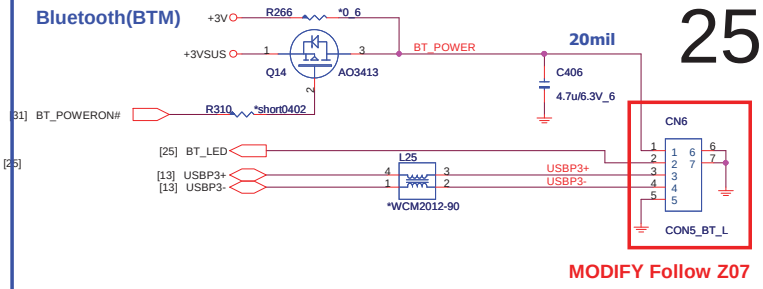
PROJECT : ZR6E

Size	Document Number	Rev
	HDD/ODD/LED/SW/TP/FAN/MMB	1A
Date: Tuesday, May 19, 2009	Sheet 24 of 39	

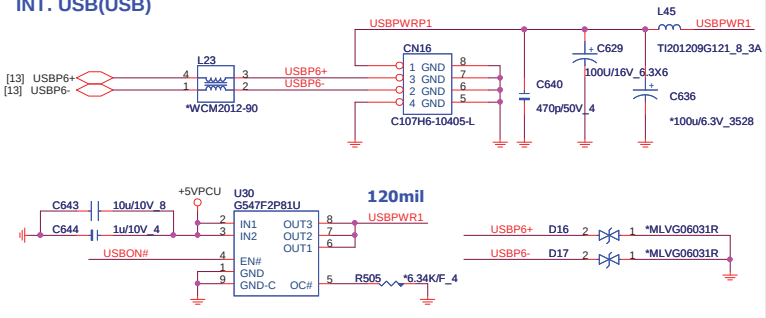
MINI-CARD(MPC)



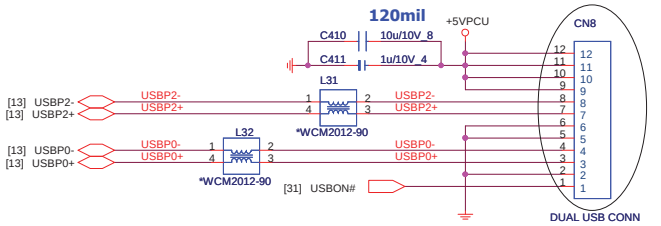
Bluetooth(BTM)



INT. USB(USB)

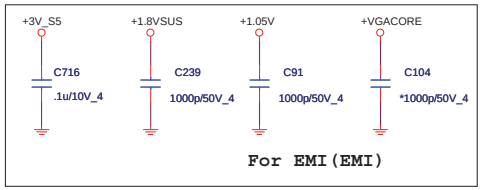


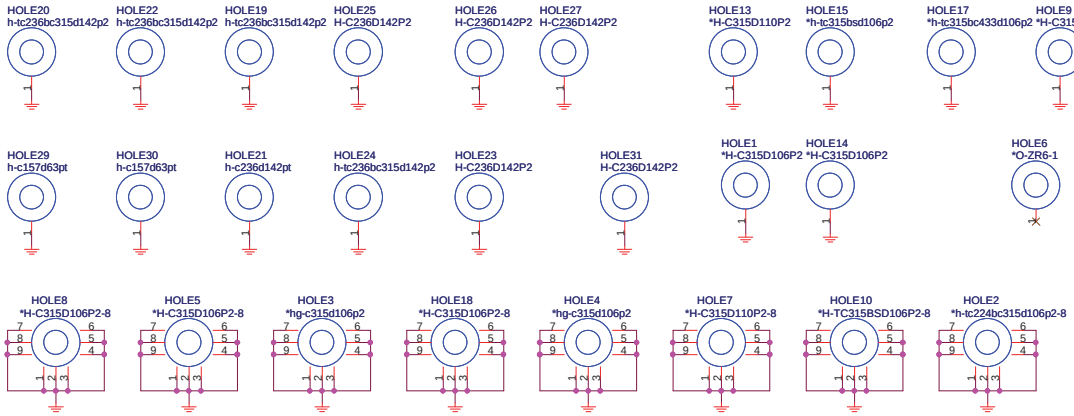
EXT. USB(USB)



Modfiy C

(OTH)





Quanta Computer Inc.

PROJECT : ZR6E

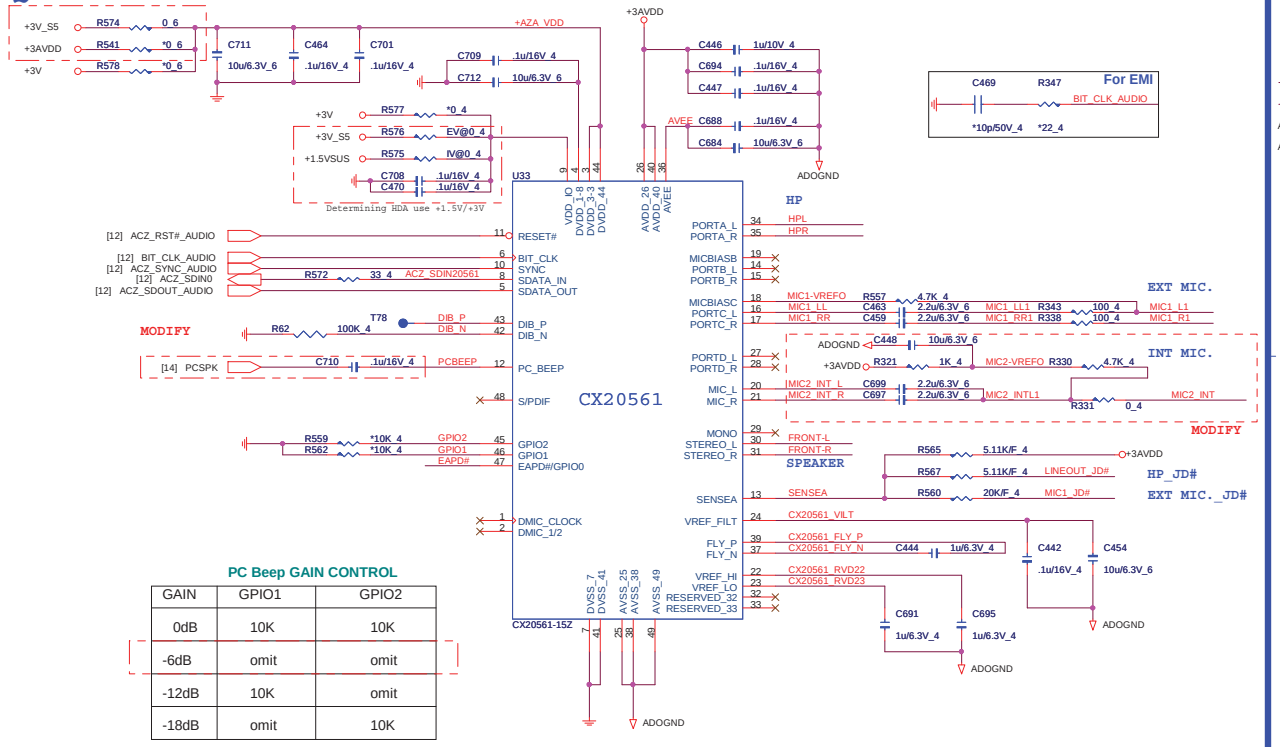
Size	Document Number	Rev
	MINI/USB/BT/HOLE	1A
Date: Tuesday, May 19, 2009	Sheet 25 of 39	

25

Codec CX20561-15Z (ADO)

QFN

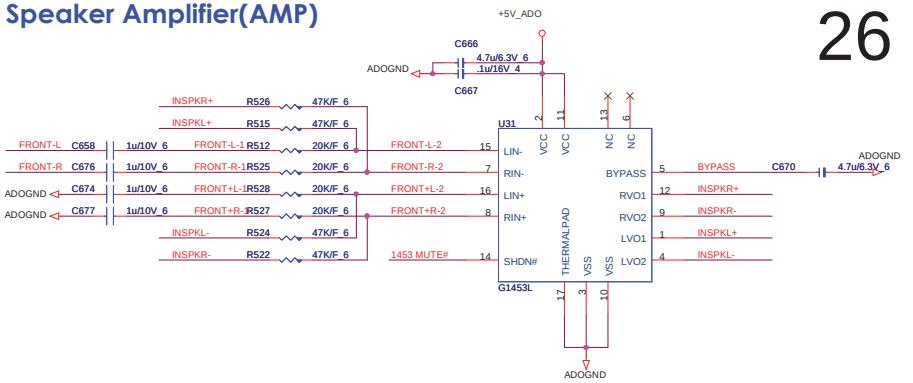
MODIFY REV:C



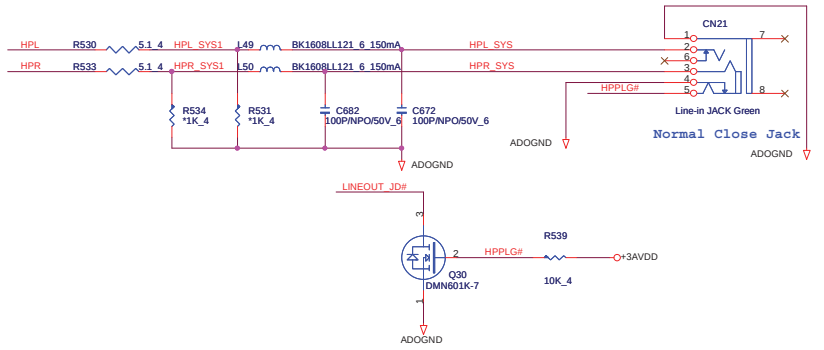
PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

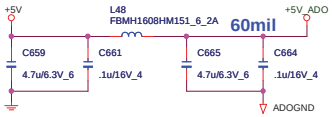
Speaker Amplifier(AMP)



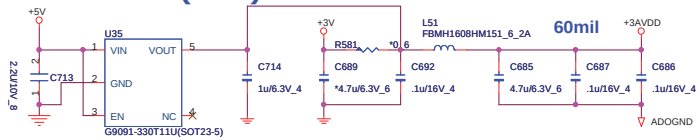
LINE OUT(AMP)



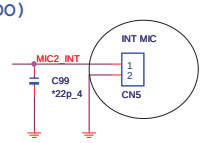
AMP Power(AMP)



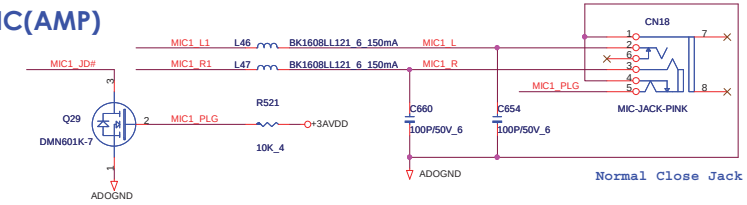
CODER Power(ADO)



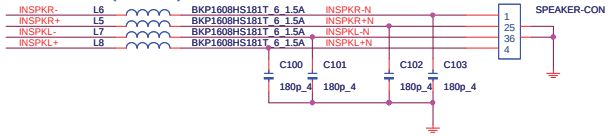
INT MIC.(ADO)



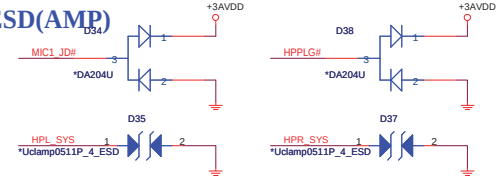
MIC(AMP)



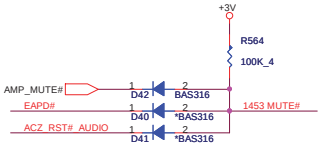
SPEAKER(AMP)



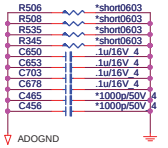
ESD(AMP)



MUTE(AMP)



(ADO)



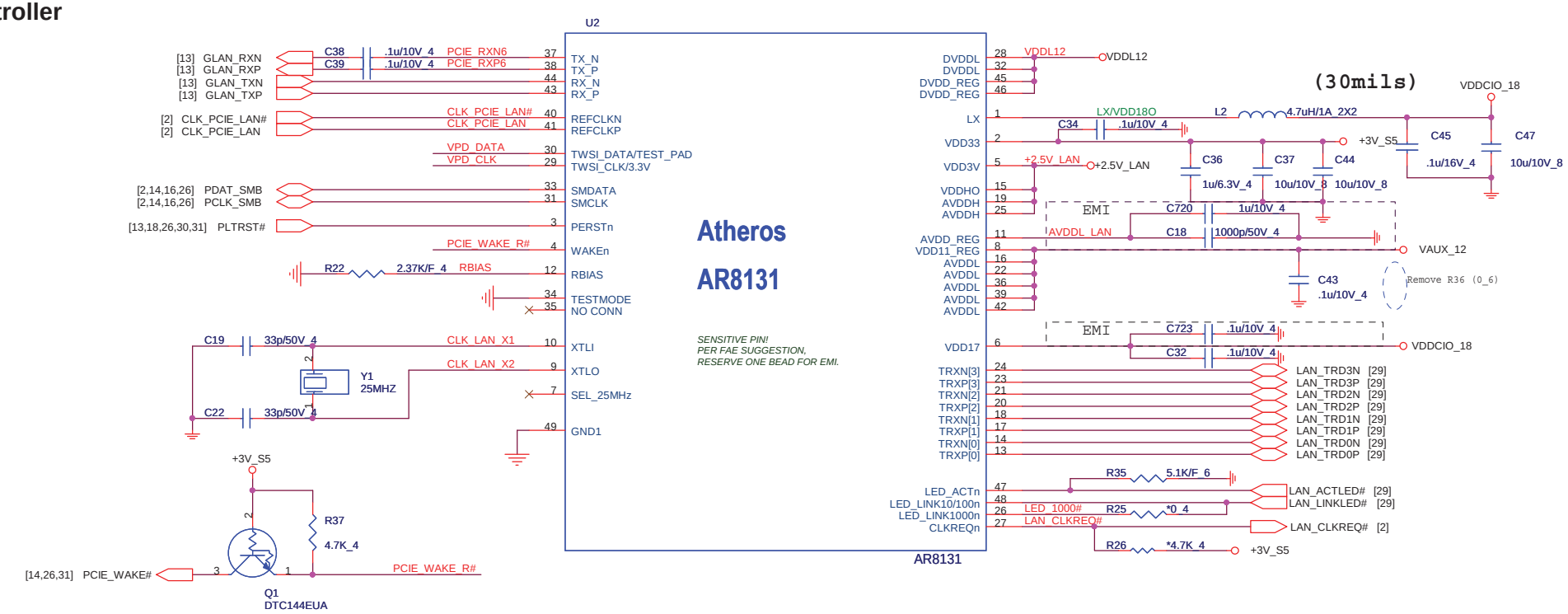
Quanta Computer Inc.

PROJECT : ZR6E

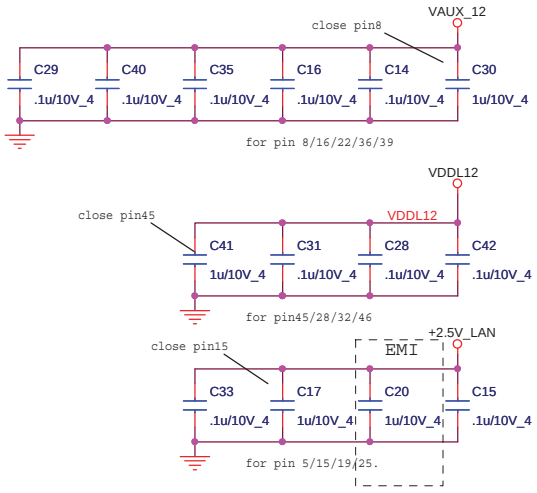
Size	Document Number	Rev
	CODEC/AMP/MDC	1A

Date: Tuesday, May 19, 2009 Sheet 26 of 39

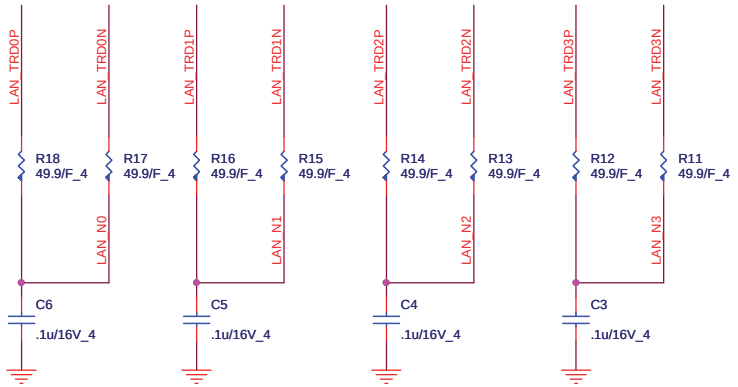
LAN Controller



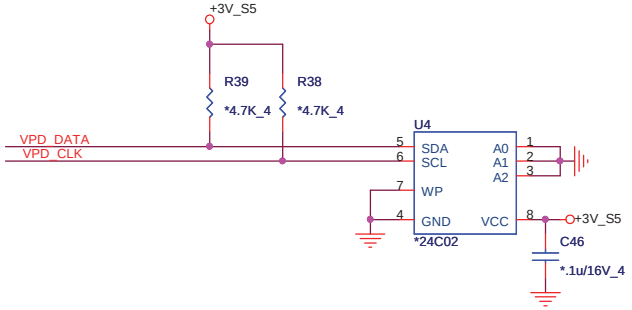
Decoupling CAP



PLACE NEAR IC SIDE



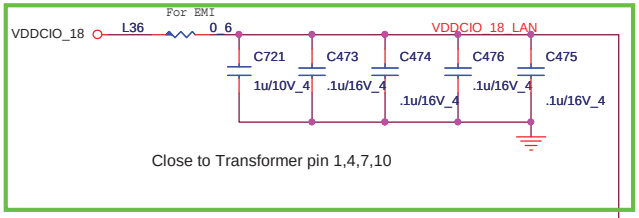
EEPROM



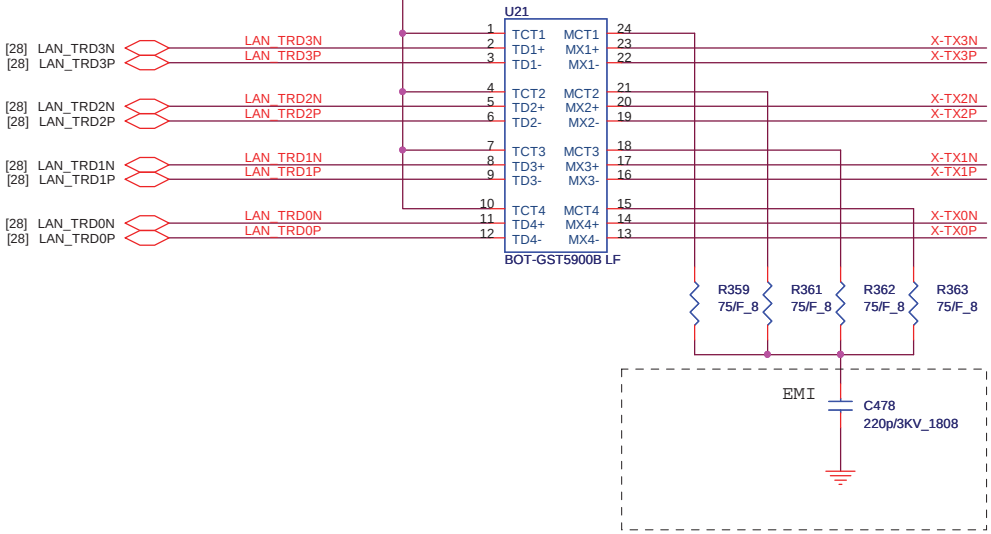
Quanta Computer Inc.

PROJECT : ZR6E

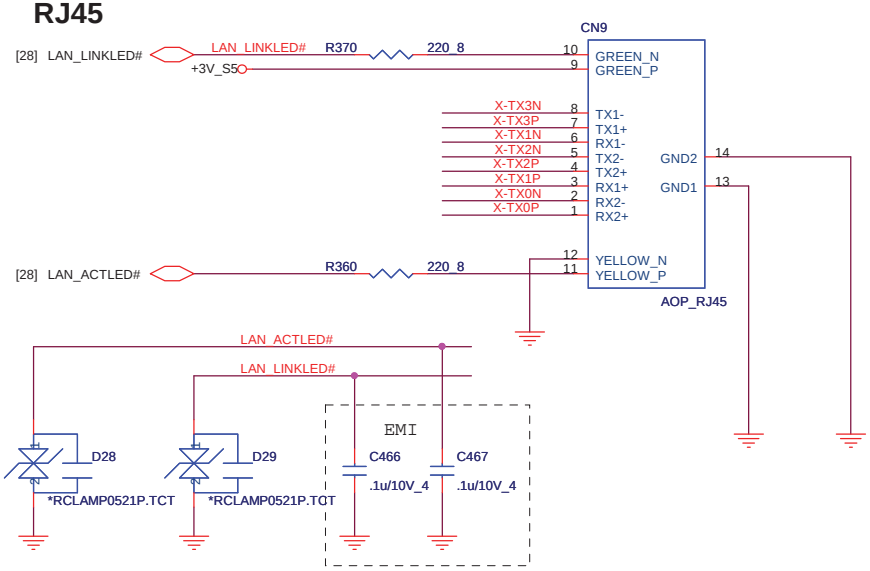
Size	Document Number	Rev
	AR8131 GLAN	1A
Date: Tuesday, May 19, 2009	Sheet 27 of 39	



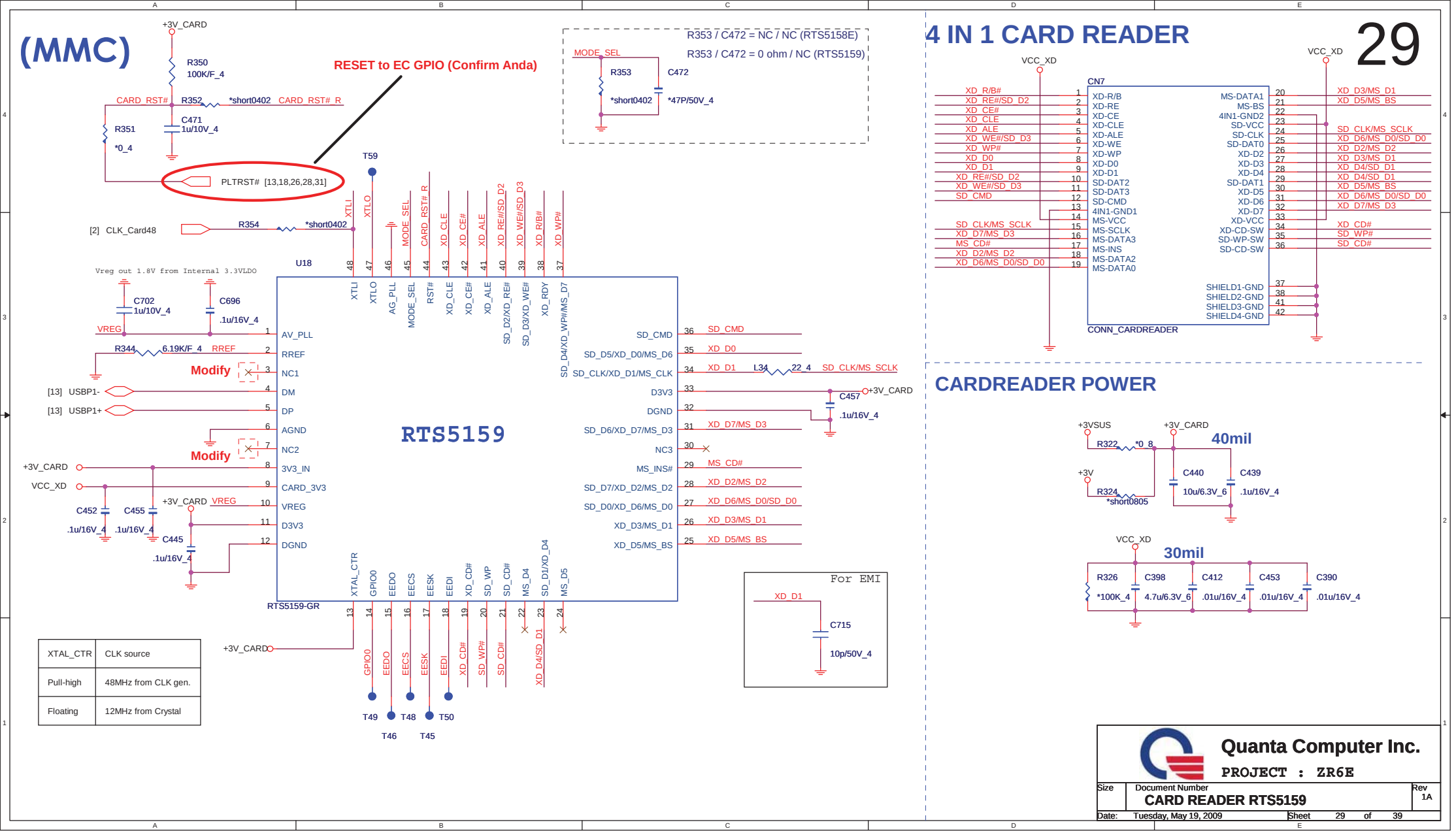
TRANSFORMER



RJ45



Quanta Computer Inc.		
PROJECT : ZR6E		
Size	Document Number: LAN Transformer and RJ45/BT	Rev 1A
Date: Tuesday, May 19, 2009	Sheet 28 of 39	


(MMC)
RESET to EC GPIO (Confirm Anda)
R353 / C472 = NC / NC (RTS5158E)
R353 / C472 = 0 ohm / NC (RTS5159)
MODE_SEL
R353
C472
*short0402
*47P/50V_4
+3V_CARD
R350
100K/F_4
CARD_RST#
R352
*short0402
CARD_RST#_R
R351
*0_4
C471
1u/10V_4
PLTRST# [13,18,26,28,31]
T59
[2] CLK_Card48
R354
*short0402
Vreg out 1.8V from Internal 3.3VLDO
C702
1u/10V_4
C696
.1u/16V_4
VREG
R344
6.19K/F_4
RREF
Modify
[13] USBP1-
[13] USBP1+
Modify
+3V_CARD
VCC_XD
C452
C455
.1u/16V_4
.1u/16V_4
+3V_CARD
VREG
C445
.1u/16V_4
U18
RTS5159
RTS5159-GR
AV_PLL
RREF
NC1
DM
DP
AGND
NC2
3V3_IN
CARD_3V3
VREG
D3V3
DGND
XTLI
XTLO
AG_PLL
MODE_SEL
RST#
XD_CLE
XD_CE#
XD_ALE
SD_D2/XD_RE#
SD_D3/XD_WE#
XD_RDY
SD_D4/XD_WP#/MS_D7
SD_CMD
SD_D5/XD_D0/MS_D6
SD_CLK/XD_D1/MS_CLK
D3V3
DGND
SD_D6/XD_D7/MS_D3
NC3
MS_INS#
SD_D7/XD_D2/MS_D2
SD_D0/XD_D6/MS_D0
XD_D3/MS_D1
XD_D5/MS_BS
XTAL_CTR
GPIO0
EEDO
EECS
EESK
EEDI
XD_CD#
SD_WP
SD_CD#
MS_D4
SD_D1/XD_D4
MS_D5
SD_CMD
XD_D0
XD_D1
L34
22_4
SD_CLK/MS_SCLK
C457
.1u/16V_4
XD_D7/MS_D3
MS_CD#
XD_D2/MS_D2
XD_D6/MS_D0/SD_D0
XD_D3/MS_D1
XD_D5/MS_BS
For EMI
XD_D1
C715
10p/50V_4
+3V_CARD
GPIO0
EEDO
EECS
EESK
EEDI
XD_CD#
SD_WP#
SD_CD#
XD_D4/SD_D1
T49
T48
T50
T46
T45
XTAL_CTR | CLK source
Pull-high | 48MHz from CLK gen.
Floating | 12MHz from Crystal
4 IN 1 CARD READER
29
VCC_XD
CN7
XD_R/B#
XD_RE#/SD_D2
XD_CE#
XD_CLE
XD_ALE
XD_WE#/SD_D3
XD_WP#
XD_D0
XD_D1
XD_RE#/SD_D2
XD_WE#/SD_D3
SD_CMD
SD_CLK/MS_SCLK
XD_D7/MS_D3
MS_CD#
XD_D2/MS_D2
XD_D6/MS_D0/SD_D0
XD-R/B
XD-RE
XD-CE
XD-CLE
XD-ALE
XD-WE
XD-WP
XD-D0
XD-D1
SD-DAT2
SD-DAT3
SD-CMD
4IN1-GND1
MS-VCC
MS-SCLK
MS-DATA3
MS-INS
MS-DATA2
MS-DATA0
MS-DATA1
MS-BS
4IN1-GND2
SD-VCC
SD-CLK
SD-DAT0
XD-D2
XD-D3
XD-D4
SD-DAT1
XD-D5
XD-D6
XD-D7
XD-VCC
XD-CD-SW
SD-WP-SW
SD-CD-SW
SHIELD1-GND
SHIELD2-GND
SHIELD3-GND
SHIELD4-GND
XD_D3/MS_D1
XD_D5/MS_BS
SD_CLK/MS_SCLK
XD_D6/MS_D0/SD_D0
XD_D2/MS_D2
XD_D3/MS_D1
XD_D4/SD_D1
XD_D4/SD_D1
XD_D5/MS_BS
XD_D6/MS_D0/SD_D0
XD_D7/MS_D3
XD_CD#
SD_WP#
SD_CD#
CONN_CARDREADER
CARDREADER POWER
+3VSUS
+3V_CARD
R322
*0_8
40mil
+3V
R324
*short0805
C440
10u/6.3V_6
C439
.1u/16V_4
VCC_XD
30mil
R326
*100K_4
C398
4.7u/6.3V_6
C412
.01u/16V_4
C453
.01u/16V_4
C390
.01u/16V_4
Quanta Computer Inc.
PROJECT : ZR6E
Size
Document Number
CARD READER RTS5159
Rev
1A
Date: Tuesday, May 19, 2009
Sheet 29 of 39

EC(KBC)

I/O ADDRESS SETTING

BADDR1-0	I/O Address	
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 — BADDR0 — R303 10K_4
BADDR1 — uR_SOUT_CR — R302 *10K_4
SHBM — SHBM — R269 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

+3VPCU
MBCLK — R513 4.7K_4
MBDATA — R509 4.7K_4
MXM_SMCLK — R304 4.7K_4
MXM_SMDATA — R305 4.7K_4
+3V
2ND_MBCLK — R259 4.7K_4
2ND_MBDATA — R261 4.7K_4
CRT_SENSE# — R523 4.7K_4

ACER ID

MXM_SMCLK
MXM_SMDATA
U16 24C02 (SCL, SDA, A0, A1, A2, WP, VCC, GND)
+3VPCU — R316 *0_4
+3V_S5 — R323 *short0402
C449 *1.1u/16V_4_X7R

SPI FLASH

2'nd Source AKE38ZA0Q00

SPI_SDI_uR R325 22_4 SPI_SDI_uR_R
SPI_SDO_uR
SPI_SCK_uR
R333 10K_4 SPI_CS0# uR
U17 W25X16AVSSIG (SO, SI, SCK, CE, VDD, HOLD, WP, VSS)
C443 .1u/16V_4_X7R

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

HWPG

+3V — R273 10K_4
[37] 1V8_ON — D19 EV@BAS316
[38] HWPG_1.5V — D24 BAS316
[34] HWPG_1.05V — D20 BAS316
[36] HWPG_1.8V — D25 BAS316
[33] SYS_HWPG — D21 BAS316
[3,6,14,35] DELAY_VR_PWRGOOD — D22 *BAS316
[37] HWPG_1.1V — D23 EV@BAS316
HWPG — R263 *short0402 — MPWROK [6,14]

1'st AKE38ZP0N01 : Winbond W25X16AVSSIG
2'nd AKE37FP0Z13 : MXIC MX25L1605AM2C-15G
3'rd AKE38ZA0Q00 : EON EN25F16-100HIP
4'rd AKE38ZN0800 : AMIC A25L016

POWER-ON PAD(UIF)

G1 — NBSWON# — *SHORT_PAD

Thermal Sensor(THM)

+3V — R300 47K/F_4 — TPD_TRIP
R301 100K/F_4 NTC

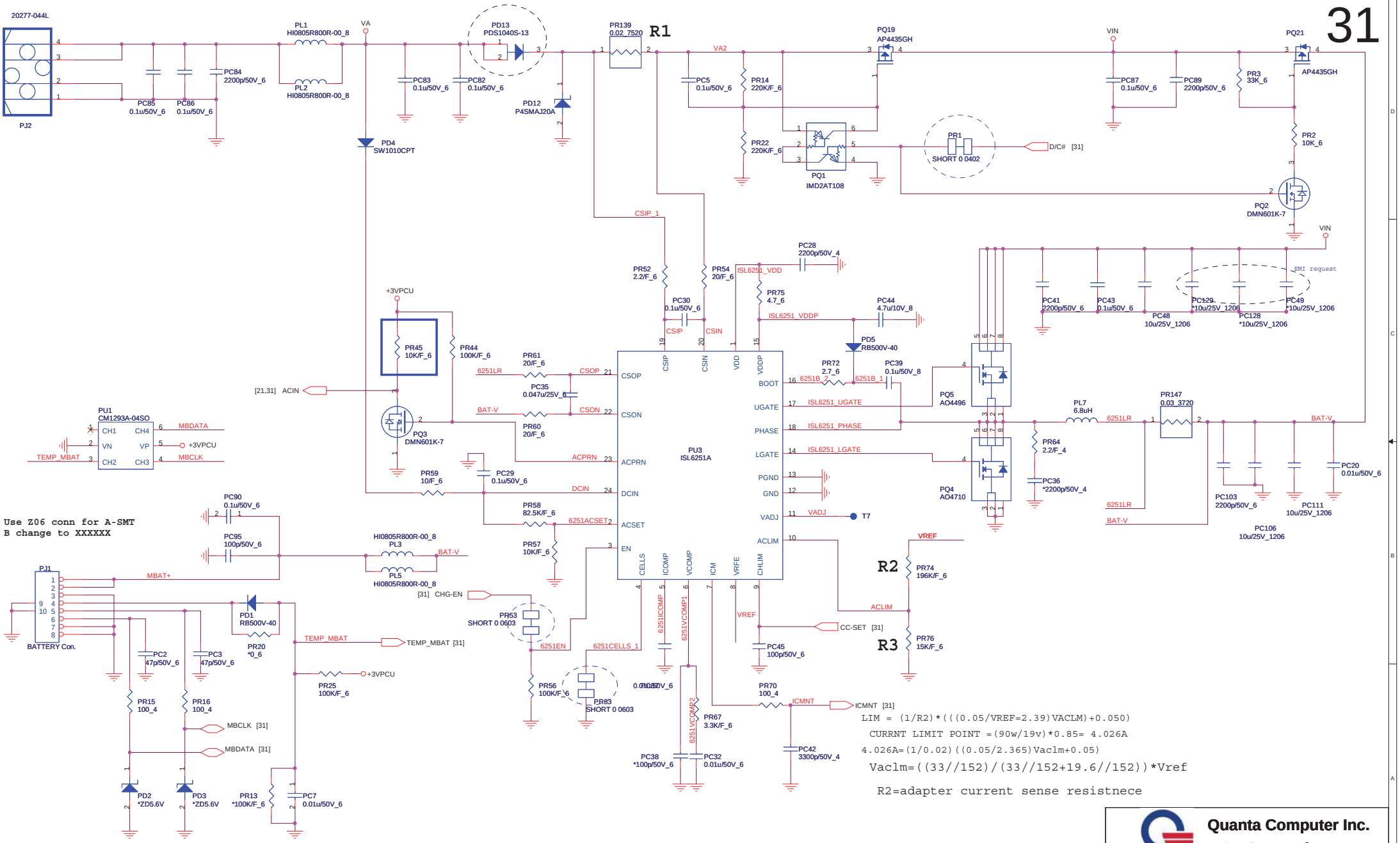
INTERNAL KEYBOARD STRIP SET

+3VPCU — MY0 — R247 10K_4

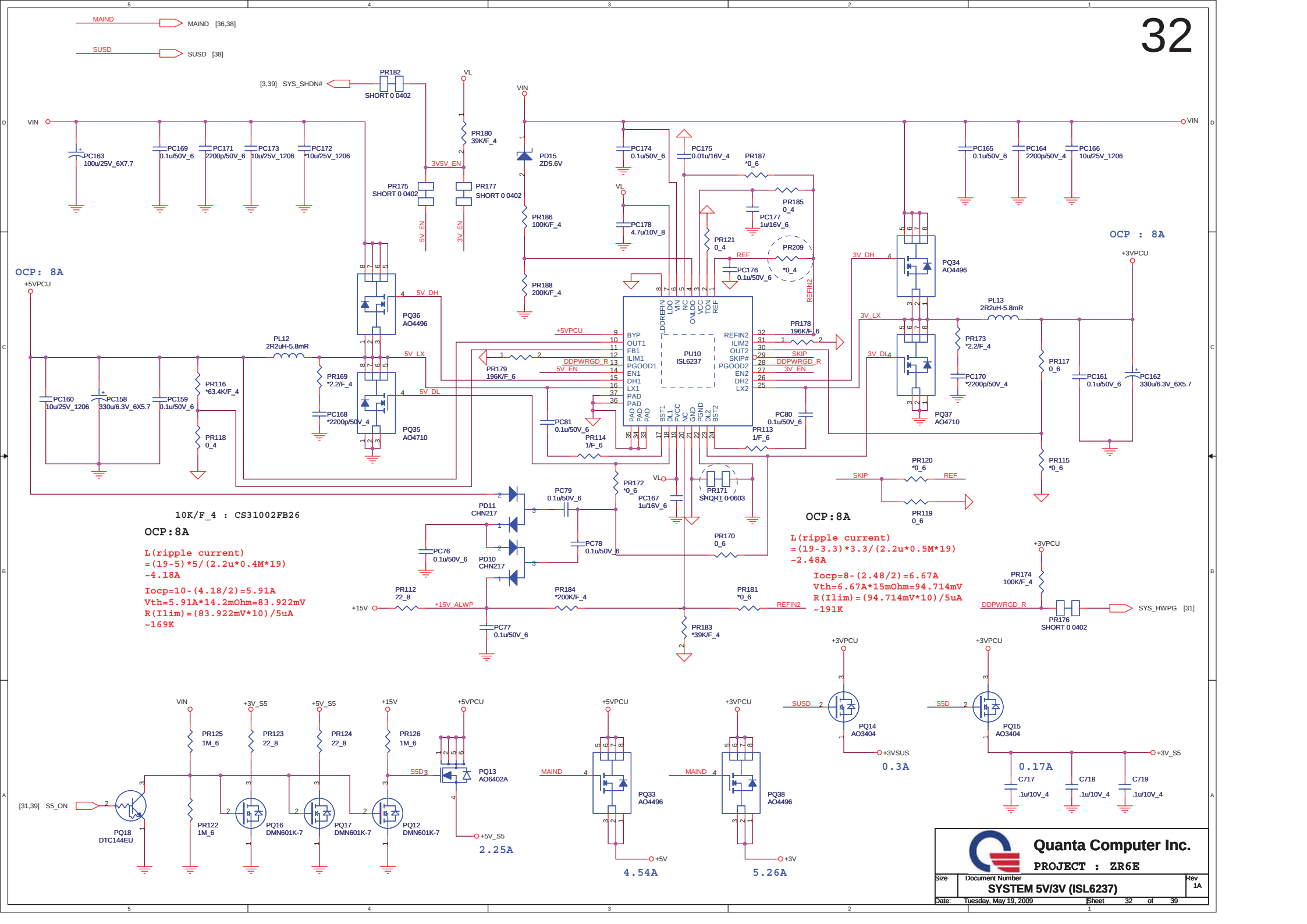
Quanta Computer Inc.
PROJECT : ZR6E

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A

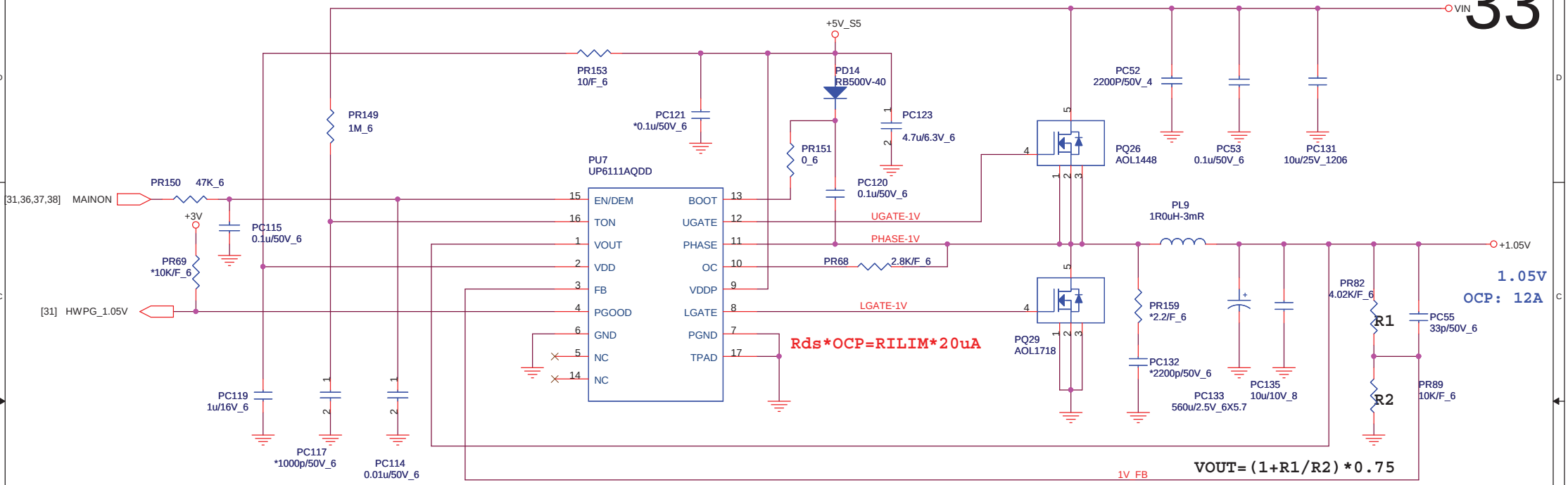
Date: Tuesday, May 19, 2009 Sheet 30 of 39



Quanta Computer Inc.		
PROJECT : ZR6E		
Size	Document Number: Charger (ISL6251A)	Rev: 1A
Date: Tuesday, May 19, 2009	Sheet 31 of 39	



Quanta Computer Inc.		
PROJECT : ZR6E		
Size	Document Number: SYSTEM 5V/3V (ISL6237)	Rev: 1A
Date: Tuesday, May 19, 2009	Sheet 32 of 39	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

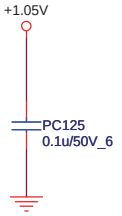
Frequency=1/(0.0036767)=272K

AOL1412 Rdson=4.6mOhm

OCP=16-0.8A

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

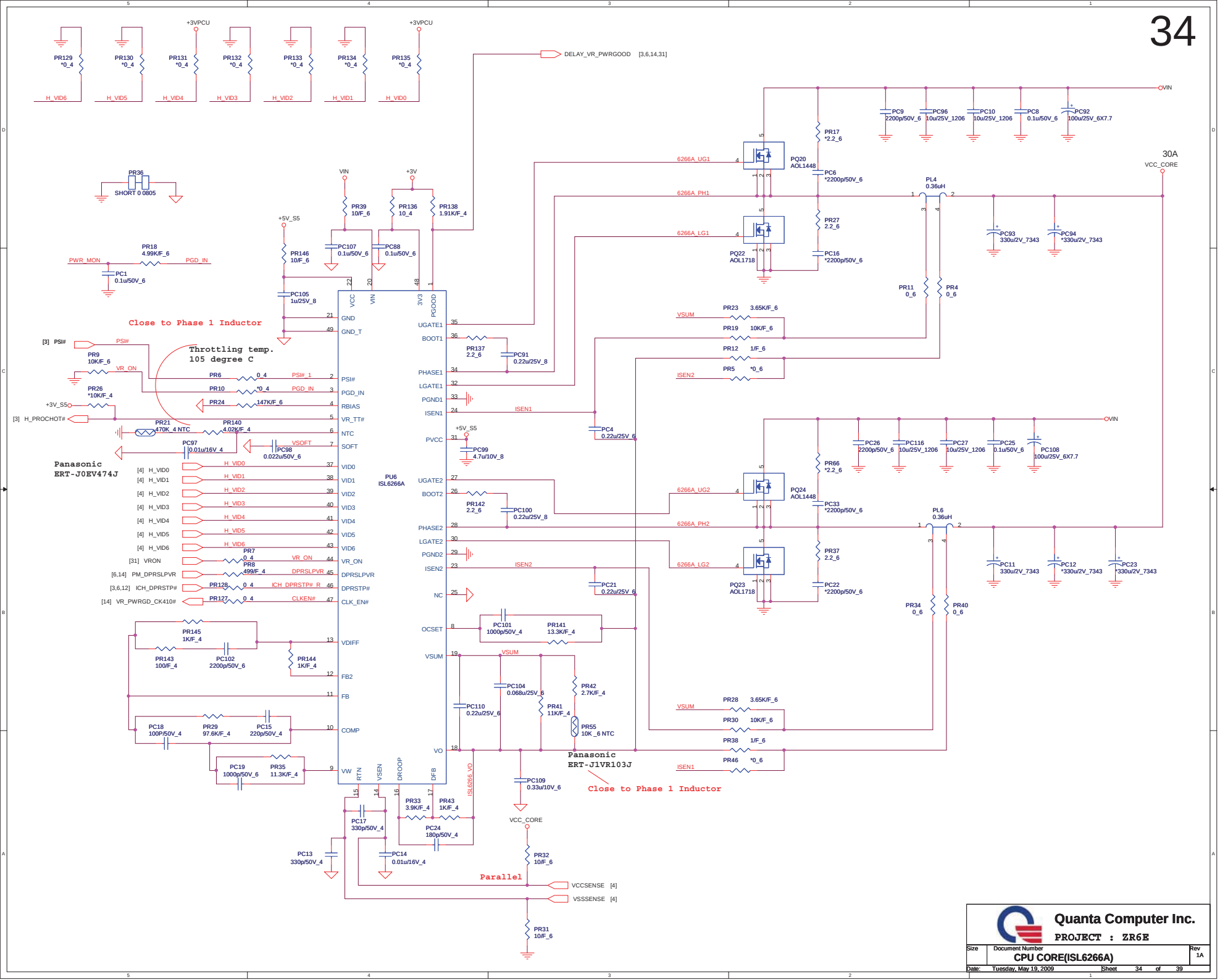
4.6m*12=RILIM*20uA
RILIM=2.76K--- 2.8K



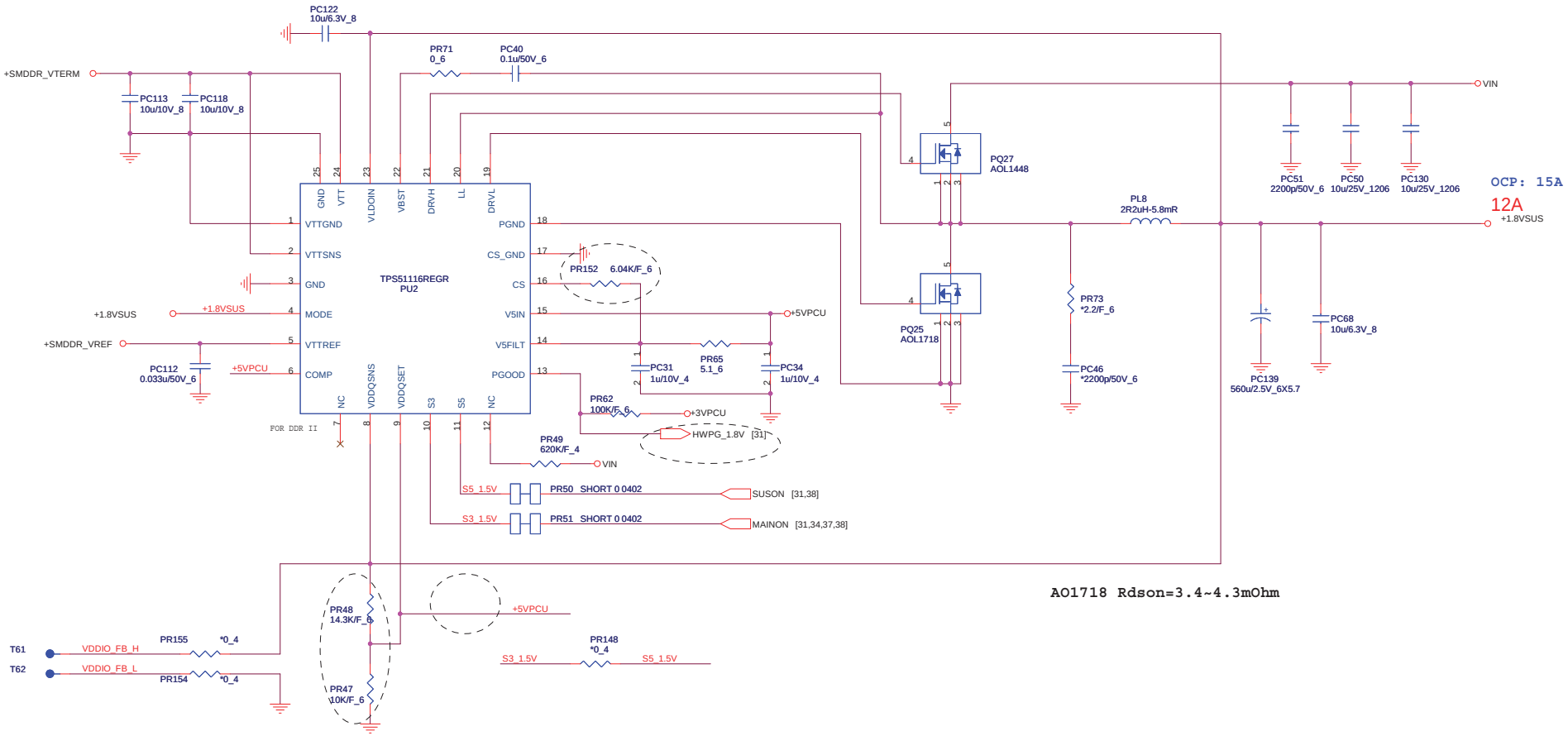
Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	VCCP 1.05V(UP6111A)	1A
Date: Tuesday, May 19, 2009	Sheet 33 of 39	



Quanta Computer Inc.			
PROJECT : ZR6E			
Size	Document Number		Rev
	CPU CORE(ISL6266A)		1A
Date: Tuesday, May 19, 2009		Sheet 34 of 39	

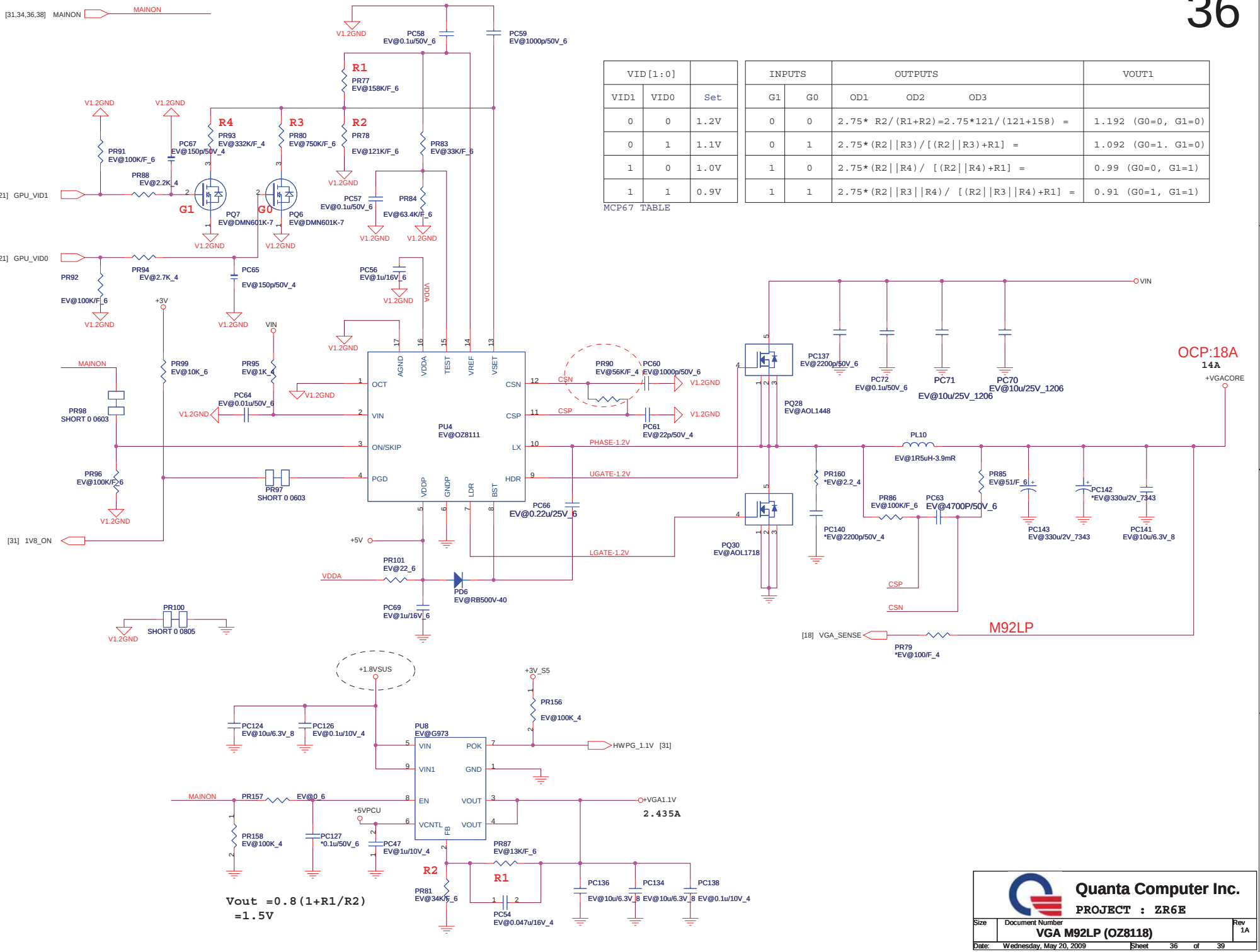


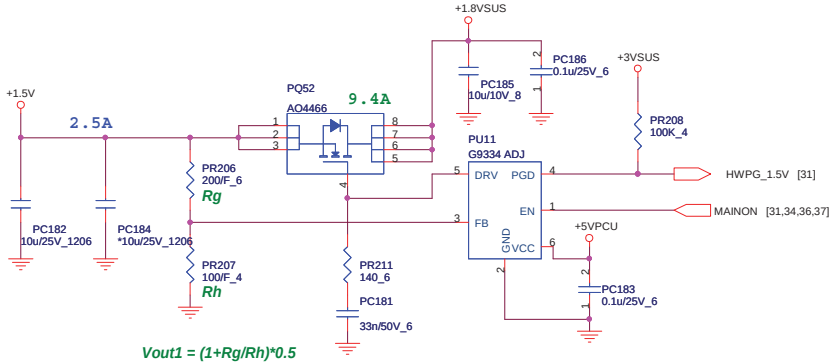
Quanta Computer Inc.		
PROJECT : ZR6E		
Size	Document Number: DDR 1.5V(TPS51116)	Rev: 1A
Date: Wednesday, May 20, 2009	Sheet 35 of 39	

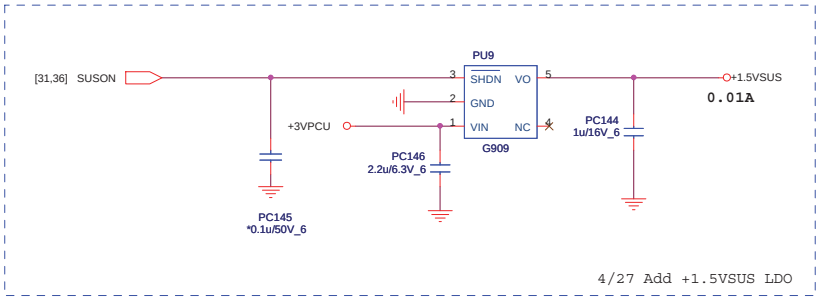
VID[1:0]		
VID1	VID0	Set
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

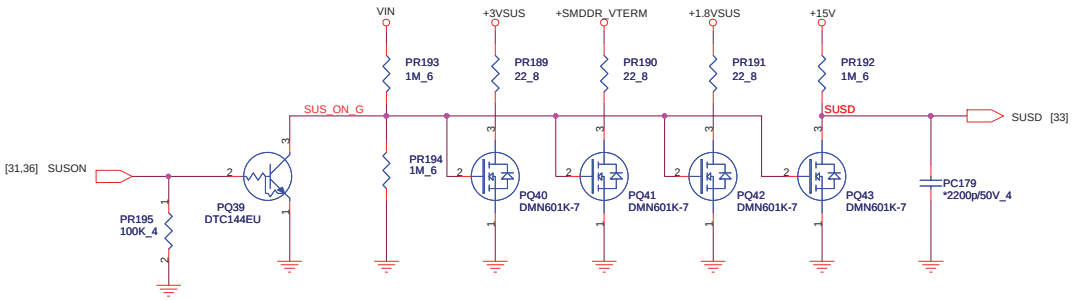
MCP67 TABLE

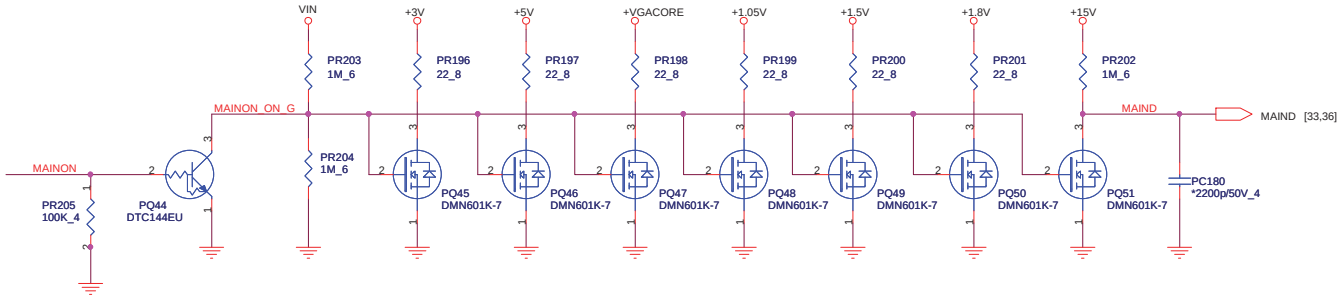
INPUTS		OUTPUTS	VOUT1
G1	G0	OD1 OD2 OD3	
0	0	2.75* R2/(R1+R2)=2.75*121/(121+158) =	1.192 (G0=0, G1=0)
0	1	2.75*(R2||R3)/[(R2||R3)+R1] =	1.092 (G0=1. G1=0)
1	0	2.75*(R2||R4)/ [(R2||R4)+R1] =	0.99 (G0=0, G1=1)
1	1	2.75*(R2||R3||R4)/ [(R2||R3||R4)+R1] =	0.91 (G0=1, G1=1)









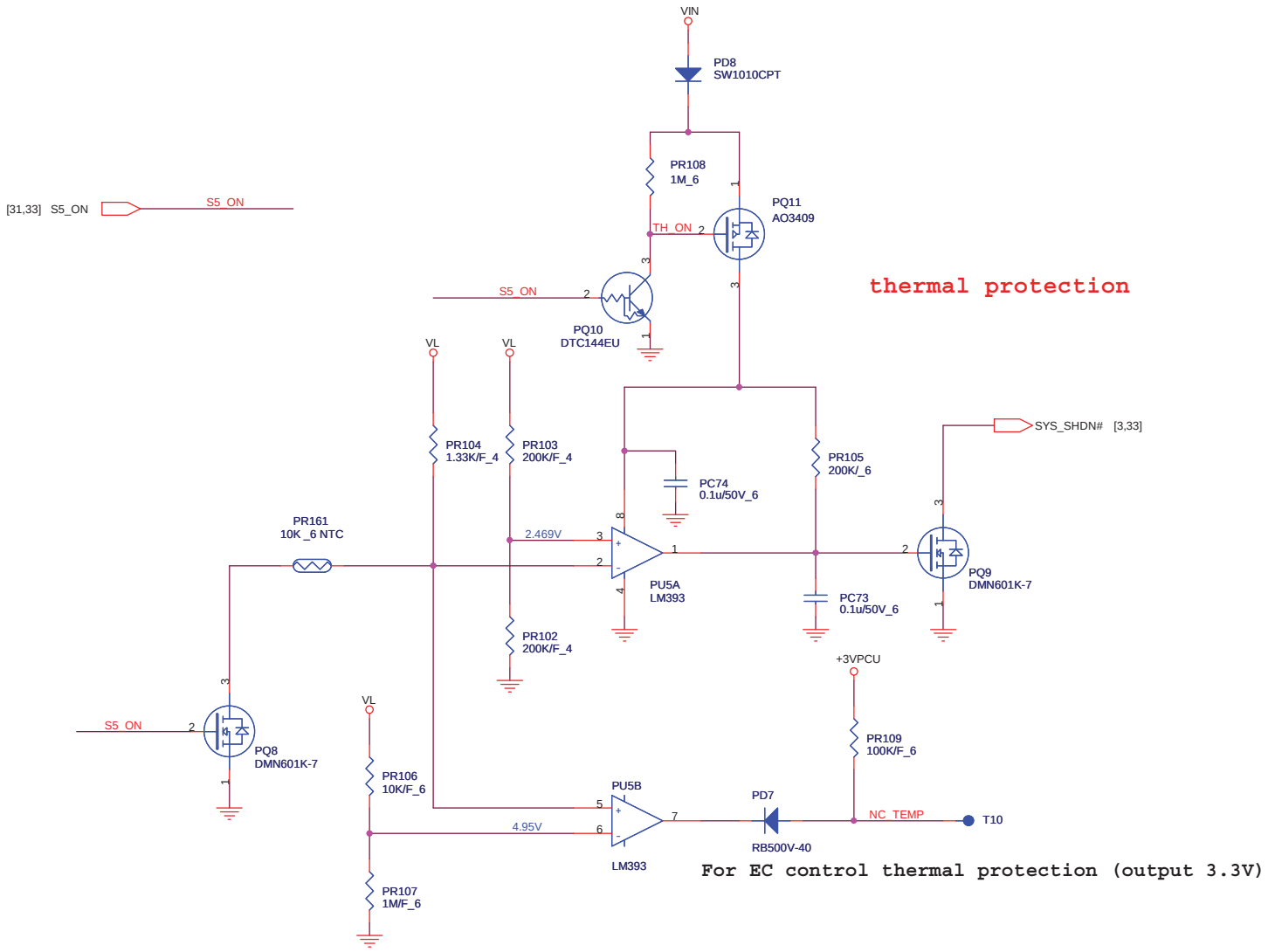


Quanta Computer Inc.

PROJECT : ZR6E

Size	Document Number	Rev
	Discharge	1A

Date: Tuesday, May 19, 2009 Sheet 37 of 39



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PROJECT : ZR6E		
Size	Document Number: Thermal Protection	Rev: 1A
Date: Tuesday, May 19, 2009	Sheet 38 of 39	

MODEL: REV

CHANGE LIST

ZR6 MB

PAGE \ MODEL	ZR6 MB FROM	ZR6 MB TO
1	1A	
2	1A	3B
3	1A	
4	1A	
5	2A	
6	1A	
7	1A	
8	1A	
9	3A	
10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
18	2A	
19	3A	
20	1A	
21	3A	
22	1A	
23	3A	
24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
30	1A	
31	3A	
32	2A	
33	2A	
34	2A	
35	2A	3B
36	2A	
37	2A	
38	2A	
39	3A	3B
40		

MB Assy' P/N: 31ZR6MB00B0,C0,D0,E0,F0,G0

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Document No.:

Approved by :

Drawing by : James Chen

DATE:

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PROJECT : ZR6E

Size	Document Number	Rev
	Thermal Protection	1A

Date: Tuesday, May 19, 2009 Sheet 39 of 39