Dallen Block Diagram

Project code: 91.4V401.001
PCB P/N : 48.4T307.0SA
Revision : 06259 -1

CLK GEN.
RTM865T-433
71.00865.B0W 3

Mobile CPU
Yonah 478
Celeron M
62.10079.001 4, 5

G792
74.00792.A79 19

HOST BUS 400/533/667MHz@1.05V

DDR2 533/667 MHz 11,12
DDR2 533/667 MHz 11,12
533/667 MHz
533/667 MHz

Calistoga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
71.CALIS.00U 6,7,8,9,10

X4 DMI 400MHz
C-Link0

TV Out 14
CRT 14
LCD 14
DVI 43
MXM conn. 27

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

Line In
MIC In
29
30
INT.SPKR
Line Out
(No-SPDIF)

ALC268
71.00268.00G 29
AZALIA
OP AMP G1431 30
OP AMP G1412 30

ICH7M
4 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
2 SATA
1 PATA 66/100
8 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
71.ICH7M.00U 15,16,17,18

PCI BUS
TI PCI7412
Cardbus Cardreader 24,25
PCMCIA I/F
PWR SW CP2211F 25
PCMCIA SLOT Support TypeII 26
1394 conn. 26
MS/MS Pro/xD/ MMC/SD 5 in 1 26

LAN GIGA BCM5787M 22
TXFM 23
RJ45 23
PCIex1
Mini Card Kedron a/b/g/n 28

RJ11
MODEM MDC Card 21

LPC BUS
LPC DEBUG CONN. 33

New card 28
PCI Express
SATA
PATA
USB

MINI USB BlueTooth 21
Finger Pad 32
USB 4 Port 21
CCD 13

KBC Winbond WPC8763L 31
SPI I/F
BIOS W25X80-VSS 33
Touch Pad 32
INT. KB 32
FIR 31

P2231NFC1 28
HDD 20
ODD 20

SYSTEM DC/DC MAX8744 37	
INPUTS	OUTPUTS
DCBATOUT	3D3V_S5(6A) 5V_S5 (6A) 5V_AUX_S5

SYSTEM DC/DC Max8717 38	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(12A) 1D8V_S3(8.5A)

TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL531230 39	
3D3V_S0	2D5V_S0(130 mA

APL5912 39	
1D8V_S3	1D5V_S0(5A)

ISL CHARGER ISL6255 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC MAX8770 35,36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: Dallen | Rev: -1
Date: Tuesday, February 13, 2007 | Sheet 1 of 43

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

History

PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	G:CARDBUS B:1394 F:Flash Media G:SD Host	0	0

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	FingerPad
5	BlueTooth
6	CCD
7	NewCard

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

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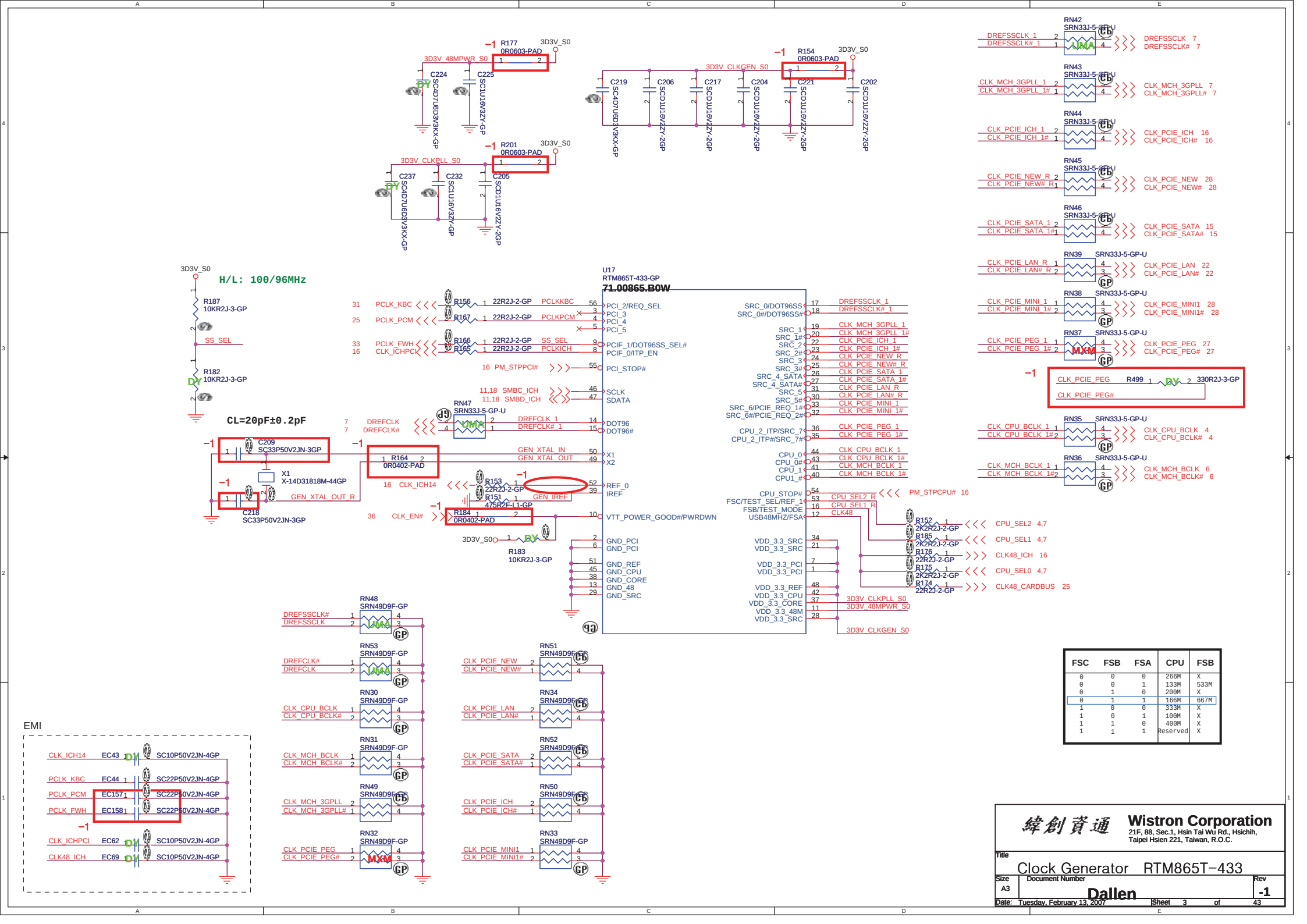
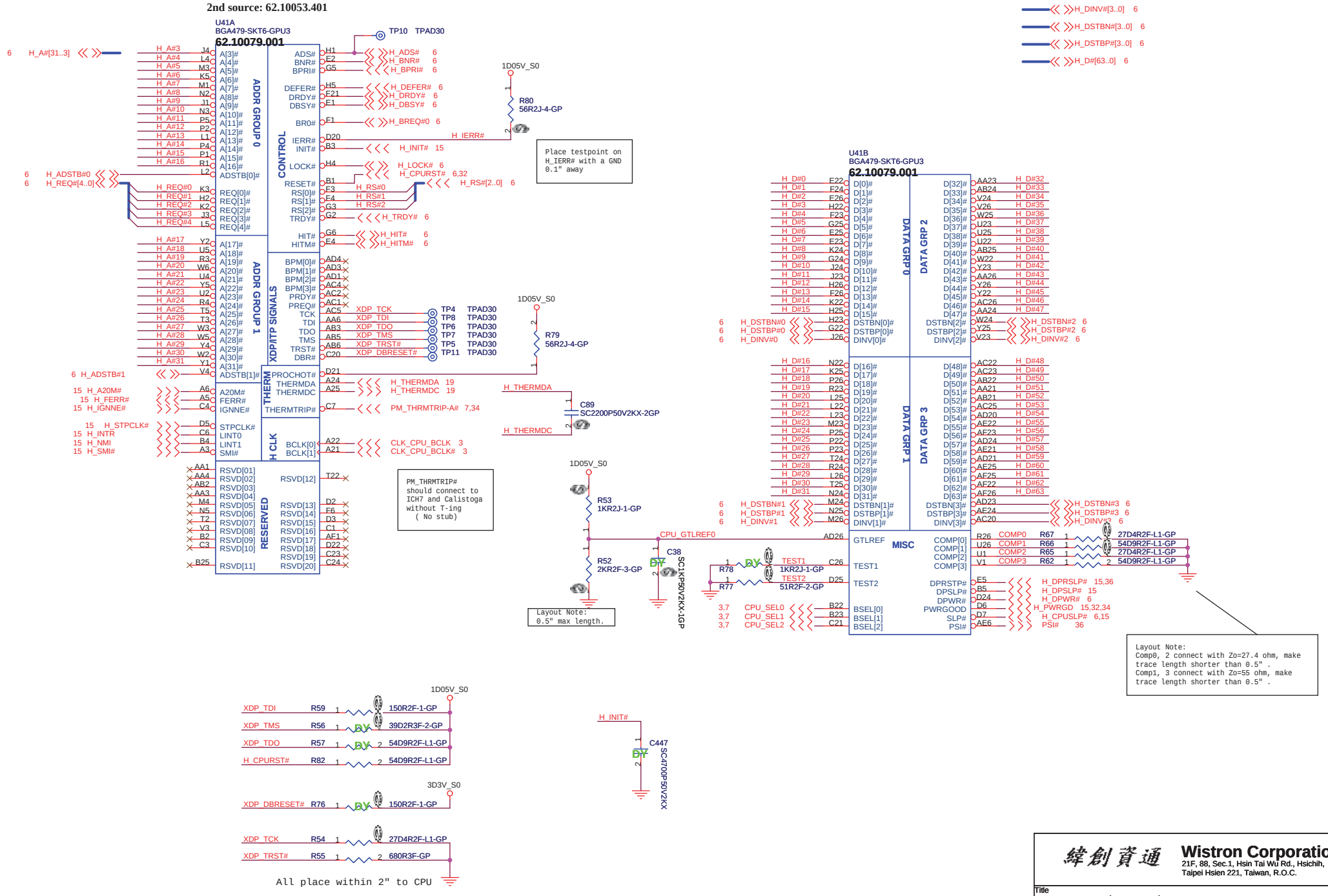
Title: Reference

Size: A3 | Document Number: Dallen | Rev: -1

Date: Tuesday, February 13, 2007 | Sheet 2 of 43


H/L: 100/96MHz
CL=20pF±0.2pF
U17
RTM865T-433-GP
71.00865.B0W
3D3V_S0
3D3V_48MPWR_S0
3D3V_CLKGEN_S0
3D3V_CLKPLL_S0
R177 0R0603-PAD
R154 0R0603-PAD
R201 0R0603-PAD
R187 10KR2J-3-GP
R182 10KR2J-3-GP
R183 10KR2J-3-GP
SS_SEL
X1 X-14D31818M-44GP
C209 SC33P50V2JN-3GP
C218 SC33P50V2JN-3GP
R164 0R0402-PAD
R184 0R0402-PAD
R153 22R2J-2-GP
R151 475R2F-L1-GP
GEN_XTAL_IN
GEN_XTAL_OUT
GEN_XTAL_OUT_R
GEN_IREF
RN47 SRN33J-5-GP-U
RN42 SRN33J-5-GP-U
RN43 SRN33J-5-GP-U
RN44 SRN33J-5-GP-U
RN45 SRN33J-5-GP-U
RN46 SRN33J-5-GP-U
RN39 SRN33J-5-GP-U
RN38 SRN33J-5-GP-U
RN37 SRN33J-5-GP-U
RN35 SRN33J-5-GP-U
RN36 SRN33J-5-GP-U
R499 330R2J-3-GP
RN48 SRN49D9F-GP
RN53 SRN49D9F-GP
RN30 SRN49D9F-GP
RN31 SRN49D9F-GP
RN49 SRN49D9F-GP
RN32 SRN49D9F-GP
RN51 SRN49D9F-GP
RN34 SRN49D9F-GP
RN52 SRN49D9F-GP
RN50 SRN49D9F-GP
RN33 SRN49D9F-GP
R152 2K2R2J-2-GP
R185 2K2R2J-2-GP
R176 22R2J-2-GP
R175 2K2R2J-2-GP
R174 22R2J-2-GP
EMI
EC43 SC10P50V2JN-4GP
EC44 SC22P50V2JN-4GP
EC157 SC22P50V2JN-4GP
EC158 SC22P50V2JN-4GP
EC62 SC10P50V2JN-4GP
EC69 SC10P50V2JN-4GP
C224 SC4D7U6D3V3KX-GP
C225 SC1U16V2ZY-GP
C237 SC4D7U6D3V3KX-GP
C232 SC1U16V2ZY-GP
C205 SCD1U16V2ZY-2GP
C219 SC4D7U6D3V3KX-GP
C206 SCD1U16V2ZY-2GP
C217 SCD1U16V2ZY-2GP
C204 SCD1U16V2ZY-2GP
C221 SCD1U16V2ZY-2GP
C202 SCD1U16V2ZY-2GP
PCLK_KBC
PCLK_PCM
PCLK_FWH
CLK_ICHPCI
PM_STPPCI#
SMBC_ICH
SMBD_ICH
DREFCLK
DREFCLK#
CLK_ICH14
CLK_EN#
PM_STPCPU#
CPU_SEL2
CPU_SEL1
CPU_SEL0
CLK48
CLK48_ICH
CLK48_CARDBUS
DREFSSCLK
DREFSSCLK#
CLK_MCH_3GPLL
CLK_MCH_3GPLL#
CLK_PCIE_ICH
CLK_PCIE_ICH#
CLK_PCIE_NEW
CLK_PCIE_NEW#
CLK_PCIE_SATA
CLK_PCIE_SATA#
CLK_PCIE_LAN
CLK_PCIE_LAN#
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
CLK_PCIE_PEG
CLK_PCIE_PEG#
CLK_CPU_BCLK
CLK_CPU_BCLK#
CLK_MCH_BCLK
CLK_MCH_BCLK#
PCI_STOP#
SCLK
SDATA
DOT96
DOT96#
REF_0
IREF
VTT_POWER_GOOD#/PWRDWN
GND_PCI
GND_REF
GND_CPU
GND_CORE
GND_48
GND_SRC
PCI_2/REQ_SEL
PCI_3
PCI_4
PCI_5
PCIF_1/DOT96SS_SEL#
PCIF_0/ITP_EN
SRC_0/DOT96SS
SRC_0#/DOT96SS#
SRC_1
SRC_1#
SRC_2
SRC_2#
SRC_3
SRC_3#
SRC_4_SATA
SRC_4_SATA#
SRC_5
SRC_5#
SRC_6/PCIE_REQ_1#
SRC_6#/PCIE_REQ_2#
CPU_2_ITP/SRC_7
CPU_2_ITP#/SRC_7#
CPU_0
CPU_0#
CPU_1
CPU_1#
CPU_STOP#
FSC/TEST_SEL/REF_1
FSB/TEST_MODE
USB48MHZ/FSA
VDD_3.3_SRC
VDD_3.3_PCI
VDD_3.3_REF
VDD_3.3_CPU
VDD_3.3_CORE
VDD_3.3_48M
VDD_3.3_SRC
FSC FSB FSA CPU FSB
0 0 0 266M X
0 0 1 133M 533M
0 1 0 200M X
0 1 1 166M 667M
1 0 0 333M X
1 0 1 100M X
1 1 0 400M X
1 1 1 Reserved X
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator RTM865T-433
Size A3
Document Number
Dallen
Rev -1
Date: Tuesday, February 13, 2007
Sheet 3 of 43

2nd source: 62.10053.401



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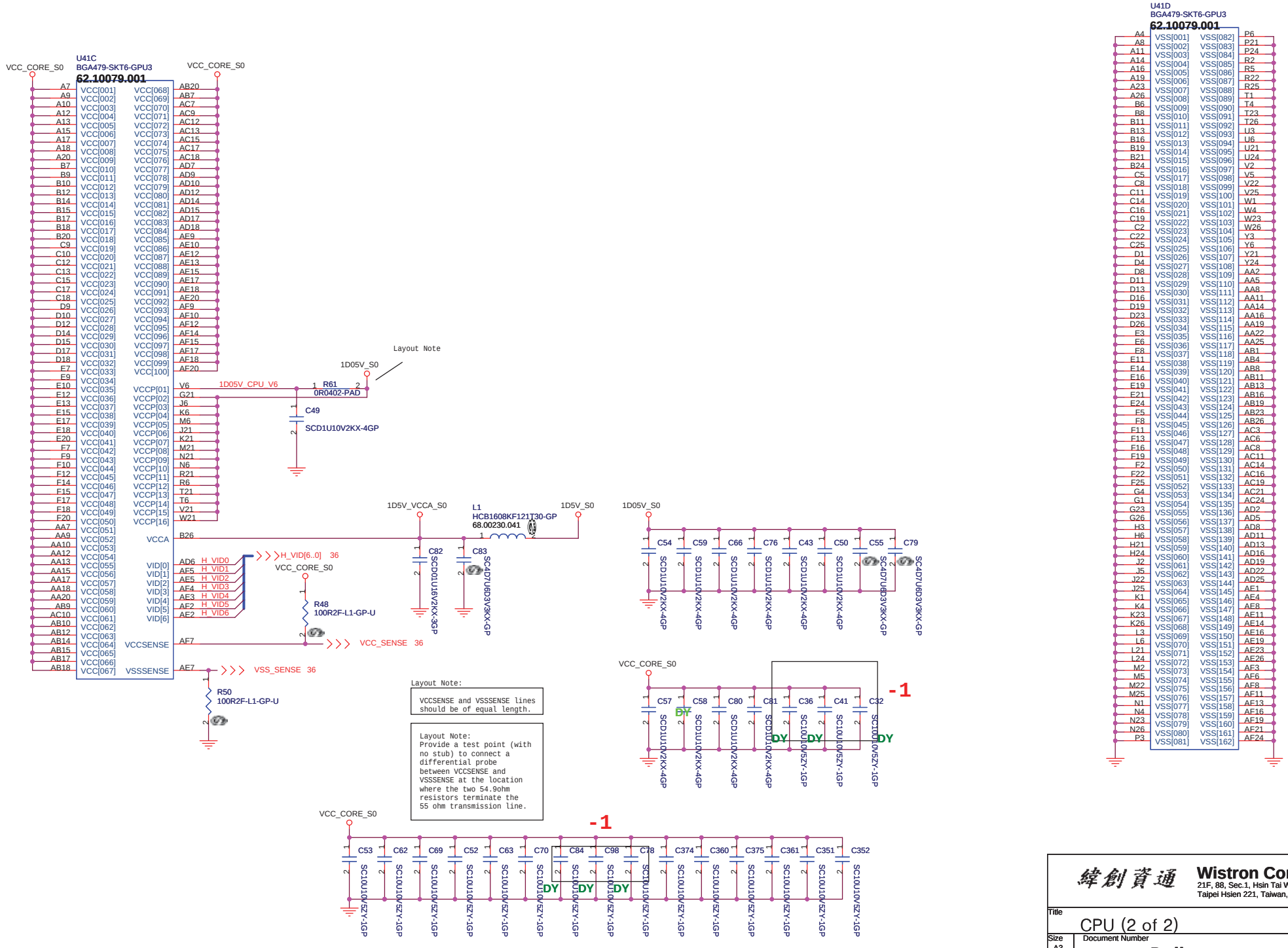
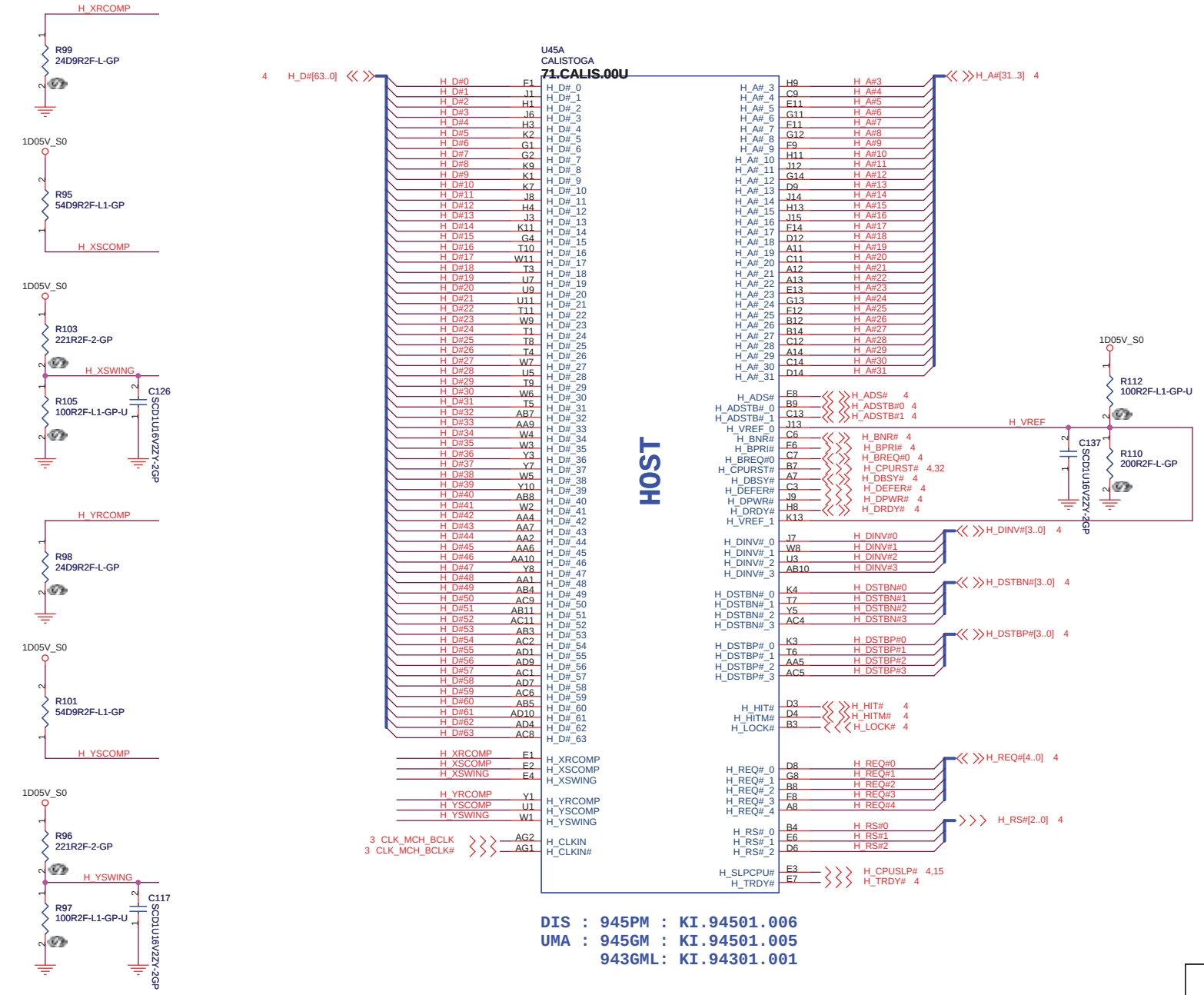
Title: CPU (1 of 2)

Size: A3 | Document Number: Dallen | Rev: -1

Date: Tuesday, February 13, 2007 | Sheet 4 of 43



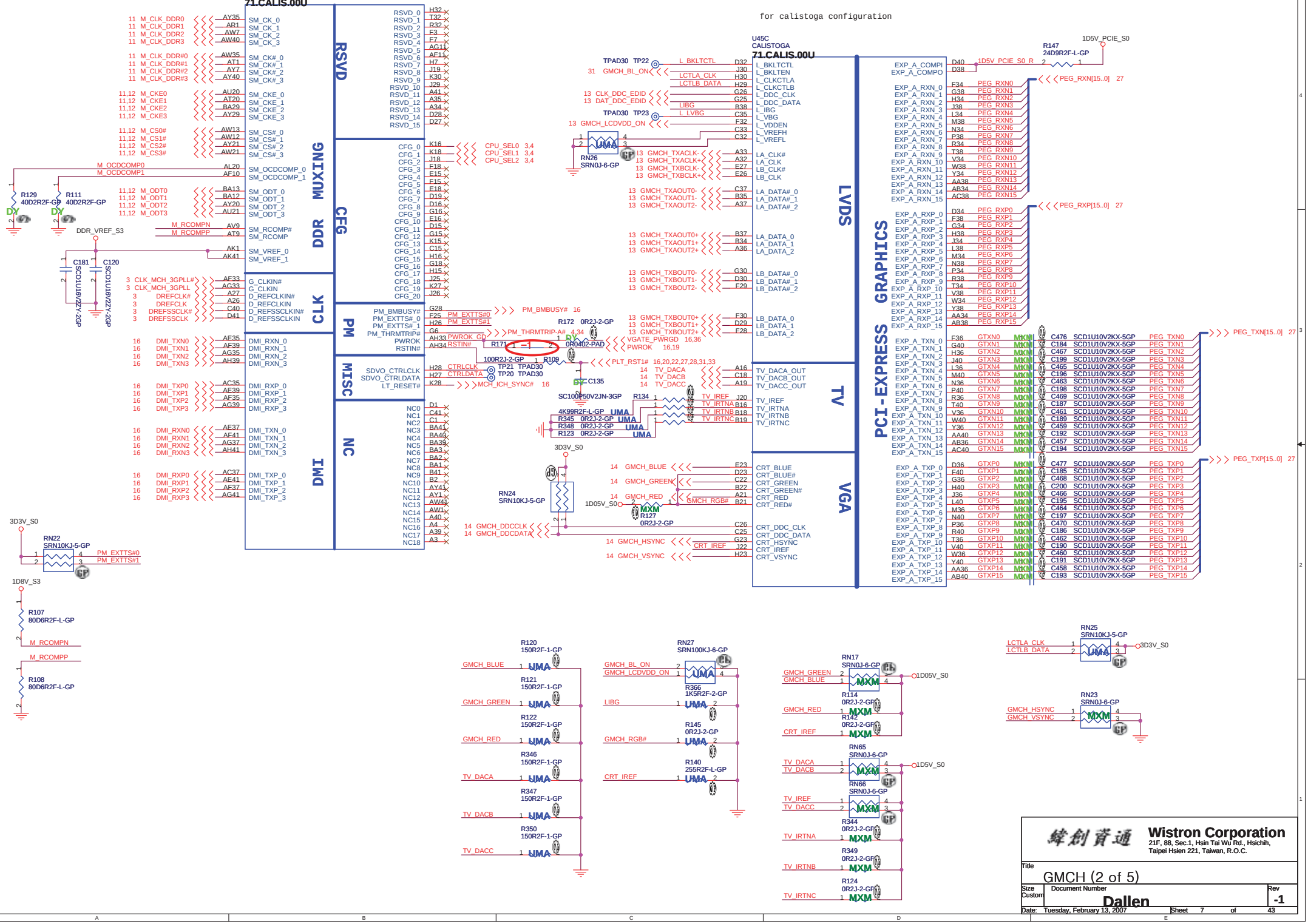
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU (2 of 2)	
Size A3	Document Number **Dallen**	Rev -1
Date: Tuesday, February 13, 2007	Sheet 5 of 43	

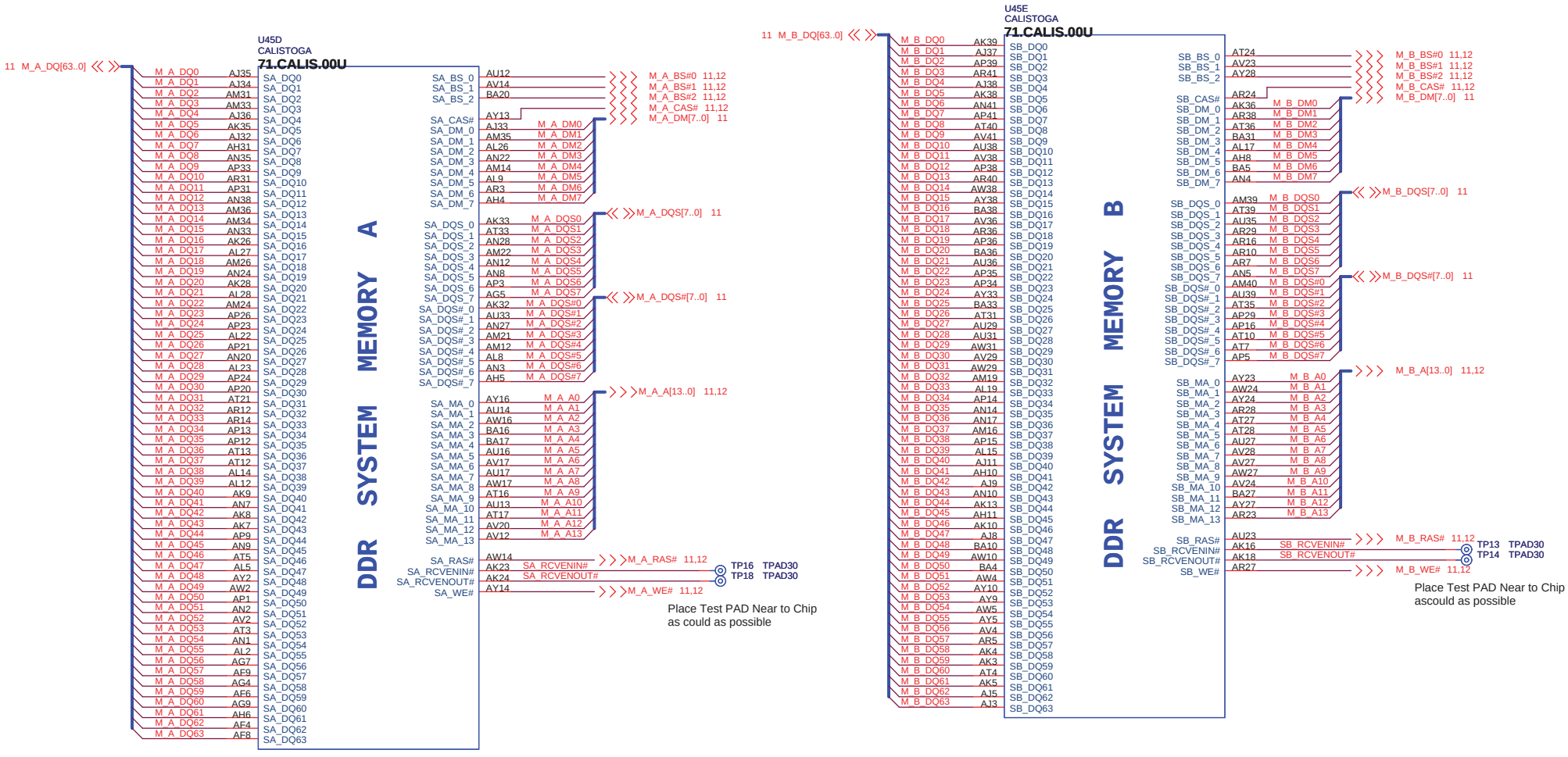


DIS : 945PM : KI.94501.006
UMA : 945GM : KI.94501.005
943GML: KI.94301.001

Place them near to the chip (< 0.5")

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: GMCH (1 of 5)		
Size: A3	Document Number: **Dallen**	Rev: -1
Date: Tuesday, February 13, 2007	Sheet 6 of 43	


for calistoga configuration
U45B
CALISTOGA
71.CALIS.00U
RSVD
CFG
DDR MUXING
CLK
PM
MISC
NC
DMI
U45C
CALISTOGA
71.CALIS.00U
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
SM_CK_0
SM_CK_1
SM_CK_2
SM_CK_3
SM_CK#_0
SM_CK#_1
SM_CK#_2
SM_CK#_3
SM_CKE_0
SM_CKE_1
SM_CKE_2
SM_CKE_3
SM_CS#_0
SM_CS#_1
SM_CS#_2
SM_CS#_3
SM_OCDCOMP_0
SM_OCDCOMP_1
SM_ODT_0
SM_ODT_1
SM_ODT_2
SM_ODT_3
SM_RCOMP#
SM_RCOMP
SM_VREF_0
SM_VREF_1
G_CLKIN#
G_CLKIN
D_REFCLKIN#
D_REFCLKIN
D_REFSSCLKIN#
D_REFSSCLKIN
DMI_RXN_0
DMI_RXN_1
DMI_RXN_2
DMI_RXN_3
DMI_RXP_0
DMI_RXP_1
DMI_RXP_2
DMI_RXP_3
DMI_TXN_0
DMI_TXN_1
DMI_TXN_2
DMI_TXN_3
DMI_TXP_0
DMI_TXP_1
DMI_TXP_2
DMI_TXP_3
RSVD_0
RSVD_1
RSVD_2
RSVD_3
RSVD_4
RSVD_5
RSVD_6
RSVD_7
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15
CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17
CFG_18
CFG_19
CFG_20
PM_BMBUSY#
PM_EXTTS#_0
PM_EXTTS#_1
PM_THRMTRIP#
PWROK
RSTIN#
SDVO_CTRLCLK
SDVO_CTRLDATA
LT_RESET#
NC0
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
NC13
NC14
NC15
NC16
NC17
NC18
L_BKLTCTL
L_BKLTEN
L_CLKCTLA
L_CLKCTLB
L_DDC_CLK
L_DDC_DATA
L_IBG
L_VBG
L_VDDEN
L_VREFH
L_VREFL
LA_CLK#
LA_CLK
LB_CLK#
LB_CLK
LA_DATA#_0
LA_DATA#_1
LA_DATA#_2
LA_DATA_0
LA_DATA_1
LA_DATA_2
LB_DATA#_0
LB_DATA#_1
LB_DATA#_2
LB_DATA_0
LB_DATA_1
LB_DATA_2
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_IREF
CRT_VSYNC
EXP_A_COMPI
EXP_A_COMPO
EXP_A_RXN_0
EXP_A_RXN_1
EXP_A_RXN_2
EXP_A_RXN_3
EXP_A_RXN_4
EXP_A_RXN_5
EXP_A_RXN_6
EXP_A_RXN_7
EXP_A_RXN_8
EXP_A_RXN_9
EXP_A_RXN_10
EXP_A_RXN_11
EXP_A_RXN_12
EXP_A_RXN_13
EXP_A_RXN_14
EXP_A_RXN_15
EXP_A_RXP_0
EXP_A_RXP_1
EXP_A_RXP_2
EXP_A_RXP_3
EXP_A_RXP_4
EXP_A_RXP_5
EXP_A_RXP_6
EXP_A_RXP_7
EXP_A_RXP_8
EXP_A_RXP_9
EXP_A_RXP_10
EXP_A_RXP_11
EXP_A_RXP_12
EXP_A_RXP_13
EXP_A_RXP_14
EXP_A_RXP_15
EXP_A_TXN_0
EXP_A_TXN_1
EXP_A_TXN_2
EXP_A_TXN_3
EXP_A_TXN_4
EXP_A_TXN_5
EXP_A_TXN_6
EXP_A_TXN_7
EXP_A_TXN_8
EXP_A_TXN_9
EXP_A_TXN_10
EXP_A_TXN_11
EXP_A_TXN_12
EXP_A_TXN_13
EXP_A_TXN_14
EXP_A_TXN_15
EXP_A_TXP_0
EXP_A_TXP_1
EXP_A_TXP_2
EXP_A_TXP_3
EXP_A_TXP_4
EXP_A_TXP_5
EXP_A_TXP_6
EXP_A_TXP_7
EXP_A_TXP_8
EXP_A_TXP_9
EXP_A_TXP_10
EXP_A_TXP_11
EXP_A_TXP_12
EXP_A_TXP_13
EXP_A_TXP_14
EXP_A_TXP_15
PEG_RXN[15..0]
PEG_RXP[15..0]
PEG_TXN[15..0]
PEG_TXP[15..0]
1D5V_PCIE_S0
1D5V_PCIE_S0_R
R147
24D9R2F-L-GP
RN26
SRN0J-6-GP
RN24
SRN10KJ-5-GP
RN22
SRN10KJ-5-GP
RN25
SRN10KJ-5-GP
RN27
SRN100KJ-6-GP
RN17
SRN0J-6-GP
RN65
SRN0J-6-GP
RN66
SRN0J-6-GP
RN23
SRN0J-6-GP
R129
40D2R2F-GP
R111
40D2R2F-GP
C181
C120
SCD1U16V2ZY-2GP
R107
80D6R2F-L-GP
R108
80D6R2F-L-GP
R171
1
R172
0R2J-2-GP
0R0402-PAD
R109
100R2J-2-GP
C135
SC100P50V2JN-3GP
R134
4K99R2F-L-GP
R345
R348
R123
0R2J-2-GP
R127
R120
150R2F-1-GP
R121
R122
R346
R347
R350
R366
1K5R2F-2-GP
R145
R140
255R2F-L-GP
R114
R142
R344
R349
R124
TPAD30 TP22
TPAD30 TP23
TP21 TPAD30
TP20 TPAD30
UMA
MXM
GP
DY
UMA
3D3V_S0
1D8V_S3
1D05V_S0
M_RCOMPN
M_RCOMPP
DDR_VREF_S3
PM_EXTTS#0
PM_EXTTS#1
CPU_SEL0 3,4
CPU_SEL1 3,4
CPU_SEL2 3,4
PM_BMBUSY# 16
PM_THRMTRIP# 4,34
PWROK 16,19
PLT_RST1# 16,20,22,27,28,31,33
CTRLCLK
CTRLDATA
MCH_ICH_SYNC# 16
GMCH_BLUE
GMCH_GREEN
GMCH_RED
GMCH_RGB#
GMCH_BL_ON
GMCH_LCDVDD_ON
GMCH_DDCCLK
GMCH_DDCDATA
GMCH_HSYNC
GMCH_VSYNC
LCTLA_CLK
LCTLB_DATA
TV_DACA
TV_DACB
TV_DACC
TV_IRTNA
TV_IRTNB
TV_IRTNC
CLK_DDC_EDID
DAT_DDC_EDID
GMCH_TXACLK-
GMCH_TXACLK+
GMCH_TXBCLK-
GMCH_TXBCLK+
GMCH_TXAOUT0-
GMCH_TXAOUT1-
GMCH_TXAOUT2-
GMCH_TXAOUT0+
GMCH_TXAOUT1+
GMCH_TXAOUT2+
GMCH_TXBOUT0-
GMCH_TXBOUT1-
GMCH_TXBOUT2-
GMCH_TXBOUT0+
GMCH_TXBOUT1+
GMCH_TXBOUT2+
VGATE_PWRGD 16,36
TV_DACA
TV_DACB
TV_DACC
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR2
M_CLK_DDR3
M_CKE0
M_CKE1
M_CKE2
M_CKE3
M_CS0#
M_CS1#
M_CS2#
M_CS3#
M_ODT0
M_ODT1
M_ODT2
M_ODT3
M_OCDCOMP0
M_OCDCOMP1
CLK_MCH_3GPLL#
CLK_MCH_3GPLL
DREFCLK#
DREFCLK
DREFSSCLK#
DREFSSCLK
DMI_RXN0
DMI_RXN1
DMI_RXN2
DMI_RXN3
DMI_TXN0
DMI_TXN1
DMI_TXN2
DMI_TXN3
DMI_RXP0
DMI_RXP1
DMI_RXP2
DMI_RXP3
DMI_TXP0
DMI_TXP1
DMI_TXP2
DMI_TXP3
PEG_RXN0
PEG_RXN1
PEG_RXN2
PEG_RXN3
PEG_RXN4
PEG_RXN5
PEG_RXN6
PEG_RXN7
PEG_RXN8
PEG_RXN9
PEG_RXN10
PEG_RXN11
PEG_RXN12
PEG_RXN13
PEG_RXN14
PEG_RXN15
PEG_RXP0
PEG_RXP1
PEG_RXP2
PEG_RXP3
PEG_RXP4
PEG_RXP5
PEG_RXP6
PEG_RXP7
PEG_RXP8
PEG_RXP9
PEG_RXP10
PEG_RXP11
PEG_RXP12
PEG_RXP13
PEG_RXP14
PEG_RXP15
PEG_TXN0
PEG_TXN1
PEG_TXN2
PEG_TXN3
PEG_TXN4
PEG_TXN5
PEG_TXN6
PEG_TXN7
PEG_TXN8
PEG_TXN9
PEG_TXN10
PEG_TXN11
PEG_TXN12
PEG_TXN13
PEG_TXN14
PEG_TXN15
PEG_TXP0
PEG_TXP1
PEG_TXP2
PEG_TXP3
PEG_TXP4
PEG_TXP5
PEG_TXP6
PEG_TXP7
PEG_TXP8
PEG_TXP9
PEG_TXP10
PEG_TXP11
PEG_TXP12
PEG_TXP13
PEG_TXP14
PEG_TXP15
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (2 of 5)
Size
Custom
Document Number
Dallen
Rev
-1
Date: Tuesday, February 13, 2007
Sheet 7 of 43

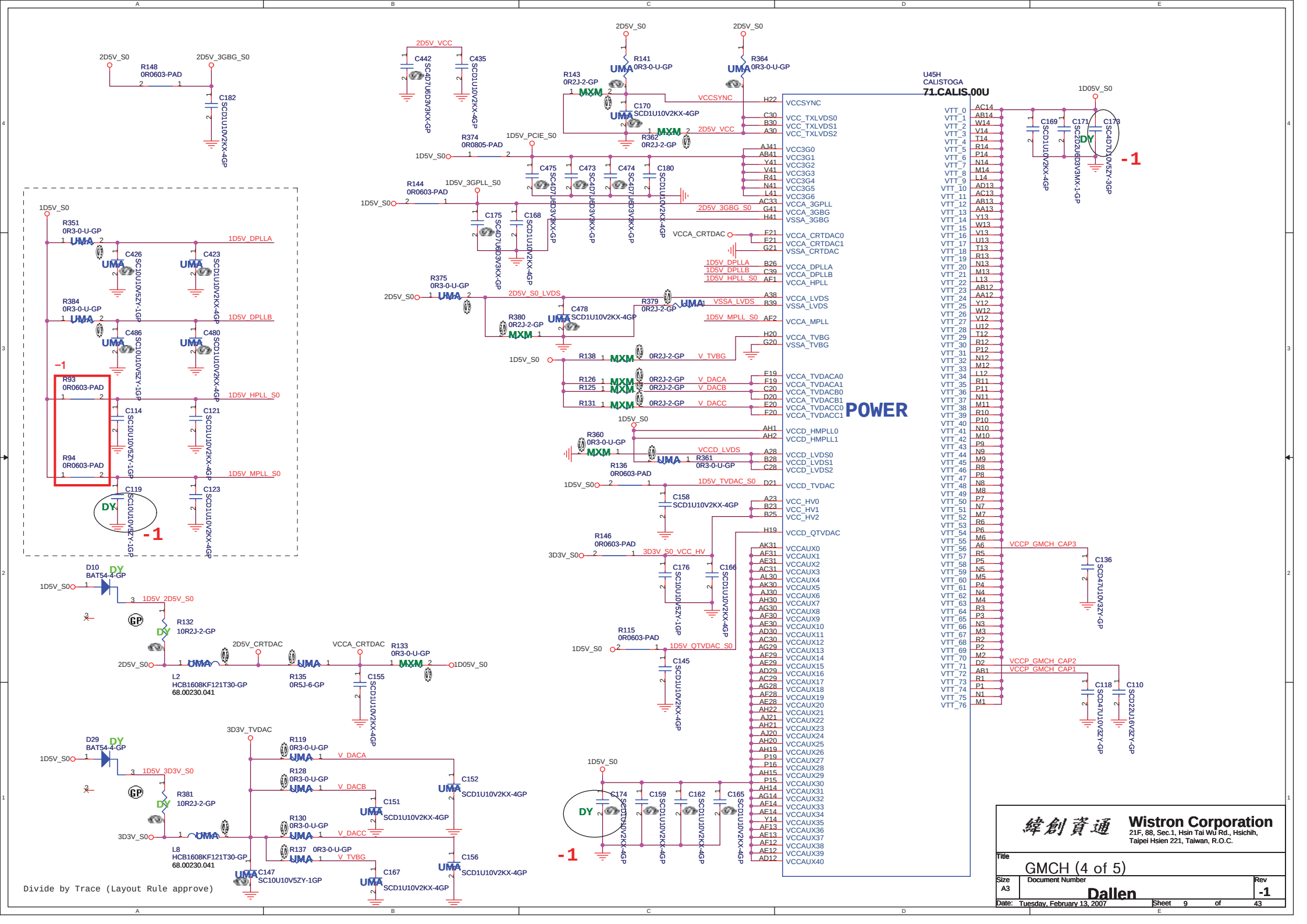


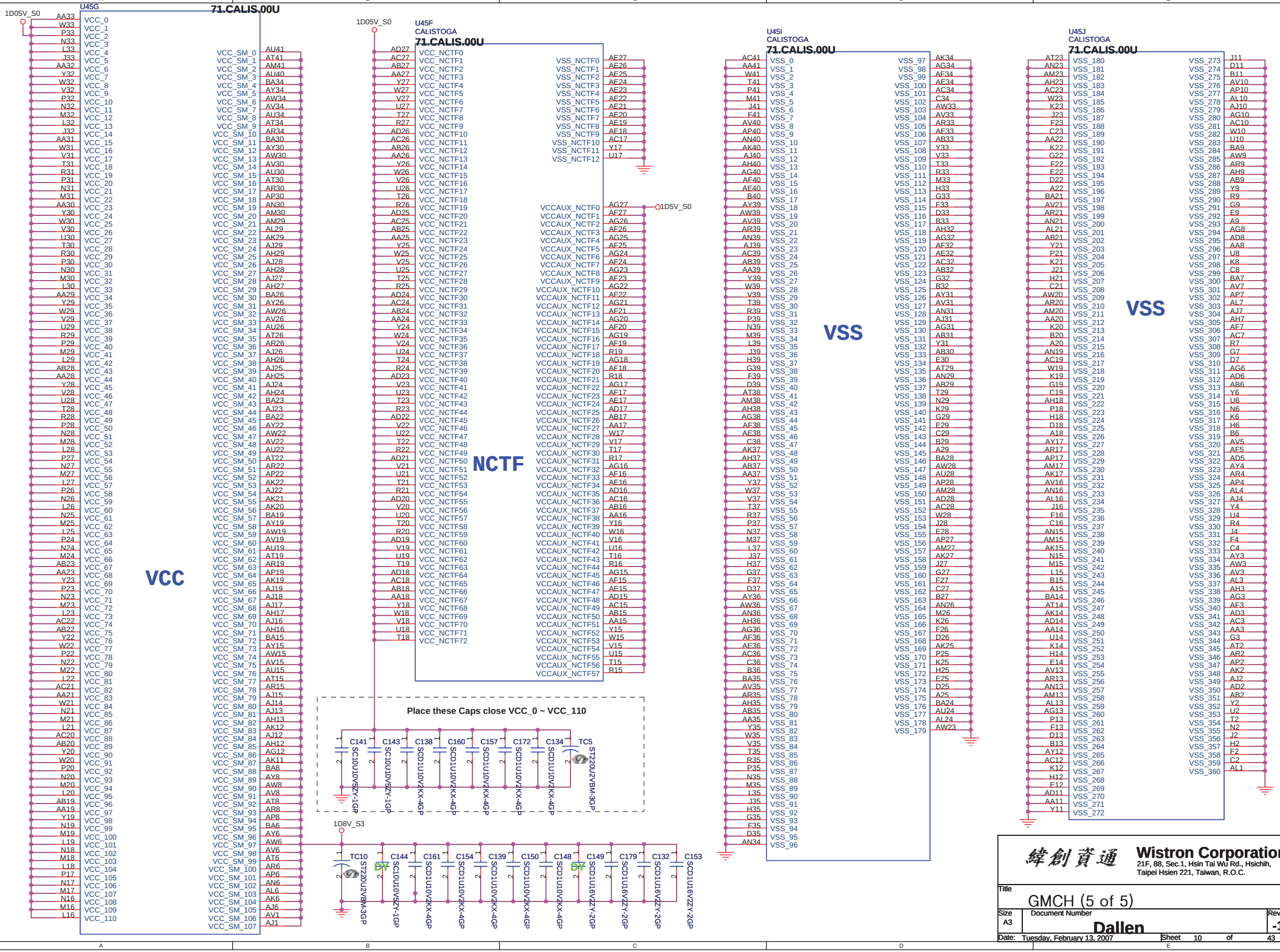
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH (3 of 5)

Size	Document Number	Rev
A3	Dallen	-1

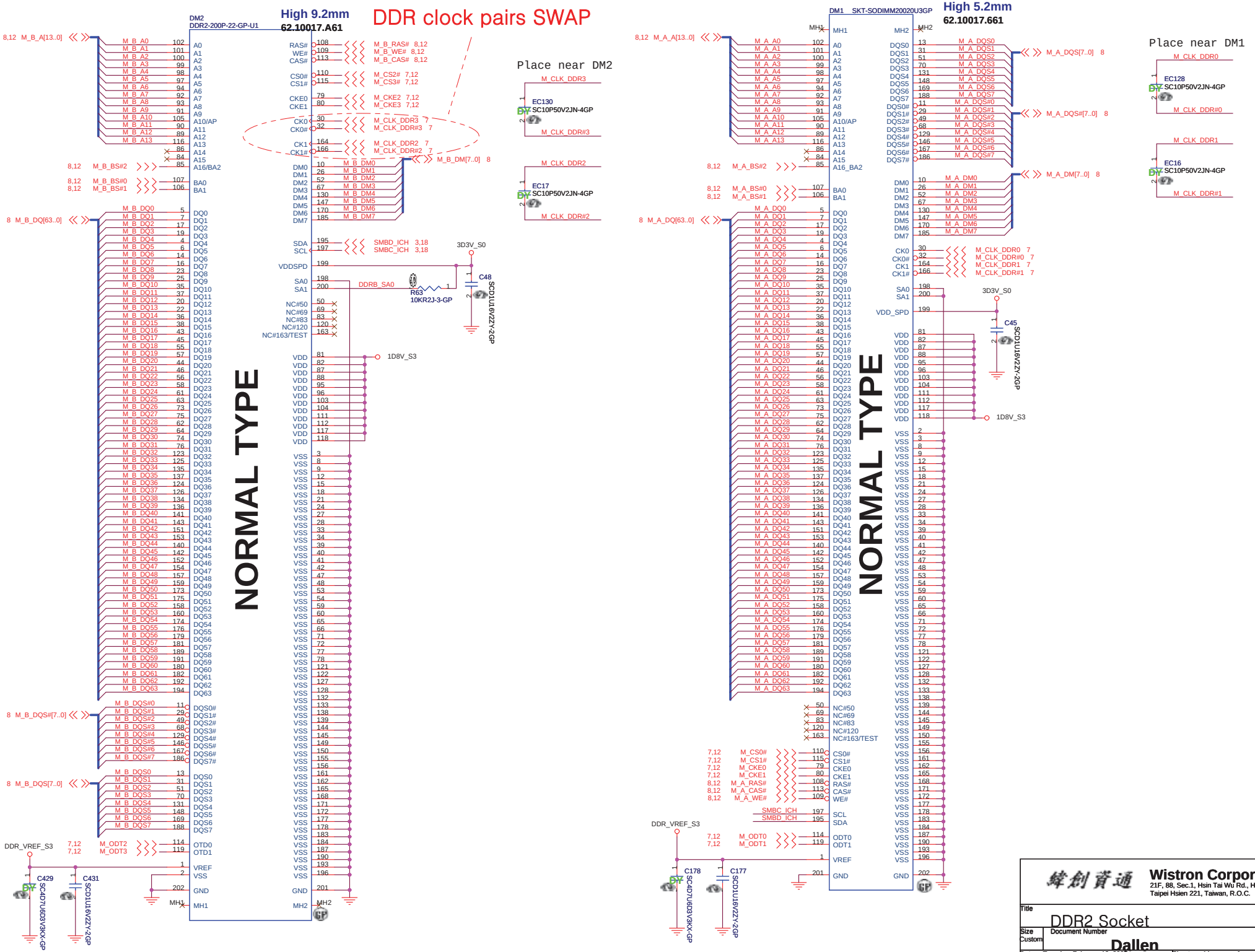
Date: Tuesday, February 13, 2007 Sheet 8 of 43


POWER
U45H
CALISTOGA
71.CALIS.00U
Divide by Trace (Layout Rule approve)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH (4 of 5)
Size
A3
Document Number
Dallen
Rev
-1
Date: Tuesday, February 13, 2007
Sheet 9 of 43

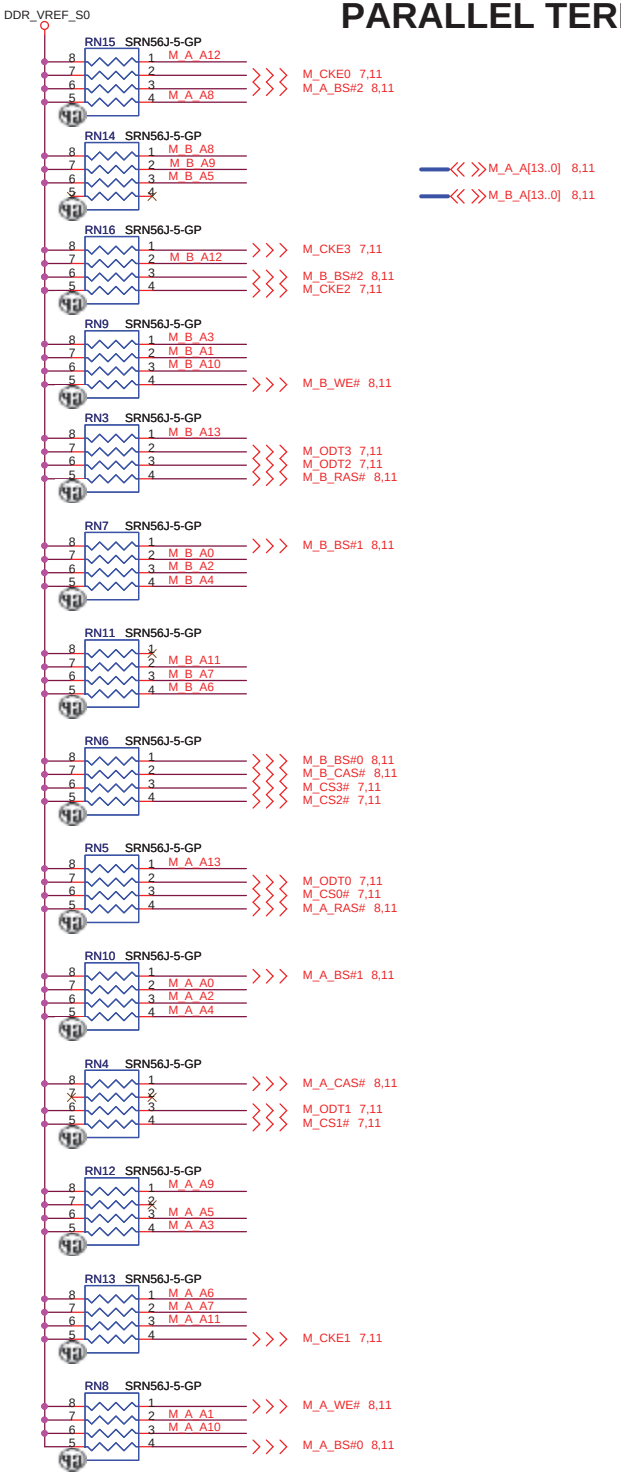


Title	GMCH (5 of 5)
Size	A3
Document Number	Dallen
Rev	-1
Date:	Tuesday, February 13, 2007
Sheet	10 of 43

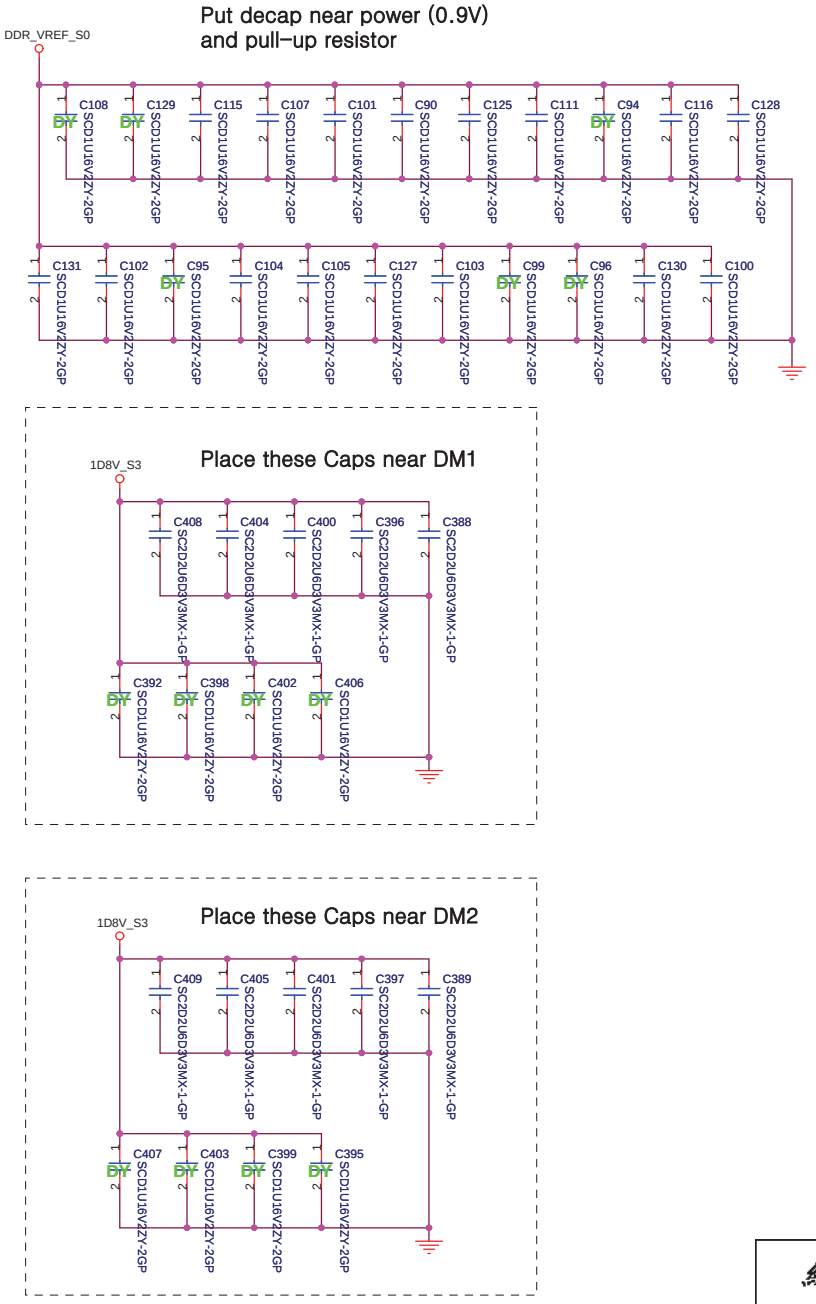
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


DM2
DDR2-200P-22-GP-U1
High 9.2mm
62.10017.A61
DDR clock pairs SWAP
NORMAL TYPE
Place near DM2
M_CLK_DDR3
EC130
SC10P50V2JN-4GP
M_CLK_DDR#3
M_CLK_DDR2
EC17
SC10P50V2JN-4GP
M_CLK_DDR#2
DDRB_SA0
R63
10KR2J-3-GP
C48
SCD1U16V2ZY-2GP
3D3V_S0
1D8V_S3
C429
SC4D7U6D3V3KX-GP
C431
SCD1U16V2ZY-2GP
DDR_VREF_S3
DM1
SKT-SODIMM20020U3GP
High 5.2mm
62.10017.661
NORMAL TYPE
Place near DM1
M_CLK_DDR0
EC128
SC10P50V2JN-4GP
M_CLK_DDR#0
M_CLK_DDR1
EC16
SC10P50V2JN-4GP
M_CLK_DDR#1
C45
SCD1U16V2ZY-2GP
C178
SC4D7U6D3V3KX-GP
C177
SCD1U16V2ZY-2GP
蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size
Custom
Document Number
Dallen
Rev
-1
Date: Tuesday, February 13, 2007
Sheet 11 of 43

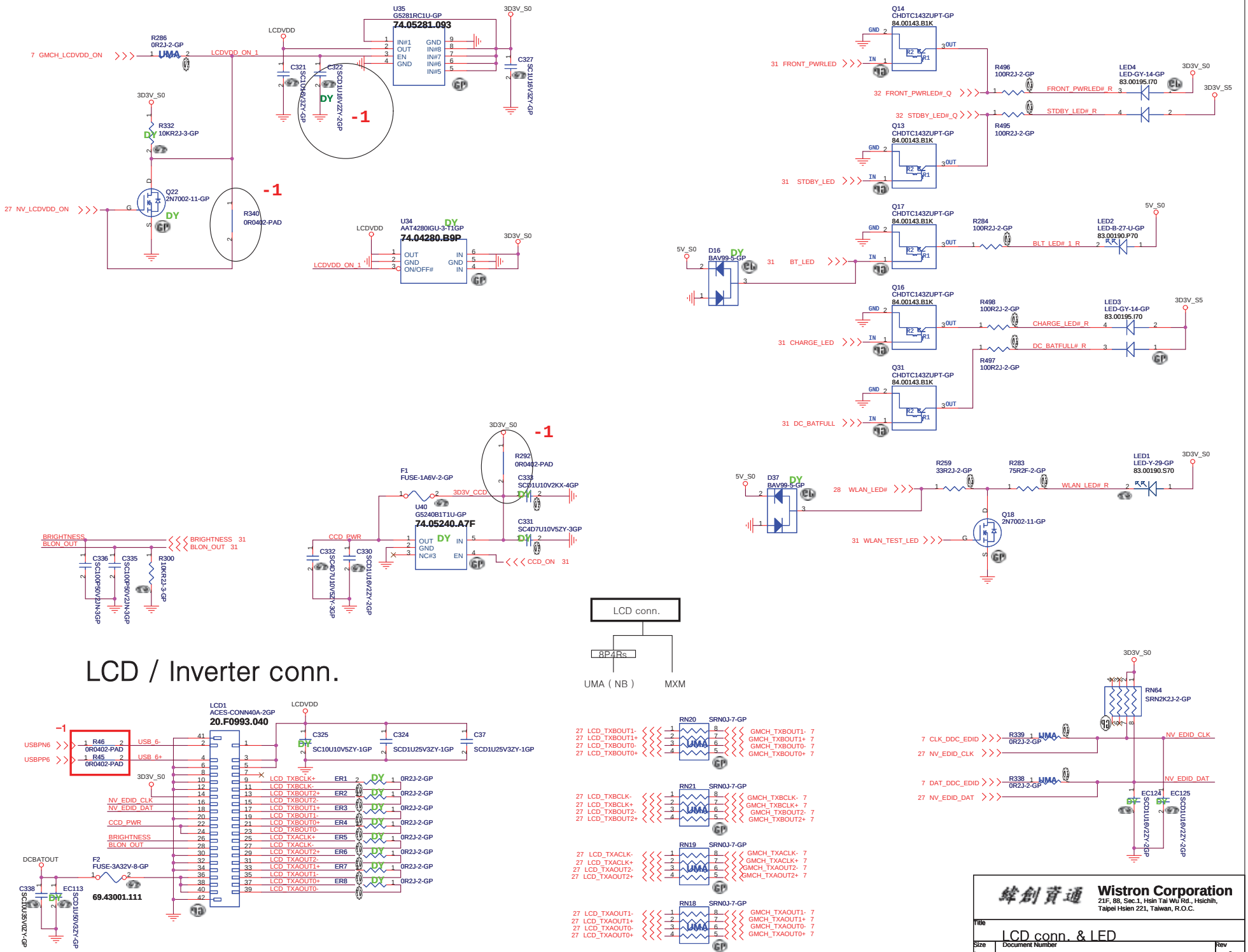
PARALLEL TERMINATION



Decoupling Capacitor



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DDR2 Termination Resistor	
Size A3	Document Number: Dallen	Rev -1
Date: Tuesday, February 13, 2007	Sheet 12 of 43	


LCD / Inverter conn.
LCD conn.
8P4Rs
UMA (NB)
MXM
U35
G5281RC1U-GP
74.05281.093
U34
AAT4280IGU-3-T1GP
74.04280.B9P
U40
G5240B1T1U-GP
74.05240.A7F
LCD1
ACES-CONN40A-2GP
20.F0993.040
F1
FUSE-1A6V-2-GP
F2
FUSE-3A32V-8-GP
69.43001.111
Q14
CHDTC143ZUPT-GP
84.00143.B1K
Q13
CHDTC143ZUPT-GP
84.00143.B1K
Q17
CHDTC143ZUPT-GP
84.00143.B1K
Q16
CHDTC143ZUPT-GP
84.00143.B1K
Q31
CHDTC143ZUPT-GP
84.00143.B1K
Q22
2N7002-11-GP
Q18
2N7002-11-GP
D16
BAV99-5-GP
D37
BAV99-5-GP
LED4
LED-GY-14-GP
83.00195.I70
LED2
LED-B-27-U-GP
83.00190.P70
LED3
LED-GY-14-GP
83.00195.I70
LED1
LED-Y-29-GP
83.00190.S70
RN20
RN21
RN19
RN18
SRN0J-7-GP
RN64
SRN2K2J-2-GP
-1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LCD conn. & LED
Size
Custom
Document Number
Dallen
Rev
-1
Date: Tuesday, February 13, 2007
Sheet 13 of 43

CRT I/F & connector

Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

27 NV_RED
7 GMCH_RED
27 NV_GREEN
7 GMCH_GREEN
27 NV_BLUE
7 GMCH_BLUE
R118 UMA 0R2J-2-GP
R117 UMA 0R2J-2-GP
R116 UMA 0R2J-2-GP
L7 FCB1608CF-GP
L6 FCB1608CF-GP
L5 FCB1608CF-GP
CRT_R
CRT_G
CRT_B
R329 150R2F-1-GP
R326 150R2F-1-GP
R324 150R2F-1-GP
C387 MXM SC22P50V2JN-4GP
C382 MXM SC22P50V2JN-4GP
C378 MXM SC22P50V2JN-4GP
C391 SC68DP50V2DN-GP
C383 SC68DP50V2DN-GP
C381 SC68DP50V2DN-GP

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT1
VIDEO-15-21-U4-GP
20.20334.015
MH1
MH2
CRT_R
CRT_G
CRT_B
DAT_DDC1_5
CRT_VSYNC1
CRT_HSYNC1
5V_CRT_S0
CLK_DDC1_5
C386 SC100P50V2JN-3GP
C376 SC18P50V2JN-1-GP
C385 SC100P50V2JN-3GP
C390 SCD1U16V2KX-3GP
C377 SC18P50V2JN-1-GP
R322 470R2J-2-GP
31 CRT_DEC#
CRT_DEC_R
C372 SC100P50V2JN-3GP
D3 BAV99-5-GP
5V_S0

Hsync & Vsync level shift

5V_S0
C106 SCD1U16V2ZY-2GP
7 GMCH_HSYNC
27 NV_HSYNC
7 GMCH_VSYNC
27 NV_VSYNC
R354 UMA 0R2J-2-GP
R355 UMA 0R2J-2-GP
U42A TSAHCT125PW-GP
U42B TSAHCT125PW-GP
CRT_HSYNC1_R
CRT_VSYNC1_R
R325 0R0402-PAD
R323 0R0402-PAD
CRT_HSYNC1
CRT_VSYNC1
C384 SC18P50V2JN-1-GP
C380 SC18P50V2JN-1-GP

DDC_CLK & DATA level shift

3D3V_S0
5V_CRT_S0
5V_S0
D22 CH751H-40PT
RN62 SRN2K2J-2-GP
RN61 SRN10KJ-6-GP
Q19 2N7002DW-1-GP
27 NV_DDCDAT
7 GMCH_DDCDATA
27 NV_DDCCLK
7 GMCH_DDCCLK
R357 UMA 0R2J-2-GP
R356 UMA 0R2J-2-GP
NV_DDCDAT
NV_DDCCLK
CRT_DEC#
DAT_DDC1_5
CLK_DDC1_5

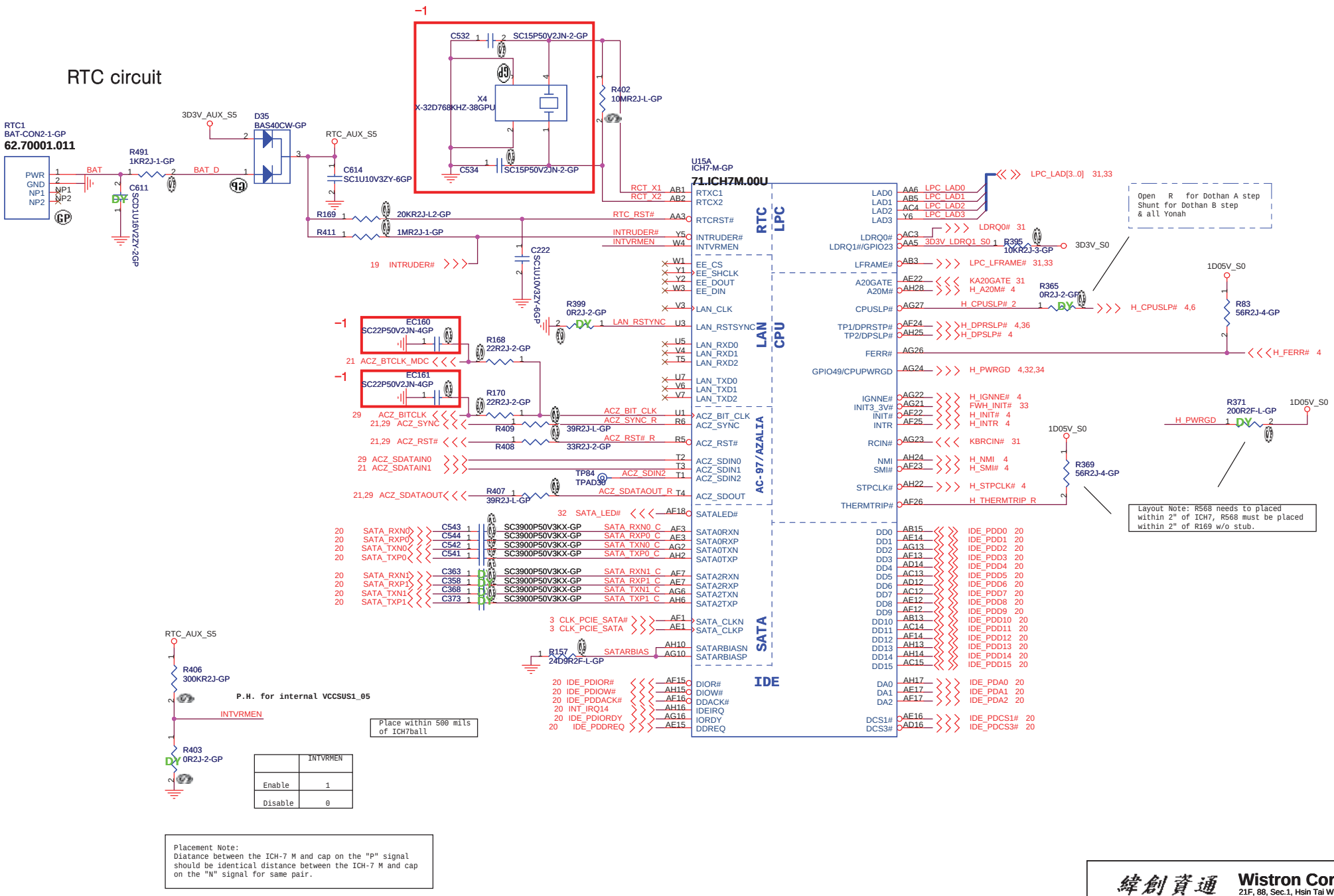
TV conn.

TVOUT1
MINDIN7-22-GP
22.10021.I81
27 NV_TV_LUMA
7 TV_DACB
27 NV_TV_CRMA
7 TV_DACC
27 NV_TV_COMP
7 TV_DACA
R336 0R2J-2-GP
R335 0R2J-2-GP
R337 0R2J-2-GP
R389 150R2F-1-GP
R386 150R2F-1-GP
R393 150R2F-1-GP
C508 SC33P50V2JN-3GP
C495 SC33P50V2JN-3GP
C518 SC33P50V2JN-3GP
L12 IND-1D2UH-5-GP
L11 IND-1D2UH-5-GP
L13 IND-1D2UH-5-GP
C512 SC150P50V2JN-3GP
C494 SC150P50V2JN-3GP
C523 SC150P50V2JN-3GP
C509 SC270P50V2JN-2GP
C496 SC270P50V2JN-2GP
C519 SC270P50V2JN-2GP
LUMA_1
CRMA_1
COMP_1

D12 BAV99-5-GP
D11 BAV99-5-GP
D14 BAV99-5-GP
D7 BAV99-5-GP
D5 BAV99-5-GP
D4 BAV99-5-GP
5V_S0

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV Connector
Size: A3
Document Number: Dallen
Rev: -1
Date: Tuesday, February 13, 2007
Sheet 14 of 43

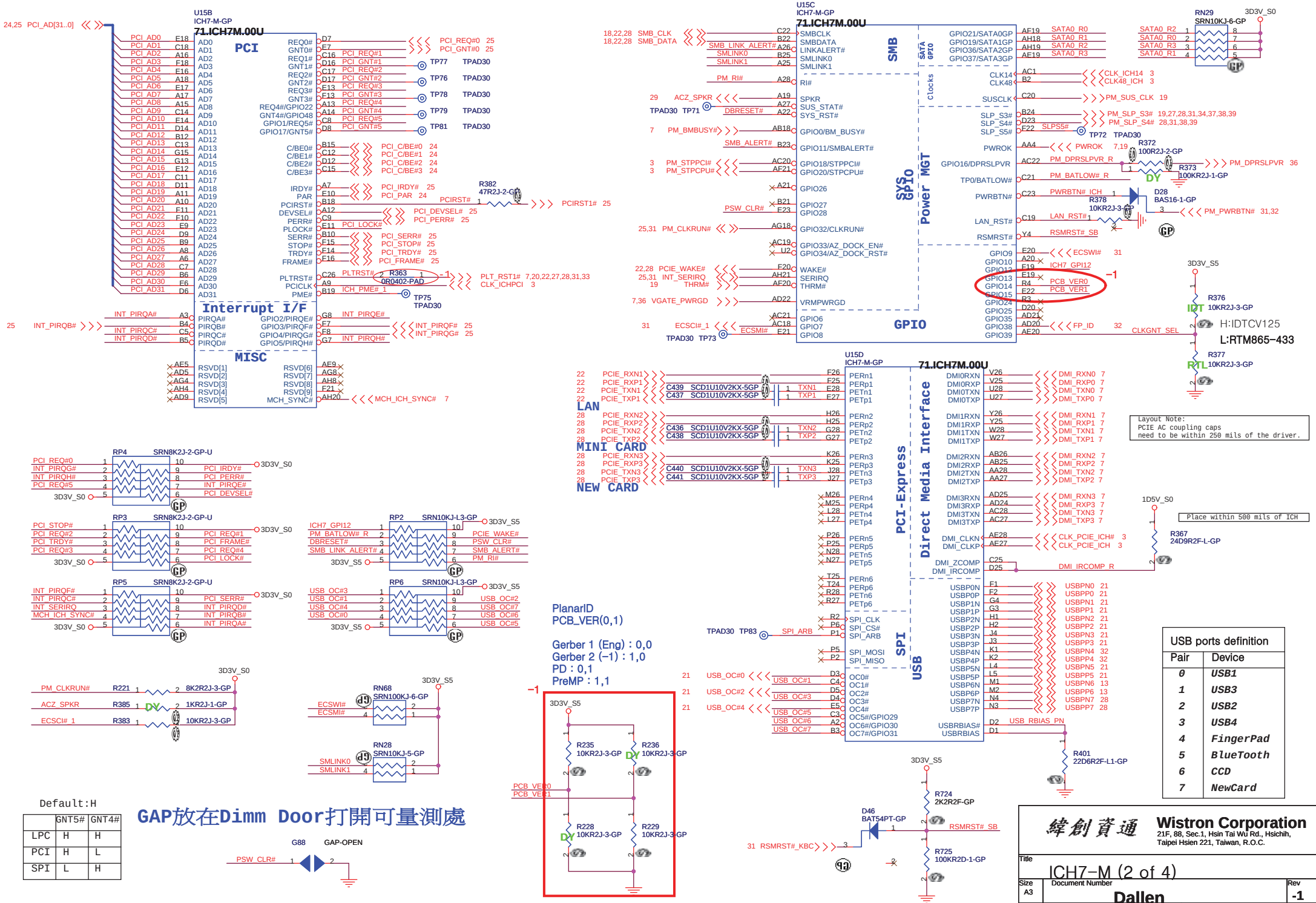


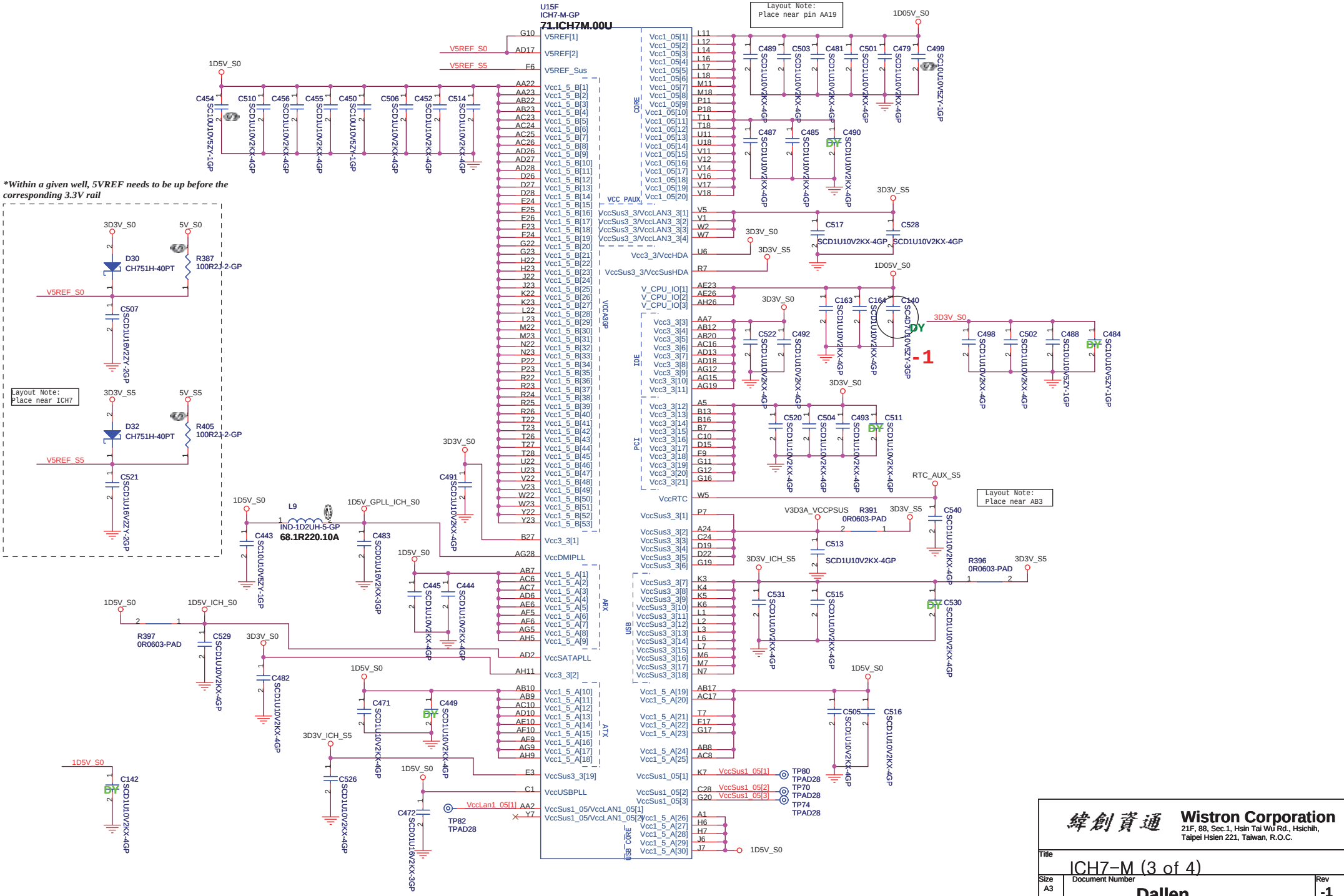
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH7-M (1 of 4)

Size	Document Number	Rev
A3	Dallen	-1

Date: Tuesday, February 13, 2007 Sheet 15 of 43

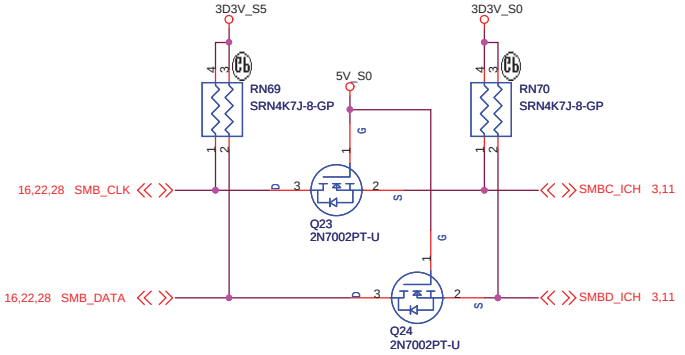

U15B
ICH7-M-GP
71.ICH7M.00U
PCI
Interrupt I/F
MISC
U15C
SMB
SYS GPIO
Power MGT
GPIO
U15D
PCI-Express
Direct Media Interface
SPI
USB
LAN
MINI CARD
NEW CARD
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Place within 500 mils of ICH
USB ports definition
Pair | Device
0 USB1
1 USB3
2 USB2
3 USB4
4 FingerPad
5 BlueTooth
6 CCD
7 NewCard
PlanarID
PCB_VER(0,1)
Gerber 1 (Eng) : 0,0
Gerber 2 (–1) : 1,0
PD : 0,1
PreMP : 1,1
Default:H
GNT5# GNT4#
LPC H H
PCI H L
SPI L H
GAP放在Dimm Door打開可量測處
G88 GAP-OPEN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
Size A3
Document Number
Dallen
Rev -1
Date: Tuesday, February 13, 2007
Sheet 16 of 43


U15F
ICH7-M-GP
71.ICH7M.00U
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH7
Layout Note: Place near AB3
1D05V_S0
3D3V_S0
3D3V_S5
5V_S0
5V_S5
V5REF_S0
V5REF_S5
D30 CH751H-40PT
D32 CH751H-40PT
R387 100R2J-2-GP
R405 100R2J-2-GP
C507 SCD1U16V2ZY-2GP
C521 SCD1U16V2ZY-2GP
L9 IND-1D2UH-5-GP
68.1R220.10A
1D5V_GPLL_ICH_S0
1D5V_ICH_S0
3D3V_ICH_S5
RTC_AUX_S5
V3D3A_VCCPSUS
R391 0R0603-PAD
R396 0R0603-PAD
R397 0R0603-PAD
TP80 TPAD28
TP70 TPAD28
TP74 TPAD28
TP82 TPAD28
-1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size A3
Document Number
Dallen
Rev -1
Date: Tuesday, February 13, 2007
Sheet 17 of 43

U15E
ICH7-M-GP
71.ICH7M.00U

A4	VSS[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
B11	VSS[5]	VSS[102]	R13
B14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B26	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T15
D18	VSS[16]	VSS[113]	T16
D21	VSS[17]	VSS[114]	T17
D24	VSS[18]	VSS[115]	U4
E1	VSS[19]	VSS[116]	U12
E2	VSS[20]	VSS[117]	U13
E4	VSS[21]	VSS[118]	U14
E8	VSS[22]	VSS[119]	U15
E15	VSS[23]	VSS[120]	U16
F3	VSS[24]	VSS[121]	U17
F4	VSS[25]	VSS[122]	U24
F5	VSS[26]	VSS[123]	U25
F12	VSS[27]	VSS[124]	U26
F27	VSS[28]	VSS[125]	V2
F28	VSS[29]	VSS[126]	V13
G1	VSS[30]	VSS[127]	V15
G2	VSS[31]	VSS[128]	V24
G5	VSS[32]	VSS[129]	V27
G6	VSS[33]	VSS[130]	V28
G9	VSS[34]	VSS[131]	W6
G14	VSS[35]	VSS[132]	W24
G18	VSS[36]	VSS[133]	W25
G21	VSS[37]	VSS[134]	W26
G24	VSS[38]	VSS[135]	Y3
G25	VSS[39]	VSS[136]	Y24
G26	VSS[40]	VSS[137]	Y27
H3	VSS[41]	VSS[138]	Y28
H4	VSS[42]	VSS[139]	AA1
H5	VSS[43]	VSS[140]	AA24
H24	VSS[44]	VSS[141]	AA25
H27	VSS[45]	VSS[142]	AA26
H28	VSS[46]	VSS[143]	AB4
J1	VSS[47]	VSS[144]	AB6
J2	VSS[48]	VSS[145]	AB11
J5	VSS[49]	VSS[146]	AB14
J24	VSS[50]	VSS[147]	AB16
J25	VSS[51]	VSS[148]	AB19
J26	VSS[52]	VSS[149]	AB21
K24	VSS[53]	VSS[150]	AB24
K27	VSS[54]	VSS[151]	AB27
K28	VSS[55]	VSS[152]	AB28
L13	VSS[56]	VSS[153]	AC2
L15	VSS[57]	VSS[154]	AC5
L24	VSS[58]	VSS[155]	AC9
L25	VSS[59]	VSS[156]	AC11
L26	VSS[60]	VSS[157]	AD1
M3	VSS[61]	VSS[158]	AD3
M4	VSS[62]	VSS[159]	AD4
M5	VSS[63]	VSS[160]	AD7
M12	VSS[64]	VSS[161]	AD8
M13	VSS[65]	VSS[162]	AD11
M14	VSS[66]	VSS[163]	AD15
M15	VSS[67]	VSS[164]	AD19
M16	VSS[68]	VSS[165]	AD23
M17	VSS[69]	VSS[166]	AE2
M24	VSS[70]	VSS[167]	AE4
M27	VSS[71]	VSS[168]	AE8
M28	VSS[72]	VSS[169]	AE11
N1	VSS[73]	VSS[170]	AE13
N2	VSS[74]	VSS[171]	AE18
N5	VSS[75]	VSS[172]	AE21
N6	VSS[76]	VSS[173]	AE24
N11	VSS[77]	VSS[174]	AE25
N12	VSS[78]	VSS[175]	AF2
N13	VSS[79]	VSS[176]	AF4
N14	VSS[80]	VSS[177]	AF8
N15	VSS[81]	VSS[178]	AF11
N16	VSS[82]	VSS[179]	AF27
N17	VSS[83]	VSS[180]	AF28
N18	VSS[84]	VSS[181]	AG1
N24	VSS[85]	VSS[182]	AG3
N25	VSS[86]	VSS[183]	AG7
N26	VSS[87]	VSS[184]	AG11
P3	VSS[88]	VSS[185]	AG14
P4	VSS[89]	VSS[186]	AG17
P12	VSS[90]	VSS[187]	AG20
P13	VSS[91]	VSS[188]	AG25
P14	VSS[92]	VSS[189]	AH1
P15	VSS[93]	VSS[190]	AH3
P16	VSS[94]	VSS[191]	AH7
P17	VSS[95]	VSS[192]	AH12
P24	VSS[96]	VSS[193]	AH23
P27	VSS[97]	VSS[194]	AH27

SMBUS



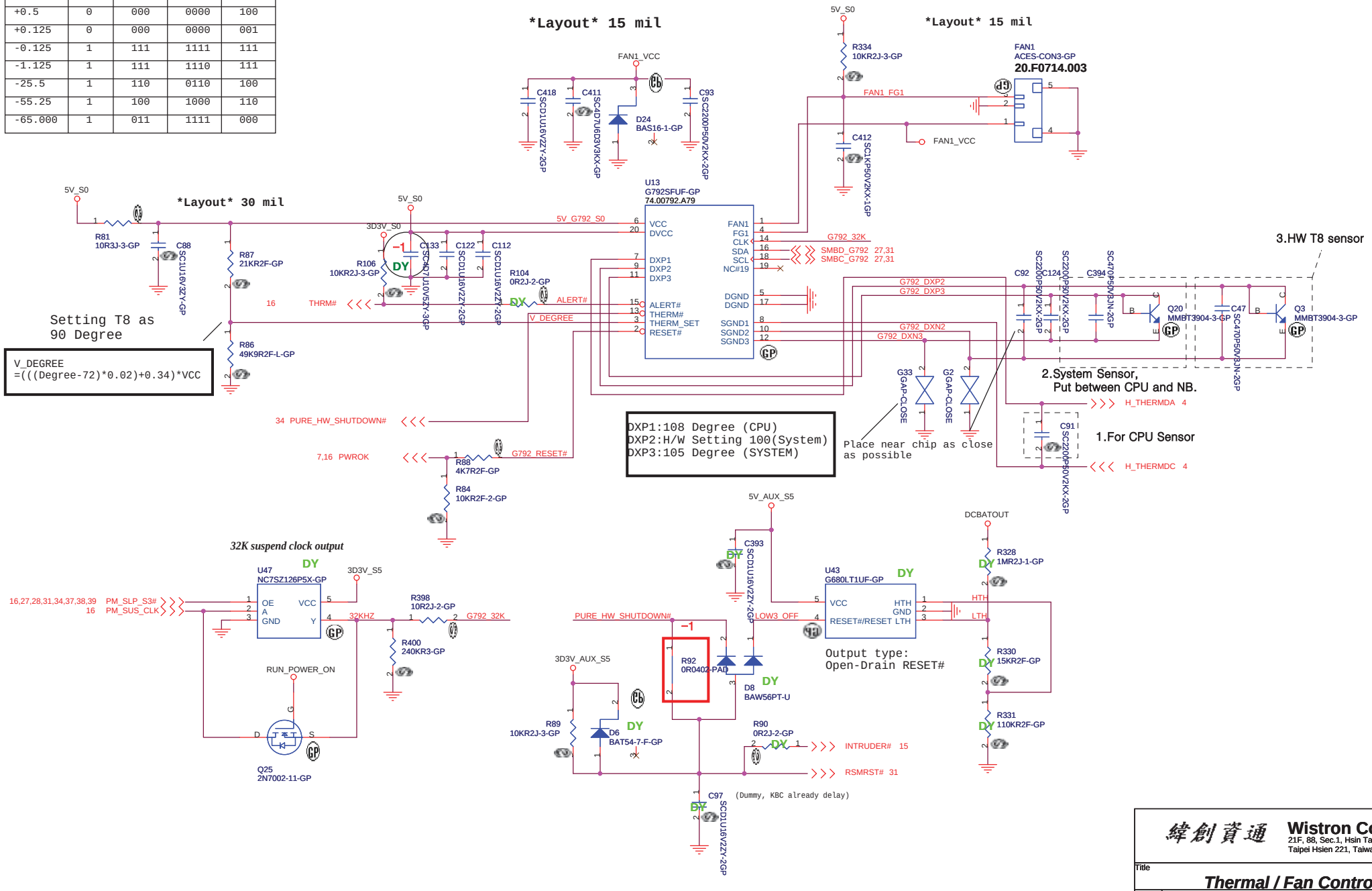
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ICH7-M (4 of 4)*

Size	Document Number	Rev
A3	Dallen	-1

Date: Tuesday, February 13, 2007 Sheet 18 of 43

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000



緯創資通 Wistron Corporation
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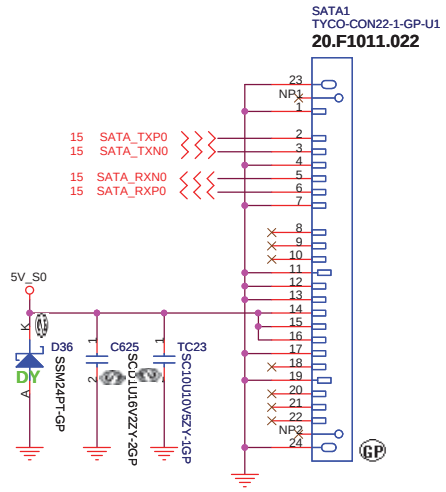
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal / Fan Controllor**

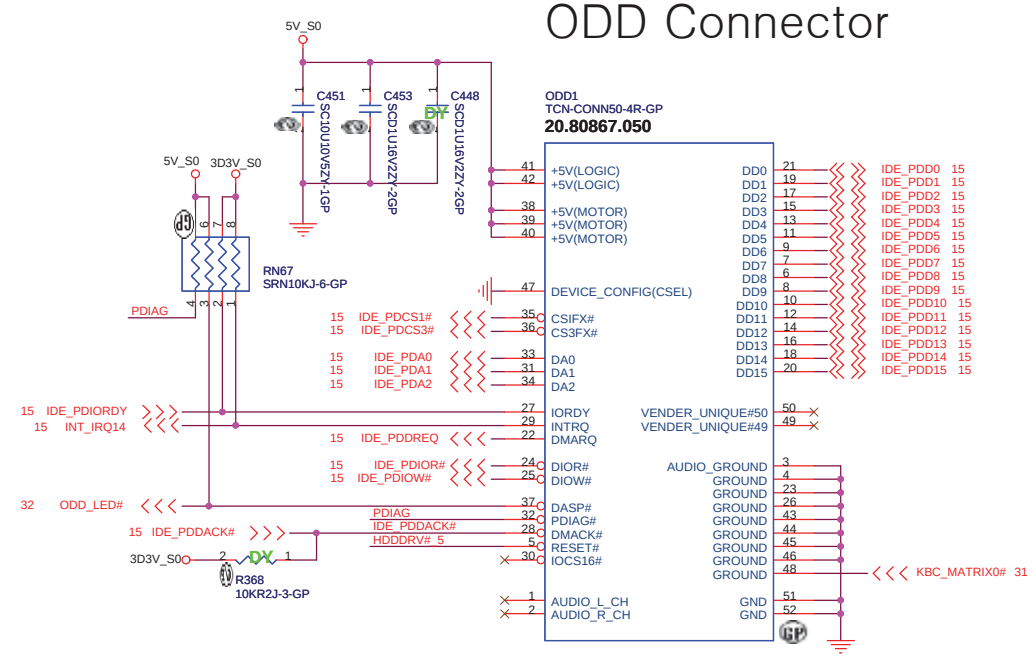
Size: A3 | Document Number: Dallen | Rev: -1

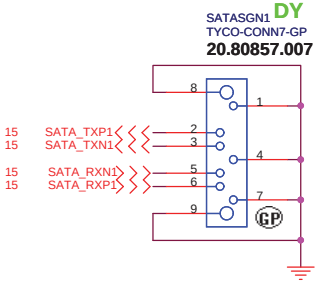
Date: Tuesday, February 13, 2007 | Sheet 19 of 43

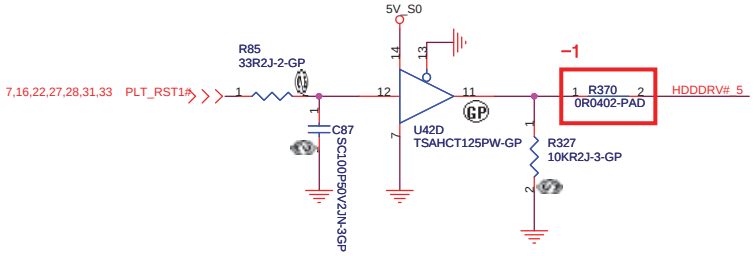
SATA HD Connector

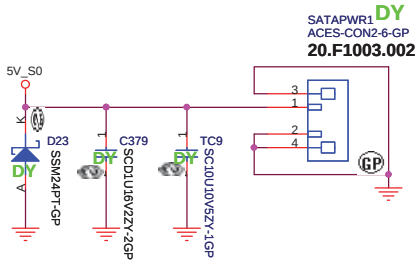


ODD Connector









緯創資通 **Wistron Corporation**
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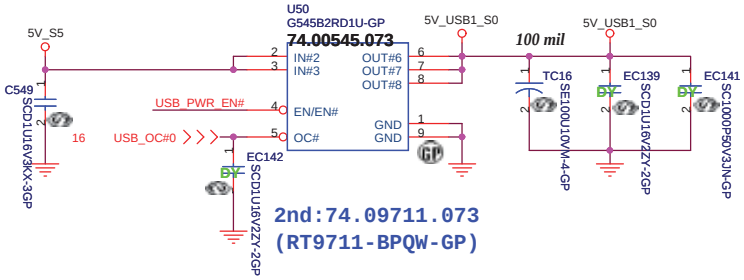
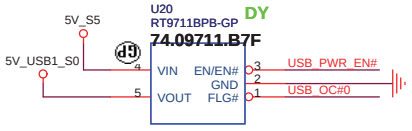
Taipei Hsien 221, Taiwan, R.O.C.

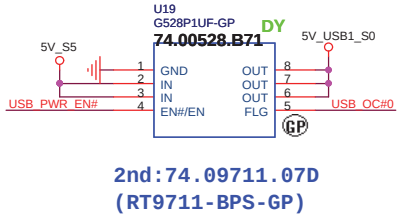
Title: ***HDD and CDROM***

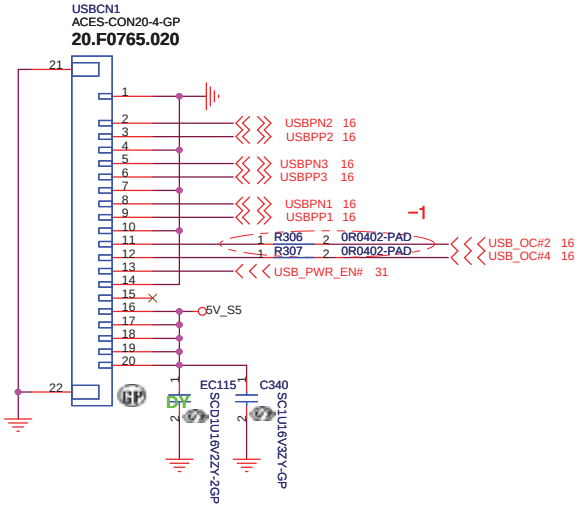
Size	Document Number	Rev
A3	Dallen	-1

Date: Tuesday, February 13, 2007 Sheet 20 of 43

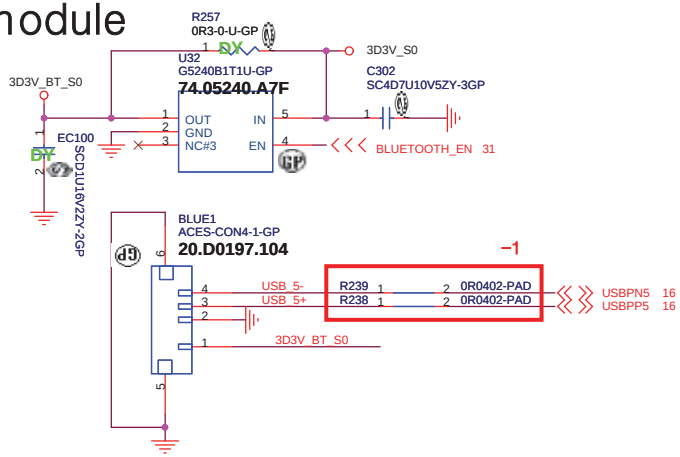


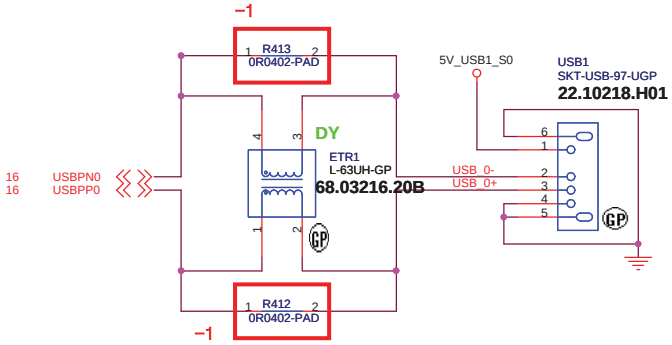




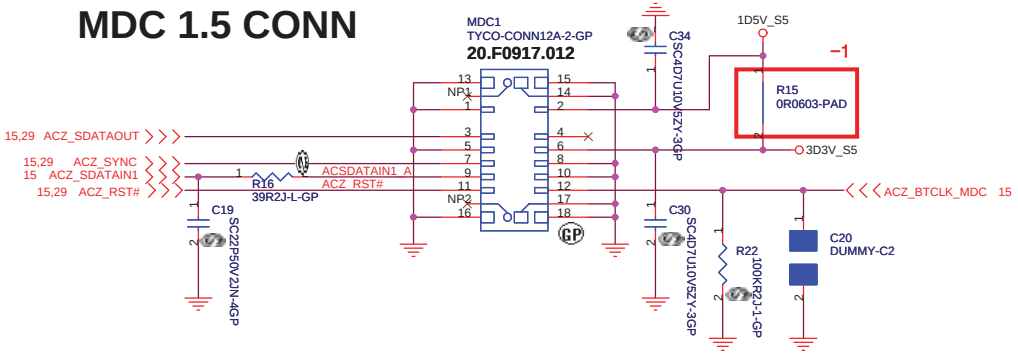


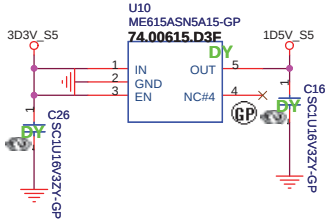
Bluetooth module





MDC 1.5 CONN





緯創資通 Wistron Corporation
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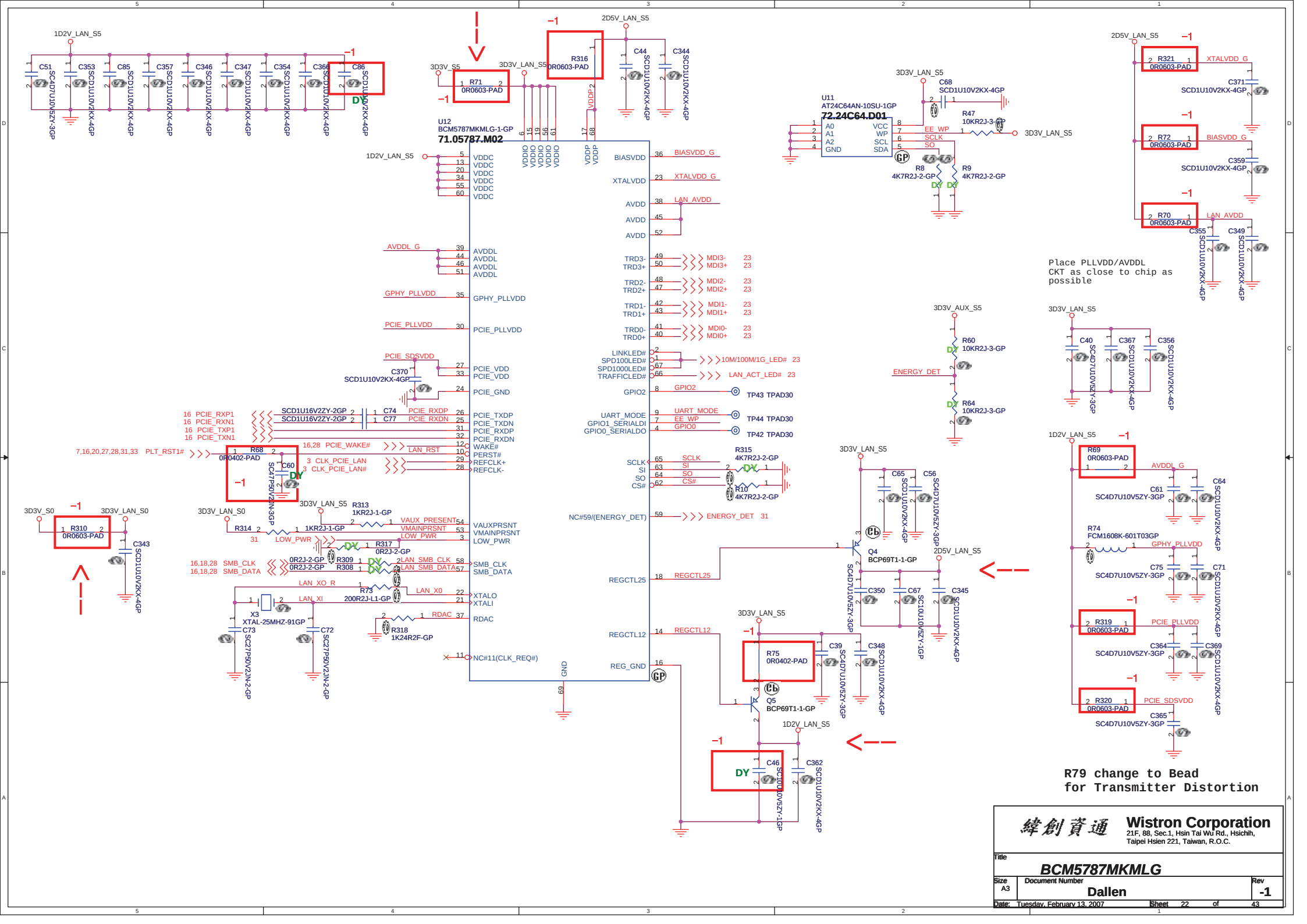
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB / MDC / BLUETOOTH**

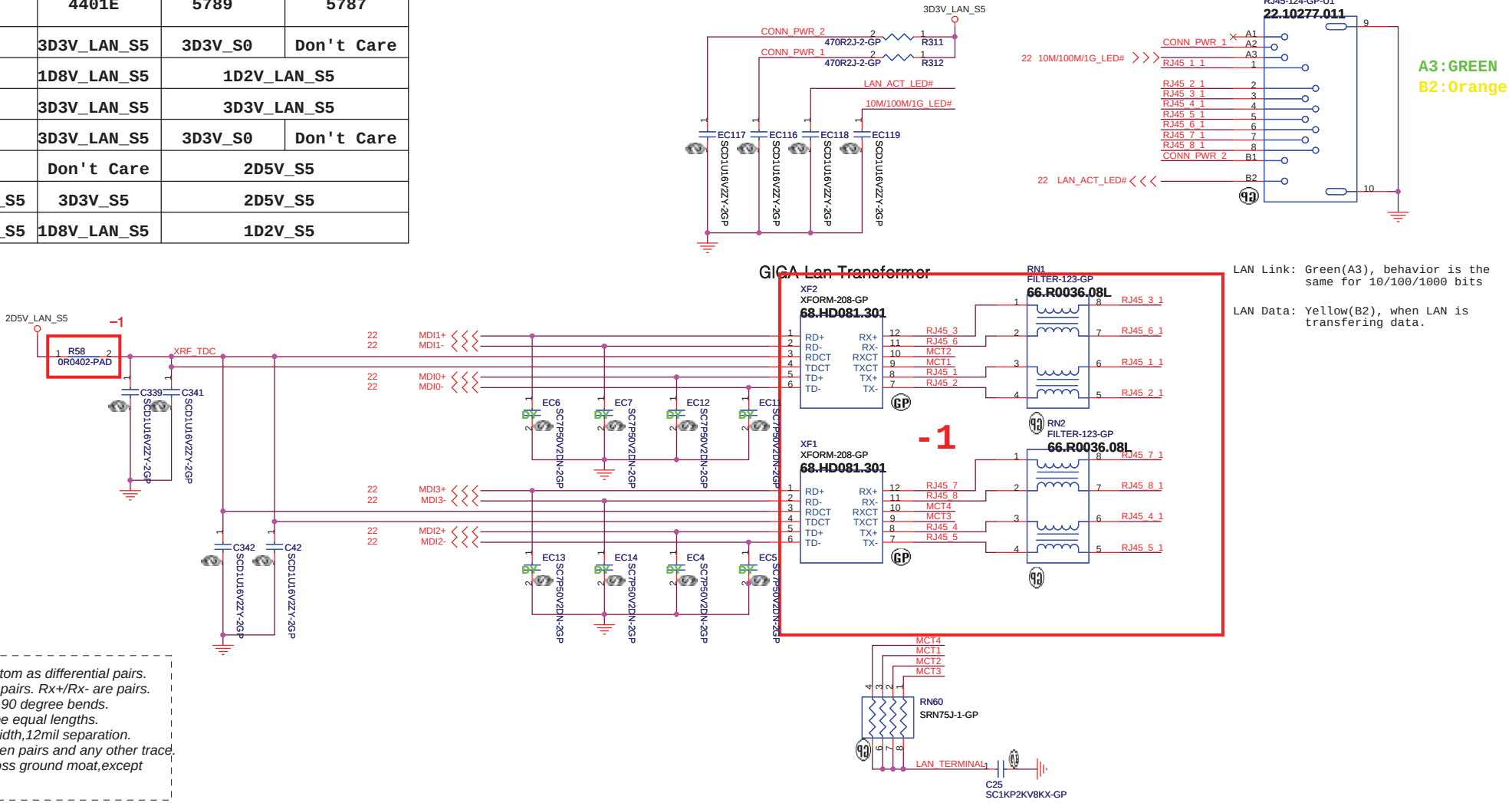
Size	Document Number	Rev
A3	Dallen	-1

Date: Tuesday, February 13, 2007 Sheet 21 of 43


U12
BCM5787MKMLG-1-GP
71.05787.M02
U11
AT24C64AN-10SU-1GP
72.24C64.D01
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R79 change to Bead
for Transmitter Distortion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5787MKMLG
Size A3
Document Number
Dallen
Rev -1
Date: Tuesday, February 13, 2007
Sheet 22 of 43

LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

緯創資通 **Wistron Corporation**
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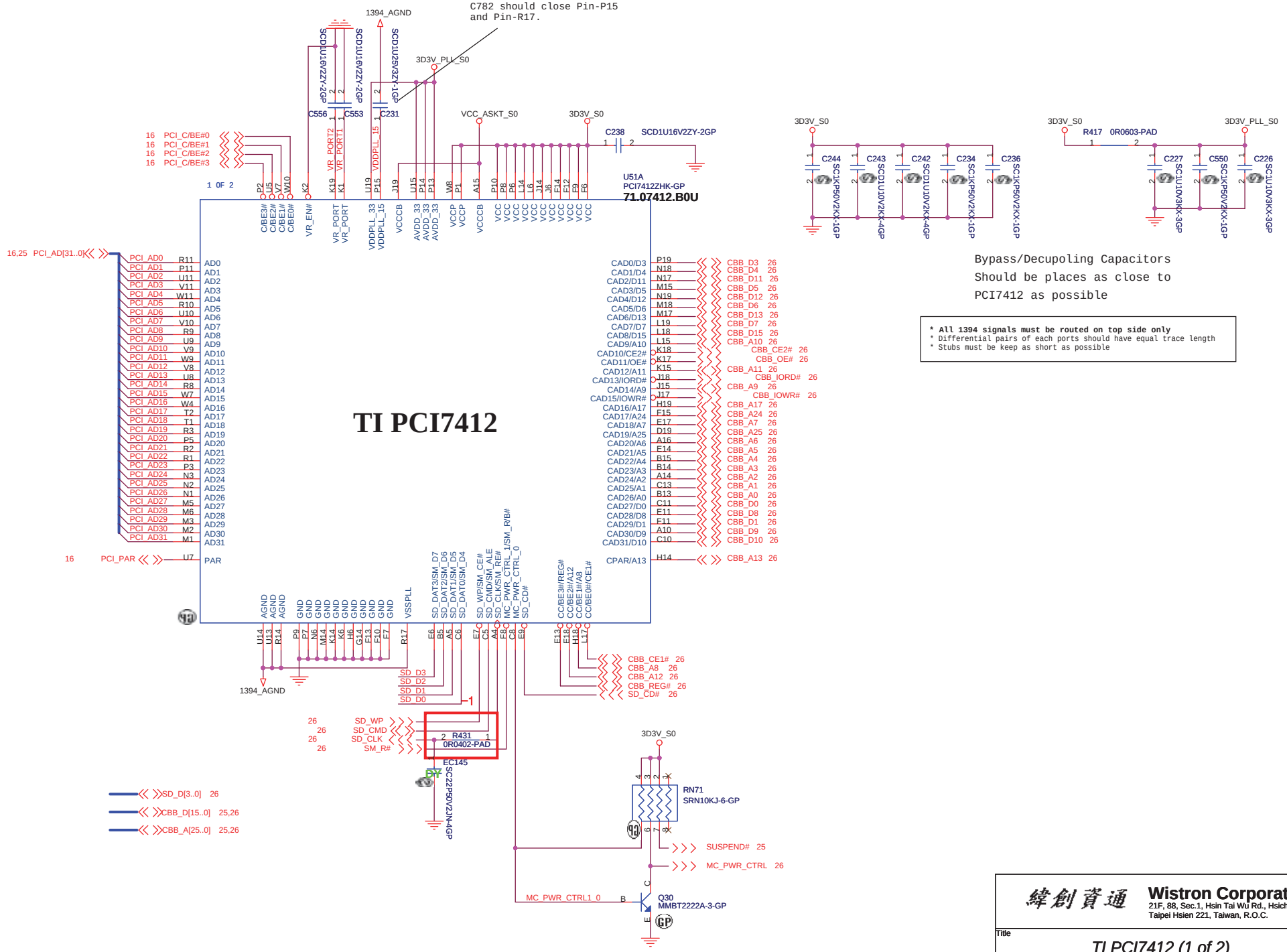
Title: **LAN Connector**

Size	Document Number	Rev
A3	Dallen	-1

Date: Tuesday, February 13, 2007 Sheet 23 of 43



Wistron Corporation			
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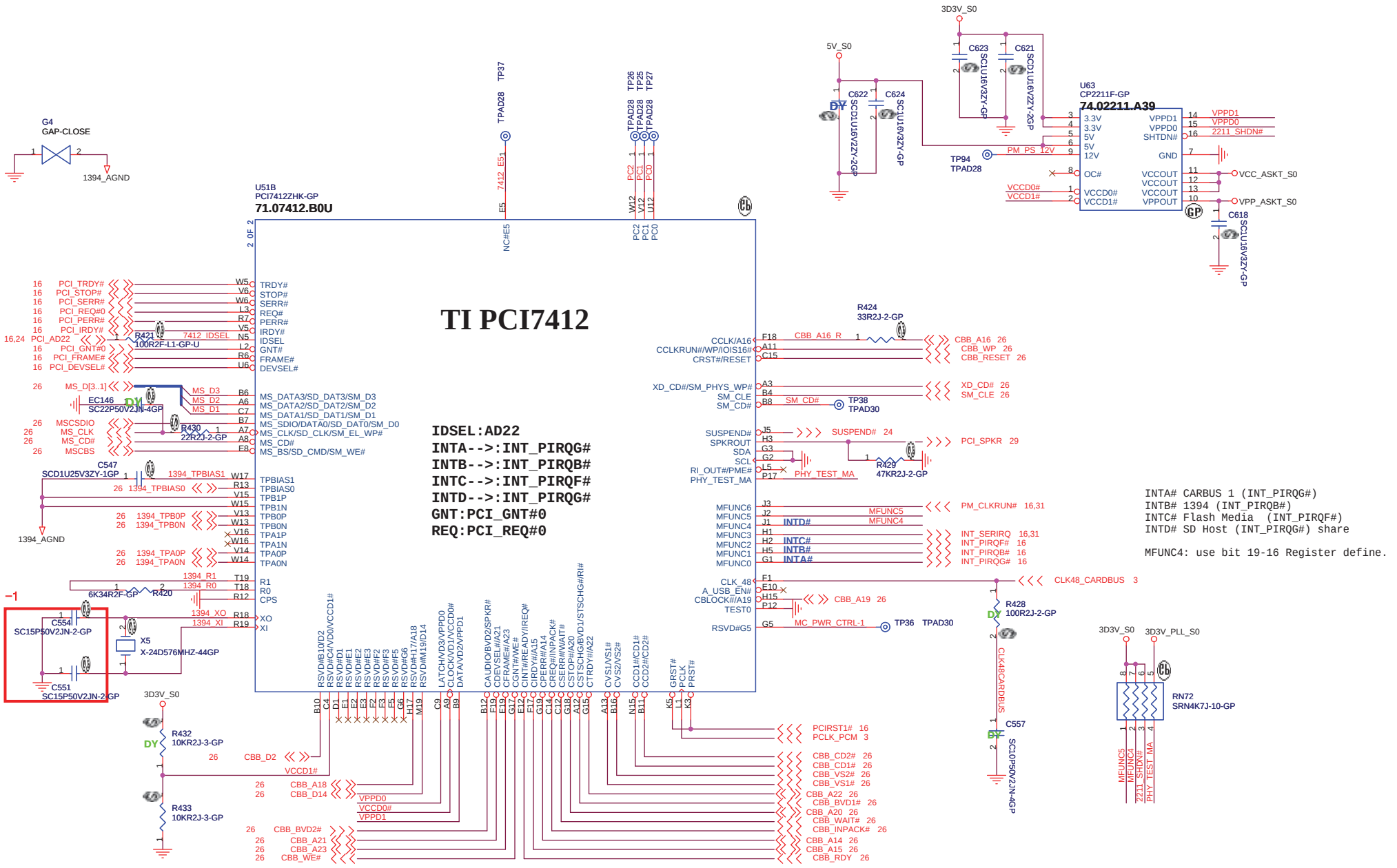
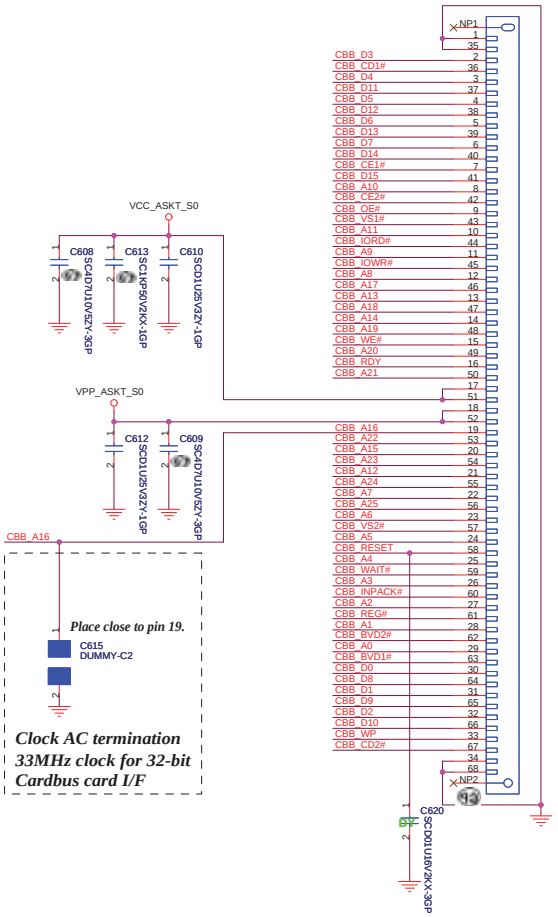
Title	TI PCI7412 (1 of 2)		
Size A3	Document Number Dallen		Rev -1
Date: Tuesday, February 13, 2007	Sheet 24 of 43		

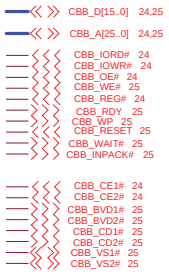


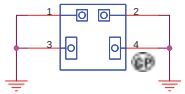
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	*TI PCI7412 (2 of 2)*		
Size A3	Document Number Dallen		Rev SB
Date: Tuesday, February 13, 2007	Sheet 25 of 43		

PCMCIA Socket

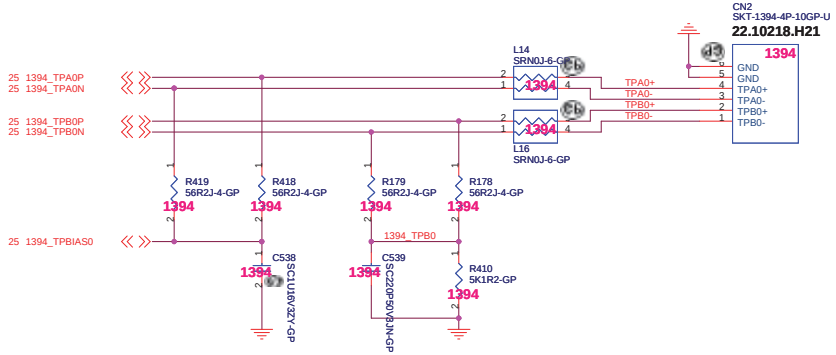


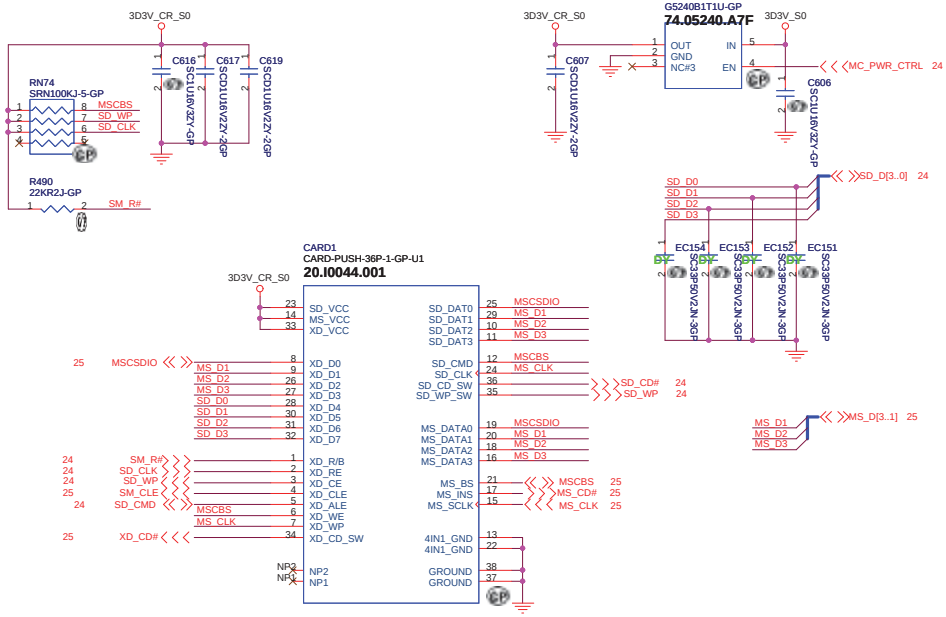
Cardbus I/F





1394 Connector





XD
MS / MS PRO
SD / SD IO / MMC

Wistron Corporation
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Title	PCMCIA / 1394 / CARD READER	
Size: Custom	Document Number: Dallen	Rev: -1
Date: Tuesday, February 13, 2007	Sheet 26 of 43	

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]

5V_S0
C416 SCD1U25V3KX-GP
R343 0R2J-2-GP
36,37,38,39 CPUCORE_ON
R333 0R0402-PAD
16,19,28,31,34,37,38,39 PM_SLP_S3#
1D8V_S3
C420 SCD1U25V3KX-GP
C419 SCD1U25V3KX-GP
DCBATOUT
C434 SCD47U25V6KX-1-GP
C433 SCD47U25V6KX-1-GP
C432 SCD47U25V6KX-1-GP
C427 SCD1U25V3KX-GP
C430 SCD1U25V3KX-GP

13 LCD_TXBOUT0+
13 LCD_TXBOUT0-
13 LCD_TXBOUT1+
13 LCD_TXBOUT1-
13 LCD_TXBOUT2+
13 LCD_TXBOUT2-
13 LCD_TXBCLK+
13 LCD_TXBCLK-
14 NV_BLUE
14 NV_GREEN
14 NV_RED
14 NV_TV_COMP
14 NV_TV_LUMA
14 NV_TV_CRMA

LCD_TXACLK- 13
LCD_TXACLK+ 13
LCD_TXAOUT2- 13
LCD_TXAOUT2+ 13
LCD_TXAOUT1- 13
LCD_TXAOUT1+ 13
LCD_TXAOUT0- 13
LCD_TXAOUT0+ 13
NV_EDID_DAT 13
NV_EDID_CLK 13
NV_LCDVDD_ON 13
NV_BLON 31
NV_DVI_DAT 42
NV_DVI_CLK 42

R113 0R3-0-U-GP
C417 SCD1U25V3KX-GP
2D5V_S0
3D3V_S0
C415 SC10U10V5ZY-1GP
MXM1 TYCO-CONN230A-GP-U3
20.F0871.230

3 CLK_PCIE_PEG#
3 CLK_PCIE_PEG
7,16,20,22,28,31,33 PLT_RST1#
R359 0R0402-PAD
PLT_RST1#_MXM
C428 SC100P50V2JN-3GP

19,31 SMBD_G792
R139 0R2J-2-GP
SMBD_MXM
19,31 SMBC_G792
R358 0R2J-2-GP
SMBC_MXM

34 MXM_THER
14 NV_HSYNC
14 NV_VSYNC
14 NV_DDCCLK
14 NV_DDCDAT

TPAD30 TP17 SPDIF_HDMI
TPAD30 TP63 GPU_BUFRST#
TPAD30 TP67 MP_INT
TPAD30 TP65 GPU_PRGM#

TPAD30 TP56 IGP_UTX2#
TPAD30 TP57 IGP_UTX2
TPAD30 TP60 TMDS_GPIO6_SW
TPAD30 TP19

EMI REQUEST

TMDS_A_TX0+ 1 ERN4 4 TMDS_A_TX0+ 42
TMDS_A_TX0- 2 3 TMDS_A_TX0- 42
SRN33J-5-GP-U
TMDS_A_TX1+ 1 ERN3 4 TMDS_A_TX1+ 42
TMDS_A_TX1- 2 3 TMDS_A_TX1- 42
SRN33J-5-GP-U
TMDS_A_TX2+ 1 ERN2 4 TMDS_A_TX2+ 42
TMDS_A_TX2- 2 3 TMDS_A_TX2- 42
SRN33J-5-GP-U
TMDS_A_TXC+ 1 ERN1 4 TMDS_A_TXC+ 42
TMDS_A_TXC- 2 3 TMDS_A_TXC- 42
SRN33J-5-GP-U

ERN* 要靠近MXM conn.

DVI_A_HPD 42

TMDS_B_TX0+ TP69 TPAD30
TMDS_B_TX0- TP68 TPAD30
TMDS_B_TX1+ TP55 TPAD30
TMDS_B_TX1- TP54 TPAD30
TMDS_B_TX2+ TP62 TPAD30
TMDS_B_TX2- TP61 TPAD30
G72_27MHZ TP58 TPAD30
G72_27MHZSS TP66 TPAD30
DVI_B_HPD TP64 TPAD30
TMDS_B_TXC+ TP53 TPAD30
TMDS_B_TXC- TP52 TPAD30

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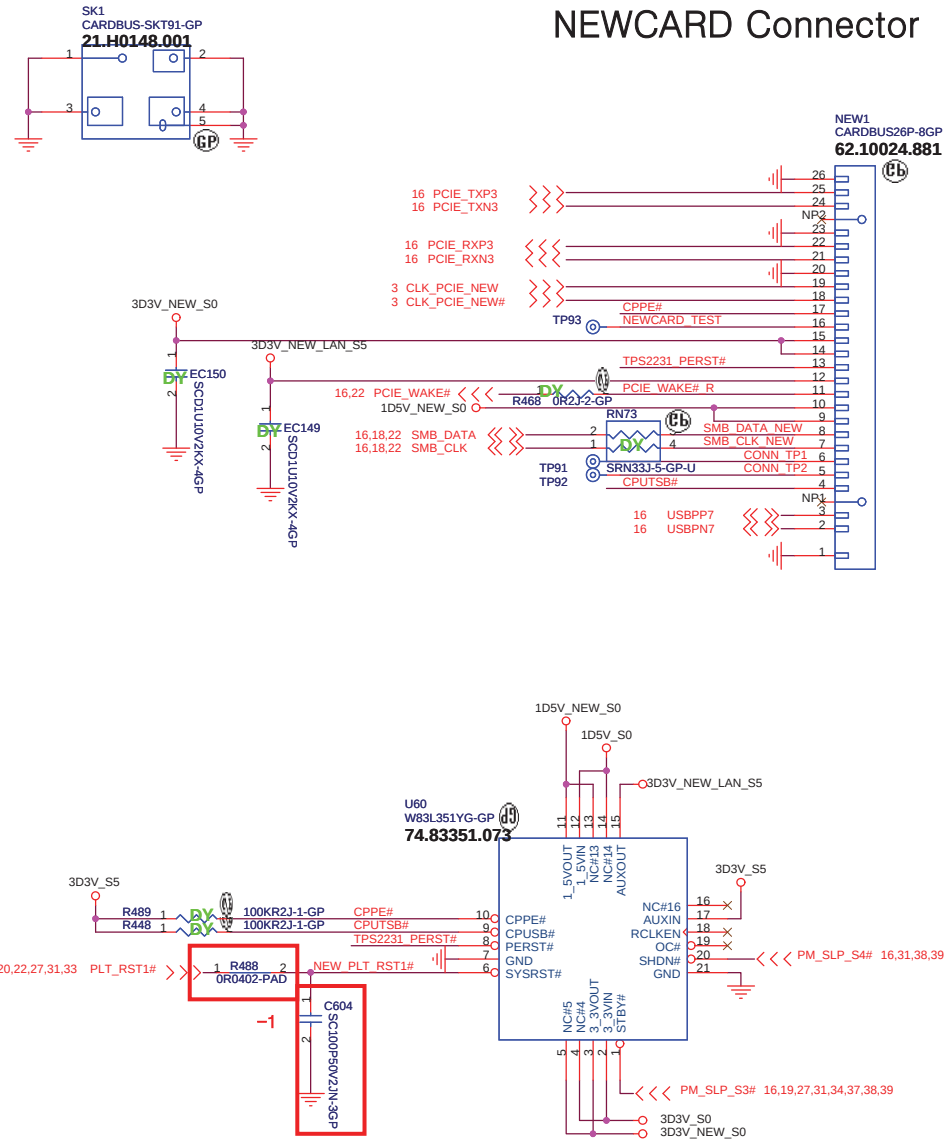
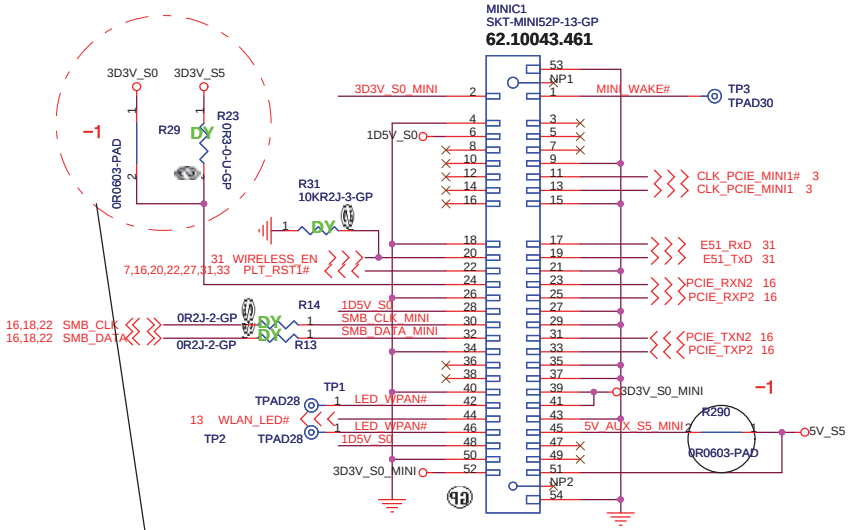
Title	Graphic MXM CONN
Size A3	Document Number Dallen
Rev	-1
Date: Tuesday, February 13, 2007	Sheet 27 of 43

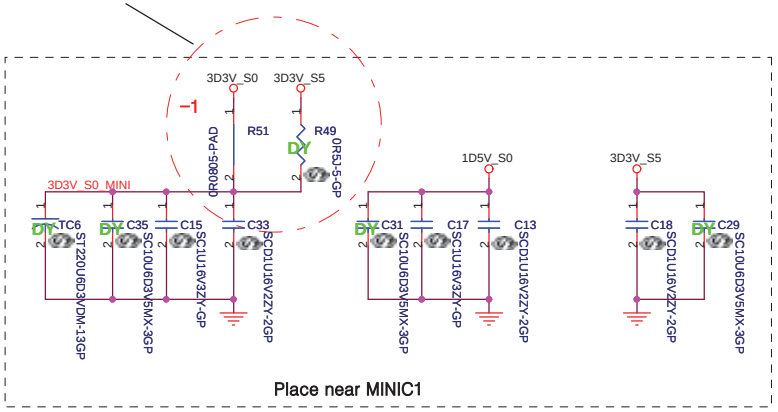
NEWCARD Connector

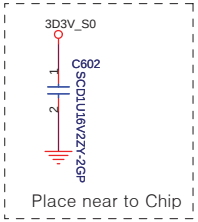


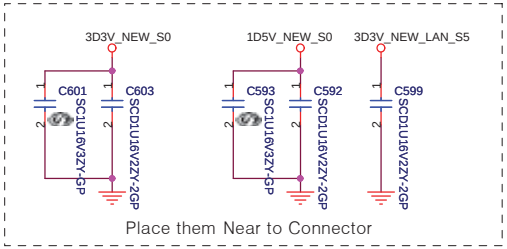
Mini Card Connector



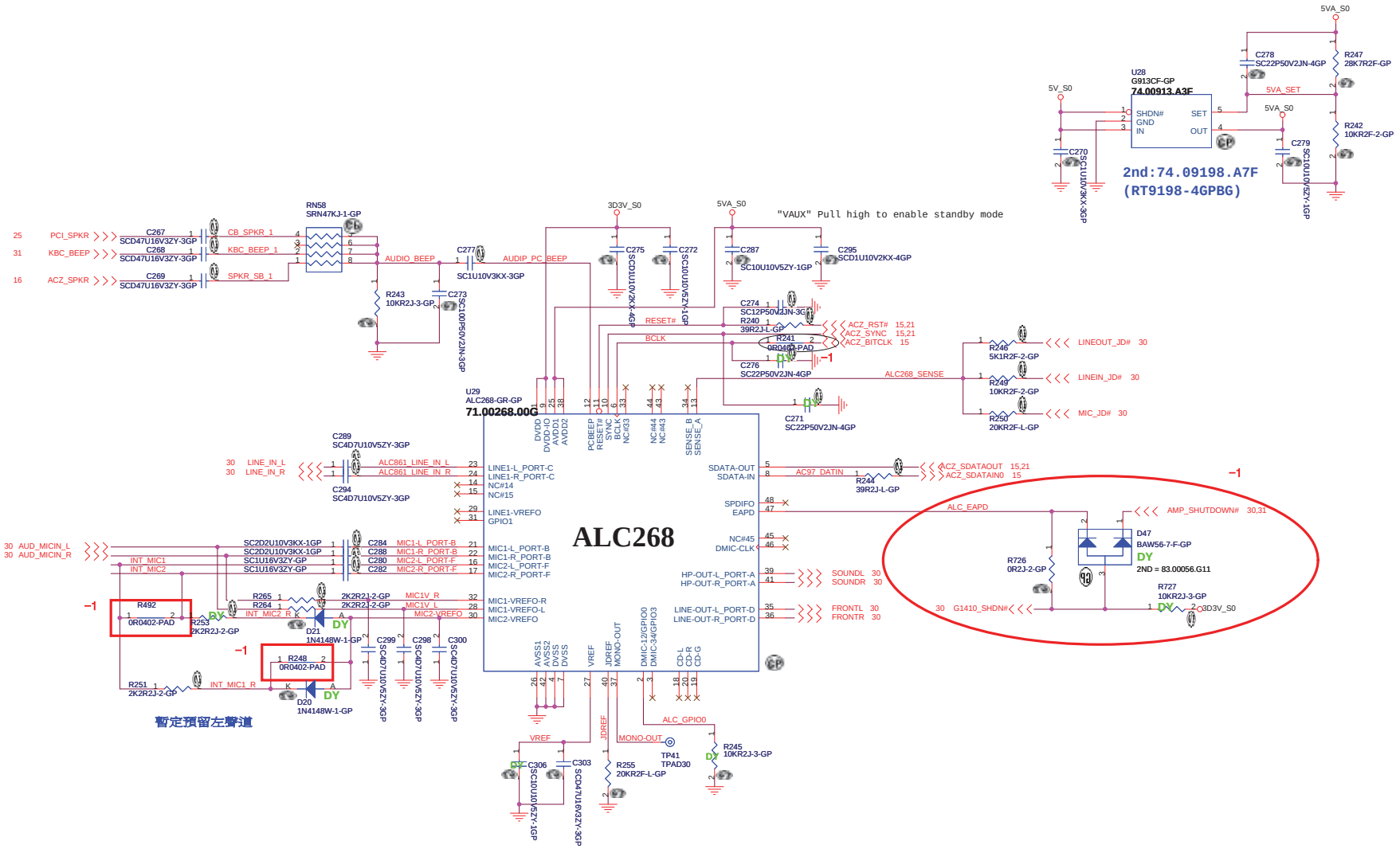
PCIE Mini Card For WLAN w/o iAMT, TV or 3G







緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MINI CARD / NEW CARD***	
Size A3	Document Number **Dallen**	Rev **-1**
Date: Tuesday, February 13, 2007	Sheet 28 of 43	



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: AZALIA CODEC - ALC268

Size	Document Number	Rev
Custom	Dallen	-1

Date: Tuesday, February 13, 2007 Sheet 29 of 43

Audio OP Amplifier

KBC_MUTE_GPIO8

R,L 1.5W Speaker
mount R274,R281
R269->63.36334.1DL
R268->63.33334.1DL

R,L 1W Speaker
mount R280,R281
R269->63.15334.1DL
R268->63.12334.1DL

R,L 1.2W Speaker
mount R280,R281
R269->63.10334.1DL
R268->63.68234.1DL

Internal Speaker

SPKR1 ACES-CON4-1-GP
20.D0197.104

MIC IN

MICIN1 PHONE-JK233-GP
22.10133.B01

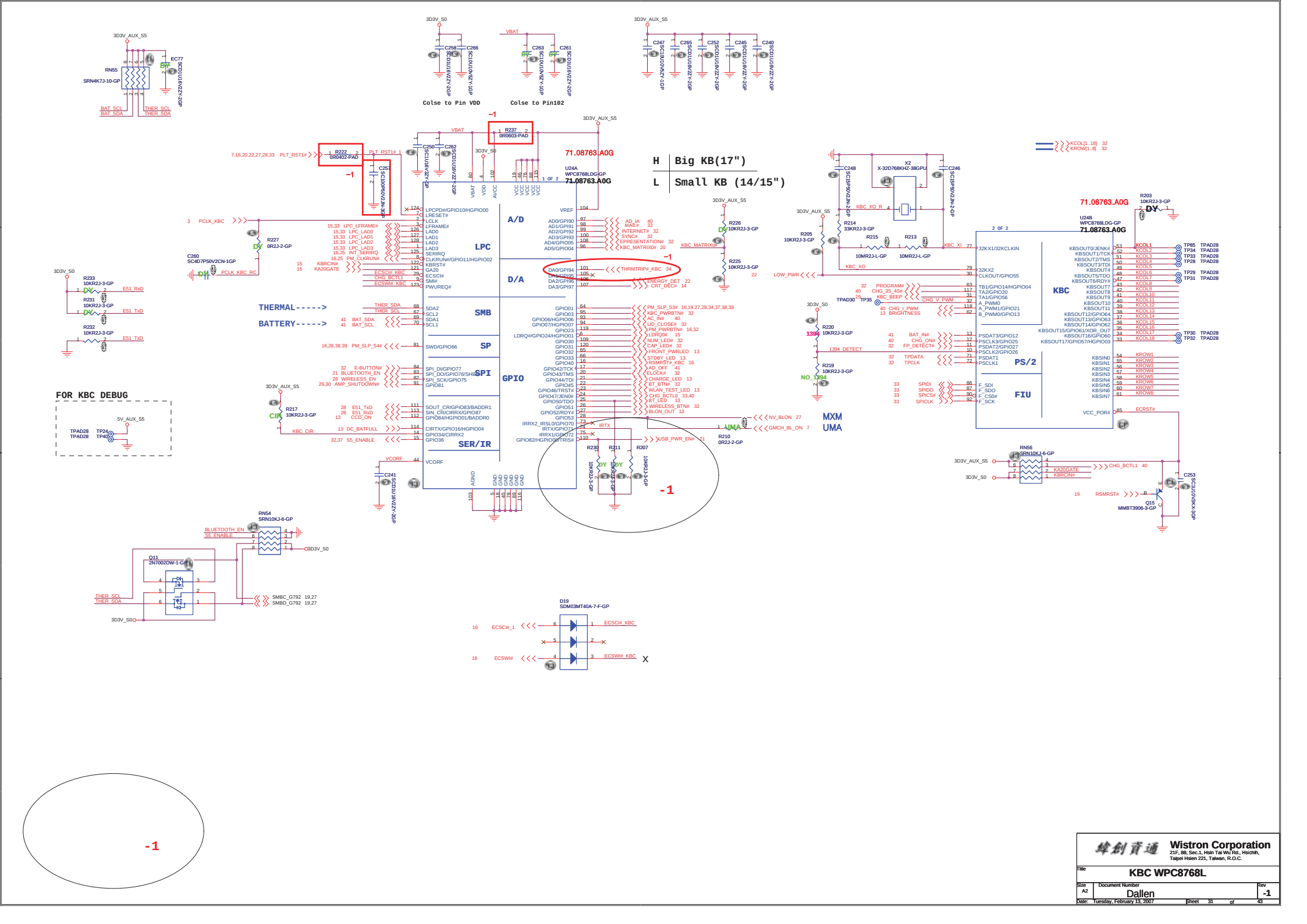
LINE IN

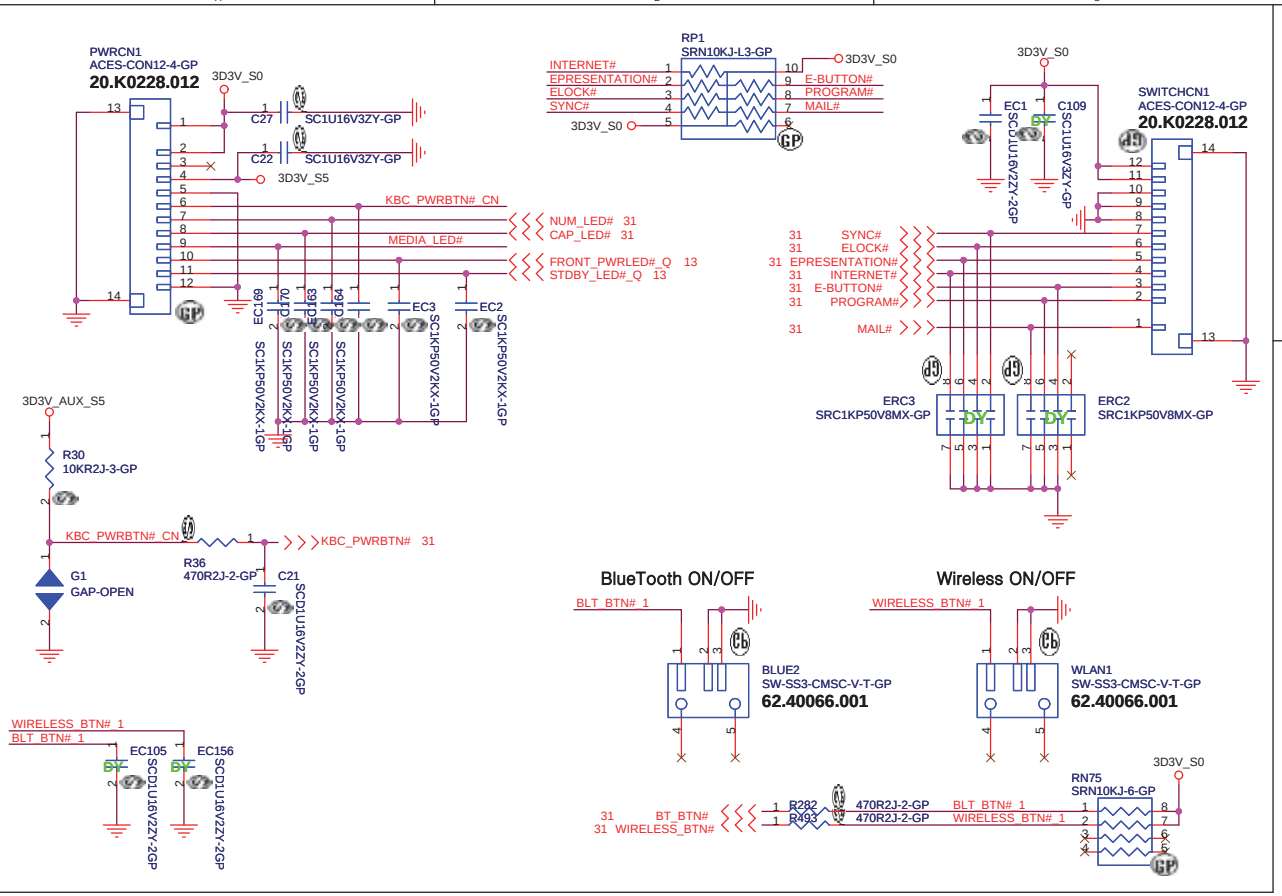
LIN1 PHONE-JK234-GP
22.10133.B11

LINE OUT

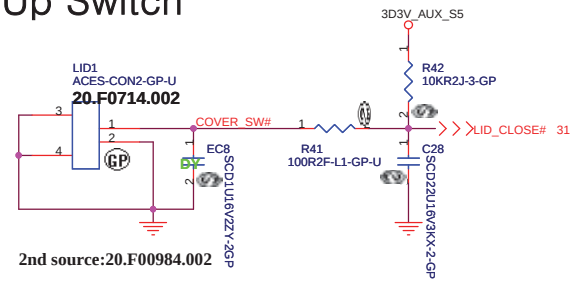
LOUT1 PHONE-JK235-GP
22.10133.B21

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AUDIO AMP AND JACK
Size: Custom	Document Number: Dallen
Rev	-1
Date: Tuesday, February 13, 2007	Sheet 30 of 43

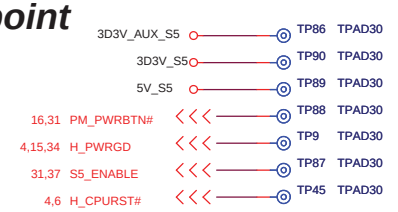

Colse to Pin VDD
Colse to Pin102
71.08763.A0G
H | Big KB(17")
L | Small KB (14/15")
U24A WPC8768LDG-GP
U24B WPC8768LDG-GP
X2 X-32D768KHZ-38GPU
THERMAL-----> BATTERY----->
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
MXM
UMA
FOR KBC DEBUG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
Dallen
Tuesday, February 13, 2007



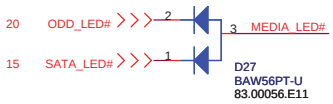
Cover Up Switch



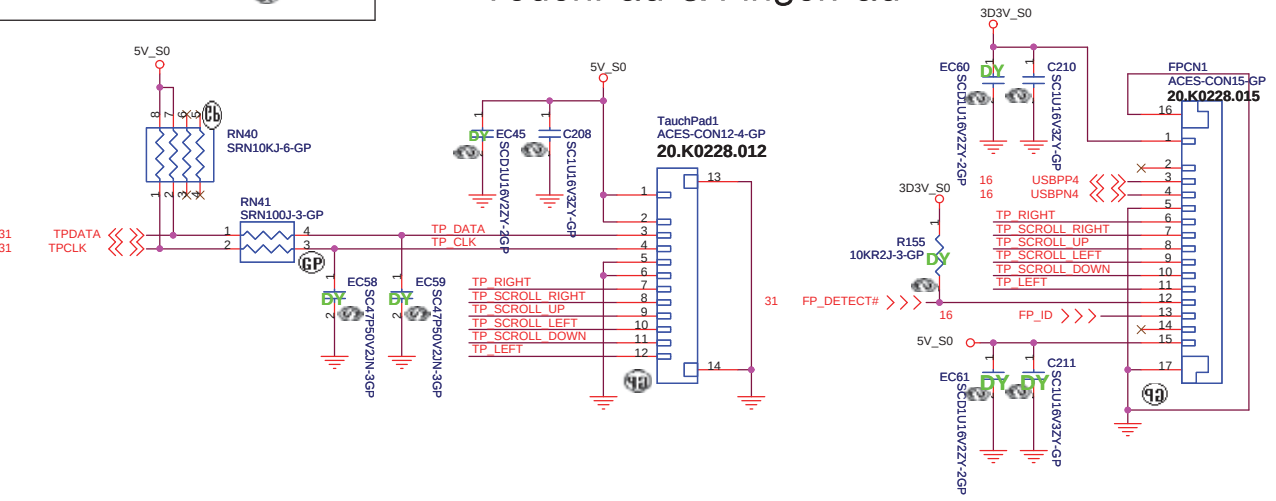
Check test point

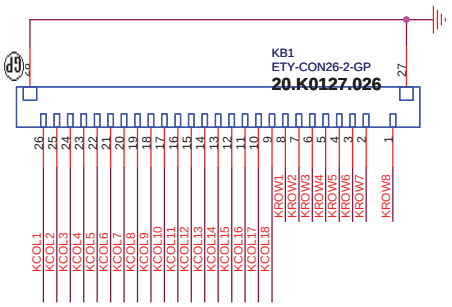


Test Point放在Dimm Door打開可量測處



TouchPad & FingerPad



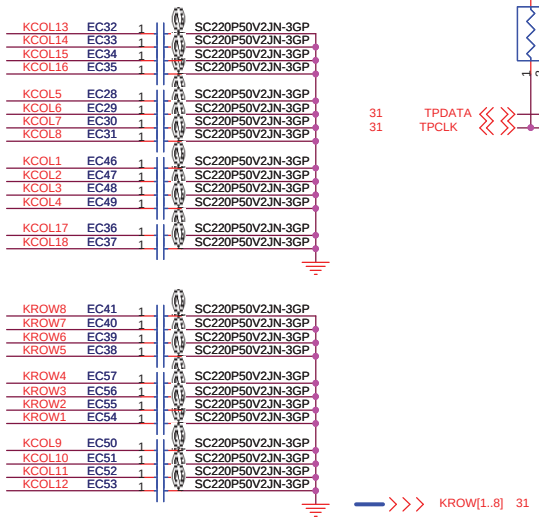


Internal KeyBoard conn.

1 25

CHECK KB SPEC. AND PIN DEFINE

EMI Bypass cap.



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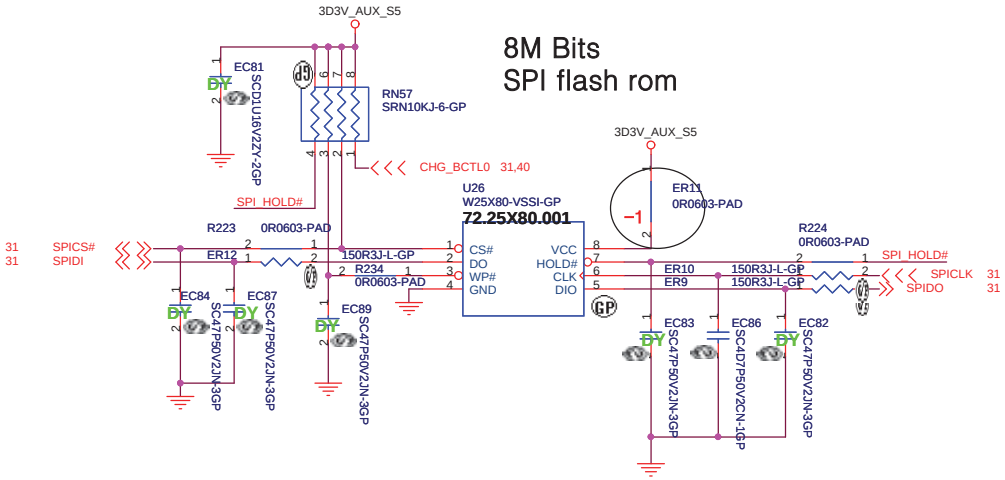
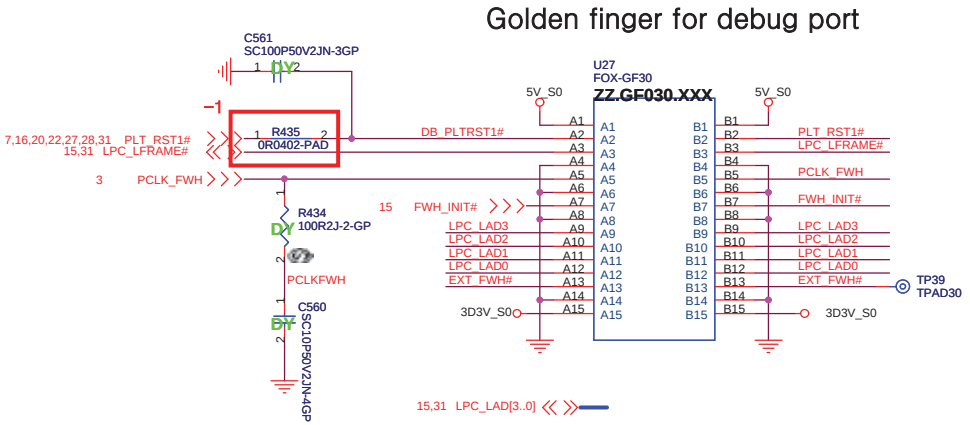
Title: *BUTTONs / KB / TOUCHPAD / FP*

Size: A3 | Document Number: Dallen | Rev: -1

Date: Tuesday, February 13, 2007 | Sheet 32 of 43





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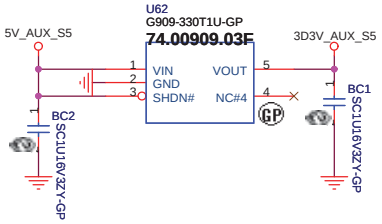
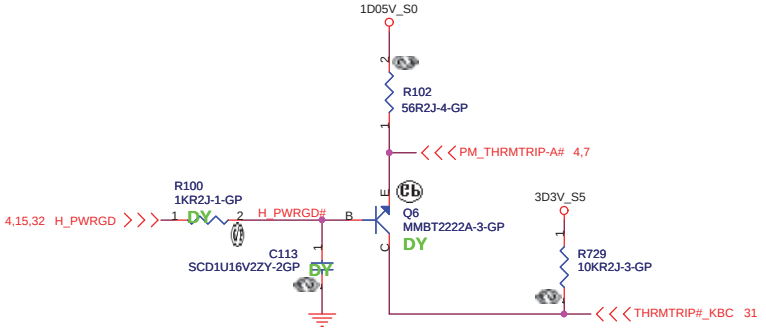
Title	BIOS and Debug Port	
Size A3	Document Number Dallen	Rev -1
Date: Tuesday, February 13, 2007	Sheet 33 of 43	

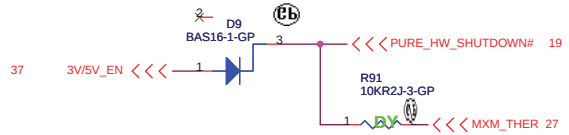
Aux Power

3D3V_AUX_S5

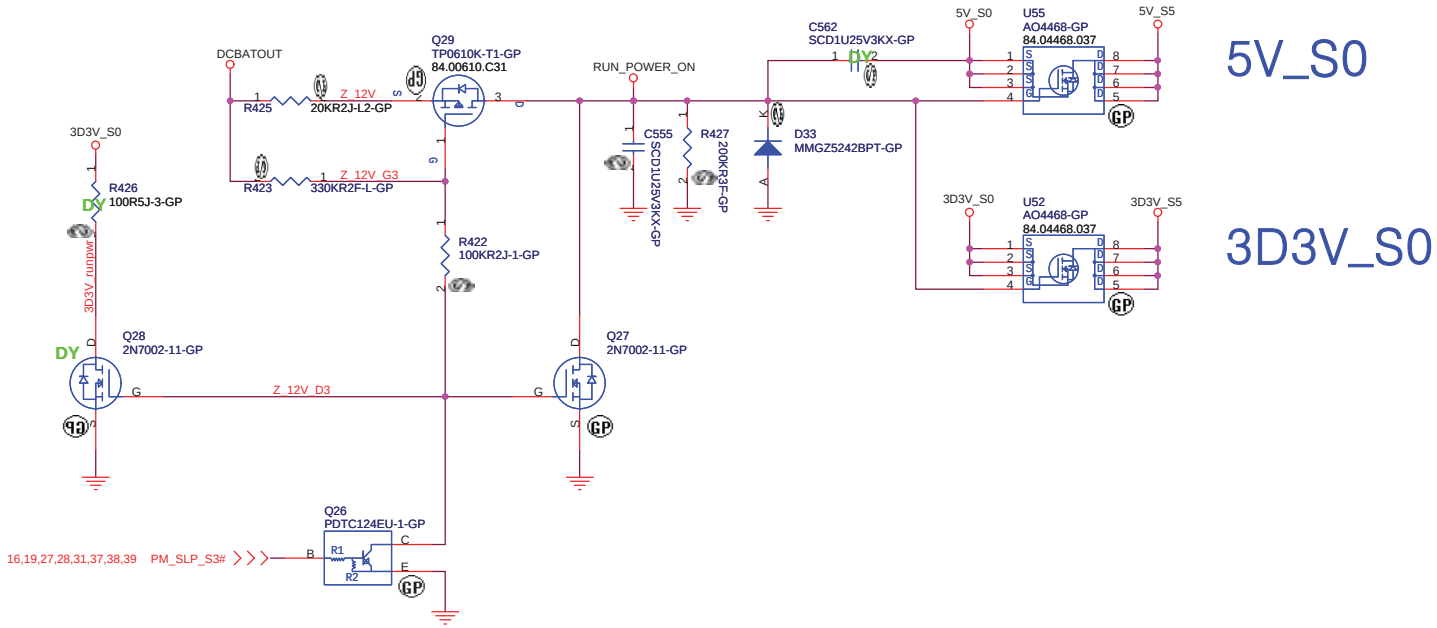
I max = 150 mA







Run Power



5V_S0

3D3V_S0

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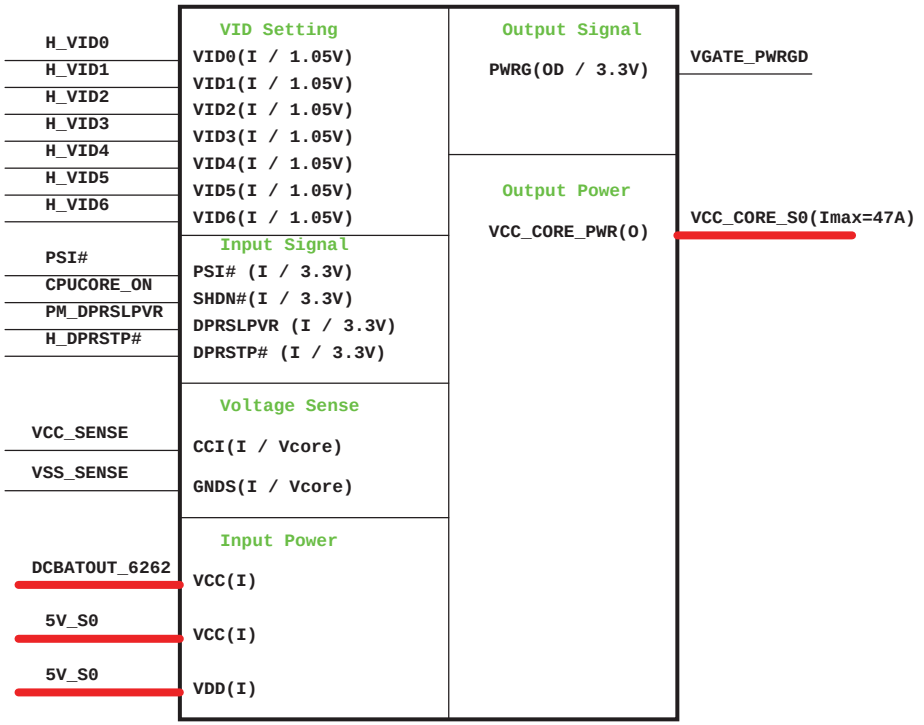
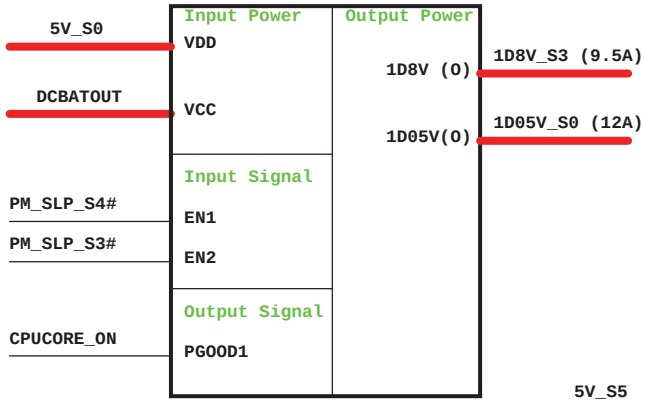
Title: 3D3V_AUX_S5 / 3D3V_S0 / 5V_S0			
Size: A3	Document Number: Dallen		Rev: -1
Date: Tuesday, February 13, 2007	Sheet 34 of 43		

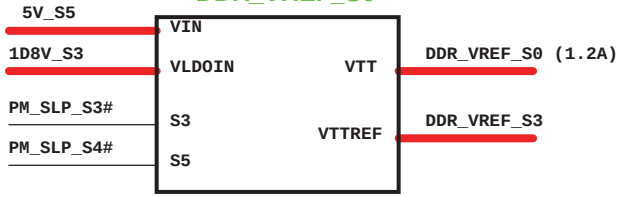
CPU_CORE
MAX8770



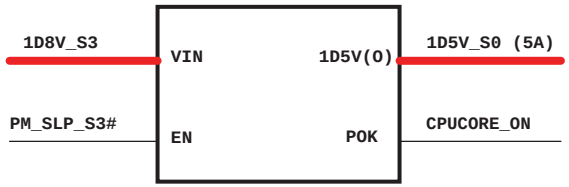
MAX8717
1D8V_S3 / 1D05V_S0



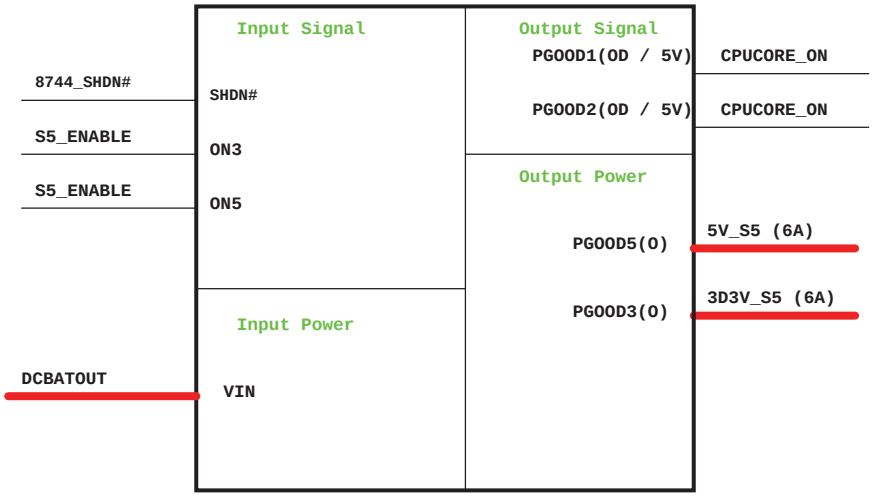
TPS51100
DDR_VREF_S0



APL5912
1D5V_S0

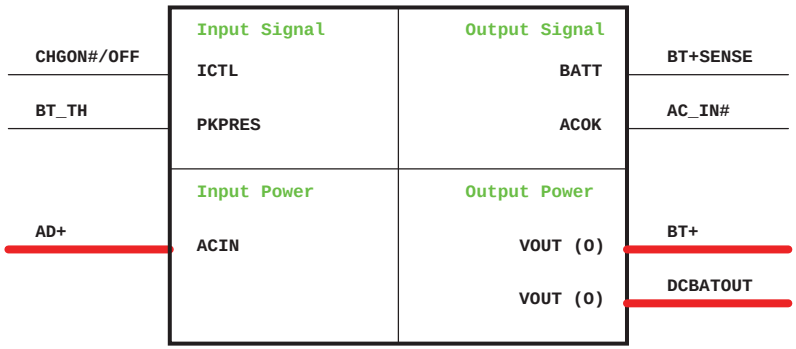


MAX8744
5V_S5 / 3D3V_S5



APL5312
2D5V_S0

Charger ISL6255



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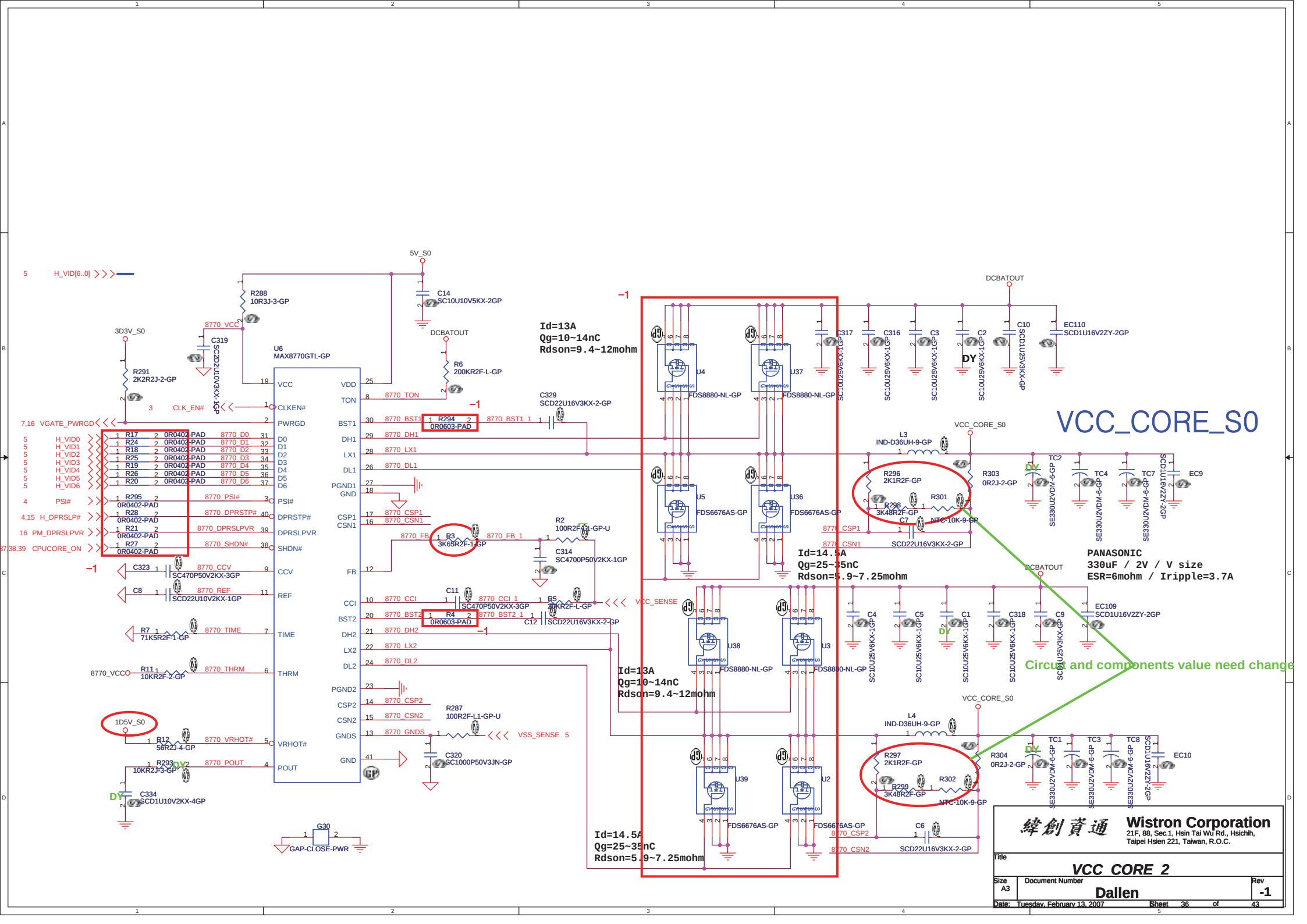
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	Dallen	-1

Date: Tuesday, February 13, 2007 Sheet 35 of 43


VCC_CORE_S0
U6
MAX8770GTL-GP
Id=13A
Qg=10~14nC
Rdson=9.4~12mohm
Id=14.5A
Qg=25~35nC
Rdson=5.9~7.25mohm
PANASONIC
330uF / 2V / V size
ESR=6mohm / Iripple=3.7A
Circuit and components value need change
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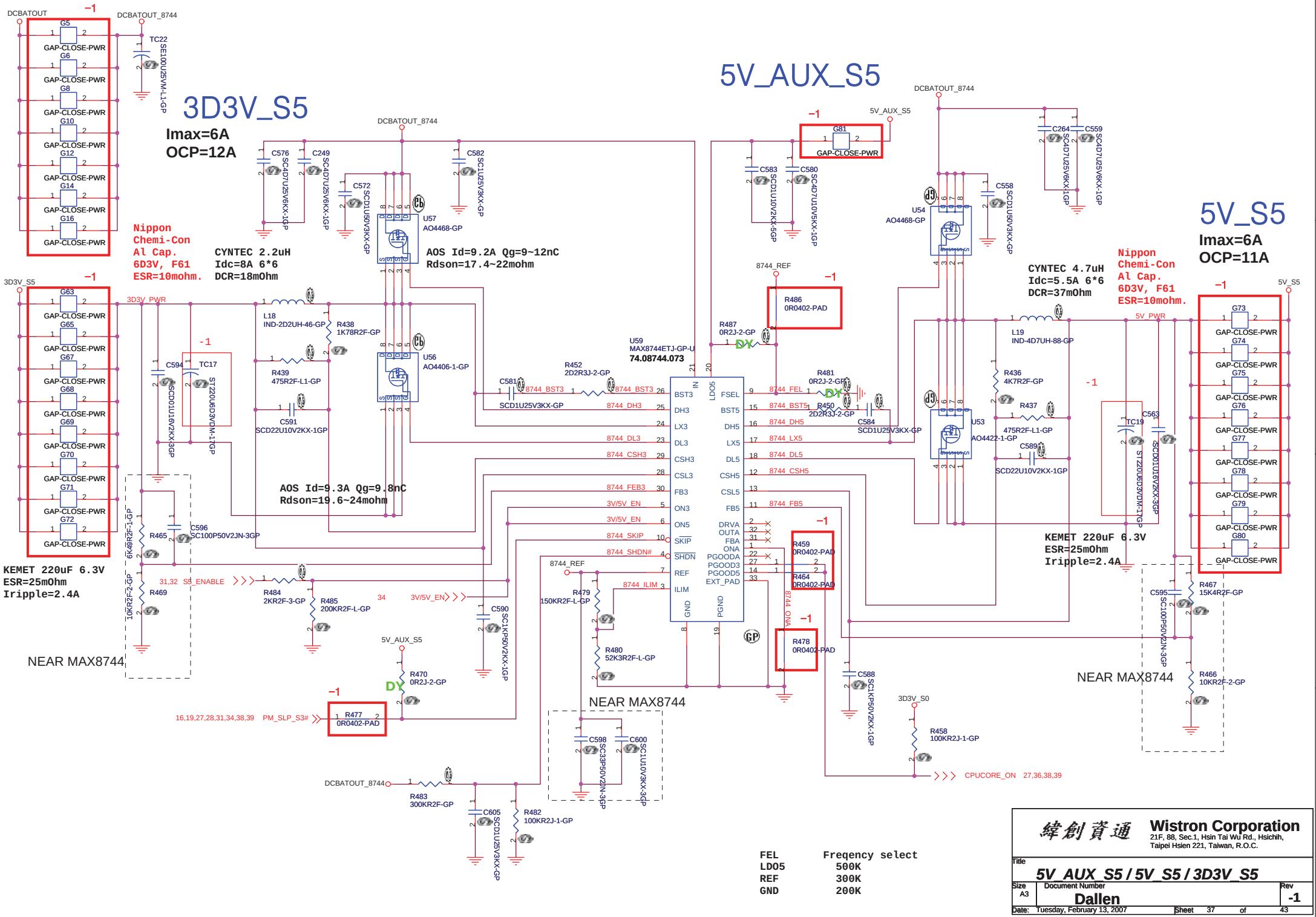
Taipei Hsien 221, Taiwan, R.O.C.
VCC_CORE_2
Dallen
Size A3
Rev -1
Date: Tuesday, February 13, 2007
Sheet 36 of 43


3D3V_S5
Imax=6A
OCP=12A
5V_AUX_S5
5V_S5
Imax=6A
OCP=11A
Nippon Chemi-Con Al Cap. 6D3V, F61 ESR=10mohm.
CYNTEC 2.2uH Idc=8A 6*6 DCR=18mOhm
AOS Id=9.2A Qg=9~12nC Rdson=17.4~22mohm
AOS Id=9.3A Qg=9.8nC Rdson=19.6~24mohm
CYNTEC 4.7uH Idc=5.5A 6*6 DCR=37mOhm
KEMET 220uF 6.3V ESR=25mOhm Iripple=2.4A
NEAR MAX8744
U59 MAX8744ETJ-GP-U 74.08744.073
FEL LDO5 REF GND Freqency select 500K 300K 200K
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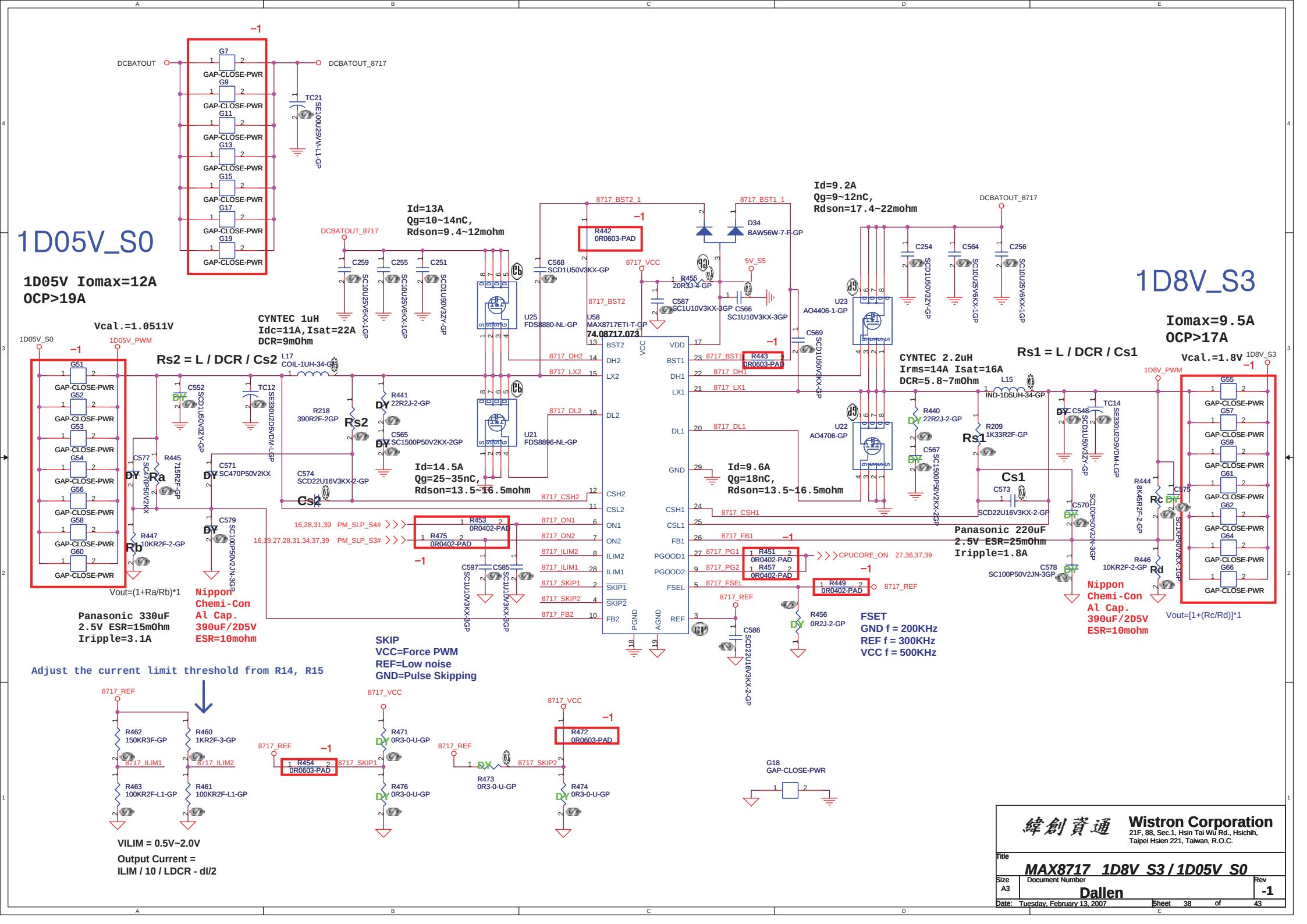
5V_AUX_S5 / 5V_S5 / 3D3V_S5
Dallen
Rev -1
Date: Tuesday, February 13, 2007
Sheet 37 of 43


1D05V_S0
1D05V Iomax=12A
OCP>19A
Vcal.=1.0511V
Rs2 = L / DCR / Cs2
Vout=(1+Ra/Rb)*1
Panasonic 330uF
2.5V ESR=15mOhm
Iripple=3.1A
Nippon
Chemi-Con
Al Cap.
390uF/2D5V
ESR=10mohm
Id=13A
Qg=10~14nC,
Rdson=9.4~12mohm
CYNTEC 1uH
Idc=11A,Isat=22A
DCR=9mOhm
Id=14.5A
Qg=25~35nC,
Rdson=13.5~16.5mohm
Id=9.6A
Qg=18nC,
Rdson=13.5~16.5mohm
Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm
CYNTEC 2.2uH
Irms=14A Isat=16A
DCR=5.8~7mOhm
Rs1 = L / DCR / Cs1
Panasonic 220uF
2.5V ESR=25mOhm
Iripple=1.8A
1D8V_S3
Iomax=9.5A
OCP>17A
Vcal.=1.8V
Vout=[1+(Rc/Rd)]*1
SKIP
VCC=Force PWM
REF=Low noise
GND=Pulse Skipping
FSET
GND f = 200KHz
REF f = 300KHz
VCC f = 500KHz
Adjust the current limit threshold from R14, R15
VILIM = 0.5V~2.0V
Output Current =
ILIM / 10 / LDCR - dI/2
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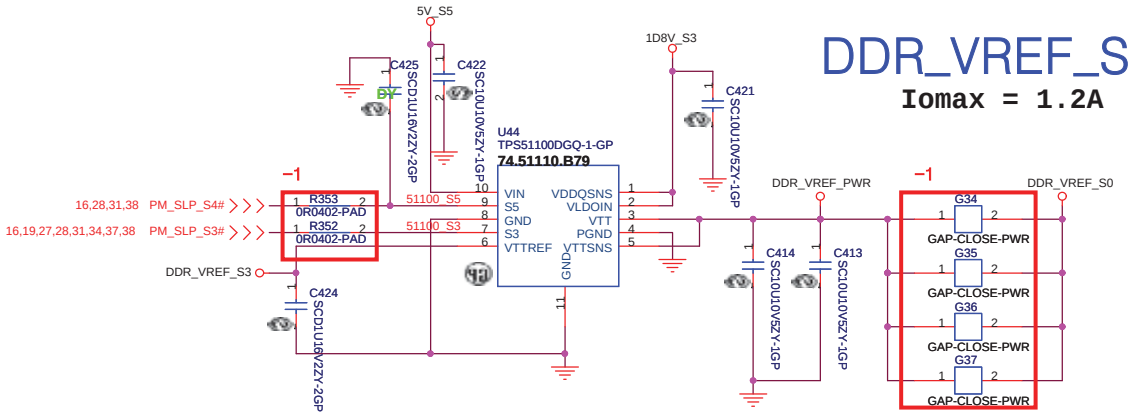
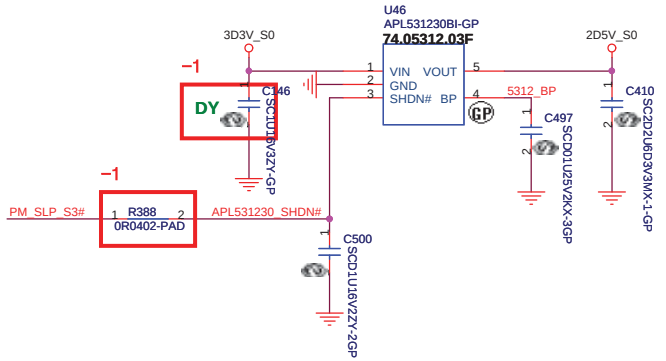
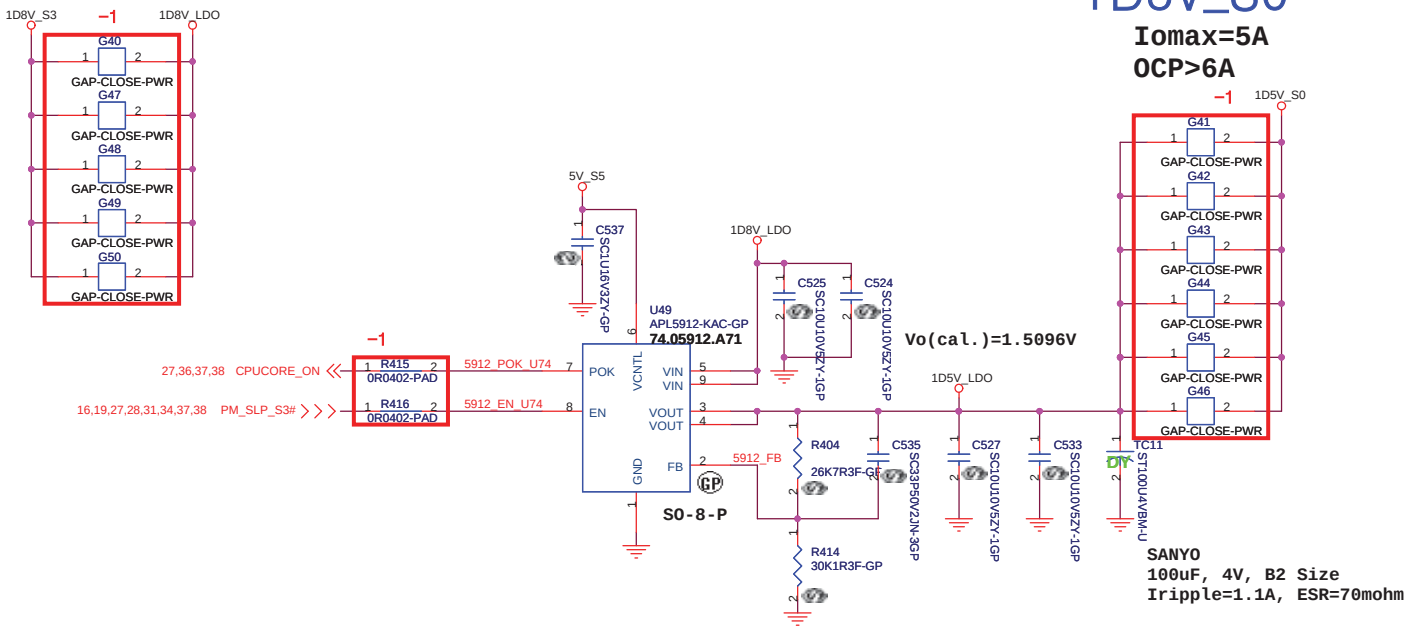
Taipei Hsien 221, Taiwan, R.O.C.
MAX8717 1D8V S3 / 1D05V S0
Dallen
Tuesday, February 13, 2007
Sheet 38 of 43







DDR_VREF_S3

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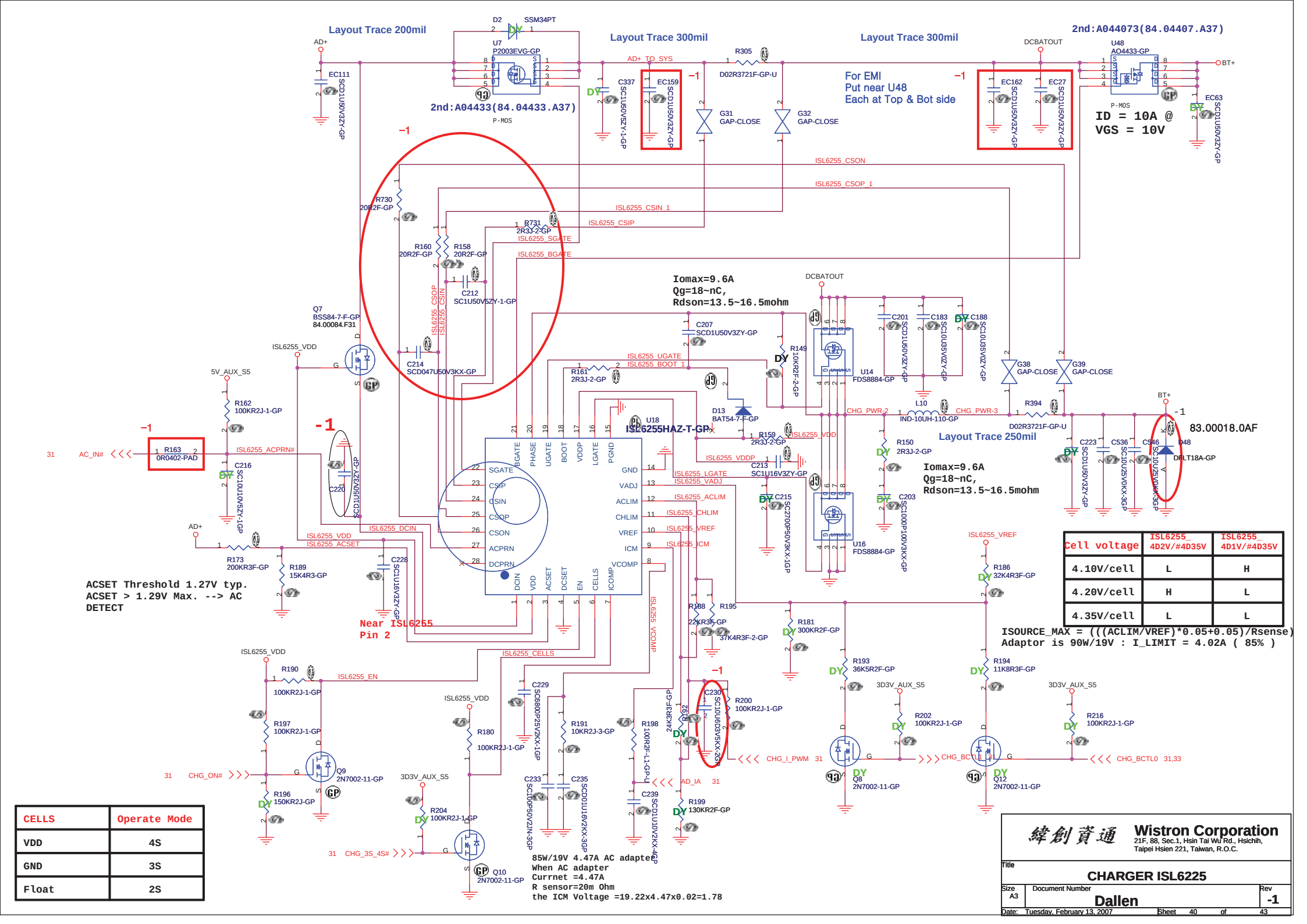
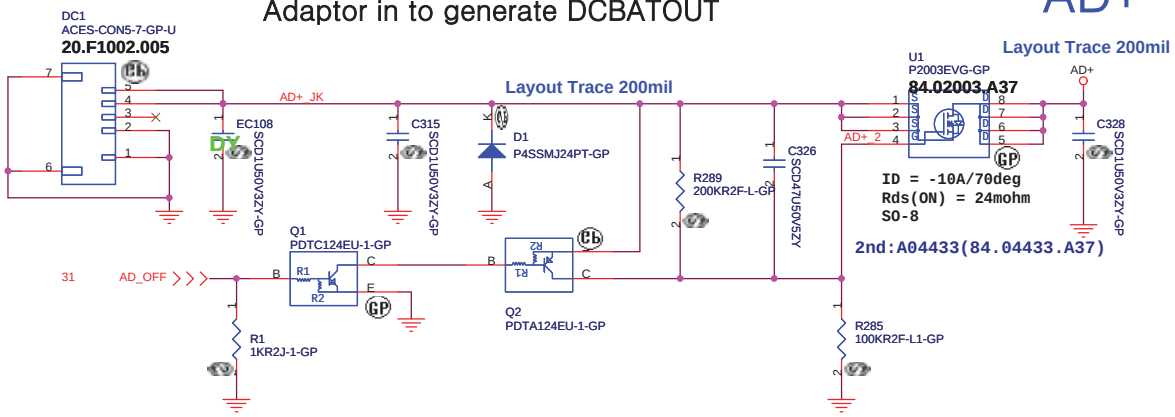
Title	1D5V_S0 / 2D5V_S0 / DDR_VREF_S0		
Size A3	Document Number: Dallen		Rev: -1
Date: Tuesday, February 13, 2007	Sheet 39 of 43		



Cell voltage	ISL6255_4D2V/#4D35V	ISL6255_4D1V/#4D35V
4.10V/cell	L	H
4.20V/cell	H	L
4.35V/cell	L	L

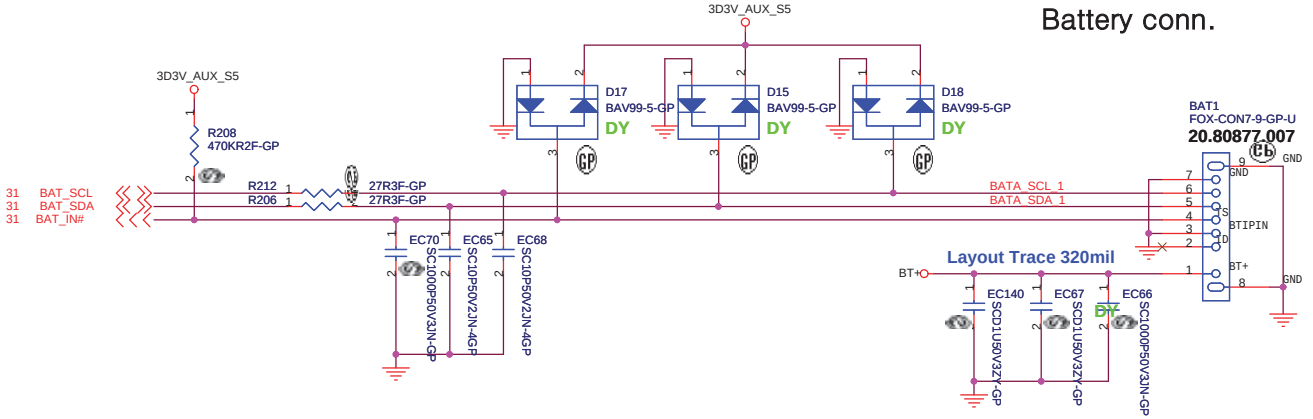
CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

Adaptor in to generate DCBATOUT



AD+

Battery conn.



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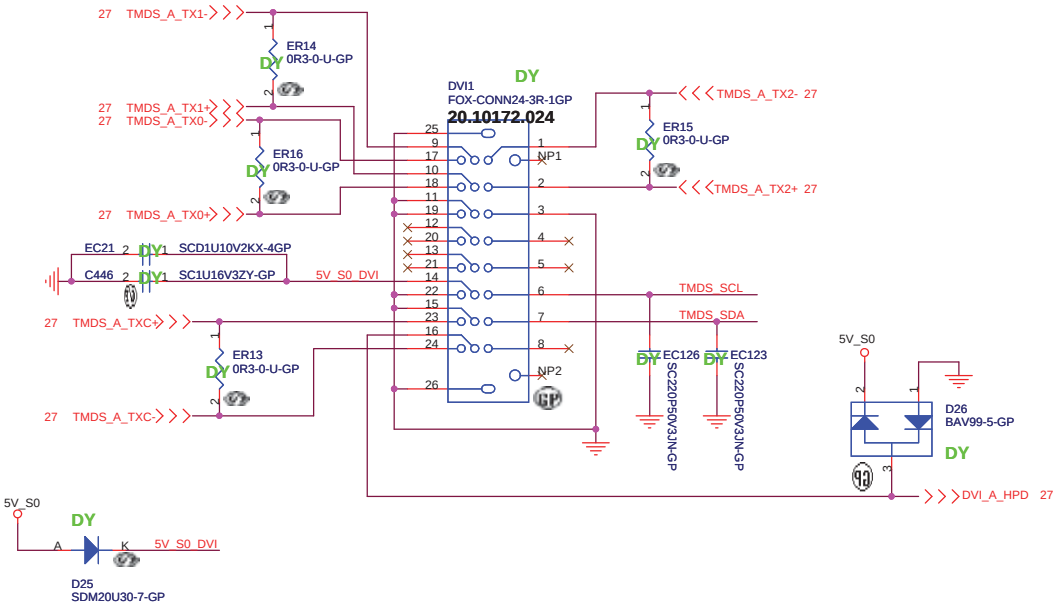
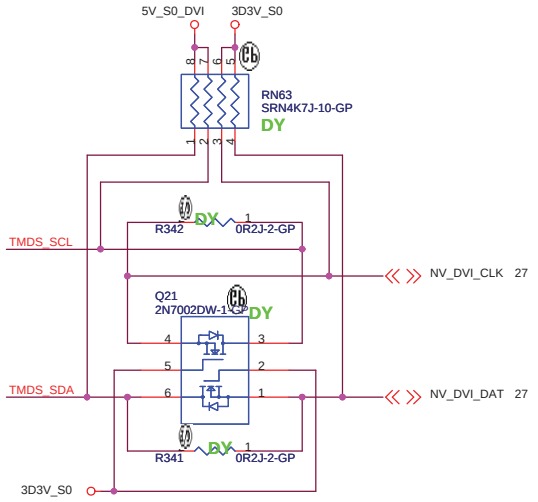
Title: AD / BATT conn.		
Size: A3	Document Number: Dallen	Rev: -1
Date: Tuesday, February 13, 2007	Sheet 41 of 43	





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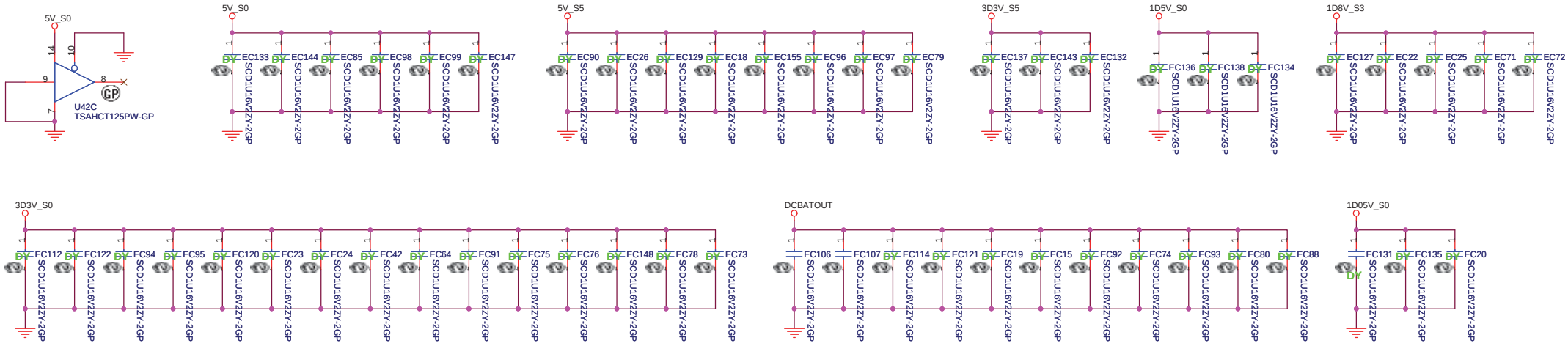
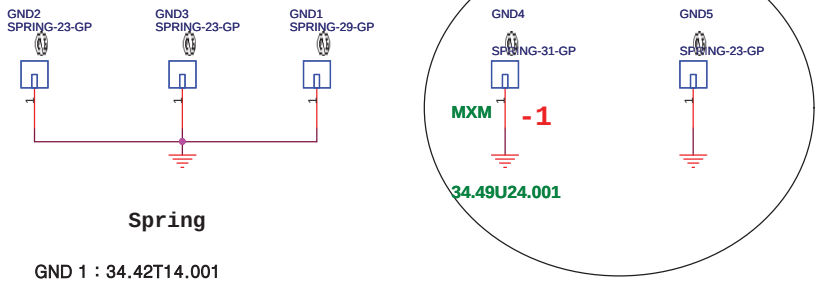
Title	DVI connector	
Size A3	Document Number Dallen	Rev -1
Date: Tuesday, February 13, 2007	Sheet 42 of 43	

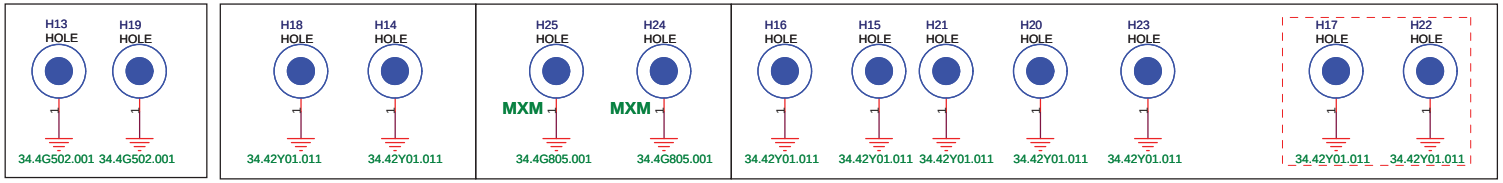


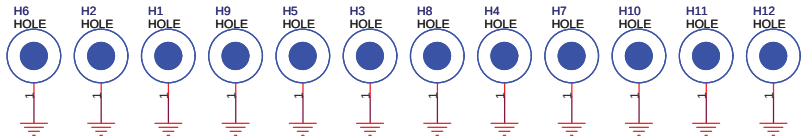


Spring

GND 1 : 34.42T14.001
GND 2/3 : 34.39S07.003

MINI CARD





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Title	***EMI / Spring / Boss***	
Size A3	Document Number **Dallen**	Rev **-1**
Date: Tuesday, February 13, 2007	Sheet 43 of 43	