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ICL50/51, ICK70/71 Schematics Document

Intel Merom Processor with Crestline(PM965/GM965) + DDRII + ICH8M
(With ATI MXM/B)

2007-8-15

REV:2.0

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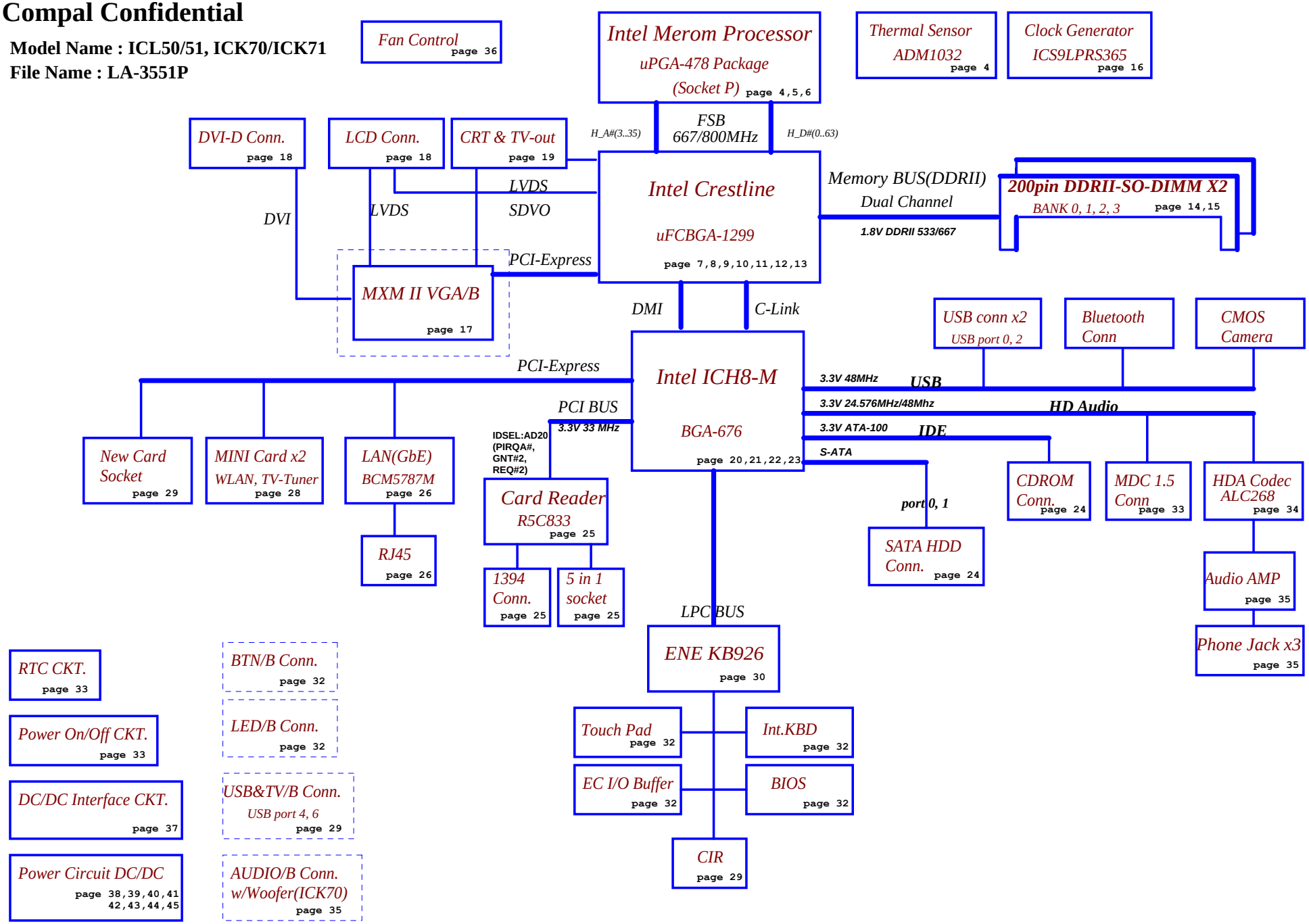
Model Name : ICL50/51, ICK70/ICK71
File Name : LA-3551P



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394/Card Reader	AD16	0	PIRQE
			PIRQG

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	1A(Nettiling)
5	1A(Acadia 960)
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	PM@
UMA	GM@

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Title: Notes List

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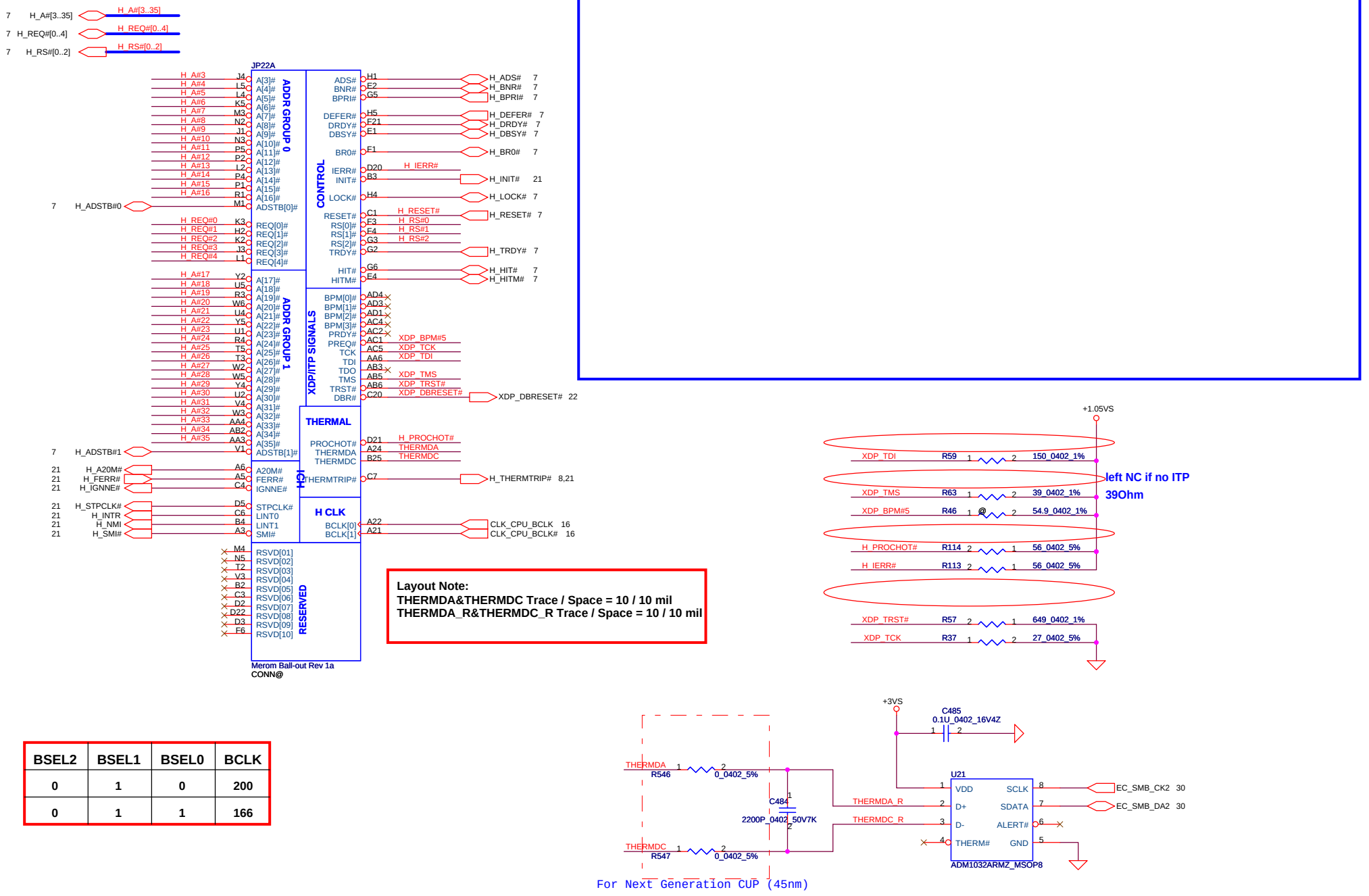

Layout Note:
THERMDA&THERMDC Trace / Space = 10 / 10 mil
THERMDA_R&THERMDC_R Trace / Space = 10 / 10 mil

BSEL2	BSEL1	BSEL0	BCLK
0	1	0	200
0	1	1	166

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Title: Merom (1/3)

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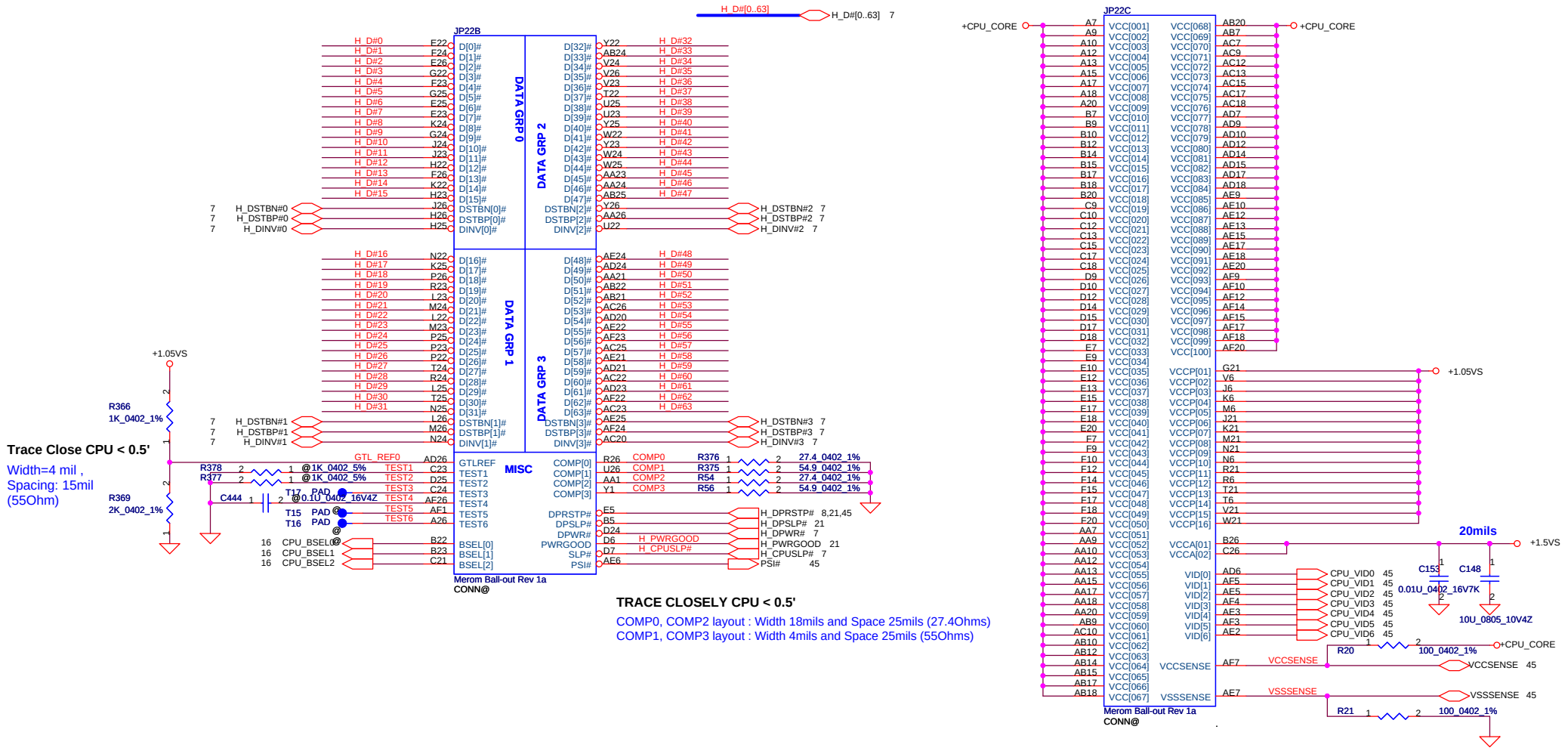

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Title: Merom (2/3)

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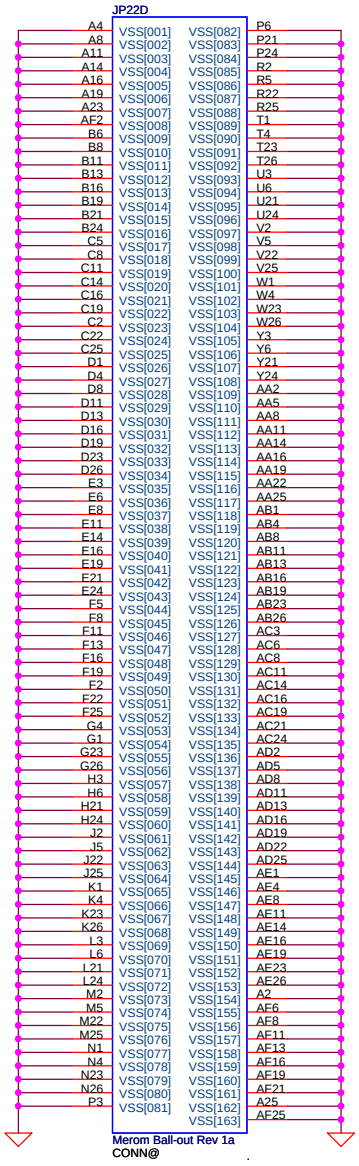

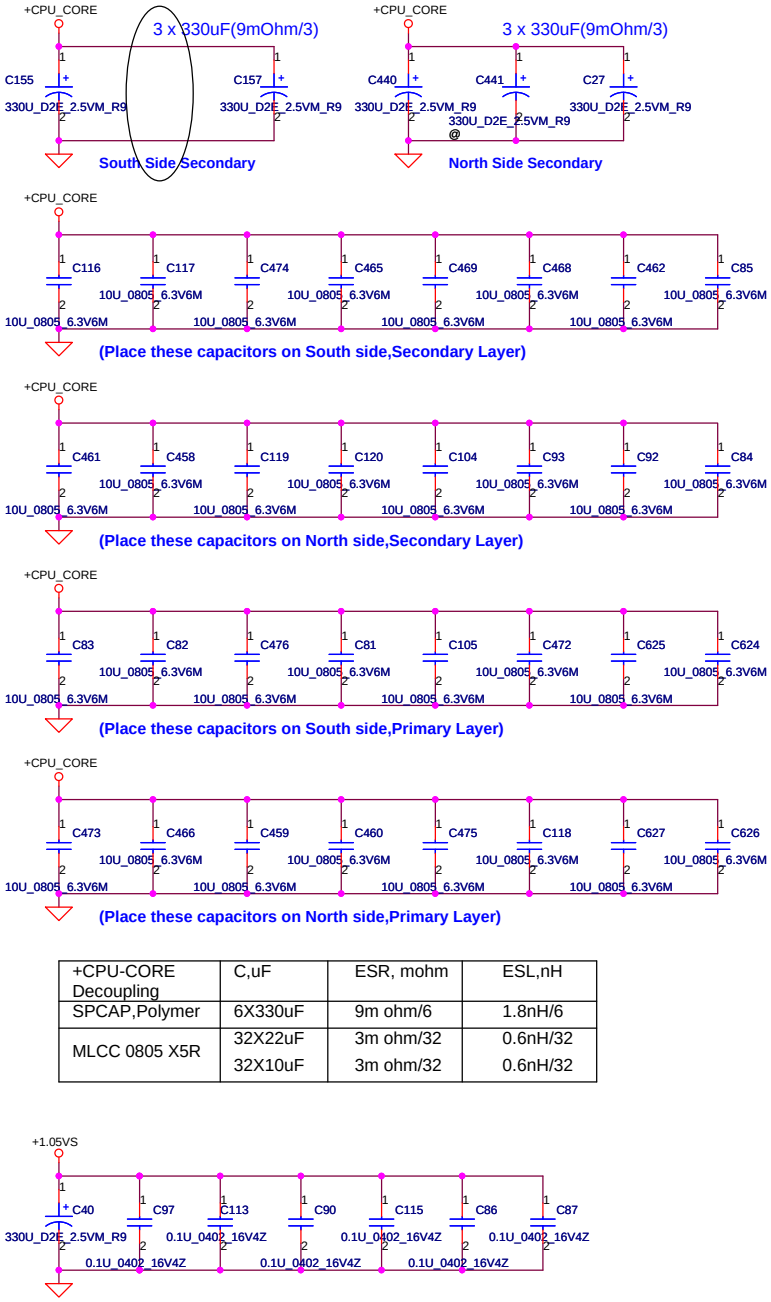

+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32

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Title: Merom (3/3)

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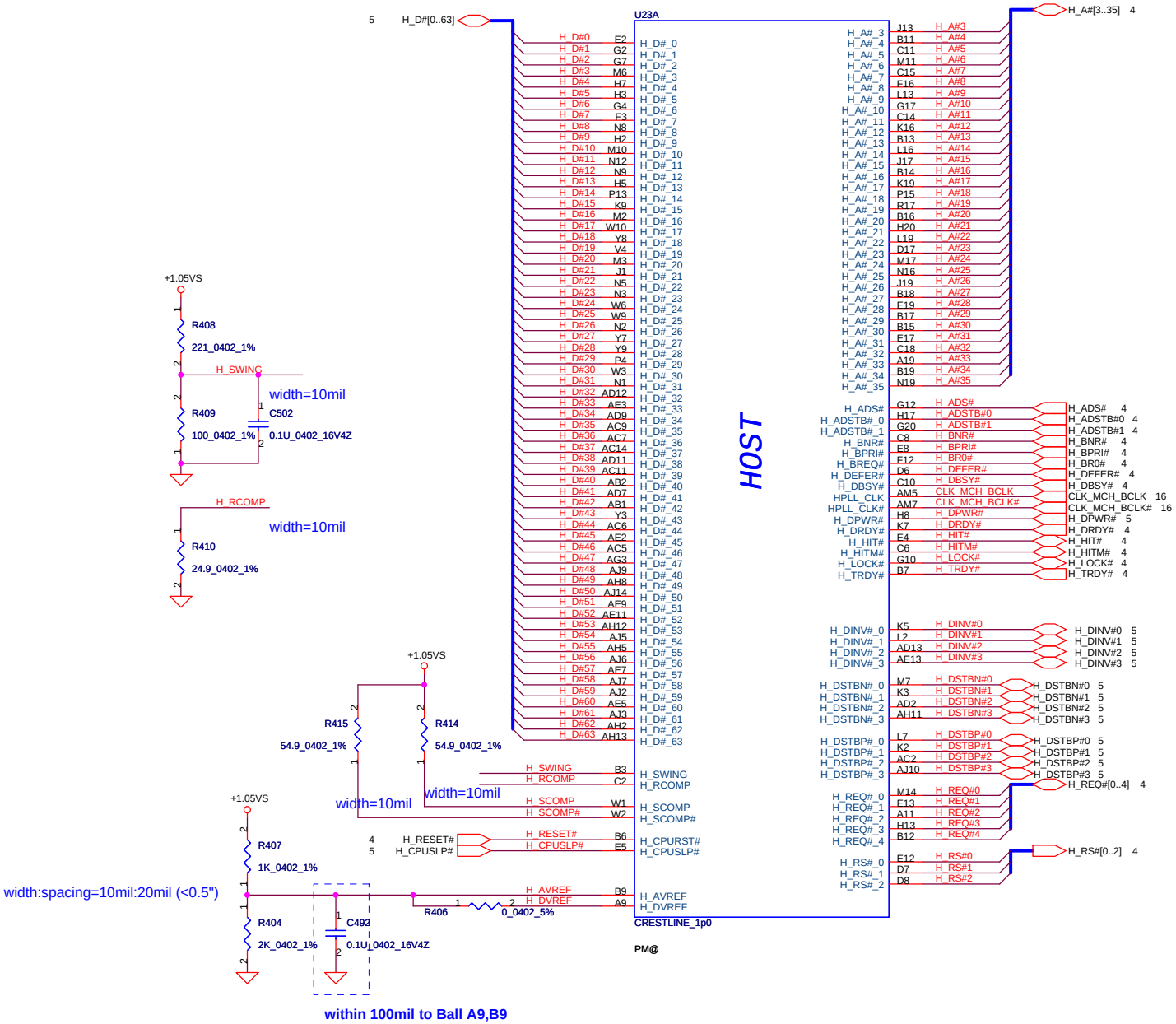

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Title: Crestline GMCH(1/7)-GTL

Size	Document Number	Rev
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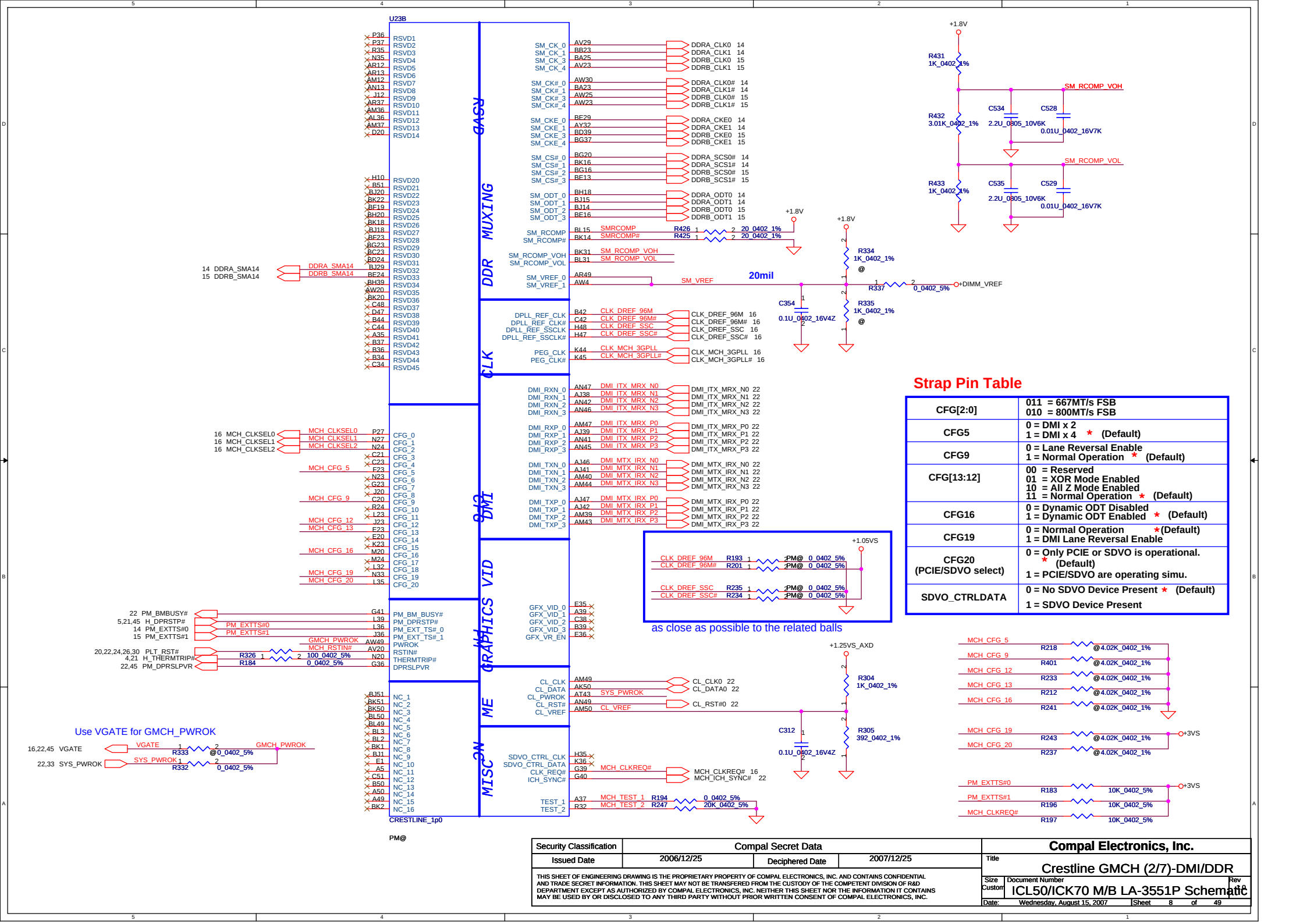

Strap Pin Table

CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present

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Title: Crestline GMCH (2/7)-DMI/DDR

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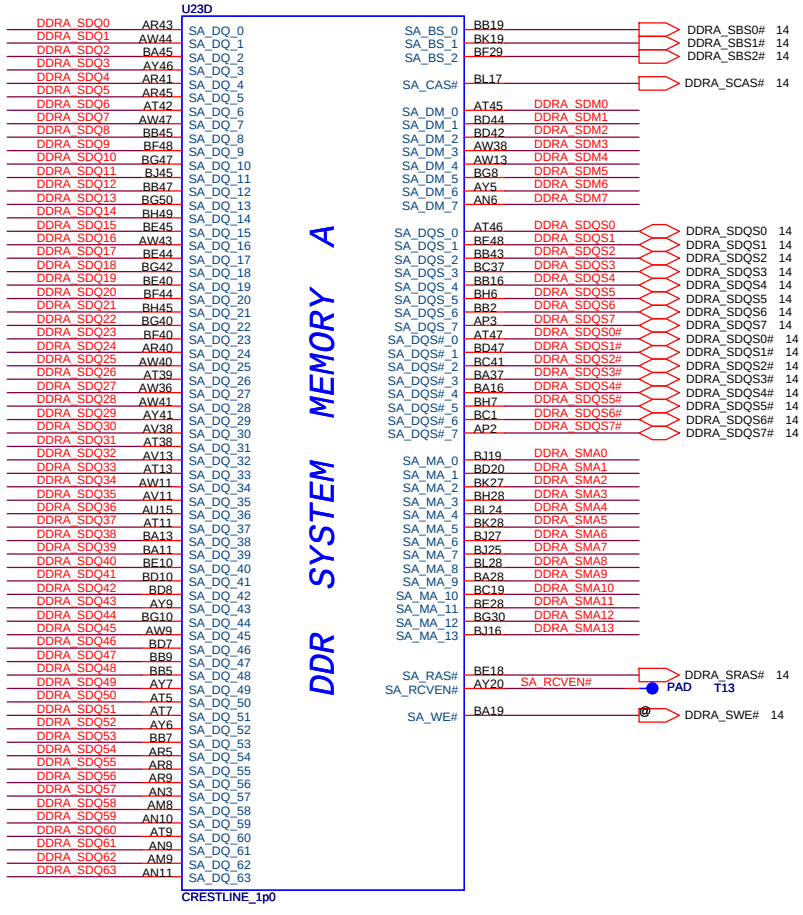
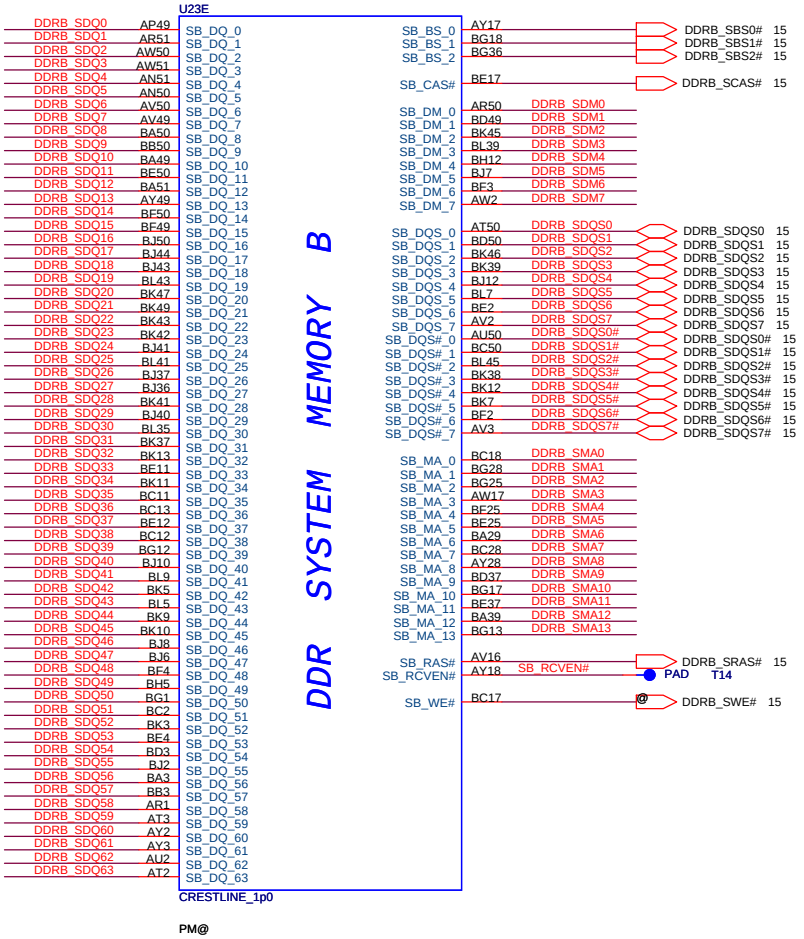
14 DDRA_SDQ[0..63] → DDRA_SDQ[0..63]
14 DDRA_SDM[0..7] → DDRA_SDM[0..7]
14 DDRA_SMA[0..13] → DDRA_SMA[0..13]

15 DDRB_SDQ[0..63] → DDRB_SDQ[0..63]
15 DDRB_SDM[0..7] → DDRB_SDM[0..7]
15 DDRB_SMA[0..13] → DDRB_SMA[0..13]





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Title: Crestline GMCH (3/7)-DDRII

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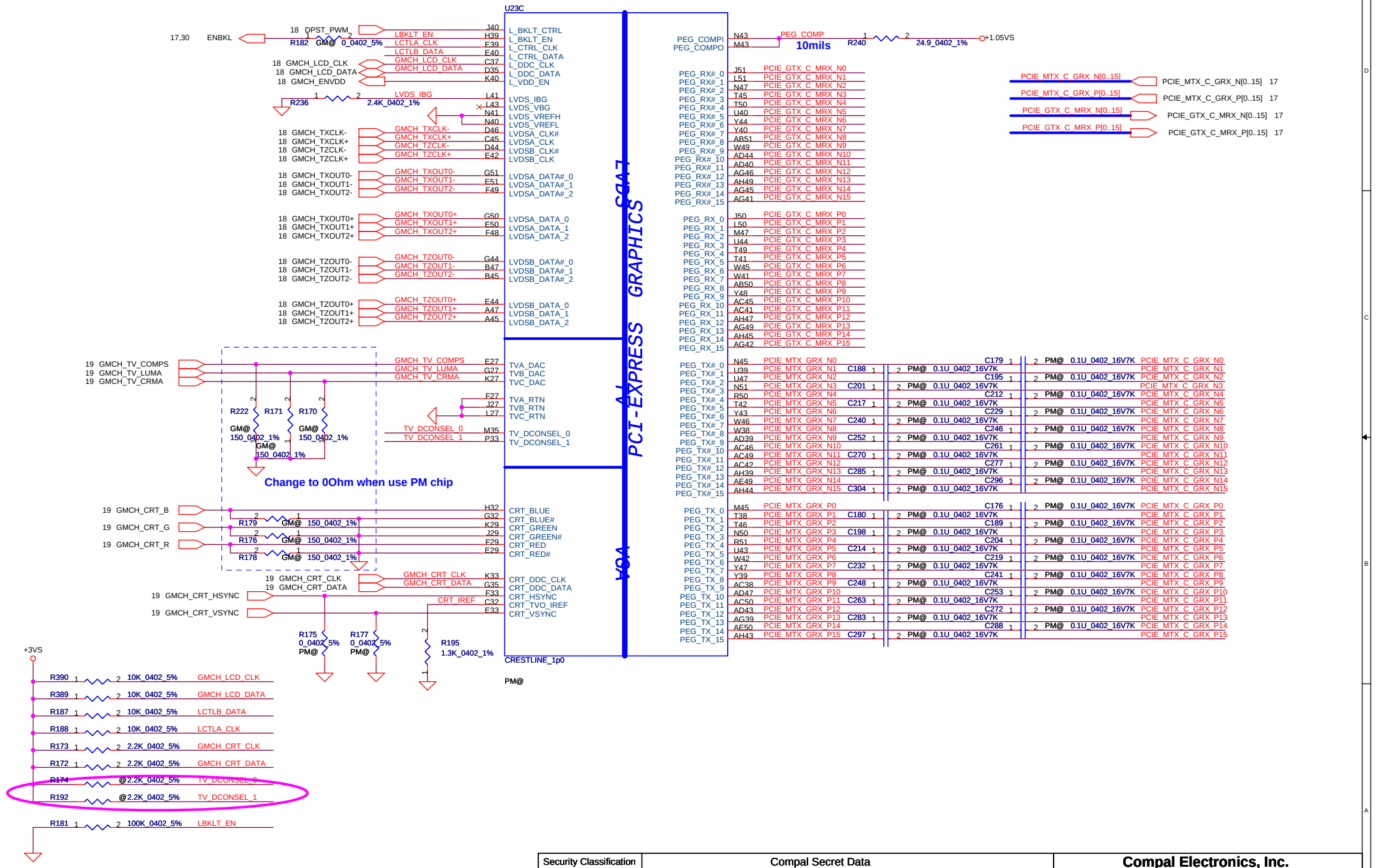

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Title: Crestline GMCH (4/7)-VGA/LVDS/TV

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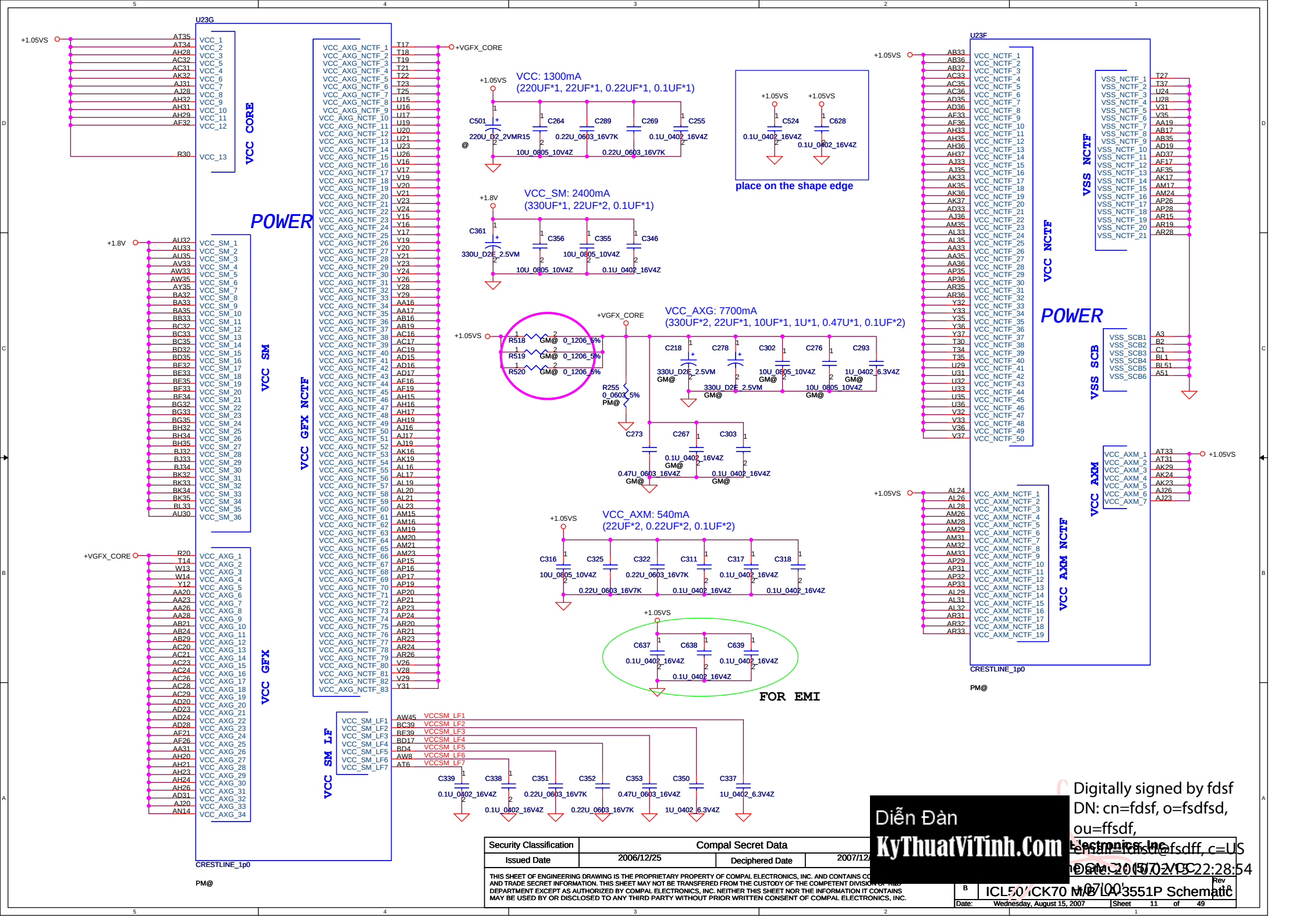
U23G
POWER
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC_CORE_1
VCC_CORE_2
VCC_CORE_3
VCC_CORE_4
VCC_CORE_5
VCC_CORE_6
VCC_CORE_7
VCC_CORE_8
VCC_CORE_9
VCC_CORE_10
VCC_CORE_11
VCC_CORE_12
VCC_CORE_13
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
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VCC_SM_34
VCC_SM_35
VCC_SM_36
VCC_AXG_1
VCC_AXG_2
VCC_AXG_3
VCC_AXG_4
VCC_AXG_5
VCC_AXG_6
VCC_AXG_7
VCC_AXG_8
VCC_AXG_9
VCC_AXG_10
VCC_AXG_11
VCC_AXG_12
VCC_AXG_13
VCC_AXG_14
VCC_AXG_15
VCC_AXG_16
VCC_AXG_17
VCC_AXG_18
VCC_AXG_19
VCC_AXG_20
VCC_AXG_21
VCC_AXG_22
VCC_AXG_23
VCC_AXG_24
VCC_AXG_25
VCC_AXG_26
VCC_AXG_27
VCC_AXG_28
VCC_AXG_29
VCC_AXG_30
VCC_AXG_31
VCC_AXG_32
VCC_AXG_33
VCC_AXG_34
VCC_SM_LF1
VCC_SM_LF2
VCC_SM_LF3
VCC_SM_LF4
VCC_SM_LF5
VCC_SM_LF6
VCC_SM_LF7
VCC_AXG_NCTF_1
VCC_AXG_NCTF_2
VCC_AXG_NCTF_3
VCC_AXG_NCTF_4
VCC_AXG_NCTF_5
VCC_AXG_NCTF_6
VCC_AXG_NCTF_7
VCC_AXG_NCTF_8
VCC_AXG_NCTF_9
VCC_AXG_NCTF_10
VCC_AXG_NCTF_11
VCC_AXG_NCTF_12
VCC_AXG_NCTF_13
VCC_AXG_NCTF_14
VCC_AXG_NCTF_15
VCC_AXG_NCTF_16
VCC_AXG_NCTF_17
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VCC_AXG_NCTF_40
VCC_AXG_NCTF_41
VCC_AXG_NCTF_42
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VCC_AXG_NCTF_45
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VCC_AXG_NCTF_70
VCC_AXG_NCTF_71
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VCC_AXG_NCTF_73
VCC_AXG_NCTF_74
VCC_AXG_NCTF_75
VCC_AXG_NCTF_76
VCC_AXG_NCTF_77
VCC_AXG_NCTF_78
VCC_AXG_NCTF_79
VCC_AXG_NCTF_80
VCC_AXG_NCTF_81
VCC_AXG_NCTF_82
VCC_AXG_NCTF_83
CRESTLINE_1p0
PM@
+1.05VS
+1.8V
+VGFX_CORE
VCC: 1300mA
(220UF*1, 22UF*1, 0.22UF*1, 0.1UF*1)
C501 220U_D2_2VMR15 @
C264 0.22U_0603_16V7K
C289 10U_0805_10V4Z
C269 0.22U_0603_16V7K
C255 0.1U_0402_16V4Z
C524 0.1U_0402_16V4Z
C628 0.1U_0402_16V4Z
place on the shape edge
VCC_SM: 2400mA
(330UF*1, 22UF*2, 0.1UF*1)
C361 330U_D2E_2.5VM
C356 10U_0805_10V4Z
C355 10U_0805_10V4Z
C346 0.1U_0402_16V4Z
VCC_AXG: 7700mA
(330UF*2, 22UF*1, 10UF*1, 1U*1, 0.47U*1, 0.1UF*2)
R518 GM@ 0_1206_5%
R519 GM@ 0_1206_5%
R520 GM@ 0_1206_5%
R255 0_0603_5% PM@
C218 330U_D2E_2.5VM GM@
C278 330U_D2E_2.5VM GM@
C302 10U_0805_10V4Z GM@
C276 10U_0805_10V4Z GM@
C293 1U_0402_6.3V4Z GM@
C273 0.47U_0603_16V4Z GM@
C267 0.1U_0402_16V4Z GM@
C303 0.1U_0402_16V4Z GM@
VCC_AXM: 540mA
(22UF*2, 0.22UF*2, 0.1UF*2)
C316 10U_0805_10V4Z
C325 0.22U_0603_16V7K
C322 0.22U_0603_16V7K
C311 0.1U_0402_16V4Z
C317 0.1U_0402_16V4Z
C318 0.1U_0402_16V4Z
C637 0.1U_0402_16V4Z
C638 0.1U_0402_16V4Z
C639 0.1U_0402_16V4Z
FOR EMI
C339 0.1U_0402_16V4Z
C338 0.1U_0402_16V4Z
C351 0.22U_0603_16V7K
C352 0.22U_0603_16V7K
C353 0.47U_0603_16V4Z
C350 1U_0402_6.3V4Z
C337 1U_0402_6.3V4Z
U23F
POWER
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
VCC_NCTF_1
VCC_NCTF_2
VCC_NCTF_3
VCC_NCTF_4
VCC_NCTF_5
VCC_NCTF_6
VCC_NCTF_7
VCC_NCTF_8
VCC_NCTF_9
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VCC_NCTF_42
VCC_NCTF_43
VCC_NCTF_44
VCC_NCTF_45
VCC_NCTF_46
VCC_NCTF_47
VCC_NCTF_48
VCC_NCTF_49
VCC_NCTF_50
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VCC_AXM_NCTF_4
VCC_AXM_NCTF_5
VCC_AXM_NCTF_6
VCC_AXM_NCTF_7
VCC_AXM_NCTF_8
VCC_AXM_NCTF_9
VCC_AXM_NCTF_10
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Compal Electronics, Inc.
ICL50/CK70 M/B LA-3551P Schematic
Rev 1.0
Date: Wednesday, August 15, 2007
Sheet 11 of 49
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Date: 2010.02.15 22:28:54 +07'00'
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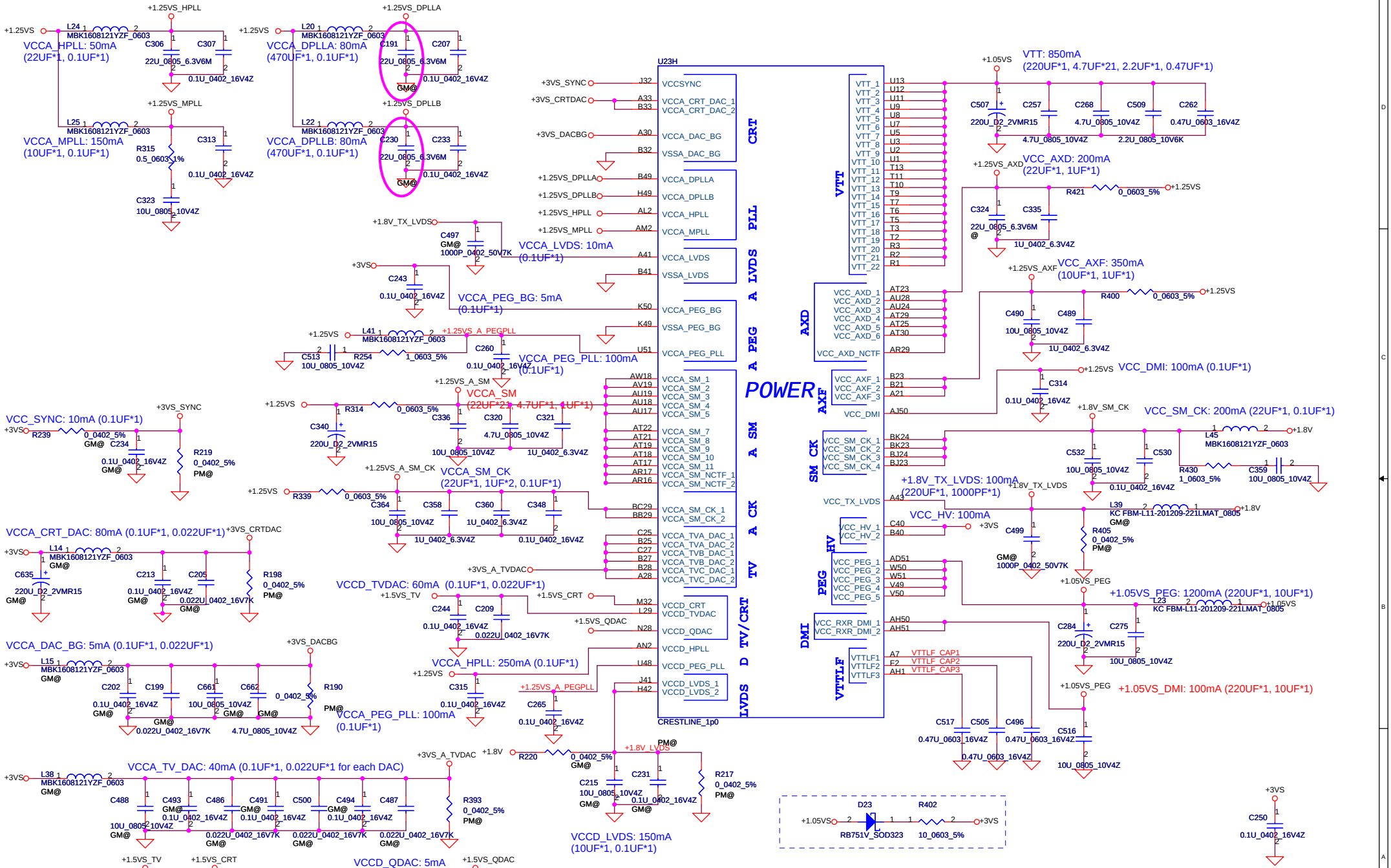
KyThuatViTinh.Com



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: Crestline GMCH (6/7)-VCC

Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematic	1.0

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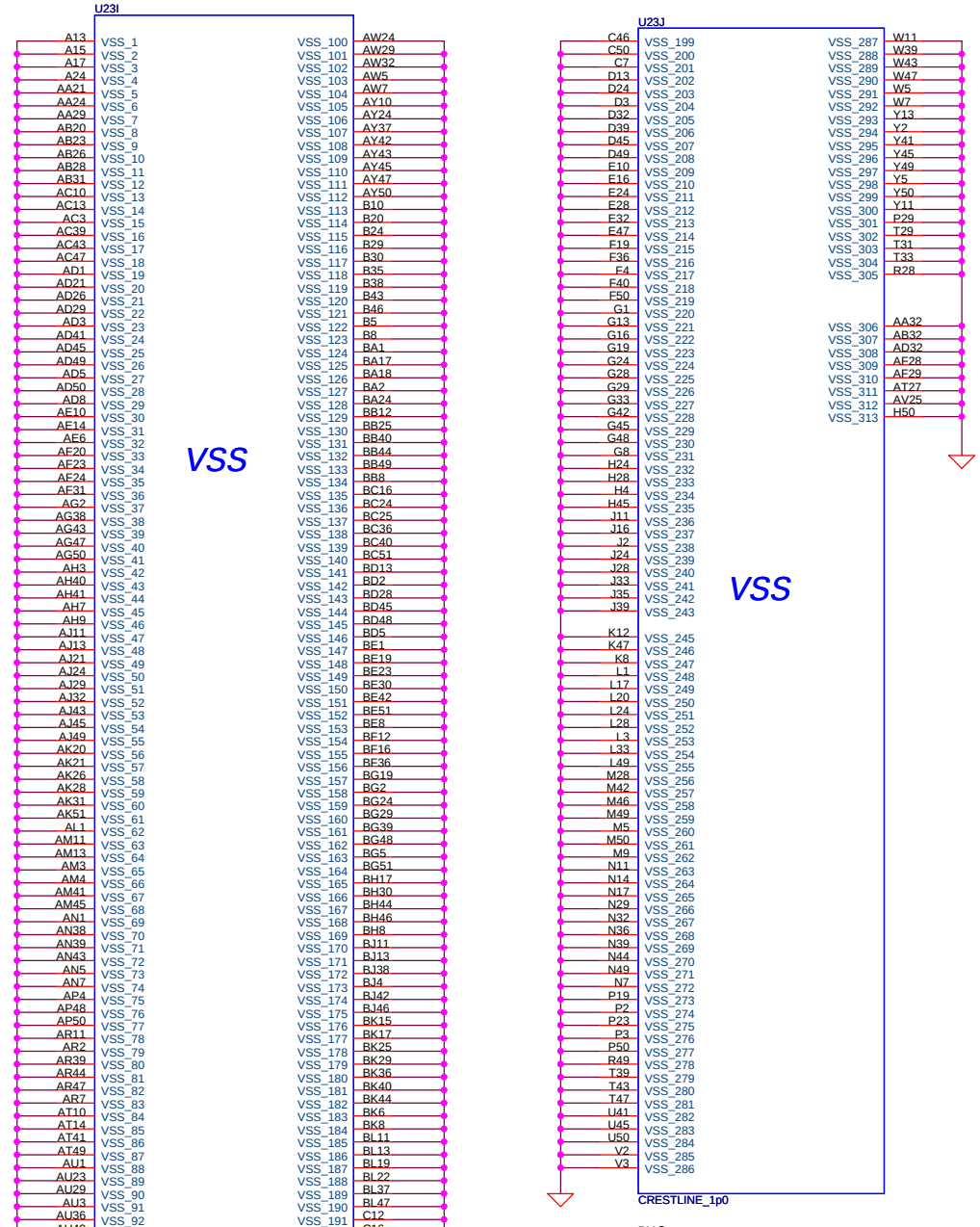

Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title	Crestline GMCH (7/7)-GND
Size	B
Document Number	ICL50/ICK70 M/B LA-3551P Schematic
Rev	1.0
Date:	Wednesday, August 15, 2007
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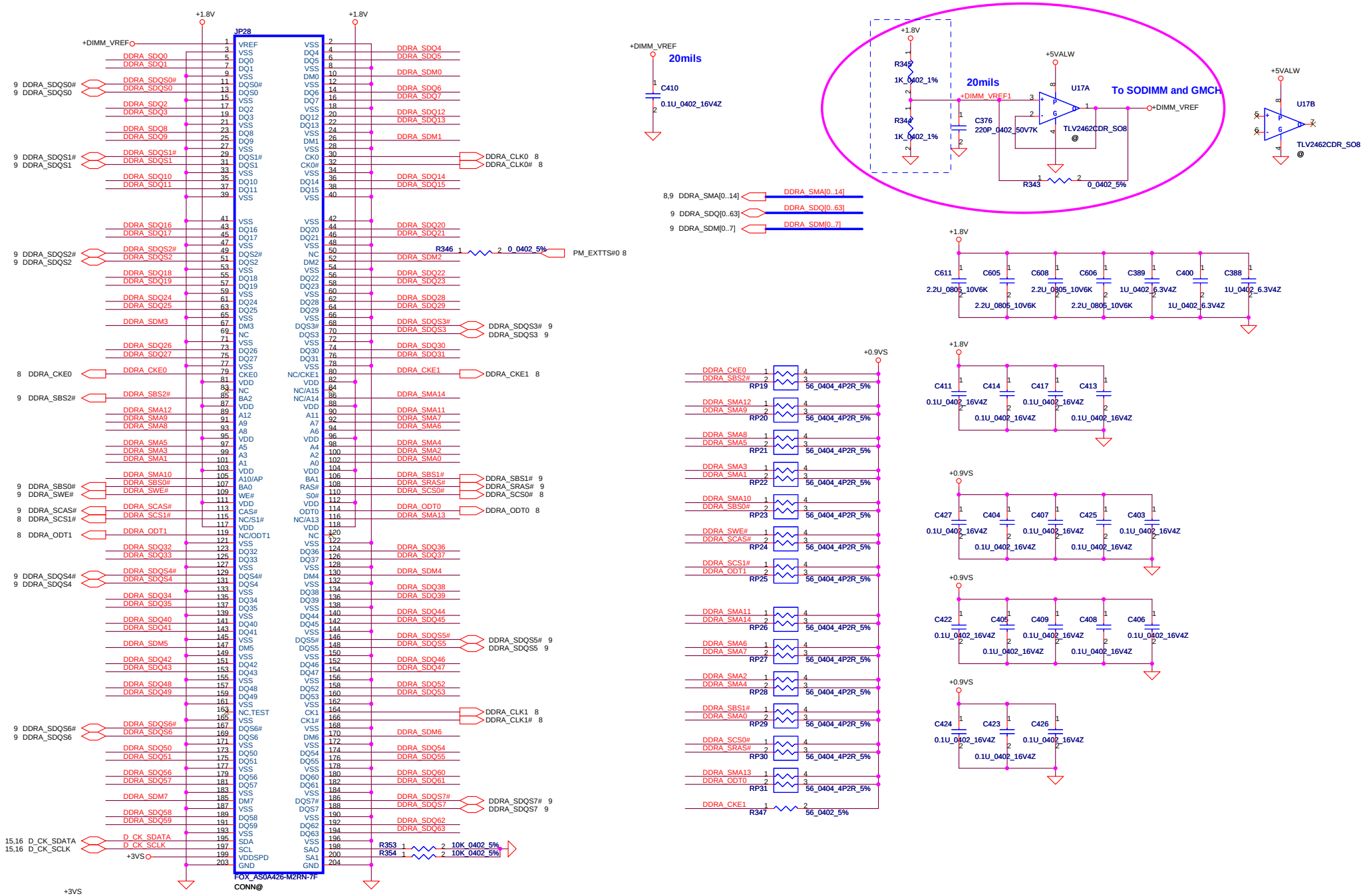

DIMM0 REV H:5.2mm (BOT)

Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: DDRII-SODIMM0

Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematic	1.0

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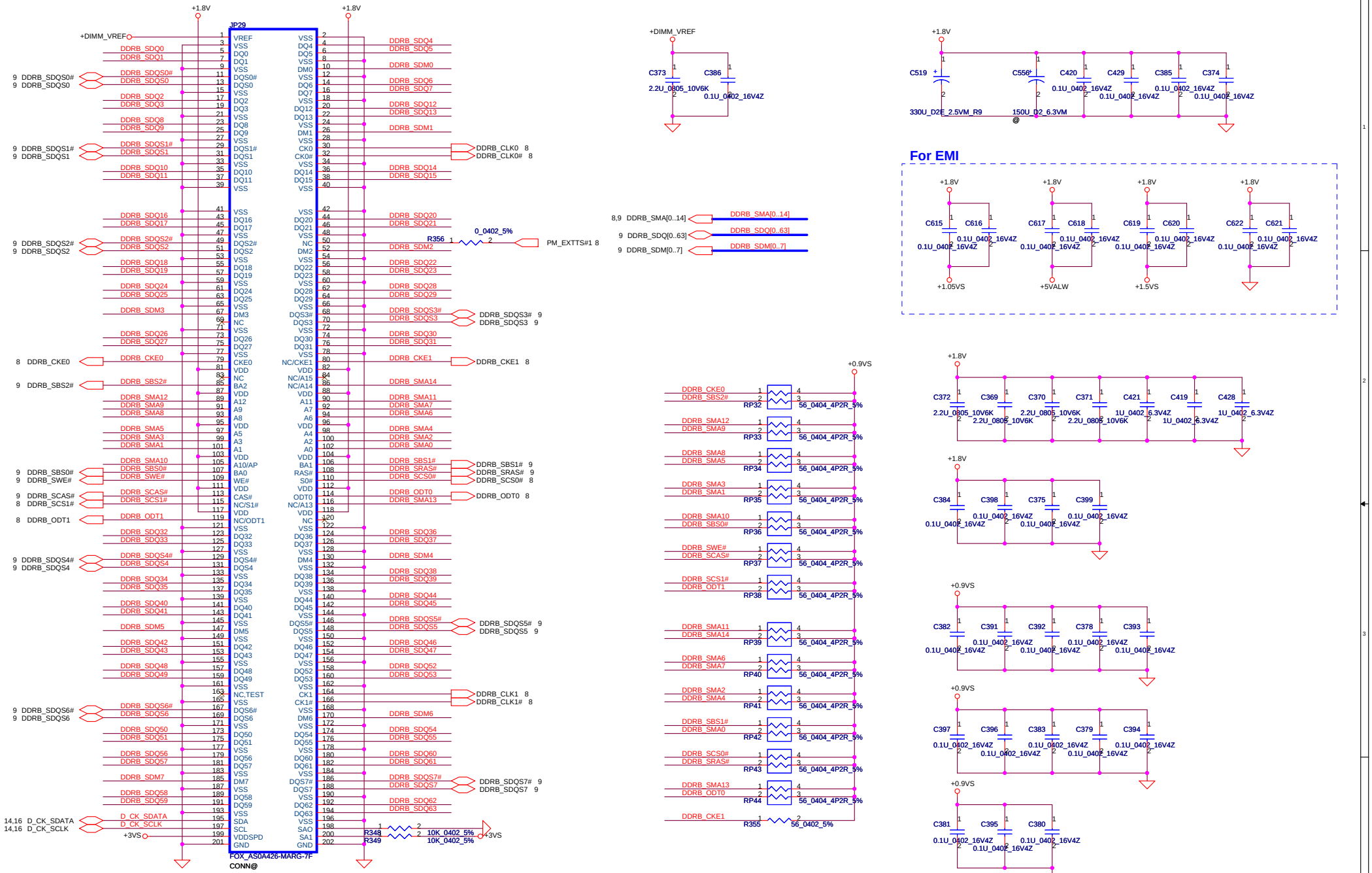

Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title	DDRII-SODIMM1
Size	B
Document Number	ICL50/ICK70 M/B LA-3551P Schematic
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Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR365

CLK_REQ#	Control	Free-Run
CR#_A(WLAN)	PCIEX2	PCIEX0
CR#_B(MCH)	PCIEX4	PCIEX1
CR#_G(NEW CARD)	PCIEX9	
CR#_H(MINI CARDII)	PCIEX10	

SRC6(VGA_CLK): Discrete VGA[Enable] UMA[Disable]

+1.25VS → L10 KC FBM-L11-201209-221LMAT_0805 → +CLK_VDDSRC
C109 10U_0805_10V4Z
C125 10U_0805_10V4Z
C47 C49 C46 C102 C103 C100 0.1U_0402_16V4Z

+3VS → L9 KC FBM-L11-201209-221LMAT_0805 → +CLK_VDD
C79 10U_0805_10V4Z
C51 10U_0805_10V4Z
C44 C45 C48 C99 C98 C101 0.1U_0402_16V4Z

mount to Enable ITP_CLK

+3VS
R104 10K_0402_5% CLK_PCI2
CLK_PCI2=1, Trusted Mode Enable(No overclocking allowed)
R106 @10K_0402_5%
mount to Enable ITP_CLK
R107 10K_0402_5% CLK_PCI5
CLK_PCI5=0, Pin46,47is SRC_CLK
CLK_PCI5=1, Pin46,47is ITP_CLK
R91 10K_0402_5% CLK_PCI4
CLK_PCI4=0, Pin17,18 is SRC_CLK
Pin13,14 is DOT96_CLK
R22 @10K_0402_5% CK_PWRGD

+3VS R47 4.7K_0402_5% → D_CK_SDATA
22,26,28,29 ICH_SMBDATA — Q8 2N7002_SOT23
+3VS R27 4.7K_0402_5% → D_CK_SCLK
22,26,28,29 ICH_SMBCLK — Q7 2N7002_SOT23

+1.05VS
R92 @56_0402_5%
R81 2.2K_0402_5% CLKSEL0
R110 1K_0402_5% → MCH_CLKSEL0 8
R100 @1K_0402_5%
R99 0_0402_5% → CPU_BSEL0 5

+1.05VS
R372 @1K_0402_5%
CLKSEL1
R370 1K_0402_5% → MCH_CLKSEL1 8
R373 @0_0402_5%
R371 0_0402_5% → CPU_BSEL1 5

+1.05VS
R363 @1K_0402_5%
R36 10K_0402_5% CLKSEL2
R362 1K_0402_5% → MCH_CLKSEL2 8
R35 @0_0402_5%
R364 0_0402_5% → CPU_BSEL2 5

+3VS
R25 10K_0402_5% @
CK505_PWRGD
Q5 2N7002_SOT23 @ → CLK_ENABLE# 45

U1 ICS9LPRS365AGLFT_TSSOP64

+CLK_VDD
2 VDDPCI
9 VDD48
16 VDDPLL3
61 VDDREF
39 VDDSRC
55 VDDCPU

+CLK_VDDSRC
12 VDD96_IO
20 VDDPLL3_IO
26 VDDSRC_IO
36 VDDSRC_IO
49 VDDCPU_IO

+3VS R72 10K_0402_5%
28 MINI1_CLKREQ# R76 475_0402_1% → 1 PCI0/CR#_A
8 MCH_CLKREQ# R90 475_0402_1% → 3 PCI1/CR#_B
25 CLK_PCI_1394 CLK_PCI_1394 R105 33_0402_5% CLK_PCI2 → 4 PCI2/TME
30 CLK_PCI_LPC CLK_PCI_LPC R79 33_0402_5% CLK_PCI3 → 5 PCI3
CLK_PCI4 → 6 PCI4/27_Select
20 CLK_PCI_ICH CLK_PCI_ICH R75 33_0402_5% CLK_PCI5 → 7 PCI_F5/ITP_EN

C32 27P_0402_50V8J
CLK_XTALIN → 60 X1
Y1 14.31818MHz_20P_FSX8L14.318181M20FDB
CLK_XTALOUT → 59 X2
C33 27P_0402_50V8J

22 CLK_ICH_48M CLK_ICH_48M R80 33_0402_5% CLKSEL0 → 10 USB_48MHZ/FSLA
CLKSEL1 → 57 FSLB/TEST_MODE
22 CLK_ICH_14M CLK_ICH_14M R43 33_0402_5% CLKSEL2 → 62 REF0/FSLC/TEST_SEL

+CLK_VDDSRC → 45 VDDSRC_IO

42 GNDSRC
8 GNDPCI
11 GND48
15 GND
19 GND
52 GNDCPU
23 GNDSRC
29 GNDSRC
58 GNDREF

NC 48

SCLK 64 D_CK_SCLK → D_CK_SCLK 14,15
SDATA 63 D_CK_SDATA → D_CK_SDATA 14,15

PCI_STOP# 38 PM_STP_PCI# → PM_STP_PCI# 22
CPU_STOP# 37 PM_STP_CPU# → PM_STP_CPU# 22

CPU0 54 CLK_CPU0 R44 0_0402_5% CLK_CPU_BCLK → CLK_CPU_BCLK 4
CPU0# 53 CLK_CPU0# R45 0_0402_5% CLK_CPU_BCLK# → CLK_CPU_BCLK# 4

CPU1_F 51 CLK_CPU1 R31 0_0402_5% CLK_MCH_BCLK → CLK_MCH_BCLK 7
CPU1#_F 50 CLK_CPU1# R32 0_0402_5% CLK_MCH_BCLK# → CLK_MCH_BCLK# 7

SRC8/CPU2_ITP 47 CLK_SRC8 R39 0_0402_5% CLK_PCIE_LAN → CLK_PCIE_LAN 26
SRC8#/CPU2_ITP# 46 CLK_SRC8# R40 0_0402_5% CLK_PCIE_LAN# → CLK_PCIE_LAN# 26

SRC10 34 CLK_SRC10 R53 0_0402_5% CLK_PCIE_MINI2 → CLK_PCIE_MINI2 28
SRC10# 35 CLK_SRC10# R52 0_0402_5% CLK_PCIE_MINI2# → CLK_PCIE_MINI2# 28

SRC11/CR#_H 33 R55 475_0402_1%
SRC11#/CR#_G 32 R97 475_0402_1% → MINI2_CLKREQ# 28, EXP_CLKREQ# 29
R60 10K_0402_5% → +3VS
R103 10K_0402_5% → +3VS

SRC9 30 CLK_SRC9 R73 0_0402_5% CLK_PCIE_CARD → CLK_PCIE_CARD 29
SRC9# 31 CLK_SRC9# R74 0_0402_5% CLK_PCIE_CARD# → CLK_PCIE_CARD# 29

SRC7/CR#_F 44 CLK_SRC7 R33 0_0402_5% CLK_PCIE_SATA → CLK_PCIE_SATA 21
SRC7#/CR#_E 43 CLK_SRC7# R34 0_0402_5% CLK_PCIE_SATA# → CLK_PCIE_SATA# 21

SRC6 41 CLK_SRC6 R41 PM@ 0_0402_5% CLK_PCIE_VGA → CLK_PCIE_VGA 17
SRC6# 40 CLK_SRC6# R42 PM@ 0_0402_5% CLK_PCIE_VGA# → CLK_PCIE_VGA# 17
UMA: disable this pair by BIOS

SRC4 27 CLK_SRC4 R86 0_0402_5% CLK_MCH_3GPLL → CLK_MCH_3GPLL 8
SRC4# 28 CLK_SRC4# R87 0_0402_5% CLK_MCH_3GPLL# → CLK_MCH_3GPLL# 8

SRC3/CR#_C 24 CLK_SRC3 R95 0_0402_5% CLK_PCIE_ICH → CLK_PCIE_ICH 22
SRC3#/CR#_D 25 CLK_SRC3# R96 0_0402_5% CLK_PCIE_ICH# → CLK_PCIE_ICH# 22

SRC2/SATA 21 CLK_SRC2 R84 0_0402_5% CLK_PCIE_MINI1 → CLK_PCIE_MINI1 28
SRC2#/SATA# 22 CLK_SRC2# R85 0_0402_5% CLK_PCIE_MINI1# → CLK_PCIE_MINI1# 28

SRC1/SE1/27MHz_NonSS 17 CLK_SRC1 R93 GM@ 0_0402_5% CLK_DREF_SSC → CLK_DREF_SSC 8
SRC1#/SE2/27MHz_SS 18 CLK_SRC1# R94 GM@ 0_0402_5% CLK_DREF_SSC# → CLK_DREF_SSC# 8

SRC0/DOT96 13 CLK_DOT R82 GM@ 0_0402_5% CLK_DREF_96M → CLK_DREF_96M 8
SRC0#/DOT96# 14 CLK_DOT# R83 GM@ 0_0402_5% CLK_DREF_96M# → CLK_DREF_96M# 8

CK_PWRGD/PD# 56 CK505_PWRGD R29 0_0402_5% → CK_PWRGD 22
R30 @ 0_0402_5% → VGATE 8,22,45

Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

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10 PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]
10 PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
10 PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
10 PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

JP19A

+MXM_B+ 1 PWR_SRC
3 PWR_SRC
5 PWR_SRC
7 PWR_SRC
9 PWR_SRC
11 PWR_SRC
13 PWR_SRC
15 PWR_SRC
17 GND
19 GND
21 GND
23 GND

2 1V8RUN +1.8VS
4 1V8RUN
6 1V8RUN 140mil(3.5A)
8 1V8RUN
10 1V8RUN
12 1V8RUN
14 1V8RUN
16 RUNPWROK VGA_ON 33
18 5VRUN +5VS
20 GND
22 GND
24 GND

PCIE_GTX_C_MRX_N15 25 PEX_RX15# 26 PRSNT2#
PCIE_GTX_C_MRX_P15 27 PEX_RX15 28 PEX_TX15# PCIE_MTX_C_GRX_N15
29 GND 30 PEX_TX15 PCIE_MTX_C_GRX_P15
PCIE_GTX_C_MRX_N14 31 PEX_RX14# 32 GND
PCIE_GTX_C_MRX_P14 33 PEX_RX14 34 PEX_TX14# PCIE_MTX_C_GRX_N14
35 GND 36 PEX_TX14 PCIE_MTX_C_GRX_P14
PCIE_GTX_C_MRX_N13 37 PEX_RX13# 38 GND
PCIE_GTX_C_MRX_P13 39 PEX_RX13 40 PEX_TX13# PCIE_MTX_C_GRX_N13
41 GND 42 PEX_TX13 PCIE_MTX_C_GRX_P13
PCIE_GTX_C_MRX_N12 43 PEX_RX12# 44 GND
PCIE_GTX_C_MRX_P12 45 PEX_RX12 46 PEX_TX12# PCIE_MTX_C_GRX_N12
47 GND 48 PEX_TX12 PCIE_MTX_C_GRX_P12
PCIE_GTX_C_MRX_N11 49 PEX_RX11# 50 GND
PCIE_GTX_C_MRX_P11 51 PEX_RX11 52 PEX_TX11# PCIE_MTX_C_GRX_N11
53 GND 54 PEX_TX11 PCIE_MTX_C_GRX_P11
PCIE_GTX_C_MRX_N10 55 PEX_RX10# 56 GND
PCIE_GTX_C_MRX_P10 57 PEX_RX10 58 PEX_TX10# PCIE_MTX_C_GRX_N10
59 GND 60 PEX_TX10 PCIE_MTX_C_GRX_P10
PCIE_GTX_C_MRX_N9 61 PEX_RX9# 62 GND
PCIE_GTX_C_MRX_P9 63 PEX_RX9 64 PEX_TX9# PCIE_MTX_C_GRX_N9
65 GND 66 PEX_TX9 PCIE_MTX_C_GRX_P9
PCIE_GTX_C_MRX_N8 67 PEX_RX8# 68 GND
PCIE_GTX_C_MRX_P8 69 PEX_RX8 70 PEX_TX8# PCIE_MTX_C_GRX_N8
71 GND 72 PEX_TX8 PCIE_MTX_C_GRX_P8
PCIE_GTX_C_MRX_N7 73 PEX_RX7# 74 GND
PCIE_GTX_C_MRX_P7 75 PEX_RX7 76 PEX_TX7# PCIE_MTX_C_GRX_N7
77 GND 78 PEX_TX7 PCIE_MTX_C_GRX_P7
PCIE_GTX_C_MRX_N6 79 PEX_RX6# 80 GND
PCIE_GTX_C_MRX_P6 81 PEX_RX6 82 PEX_TX6# PCIE_MTX_C_GRX_N6
83 GND 84 PEX_TX6 PCIE_MTX_C_GRX_P6
PCIE_GTX_C_MRX_N5 85 PEX_RX5# 86 GND
PCIE_GTX_C_MRX_P5 87 PEX_RX5 88 PEX_TX5# PCIE_MTX_C_GRX_N5
89 GND 90 PEX_TX5 PCIE_MTX_C_GRX_P5
PCIE_GTX_C_MRX_N4 91 PEX_RX4# 92 GND
PCIE_GTX_C_MRX_P4 93 PEX_RX4 94 PEX_TX4# PCIE_MTX_C_GRX_N4
95 GND 96 PEX_TX4 PCIE_MTX_C_GRX_P4
PCIE_GTX_C_MRX_N3 97 PEX_RX3# 98 GND
PCIE_GTX_C_MRX_P3 99 PEX_RX3 100 PEX_TX3# PCIE_MTX_C_GRX_N3
101 GND 102 PEX_TX3 PCIE_MTX_C_GRX_P3
PCIE_GTX_C_MRX_N2 103 PEX_RX2# 104 GND
PCIE_GTX_C_MRX_P2 105 PEX_RX2 106 PEX_TX2# PCIE_MTX_C_GRX_N2
107 GND 108 PEX_TX2 PCIE_MTX_C_GRX_P2

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JP19B

PCIE_GTX_C_MRX_N1 PCIE_GTX_C_MRX_N1 109 PEX_RX1# 110 GND
PCIE_GTX_C_MRX_P1 PCIE_GTX_C_MRX_P1 111 PEX_RX1 112 PEX_TX1# PCIE_MTX_C_GRX_N1
113 GND 114 PEX_TX1 PCIE_MTX_C_GRX_P1
PCIE_GTX_C_MRX_N0 PCIE_GTX_C_MRX_N0 115 PEX_RX0# 116 GND
PCIE_GTX_C_MRX_P0 PCIE_GTX_C_MRX_P0 117 PEX_RX0 118 PEX_TX0# PCIE_MTX_C_GRX_N0
16 CLK_PCIE_VGA# CLK_PCIE_VGA# 119 GND 120 PEX_TX0 PCIE_MTX_C_GRX_P0
16 CLK_PCIE_VGA CLK_PCIE_VGA 121 PEX_REFCLK# 122 PRSNT1#
123 PEX_REFCLK TV_C/HDTV_Pr 124 VGA_TV_CRMA VGA_TV_CRMA 19
20 PLTRST_VGA# 125 CLK_REQ# 126 GND
127 PEX_RST# TV_Y/HDTV_Y 128 VGA_TV_LUMA VGA_TV_LUMA 19
129 RSVD 130 GND
131 RSVD TV_CVBS/HDTV_Pb 132 VGA_TV_COMPS VGA_TV_COMPS 19
D_EC_SMB_DA1 133 SMB_DAT 134 GND
D_EC_SMB_CK1 135 SMB_CLK VGA_RED 136 VGA_CRT_R VGA_CRT_R 19
137 THERM# 138 GND
19 VGA_CRT_HSYNC VGA_CRT_HSYNC 139 VGA_HSYNC VGA_GRN 140 VGA_CRT_G VGA_CRT_G 19
19 VGA_CRT_VSYNC VGA_CRT_VSYNC 141 VGA_VSYNC 142 GND
19 VGA_DDC_CLK VGA_DDC_CLK 143 DDCA_CLK VGA_BLU 144 VGA_CRT_B VGA_CRT_B 19
19 VGA_DDC_DATA VGA_DDC_DATA 145 DDCA_DAT 146 GND
147 IGP_UCLK# LVDS_UCLK# 148 VGA_TZCLK- VGA_TZCLK- 18
149 IGP_UCLK LVDS_UCLK 150 VGA_TZCLK+ VGA_TZCLK+ 18
151 GND 152 GND
153 RSVD LVDS_UTX3# 154
155 RSVD LVDS_UTX3 156
157 RSVD 158 GND
159 IGP_UTX2# LVDS_UTX2# 160 VGA_TZOUT2- VGA_TZOUT2- 18
161 IGP_UTX2 LVDS_UTX2 162 VGA_TZOUT2+ VGA_TZOUT2+ 18
163 GND 164 GND
165 IGP_UTX1# LVDS_UTX1# 166 VGA_TZOUT1- VGA_TZOUT1- 18
167 IGP_UTX1 LVDS_UTX1 168 VGA_TZOUT1+ VGA_TZOUT1+ 18
169 GND 170 GND
171 IGP_UTX0# LVDS_UTX0# 172 VGA_TZOUT0- VGA_TZOUT0- 18
173 IGP_UTX0 LVDS_UTX0 174 VGA_TZOUT0+ VGA_TZOUT0+ 18
175 GND 176 GND
177 IGP_LCLK#/DVI_B_CLK# LVDS_LCLK# 178 VGA_TXCLK- VGA_TXCLK- 18
179 IGP_LCLK/DVI_B_CLK LVDS_LCLK 180 VGA_TXCLK+ VGA_TXCLK+ 18
181 DVI_B_HPD/GND 182 GND
183 RSVD LVDS_LTX3# 184
185 RSVD LVDS_LTX3 186
187 GND 188 GND
189 IGP_LTX2#/DVI_B_TX2# LVDS_LTX2# 190 VGA_TXOUT2- VGA_TXOUT2- 18
191 IGP_LTX2/DVI_B_TX2 LVDS_LTX2 192 VGA_TXOUT2+ VGA_TXOUT2+ 18
193 GND 194 GND
195 IGP_LTX1#/DVI_B_TX1# LVDS_LTX1# 196 VGA_TXOUT1- VGA_TXOUT1- 18
197 IGP_LTX1/DVI_B_TX1 LVDS_LTX1 198 VGA_TXOUT1+ VGA_TXOUT1+ 18
199 GND 200 GND
201 IGP_LTX0#/DVI_B_TX0# LVDS_LTX0# 202 VGA_TXOUT0- VGA_TXOUT0- 18
203 IGP_LTX0/DVI_B_TX0 LVDS_LTX0 204 VGA_TXOUT0+ VGA_TXOUT0+ 18
205 DVI_A_HPD 206 GND
18 DVI_DET DVI_DET 207 DVI_A_CLK# DDCC_DAT 208 I2CC_SDA I2CC_SDA 18
18 VGA_DVI_TXC- VGA_DVI_TXC- 209 DVI_A_CLK DDCC_CLK 210 I2CC_SCL I2CC_SCL 18
18 VGA_DVI_TXC+ VGA_DVI_TXC+ 211 GND LVDS_PPEN 212 ENVDD ENVDD 18
18 VGA_DVI_TXD2- VGA_DVI_TXD2- 213 DVI_A_TX2# LVDS_BL_BRGHT 214
18 VGA_DVI_TXD2+ VGA_DVI_TXD2+ 215 DVI_A_TX2 LVDS_BLEN 216 ENBKL ENBKL 10,30
217 GND DDCB_DAT 218 VGA_DVI_SDATA VGA_DVI_SDATA 18
18 VGA_DVI_TXD1- VGA_DVI_TXD1- 219 DVI_A_TX1# DDCB_CLK 220 VGA_DVI_SCLK VGA_DVI_SCLK 18
18 VGA_DVI_TXD1+ VGA_DVI_TXD1+ 221 DVI_A_TX1 2V5RUN 222 +2.5VS
223 GND 224
18 VGA_DVI_TXD0- VGA_DVI_TXD0- 225 DVI_A_TX0# 3V3RUN 226 +3VS
18 VGA_DVI_TXD0+ VGA_DVI_TXD0+ 227 DVI_A_TX0 3V3RUN 228
229 GND 3V3RUN 230
231 GND GND 232

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CONN@

+MXM_B+
160mil(4A)
L44 2 1 KC FBM-L11-201209-221LMAT_0805 PM@
L43 2 1 KC FBM-L11-201209-221LMAT_0805 PM@
B+
160mil(4A)
C525 0.1U_0603_25V7K
C526 PM@ 680P_0603_50V7K
C527 68P_0402_50V8J

+2.5VS
C471 0.1U_0402_16V4Z PM@
+5VS
C520 0.1U_0402_16V4Z PM@

+3VS
30,32,41 EC_SMB_DA1 D_EC_SMB_DA1
Q46 PM@ 2N7002_SOT23
30,32,41 EC_SMB_CK1 D_EC_SMB_CK1
Q47 PM@
2N7002_SOT23

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Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: MXM Connector

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

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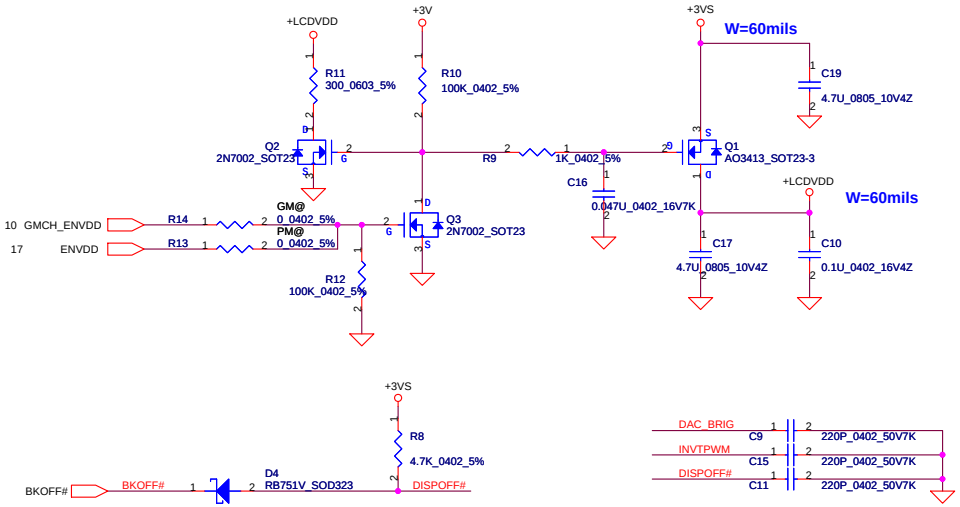
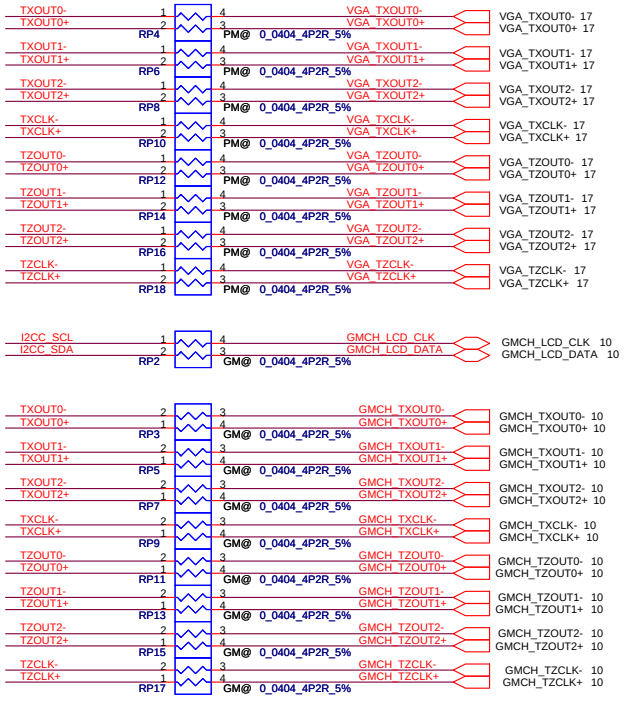
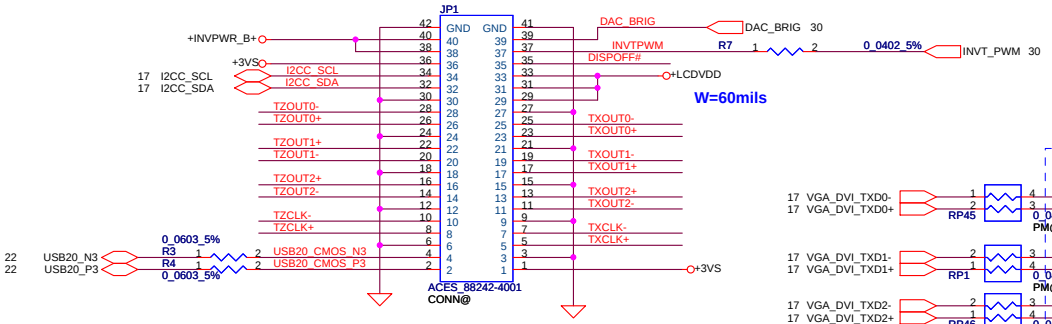
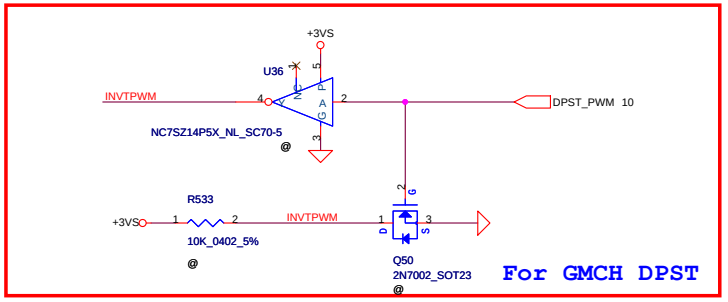
LCD POWER CIRCUIT

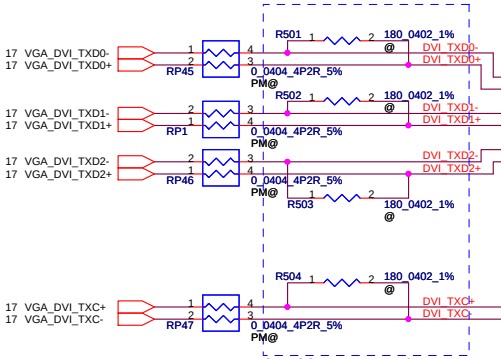


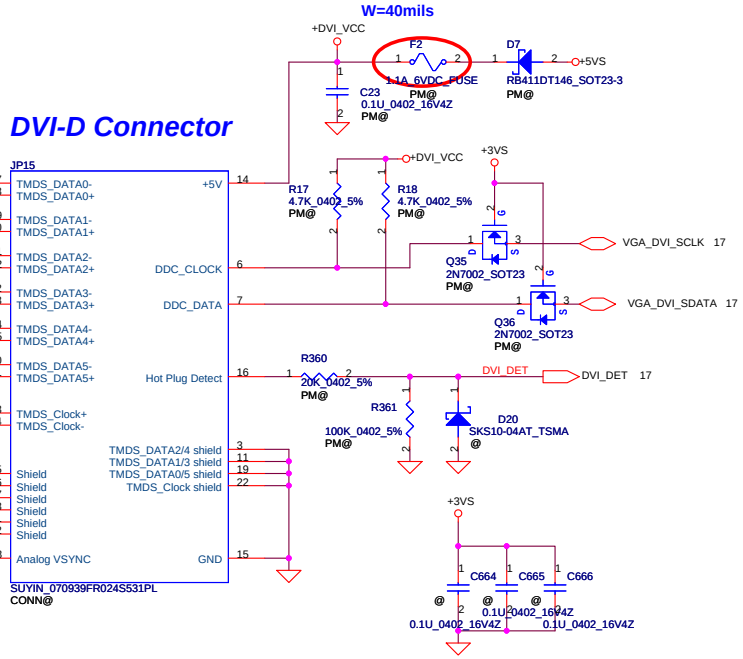


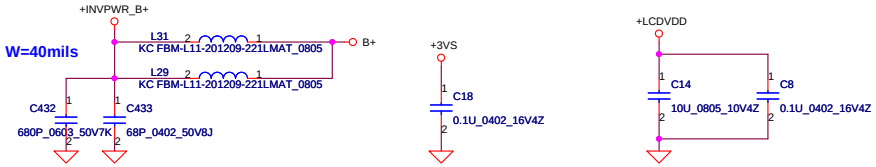
LCD/PANEL BD. Conn.











Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

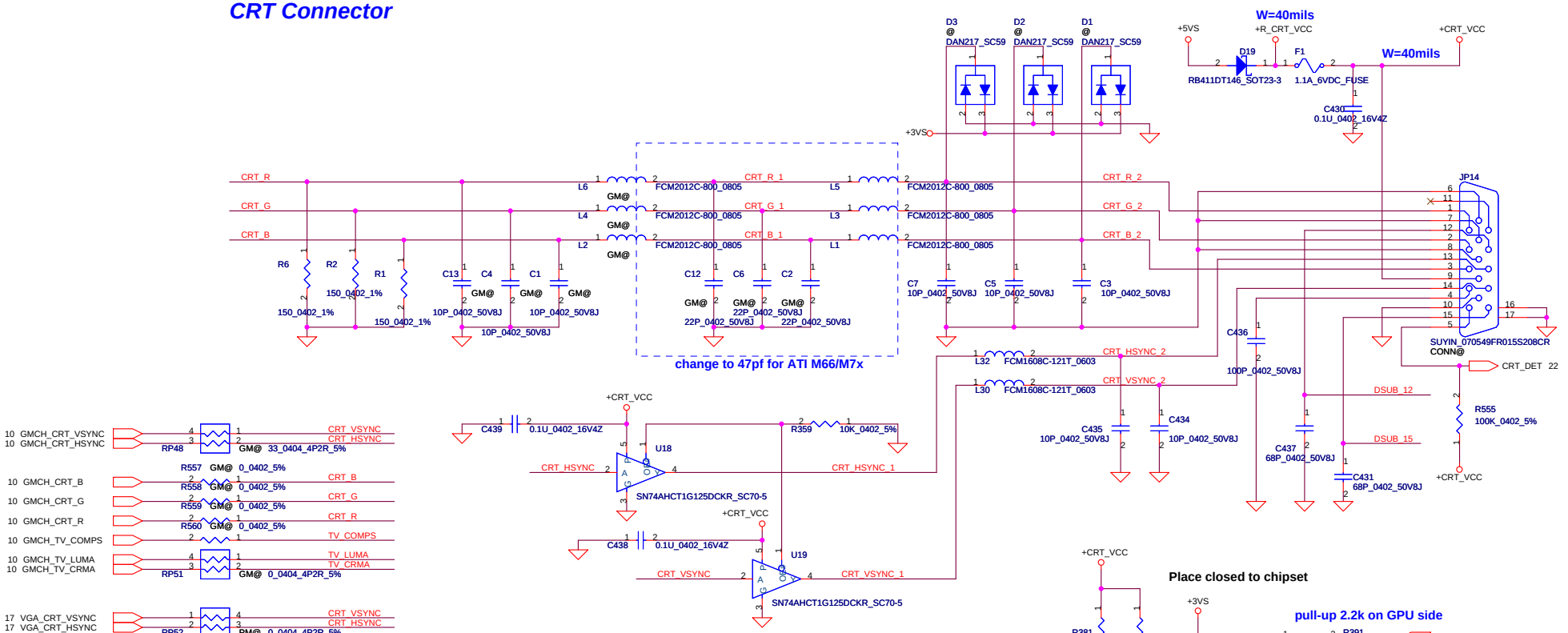
Compal Electronics, Inc.

Title: LVDS & DVI Connector

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

Date: Thursday, August 23, 2007 | Sheet 18 of 49

CRT Connector



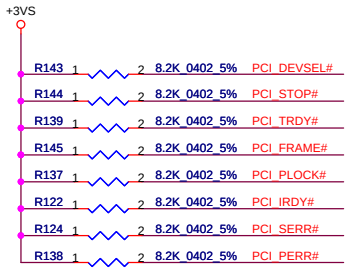
Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

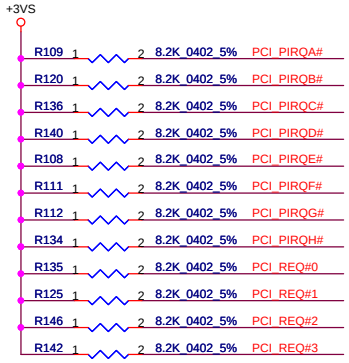
Compal Electronics, Inc.

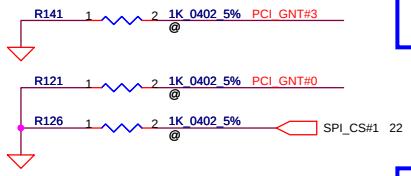
Title: CRT & TV-OUT Connector

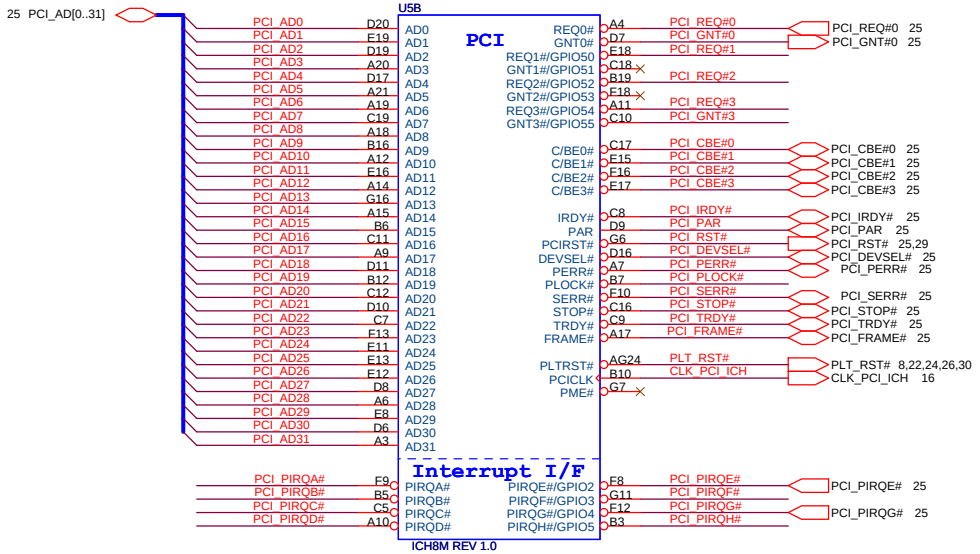
Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematic	1.0

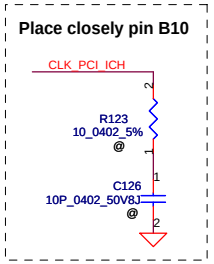
Date: Wednesday, August 15, 2007 | Sheet 19 of 49





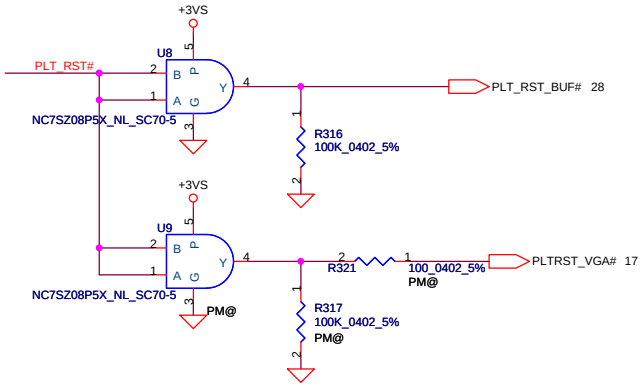






A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*



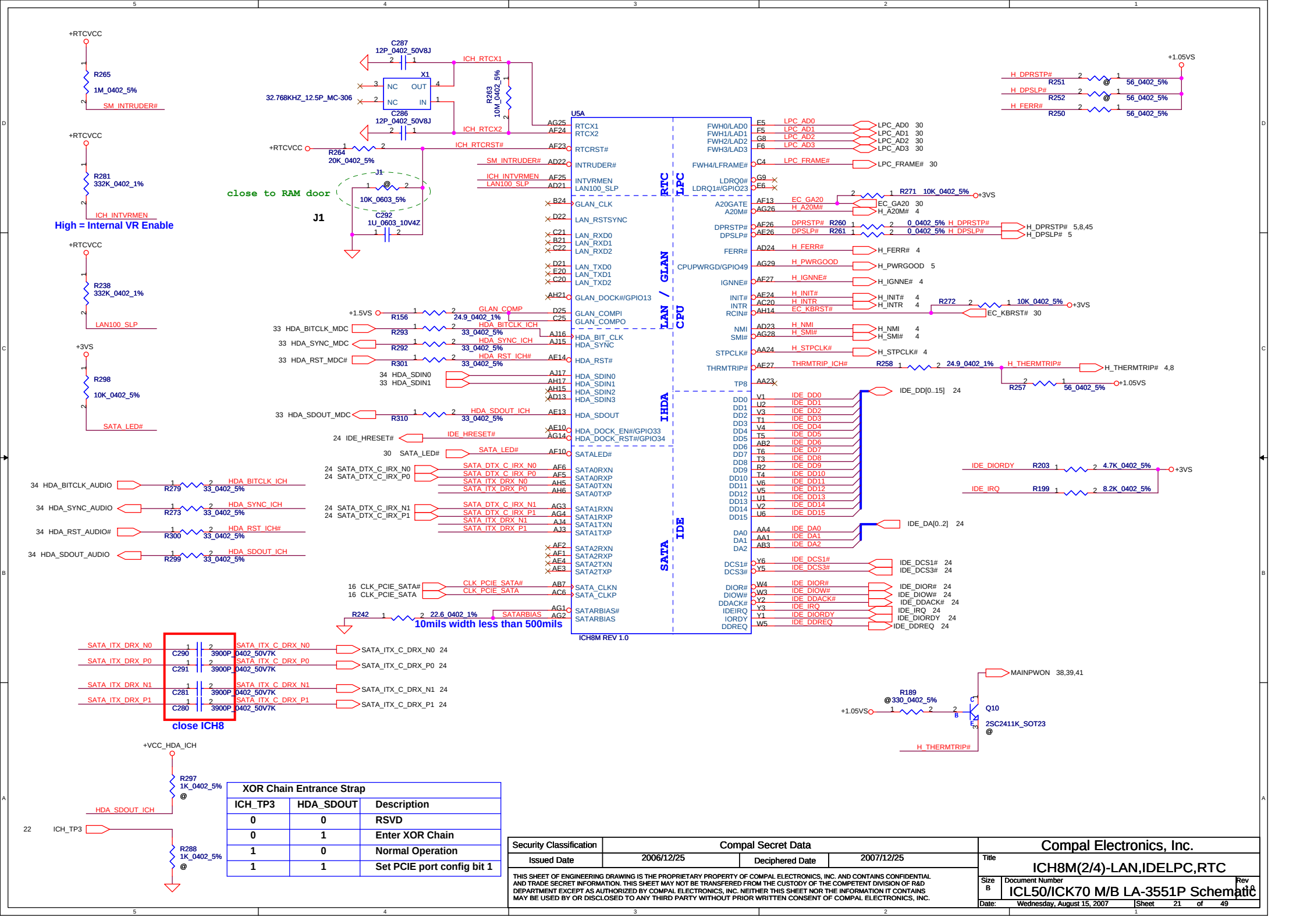
Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: ICH8M(1/4)-PCI

Size | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

Date: Wednesday, August 15, 2007 | Sheet 20 of 49


+RTCVCC
R265
1M_0402_5%
SM_INTRUDER#
High = Internal VR Enable
R281
332K_0402_1%
ICH_INTVRMEN
R238
332K_0402_1%
LAN100_SLP
+3VS
R298
10K_0402_5%
SATA_LED#
C287
12P_0402_50V8J
X1
32.768KHZ_12.5P_MC-306
C286
12P_0402_50V8J
ICH_RTCX1
ICH_RTCX2
R263
10M_0402_5%
R264
20K_0402_5%
ICH_RTCRST#
close to RAM door
J1
10K_0603_5%
C292
1U_0603_10V4Z
U5A
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
RTC
LPC
GLAN
LAN / CPU
HDA
IDE
SATA
ICH8M REV 1.0
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
+1.05VS
H_DPRSTP#
H_DPSLP#
H_FERR#
R251
R252
R250
56_0402_5%
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
R271
10K_0402_5%
EC_GA20
H_A20M#
R260
R261
0_0402_5%
H_DPRSTP
H_DPSLP
H_DPRSTP# 5,8,45
H_DPSLP# 5
H_FERR# 4
H_PWRGOOD
H_PWRGOOD 5
H_IGNNE#
H_IGNNE# 4
H_INIT#
H_INTR
EC_KBRST#
R272
10K_0402_5%
H_NMI
H_SMI#
H_STPCLK#
H_STPCLK# 4
THRMTRIP_ICH#
R258
24.9_0402_1%
H_THERMTRIP#
H_THERMTRIP# 4,8
R257
56_0402_5%
IDE_DD[0..15] 24
IDE_DD0
IDE_DD1
IDE_DD2
IDE_DD3
IDE_DD4
IDE_DD5
IDE_DD6
IDE_DD7
IDE_DD8
IDE_DD9
IDE_DD10
IDE_DD11
IDE_DD12
IDE_DD13
IDE_DD14
IDE_DD15
IDE_DA[0..2] 24
IDE_DA0
IDE_DA1
IDE_DA2
IDE_DCS1#
IDE_DCS3#
IDE_DIOR#
IDE_DIOW#
IDE_DDACK#
IDE_IRQ
IDE_DIORDY
IDE_DDREQ
IDE_DIORDY
R203
4.7K_0402_5%
IDE_IRQ
R199
8.2K_0402_5%
+3VS
R156
24.9_0402_1%
GLAN_COMP
R293
R292
R301
HDA_BITCLK_ICH
HDA_SYNC_ICH
HDA_RST_ICH#
33_0402_5%
R310
HDA_SDOUT_ICH
HDA_BITCLK_MDC
HDA_SYNC_MDC
HDA_RST_MDC#
HDA_SDOUT_MDC
34 HDA_SDIN0
33 HDA_SDIN1
IDE_HRESET#
24 IDE_HRESET#
30 SATA_LED#
SATA_DTX_C_IRX_N0
SATA_DTX_C_IRX_P0
SATA_ITX_DRX_N0
SATA_ITX_DRX_P0
SATA_DTX_C_IRX_N1
SATA_DTX_C_IRX_P1
SATA_ITX_DRX_N1
SATA_ITX_DRX_P1
16 CLK_PCIE_SATA#
16 CLK_PCIE_SATA
CLK_PCIE_SATA#
CLK_PCIE_SATA
R242
22.6_0402_1%
SATARBIAS
10mils width less than 500mils
34 HDA_BITCLK_AUDIO
34 HDA_SYNC_AUDIO
34 HDA_RST_AUDIO#
34 HDA_SDOUT_AUDIO
R279
R273
R300
R299
C290
C291
C281
C280
3900P_0402_50V7K
SATA_ITX_C_DRX_N0
SATA_ITX_C_DRX_P0
SATA_ITX_C_DRX_N1
SATA_ITX_C_DRX_P1
SATA_ITX_C_DRX_N0 24
SATA_ITX_C_DRX_P0 24
SATA_ITX_C_DRX_N1 24
SATA_ITX_C_DRX_P1 24
close ICH8
MAINPWON 38,39,41
R189
@330_0402_5%
Q10
2SC2411K_SOT23
@
+VCC_HDA_ICH
R297
1K_0402_5%
R288
1K_0402_5%
22 ICH_TP3
XOR Chain Entrance Strap
ICH_TP3
HDA_SDOUT
Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation
1 1 Set PCIE port config bit 1
Security Classification
Compal Secret Data
Issued Date
2006/12/25
Deciphered Date
2007/12/25
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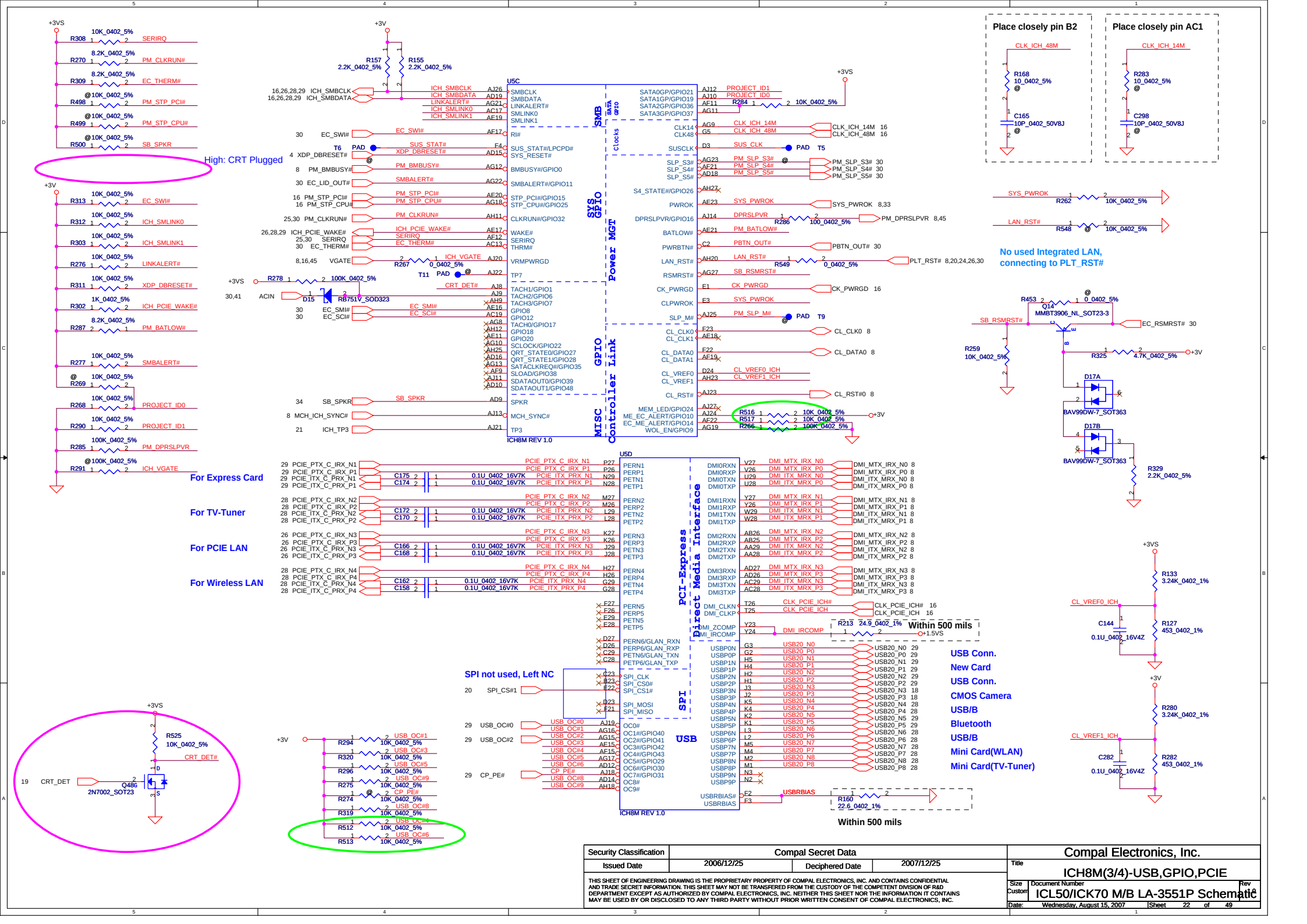
Compal Electronics, Inc.
Title
ICH8M(2/4)-LAN,IDELPC,RTC
Size B
Document Number
ICL50/ICK70 M/B LA-3551P Schematic
Rev 1.0
Date: Wednesday, August 15, 2007
Sheet 21 of 49


Place closely pin B2
Place closely pin AC1
CLK_ICH_48M
CLK_ICH_14M
R168 10_0402_5% @
R283 10_0402_5% @
C165 10P_0402_50V8J @
C298 10P_0402_50V8J @
High: CRT Plugged
SERIRQ
PM_CLKRUN#
EC_THERM#
PM_STP_PCI#
PM_STP_CPU#
SB_SPKR
EC_SWI#
ICH_SMLINK0
ICH_SMLINK1
LINKALERT#
XDP_DBRESET#
ICH_PCIE_WAKE#
PM_BATLOW#
SMBALERT#
PROJECT_ID0
PROJECT_ID1
PM_DPRSLPVR
ICH_VGATE
U5C
ICH8M REV 1.0
SMB
GPIO
Clocks
Power MGT
SYS GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
MEM_LED/GPIO24
ME_EC_ALERT/GPIO10
EC_ME_ALERT/GPIO14
WOL_EN/GPIO9
PROJECT_ID1
PROJECT_ID0
CLK_ICH_14M
CLK_ICH_48M
SUS_CLK
PM_SLP_S3#
PM_SLP_S4#
PM_SLP_S5#
SYS_PWROK
PM_DPRSLPVR
BATLOW#
PBTN_OUT#
LAN_RST#
SB_RSMRST#
CK_PWRGD
SYS_PWROK
PM_SLP_M#
CL_CLK0
CL_DATA0
CL_VREF0_ICH
CL_VREF1_ICH
CL_RST#0
SYS_PWROK
LAN_RST#
No used Integrated LAN, connecting to PLT_RST#
Q14 MMBT3906_NL_SOT23-3
D17A
D17B
BAV99DW-7_SOT363
R329 2.2K_0402_5%
For Express Card
For TV-Tuner
For PCIE LAN
For Wireless LAN
U5D
PCI-Express Direct Media Interface
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6/GLAN_RXN
PERP6/GLAN_RXP
PETN6/GLAN_TXN
PETP6/GLAN_TXP
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
C175 0.1U_0402_16V7K
C174 0.1U_0402_16V7K
C172 0.1U_0402_16V7K
C170 0.1U_0402_16V7K
C166 0.1U_0402_16V7K
C168 0.1U_0402_16V7K
C162 0.1U_0402_16V7K
C158 0.1U_0402_16V7K
R213 24.9_0402_1%
Within 500 mils
R160 22.6_0402_1%
Within 500 mils
SPI not used, Left NC
SPI
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
USB
OC0#
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
OC8#
OC9#
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBP8N
USBP8P
USBP9N
USBP9P
USBRBIAS#
USBRBIAS
USB Conn.
New Card
USB Conn.
CMOS Camera
USB/B
Bluetooth
USB/B
Mini Card(WLAN)
Mini Card(TV-Tuner)
R133 3.24K_0402_1%
R127 453_0402_1%
R280 3.24K_0402_1%
R282 453_0402_1%
C144 0.1U_0402_16V4Z
C282 0.1U_0402_16V4Z
Q486 2N7002_SOT23
R525 10K_0402_5%
CRT_DET
R294 10K_0402_5%
R320 10K_0402_5%
R296 10K_0402_5%
R275 10K_0402_5%
R274 10K_0402_5%
R319 10K_0402_5%
R512 10K_0402_5%
R513 10K_0402_5%
USB_OC#1
USB_OC#3
USB_OC#5
USB_OC#9
CP_PE#
USB_OC#8
USB_OC#4
USB_OC#6
Security Classification
Compal Secret Data
Issued Date
2006/12/25
Deciphered Date
2007/12/25
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Compal Electronics, Inc.
Title
ICH8M(3/4)-USB,GPIO,PCIE
Size
Custom
Document Number
ICL50/ICK70 M/B LA-3551P Schematic
Rev
1.0
Date:
Wednesday, August 15, 2007
Sheet
22
of
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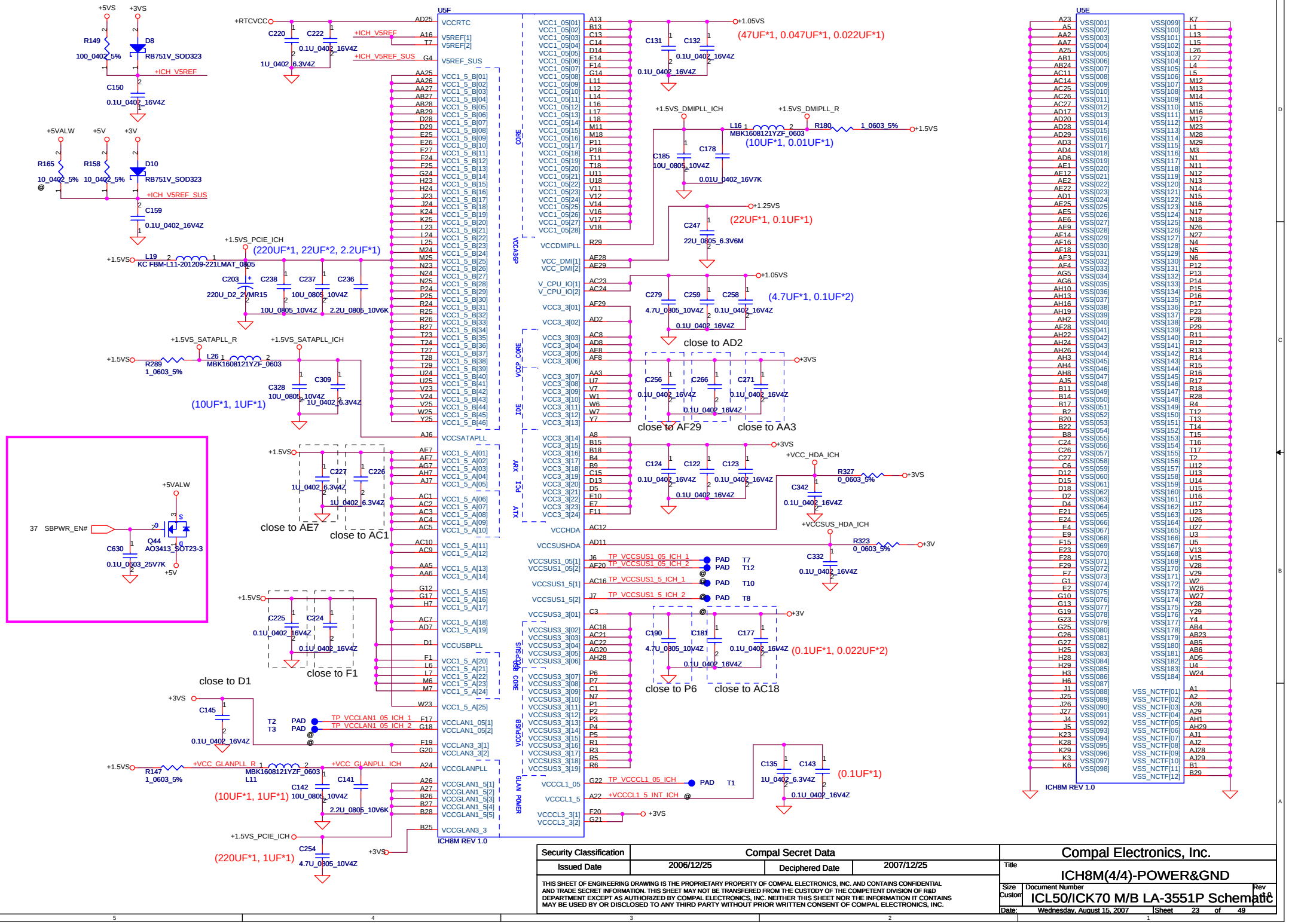
U5F
ICH8M REV 1.0
U5E
ICH8M REV 1.0
close to AD2
close to AF29
close to AA3
close to AE7
close to AC1
close to D1
close to F1
close to P6
close to AC18
(47UF*1, 0.047UF*1, 0.022UF*1)
(10UF*1, 0.01UF*1)
(22UF*1, 0.1UF*1)
(4.7UF*1, 0.1UF*2)
(0.1UF*1, 0.022UF*2)
(220UF*1, 22UF*2, 2.2UF*1)
(10UF*1, 1UF*1)
(220UF*1, 1UF*1)
(0.1UF*1)
+1.05VS
+1.25VS
+1.5VS
+3VS
+3V
+5VS
+5V
+5VALW
+RTCVCC
+1.5VS_DMIPLL_ICH
+1.5VS_DMIPLL_R
+1.5VS_PCIE_ICH
+1.5VS_SATAPLL_R
+1.5VS_SATAPLL_ICH
+VCC_HDA_ICH
+VCCSUS_HDA_ICH
+VCC_GLANPLL_R
+VCC_GLANPLL_ICH
+ICH_V5REF
+ICH_V5REF_SUS
SBPWR_EN#
TP_VCCSUS1_05_ICH_1
TP_VCCSUS1_05_ICH_2
TP_VCCSUS1_5_ICH_1
TP_VCCSUS1_5_ICH_2
TP_VCCLAN1_05_ICH_1
TP_VCCLAN1_05_ICH_2
TP_VCCCL1_05_ICH
+VCCCL1_5_INT_ICH
Security Classification
Compal Secret Data
Issued Date
2006/12/25
Deciphered Date
2007/12/25
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Compal Electronics, Inc.
Title
ICH8M(4/4)-POWER&GND
Size
Custom
Document Number
ICL50/ICK70 M/B LA-3551P Schematic
Rev
1.0
Date:
Wednesday, August 15, 2007
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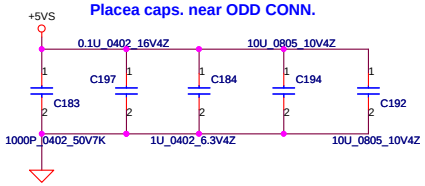
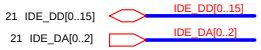
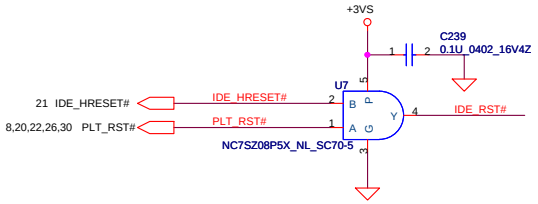
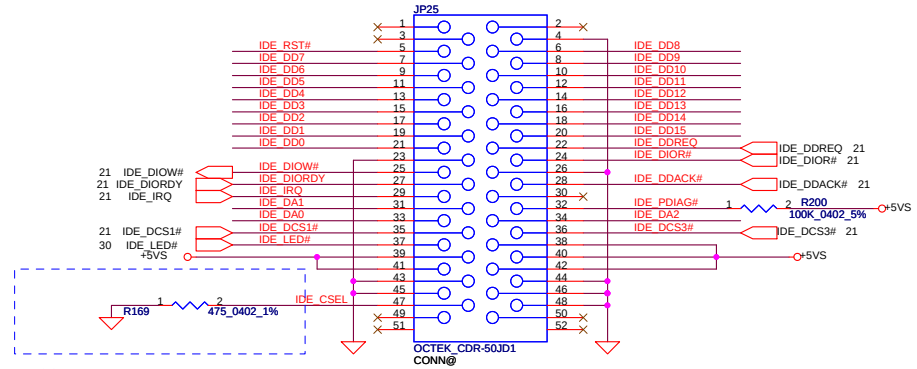
Placea caps. near ODD CONN.

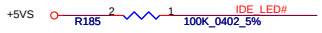


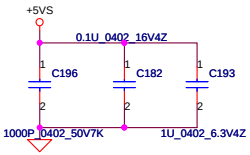


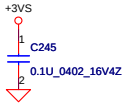




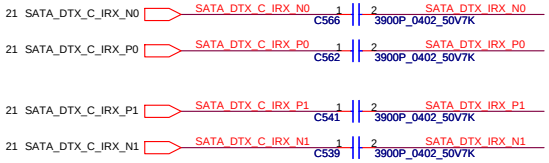
IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

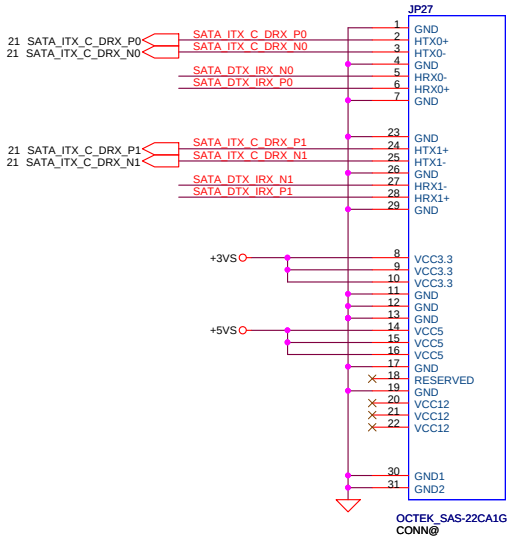






SATA HDD Conn.(SAS Connector)





First HDD for 15.4"

2nd HDD for 17"

Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: HDD & ODD Connector

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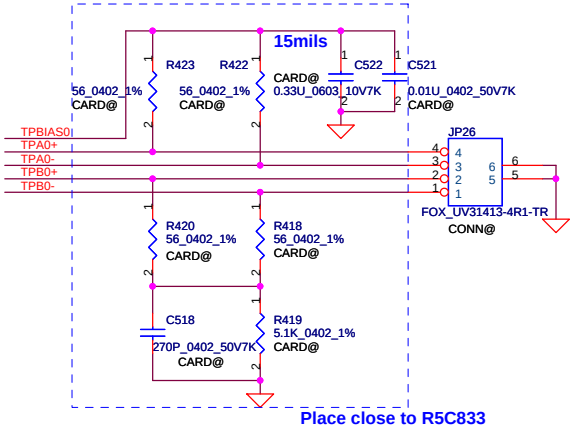
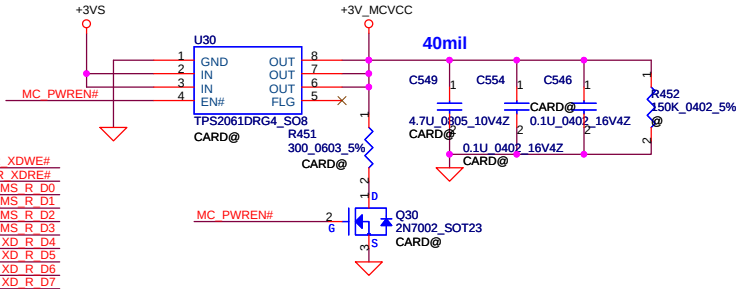
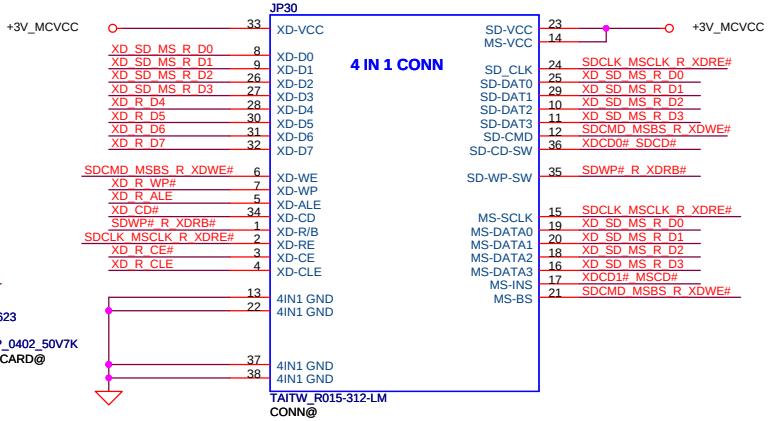
IEEE1394 CONN.



Memory Card Power Switch



4 IN 1 Socket Push Type(New)



R5C833

Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title	R5C833 5IN1 & IEEE1394		
Size B	Document Number ICL50/ICK70 M/B LA-3551P Schematic		Rev 1.0
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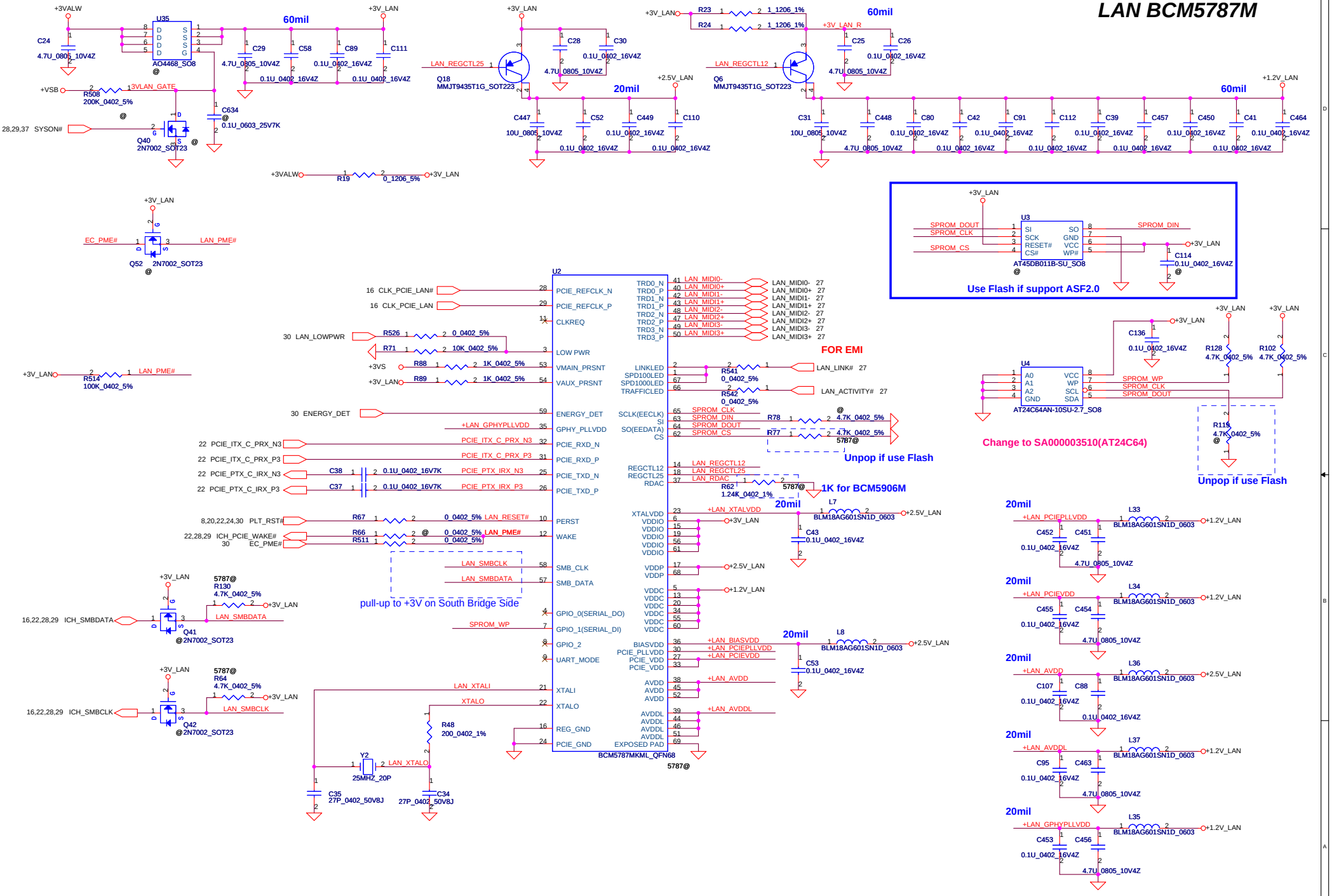
LAN BCM5787M



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: LAN BCM5787M

Size: B | Document Number: ICL50/ICK70 M/B LA-3551P Schematic | Rev: 1.0

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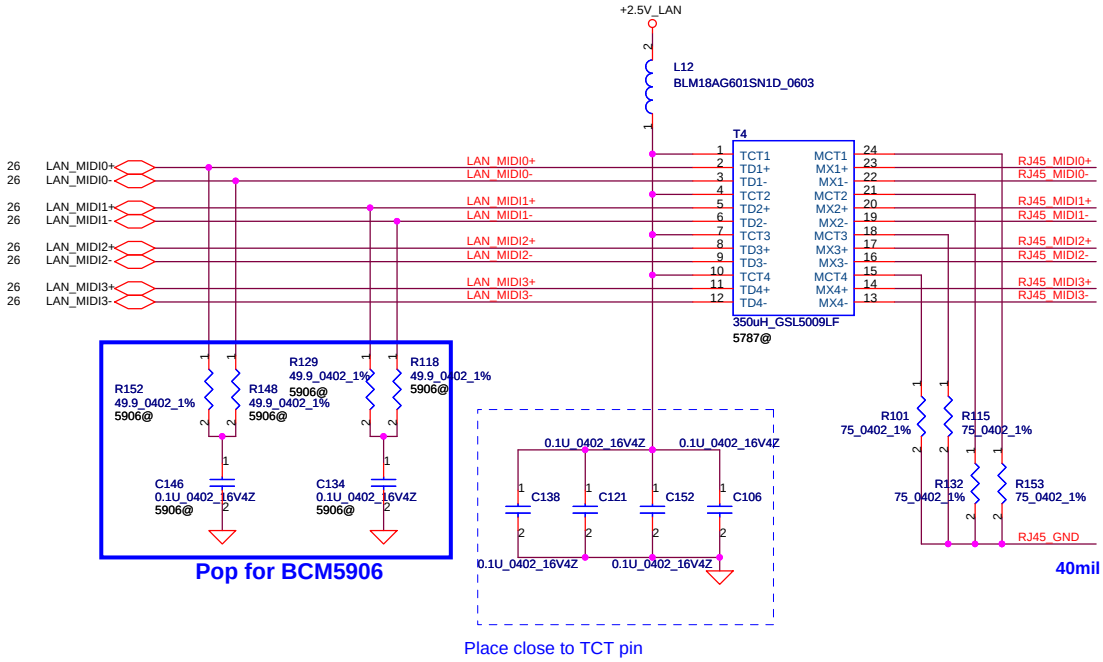
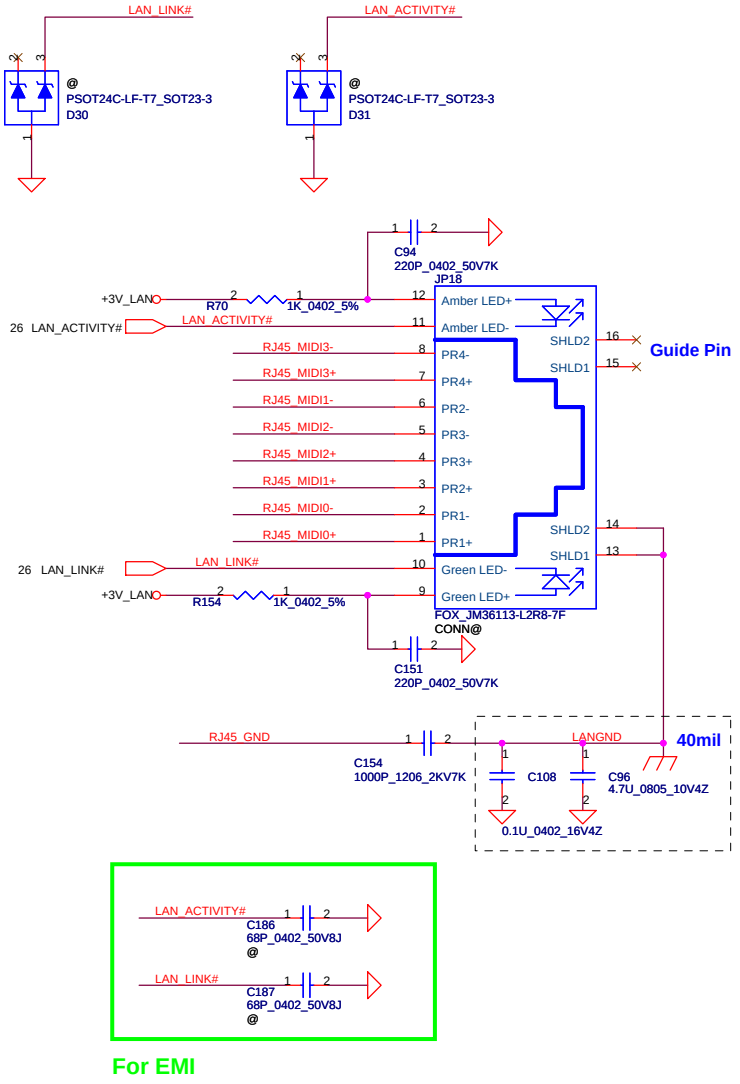
LAN BCM5787M





Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45/RJ11

Size	Document Number	Rev
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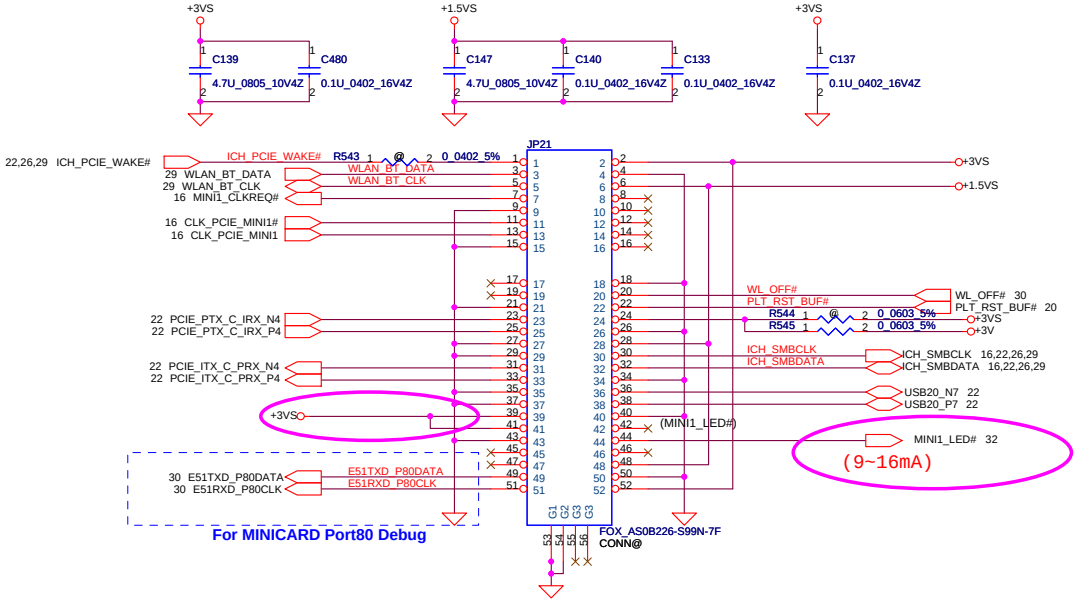
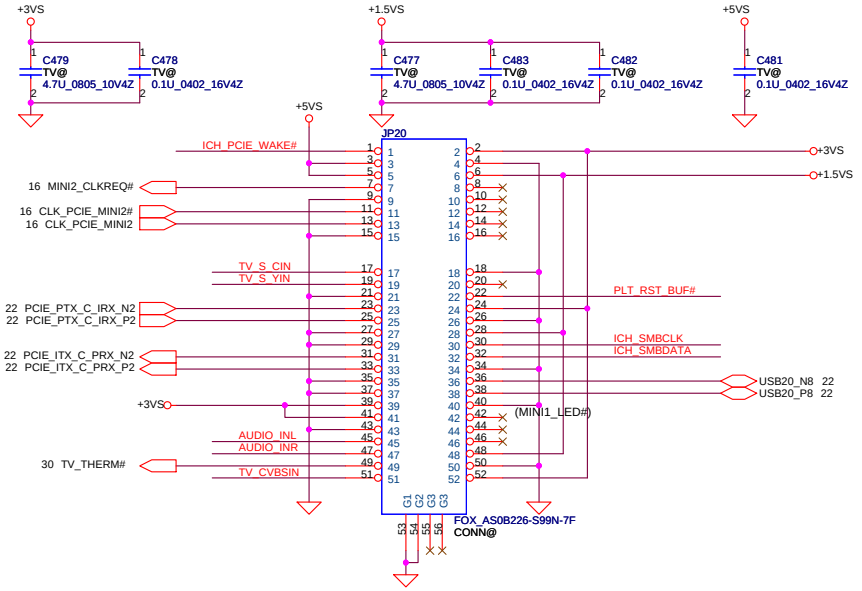
For Wireless LAN

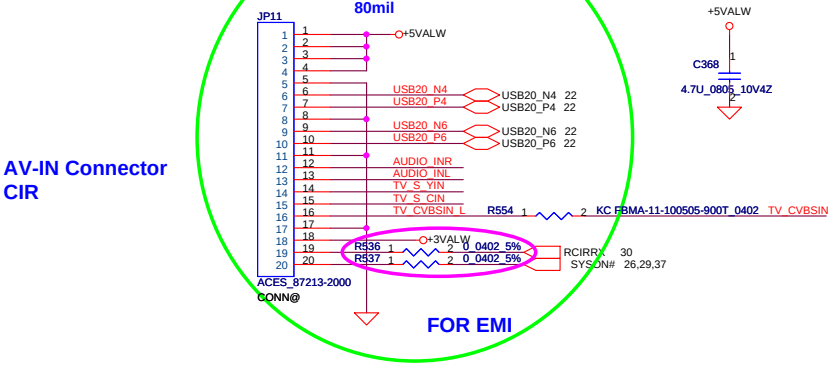


For TV-Tuner/HW MPEG



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

To USB/B Connector



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)

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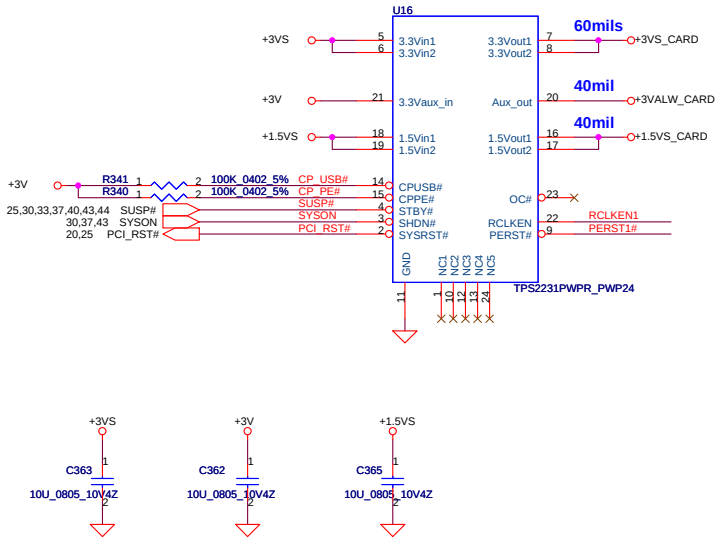
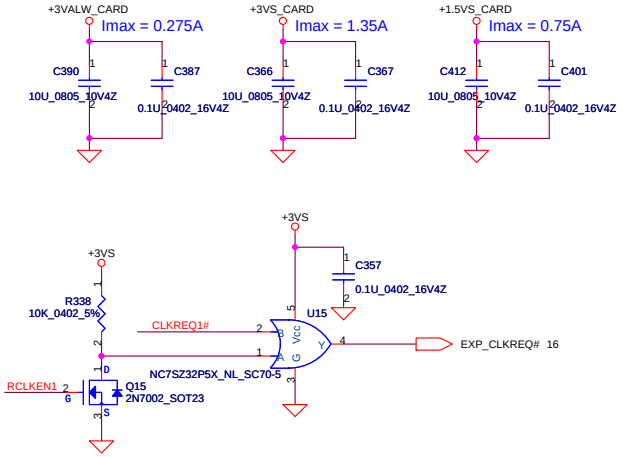
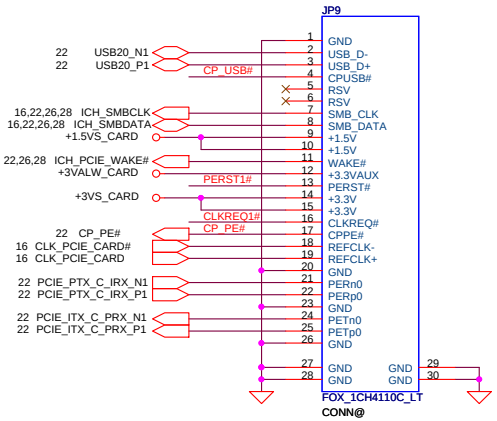
New Card Power Switch

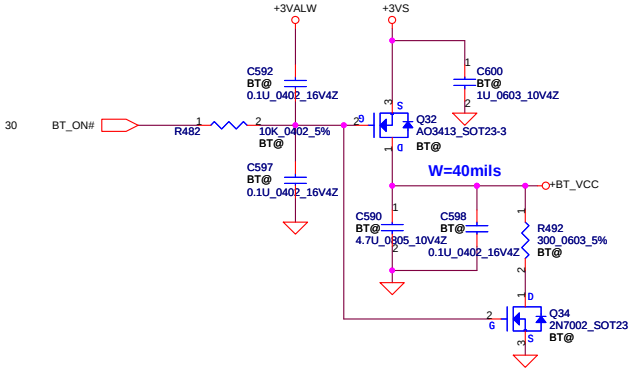


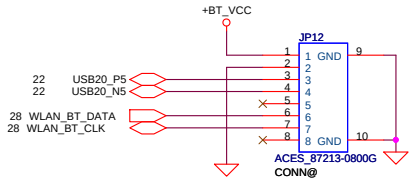


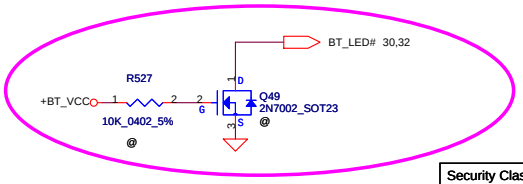
New Card Socket (Left/TOP)



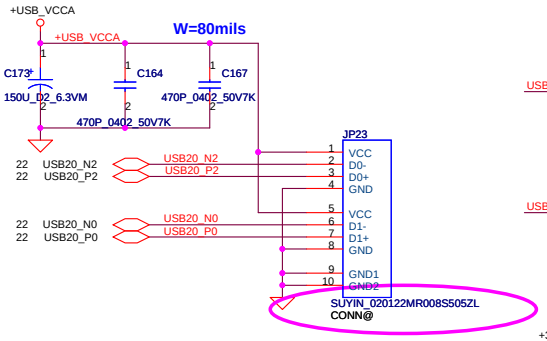
Bluetooth Conn.

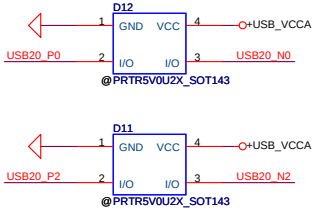


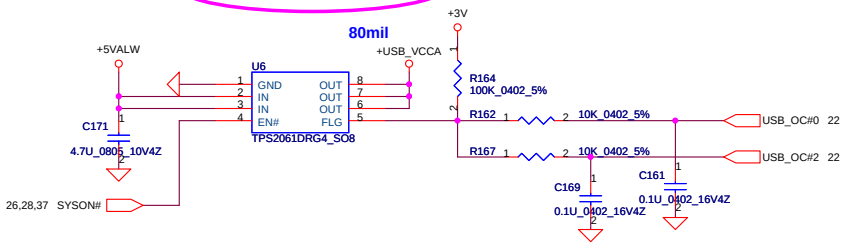




USB CONN. (Stack-up Type)







Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: NEW CARD & USB Connector

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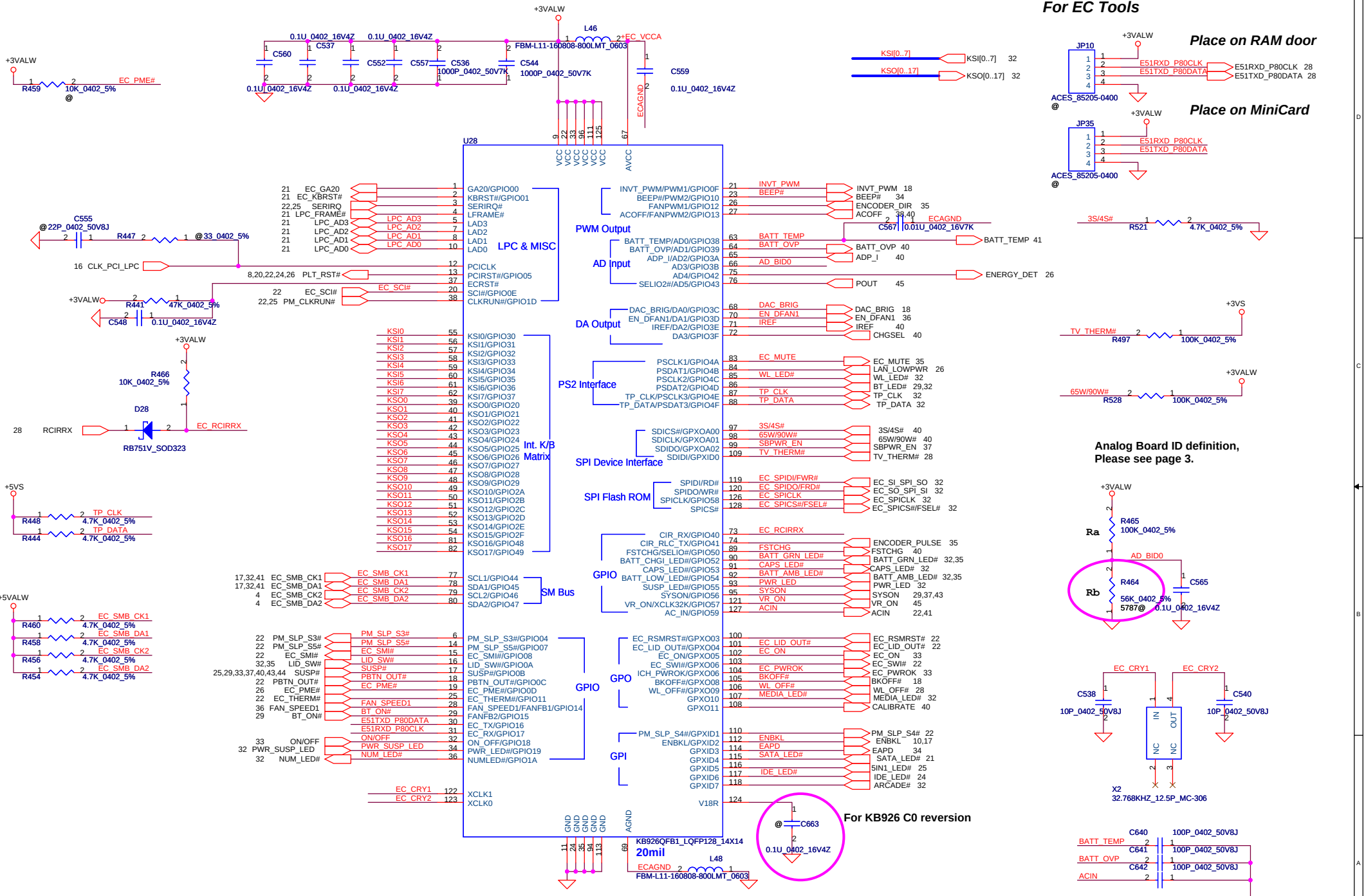
For EC Tools
Place on RAM door
Place on MiniCard
U28
KB926QFB1_LQFP128_14X14
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
Analog Board ID definition, Please see page 3.
For KB926 C0 reversion
Security Classification
Compal Secret Data
Issued Date
2006/12/25
Deciphered Date
2007/12/25
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Compal Electronics, Inc.
Title
EC ENE KB926
Size B
Document Number
ICL50/ICK70 M/B LA-3551P Schematic
Rev 1.0
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Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: EC ENE KB925(Reserved)

Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematic	1.0

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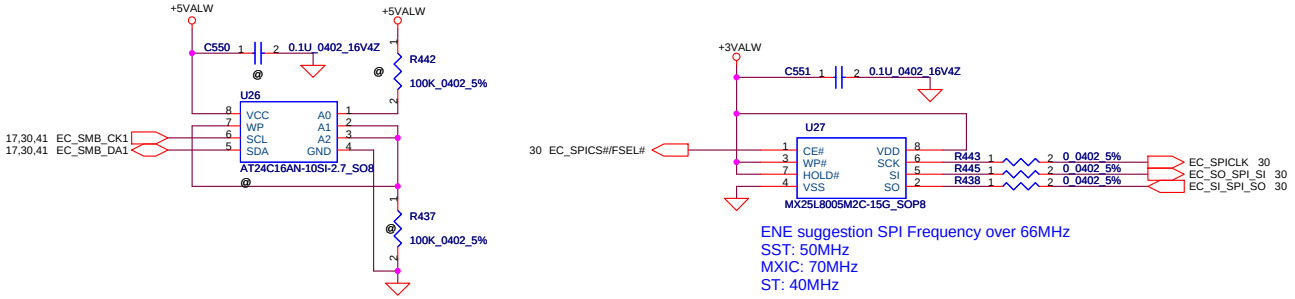
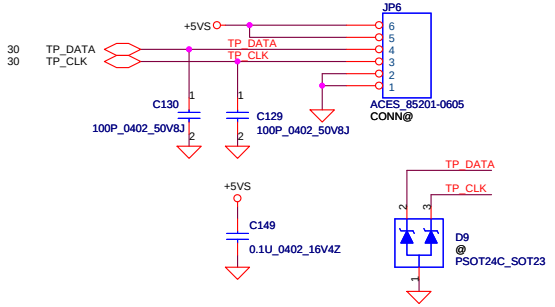
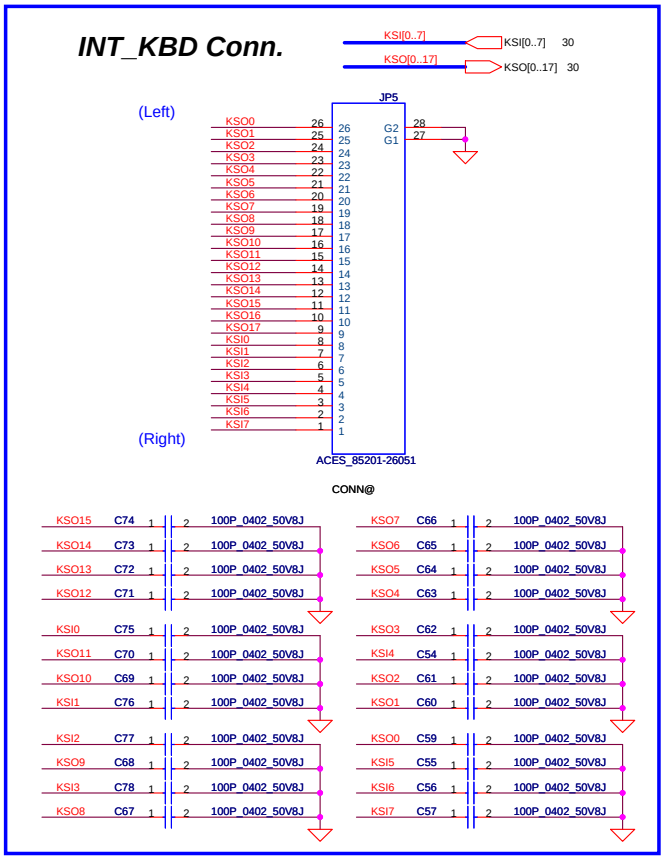


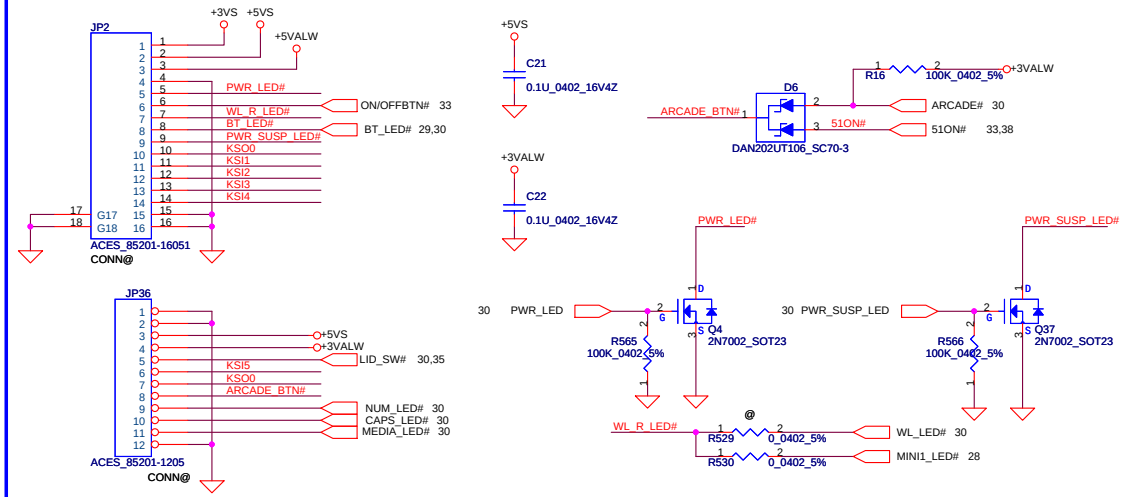
To TP/B Conn.



INT_KBD Conn.

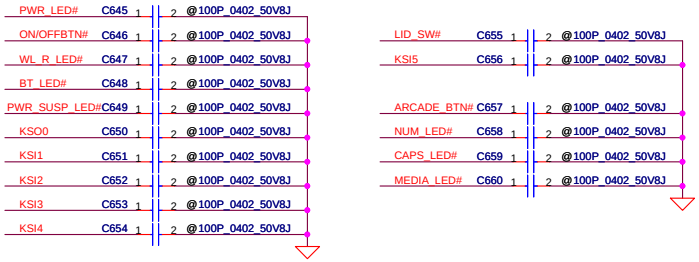


To BTN/B Conn.



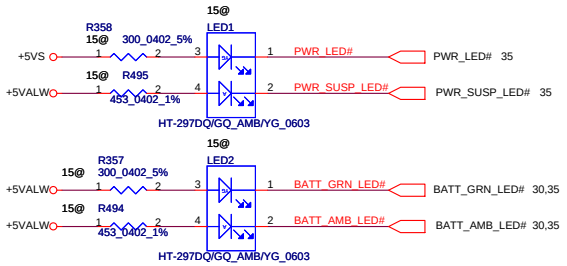
	KSO0	(Acadia 960)
KSI1	WL_BTN#	WL_BTN#
KSI2	BT_BTN#	VOL_DOWN
KSI3	EMAIL_BTN#	VOL_UP
KSI4	IE_BTN#	N/A
KSI5	E-KEY_BTN#	E-KEY_BTN#

FOR EMI



Compal Footprint

15" ONLY



Security Classification	Compal Secret Data
Issued Date	2006/12/25
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Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size	Document Number	Rev
B	ICL50/ICK70 M/B LA-3551P Schematic	1.0

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