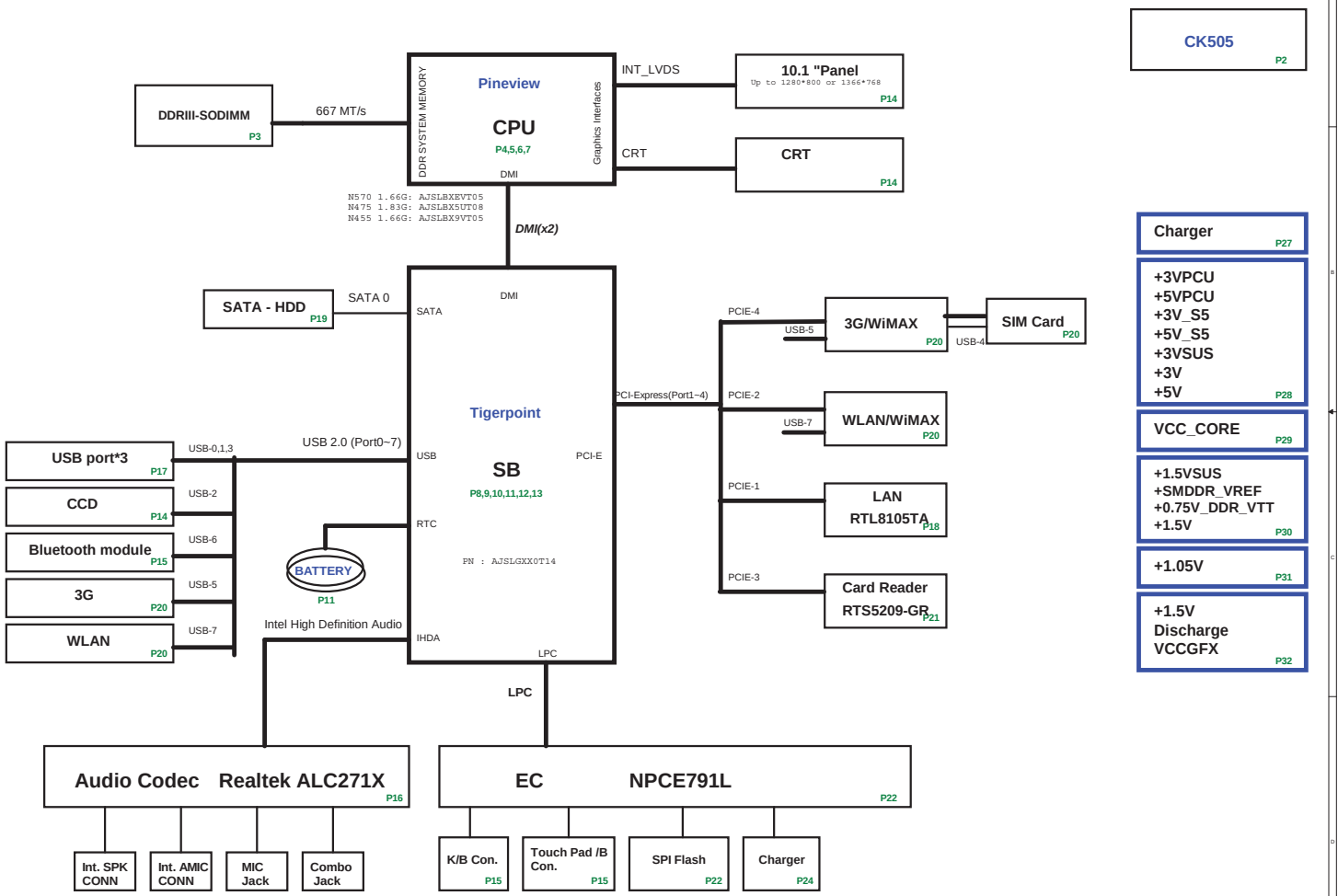
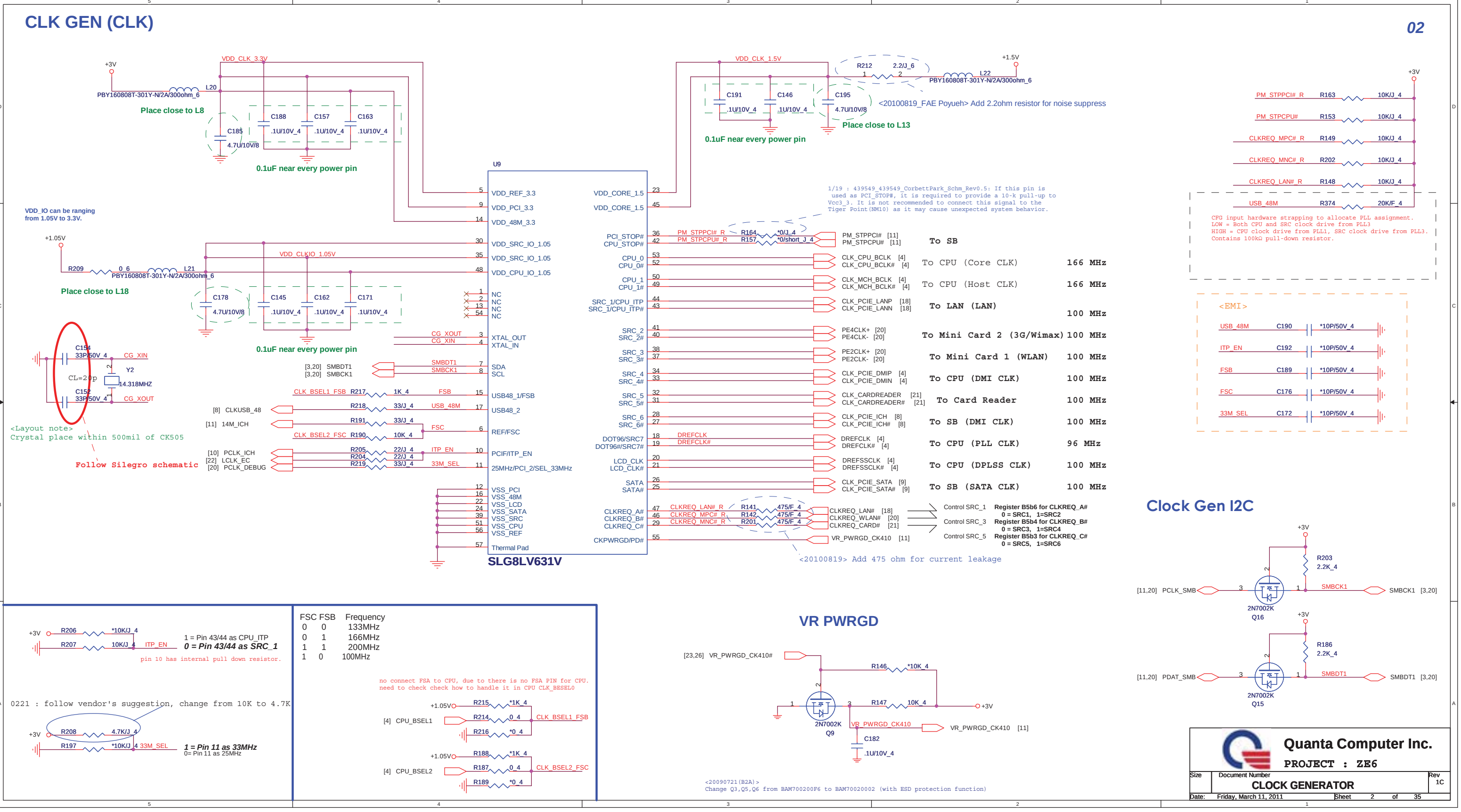
ZE6 Block Diagram

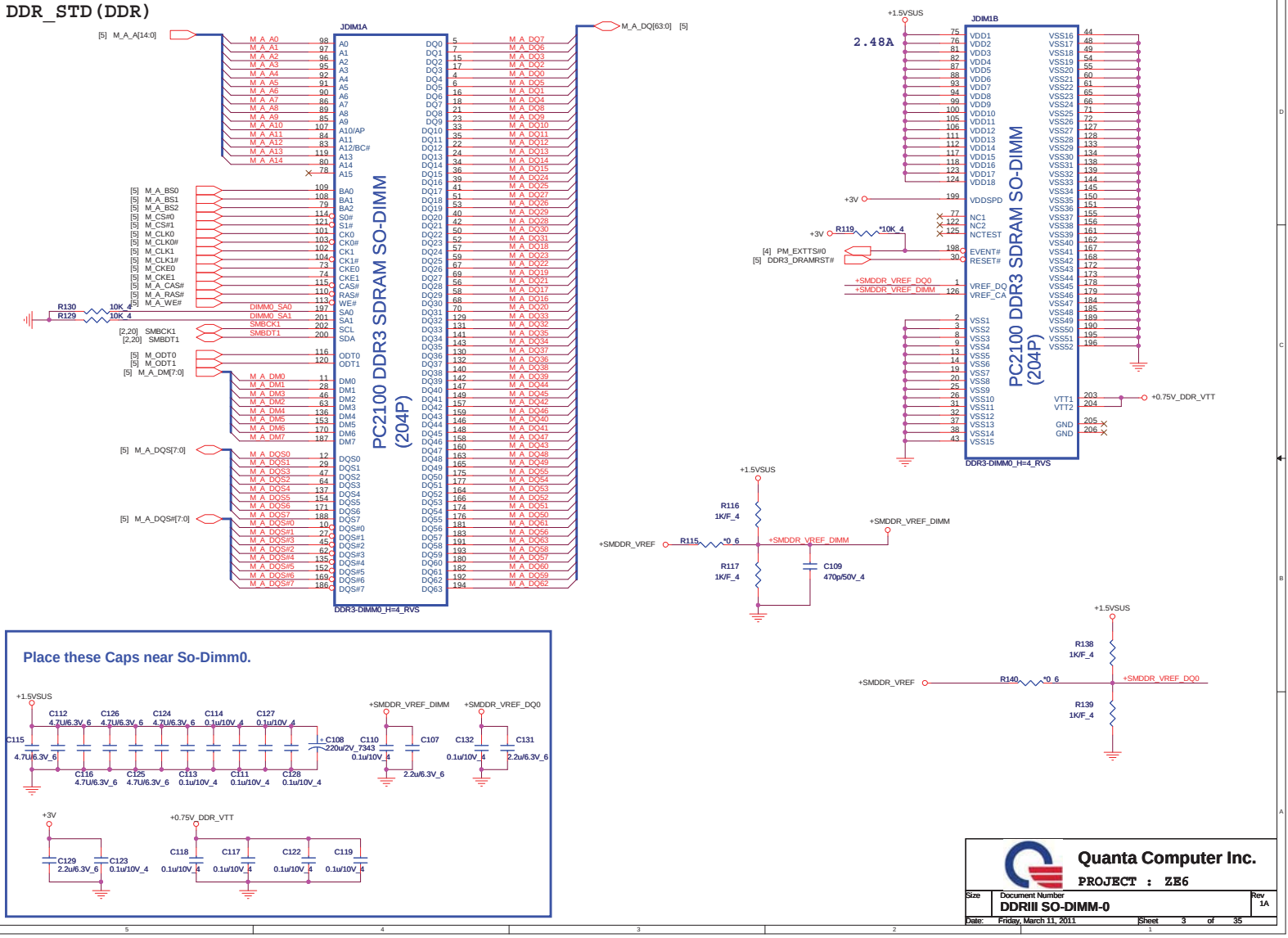


Quanta Computer Inc.
PROJECT : ZE6
Size | Document Number | Rev 1B
Block Diagram
Date: Friday, March 11, 2011 | Sheet 1 of 35



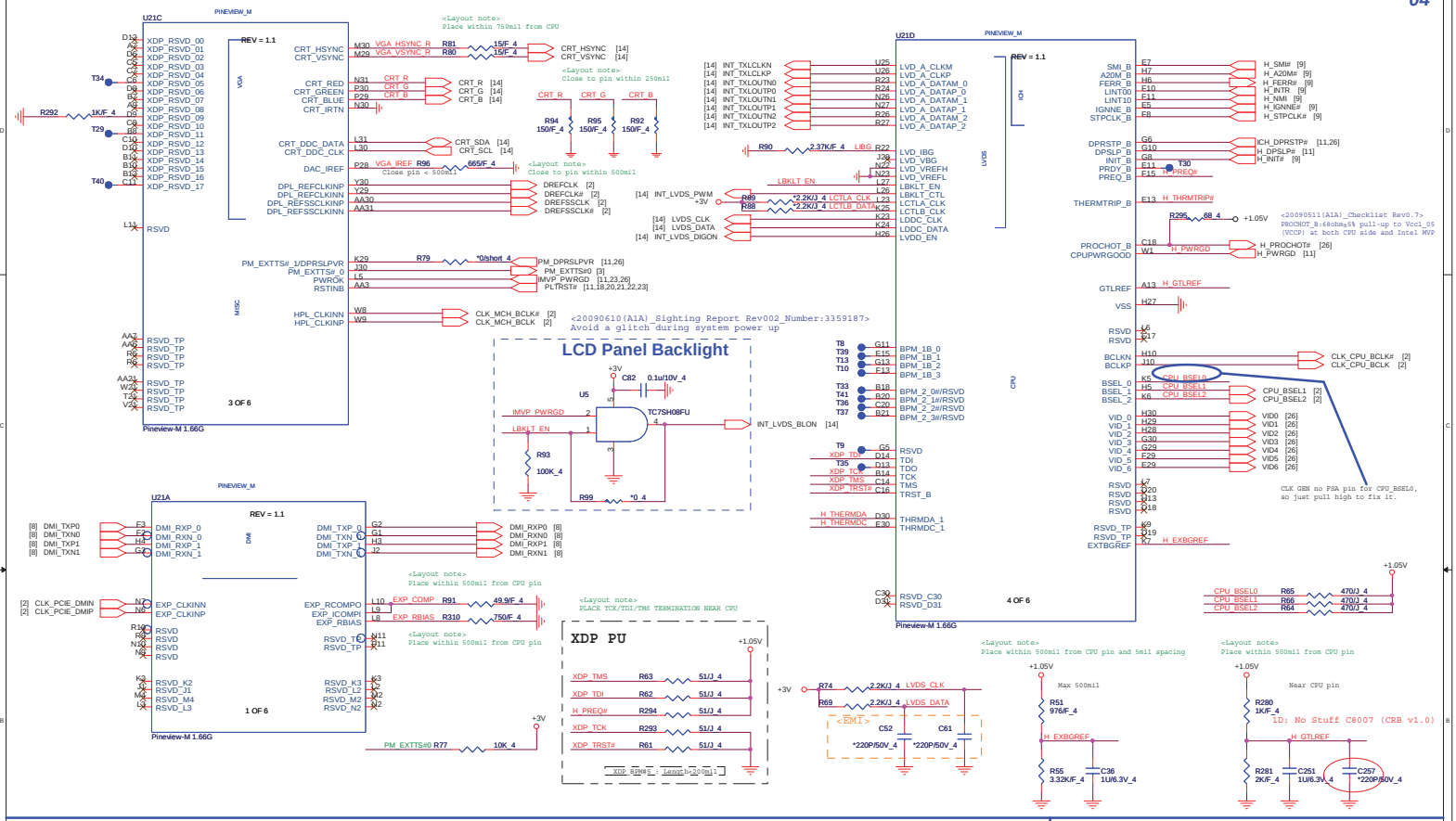
CLK GEN (CLK)
02
VDD_CLK_3.3V
PBY160808T-301Y-N/2A/300ohm_6
Place close to L8
0.1uF near every power pin
VDD_IO can be ranging from 1.05V to 3.3V.
Place close to L18
VDD_CLKIO_1.05V
VDD_CLK_1.5V
<20100819_FAE Poyueh> Add 2.2ohm resistor for noise suppress
Place close to L13
U9
VDD_REF_3.3
VDD_PCI_3.3
VDD_48M_3.3
VDD_SRC_IO_1.05
VDD_CPU_IO_1.05
XTAL_OUT
XTAL_IN
SDA
SCL
USB48_1/FSB
USB48_2
REF/FSC
PCIF/ITP_EN
25MHz/PCI_2/SEL_33MHz
VSS_PCI
VSS_48M
VSS_LCD
VSS_SATA
VSS_SRC
VSS_CPU
VSS_REF
Thermal Pad
SLG8LV631V
VDD_CORE_1.5
PCI_STOP#
CPU_STOP#
CPU_0
CPU_0#
CPU_1
CPU_1#
SRC_1/CPU_ITP
SRC_1/CPU_ITP#
DOT96/SRC7
DOT96#/SRC7#
LCD_CLK
LCD_CLK#
SATA
SATA#
CLKREQ_A#
CLKREQ_B#
CLKREQ_C#
CKPWRGD/PD#
1/19 : 439549_439549_CorbettPark_Schm_Rev0.5: If this pin is used as PCI_STOP#, it is required to provide a 10-k pull-up to Vcc3_3. It is not recommended to connect this signal to the Tiger Point(NM10) as it may cause unexpected system behavior.
To SB
To CPU (Core CLK) 166 MHz
To CPU (Host CLK) 166 MHz
To LAN (LAN) 100 MHz
To Mini Card 2 (3G/Wimax) 100 MHz
To Mini Card 1 (WLAN) 100 MHz
To CPU (DMI CLK) 100 MHz
To Card Reader 100 MHz
To SB (DMI CLK) 100 MHz
To CPU (PLL CLK) 96 MHz
To CPU (DPLSS CLK) 100 MHz
To SB (SATA CLK) 100 MHz
Register B5b6 for CLKREQ_A# 0 = SRC1, 1=SRC2
Register B5b4 for CLKREQ_B# 0 = SRC3, 1=SRC4
Register B5b3 for CLKREQ_C# 0 = SRC5, 1=SRC6
<20100819> Add 475 ohm for current leakage
CFG input hardware strapping to allocate PLL assignment. LOW = Both CPU and SRC clock drive from PLL3 HIGH = CPU clock drive from PLL1, SRC clock drive from PLL3. Contains 100KΩ pull-down resistor.
<EMI>
CL=20p
14.318MHZ
<Layout note> Crystal place within 500mil of CK505
Follow Silegro schematic
Clock Gen I2C
2N7002K
VR PWRGD
1 = Pin 43/44 as CPU_ITP
0 = Pin 43/44 as SRC_1
pin 10 has internal pull down resistor.
0221 : follow vendor's suggestion, change from 10K to 4.7K
1 = Pin 11 as 33MHz
0= Pin 11 as 25MHz
FSC FSB Frequency
0 0 133MHz
0 1 166MHz
1 1 200MHz
1 0 100MHz
no connect FSA to CPU, due to there is no FSA PIN for CPU. need to check check how to handle it in CPU CLK_BSEL0
<20090721(B2A)> Change Q3,Q5,Q6 from BAM700200F6 to BAM70020002 (with ESD protection function)
Quanta Computer Inc.
PROJECT : ZE6
Size
Document Number
CLOCK GENERATOR
Rev
1C
Date: Friday, March 11, 2011
Sheet 2 of 35

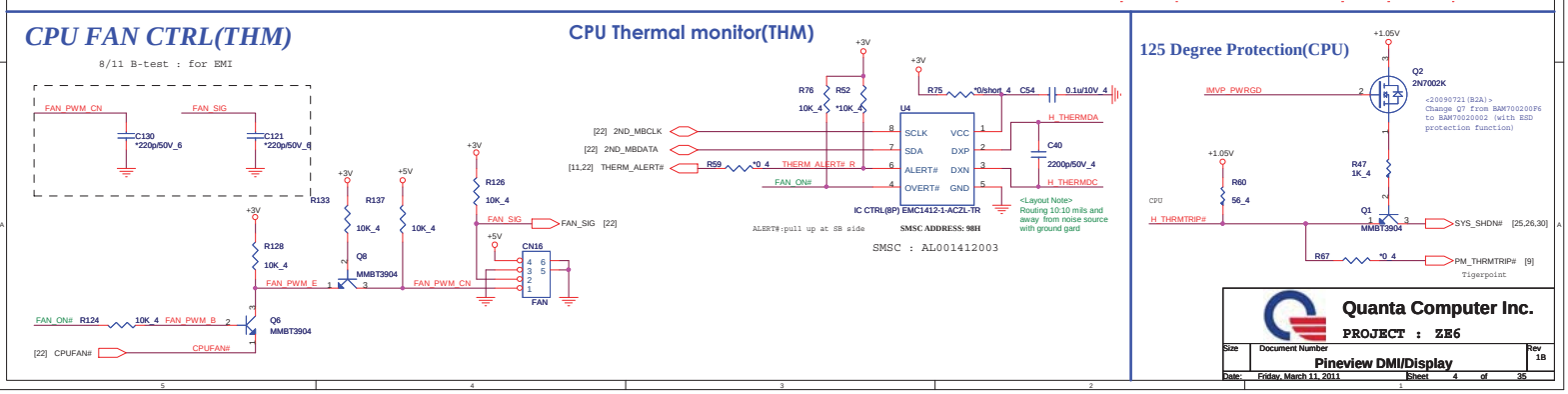
DDR_STD(DDR)



Place these Caps near So-Dimm0.

Quanta Computer Inc.		
PROJECT : ZE6		
Size	Document Number: DDRIII SO-DIMM-0	Rev: 1A
Date: Friday, March 11, 2011	Sheet 3 of 35	


U21C
PINEVIEW_M
REV = 1.1
3 OF 6
Pineview-M 1.66G
U21D
4 OF 6
U21A
1 OF 6
LCD Panel Backlight
XDP PU
CPU FAN CTRL(THM)
CPU Thermal monitor(THM)
125 Degree Protection(CPU)
SMSC : AL001412003


8/11 B-test : for EMI
IC CTRL(8P) EMC1412-1-AC2L-TR
SMSC ADDRESS: 98H

Quanta Computer Inc.
PROJECT : ZE6
Pineview DMI/Display
Friday, March 11, 2011
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PINEVIEW_M

U21B

REV = 1.1

[3] M_A_A[14..0]

M_A_A0 AH19 DDR_A_MA_0
M_A_A1 AJ18 DDR_A_MA_1
M_A_A2 AK18 DDR_A_MA_2
M_A_A3 AK16 DDR_A_MA_3
M_A_A4 AJ14 DDR_A_MA_4
M_A_A5 AH14 DDR_A_MA_5
M_A_A6 AK14 DDR_A_MA_6
M_A_A7 AJ12 DDR_A_MA_7
M_A_A8 AH13 DDR_A_MA_8
M_A_A9 AK12 DDR_A_MA_9
M_A_A10 AK20 DDR_A_MA_10
M_A_A11 AH12 DDR_A_MA_11
M_A_A12 AJ11 DDR_A_MA_12
M_A_A13 AJ24 DDR_A_MA_13
M_A_A14 AJ10 DDR_A_MA_14

[3] M_A_WE#
[3] M_A_CAS#
[3] M_A_RAS#
M_A_WE# AK22 DDR_A_WEB
M_A_CAS# AJ22 DDR_A_CASB
M_A_RAS# AK21 DDR_A_RASB

[3] M_A_BS0
[3] M_A_BS1
[3] M_A_BS2
M_A_BS0 AJ20 DDR_A_BS_0
M_A_BS1 AH20 DDR_A_BS_1
M_A_BS2 AK11 DDR_A_BS_2

[3] M_CS#0
[3] M_CS#1
M_CS#0 AH22 DDR_A_CSB_0
M_CS#1 AK25 DDR_A_CSB_1
AJ21 DDR_A_CSB_2
AJ25 DDR_A_CSB_3

[3] M_CKE0
[3] M_CKE1
M_CKE0 AH10 DDR_A_CKE_0
M_CKE1 AH9 DDR_A_CKE_1
AK10 DDR_A_CKE_2
AJ8 DDR_A_CKE_3

[3] M_ODT0
[3] M_ODT1
M_ODT0 AK24 DDR_A_ODT_0
M_ODT1 AH26 DDR_A_ODT_1
AH24 DDR_A_ODT_2
AK26 DDR_A_ODT_3

[3] M_CLK0
[3] M_CLK0#
[3] M_CLK1
[3] M_CLK1#
M_CLK0 AG15 DDR_A_CK_0
M_CLK0# AF15 DDR_A_CKB_0
M_CLK1 AD13 DDR_A_CK_1
M_CLK1# AC13 DDR_A_CKB_1

AC15 DDR_A_CK_3
AD15 DDR_A_CKB_3
AF13 DDR_A_CK_4
AG13 DDR_A_CKB_4

AD17 RSVD_AD17
AC17 RSVD_AC17
AB15 RSVD_AB15
AB17 RSVD_AB17

AB11 RSVD_TP
AB13 RSVD_TP

AL28 DDR_VREF
AK28 DDR_VREF
AJ26 DDR_RPD
DDR_RPU

AK29 RSVD

DDR_A

AB4 VSS
AK8 RSVD

DDR_A_DQS0 AD3 M_A_DQS0
DDR_A_DQSB0 AD2 M_A_DQS#0
DDR_A_DM_0 AD4 M_A_DM0

DDR_A_DQ_0 AC4 M_A_DQ0
DDR_A_DQ_1 AC1 M_A_DQ1
DDR_A_DQ_2 AE4 M_A_DQ2
DDR_A_DQ_3 AC2 M_A_DQ3
DDR_A_DQ_4 AB2 M_A_DQ4
DDR_A_DQ_5 AB3 M_A_DQ5
DDR_A_DQ_6 AE2 M_A_DQ6
DDR_A_DQ_7 AE3 M_A_DQ7

DDR_A_DQS1 AB8 M_A_DQS1
DDR_A_DQSB1 AD7 M_A_DQS#1
DDR_A_DM_1 AA9 M_A_DM1

DDR_A_DQ_8 AB6 M_A_DQ8
DDR_A_DQ_9 AB7 M_A_DQ9
DDR_A_DQ_10 AE5 M_A_DQ10
DDR_A_DQ_11 AG5 M_A_DQ11
DDR_A_DQ_12 AA5 M_A_DQ12
DDR_A_DQ_13 AB5 M_A_DQ13
DDR_A_DQ_14 AB9 M_A_DQ14
DDR_A_DQ_15 AD6 M_A_DQ15

DDR_A_DQS2 AD8 M_A_DQS2
DDR_A_DQSB2 AD10 M_A_DQS#2
DDR_A_DM_2 AE8 M_A_DM2

DDR_A_DQ_16 AG8 M_A_DQ16
DDR_A_DQ_17 AG7 M_A_DQ17
DDR_A_DQ_18 AF10 M_A_DQ18
DDR_A_DQ_19 AG11 M_A_DQ19
DDR_A_DQ_20 AF7 M_A_DQ20
DDR_A_DQ_21 AF8 M_A_DQ21
DDR_A_DQ_22 AD11 M_A_DQ22
DDR_A_DQ_23 AE10 M_A_DQ23

DDR_A_DQS3 AK5 M_A_DQS3
DDR_A_DQSB3 AK3 M_A_DQS#3
DDR_A_DM_3 AJ3 M_A_DM3

DDR_A_DQ_24 AH1 M_A_DQ24
DDR_A_DQ_25 AJ2 M_A_DQ25
DDR_A_DQ_26 AK6 M_A_DQ26
DDR_A_DQ_27 AJ7 M_A_DQ27
DDR_A_DQ_28 AF3 M_A_DQ28
DDR_A_DQ_29 AH2 M_A_DQ29
DDR_A_DQ_30 AL5 M_A_DQ30
DDR_A_DQ_31 AJ6 M_A_DQ31

DDR_A_DQS4 AG22 M_A_DQS4
DDR_A_DQSB4 AG21 M_A_DQS#4
DDR_A_DM_4 AD19 M_A_DM4

DDR_A_DQ_32 AE19 M_A_DQ32
DDR_A_DQ_33 AG19 M_A_DQ33
DDR_A_DQ_34 AF22 M_A_DQ34
DDR_A_DQ_35 AD22 M_A_DQ35
DDR_A_DQ_36 AG17 M_A_DQ36
DDR_A_DQ_37 AF19 M_A_DQ37
DDR_A_DQ_38 AE21 M_A_DQ38
DDR_A_DQ_39 AD21 M_A_DQ39

DDR_A_DQS5 AE26 M_A_DQS5
DDR_A_DQSB5 AG27 M_A_DQS#5
DDR_A_DM_5 AJ27 M_A_DM5

DDR_A_DQ_40 AE24 M_A_DQ40
DDR_A_DQ_41 AG25 M_A_DQ41
DDR_A_DQ_42 AD25 M_A_DQ42
DDR_A_DQ_43 AD24 M_A_DQ43
DDR_A_DQ_44 AC22 M_A_DQ44
DDR_A_DQ_45 AG24 M_A_DQ45
DDR_A_DQ_46 AD27 M_A_DQ46
DDR_A_DQ_47 AE27 M_A_DQ47

DDR_A_DQS6 AE30 M_A_DQS6
DDR_A_DQSB6 AE29 M_A_DQS#6
DDR_A_DM_6 AE30 M_A_DM6

DDR_A_DQ_48 AG31 M_A_DQ48
DDR_A_DQ_49 AG30 M_A_DQ49
DDR_A_DQ_50 AD30 M_A_DQ50
DDR_A_DQ_51 AD29 M_A_DQ51
DDR_A_DQ_52 AJ30 M_A_DQ52
DDR_A_DQ_53 AJ29 M_A_DQ53
DDR_A_DQ_54 AE29 M_A_DQ54
DDR_A_DQ_55 AD28 M_A_DQ55

DDR_A_DQS7 AB27 M_A_DQS7
DDR_A_DQSB7 AA27 M_A_DQS#7
DDR_A_DM_7 AB26 M_A_DM7

DDR_A_DQ_56 AA24 M_A_DQ56
DDR_A_DQ_57 AB25 M_A_DQ57
DDR_A_DQ_58 W24 M_A_DQ58
DDR_A_DQ_59 W22 M_A_DQ59
DDR_A_DQ_60 AB24 M_A_DQ60
DDR_A_DQ_61 AB23 M_A_DQ61
DDR_A_DQ_62 AA23 M_A_DQ62
DDR_A_DQ_63 W27 M_A_DQ63

2 OF 6

Pineview-M 1.66G

M_A_DQ[63..0] [3]
M_A_DM[7..0] [3]
M_A_DQS[7..0] [3]
M_A_DQS#[7..0] [3]

DDR3 PWROK

+3V_S5

[22,23,27,29] SUSON
[22,23,27] HWPG_1.5V

U7
TC7SH08FU

R121 12.1K/F_4
DDRAM_PWROK
R120 10K_4

+1.5VSUS

R350 *10K_4

[3] DDR3_DRAMRST#

C294 0.1U/10V_4

<Layout note>
Close to pin

R348 80.6/F_4 SM_RCOMP
R349 80.6/F_4 SM_RCOMP#

C295 0.01U/25V_4

+1.5VSUS

R351 1K/F_4
R352 *0_4
R353 1K/F_4
C296 0.1u/16V_6
C297 *1000p/50V_4

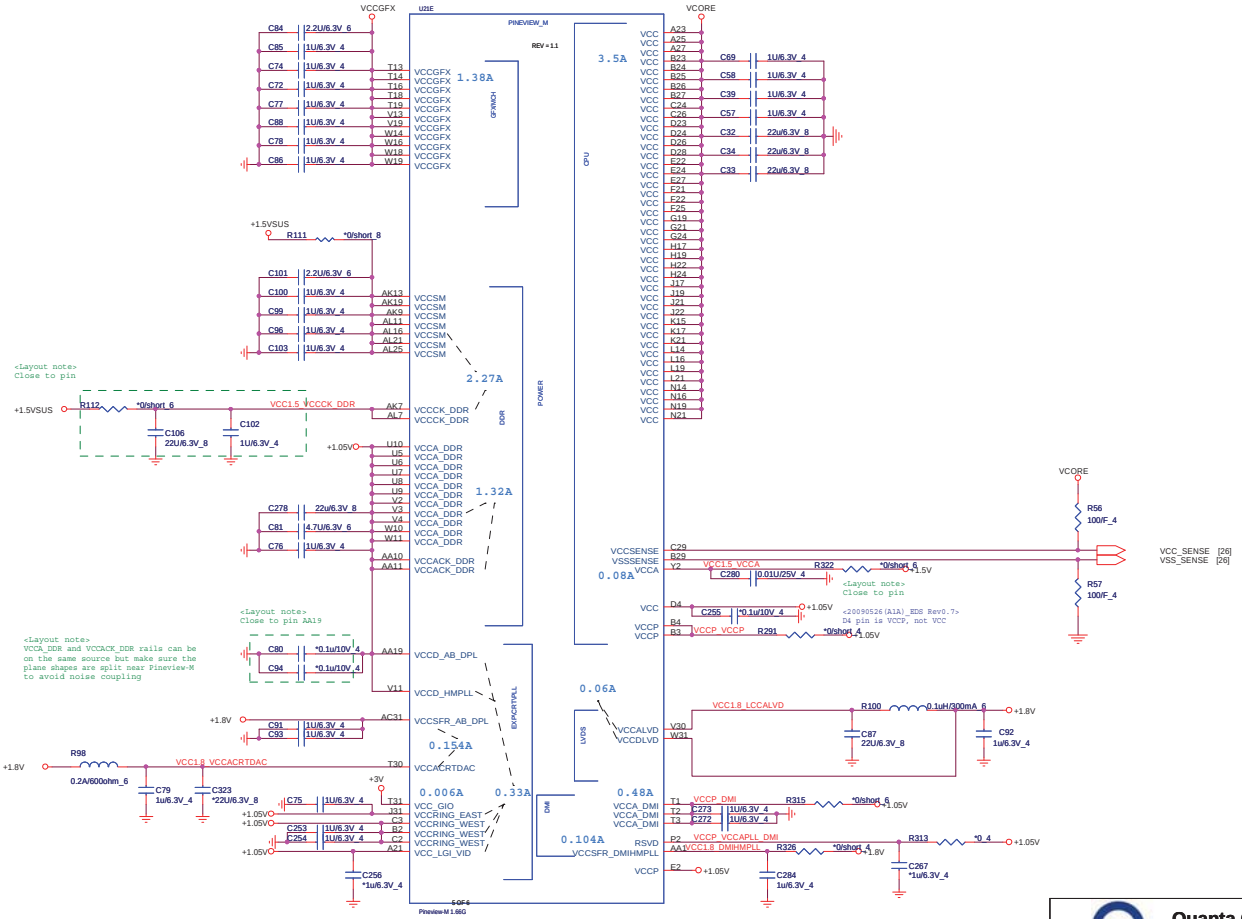
+SMDDR_VREF

<Layout note>
Close to DDR_VREF pin

DG 2.1 : It is strongly recommended that the SODIMM VREF motherboard traces, going from their VREF resistor dividers to their specified SODIMM VREF pins, be ground referenced on the motherboard where ever possible to help minimize risks of any possible noise being coupled onto VREF. If they can't be referenced to ground we recommend placing a site for a 0603 capacitor near the VREF divider. These 0603 capacitor sites must be connected on one end to the non ground reference plane the VREF trace is referenced to and the other end must be connected to ground.

Quanta Computer Inc.
PROJECT : ZE6

Size	Document Number	Rev
	Pineview DDR	1B
Date: Friday, March 11, 2011	Sheet 5 of 35	

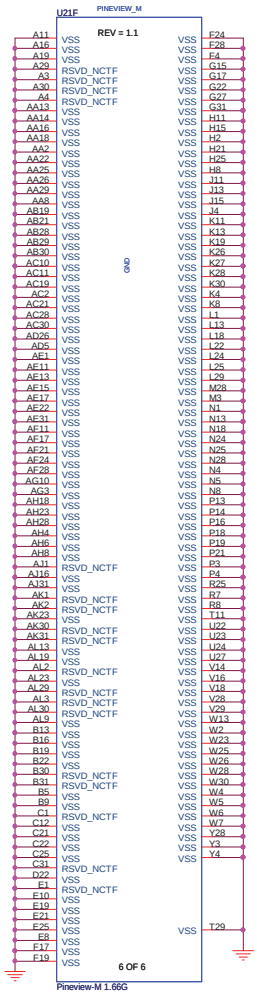


Quanta Computer Inc.

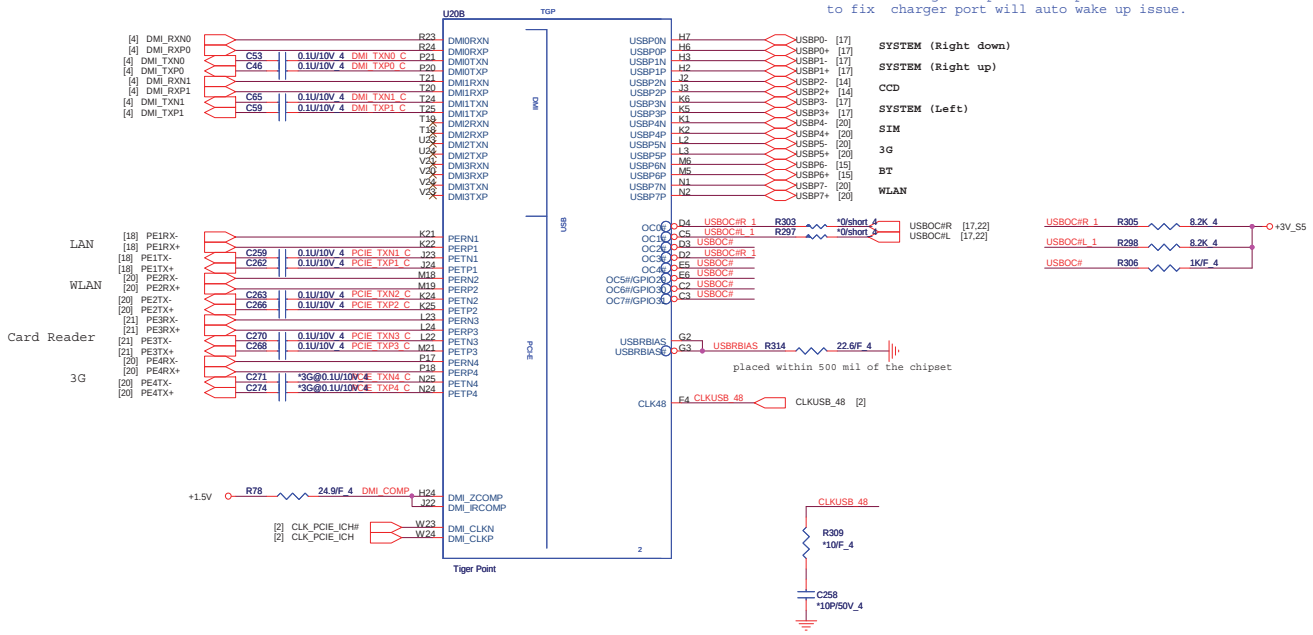
PROJECT : ZE6

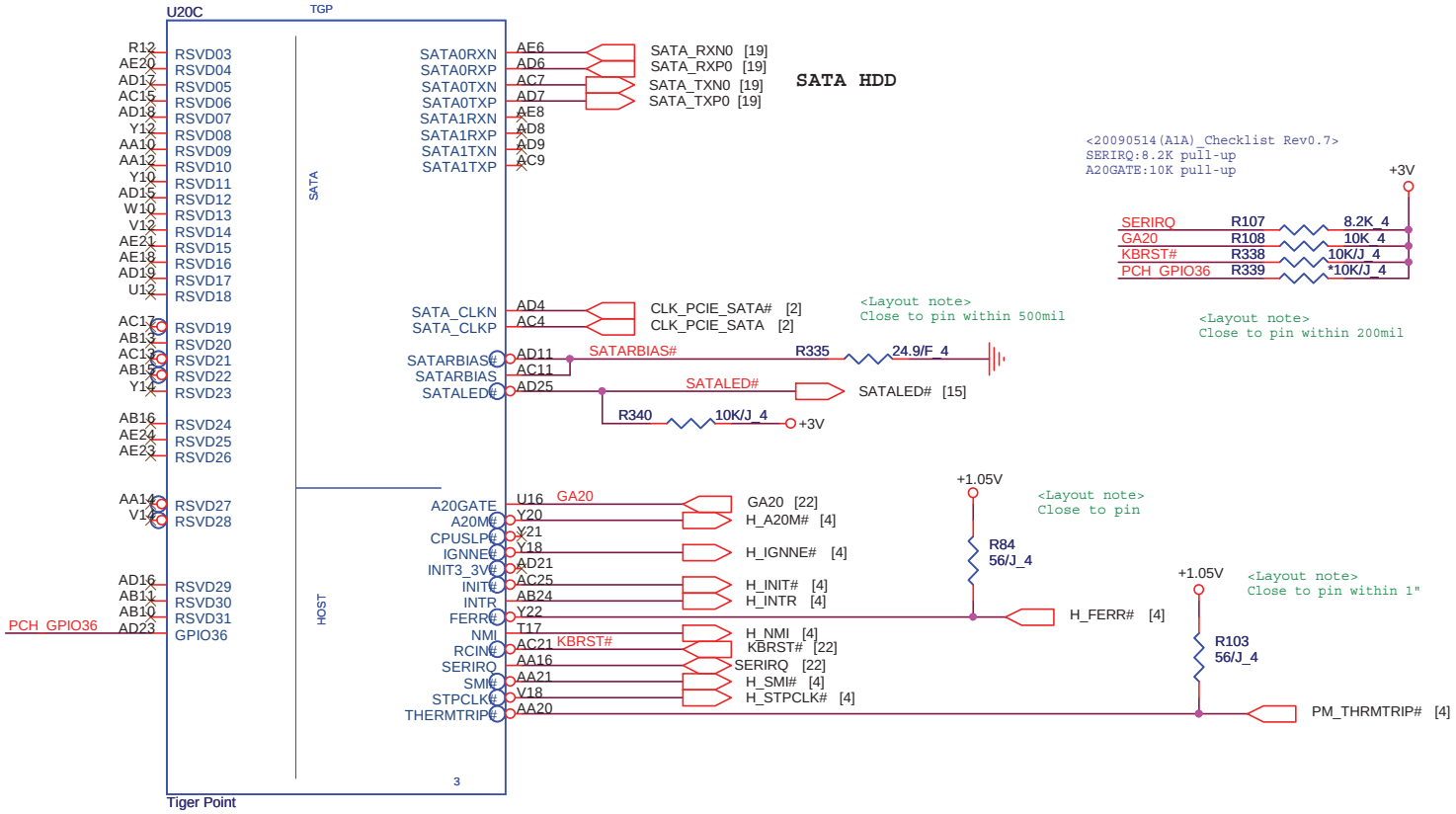
Size	Document Number	Rev
	Pineview Power	1B

Date: Friday, March 11, 2011 Sheet 6 of 35



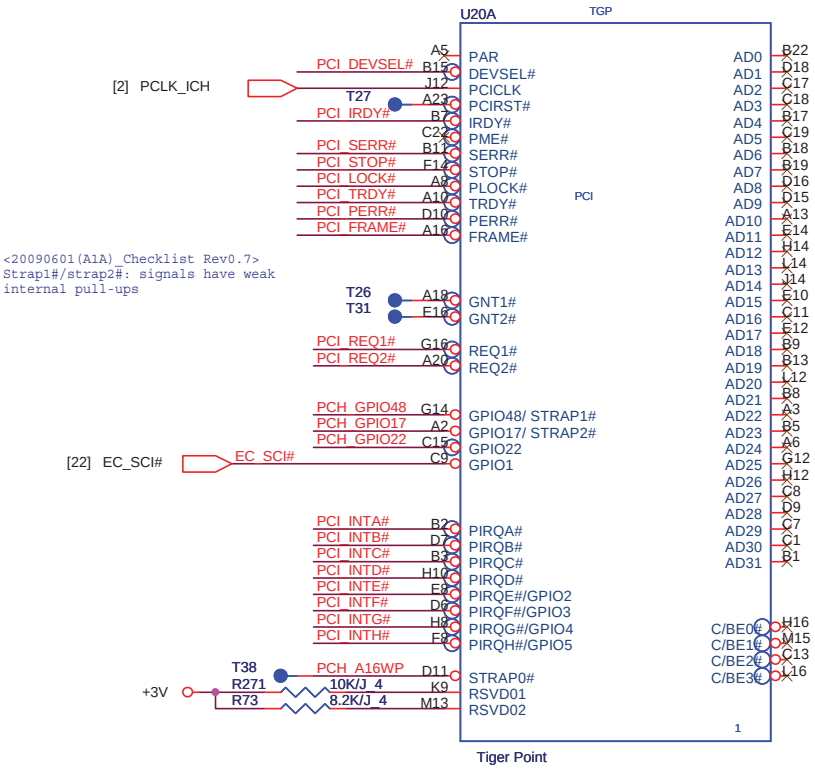
Quanta Computer Inc.		
PROJECT : ZE6		
Size	Document Number	Rev
	Pineview GND	1B
Date: Friday, March 11, 2011	Sheet 7 of 35	


0110 : exchange USB port 1 and port 3
to fix charger port will auto wake up issue.
U20B
TGP
DMI
USB
PCIE
SYSTEM (Right down)
SYSTEM (Right up)
CCD
SYSTEM (Left)
SIM
3G
BT
WLAN
LAN
WLAN
Card Reader
3G
placed within 500 mil of the chipset
Tiger Point
2



NOTE :
1. CPUSLP# is supported only on nettop platforms.

Quanta Computer Inc.		
PROJECT : ZE6		
Size	Document Number: Tiger Point Sata/Host	Rev 1B
Date: Friday, March 11, 2011	Sheet 9 of 35	

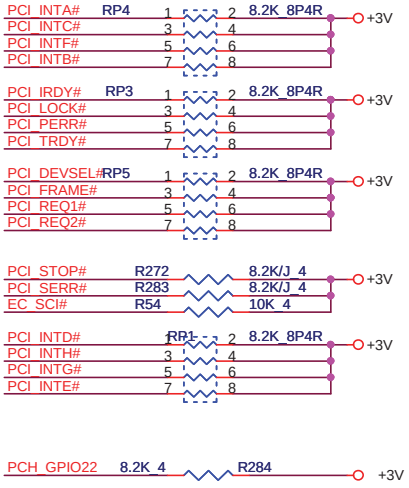


ICH Boot BIOS select

PCH_GPIO17 (INT PU)	PCH_GPIO48 (INT PU)	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC (Default)

A16 SWAP Override strap

PCH_A16WP (INT PU)	Low = A16 swap override enabled High = Default



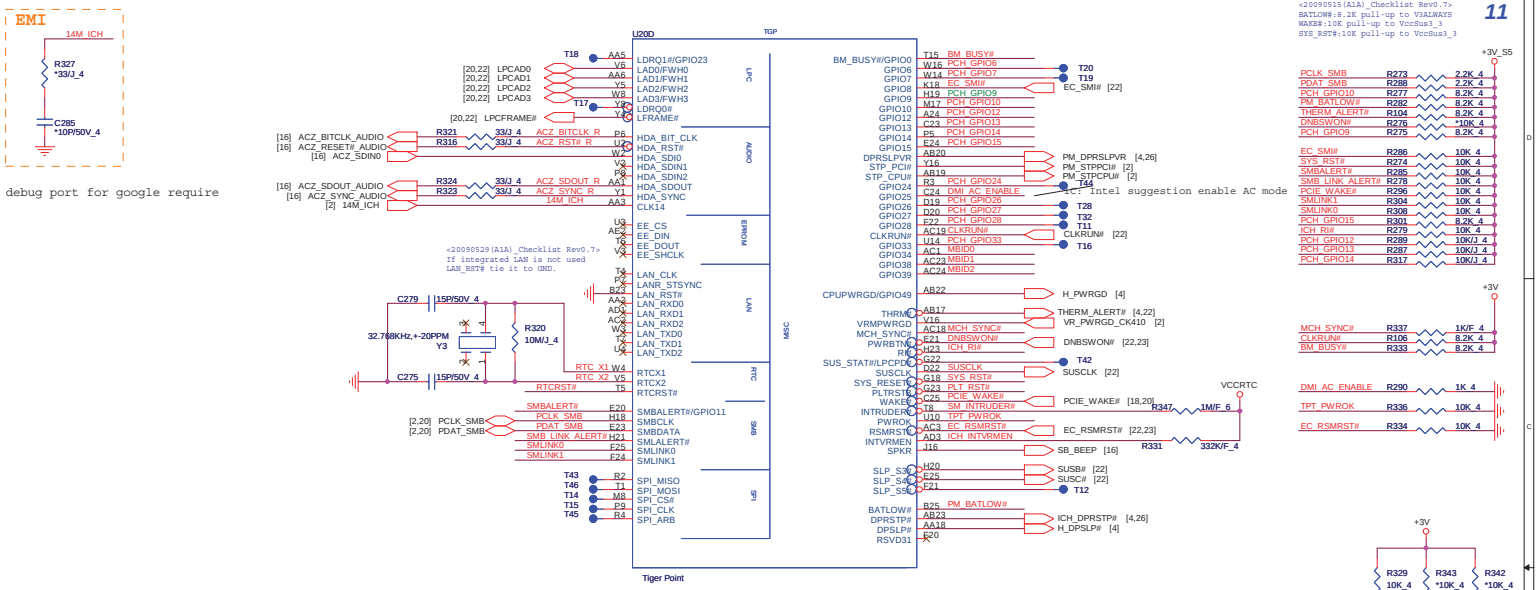
IRQ	Description
PIRQA	USB UHCI Controller #1, #4
PIRQB	AC'97 Codec; option for SMBUS
PIRQC	USB UH Controller #3; SATA/IDE Native Mode
PIRQD	USB UHCI Controller #2
PIRQE	Internal LAN; Option for SCI, TCO, HPET#0,1,2
PIRQF	Option for SCI, TCO, HPET#0,1,2
PIRQG	Option for SCI, TCO, HPET#0,1,2
PIRQH	USB EHCI Controller; Option for SCI, TCO, HPET#0,1,2

PCI_GNT#2	Internal PU Should not be PD

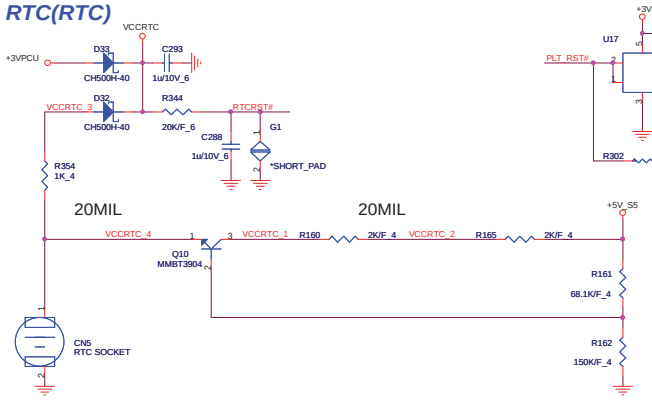
Quanta Computer Inc.

PROJECT : ZE6

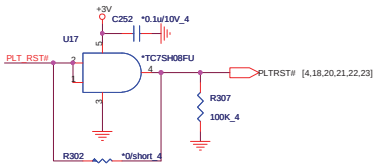
Size	Document Number	Rev
	TigerPoint PCI(3/6)	1B
Date: Friday, March 11, 2011	Sheet 10 of 35	



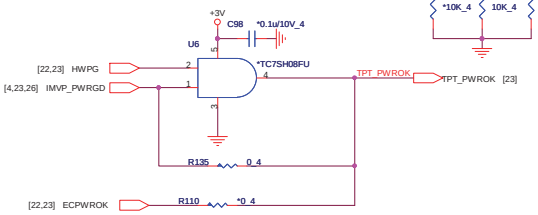
RTC(RTC)



Platform Reset



TPT Power OK



ACZ_SDOUT (INT PD)	ACZ_SYNC (INT PD)	Description
0	0	★ 4 x 1s
1	0	Reserved
0	1	Reserved
1	1	1 x 4s(1 port/4 lanes)

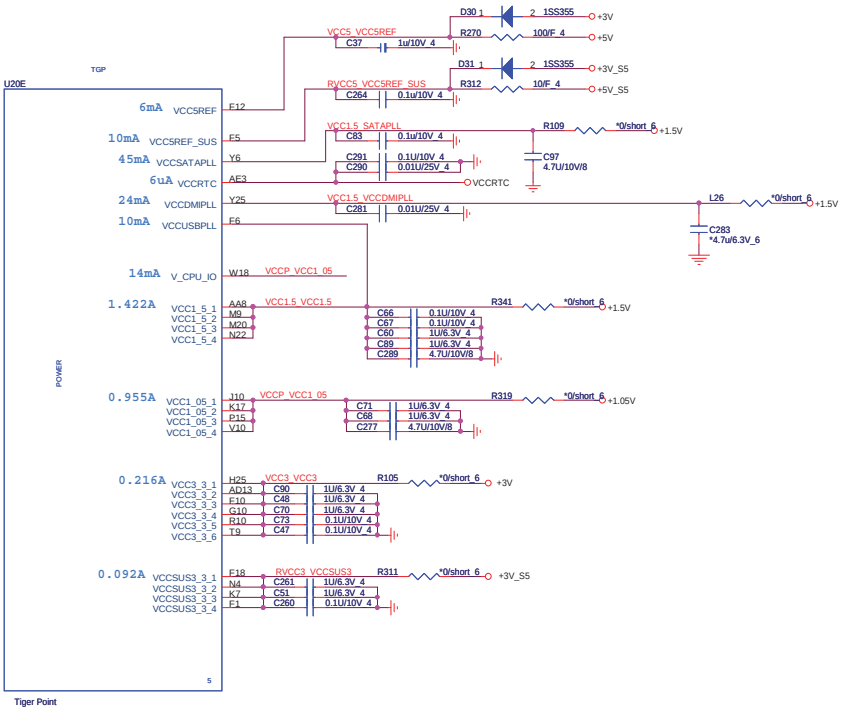
INTVRMEN	
1	Enable internal VccSus1_5 VRM (default)
0	Disable

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZE6

Size	Document Number	Rev
	TigerPoint GPIO	1A
Date: Friday, March 11, 2011	Sheet 11 of 35	

<Layout note>
Place 0402 caps close to ball
Place 0603/0805 caps close to ICH

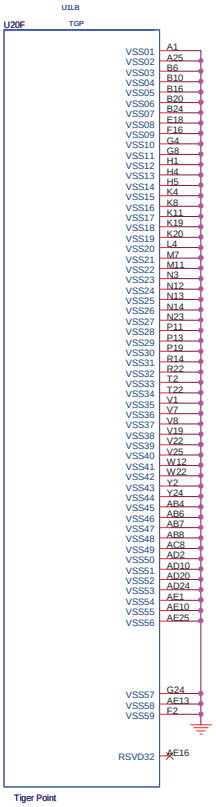


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZE6

Size	Document Number	Rev
	TigerPoint Power	1B

Date: Friday, March 11, 2011 Sheet 12 of 35



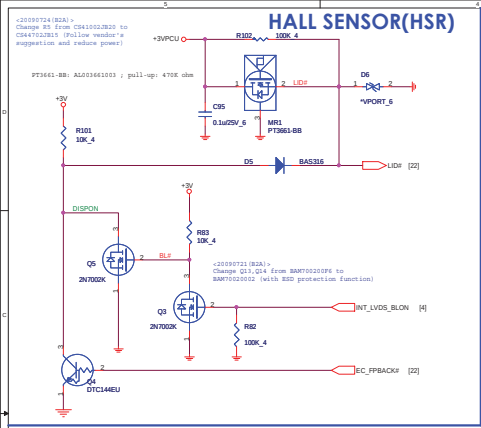
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZE6

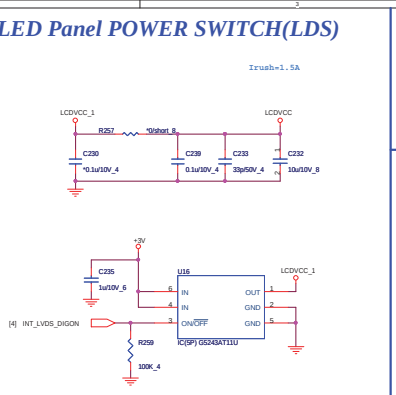
Size	Document Number	Rev
	TigerPoint GND	1B

Date: Friday, March 11, 2011 Sheet 13 of 35

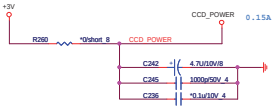
HALL SENSOR(HSR)



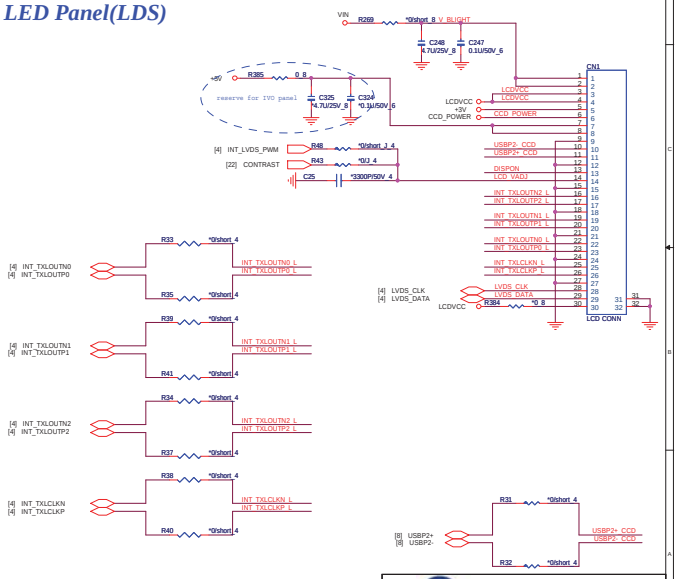
LED Panel POWER SWITCH(LDS)



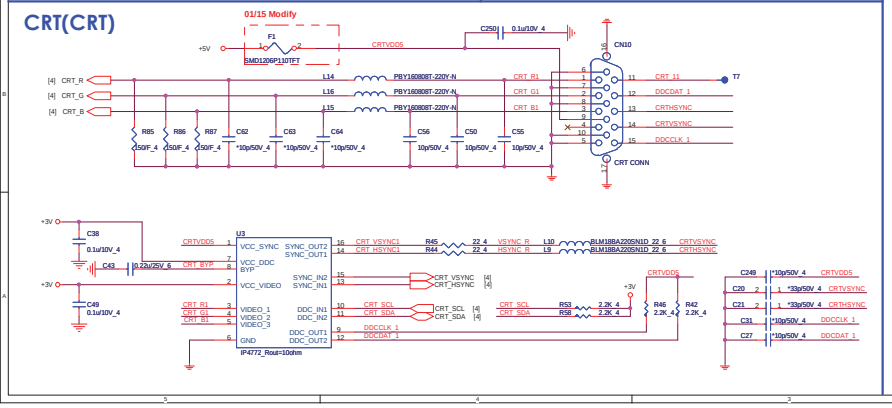
CAMERA POWER(CCD)



LED Panel(LDS)



CRT(CRT)



Quanta Computer Inc.
PROJECT : ZE6
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CRT/LVDS
1B
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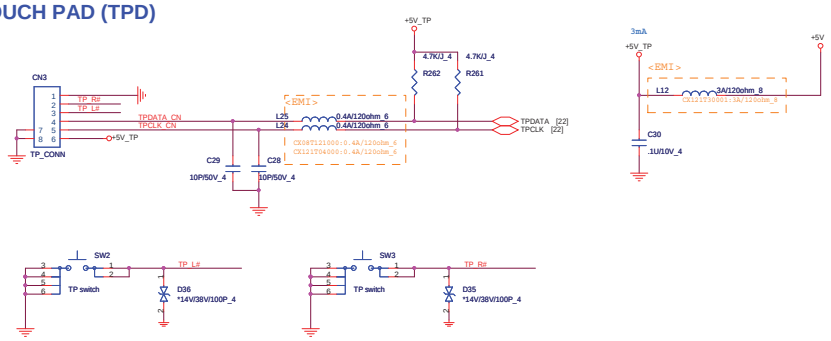
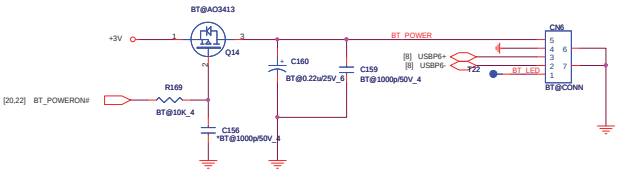
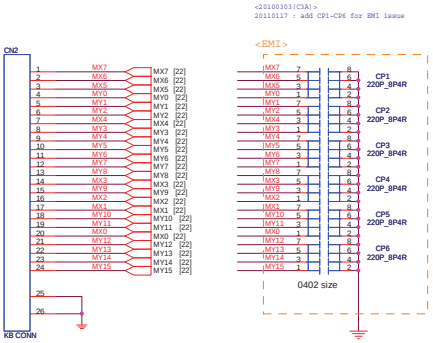
TOUCH PAD (TPD)



BLUETOOTH(BTM)

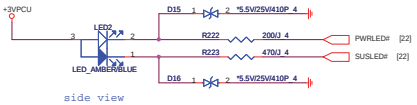


KEYBOARD (KBC)



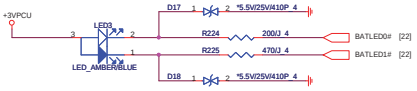
LED/SW (UIF)

PWR LED / SUS LED



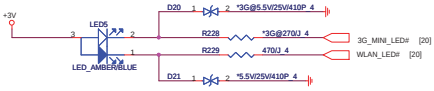
side view

FULL LED / CHG LED



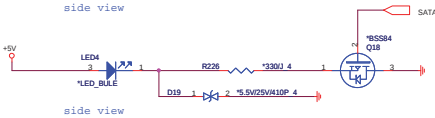
side view

3G LED / WLAN LED



side view

HDD LED

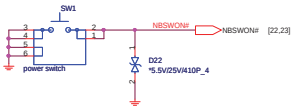


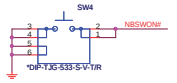
side view

PWR: Blue Vf: 2.55~3.15V, If=20mA
SUS: Orange Vf=1.6~2.0V, If=20mA

PWR indicator

PWR Button





W/O 3G: use BE0R0083Z00
W 3G: use BEB00023ZA0

<20090609(A1A)_Checklist Rev1.0>
Need the buffer for LED driving capability since the IOL is 6mA only.

Quanta Computer Inc.		
PROJECT : ZE6		
Size	Document Number: KB/BT/TP/LED/Power Connector	Rev 1B
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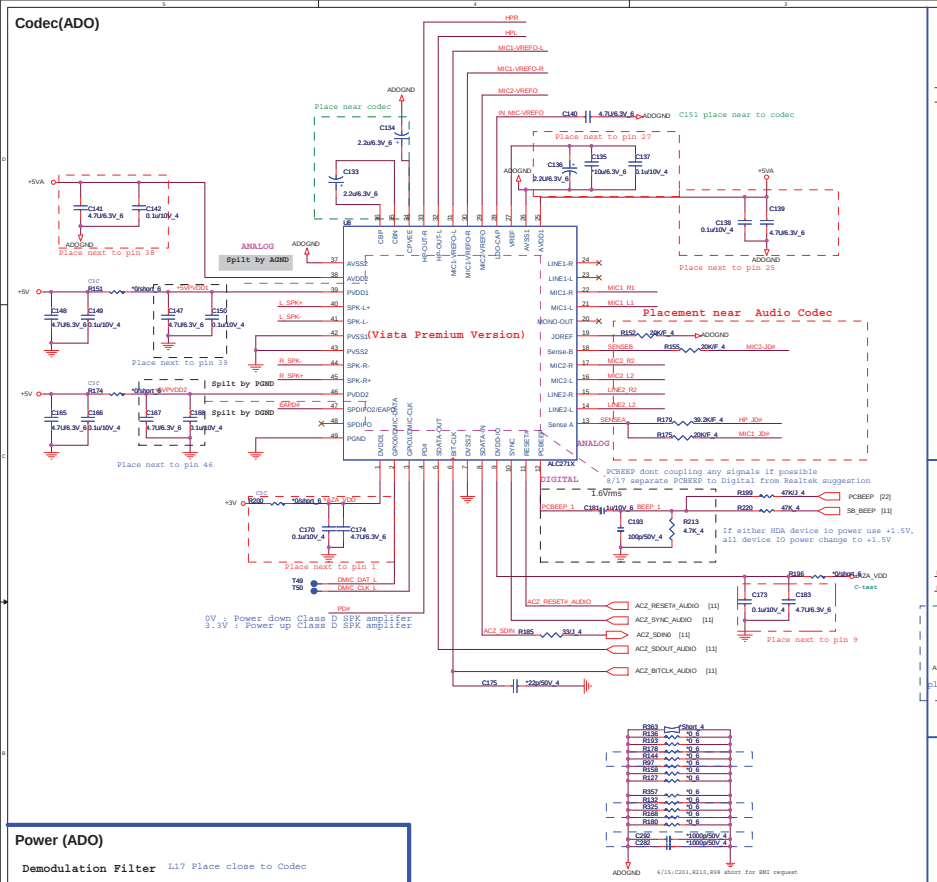
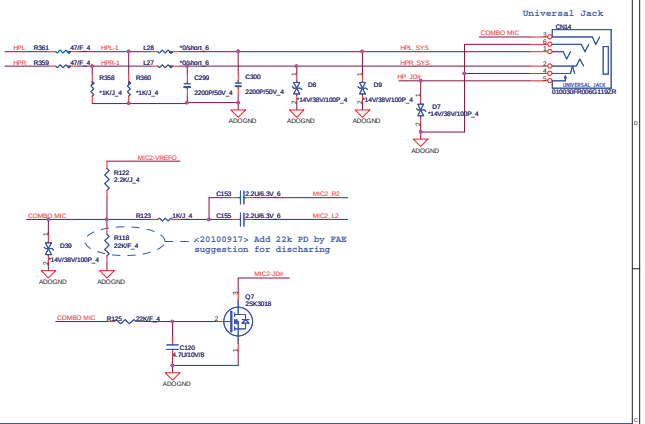
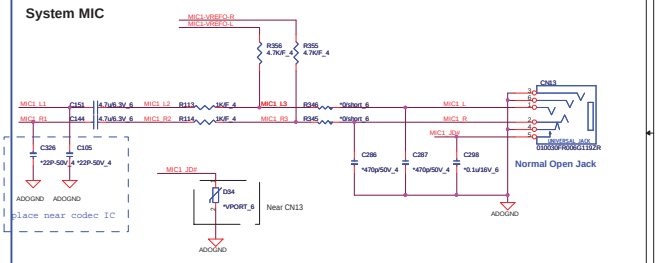
Codec(ADO)



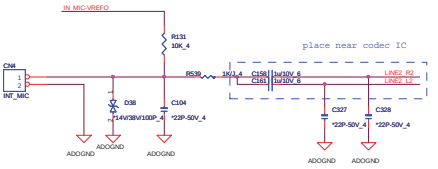
HEADPHONE



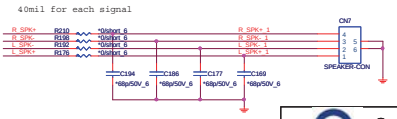
System MIC



Internal Analog MIC

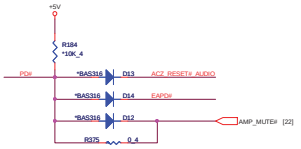


Internal Speaker



Power (ADO)

Mute(ADO)



Quanta Computer Inc.			
PROJECT : ZE6			
Size	Document Number		Rev
	AUO/AMP		1A
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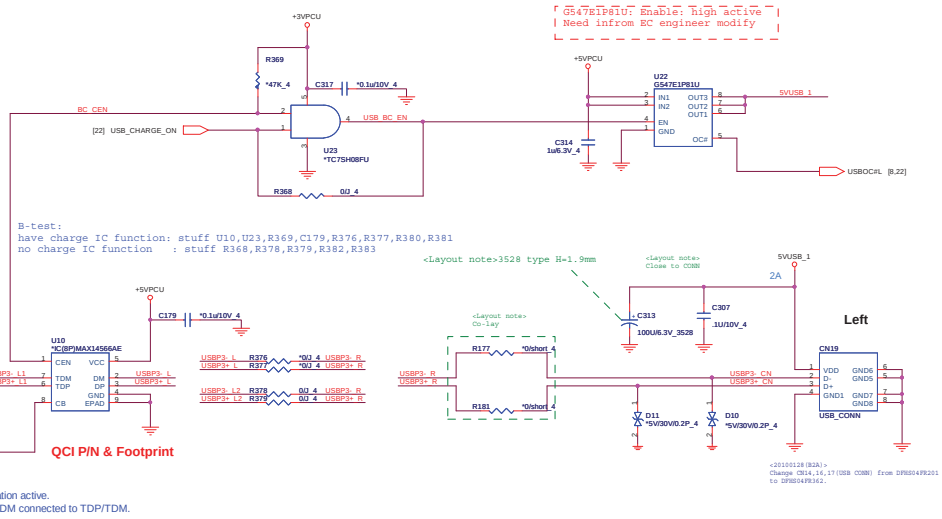
USB for iPod charge (USB)

Enable USB Charger						
	AC		DC(Battery > Setting%)		DC(Battery < Setting%)	
	S3	S4/S5	S3	S4/S5	S3	S4/S5
Charge Feature	O	O	O	O	△ (Note 1)	X
Wake Feature	X		X		X	

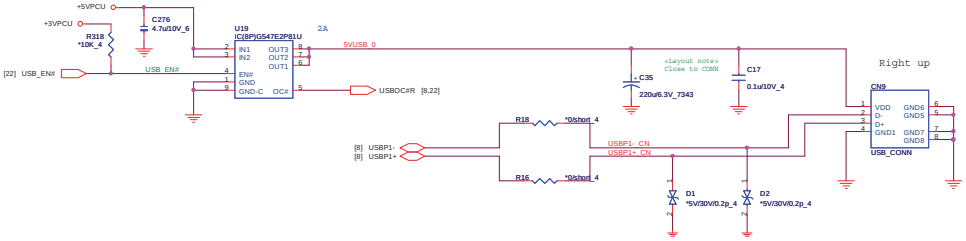
Disable USB Charger						
	AC		DC(Battery > Setting%)		DC(Battery < Setting%)	
	S3	S4/S5	S3	S4/S5	S3	S4/S5
Charge Feature	△ (Note 1)	X	△ (Note 1)	X	△ (Note 1)	X
Wake Feature	O		O		O	

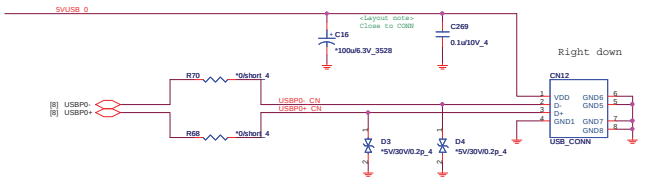
Note.1 Devices can be charged or not should same as other USB ports



System Status: .
> Lo: AM, autodetection charger identification active.
> HI: PM, pass-through mode active, DP/DM connected to TDP/TDM.

USB(USB)





Quanta Computer Inc.
PROJECT : ZE6
Size | Document Number: USB on Board/LED/SW/HOLE | Rev: 1B
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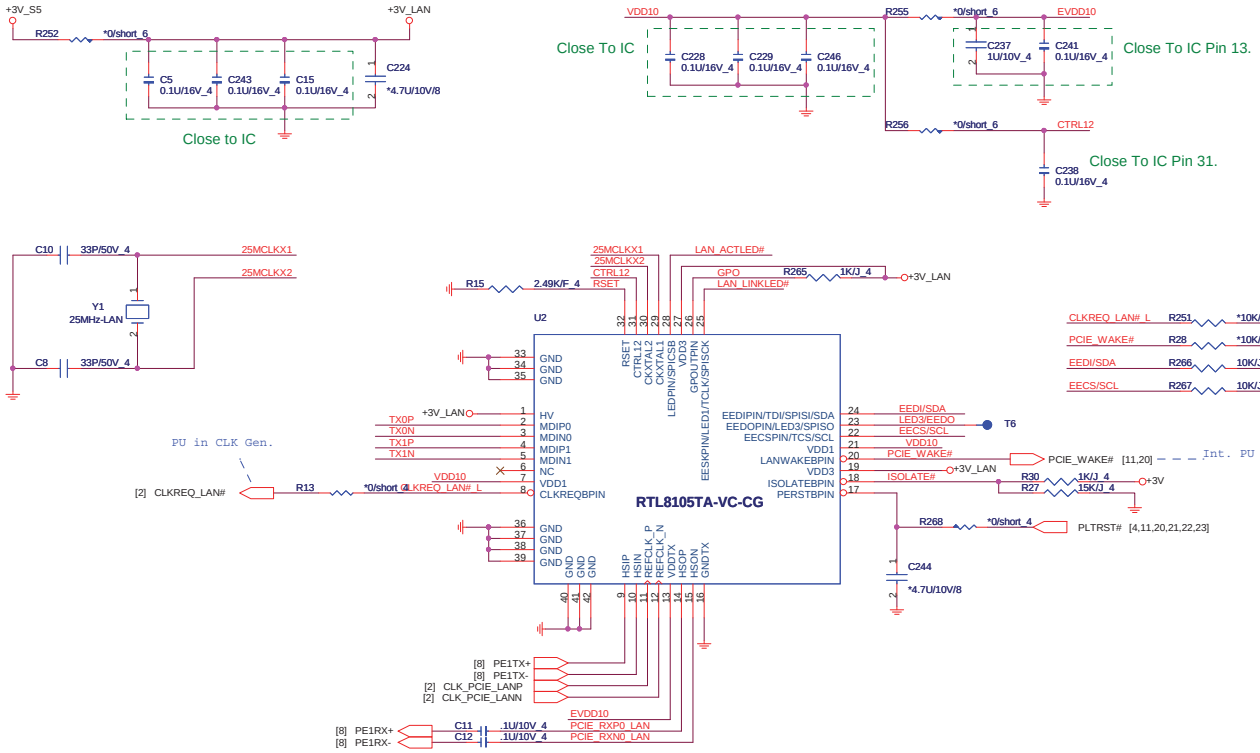
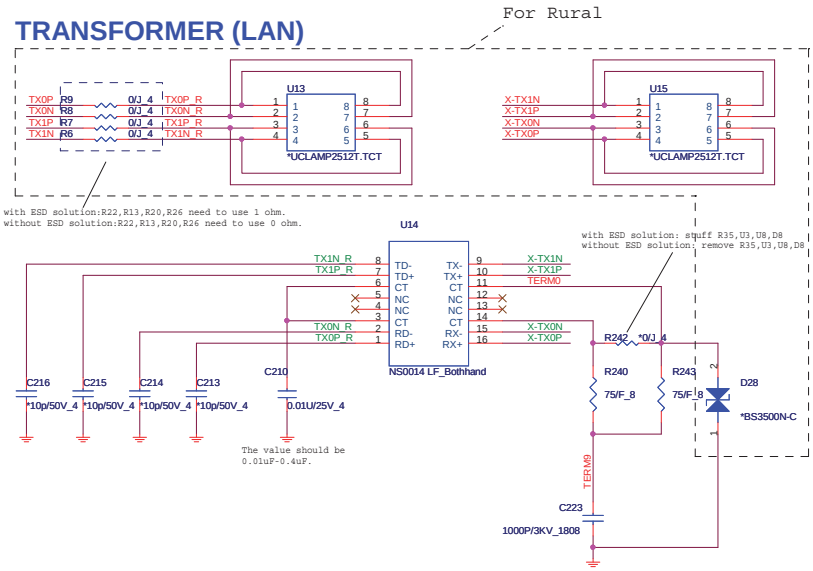
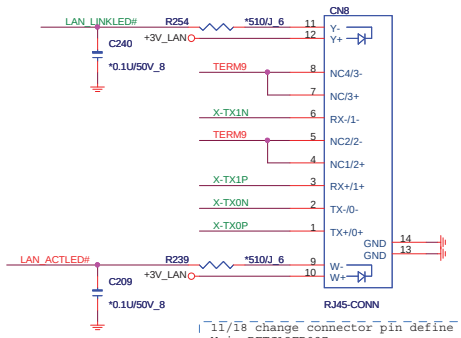
LAN (LAN)



TRANSFORMER (LAN)



RJ45 Connector (LAN)



Quanta Computer Inc.

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Size	Document Number	Rev
	LAN RTL8105TA-VC-CG	1B

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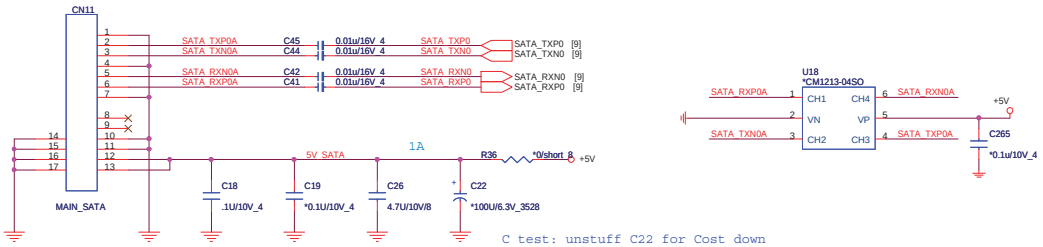

C test: unstuff C22 for Cost down

Quanta Computer Inc.		
PROJECT : ZE6		
Size	Document Number	Rev
	SATA-HDD	1B
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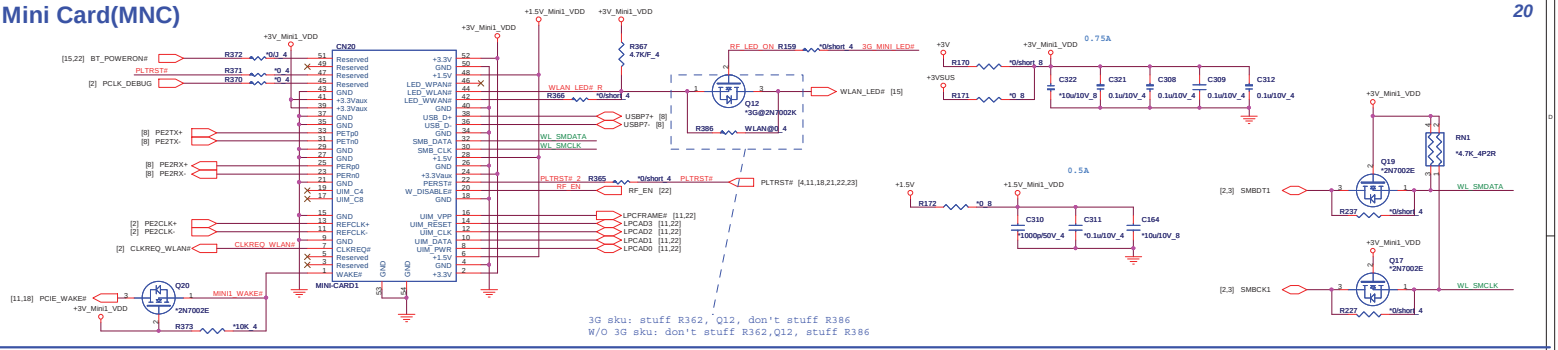
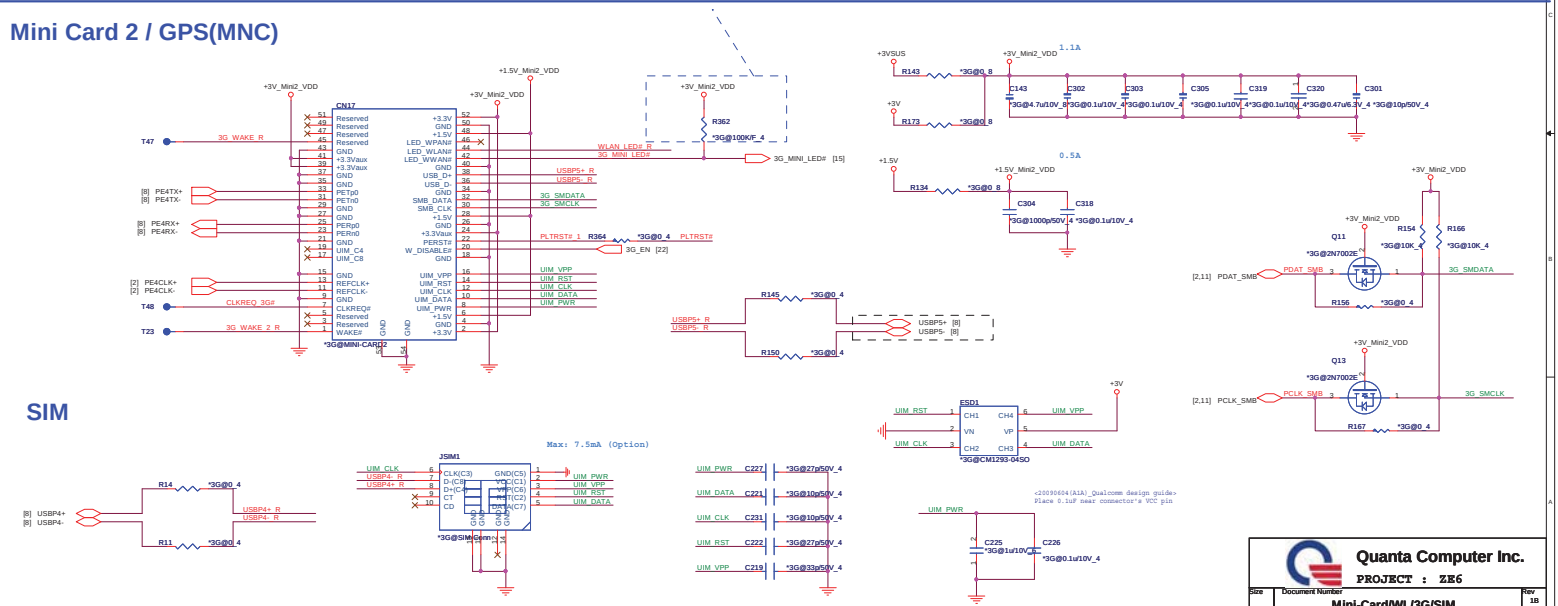
Mini Card(MNC)



Mini Card 2 / GPS(MNC)



SIM

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PROJECT : ZE6			
Size	Document Number		Rev
	Mini-Card/WL/3G/SIM		1B
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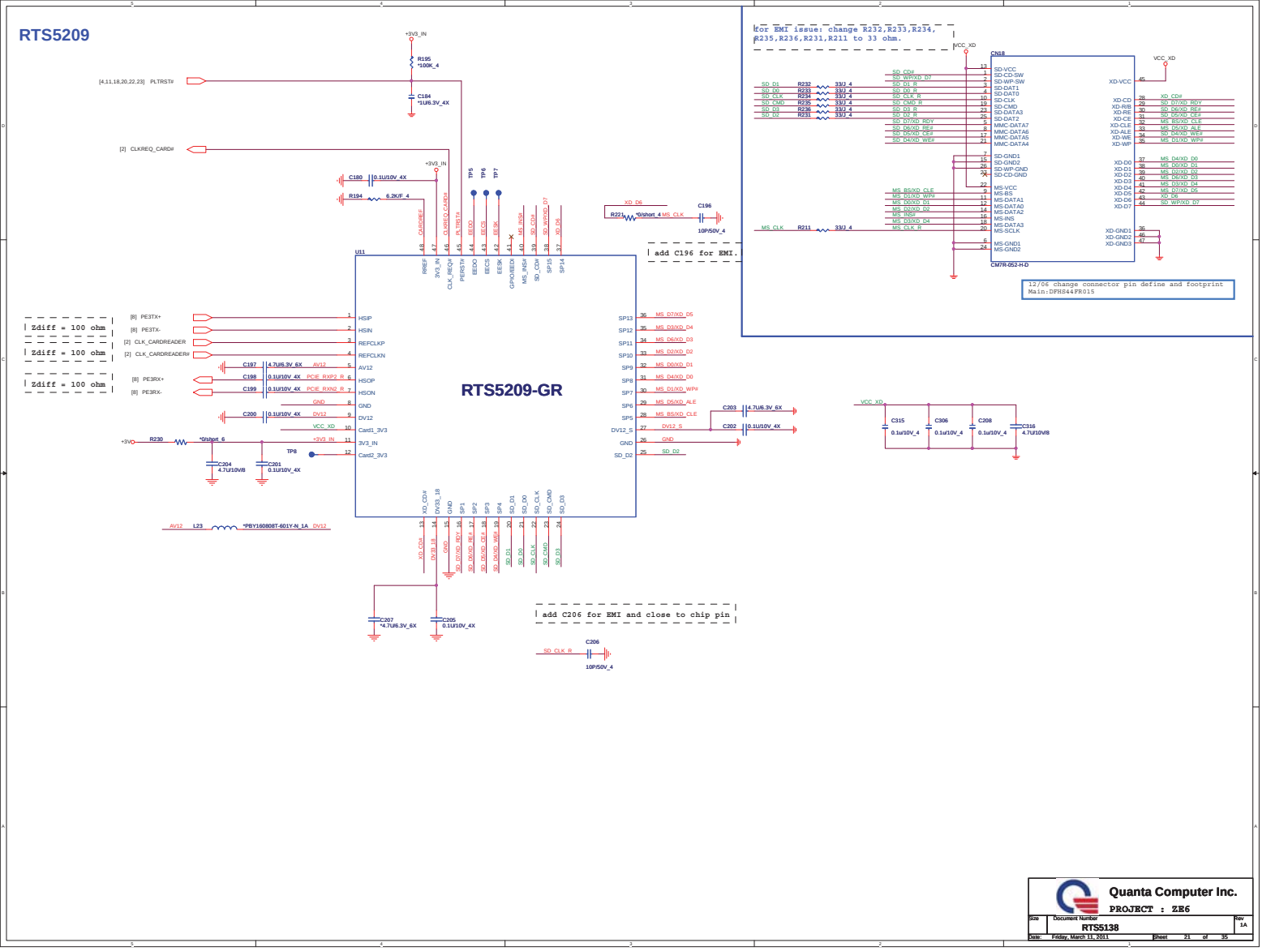

Quanta Computer Inc.			
PROJECT : ZE6			
Size	Document Number		Rev
	RTS5138		1A
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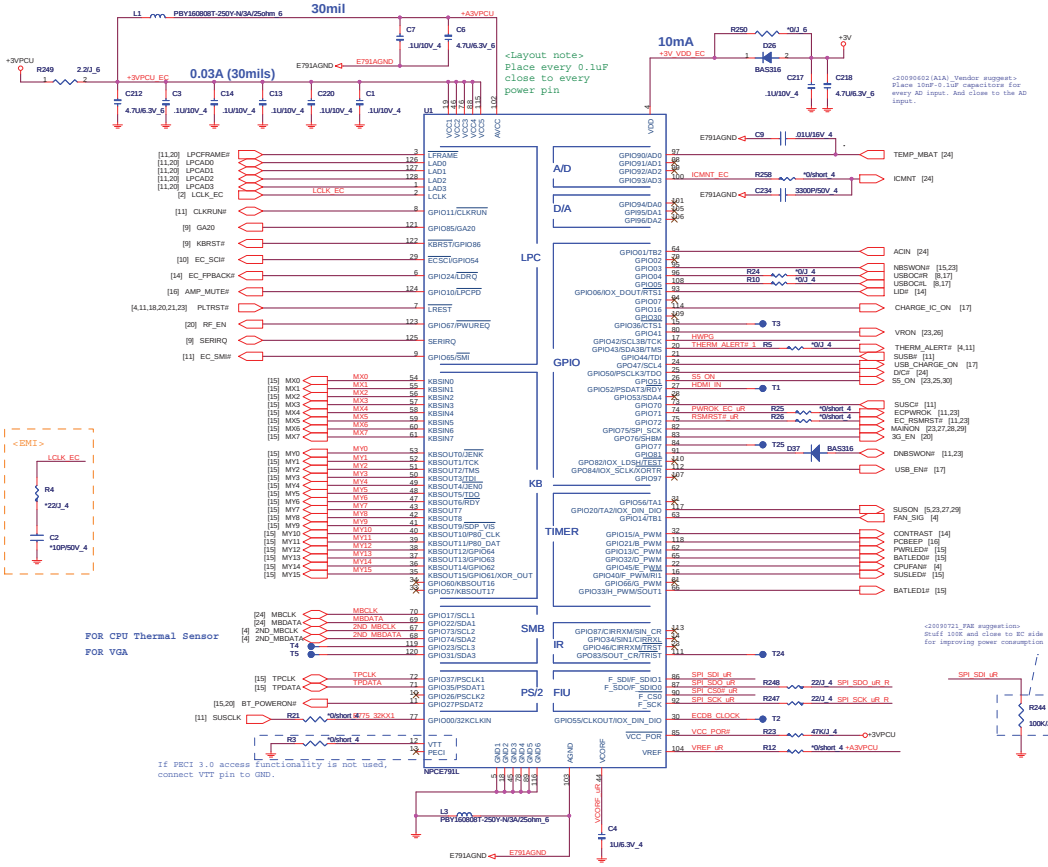
EC (KBC)



I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

SHBM — 3G_EN — R22 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

BATLED0# R17 100K/J_4
BATLED1# R29 100K/J_4

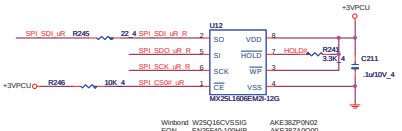
<20090831(AIA)_EC team suggest>
1.change R7027/R7028 to 1M or 100K ohm
2.change PWR/SUS LED's power from +3VPCU to +3V_S5 or +3VSUS
can reduce pull-high resistor of SUSLED#/PWRLED#

SM BUS PU(KBC)

MBCLK R20 4.7K/J_4
MBDATA R19 4.7K/J_4

2ND_MBCLK R264 10K_4
2ND_MBDATA R263 10K_4

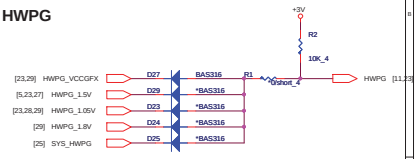
SPI FLASH(KBC)



Winbond W25Q16CVSSIG AKE38ZP0N02
EON EN25F40-100HIP AKE38ZA0Q00
MXIC MX25L1606EM2I-12G AKE38FP0Z01

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG



INTERNAL KEYBOARD STRIP SET (KBC)

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU thermal sensor

INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.			
PROJECT : ZE6			
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	WPCE781 & FLASH		1A
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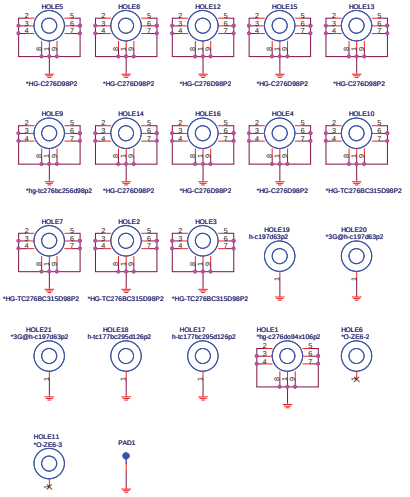
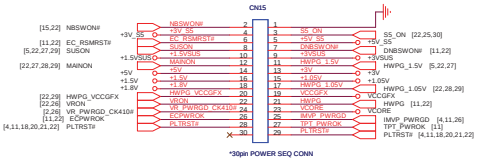
EMI

Hole



Power Sequence Connector 30pin (CPU)



1	GND	11	HWPG_1.5V	21	HWPG
2	NBSWON#	12	MAINON	22	VRON
3	S5_ON	13	+3V	23	VCORE
4	+3V_S5	14	+5V	24	VR_PWRGD_CK410#
5	+5V_S5	15	+1.05V	25	IMVP_PWRGD
6	EC_RSMRST#	16	+1.5V	26	ECPWROK
7	DNBSWON#	17	HWPG_1.05V	27	TPT_PWROK
8	SUSON	18	+1.8V	28	H_PWRGD
9	+3VSUS	19	VCCGFX	29	PLTRST#
10	+1.5VSUS	20	HWPG_VCCGFX	30	RESERVE

Quanta Computer Inc.

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Size	Document Number	Rev
	HDMI(1/2)	1A

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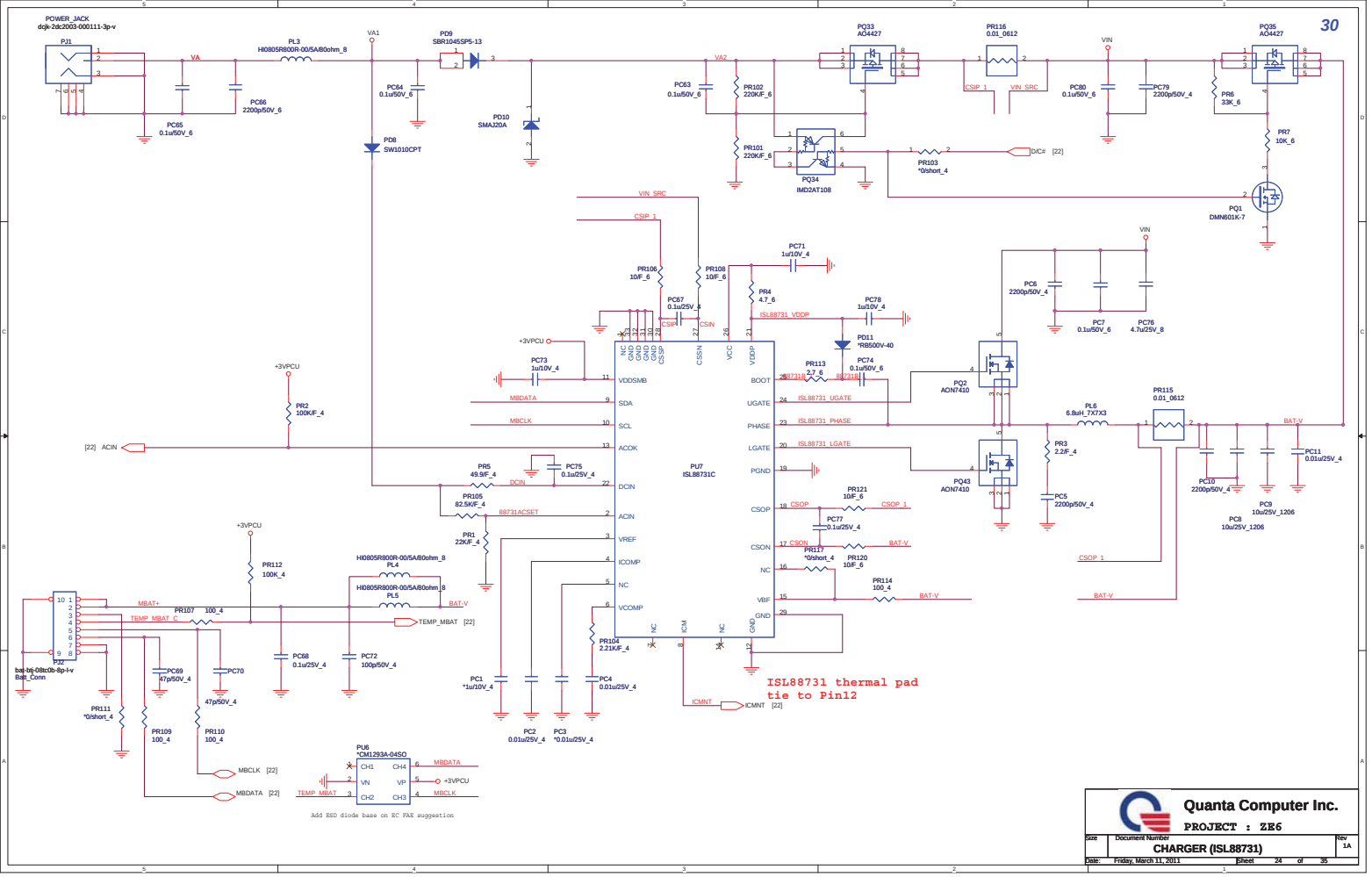
POWER_JACK
dcjk-2dc2003-000111-3p-v
PJ1
PL3
HI0805R600R-00/5A/80ohm_8
PD9
SBR1045SP5-13
PD8
SW1010CPT
PD10
SMAJ20A
PC64
0.1u/50V_6
PC65
0.1u/50V_6
PC66
2200p/50V_6
PC63
0.1u/50V_6
PR102
220K/F_6
PR101
220K/F_6
PQ33
AO4427
PQ34
IMD2A7108
PR116
0.01_0612
PR103
*0/short_4
PC30
0.1u/50V_6
PC79
2200p/50V_4
PQ35
AO4427
PR6
33K_6
PR7
10K_6
PQ1
DMN601K-7
PC71
1u/10V_4
PR106
10/F_6
PR108
10/F_6
PR4
4.7_6
PC67
0.1u/25V_4
PC78
1u/10V_4
PD11
*RB500V-40
PC73
1u/10V_4
PR113
2.7_6
PC74
0.1u/50V_6
PQ2
AON7410
PQ43
AON7410
PC6
2200p/50V_4
PC7
0.1u/50V_6
PC76
4.7u/25V_8
PR2
100K/F_4
PR5
49.9/F_4
PC75
0.1u/25V_4
PR105
82.5K/F_4
PR1
22K/F_4
PU7
ISL88731C
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
PR121
10/F_6
PC77
0.1u/25V_4
PR117
*0/short_4
PR120
10/F_6
PR114
100_4
PL6
6.8uH_7X7X3
PR115
0.01_0612
PR3
2.2/F_4
PC5
2200p/50V_4
PC10
2200p/50V_4
PC8
10u/25V_1206
PC9
10u/25V_1206
PC11
0.01u/25V_4
PR112
100K_4
PL4
HI0805R800R-00/5A/80ohm_8
PL5
HI0805R800R-00/5A/80ohm_8
PR107
100_4
PJ2
bat-blj-08tc0b-8p-l-v
Batt_Conn
PC68
0.1u/25V_4
PC72
100p/50V_4
PC69
47p/50V_4
PC70
47p/50V_4
PR111
*0/short_4
PR109
100_4
PR110
100_4
PC1
*1u/10V_4
PC2
0.01u/25V_4
PC3
*0.01u/25V_4
PC4
0.01u/25V_4
PR104
2.21K/F_4
PU6
*CM1293A-04SO
ISL88731 thermal pad
tie to Pin12
Add ESD diode base on EC PAR suggestion
Quanta Computer Inc.
PROJECT : ZE6
CHARGER (ISL88731)
Size
Document Number
Rev
1A
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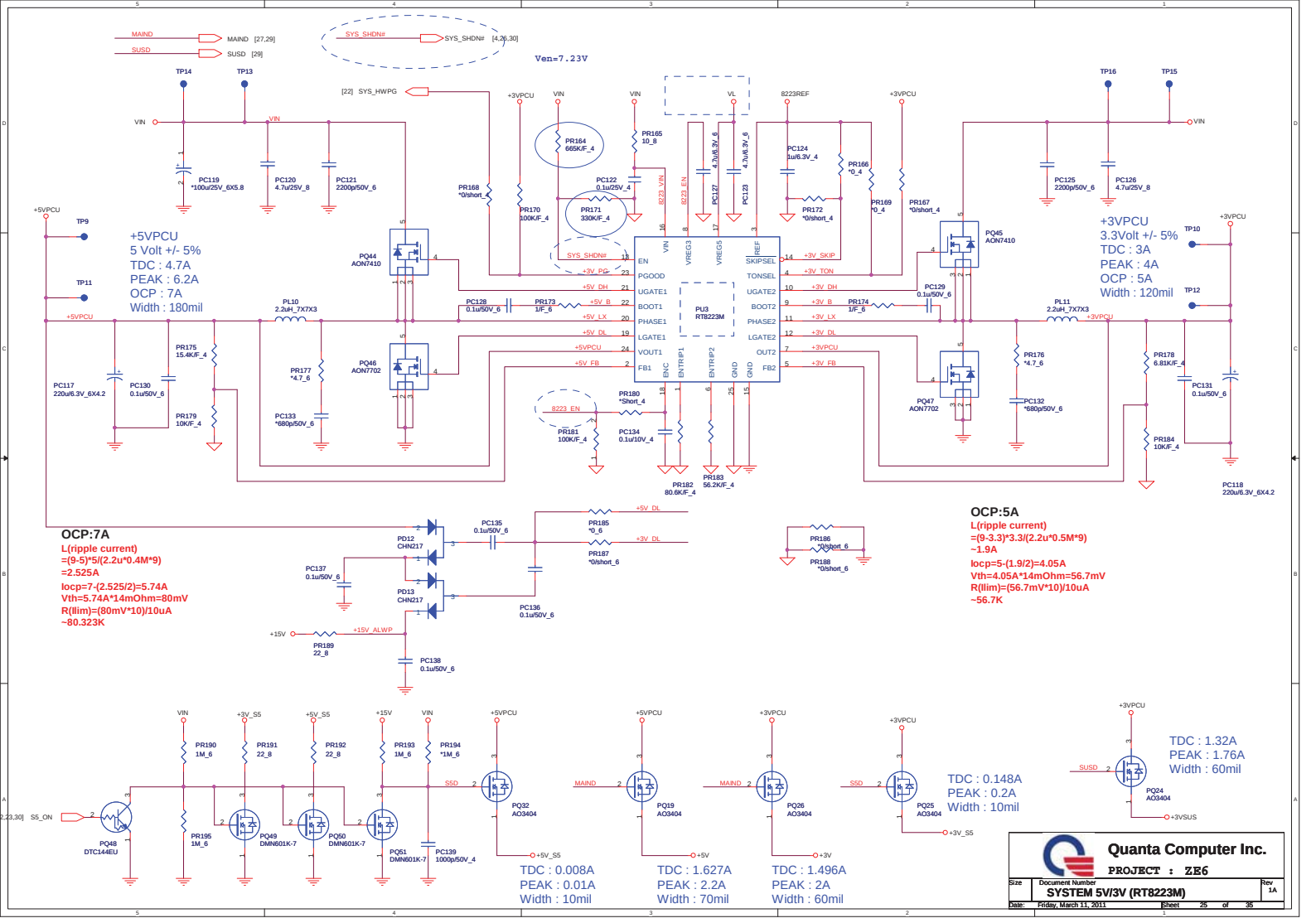

Quanta Computer Inc.

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Size	Document Number	Rev
	SYSTEM 5V/3V (RT8223M)	1A

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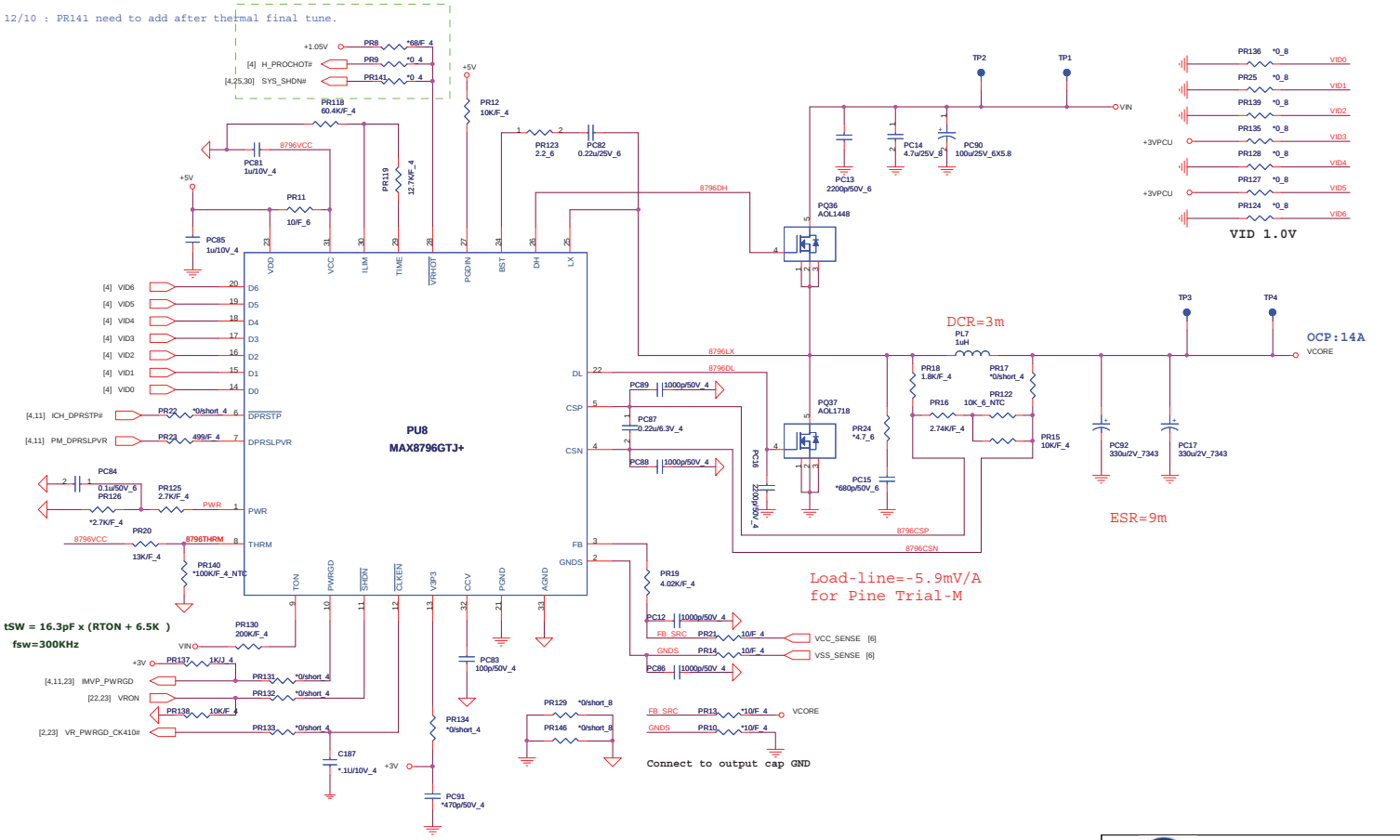
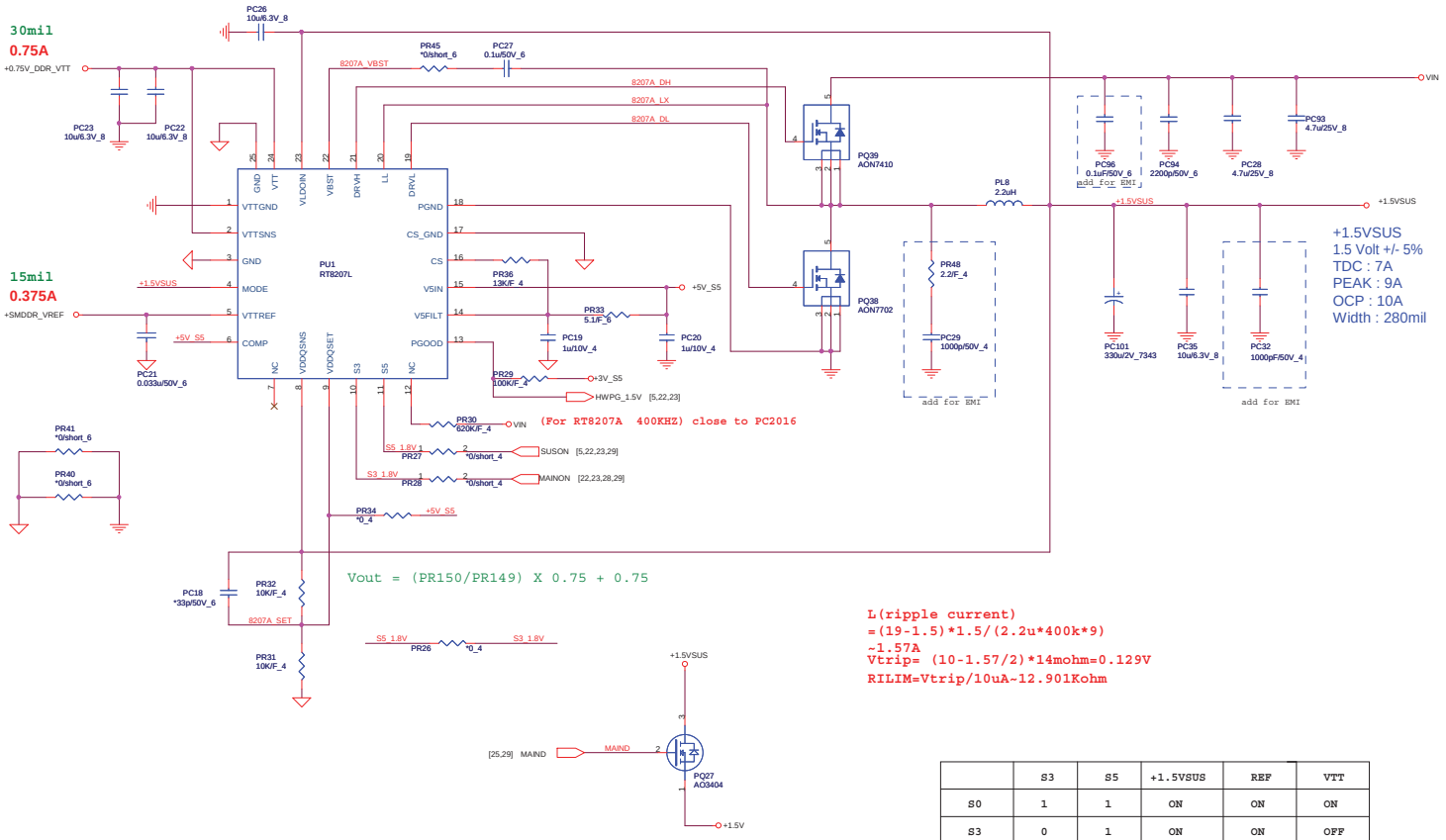
12/10 : PR141 need to add after thermal final tune.



[PWM]



L(ripple current)
=(19-1.5)*1.5/(2.2u*400k*9)
~1.57A
Vtrip= (10-1.57/2)*14mohm=0.129V
RILIM=Vtrip/10uA~12.901Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
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Size | Document Number: DDR 1.5V(TPS51116) | Rev 1A
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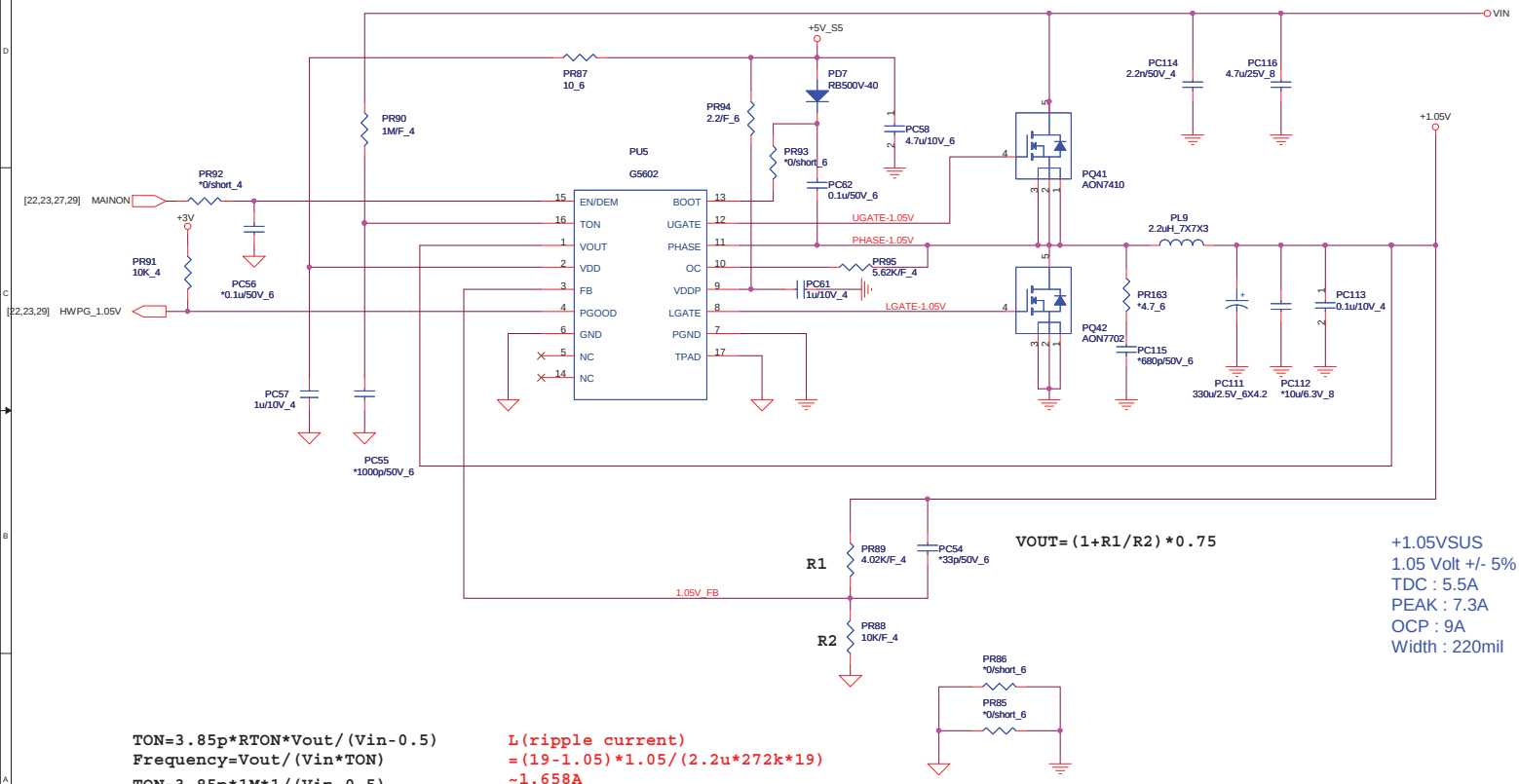

VOUT=(1+R1/R2)*0.75

+1.05VSUS
1.05 Volt +/- 5%
TDC : 5.5A
PEAK : 7.3A
OCP : 9A
Width : 220mil

TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

L(ripple current)
=(19-1.05)*1.05/(2.2u*272k*19)
~1.658A
Rth=14m*(9-0.829)/20uA
RILIM=5.719Kohm

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	+1.05V(G5602)	1A
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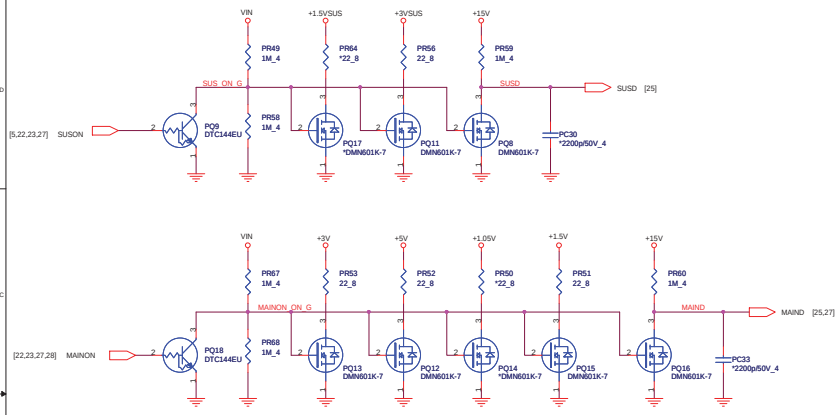
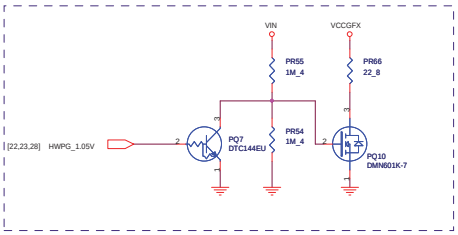
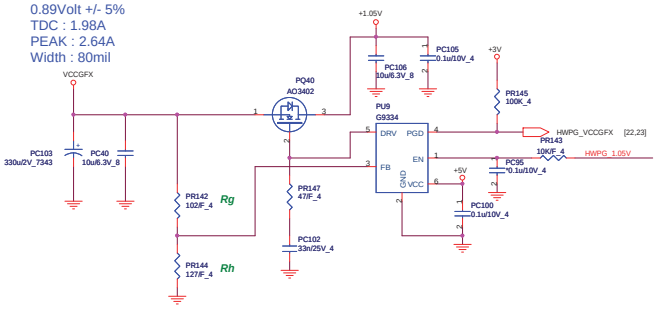
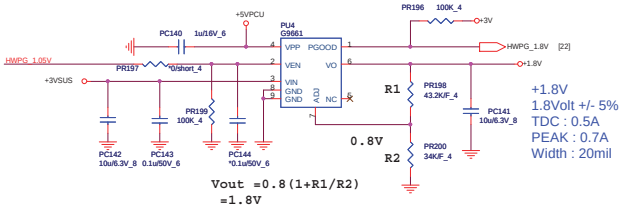




VCCGFX
0.89Volt +/- 5%
TDC : 1.98A
PEAK : 2.64A
Width : 80mil



*Vout1 = (1+Rg/Rh)*0.5*



Vout =0.8(1+R1/R2)
=1.8V

+1.8V
1.8Volt +/- 5%
TDC : 0.5A
PEAK : 0.7A
Width : 20mil

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	Discharge/1.8V	1A
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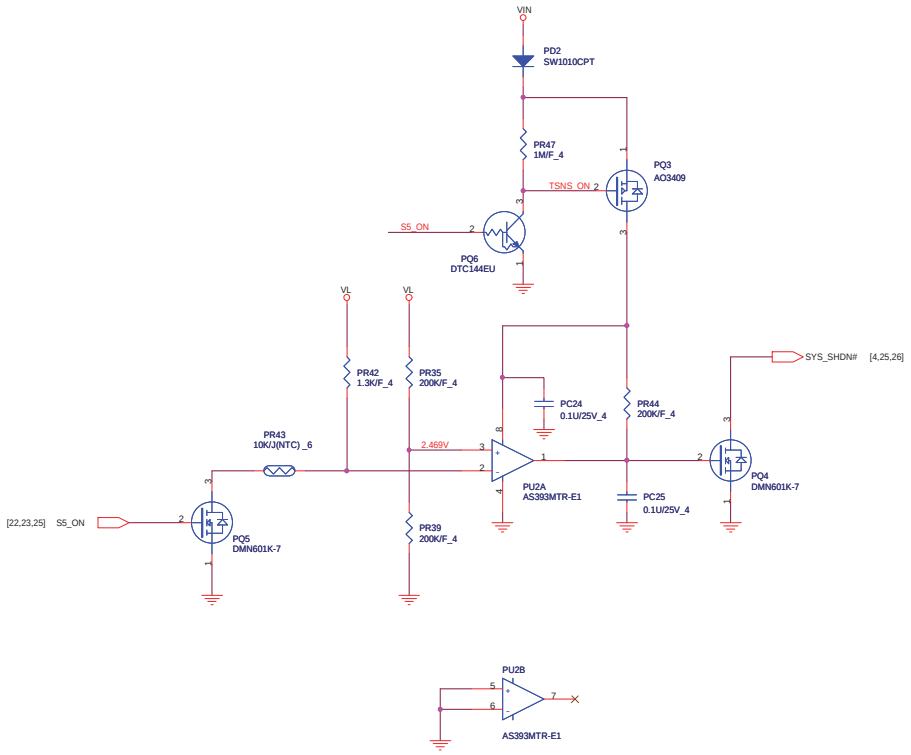
Thermal Protection (DCD)



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Size	Document Number	Rev
	Thermal protect	1A

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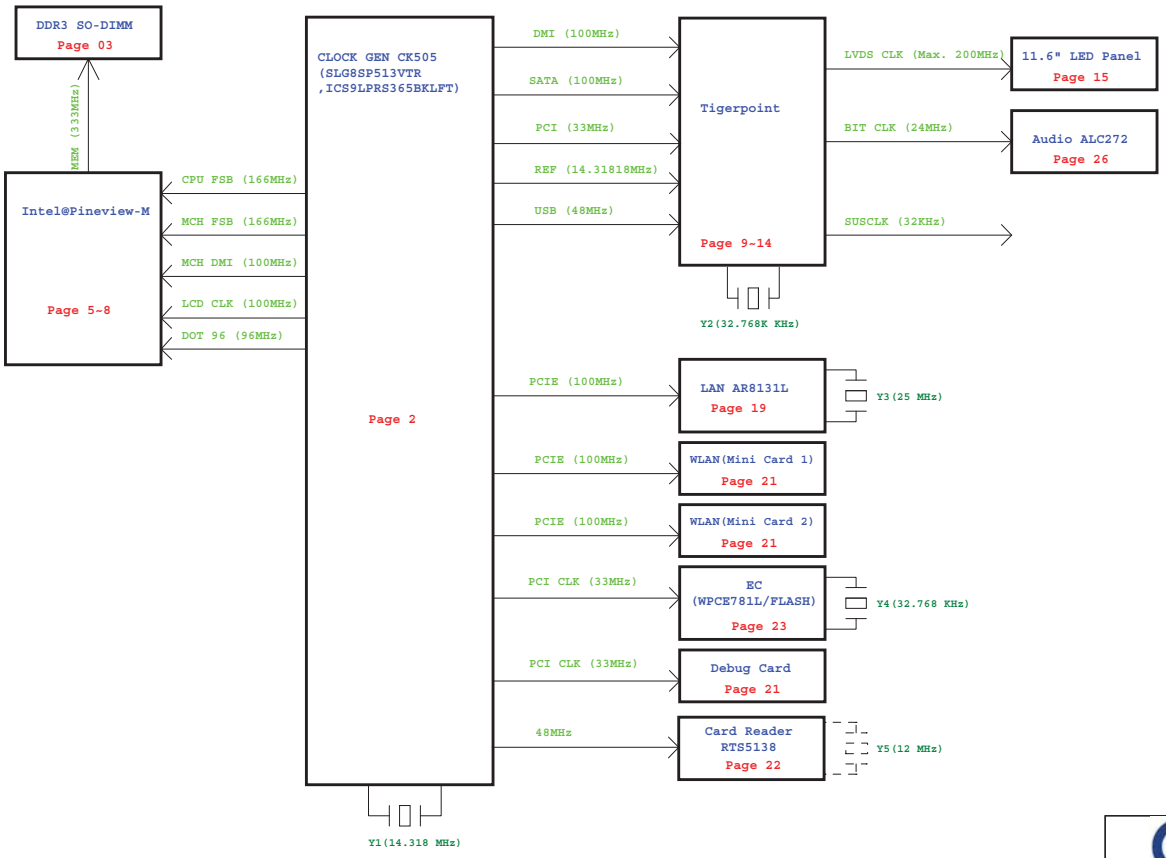

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Size	Document Number	Rev
	Clock Distribution Diagram	1B

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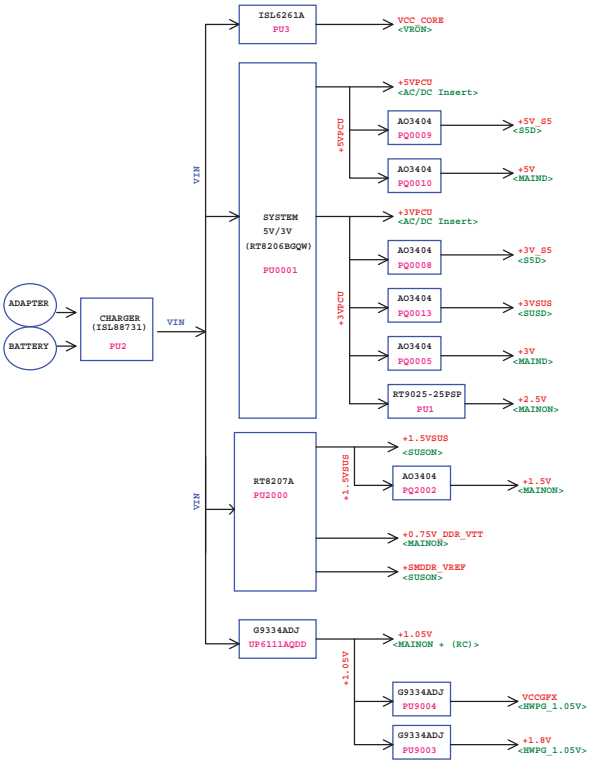
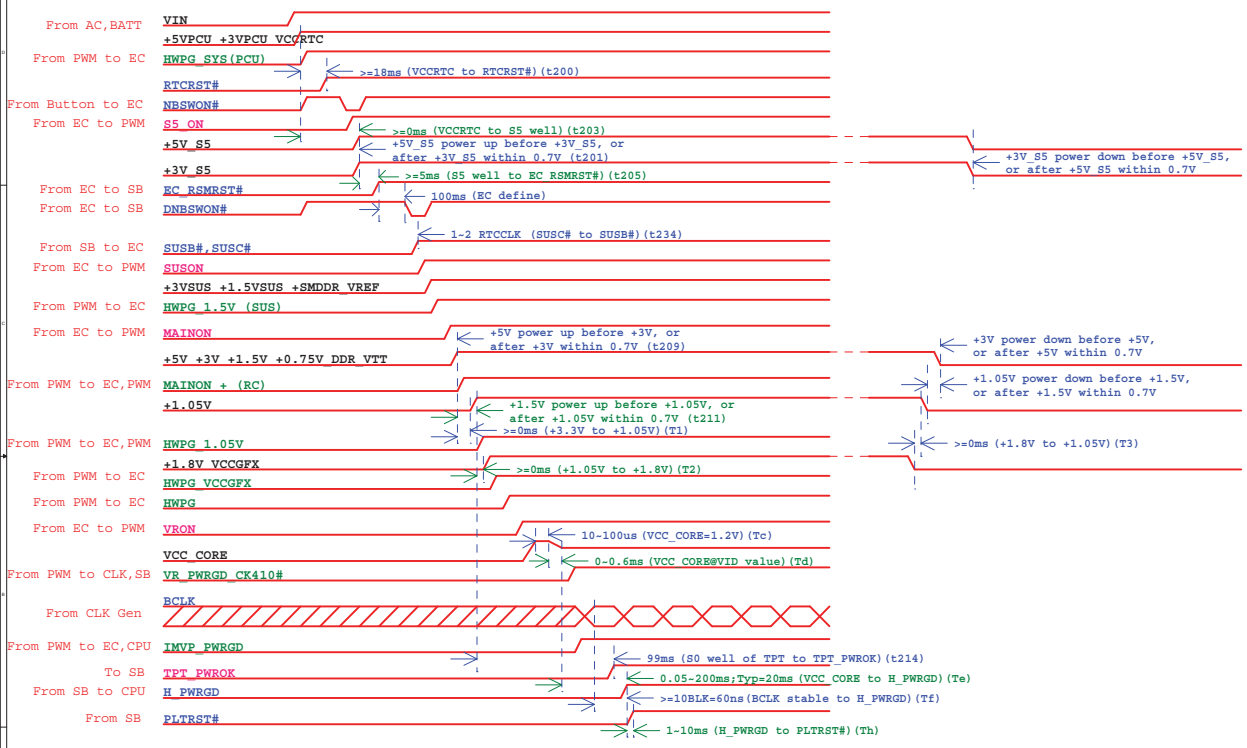


POWER	Distribution
VIN	LCD Backlight
VCC_CORE	CPU
+5VPCU	USB Connecter
+5V_S5	RTC, TPT
+5V	TPT , CRT , TouchPad , Codec , SATA , FAN , HDMI
+3VPCU	RTC, Hall Sensor, Light Sensor, EC, BIOS
+3V_S5	TPT , LAN , LAN EEPROM , RJ45 LED
+3VSUS	3G
+3V	CLK_GEN, CPU, TPT , LCD , CCD, DMIC, BT, Codec, WLAN/Wimax, Card reader, EC, DDR, HDMI
+1.5VSUS	DDR
+1.8V	CPU, HDMI
+1.5V	CPU, TPT
+0.75V_DDR_VTT	DDR
+SMDDR_VREF	CPU, DDR
+1.05V	CLK_GEN , CPU, TPT
VCCGFX	CPU
+2.5V	HDMI

ZGA Power On Sequence



*Note: EC will sampling SUSB# & SUSC# every 5ms.

ICH SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)	Mini Card (3G)
(SMB_DATA)/(SMB_CLK) (+3V_S5)	V	V	V	V
Power Plane	+3V	+3V	+3V	+3V_SUS
MOS CKT (Level shift)	Stuff	Stuff	*Reserve	Stuff

*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor	
EC781 SDA1 / SCL1 (+3VPCU)	V		
EC781 SDA2 / SCL2 (+3V)		V	
EC781 SDA3 / SCL3 (+3VPCU)			
Power Plane	+3VPCU	+3V	
MOS CKT (Level shift)	X	X	

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SYSTEM INFORMATION
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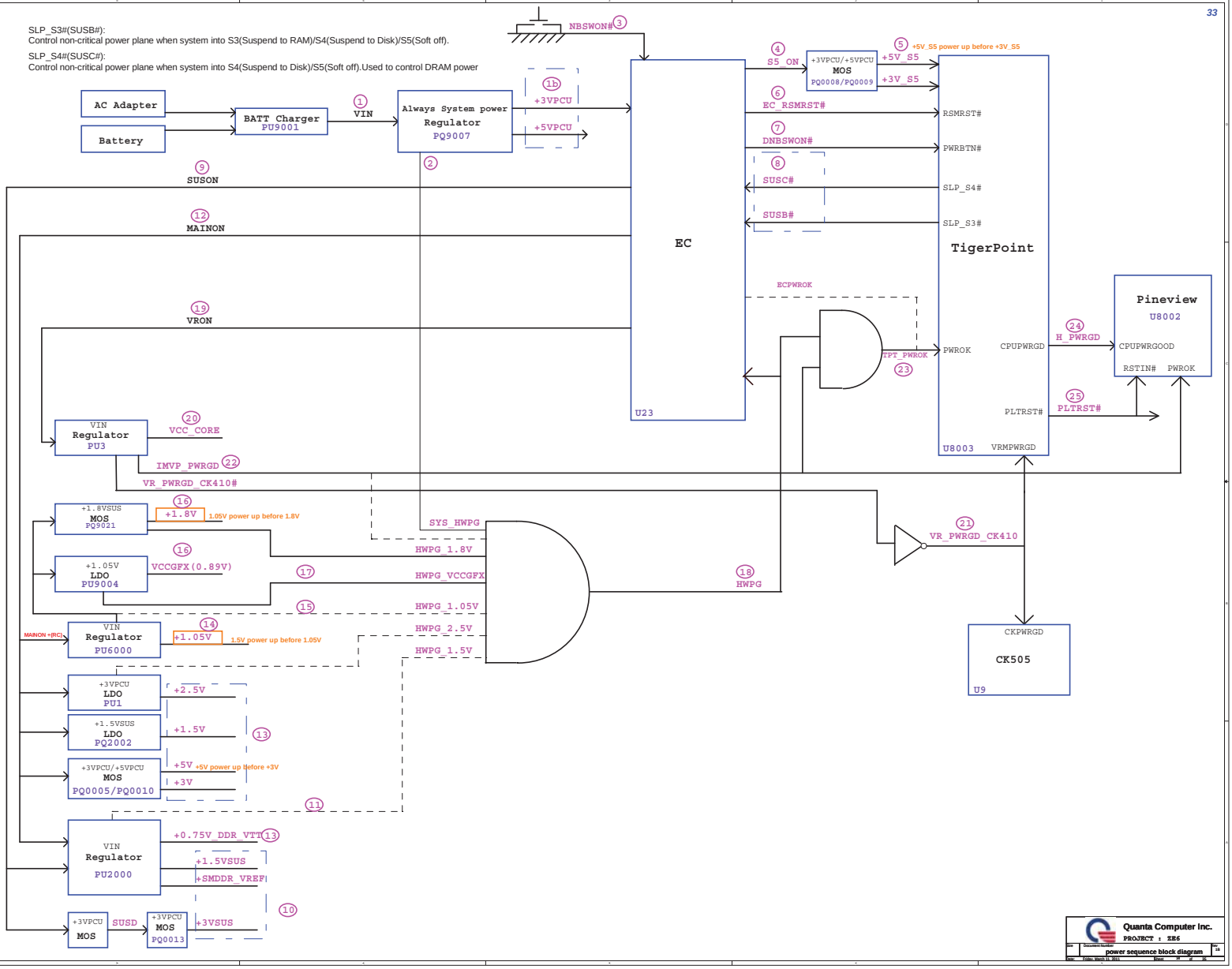
SLP_S3#(SUSB#):
Control non-critical power plane when system into S3(Suspend to RAM)/S4(Suspend to Disk)/S5(Soft off).

SLP_S4#(SUSC#):
Control non-critical power plane when system into S4(Suspend to Disk)/S5(Soft off).Used to control DRAM power



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power sequence block diagram

Model	REV	CHANGE LIST	MODEL	ZE6	
				FROM	To
ZE6 MB	A1	FIRST RELEASED: (PCB:A)		X	1A
	B	Page 2 : add R374 for CLK GEN change version			
		Page 11 : change RTC connector type from SMT to holder.			
		Page 15 : modify TP connector pin define			
		Page 16 : modify audio and mic connector pin define.			
		Page 17 : modify USB charger IC circuit to support or not support charger function.			
		Page 29 : modify 1.8V IC enable signal to HWPG_1.05V			
		20110117 Page 15 : add CP1-CP6 for EMI issue			
		20110117 Page 15 : for EMI issue: change R232,R233,R234,R235,R236,R231,R211 to bead CX5BB121001			
		20110118 Page 27 : for EMI issue: add PC96 ,PC32 and stuff PR48, PC29			
		20110118 Page 30 : Thermal temperature setting at 75C, change PR42 from 1.54K/F to 1.3K/F			
	B	20110131 Page 14 : add 5V into LCD connector for IVO panel to use.			
	1D				

DOC NO.						
	PROJECT MODEL :	11.6	APPROVED BY:		DATE:	2009/12/05
	PART NUMBER:		DRAWING BY:		REVISON:	1B

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