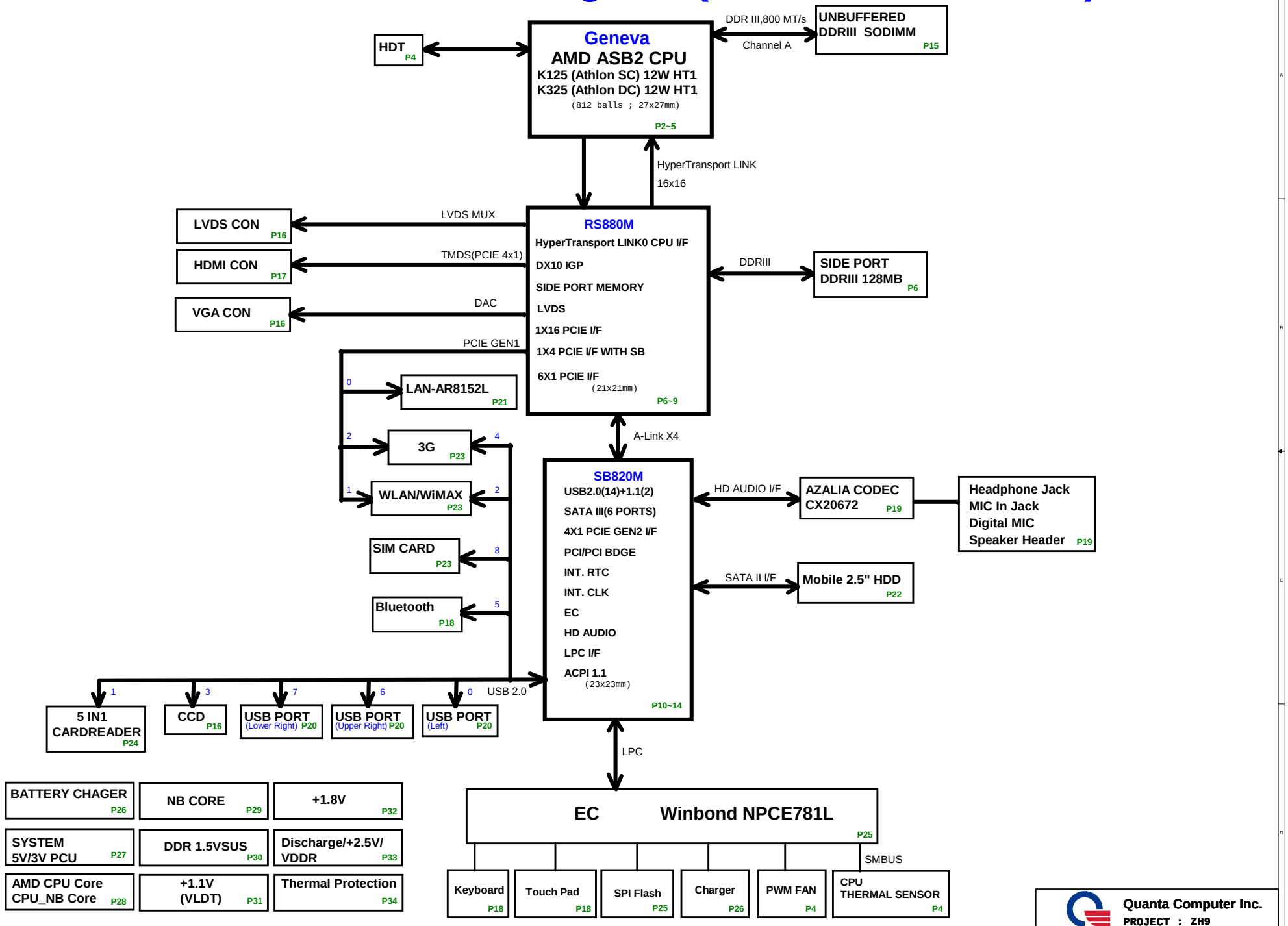
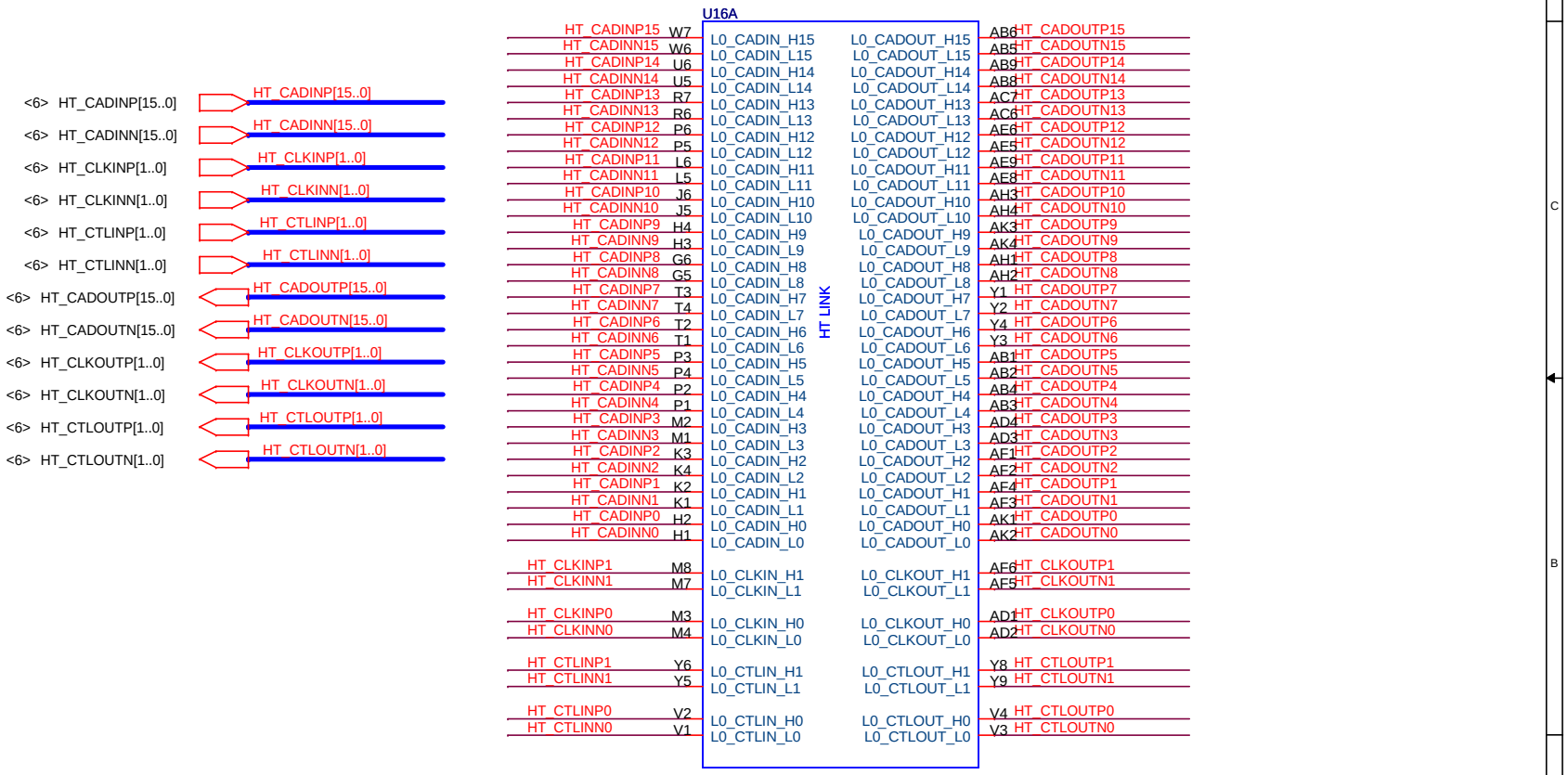
ZH9 Block Diagram (AMD Nile Platform)



Quanta Computer Inc.
PROJECT : ZH9

Size	Document Number	Rev
	Block Diagram	4A

Date: Sunday, March 28, 2010 Sheet 1 of 40



Quanta Computer Inc.

PROJECT : ZH9

Size	Document Number	Rev
	ASB2 HT I/F 1/4	4A

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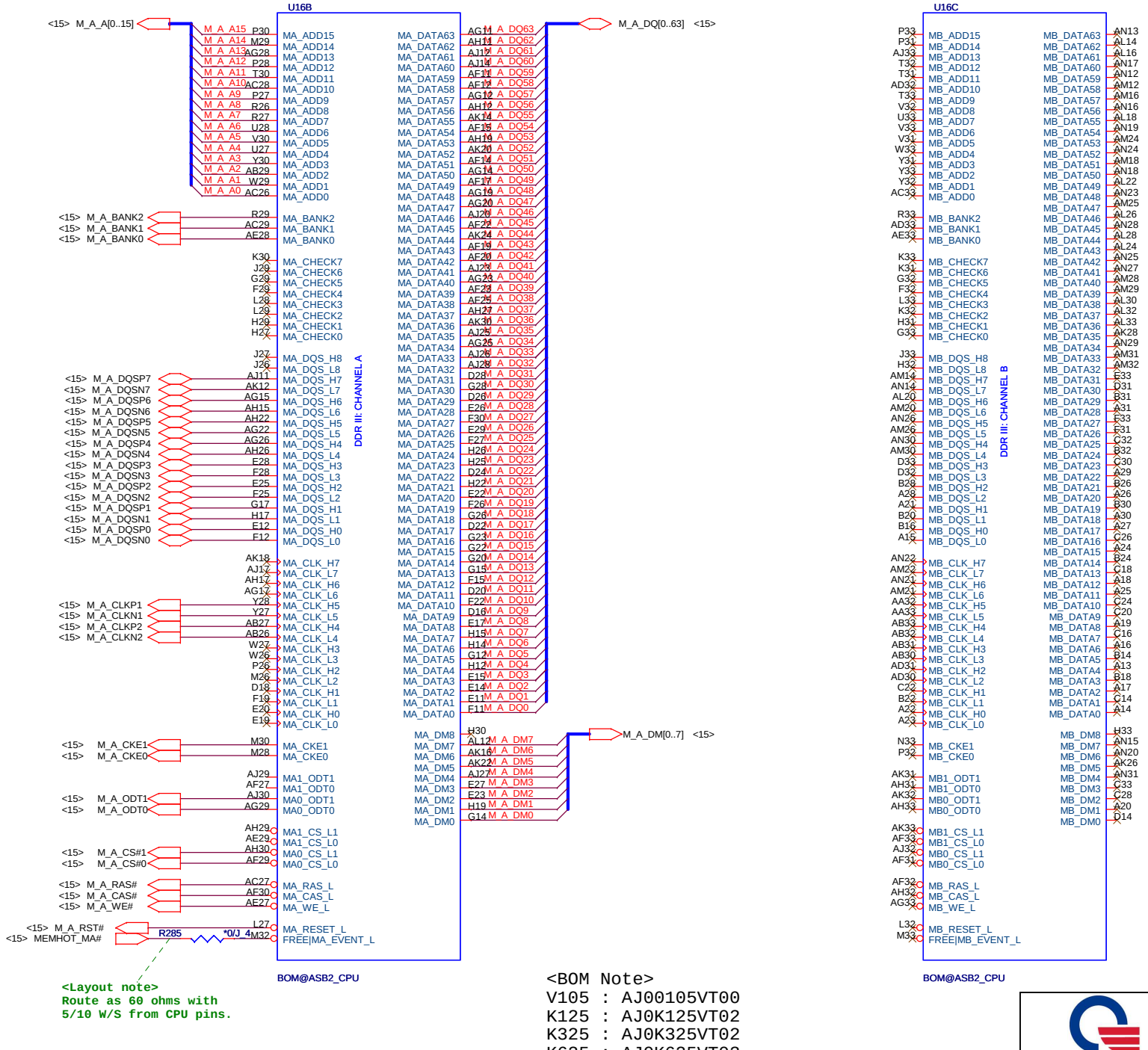
Processor Memory Interface



<Layout note>
Route as 60 ohms with
5/10 W/S from CPU pins.

<BOM Note>
V105 : AJ00105VT00
K125 : AJ0K125VT02
K325 : AJ0K325VT02
K625 : AJ0K625VT03

Quanta Computer Inc.
PROJECT : ZH9

Size	Document Number	Rev
	ASB2 DDRIII MEMORY 2/4	4A
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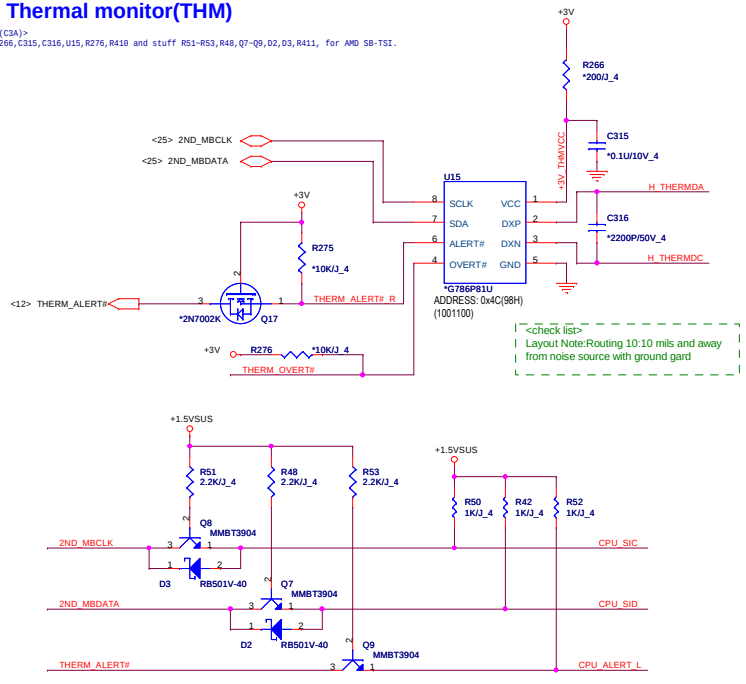
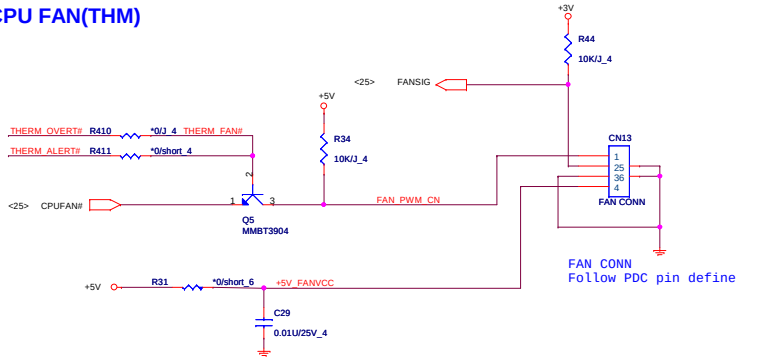
CPU Thermal monitor(THM)

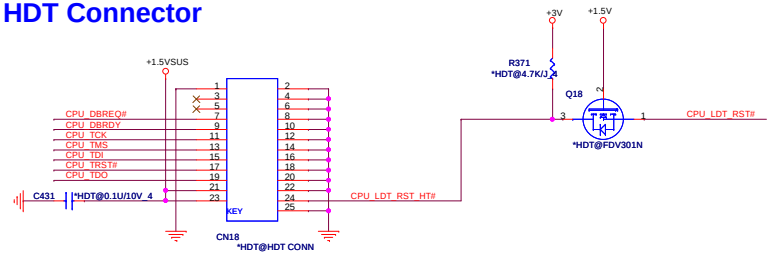
<20100303(C3A)>
Reserve R266,C315,C316,U15,R276,R410 and stuff R51~R53,R48,Q7~Q9,D2,D3,R411, for AMD SB-TSI.

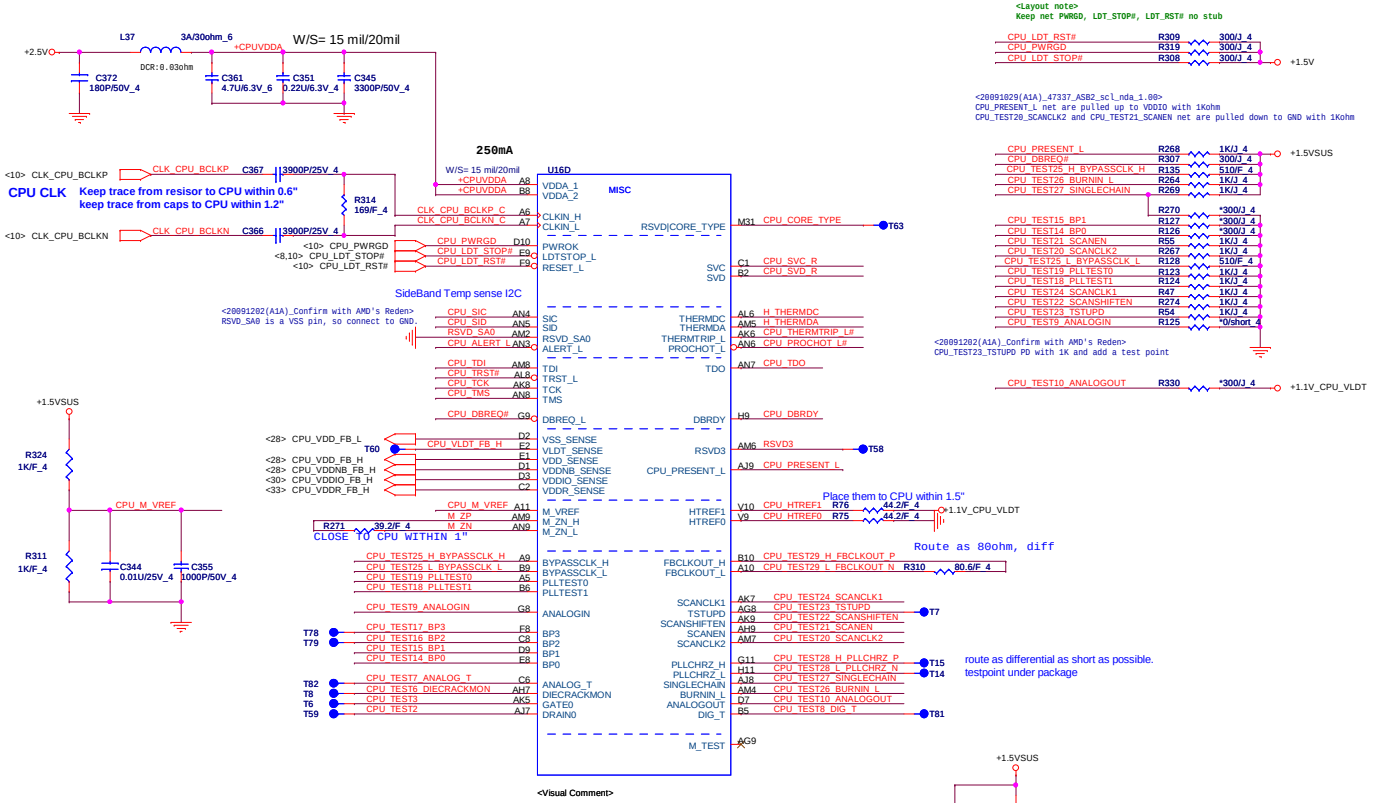


CPU FAN(THM)



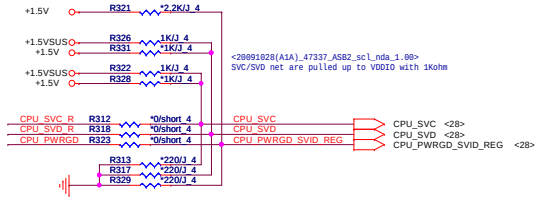
HDT Connector





Serial VID

To override VID,
Remove three 0ohms and install 220ohm of CPU_PWRGD to GND



Pre-PWROK Metal MODE			VFIX MODE(Don't Support)
SVC	SVD	Voltage Output	Voltage Output
0	0	1.1V	1.4V
0	1	1.0V	1.2V
1	0	0.9V	1.0V
1	1	0.8V	0.8V

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Size	Document Number	Rev
	ASB2 CTRL & DEBUG 3/4	4A

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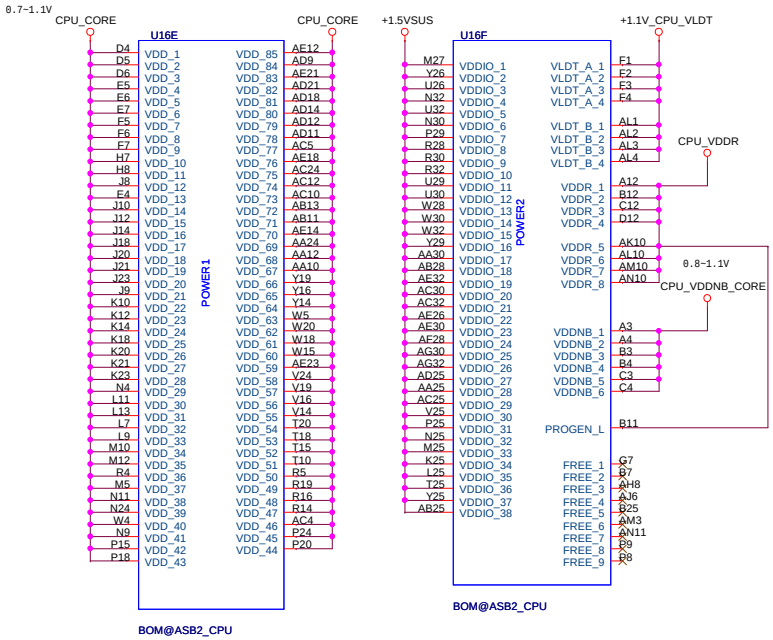
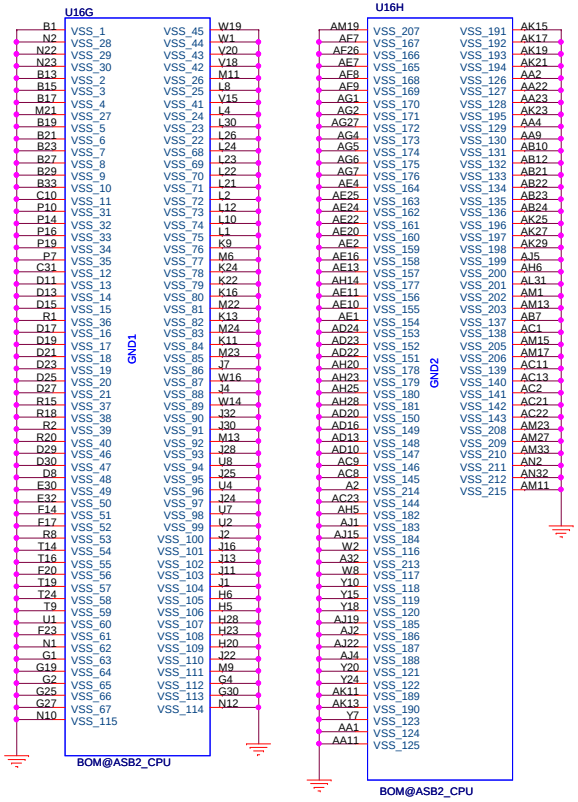
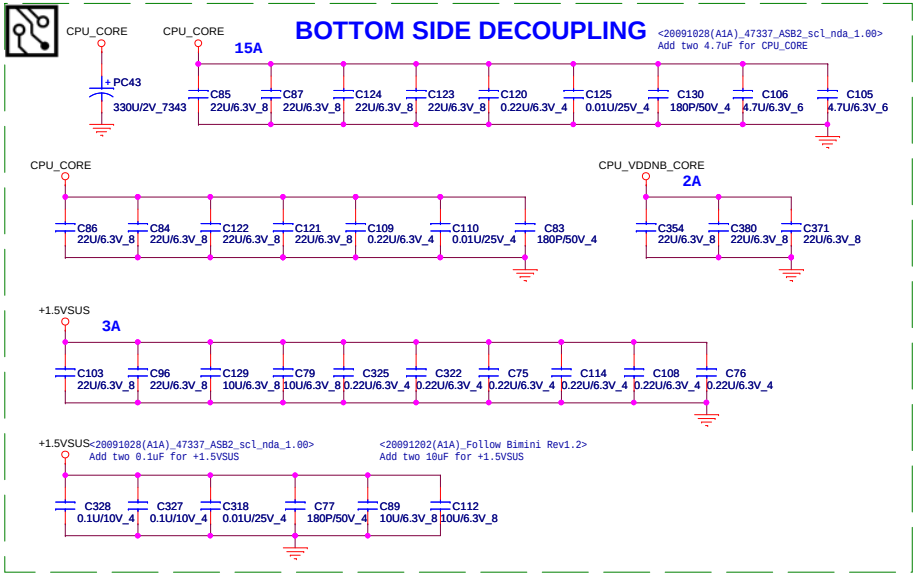
PROCESSOR POWER AND GROUND

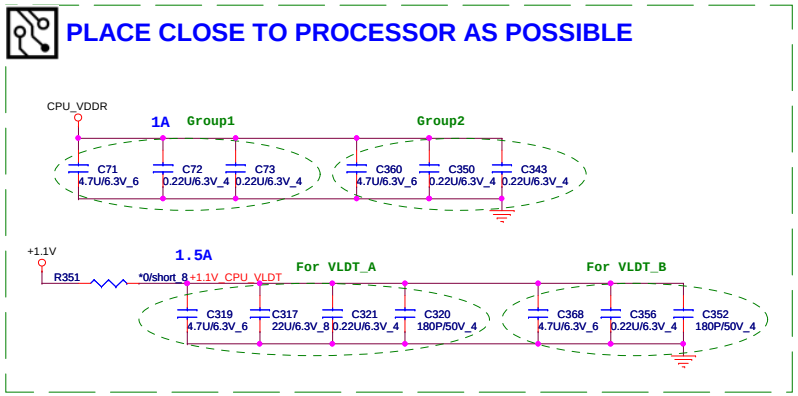




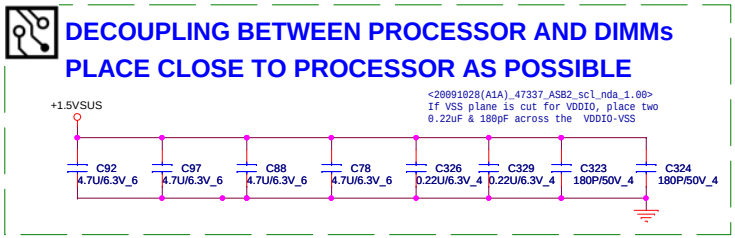
BOTTOM SIDE DECOUPLING



PLACE CLOSE TO PROCESSOR AS POSSIBLE



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



Quanta Computer Inc.		
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Size	Document Number: ASB2 PWR & GND 4/4	Rev: 4A
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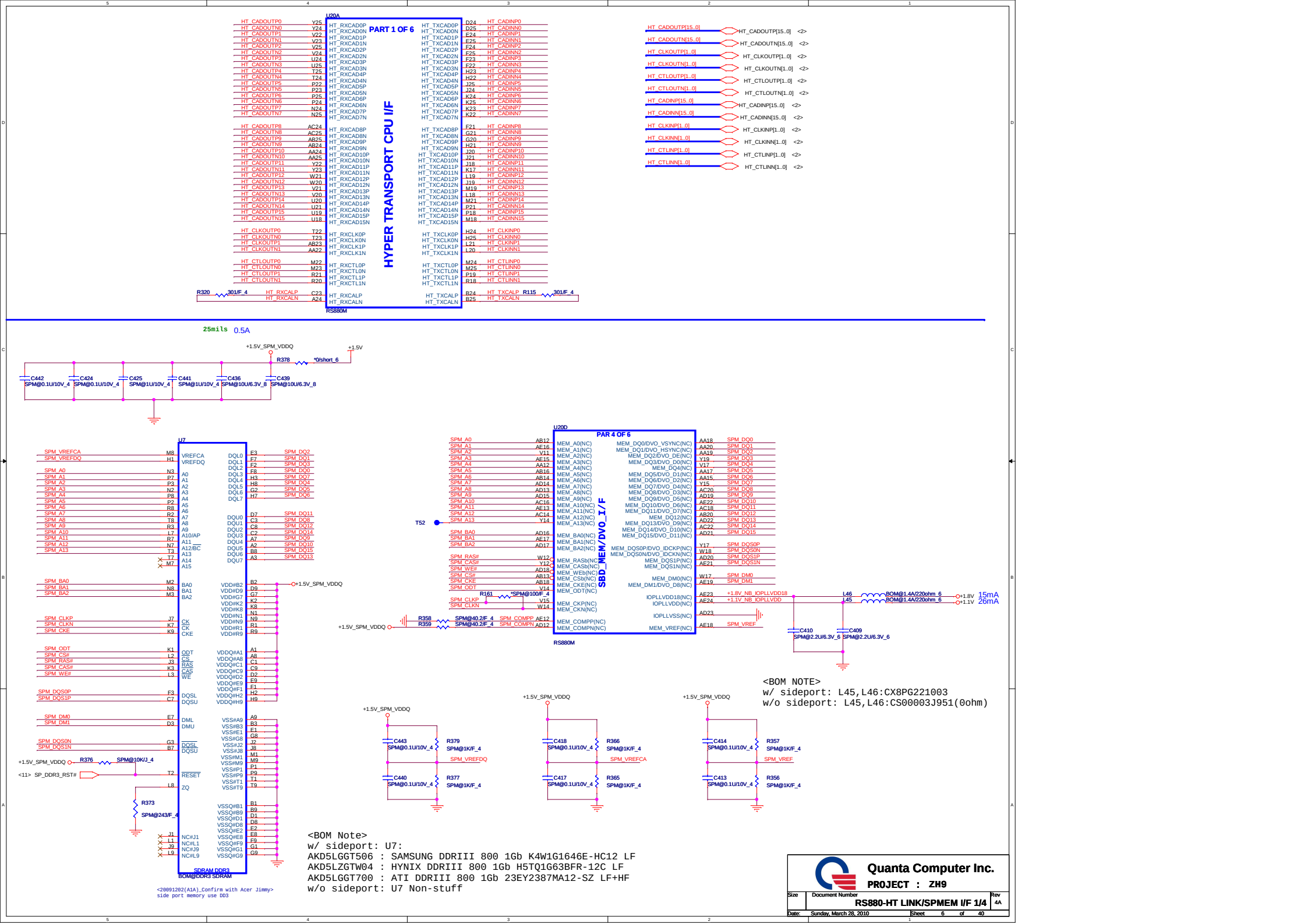
U20A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS880M
HT_CADOUTP[15..0]
HT_CADOUTN[15..0]
HT_CLKOUTP[1..0]
HT_CLKOUTN[1..0]
HT_CTLOUTP[1..0]
HT_CTLOUTN[1..0]
HT_CADINP[15..0]
HT_CADINN[15..0]
HT_CLKINP[1..0]
HT_CLKINN[1..0]
HT_CTLINP[1..0]
HT_CTLINN[1..0]
R320 301/F_4
R115 301/F_4
25mils 0.5A
+1.5V_SPM_VDDQ
+1.5V
R378 *0/short_6
C442 SPM@0.1U/10V_4
C424 SPM@0.1U/10V_4
C425 SPM@1U/10V_4
C441 SPM@1U/10V_4
C436 SPM@10U/6.3V_8
C439 SPM@10U/6.3V_8
U7
SDRAM DDR3
BOM@DDR3 SDRAM
U20D
PAR 4 OF 6
SB_MEM/DVO_I/F
T52
R161 *SPM@100/F_4
R358 SPM@40.2/F_4
R359 SPM@40.2/F_4
C410 SPM@2.2U/6.3V_6
C409 SPM@2.2U/6.3V_6
L46 BOM@1.4A/220ohm_6
L45 BOM@1.4A/220ohm_6
+1.8V 15mA
+1.1V 26mA
R376 SPM@10K/J_4
R373 SPM@243/F_4
C443 SPM@0.1U/10V_4
R379 SPM@1K/F_4
C440 SPM@0.1U/10V_4
R377 SPM@1K/F_4
C418 SPM@0.1U/10V_4
R366 SPM@1K/F_4
C417 SPM@0.1U/10V_4
R365 SPM@1K/F_4
C414 SPM@0.1U/10V_4
R357 SPM@1K/F_4
C413 SPM@0.1U/10V_4
R356 SPM@1K/F_4
<BOM NOTE>
w/ sideport: L45,L46:CX8PG221003
w/o sideport: L45,L46:CS00003J951(0ohm)
<BOM Note>
w/ sideport: U7:
AKD5LGGT506 : SAMSUNG DDRIII 800 1Gb K4W1G1646E-HC12 LF
AKD5LZGTW04 : HYNIX DDRIII 800 1Gb H5TQ1G63BFR-12C LF
AKD5LGGT700 : ATI DDRIII 800 1Gb 23EY2387MA12-SZ LF+HF
w/o sideport: U7 Non-stuff
<20091202(AIA)_Confirm with Acer Jimmy>
side port memory use DD3
Quanta Computer Inc.
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Size
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RS880-HT LINK/SPMEM I/F 1/4
Rev 4A
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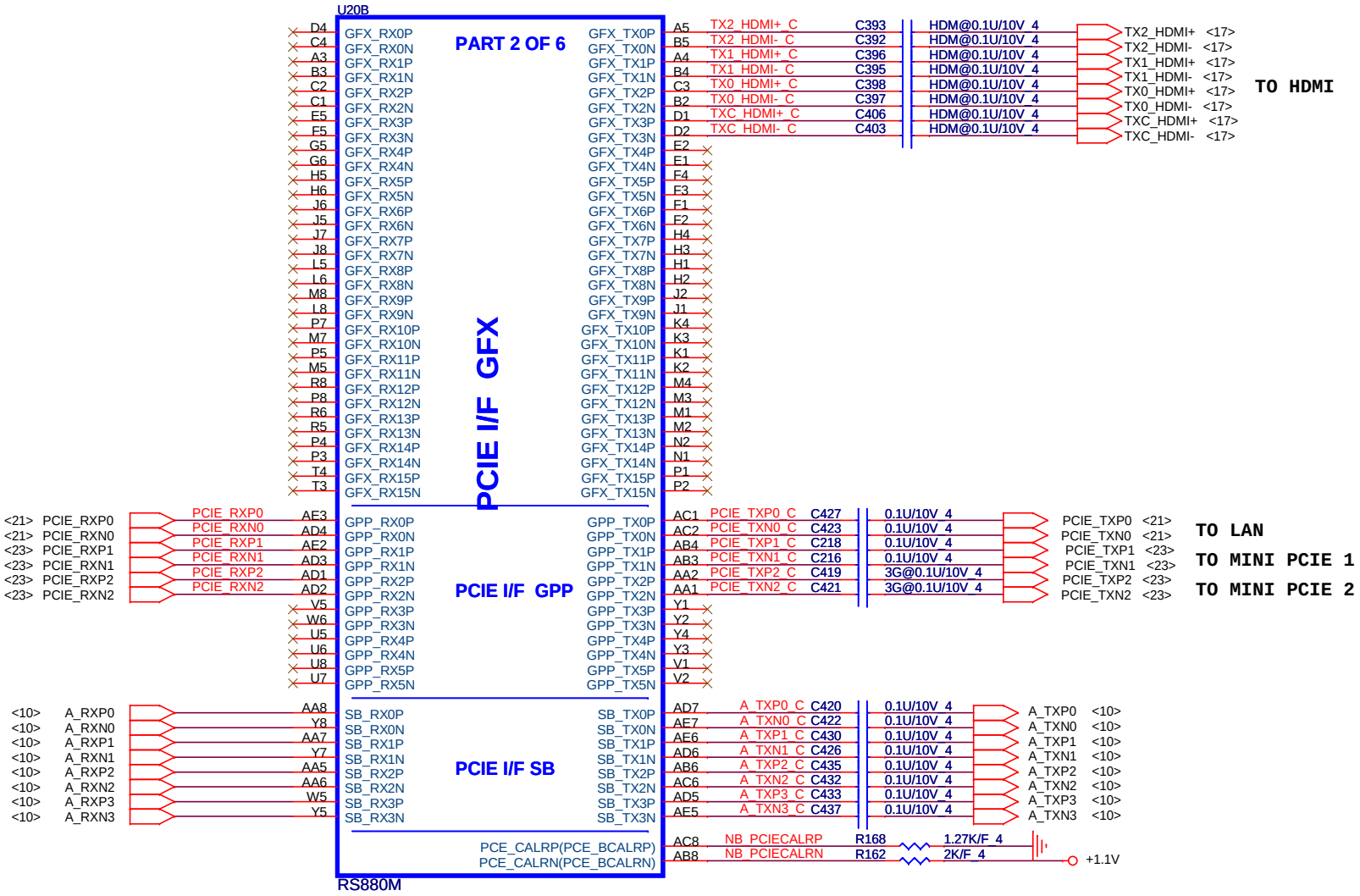

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Quanta Computer Inc.

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Size	Document Number	Rev
	RS880-PCIE I/F 2/4	4A

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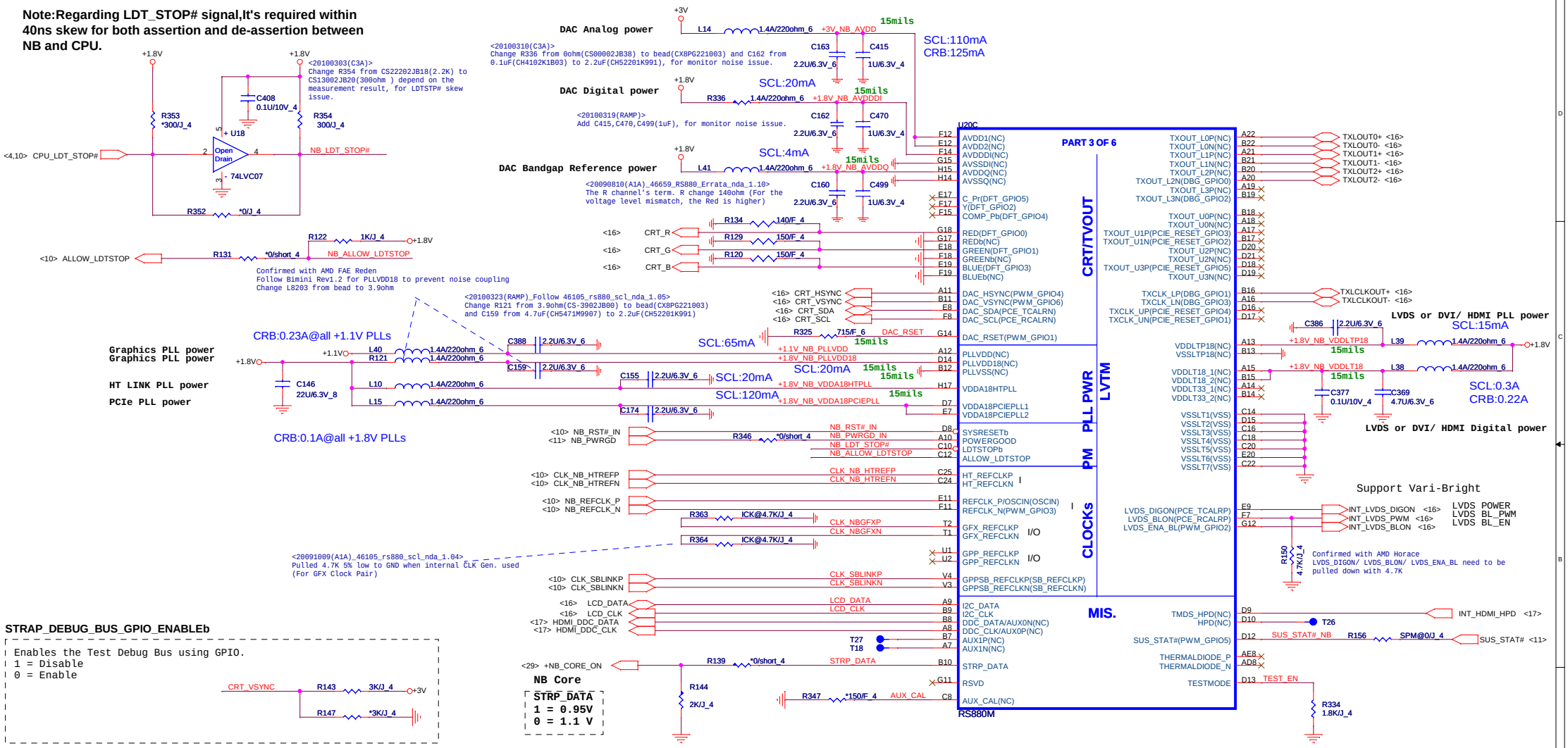
Note:Regarding LDT_STOP# signal,It's required within 40ns skew for both assertion and de-assertion between NB and CPU.



STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 = Disable
0 = Enable

RS880M: Enables Side port memory

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available

<BOM NOTE>
w/ sideport: R142 non-stuff
w/o sideport: R142 stuff

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

EEPROM not implemented

Quanta Computer Inc.
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Size	Document Number	Rev
	RS880-SYSTEM I/F 3/4	4A

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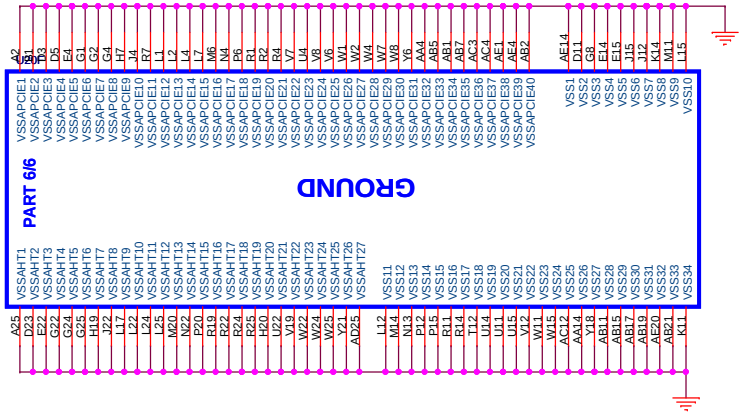
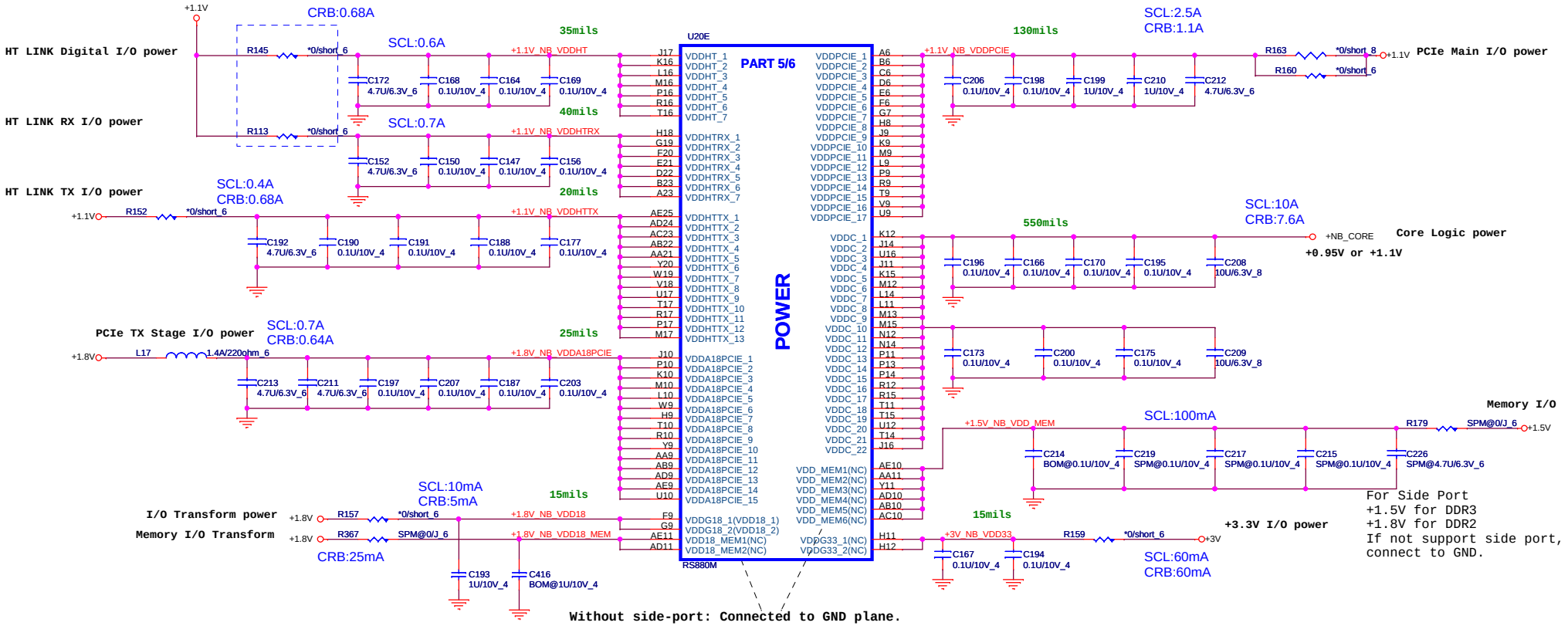


RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVDD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDD18	+1.8V	+1.8V	PLLVDD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVDD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+0.95V~+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDD33	+3.3V	+3.3V	VDDLT18	GND	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	NC	NC



<BOM NOTE>
w/ sideport: C214:CH4102K1B03 ; C416:CH5102K9B06
w/o sideport: C214,C416:CS00002JB38(0ohm)

Quanta Computer Inc.
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	RS880-POWER 4/4	4A
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PCIE_RST#: Reset PCIe Slot/Device (PCIe interface from SB)
A_RST#: Reset NB, MXM, EC, PCIe Slot/Device (PCIe interface from NB)

NB
EC

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB820

U5A
SB800 Part 1 of 5

PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC

<BOM Note>
ID0/1/2 P/N Model
000 AKD5LGGT506 SAM DDR3-800 1Gb K4W1G1646E-HC12
001 AKD5LZGTW04 HYN DDR3-800 1Gb H5TQ1G63BFR-12C
010 AKD5LGGT700 ATI DDR3-800 1Gb 23EY2387MA12-SZ

<Layout note>
Share pad with other resisters and close to external CLK Gen.

<20100325(RAMP)>
Change RP1~RP4,RP6~RP8 to shortpad.

to NB for A-LINK/PCIe REF CLK
to NB Display Eng
to MINI PCIE 2
to LAN
to MINI PCIE 1
to LAN chip 25MHz

<20100129(B2A)>
Stuff R345. (CLK for LAN from crystal change to internal CLK.)

<20100310(C3A)>
Non-Stuff R345. (14M_25M_48M_OSC is S0 plane, doesn't support WoL.)

<20100303(C3A)>
Change C411,C412 from CH02206JB08(22pF) to CH02706JB06(27pF), for Y4.

SB820M

IC CTRL(605P)SB820M 218-0697014(FCBGA)
P/N : AJ069700T01

From MINI PCIE 1

INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).

For AMD RST
MINI-PCIE
LAN chip
Card reader

For VDDR
<20100119(B2A)_Bimini Rev1.4>
Non-stuff U21,C429,C428,R372,R300 (Nile doesn't support +1.05V for DDR3-1333)

The Nile VDDR should be 0.9V all the time. The 1.05V is only for DDR3_1333 which is not supported on Nile.

MEM_1V5 is for gating the glitch on VDDR_1.2_EN

VDDR_1.2_EN:
1 : VDDR =1.05V
0: VDDR = 0.90V (Default)

VDDR_1.2_EN="0" is for DDRIII-1066, VDDR=0.9V
VDDR_1.2_EN="1" is for DDRIII-1333, VDDR=1.05V

RTC(RTC)

R = (5V - 0.2V-2V)/0.2mA = 14k

<BOM Note>
RTC BATTERY
AHL03001033 : JHT (18mAh)
AHL03001032 : MAT (17mAh)
AHL03001035 : FDK (15mAh)

<20100303(C3A)>
Delete CN5 and Add BT1, for Battery SMT type.
<20100310(C3A)>
Swap BT1's pin, for pin define error

<20100303(C3A)>
Change C93,C111 from CH02206JB08(22pF) to CH01806JB07(18pF), for Y2.

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Size	Document Number	Rev
	SB820-PCIE/CPU/LPC 1/5	4A
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NC only ,Can't be install

+3V_S5
R100 *2.2K/J_4 SB_TEST0
R98 *2.2K/J_4 SB_TEST1
R280 *2.2K/J_4 SB_TEST2

SCL0/SDATA0 is +3.3V_S0 domain
To Clock gen/DDR/WLAN
+3V
R338 2.2K/J_4 SB_SCLK0
R335 2.2K/J_4 SB_SDATA0

SMBUS1~3 is +3.3V_S5 domain
If SMBUS and GPIO not implemented
10K PU to +3V_S5 or 10K PD
R279 10K/J_4 SB_SCLK1
R92 10K/J_4 SB_SDATA1
R133 10K/J_4 SB_SCLK2
R337 10K/J_4 SB_SDATA2
R136 10K/J_4 SB_SCLK3
R148 10K/J_4 SB_SDATA3

+1.8V
R340 300/J_4 NB_PWRGD

<20100129(B2A)>
Stuff R110. (CLK for Cardreader from crystal change to internal CLK.)

U5D
SB800
Part 4 of 5
SB820M

<10,15> CPU_MEMHOT# R91 *0/J_4
T9
<25> SUSB#
<25> SUSC#
<25> DNBSWON#
<25> ECPWROK
<8> SUS_STAT#
R294 *0/short_4 SB_PWRGD
SUS_STAT#
SB_TEST0
SB_TEST1
SB_TEST2
<25> GA20
<25> KBRST#
<25> EC_SMI#
<25> EC_SCI#
T13 SYS_RST#
<21,23> PCIE_WAKE#
<4> CPU_THERMTRIP#
<8> NB_PWRGD
CPU_THERMTRIP#
NB_PWRGD
<25> EC_RSMRST#
RSMRST#

From MINI PCIE 2
<10> SB_GPIO_PCIE_RST#
<23> CLKREQ_MNC#
R341 *0/short_4
SB_GPIO_PCIE_RST#
INT_CLKREQ_MNC#

<19> SB_BEEP
<15,23> SB_SCLK0
<15,23> SB_SDATA0
SB_SCLK0
SB_SDATA0
SB_SCLK1
SB_SDATA1

From LAN
<21> CLKREQ_LAN#
R333 *0/short_4
INT_CLKREQ_LAN#

T10 LLB#
T19 SHUTDOWN#
<6> SP_DDR3_RST#
R281 SPM@0/J_4

<20091202(A1A)_Confirm with AMD's Horace>
IDLEEXIT#(Multi function of Pin AA20) is used for server CPU.

<20> USBOC#R R277 *0/J_4 USBOC#67
<20> USBOC#L R278 *0/J_4 USBOC#0
T73 SB_JTAG_TDO
T69 SB_JTAG_TCK
T68 SB_JTAG_TDI
T70 SB_JTAG_RST#

HD audio interface is +3V_S5 voltage
<14> ACZ_SDOUT
ACZ_BCLK
ACZ_SDOUT
ACZ_SDIN0
ACZ_SYNC
ACZ_RST#

To Azalia
ACZ_SDOUT R85 33/J_4 C99 *10P/50V_4 ACZ_SDOUT_AUDIO <19>
ACZ_SYNC R86 33/J_4 C100 *10P/50V_4 ACZ_SYNC_AUDIO <19>
<20091030(A1A)_EMI's Suggest>
Add one 10pF to GND for BITCLK
ACZ_BCLK R87 33/J_4 C101 *10P/50V_4 ACZ_BITCLK_AUDIO <19>
R88 *10K/J_4
ACZ_RST# R71 33/J_4 ACZ_RST#_AUDIO <19>
ACZ_SDIN0 R90 *10K/J_4 ACZ_SDIN0 <19>

+3V_S5
R70 10K/J_4
R84 10K/J_4
R286 10K/J_4
R83 10K/J_4
R282 10K/J_4

T17
T22

PCI_PME#/GEVENT4#
RI#/GEVENT22#
SPI_CS3#/GBE_STAT1/GEVENT21#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST0
TEST1/TMS
TEST2
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/GEVENT23#
GEVENT5#
SYS_RESET#/GEVENT19#
WAKE#/GEVENT8#
IR_RX1/GEVENT20#
THRMTRIP#/SMBALERT#/GEVENT2#
NB_PWRGD
RSMRST#
ACPI / WAKE UP EVENTS

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB 1.1 USB MISC

CLK_REQ4#/SATA_IS0#/GPIO64
CLK_REQ3#/SATA_IS1#/GPIO63
SMARTVOLT1/SATA_IS2#/GPIO50
CLK_REQ0#/SATA_IS3#/GPIO60
SATA_IS4#/FANOUT3/GPIO55
SATA_IS5#/FANIN3/GPIO59
SPKR/GPIO66
SCL0/GPIO43
SDA0/GPIO47
SCL1/GPIO227
SDA1/GPIO228
CLK_REQ2#/FANIN4/GPIO62
CLK_REQ1#/FANOUT4/GPIO61
IR_LED#/LLB#/GPIO184
SMARTVOLT2/SHUTDOWN#/GPIO51
DDR3_RST#/GEVENT7#
GBE_LED0/GPIO183
GBE_LED1/GEVENT9#
GBE_LED2/GEVENT10#
GBE_STAT0/GEVENT11#
CLK_REQG#/GPIO65/OSCIN
GPIO

BLINK/USB_OC7#/GEVENT18#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GEVENT17#
USB_OC4#/IR_RX0/GEVENT16#
USB_OC3#/AC_PRES/TDO/GEVENT15#
USB_OC2#/TCK/GEVENT14#
USB_OC1#/TDI/GEVENT13#
USB_OC0#/TRST#/GEVENT12#
USB OC

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO167
AZ_SDIN1/GPIO168
AZ_SDIN2/GPIO169
AZ_SDIN3/GPIO170
AZ_SYNC
AZ_RST#
HD AUDIO

GBE_COL
GBE_CRS
GBE_MDCK
GBE_MDIO
GBE_RXCLK
GBE_RXD3
GBE_RXD2
GBE_RXD1
GBE_RXD0
GBE_RXCTL/RXDV
GBE_RXERR
GBE_TXCLK
GBE_TXD3
GBE_TXD2
GBE_TXD1
GBE_TXD0
GBE_TXCTL/TXEN
GBE_PHY_PD
GBE_PHY_RST#
GBE_PHY_INTR
GBE LAN

PS2_DAT/SDA4/GPIO187
PS2_CLK/SCL4/GPIO188
SPI_CS2#/GBE_STAT2/GPIO166
FC_RST#/GPO160
PS2KB_DAT/GPIO189
PS2KB_CLK/GPIO190
PS2M_DAT/GPIO191
PS2M_CLK/GPIO192
EMBEDDED CTRL

USB 2.0

A10 SB_CLK_48M_CR R110 ICK@22/J_4 CLK_48M_CR <24> to CARD READER 48MHz
G19 USB_RCOMP_SB R332 11.8K/F_6

OHCI (dev-20, fun-5)
J10 USB_FSD13P T75
H11 USB_FSD13N T77
USB_FSD1P/GPIO186
USB_FSD1N
H9 USB_FDS12P T72
J8 USB_FSD12N T71
USB_FSD0P/GPIO185
USB_FSD0N

Controller	Ports mapping
OHCI0 (dev-18, fun-0)	Port 0 - 4
EHCI (dev-18, fun-2)	Port 0 - 4
OHCI0 (dev-19, fun-0)	Port 5 - 9
EHCI (dev-19, fun-2)	Port 5 - 9
OHCI0 (dev-22, fun-0)	Port 10 - 14
EHCI (dev-22, fun-2)	Port 10 - 14

USB_HSD13P B12
USB_HSD13N A12
USB_HSD12P F11
USB_HSD12N E11
USB_HSD11P E14
USB_HSD11N E12
USB_HSD10P J12
USB_HSD10N J14
USB_HSD9P A13
USB_HSD9N B13
USB_HSD8P D13 USB+_SIM <23> MM-SIM
USB_HSD8N C13 USB-_SIM <23>
USB_HSD7P G12 USBP7+ <20> CONN (Lower Right)
USB_HSD7N G14 USBP7- <20>
USB_HSD6P G16 USBP6+ <20> CONN (Upper Right)
USB_HSD6N G18 USBP6- <20>
USB_HSD5P D16 USBP5+ <18> BT
USB_HSD5N C16 USBP5- <18>
USB_HSD4P B14 USBP4+ <23> MNC
USB_HSD4N A14 USBP4- <23>
USB_HSD3P E18 USBP3+ <16> CCD
USB_HSD3N E16 USBP3- <16>
USB_HSD2P J16 USBP2+ <23> MPC
USB_HSD2N J18 USBP2- <23>
USB_HSD1P B17 USBP1+ <24> Card reader
USB_HSD1N A17 USBP1- <24>
USB_HSD0P A16 USBP0+ <20> CONN (Left)
USB_HSD0N B16 USBP0- <20>

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 F23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_SCLK3
SDA3_LV/GPIO196 E26 SB_SDATA3
EC_PWM0/EC_TIMER0/GPIO197 F25
EC_PWM1/EC_TIMER1/GPIO198 E22
EC_PWM2/EC_TIMER2/GPIO199 F22 EC_PWM2 <14>
EC_PWM3/EC_TIMER3/GPIO200 E21 EC_PWM3 <14>

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D28
KSI_5/GPIO206 D29
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28
KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22
EMBEDDED CTRL

Quanta Computer Inc.
PROJECT : ZH9

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	SB820-ACPI/GPIO/USB 2/5	4A

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SATA PORT 0,1,2,3
can support AHCI
mode

SATA HDD

PLACE SATA AC COUPLING
CAPS CLOSE TO SB820

<22> SATA_TXP0
<22> SATA_TXN0
<22> SATA_RXN0
<22> SATA_RXP0

C141 0.01U/25V_4 SATA_TXP0_C
C142 0.01U/16V_4 SATA_TXN0_C
C140 0.01U/25V_4 SATA_RXN0_C
C137 0.01U/25V_4 SATA_RXP0_C

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB820

+1.1V_SB_VDDAN_11_SATA

R316 1K/F_4 SATA_CALRP
R315 931/F_4 SATA_CALRN

To meet SB800 SCL1.02:
DNI SATA XTAL circuit's parts

<22> SATALED#
+3V R304 10K/J_4

C151 *22P/50V_4 SATA_X1
Y3 *25MHz-SATA
R114 *1M/J_4
C145 *22P/50V_4 SATA_X2

U5B

SB800
Part 2 of 5

SERIAL ATA

AH9 SATA_TX0P
AJ9 SATA_TX0N
AJ8 SATA_RX0P
AH8 SATA_RX0N
AH10 SATA_TX1P
AJ10 SATA_TX1N
AG10 SATA_RX1P
AE10 SATA_RX1N
AG12 SATA_TX2P
AE12 SATA_TX2N
AJ12 SATA_RX2P
AH12 SATA_RX2N
AH14 SATA_TX3P
AJ14 SATA_TX3N
AG14 SATA_RX3P
AE14 SATA_RX3N
AG17 SATA_TX4P
AE17 SATA_TX4N
AJ17 SATA_RX4P
AH17 SATA_RX4N
AJ18 SATA_TX5P
AH18 SATA_TX5N
AH19 SATA_RX5P
AJ19 SATA_RX5N
AB14 SATA_CALRP
AA14 SATA_CALRN
AD11 SATA_ACT#/GPIO67
AD16 SATA_X1
AC16 SATA_X2

FLASH

The flash controller function is NOT supported by the SB820M.

AH28 FC_CLK
AG28 FC_FBCLKOUT
AF26 FC_FBCLKIN
AF28 FC_OE#/GPIOD145
AG29 FC_AVD#/GPIOD146
AG26 FC_WE#/GPIOD148
AF27 FC_CE1#/GPIOD149
AE29 FC_CE2#/GPIOD150
AF29 FC_INT1/GPIOD144
AH27 FC_INT2/GPIOD147
AJ27 FC_ADQ0/GPIOD128
AJ26 FC_ADQ1/GPIOD129
AH25 FC_ADQ2/GPIOD130
AH24 FC_ADQ3/GPIOD131
AG23 FC_ADQ4/GPIOD132
AH23 FC_ADQ5/GPIOD133
AJ22 FC_ADQ6/GPIOD134
AG21 FC_ADQ7/GPIOD135
AF21 FC_ADQ8/GPIOD136
AH22 FC_ADQ9/GPIOD137
AJ23 FC_ADQ10/GPIOD138
AF23 FC_ADQ11/GPIOD139
AJ24 FC_ADQ12/GPIOD140
AJ25 FC_ADQ13/GPIOD141
AG25 FC_ADQ14/GPIOD142
AH26 FC_ADQ15/GPIOD143

T45 T31 T39 T38 T37 T36 T43 T44 T32 T33 T42 T30 T29 T28 T23 T24 T21 T16 T80 T20 T25 T84 T34 T35 T40 T41

IF THERE IS NO IDE, TEST
POINTS FOR DEBUG BUS
IS MANDATORY

+3V
R106 10K/J_4
R105 10K/J_4
Q11 MMBT3904
SB_PROCHOT# <4>
SB_PROCHOT_C

HW MONITOR

W5 FANOUT0/GPIO52
W6 FANOUT1/GPIO53
Y9 FANOUT2/GPIO54
W7 FANIN0/GPIO56
V9 FANIN1/GPIO57
W8 FANIN2/GPIO58
B6 TEMPIN0/GPIO171 TEMPIN0 R109 10K/J_4
A6 TEMPIN1/GPIO172 TEMPIN1 R108 10K/J_4
A5 TEMPIN2/GPIO173 TEMPIN2 R103 10K/J_4
B5 TEMPIN3/TALERT#/GPIO174
C7 TEMP_COMM
R107 10K/J_4 +3V_S5
THERM_ALERT# <4>

A3 VIN0/GPIO175 VIN0 R290 10K/J_4
B4 VIN1/GPIO176 VIN1 R289 10K/J_4
A4 VIN2/GPIO177 VIN2 R288 10K/J_4
C5 VIN3/GPIO178 VIN3 R102 10K/J_4
A7 VIN4/GPIO179 VIN4 R409 10K/J_4
B7 VIN5/GPIO180 VIN5 R298 10K/J_4
B8 VIN6/GBE_STAT3/GPIO181 VIN6 R301 10K/J_4
A8 VIN7/GBE_LED3/GPIO182 VIN7 R297 10K/J_4

<20100119(B2A)_Bimini Rev1.4>
Non-stuff R408 ; stuff R409
(Nile doesn't support VDDR = +1.05V for DDR3-1333)

VIN4 R408 *0/J_4 MEM_1V5 <10>

SPI ROM

T67 J5 SPI_DI/GPIO164
T12 E2 SPI_DO/GPIO163
T11 K4 SPI_CLK/GPIO162
T65 K9 SPI_CS1#/GPIO165
T66 G2 ROM_RST#/GPIO161

G27 NC1
Y2 NC2

SB820M

Quanta Computer Inc.
PROJECT : ZH9

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	SB820-SATA/HWM/SPI 3/5	4A
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PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

3.3V I/O power

131mA

Not used: Connected to GND through a 0Ω.

1.8V GPIOD I/O Power

A-Link Express III/PCIe PLL power

43mA 15mils

A-Link Express III/PCIe analog power

600mA 100mils

Check

SATA PHY PLL power

93mA 15mils

SATA PHY analog / I/O Power

567mA 50mils

USB PHY analog / I/O Power

658mA 50mils

Support S3 wake up

USB PHY DLL analog power

xx mA 20mils

Support S3 wake up

SB820M

Core logic power

100mils 510mA

Check

System Clock Gen analog/output power

xx mA

<45484_sb800_dg_nda_1.02>
Not use interal CLK Gen: Connected to +1.1V directly.

Not support GBE: Connected to GND.

S5 I/O Power

20mils 32mA

S5 Core logic standby power

15mils 113mA

20mils xx mA HD Audio I/O Power

15mils 197mA

USB PHY core power

15mils 47mA System CLK Gen PLLs analog power

15mils 62mA System CLK Gen PLLs analog power

17mA USB PHY PLL analog power

5mA Hardware monitor analog / I/O power

25-MHz XTAL I/O Power

WoL--> +3.3V_S5 rail
Non-WoL--> +3.3V_S0 rail

15mils
xx mA

Part 5 of 5

SB820M

WoL--> +1.1V_S5 rail
Non-WoL--> +1.1V_S0 rail

<20100310(C3A)_Follow CRB>
Connect +3VSUS_SB_VDDPL_33_USB_S to
+3VSUS directly.

As GPIOs: Stuff 0.1uF

Quanta Computer Inc.		
PROJECT : ZH9		
Size	Document Number: SB820-PWR/DECOUPLING 4/5	Rev: 4A
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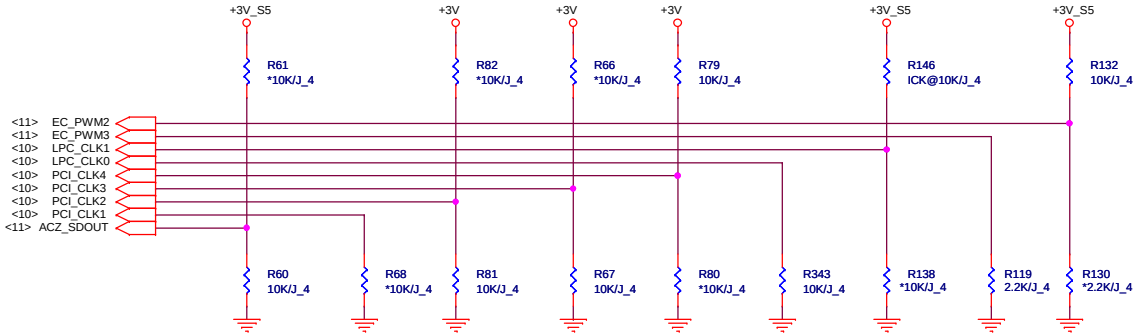
STANDARD STRAPS

<20091202(A1A)_Confirm with AMD's Horace>
PCI_CLK4 PU with 10K for both internal and external CLK Gen.



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM3 EC_PWM2
PULL HIGH	LOW POWER MODE	PCIe Gen II	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLK MODE ICK@DEFAULT	EC ENABLED	CLKGEN ENABLED ICK@DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	PCIe Gen I	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION CLK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED ECK@DEFAULT	L, H=LPC ROM DEFAULT L, L=Reserved

This is required as the low power mode is not supported on the SB8xx.

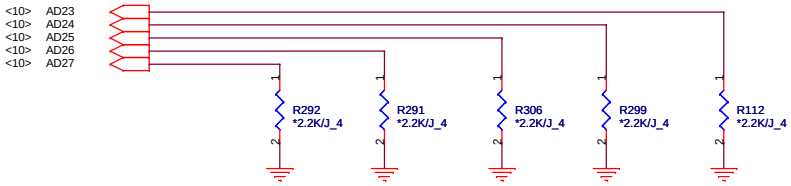
Not Applicable to SB820M--Leave provision for PD.

PCICLK4:
CPU/NB HT Clock Selection
This strap is not used if the strap CLKGEN is configured for external clock generator mode.

internal have pull Hi 10K

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Quanta Computer Inc.
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Size	Document Number	Rev
	SB820-STRAPS,PWRGD 5/5	4A
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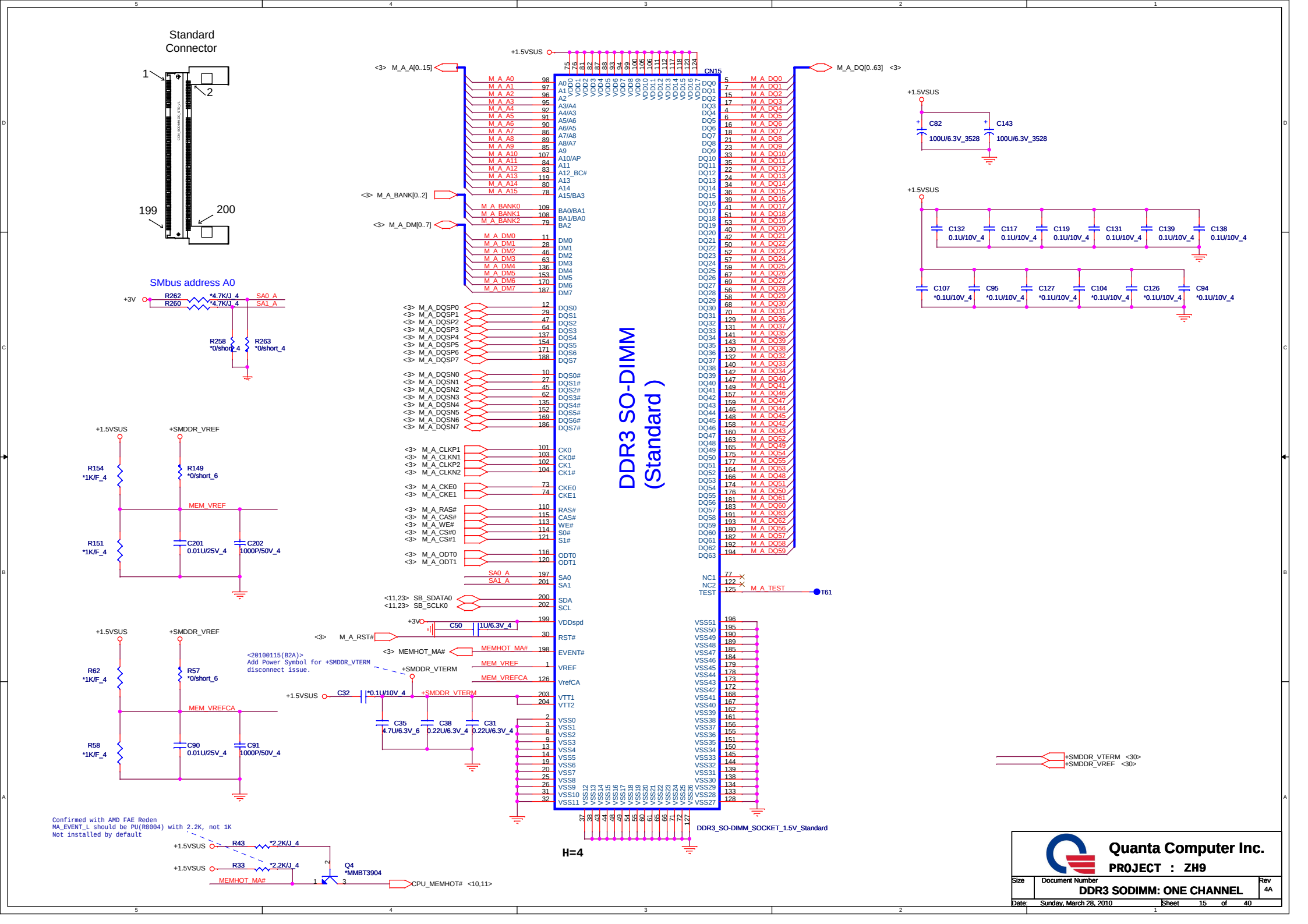
Standard Connector
1
2
199
200
SMbus address A0
+3V
R262 *4.7K/J_4
R260 *4.7K/J_4
SA0_A
SA1_A
R258 *0/short_4
R263 *0/short_4
+1.5VSUS
+SMDDR_VREF
R154 *1K/F_4
R149 *0/short_6
MEM_VREF
R151 *1K/F_4
C201 0.01U/25V_4
C202 1000P/50V_4
R62 *1K/F_4
R57 *0/short_6
MEM_VREFCA
R58 *1K/F_4
C90 0.01U/25V_4
C91 1000P/50V_4
<20100115(B2A)>
Add Power Symbol for +SMDDR_VTERM
disconnect issue.
+SMDDR_VTERM
C32 *0.1U/10V_4
C35 4.7U/6.3V_6
C38 0.22U/6.3V_4
C31 0.22U/6.3V_4
Confirmed with AMD FAE Reden
MA_EVENT_L should be PU(R8004) with 2.2K, not 1K
Not installed by default
R43 *2.2K/J_4
R33 *2.2K/J_4
Q4 *MMBT3904
MEMHOT_MA#
CPU_MEMHOT# <10,11>
<3> M_A_A[0..15]
<3> M_A_BANK[0..2]
<3> M_A_DM[0..7]
<3> M_A_DQSP0
<3> M_A_DQSP1
<3> M_A_DQSP2
<3> M_A_DQSP3
<3> M_A_DQSP4
<3> M_A_DQSP5
<3> M_A_DQSP6
<3> M_A_DQSP7
<3> M_A_DQSN0
<3> M_A_DQSN1
<3> M_A_DQSN2
<3> M_A_DQSN3
<3> M_A_DQSN4
<3> M_A_DQSN5
<3> M_A_DQSN6
<3> M_A_DQSN7
<3> M_A_CLKP1
<3> M_A_CLKN1
<3> M_A_CLKP2
<3> M_A_CLKN2
<3> M_A_CKE0
<3> M_A_CKE1
<3> M_A_RAS#
<3> M_A_CAS#
<3> M_A_WE#
<3> M_A_CS#0
<3> M_A_CS#1
<3> M_A_ODT0
<3> M_A_ODT1
<11,23> SB_SDATA0
<11,23> SB_SCLK0
<3> M_A_RST#
<3> MEMHOT_MA#
DDR3 SO-DIMM (Standard)
CN15
M_A_DQ[0..63] <3>
NC1
NC2
TEST
M_A_TEST
T61
C50 1U/6.3V_4
DDR3_SO-DIMM_SOCKET_1.5V_Standard
H=4
C82 100U/6.3V_3528
C143 100U/6.3V_3528
C132 0.1U/10V_4
C117 0.1U/10V_4
C119 0.1U/10V_4
C131 0.1U/10V_4
C139 0.1U/10V_4
C138 0.1U/10V_4
C107 *0.1U/10V_4
C95 *0.1U/10V_4
C127 *0.1U/10V_4
C104 *0.1U/10V_4
C126 *0.1U/10V_4
C94 *0.1U/10V_4
+SMDDR_VTERM <30>
+SMDDR_VREF <30>
Quanta Computer Inc.
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DDR3 SODIMM: ONE CHANNEL
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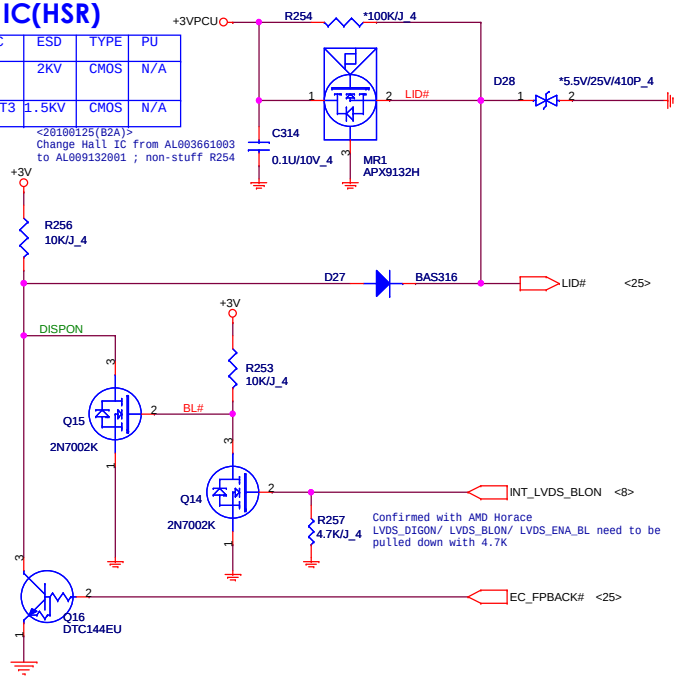
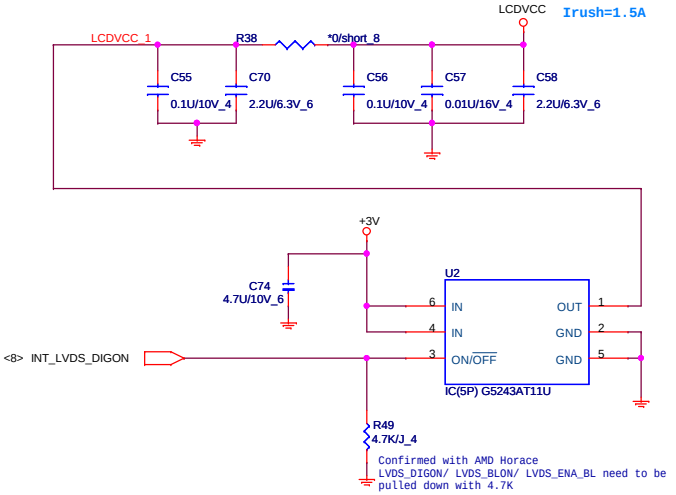
HALL IC(HSR)

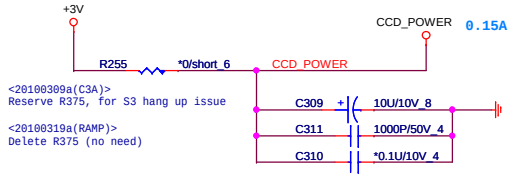
Hall IC	ESD	TYPE	PU
APX9132H AI-TRG	2KV	CMOS	N/A
EM-6781-T3	1.5KV	CMOS	N/A



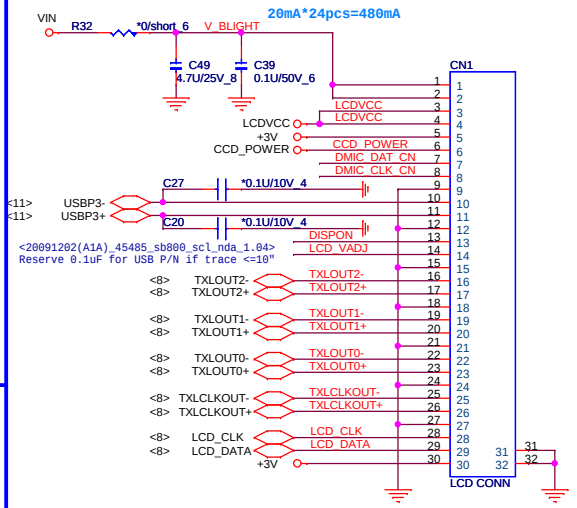
LCD POWER SWITCH(LDS)



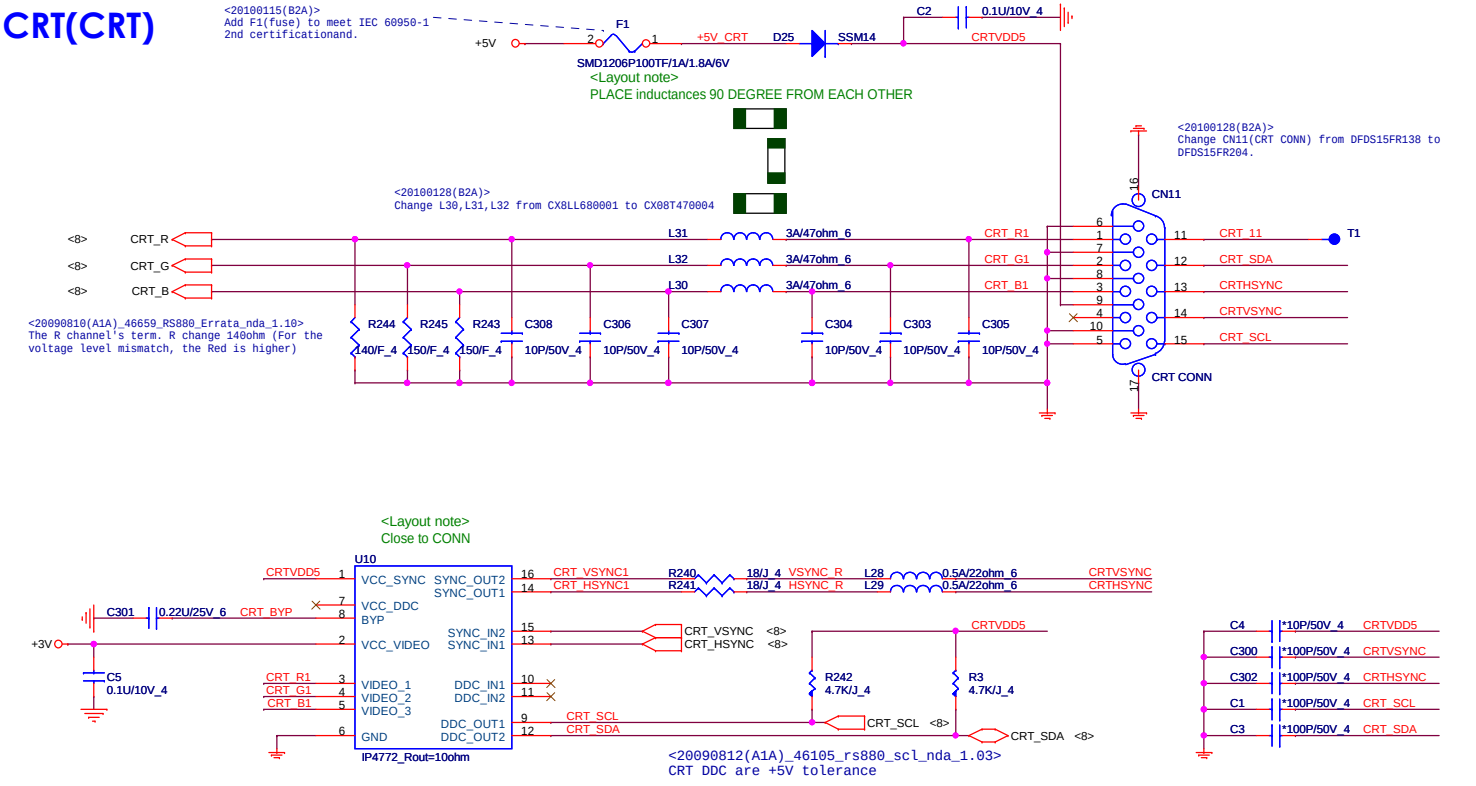
CAMERA POWER(CCD)

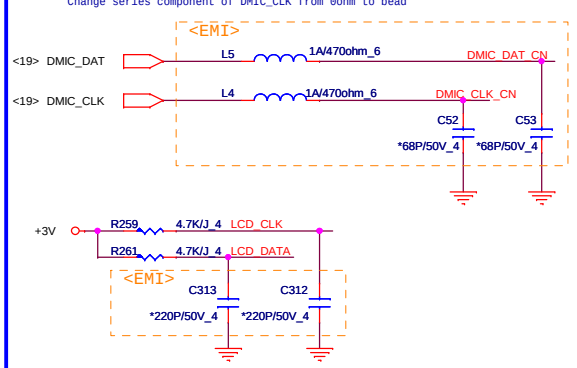


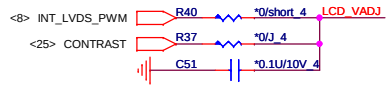
LCD MODULE(LDS)



CRT(CRT)







Quanta Computer Inc.

PROJECT : ZH9

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	CRT/LVDS	4A

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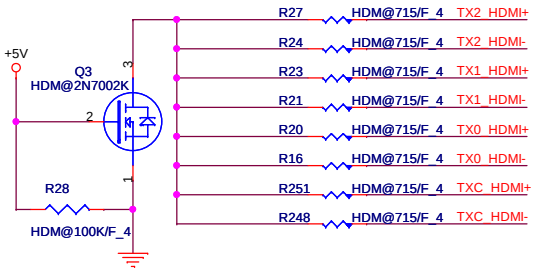
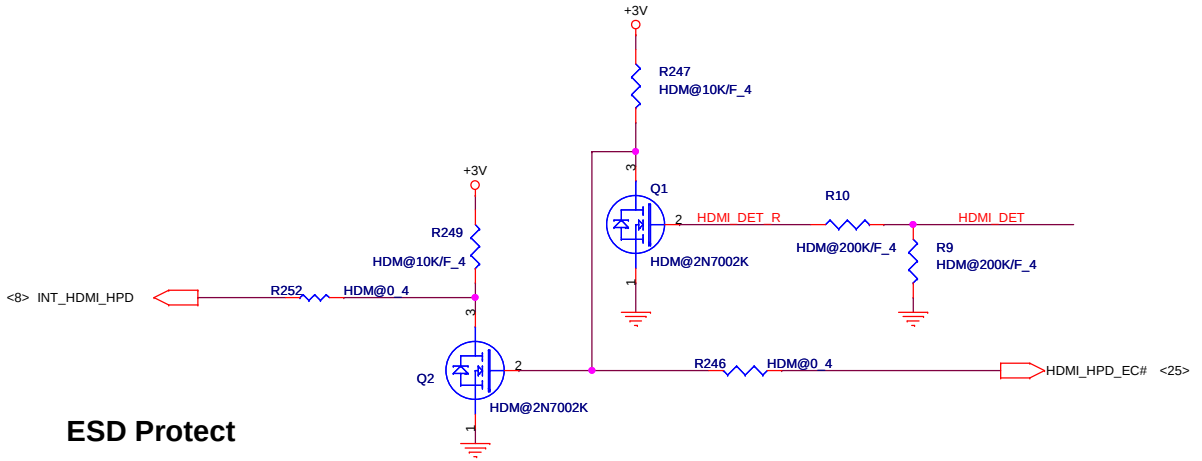
(HDM)

Close to HDMI Connector

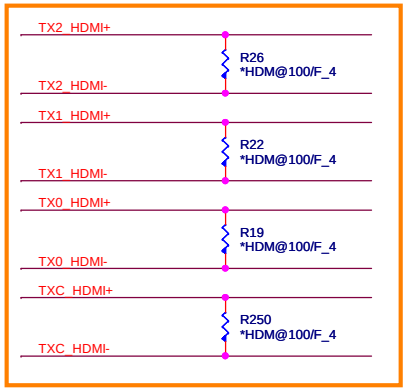


HDMI HPD SENSE



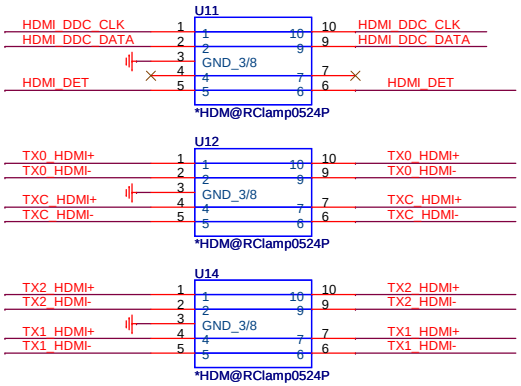
EMI reserve for HDMI(HDM)

Close connector

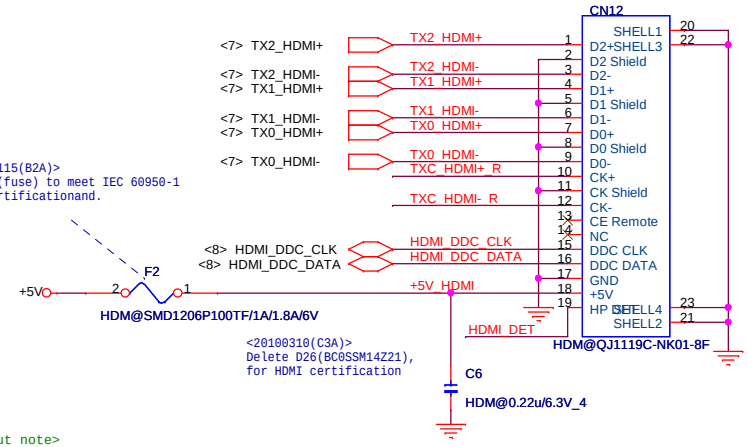


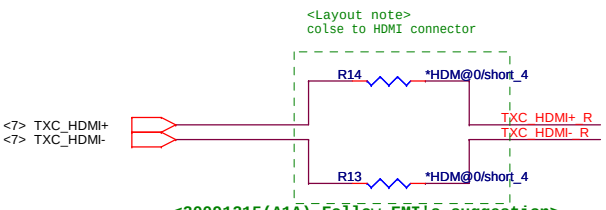
ESD Protect

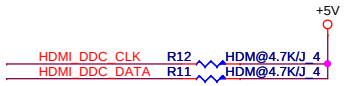
close to HDMI connector



HDMI PORT







<20091215(A1A)_Follow EMI's suggestion>
add a common mode chock in HDMI CLK to
prevent AMD issue

<20100324(RAMP)>
Delete L1 and change R13,R14 to shortpad.

Quanta Computer Inc.
PROJECT : ZH9

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	HDMI	4A
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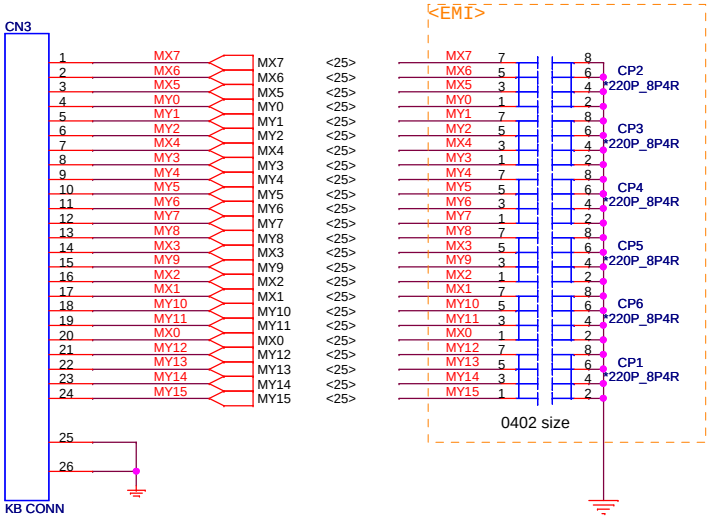
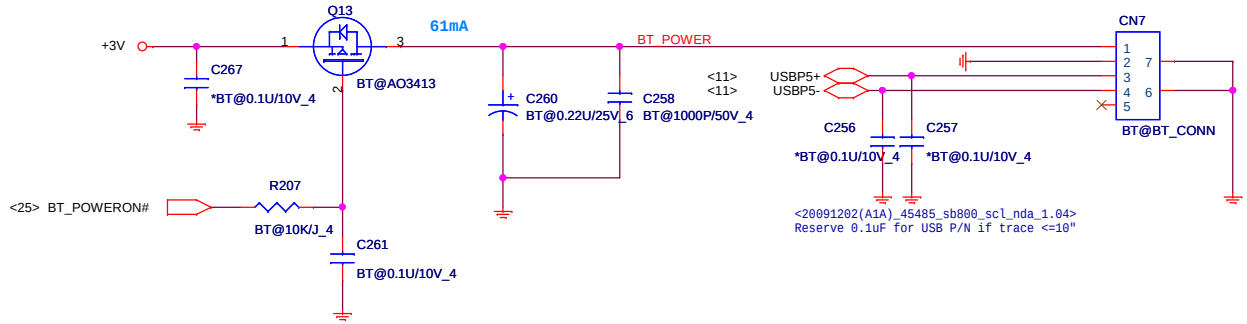
KEYBOARD(KBC)

<20100303(C3A)>
Change CP1~CP6 footprint from 8p4r-0402 to 8p4r-0402-smt, for SMT open issue.

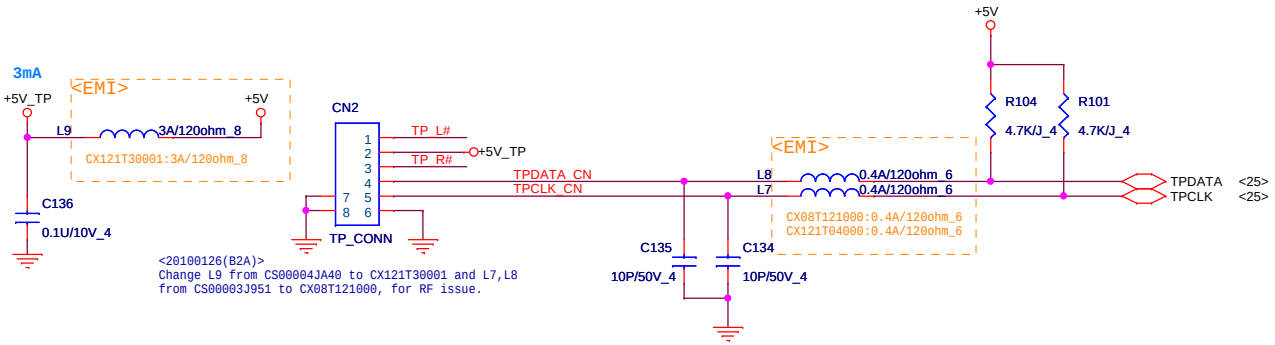


BLUETOOTH(BTM)

BT	PWR	LED
T77H056.00	+3V	
T60H928.33	+3V	



TOUCH PAD(TPD)



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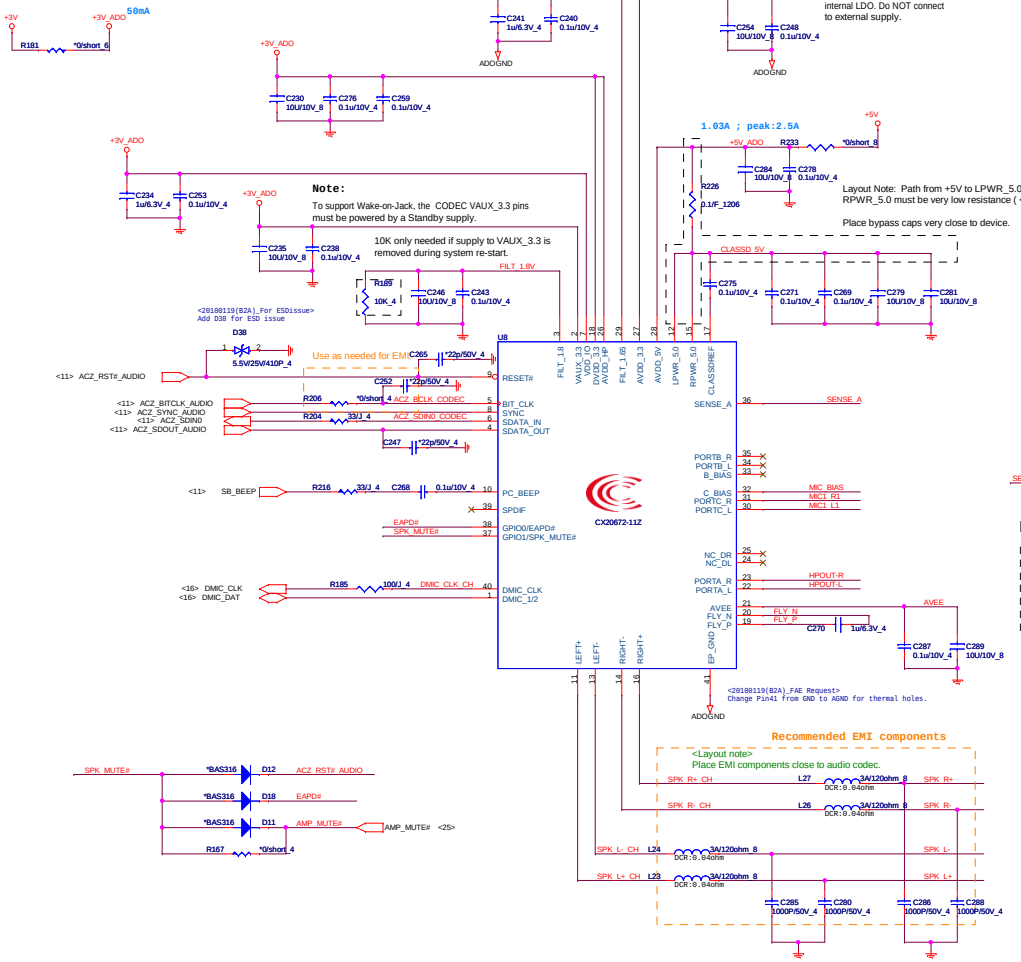
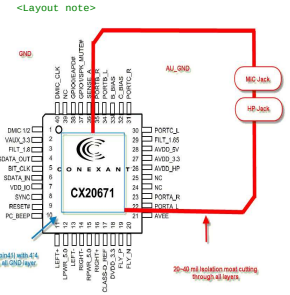
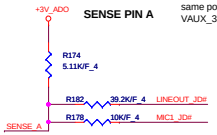
AUDIO CODEC





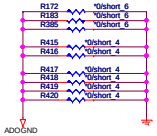
JACK DETECT RESISTORS



Sense resistor 5.11K must be connected to same power supply that is used for VAUX_3.3 pins.

Port Configuration

```
Port A:  Headphone jack (jack shared with S/PDIF)
Port B:  Internal analog mono mic (stereo option)/Line In
Port C:  Microphone jack
Port D:  LineOut jack(need cap) or Headphone jack(cap less)
Port G:  Internal stereo speakers
Port J:  Optional Internal stereo digital mic
Port H:  S/PDIF (jack shared with headphone)
```



<20100309(C3A)>
Delete R388,R375 ; Change C415,C290 to R415,R416(0ohm),
Stuff R172,R183,R385, Add R417~R420(0ohm), for EMI issue.

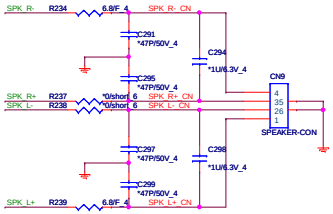
<20100311(C3A)>
Change R415,R417 to shortpad, for layout issue

<20100324(RAMP)>
Change R172,R183,R385,R416,R418~R420 to shortpad.

Speaker (AMP)

<20100126(B2A)>
Change R234,R239 from 0ohm(CS0800J3951) to 6.8ohm(CS-6803J900), for SPL

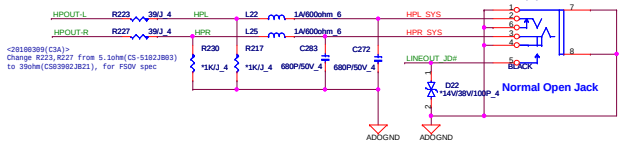
<20100323(RAMP)>
Change R234,R239 from 6.8ohm(CS-6803J900) to 6.8ohm(CS-6802FB80), for cost and shortage issue.



Earphone(AMP)

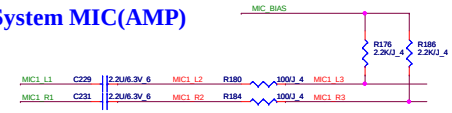
<Layout note>20091223
follow EMI suggestion , modify PIN6 from dummy to ADOGND

<20100309(C3A)>
Change L22,L25 from 0ohm to CX08T601000, C272,C283 to CH1606K9B00, for EMI issue.



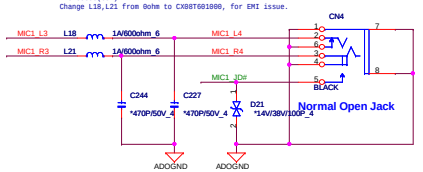
<20100309(C3A)>
Change R223,R227 from 5.1ohm(CS-5102JB03) to 39ohm(CS0390EJB21), for FSOV spec

System MIC(AMP)



<Layout note>20091223
follow EMI suggestion , modify PIN6 from dummy to ADOGND

<20100309(C3A)>
Change L18,L21 from 0ohm to CX08T601000, for EMI issue.



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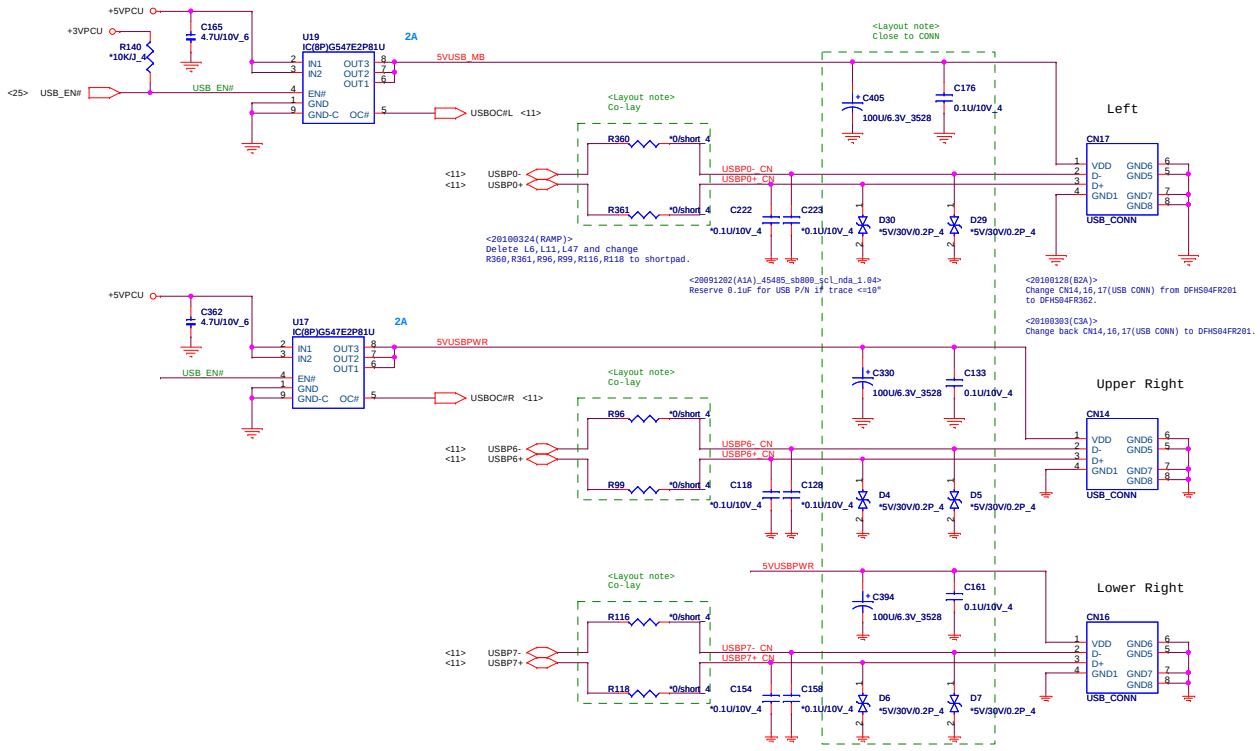
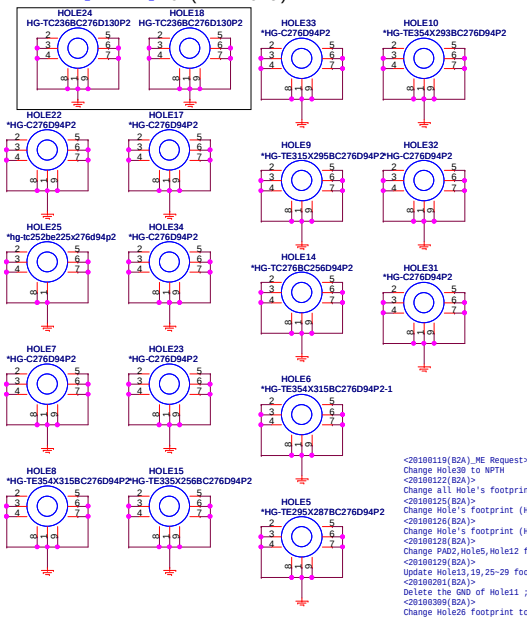
USB(USB)

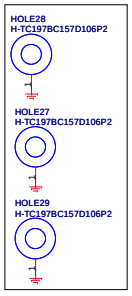


HOLE(OTH)

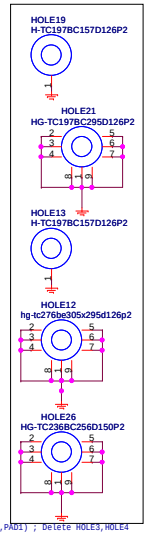
TOP(HDD Hole)

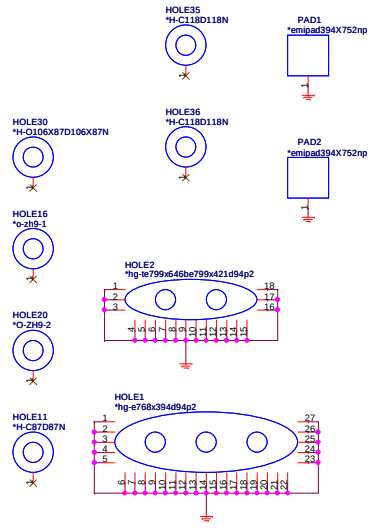


BOT (Mini-PCIe Hole)



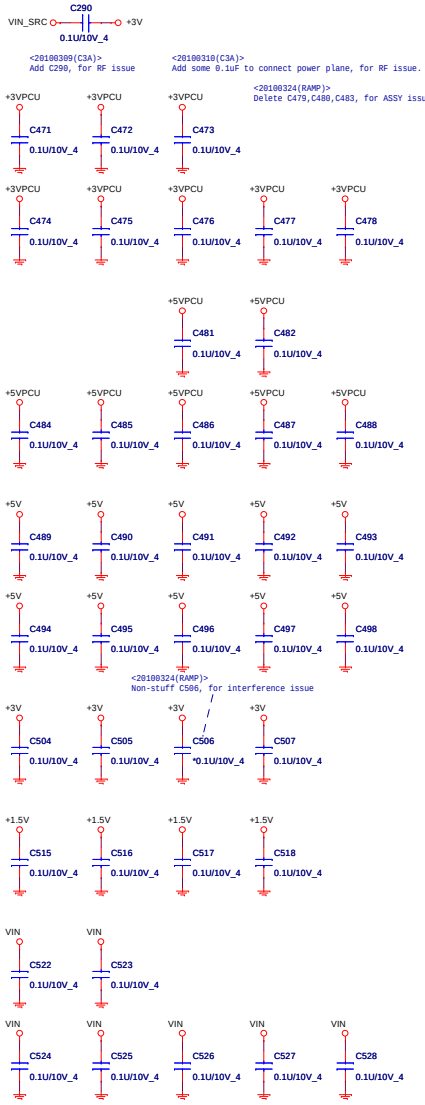
BOT(Thermal Hole)





<20100119(B2A)_ME Request>
Change Hole30 to NPTH
<20100122(B2A)>
Change all Hole's footprint for 凸鍋
<20100125(B2A)>
Change Hole's footprint (HOLE12,HOLE25,HOLE1,HOLE2,HOLE20,PAD1) ; Delete HOLE3,HOLE4
<20100126(B2A)>
Change Hole's footprint (HOLE12)
<20100128(B2A)>
Change PAD2,Hole5,Hole12 footprint ; add two holes (Hole35,Hole36)
<20100129(B2A)>
Update Hole13,19,25~29 footprint.
<20100201(B2A)>
Delete the GND of Hole11 ; add a nut(MBFJ6002010) on Hole26 on BOT side.
<20100309(B2A)>
Change Hole26 footprint to HG-TC236BC256D150P2

EMI(EMC)



Quanta Computer Inc.

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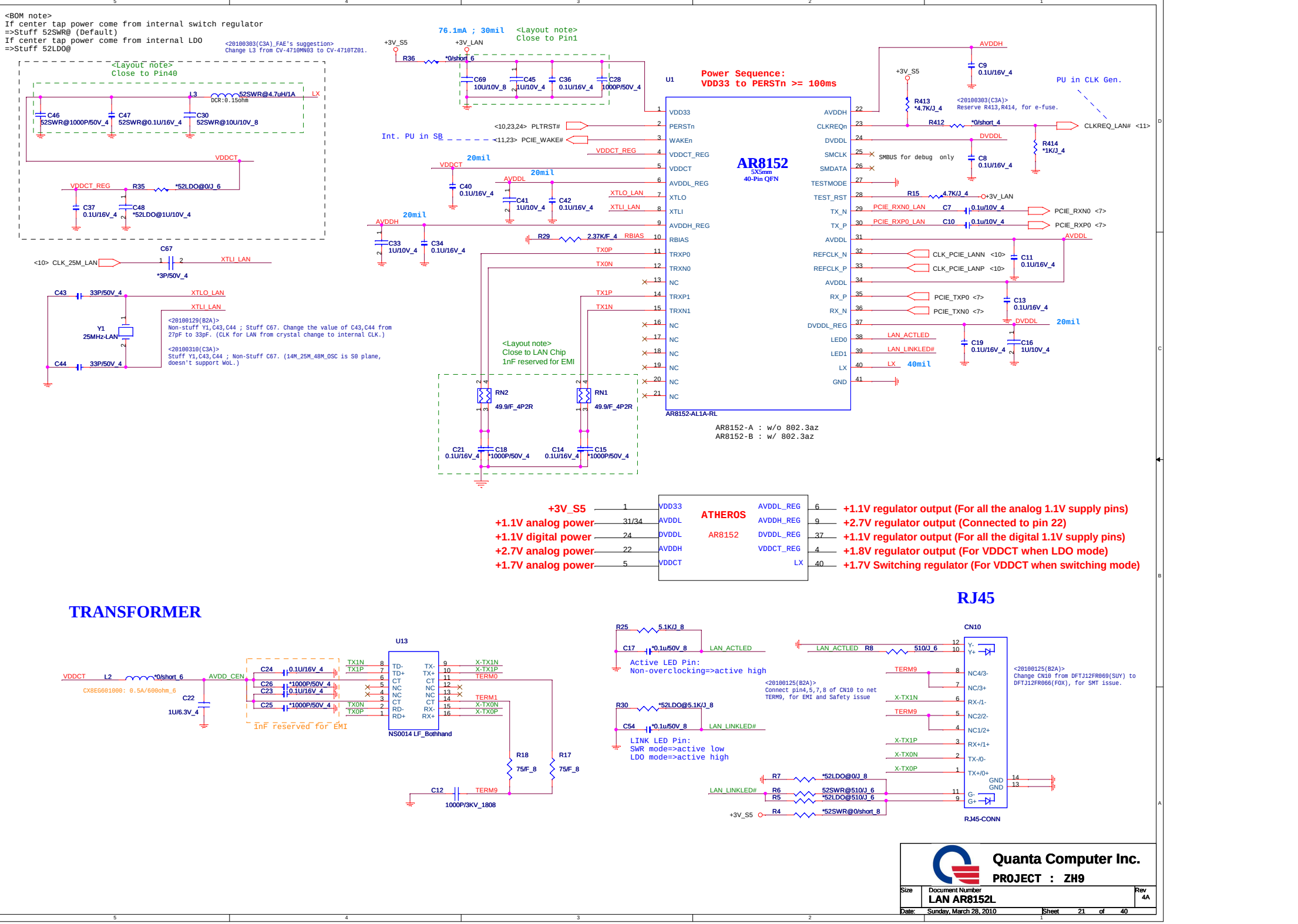
<BOM note>
If center tap power come from internal switch regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@
<20100303(C3A)_FAE's suggestion>
Change L3 from CV-4710MN03 to CV-4710TZ01.
<Layout note>
Close to Pin40
L3
52SWR@4.7uH/1A
DCR:0.15ohm
LX
C46
52SWR@1000P/50V_4
C47
52SWR@0.1U/16V_4
C30
52SWR@10U/10V_8
VDDCT
VDDCT_REG
R35
*52LDO@0/J_6
C37
0.1U/16V_4
C48
*52LDO@1U/10V_4
C67
<10> CLK_25M_LAN
XTLI_LAN
*3P/50V_4
C43
33P/50V_4
XTLO_LAN
Y1
25MHz-LAN
C44
33P/50V_4
<20100129(B2A)>
Non-stuff Y1,C43,C44 ; Stuff C67. Change the value of C43,C44 from 27pF to 33pF. (CLK for LAN from crystal change to internal CLK.)
<20100310(C3A)>
Stuff Y1,C43,C44 ; Non-Stuff C67. (14M_25M_48M_OSC is S0 plane, doesn't support WoL.)
76.1mA ; 30mil
<Layout note>
Close to Pin1
+3V_S5
+3V_LAN
R36
*0/short_6
C69
10U/10V_8
C45
1U/10V_4
C36
0.1U/16V_4
C28
1000P/50V_4
U1
Power Sequence:
VDD33 to PERSTn >= 100ms
Int. PU in SB
<10,23,24> PLTRST#
<11,23> PCIE_WAKE#
VDDCT_REG
20mil
VDDCT
C40
0.1U/16V_4
AVDDL
C41
1U/10V_4
C42
0.1U/16V_4
XTLO_LAN
XTLI_LAN
AVDDH
C33
1U/10V_4
C34
0.1U/16V_4
R29
2.37K/F_4
RBIAS
TX0P
TX0N
TX1P
TX1N
<Layout note>
Close to LAN Chip
1nF reserved for EMI
RN2
49.9/F_4P2R
RN1
49.9/F_4P2R
C21
0.1U/16V_4
C18
*1000P/50V_4
C14
0.1U/16V_4
C15
*1000P/50V_4
VDD33
PERSTn
WAKEn
VDDCT_REG
VDDCT
AVDDL_REG
XTLO
XTLI
AVDDH_REG
RBIAS
TRXP0
TRXN0
NC
TRXP1
TRXN1
NC
NC
NC
NC
NC
AR8152
5X5mm
40-Pin QFN
AR8152-AL1A-RL
AVDDH
CLKREQn
DVDDL
SMCLK
SMDATA
TESTMODE
TEST_RST
TX_N
TX_P
AVDDL
REFCLK_N
REFCLK_P
AVDDL
RX_P
RX_N
DVDDL_REG
LED0
LED1
LX
GND
SMBUS for debug only
R15
4.7K/J_4
+3V_LAN
PCIE_RXN0_LAN
C7
0.1u/10V_4
PCIE_RXN0 <7>
PCIE_RXP0_LAN
C10
0.1u/10V_4
PCIE_RXP0 <7>
CLK_PCIE_LANN <10>
CLK_PCIE_LANP <10>
PCIE_TXP0 <7>
PCIE_TXN0 <7>
LAN_ACTLED
LAN_LINKLED#
LX
40mil
C9
0.1U/16V_4
PU in CLK Gen.
R413
*4.7K/J_4
<20100303(C3A)>
Reserve R413,R414, for e-fuse.
R412
*0/short_4
CLKREQ_LAN# <11>
R414
*1K/J_4
C8
0.1U/16V_4
C11
0.1U/16V_4
C13
0.1U/16V_4
C19
0.1U/16V_4
C16
1U/10V_4
20mil
AR8152-A : w/o 802.3az
AR8152-B : w/ 802.3az
+3V_S5
1
+1.1V analog power
31/34
+1.1V digital power
24
+2.7V analog power
22
+1.7V analog power
5
VDD33
AVDDL
DVDDL
AVDDH
VDDCT
ATHEROS
AR8152
AVDDL_REG
AVDDH_REG
DVDDL_REG
VDDCT_REG
LX
6
9
37
4
40
+1.1V regulator output (For all the analog 1.1V supply pins)
+2.7V regulator output (Connected to pin 22)
+1.1V regulator output (For all the digital 1.1V supply pins)
+1.8V regulator output (For VDDCT when LDO mode)
+1.7V Switching regulator (For VDDCT when switching mode)
TRANSFORMER
VDDCT
L2
*0/short_6
CX8EG601000: 0.5A/600ohm_6
AVDD_CEN
C22
1U/6.3V_4
C24
0.1U/16V_4
C26
*1000P/50V_4
C23
0.1U/16V_4
C25
*1000P/50V_4
InF reserved for EMI
U13
TD-
TD+
CT
NC
NC
CT
RD-
RD+
TX-
TX+
CT
NC
NC
CT
RX-
RX+
TX1N
TX1P
TX0N
TX0P
X-TX1N
X-TX1P
TERM0
TERM1
X-TX0N
X-TX0P
NS0014 LF_Bothhand
R18
75/F_8
R17
75/F_8
C12
1000P/3KV_1808
TERM9
RJ45
R25
5.1K/J_8
C17
*0.1u/50V_8
LAN_ACTLED
Active LED Pin:
Non-overclocking=>active high
R30
*52LDO@5.1K/J_8
C54
*0.1u/50V_8
LAN_LINKLED#
LINK LED Pin:
SWR mode=>active low
LDO mode=>active high
<20100125(B2A)>
Connect pin4,5,7,8 of CN10 to net TERM9, for EMI and Safety issue
CN10
LAN_ACTLED
R8
510/J_6
Y-
Y+
NC4/3-
NC/3+
RX-/1-
NC2/2-
NC1/2+
RX+/1+
TX-/0-
TX+/0+
G-
G+
GND
GND
<20100125(B2A)>
Change CN10 from DFTJ12FR069(SUY) to DFTJ12FR066(FOX), for SMT issue.
R7
*52LDO@0/J_8
R6
52SWR@510/J_6
R5
*52LDO@510/J_6
R4
*52SWR@0/short_8
RJ45-CONN
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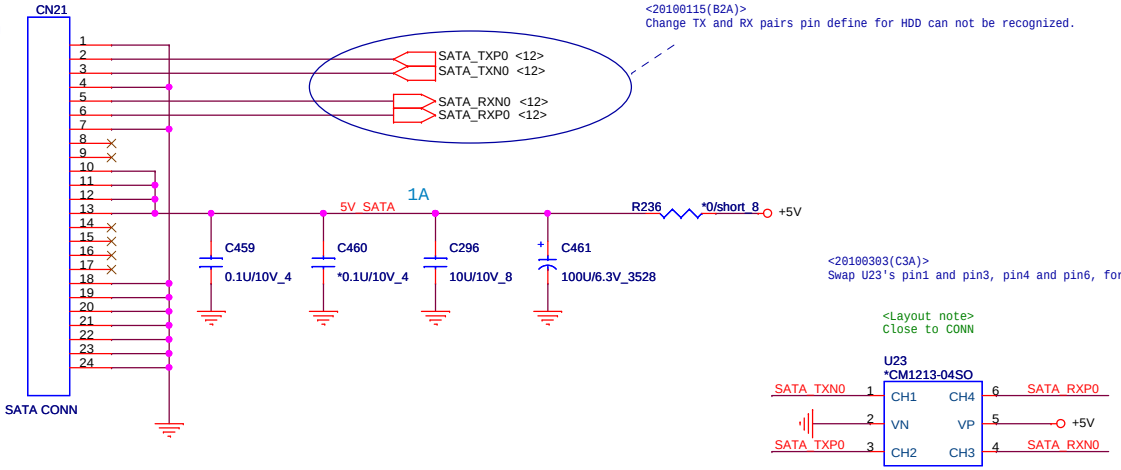
2.5" SATA HDD(HDD)



<20100115(B2A)>
Change TX and RX pairs pin define for HDD can not be recognized.

<20100303(C3A)>
Swap U23's pin1 and pin3, pin4 and pin6, for layout issue.

<Layout note>
Close to CONN

LED/SW(UIF)

<20091214(A1A)_Confirm with Acer Johnson_Yeh>
The JV01_NL and SJV01_NL had 4 LEDs --> Power / Battery / HDD / Communication

<20100203(B2A)>
Change R401 from CS13302JB21 to CS12702JB14
Change R402 from CS13302JB21 to CS14702JB28
Change R403 from CS13302JB21 to CS11202JB21
Change R404,R406 from CS13302JB21 to CS15602JB19
Change R405,R407 from CS13302JB21 to CS13602JB13
For LED's light issue.

<20100326(RAMP)>
Change R401 from CS12702JB14 to CS13302JB21
Change R404,R406 from CS15602JB19 to CS14702JB28
Change R403 from CS11202JB21 to CS12702JB14
Change R405,R407 from CS13602JB13 to CS12702JB14
For LED's light issue.

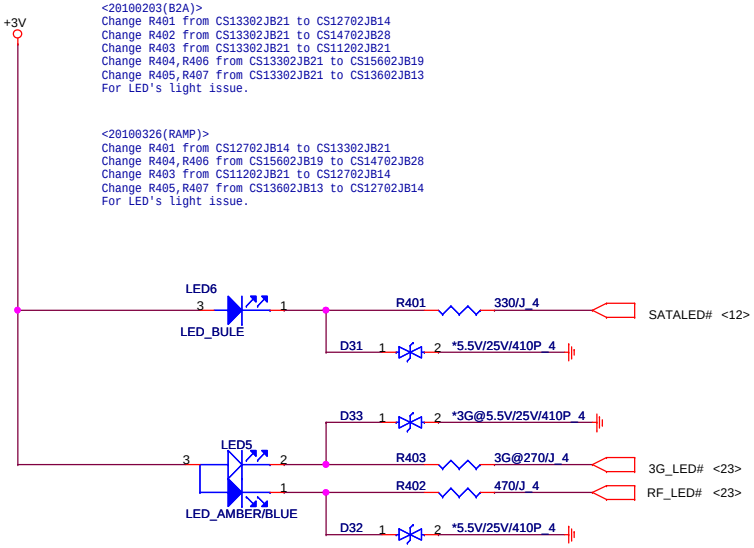
CAPS LED

NUM LED

HDD LED

3G LED

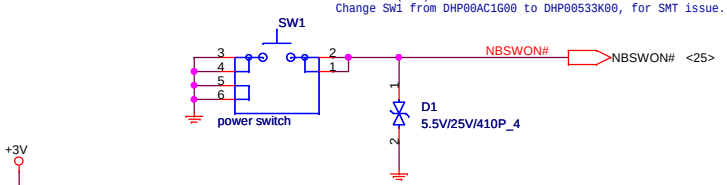
WLAN LED

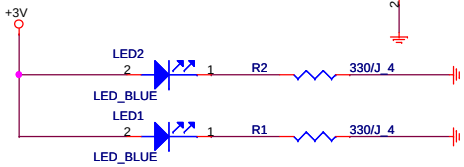


BT LED

PWR indicator

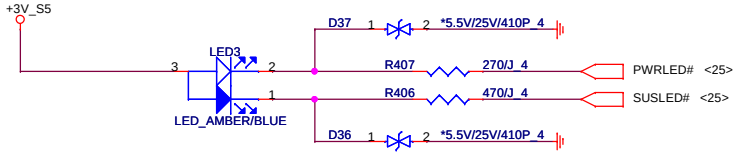
<20100125(B2A)>
Change SW1 from DHP00AC1G00 to DHP00533K00, for SMT issue.





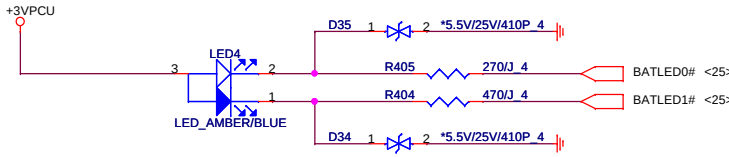
PWR LED

SUS LED



FULL LED

CHG LED



<LED spec>
BLUE :
Vf = 2.7~3.2V ; If = 5mA
BLUE/ORANGE :
BH→Vf = 2.7~3.7V ; If = 20mA max=25mA
S2→Vf = 1.7~2.4V ; If = 20mA max=25mA

ID(Left-->Right)
Power LED/BATT LED/HDD LED/WiFi LED

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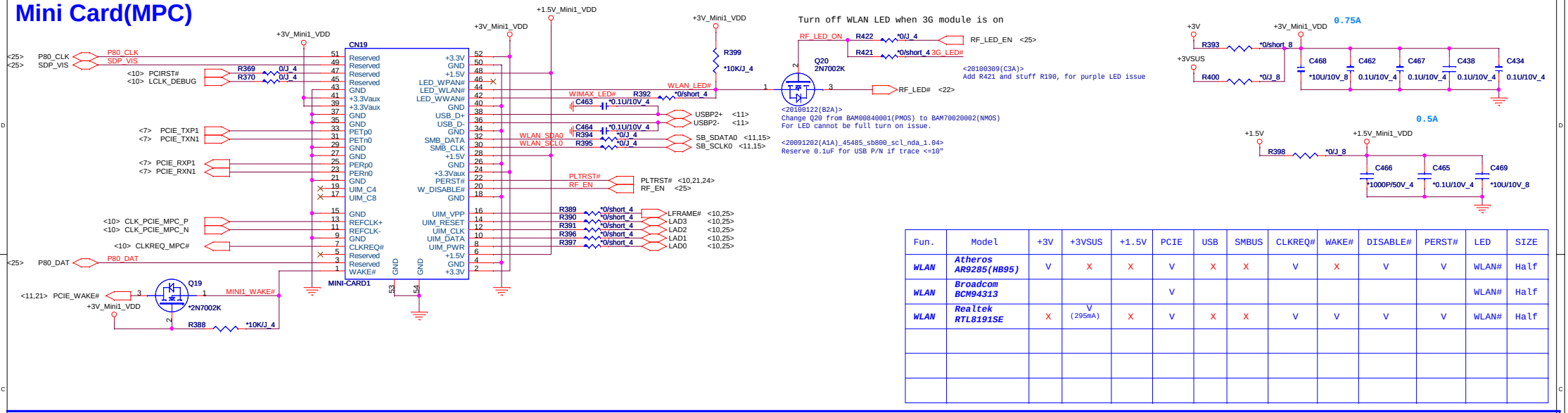
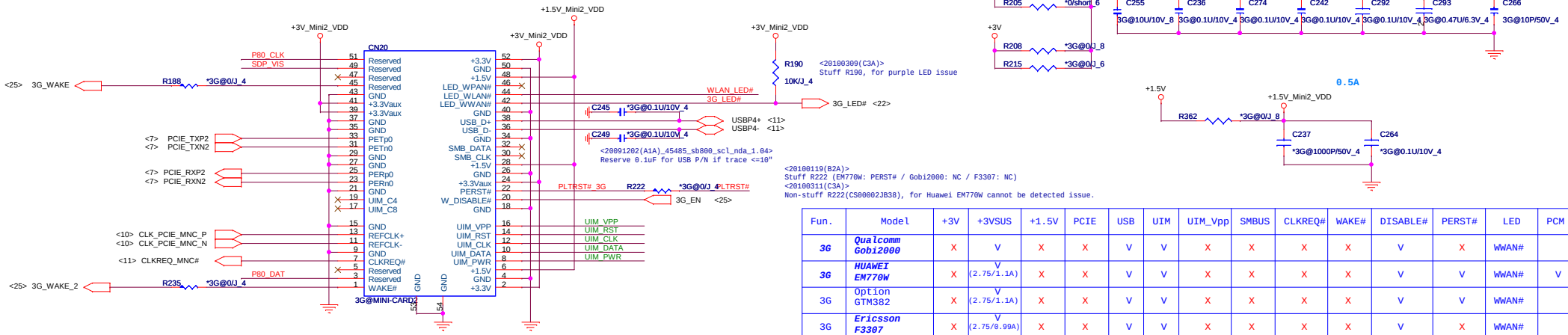
Mini Card(MPC)



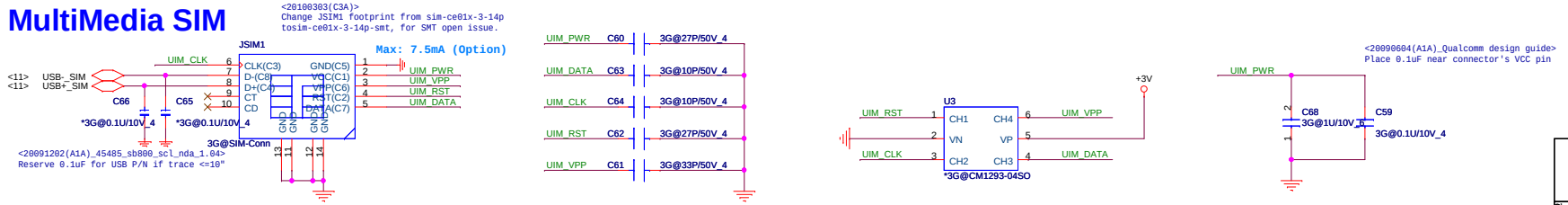
Fun.	Model	+3V	+3VSUS	+1.5V	PCIE	USB	SMBUS	CLKREQ#	WAKE#	DISABLE#	PERST#	LED	SIZE
WLAN	Atheros AR9285(HB95)	V	X	X	V	X	X	V	X	V	V	WLAN#	Half
WLAN	Broadcom BCM94313				V							WLAN#	Half
WLAN	Realtek RTL8191SE	X	V (295mA)	X	V	X	X	V	V	V	V	WLAN#	Half

Mini Card 2(MNC)



Fun.	Model	+3V	+3VSUS	+1.5V	PCIE	USB	UIM	UIM_Vpp	SMBUS	CLKREQ#	WAKE#	DISABLE#	PERST#	LED	PCM	SIZE
3G	Qualcomm Gobi2000	X	V	X	X	V	V	X	X	X	X	V	X	WWAN#		Full
3G	HUAWEI EM770W	X	V (2.75/1.1A)	X	X	V	V	X	X	X	X	V	V	WWAN#	V	Full
3G	Option GTM382	X	V (2.75/1.1A)	X	X	V	V	X	X	X	X	V	V	WWAN#		Full
3G	Ericsson F3307	X	V (2.75/0.99A)	X	X	V	V	X	X	X	X	V	X	WWAN#		Full
Wimax	Intel 5150(512...)	X	V (643mA)	X	V	V	X	X	X	V	V	V	V	WLAN# WWAN#		Full

MultiMedia SIM



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	Mini-Card/WL/3G/SIM	4A
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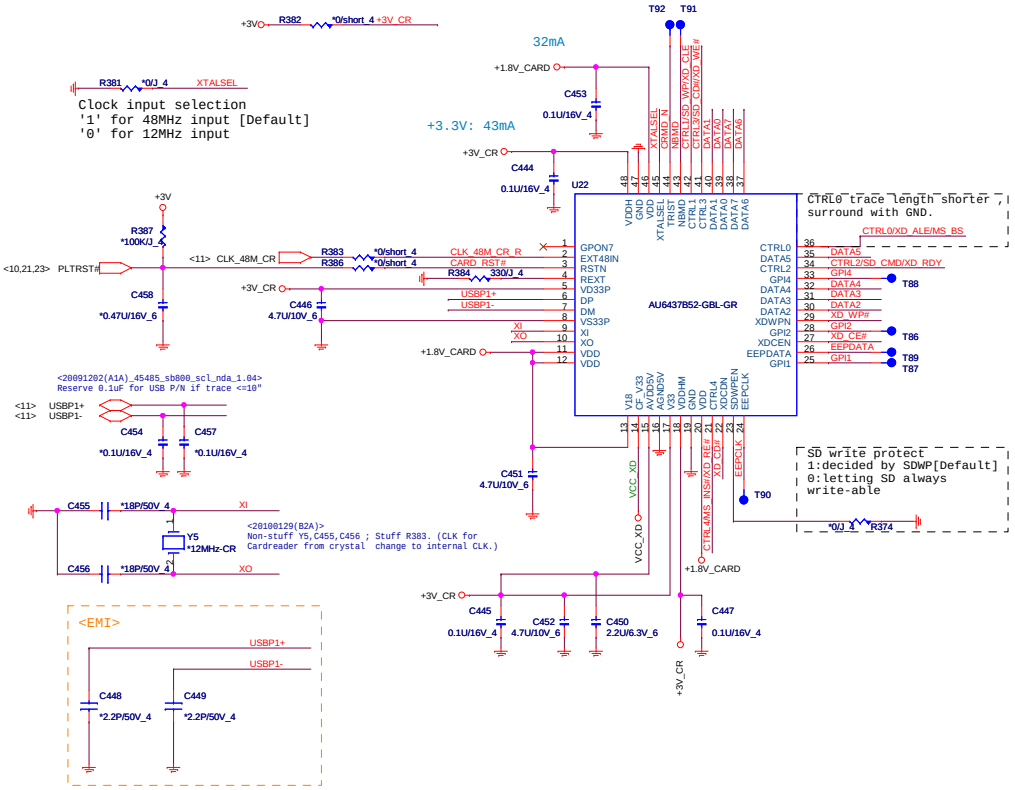
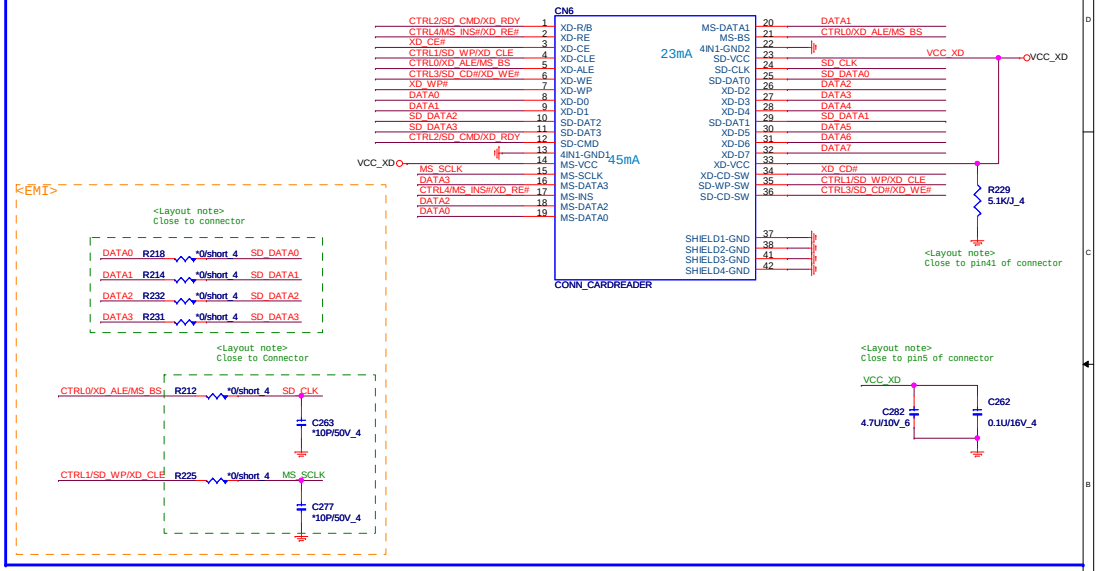
AU6437B52-GBL-GR (MMC)



4 IN 1 CARD READER (MMC)



Quanta Computer Inc.			
PROJECT : ZH9			
Size	Document Number		Rev
	AU6437 (Card Reader)		4A
Date: Sunday, March 28, 2010	Sheet 24	of	40

EC(KBC)

U6

NPCE781L(A0DX)

<Layout note>
Place every 0.1uF
close to every
power pin

<20090602(A1A)_Vendor suggest>
Place 10nF-0.1uF capacitors for
every AD input. And close to the AD
input.

DS page248, GA20/KBRST# are VCC well, but
they were held low when VDD well is off.

<20090831(A1A)_EC team suggest>
1.remove diode from EC_SCI#

<EMI>

<20090602(A1A)_Vendor suggest>
Add 2.2ohm series resister for
ESD/EOS issue

<20090831(A1A)_EC team suggest>
1.remove diode from DNBSWON#

<20090831(A1A)_EC team suggest>
1.change R7027/R7028 to 1M or 100K ohm
2.change PWR/SUS LED's power from +3VPCU to +3V_S5 or +3VSUS
can reduce pull-high resistor of SUSLED#/PWRLED#

<20090721_FAE suggestion>
Stuff 100K and close to EC side
for improving power consumption

<20100319(RAMP)>
Non-stuff D9,D17, for cost down.

I/O ADDRESS SETTING

TEST Mode	TEST#	XORTR#	TRIST#
no test mode selected (normal operation)	1	X	X
XOR-tree test mode	0	0	1
ICT mode	0	1	0
Reserved exclusively for Nuvoton use	0	00 or 11	

SHBM=0: Enable shared memory with host BIOS

SM BUS PU

1ST: Battery
2ND: CPU Thermal Sensor / DTS
3RD: VGA Thermal Sensor

SPI FLASH

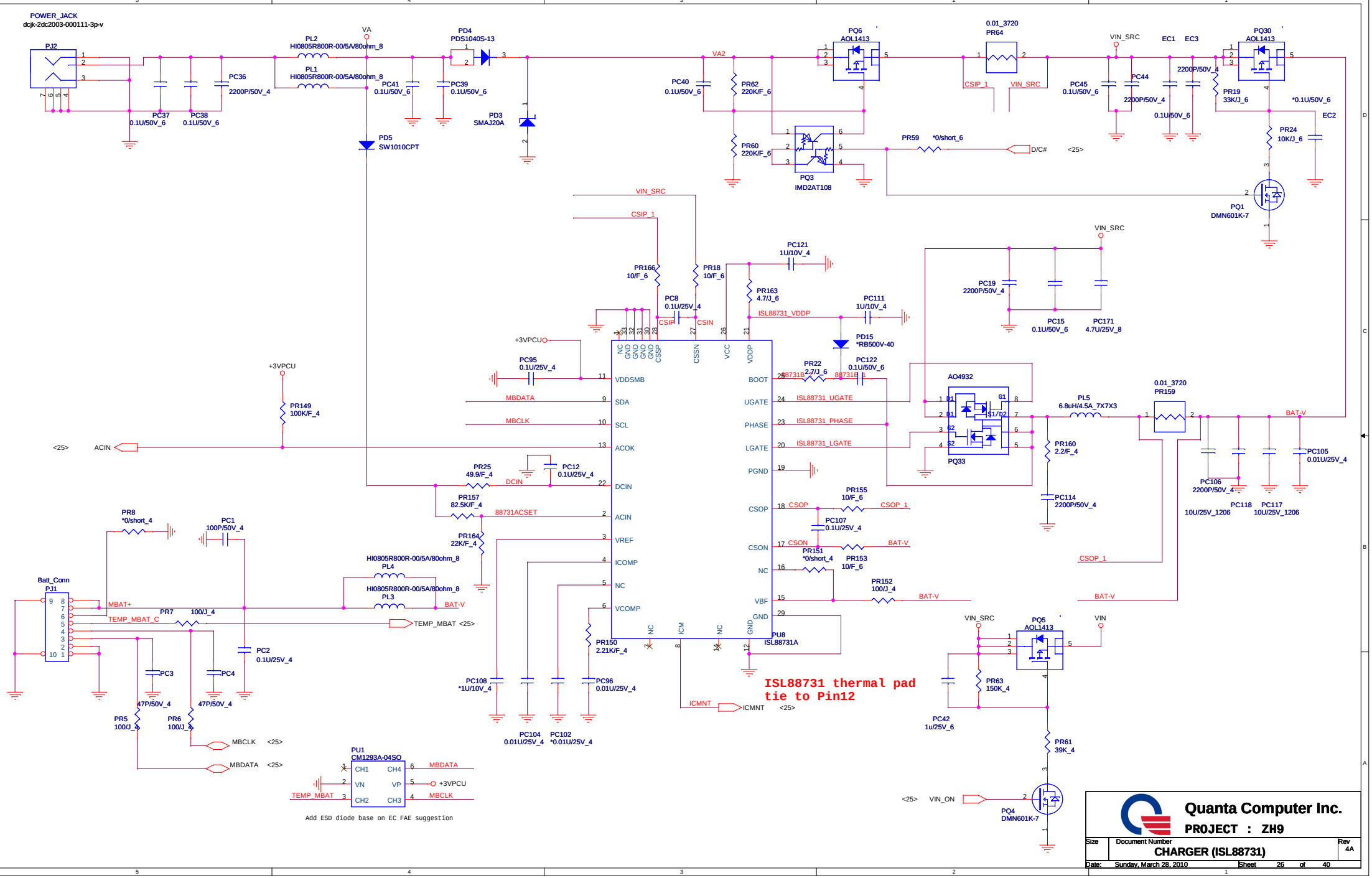
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the
flash device should be 50MHz (or faster)

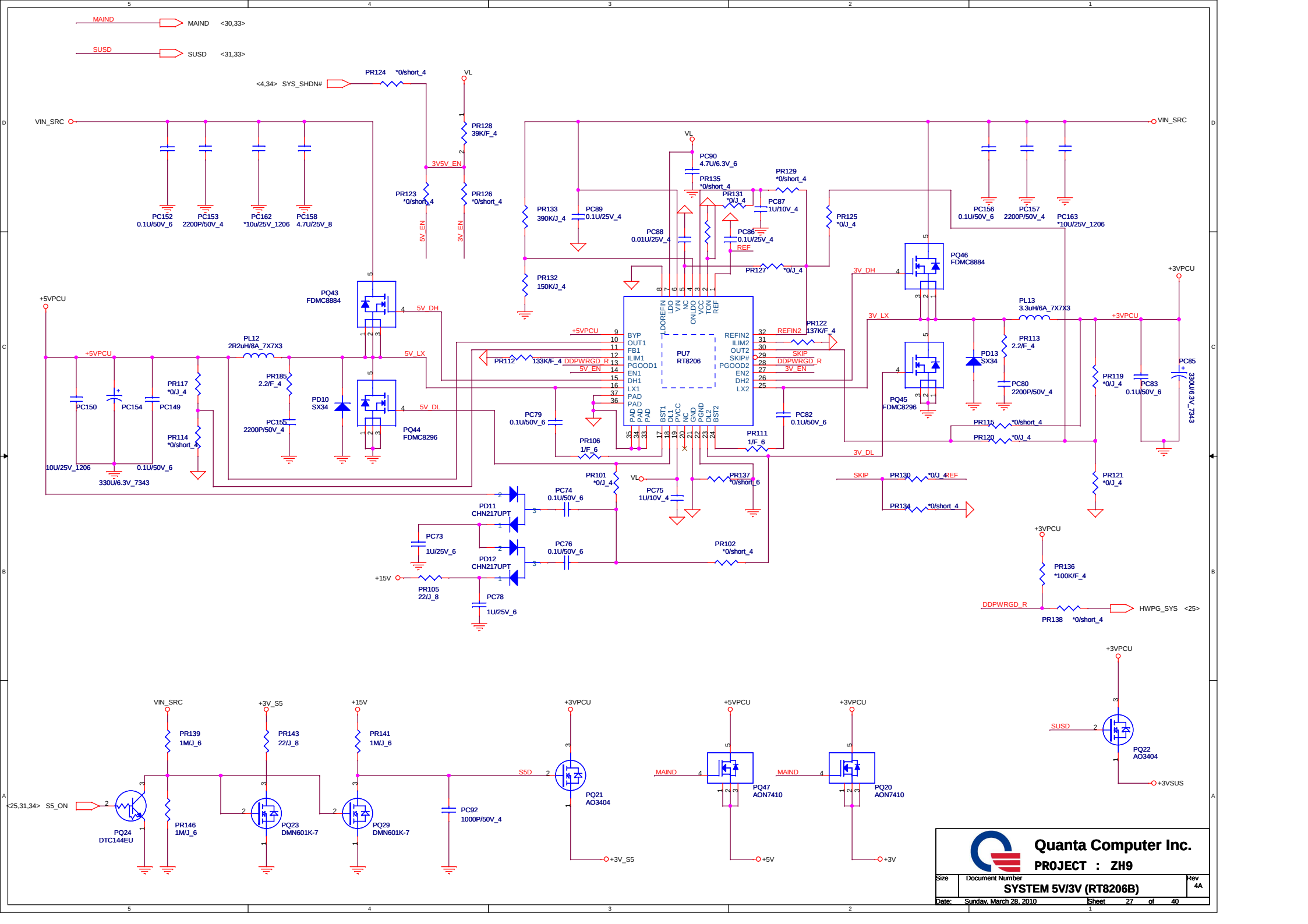
HWPG

INTERNAL KEYBOARD STRIP SET

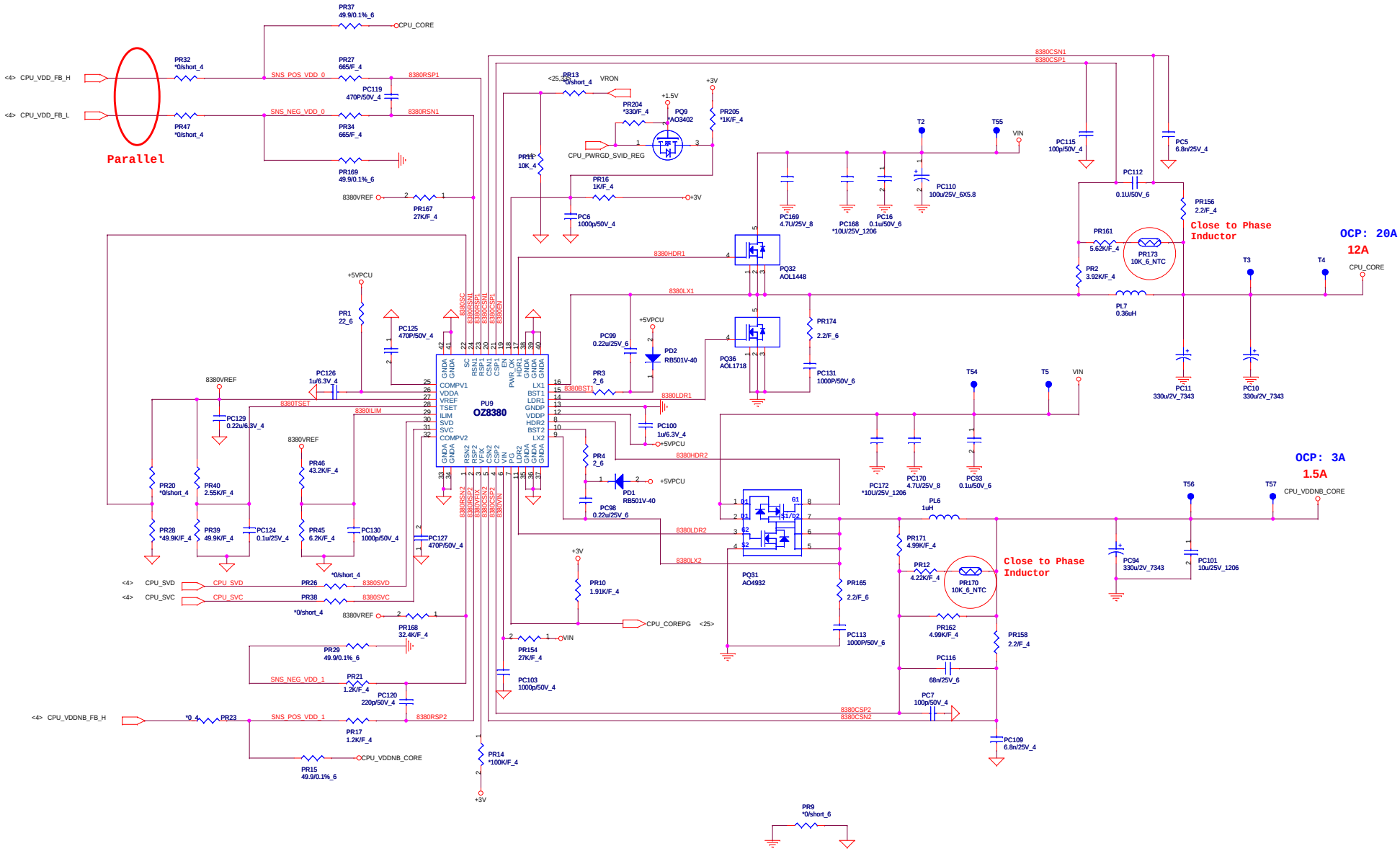
Plam Rest
Thermal Sersor

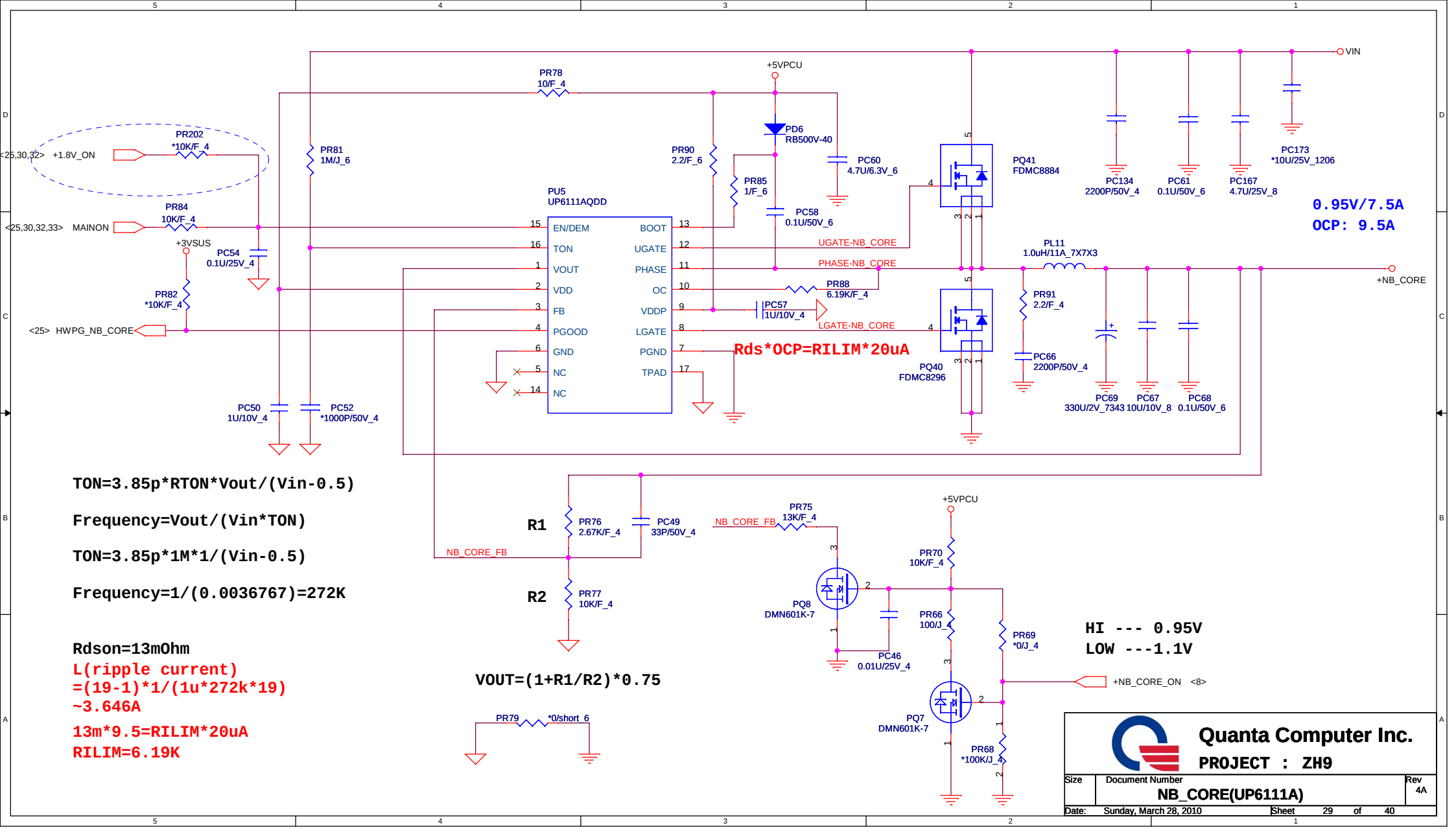
Quanta Computer Inc.	
PROJECT : ZH9	
Size	Document Number: NPCE781L & FLASH — Rev: 4A
Date: Sunday, March 28, 2010	Sheet 25 of 40


POWER_JACK
dcjk-2dc2003-000111-3p-v
PJ2
VA
PL2
HI0805R800R-00/5A/80ohm_8
PL1
HI0805R800R-00/5A/80ohm_8
PD4
PDS1040S-13
PD3
SMAJ20A
PD5
SW1010CPT
PC36
2200P/50V_4
PC37
0.1U/50V_6
PC38
0.1U/50V_6
PC41
0.1U/50V_6
PC39
0.1U/50V_6
VA2
PC40
0.1U/50V_6
PR62
220K/F_6
PR60
220K/F_6
PQ6
AOL1413
PQ3
IMD2AT108
PR64
0.01_3720
CSIP_1
VIN_SRC
PR59
*0/short_6
D/C#
<25>
PC45
0.1U/50V_6
PC44
2200P/50V_4
EC1
EC3
EC2
PR19
33K/J_6
PR24
10K/J_6
PQ30
AOL1413
PQ1
DMN601K-7
PR166
10/F_6
PR18
10/F_6
PC8
0.1U/25V_4
PR163
4.7/J_6
PC121
1U/10V_4
PC111
1U/10V_4
ISL88731_VDDP
PD15
*RB500V-40
PC122
0.1U/50V_6
PC19
2200P/50V_4
PC15
0.1U/50V_6
PC171
4.7U/25V_8
+3VPCU
PC95
0.1U/25V_4
PR149
100K/F_4
ACIN
PR25
49.9/F_4
PC12
0.1U/25V_4
DCIN
PR157
82.5K/F_4
88731ACSET
PR164
22K/F_4
MBDATA
MBCLK
NC
GND
CSSP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
PU8
ISL88731A
PR22
2.7/J_6
AO4932
PQ33
PL5
6.8uH/4.5A_7X7X3
0.01_3720
PR159
BAT-V
PR160
2.2/F_4
PC114
2200P/50V_4
PC106
2200P/50V_4
PC118
10U/25V_1206
PC117
10U/25V_1206
PC105
0.01U/25V_4
PR155
10/F_6
CSOP_1
PC107
0.1U/25V_4
PR151
*0/short_4
PR153
10/F_6
PR152
100/J_4
PR150
2.21K/F_4
PC108
*1U/10V_4
PC104
0.01U/25V_4
PC102
*0.01U/25V_4
PC96
0.01U/25V_4
ICMNT
<25>
ISL88731 thermal pad
tie to Pin12
PR8
*0/short_4
PC1
100P/50V_4
Batt_Conn
PJ1
MBAT+
TEMP_MBAT_C
PR7
100/J_4
HI0805R800R-00/5A/80ohm_8
PL4
HI0805R800R-00/5A/80ohm_8
PL3
BAT-V
TEMP_MBAT
<25>
PC2
0.1U/25V_4
PC3
PC4
47P/50V_4
47P/50V_4
PR5
100/J_4
PR6
100/J_4
MBCLK
<25>
MBDATA
<25>
PU1
CM1293A-04SO
CH1
CH4
VN
VP
CH2
CH3
MBDATA
+3VPCU
MBCLK
TEMP_MBAT
Add ESD diode base on EC FAE suggestion
PR63
150K_4
PC42
1u/25V_6
PQ5
AOL1413
VIN
PR61
39K_4
PQ4
DMN601K-7
VIN_ON
Quanta Computer Inc.
PROJECT : ZH9
Size
Document Number
CHARGER (ISL88731)
Rev
4A
Date: Sunday, March 28, 2010
Sheet 26 of 40



Quanta Computer Inc.		
PROJECT : ZH9		
Size	Document Number: SYSTEM 5V/3V (RT8206B)	Rev: 4A
Date: Sunday, March 28, 2010	Sheet 27 of 40	


Parallel
PU9
OZ8380
Close to Phase Inductor
OCP: 20A
12A
Close to Phase Inductor
OCP: 3A
1.5A
Quanta Computer Inc.
PROJECT : ZH9
AMD CPU Core (OZ8380)
Size
Document Number
Rev
4A
Date: Sunday, March 28, 2010
Sheet 28 of 40


VIN
+5VPCU
PR78
10/F_4
PD6
RB500V-40
PR202
*10K/F_4
<25,30,32> +1.8V_ON
PR81
1M/J_6
PR90
2.2/F_6
PR85
1/F_6
PC60
4.7U/6.3V_6
PC58
0.1U/50V_6
PU5
UP6111AQDD
PR84
10K/F_4
<25,30,32,33> MAINON
+3VSUS
PC54
0.1U/25V_4
PR82
*10K/F_4
<25> HWPG_NB_CORE
EN/DEM
TON
VOUT
VDD
FB
PGOOD
GND
NC
NC
BOOT
UGATE
PHASE
OC
VDDP
LGATE
PGND
TPAD
UGATE-NB_CORE
PHASE-NB_CORE
LGATE-NB_CORE
PR88
6.19K/F_4
PC57
1U/10V_4
Rds*OCP=RILIM*20uA
PQ41
FDMC8884
PQ40
FDMC8296
PC134
2200P/50V_4
PC61
0.1U/50V_6
PC167
4.7U/25V_8
PC173
*10U/25V_1206
0.95V/7.5A
OCP: 9.5A
PL11
1.0uH/11A_7X7X3
PR91
2.2/F_4
PC66
2200P/50V_4
PC69
330U/2V_7343
PC67
10U/10V_8
PC68
0.1U/50V_6
+NB_CORE
PC50
1U/10V_4
PC52
*1000P/50V_4
TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K
Rdson=13mOhm
L(ripple current)
=(19-1)*1/(1u*272k*19)
~3.646A
13m*9.5=RILIM*20uA
RILIM=6.19K
R1
R2
PR76
2.67K/F_4
PC49
33P/50V_4
NB_CORE_FB
PR77
10K/F_4
VOUT=(1+R1/R2)*0.75
PR79
*0/short_6
PR75
13K/F_4
PR70
10K/F_4
PQ8
DMN601K-7
PR66
100/J_4
PC46
0.01U/25V_4
PR69
*0/J_4
PQ7
DMN601K-7
PR68
*100K/J_4
+NB_CORE_ON <8>
HI --- 0.95V
LOW ---1.1V
Quanta Computer Inc.
PROJECT : ZH9
Size
Document Number
NB_CORE(UP6111A)
Rev
4A
Date: Sunday, March 28, 2010
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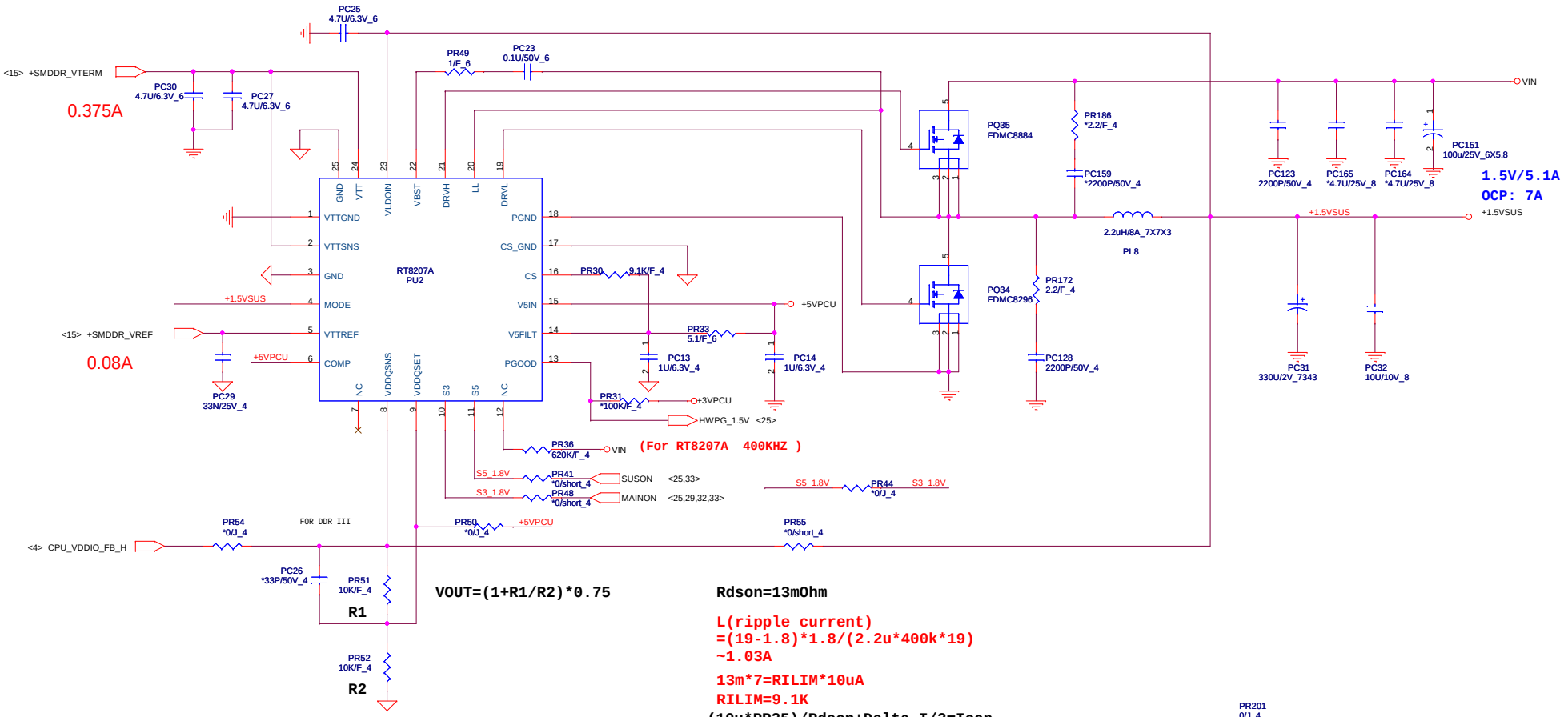
[PWM]



VOUT=(1+R1/R2)*0.75

Rdson=13mOhm

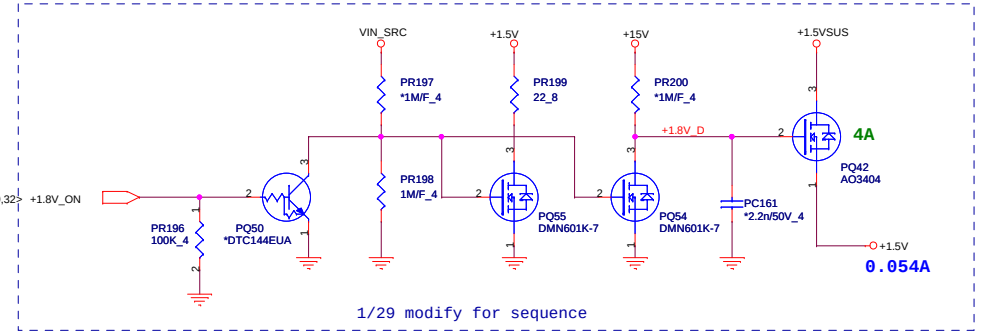
L(ripple current)
=(19-1.8)*1.8/(2.2u*400k*19)
~1.03A

13m*7=RILIM*10uA
RILIM=9.1K
(10u*PR35)/Rdson+Delta_I/2=Iocp

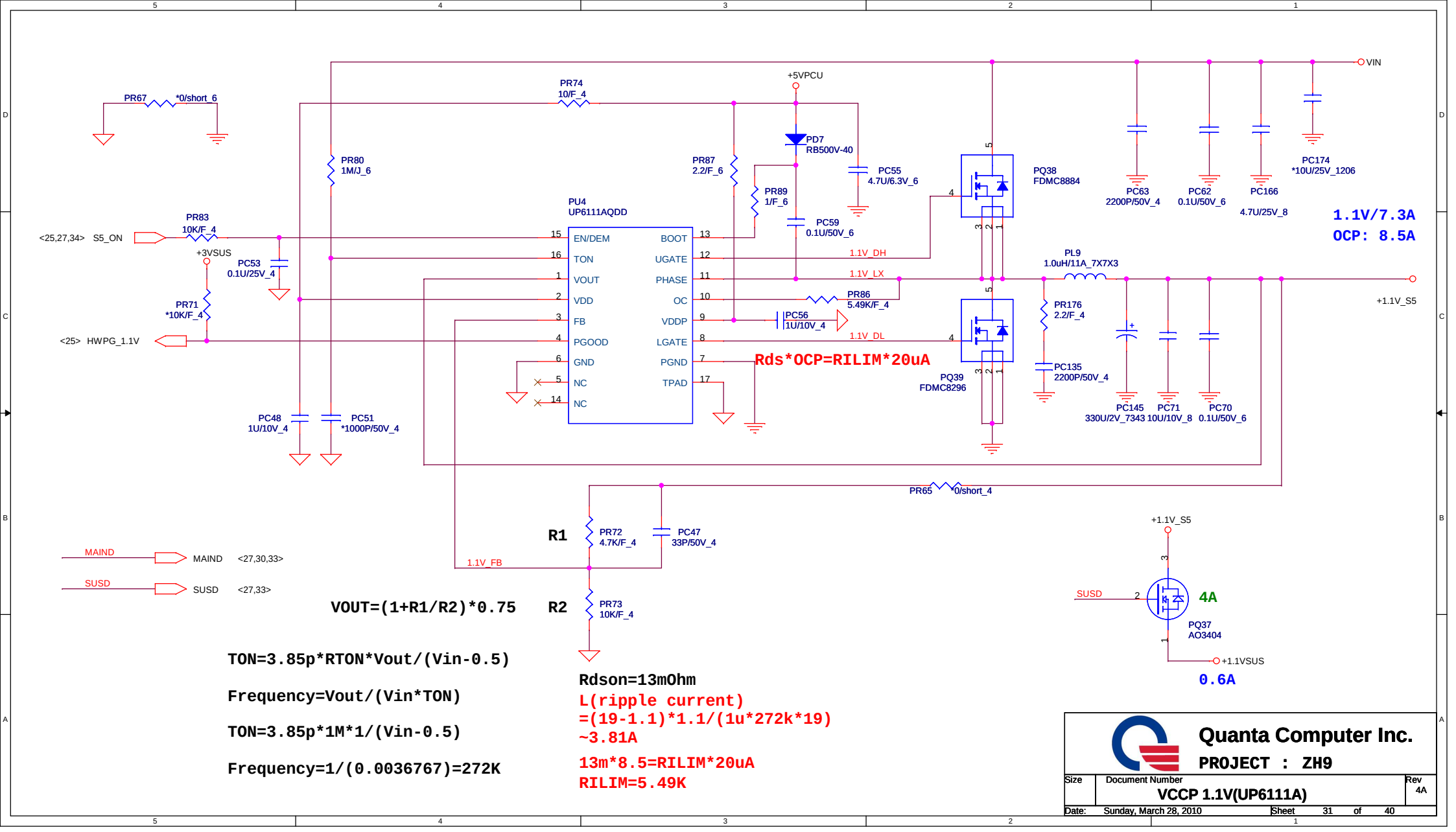
PR56 *0/short_6

MAIND MAIND <27,33>

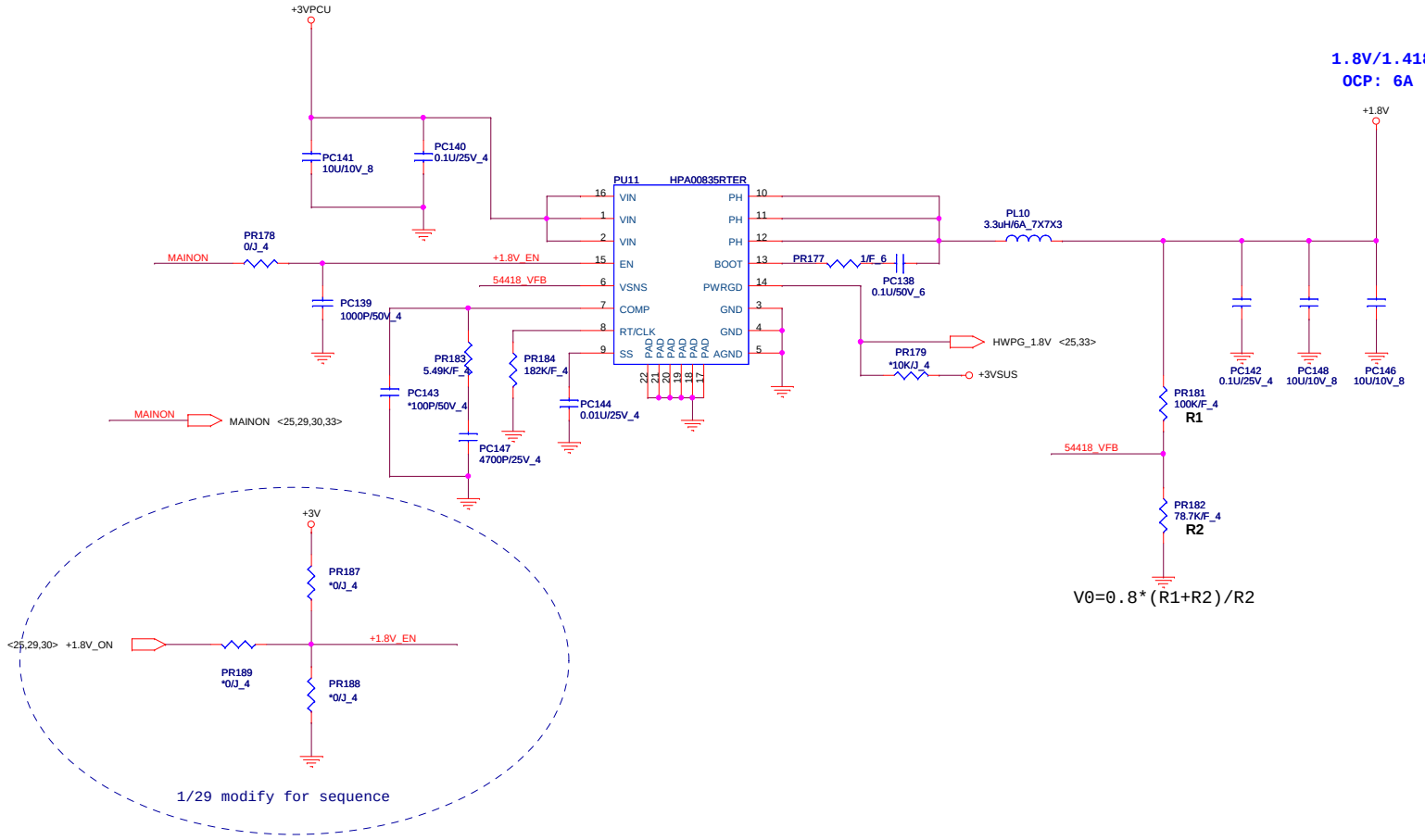
PR201 0/J_4
MAIND +1.8V_D



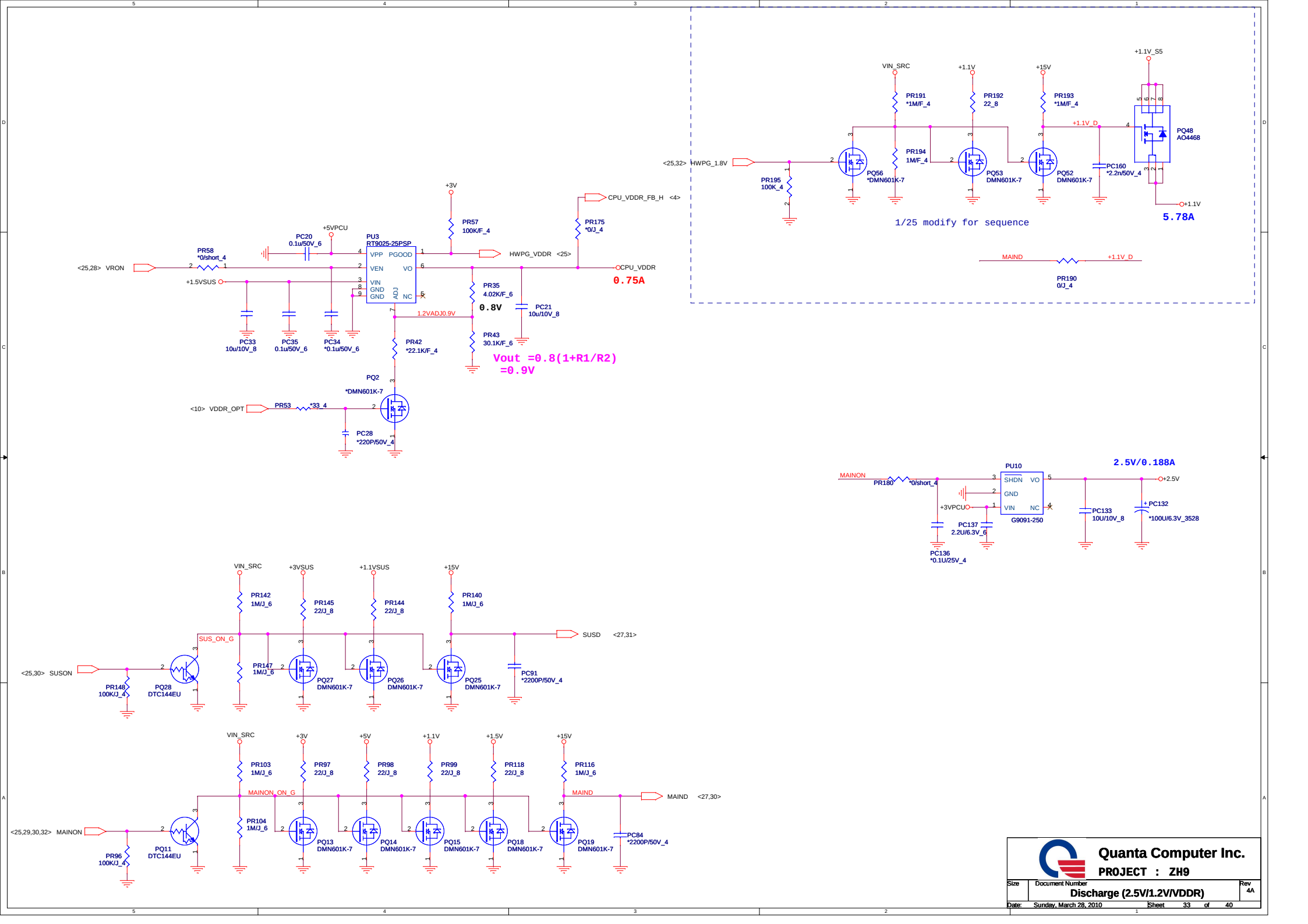
Quanta Computer Inc.			
PROJECT : ZH9			
Size	Document Number: DDR 1.5V(RT8207A)		Rev 4A
Date: Sunday, March 28, 2010		Sheet 30 of 40	



Quanta Computer Inc.		
PROJECT : ZH9		
Size	Document Number: VCCP 1.1V(UP6111A)	Rev: 4A
Date: Sunday, March 28, 2010	Sheet 31 of 40	



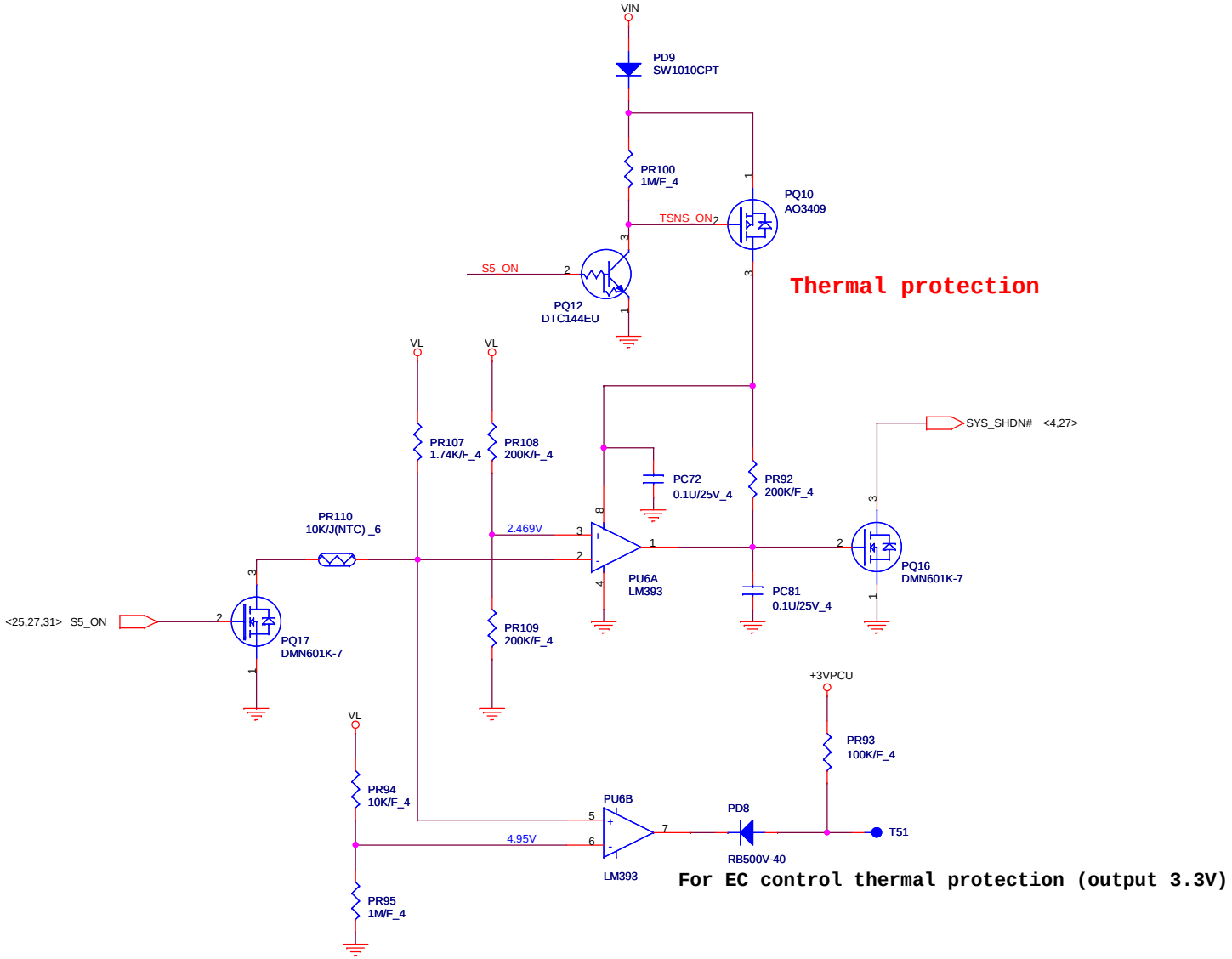
Quanta Computer Inc.		
PROJECT : ZH9		
Size	Document Number: +1.8V(TPS54418)	Rev: 4A
Date: Sunday, March 28, 2010	Sheet 32 of 40	



Quanta Computer Inc.

PROJECT : ZH9

Size	Document Number	Rev
	Discharge (2.5V/1.2V/VDDR)	4A
Date: Sunday, March 28, 2010	Sheet 33 of 40	



Quanta Computer Inc.

PROJECT : ZH9

Size	Document Number	Rev
	Thermal protect	4A
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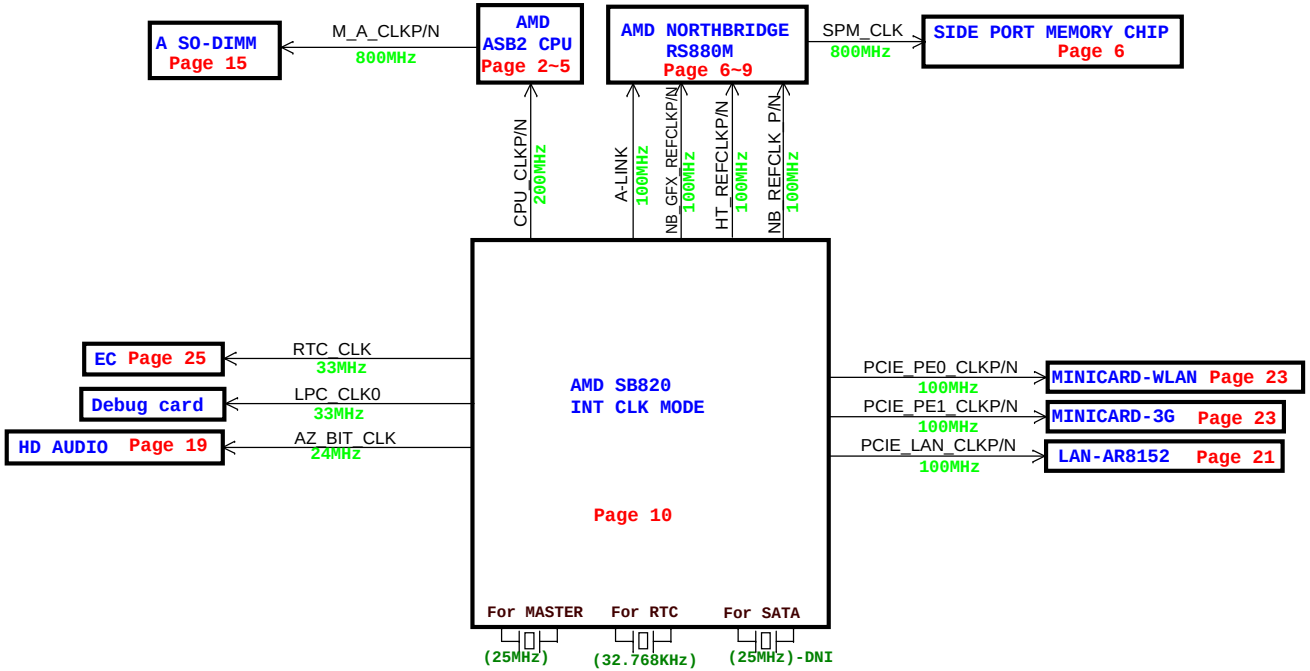
INTERNAL CLOCK MODE



Quanta Computer Inc.

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Size	Document Number	Rev
	Clock Distribution Diagram	4A

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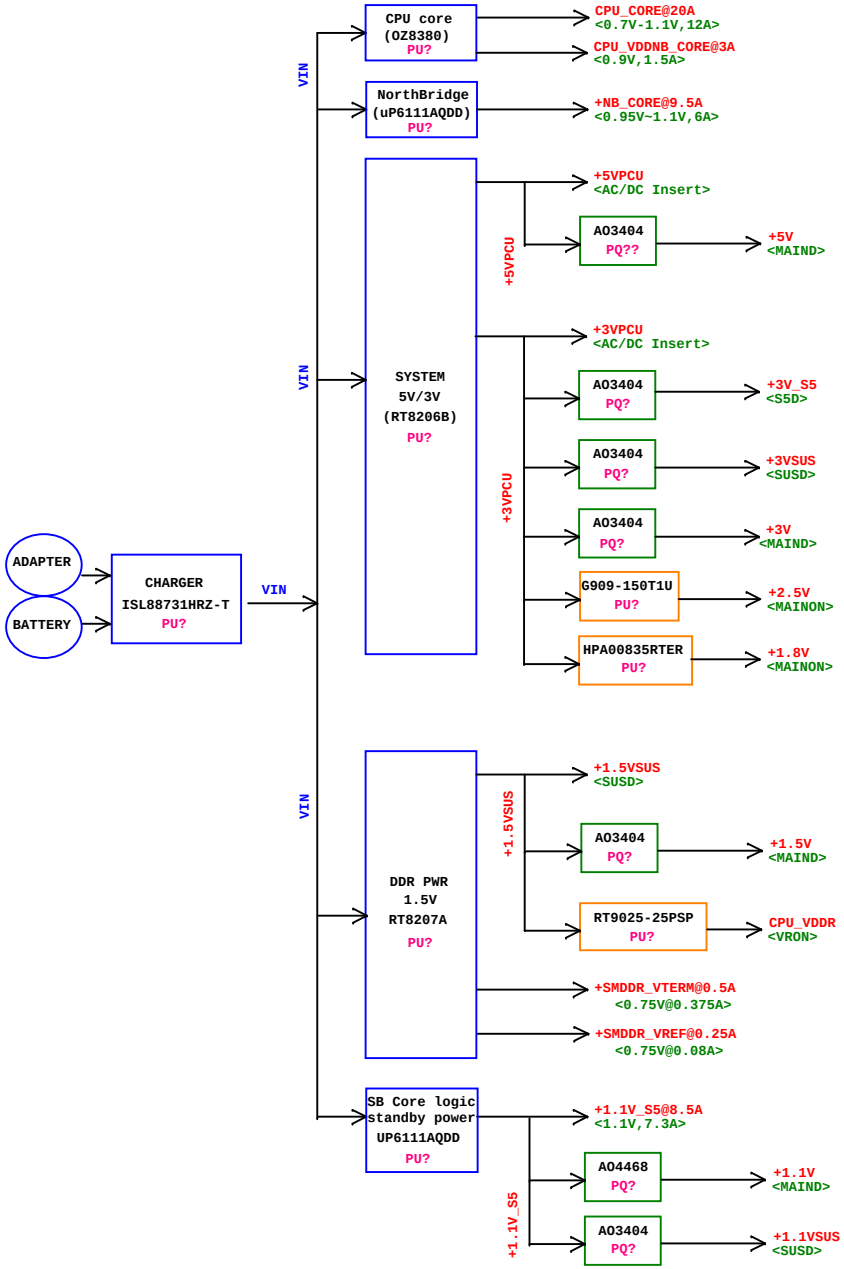


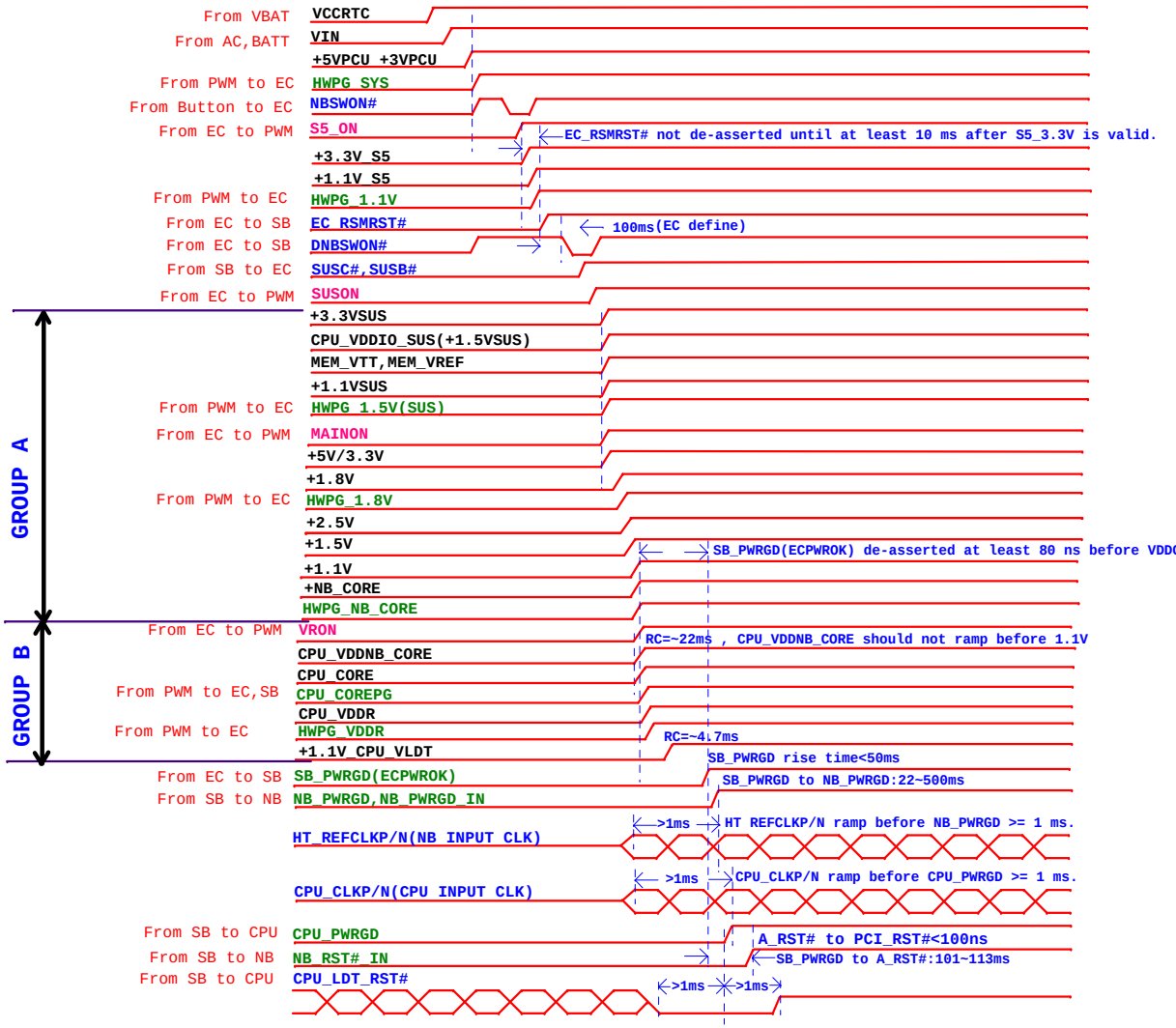
POWER	Distribution
VIN	LCD Backlight, CPU_CORE,NB_CORE, +5VPCU, +3VPCU, +1.5VSUS, +1.1V_S5
CPU_CORE	CPU
CPU_VDDNB_CORE	power supply for on-die NorthBridge
NB_CORE	NorthBridge power supply
+5VPCU	USB Connecter
+5V	CRT,Touch Pad ,Audio codec,SATA
+1.8V	NB & SB power supply
+3VPCU	RTC, Hall Sensor, System LED, EC, BIOS, Acer ID EEPROM, +3V_S5, +3VSUS, +3V
+3V_S5	SouthBridge,LAN , LAN EEPROM , RJ45 LED
+3VSUS	3G
+3V	CLK_GEN, CPU, NB,SB, LCD power switch,CCD, DMIC, BT, System LED, Codec, WLAN/Wimax, Card reader, EC
+2.5V	CPU,Discharge
+1.5VSUS	CPU,DDR,Discharge
+1.5V	CPU,DDR,NB
+SMDDR_VTERM	DDR
+SMDDR_VREF	CPU, DDR
+1.1V_S5	NorthBridge,Discharge
+1.1VSUS	Southbridge
+1.1V	CLK_GEN,CPU,NB,SB
CPU_VDDR	CPU

BOM Structure	
Fun.	Description
SPM@	w/ Sideport RAM
3G@	w/ 3G module
BT@	w/ BT module
HDM@	w/ HDMI
BOM@	BOM Control

BOM@		
Function		Description
CPU	CPU V105	U16: AJ00105VT00
	CPU K125	U16: AJ0K125VT02
	CPU K325	U16: AJ0K325VT02
	CPU K625	U16: AJ0K625VT03
w/ Sideport	w/ Sideport	L45,L46: Stuff(CX8PG221003) R142: Non-stuff C214: Stuff(CH4102K1B03) C416: Stuff(CH5102K9B06) Check U7,R295,R296,R283,R284
	w/ SAM Sideport	U7: AKD5LGGT506 ; R295,R284: Stuff ; R296,R283: Non-stuff
	w/ Hynix Sideport	U7: AKD5LZGTW04 ; R295,R283: Stuff ; R296,R284: Non-stuff
	w/ ATI Sideport	U7: AKD5LGGT700 ; R296,R284: Stuff ; R295,R283: Non-stuff
w/o Sideport	w/o Sideport	L45,L46: CS00003J951(0ohm) R142: Stuff(CS23002JB13) C214,C416: CS00002JB38(0ohm) U7,R295,R296,R283,R284: Non-stuff

Quanta Computer Inc.
PROJECT : ZH9
Size | Document Number: Power Tree | Rev: 4A
Date: Sunday, March 28, 2010 | Sheet 36 of 40

Nile Power On Sequence



Power on sequence required:

SB820:

1. EC_RSMRST# ramp up time (10% to 90%) <= 50 ms
2. SB_PWRGD(ECPWROK) rise time <= 50 ms
3. SB_PWRGD(ECPWROK) fail time <= 1 ms
4. SB_PWRGD(ECPWROK) de-asserted at least 1 ns before EC_RSMRST# is asserted when entering G3 state.
5. VBAT will be valid at least 5 seconds before S5_3.3V and S5_1.1V are ramped up to allow start time for internal RTC.
6. 50us<=all power rails rise time except +3.3V_S5<=40ms
7. 100us<=+3.3V_S5 rise time<=40ms
8. +1.8V_S0 rails cannot ramp before the +3.3V_S0 rails.
9. +1.1V_S0 rails cannot ramp before the +1.8V_S0 rails.
10. +1.1V_S0 rails cannot ramp before the +3.3V_S0 rails.
11. +1.1V_S5 rails cannot ramp before the +3.3V_S5 rails.
12. +3V_S5 ramp down time > 300 µs.

RS880:

1. +1.1V valid before NB_PWRGD HIGH >= 1 ms
2. +1.8V_NB_IOPLLVDD18c(+1.8V) cannot ramp before the 3.3-V rails
3. +1.5V_SPM_VDDQ(+1.5V)cannot ramp before the 3.3-V rails
4. +1.8V_NB_VDDLTP18(+1.8V)cannot ramp before the 3.3-V rails
5. +1.8V_NB_PLLVDD18(1.8V)cannot ramp before the 3.3-V rails
6. 3.3-V rails cannot exceed the 1.8/1.5-V Sideport or 1.8-V Display and PLL rails by > 2.1 V.
7. IOPLLVDD/PLLVDD(+1.1V) cannot ramp up before the 1.8/1.5-V Sideport or 1.8-V Display and PLL rails.
8. VDDC(+NB_CORE) rail cannot ramp before the 1.1-V PLL rails.

Notice:

1. CPU_LDT_RST# msut be asserted a minimum of 1ms prior to the assertion of CPU_PWRGD
2. CPU_CLKP/N must be within specification a minimum of 1ms prior to the assertion of CPU_PWRGD
3. CPU_PWRGD remains deasserted at least 1ms after both CPU_CLKP/N and all voltages to the processor are within specification for operation
4. all NB power rails(1.8V/1.2V/1.1V) valid before NB_PWRGD at least 1ms
5. stable input clocks from CLKGEN(HT_REFCLKP/N) to NB before NB_PWRGD at least 1ms

SB SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN)
(SB_DA0)/(SB_CL0) (+3V)	V	V	V
Power Plane	+3V	+3V	+3V
MOS CKT (Level shift)	X	X	X*

*Reserve: There is not SMBUS function in AVL

EC SMBUS Table

	Battery	CPU thermal Sensor
EC775 SDA1 / SCL1 (+3VPCU)	V	
EC775 SDA2 / SCL2 (+3V)		V
EC775 SDA3 / SCL3 ()		
Power Plane	+3VPCU	+3V
MOS CKT (Level shift)	X	X

Quanta Computer Inc.
PROJECT : ZH9
Size | Document Number | Rev 4A
POWER SEQUENCE
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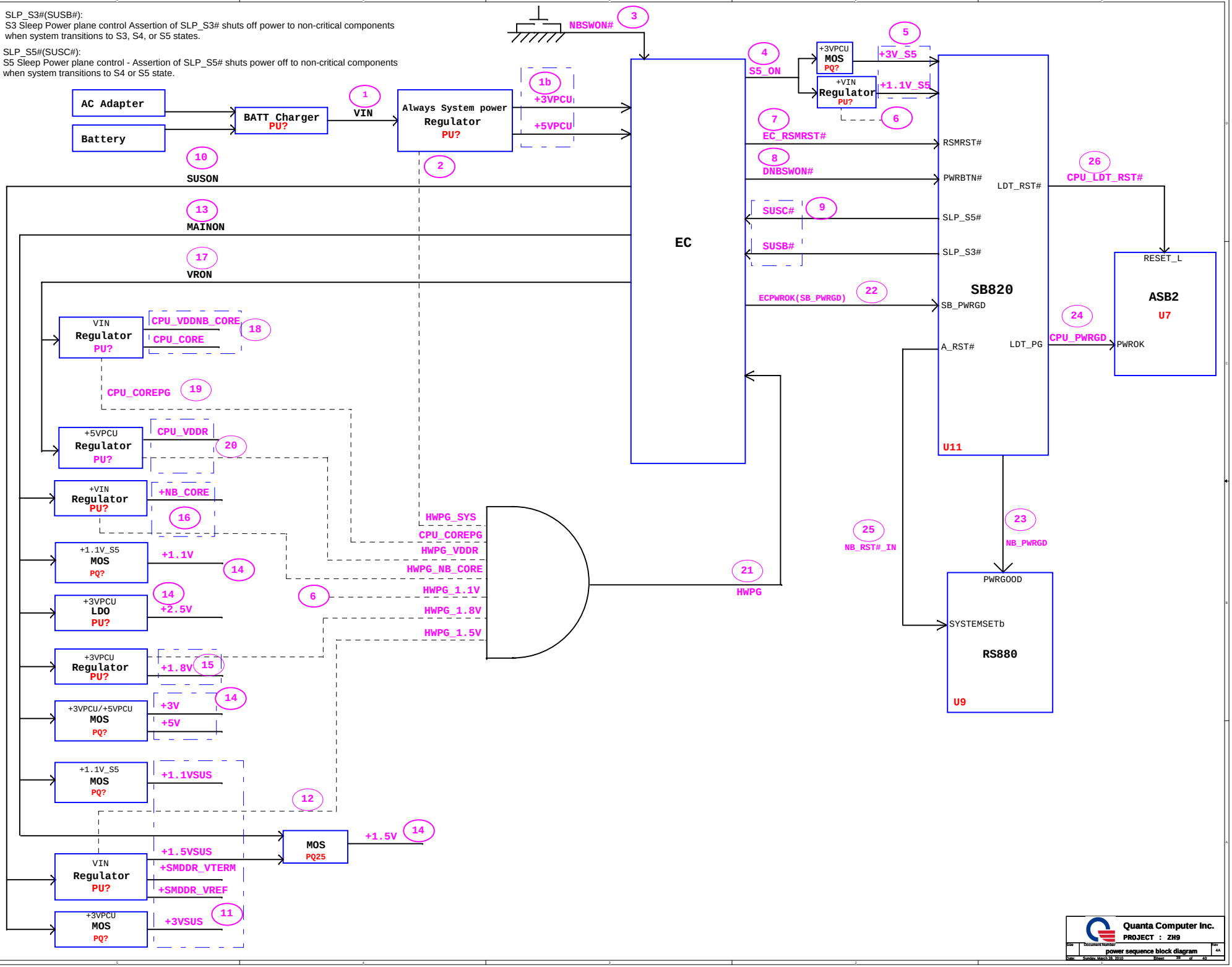
SLP_S3#(SUSB#):
S3 Sleep Power plane control Assertion of SLP_S3# shuts off power to non-critical components when system transitions to S3, S4, or S5 states.

SLP_S5#(SUSC#):
S5 Sleep Power plane control - Assertion of SLP_S5# shuts power off to non-critical components when system transitions to S4 or S5 state.



Quanta Computer Inc.
PROJECT : ZH9
power sequence block diagram