

PCB DAZ0I200101

MB
USB IO/B
HDD/B
LED/B
TP/B

DA60000KP10
DA60000KQ10
DA400011R10
DA400011T10
DA400013910

Compal Confidential

P1VE6 LA7071P Schematics Document

AMD Ontario Processor with DDRIII + Hudson M1

11.6" M/B

2011-03-17

Rev : 1.0

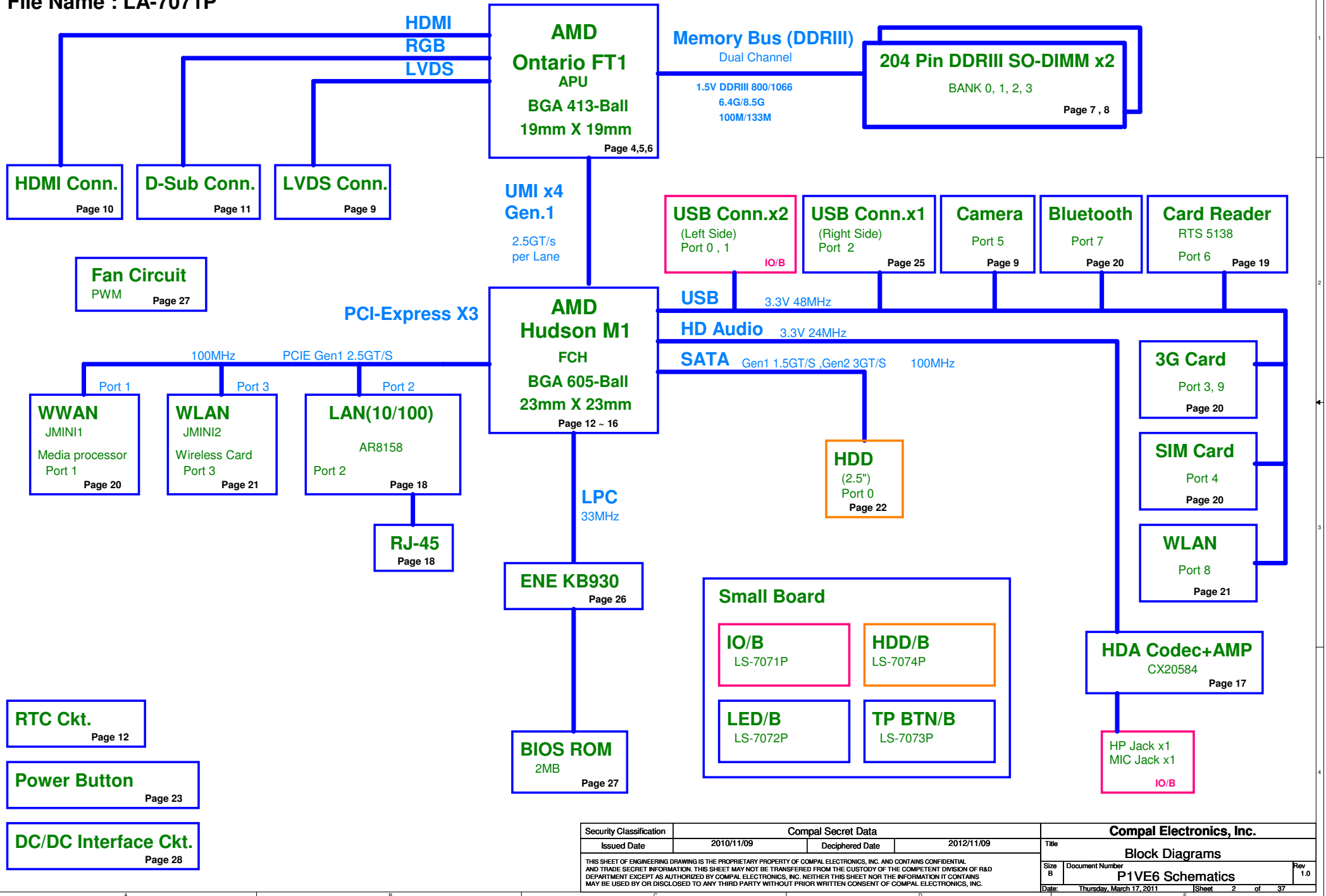
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Model Name : P1VE6

File Name : LA-7071P

Brazos Platform



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCBATT	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	16H	SB-TSI	1001-100xb	98H

SM Bus Controller 0		
	(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)	
Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1		
	(FCH_SMB0)	
Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90

BOM Structure

HDMI@ : HDMI function
BT@ : BT function
CONN@ : Conneters
45@ : 45 Level
3G@ : 3G function
N3G@ : None 3G function
CMBS@ : Combo Jack POPO noise Solution
NCMBS@: None Combo Jack POPO noise Solution

FCH Hudson-M1 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Left conn
Port1	Left conn
Port2	Right conn
Port3	WWAN
Port4	SIM
Port5	USB Camera
Port6	CardReader
Port7	BT
Port8	WiMax
Port9	WWAN
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List		
APU	PCIE0	NC
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	NC
	PCIE1	WWAN
	PCIE2	LAN
	PCIE3	WLAN

FCH Hudson-M1 SATA Port List	
SATA0	HDD
SATA1	NC
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

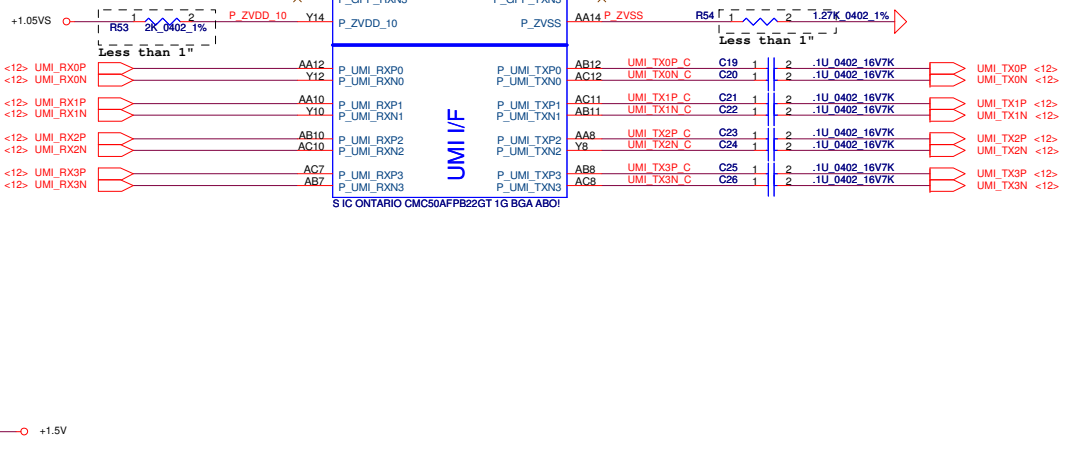
Board ID / SKU ID Table for AD channel

Vcc	+3VALW				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	PCB Revision
0	0	0 V	0 V	0 V	0.1
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	0.2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

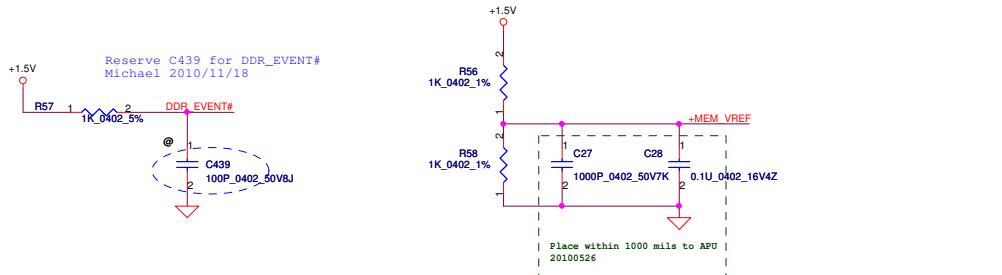
SMBUS Control Table

	Source	BATT	DIMM	MINI Card	LCD DDC ROM	HDMI DDC ROM	APU
EC_SMB_CK1 EC_SMB_DA1	KB930	V					
EC_SMB_CK2 EC_SMB_DA2	KB930						V
HDMI_DATA HDMI_CLK	APU FT1					V	
EDID_DATA EDID_CLK	APU FT1				V		
FCH_SMDAT0 FCH_SMCLK0	FCH M1		V	V			

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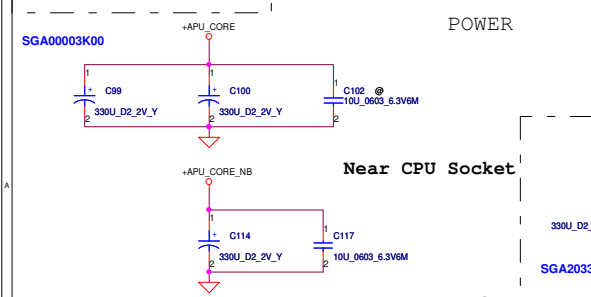
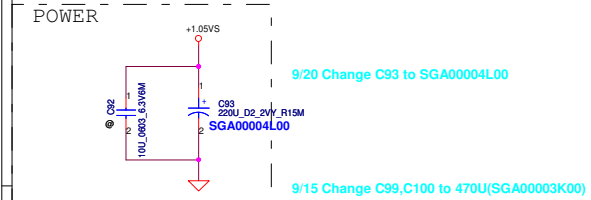
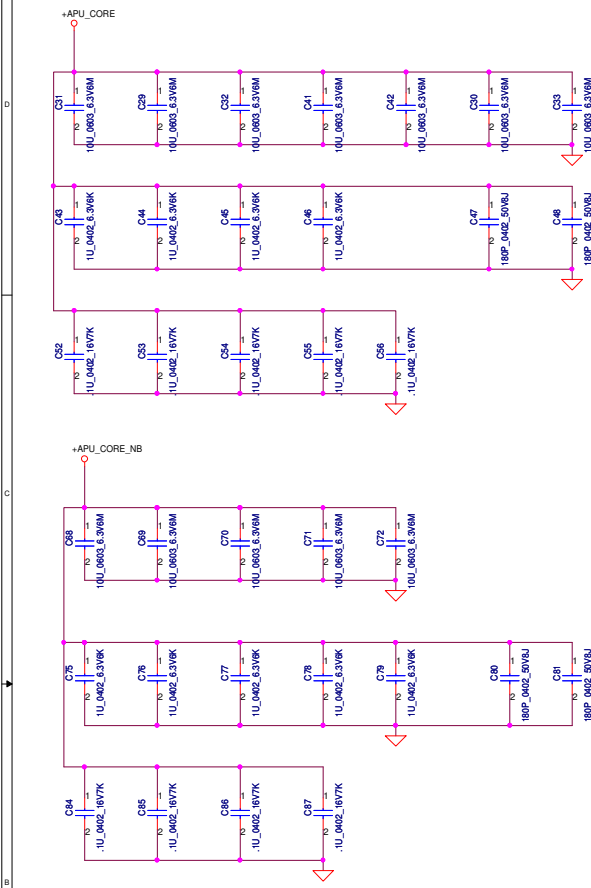


9/15 Change PCI-E from APU to FCH



Place within 1000 miles to APO
20100526

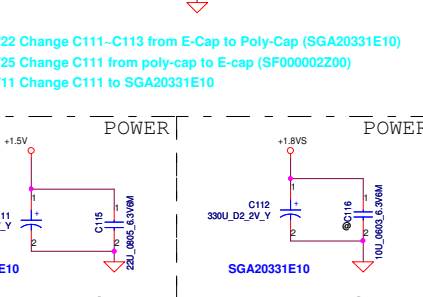
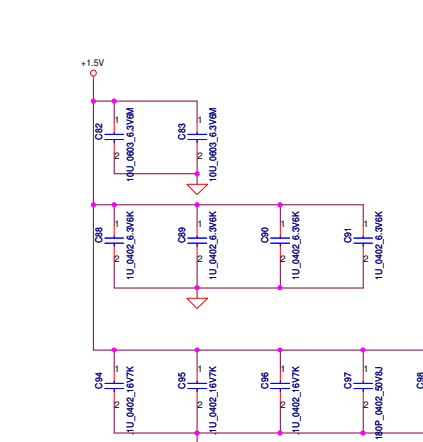
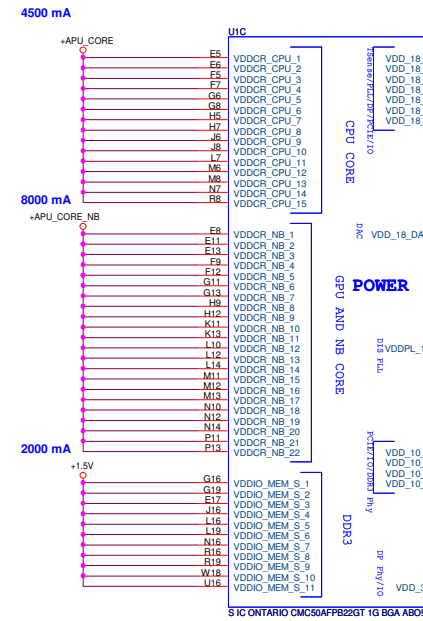
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SGA00003K00

SGA20331E10

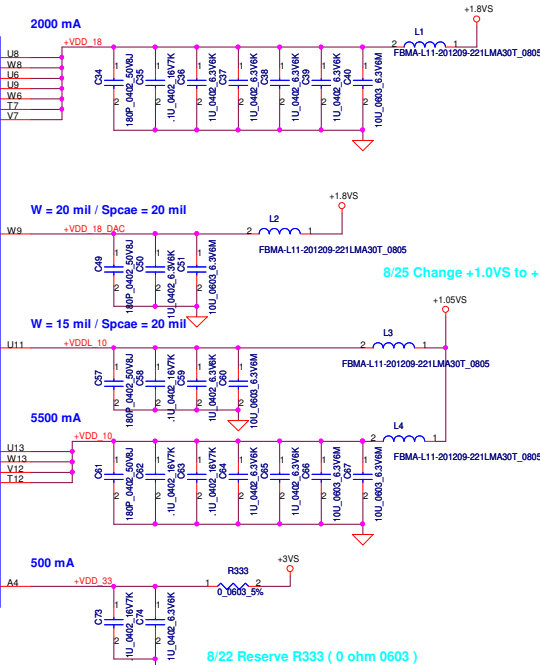
change C99,C100 from 470U to 330U , 2011/01/28 Tock
change C99,C100 footprint from C_D2 to C_X for placement



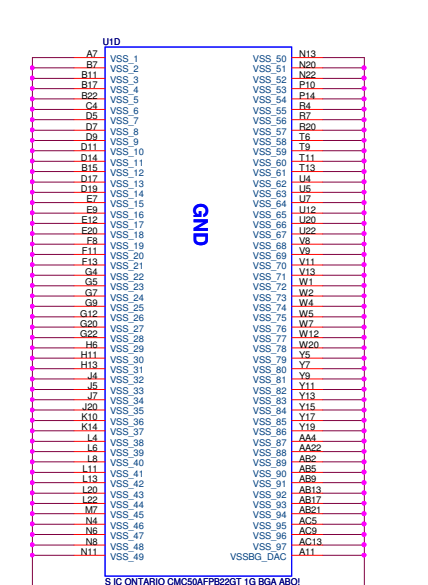
SGA00003K00

SGA20331E10

change C99,C100 from 470U to 330U , 2011/01/28 Tock
change C99,C100 footprint from C_D2 to C_X for placement



8/22 Reserve R333 (0 ohm 0603)



8/25 Change +1.0VS to +1.05VS

8/22 Reserve R333 (0 ohm 0603)

8/20 Change C93 to SGA00004L00

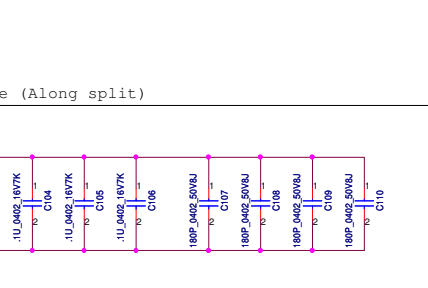
9/15 Change C99,C100 to 470U(SGA00003K00)

8/22 Change C111~C113 from E-Cap to Poly-Cap (SGA20331E10)

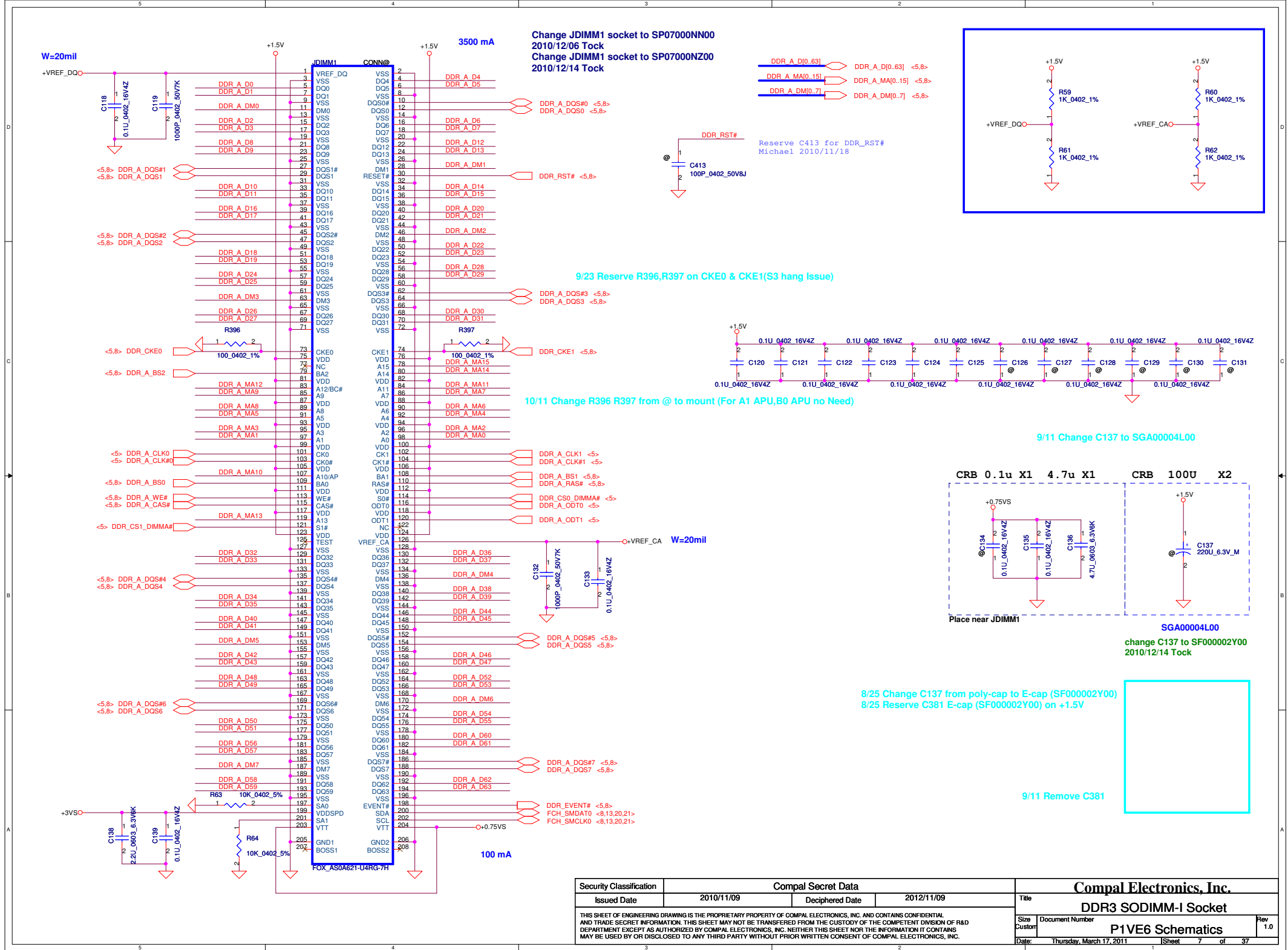
8/25 Change C111 from poly-cap to E-cap (SF000002200)

9/11 Change C111 to SGA20331E10

By case (Along split)



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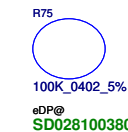


11/02 Change Q3 PN to SB934130020
2011/02/11 Change Q3 PN to SB000006R10



Connect DMIC_CLK,
DMIC_DATA
to JLVD51 pin 5 and 6
Michael 2010/11/18

8/25 JLVDS1.5 change to INT_MIC0 JLVDS1.6 change to GNDA
8/31 Update JLVDS1 Pin definition Delete R74 R76
9/13 Update LVDS Pin definition, Add R74,R76
9/13 Add Net Name +3VS_DMIC 10/01 Remove R74,R76



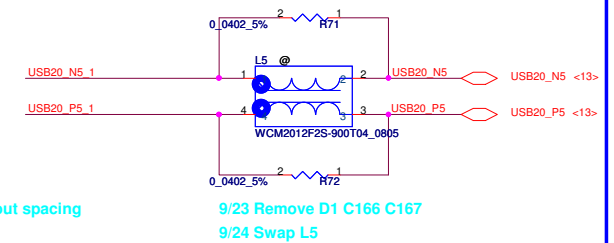
Display	LVDS	eDP
R327	0 ohm	0.1uF
R328	0 ohm	0.1uF
R381	0 ohm	0.1uF
R382	0 ohm	0.1uF
R383	@	100k ohm
R73	2.2k ohm	@
R75	2.2k ohm	100k ohm

R327 R328 R381 R382

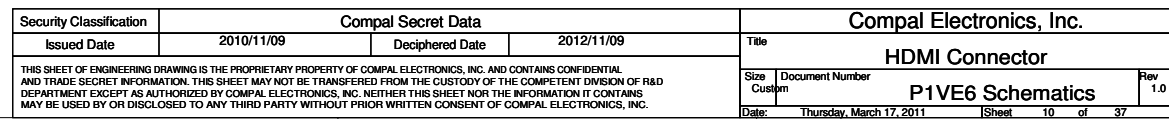
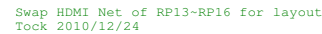
0.1U_0402_16V4Z 0.1U_0402_16V4Z 0.1U_0402_16V4Z 0.1U_0402_16V4Z

eDP@ eDP@ eDP@ eDP@

SE070104Z80

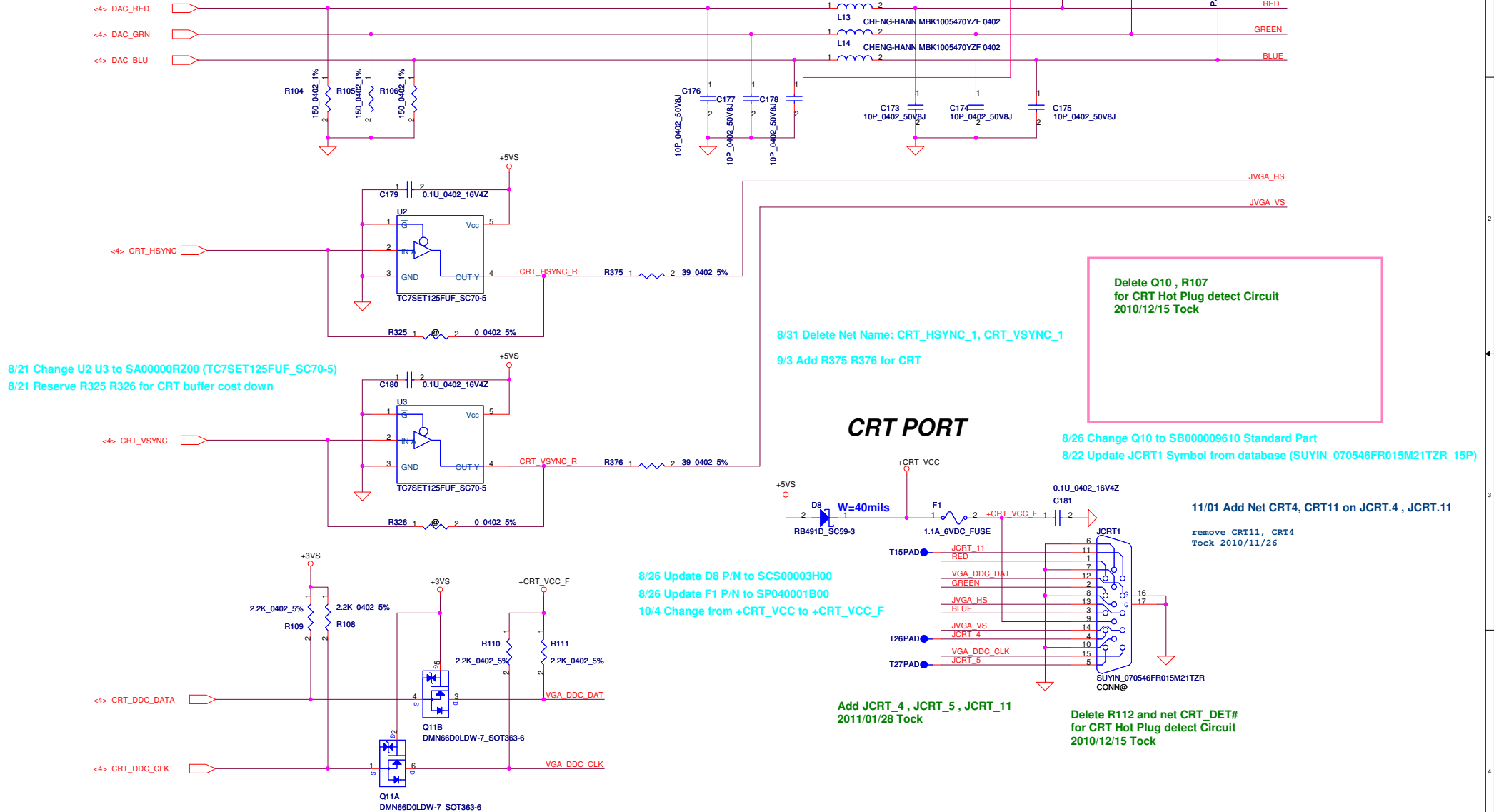


9/15 Remove D1 L5 R71 R72 C166 C167 for layout spacing
9/23 Add D1 L5 R71 R72 C166 C167 for ESD

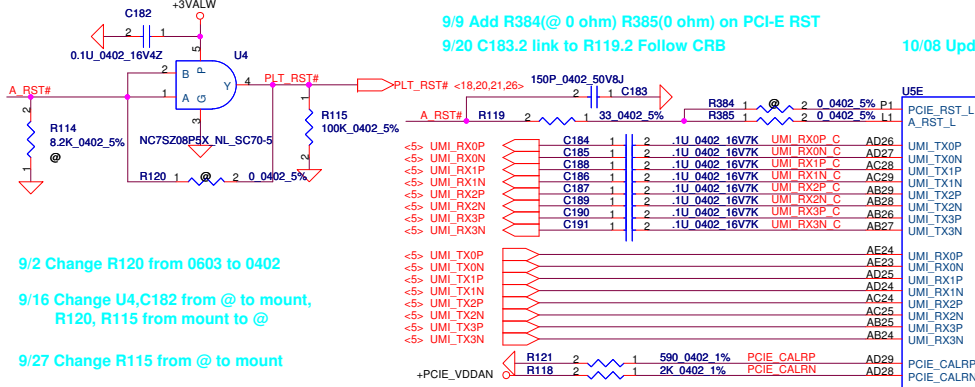


Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615

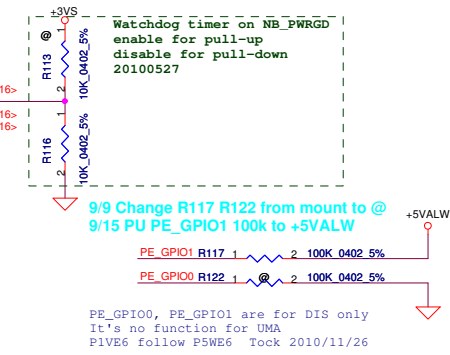
Change L12. L14, L15 to SM01000C600 2010/04/06



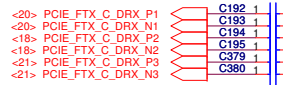
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				Deciphered Date				CRT PORT			
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10/08 Update U5 to SA000046H70 S IC 218-0792006 A13 HUDSON-M1 605P ABO!



WWAN FCH TX
LAN FCH TX
WLAN FCH TX

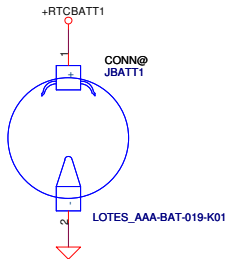


WWAN FCH RX
LAN FCH RX
WLAN FCH RX



9/6 Change PCI-E from FCH to APU
9/15 Change PCI-E from APU to FCH

8/25 Update JBATT1 Symbol (LOTES_AAA-BAT-019-K01_2P)



LAN
WLAN
WWAN

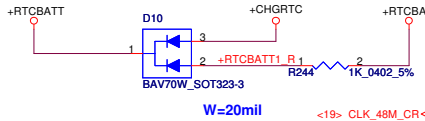


8/23 Add R348 R349 for WWAN PCIE

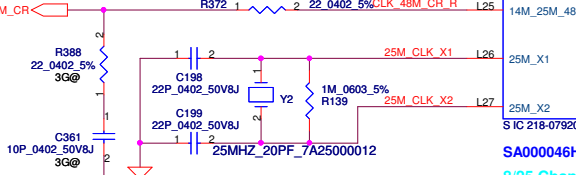
9/6 Change D10 to SC600000800 Standard Part

9/13 Add NONCHARGE@ for D10 R244

12/07 Remove BOM structure NONCHARGE@ for D10 R244 Tock



9/1 Add R372 on CLK_48M_CR
9/7 Change R372 to 22 ohm



9/13 Add Net Name +RTCBATT1_RR

9/13 Change Net Name +RTCBATT1 to +RTCBATT2

9/13 Add C392,R392,D23(CHARGE@) for RTC Charge Circuit

10/07 Change R392 from 1k to 0 ohm

10/08 Change R392 from 0 ohm to 1k ohm

11/01 Change R392 from 1k to 0 ohm

12/07 Remove R392, C392, D23 Tock

PCI EXPRESS I/F

PCI I/F

LPC

CPU

RTC

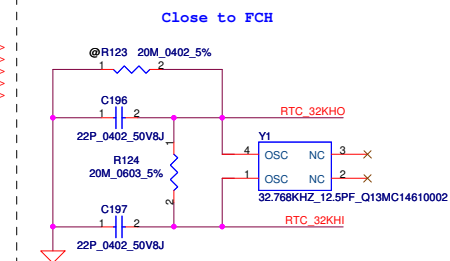
S IC 218-0792006 A13 HUDSON-M1 FCBGA 0FA

SA000046HA0

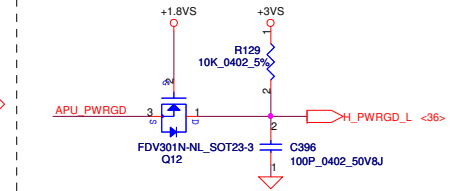
8/25 Change FCH(U5) PN to SA000046H30

11/04 Change U5 PN to SA000046HA0 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 0FA)

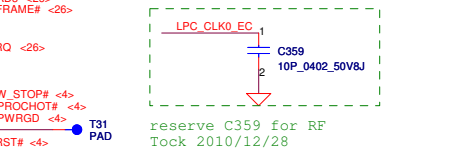
10/11 Change Y1 from SJ100006600 to SJ132P7KW10



10/05 PD 10k(R405) on CLKRUN



10/04 Add 100p(C396) on H_PWRGD_L



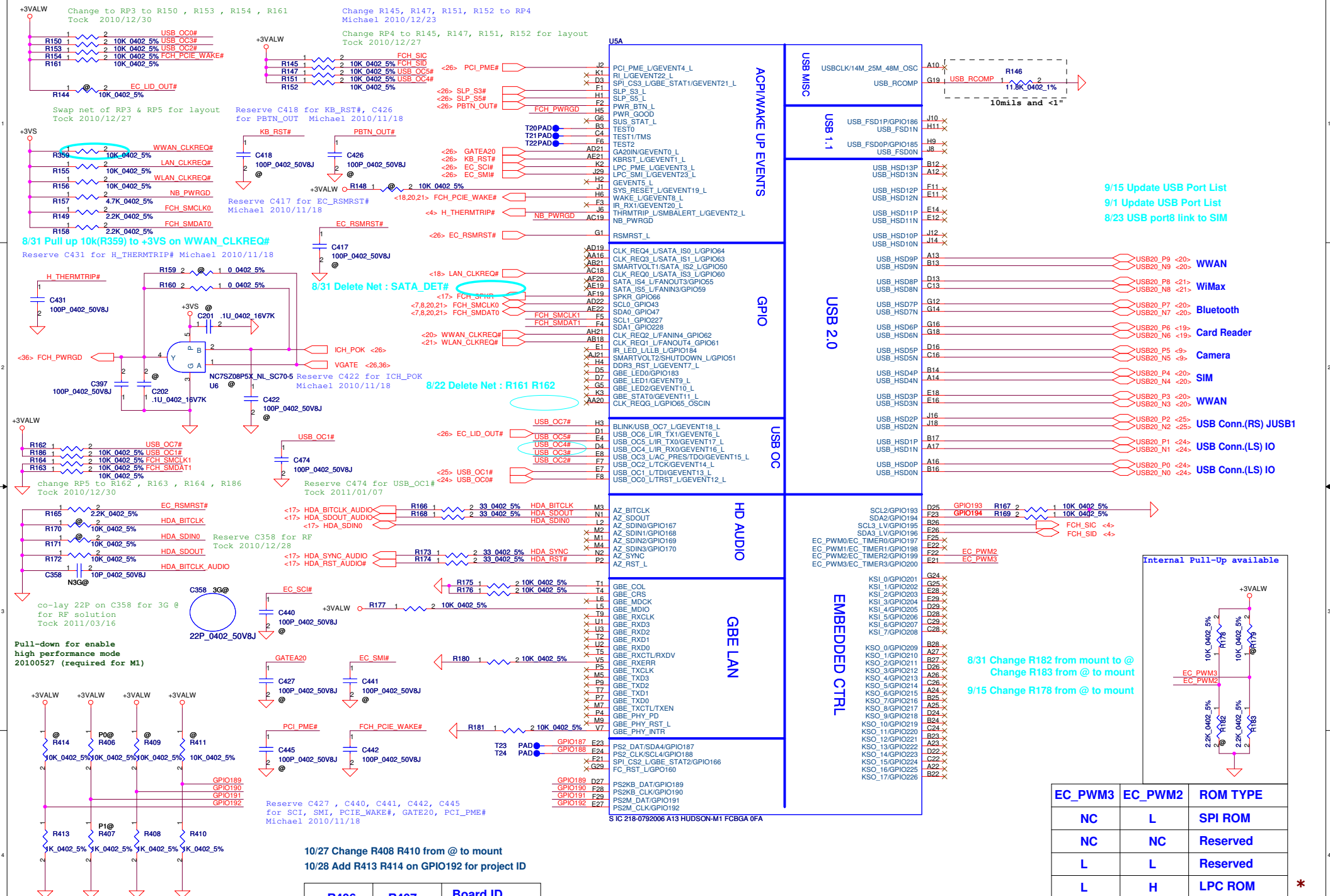
10/07 Change R140 from 560 to 1k ohm

11/01 Add Net U5_G22 on U5.G22

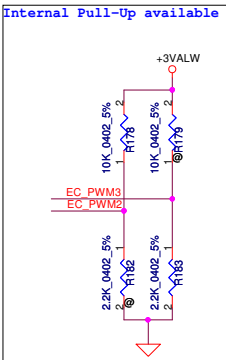


For Clear CMOS, near to RAM door

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- 9/15 Update USB Port List
 - 9/1 Update USB Port List
 - 8/23 USB port8 link to SIM
- USB20_P9 <20> WWAN
 - USB20_N9 <20>
 - USB20_P8 <21> WiMax
 - USB20_N8 <21>
 - USB20_P7 <20> Bluetooth
 - USB20_N7 <20>
 - USB20_P6 <19> Card Reader
 - USB20_N6 <19>
 - USB20_P5 <9> Camera
 - USB20_N5 <9>
 - USB20_P4 <20> SIM
 - USB20_N4 <20>
 - USB20_P3 <20> WWAN
 - USB20_N3 <20>
 - USB20_P2 <25> USB Conn.(RS) JUSB1
 - USB20_N2 <25>
 - USB20_P1 <24> USB Conn.(LS) IO
 - USB20_N1 <24>
 - USB20_P0 <24> USB Conn.(LS) IO
 - USB20_N0 <24>



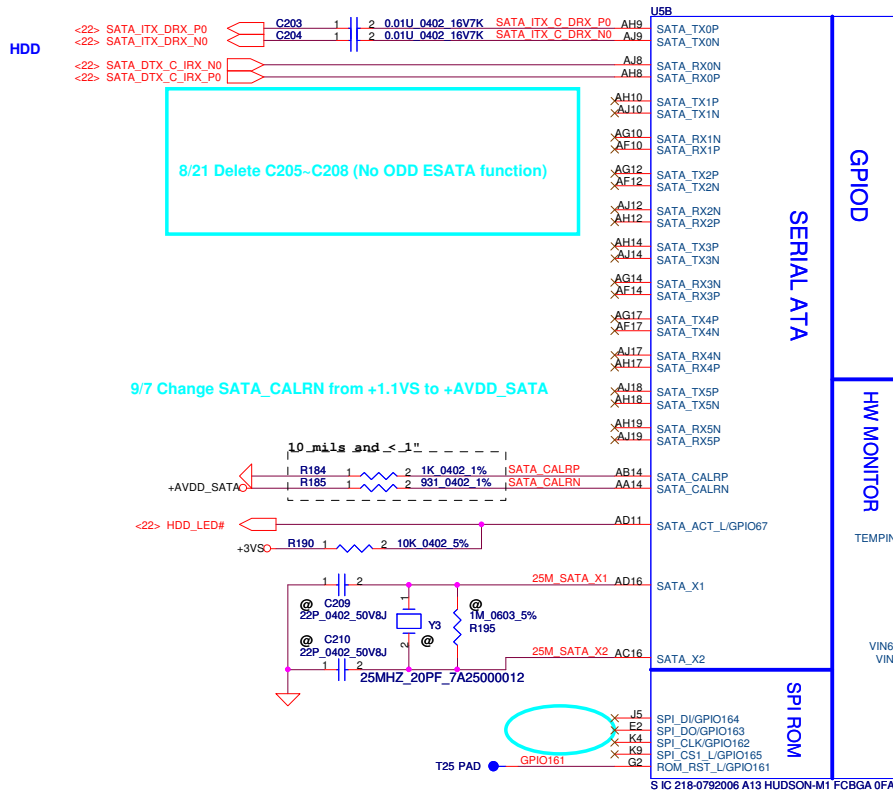
EC_PWM3	EC_PWM2	ROM TYPE
NC	L	SPI ROM
NC	NC	Reserved
L	L	Reserved
L	H	LPC ROM

change R407,R408,R410,R413 from 10K to 1K 11/26 Tock

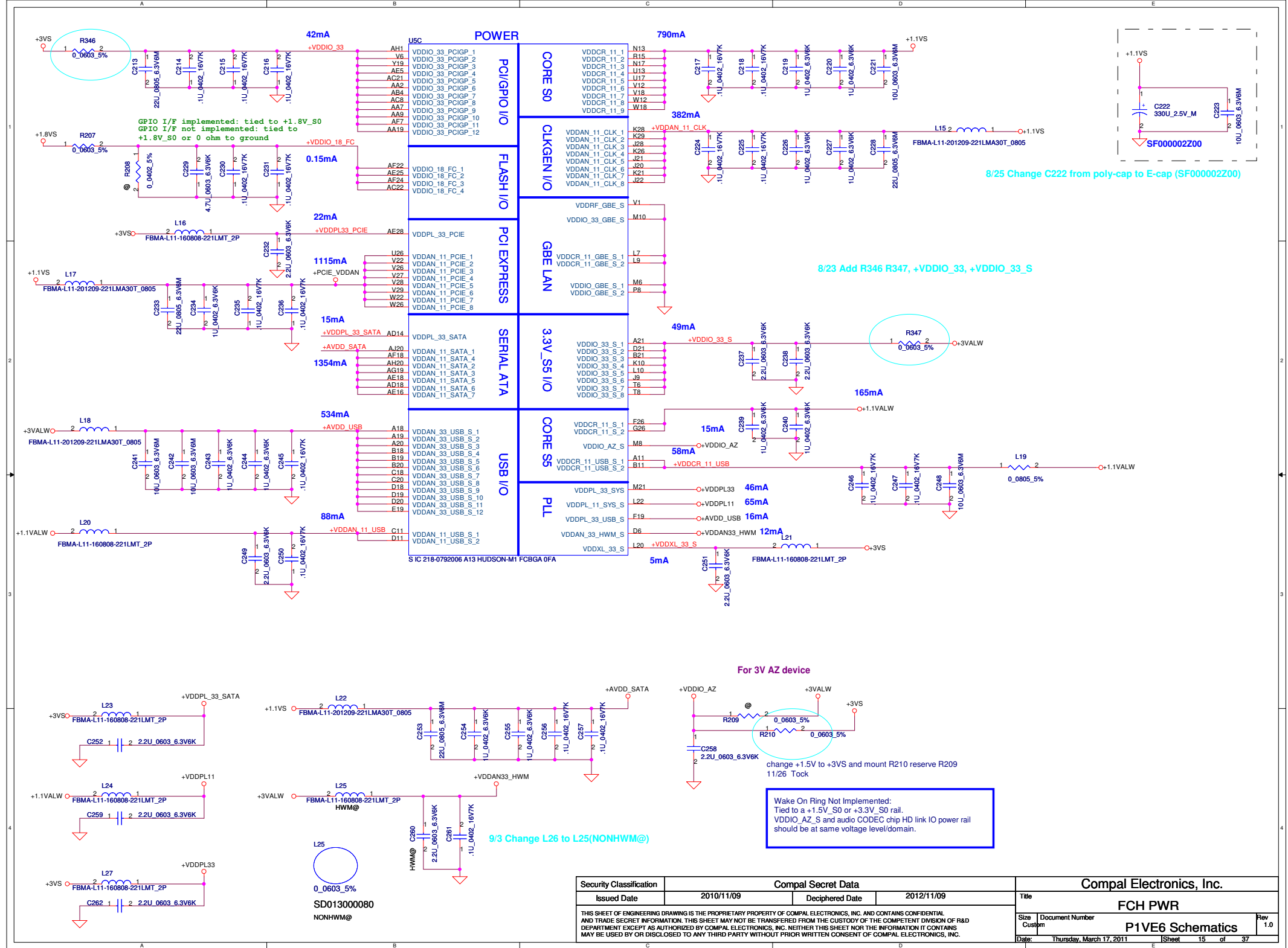
change R406 BOM to P0@ , R407 BOM to P1@ 2011/01/04 Tock

R406	R407	Board ID
mount	@	P1VE6
@	mount	P1VS6

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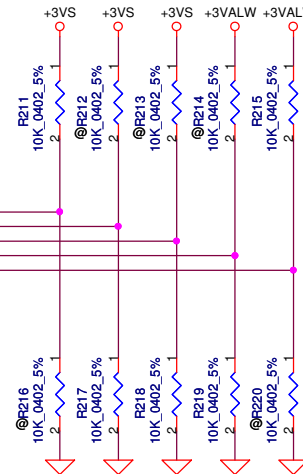


REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	CLK_PCI_DB				
PULL HIGH	ALLOW PCIE GEN2 ★	USE DEBUG STRAP	Reserved	Internal EC ENABLE	Internal CLKGEN Mode ★				
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP ★	CLKGEN Mode Internal ★	Internal EC DISABLE ★	External CLKGEN Mode				

<12> PCI_CLK1
<12> PCI_CLK3
<12> PCI_CLK4
<12> LPCCLK0
<12> CLK_PCI_DB



9/13 Change R211 from mount to @, R216 from @ to mount
9/13 Change R211 from @ to mount, R216 from mount to @

DEBUG STRAPS

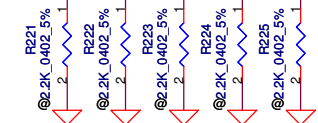
FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH	USE internal PLL generated PLL CLK ★	ILA AUTORUN Disabled ★	Selects FC PLL ★	Disable I2C ROM ★	Required Setting ★
PULL LOW	BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function

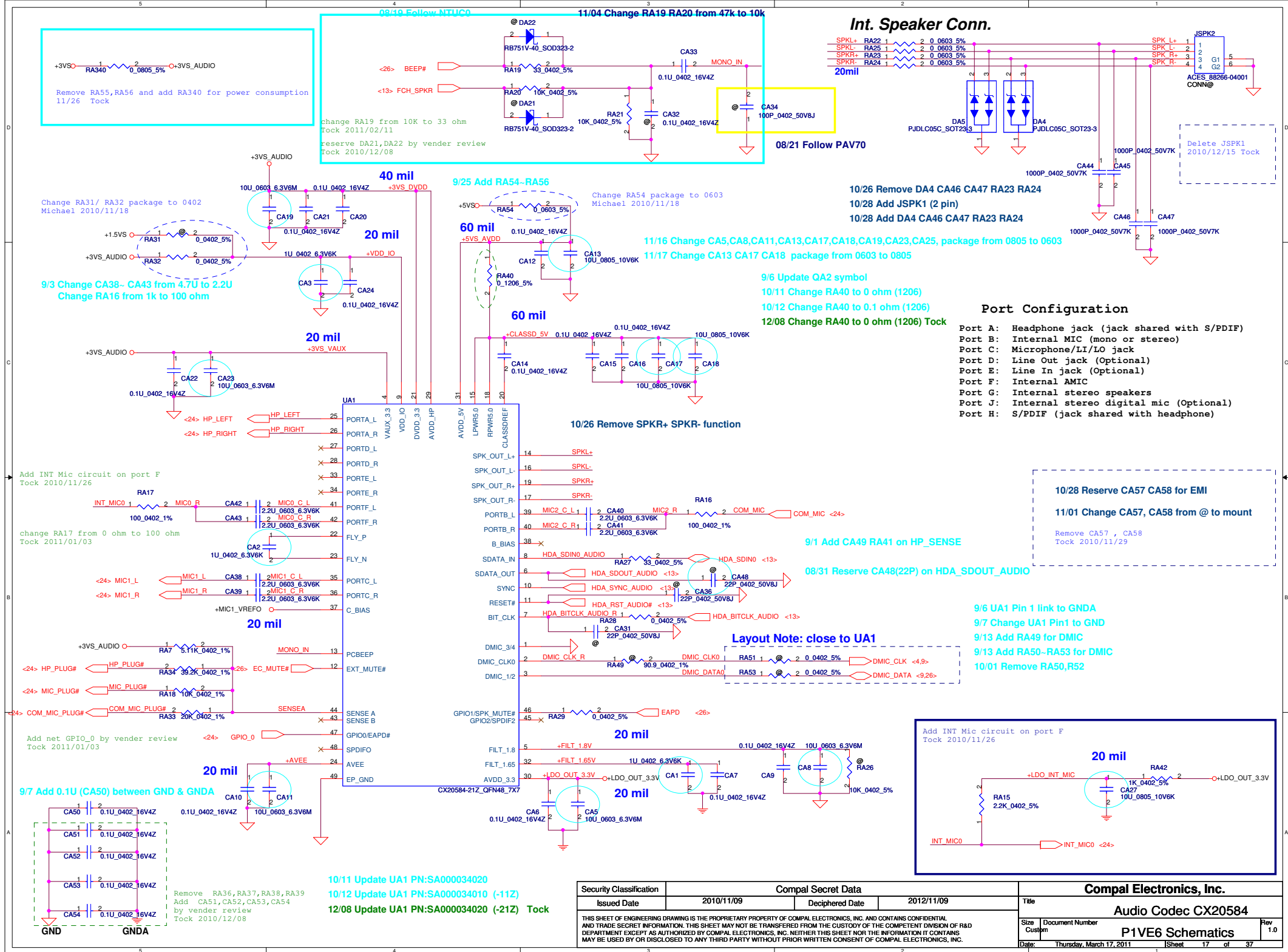
check default

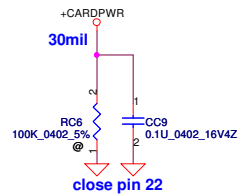
<12> PCI_AD27
<12> PCI_AD26
<12> PCI_AD25
<12> PCI_AD24
<12> PCI_AD23



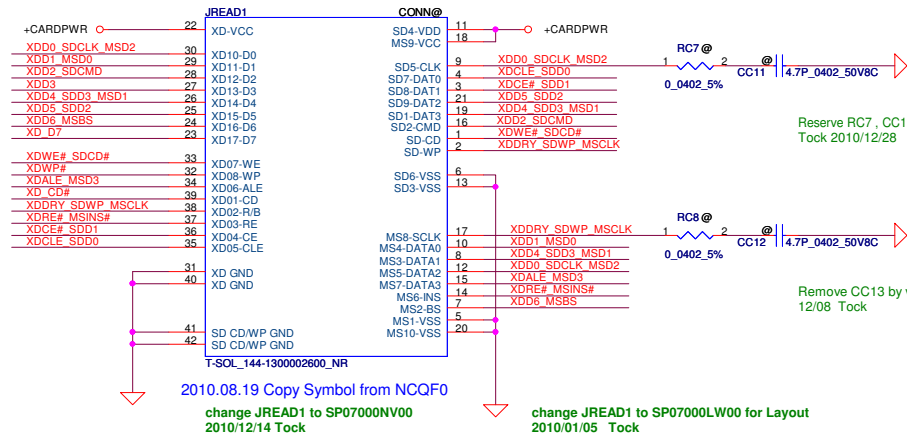
Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2010/11/09		Deciphered Date		2012/11/09		Title	
								FCH-VSS/Strap	
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Size B		Document Number		P1VE6 Schematics				Rev 1.0	
Date:		Thursday, March 17, 2011				Sheet 16 of 37			

P1VE6 Schematics

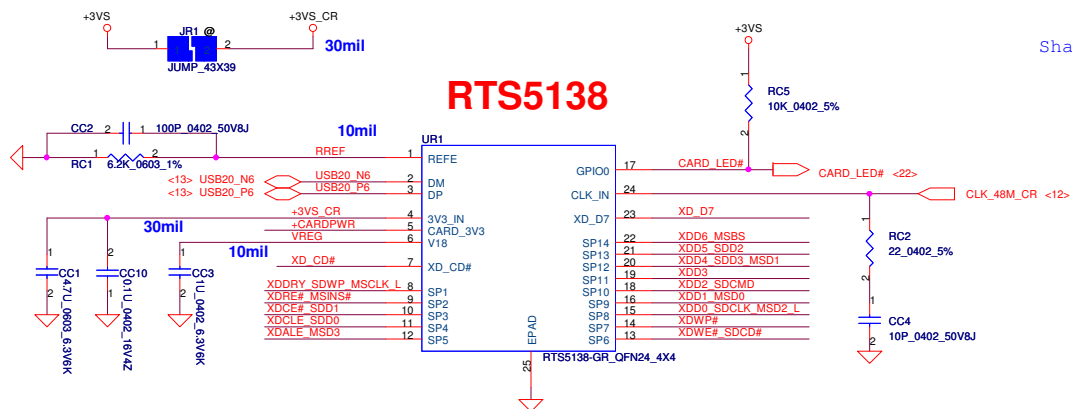




Card Reader Connector



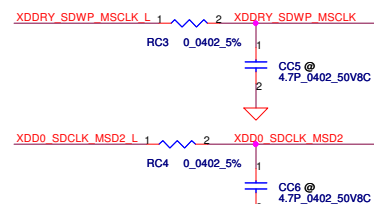
2010.11.02 Del LED circuit



Share Pin

	XD	SD	MS
	XD_CD#		
SP1	XD_RDY	SD_WP	MS_CLK
SP2	XD_RE#		MS_INS#
SP3	XD_CE#	SD_D1	
SP4	XD_CLE	SD_D0	
SP5	XD_ALE		MS_D3
SP6	XD_WE#	SD_CD#	
SP7	XD_WP		
SP8	XD_D0	SD_CLK	MS_D2
SP9	XD_D1		MS_D0
SP10	XD_D2	SD_CMD	
SP11	XD_D3		
SP12	XD_D4	SD_D3	MS_D1
SP13	XD_D5	SD_D2	
SP14	XD_D6		MS_BS
	XD_D7		

Close to chip



Add RC3, CC5, RC4, CC6 by vender review for EMI sol.
12/08 Tock
change CC5, CC6 BOM structure to @
2011/01/03 Tock

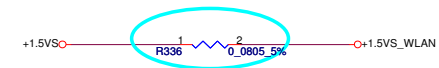
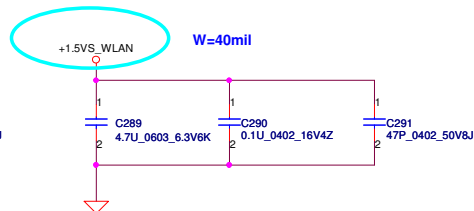
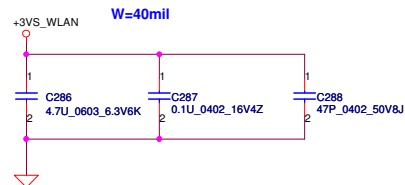
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/09	Deciphered Date	2012/11/09	Title
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<26> EC_TX_P80_DATA
<26> EC_RX_P80_CLK

Change R236, R237 to RP11
Michael 2010/12/23

Change RP11 to R253, R254
Michael 2010/12/30

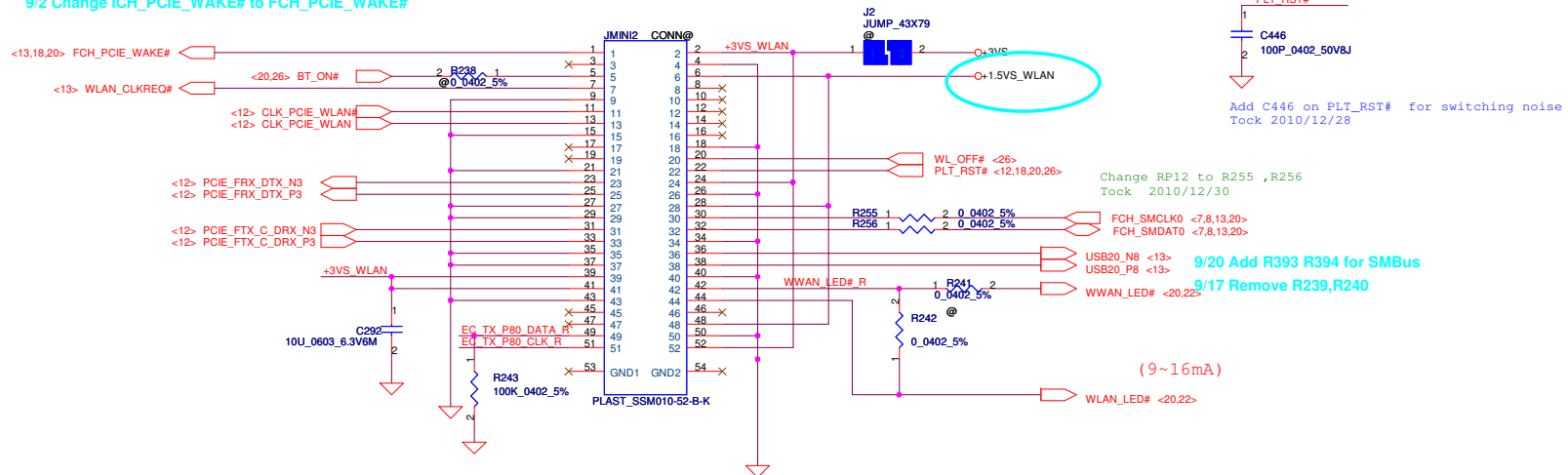
Mini-Express Card for WLAN



8/22 Reserve R336 (0 ohm 0805) Add net +1.5VS_WLAN

change JMIN2 to SP07000QC00
2010/12/14 Tock

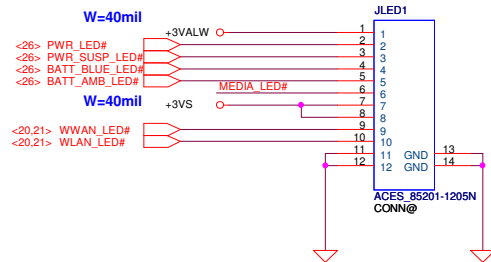
9/2 Change ICH_PCIE_WAKE# to FCH_PCIE_WAKE#



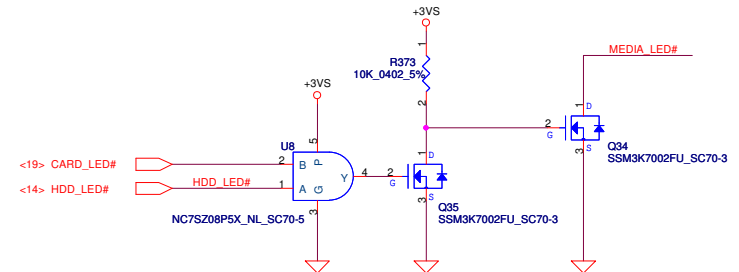
5/12 Update WLAN connector (the same as KAV60)
6/1 Revised 37、39、41、42、43 to NC
6/12 Update connector to DC040006S00
6/26 Update JMINI1 footprint
7/01 update pin 23,25,31,33

Compal Electronics, Inc.				
Title		WLAN		
Size		WLAN		
Customer	Document Number	LA-6222P		Rev 1.0
Date:	Thursday, March 17, 2011	Sheet	21	of 37

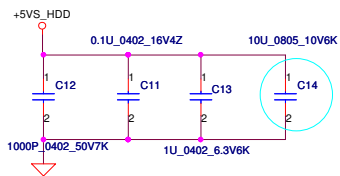
LED PCB CONN



8/22 Update JP2 Symbol from database (ACES_85201-1605N_16P)
 8/24 Update JLED1 Symbol from database (ACES_85201-1205N_12P) & Update pin definition
 9/1 Add LED Circuit (LED2~4(SC597UDB000)LED5(SC5191NB000), R360~R369, Q33)
 9/1 Change All LED power to 5V
 9/9 Change LED2~4 footprint to LED_HT-297DQ-GQ_4P
 9/11 Remove LED portion

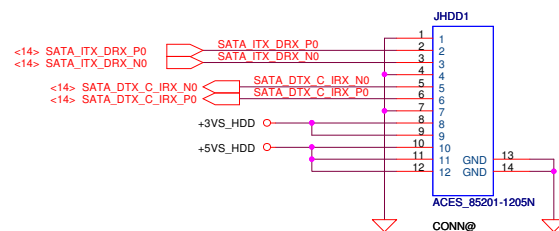
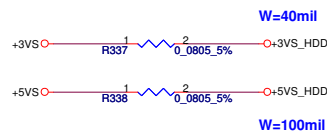


9/1 Add R373, Q34, Q35 for MEDIA_LED#



Add C11~C14 from HDD board
 2011/01/07 Tock

SATA HDD Conn.

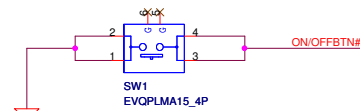


8/22 Change C298 from 10U 6.3V to 10U 10V
 8/22 Reserve R337 R338 Add net +3VS_HDD,+5VS_HDD
 9/1 Change Q33 to SB000009610(SSM3K7002FU_SC70-3)
 change JHDD1 to SP01000E400 , delete C293 ~ C298
 2010/12/14 Tock
 Modify JHDD1 pin define
 2010/12/15 Tock

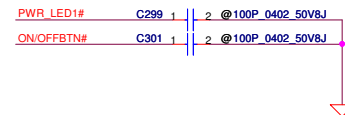
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/09	Deciphered Date	2012/11/09	Title	SATA CONN./LED/B CONN./BATT CONN.
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updated SW1 symbol for SN100002K00
2010/12/06 Tock

ON/OFF Button



FOR EMI



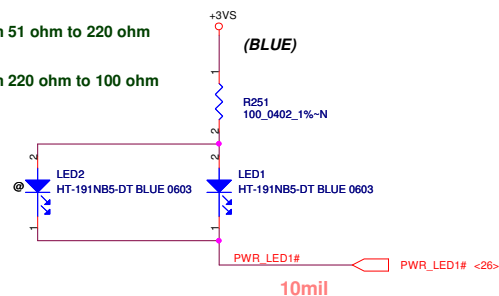
9/6 Change D13 from mount to @
10/05 Remove D13

9/1 Remove LED2 LED3 circuit, Change 70@ to mount

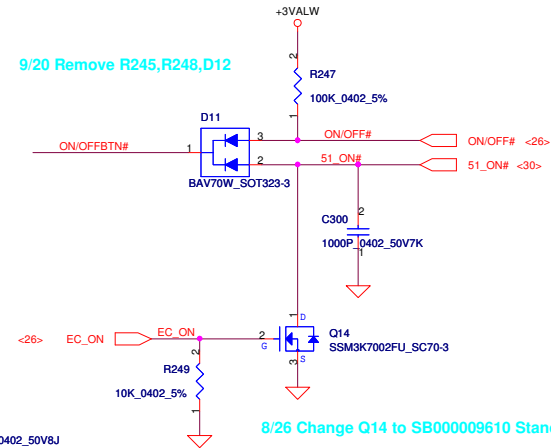
9/20 Add LED2 LED3 Circuit
9/21 Remove LED2 LED3 Circuit

change R251 from 51 ohm to 220 ohm
2011/03/07 Tock

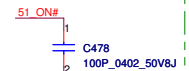
change R251 from 220 ohm to 100 ohm
2011/03/16 Tock



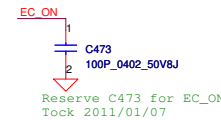
8/26 Change D11 to SC600000B00 Standard Part



place close to PR4



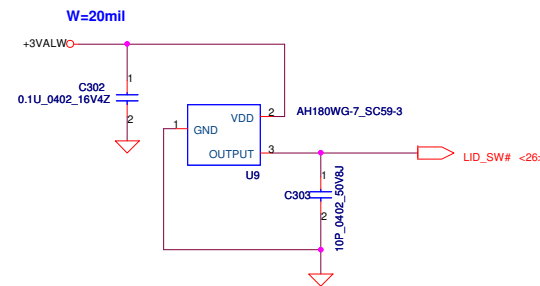
Reserve C478 for 51_ON#
Tock 2011/01/07



8/26 Change Q14 to SB000009610 Standard Part

9/24 Change U9 to SA00001TC00

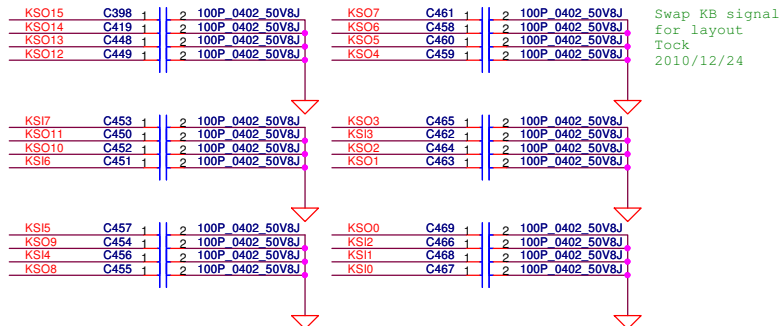
LID Switch



Security Classification		Compal Secret Data				Compal Electronics, Inc.									
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								ON/OFF / PWR SW/ LID SW							
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	JKB1
	G2
	G1
KS10	24
KS11	23
KS12	22
KS00	21
KS01	20
KS02	19
KS13	18
KS03	17
KS05	16
KS06	15
KS07	14
KS08	13
KS14	12
KS09	11
KS15	10
KS8	9
KS10	8
KS011	7
KS17	6
KS012	5
KS013	4
KS014	3
KS015	2
	1

ACES 85202-24051
CONN@

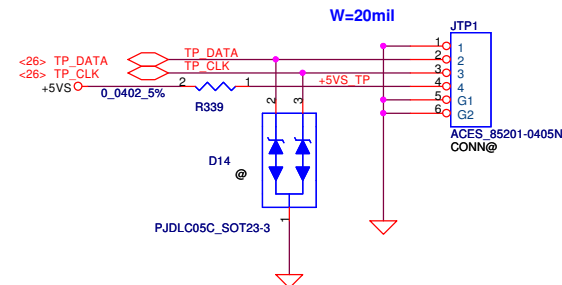


KS[0..7] KS[0..7] <26>
KS[0..15] KS[0..15] <26>

8/22 Update JKB1 Symbol from database (ACES_85202-24051_24P)
8/23 Update KB pin definition

To TP/B Conn.

8/24 Update JTP1 Symbol from database (ACES_85201-0405N_4P)
& Update pin definition



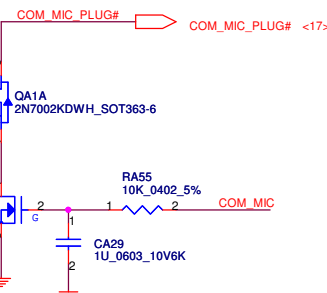
change RA52,DA10,CA26 BOM structure to @
by vender review for pop issue
Tock 2010/12/08

change RA9 from 20K to 0 ohm
Tock 2011/03/03

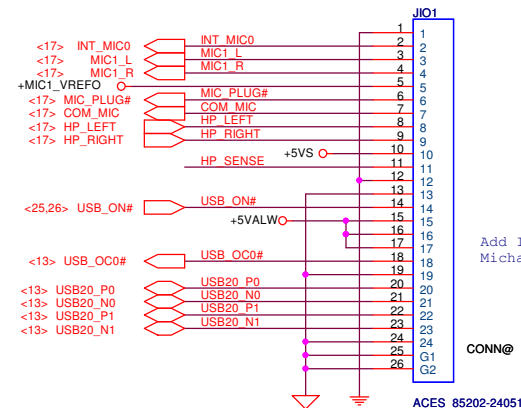
Add QA4,RA55,CA29,RA36 for Internal Mic
can't record issue . Tock 2011/02/21

remove CA4 change QA1 , QA2 from SB501380020 <BSS138> to SB00000E010 <2N7002>. Tock 2011/02/24

-change CA49 BOM structure to @
change RA41 from 47K to 4.7K
by vender review for pop issue
Tock 2010/12/08



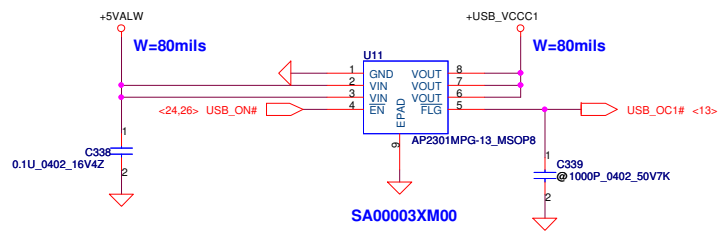
```
Add net INT_MIC0 on JIO1 pin 2
Tock 2010/11/26
```



Add IO connector
Michael 2010/11/18

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				Size	Document Number
				P1VE6 Schematics	
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11/17 Move Left Side USB CONN. Circuit to IO board



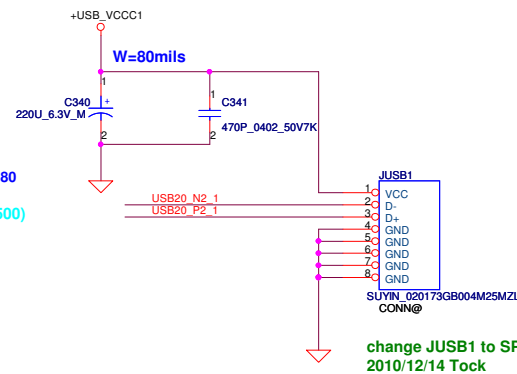
SA00003XM00

8/25 Change C340 from poly-cap to E-cap (SF000001500)

delete D17 for DFB issue
2011/02/25 Tock

SGA00002N80

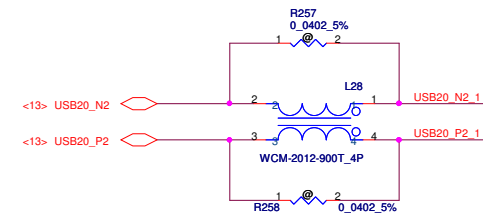
Change C340 to SF000001500
2010/12/14 Tock



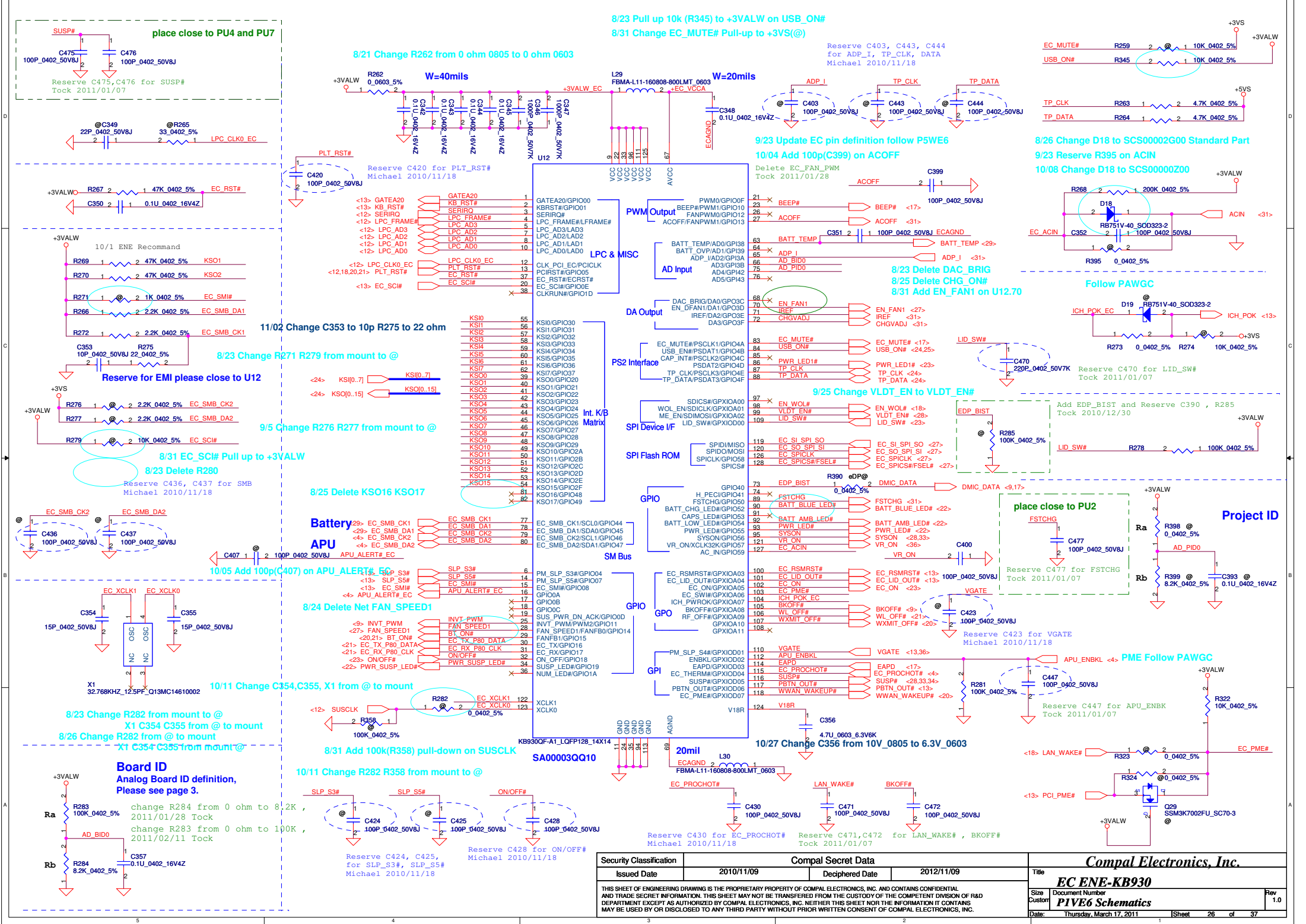
change JUSB1 to SP060004B00
2010/12/14 Tock

Right Side USB CONN.

9/28 Swap L28

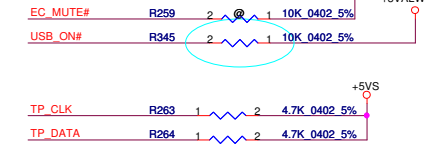


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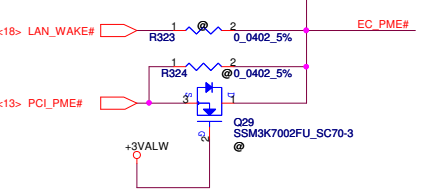
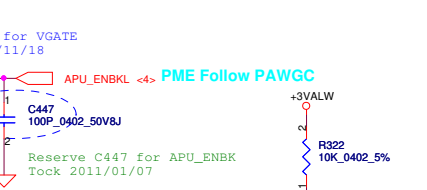
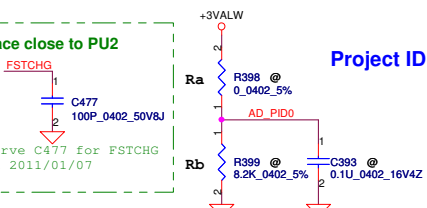
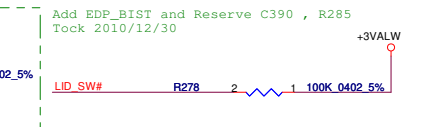
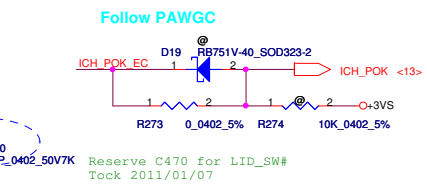
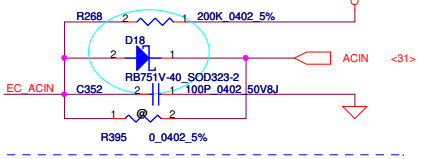


8/23 Pull up 10k (R345) to +3VALW on USB_ON#
8/31 Change EC_MUTE# Pull-up to +3VS(@)

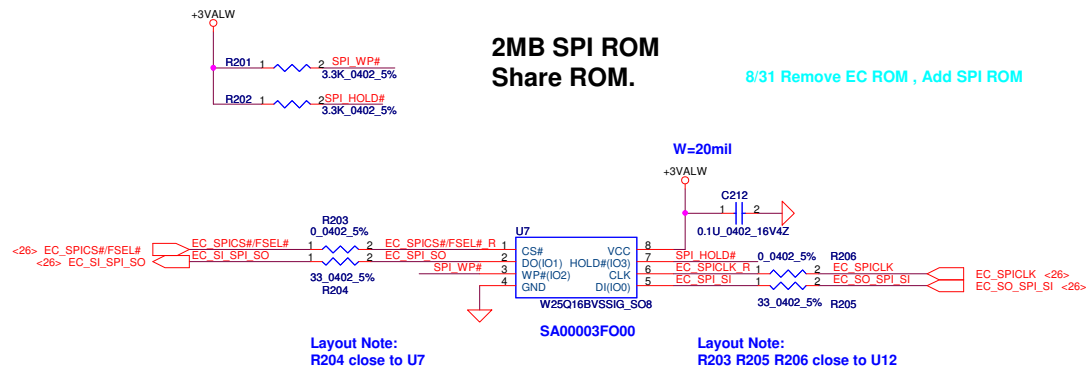
Reserve C403, C443, C444
for ADP_I, TP_CLK, DATA
Michael 2010/11/18



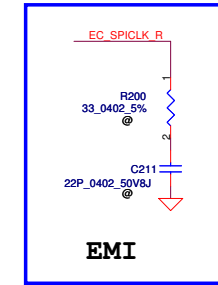
8/26 Change D18 to SCS00002G00 Standard Part
9/23 Reserve R395 on ACIN
10/08 Change D18 to SCS00000200



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Deciphered Date				2012/11/09				PIVE6 Schematics			
Title				Thursday, March 17, 2011				Sheet 26 of 37			
Size				Rev 1.0							
Document Number											
Date											



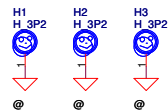
9/2 Change EC_SPICLK to EC_SPICLK_R



Delete U17,C382,C386,R355,D20,C383,C384,C385
for Fan control IC circuit
2010/12/15 Tock

Add U17,C382,C386,R355,D20,C383,C384,C385
for Fan control IC circuit
2011/01/19 Tock

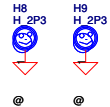
3P2 x 3 (APU)



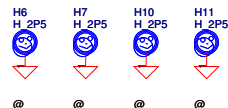
3P0N x 1



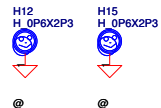
2P3 x 2



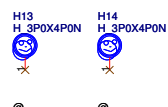
2P5 x 4



0P6X2P3 x 2



3P0X4P0N x 2

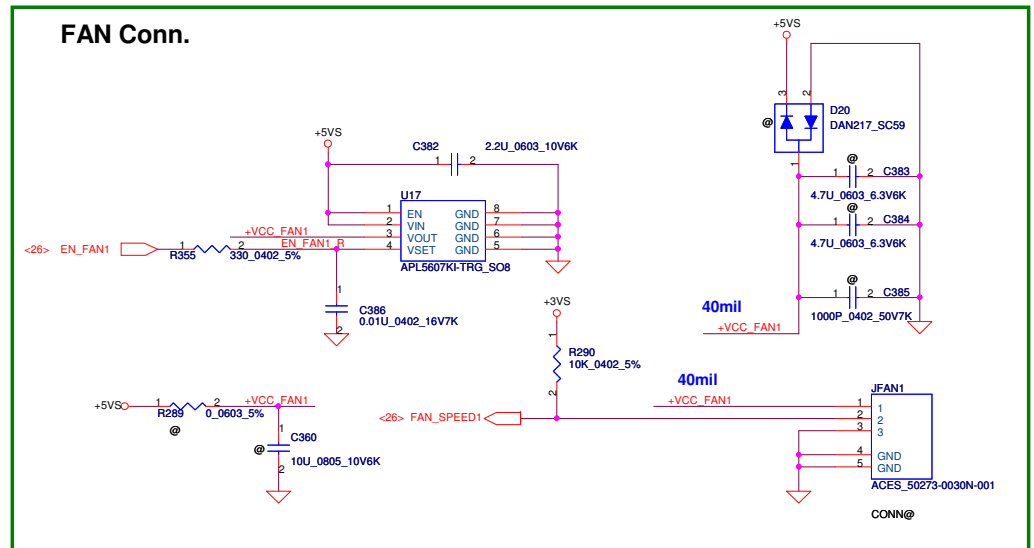


9/15 Update the Screw Hole
9/20 Add H20 (H_3P4X3P2N)
10/07 Change H13 from GND to LANGND
10/07 Change H13 from LANGND to GND

Update the Screw Hole
2010/12/16 Tock
Update the Screw Hole
2010/12/22 Tock



FAN Conn.



8/24 Update JFAN1 Symbol from database (ACES_85205-03001_3P) & Update pin definition
8/24 Delete R290

8/25 Update JFAN1 Symbol from database (ACES_85205-04001_4P) & Update pin definition
8/25 Add R290 10k pull-up tp +3VS

8/31 Reserve U17,C382~C386, R355~R357, D20 (Fan Drive Circuit)

change JFAN1 footprint from ACES_85205-04001_4P to ACES_50273-0030N-001_3P , 2011/01/28 Tock ,
delete EC_FAN_PWM and R356,R357 , 2011/01/28 Tock ,

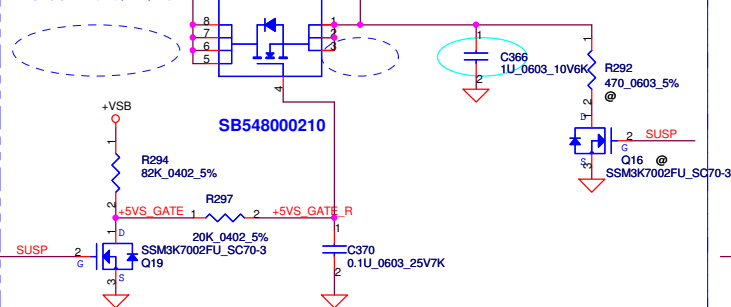
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/11/09		Deciphered Date		2012/11/09		Title	
										Screw / EC ROM /FAN	
										P1VE6 Schematics	
										Rev 1.0	
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+5VALW TO +5VS

Remove C364 10U
Michael 2010/11/18

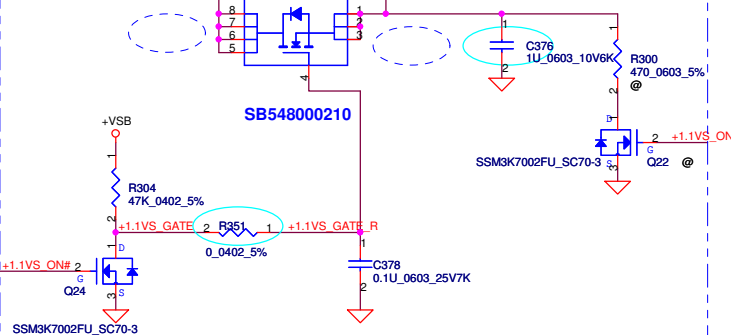
Remove C365 10U
Michael 2010/11/18



+1.1ALW to +1.1VS

Remove C374 10U
Michael 2010/11/18

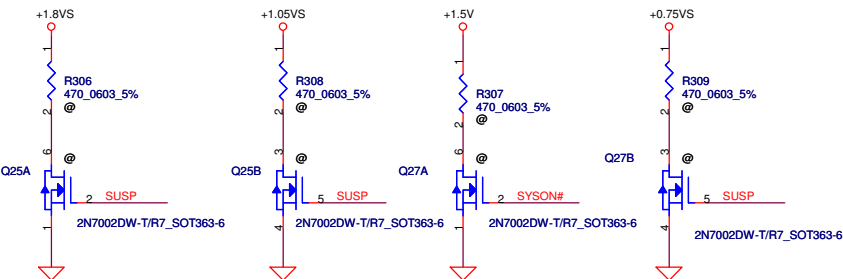
Remove C375 10U
Michael 2010/11/18



9/27 Change R304.1 from +5VALW to +VSB

Change Q25 package to SOT363-6
Remove Q26
Michael 2010/11/18

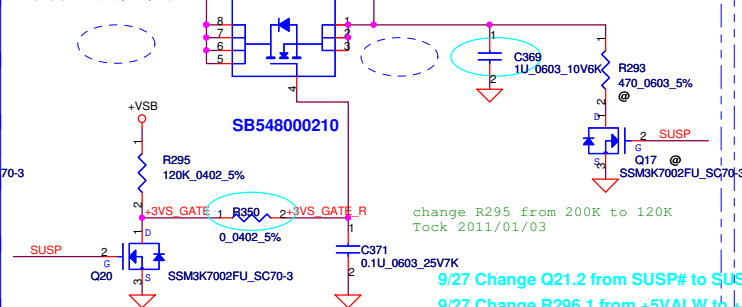
Change Q27 package to SOT363-6
Remove Q28
Michael 2010/11/18



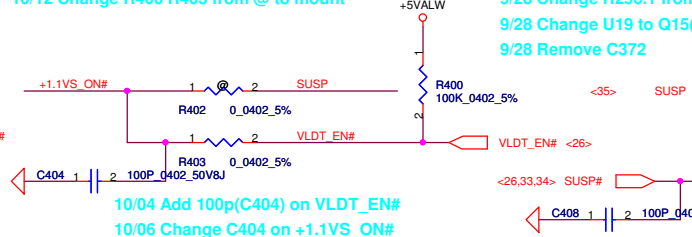
+3VALW TO +3VS

Remove C367 10U
Michael 2010/11/18

Remove C368 10U
Michael 2010/11/18



10/12 Change R402 from mount to @
10/12 Change R400 R403 from @ to mount



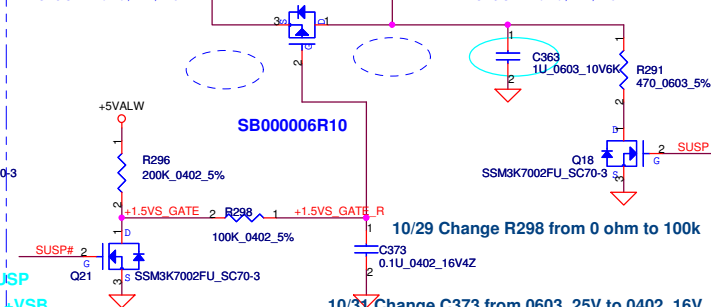
10/27 Add C408(100P) on SUSP# close to PR70

10/12 Change R294 to 100k
10/12 Change R295, R296 to 200k
10/12 Change R304 to 47k
10/12 Change R294 to 82k
10/12 Change R297 to 20k

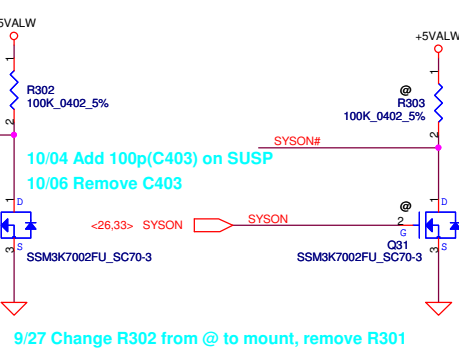
+1.5V to +1.5VS

Remove C361 10U
Michael 2010/11/18

Remove C362 10U
Michael 2010/11/18



2011/02/11 Change Q15 to SB000006R10



9/27 Change R302 from @ to mount, remove R301

10/31 Change C361 C362 from mount to @

8/19 Change Q16-Q22 Q24-Q28 to SB000009610(SSM3K7002FU_SC70-3)

8/19 Change Q29 Q30 to Q23A Q23B (SB00000DH00 S TR DMN66D0LDW-7 2N SOT363-6)

8/21 Change U14-U16 to SB548000310 (SI4800BDY-T1-E3_SO8)

8/23 Remove R305 R299 Add R350 R351 for Sequence

8/24 Change Q23A Q23B to Q30 Q31(@) (SB000009610 SSM3K7002FU_SC70-3)

8/25 Change C363,C366,C369,C376 to SE080105K80 Standard Part

8/25 Change C361,C362,C364,C365,C367,C368,C374,C375 to SE000004880 Standard Part

8/26 Change U14, U15, U16 to SB00000GV00 Standard Part

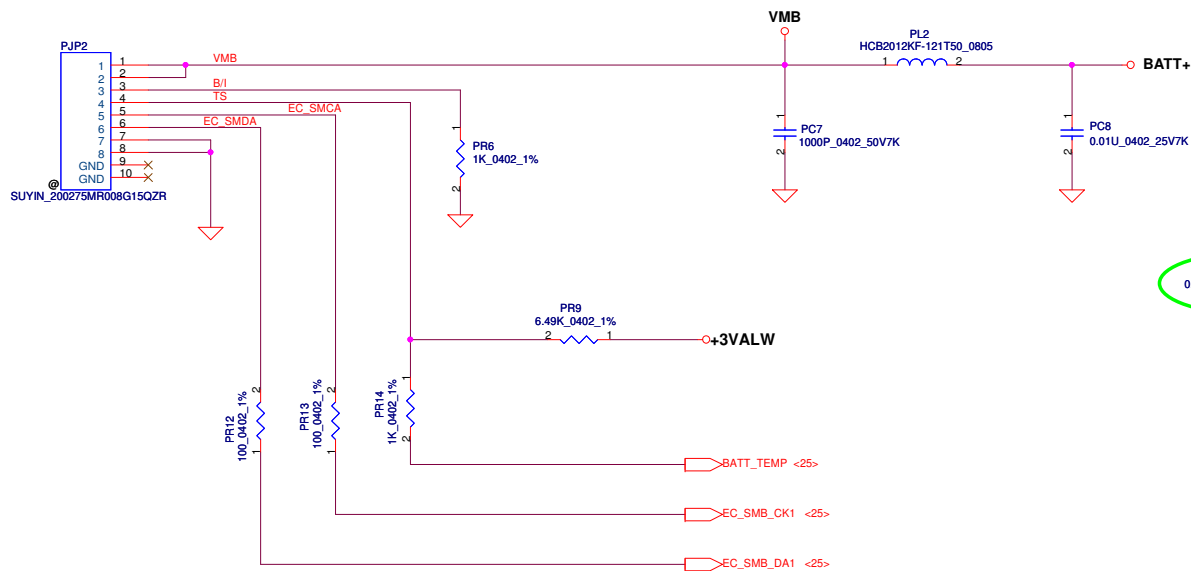
9/3 Delete C377(DIS@)

9/23 Reserve R400-403, Q36 for VLDT_EN

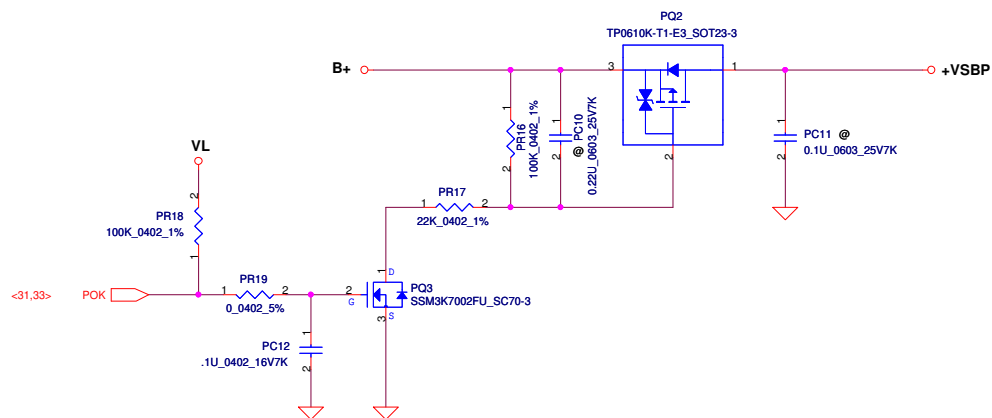
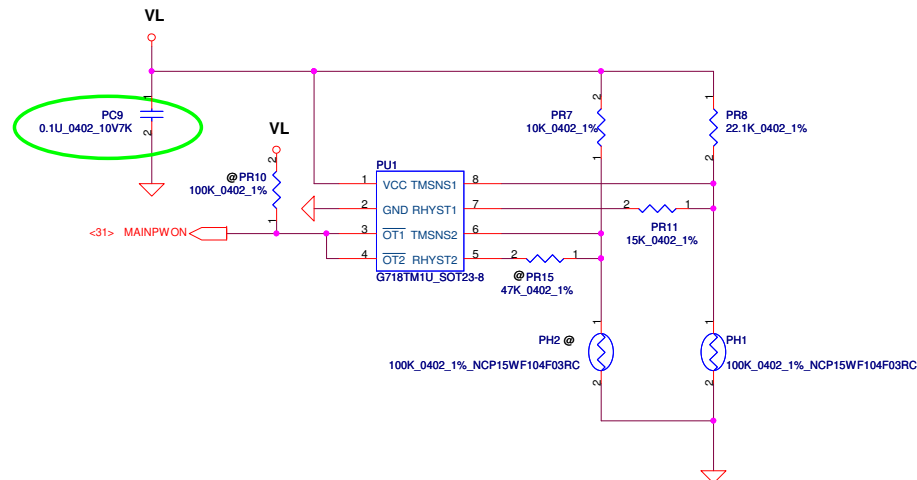
9/25 Remove R401 Q36 on VLDT_EN

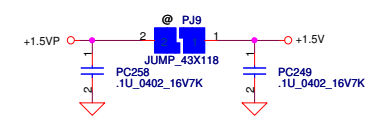
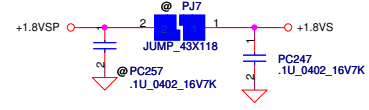
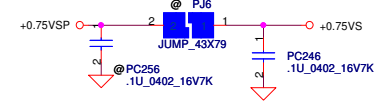
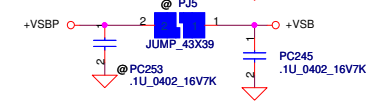
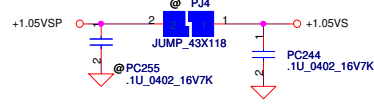
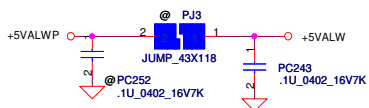
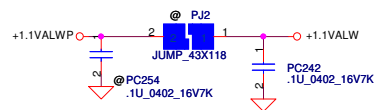
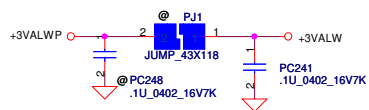
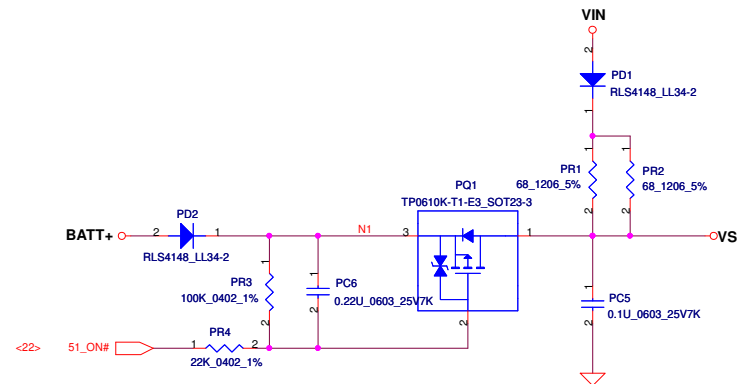
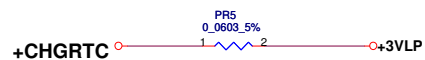
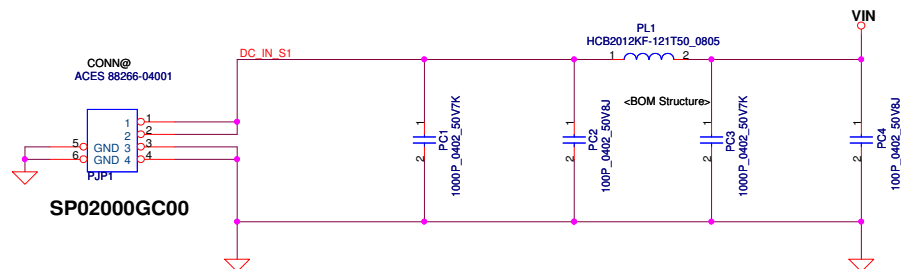
9/25 Add 10k(R404) PD on SUSP#

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				Custom	P1VE6 Schematics	1.0
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PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C



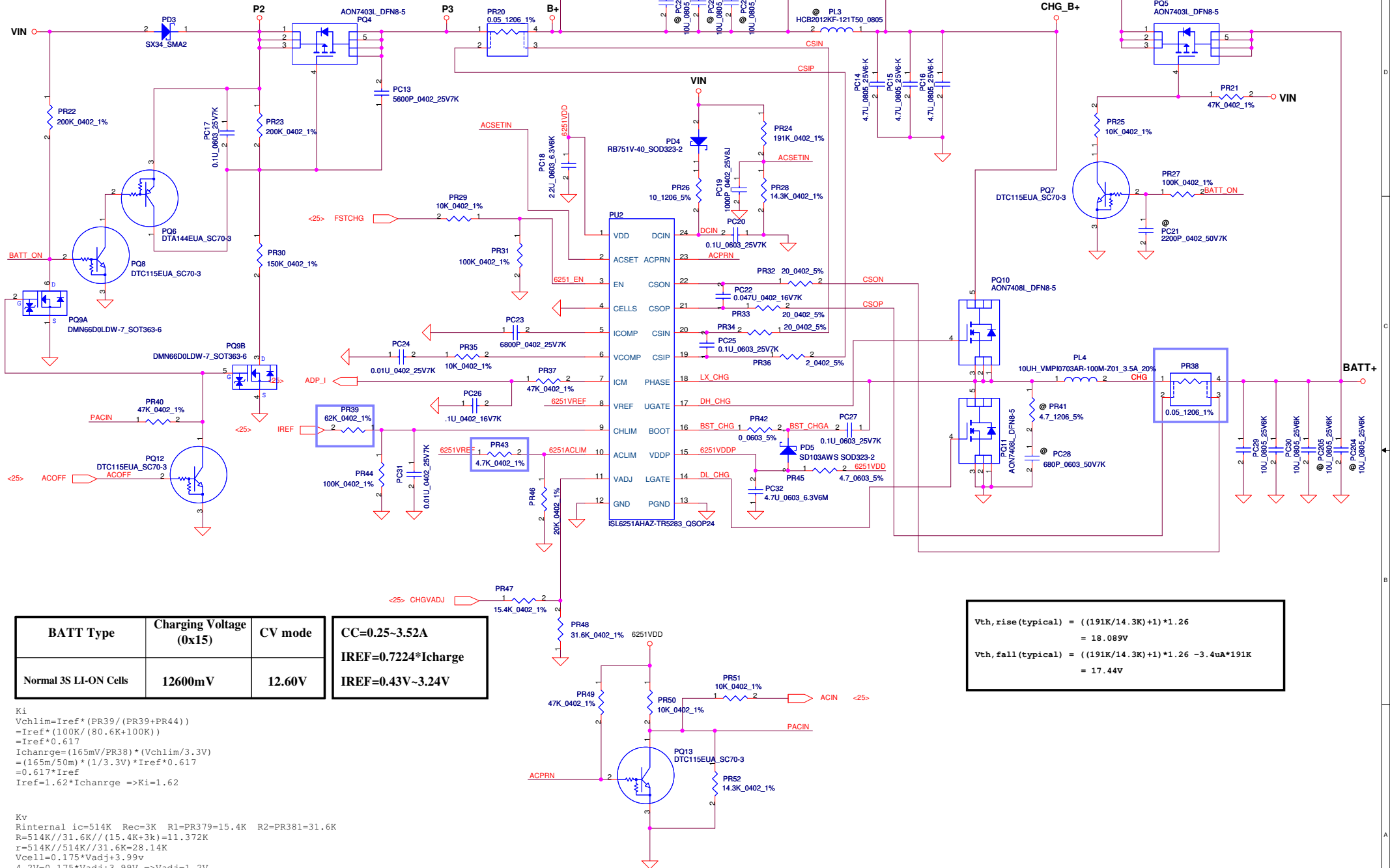


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				DCIN/VIN DETECTOR		
				1.0		

Iada=0~2.105A (40W/19V=2.105A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 1.789A



BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

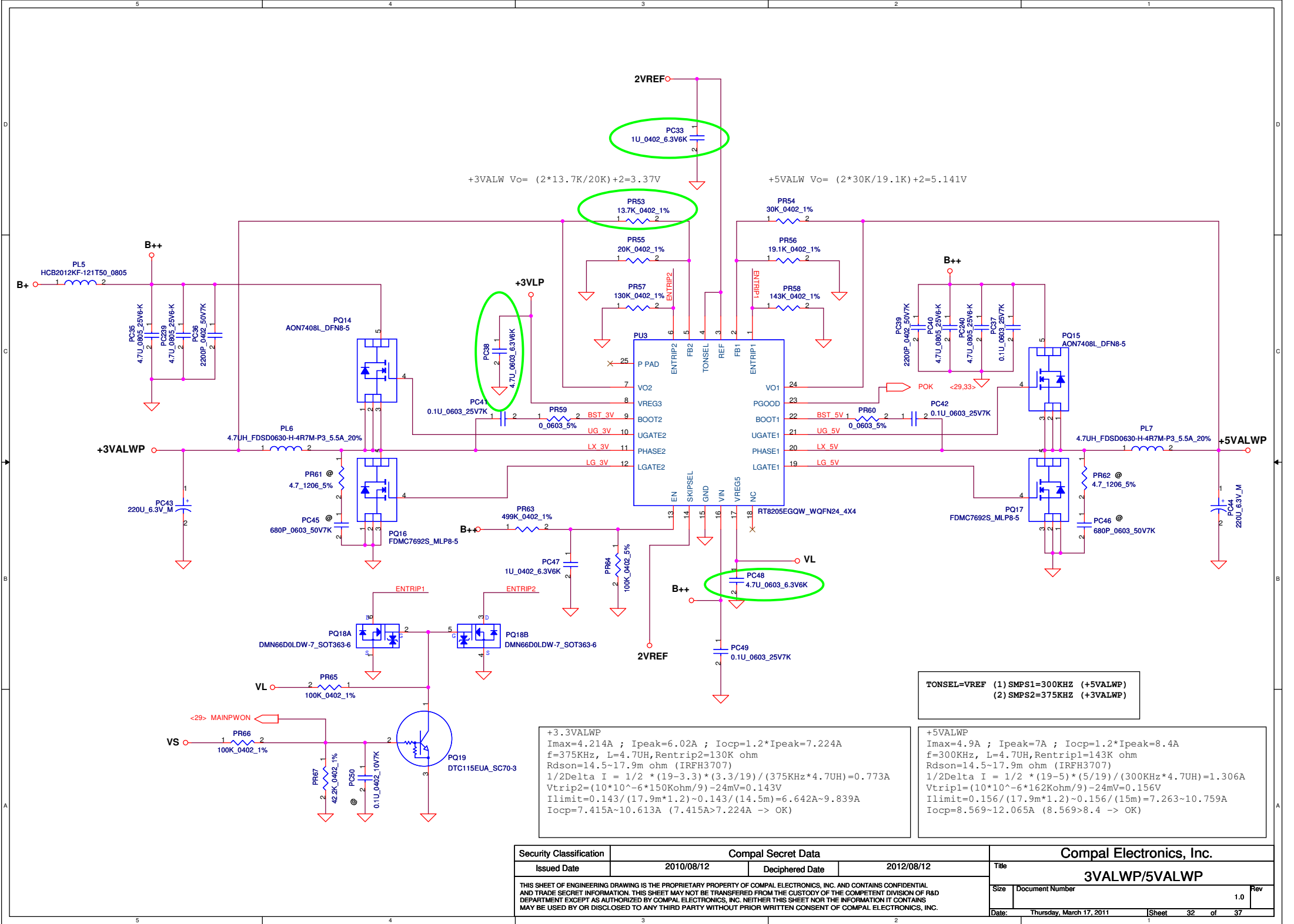
CC=0.25~3.52A
IREF=0.7224*Icharge
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR39/(PR39+PR44))
=Iref*(100K/(80.6K+100K))
=Iref*0.617
Ichange=(165mV/PR38)*(Vchlim/3.3V)
=(165m/50m)*(1/3.3V)*Iref*0.617
=0.617*Iref
Iref=1.62*Ichange => Ki=1.62

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K/(31.6K/(15.4K+3K))=11.372K
r=514K/(514K/31.6K)=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V => Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r+514K))
1.1483=CALIBRATE*0.6046 => CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

Vth, rise (typical) = ((191K/14.3K)+1)*1.26
= 18.089V
Vth, fall (typical) = ((191K/14.3K)+1)*1.26 - 3.4uA*191K
= 17.44V

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								Size	Document Number						Rev
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								1.0							



+3VALW $V_o = (2 \times 13.7K / 20K) + 2 = 3.37V$

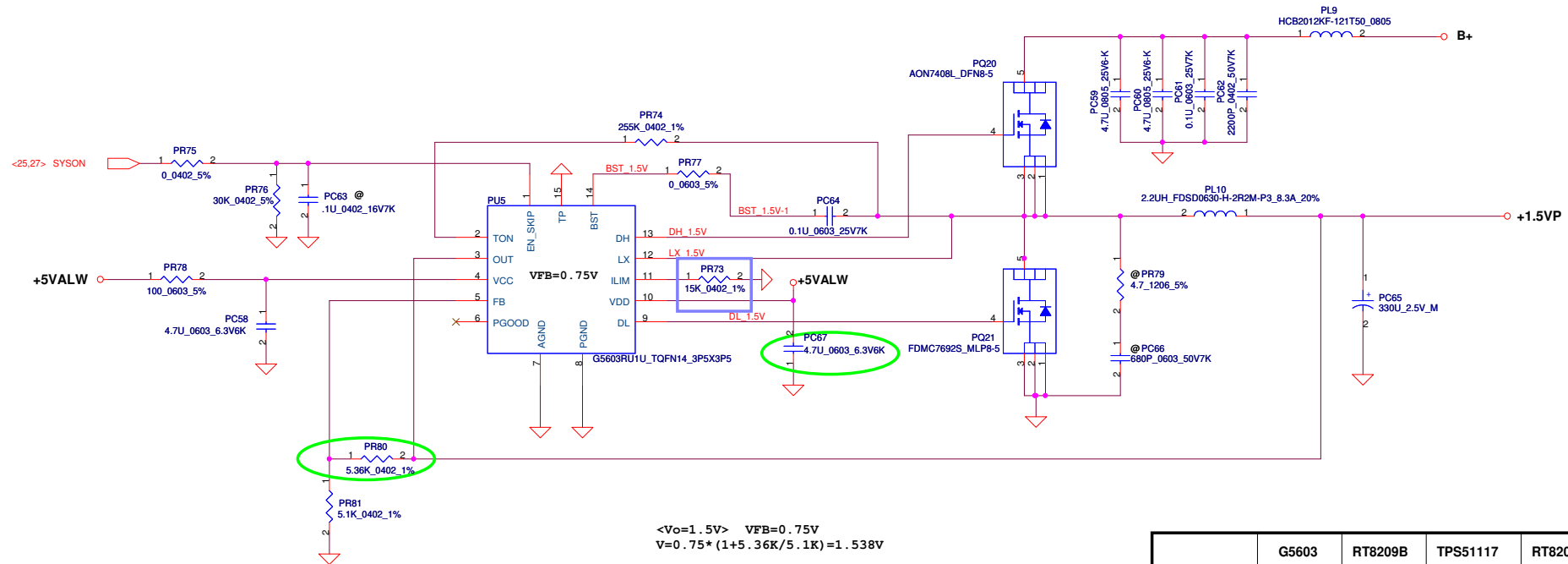
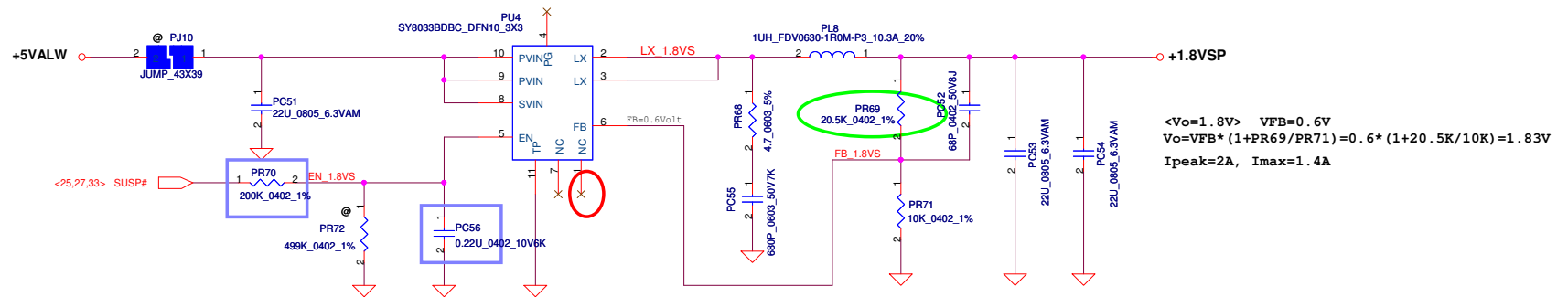
+5VALW $V_o = (2 \times 30K / 19.1K) + 2 = 5.141V$

+3.3VALWP
Imax=4.214A ; Ipeak=6.02A ; Iocp=1.2*Ipeak=7.224A
f=375KHz, L=4.7UH, Rentrtp2=130K ohm
Rdson=14.5~17.9m ohm (IRFH3707)
1/2Delta I = 1/2 * (19-3.3) * (3.3/19) / (375KHz*4.7UH) = 0.773A
Vtrip2=(10*10^-6*150Kohm/9)-24mV=0.143V
Ilimit=0.143/(17.9m*1.2)-0.143/(14.5m)=6.642A~9.839A
Iocp=7.415A~10.613A (7.415A>7.224A -> OK)

+5VALWP
Imax=4.9A ; Ipeak=7A ; Iocp=1.2*Ipeak=8.4A
f=300KHz, L=4.7UH, Rentrtp1=143K ohm
Rdson=14.5~17.9m ohm (IRFH3707)
1/2Delta I = 1/2 * (19-5) * (5/19) / (300KHz*4.7UH) = 1.306A
Vtrip1=(10*10^-6*162Kohm/9)-24mV=0.156V
Ilimit=0.156/(17.9m*1.2)-0.156/(15m)=7.263~10.759A
Iocp=8.569~12.065A (8.569>8.4 -> OK)

TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
(2) SMPS2=375KHZ (+3VALWP)

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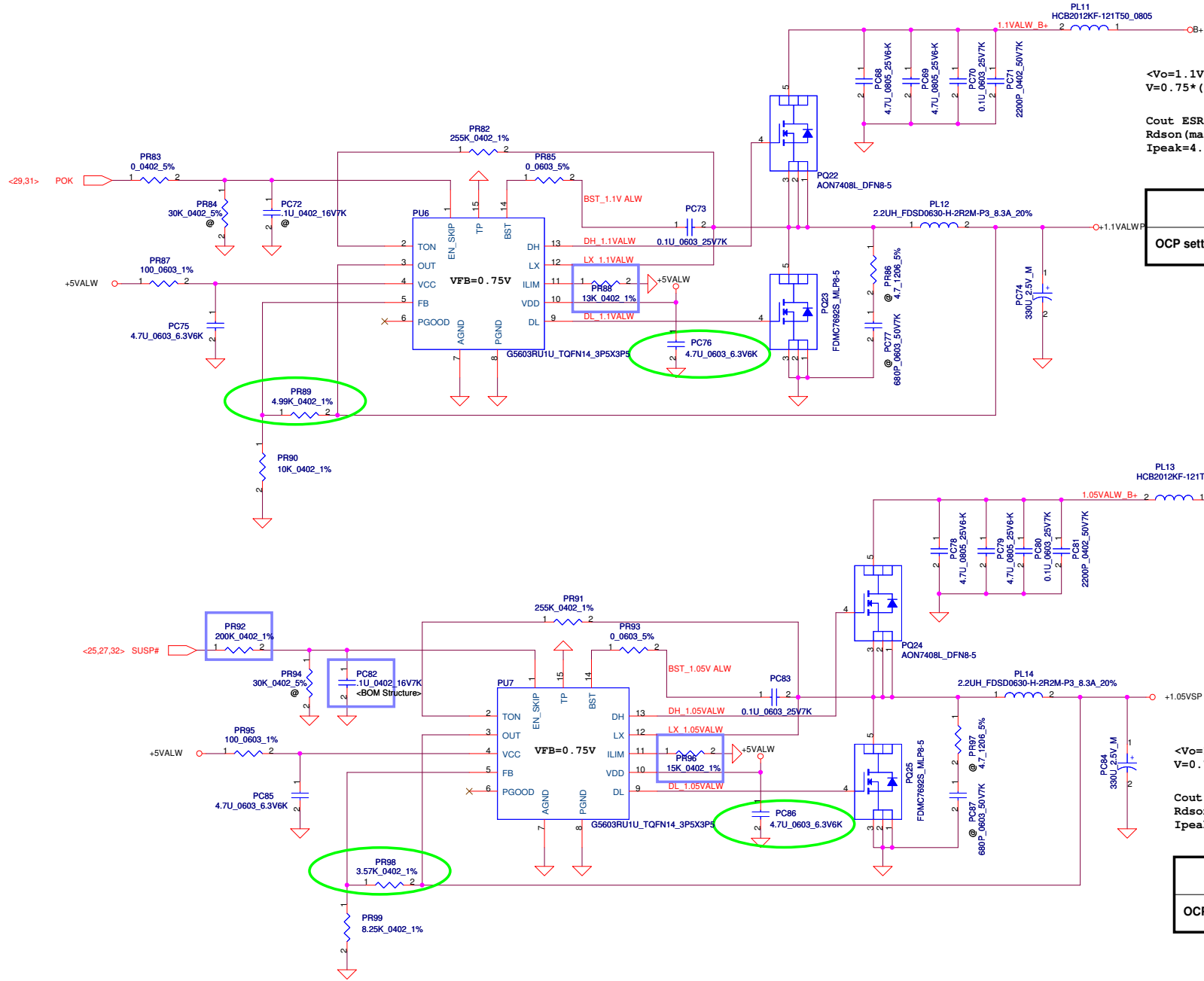


Cout ESR=25m ohm
 Rdson(max)=17.9 mohm Rdson(typ)=14.5 mohm. (IRFH3707)
 Ipeak=6.5A, Imax=4.55A, Iocp > 7.8A

	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.821A	7.235A	8.000A	8.178A

	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/°C	1600ppm/°C	4500ppm/°C	4800ppm/°C
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

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$$V_o = 1.1V \quad V_{FB} = 0.75V$$

$$V = 0.75 * (1 + 4.99K/10K) = 1.124V$$

Cout ESR=25m ohm
 Rdson(max)=17.9 mohm Rdson(typ)=14.5 mohm. (IRFH3707)
 Ipeak=4.02A, Imax=2.814A, Iocp > 4.824A

	G5603	RT8209B	TPS51117	RT8209M
OCP setting	5.799A	6.183A	6.845A	6.976A

$$V_o = 1.05V \quad V_{FB} = 0.75V$$

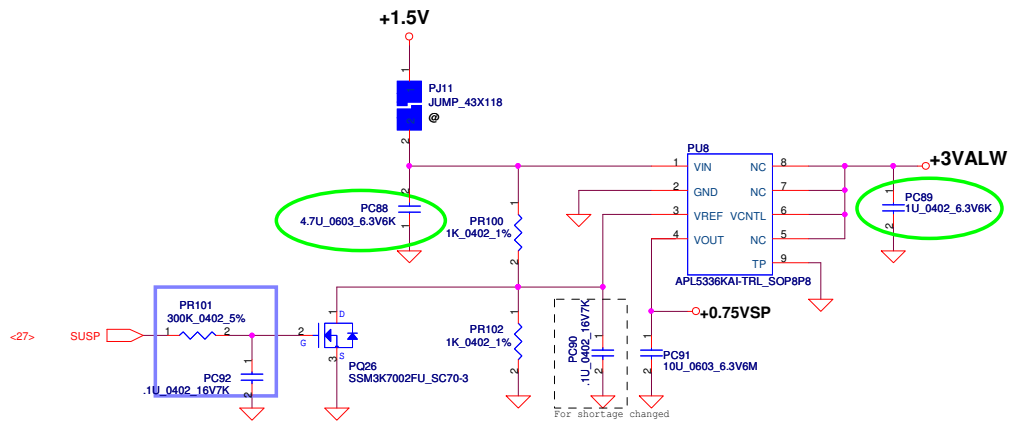
$$V = 0.75 * (1 + 3.57K/8.25K) = 1.074V$$

Cout ESR=25m ohm
 Rdson(max)=17.9m ohm Rdson(typ)=14.5 mohm. (IRFH3707)
 Ipeak=5.5A, Imax=3.85A, Iocp > 6.6A

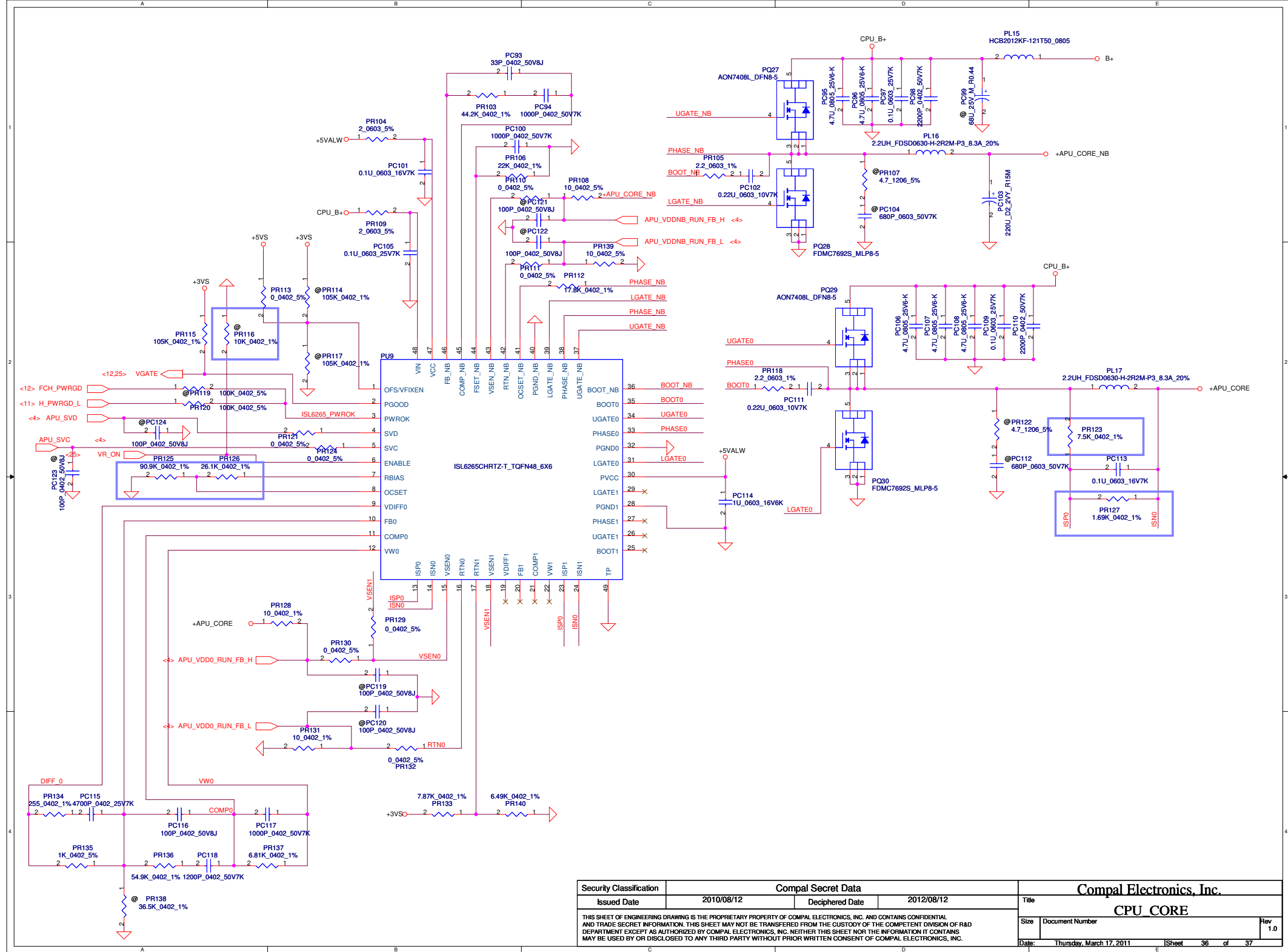
	G5603	RT8209B	TPS51117	RT8209M
OCP setting	6.524A	7.003A	7.768A	7.881A

	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/°C	1600ppm/°C	4500ppm/°C	4800ppm/°C
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify DCIN/VIN DETECTOR power sequence	1	30	Add PC248 for +3VALWP PC252 for +5VALWP PC253 for +VSBP PC254 for +1.1VALWP PC255 for +1.05VSP PC256 for +0.75VSP PC257 for +1.8VSP	20101228	EVT
2		Modify charger power sequence	1	31	delete PC234	20101228	EVT
3		Modify 3VALWP/5VALWP power sequence	1	32	delete PC34	20101228	EVT
4		Modify charger power sequence	1	31	Chang PD5 from SCS00000200 (RB751V-40_SOD323-2 to SCS00005I00 (SD103AWS SOD323-2)	20110104	EVT
5		Modify charger power sequence	1	31	Chang PD3 from SCS00001180 (B340A SMA) to SCS00000W00 (SX34_SMA2) Chang PQ4&PQ5 from SB00000KI00 (SI7121DN-T1-GE3 1P POWERPAK1212-8) to SB00000KZ00 (AON7403L_DFN8-5)	20110106	EVT
6		Modify 3VALWP/5VALWP power sequence	1	32	Chang PL6 & PL7 from SH00000F900 (4.7UH_FDVE0630-H-4R7M= P3_5.5A_20%) to SH00000MB00 (4.7UH_FDS0630-H-4R7M-P3_5.5A_20%)	20110110	EVT
7		Modify 1.8VSP/1.5VP power sequence	1	33	Chang PL10 from SH00000F800 (2.2UH_FDVE0630-H-2R2M=P3_8.3A_20% to SH00000M700 (2.2UH_FDS0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
8		Modify 1.1VALWP/1.05VSP power sequence	1	34	Chang PL12 & PL14 from SH00000F800 (2.2UH_FDVE0630-H-2R2M= P3_8.3A_20%) to SH00000M700 (2.2UH_FDS0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
9		Modify CPU_CORE power sequence	1	36	Chang PL16 & PL17 from SH00000F800 (2.2UH_FDVE0630-H-2R2M= P3_8.3A_20%) to SH00000M700 (2.2UH_FDS0630-H-2R2M-P3_8.3A_20%)	20110110	EVT
10		Modify CPU_CORE power sequence	1	36	Chang PR117 from SD034737280 (7.5k_0402_1%) to SD034737280 (17.5k_0402_1%) Chang PR123 from SD000002680 (6.98k_0402_1%) to SD034750180 (7.5k_0402_1%) Chang PR127 from SD034187180 (1.87k_0402_1%) to SD00000J780 (1.69k_0402_1%)	20110110	EVT
11		Modify 1.8VSP/1.5VP power sequence	2	33	add PC258 to +1.5V output capacitor (co-lay higt from 4.5 to 2.5) for thermal issue	20110208	DVT
12		Modify 1.1VALWP/1.05VSP power sequence	2	34	add PC259 to +1.1VALWP output capacitor (co-lay higt from 4.5 to 2.5) for thermal issue	20110208	DVT
13		Modify 1.8VSP/1.5VP power sequence	3	33	delete co-lay PC258 for +1.5V output capacitor	20110225	PVT
14		Modify 1.1VALWP/1.05VSP power sequence	3	34	delete co-lay PC259 for +1.1VALW output capacitor	20110225	PVT
15		Modify charger power sequence	3	31	delete co-lay PJ32 modify PQ4 PQ5 footprint from AON7403L_DFN8-5 to SIS412DN-T1-GE3_POWERPAK8-5	20110226	PVT
16		Modify charger power sequence	3	31	change charger IC from G5209 to ISL6251 change output choke from 8.2u to 10u	20110226	PVT
17		Modify DCIN/VIN DETECTOR power sequence	3	30	Add PC258 for +1.5V jump by RF test	2010302	PVT
18							
19							
20							
21							
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				PIR (PWR)	
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