

Compal Confidential

HQD70/HDQ71 Schematics Document

Intel Dothan Processor with 915PM/915GM + DDRII + ICH6M
(With ATi M26-P)

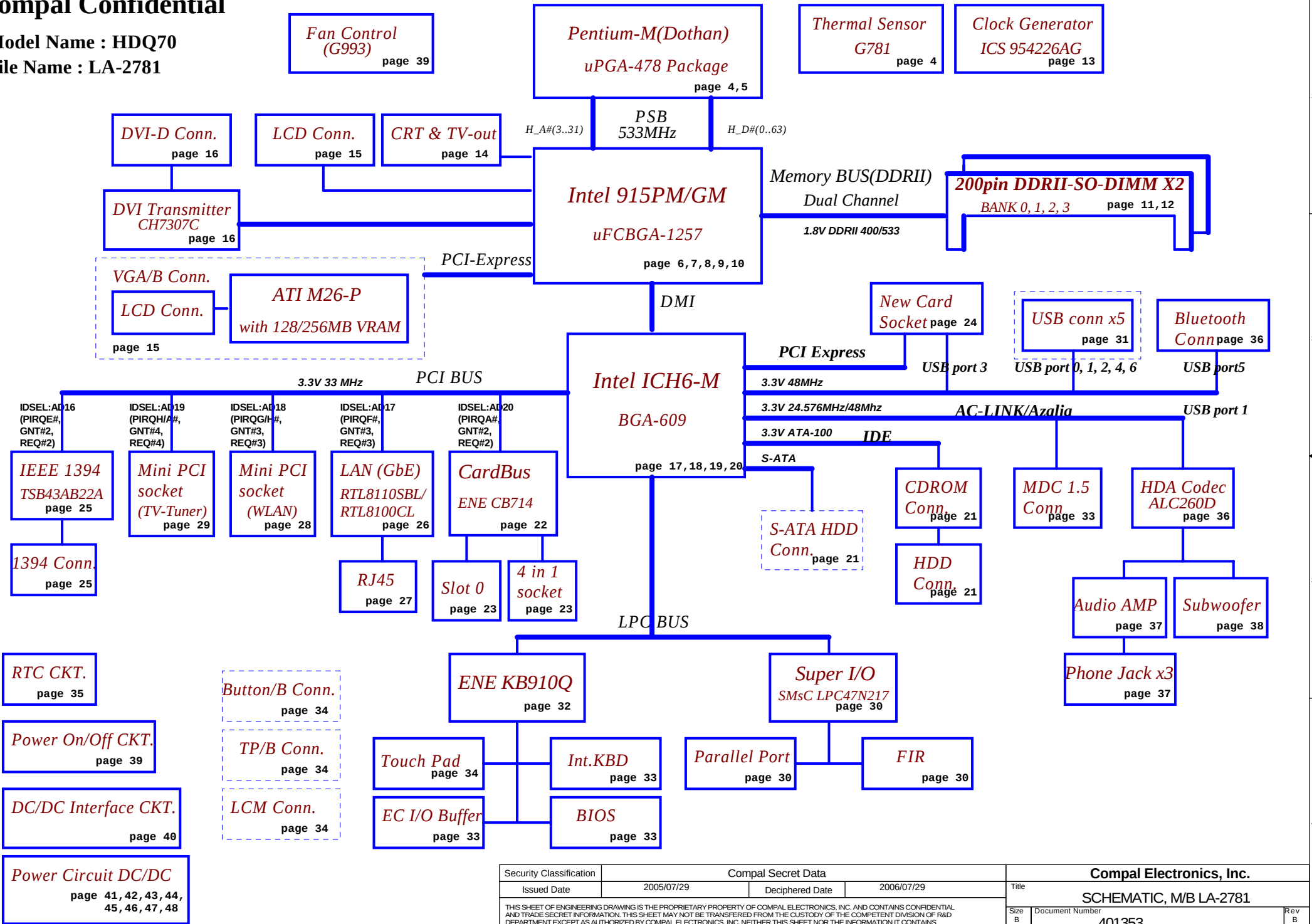
2005 - 07 - 29

REV: 2.0

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Model Name : HDQ70
File Name : LA-2781



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN	AD17	3	PIRQF
Mini-PCI(WLAN)	AD18	1	PIRQG/PORQH
Mini-PCI(TV-Tuer)	AD19	4	PIRQH/PORQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	GMT G781	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 954226)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

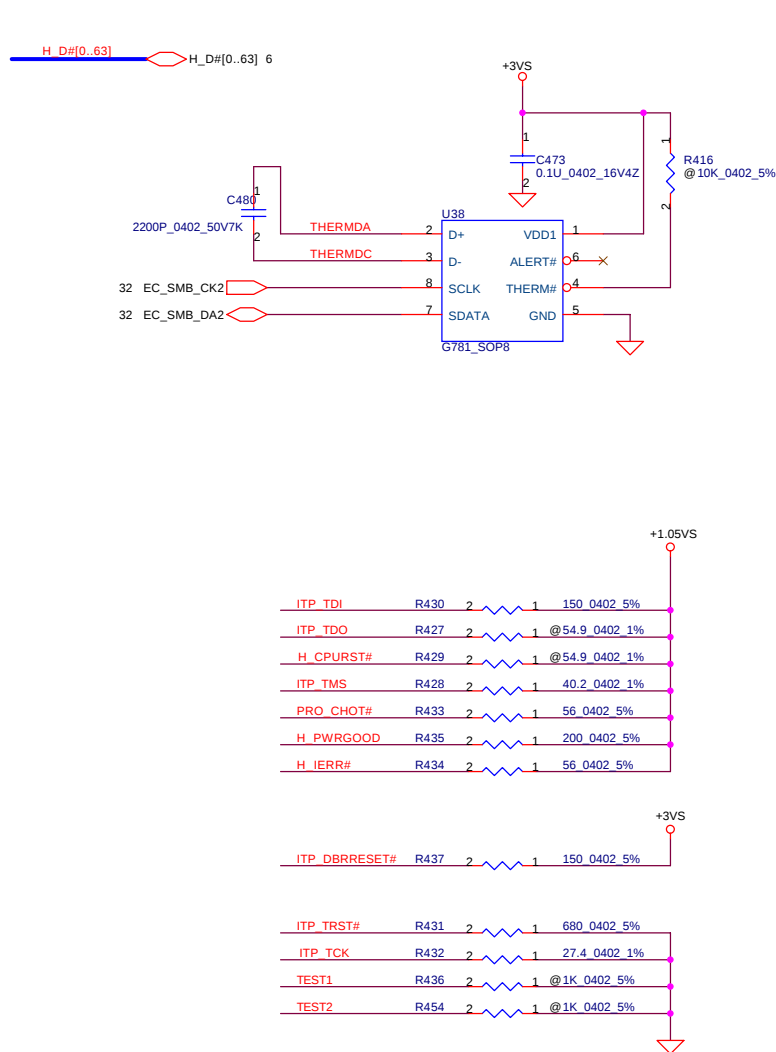
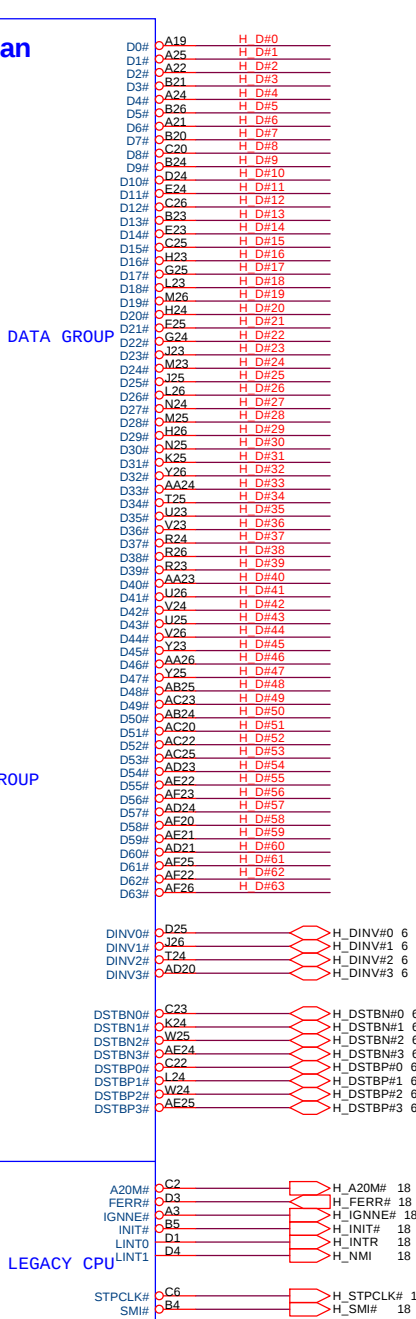
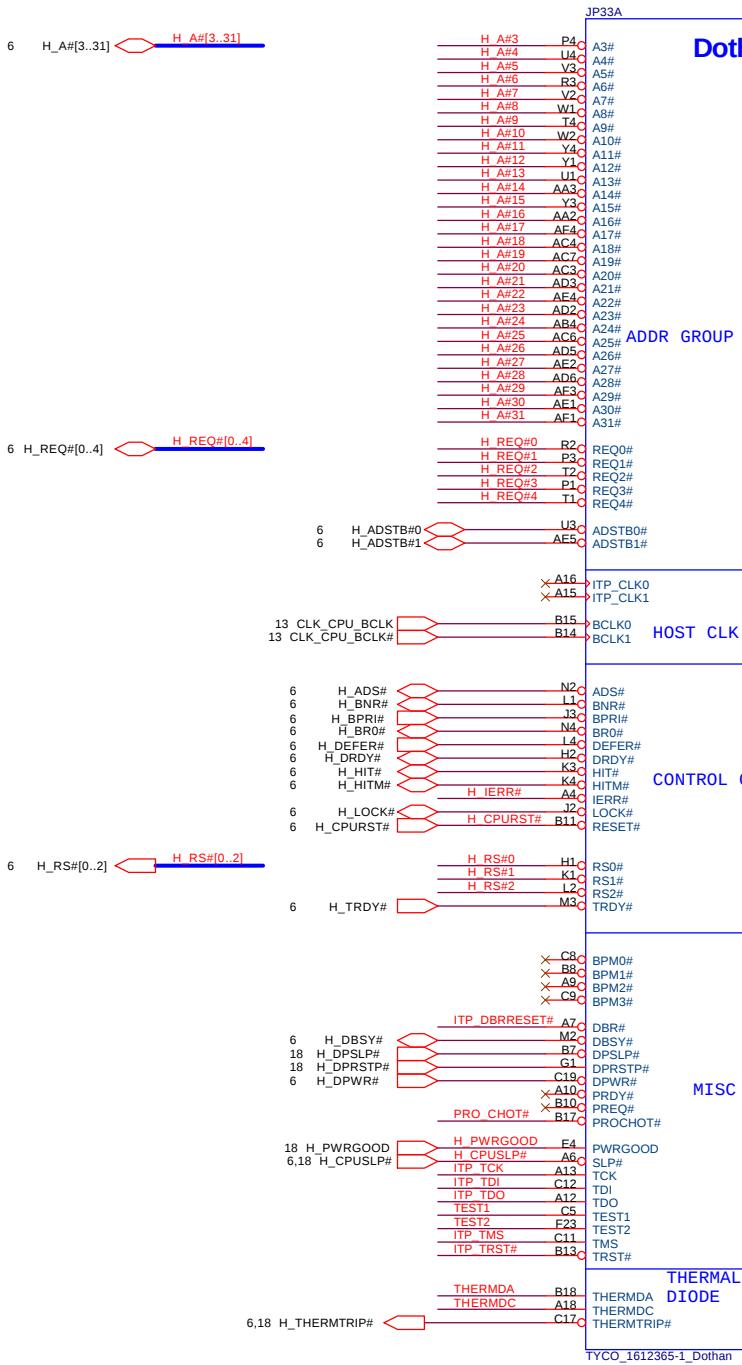
BTO Option Table

BTO Item	BOM Structure
VGA	PM0 GM0
LAN	8118S@ 8110C@
TV-TUNER	TV_TUNER@

SKU ID Table

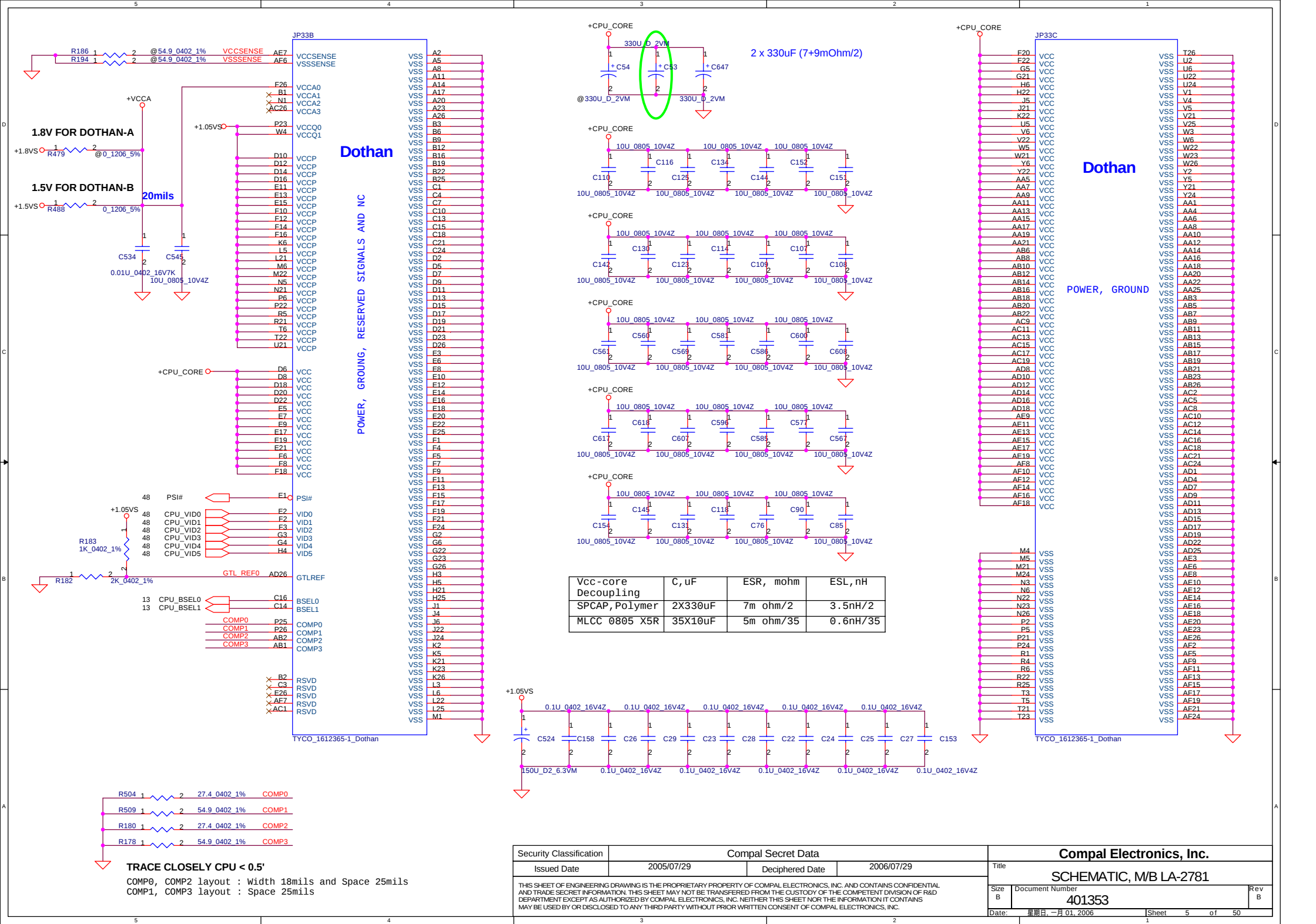
SKU ID	SKU
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1	GM
2	
3	
4	
5	
6	
7	

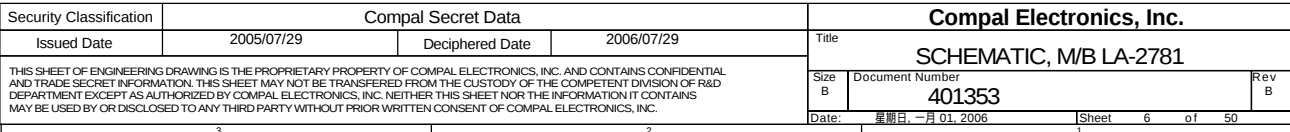
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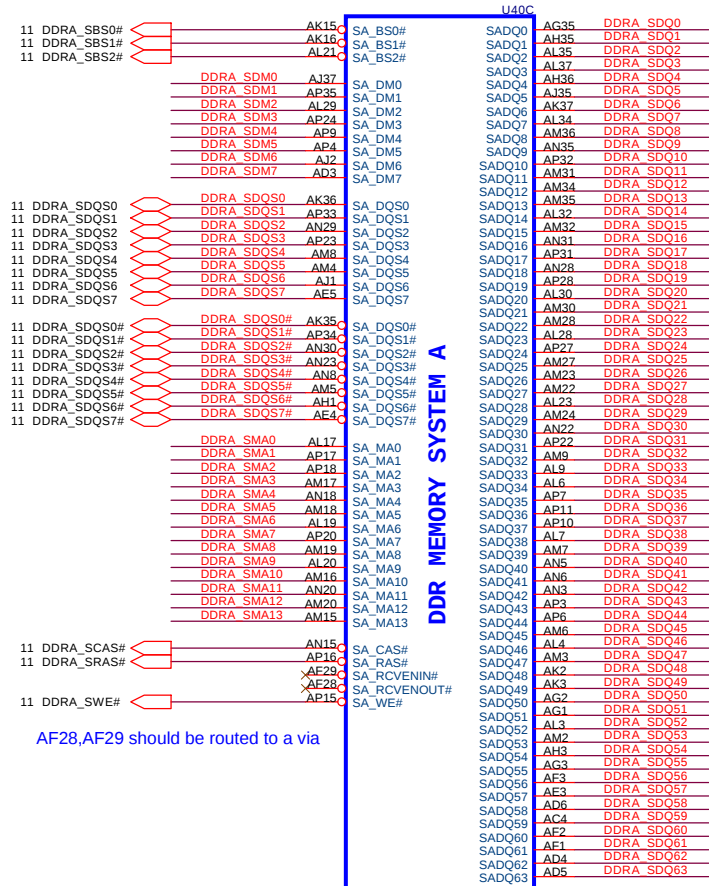
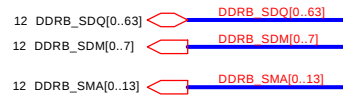
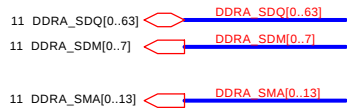


THERMDA & THERMDC Trace / Space = 10 / 10 mil

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DDR MEMORY SYSTEM A

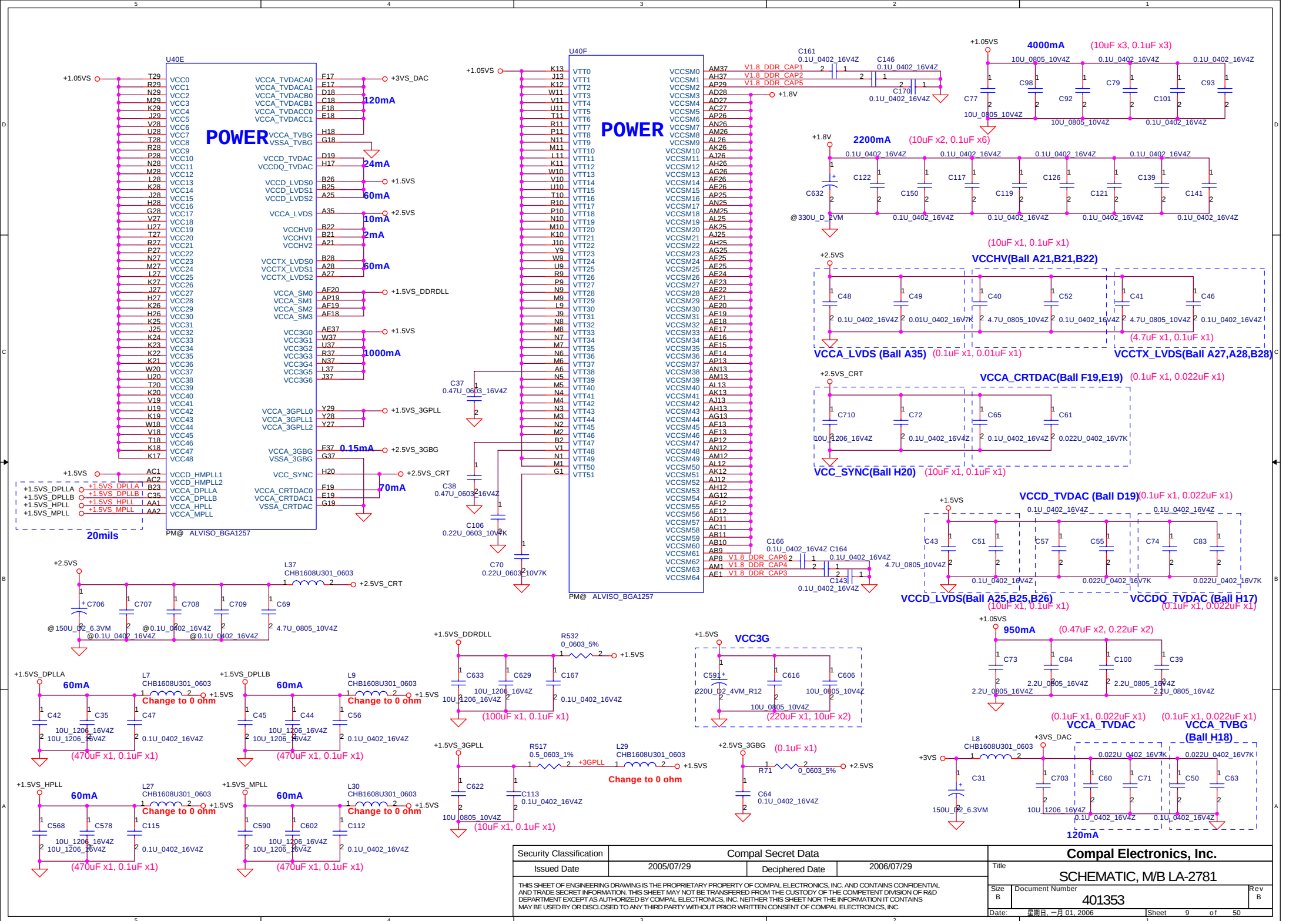
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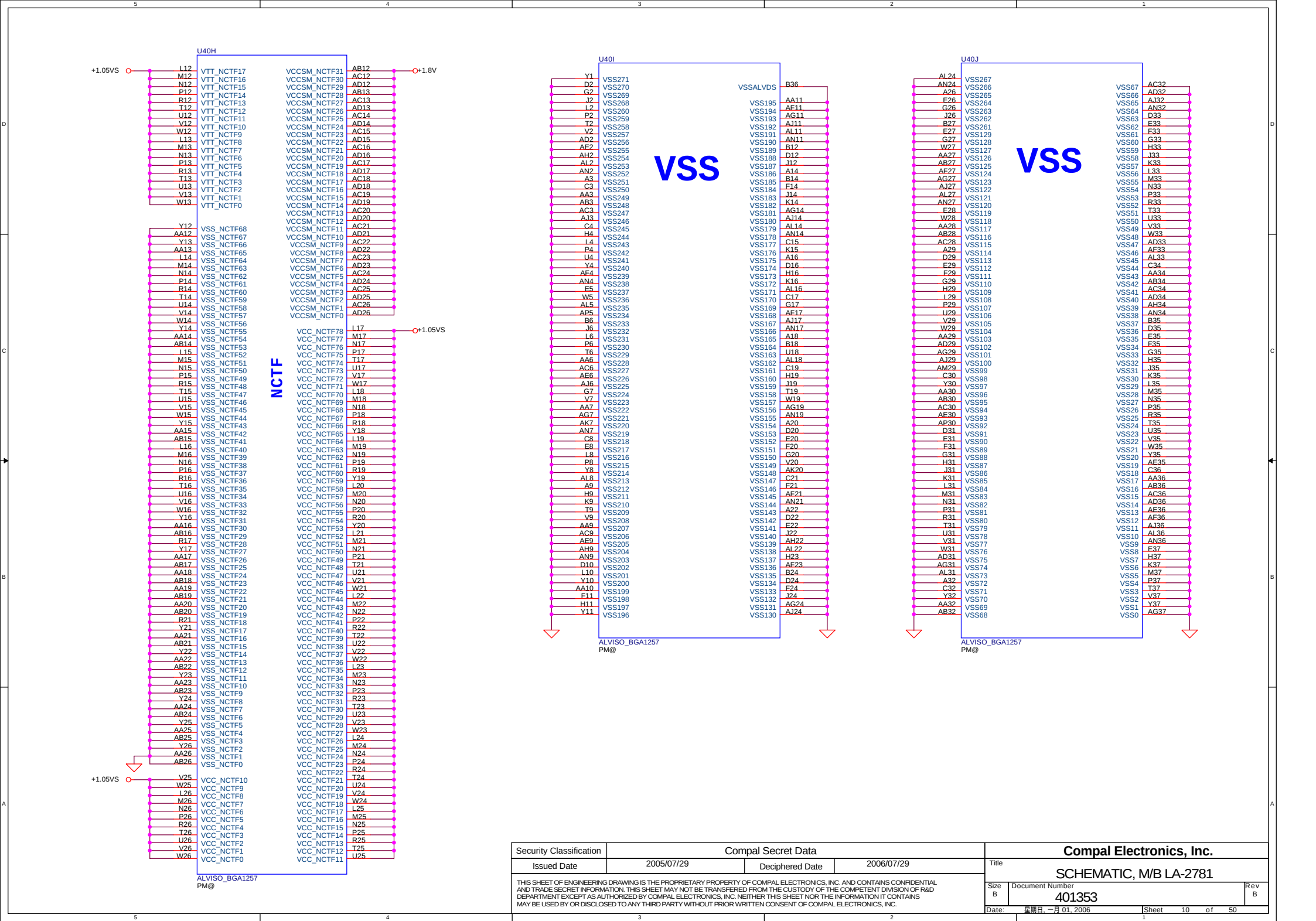


DDR SYSTEM MEMORY B

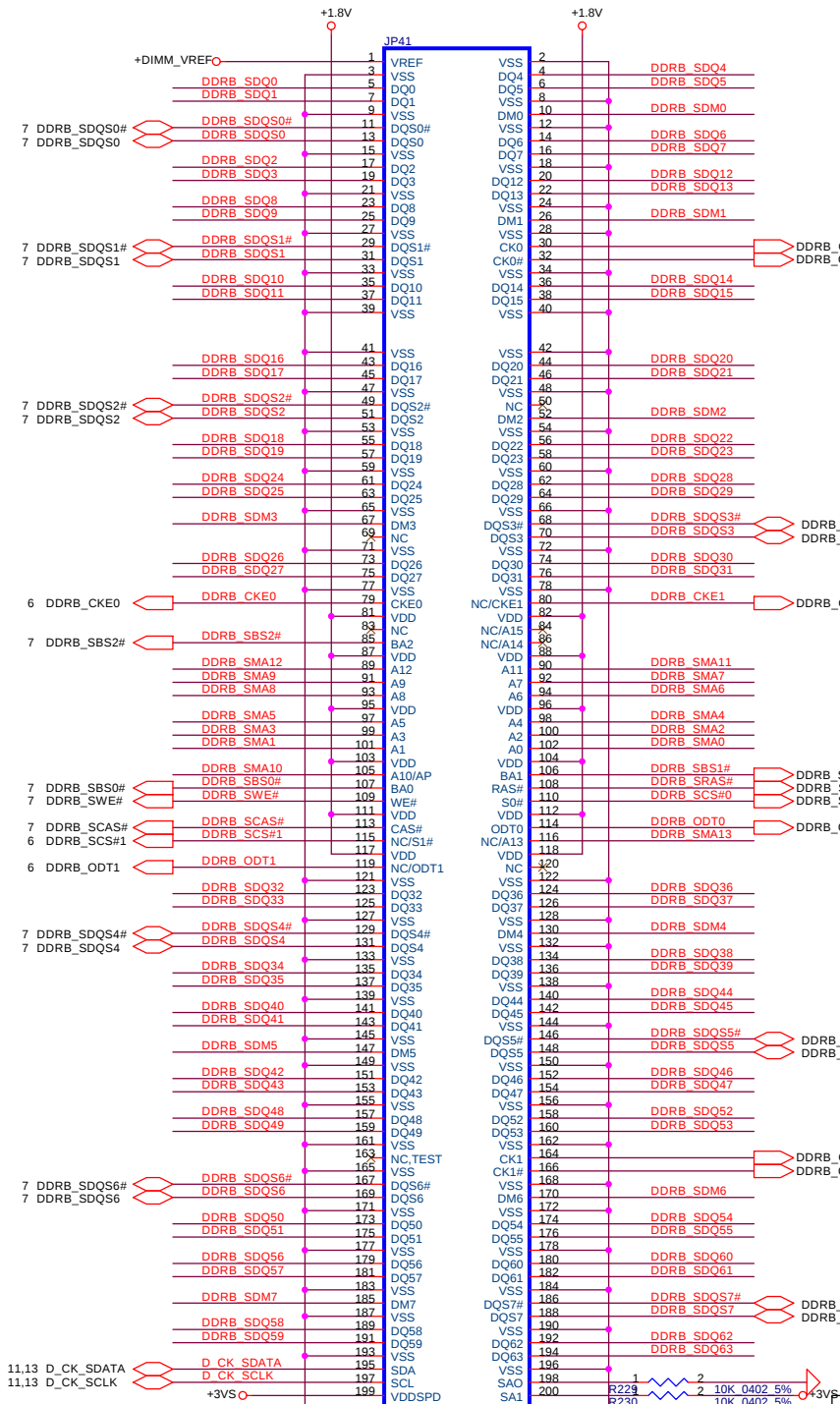
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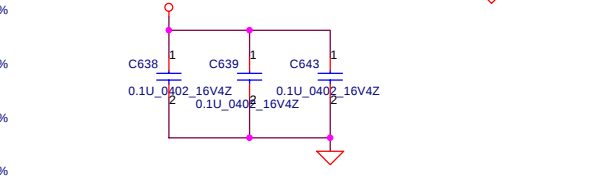
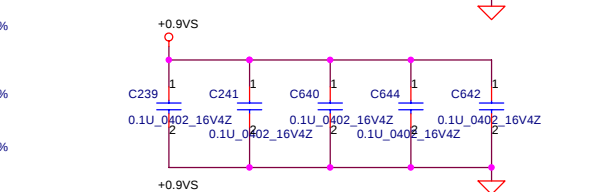
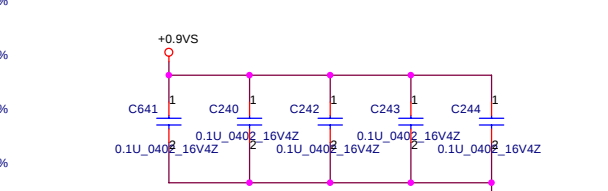
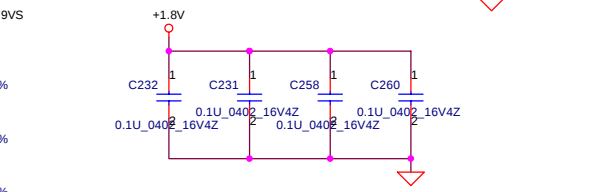
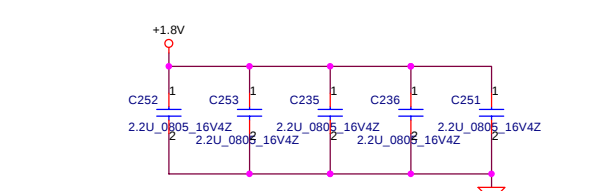
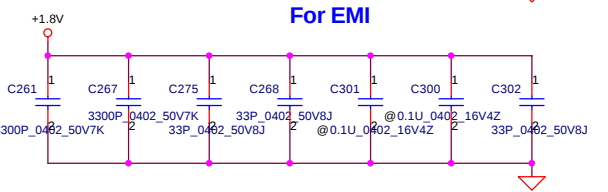
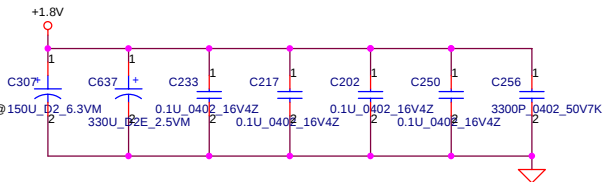
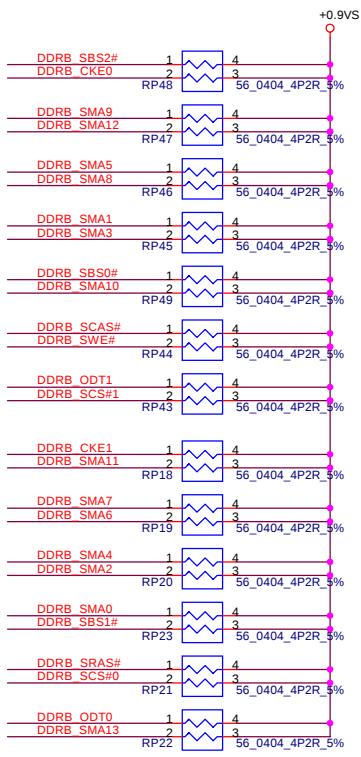
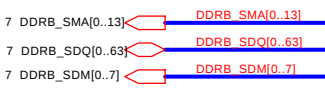
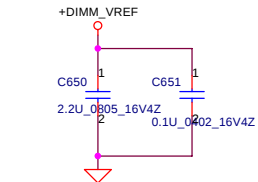




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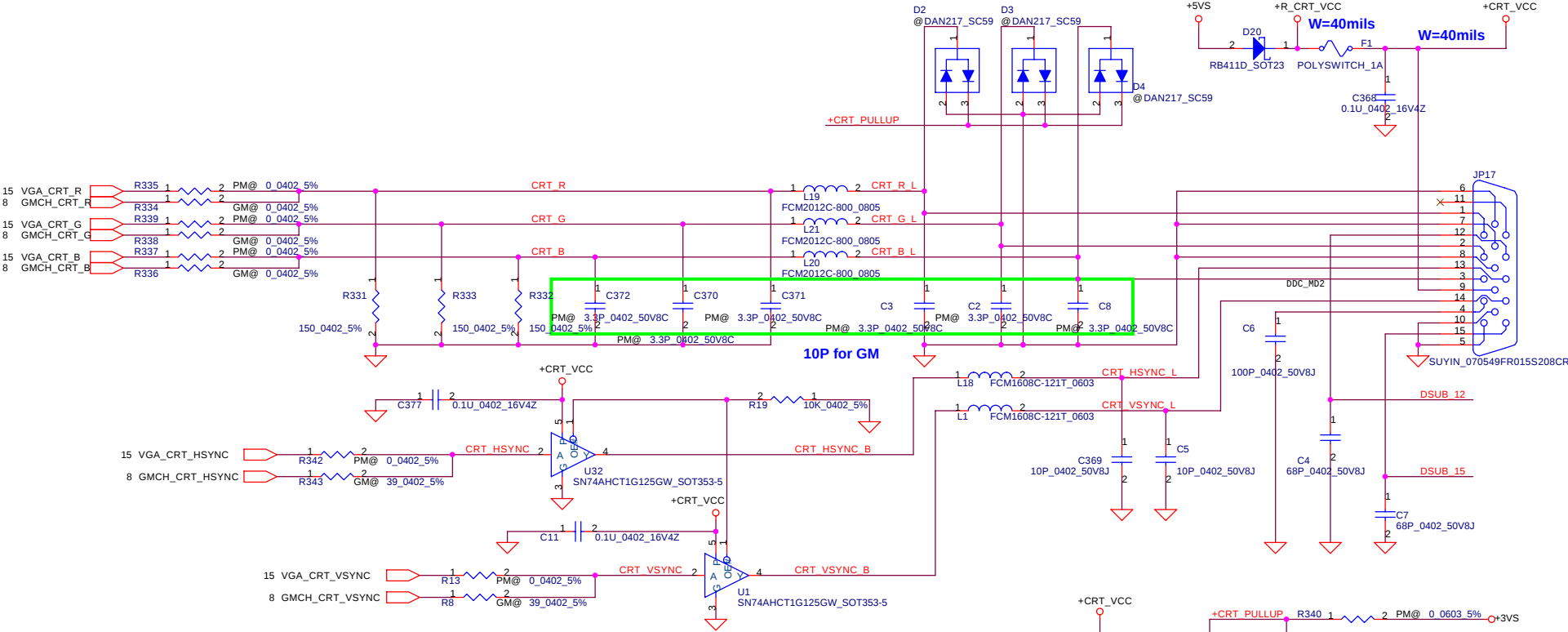


DIMM1 STD H:9.2mm (BOT)

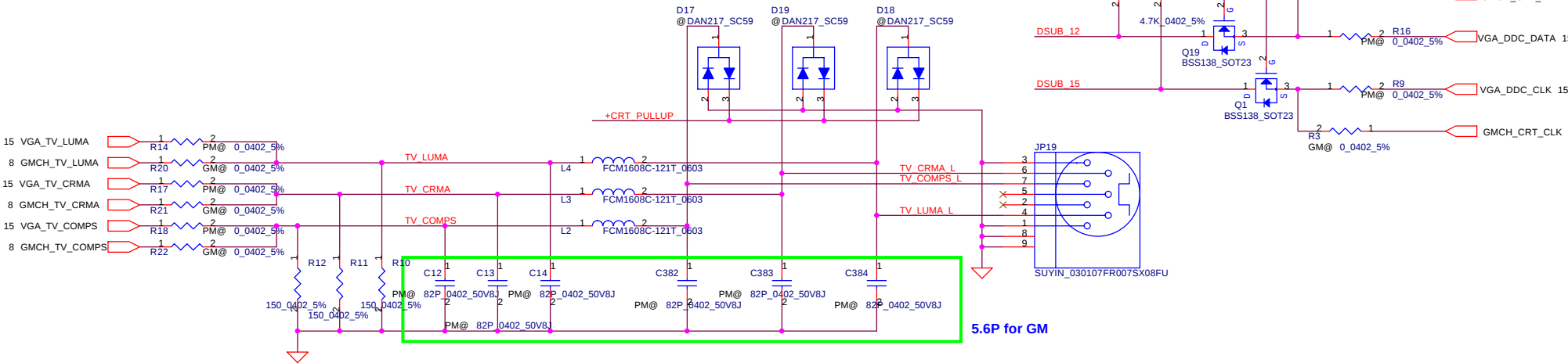


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CRT Connector

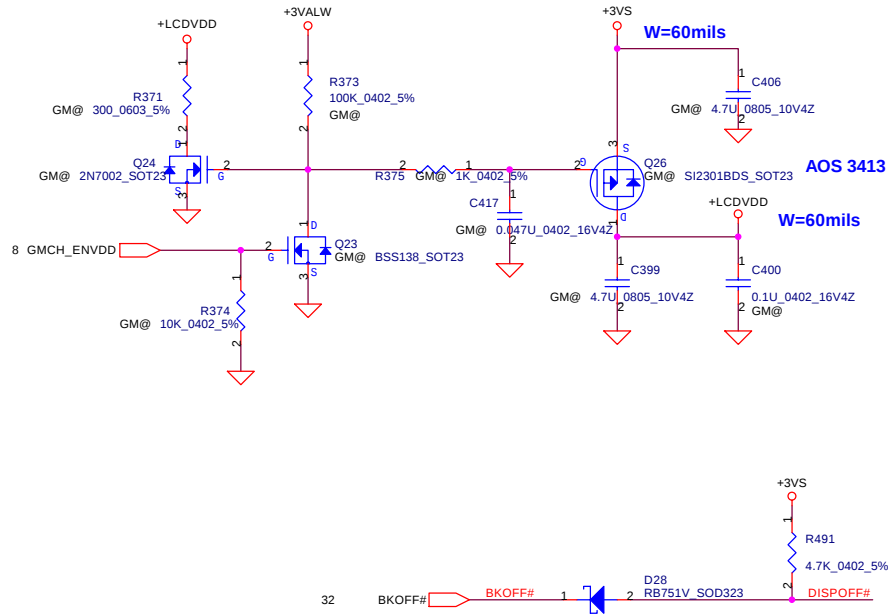


TV-OUT Conn.

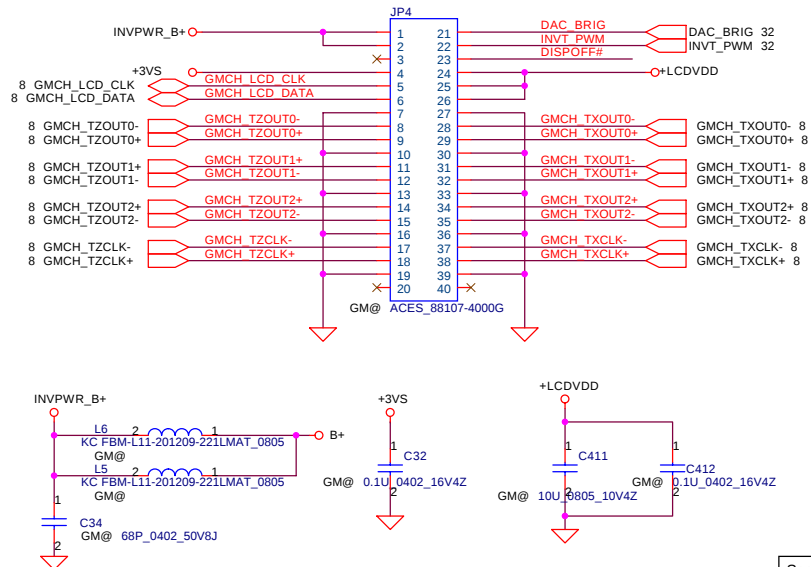


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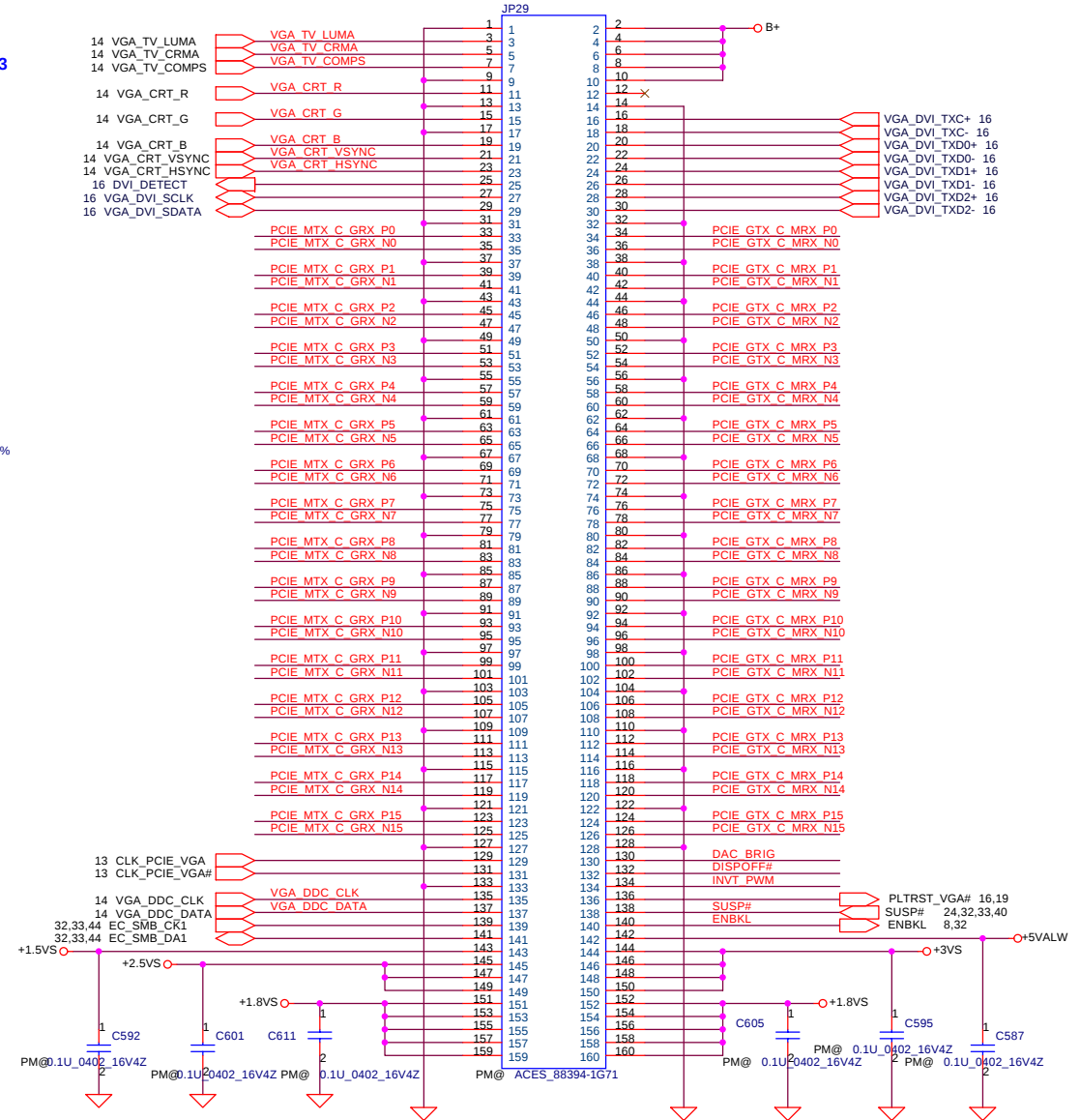
LCD POWER CIRCUIT



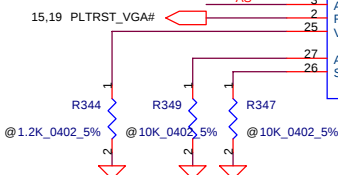
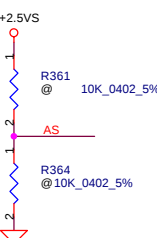
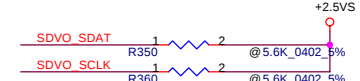
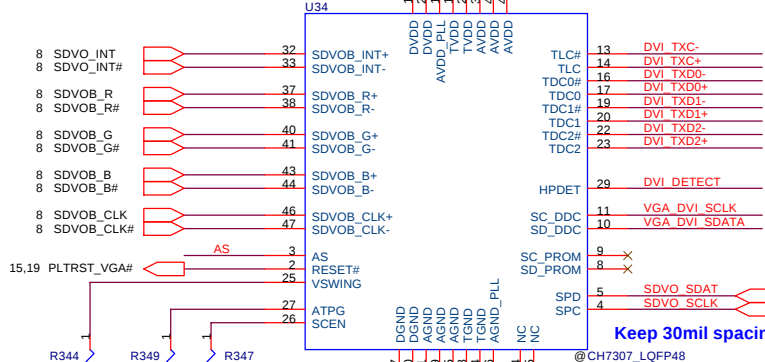
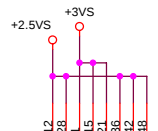
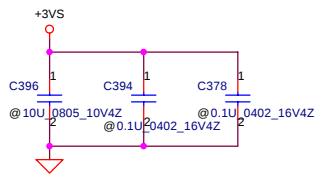
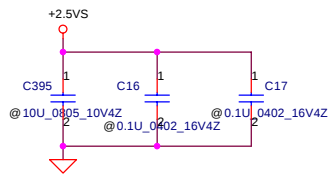
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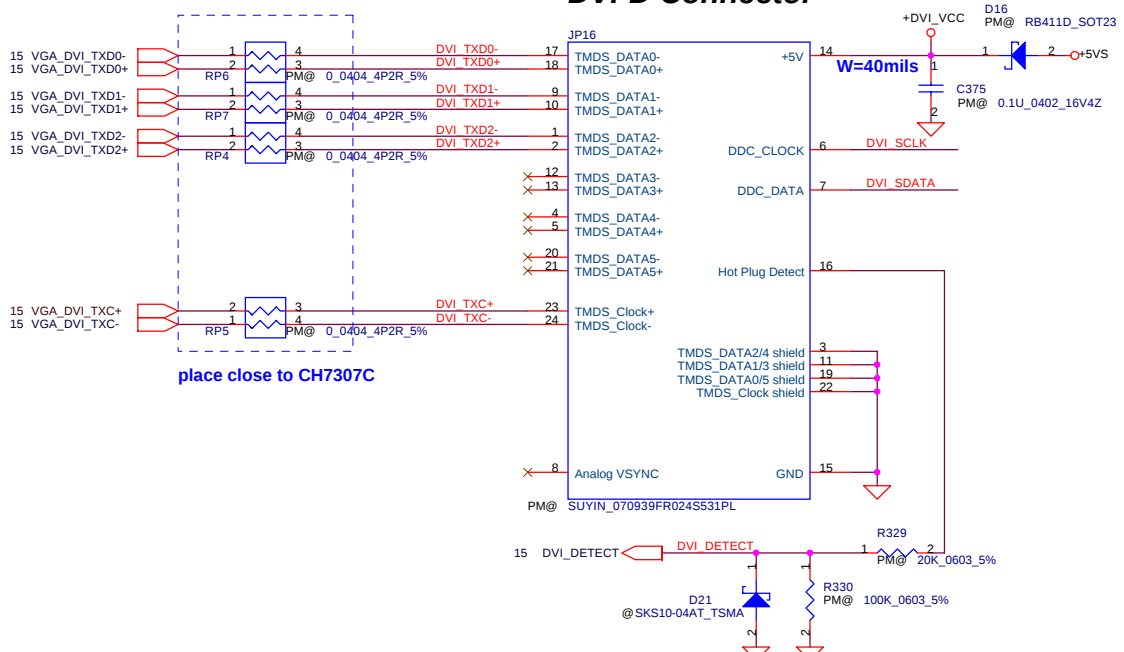
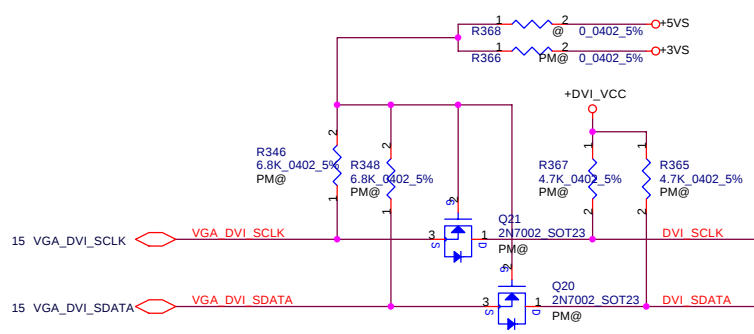
VGA BOARD Conn.



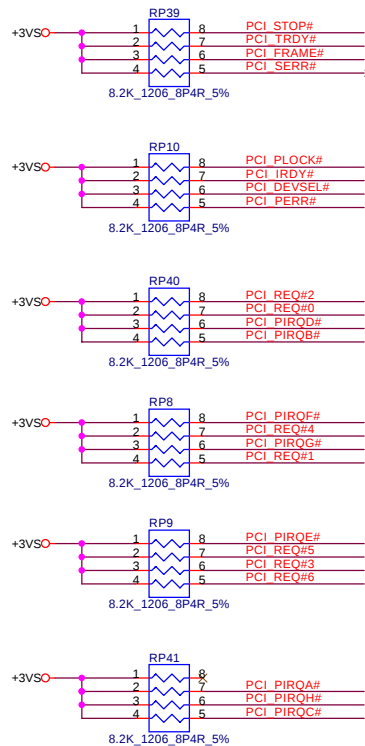
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DVI-D Connector



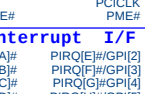
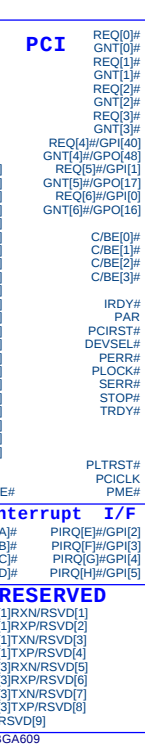
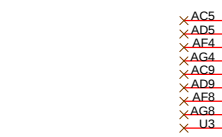
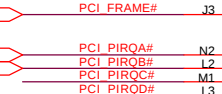
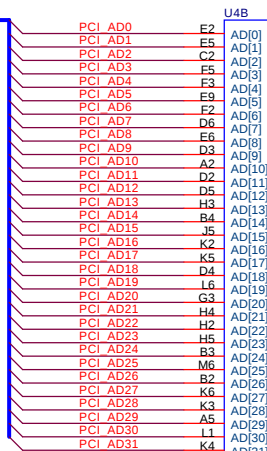
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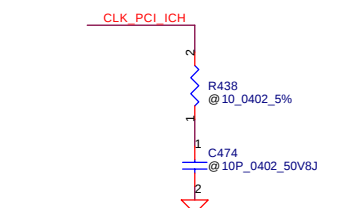
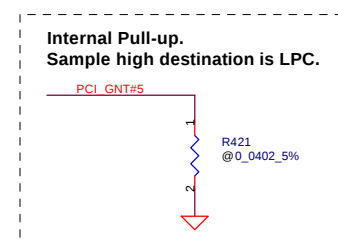
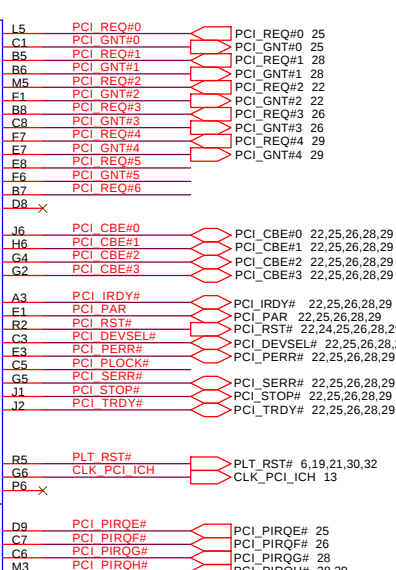
22,25,26,28,29 PCI_AD[0..31]

22,25,26,28,29 PCI_FRAME#

22,29 PCI_PIRQA#
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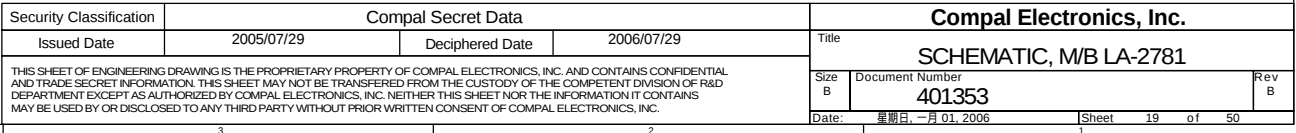
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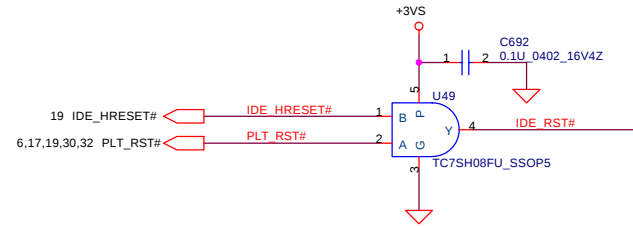
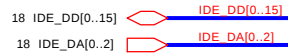
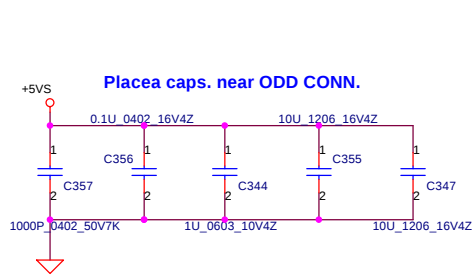


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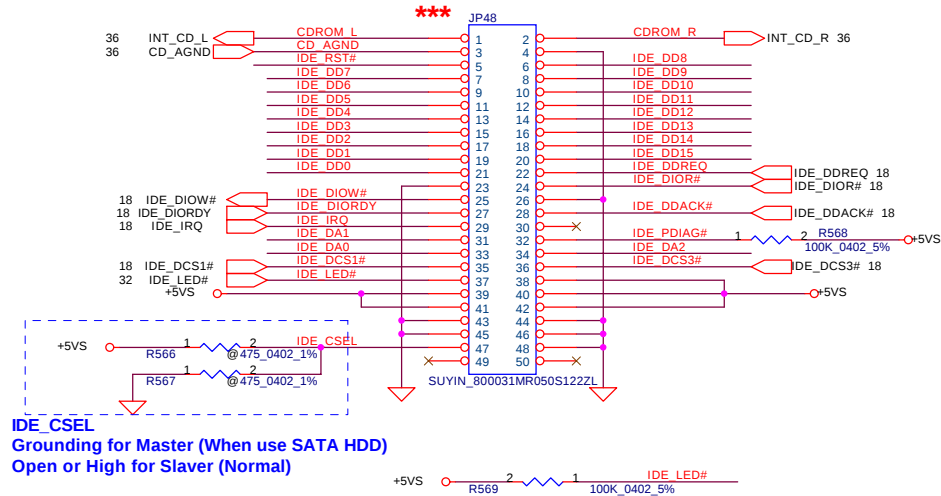


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					Date:	星期日, 一月 01, 2006		Sheet 18 of 50

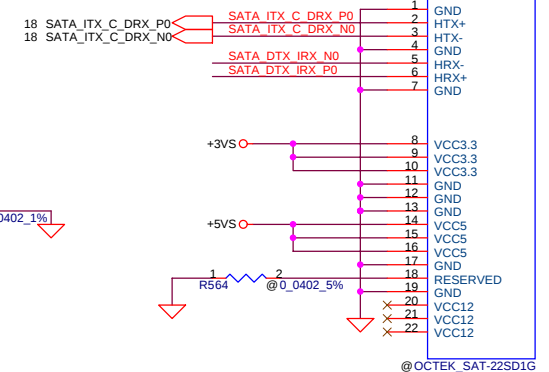
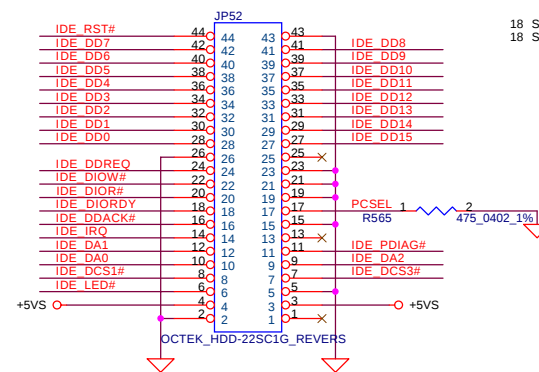
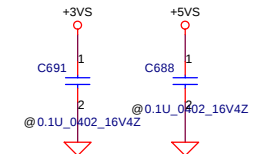
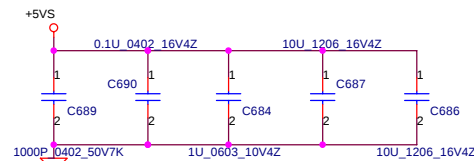
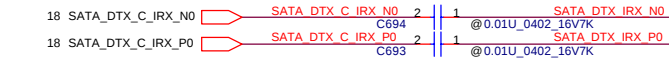




ODD Conn.

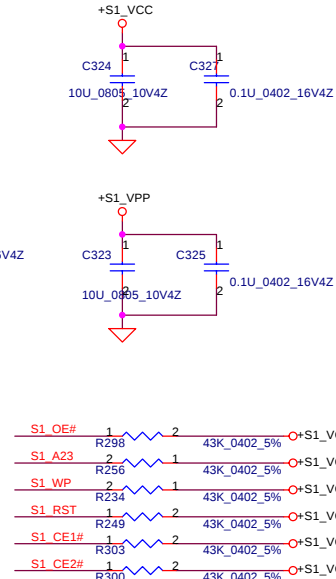
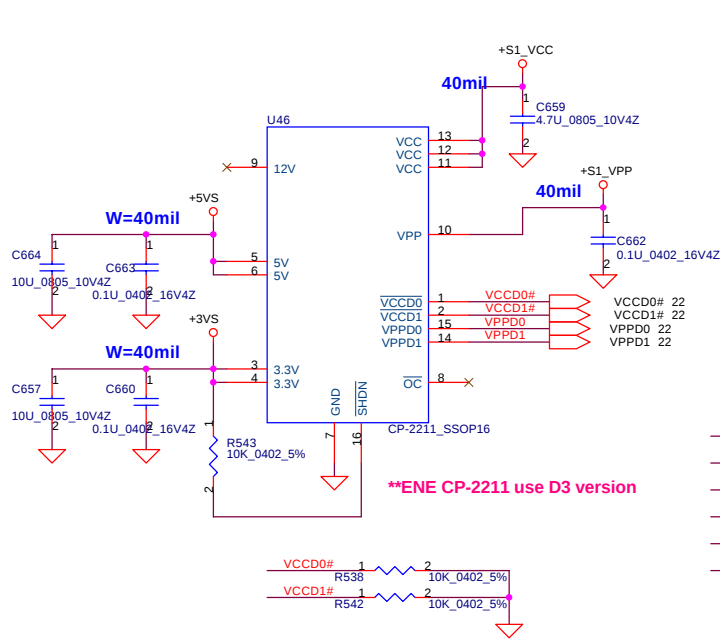


PATA/SATA HDD Conn.

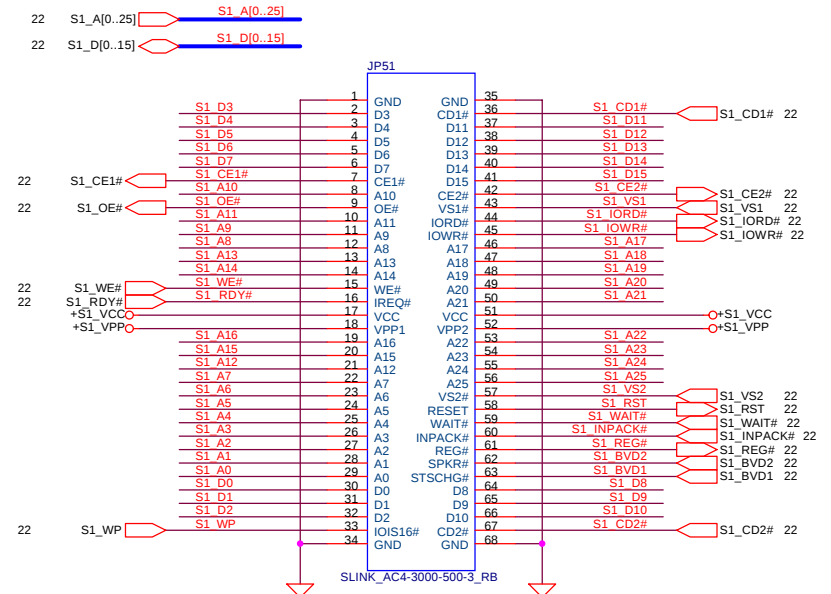


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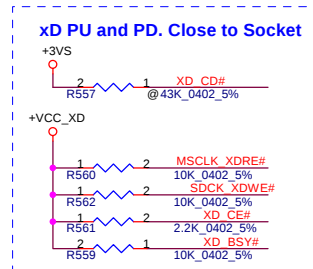
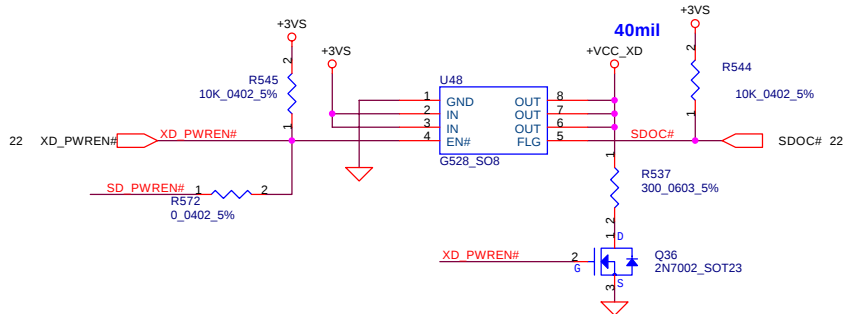
PCMCIA Power Control



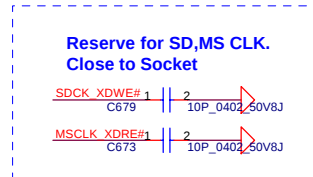
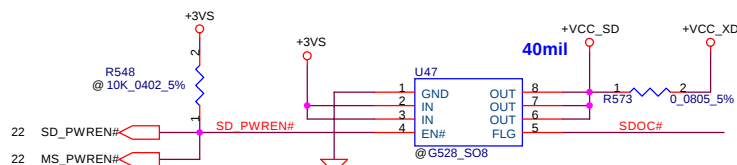
PCMCIA Socket



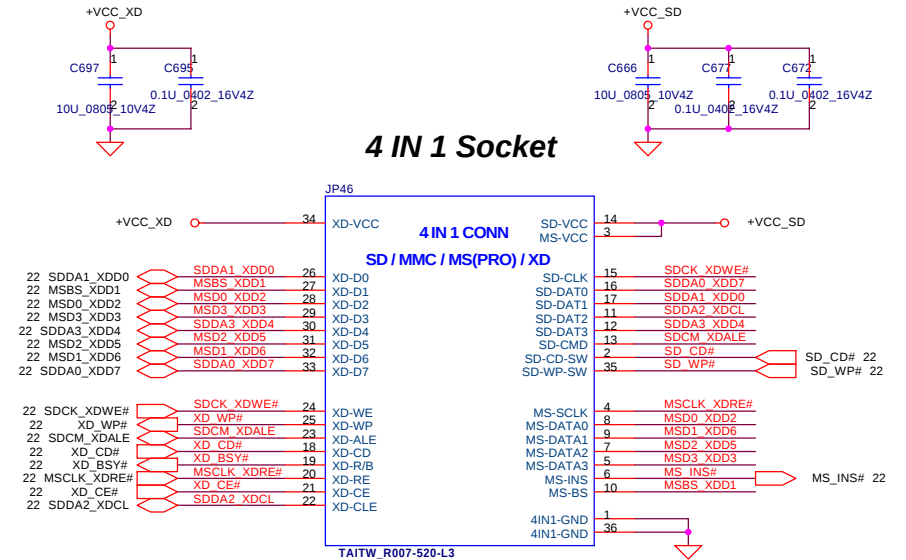
XD Power Control



SD/MS Power Control

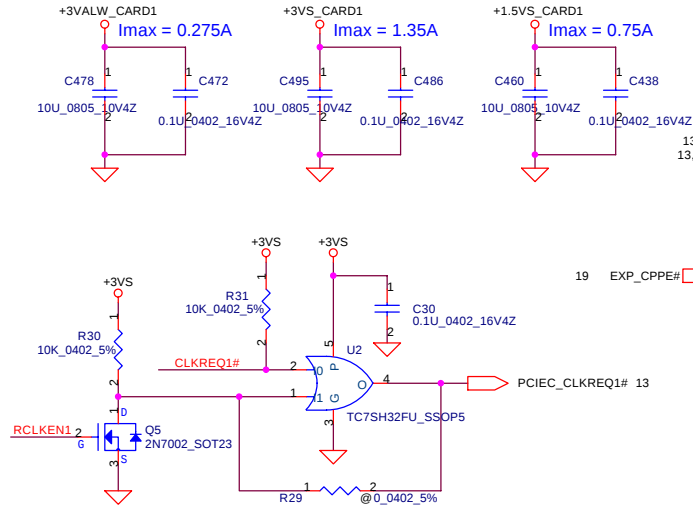
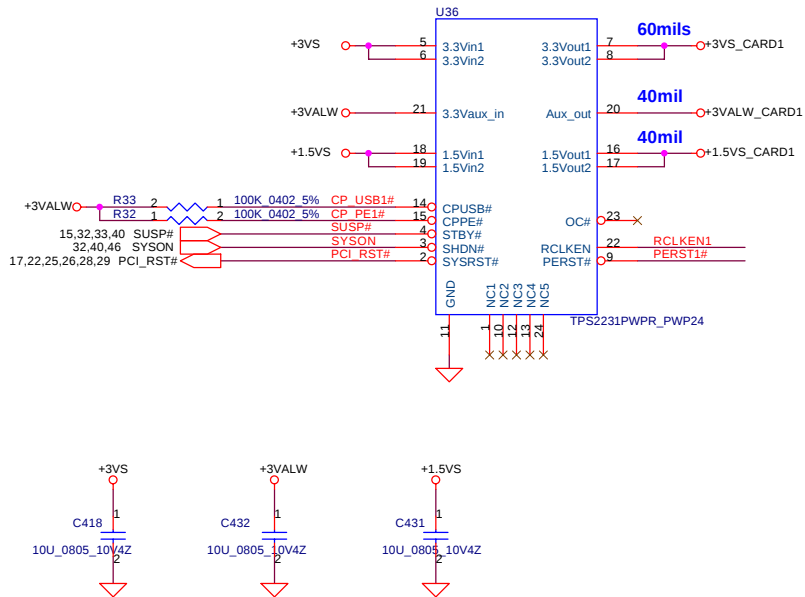


4 IN 1 Socket

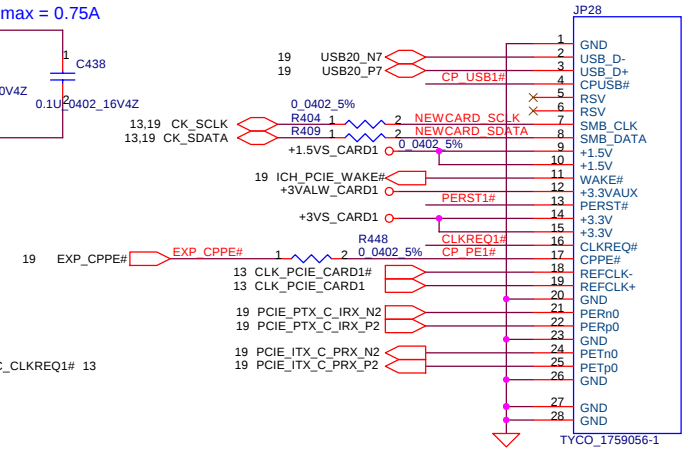


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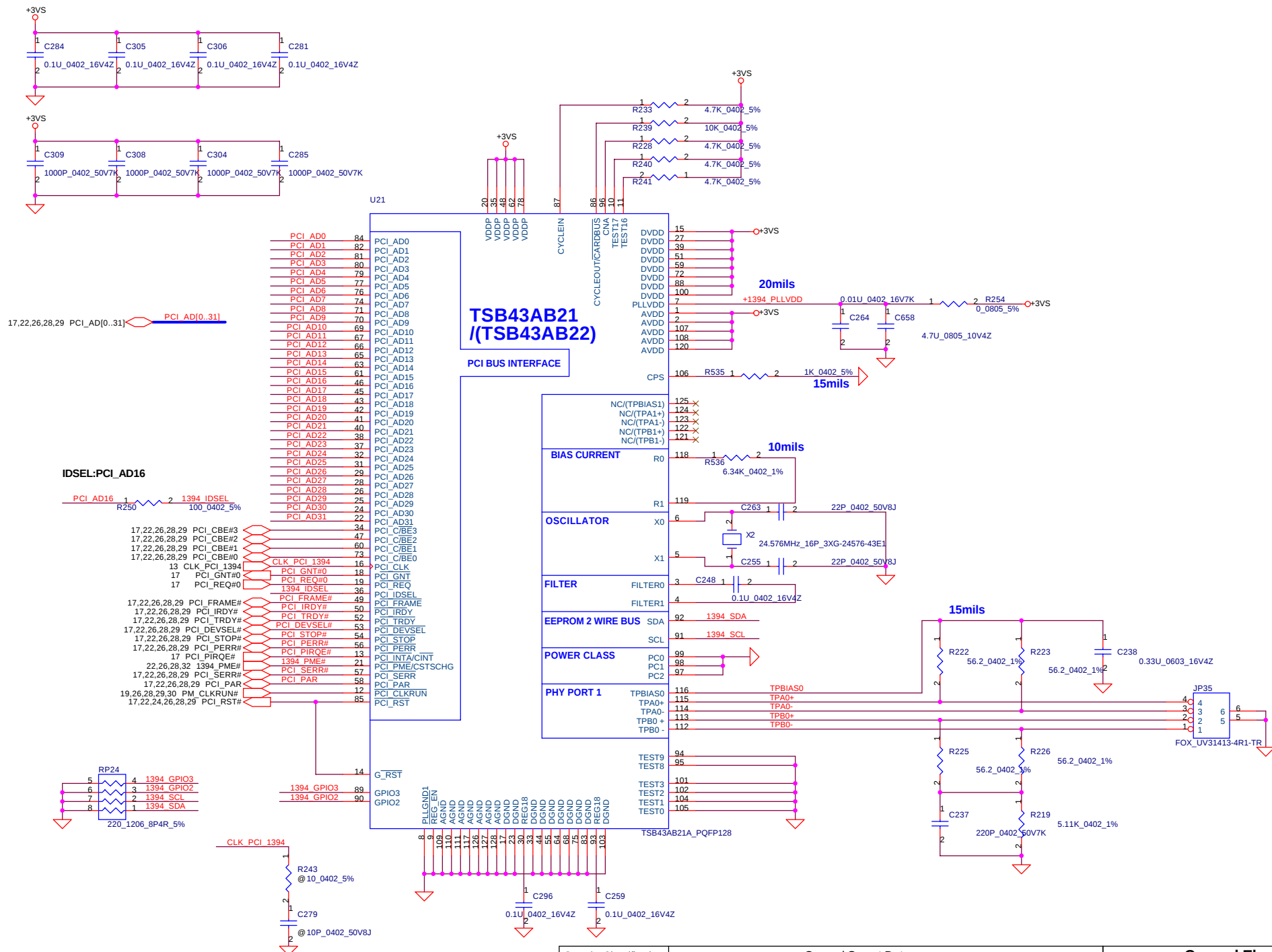
New Card Power Switch



New Card Socket (Left)



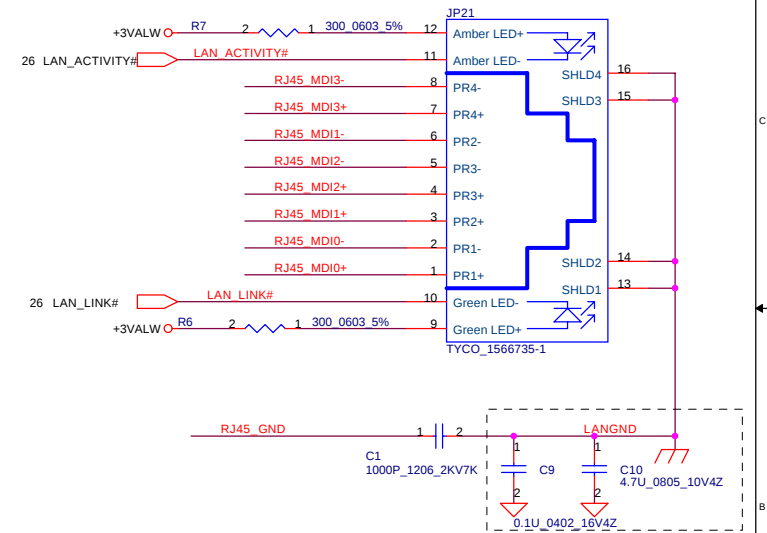
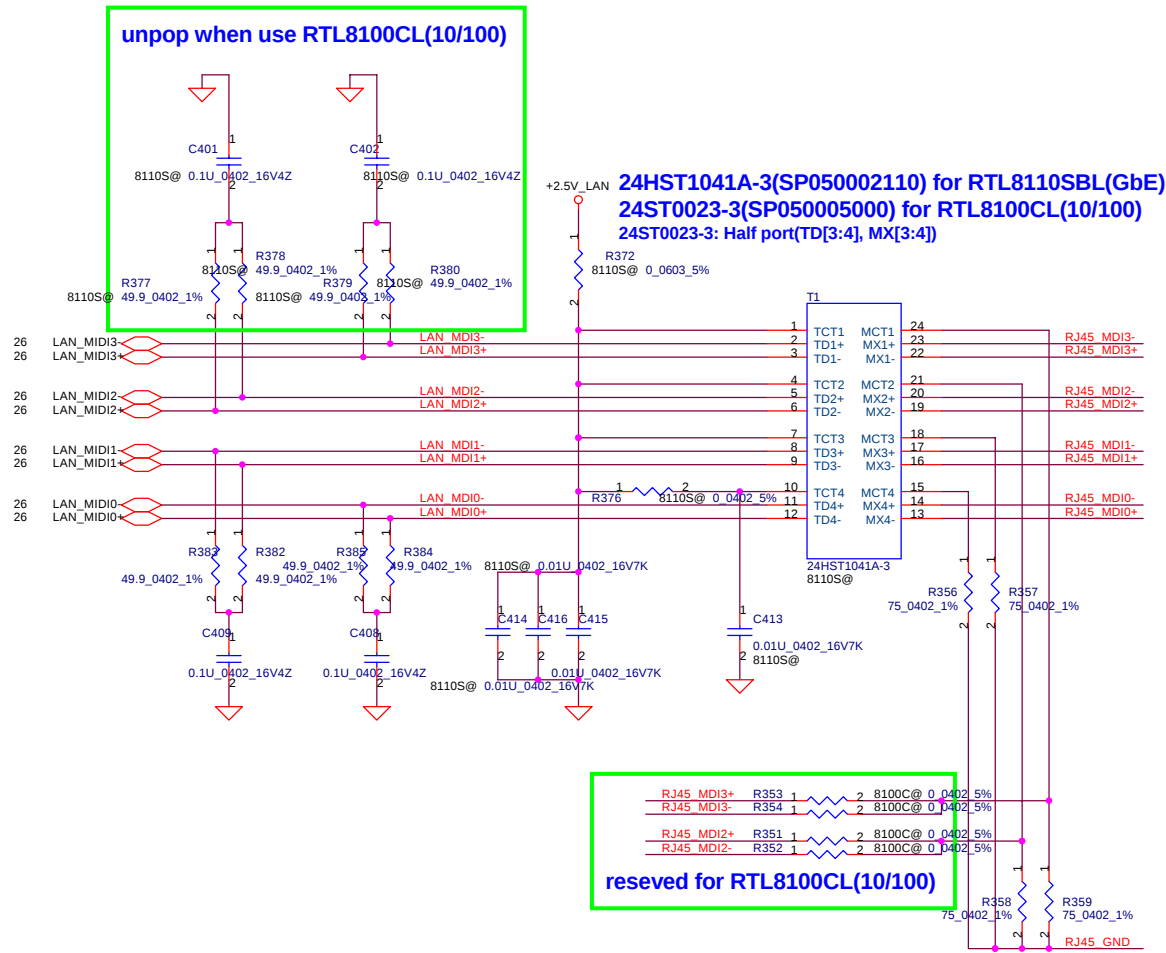
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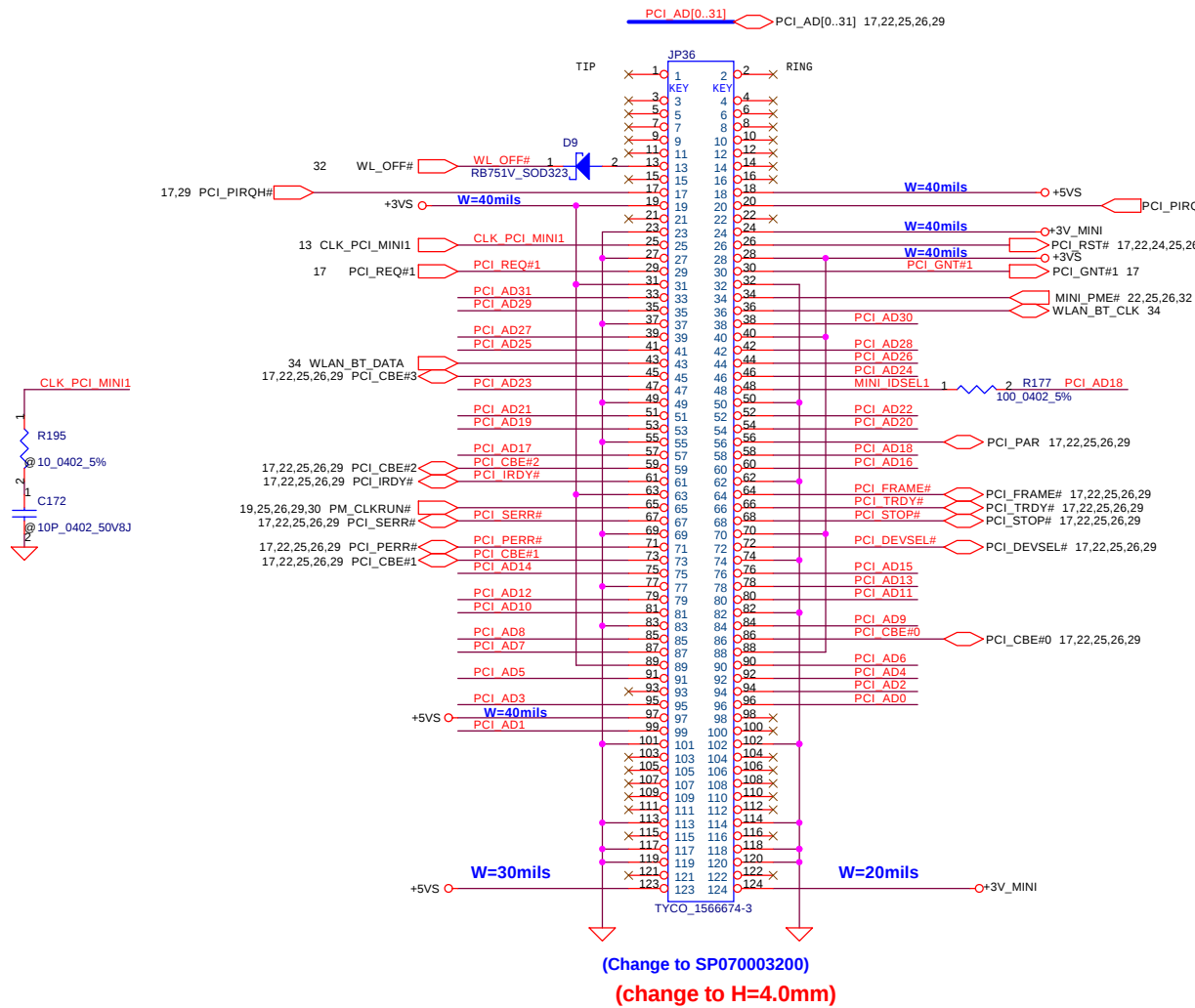
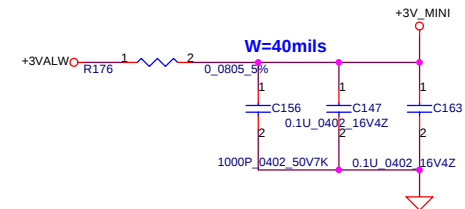
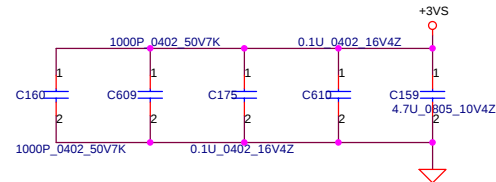
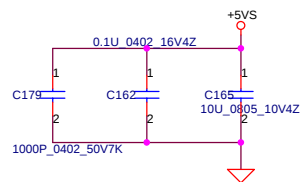
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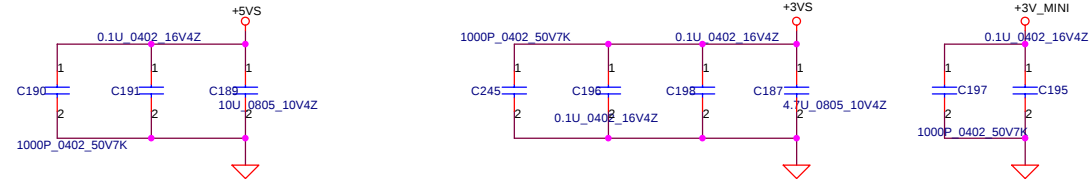
LAN RTL8110SBL/RTL8100CL



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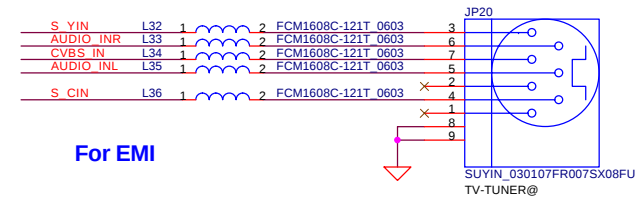


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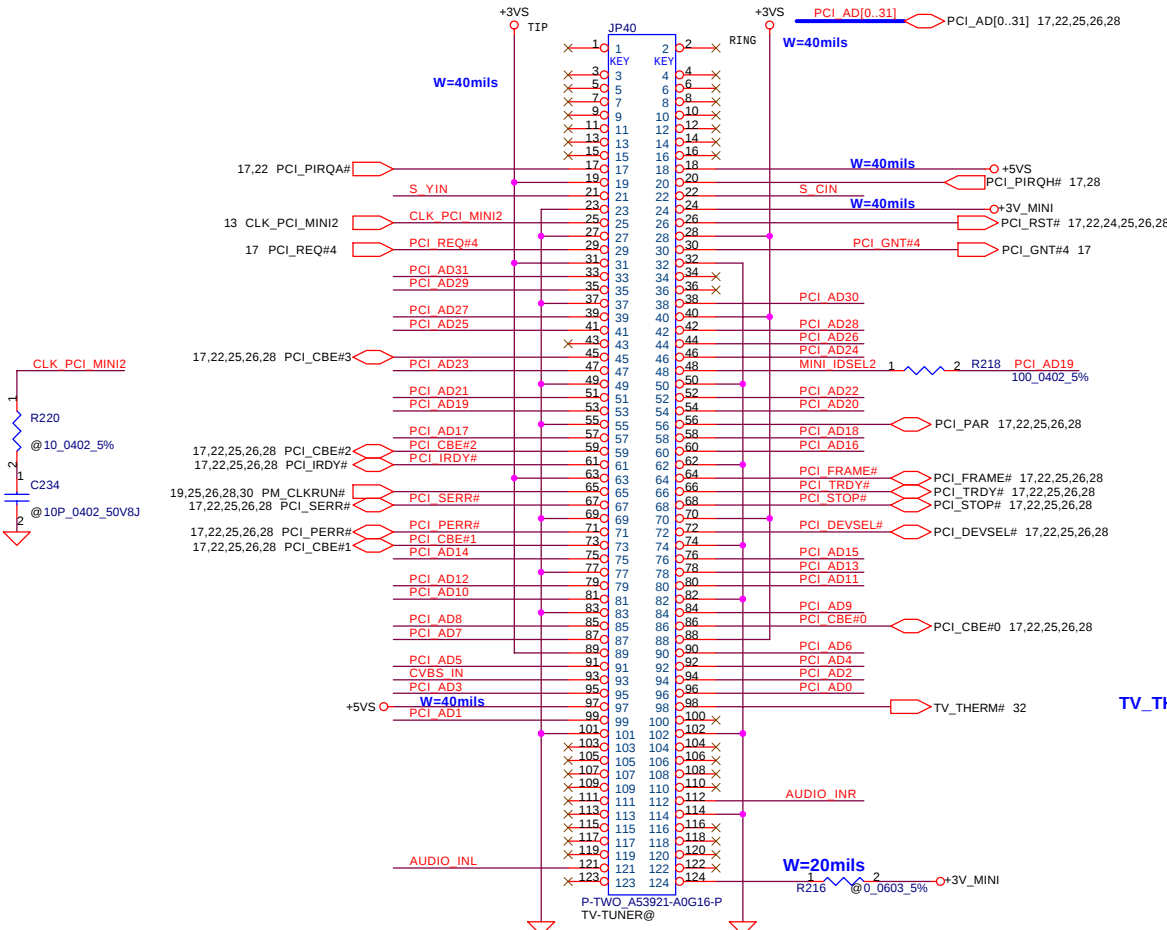
TV-Tuner

AV In



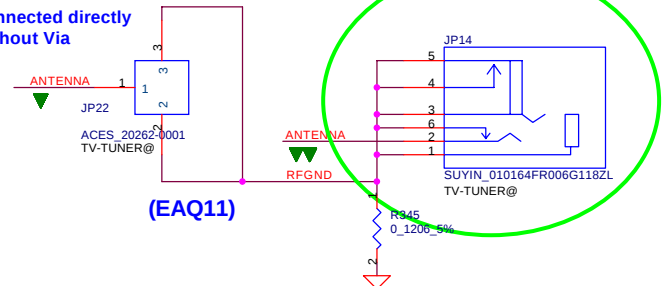
For EMI

- Acer TV-Tuner Design Guide Rev1.1
1. N/A
 2. N/A
 3. S-Video - Y
 4. S-Video - C
 5. Audio - Left
 6. Audio - Right
 7. CVBS



RF In

connected directly
without Via

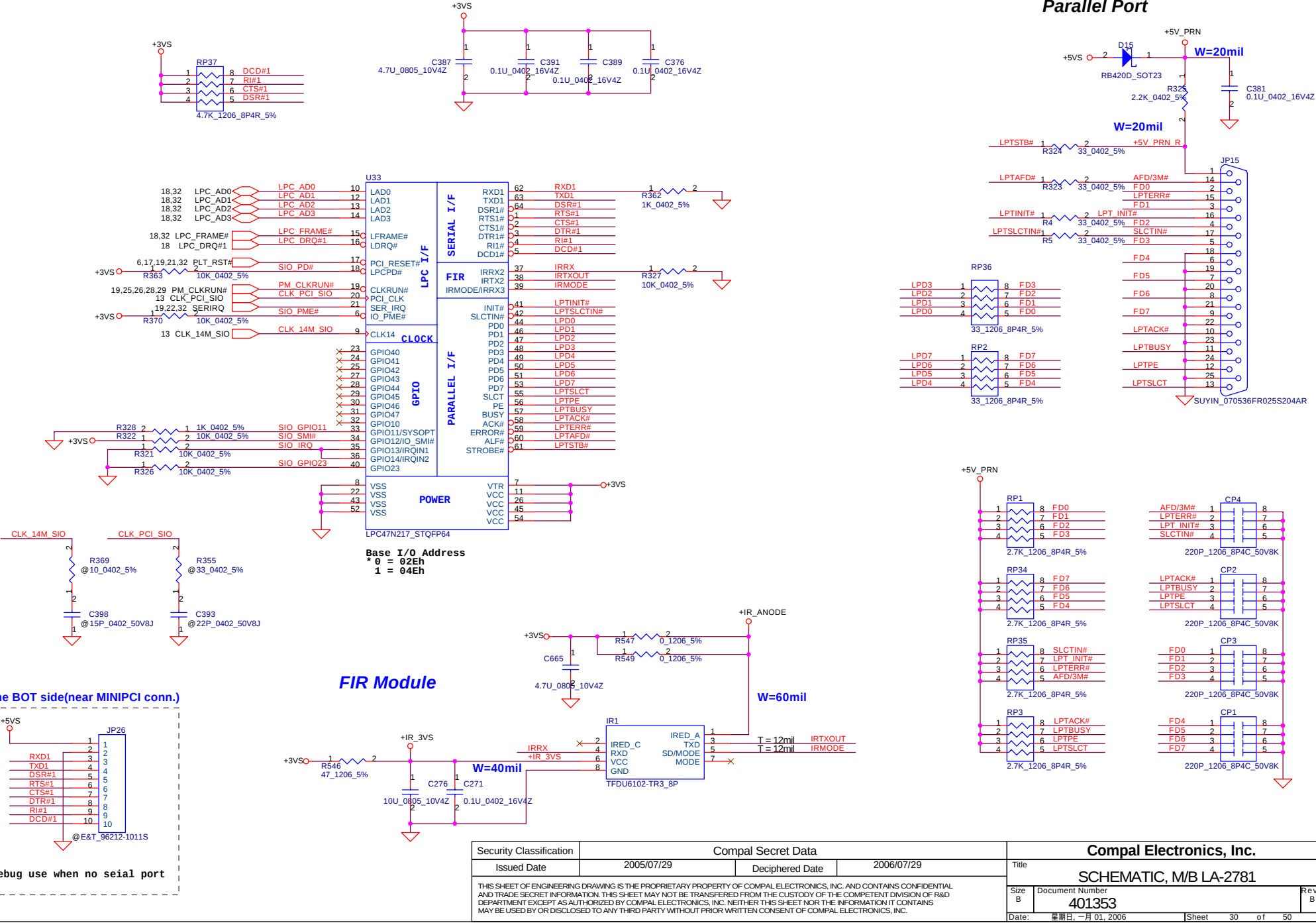


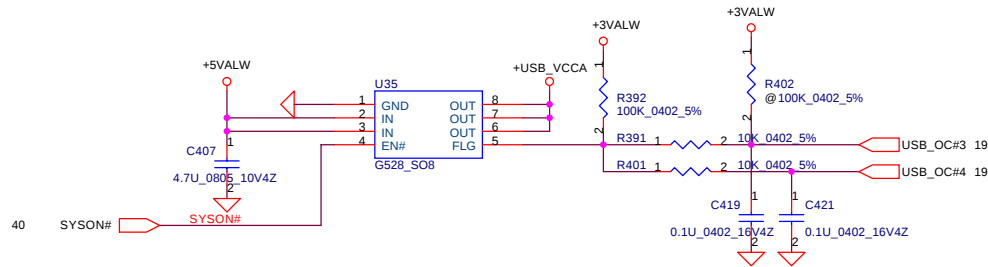
TV_THERM#: Normal High(+3VS),
Active Low

(EDL71 pin define)
(For TV-Tuner change to H=9.2mm)

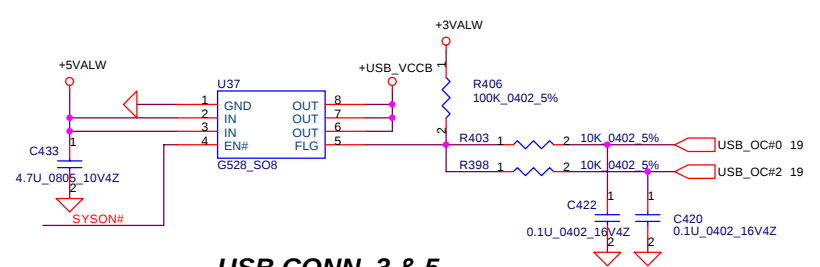
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SUPER I/O SMC LPC47N217

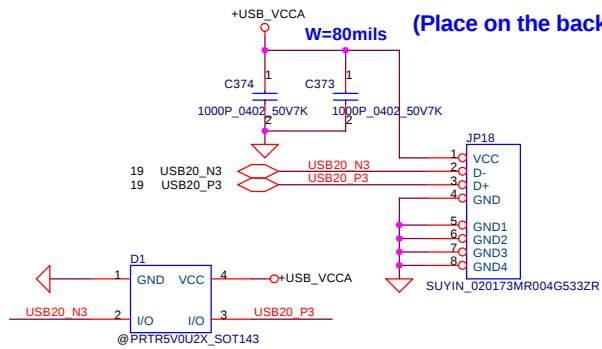
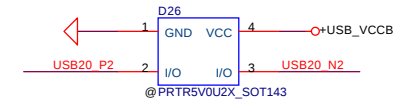
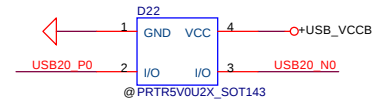
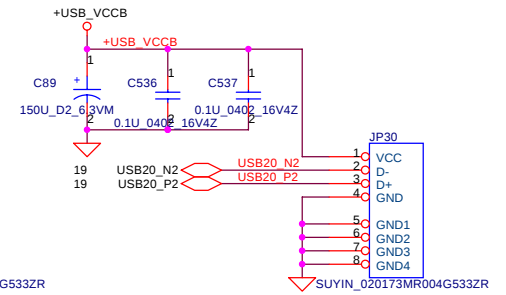
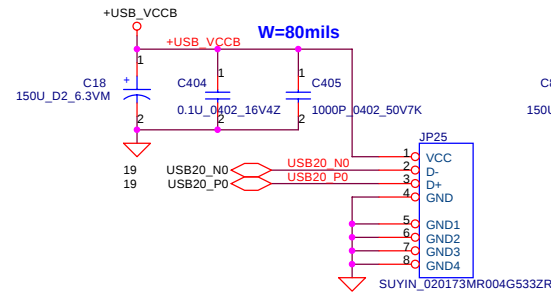
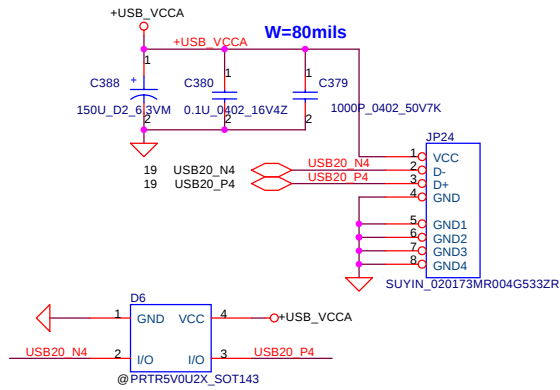




USB CONN. 1 & 2
(Place on the left-back side)

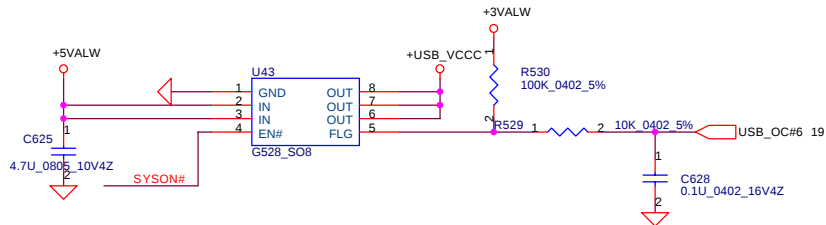
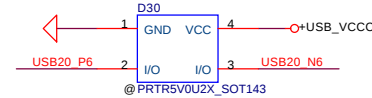
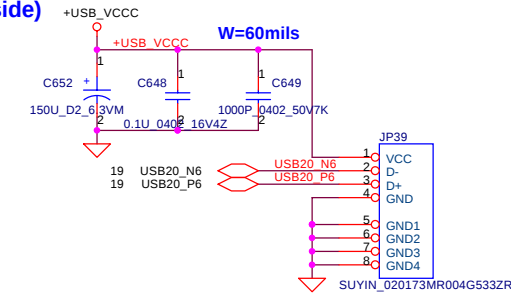


USB CONN. 3 & 5
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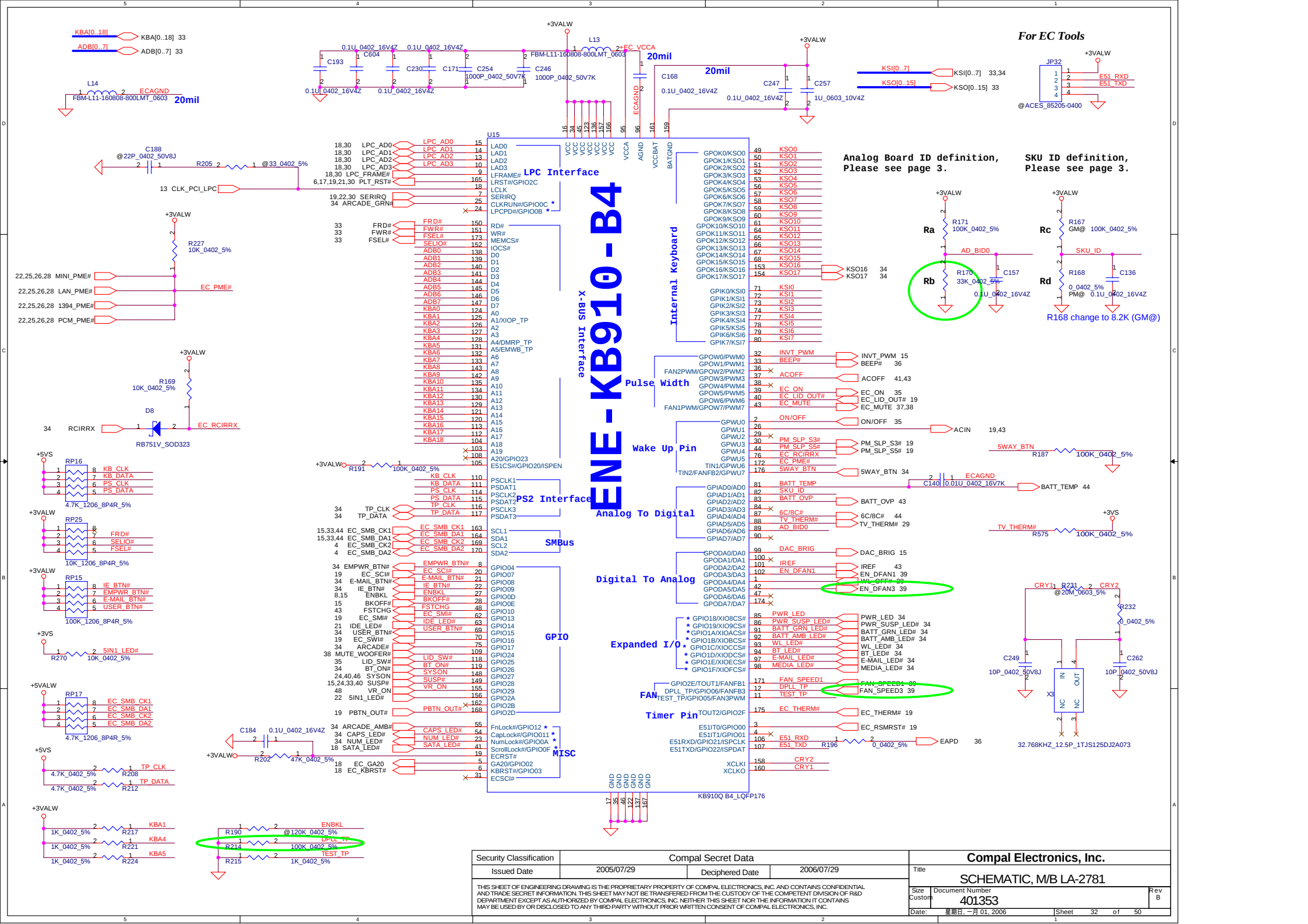


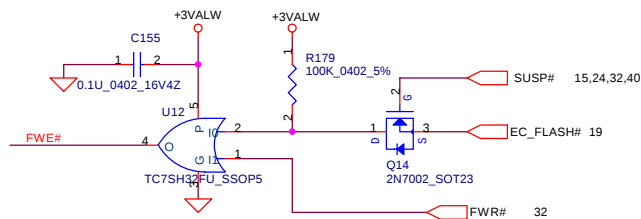
(Place on the back side)

USB CONN. 5
(Place on the left-front side)



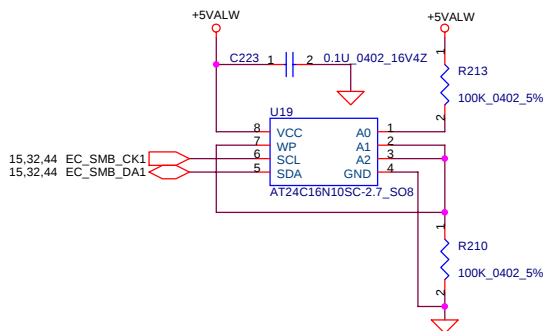
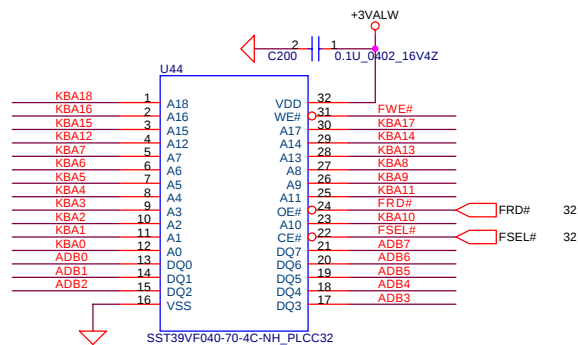
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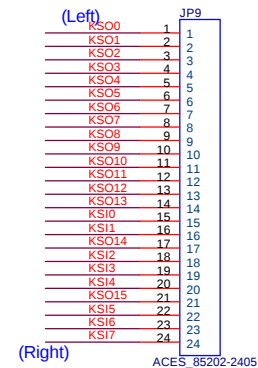
512KB Flash ROM

32 KBA[0..18] KBA[0..18]
32 ADB[0..7] ADB[0..7]

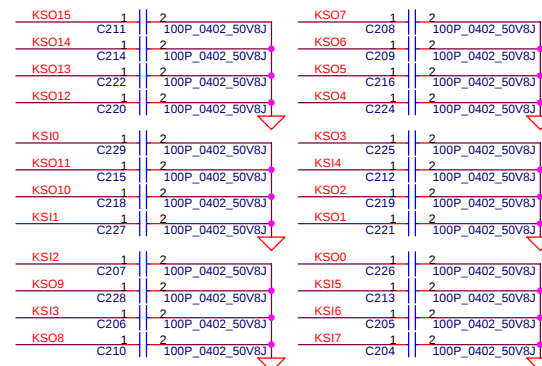


INT_KBD Conn.

KSI[0..7] KSI[0..7] 32,34
KSO[0..15] KSO[0..15] 32



ECQ60 for 17"



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[illegible]

Pinout diagram for the ACES_85201-2405 connector. The diagram shows 24 pins connected to various components. Pins 1 and 2 are labeled +5VALWO and +5VS. Pins 3-4 are BATT_AMB_LED# and BATT_GRN_LED#. Pins 5-6 are PWR_LED# and PWR_SUSP_LED#. Pins 7-8 are BT_LED# and WL_LED#. Pins 9-10 are KS017 and KS017. Pins 11-12 are KS13 and KS14. Pins 13-14 are 5WAY_BTN and RCIRRX. Pins 15-16 are KS10 and KS11. Pins 17-18 are KS12 and KS15. Pins 19-20 are KSO16 and ARCADE_BTN#. Pins 21-22 are ARCADE_GRN# and ARCADE_AMB#. Pins 23-24 are ACES_85201-2405. The diagram is labeled JP13 at the top right.

TP_DATA
TP_CLK

TP DATA
TP CLK

C712 2
100P_0402_50VB3

C712 2
100P_0402_50VB3

For EMI

JP12
1
2
3
4
5
6
ACES_85201-0605

+5VPS

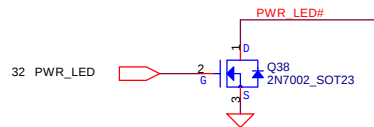
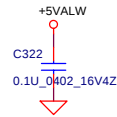
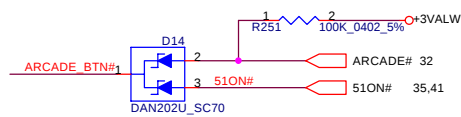
C676
0.1U_0402_16V4Z

Diagram illustrating the pin configuration for the ACES_8801-1610 module. The module is connected to a 16-pin connector (JP1) and a +5V power source.

Pin Connections:

- Pin 1: +5V
- Pin 2: (Marked with a red X)
- Pin 3: CAPS_LED#
- Pin 4: NUM_LED#
- Pin 5: MEDIA_LED#
- Pin 6: E-MAIL_LED#
- Pin 7: ON/OFFBTN#
- Pin 8: PWR_LED#
- Pin 9: EMPWR_BTN# 32
- Pin 10: IE_BTN# 32
- Pin 11: E-MAIL_BTN# 32
- Pin 12: USER_BTN# 32
- Pin 13: SVALW
- Pin 14: +5V
- Pin 15: +5V
- Pin 16: +5V

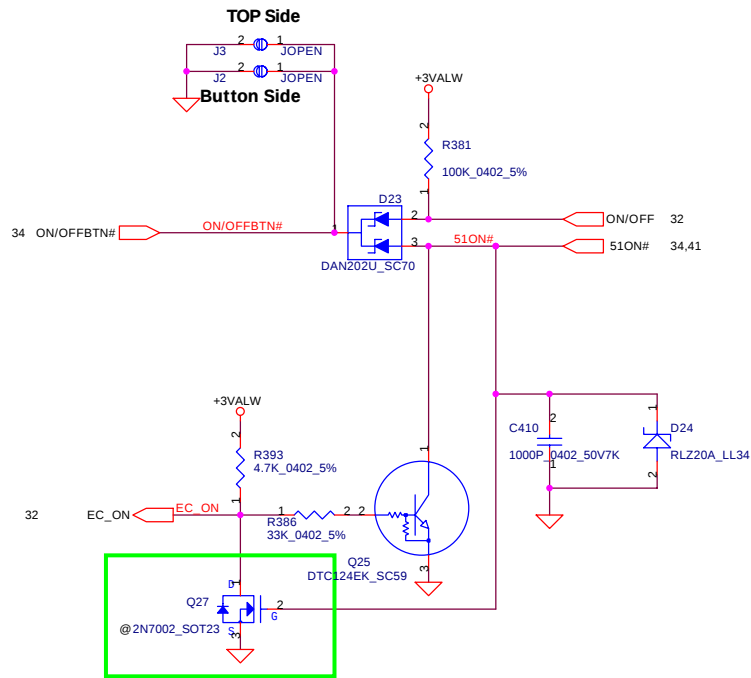
Module Label: ACES_8801-1610



	KSO16	KSO17
KSI0	VOL_UP	LEFT
KSI1	RIGHT	VOL_DOWN
KSI2	PLAY	ENTER
KSI3	STOP	BT_EN#
KSI4	NEXT	WL_EN#
KSI5	REV	

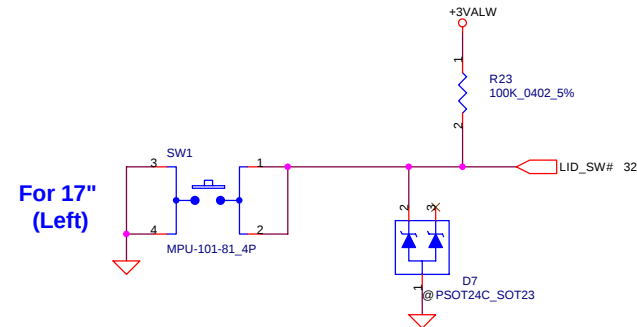
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ON/OFF switch

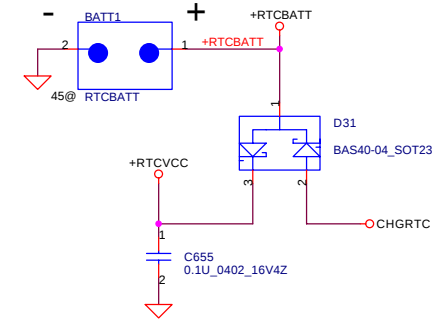


For Remove Control Issue

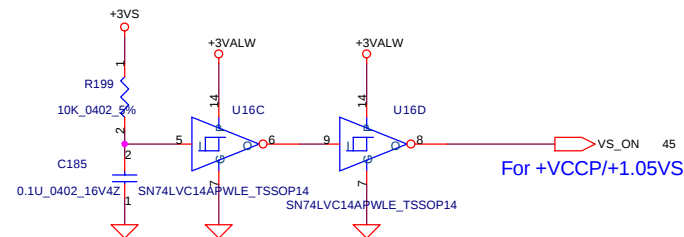
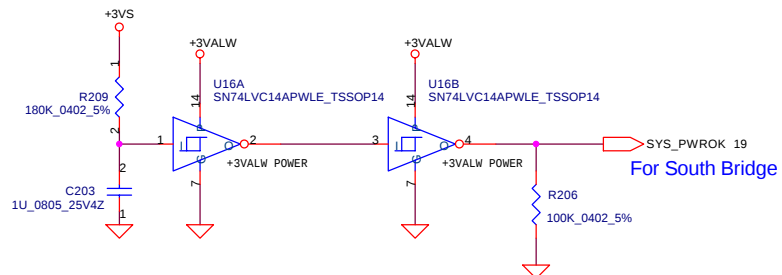
Lid Switch



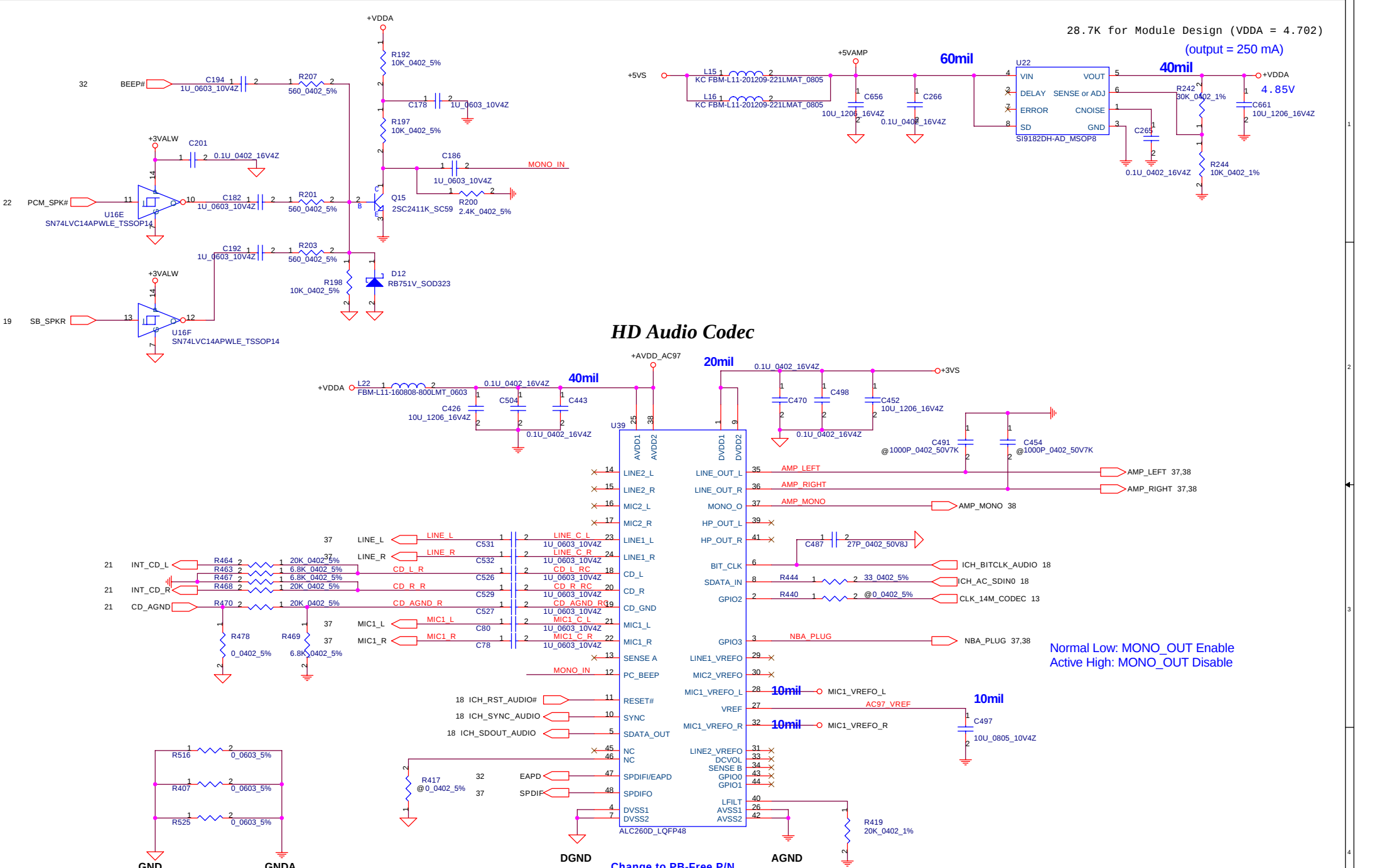
RTC Battery



Power ON Circuit



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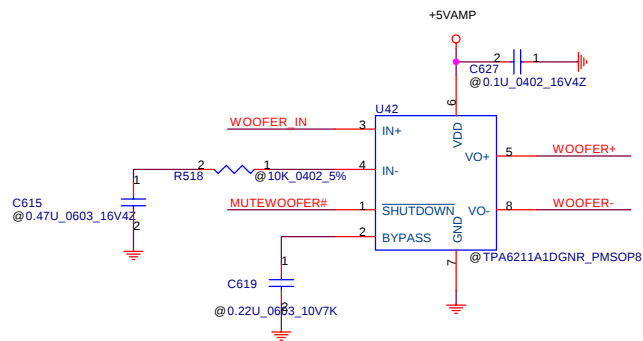
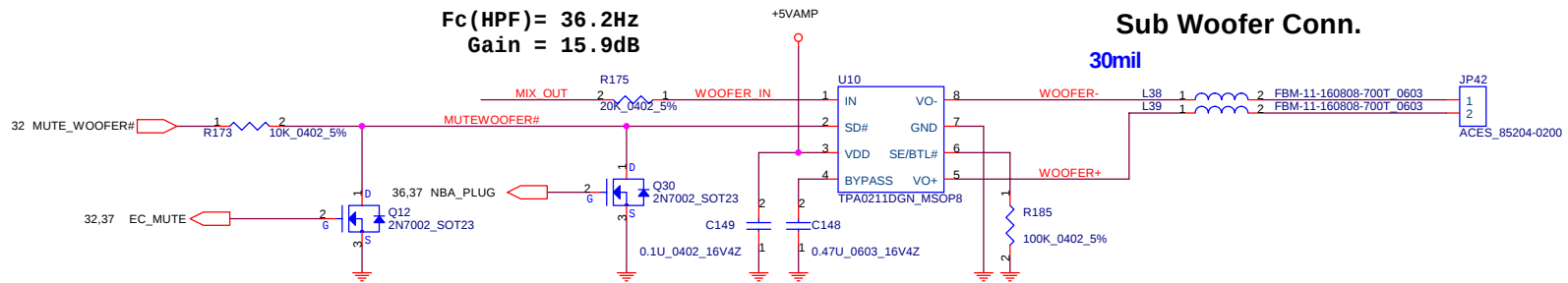
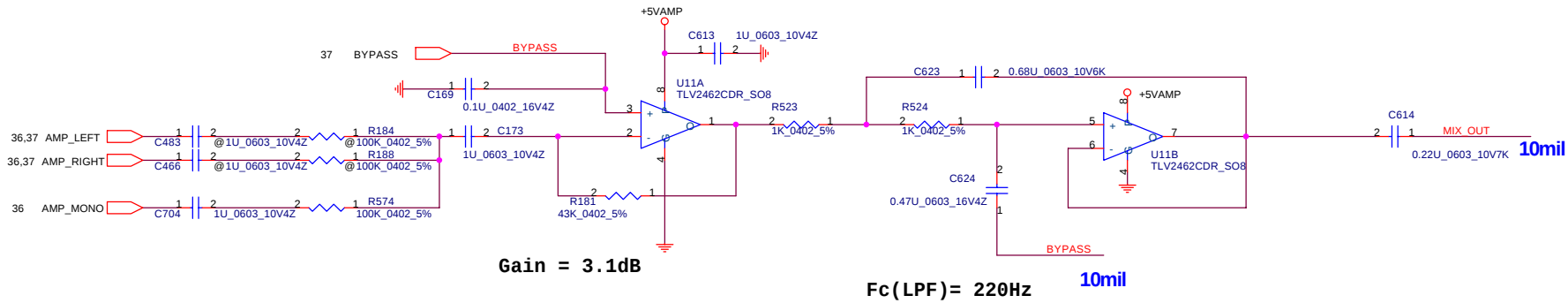
HD Audio Codec

28.7K for Module Design (VDDA = 4.702)
(output = 250 mA)
4.85V

Normal Low: MONO_OUT Enable
Active High: MONO_OUT Disable

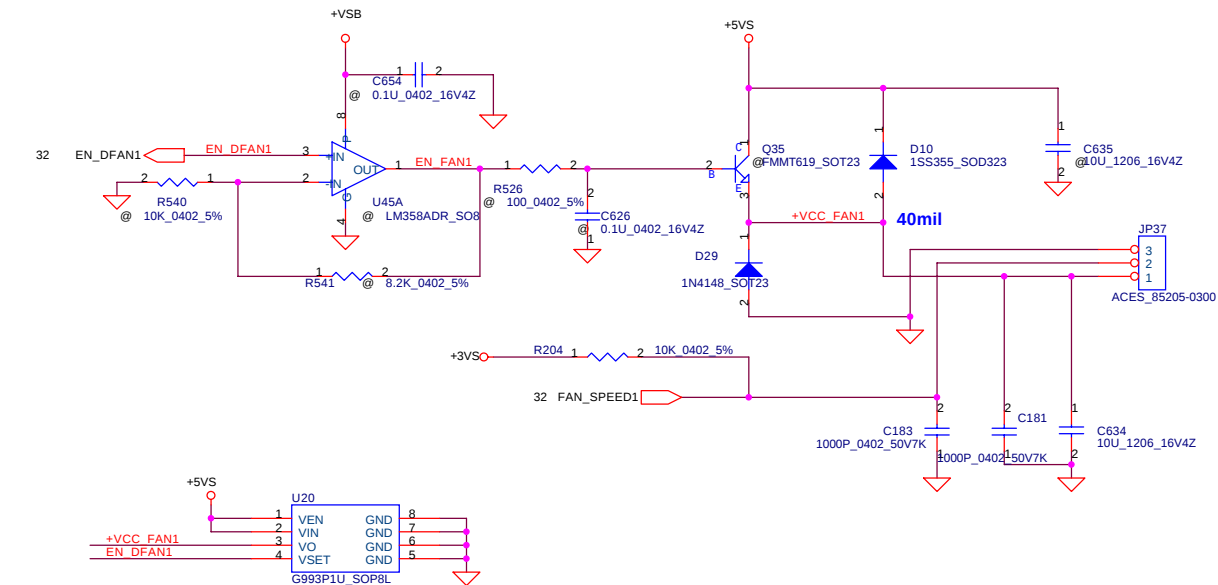
Change to PB-Free P/N

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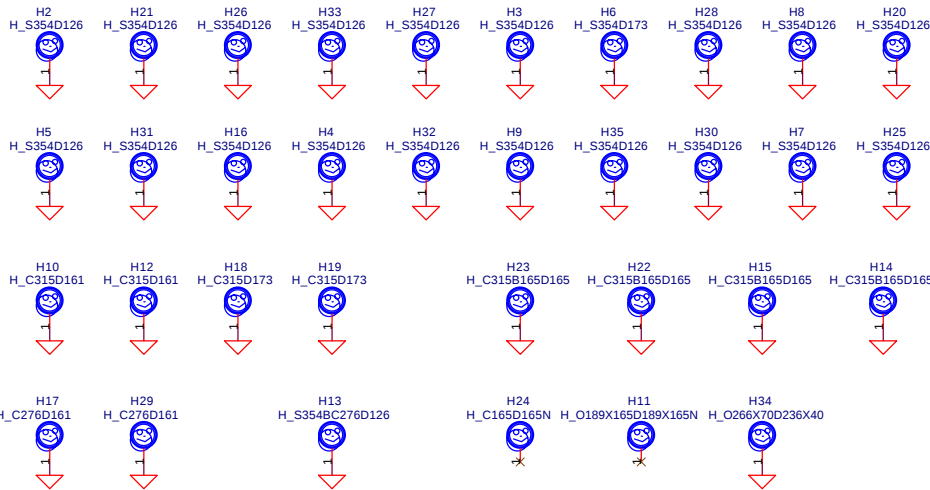


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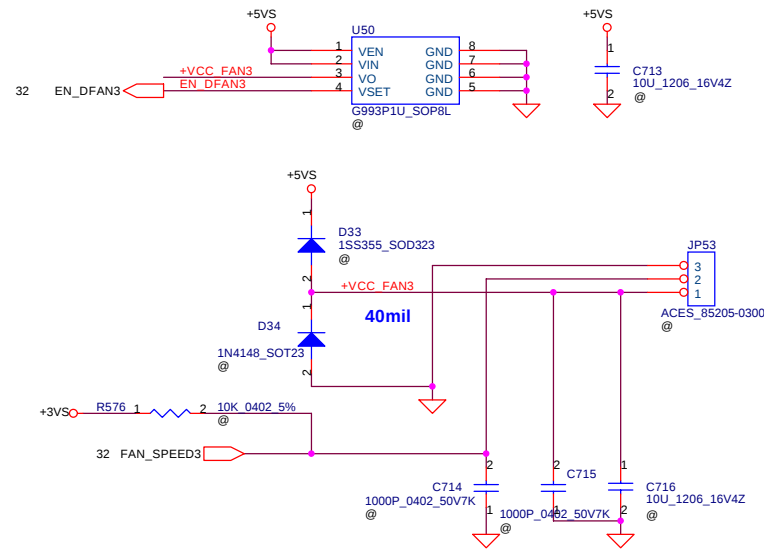
FAN Conn



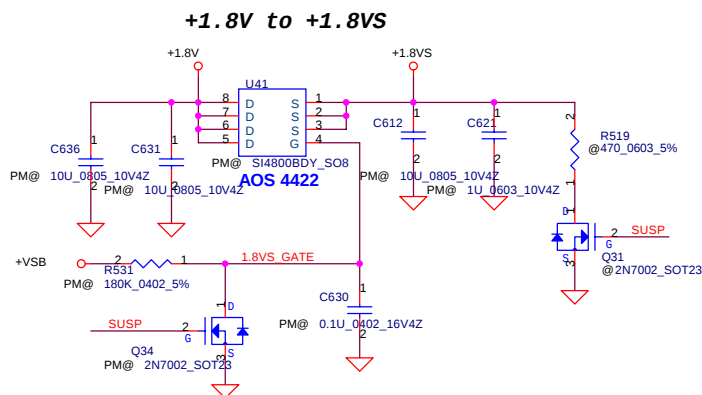
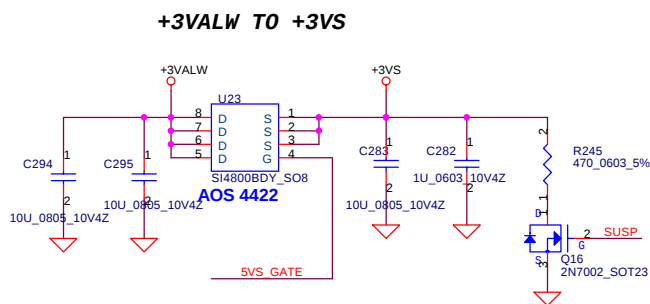
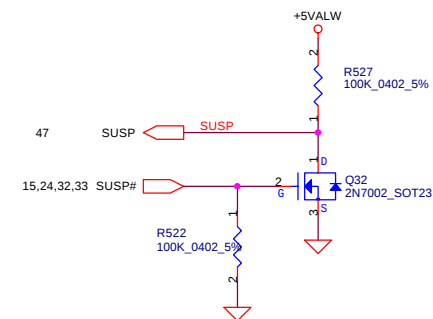
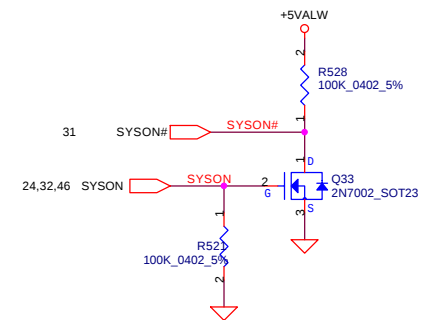
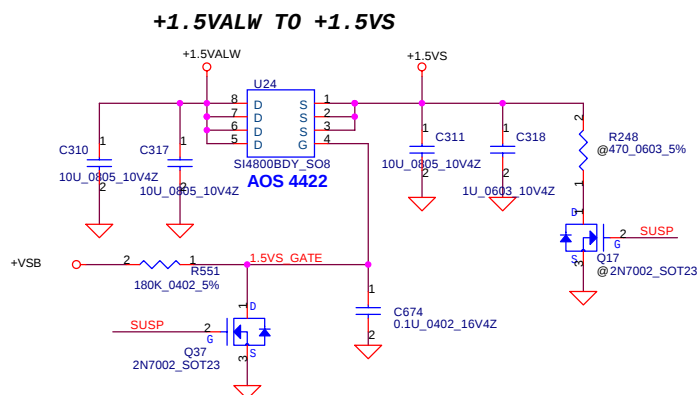
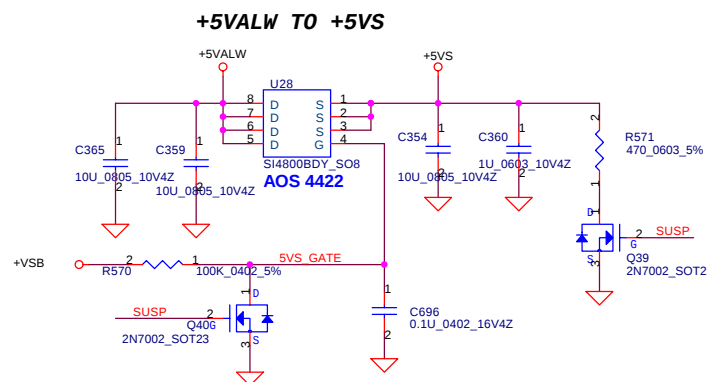
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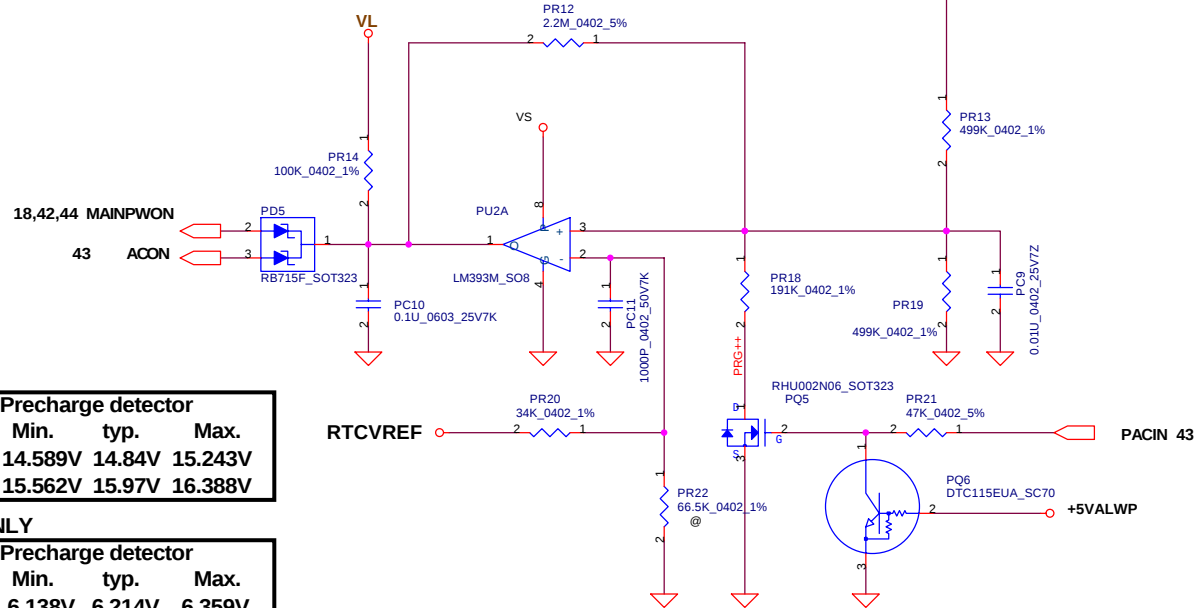
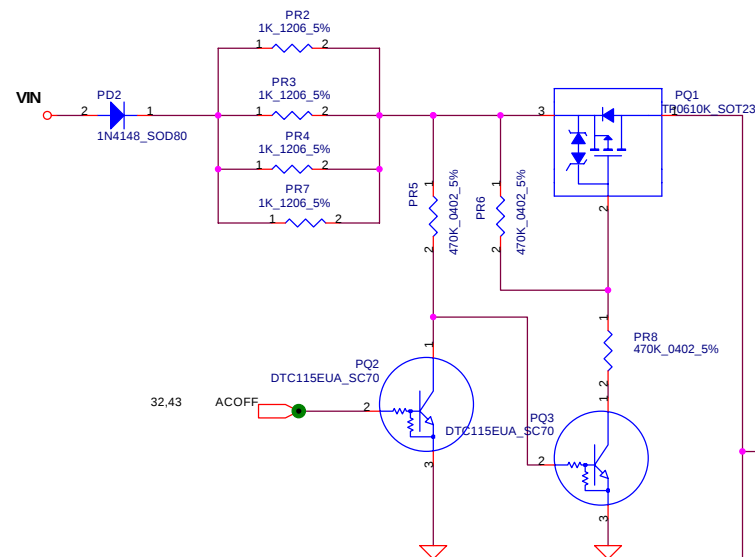
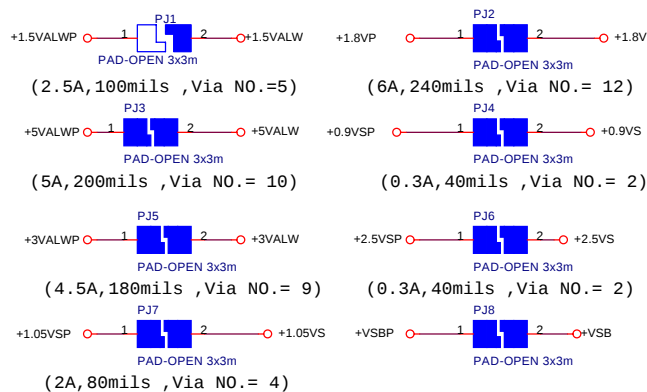
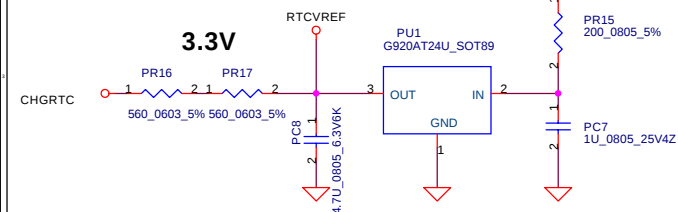
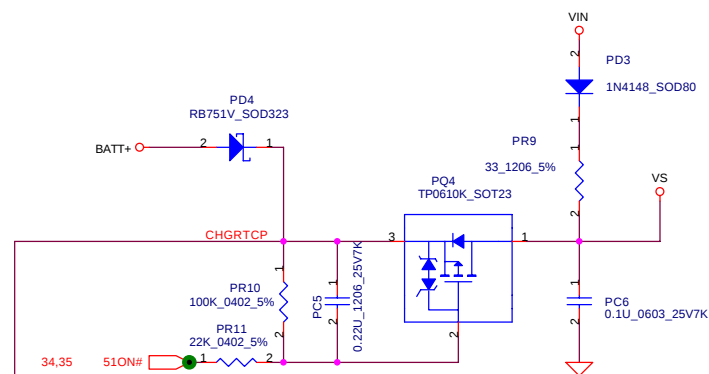
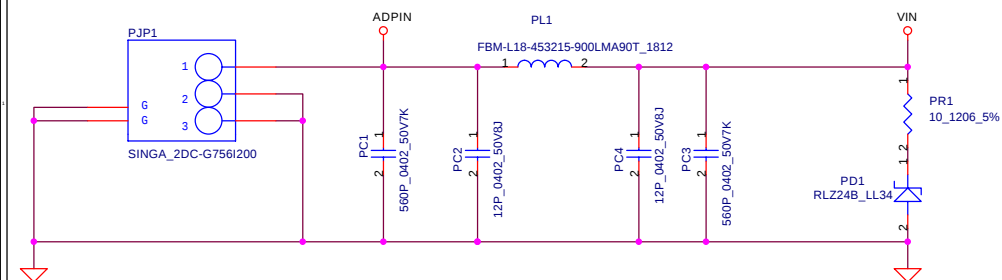
Add 2ND FAN Circuit for TV-Tuner



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ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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$$F_{osc} = 14100 / R_t = 14100 / 47 = 300 \text{ KHz}$$

IREF=1.31*Icharge
IREF=0.73~3.3V

Vin Detector
L->H 18.49 17.92 17.35
H->L 17.17 16.64 16.11

LI-4S : 17.8V --- BATT-OVP=1.9758V
BATT-OVP=0.111*BATT+

CC=3.046A
 $(120K / (205K + 120K)) * 3.3V = 1.2184V$
 $1.2184V / (20 * 0.02) = 3.046A$

CP Point=4.216A
 $5V * (59K / (20K + 59K)) = 1.265V$
 $1.265V / (20 * 0.015) = 4.216A$

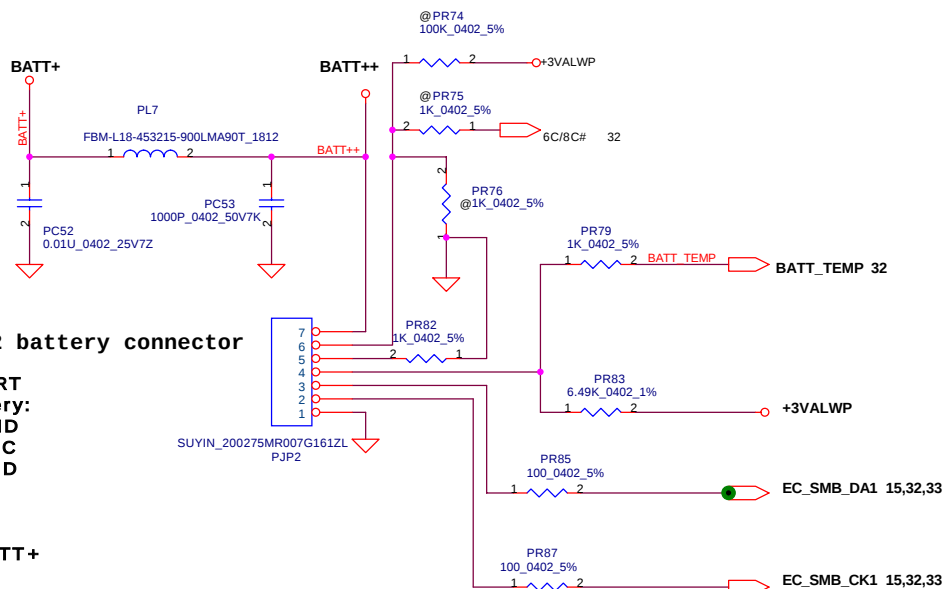
Charge voltage
4S CC-CV MODE : 16.8V
VCHG is H

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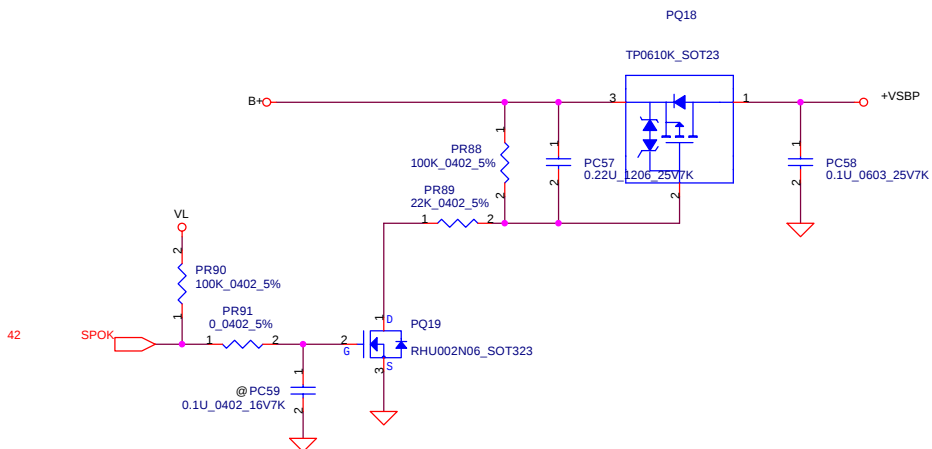
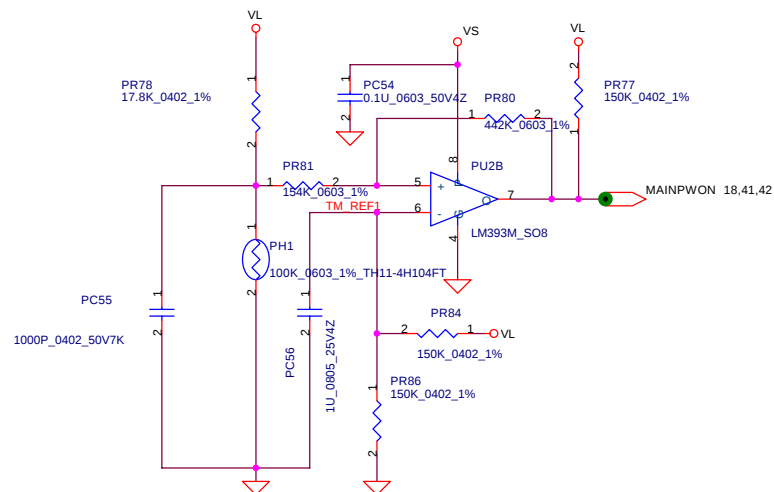
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PJP2 battery connector

SMART Battery:
1.GND
2.SMC
3.SMD
4.TS
5.B/I
6.ID
7.BATT+

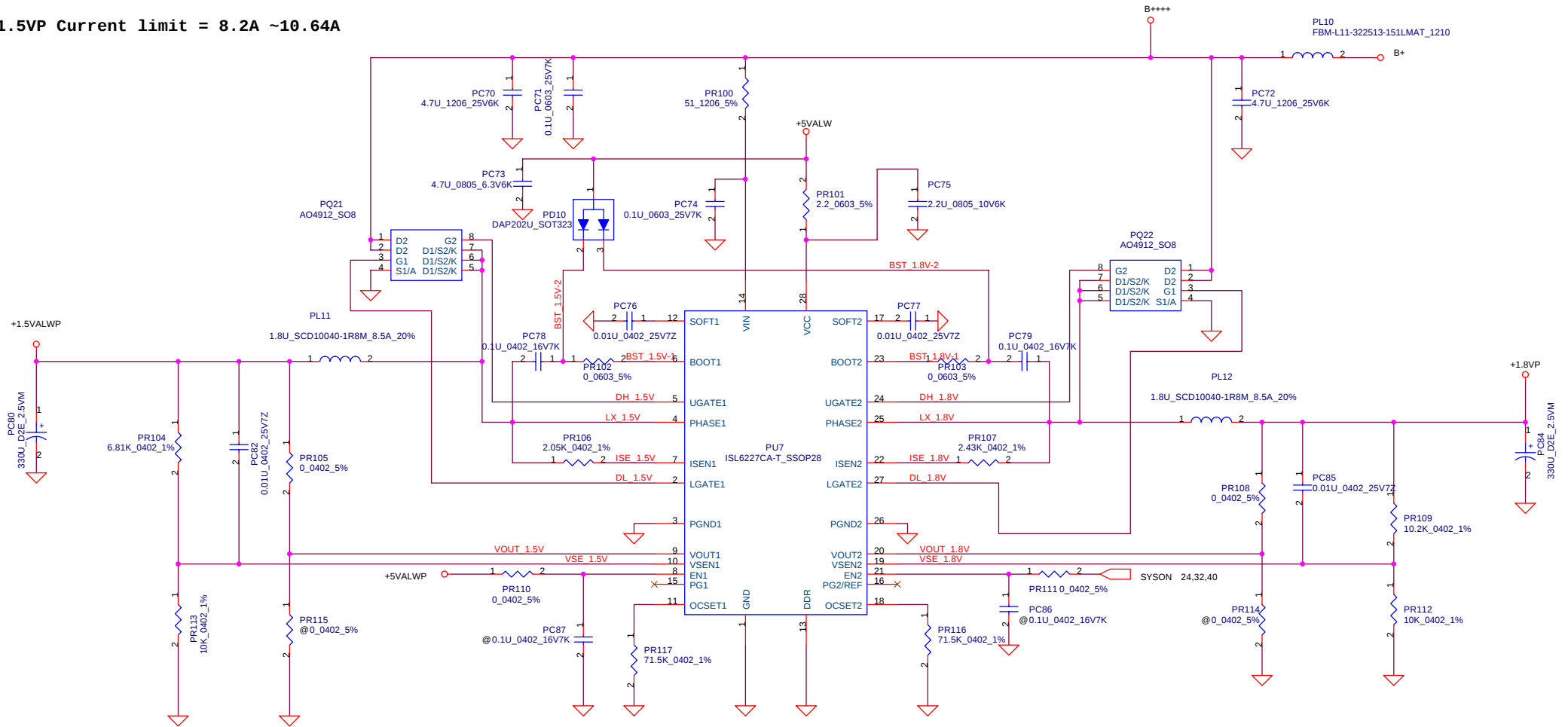


PH1 under CPU bottom side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C

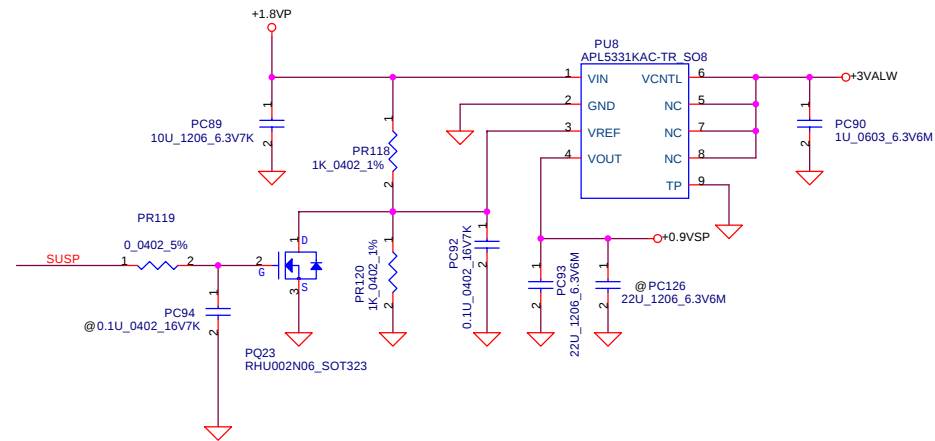
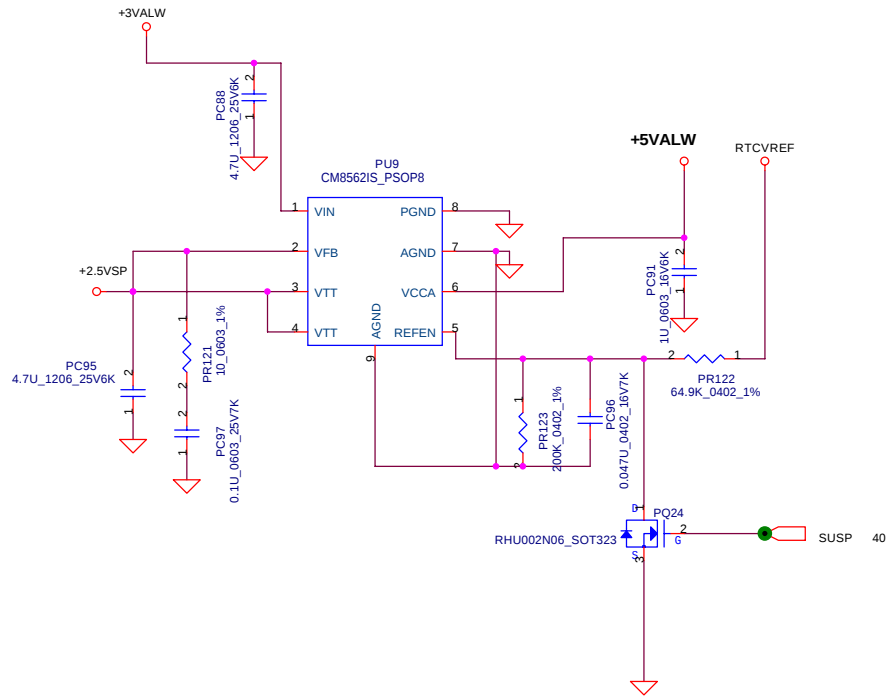


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+1.5VP Current limit = 8.2A ~10.64A



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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	B.Ver #	Phase
1	For HDQ70, change RTC change current.	Because the charge cuurent needs to meet battery spec.	0.1	41	Change PR16 and PR17 from SD028300000 to SD028560000.	0.1	DVT
2	For HDQ70, change MAX1999 to MAX8734A	Because MAX1999 has triggered UVP when AC Adapter plug in or plug out.	0.1	42	Change PU3 from SA019990000(S IC MAX1999EEI QSOP28 PWM) to SA00000G100(MAX8734AEEI+ QSOP 28P)	0.1	DVT
3	For HDQ70, fix Vin detector accuracy.	For HDQ70, fix Vin detector accuracy.	0.1	43	Change PR65 from SD034150200(S RES 1/16W 15K 0402 1%) to SD034000000(S RES 1/16W 0 0402 1%).	0.1	DVT
4	For HDQ70, fix Vin detector accuracy.	For HDQ70, fix Vin detector accuracy.	0.1	43	Change PR68 from SD034100300(S RES 1/16W 100K 0402 1%) to SD000008A00(S RES 1/16W 118K 0402 0.1%).	0.1	DVT
5	For HDQ70, fix Vin detector accuracy.	For HDQ70, fix Vin detector accuracy.	0.1	43	Change PR73 from SD034100200(S RES 1/16W 10K 0402 1%) to SD0000008B00(S RES 1/16W 10K 0402 0.1%).	0.1	DVT
6	For HDQ70, fix the battery temp curve	Because we need to improve the curve of temp detector of battery more smoothly.	0.1	44	Change PR83 from SD034255200(S RES 1/16W 25.5K 0402 1%) to SD034649100(S RES 1/16W 6.49K 0402 1%).	0.1	DVT
7	For HDQ70, change 1.05VSP OCP point.	For HDQ70, change 1.05VSP OCP point.	0.1	45	Change PR93 from SD034412100(S RES 1/16W 4.12K 0402 1%) to SD034499100(S RES 1/16W 4.99K 0402 1%).	0.1	DVT
8	For HDQ70, fix the output voltage.	For HDQ70, fix the output voltage within spec.	0.1	45	Change PR96 from SD034715100(S RES 1/16W 7.15K 0402 1%) to SD034499100(S RES 1/16W 4.99K 0402 1%).	0.1	DVT
9	For HDQ70, fix the FB voltage.	For HDQ70, fix the FB voltage within spec.	0.1	45	Change PC68 from SE075682K00(S CER CAP 6800P 25V +-10% X7R 0402) to SE042333K00(S CER CAP .033U 25V K X7R 0603).	0.1	DVT
10	For HDQ70, add snuber on LX.	Add snuber on LX to improve high side noise.	0.1	45	Add PR170 SD011470BT9(S RES 1/10W 4.7 +-5% 1206).	0.1	DVT
11	For HDQ70, add snuber on LX.	Add snuber on LX to improve high side noise.	0.1	45	Add PC130 SE024681J00(S CER CAP 680P 50V J NPO 0603).	0.1	DVT
12	For HDQ70, 1.5VALWP ripple voltage is too large.	Because we need to improve the ripple of 1.5VALWP.	0.1	46	Change PC80 from SGA20151330 to SGASGA19331D00.	0.1	DVT
13	For HDQ70, 1.8VP ripple voltage is too large.	Because we need to improve the ripple of 1.8VP.	0.1	46	Change PC84 from SGA20151330 to SGASGA19331D00.	0.1	DVT
14	For HDQ70, change 1.8VP OCP point.	For HDQ70, change 1.8VP OCP point.	0.1	46	Change PR107 from SD034174100(S RES 1/16W 1.74K 0402 1%) to SD034243100(S RES 1/16W 2.43K 0402 1%)	0.1	DVT
15	For HDQ70, change 1.8VP OCP point.	For HDQ70, change 1.8VP OCP point.	0.1	46	Change PR116 from SD034806200(S RES 1/16W 80.6K 0402 1%) to SD034715200(S RES 1/16W 71.5K 0402 1%).	0.1	DVT
16	For HDQ70, fix the 2.5VSP's power sequence.	Because we need to fix the power sequence of 2.5VSP.	0.1	47	Change PC96 from SE075222K00(S CER CAP 2200P 25V +-10% X7R 0402) to SE076473K00(S CER CAP 0.047U 16V K X7R 0402).	0.1	DVT

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HW section

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Item	Reason for change	PG #	Modify List	Date	
1	AC_IN Signal	P.32	Remove R189, D11		DVT(Rev02)
2	LAN LED on 8110SBL	P.26	Unpop R449 on both 8100CL and 8110SBL		DVT(Rev02)
3	Modify +1.8VS and +1.5VS power sequence	P.40	Change R531,R551 value from 100K to 180K		DVT(Rev02)
4	5 Way BTN problem	P.33,34	Add 5WAY_BTN signal and R184		DVT(Rev02)
5	Remove New Card circuit	P.24	Remove New Card Circuit		DVT(Rev02)
6	New Card Clock Request	P.13	Connect PCIE_CLKREQ1# to Clock Gen pin.32		DVT(Rev02)
7	Change IEEE1394 Connector	P.25	Change IEEE1394 Connector Type		DVT(Rev02)
8	Codec VREF capacitor	P.36	Change C497 value from 0.1uf to 10uf		DVT(Rev02)
9	+SD_VCC and +XD_VCC Power Switch	P.23	Add R572, R573 for SD, XD Power Switch		DVT(Rev02)
10	Un-used Codec Clock	P.13	unpopped R89		DVT(Rev02)
11	Un-used ODD Connector	P.21	Remove the JP47 and C362,C366,C675,C678,C681		DVT(Rev02)
12	Add 10uF capacitor on GMCH	P.9	Add C703 on +3VS_DAC		DVT(Rev02)
13	Changed for Speaker and Subwoofer	P.37,38	Change Main Amplifier Gain form 10dB to 8dB, and Modify Woofer BPF value		DVT(Rev02)
14	Change CRT and TV-out Pi Filter Value	P.14	Change CRT and TV-out Pi Filter Value to Following Chipset Recommand		DVT(Rev02)
15	Change DVI SMBUS Pull-up Value	P.16	Change R346,R348 from 30K to 6.8K		DVT(Rev02)
16	Change TV-Tuner Pin98,100 definition	P.29,32,36	Add TV_THERM# signal, Del C81, C82		PVT(Rev03)
17	Change S/PDIF /Headphone Out Pin Define	P.37	Change S/PDIF /Headphone Out Pin Define		PVT(Rev03)
18	Add AMP_MONO for sub-woofer	P.38	Add AMP_MONO signal and C704, R574		PVT(Rev03)
19	Del reserved Audio Jack	P.37	Del JP27, JP31, JP34, JP3		PVT(Rev03)
20	Change Amplifier Gain	P.37	R120 change to 10K, C97 change to 0.01uf		PVT(Rev03)
21	Del reserved USB port	P.31	Del JP23,C390,C385,C386,D5,JP38,C653,C646,C645,D13		PVT(Rev03)
22	Change FAN control circuit	P.39	Change FAN control circuit to GMT G993		PVT(Rev03)
23	Add EMI Solution on AV-In Connector	P.29	Add L32, L33, L34, L35, L36 on AV-IN Signals		PVT(Rev03)
24	Add ESD Diode on MIC Signals	P.37	Add D32 on MIC Signals		PVT(Rev03)
25	Add NBA_PLUG to Disable MONO_OUT	P.36	Connect NBA_PLUG to Disable Codec MONO_OUT when Headphone Plugged		PVT(Rev03)
26	Separate +2.5VS_CRT from +2.5VS	P.9	Add L37,C706,C707,C708,C709.C710		PVT(Rev03)
27	Change ICH6 Crystal Load Capacitor	P.18	Chang C96, C102 from 18P to 10P		PVT(Rev03)
28	Add L38, L39 on Subwoofer Conn. for EMI	P.38	Add L38, L39 on Subwoofer Conn.		PRE-MP(Rev1)
29	Change Speaker 00hm Resistor to Bead	P.37	Change R235, R236, R237, R238 to Bead		PRE-MP(Rev1)
30	Add Capacitor for EMI	P.34	Add C711, C712 on T/P Signal		PRE-MP(Rev1)
31	Add 2ND FAN Circuit For TV-Tuner	P.39	Add 2ND FAN Circuit For TV-Tuner		PRE-MP(Rev1)
32	Change RF-Jack Material	P.29	Change RF-Jack Material		PRE-MP(Rev2)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/07/29	Deciphered Date	2006/07/29	Title SCHEMATIC, M/B LA-2781	
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