

Compal Confidential

HBQ60 Schematics Document

**Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M
(With nVIDIA G73M/72MV)**

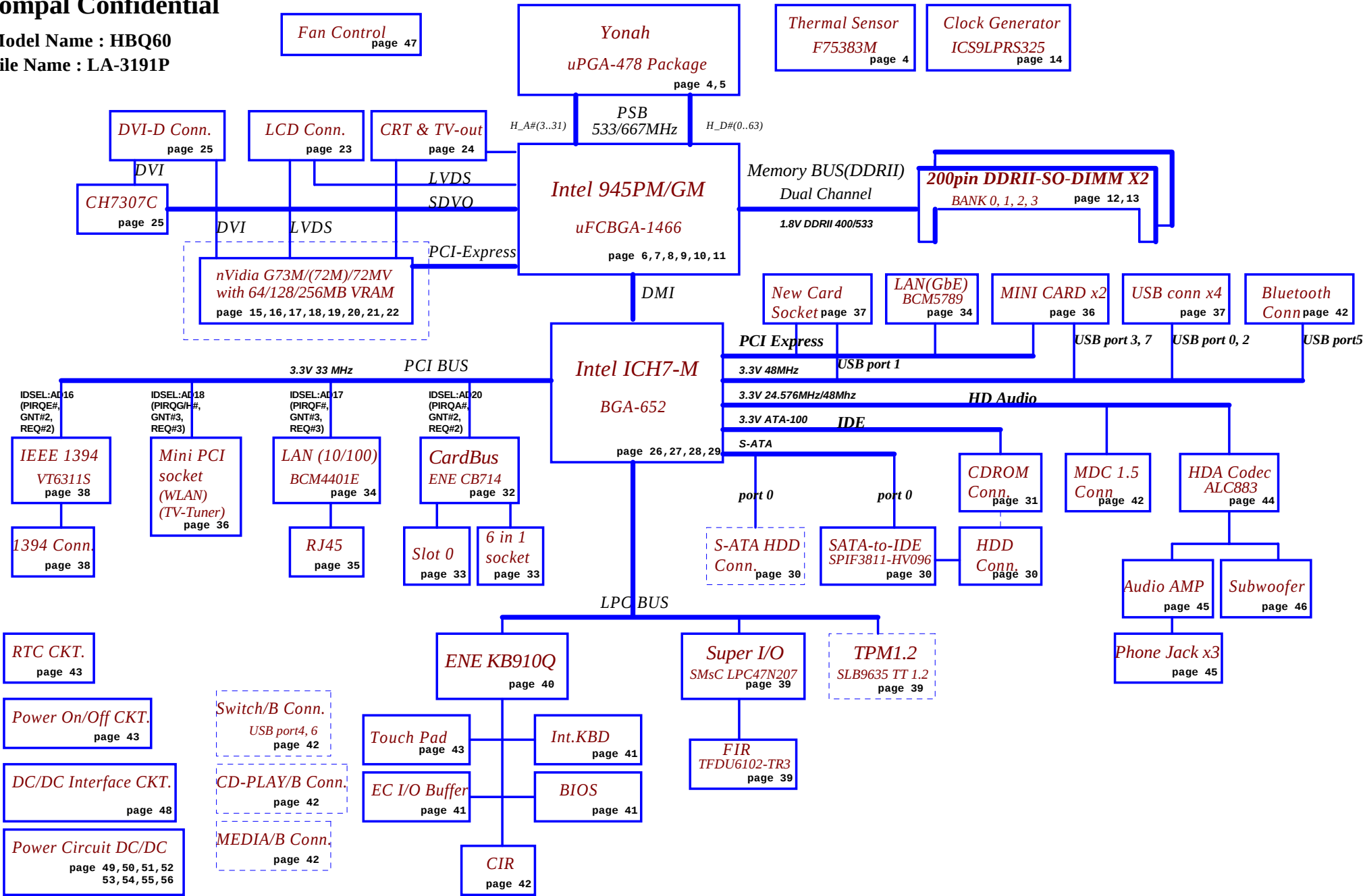
2005-02-11

REV: 1.0

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Model Name : HBQ60
File Name : LA-3191P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

EC SM Bus2 address

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

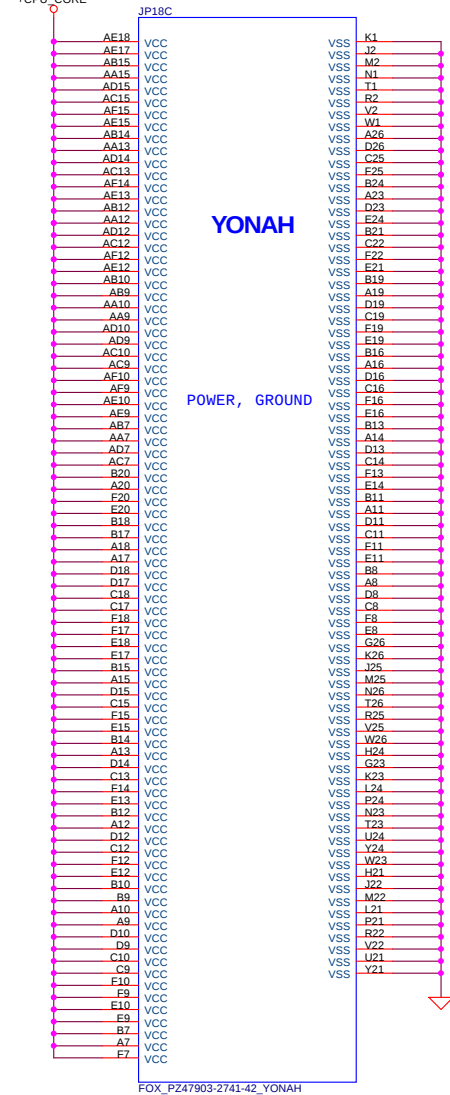
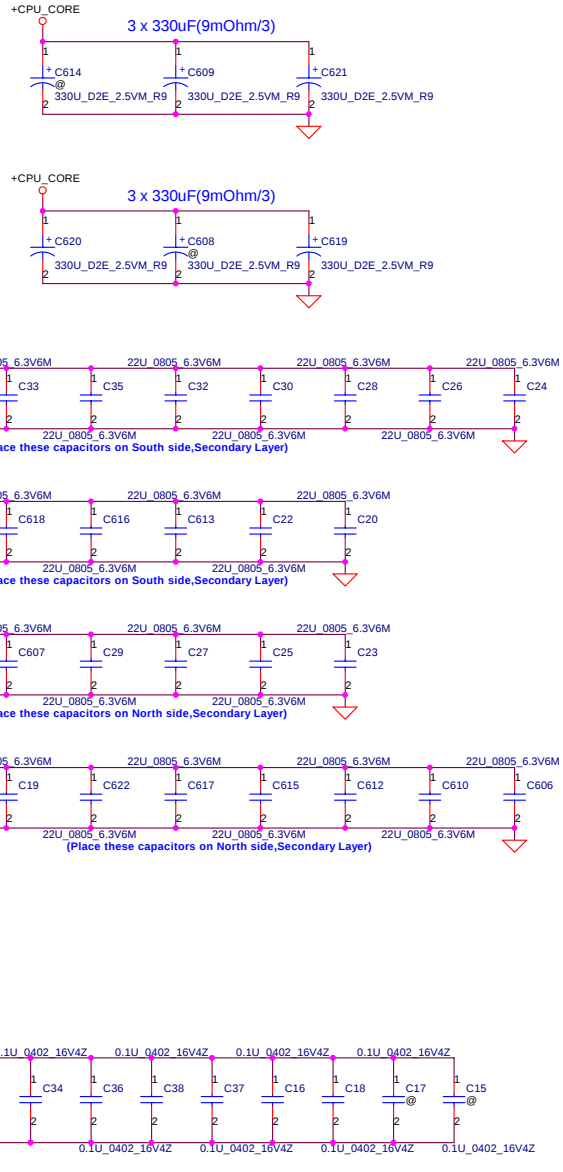
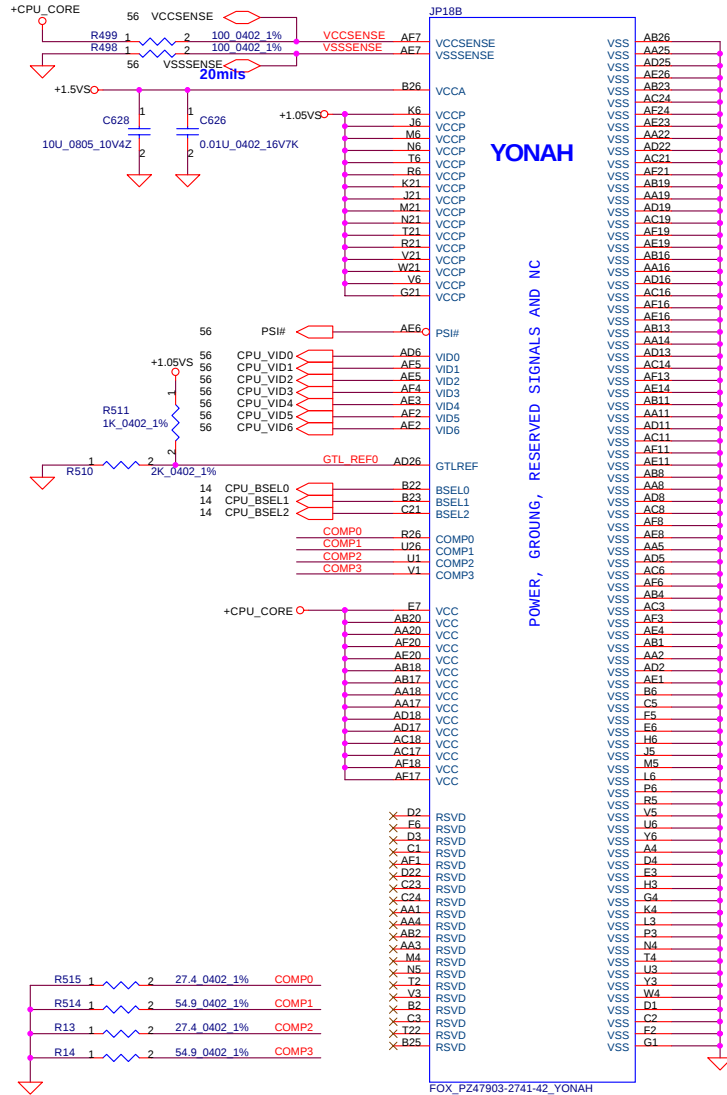
SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

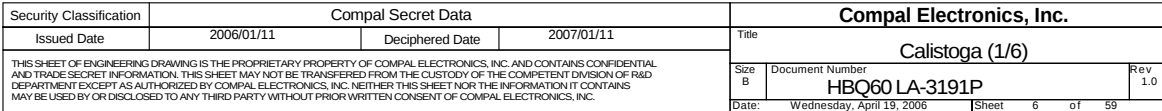
BTO Option Table

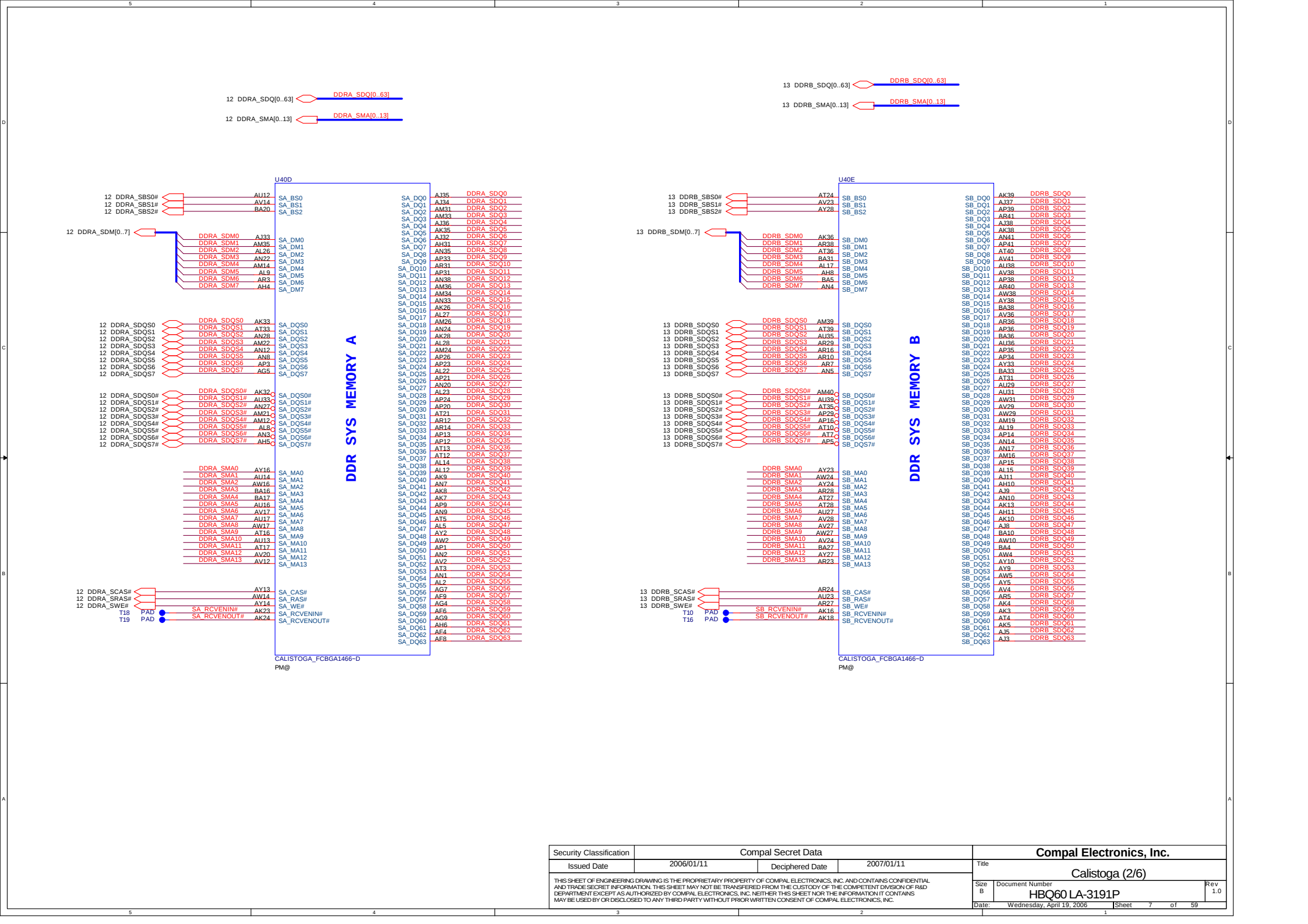
BTO Item	BOM Structure
VGA	PM@ + VGA@
UMA	GM@
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI_CARD1	MINI1@
MINI_CARD2	MINI2@
SATA-to-IDE	8040@
PATA	PATA@
GRAPEVINE	GRA@
672MV Only	G72@
673 Only	G73@
VRAM	X76@
VRAM 64M	64@
VRAM 128M	64@+128@
VRAM 256M	64@+128@+256@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
Sub-woofer	SUB@
5789&5787	8789@
4401&5789	0189@
VP1020	VP1020@
INTERNAL MIC	INTMIC@
1394	1394@
SATA HDD	SATA@
DVI	DVI@
CardReader	4IN1@
New Card	EXP@

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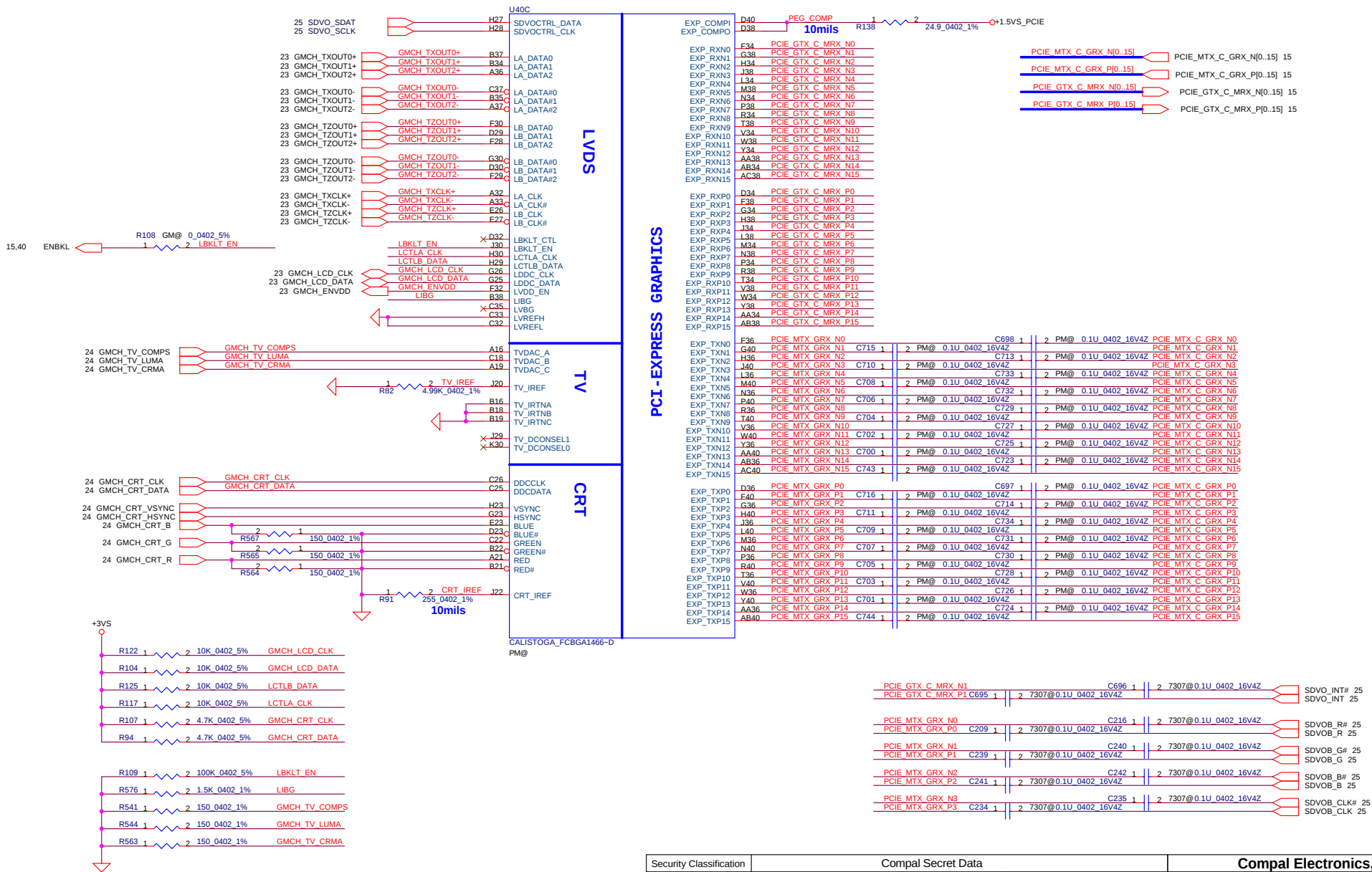


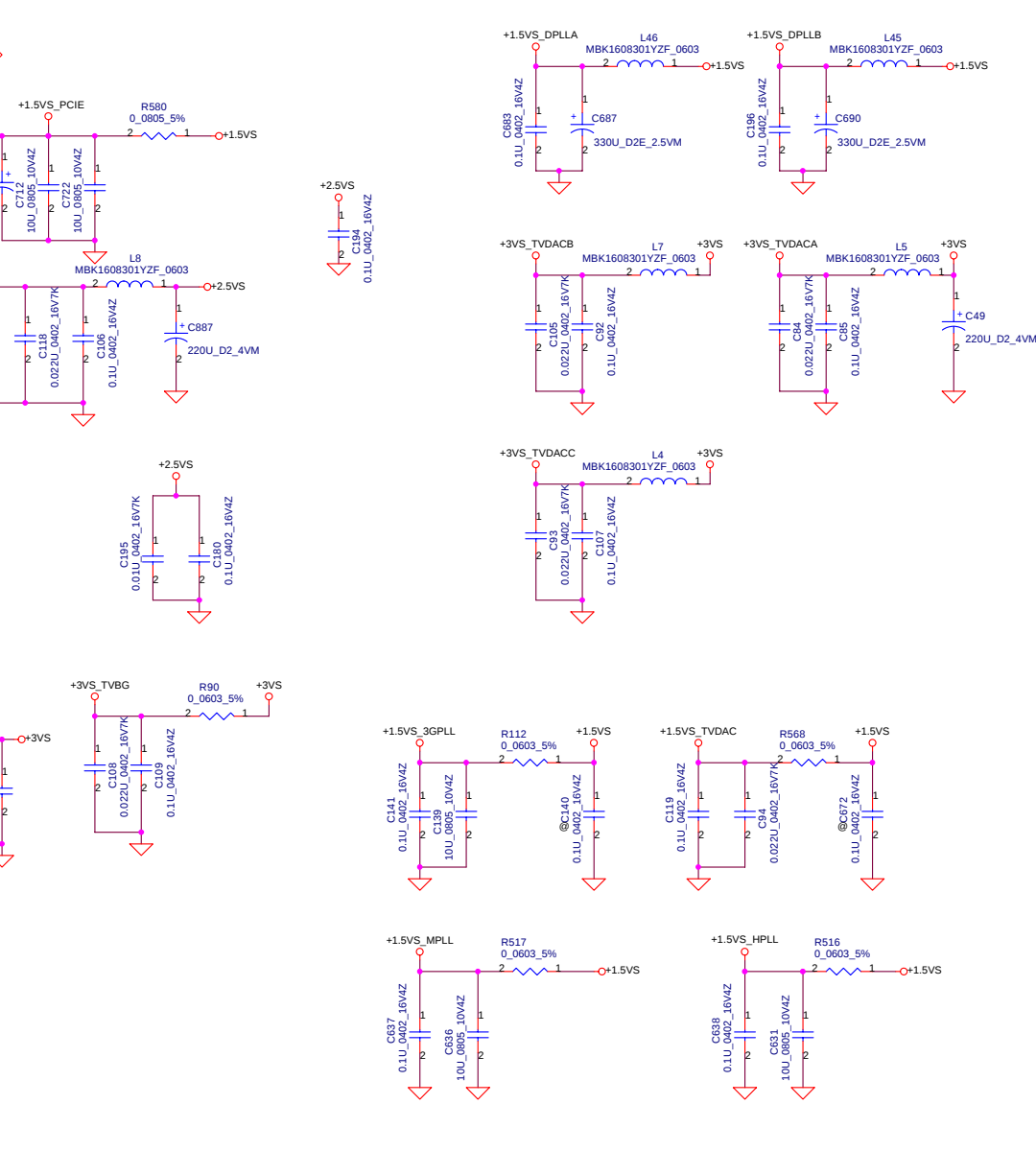
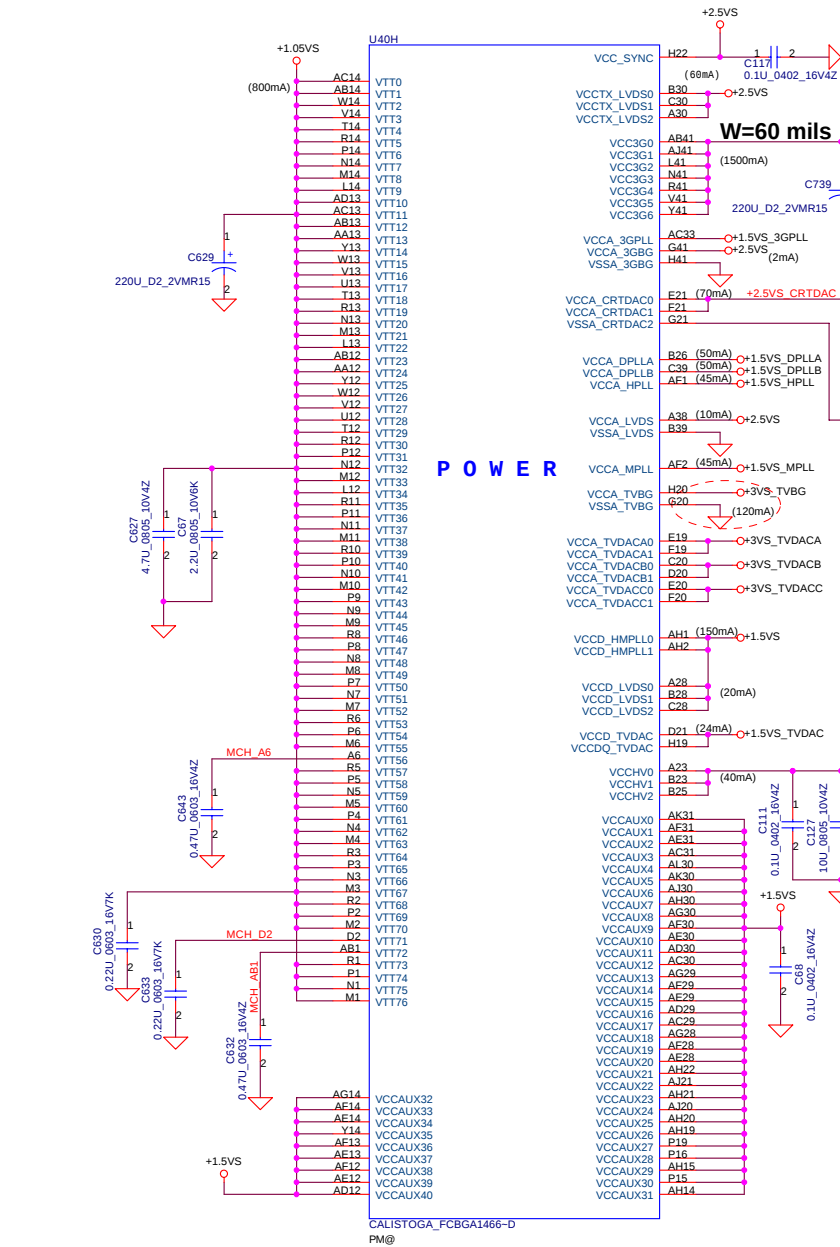
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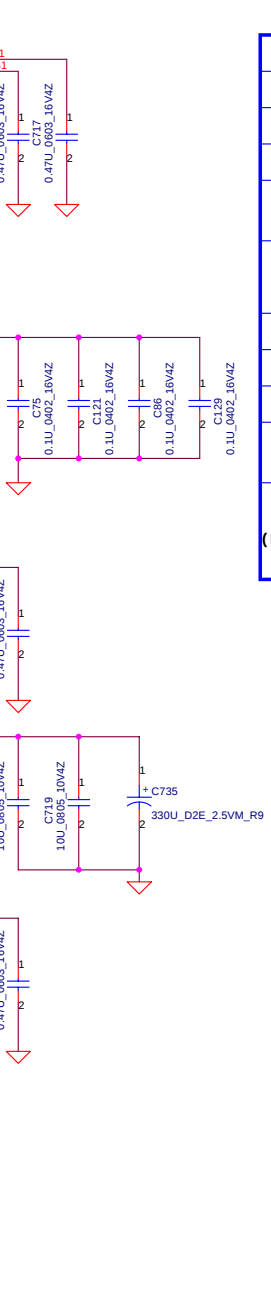
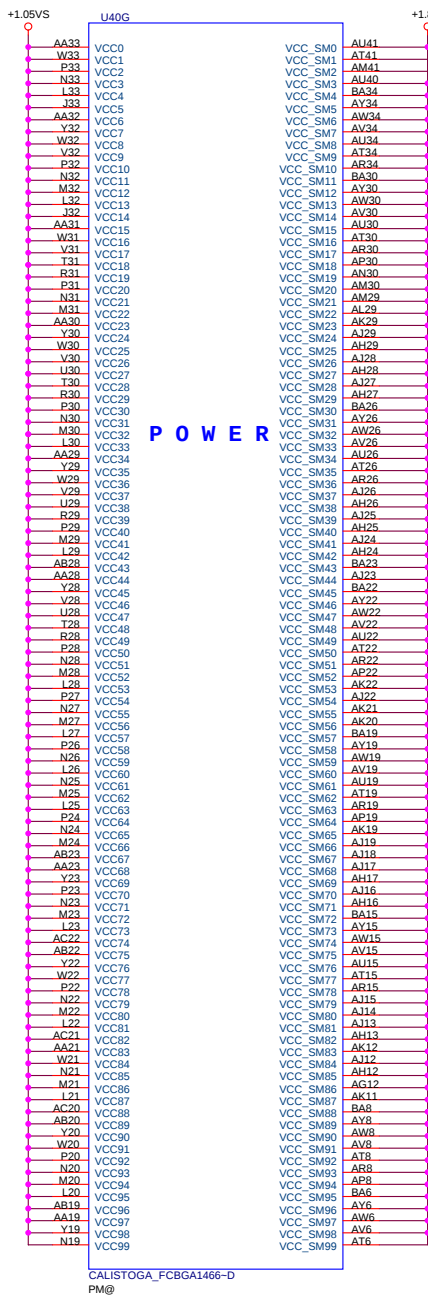
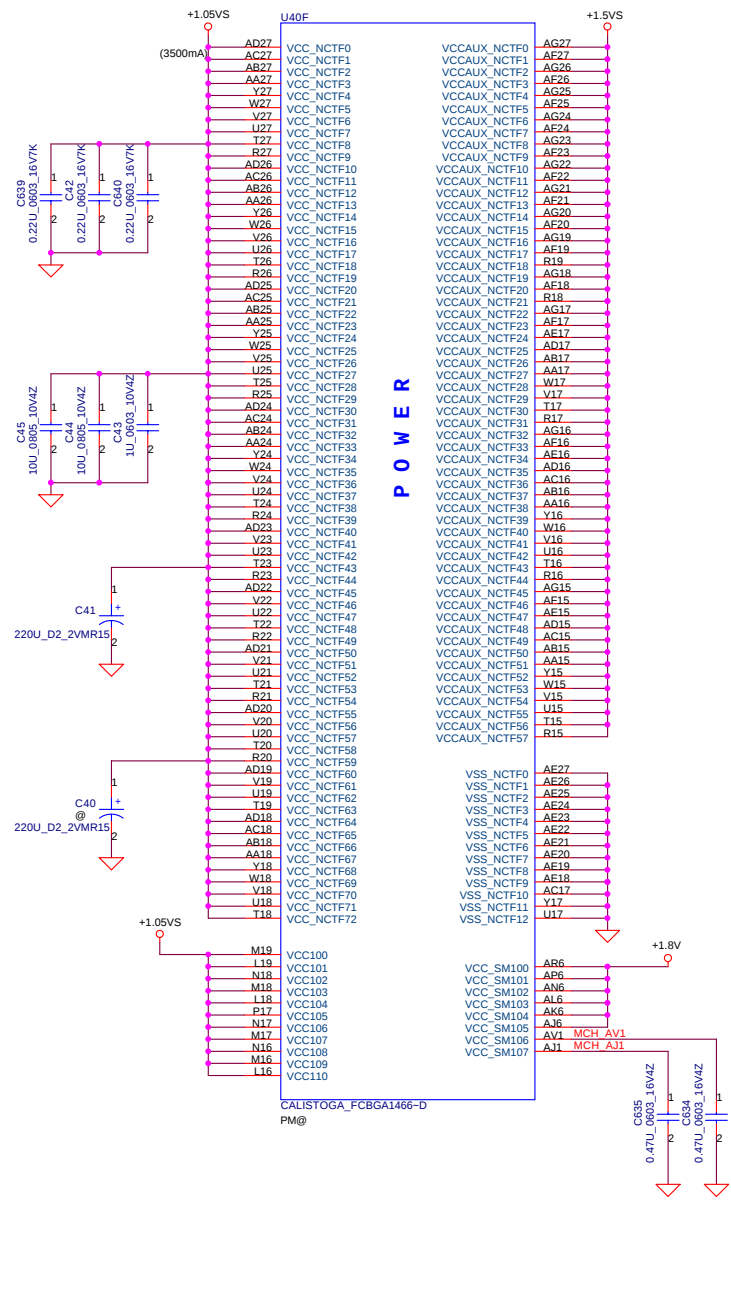


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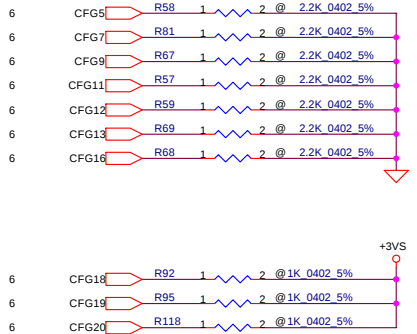


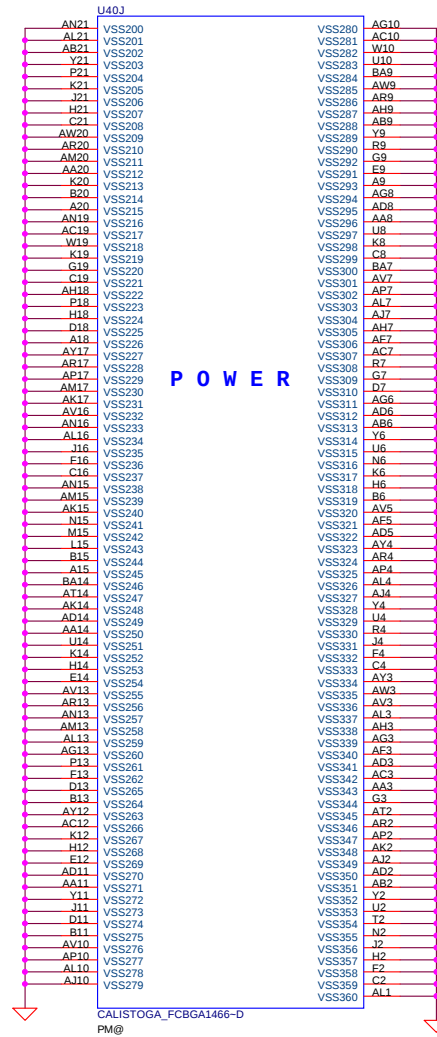
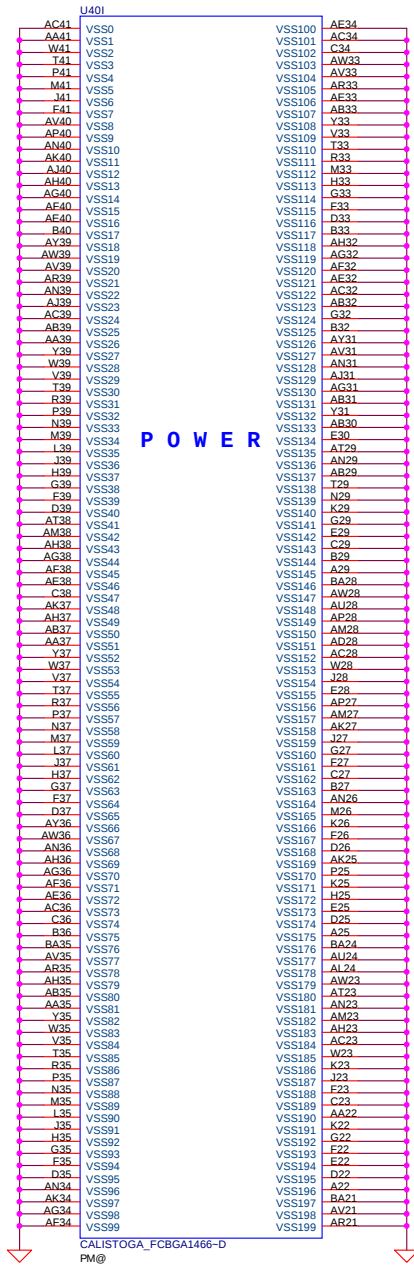


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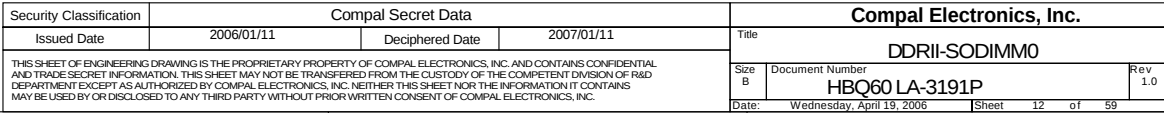


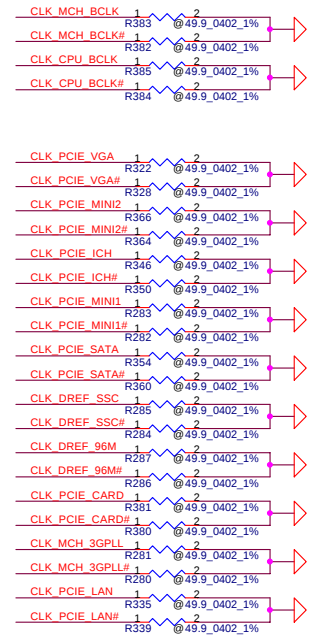
CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG11	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



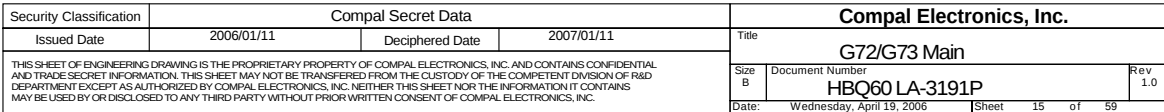


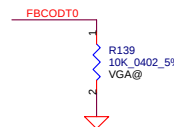
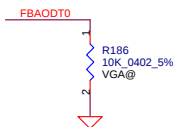
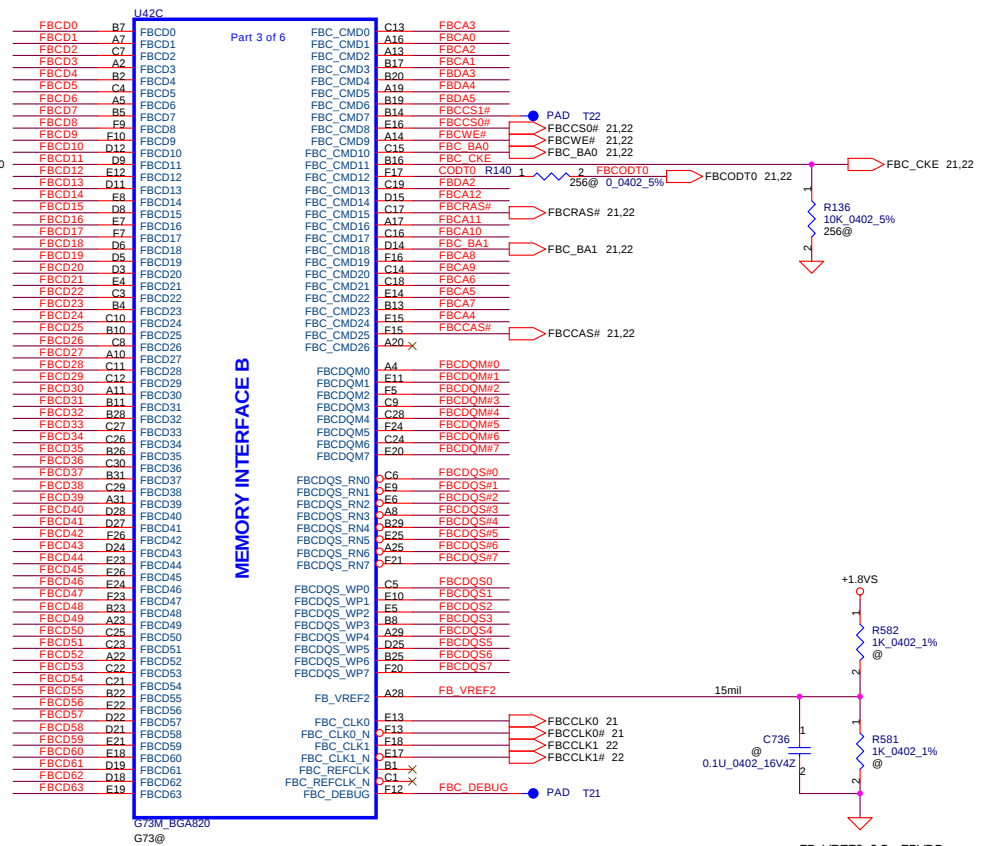
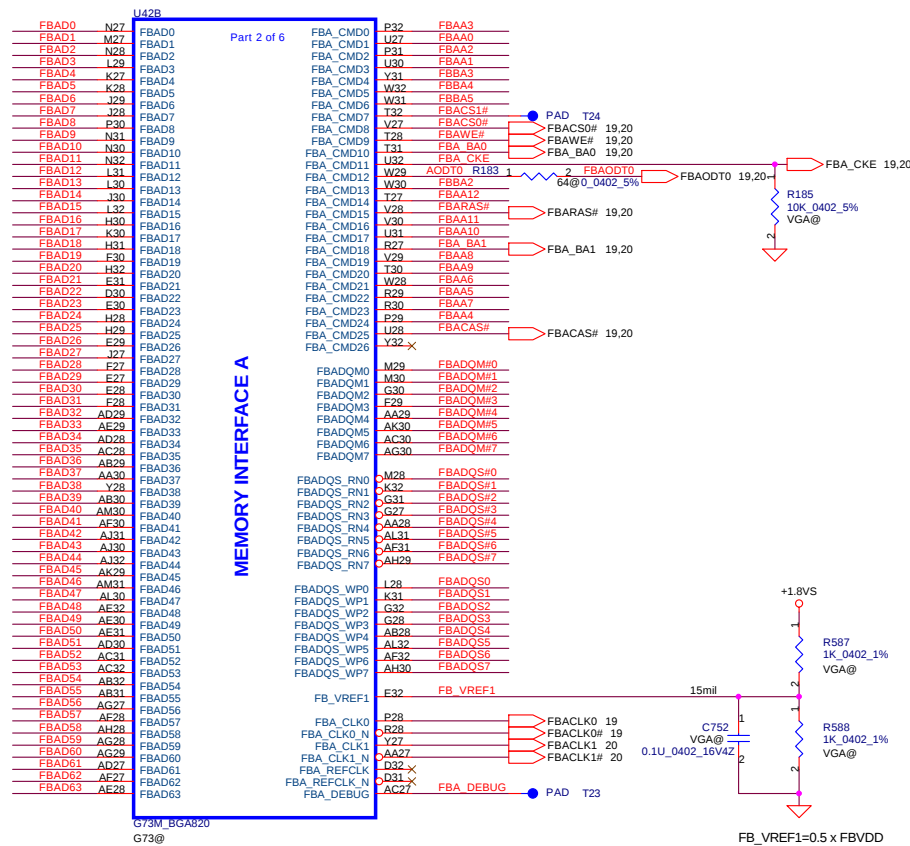
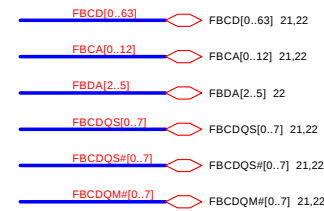
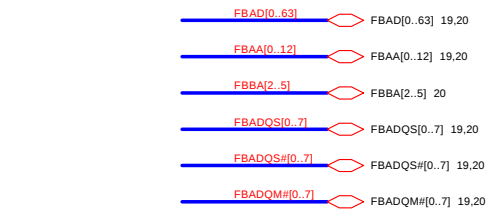
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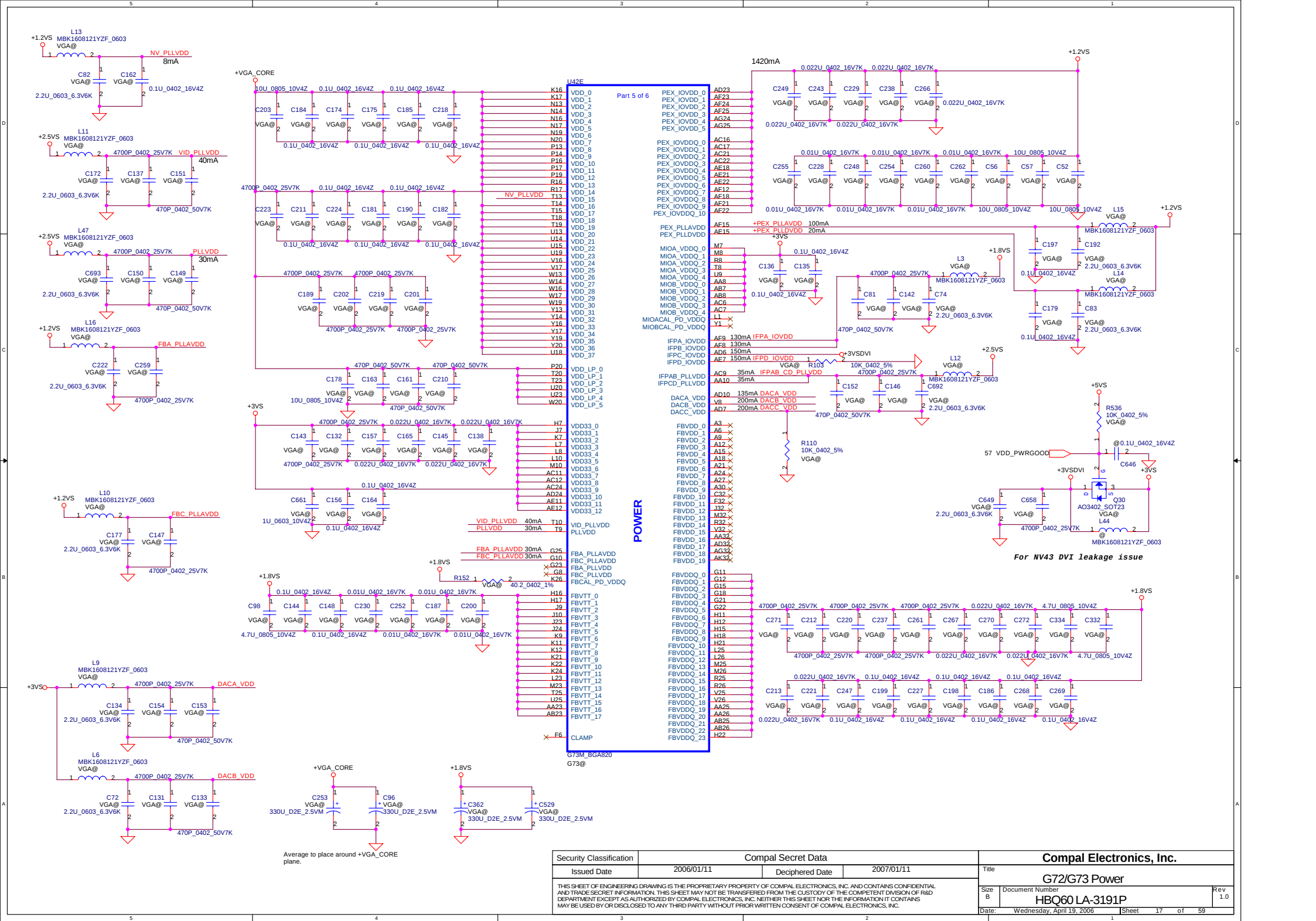


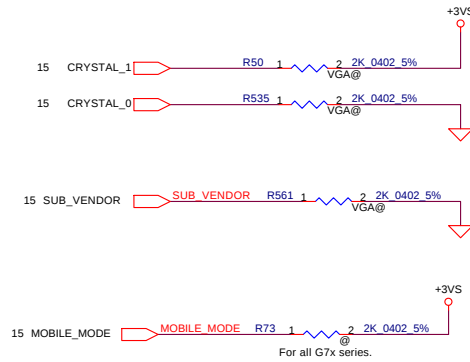
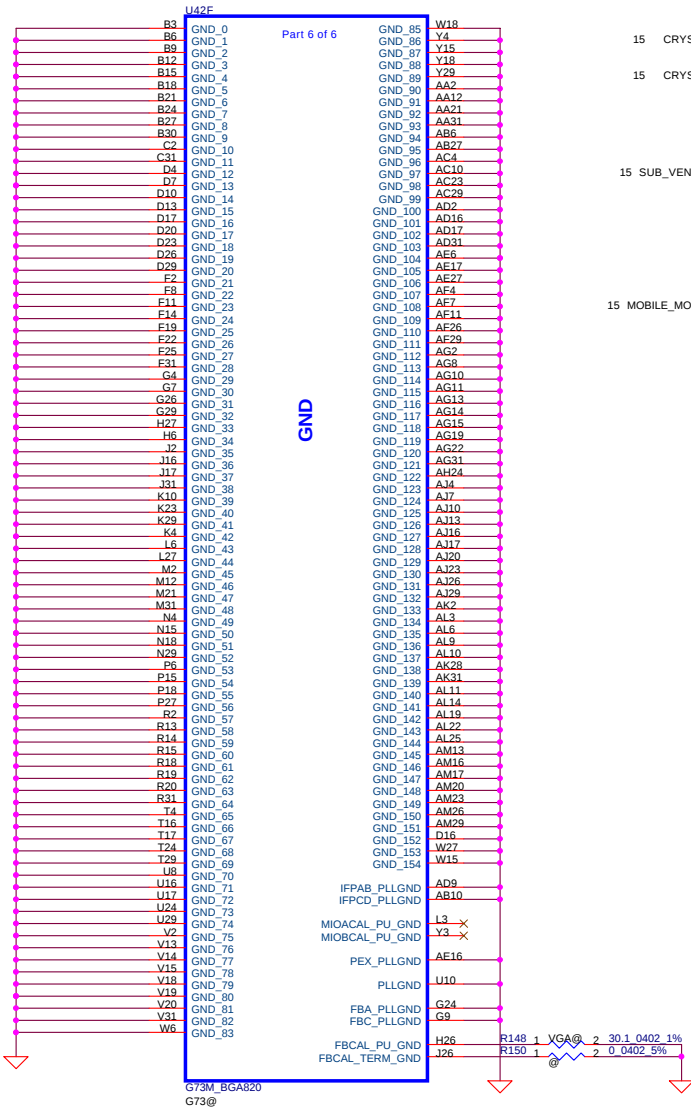
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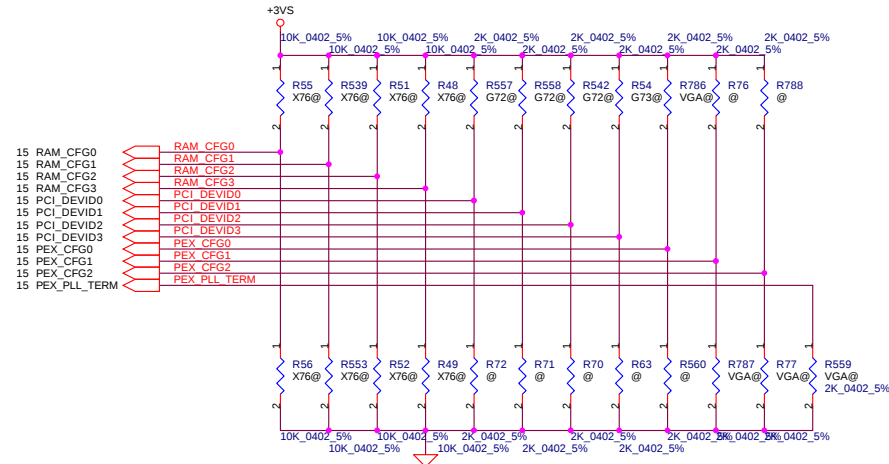


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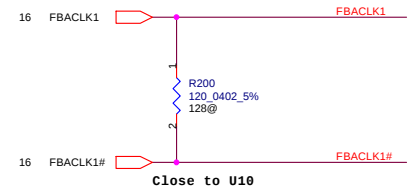
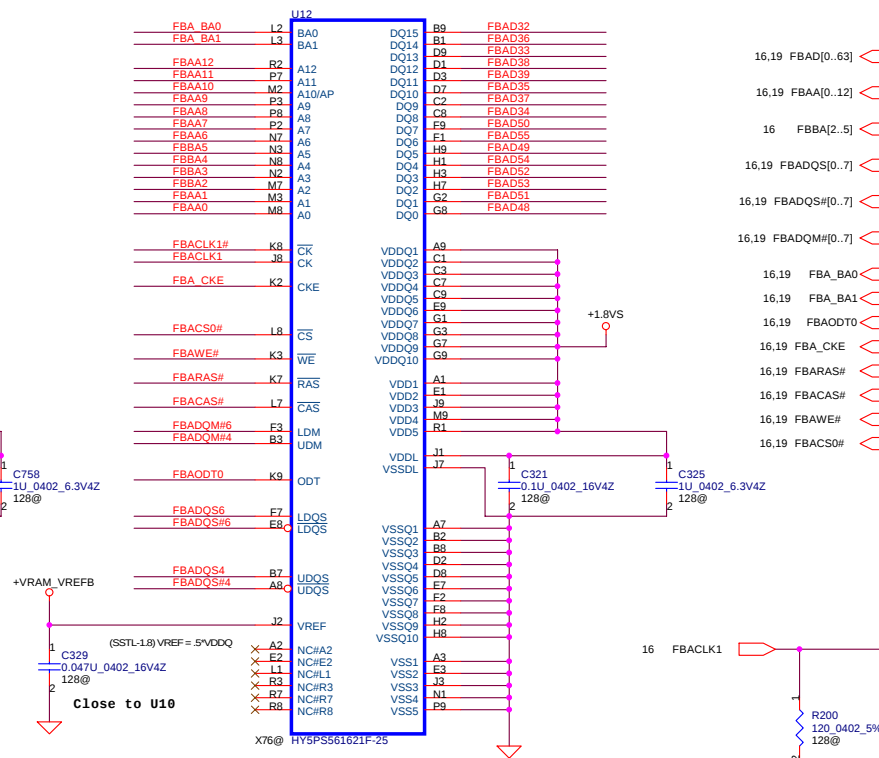
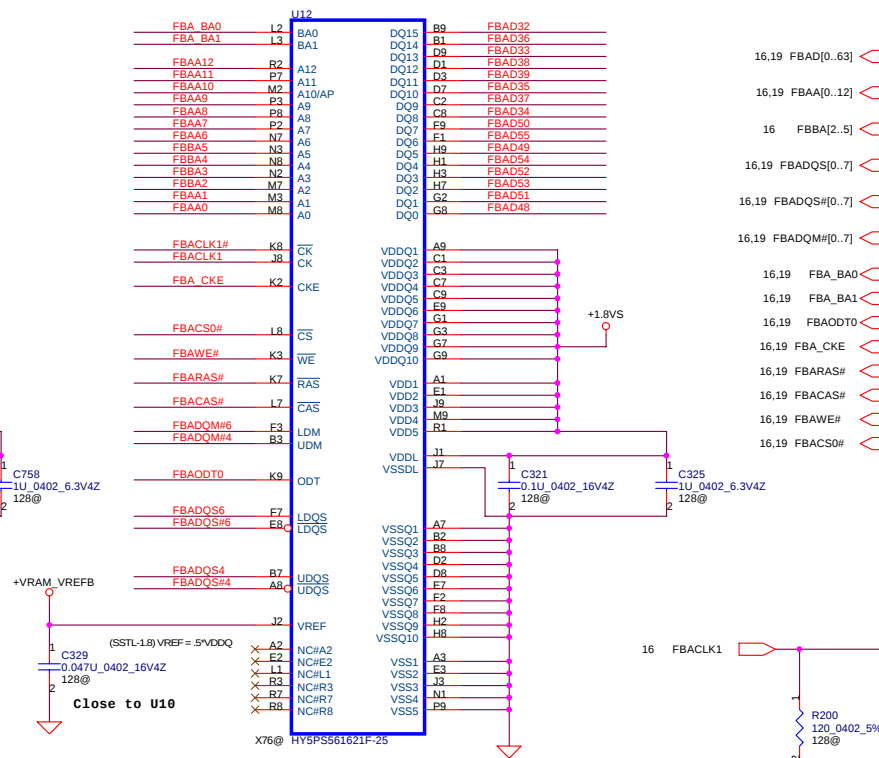




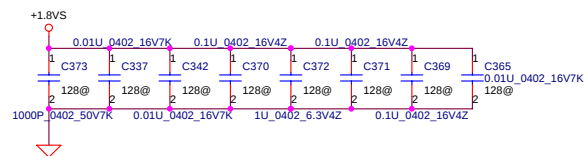
STRAPS	PIN	DESCRIPTION	Value	Value
CRYSTAL[1:0]	MIOBD[6,2]	27MHz=10, 14.318MHz=01, 13.5MHz=00	10	
ROM_TYPE[1:0]	MIOBD[11:10]	Parallel=00, SERIAL M25P10=01, Serial SST45VF=10	01	
SUB_VENDOR	MIOAD1	VBIOS on card (pull high) VBIOS with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD[9,8,6]	Recommended for G7x	010	
RAM_CFG[3:0]	MIOAD[5:2]	16Mx16x4 1.8V (128bit G73M)	0001	Samsung
		16Mx16x4 1.8V (128bit G73M)	0011	Hynix
		16Mx16x4 1.8V (128bit G73M)	0010	Infineon
		16Mx16x4 1.8V (64bit G73M)	1001	Samsung
		16Mx16x4 1.8V (64bit G73M)	1011	Hynix
		16Mx16x4 1.8V (64bit G73M)	1010	Infineon
		16Mx16x4 1.8V (64bit G72MV)	0001	Samsung
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxx8 G72M-0x01D8	1000	
		G72MV-0x01D7 TBD/TBD	0111	
MOBILE_MODE	MIOBD7	For NV44M/G7x		0



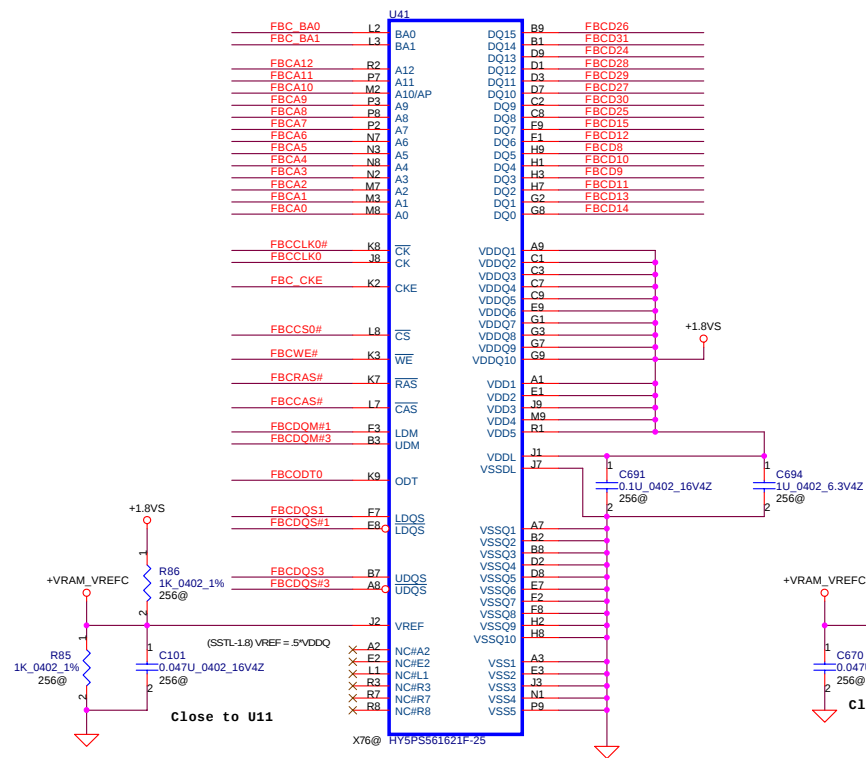
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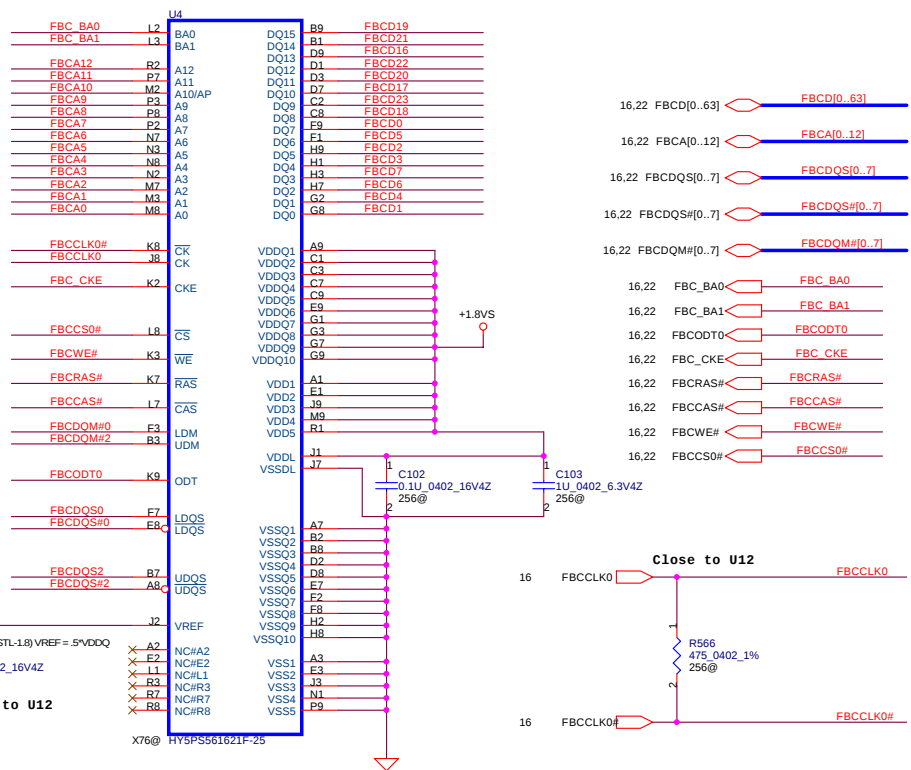
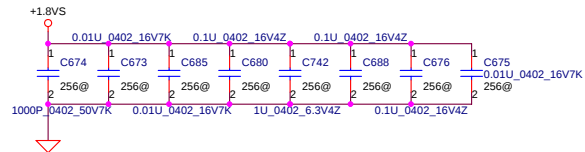
DDR2 BGA MEMORY



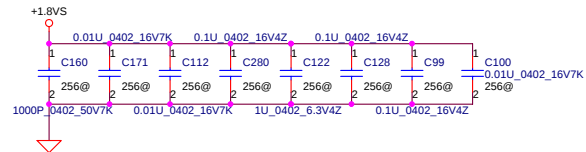
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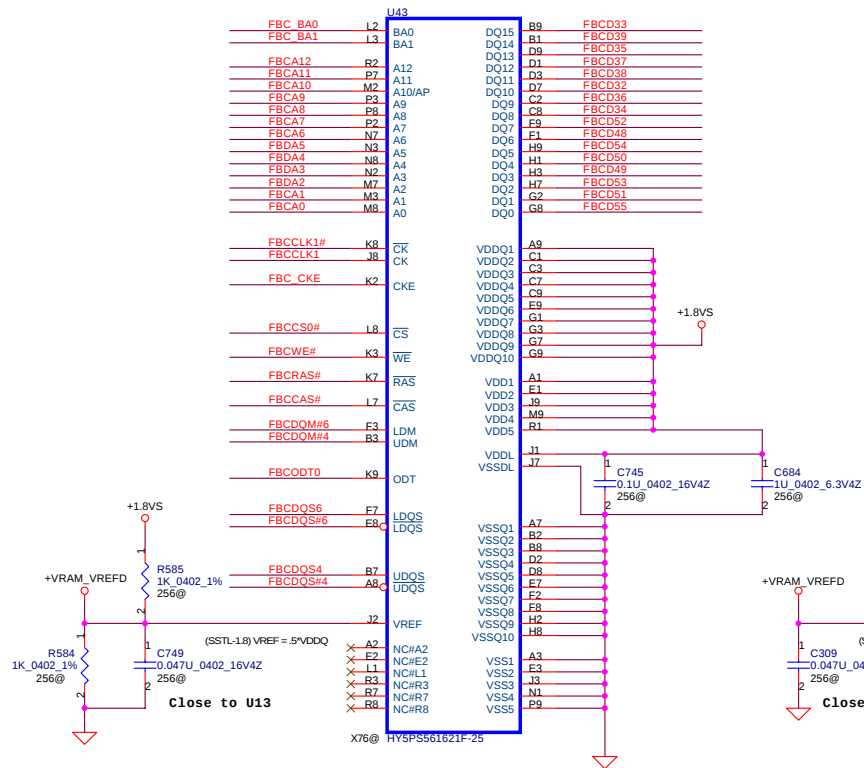
DDR2 BGA MEMORY



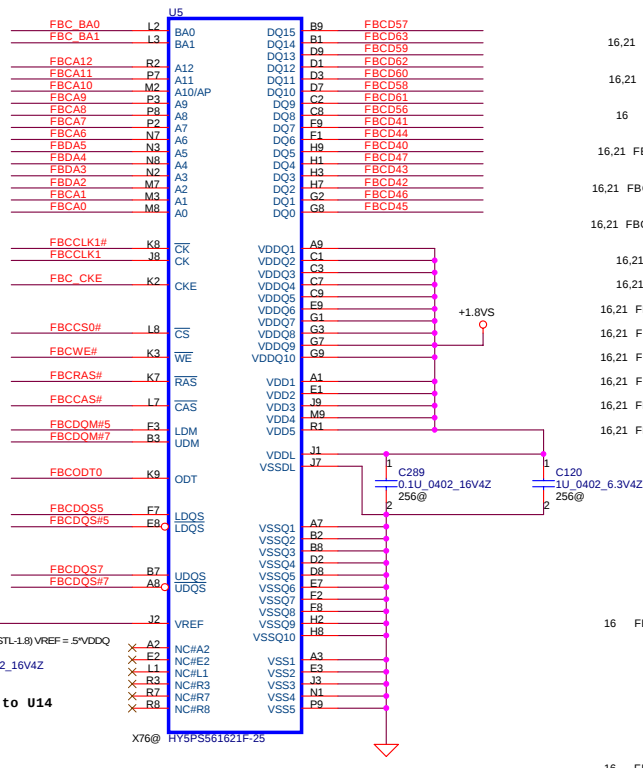
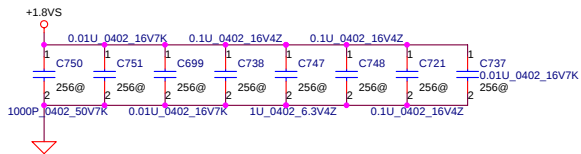
DDR2 BGA MEMORY



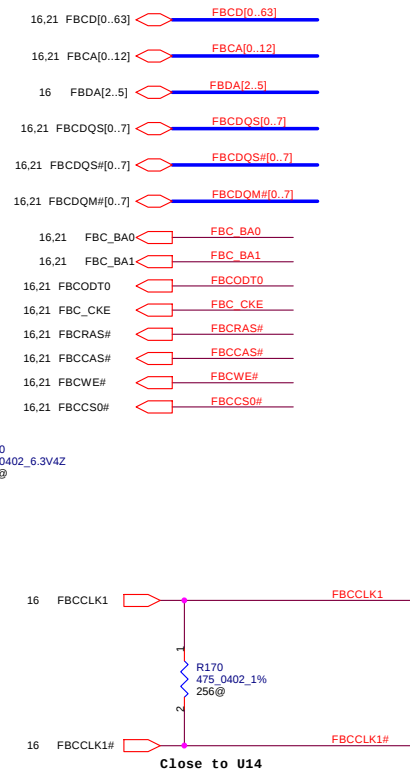
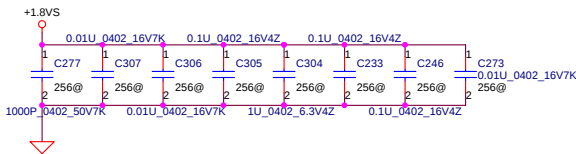
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Issued Date	2006/01/11	Deciphered Date	2007/01/11	Title				
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				Size	Document Number	HBQ60 LA-3191P		Rev 1.0
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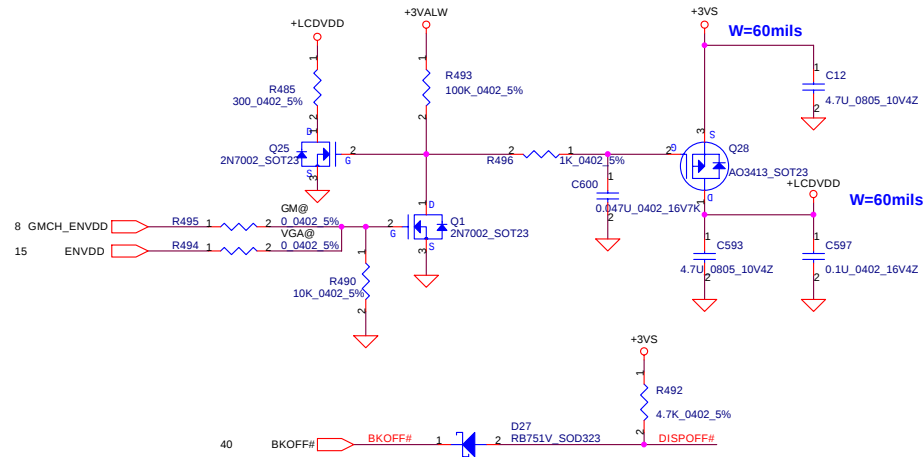
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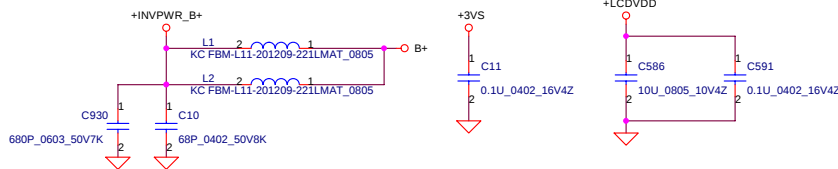
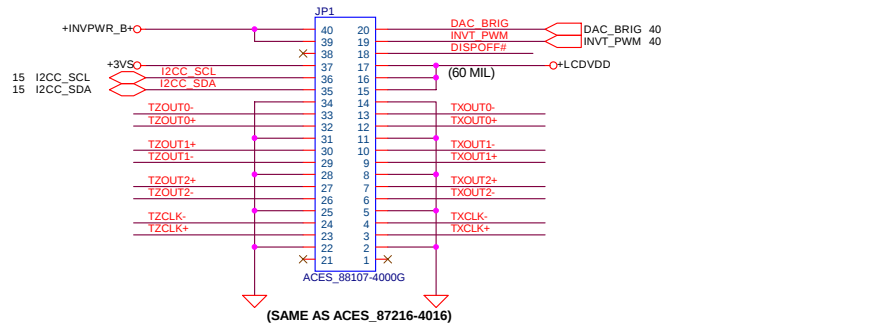
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LCD POWER CIRCUIT

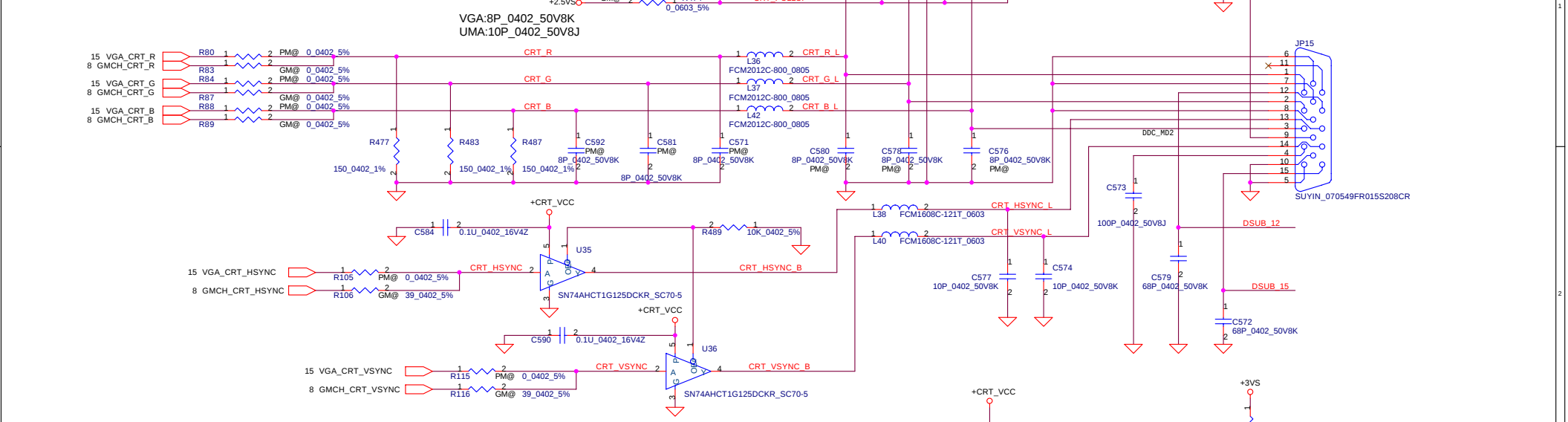


LCD/PANEL BD. Conn.

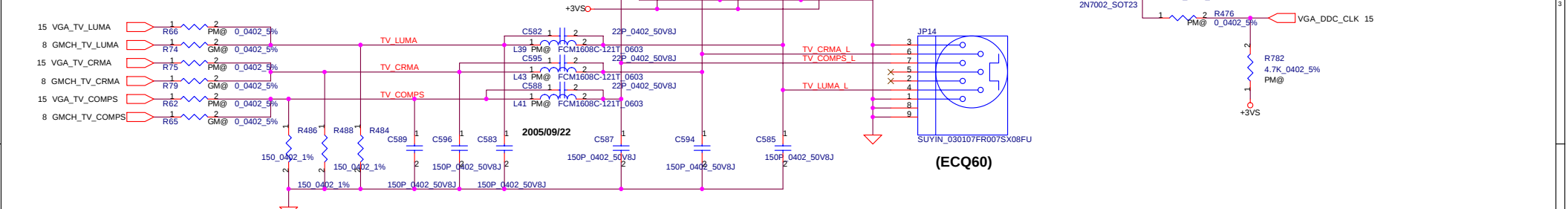


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								LCD Connector			
								Size B Document Number			
								HBQ60 LA-3191P			
								Rev 1.0			
								Date: Wednesday, April 19, 2006			
								Sheet 23 of 59			

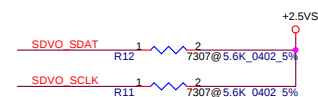
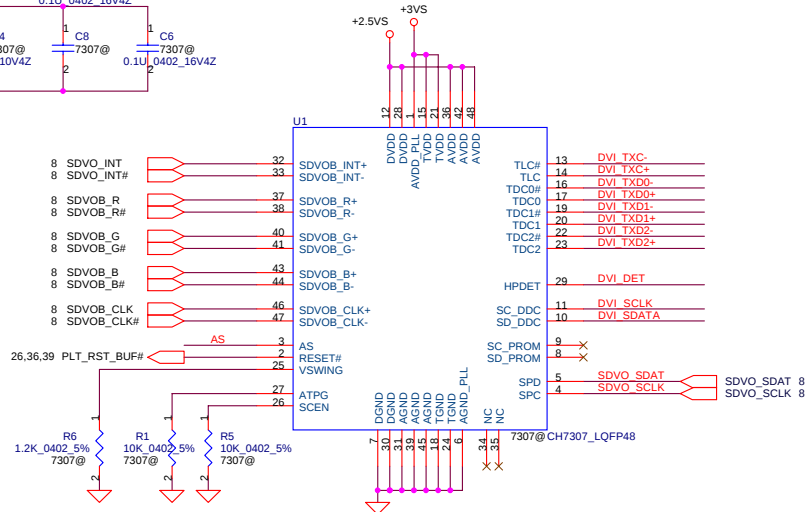
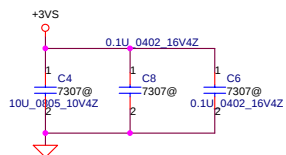
CRT Connector



TV-OUT Conn.

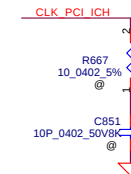
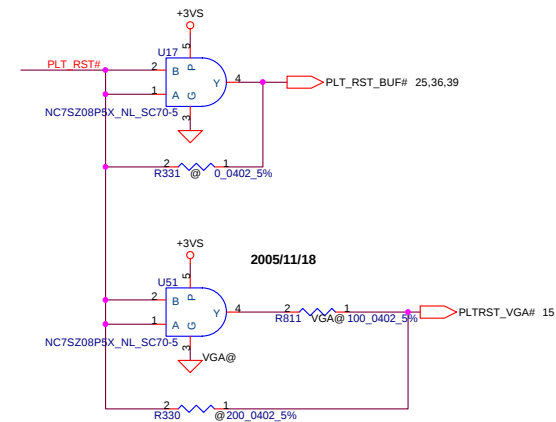
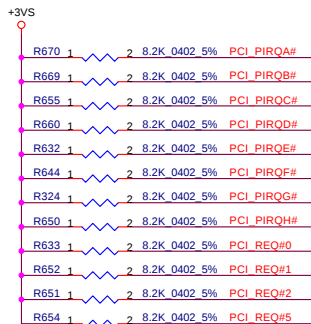


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Issued Date	2006/01/11	Deciphered Date	2007/01/11	Title CRT & TV-OUT Connector		
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Size B		Document Number		Rev 1.0		
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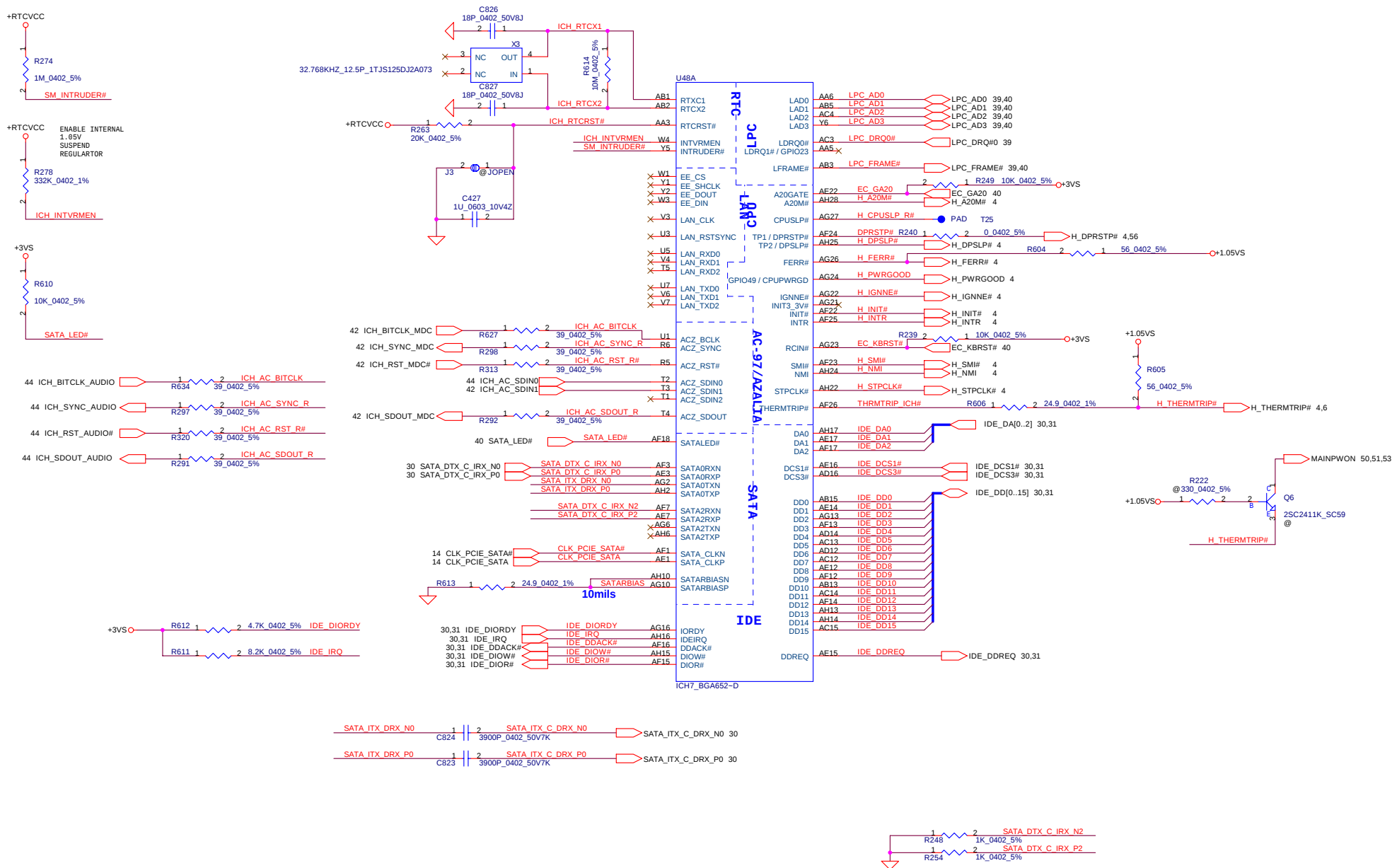


The diagram illustrates the internal wiring of a DVI-I to DVI-D adapter. It shows the connection between a DVI-I connector (left) and a DVI-D connector (right). The wiring includes signal paths for TMDS data (TMDs_DATA0+ to TMDs_DATA5+), clock (TMDs_Clock+ and TMDs_Clock-), and auxiliary signals (DVI_TXC+, DVI_TXC-, DVI_DET). Power planes (+5V, GND) and shielding (TMDS_DATA2/4 shield, TMDS_DATA1/3 shield, TMDS_DATA0/5 shield, TMDS_Clock shield) are also indicated. Component values like resistors (R481, R482, R2, R7) and capacitors (C1) are specified.

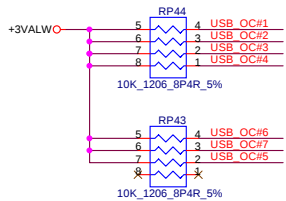
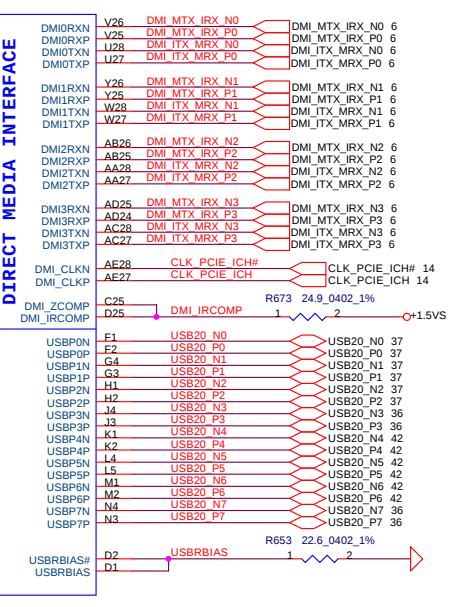
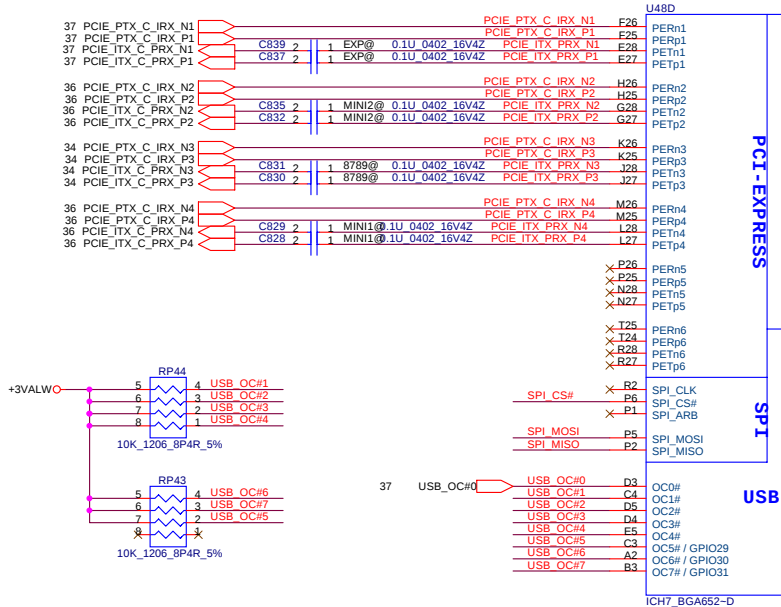
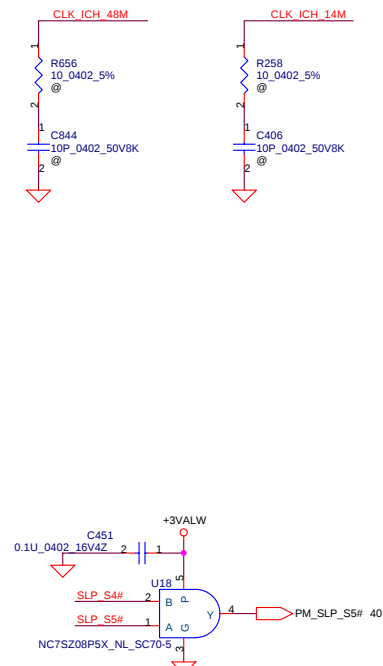
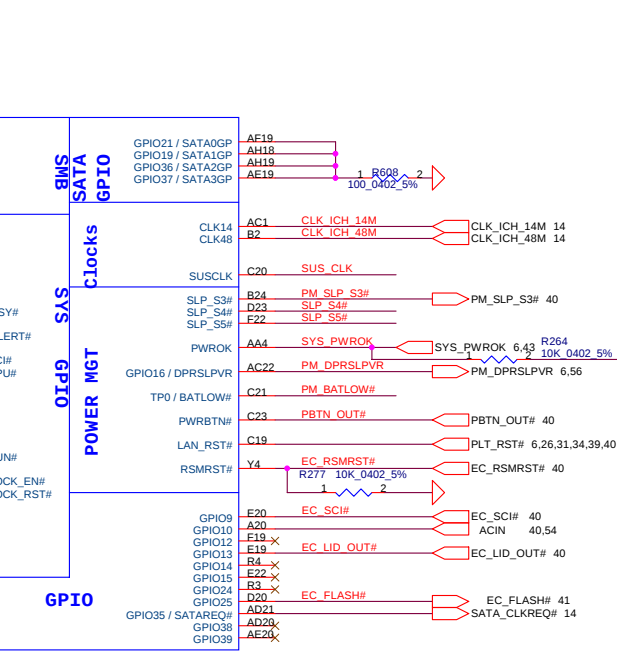
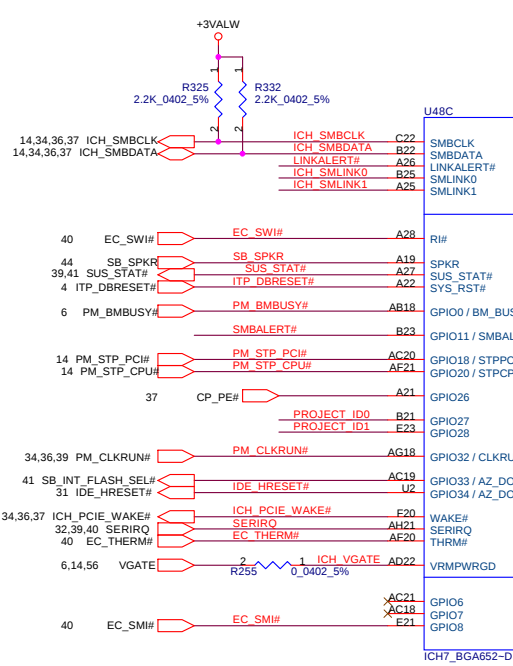
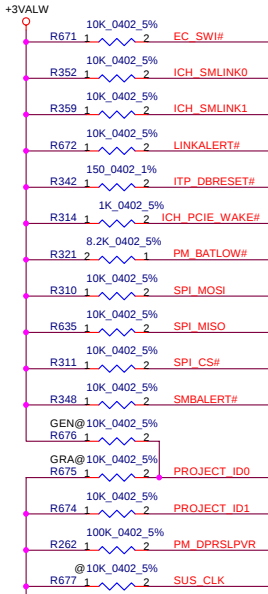
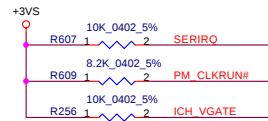
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		Size	Document Number					Rev
		HBQ60 LA-3191P					1.0	
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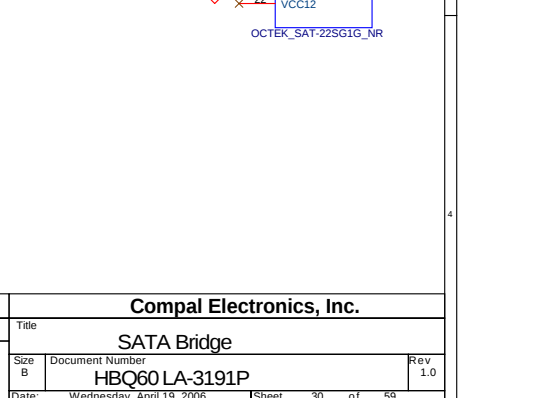
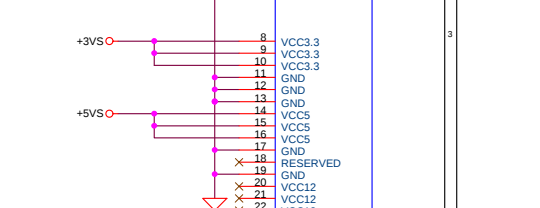
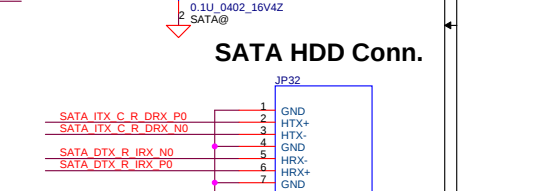
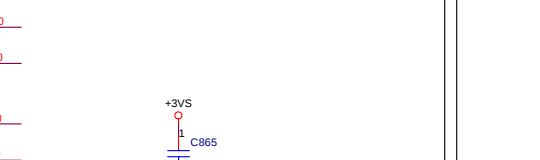
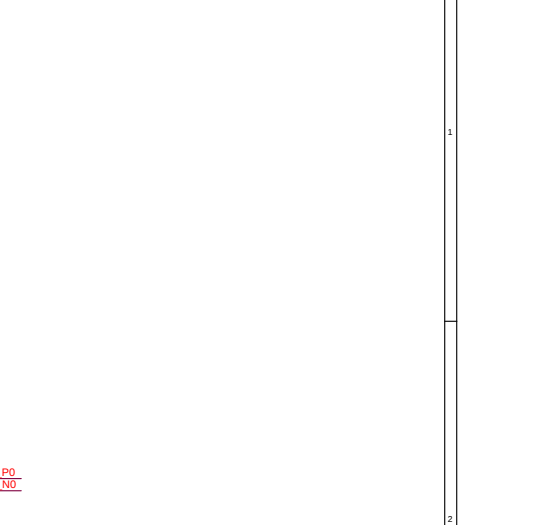
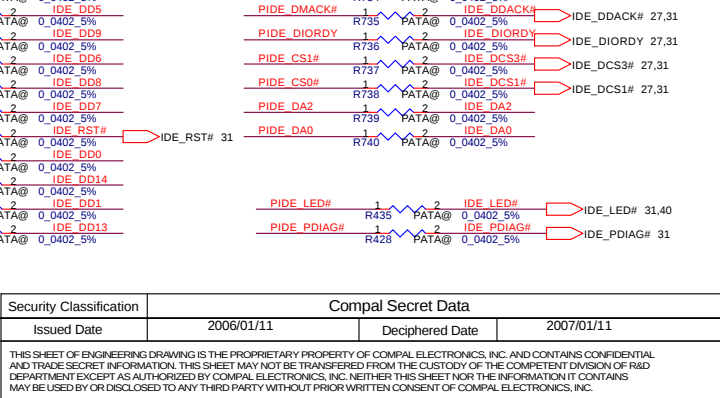
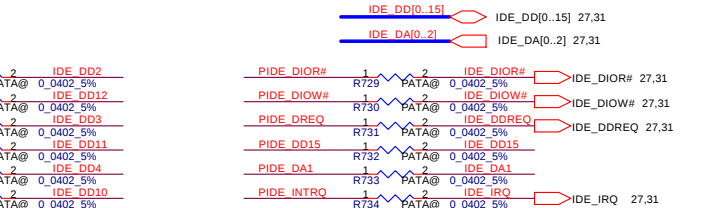
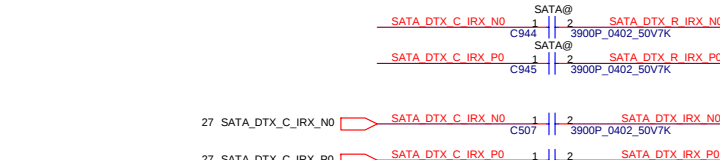
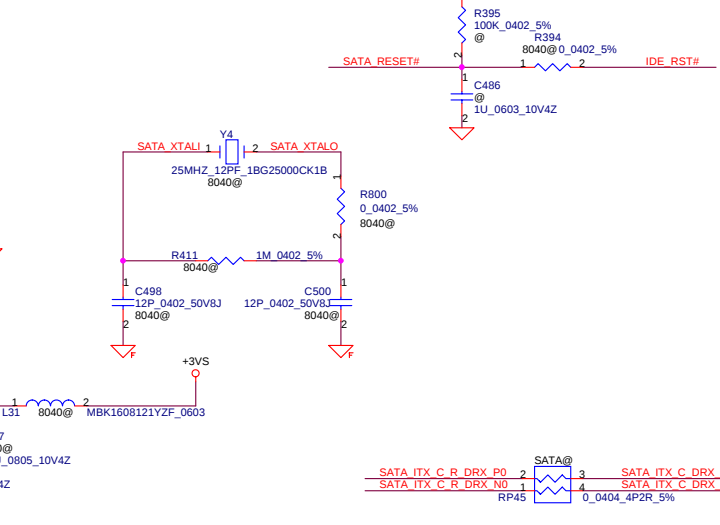
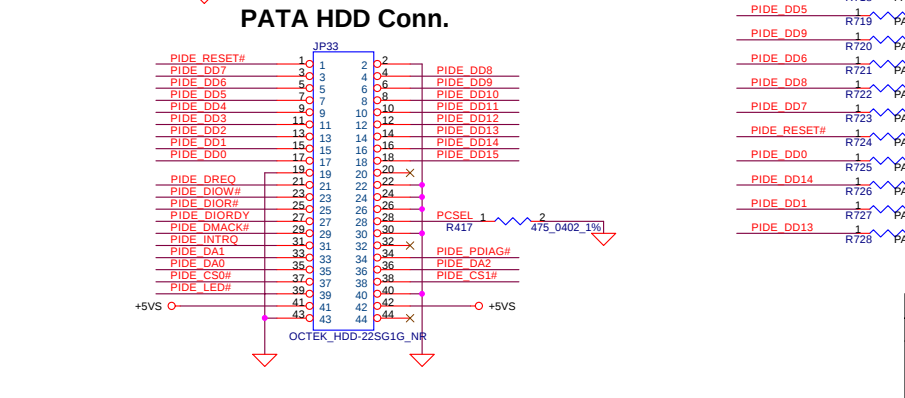
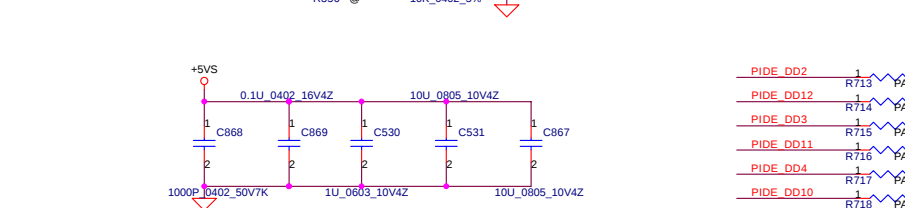
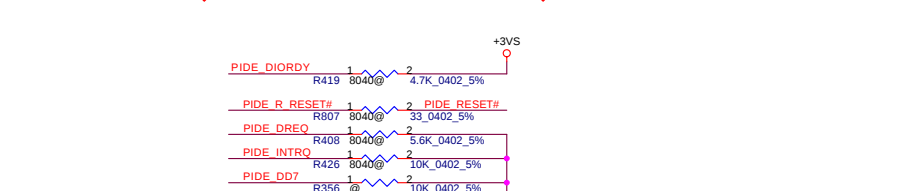
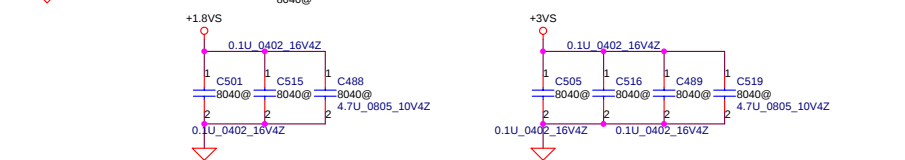
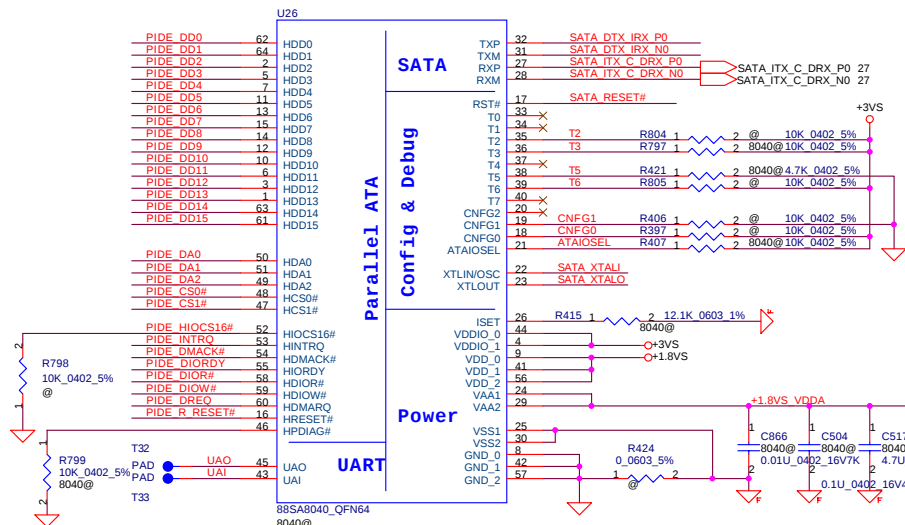
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Issued Date	2006/01/11	Deciphered Date	2007/01/11	Title ICH7-M(1/4)			
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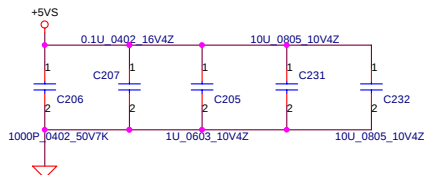
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				Custom	HBQ60 LA-3191P
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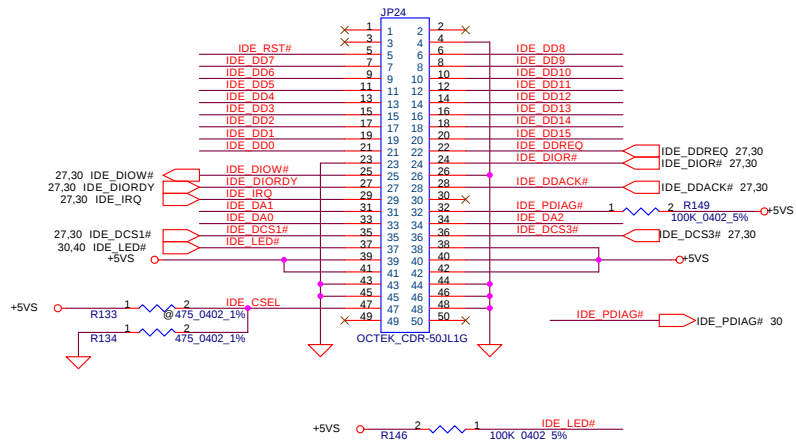
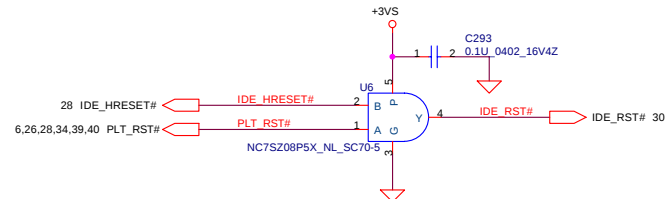
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				Customer		HBQ60 LA-3191P		1.0	
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								SATA Bridge			
								HBQ60 LA-3191P			
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								Date: Wednesday, April 19, 2006			
								Sheet 30 of 59			

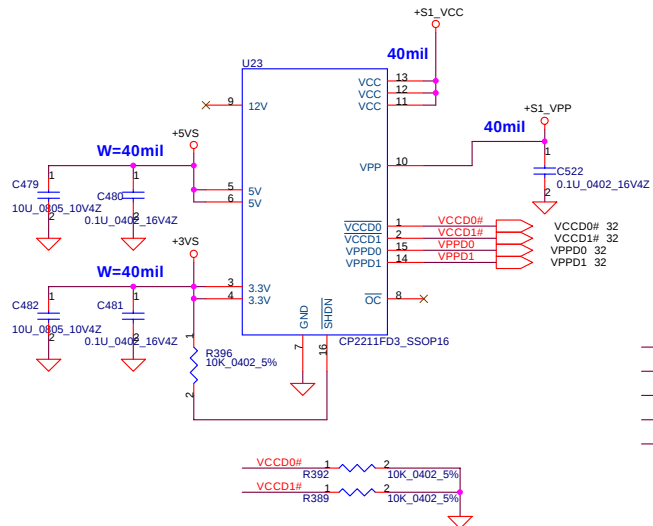


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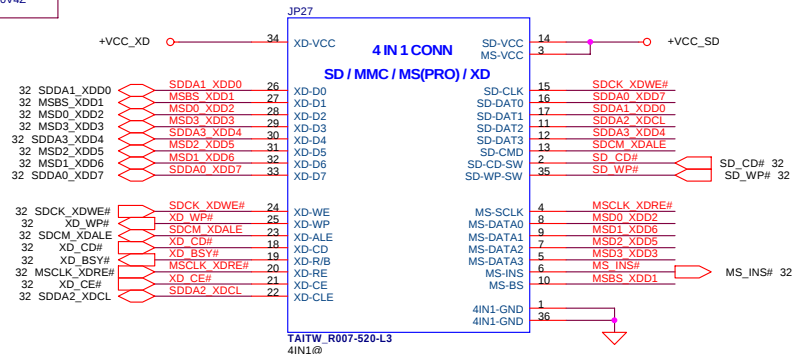
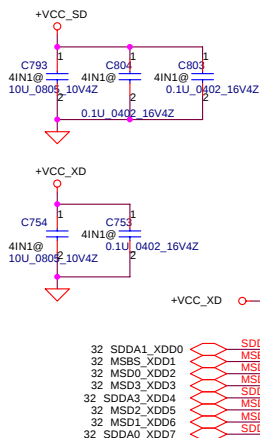
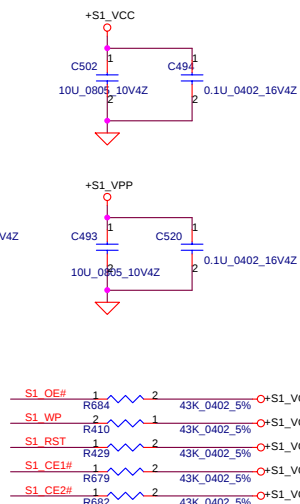
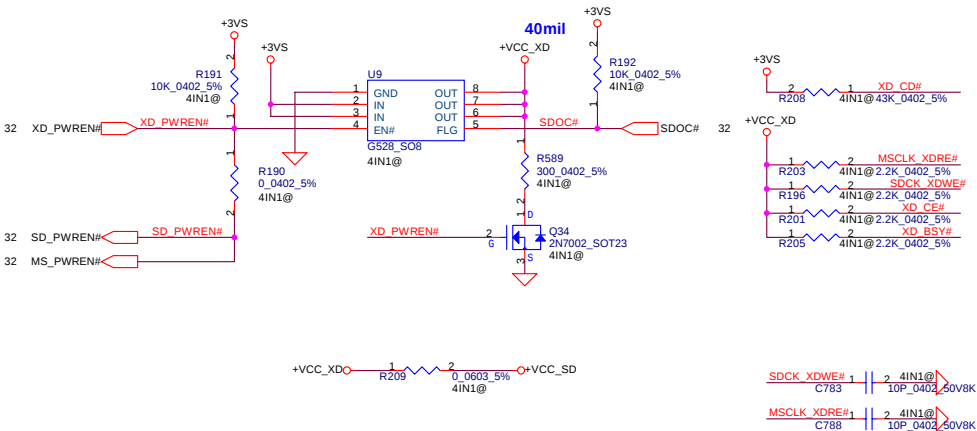


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				Date:	Wednesday, April 19, 2006	Sheet 31 of 59

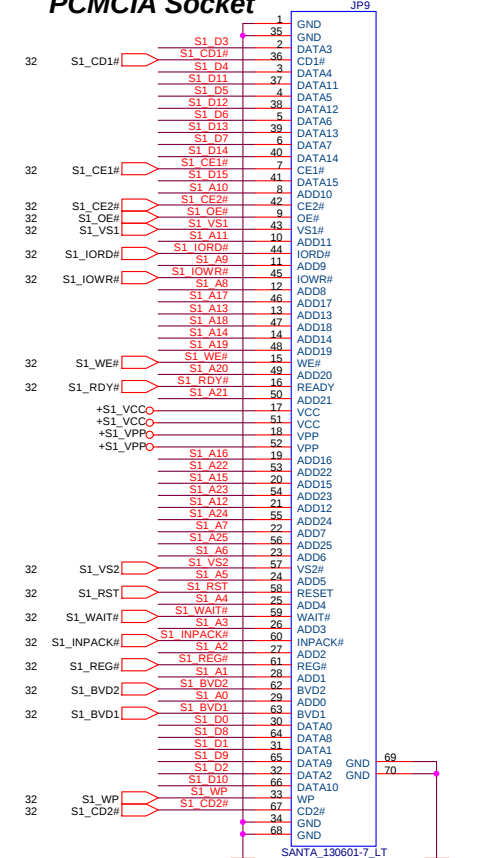
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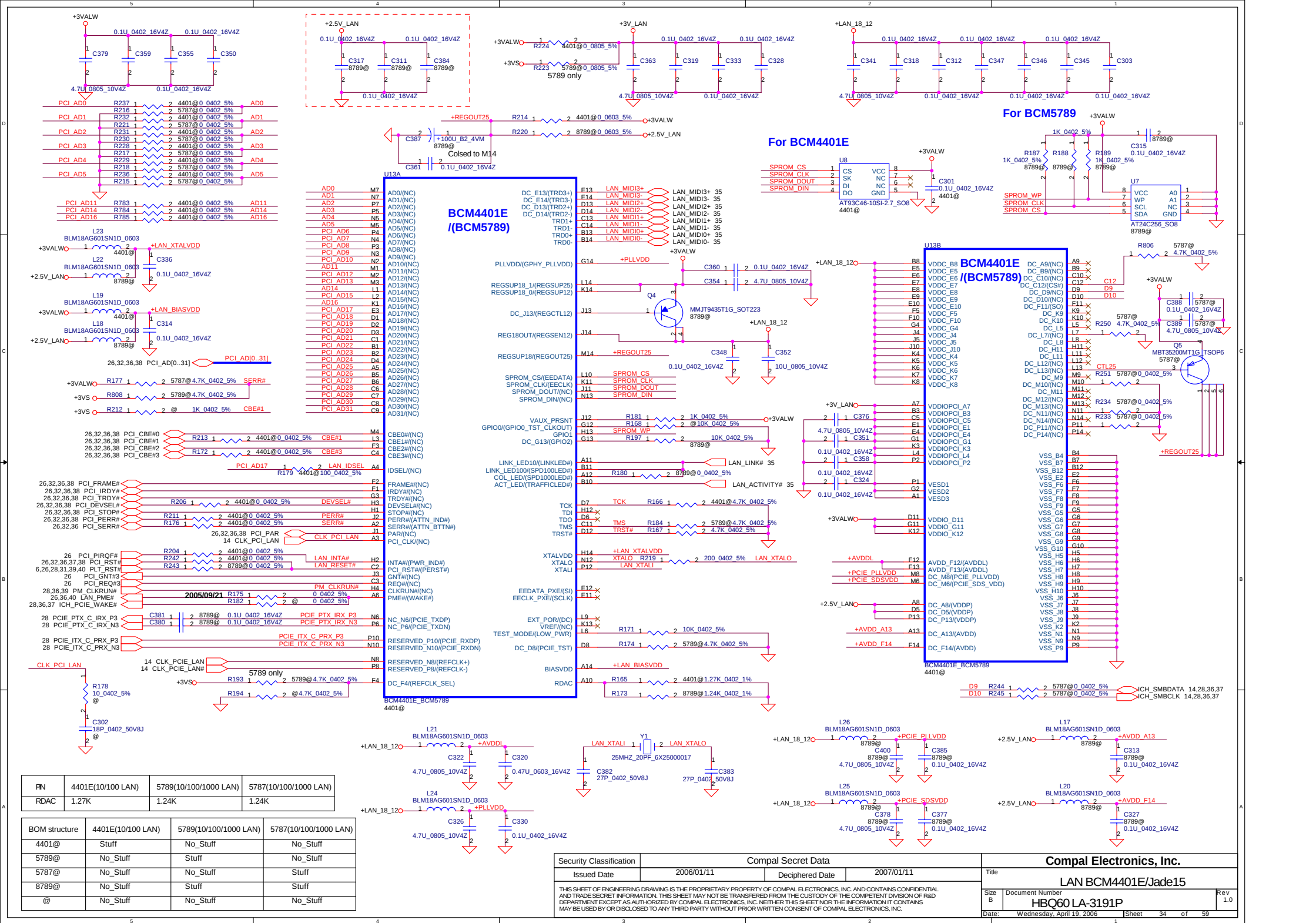
SD/MS Power Control
XD Power Control



PCMCIA Socket



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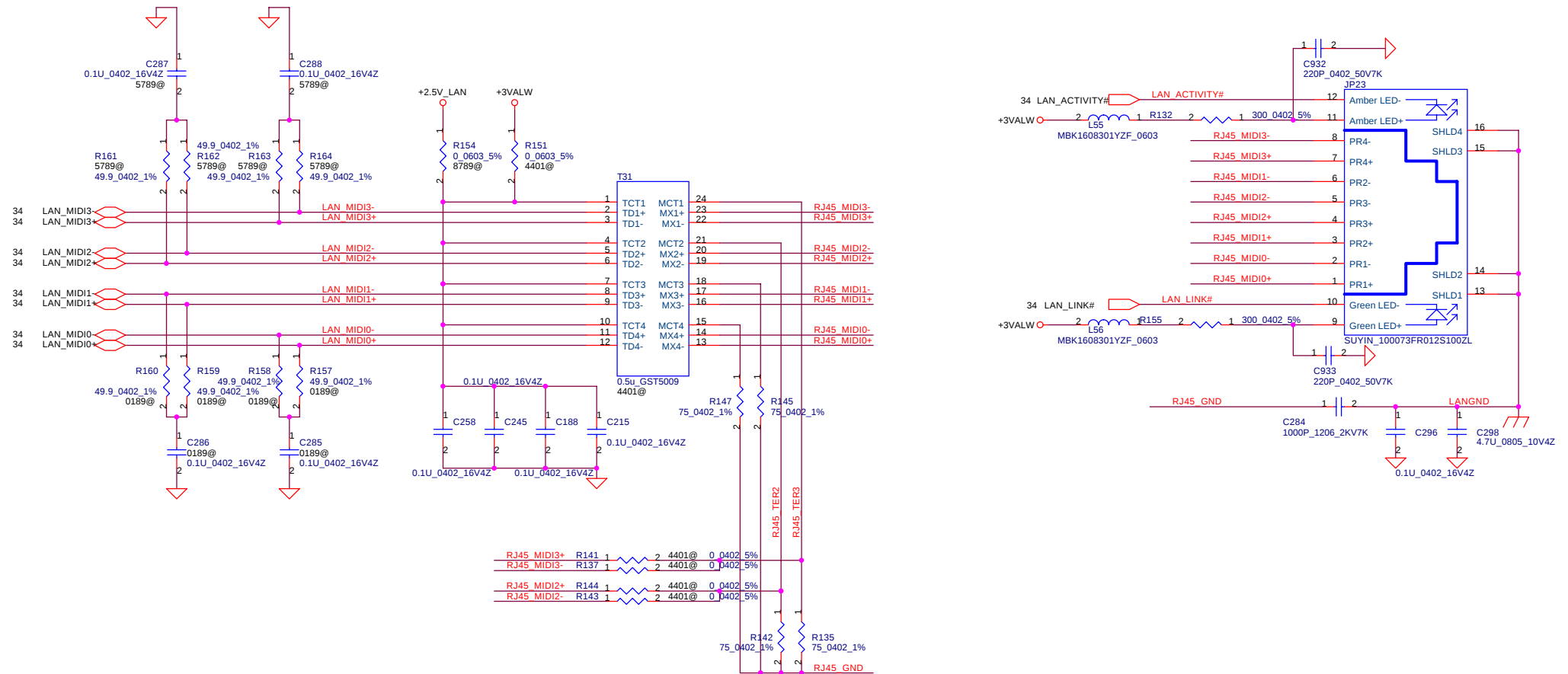


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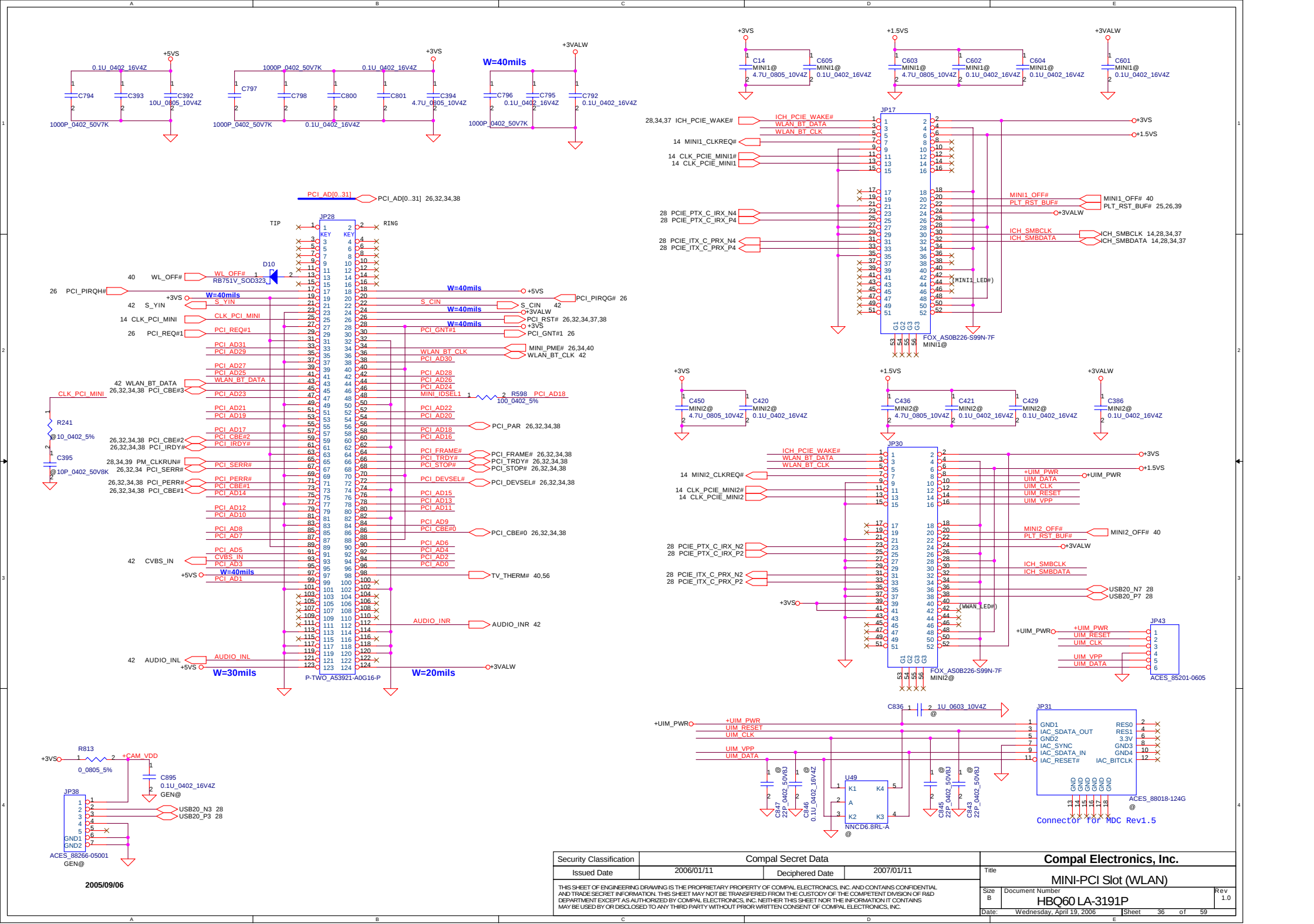
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5787@	No_Stuff	No_Stuff	Stuff
8789@	No_Stuff	Stuff	Stuff
@	No_Stuff	No_Stuff	No_Stuff

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				Size B Document Number HBQ60 LA-3191P			
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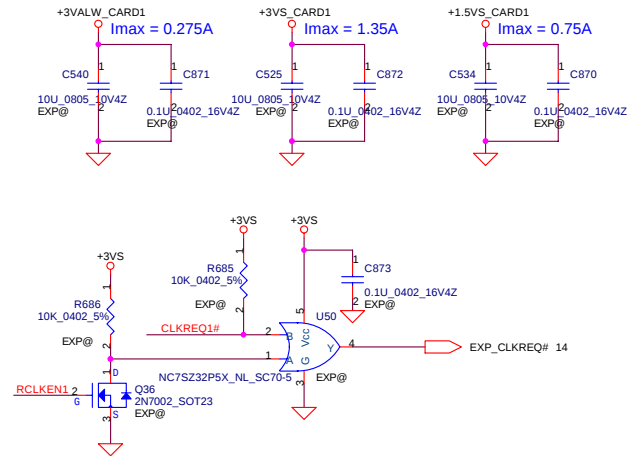
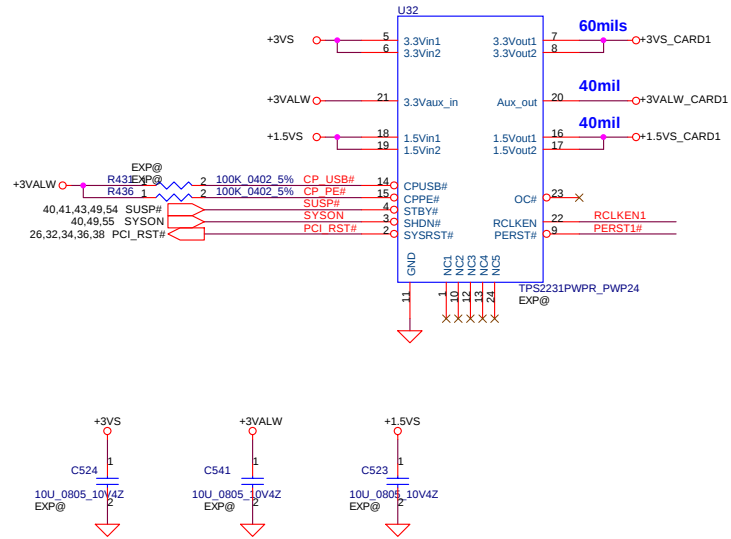
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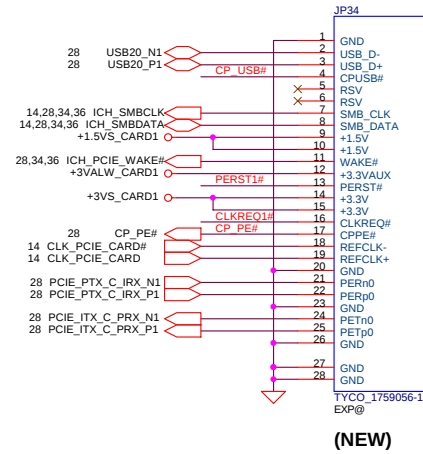
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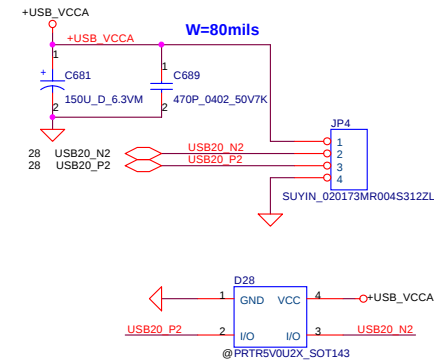
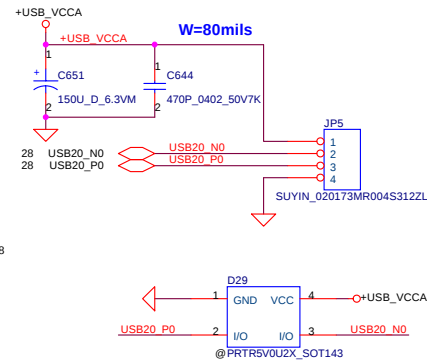
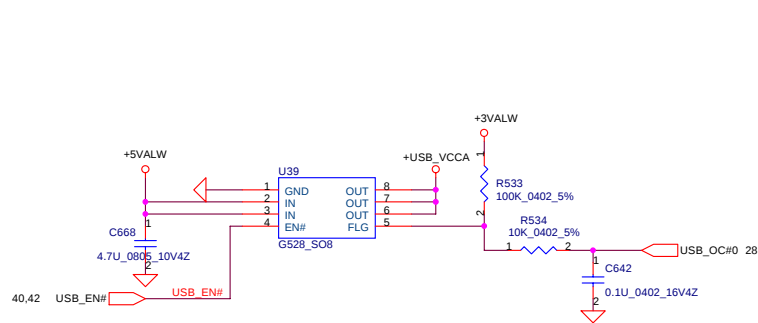
New Card Power Switch



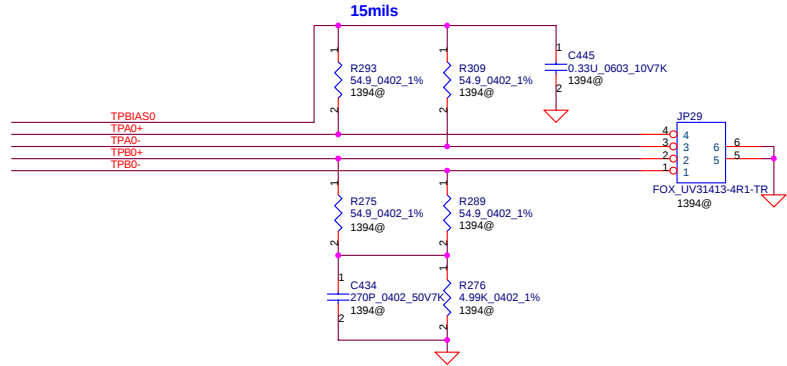
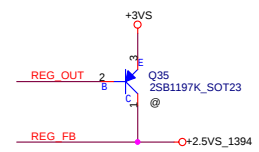
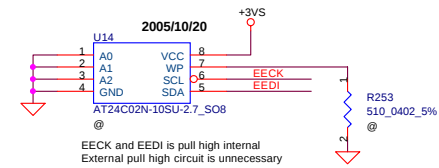
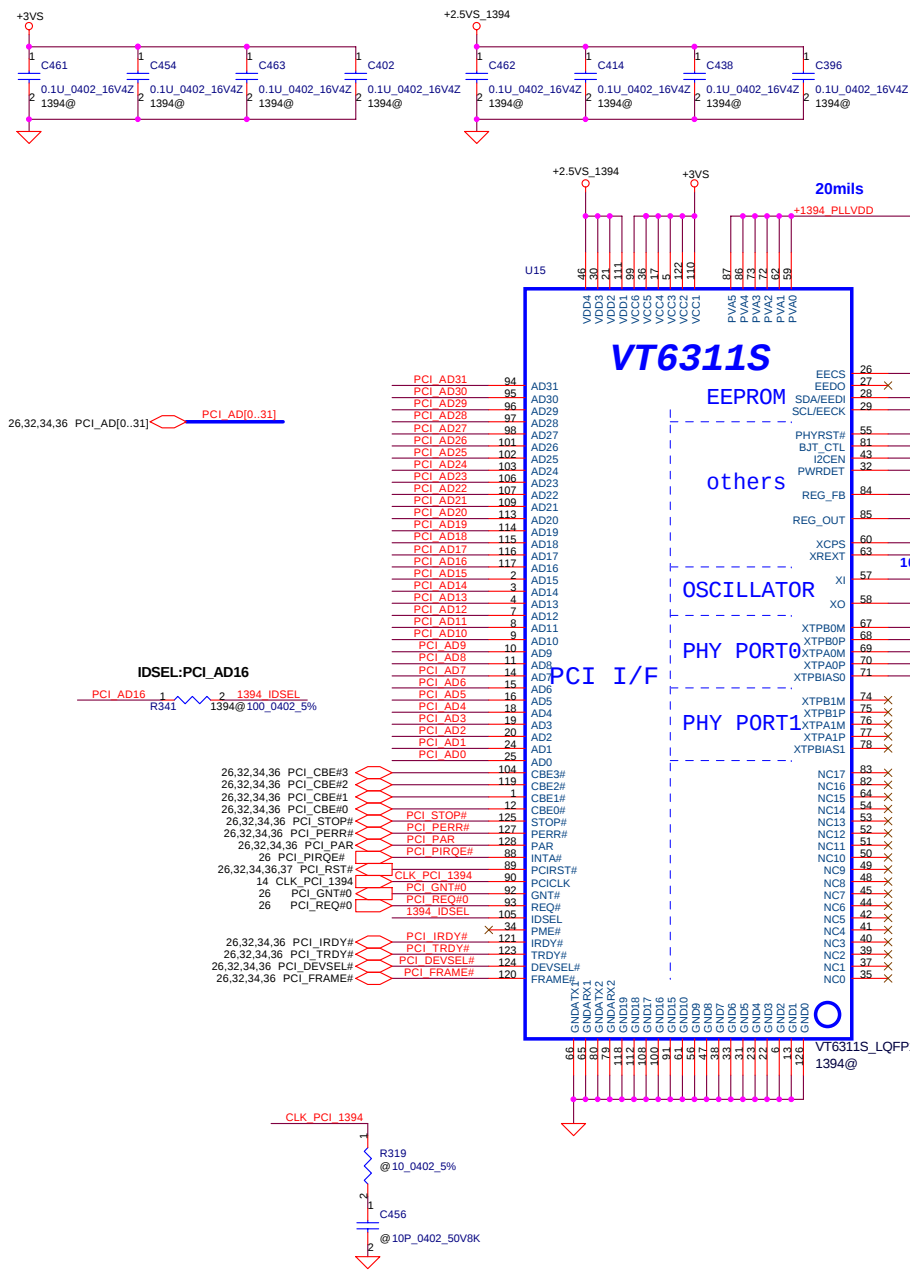
New Card Socket (Left)



USB CONN. 1 & 2

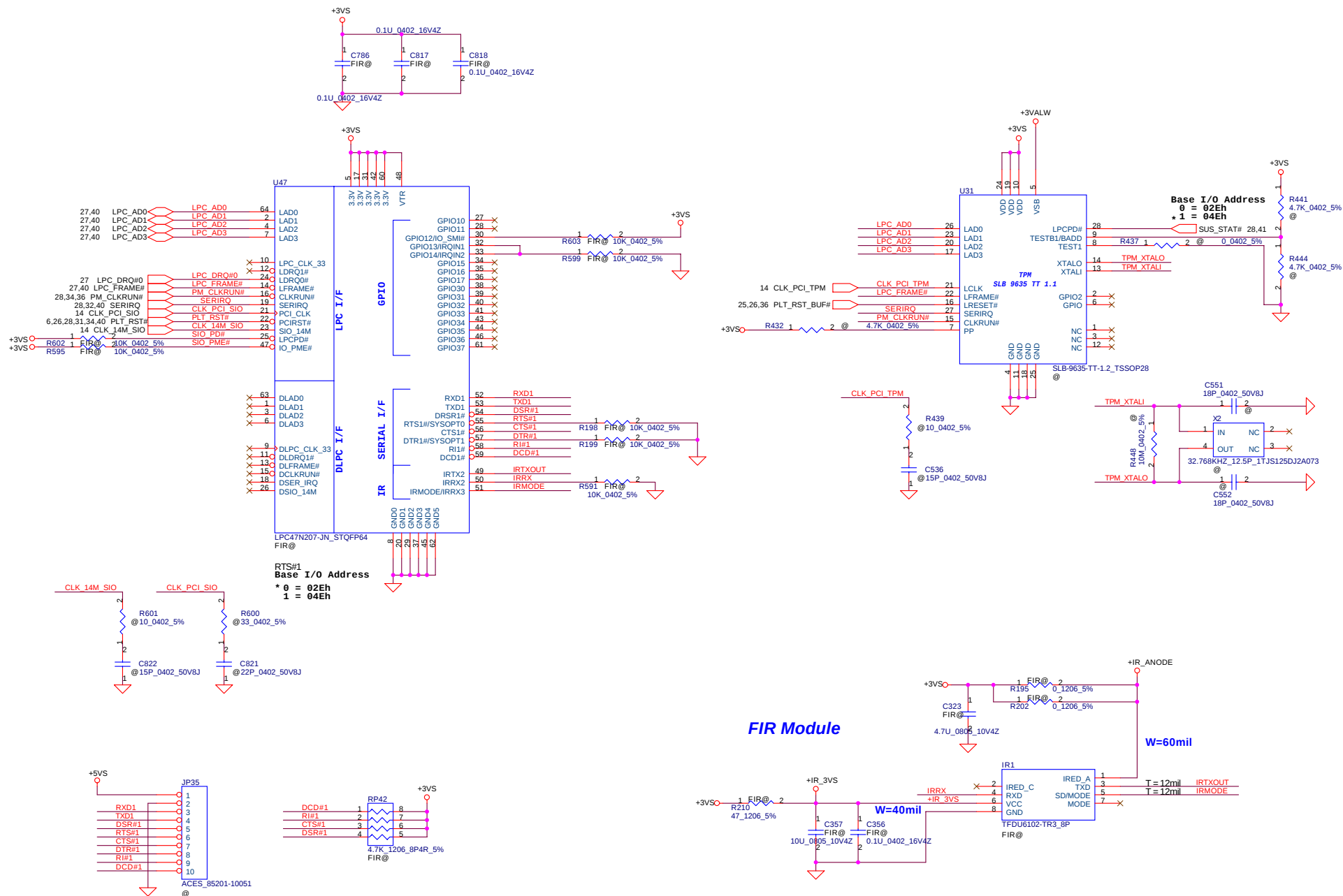


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				Date	Wednesday, April 19, 2006	Sheet 37 of 50

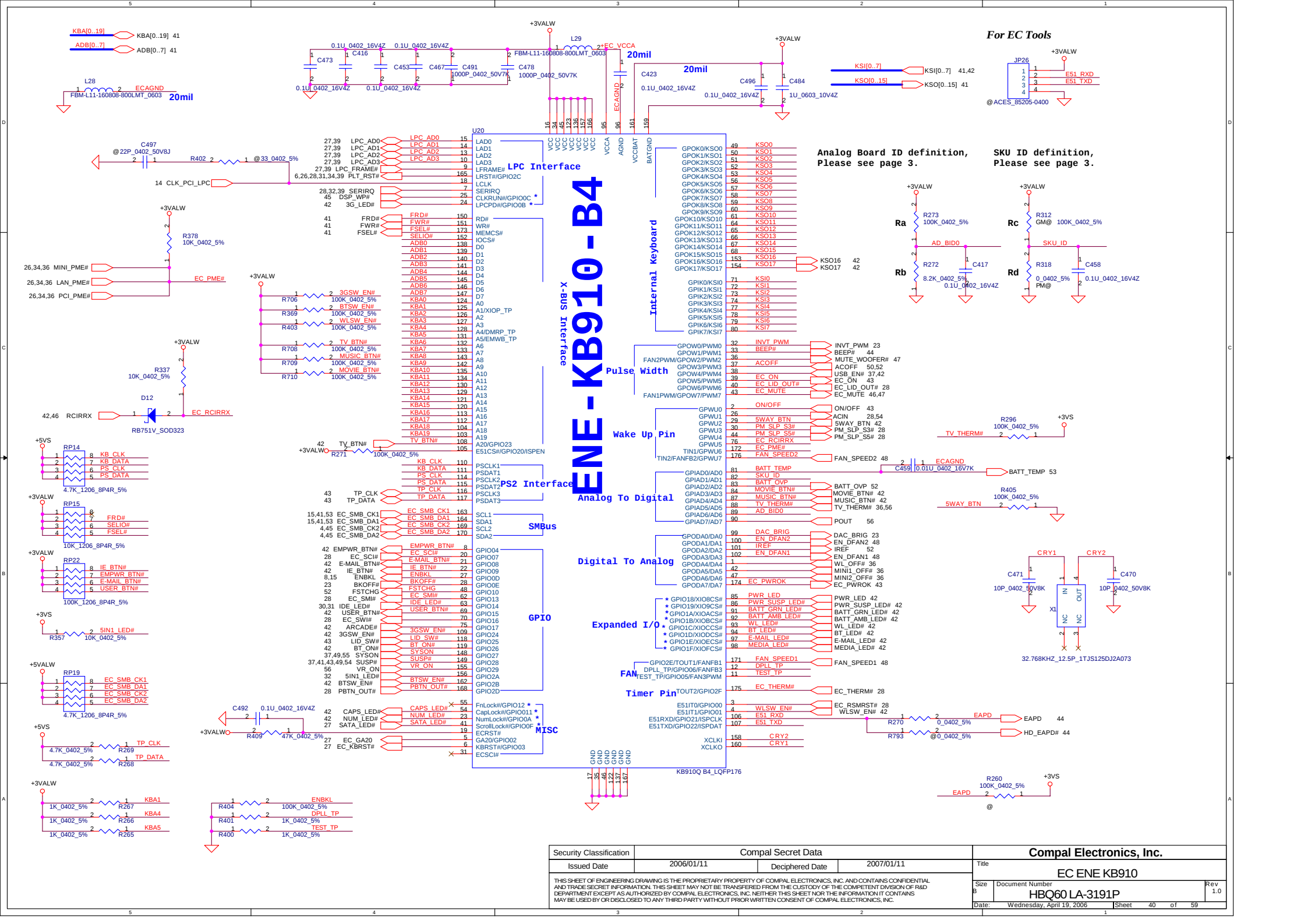


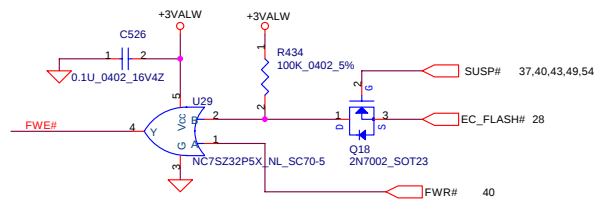
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2006/01/11		Deciphered Date		2007/01/11		Title			
								IEEE1394 VIA VT6311S			
								Size		Document Number	
								B		HBQ60 LA-3191P	
								Date		Wednesday, April 19, 2006	
										Sheet 38 of 59	
										Rev 1.0	

SUPER I/O SMsC LPC47N207

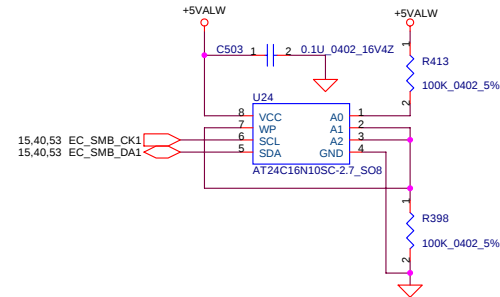


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				B	HBQ60 LA-3191P	1.0
				Date	Wednesday, April 19, 2006	Sheet 39 of 59

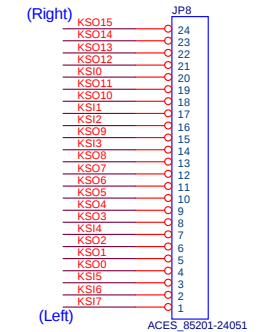
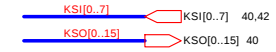




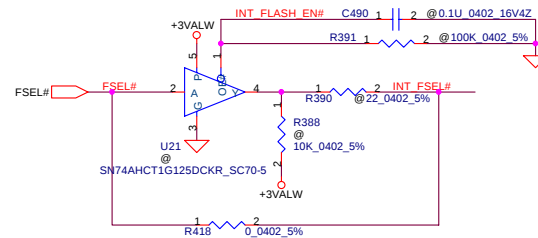
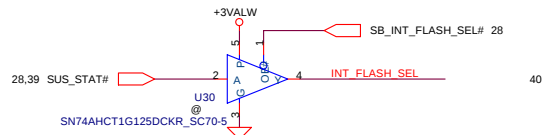
Check PCB Footprint



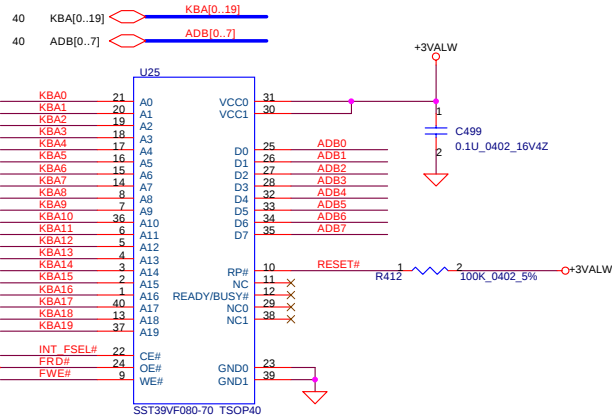
INT_KBD Conn.



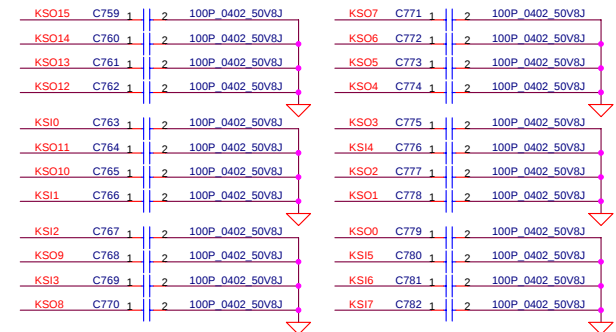
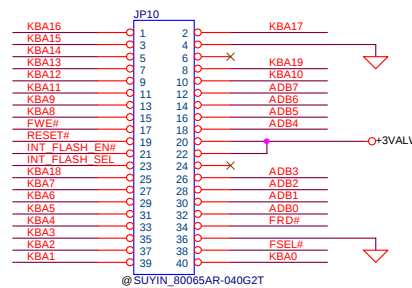
FOR DEBUG ONLY



1MB Flash ROM

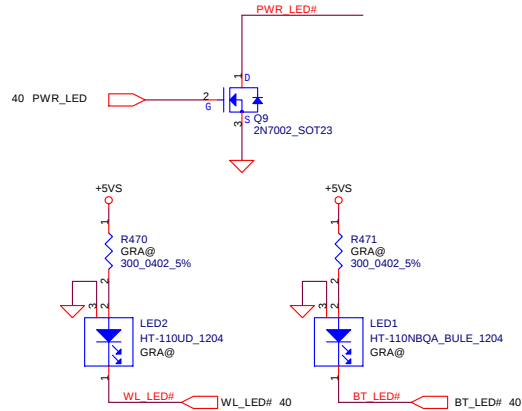
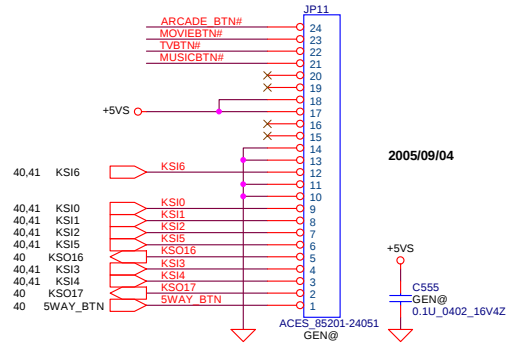


1MB ROM Socket

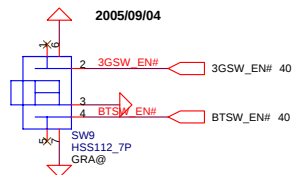


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						Size B	Document Number			Rev 1.0	
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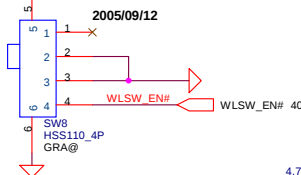
To CD-PLAY/B Conn.



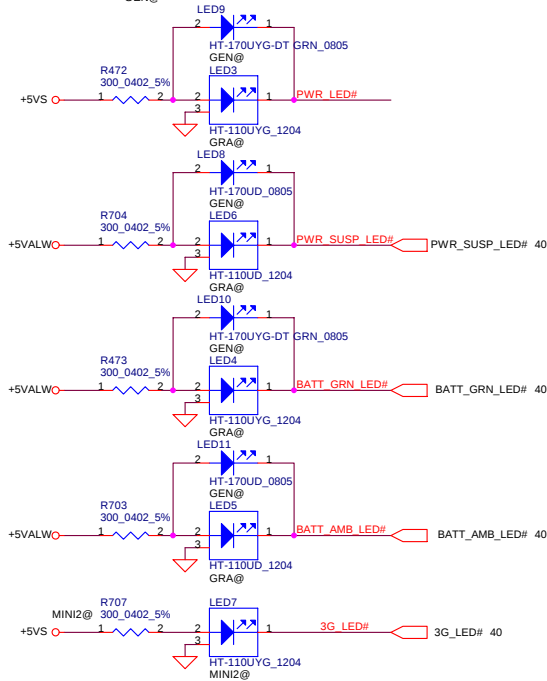
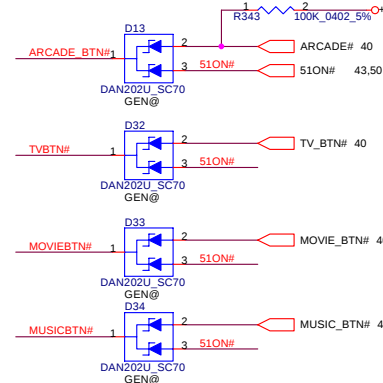
BT_SW & 3G_SW



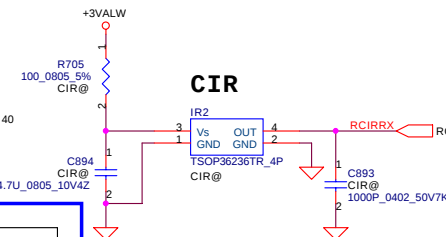
WL_SW



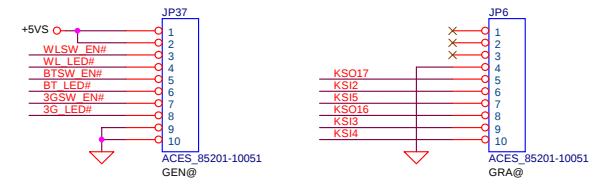
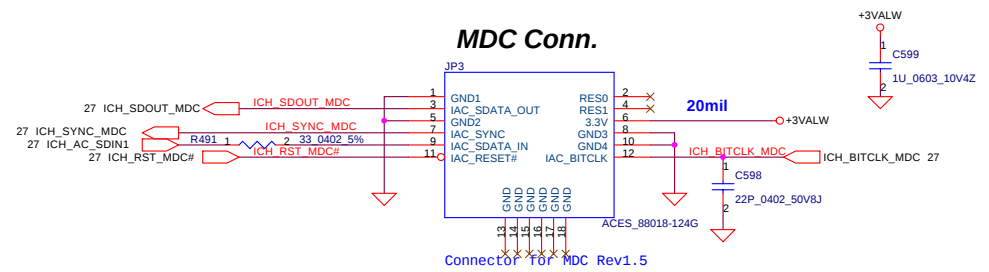
Geneva			Grapevine		
	KSO16	KSO17		KSO16	KSO17
KSI0	VOL_UP	LEFT			
KSI1	RIGHT	VOL_DOWN			
KSI2	PLAY	ENTER	KSI2	PLAY	
KSI3	STOP		KSI3	STOP	VOL_UP
KSI4	NEXT		KSI4	NEXT	VOL_DOWN
KSI5	REV		KSI5	REV	ARCADE_TV
KSI6		RECORD			



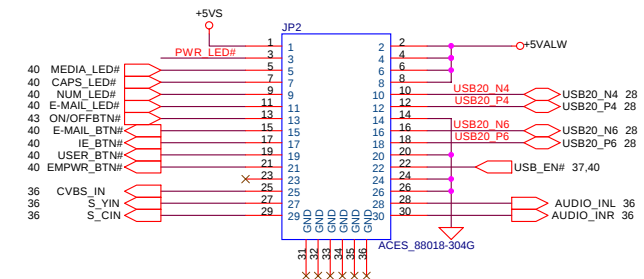
CIR



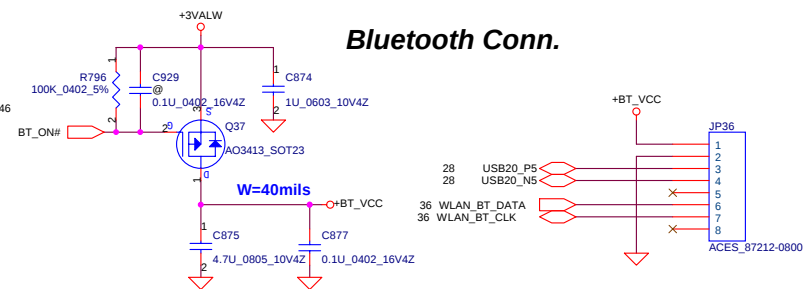
MDC Conn.



To LED/B Conn.

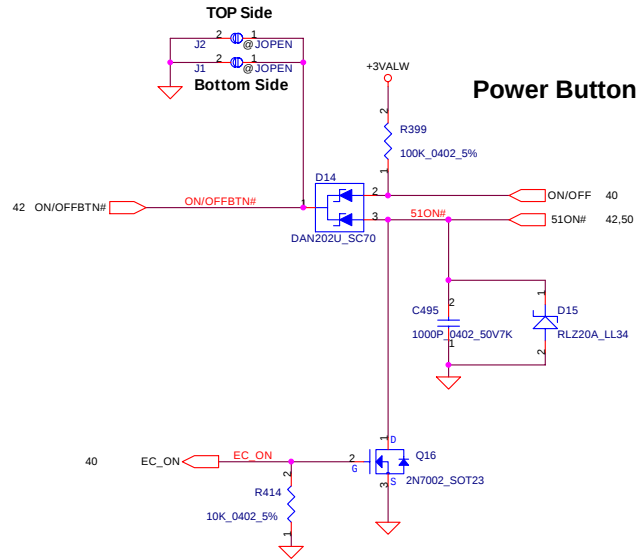


Bluetooth Conn.

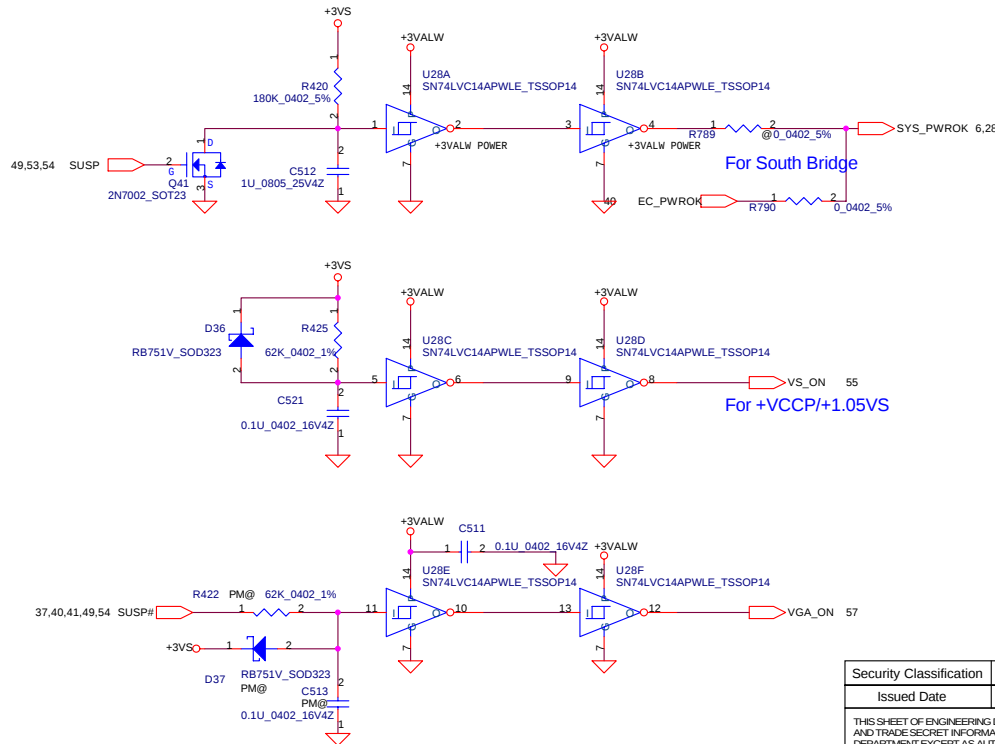


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								Size B	Document Number		Rev 1.0
								HBQ60 LA-3191P			
Date:		Wednesday, April 19, 2006			Sheet		42 of 59				

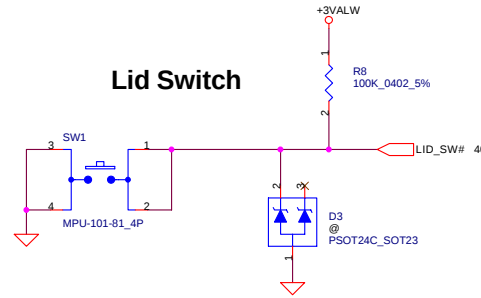
ON/OFF switch



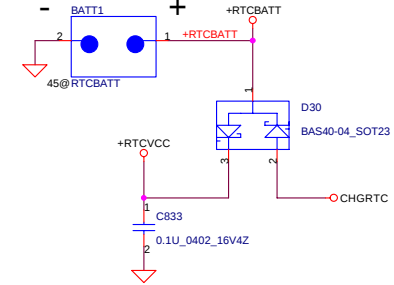
Power ON Circuit



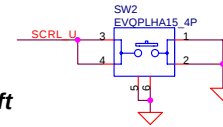
Lid Switch



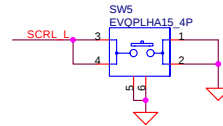
RTC Battery



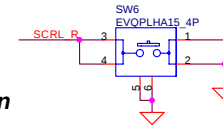
Scroll Up



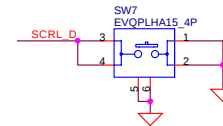
Scroll Left



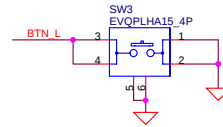
Scroll Right



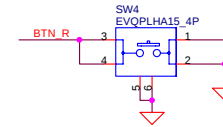
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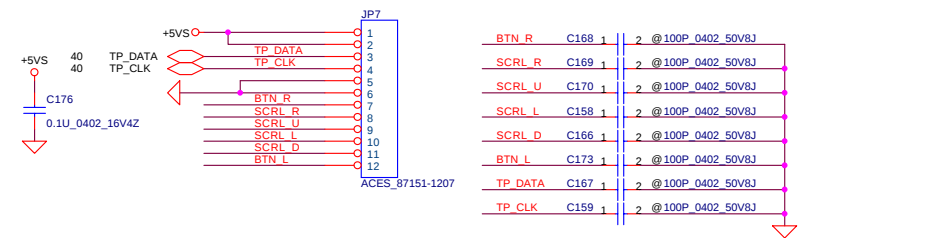
Left



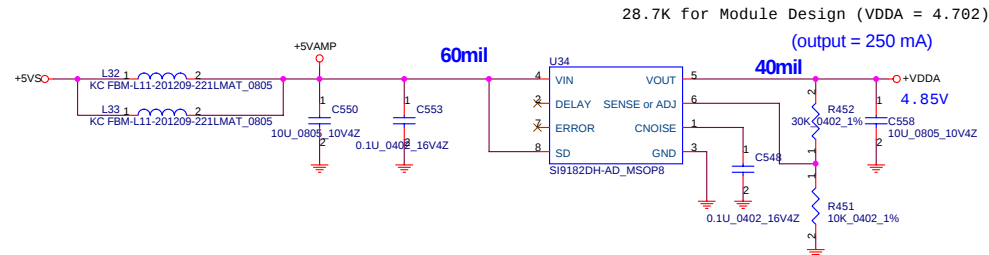
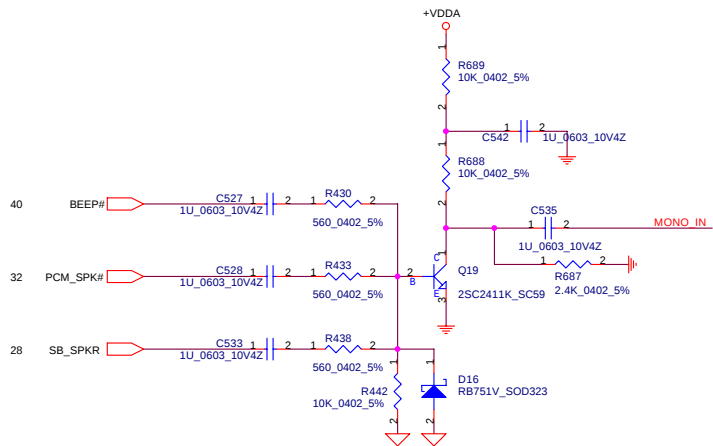
Right



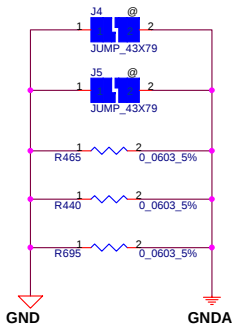
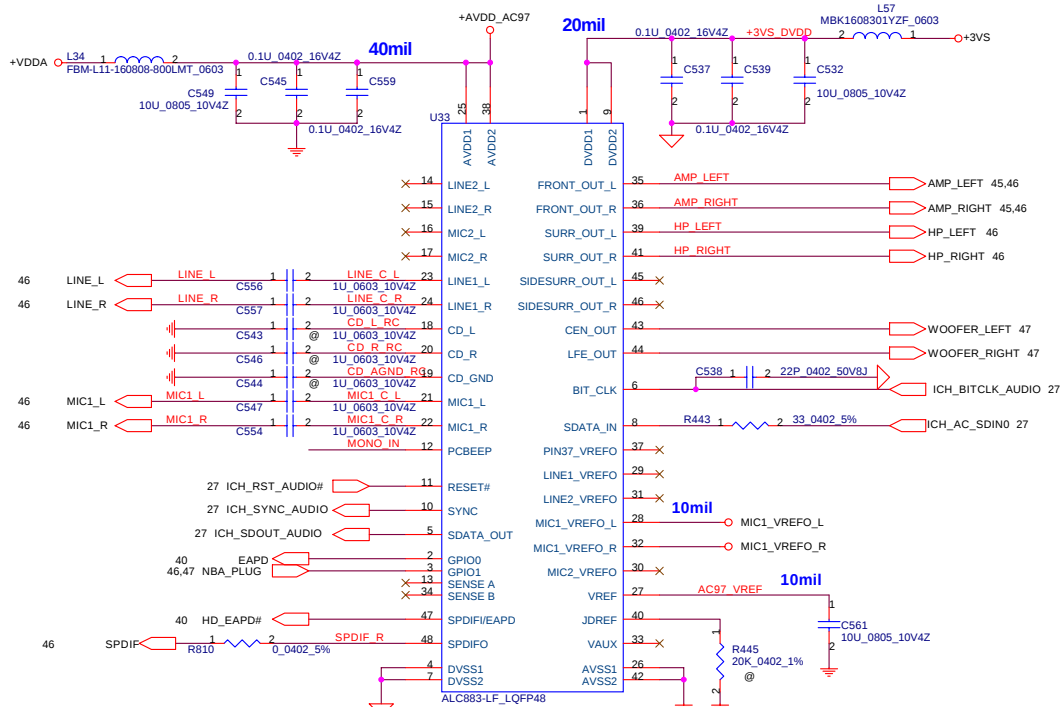
To TP/B Conn.



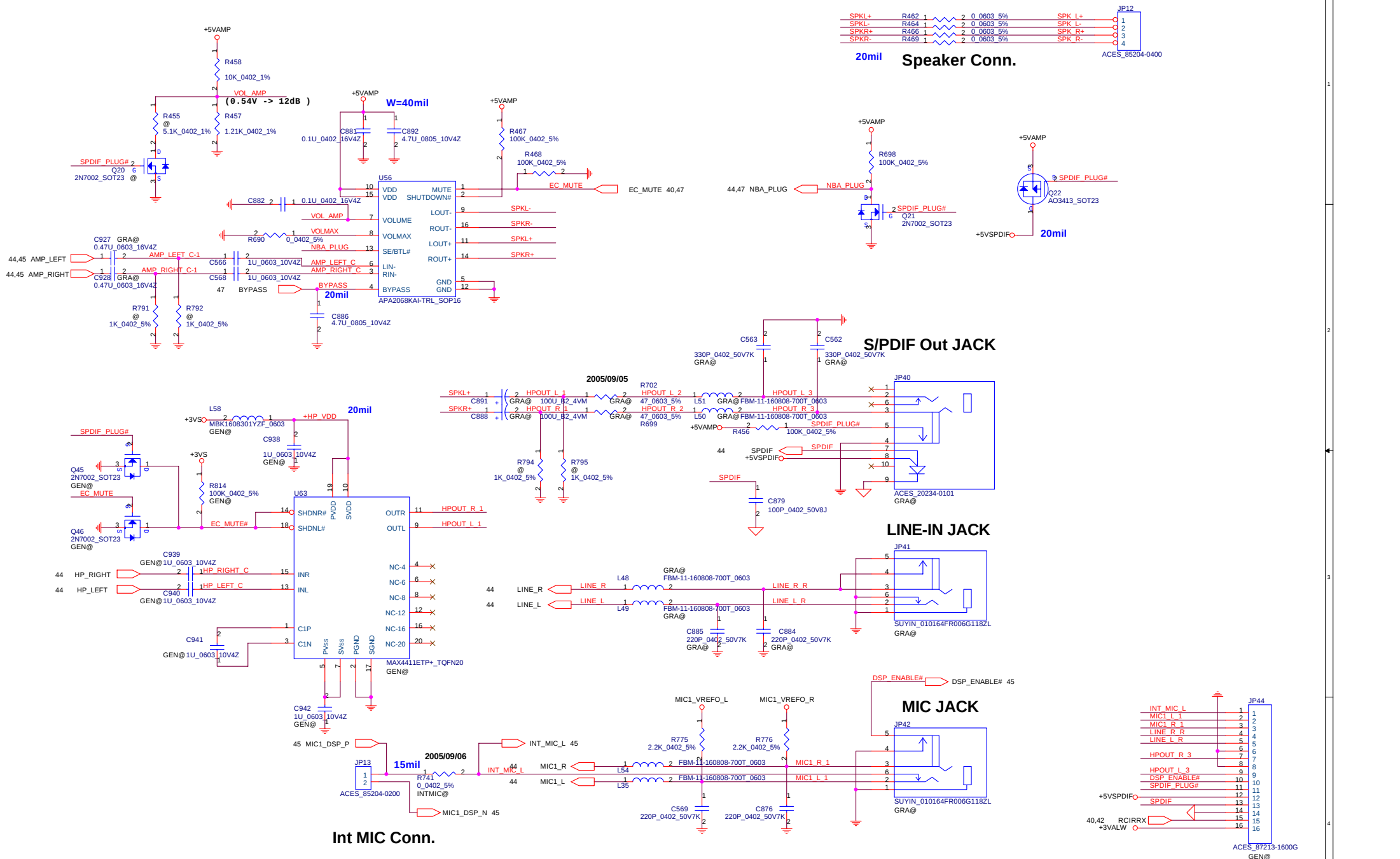
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HD Audio Codec



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Int MIC Conn.

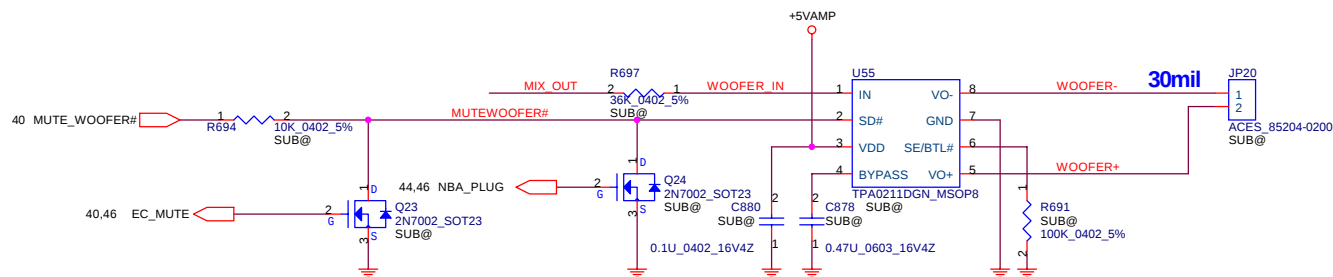
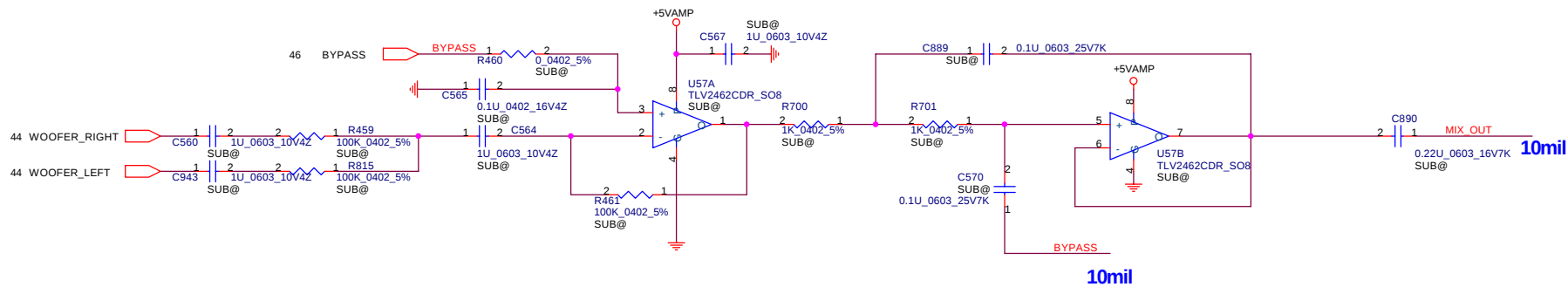
Speaker Conn.

SPDIF Out JACK

LINE-IN JACK

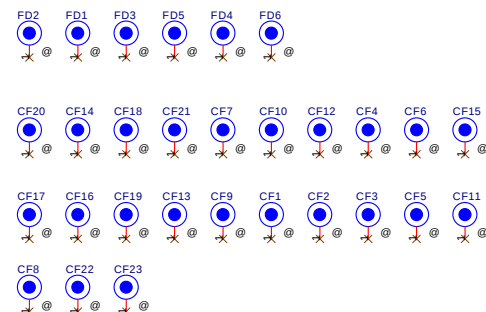
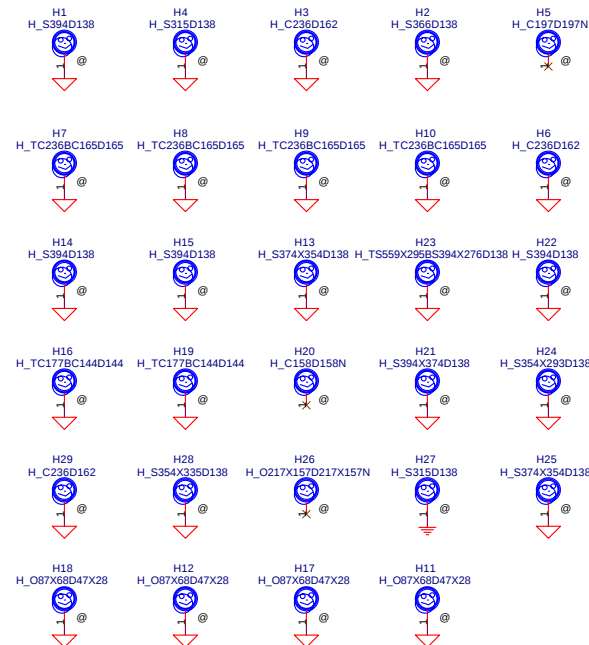
MIC JACK

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2006/01/11				2007/01/11				Amplifier & Audio Jack			
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								HBQ60 LA-3191P			
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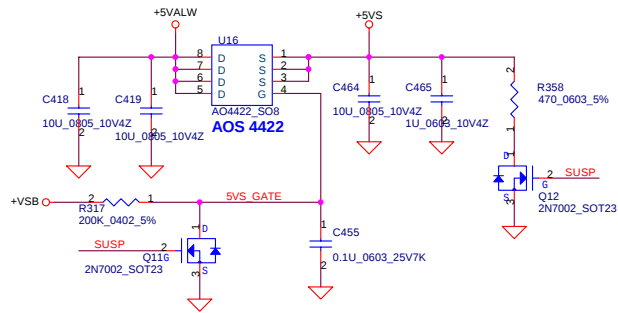
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/01/11	Deciphered Date	2007/01/11	Title	
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				Size B	Document Number
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				Rev	1.0

The schematic diagram illustrates the fan speed control circuit. It features a 5V power supply connected to a 100nF capacitor (C338) and a 100k resistor (R207). The 3V power supply is connected to a 100nF capacitor (C344). The 40-pin connector is connected to the fan speed control circuit. The circuit includes a 40-pin connector (40 EN_DFAN2) connected to the fan speed control circuit. The circuit is labeled with component values and part numbers.

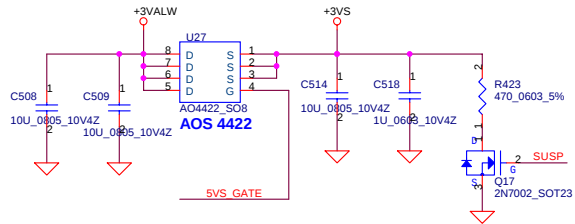


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				Date:	Wednesday, April 19, 2006	Sheet 48 of 59	

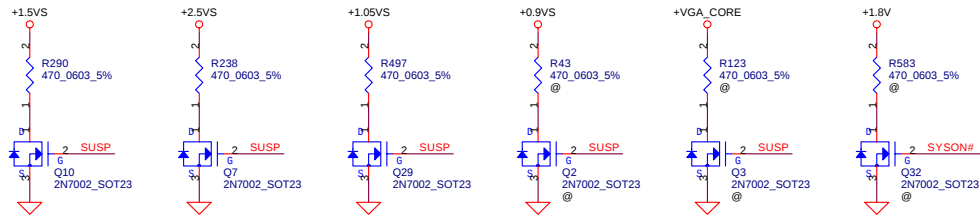
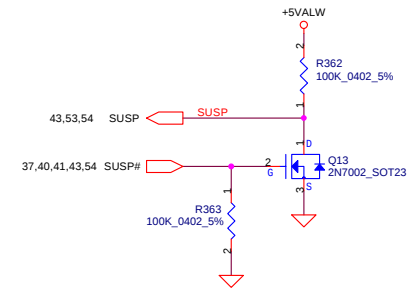
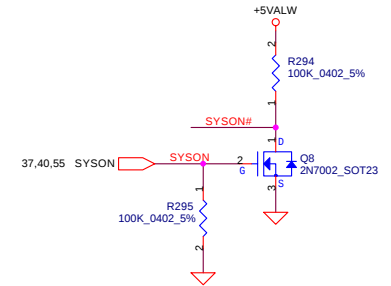
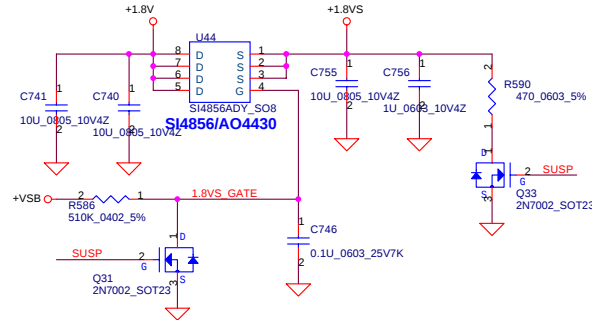
+5VALW TO +5VS



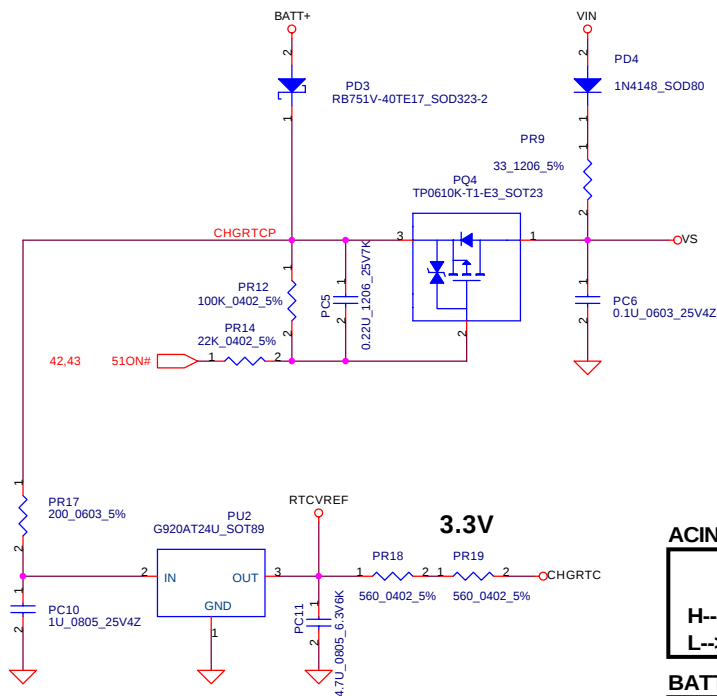
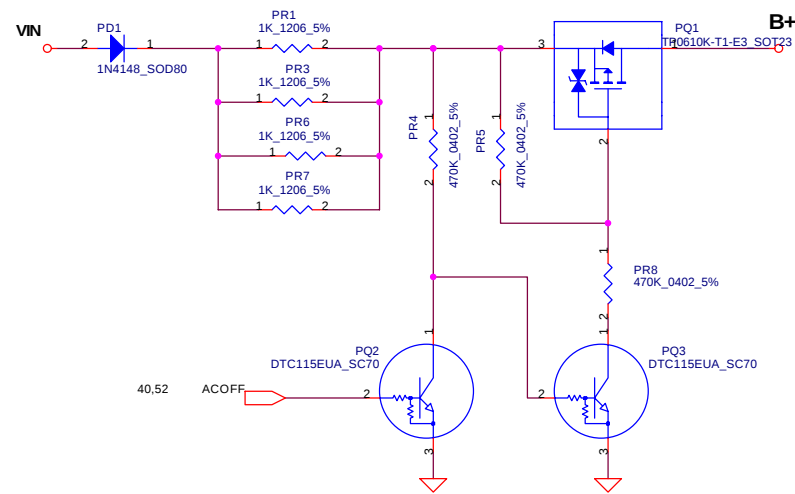
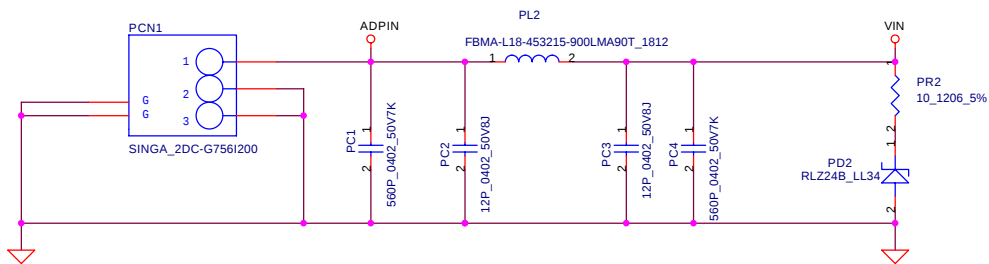
+3VALW TO +3VS



+1.8V to +1.8VS



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ACIN

Precharge detector

	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

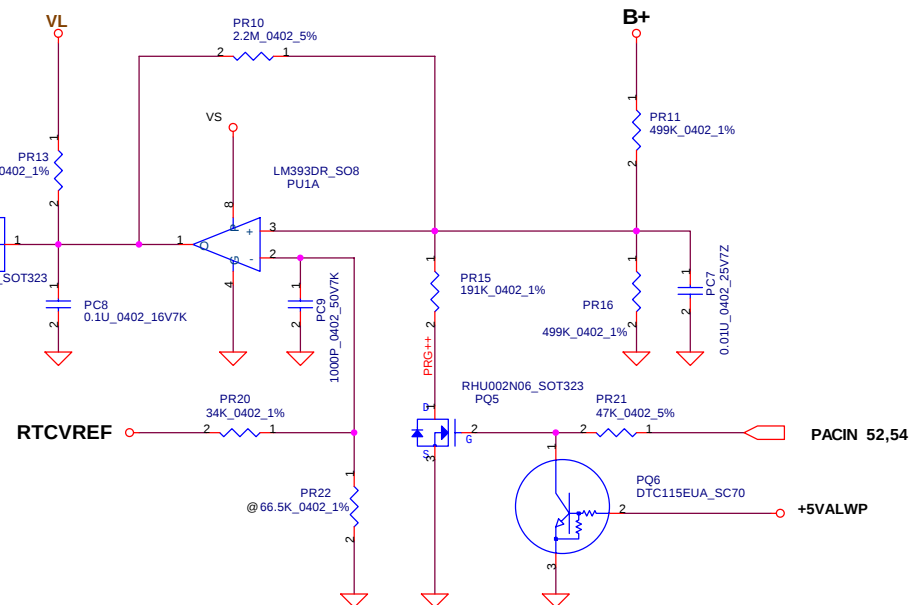
BATT ONLY

Precharge detector

	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

27,51,53 MAINPWON

52 ACON



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Issued Date

2006/01/11

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2007/01/11

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Title

DCIN/DECTOR/RTC

Size

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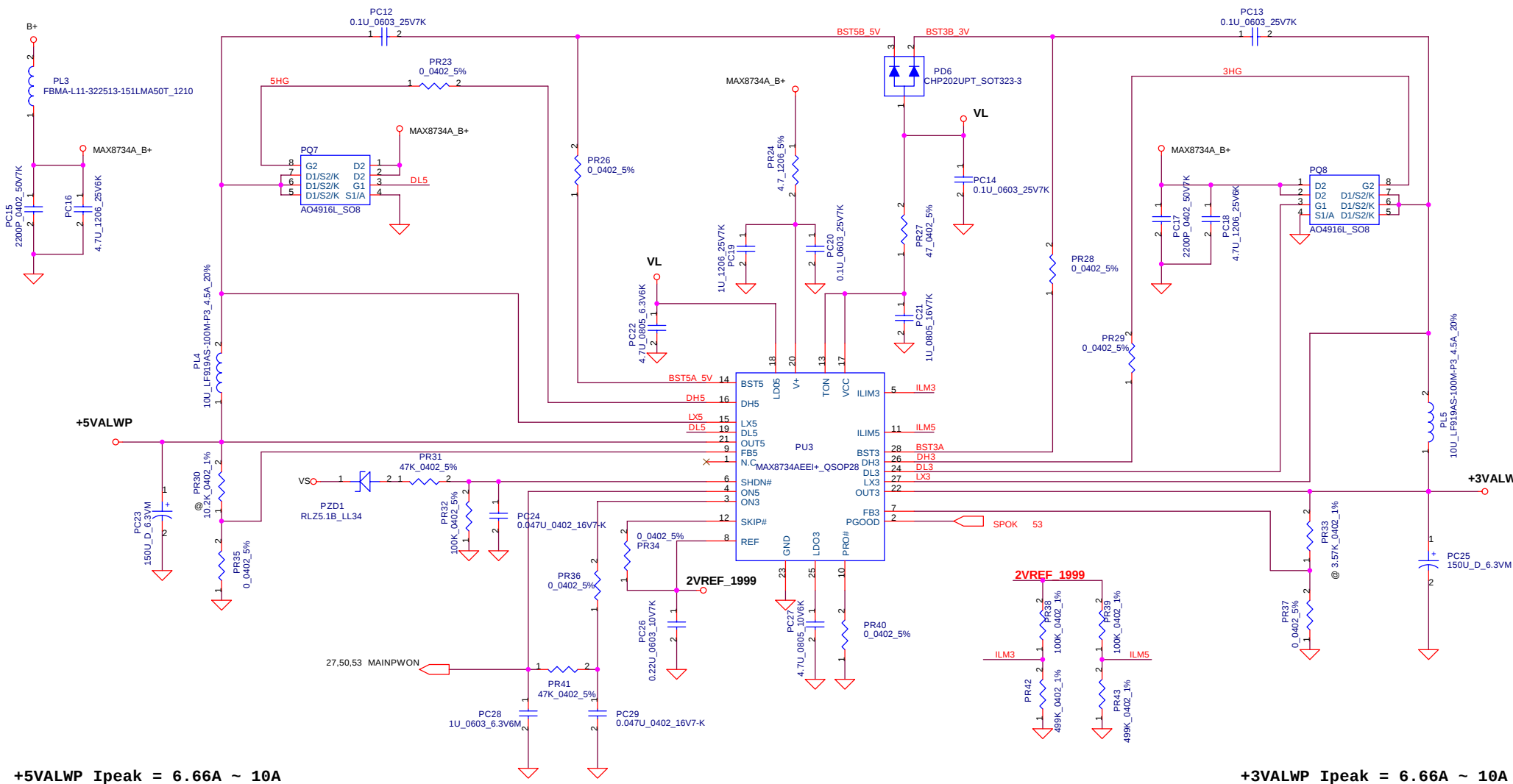
HBQ60 LA-3191P

Rev

1.0

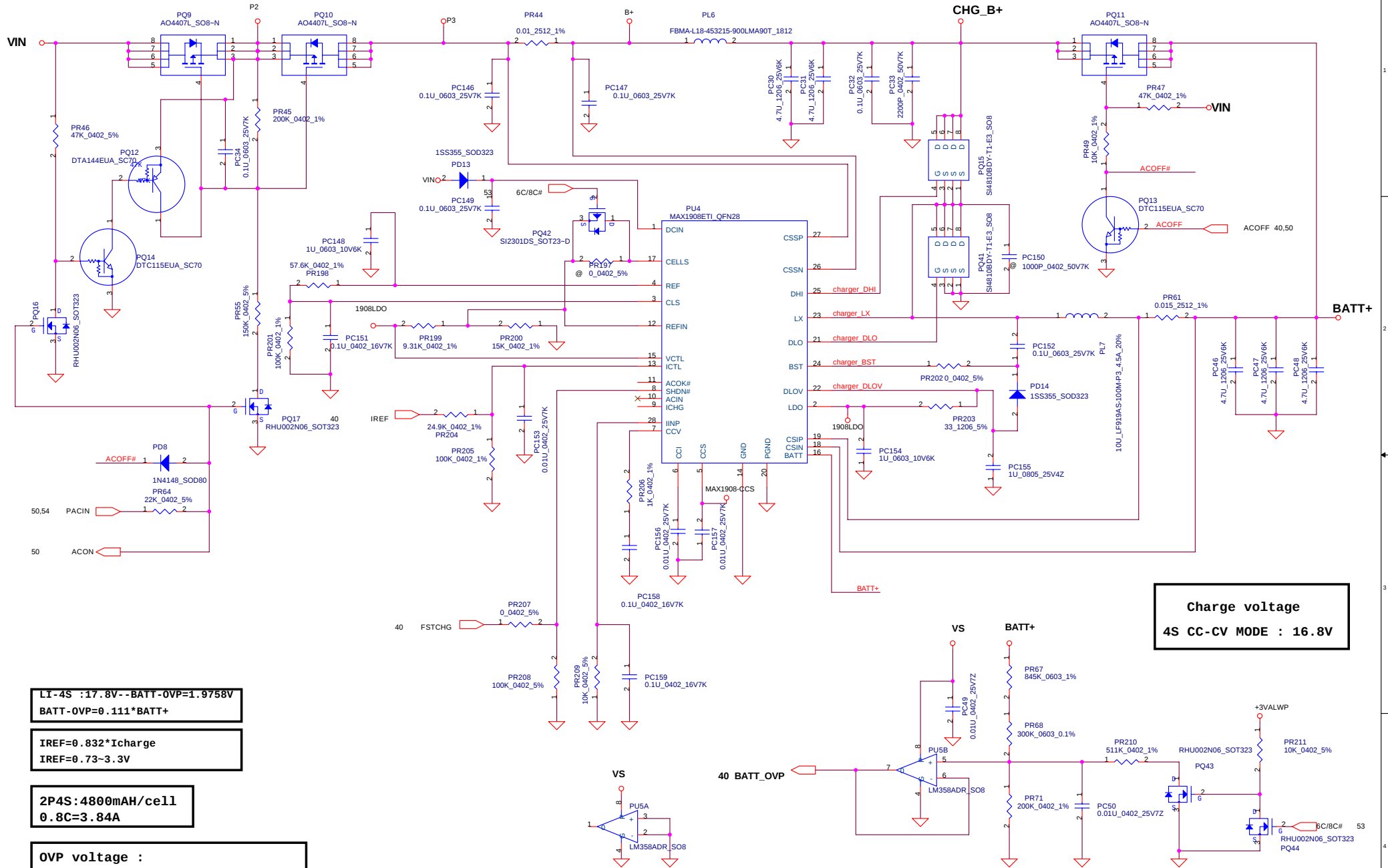
Date: Wednesday, April 19, 2006

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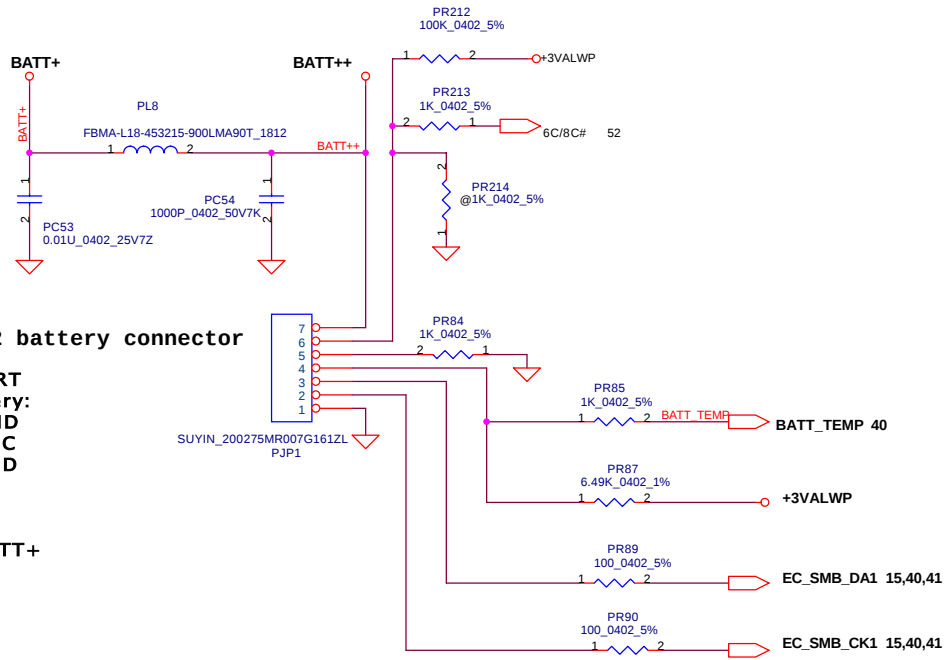
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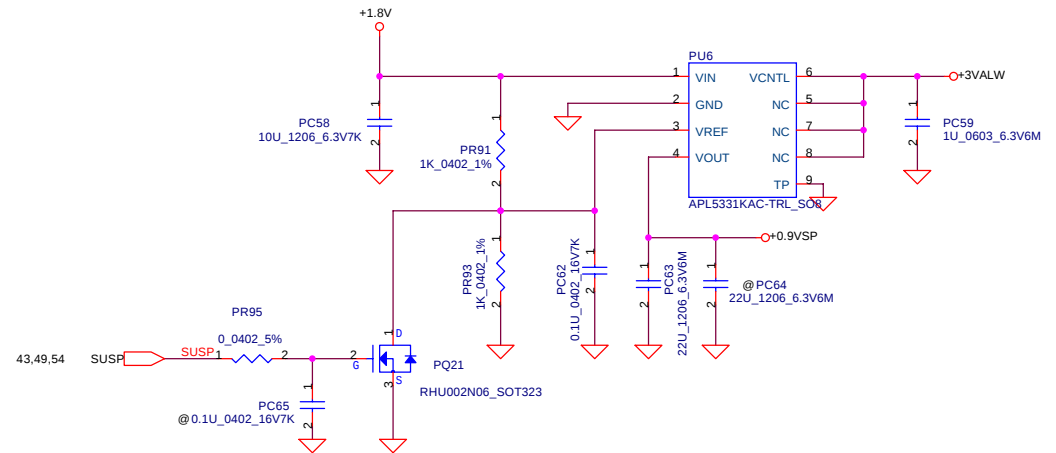
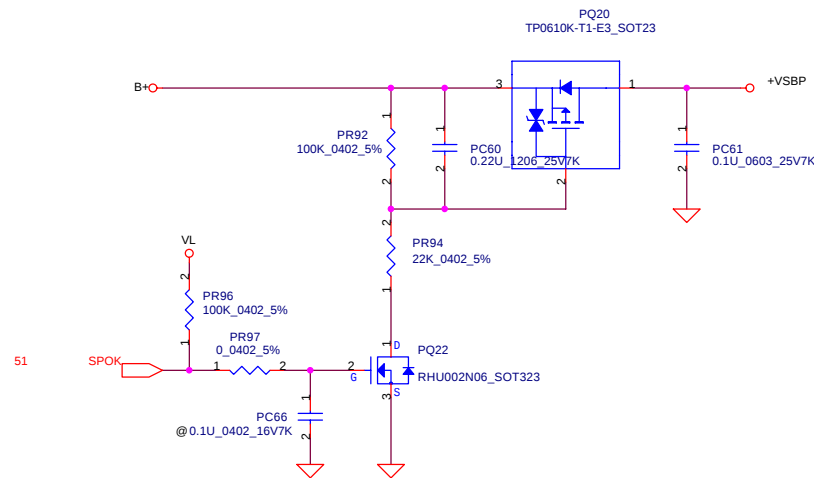
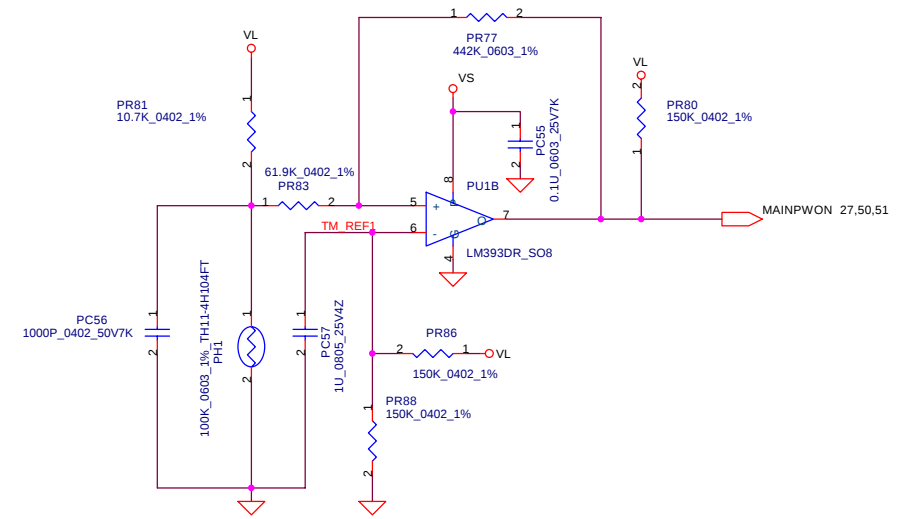
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PJP2 battery connector

SMART Battery:
 1.GND
 2.SMC
 3.SMD
 4.TS
 5.B/I
 6.ID
 7.BATT+

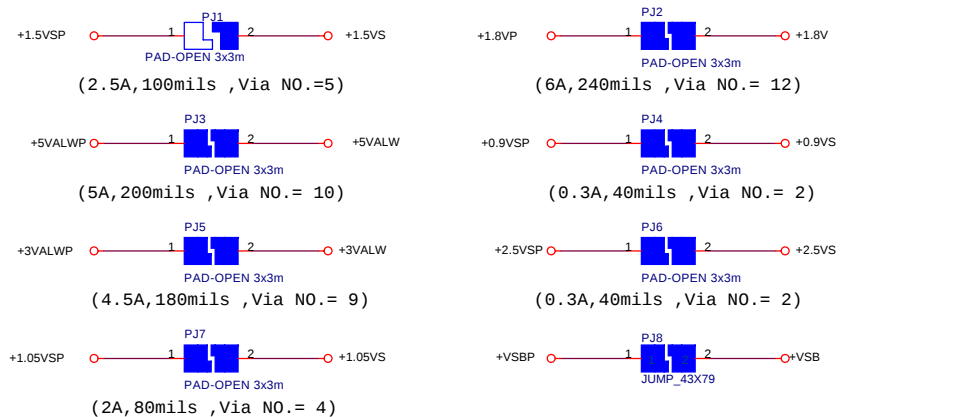


PH1 under CPU botten side :
 CPU thermal protection at 80 degree C
 Recovery at 44(45) degree C

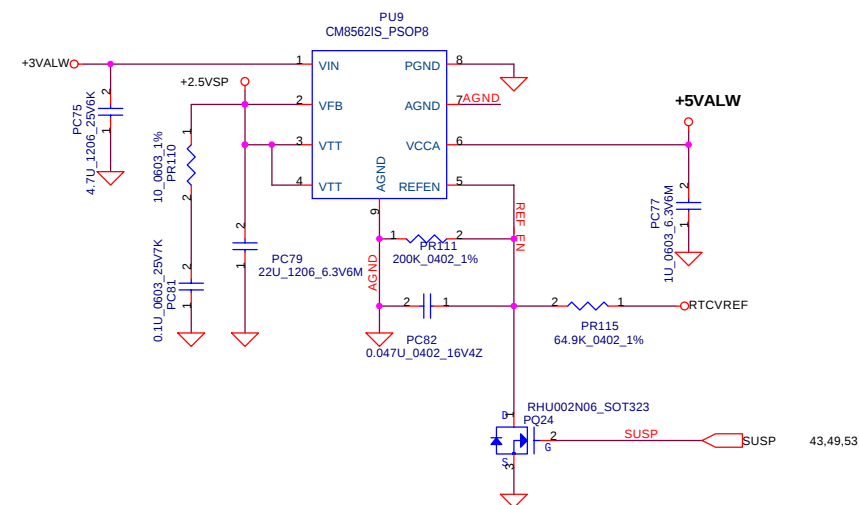
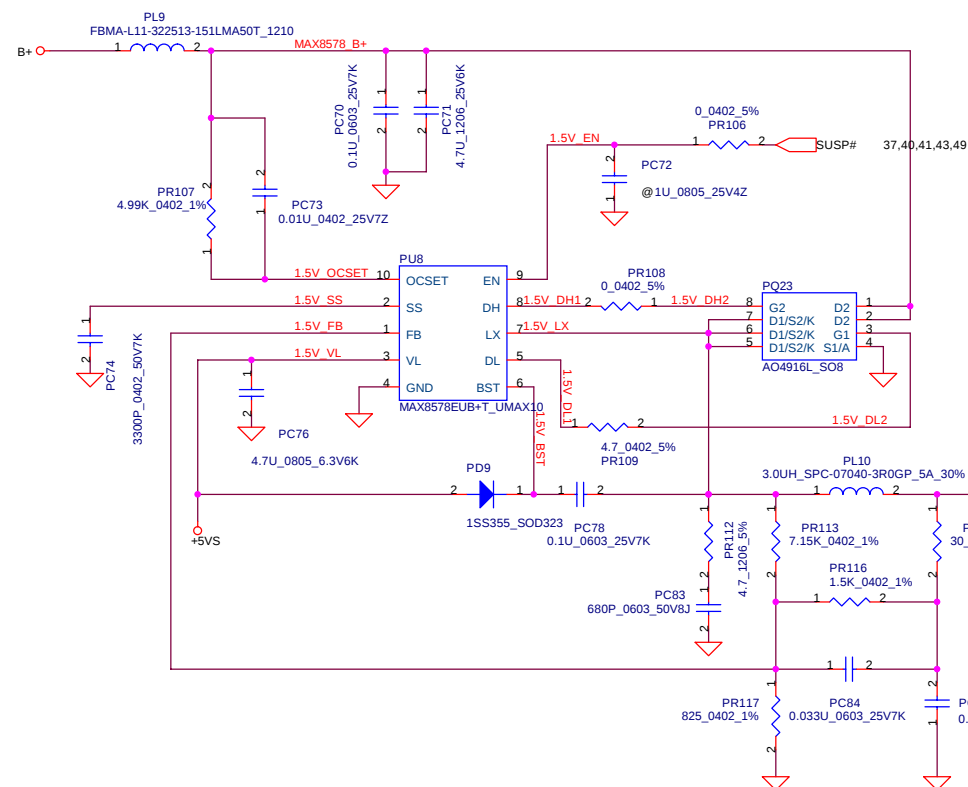
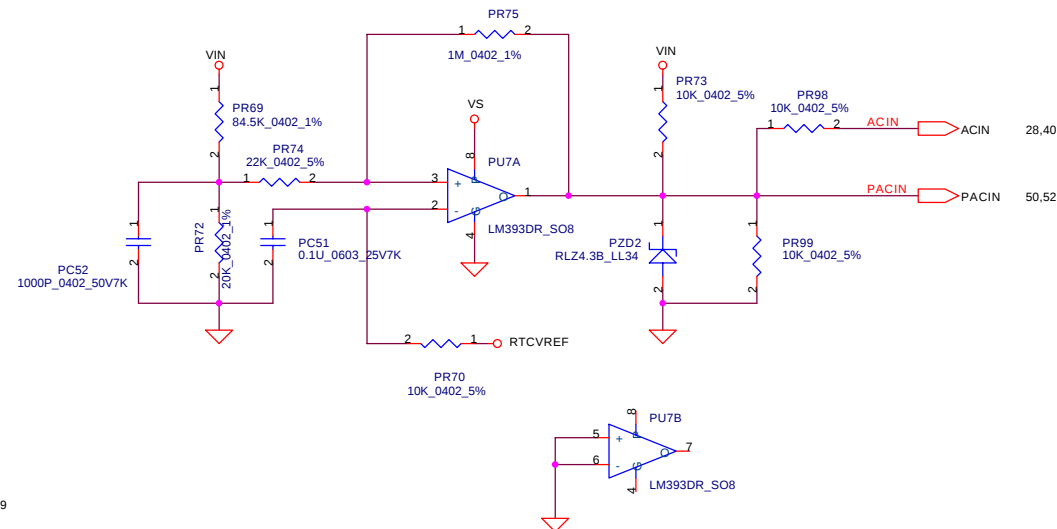


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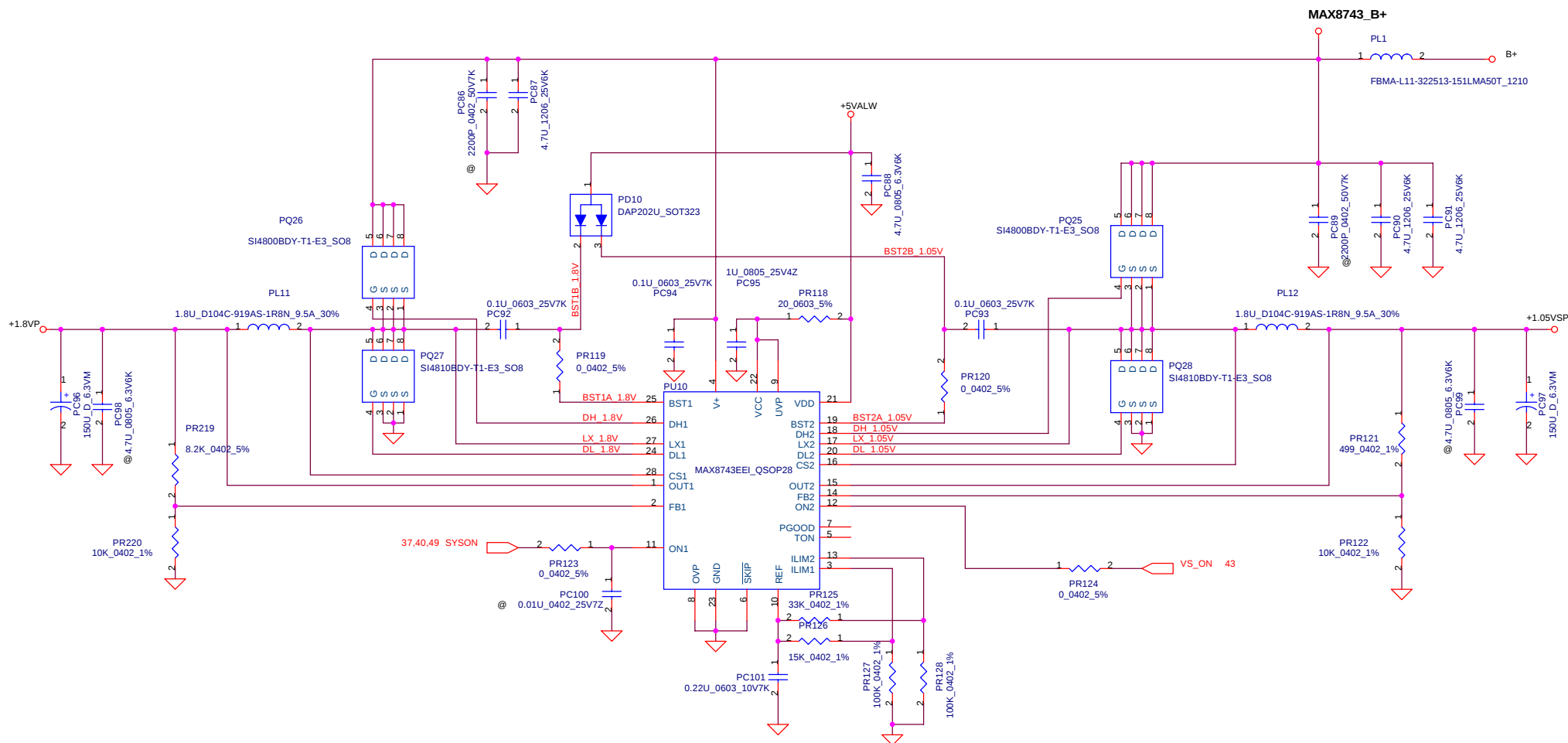
AC Adapter Detector



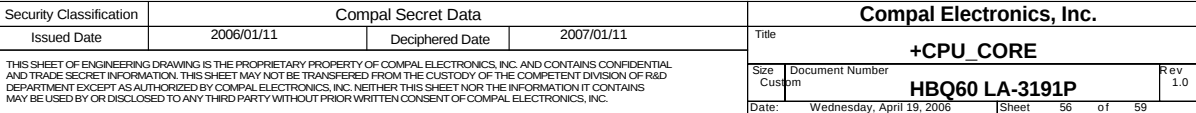
Vin Detector 17.90V/17.24V



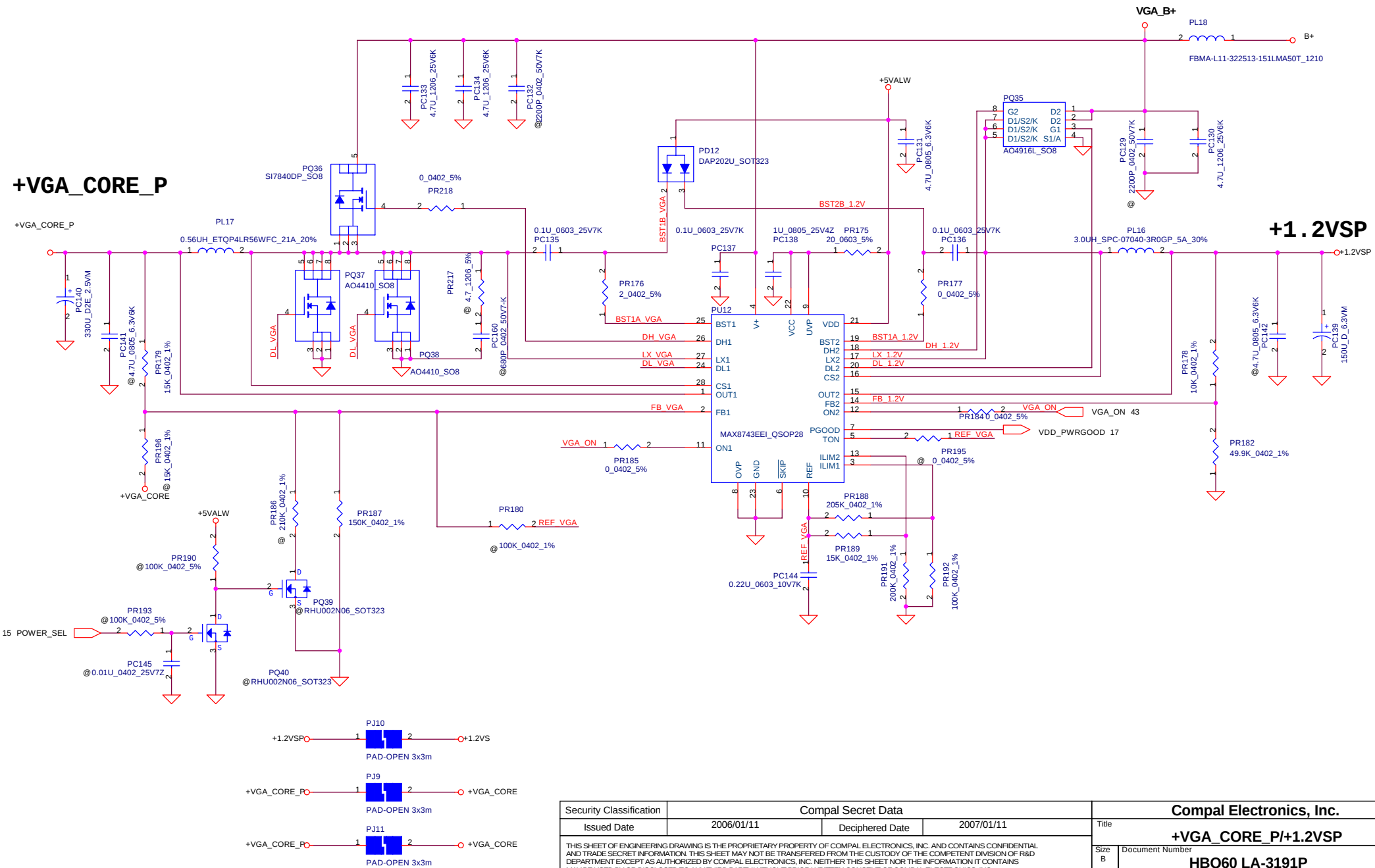
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POWER_SEL	H	L
+VGA_CORE FOR G73.	+0.95V(VGA@+G72@)	+1.025V
+VGA_CORE FOR G72.	+1.1V(VGA@)	



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