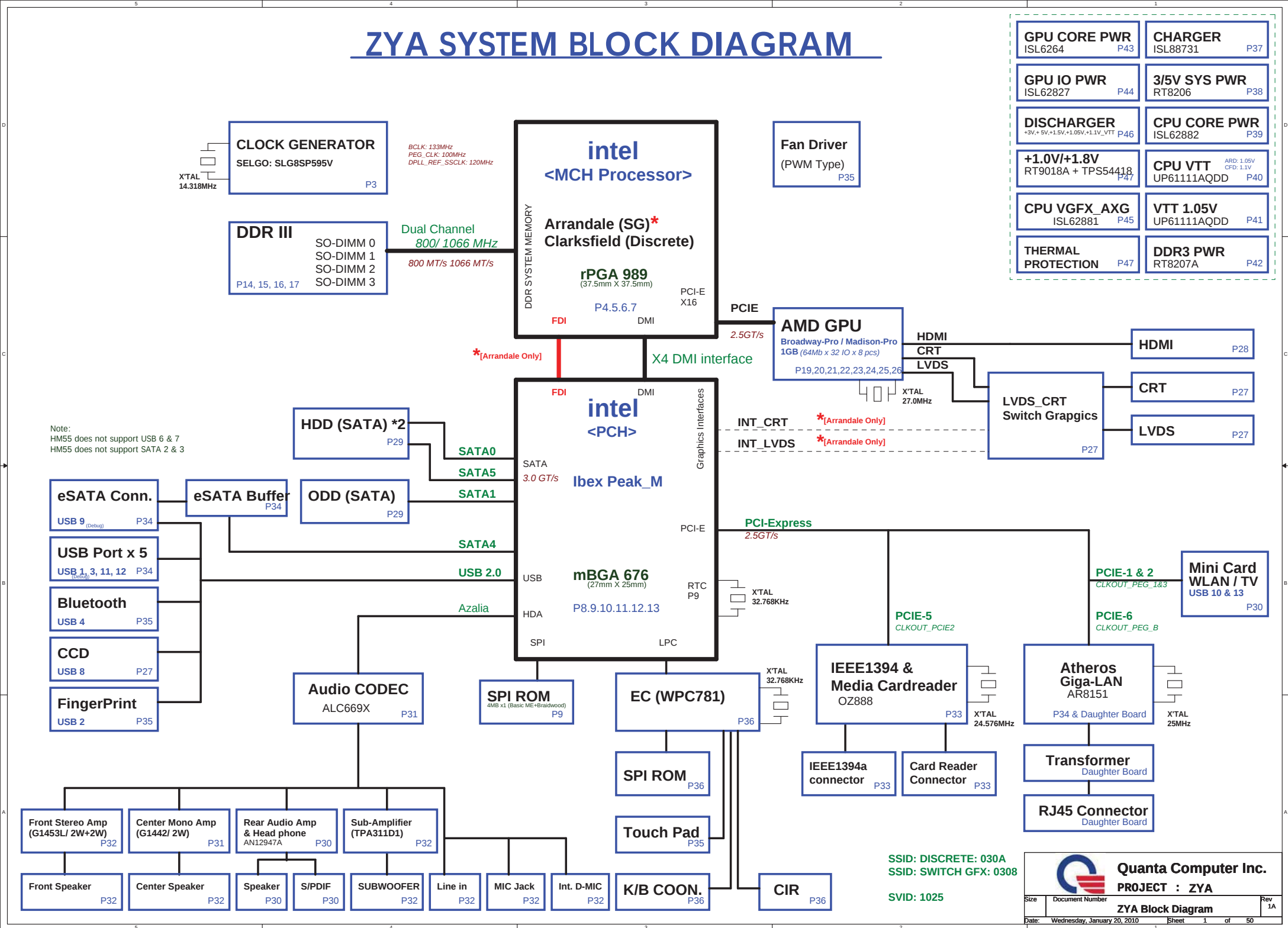
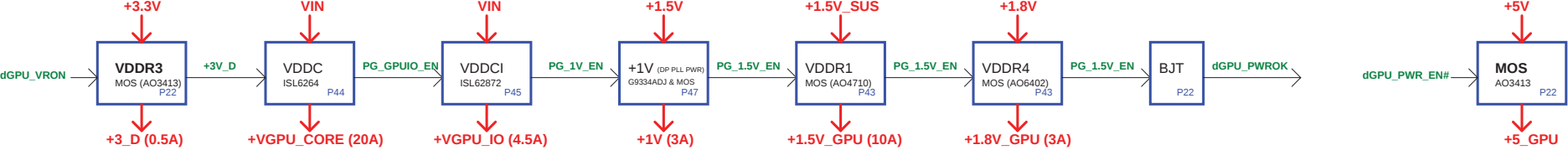


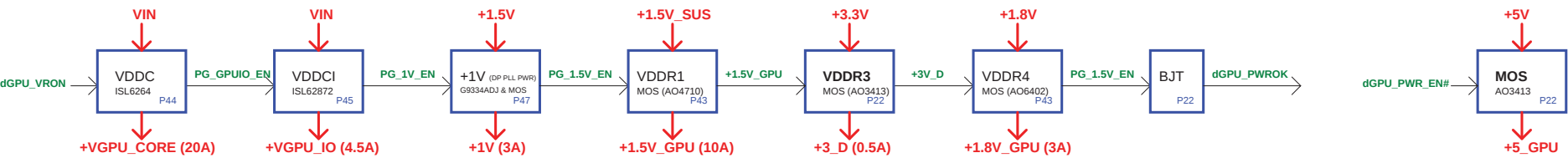
ZYA SYSTEM BLOCK DIAGRAM



GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



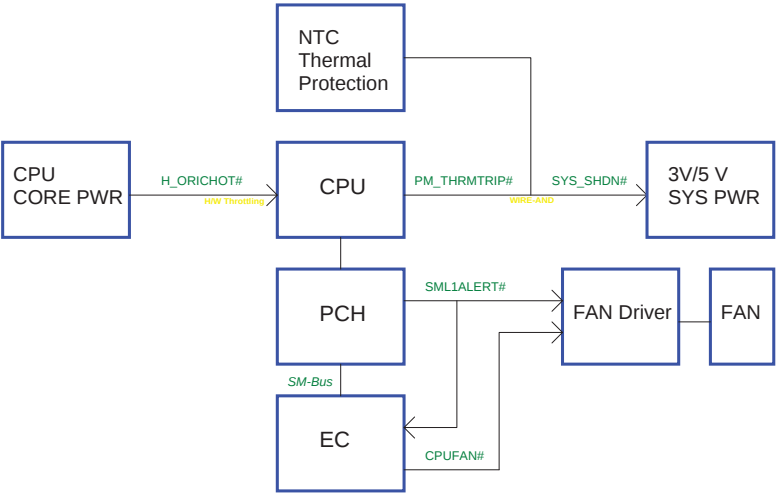
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



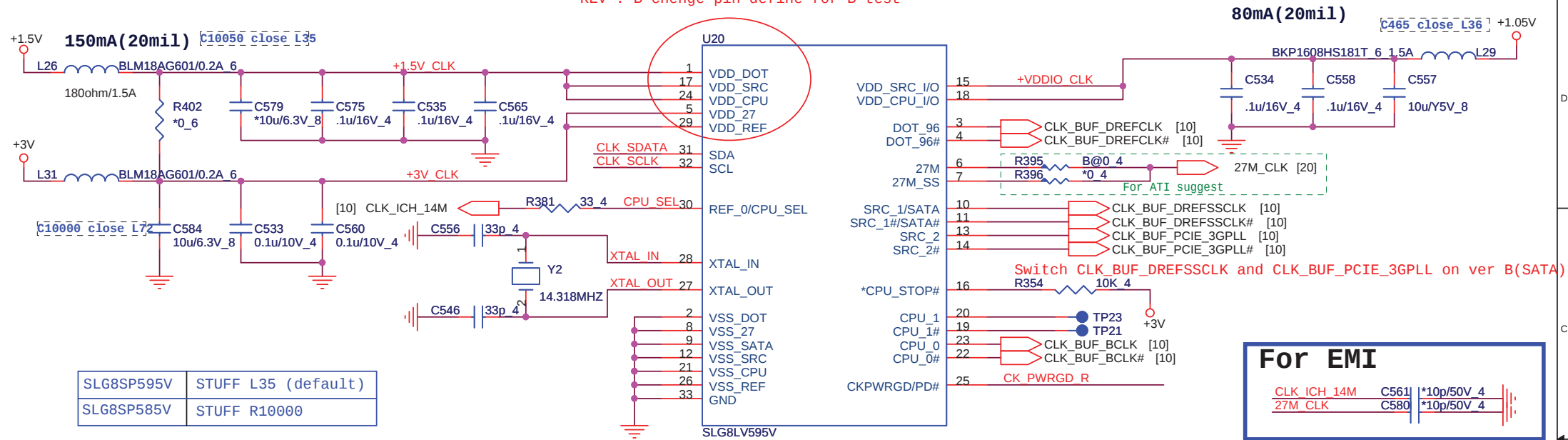
Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

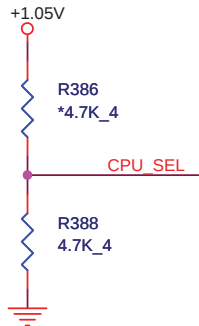
Thermal Follow Chart



REV : B change pin define for B-test

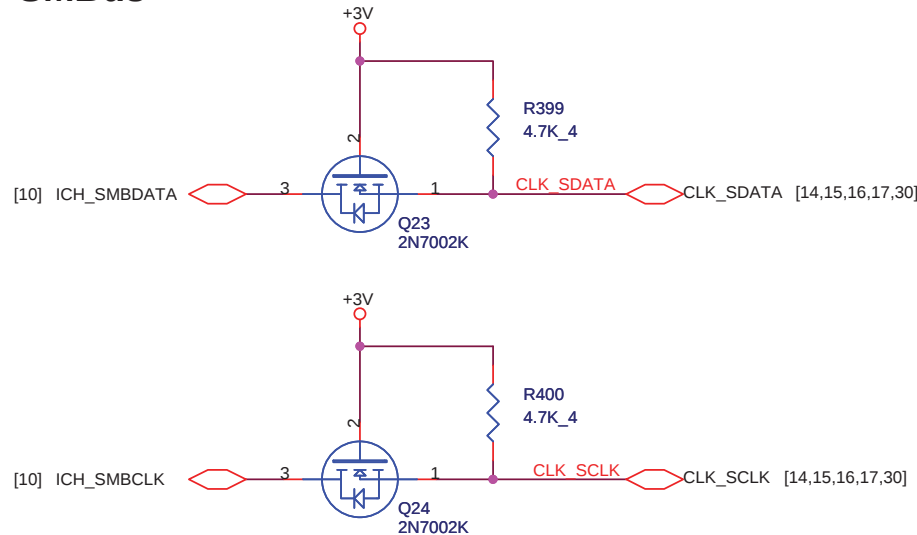


CPU_CLK select

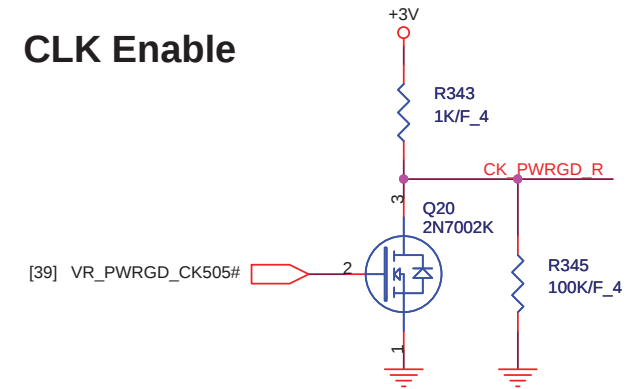


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus

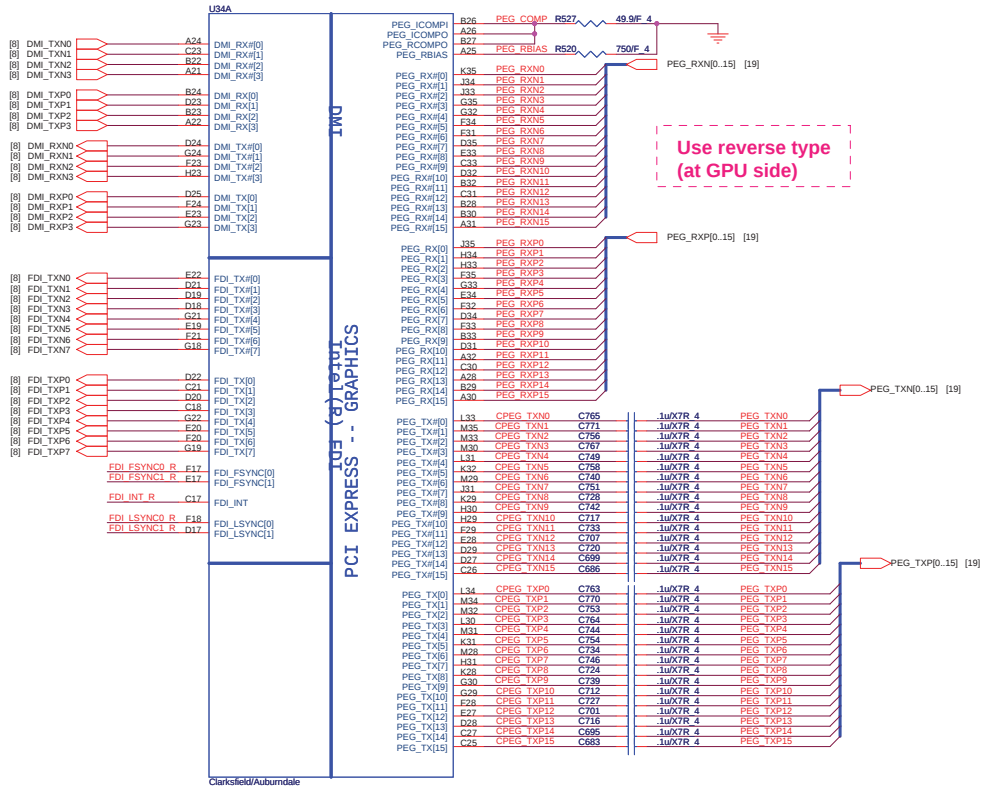


CLK Enable

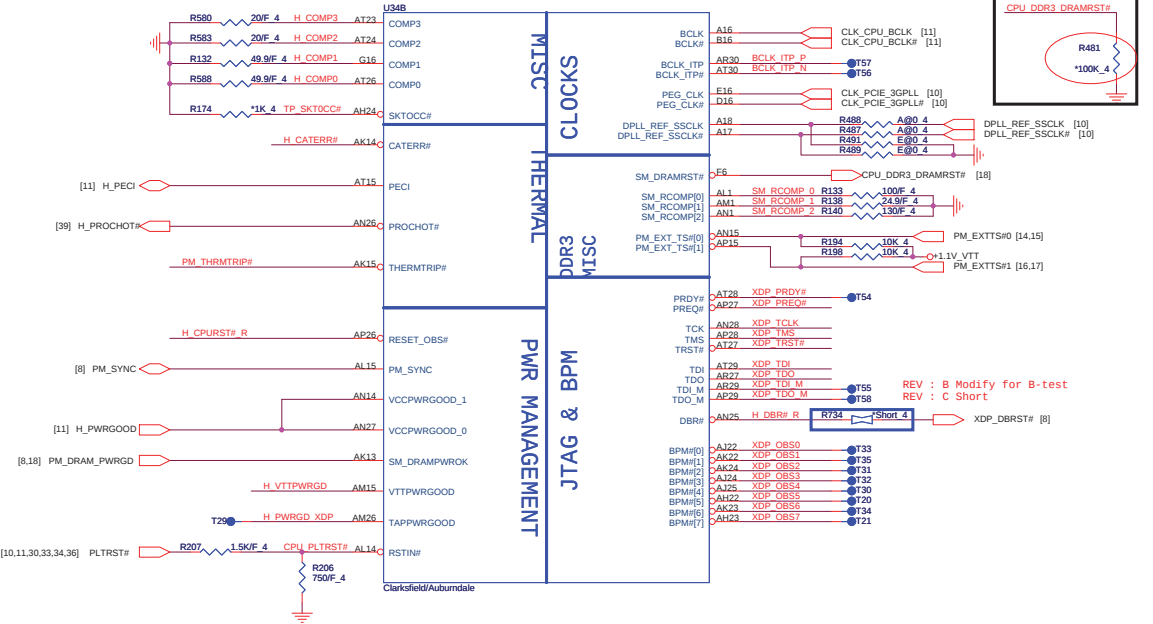


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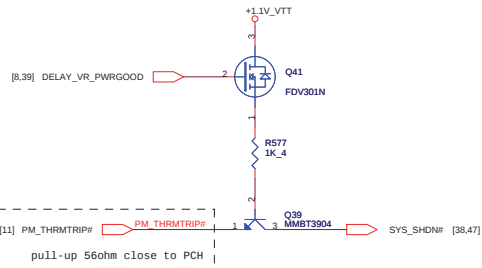
Size	Document Number	Rev
	Clock Generator	1A
Date:	Wednesday, January 20, 2010	Sheet 3 of 50



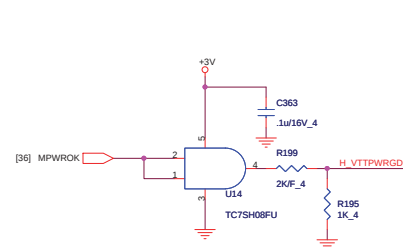
Processor Compensation Signals



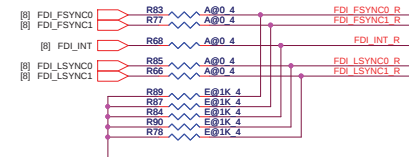
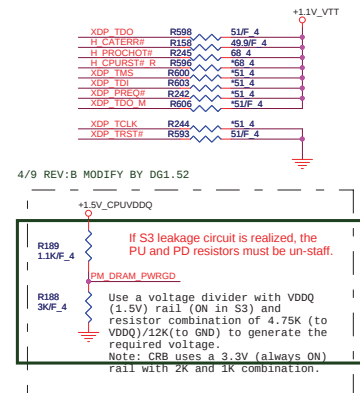
Thermaltrip protect



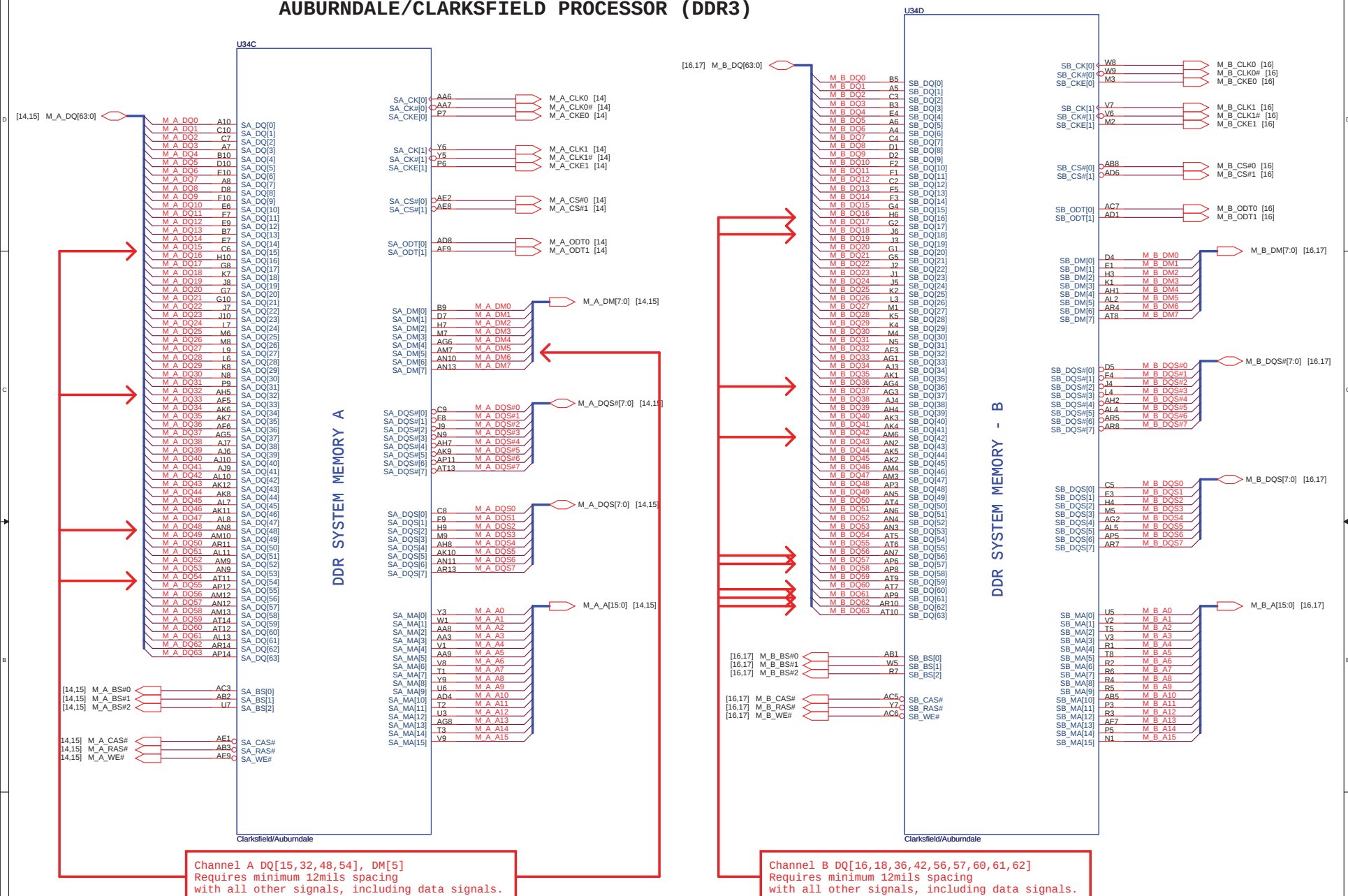
VTT PWR_Good



Processor pull-up



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



U34F





```
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
```

AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



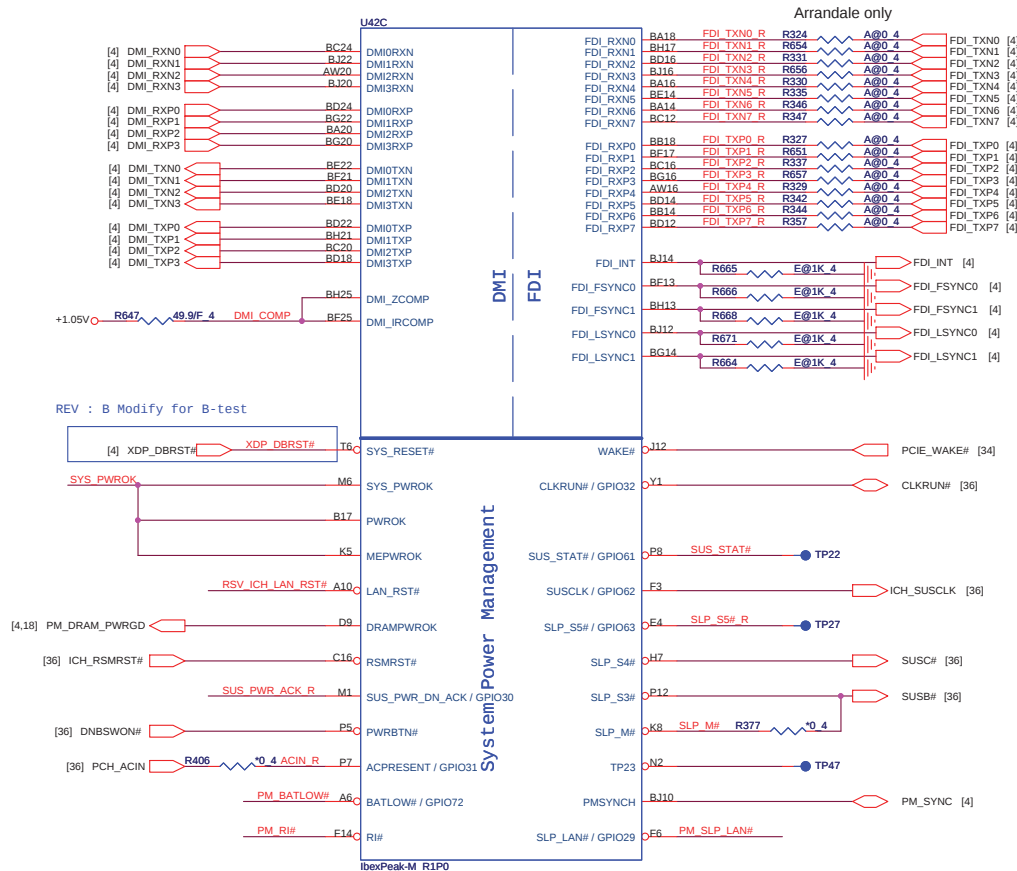
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



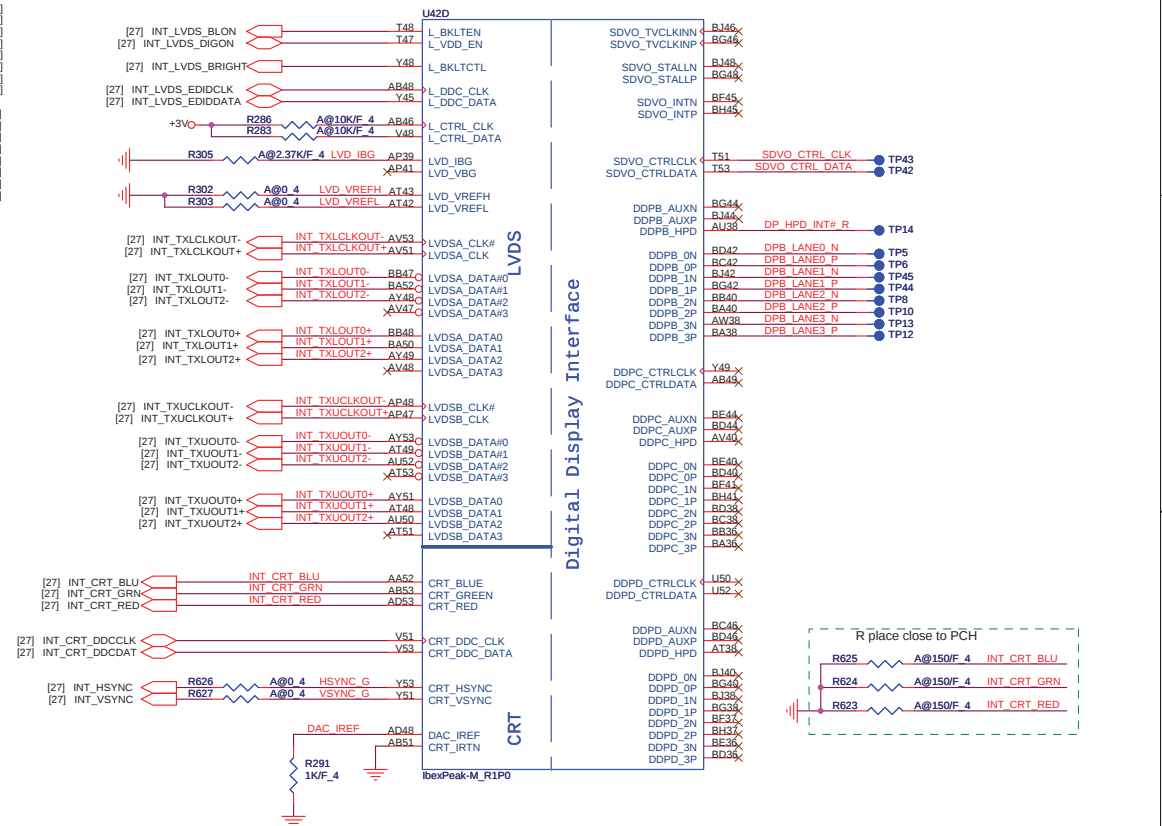
Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number AUBURND 4/4	Rev 1A
Date:	Wednesday, January 20, 2010	Sheet 7 of 50

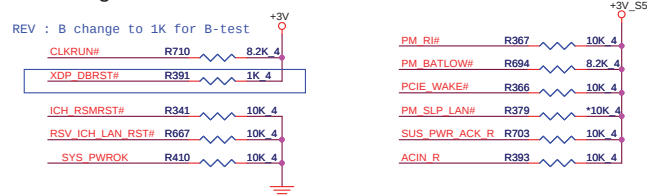
IBEX PEAK-M (DMI, FDI, GPIO)



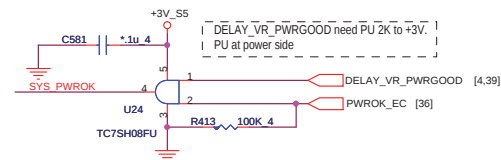
IBEX PEAK-M (LVDS, DDI)



PCH Pull-high/low



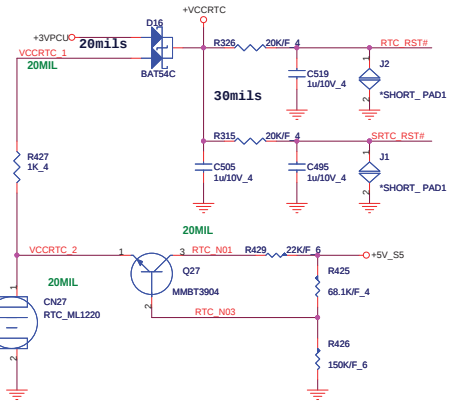
System PWR_OK



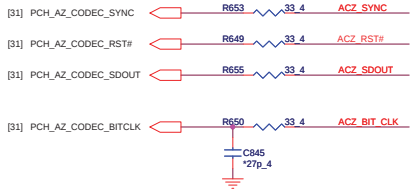
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Size	Document Number	Rev
	IBEX PEAK-M 1/6	1A
Date:	Wednesday, January 20, 2010	Sheet 8 of 50

RTC Circuitry

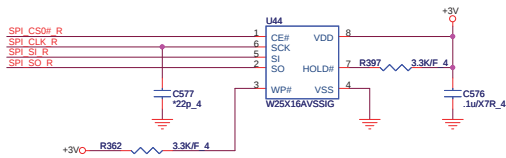


HDA Bus



Place all series terms close to PCH except for SDIN input lines, which should be close to source. Placement of R773, R775, R776 & R777 should equal distance from T for all series termination resistors.

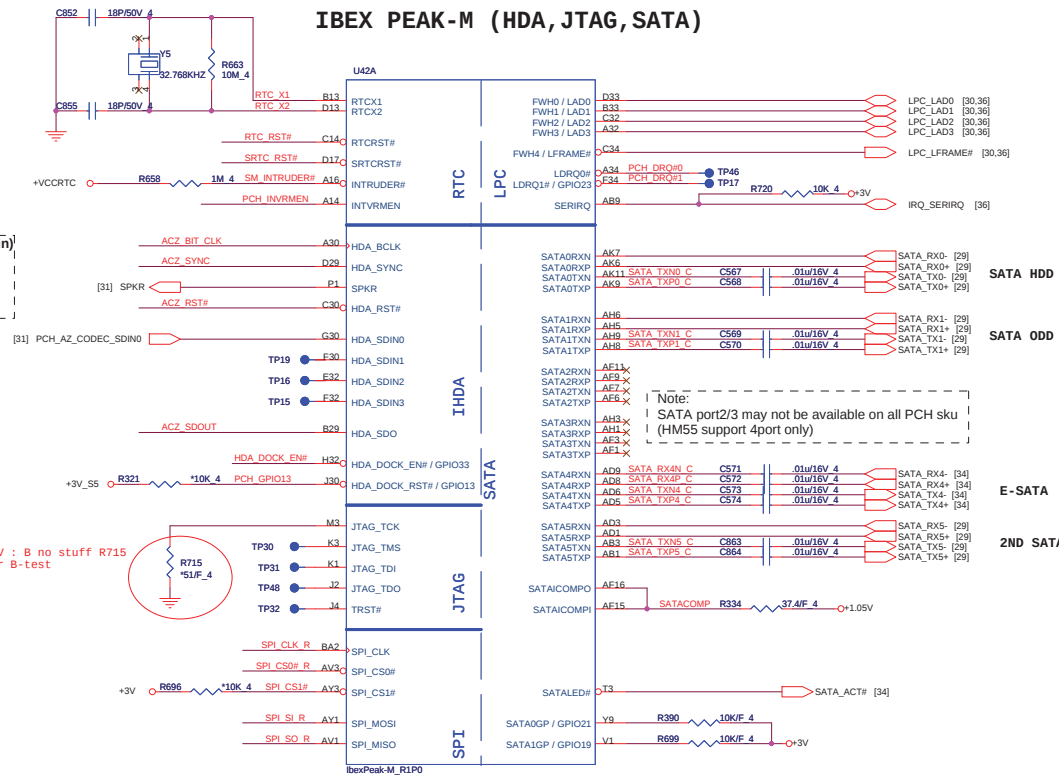
PCH SPI



At 11/24 add Winbond W25X16AVSSIG EON EN25F16-100HIP AMIC A25L016

AKE382P0N01 AKE382A0Q00 AKE382N0800

IBEX PEAK-M (HDA, JTAG, SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZY9B note												
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode													
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down													
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)													
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up													
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>1</td><td>0</td><td>PCI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	1	SPI	1	0	PCI	0	0	LPC	Default weak pull-up on GNT0/L# [Need external pull-down for LPC BIOS]
GNT1#	GNT0#	Boot Location														
1	1	SPI														
1	0	PCI														
0	0	LPC														
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK														
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN												
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)													
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm													
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)													
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable													
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)													
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)													
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)													
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use default (0 = 1.8V supply)												
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality													

A16 swap override Strap/Top-Block Swap Override jumper

Low = A16 swap override/Top-Block Swap Override enabled
High = Default

Boot BIOS Strap	GNT1#	GNT1#	Boot BIOS Location
0	0	0	LPC
0	1	0	Reserved (NAND)
1	0	1	PCI
1	1	1	SPI

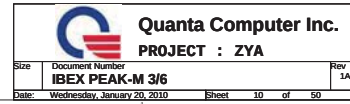
Danbury Technology Enabled

High = Enable
Low = Disable

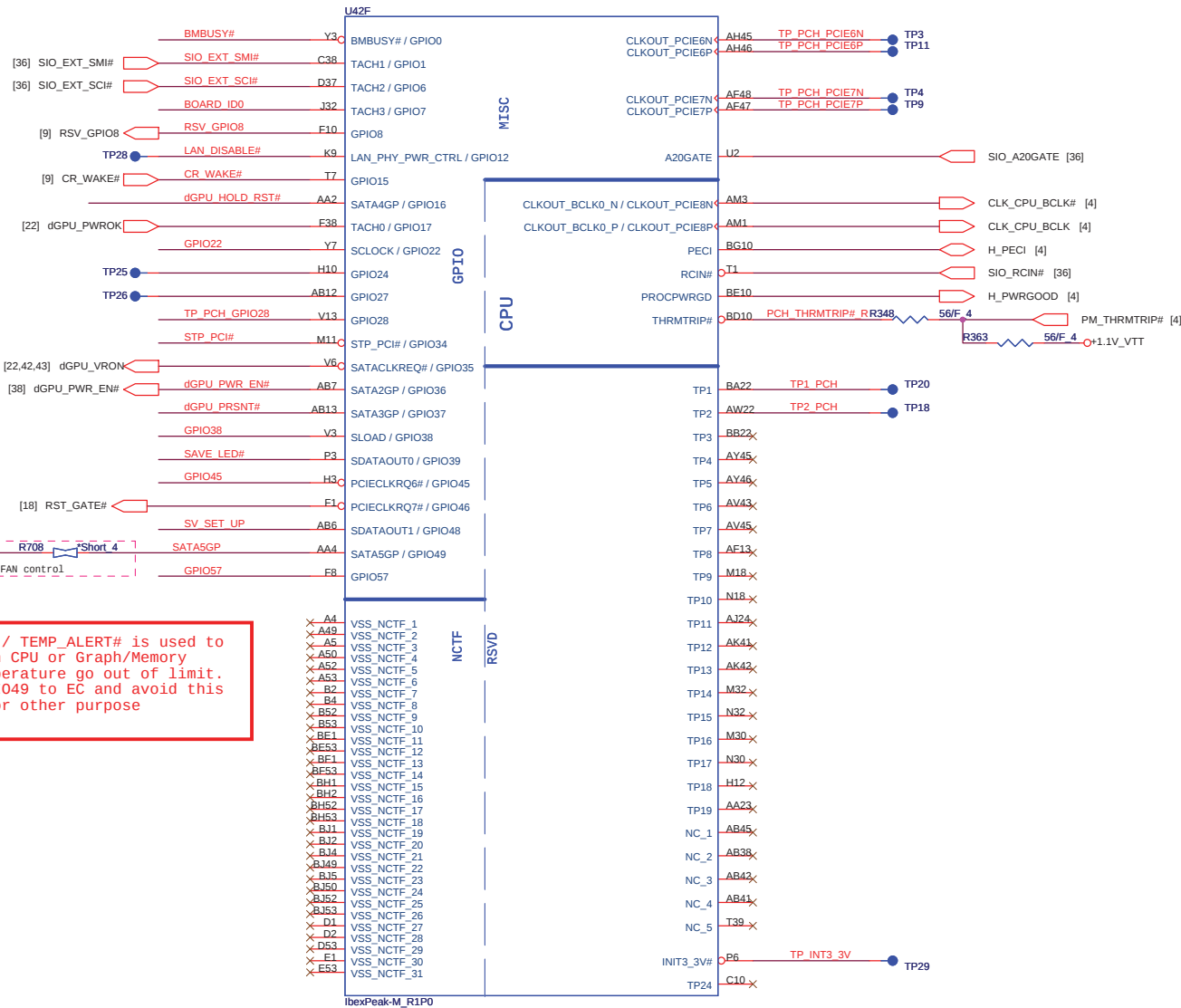
DMI Termination Voltage

NV_CLE Set to Vcc when LOW
Set to Vcc/2 when HIGH

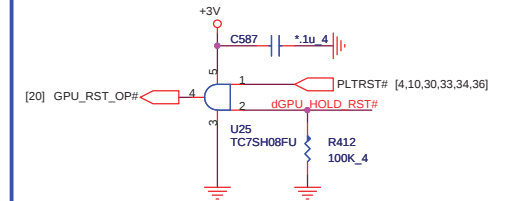
IBEX PEAK-M (PCI-E, SMBUS, CLK)



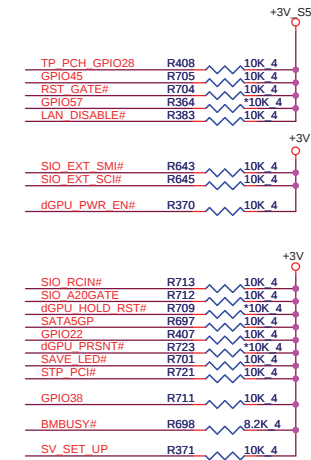
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



GPU RST#

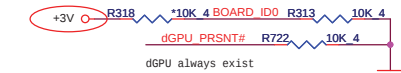


GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

REV : B , Change +3V_S5 to +3V

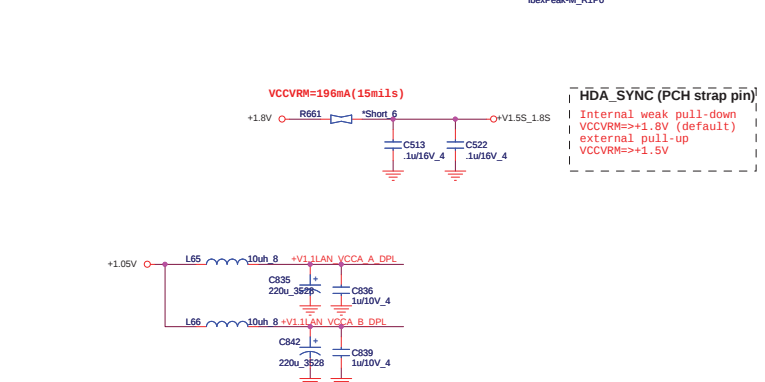
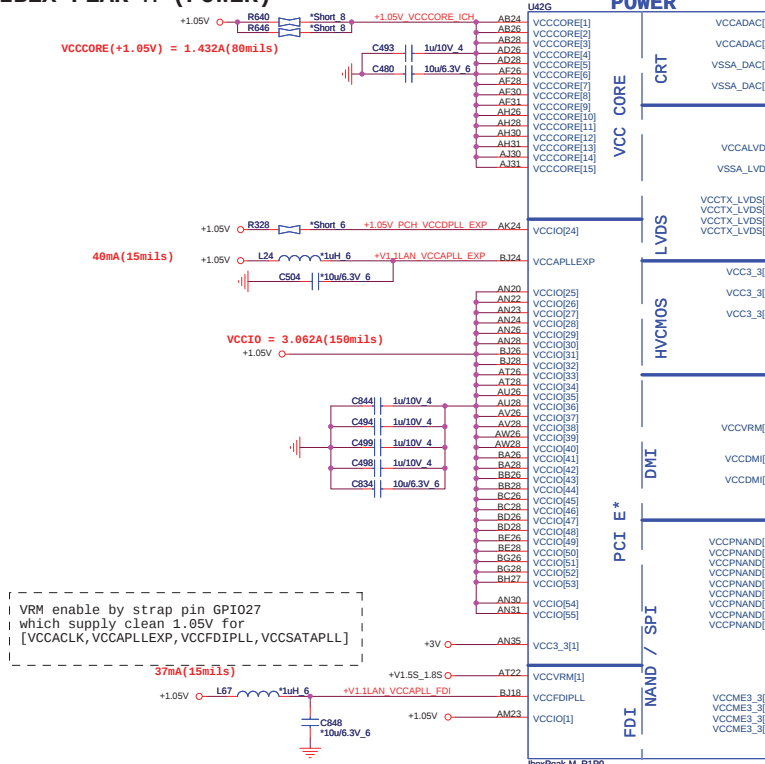


Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

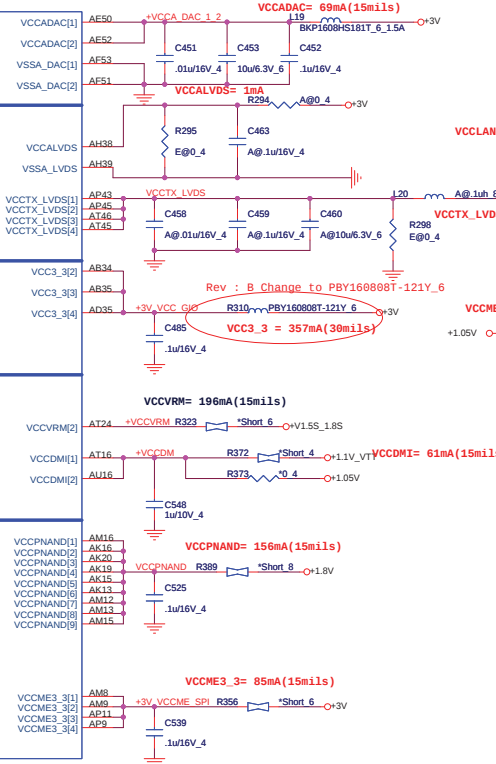


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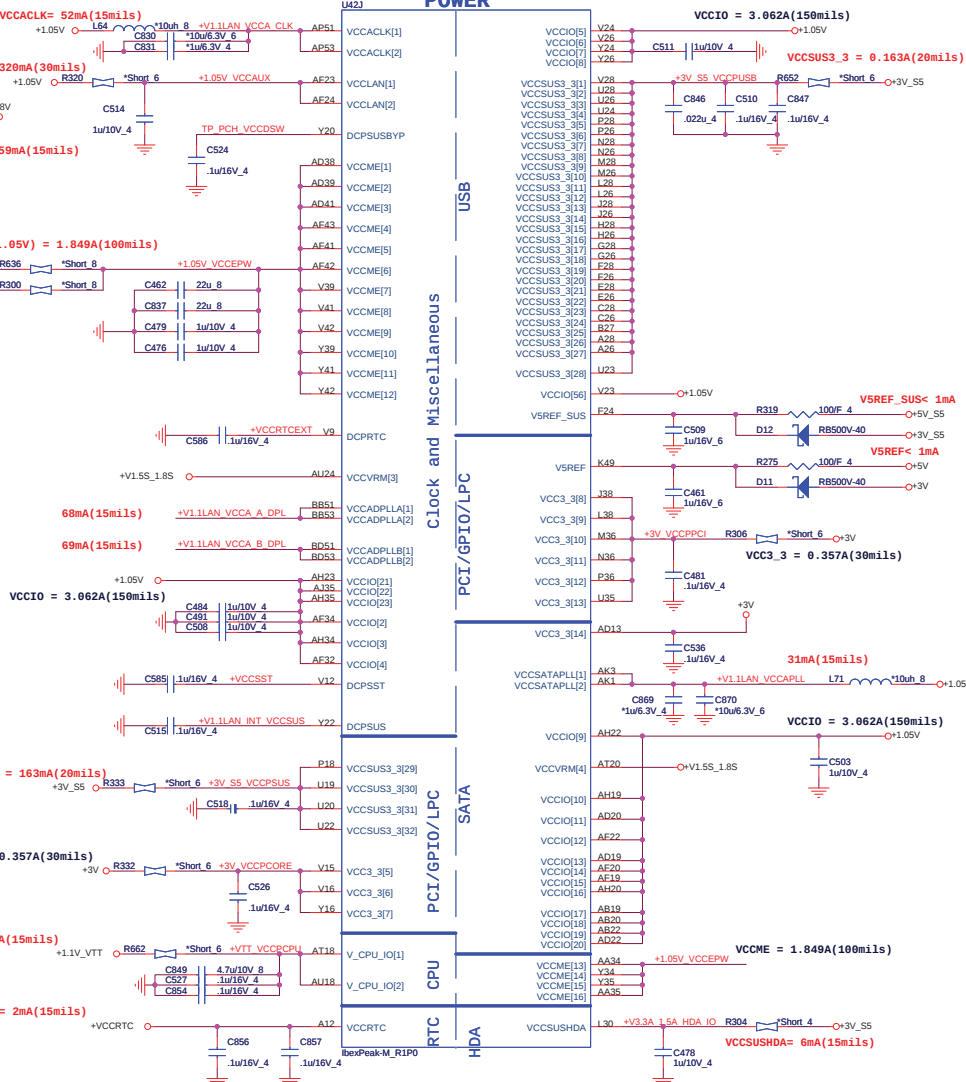
IBEX PEAK-M (POWER)



POWER



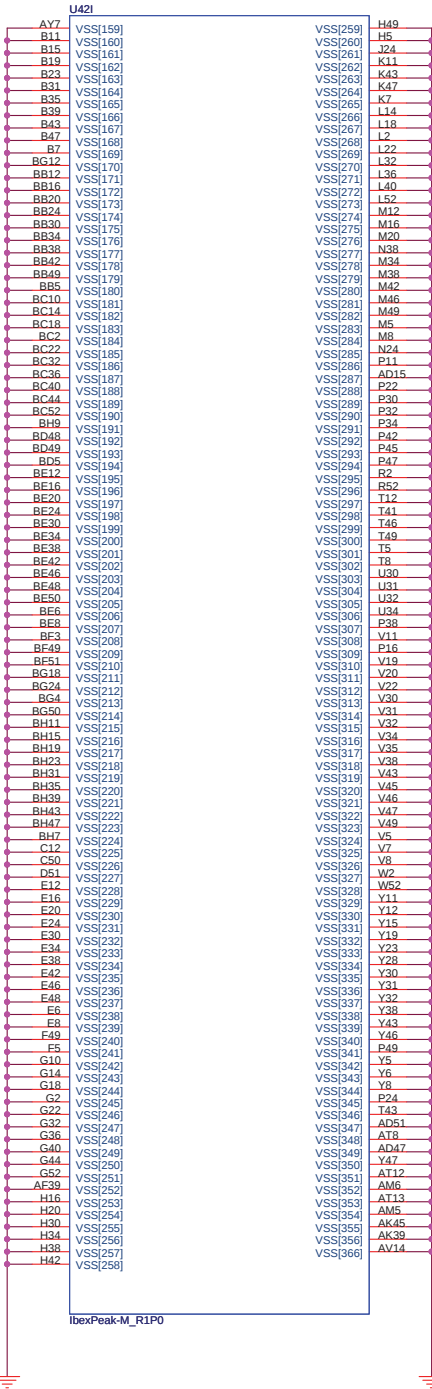
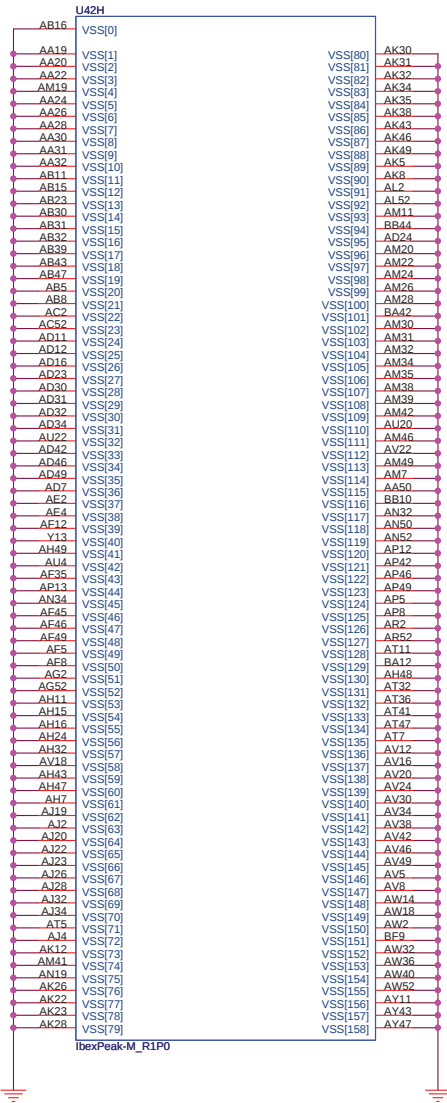
POWER



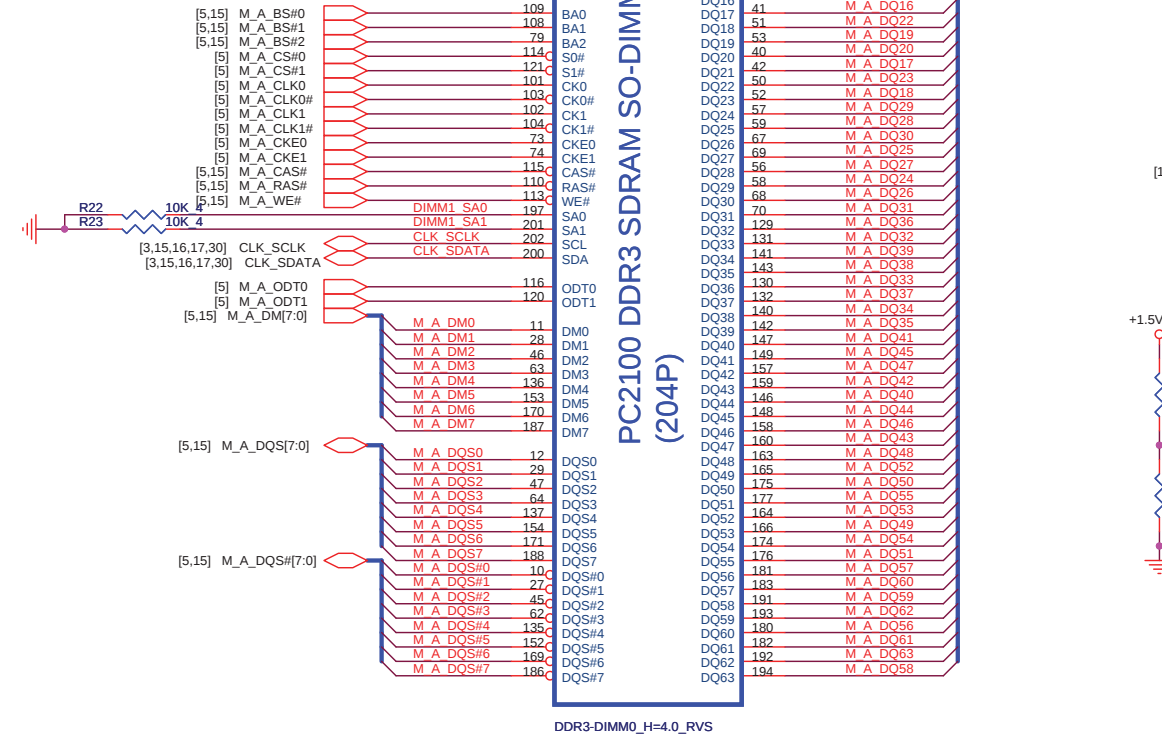
Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	IBEX PEAK-M 5/6	1A
Date:	Wednesday, January 20, 2010	Sheet 12 of 50

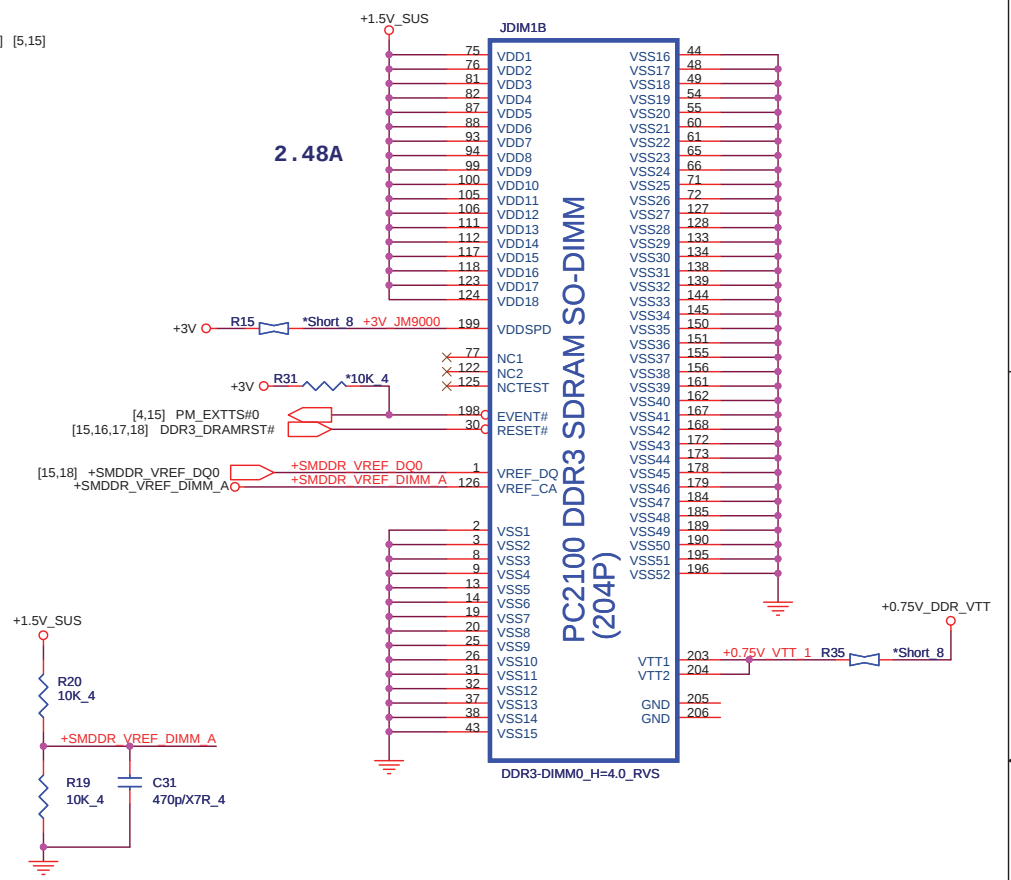
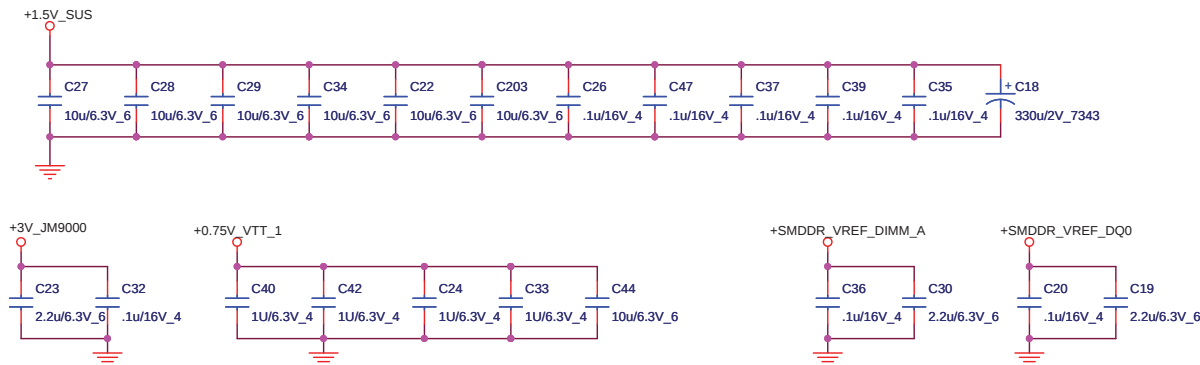
IBEX PEAK-M (GND)



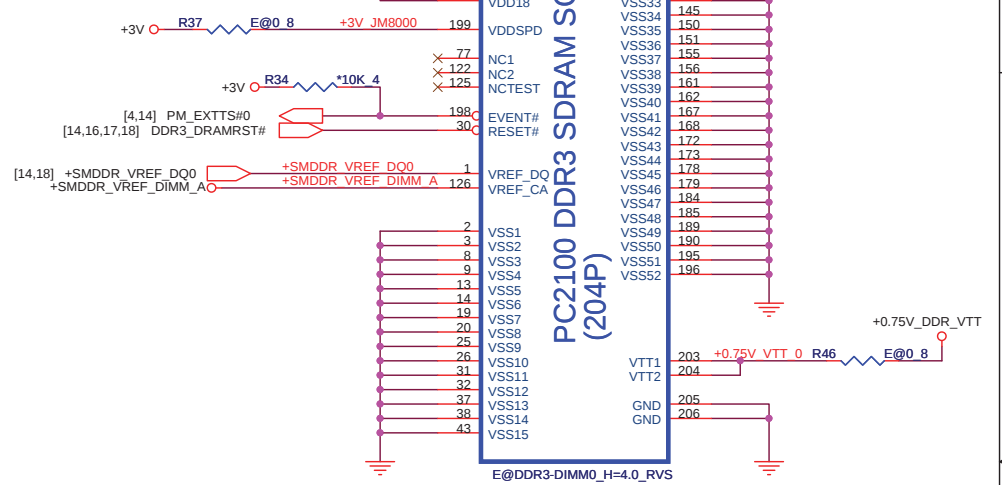
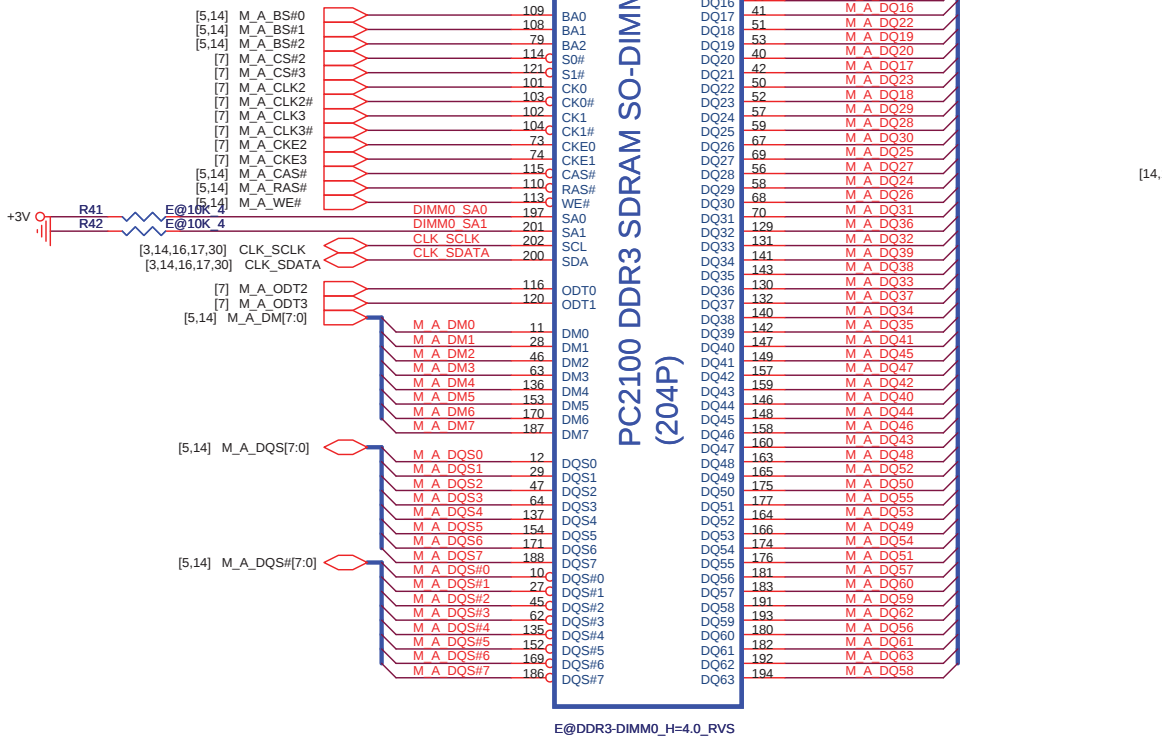
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



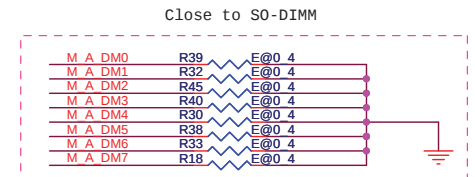
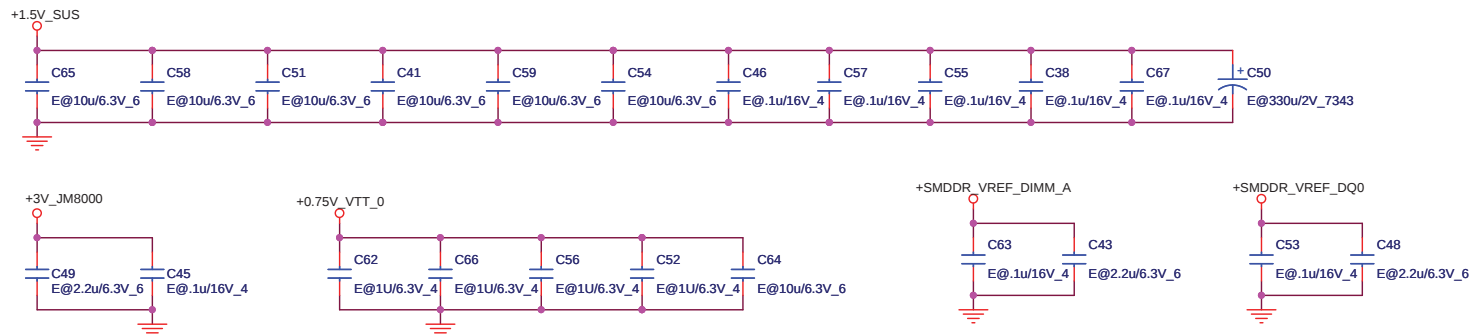
Place these Caps near So-Dimm0.



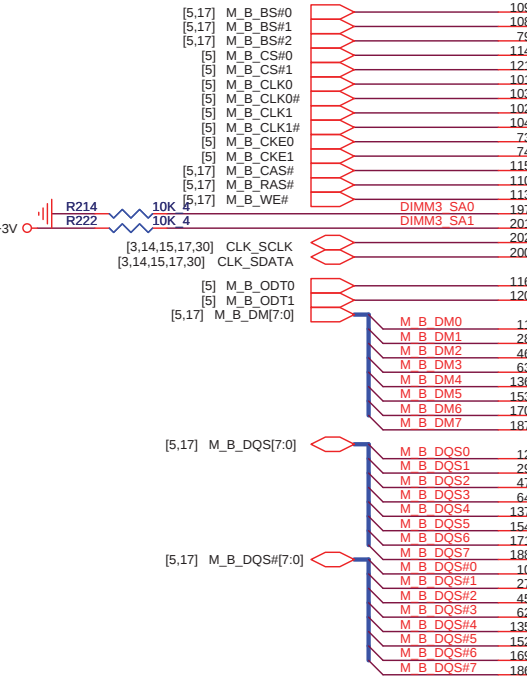
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



Place these Caps near So-Dimm0.



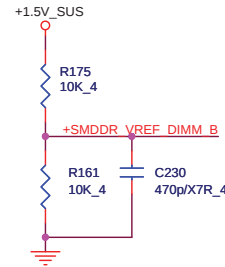
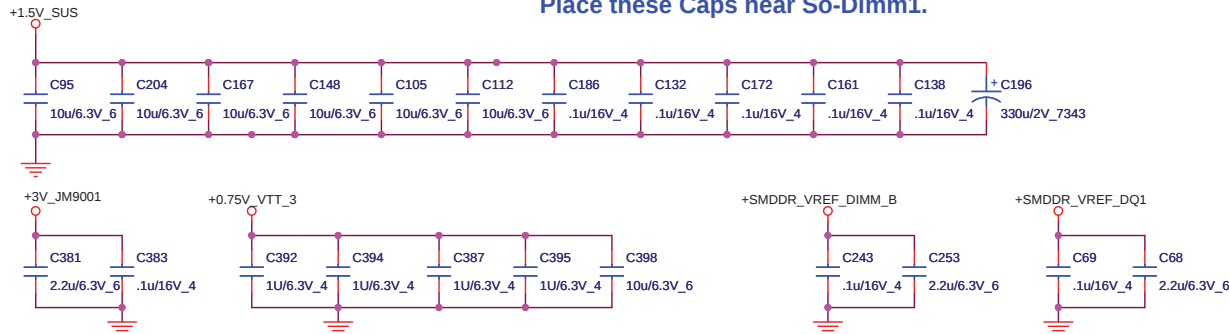
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



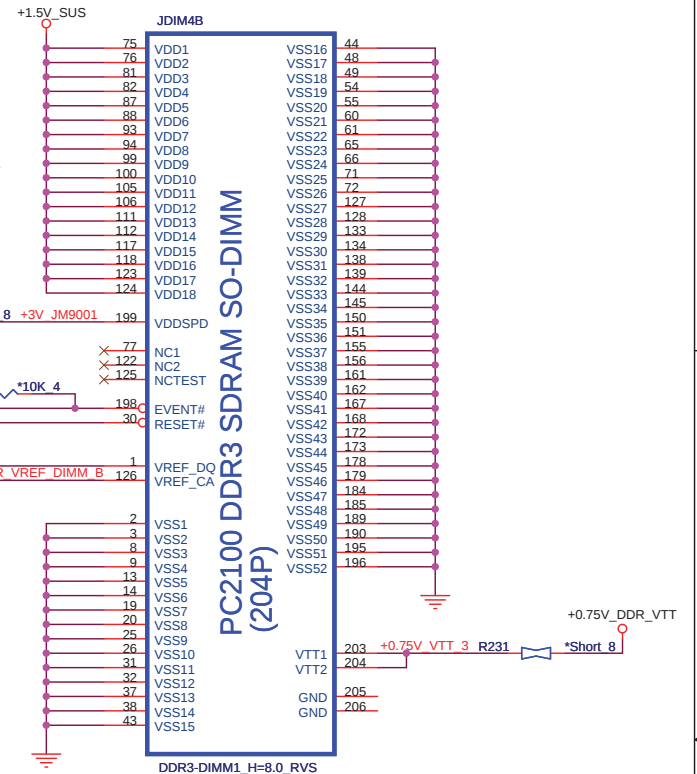
PC2100 DDR3 SDRAM SO-DIMM (204P)

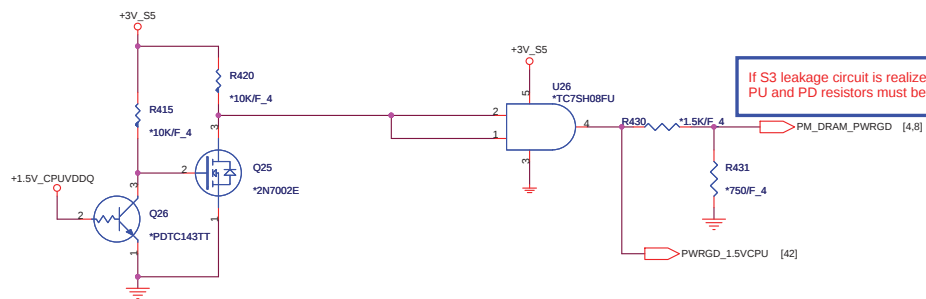
DDR3-DIMM1_H=8.0_RVS

Place these Caps near So-Dimm1.



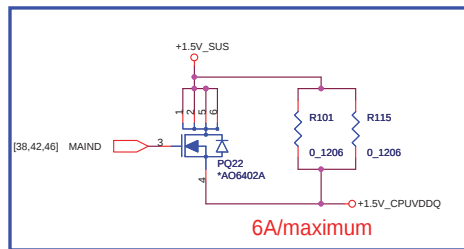
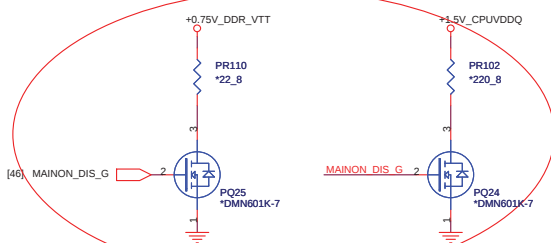
2.48A



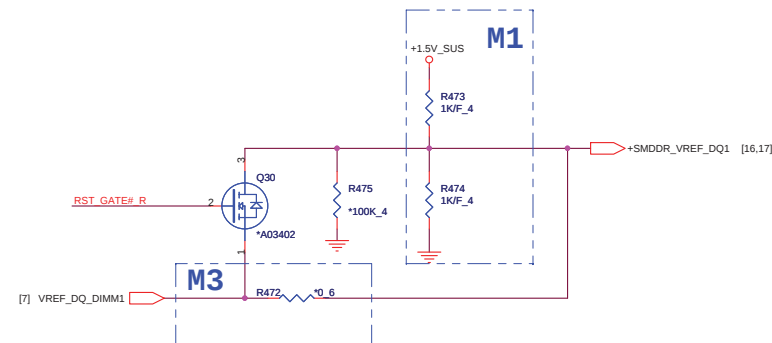
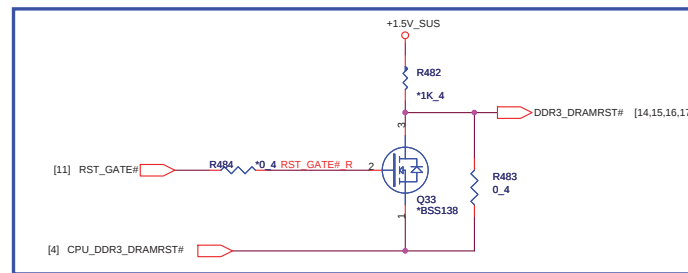


If S3 leakage circuit is realized, the PU and PD resistors must be un-staff.

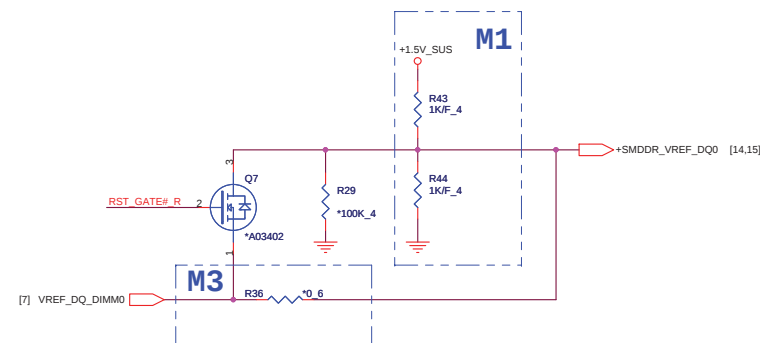
REV : B , No stuff for B-test

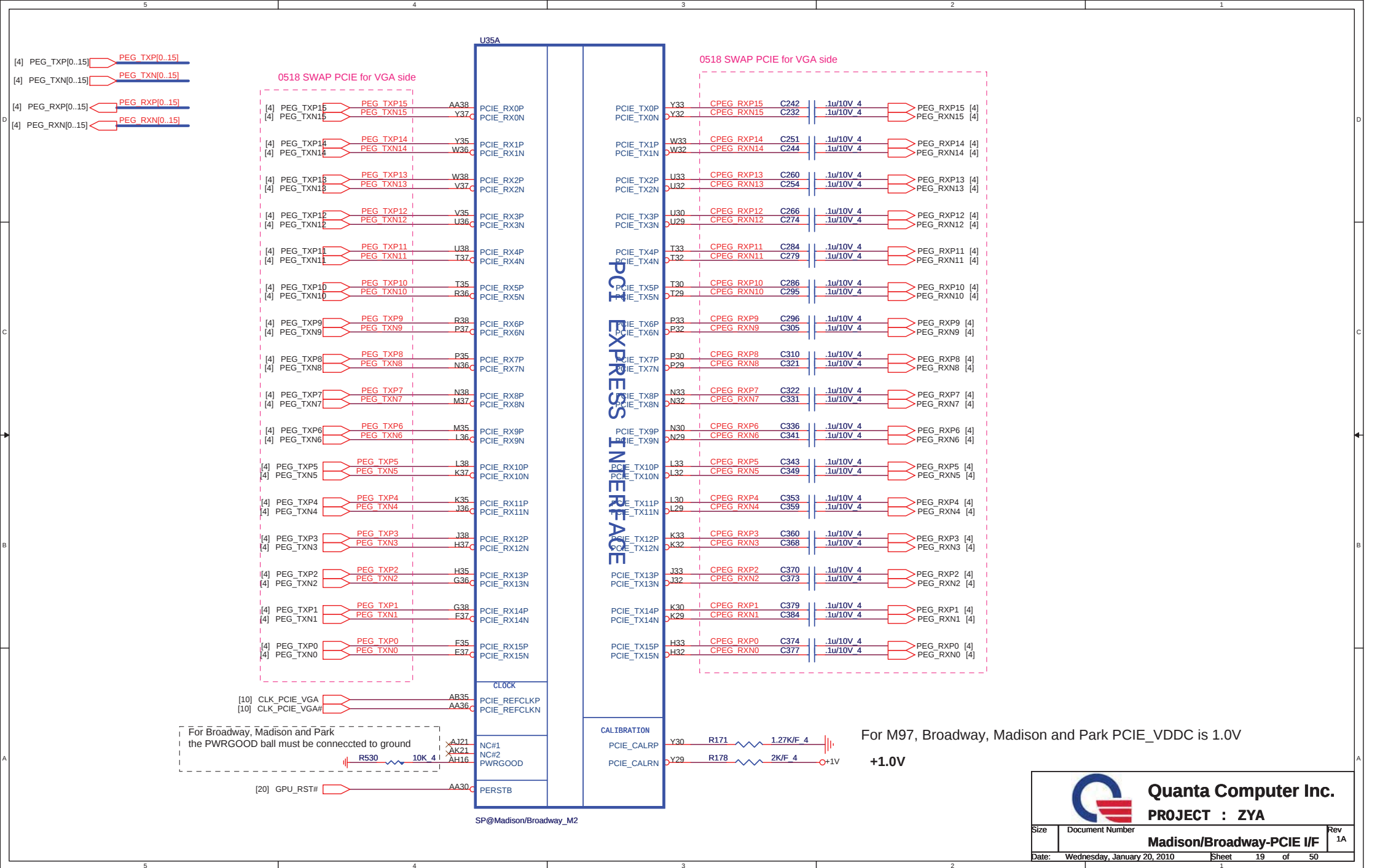


6A/maximum



REV : B , ZYA no support M3





```
1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK
```

1.8V GPIO

3.3V GPIO

For EMI

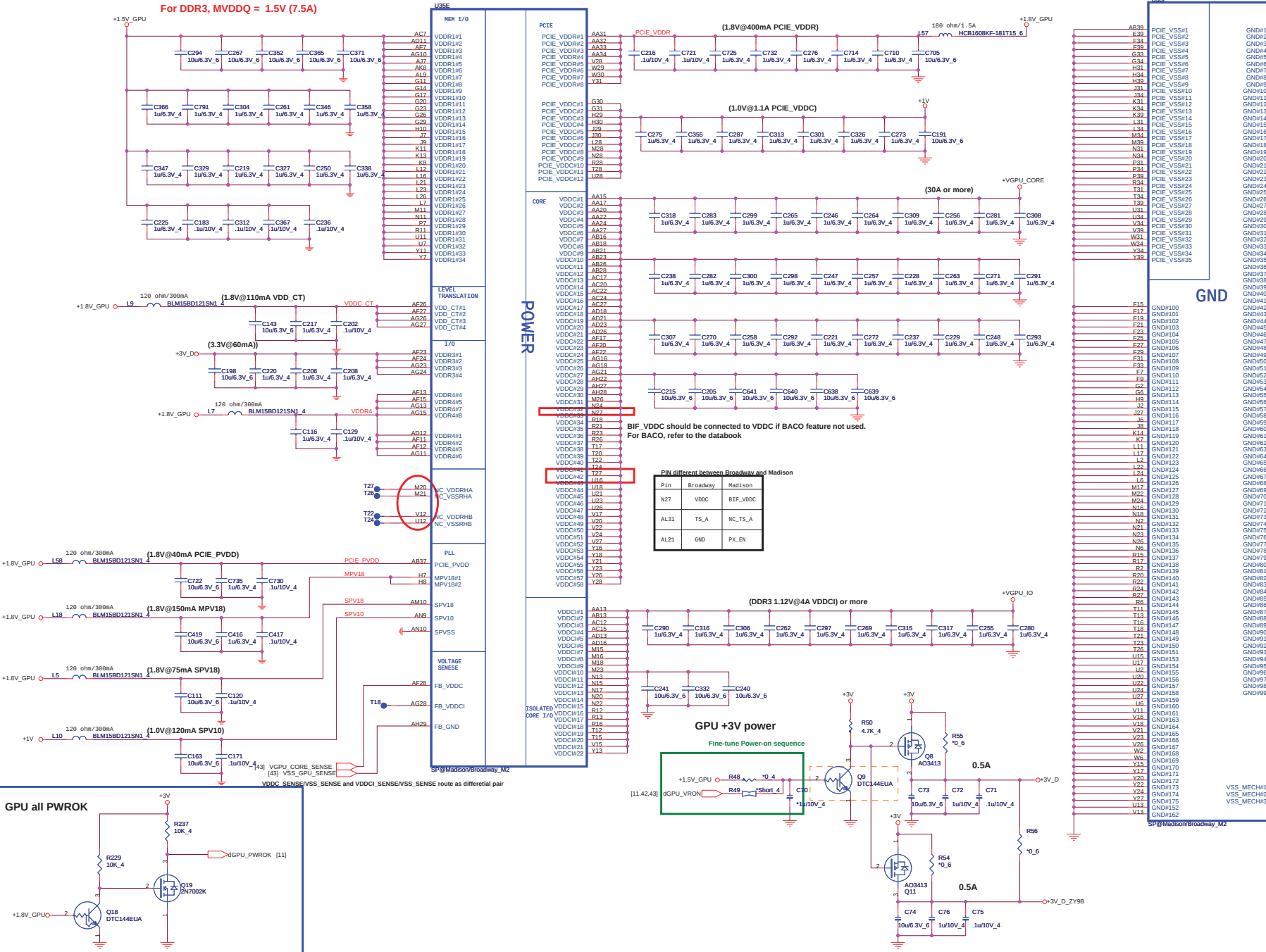
HDMI

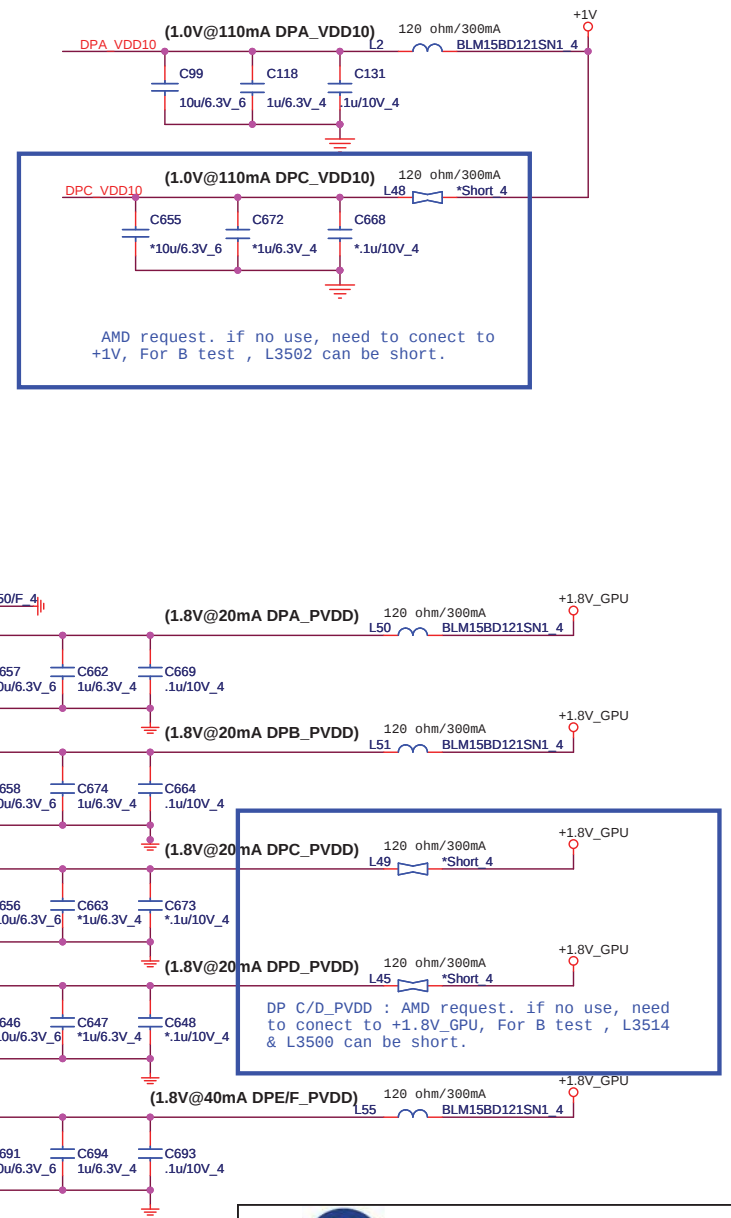
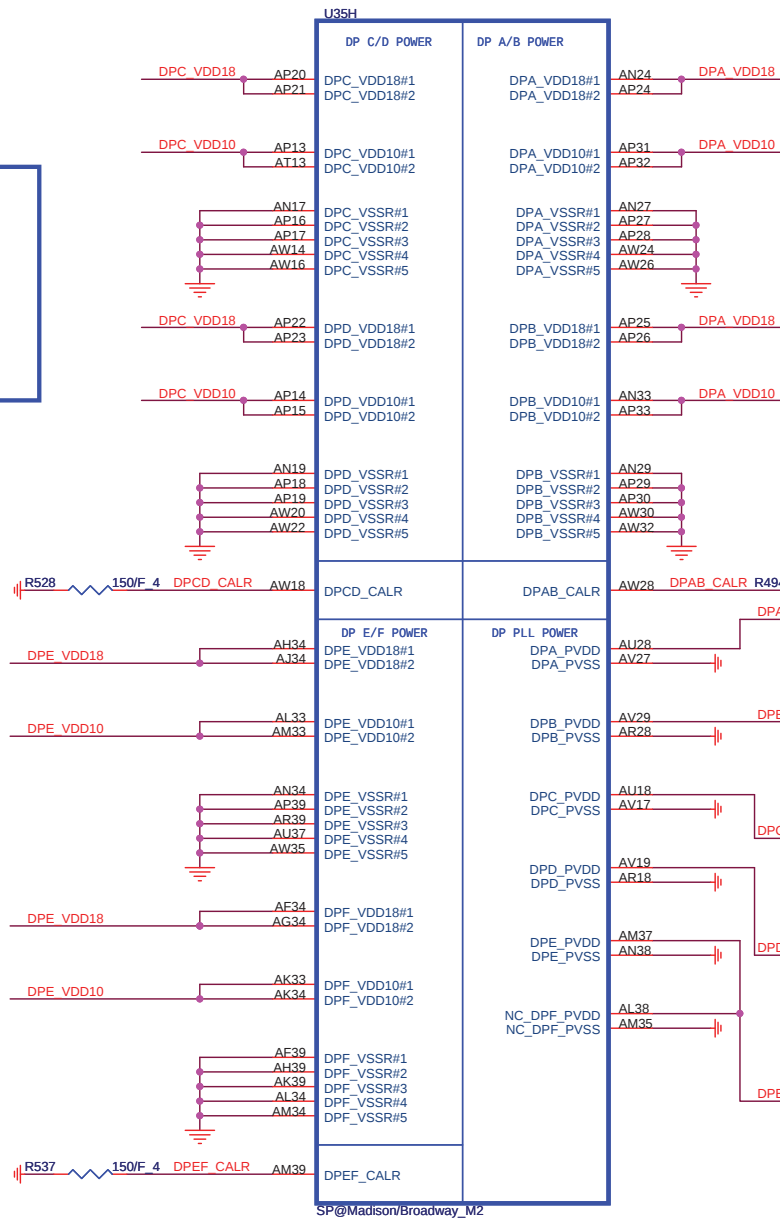
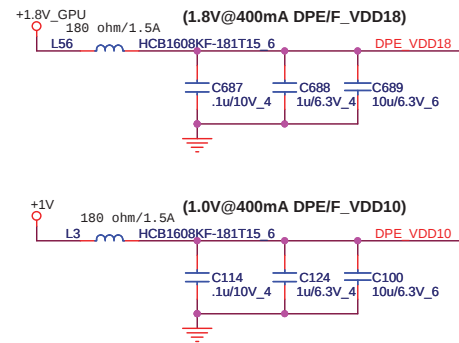
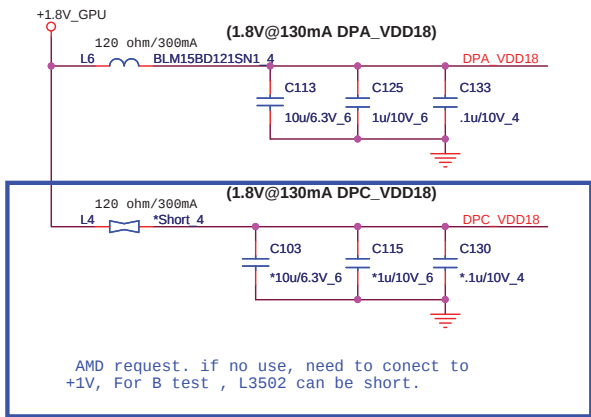
Display Port

LVDS

CRT

For DDR3, MVDDQ = 1.5V (7.5A)



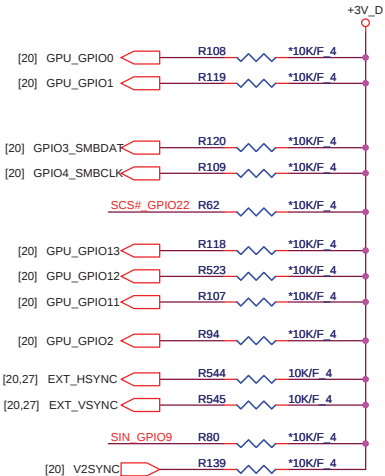


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Size	Document Number	Rev
	Madison/Broadway (DP_PWR/GND)	1A

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PIN STRAPS



Memory Aperture size

GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

Audio Table

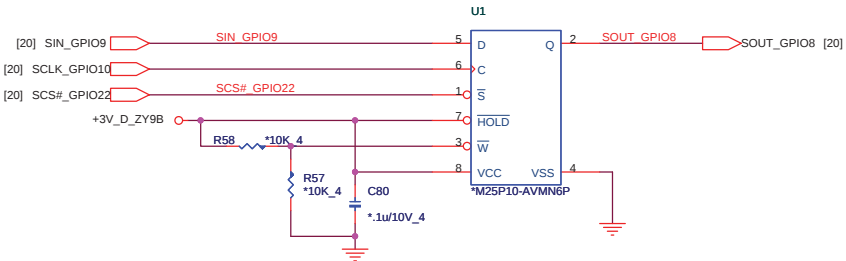
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM

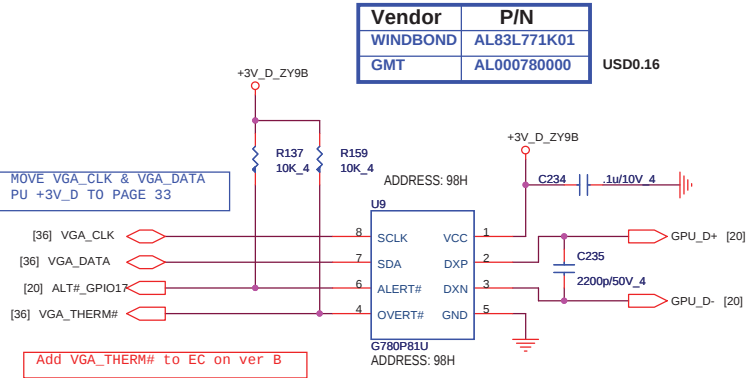


DDR3 VRAM SIZE Strap

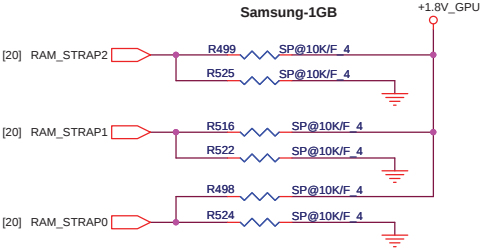
DDR3 VRAM size

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB	1	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1
AMD	23EY2387MA-12	AKD5LGGT700	1GB	0	1	0

Thermal Sensor



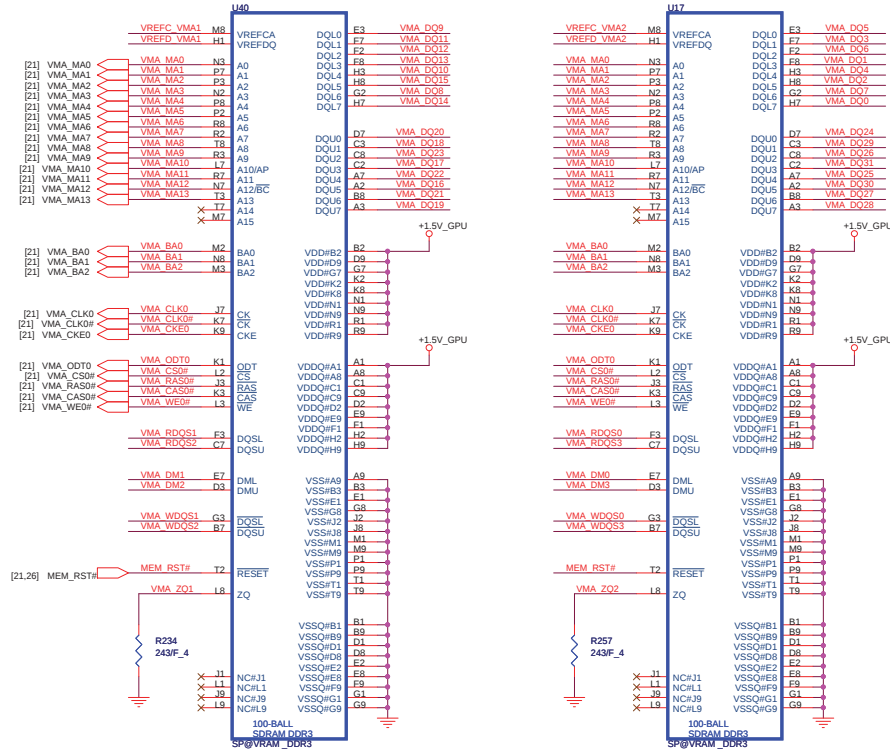
Samsung-1GB



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

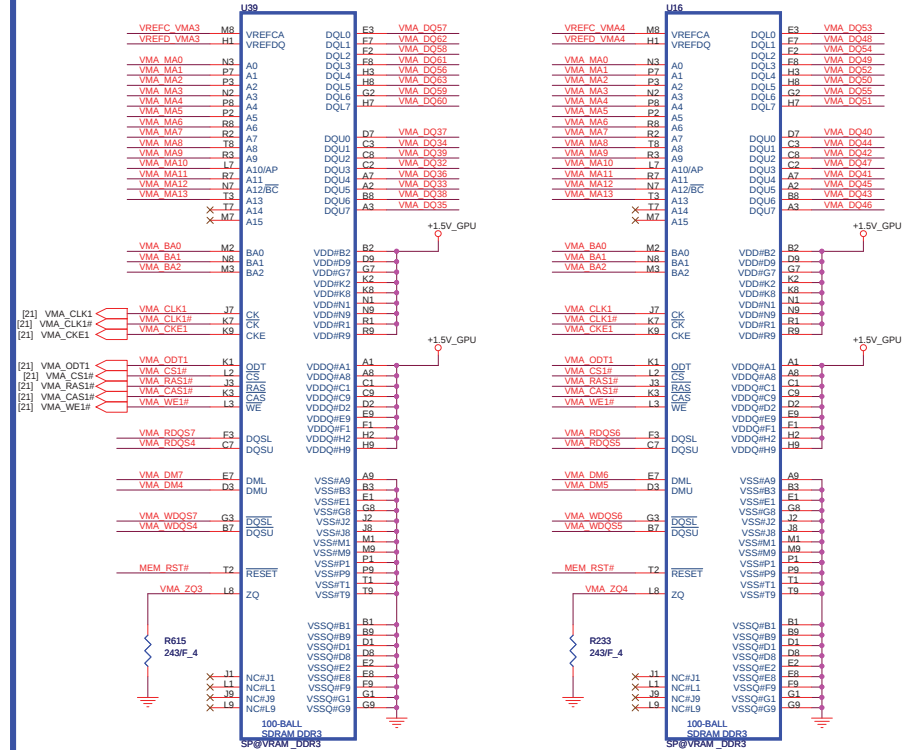
CHANNEL A: 512MB DDR3 (64M*16*4pcs)

[21] VMA_DQ[63..0] VMA_DQ[63..0]
[21] VMA_DM[7..0] VMA_DM[7..0]
[21] VMA_RDQS[7..0] VMA_RDQS[7..0] QSA#[7..0]
[21] VMA_WDQS[7..0] VMA_WDQS[7..0] QSA#[7..0]



TOP Left

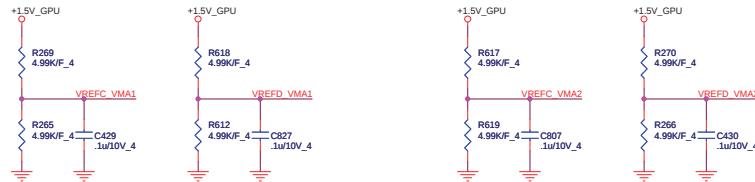
BOT Left



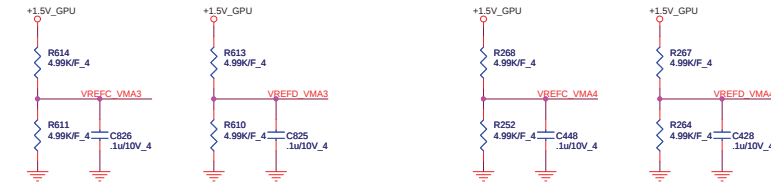
BOT Right

TOP Right

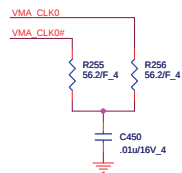
Group-A0 VREF



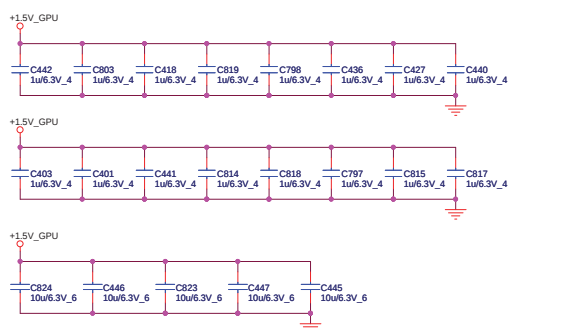
Group-A1 VREF



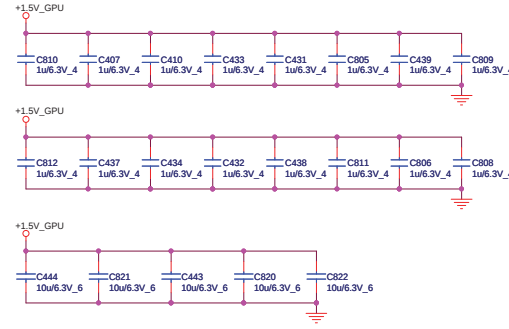
MEM_A0 CLK



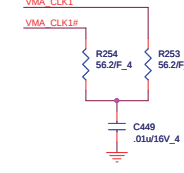
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



Quanta Computer Inc.
PROJECT : ZYA

CHANNEL B: 512MB DDR3 (64M*16*4pcs)

[21] VMB_DQ[63..0]

[21] VMB_DM[7..0]

[21] VMB_RDOQS[7..0]

[21] VMB_WDQS[7..0]

QSA[7..0]

QSA# [7..0]

BOT Down

TOP Down

TOP Up

BOT Up

Group-B0 VREF

Group-B1 VREF

MEM_B0 CLK

Group-B0 decoupling CAP

Group-B1 decoupling CAP

MEM_B1 CLK

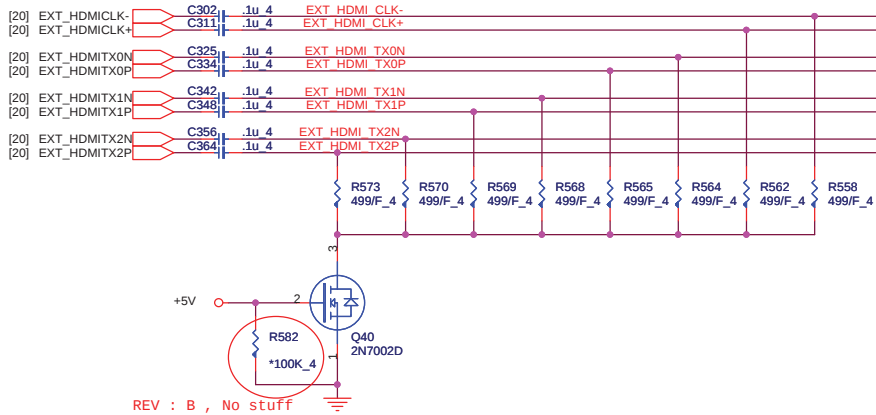
Quanta Computer Inc.
PROJECT : ZYA
Date: Wednesday, January 20, 2010 Sheet 28 of 50

 **Quanta Computer Inc.**
PROJECT : ZYA

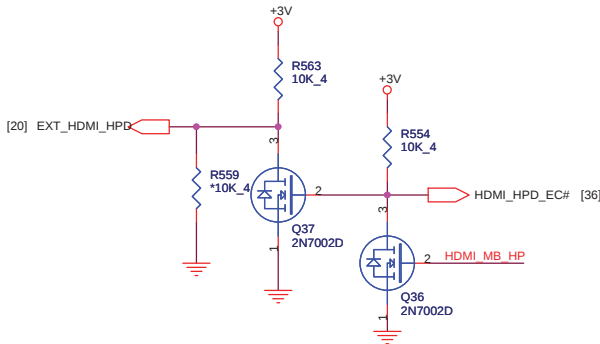
Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	MEMORY 2 channel B	1A
Date:	Wednesday, January 20, 2010	Sheet 26 of 50

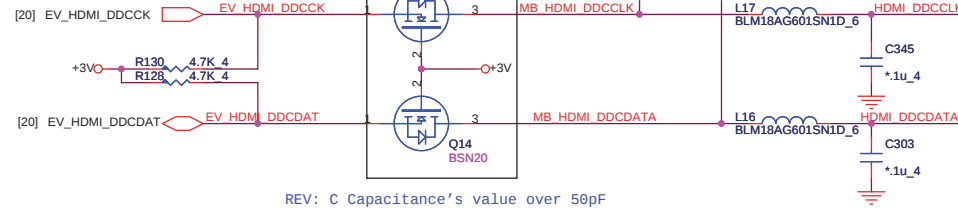
HDMI



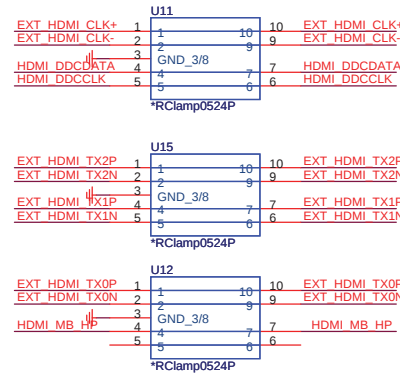
HDMI Hot-PLUG to EC and GPU



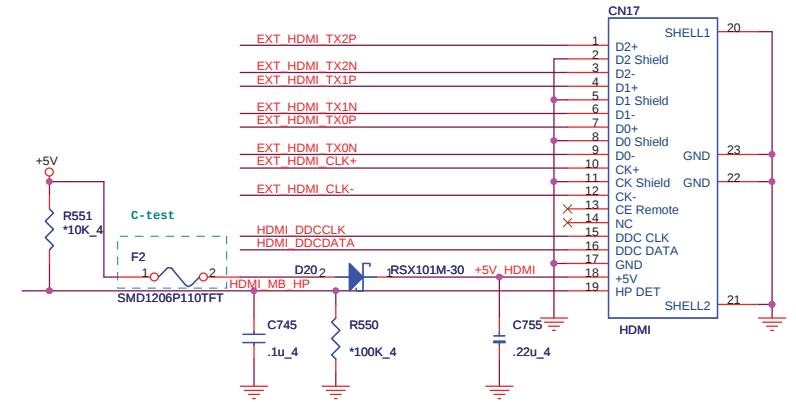
SDVO I2C Control



ESD Protect

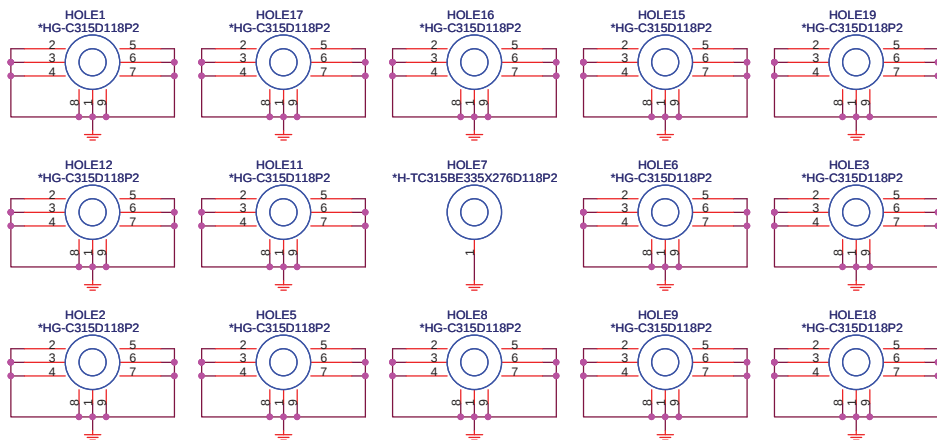


HDMI connector

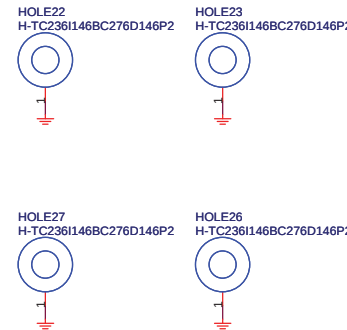


EXT_HDMI_CLK- R1008 *100 4 EXT_HDMI_CLK+
EXT_HDMI_TX2N R1007 *100 4 EXT_HDMI_TX2P
EXT_HDMI_TX1N R1008 *100 4 EXT_HDMI_TX1P
EXT_HDMI_TX0N R1008 *100 4 EXT_HDMI_TX0P
REV : B HDMI reserve 100 ohm parallel
resistor for EMI

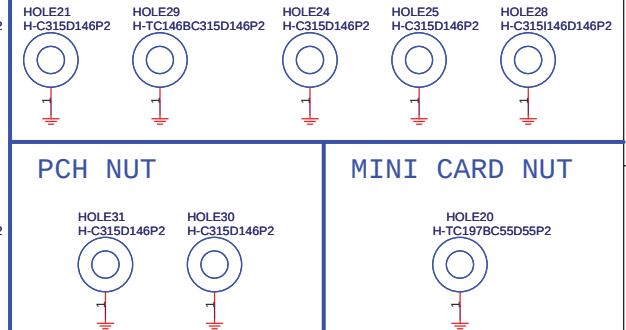
SCREW HOLE



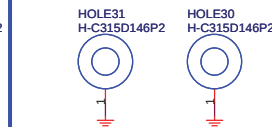
CPU NUT



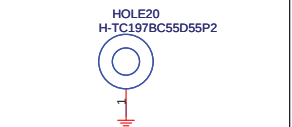
PCH & GPU NUT



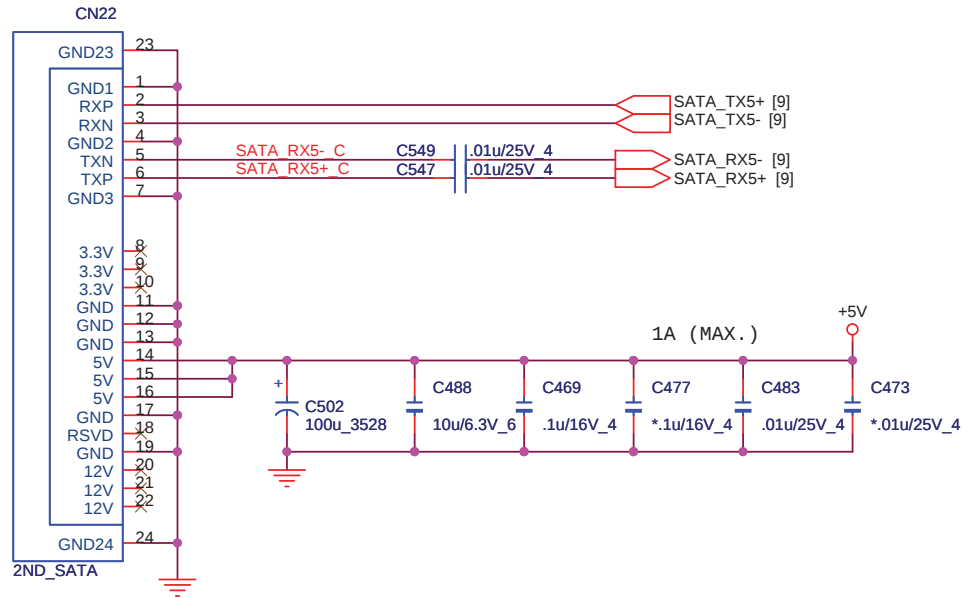
PCH NUT



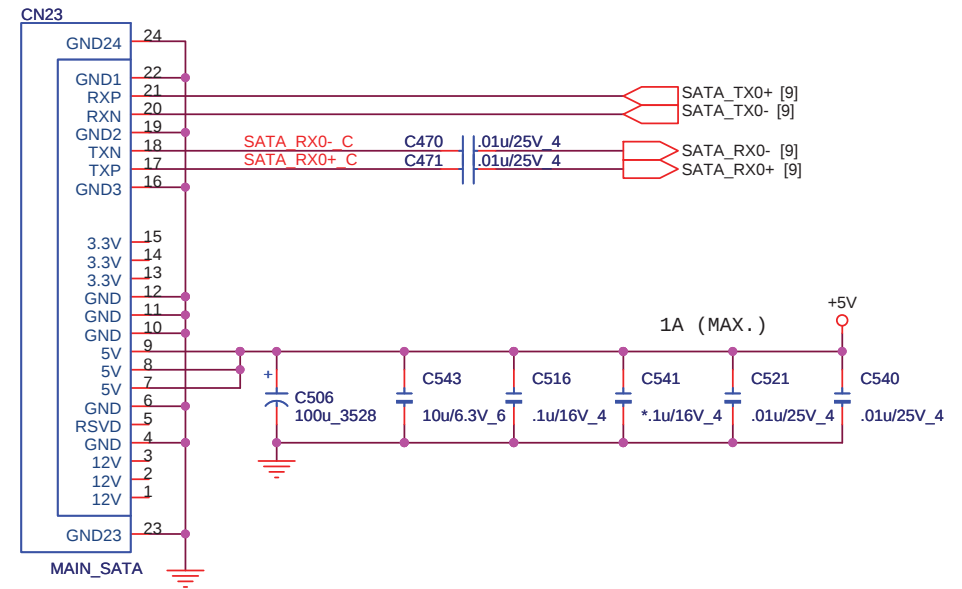
MINI CARD NUT



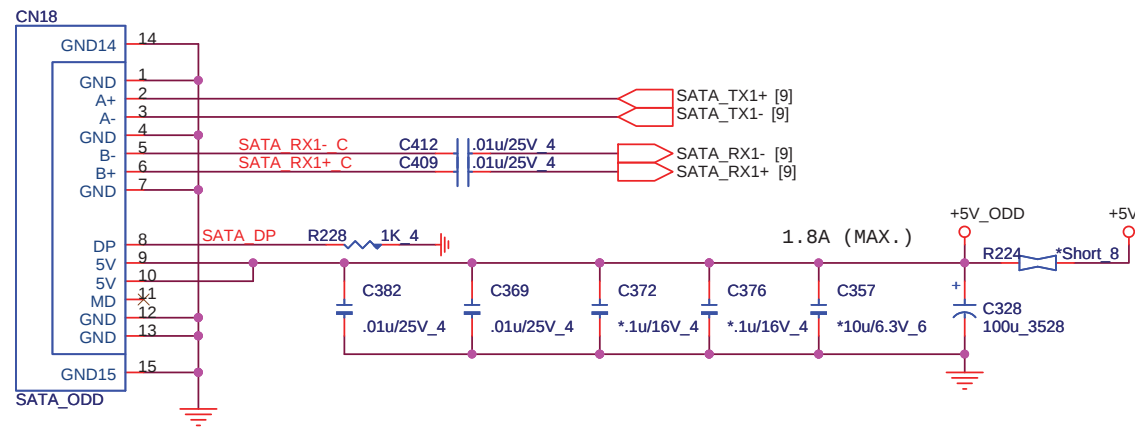
2nd SATA HDD (edge of board)



MAIN SATA HDD



ODD (SATA)



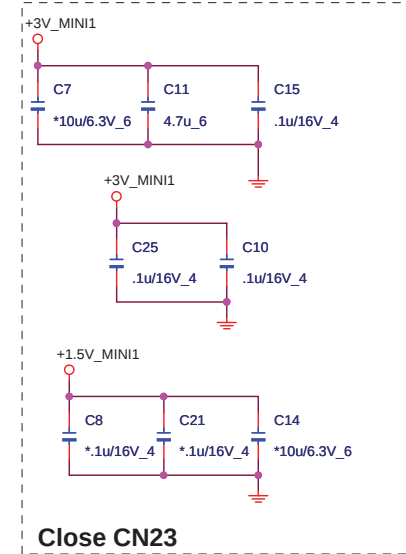
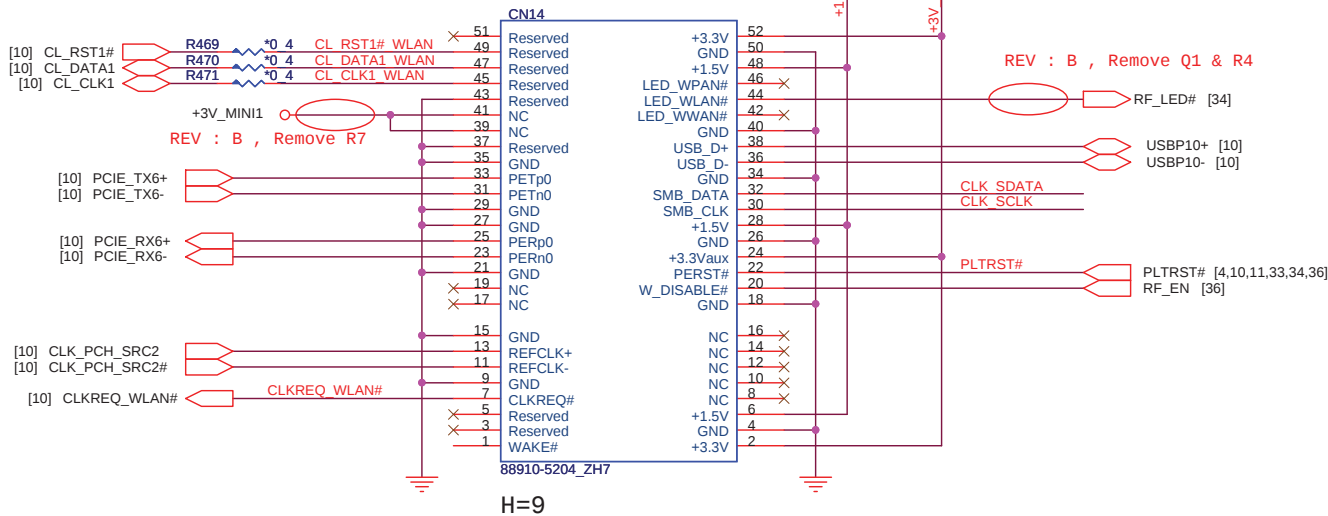
Quanta Computer Inc.
PROJECT : ZYA

Size	Document Number	Rev
	SATA-HDD/ODD	1A
Date:	Wednesday, January 20, 2010	Sheet 29 of 50

Wireless

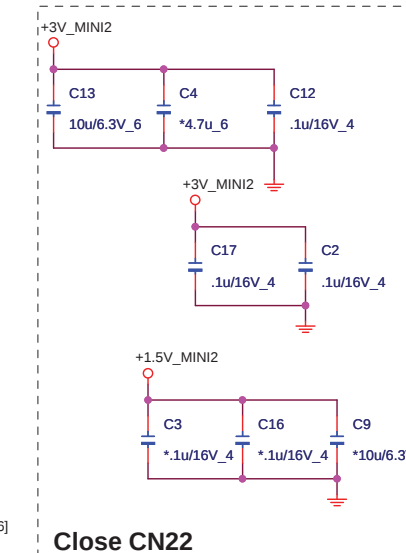
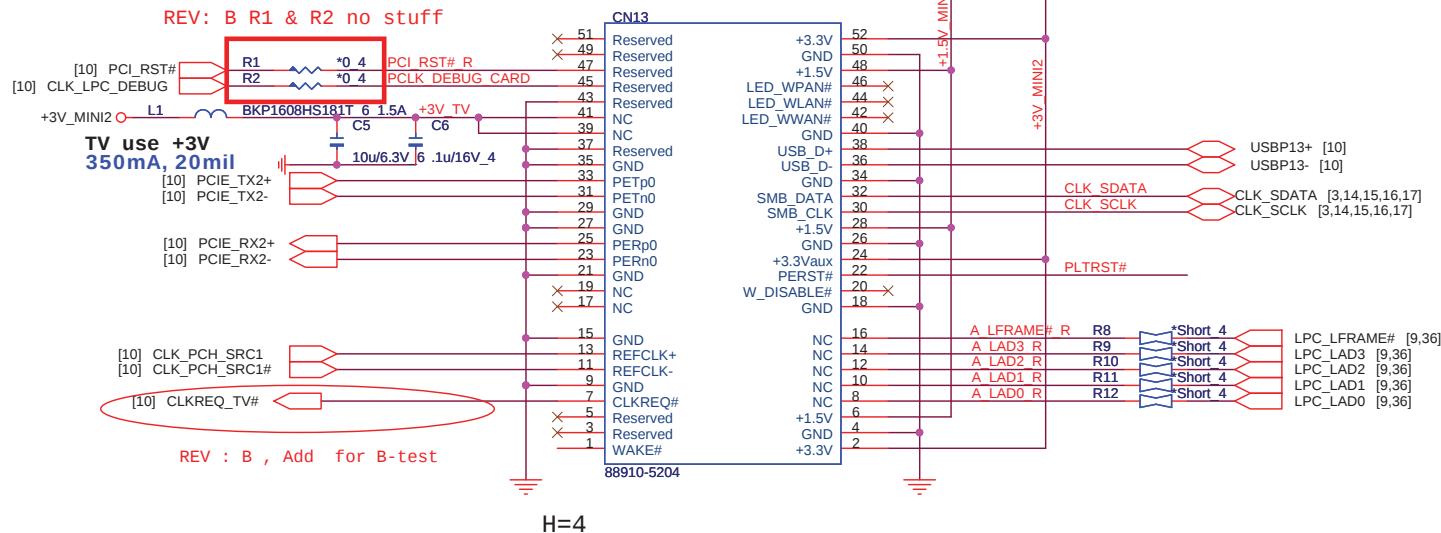
+3.3V: 2700mA
+1.5V: 500mA

Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4



TV and Debug

REV: B R1 & R2 no stuff

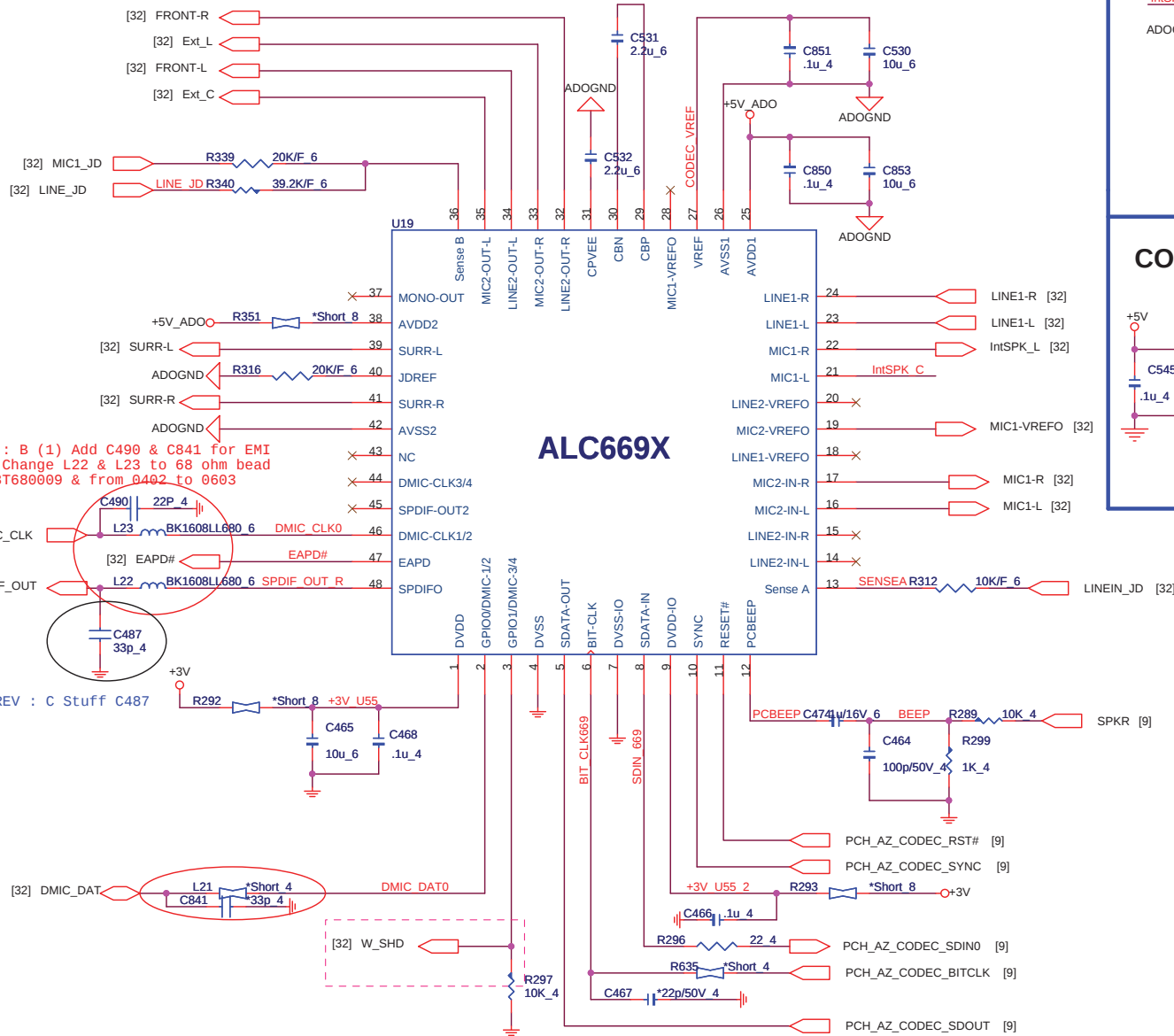


Quanta Computer Inc.

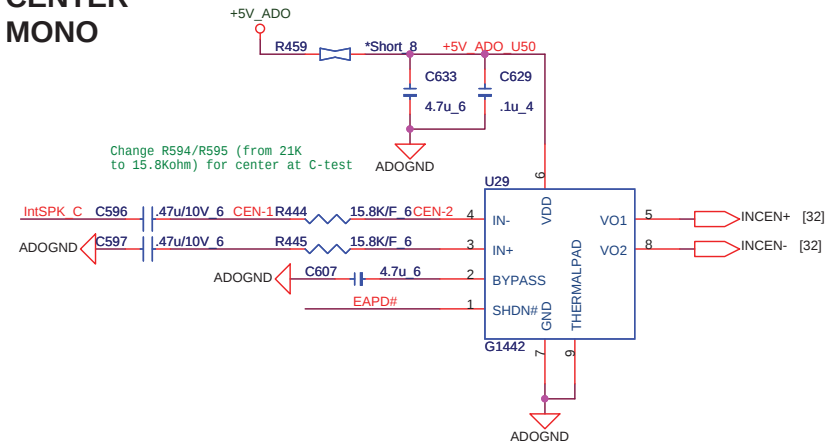
PROJECT : ZYA

Size	Document Number	Rev
		1A
Date:	Wednesday, January 20, 2010	Sheet 30 of 50

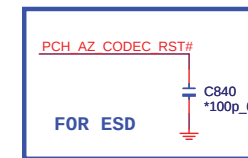
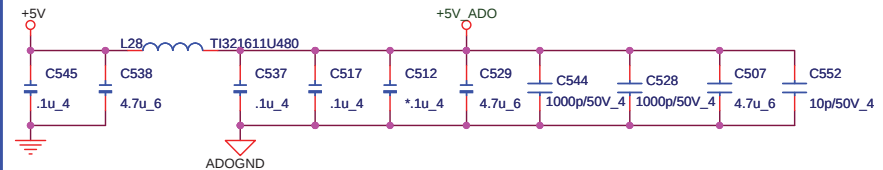
CODEC(ALC669X)



CENTER MONO



CODEC/AMP Power

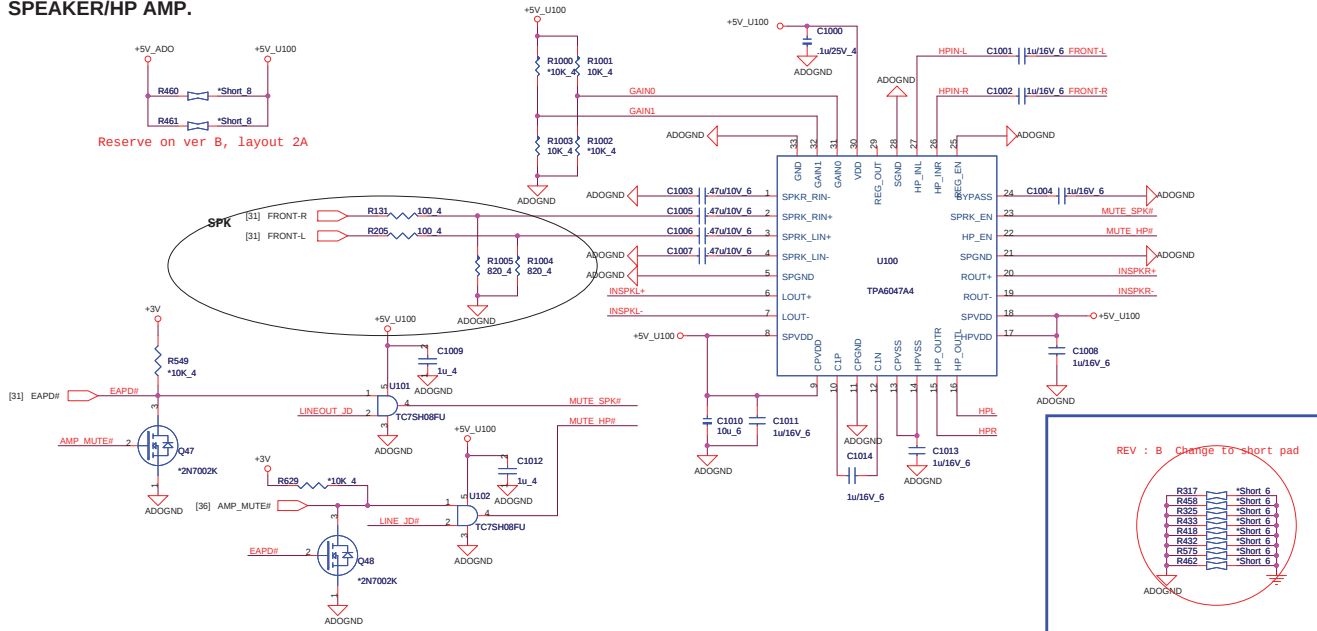


Quanta Computer Inc.
PROJECT : ZYA

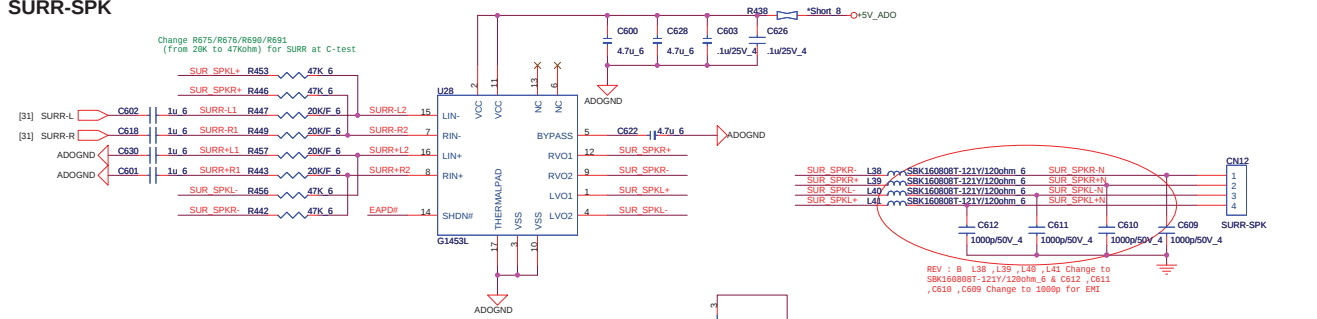
Size	Document Number	Rev 1A
Date: Wednesday, January 20, 2010	Sheet 31 of 50	

REALTEK ALC889X/MONO-AMP

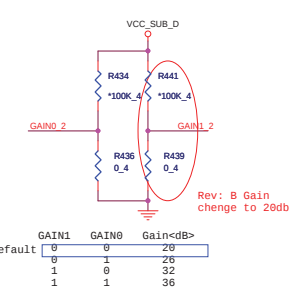
SPEAKER/HP AMP.



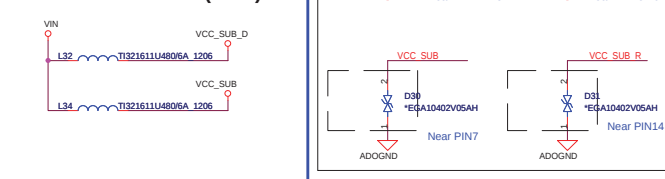
SURR-SPK



AMO GAIN



SUBWOOFER Power(AMP)

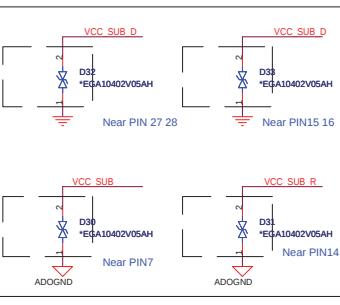


SUBWOOFER

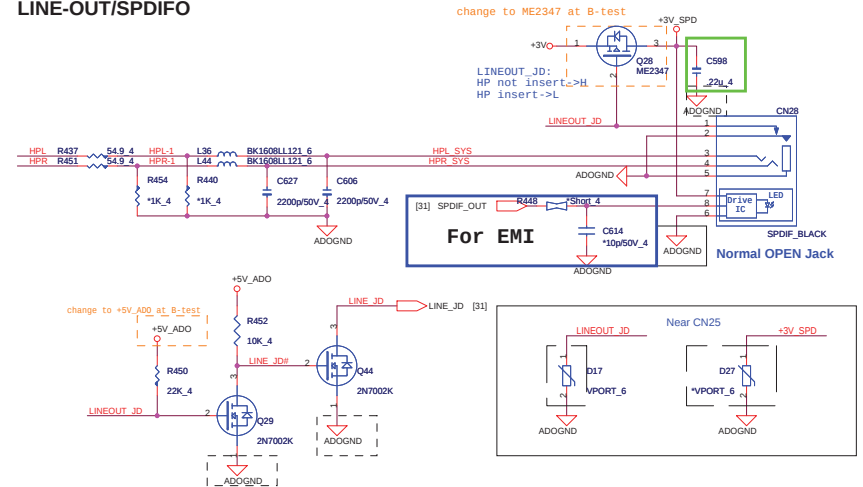
LPF for $f_c(-3dB)=500Hz$

SDZ :: shutdown signal for IC<LOW=disable>, HIGH=enable>

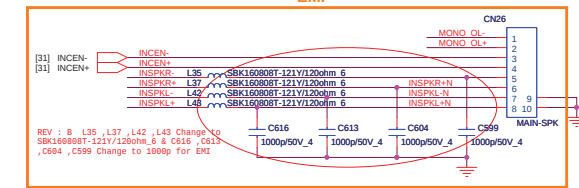
SHUTDOWN	TPA3110D1
L (0V~0.8V)	SHUTDOWN
H (2V ~ VDD)	ACTIVE



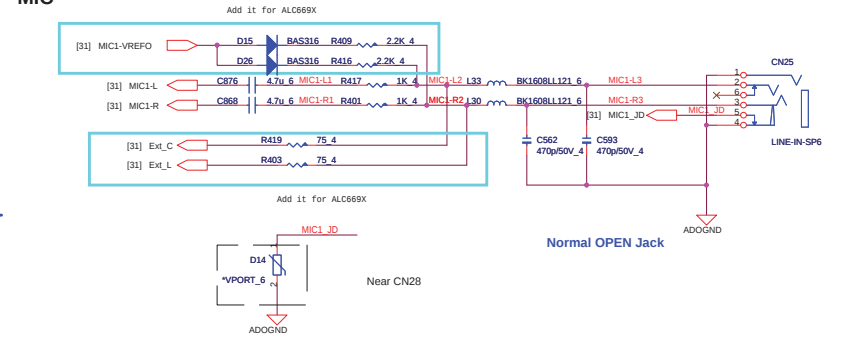
LINE-OUT/SPDIFO



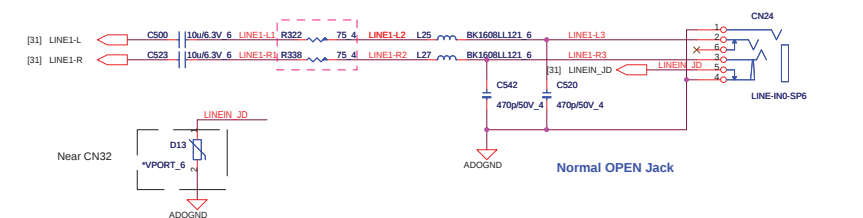
Main SPK/Center/Subwoofer EMI



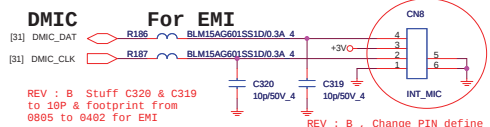
MIC

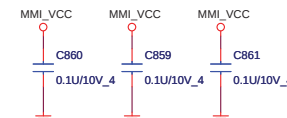


LINE IN



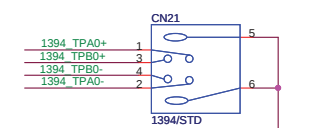
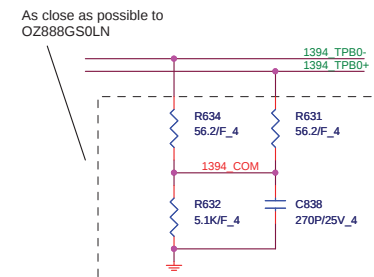
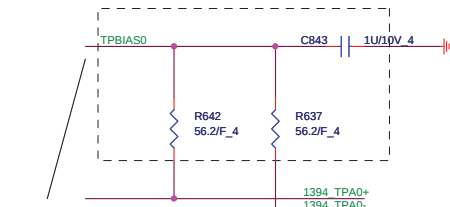
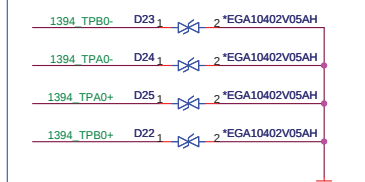
DMIC





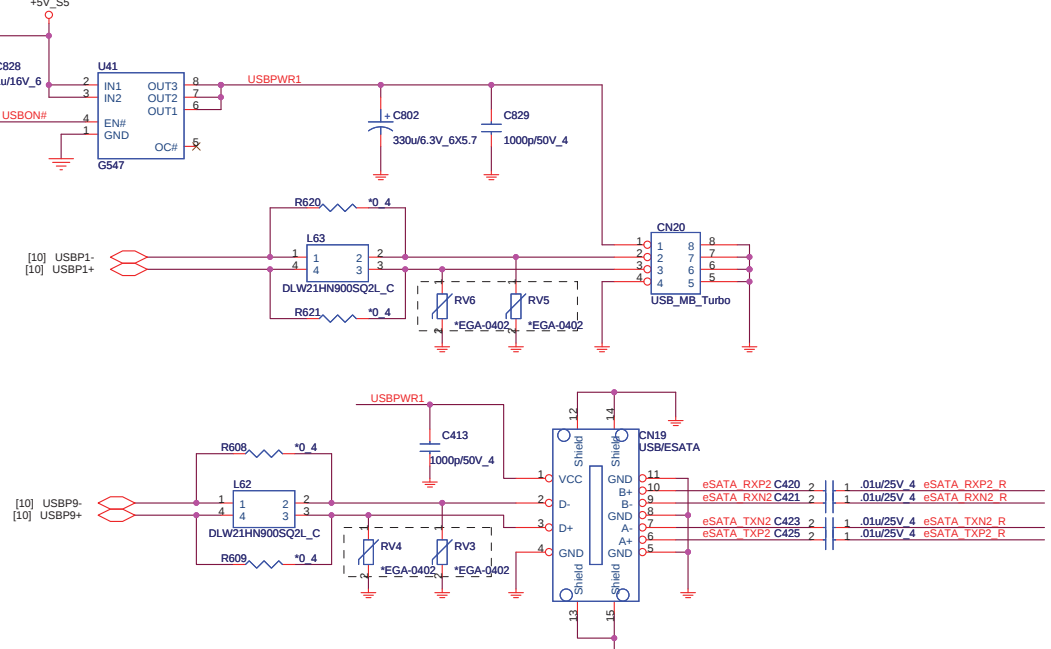
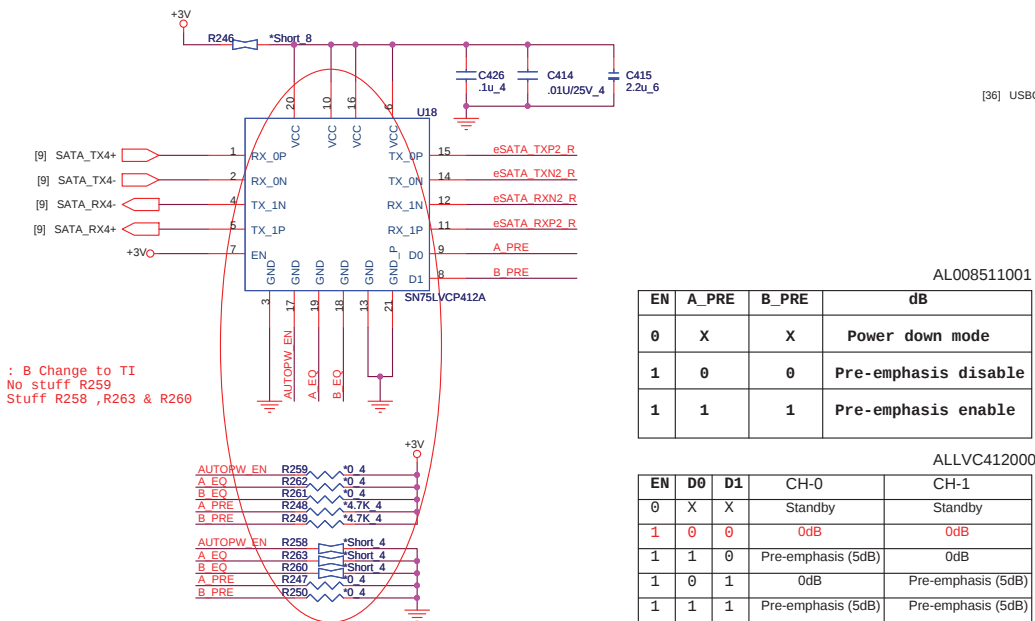
CN11					
XD_R/B	1	XD-R/B	MS-DATA1	20	<u>XD/MS DATA1</u>
XD-RE#	2	XD-RE	MS-BS	21	<u>SD/XD/MS CMD</u>
XD_CE#	3	XD-CE	4IN1-DIO2	22	
XD-CLE	4	XD-CLE	SD-VCC	23	
<u>SD/XD/MS CMD</u>	5	XD-ALE	SD-CLK	24	<u>XD_CE#</u>
XD-WE	6	XD-WE	SD-DAT0	25	<u>XD/MS/MS DATA0</u>
XD_WP#	7	XD-WP	XD-D2	26	<u>XD/MS DATA2</u>
<u>SD/XD/MS DATA0</u>	8	XD-D0	XD-D3	27	<u>XD/MS DATA3</u>
XD/MS DATA1	9	XD-D1	XD-D4	28	<u>XD/MS DATA4</u>
SD DATA2	10	SD-DAT2	SD-DAT1	29	<u>SD DATA1</u>
<u>SD/XD/MS DATA3</u>	11	XD-D5	XD-D6	30	<u>XD/MS DATA5</u>
<u>SD/XD/MS CMD</u>	12	SD-CMD	XD-D7	31	<u>XD/MS DATA6</u>
	13	4IN1-GND1	XD-VCC	32	<u>XD/MS DATA7</u>
	14	MS-VCC	XD-DCC	33	
XD_CE#	15	MS-SCLK	XD-CD-SW	34	<u>XD_CDSW#</u>
<u>SD/XD/MS DATA3</u>	16	MS-DATA3	SD-WP-SW	35	<u>XD_WP#</u>
MS_IN#	17	MS-INS	SD-CD-SW	36	<u>SD CD</u>
<u>XD/MS DATA2</u>	18	MS-DATA2			
<u>SD/XD/MS DATA0</u>	19	MS-DATA0			

As close as possible to
CN35 Pin12

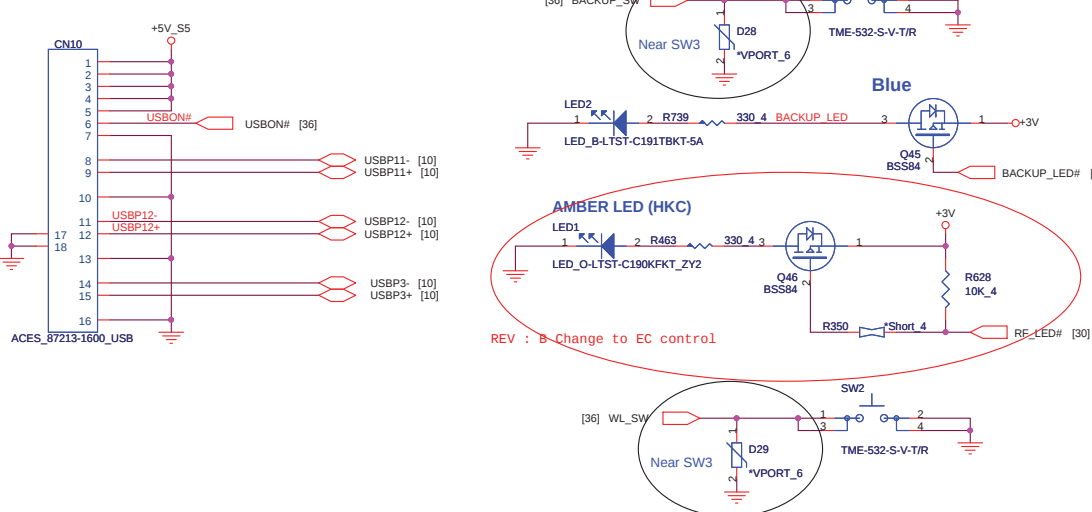


These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance (Zo) of 110ohms.

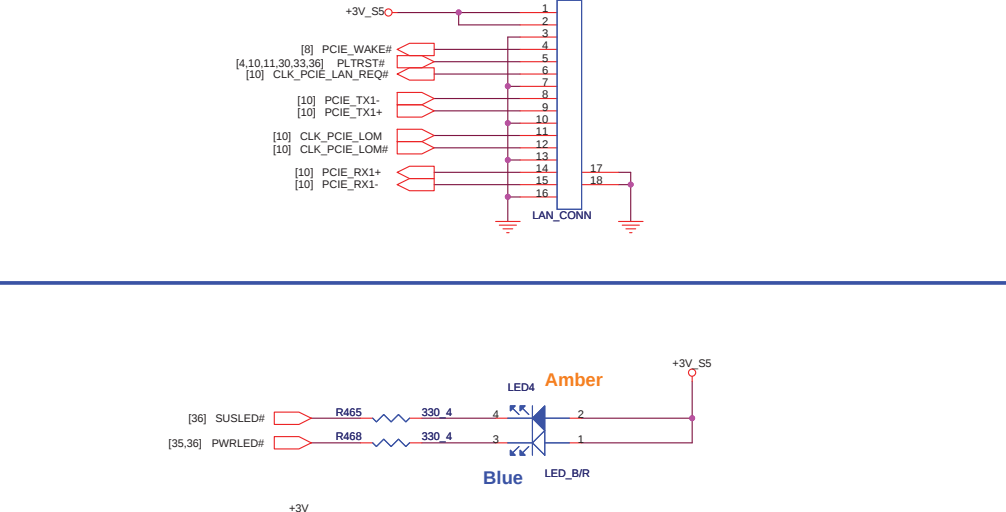
ESATA & USB



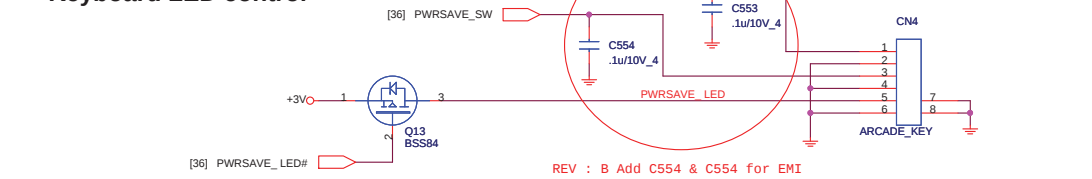
To USB/B



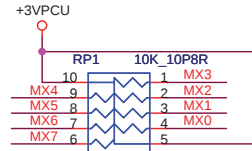
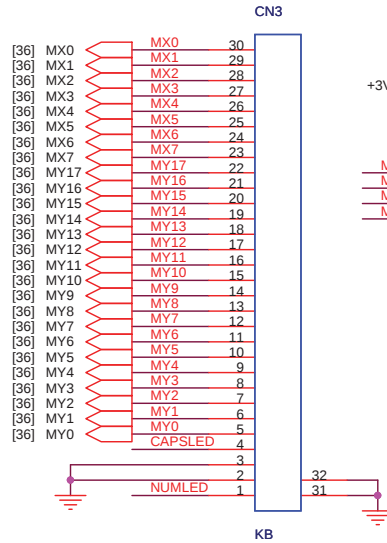
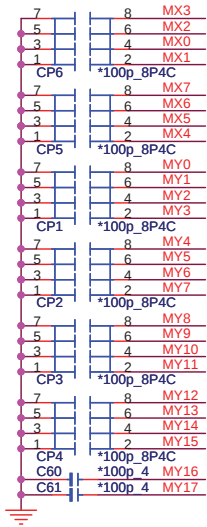
To LAN/B



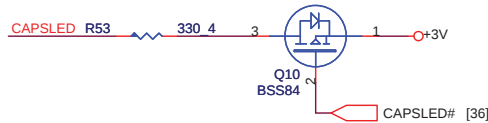
Keyboard LED control



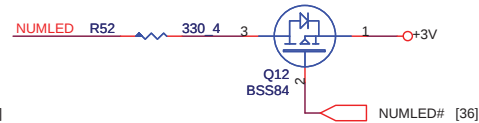
INT K/B



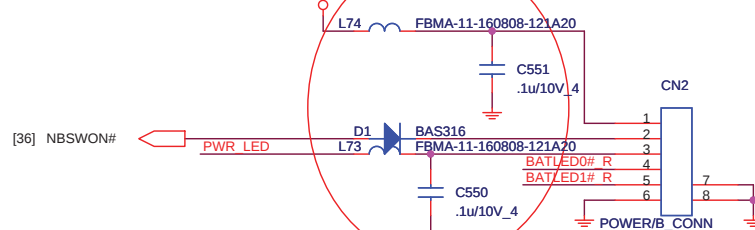
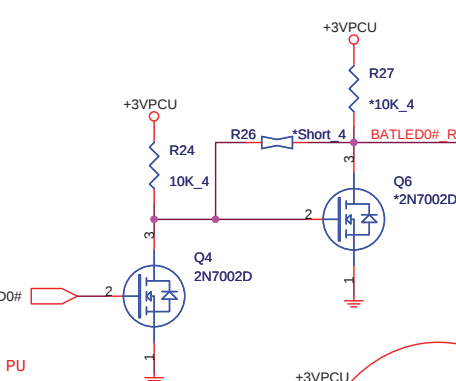
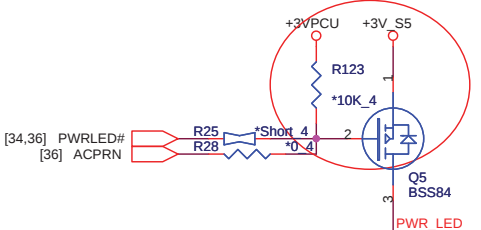
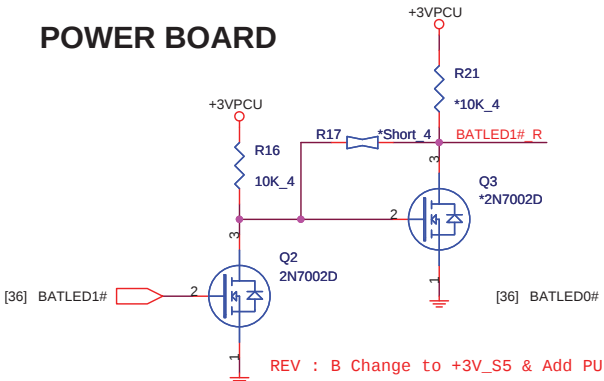
AMBER LED (HKC)



AMBER LED (HKC)

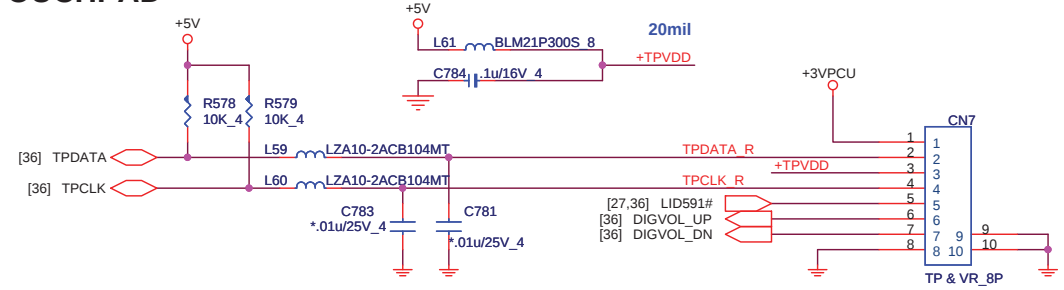


POWER BOARD

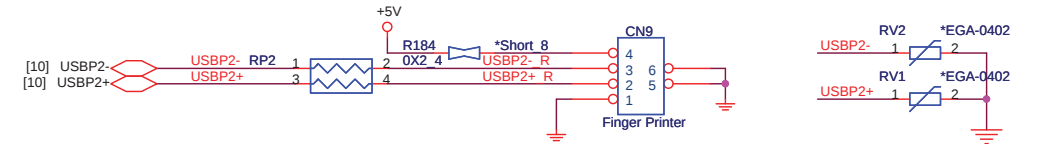


REV : B Add L73 ,L74 , C551 & C550 for EMI

TOUCHPAD

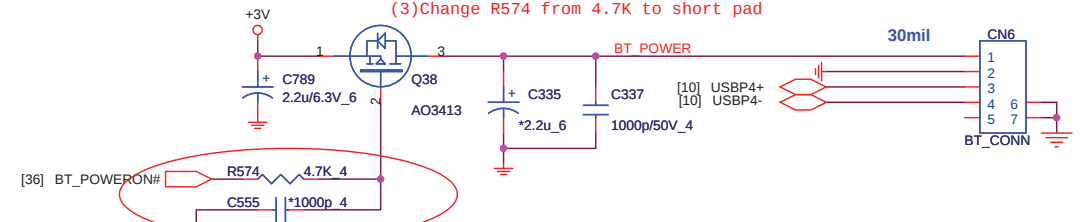


Finger-Printer

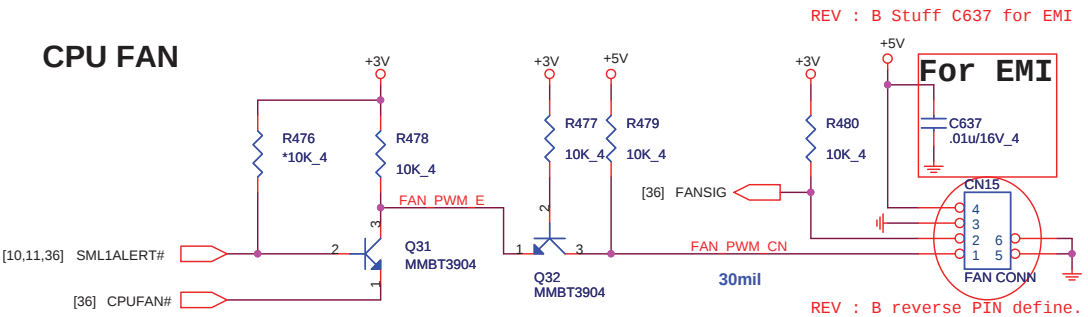


BLUETOOTH

Rev: B (1) del. R575
(2)change C789 from .33u to 2.2u
(3)Change R574 from 4.7K to short pad



CPU FAN

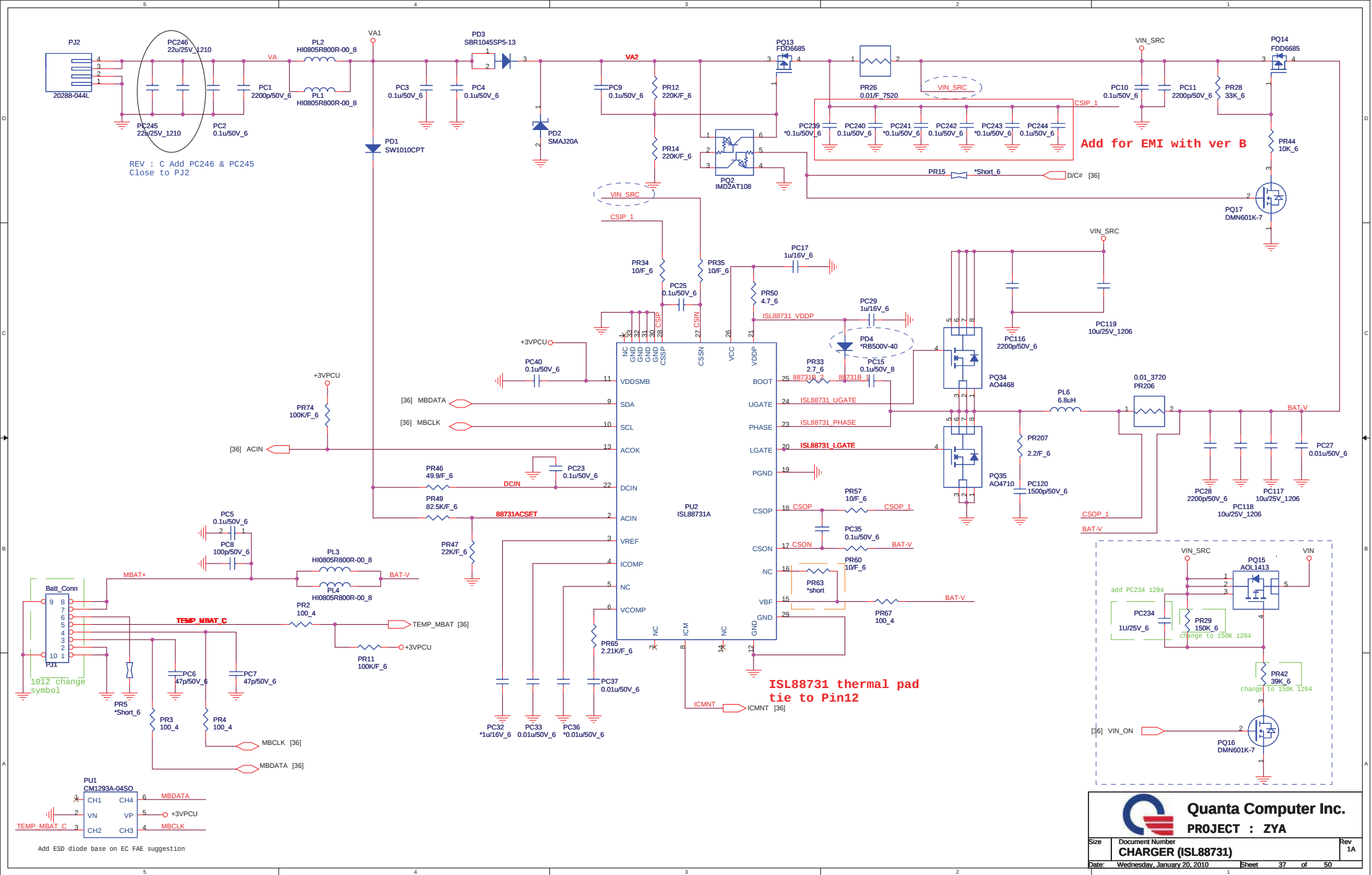


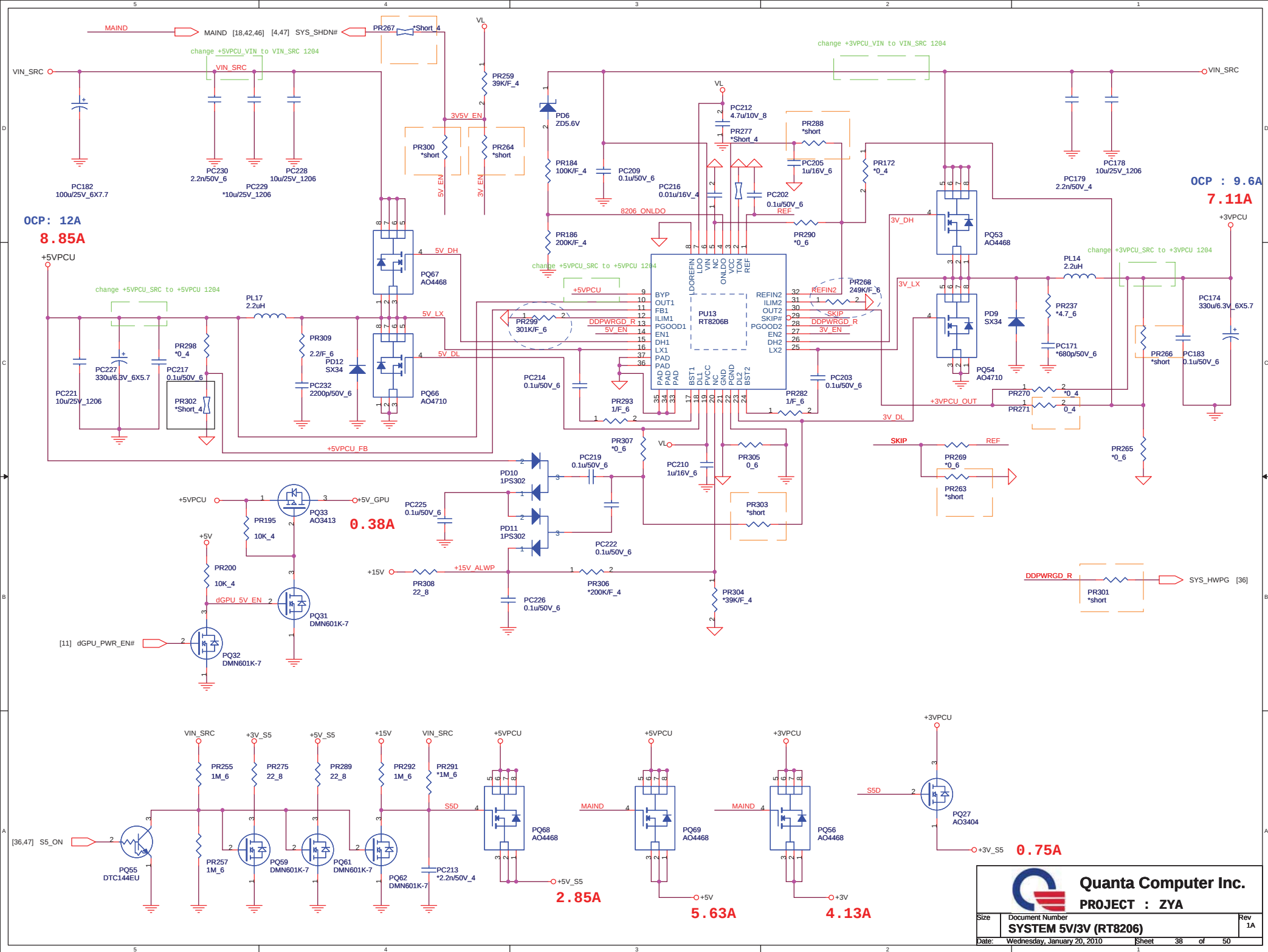
REV : B Stuff C637 for EMI

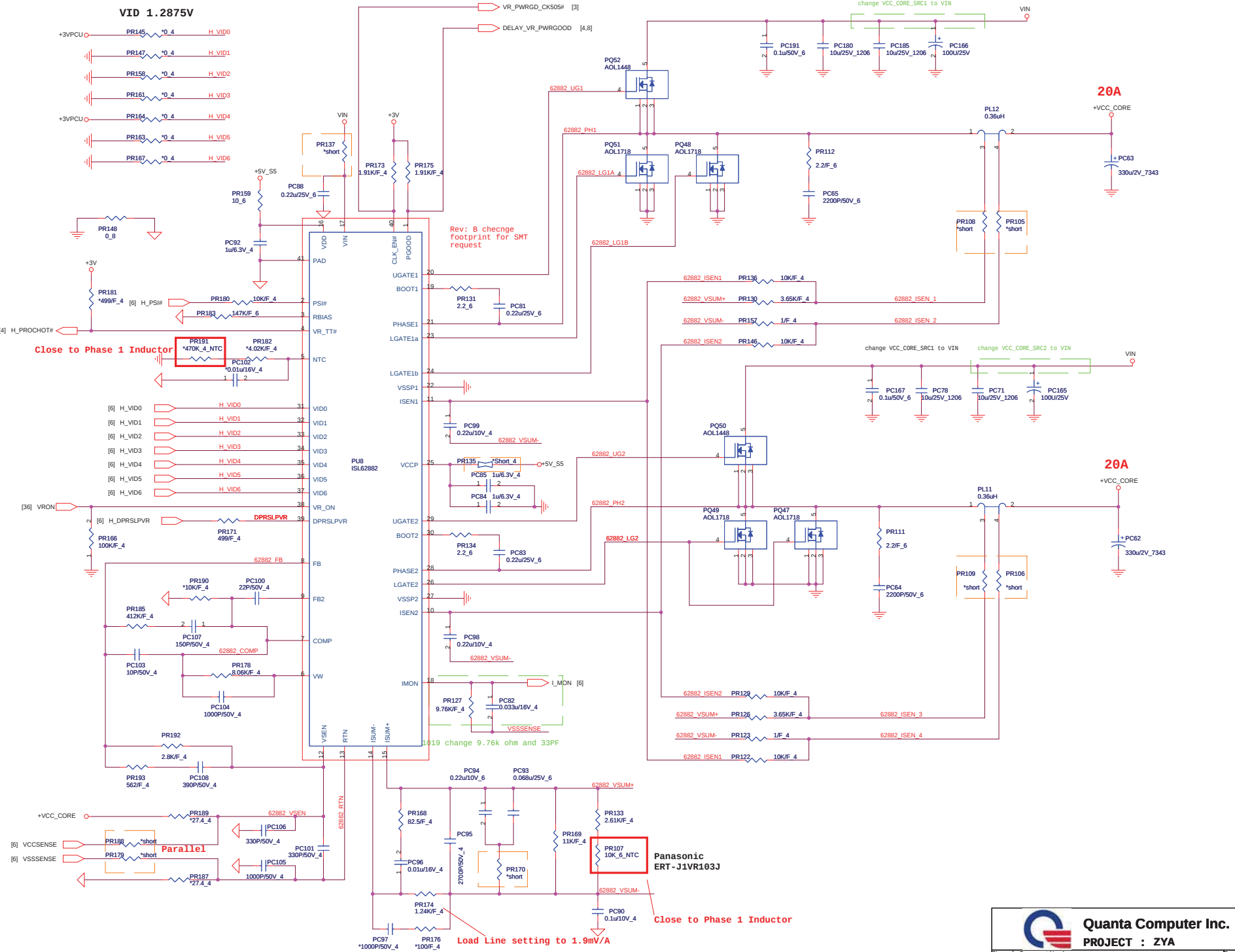
REV : B reverse PIN define.



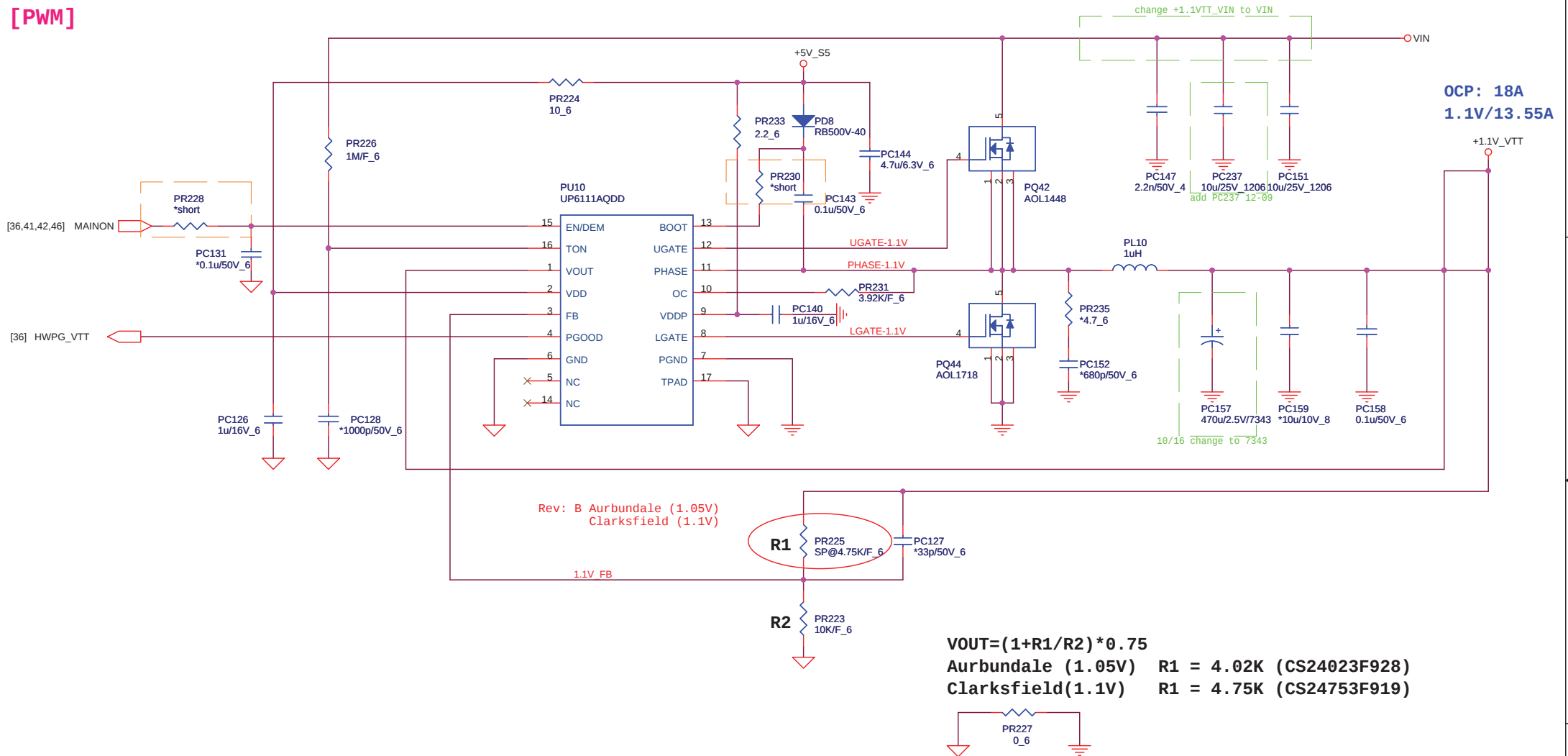
Quanta Computer Inc.
PROJECT : ZYA







[PWM]



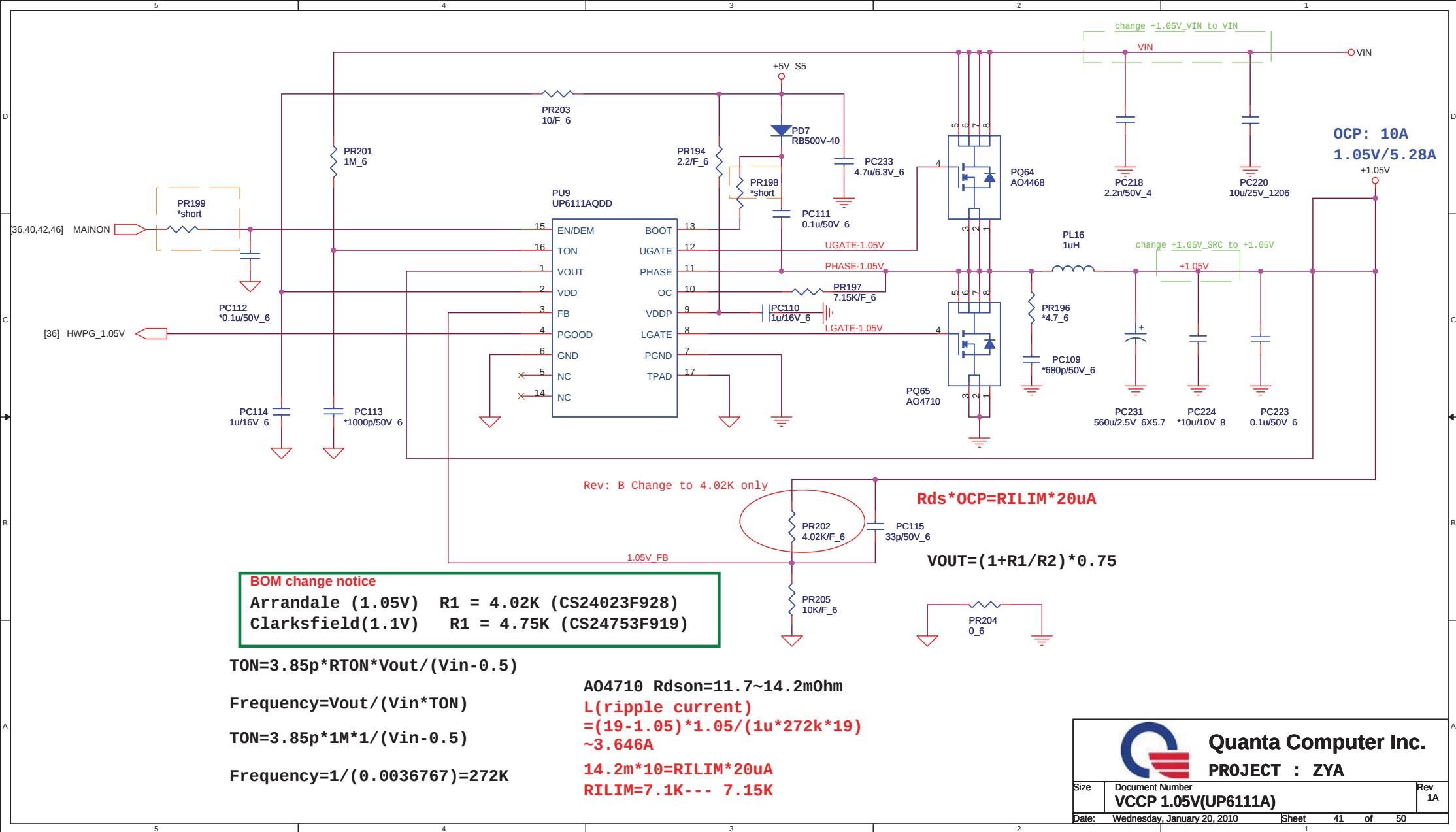
$$TON=3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$$

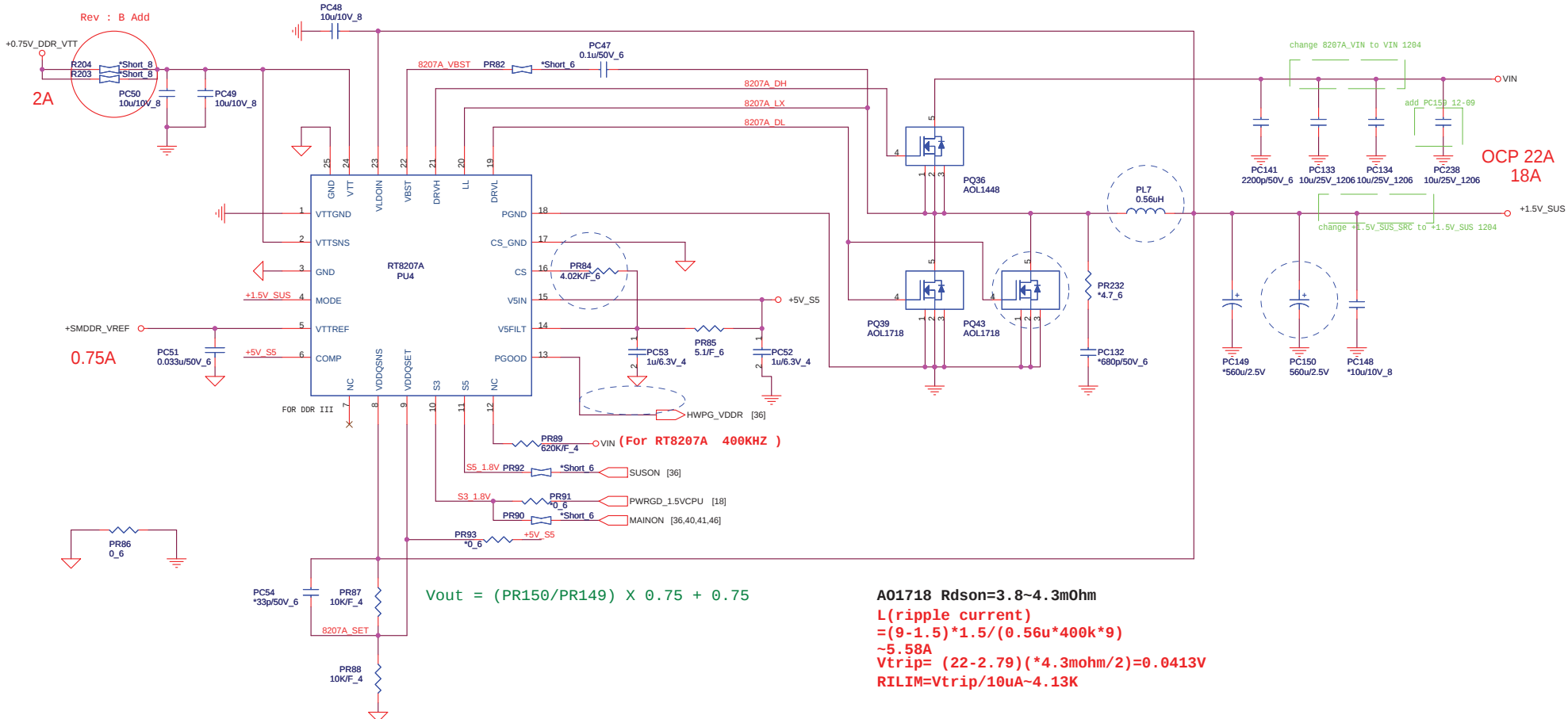
$$Frequency = Vout / (Vin \cdot TON)$$

$$TON=3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

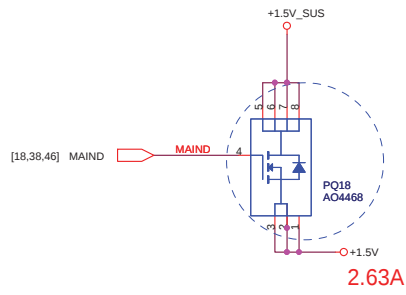
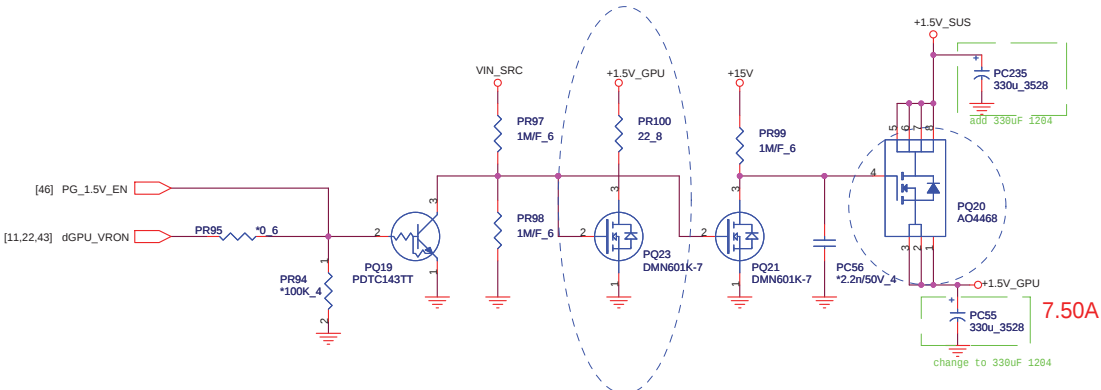
A01718 Rdson=3~4.3mOhm
L(ripple current)
=(19-1.1)*1.1(1u*272k*19)
~3.81A
4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K

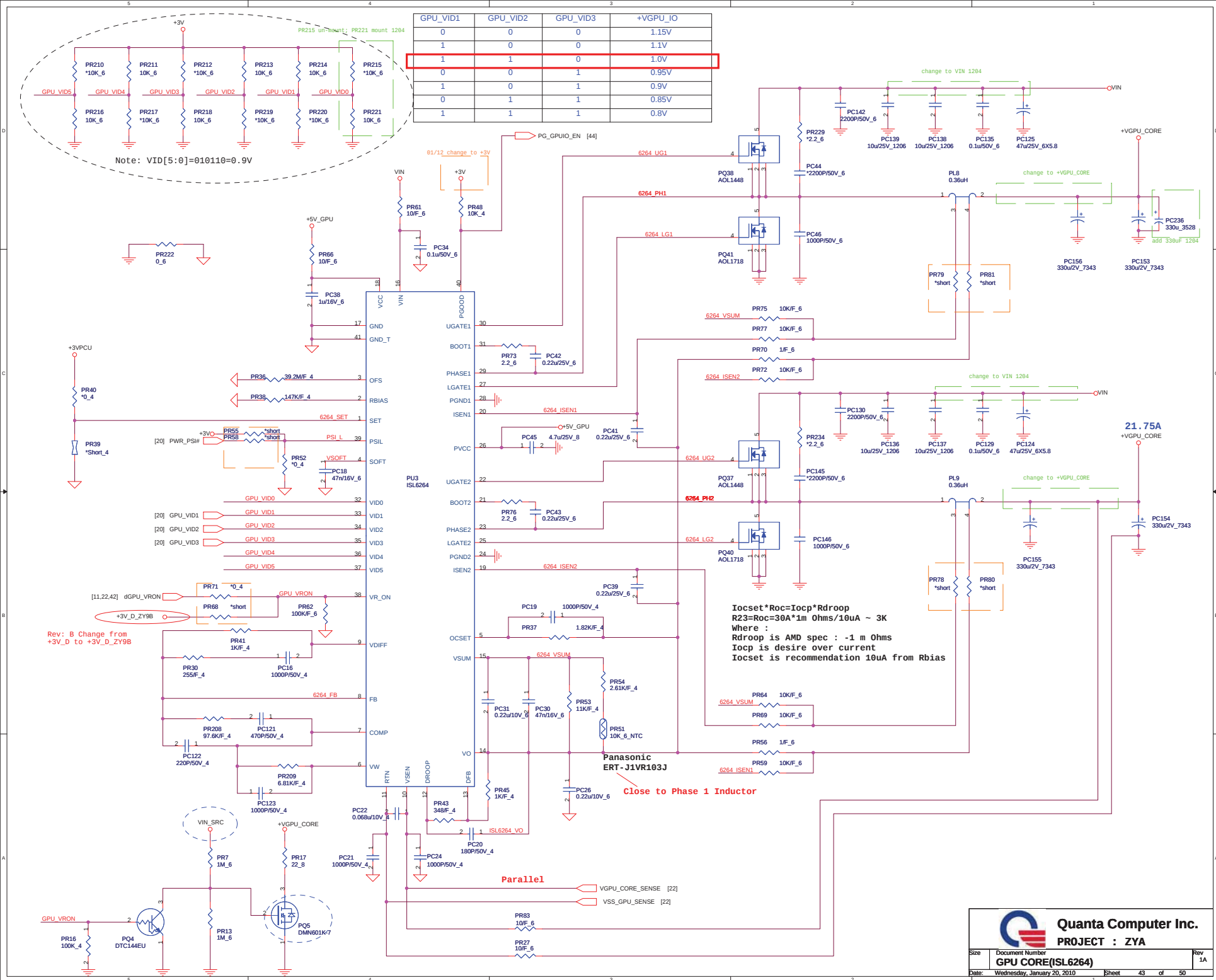




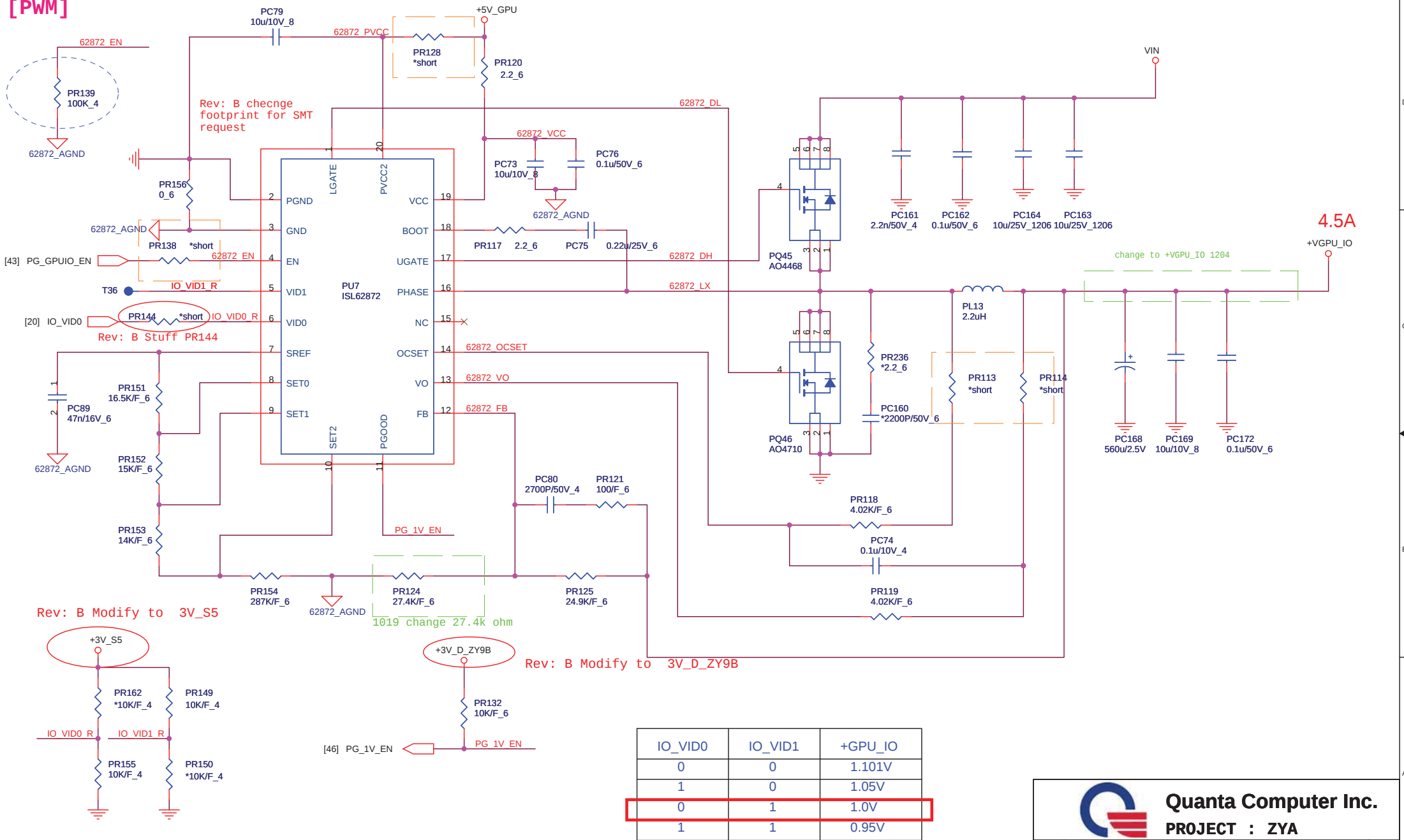
$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

A01718 R_{dson}=3.8~4.3mOhm
L(ripple current)
=(9-1.5)*1.5/(0.56u*400k*9)
~5.58A
V_{trip}= (22-2.79)*(4.3mohm/2)=0.0413V
R_{IILIM}=V_{trip}/10uA=4.13K

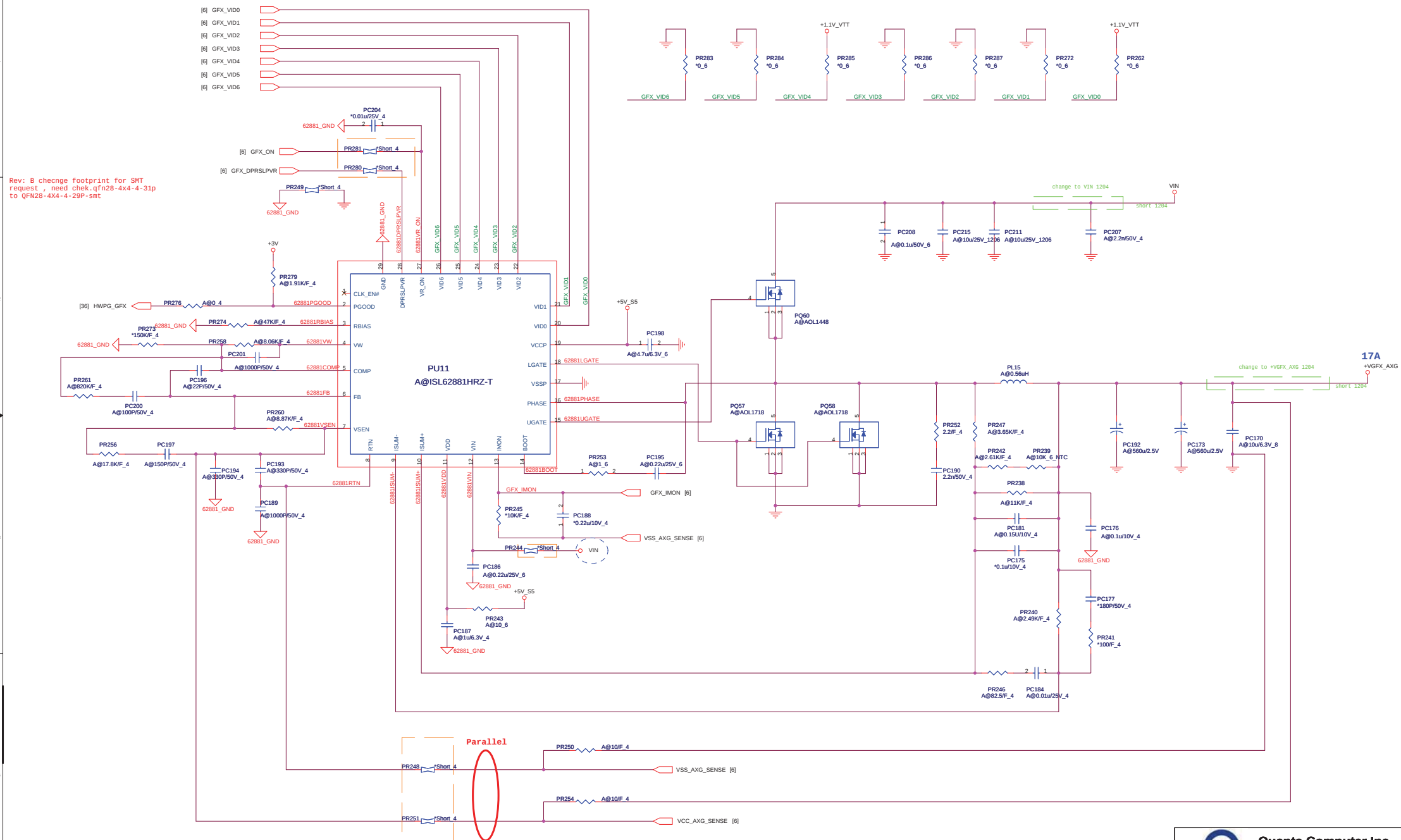




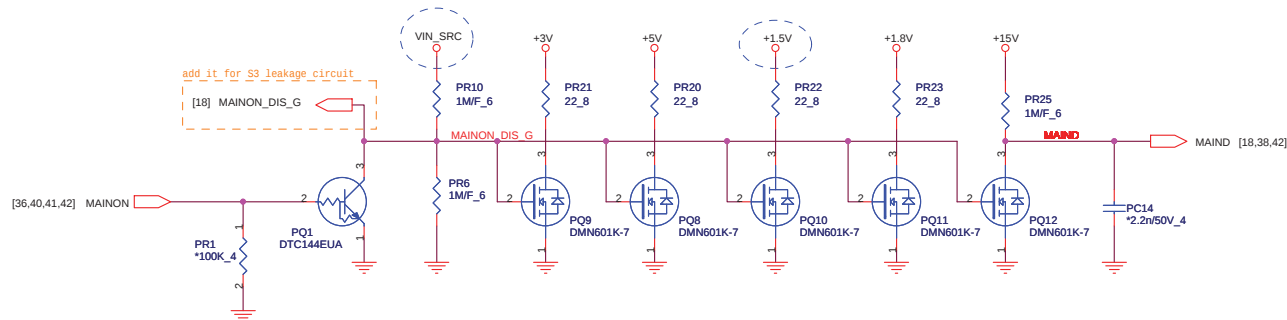
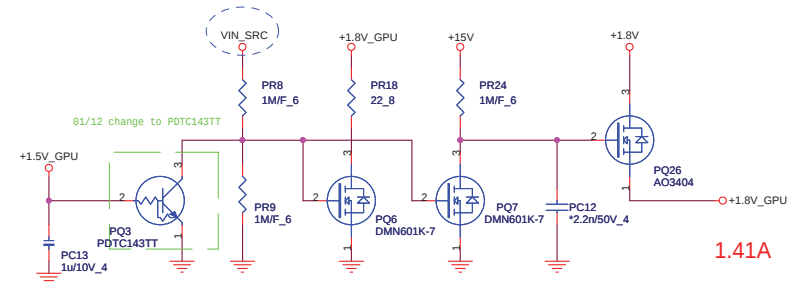
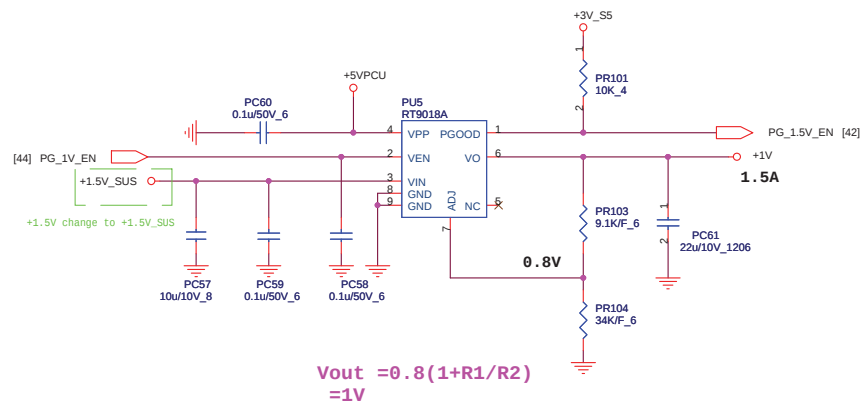
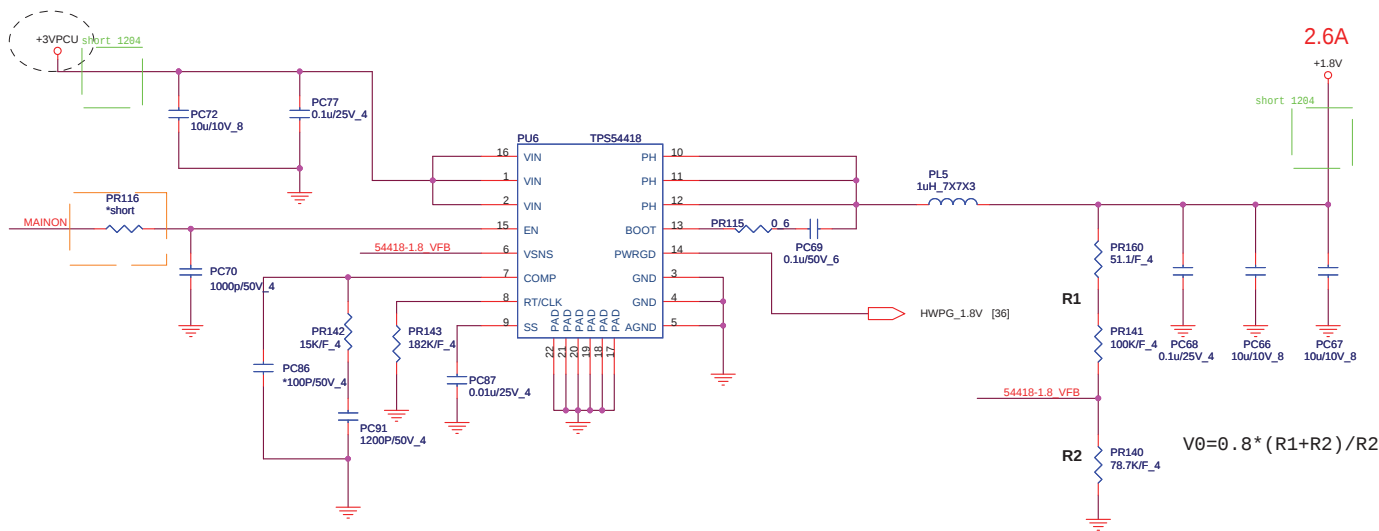
[PWM]

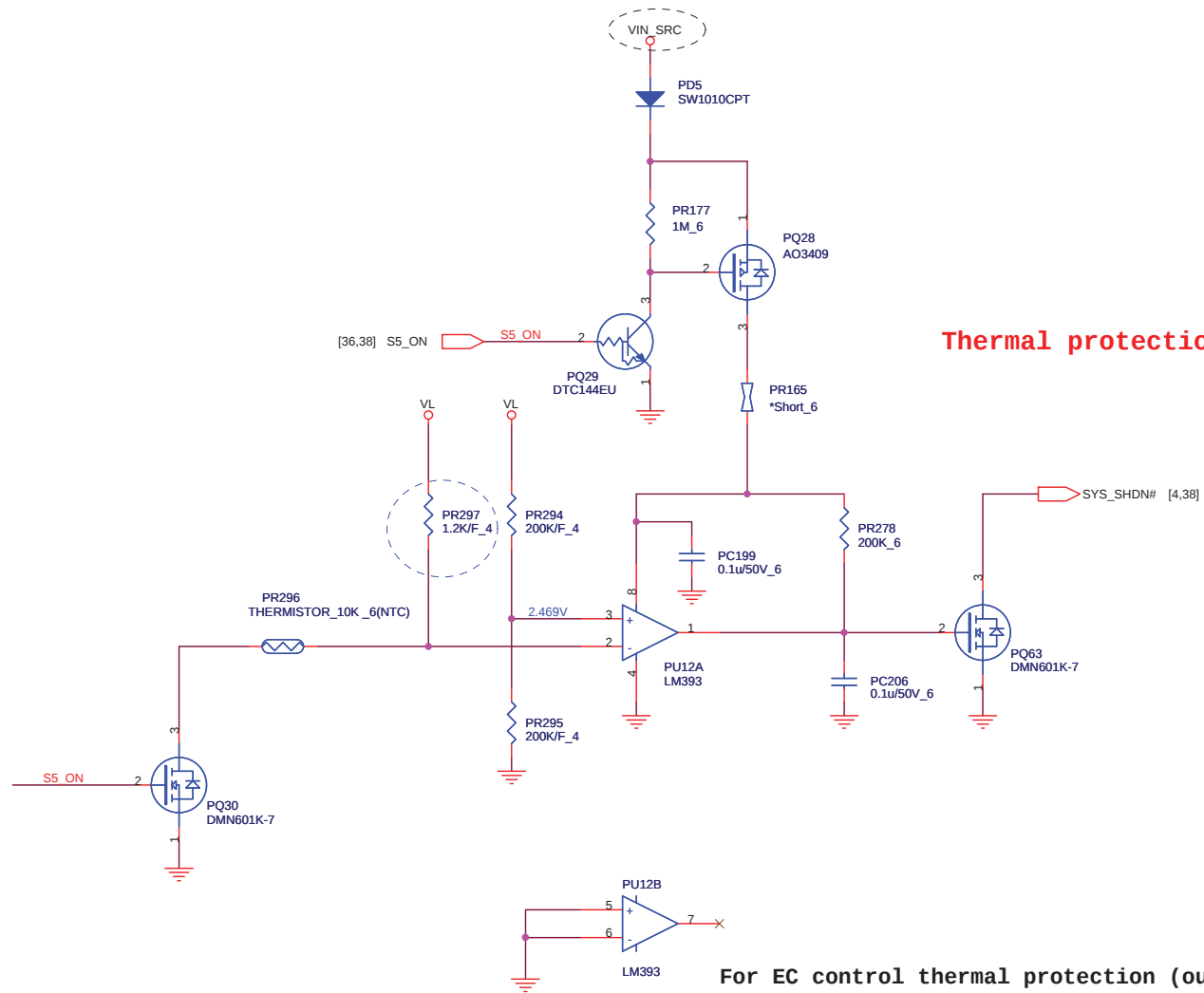


Int_VGA [PWM]

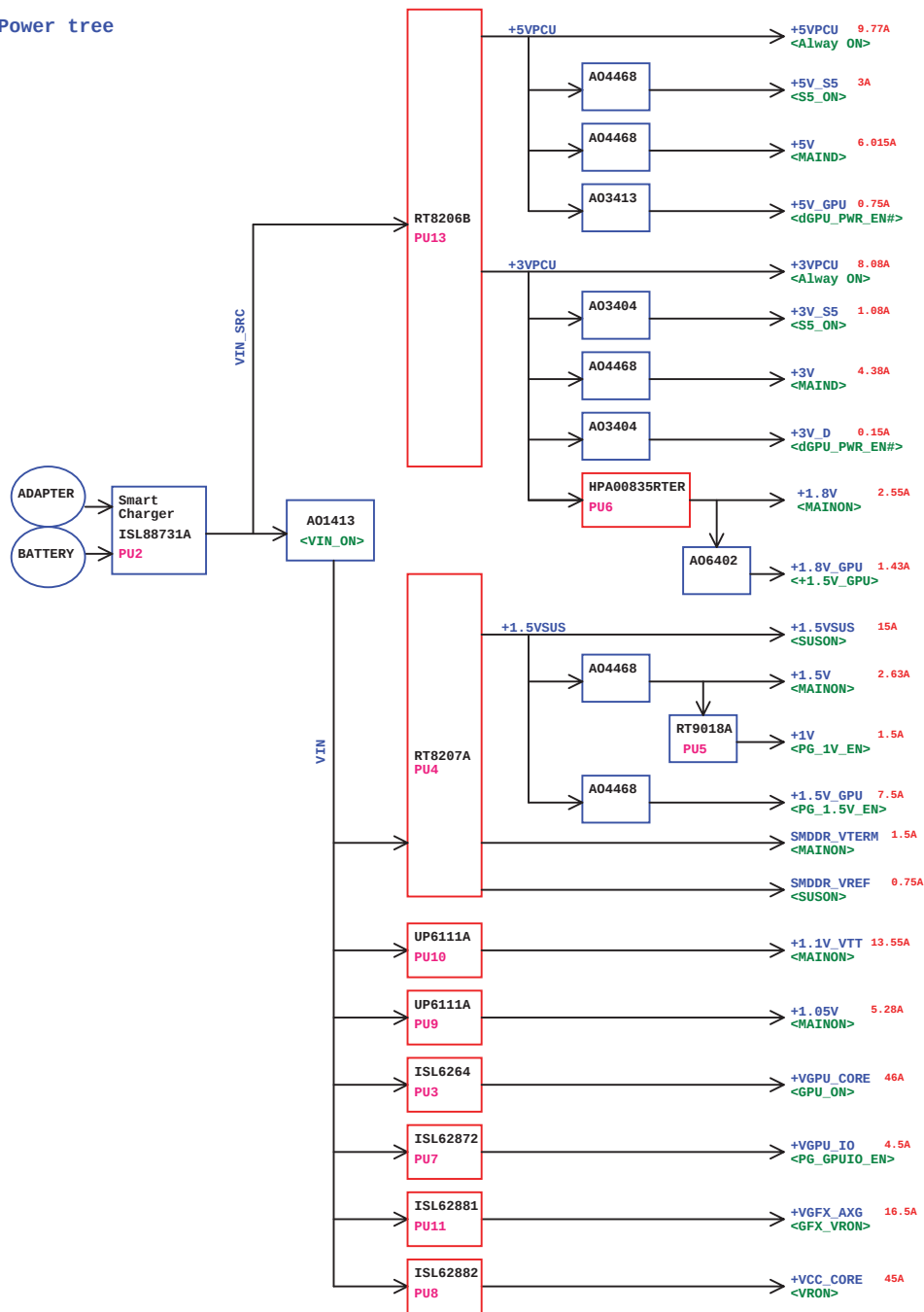


2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.





ZYB Power tree



EC GPIO Setting

Pin Name	Net Name	Setting	Description
GPIO1	ACIN	GPI	EC Detect AC Adapter State
GPIO3	NBSWON#	GPI	Pwr switch in
GPIO4/AD5	DIGVOL_DN	GPI	Digital Volume wheel.
GPIO5/AD4	DIGVOL_UP	GPI	Digital Volume wheel.
GPIO6	LID3#	GPI	Reserved for Lid function
GPIO7	SUSB#	GPI	S.B sleep S3 pin
GPIO10/LPCPD#	ARCADE_KEY	GPI	Arcade Button switch
GPIO11/CLKRUN#	CLKRUN#	O	Clock Run
GPIO12/PSDAT3	CR_CPPE#SD	GPI	OZ888 Wake indicator
GPIO13/C_PWM	PWRLED#	O	Power on LED drive
GPIO14/TB1	FANSIG	GPI	To detect FAN speed
GPIO15/A_PWM	CONTRAST	O	EC PWM for Panel Brightness
GPIO16/CIRTX	HWPG	GPI	
GPIO17/SC11	MBCLK	O	SMBus Clock for M/B
GPIO18/TACH2	SUSON	GPO	S3 Power Panel
GPIO21/B_PWM	NUMLED#	O	Number Lock LED drive
GPIO22/SDA1	MBDATA	I/O	SMBus Data for M/B
GPIO23/SC13	VGA_CLK	O	SMBus Clock for acer ID flash
GPIO24/LDRQ#	EC_FPBAC#	GPO	Panel back light control
GPIO25/PSCLK3	MAINON	GPO	Turn On/Off main power
GPIO26/PSCLK2	PCH_ACIN	GPI	Power on LED drive
GPIO27/PSDA2	BT_POWERON#	GPO	Turn On/Off bluetooth power
GPIO30/CIRTX2	ACPRN	GPI	
GPIO31/SDA3	VGA_DATA	I/O	SMBus Data for acer ID flash
GPIO32/D_PWM	BATLED#	GPO	Battery status LED drive
GPIO33/H_PWM	BATLED#	GPO	Battery status LED drive
GPIO34/CIRRX1	CIR_R_X2	GPI	CIR signal
GPIO35/PSDAT1	TPDATA	O	PS/2 data for touch pad
GPIO36/TB3	VRON	GPO	Turn On/Off CPU Power
GPIO37/PSCLK1	TPCLK	O	PS/2 clock for touch pad
GPIO40/F_PWM	SUSLED	GPO	S3 state LED drive
GPIO42/TCCK	No used	GPI	No used
GPIO43/TMS	AMP_MUTE#	GPO	Turn On/Off Audio Amplifier
GPIO44/TDI	No used	GPI	No used
GPIO45/E_PWM	CPUFAN#	O	EC PWM for Fan Module
GPIO46/cirrxm/trst#	No used	GPI	No used
GPIO47/SC14	VIN_ON	GPI	Turn On/Off VIN_SRC Power plane
GPIO58/TDO	D/C#	GPO	Battery charge / discharge control
GPIO51/TA3	S5_ON	GPO	Turn On/Off S5 Power plane
GPIO52/cirtx2/trdy#	HDMI_HPD_EC#	GPI	EC Detect HDMI State
GPIO53/SDA4	No used	O	No used
GPIO54/E_CSC#	SIO_EXT_SC1#	GPI	EC SCI
GPIO55/CLKOUT	ECDB_CLOCK	GPI	EC core clock
GPIO56/TA1	No used	GPI	No used
GPIO57/KBSOUT17	MY17	O	Keyboard scan output
GPIO60/KBSOUT16	MY16	O	Keyboard scan output
GPIO61/KBSOUT15	MY15	O	Keyboard scan output
GPIO62/KBSOUT14	MY14	O	Keyboard scan output
GPIO63/KBSOUT13	MY13	O	Keyboard scan output
GPIO64/KBSOUT12	MY12	O	Keyboard scan output
GPIO65/SM1#	SIO_EXT_SM1#	O	EC SMI
GPIO66/G_PWM	CAPSLED#	O	Caps Lock LED drive
GPIO67/PWUREQ	USBON#	GPO	USB power enable/disable
GPIO70/IRRX2_IRSL0	SUSC#	GPI	S.B sleep S4 pin
GPIO71/IRTX/SOUT2	PWR0K_EC	GPO	System Power Good for PC1 Reset
GPIO72/IRRX1/SIN2	ICH_RSMRST#	GPO	S.B Resume Power Reset
GPIO73/SC12	2ND_MBCLK	O	SMBus Clock for CPU thermal
GPIO74/SDA2	2ND_MBDATA	I/O	SMBus Data for CPU thermal
GPIO75/SP1_SCK	BACKUP_SW	GPO	Backup Switch
GPIO76/SP1_DO#SHBM	SHBM_R	GPO	Using SPI flash for BIOS and EC firmware
GPIO77/SP1_D1	No used	GPI	No used
GPIO81	DNBSWON#	GPO	S.B Power button Event
GPO82/TRIS	No used	GPI	No used
GPO83/SOUT_CR/BADDR1	PWRSAVE_LED#	GPI	Power Save LED
GPO84/BADDR0	BACKUP_LED#	GPI	Backup LED
GPIO87/CIRRRXM/SIN_CR	RE_EN	GPO	Mini card 1 (WLAN) enable/disable
GP190/AD0	TEMP_MBAT	I	EC detect battery state
GP191/AD1	WL_SW	GPI	Wireless Switch
GP192/AD2	SML1ALERT#	GPI	Touchpad temperature / PCH thermal Hot
GP193/AD3	ICMNT	I	EC detect system current in AC mode
GP194/DA0	PWRSAVE_SW	GPI	Power Save (Battery) Button Switch
GP195/DA1	No used	GPI	No used
GP196/DA2	No used	GPI	No used
GP197/DA3	No used	GPI	No used

PCH GPIO Setting

Pin Name	Power	PCH Default	Net Name	Description	Setting	Internal PU/PD	External PU/PD
GPIO0 / BMBUSY#	Core	GPI	BMBUSY#	No used	GPO		PU 8.2KΩ to +3V
GPIO1 / TACH1	Core	GPI	SIO_EXT_SM1#	EC SMI	GPI		PU 10KΩ to +3V
GPIO2 / PIRQE#	Core	GPI	PCI_PIRQE#	No used	GPO		PU 8.2KΩ to +3V
GPIO3 / PIRQ#	Core	GPI	PCI_PIRQ#	No used	GPI		PU 8.2KΩ to +3V
GPIO4 / PIRQG	Core	GPI	PCI_PIRQG#	No used	GPO		PU 8.2KΩ to +3V
GPIO5 / PIRQH#	Core	GPI	PCI_PIRQH#	No used	GPO		PU 8.2KΩ to +3V
GPIO6 / TACH2	Core	GPI	SIO_EXT_SC1#	EC SCI Interrupt	GPI		PU 10KΩ to +3V
GPIO7 / TACH3	Core	GPI	BOARD_ID0	M/B ID Setting	GPI		PD 10K to GND & PU to +3V
GPIO8	S5	GPO	RSV_GPIO8	No used	GPO		PU 10KΩ to +3V S5
GPIO9 / OC5#	S5	Native	USB_OC5#	No used	Native		PU 8.2KΩ to +3V S5
GPIO10 / OC6#	S5	Native	USB_OC6#	No used	Native		PU 8.2KΩ to +3V S5
GPIO11 / SMBALERT#	S5	Native	RSV_SMBALERT#	No used	GPO		PU 10KΩ to +3V S5
GPIO12 / LAN_PHY_PWR_CTRL	S5	Native	LAN_DISABLE#	No used	GPI		PU 10KΩ to +3V S5
GPIO13 / HDA_DOCK_RST#	S5	GPI	PCH_GPIO13	No used	GPI		RV PU 10KΩ to +3V S5
GPIO14 / OC7#	S5	Native	USB_OC7#	No used	Native		PU 8.2KΩ to +3V S5
GPIO15	S5	GPO	CR_WAKE#	No used	GPO	PU 20KΩ	PU 1KΩ to +3V S5
GPIO16 / SATA4GP	Core	GPI	dGPU_HOLD_RST#	GPU Reset	GPO		PD 100K to G RV PU 10K to +3V
GPIO17 / TACH0	Core	GPI	dGPU_PWR0K	GPU Power OK	GPI		PU 10KΩ to +3V
GPIO18 / PCIECLKRQ1#	Core	Native	CLK_PCIE_REQ1#_R	No used	GPO		PU 10KΩ to +3V
GPIO19 / SATA1GP	Core	GPI	No used	No used	GPO		PU 10KΩ to +3V
GPIO20 / PCIECLKRQ2#	Core	Native	CLK_PCIE_REQ2#	Clock Request for PCIE Clocks	Native		PU 10KΩ to +3V
GPIO21 / SATA8GP	Core	GPI	No used	No used	GPO		PU 10KΩ to +3V
GPIO22 / SCLK0C	Core	GPI	GPIO22	No used	GPO		PU 10KΩ to +3V
GPIO23 / LDRQ1#	Core	Native	No used	No used	GPO		
GPIO24	S5	GPO	No used	No used	GPO		
GPIO25 / PCIECLKRQ3#	S5	Native	CLK_PCIE_REQ3#_R	Clock Request for PCIE Clocks	Native		PU 10KΩ to +3V S5
GPIO26 / PCIECLKRQ4#	S5	Native	CLK_PCIE_REQ4#_R	Clock Request for PCIE Clocks	Native		PU 10KΩ to +3V S5
GPIO27	S5	GPO	No used	No used	GPO		
GPIO28	S5	GPI	TP_PCH_GPIO28	No used	GPO		PU 10KΩ to +3V S5
GPIO29 / SLP_LAN#	S5	GPI	PM_SLP_LAN#	No used	GPO		RV PU 10KΩ to +3V S5
GPIO30 / SUS_PWR_DN_ACK	S5	GPI	SUS_PWR_ACK_R	No used	GPO		PU 10KΩ to +3V S5
GPIO31 / ACPI_PWENT	S5	GPI	ACIN_R	No used	GPI		PU 8.2KΩ to +3V S5
GPIO32 / CLKRUN#	Core	GPO / Native	CLKRUN#	PCI Clock Run	Native		PU 8.2KΩ to +3V
GPIO33 / HDA_DOCK_EN#	Core	GPO	HDA_DOCK_EN#	No used	GPO	PU 20KΩ	RV PU 10K to +3V & 1K to GND
GPIO34 / STP_PCI#	Core	GPI	STP_PCI#	No used	GPO		PU 10KΩ to +3V
GPIO35 / SATA1_KREQ#	Core	GPO	dGPU_VRON	GPU Voltage Regulator Enable	GPI		
GPIO36 / SATA2GP	Core	GPI	dGPU_PWR_EN#	GPU Power Enable	GPO		PU 10KΩ to +3V
GPIO37 / SATA3GP	Core	GPI	dGPU_PRSNT#	No used	GPI		PD 10KΩ to GND
GPIO38 / SLOAD	Core	GPI	GPIO38	No used	GPO		PU 10KΩ to +3V
GPIO39 / SDATAOUT0	Core	GPI	SAVE_LED#	No used	GPO		PU 10KΩ to +3V
GPIO40 / OC1#	S5	Native	USB_OC1#	No used	Native		PU 8.2KΩ to +3V S5
GPIO41 / OC2#	S5	Native	USB_OC2#	No used	Native		PU 8.2KΩ to +3V S5
GPIO42 / OC3#	S5	Native	USB_OC3#	No used	Native		PU 8.2KΩ to +3V S5
GPIO43 / OC4#	S5	Native	USB_OC4#	No used	Native		PU 8.2KΩ to +3V S5
GPIO44 / PCIECLKRQ5#	S5	Native	CLK_PCIE_REQ5#	No used	Native		PU 10KΩ to +3V S5
GPIO45	S5	Native	GPIO45	No used	GPO		PU 10KΩ to +3V S5
GPIO46 / PCIECLKRQ6#	S5	Native	RST_GATE#	S3 Power Reduction	GPO		PU 10KΩ to +3V S5
GPIO47 / PEG_A_CLKRQ#	S5	Native	PEG_CLKREQ#_R	Clock Request Signals for PEG	Native		PD 10KΩ to GND
GPIO48 / SDATAOUT1	Core	GPI	SV_SET_UP	No used	GPO		PU 10KΩ to +3V
GPIO49 / SATA5GP	Core	GPI	SATA5GP	CPU alert for EC	GPO		PU 10KΩ to +3V
GPIO50 / REQ1#	Core	Native	PCI_REQ1#	No used	GPO		PU 8.2KΩ to +3V
GPIO51 / GNT1#	Core	Native	PCI_GNT1#	Boot BIOS Selection	Native		PD 1K to GND RV PU 1K to +3V
GPIO52 / REQ2#	Core	Native	dGPU_SELECT#	GPU Output Select	GPO		PU 10KΩ to +3V
GPIO53 / GNT2#	Core	Native	PWM_SELECT#	LVDS_BRIGHT Select	GPO		
GPIO54 / REQ3#	Core	Native	PCI_REQ3#	No used	GPO		PU 8.2KΩ to +3V
GPIO55 / GNT3#	Core	Native	PCI_GNT3#	No used	Native		PU 8.2KΩ to +3V
GPIO56 / PEG_B_CLKRQ#	S5	Native	CLK_PCIE_LAN_REQ#	Clock Request Signals for PEG	Native		PU 10KΩ to +3V S5
GPIO57	S5	GPI	GPIO57	No used	GPI		PD 10KΩ to GND
GPIO58 / SML1CLK	S5	Native	SMB_CLK_ME1	SMBus Clock for EC	Native		PU 2.2KΩ to +3V S5
GPIO59 / OC0#	S5	Native	USB_OC0#	No used	Native		PU 8.2KΩ to +3V S5
GPIO60 / SML1ALERT#	S5	Native	RSV_SML1ALERT#	No used	Native		PU 10KΩ to +3V S5
GPIO61 / SUS_STAT#	S5	Native	SUS_STAT#	No used	GPO		
GPIO62 / SUSCLK	S5	Native	ICH_SUSCLK	Suspend Clock	Native		
GPIO63 / SLP_S5#	S5	Native	SLP_S5#_R	No used	GPO		
GPIO64 / CLKOUTFLEX0	Core	Native	CLK_FLEX0	No used	GPO		
GPIO65 / CLKOUTFLEX1	Core	Native	CLK_FLEX1	No used	GPO		
GPIO66 / CLKOUTFLEX2	Core	Native	CLK_FLEX2	No used	GPO		
GPIO67 / CLKOUTFLEX3	Core	Native	dGPU_EDIDSEL#	GPU EDID Select	GPO		PU 10KΩ to +3V
GPIO72 / BATLOW#	S5	Native	PM_BATLOW#	No used	GPO		PU 8.2KΩ to +3V S5
GPIO73 / PCIECLKRQ0#	S5	Native	CLK_PCIE_REQ0#	No used	GPO		PU 10KΩ to +3V S5
GPIO74 / SML1ALERT#	S5	Native	RSV_SML1ALERT#	No used	GPO		PU 10KΩ to +3V S5
GPIO75 / SMLIDATA	S5	Native	SMB_DATA_ME1	SMBus Data for EC	Native		PU 2.2KΩ to +3V S5

CK595 Clock Setting Table

Pin Name	Pin	Net Name	Description
CPU_0	23	CLK_BUF_BCLK	
CPU_0#	22	CLK_BUF_BCLK#	Differential CPU clock

CK595 PCI Express Clock

Pin Name	Pin	Net Name	Description
DOT96	3	CLK_BUF_DREFCLK	
DOT96#	4	CLK_BUF_DREFCLK#	96MHz DOT clock for PCH
SRC_2	13	CLK_BUF_DREFSSCLK	
SRC_2#	14	CLK_BUF_DREFSSCLK#	Clock output for PCH graphic controller
SRC_USATA	10	CLK_BUF_PCIE_3GPLL	
SRC_1#SATA#	11	CLK_BUF_PCIE_3GPLL#	Differential Serial Reference Clock for PCH

PCH PCI Express Clock

Pin Name	Pin	Net Name	Description
CLKOUT_BCLK0_P	AM3	CLK_CPU_BCLK	
CLKOUT_BCLK0_N	AM1	CLK_CPU_BCLK#	Differential Serial Reference Clock for CPU
CLKOUT_DP_P	AT1	DPLL_REF_SSCLK	
CLKOUT_DP_N	AT3	DPLL_REF_SSCLK#	Differential Serial Reference Clock for CPU
CLKOUT_DMI_P	AN2	CLK_PCIE_3GPLL#	
CLKOUT_DMI_N	AN4	CLK_PCIE_3GPLL#	Differential Serial Reference Clock for CPU
CLKOUT_PEG_A_P	AD43	CLK_PCIE_VGA	
CLKOUT_PEG_A_N	AD45	CLK_PCIE_VGA#	Differential Serial Reference Clock for PCI-Express Graphics device
CLKOUT_PCIE0P	AK47		
CLKOUT_PCIE0N	AK48		No use
CLKOUT_PCIE1P	AM45	CLK_PCH_SCL1	
CLKOUT_PCIE1N	AM43	CLK_PCH_SCL1#	Differential Serial Reference Clock for MINI CARD 2
CLKOUT_PCIE2P	AM48	CLK_PCH_SCL2	
CLKOUT_PCIE2N	AM47	CLK_PCH_SCL2#	Differential Serial Reference Clock for MINI CARD 1
CLKOUT_PCIE3P	AH41	CLK_PCH_SCL3	
CLKOUT_PCIE3N	AH42	CLK_PCH_SCL3#	Differential Serial Reference Clock for OZ888
CLKOUT_PCIE4P	AM53		
CLKOUT_PCIE4N	AM51		No use
CLKOUT_PCIE5P	AJ52		
CLKOUT_PCIE5N	AJ50		No use
CLKOUT_PEG_B_P	AK51	CLK_PCIE_LOM	
CLKOUT_PEG_B_N	AK53	CLK_PCIE_LOM#	Differential Serial Reference Clock for on board LAN

Other Clock

Pin Name	Pin	Net Name	Description
27M_SS	6	27M_CLK	27MHz for GPU
REF	30	CLK_1CH_14M	14.318MHz for PCH

Clock Request Table

CLKREQ#	Control
PEG_A_CLKRQ#	GPU
PCIECLKRQ0#	N/A
PCIECLKRQ1#	MINI2
PCIECLKRQ2#	MINI1
PCIECLKRQ3#	OZ888
PCIECLKRQ4#	N/A
PCIECLKRQ5#	N/A
PEG_B_CLKRQ#	LAN



QUANTA
COMPUTER

Title			Schematic Setting		
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