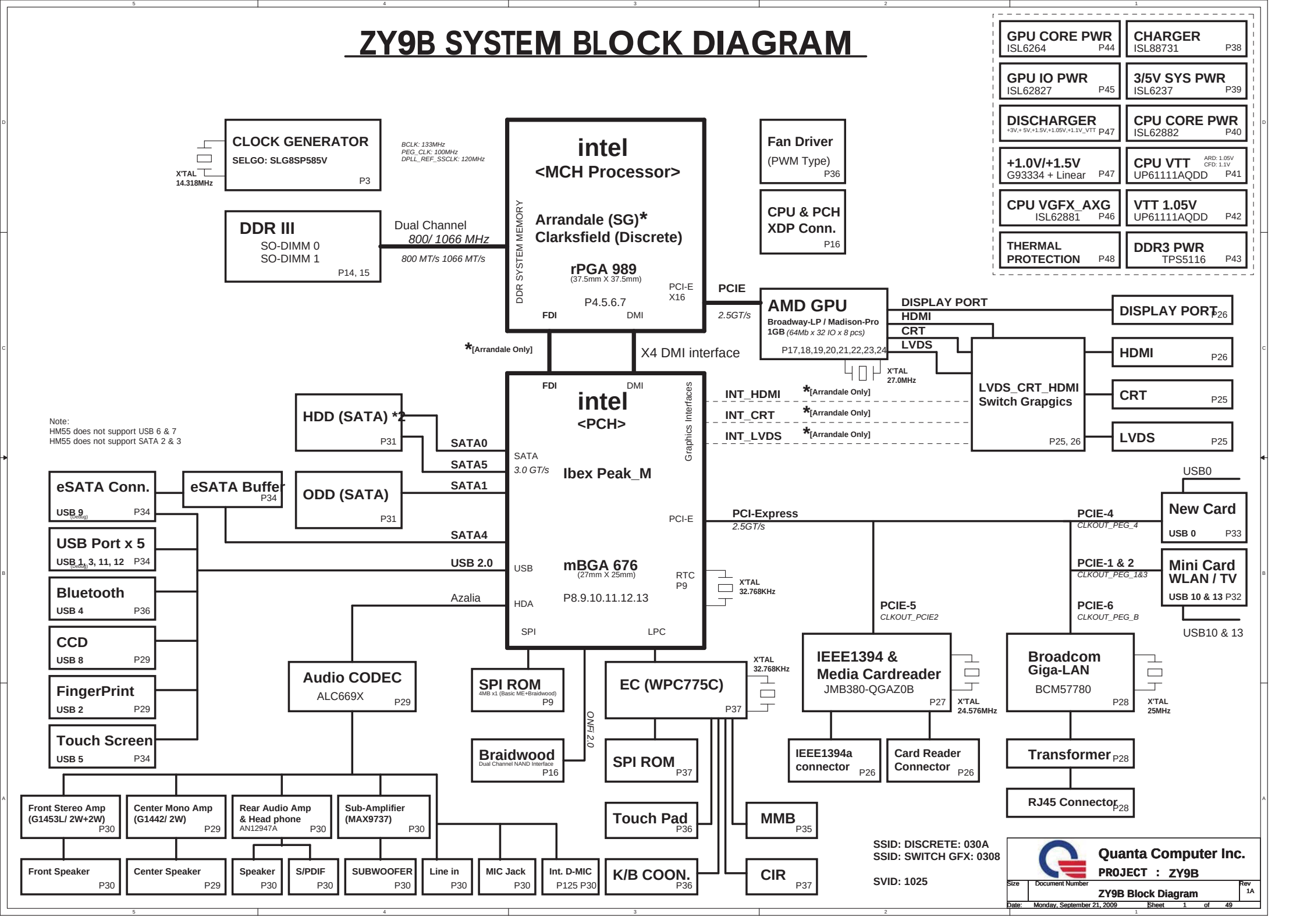
ZY9B SYSTEM BLOCK DIAGRAM



Note:
HM55 does not support USB 6 & 7
HM55 does not support SATA 2 & 3

SSID: DISCRETE: 030A
SSID: SWITCH GFX: 0308

SVID: 1025

Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	ZY9B Block Diagram	1A

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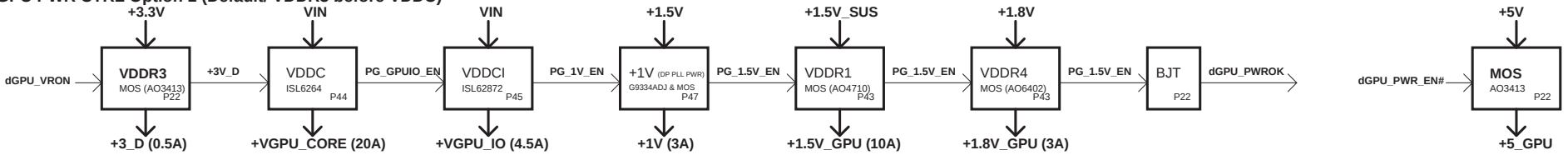
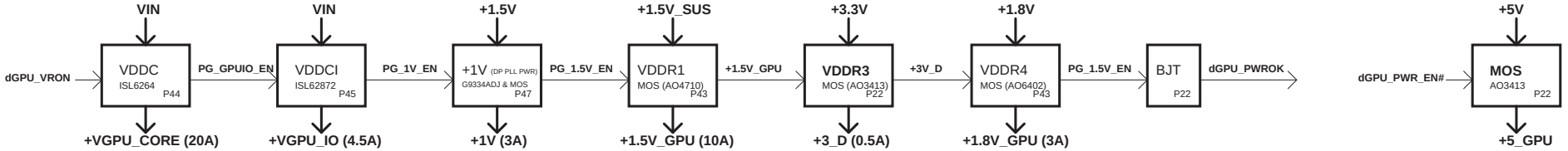
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



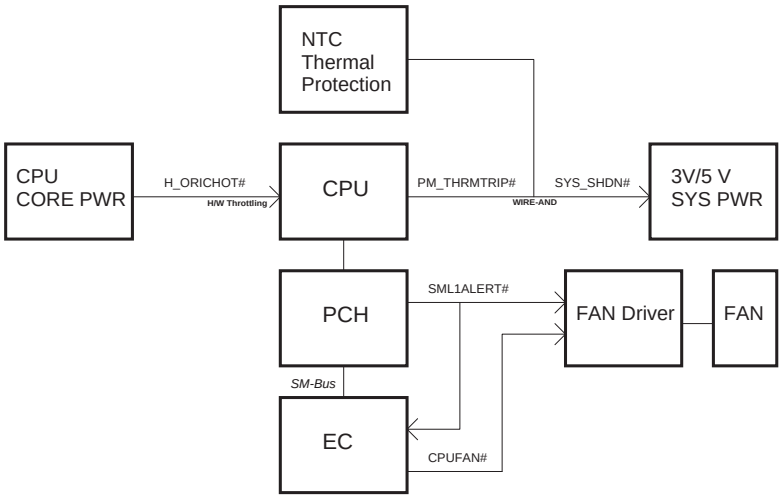
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart

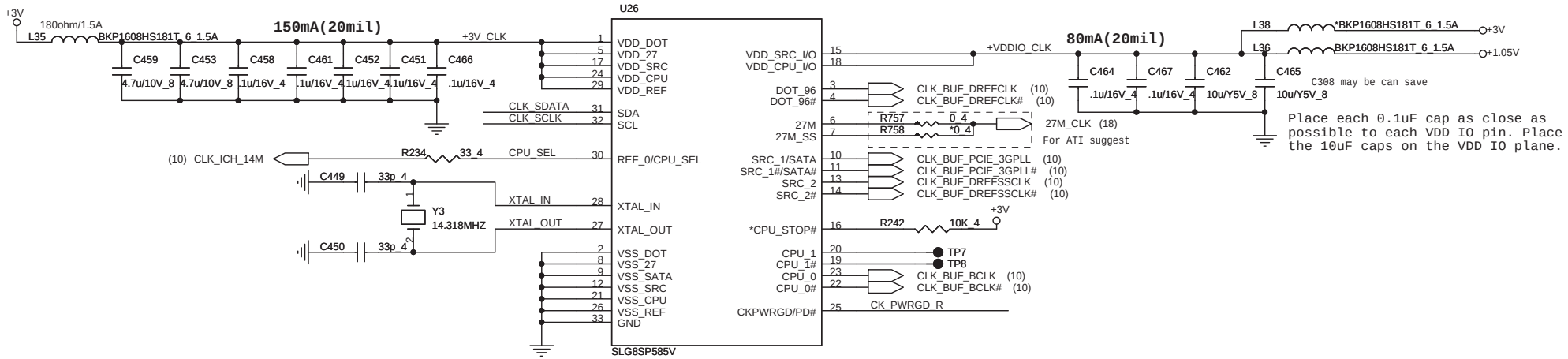


Quanta Computer Inc.

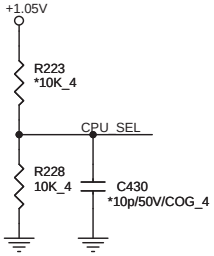
PROJECT : ZY9B

Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

Date: Wednesday, June 24, 2009 Sheet 2 of 49

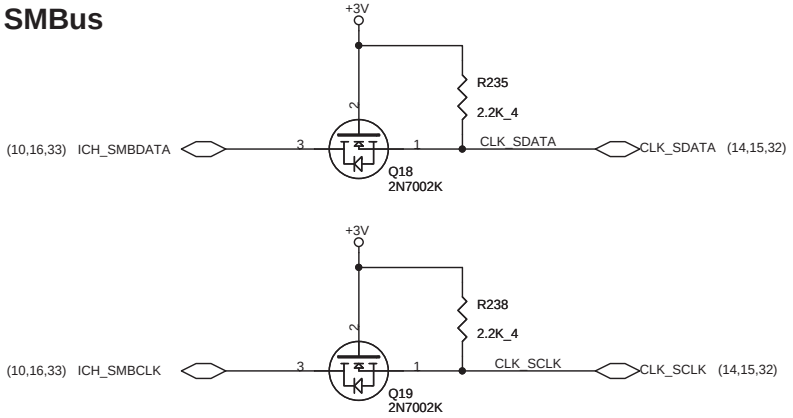


CPU_CLK select

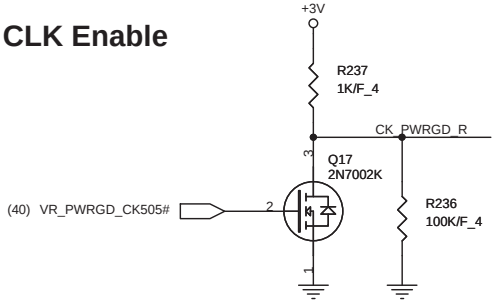


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable

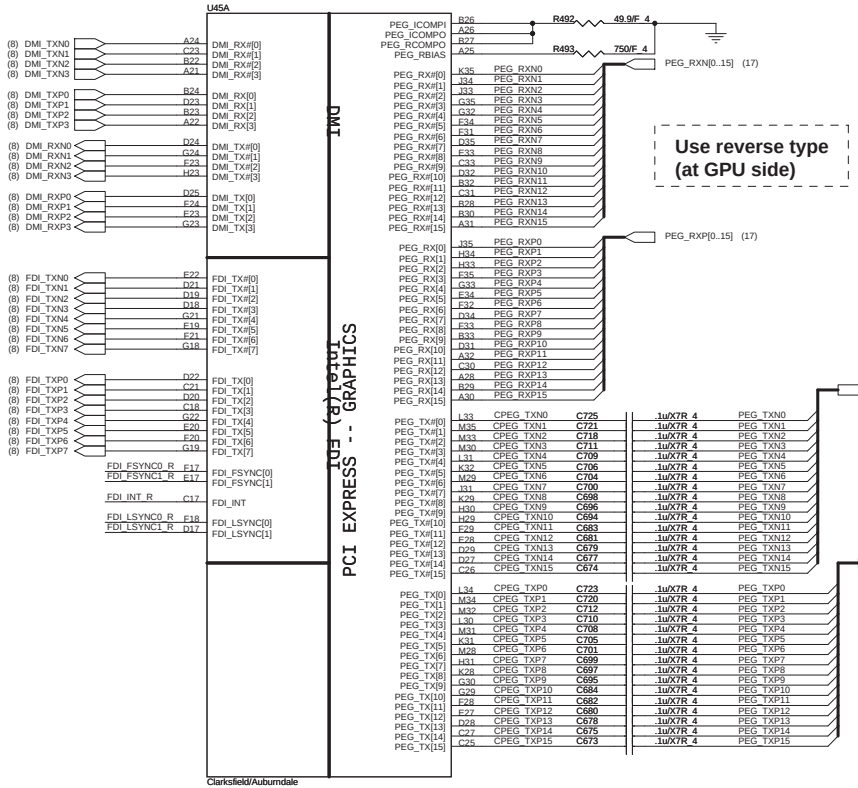


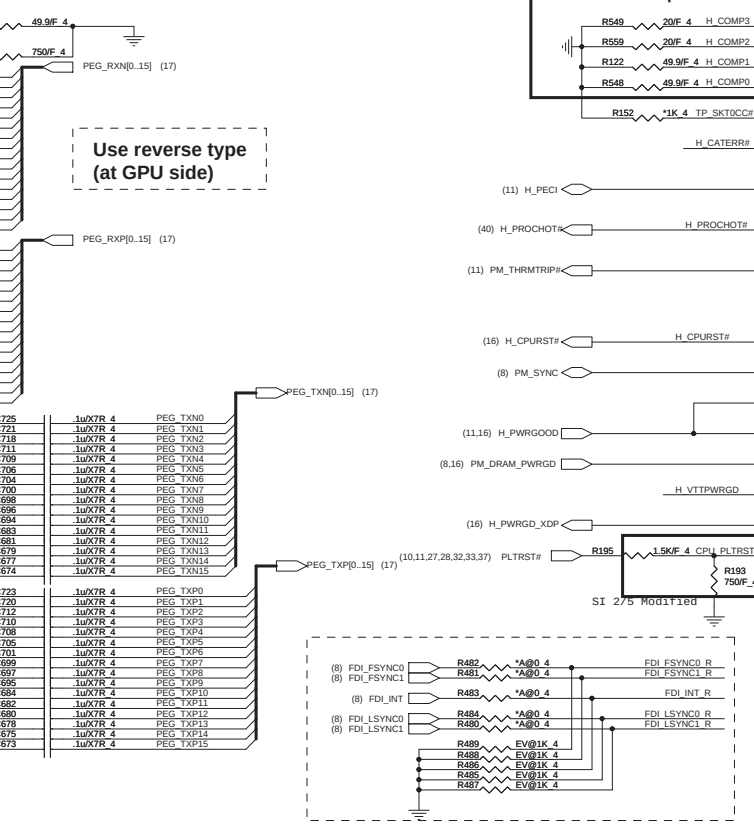
Quanta Computer Inc.

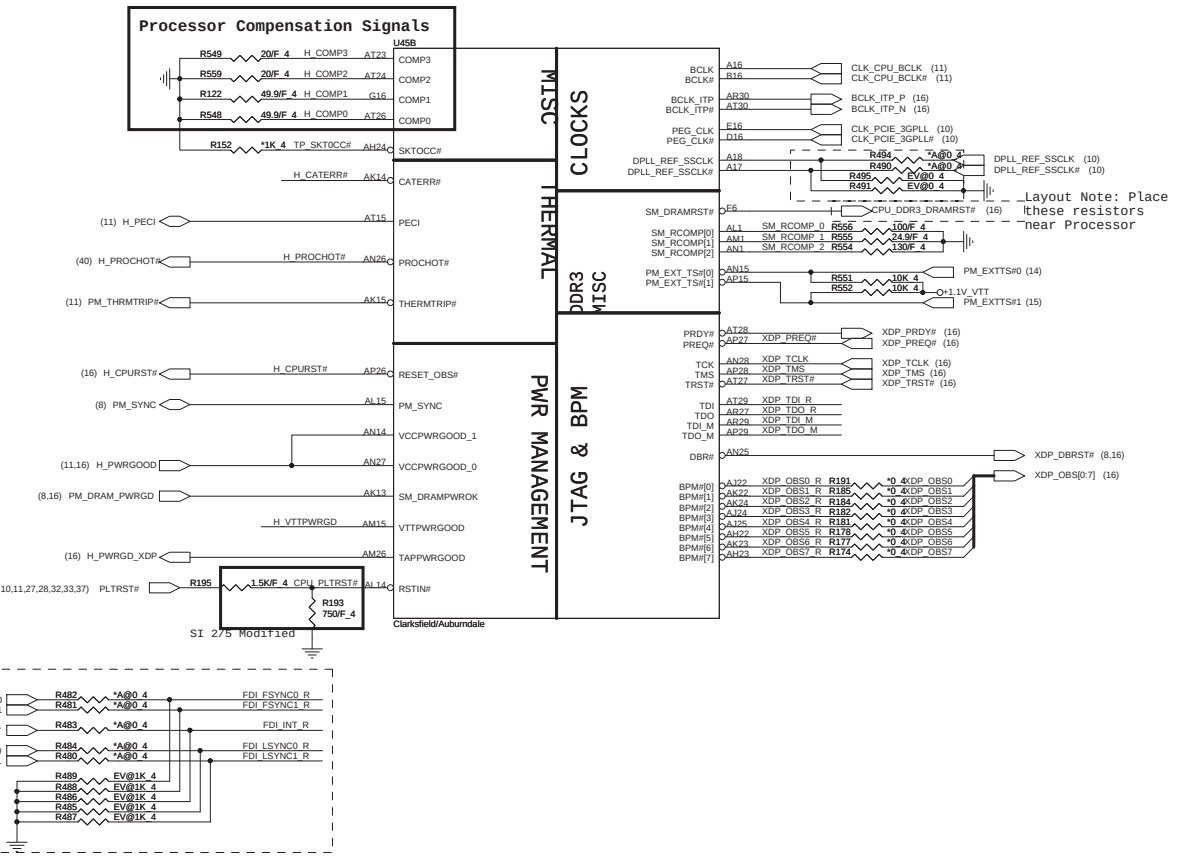
PROJECT : ZY9B

Size	Document Number	Rev
	Clock Generator	1A
Date: Thursday, September 17, 2009	Sheet 3 of 49	

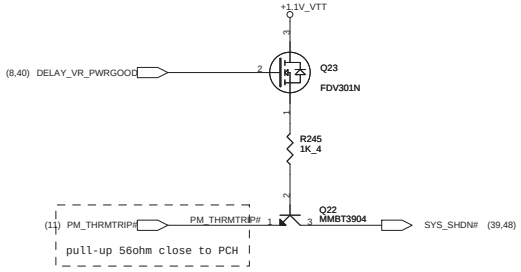
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)



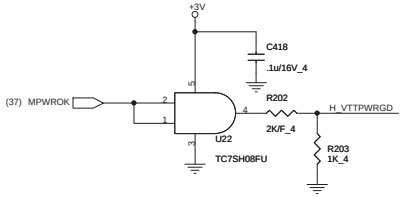




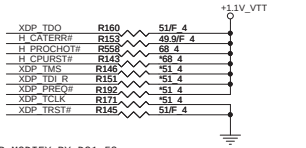
Thermaltrip protect



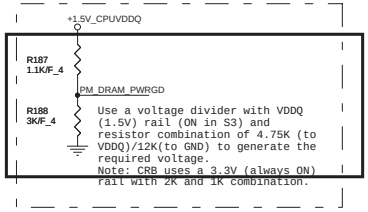
VTT PWR_Good



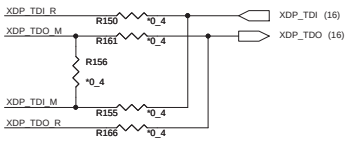
Processor pull-up



4/9 REV:B MODIFY BY DG1.52



JTAG MAPPING



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469

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Size	Document Number	Rev
	AUBURNDA 1/4	1A
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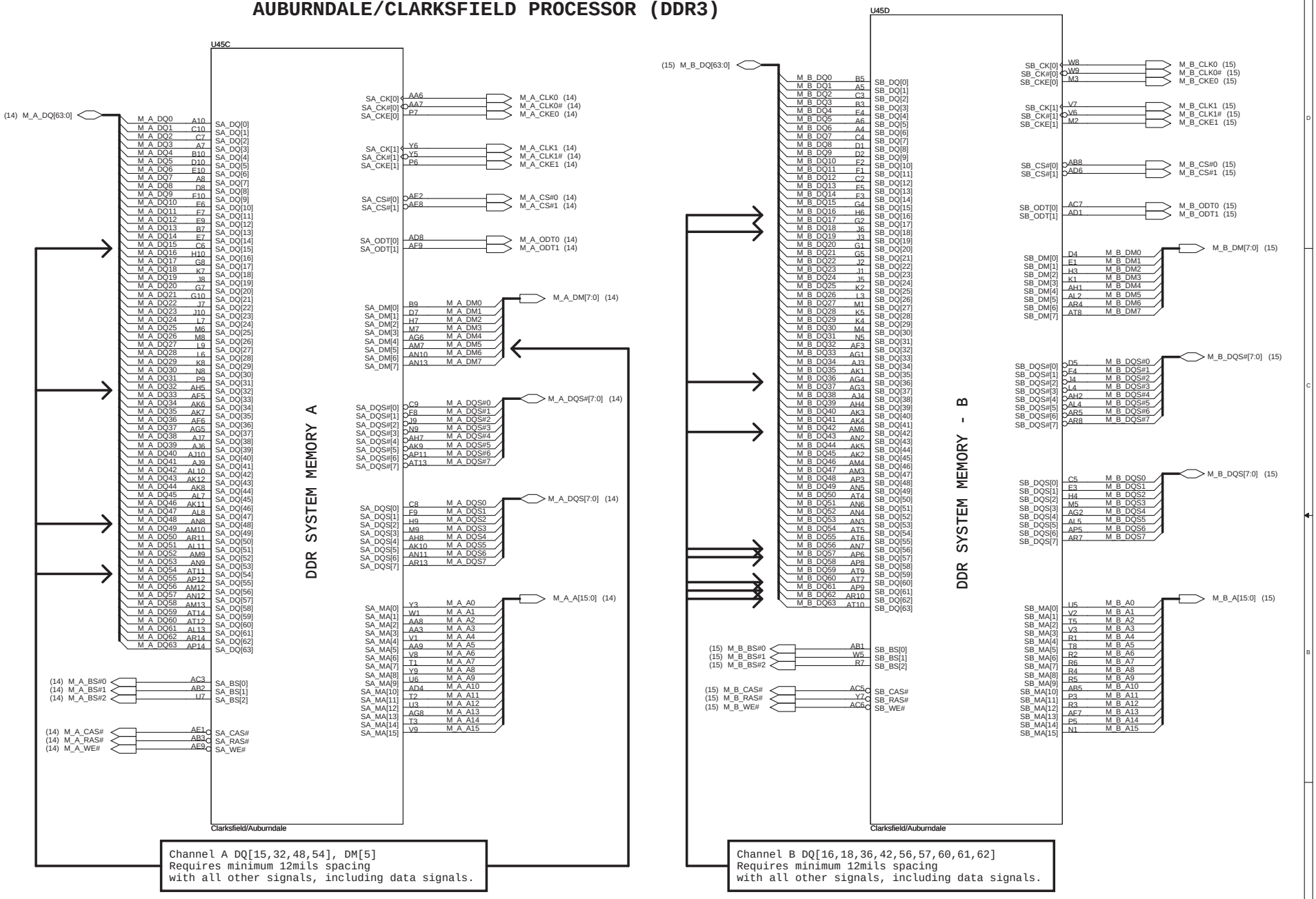
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



Quanta Computer Inc.			
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	AUBURNDA 2/4		1A
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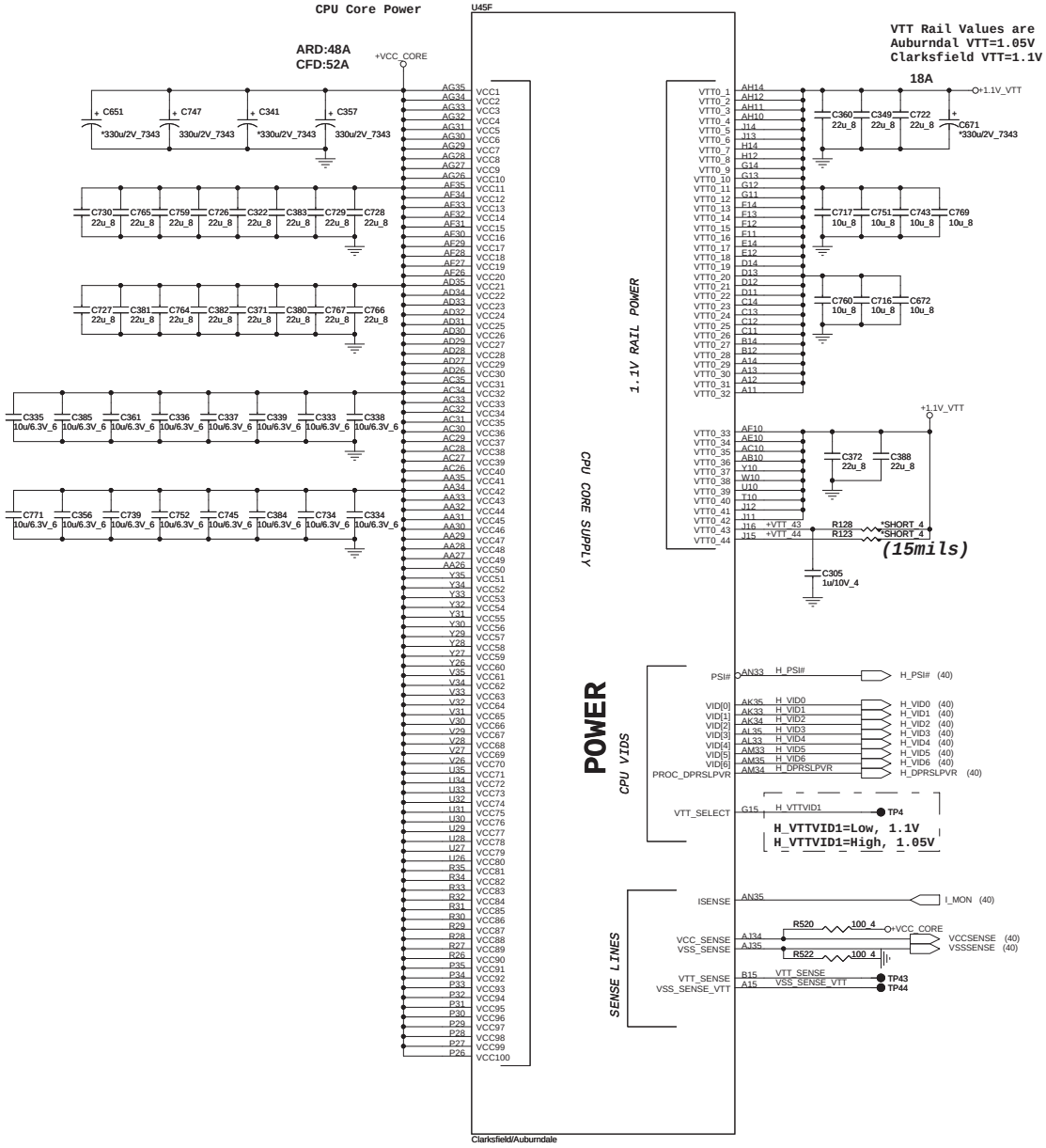
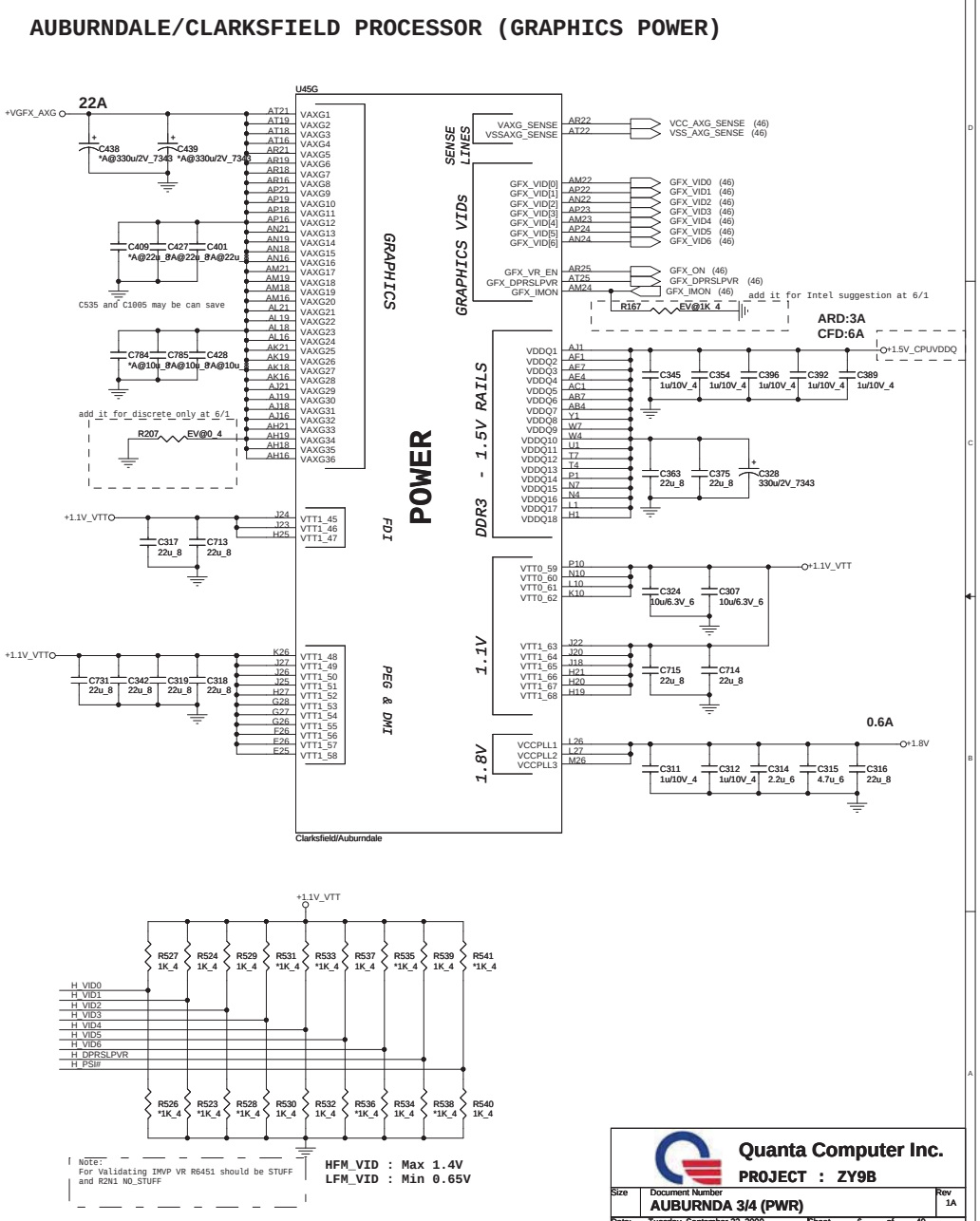
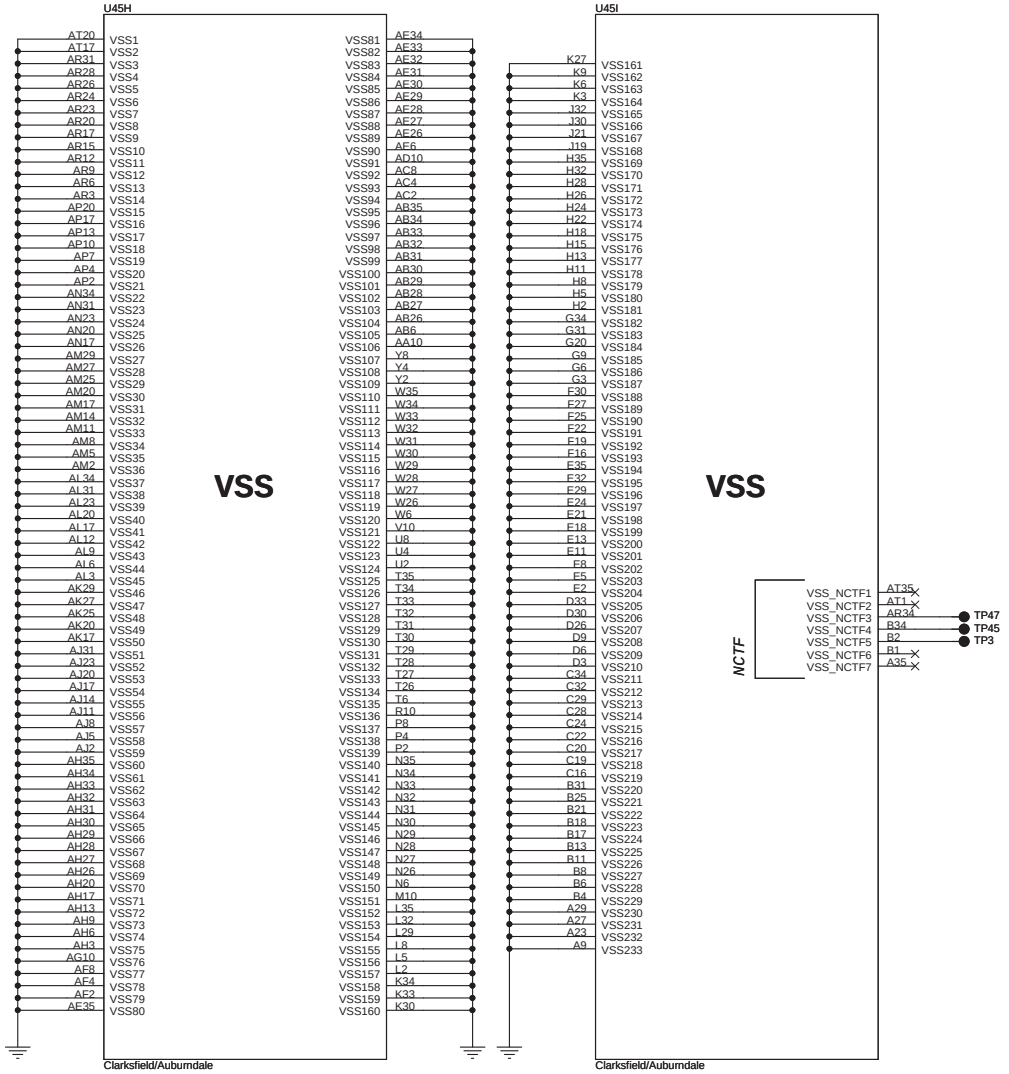


AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

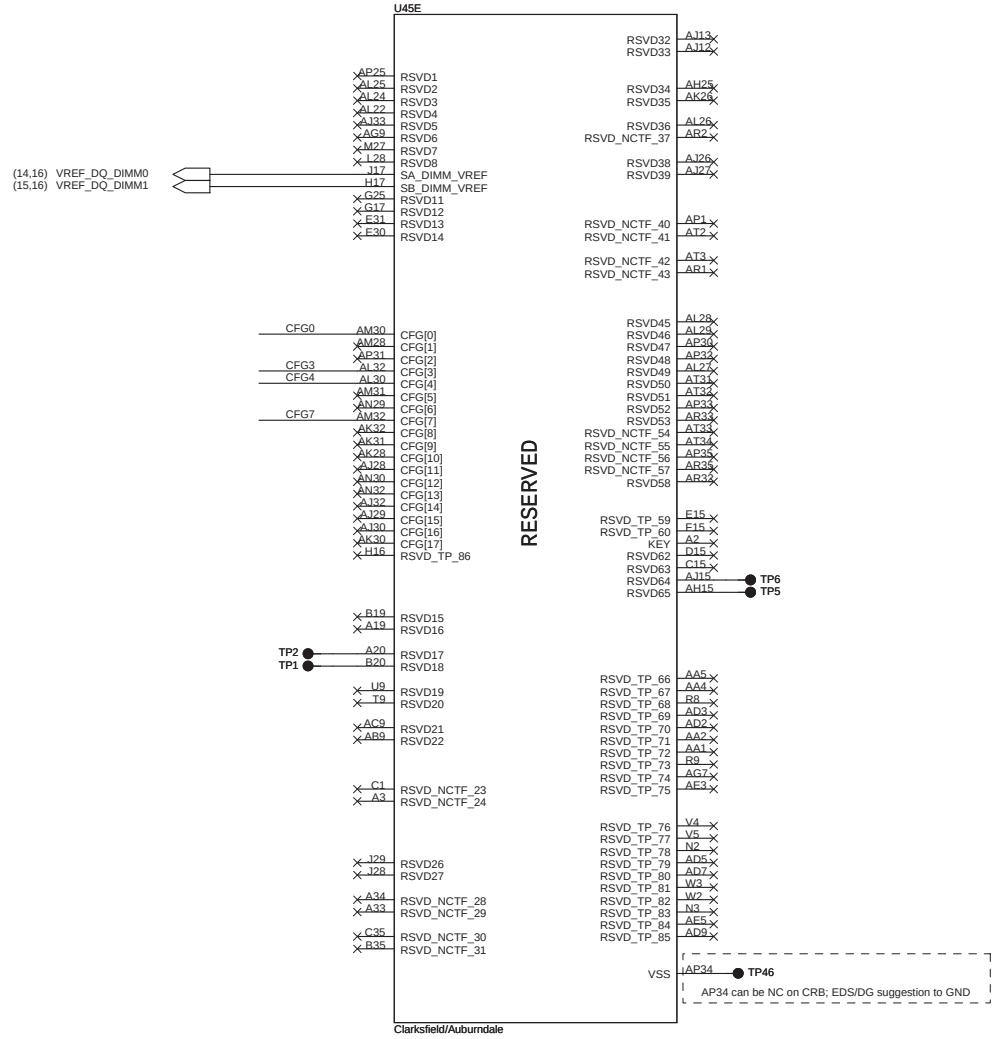


Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number	Rev
	AUBURNDA 3/4 (PWR)	1A
Date: Tuesday, September 22, 2009	Sheet 6 of 49	

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

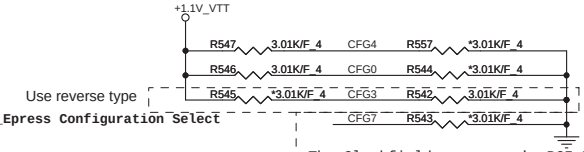


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



Use reverse type

CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

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	AUBURNDA 4/4	1A
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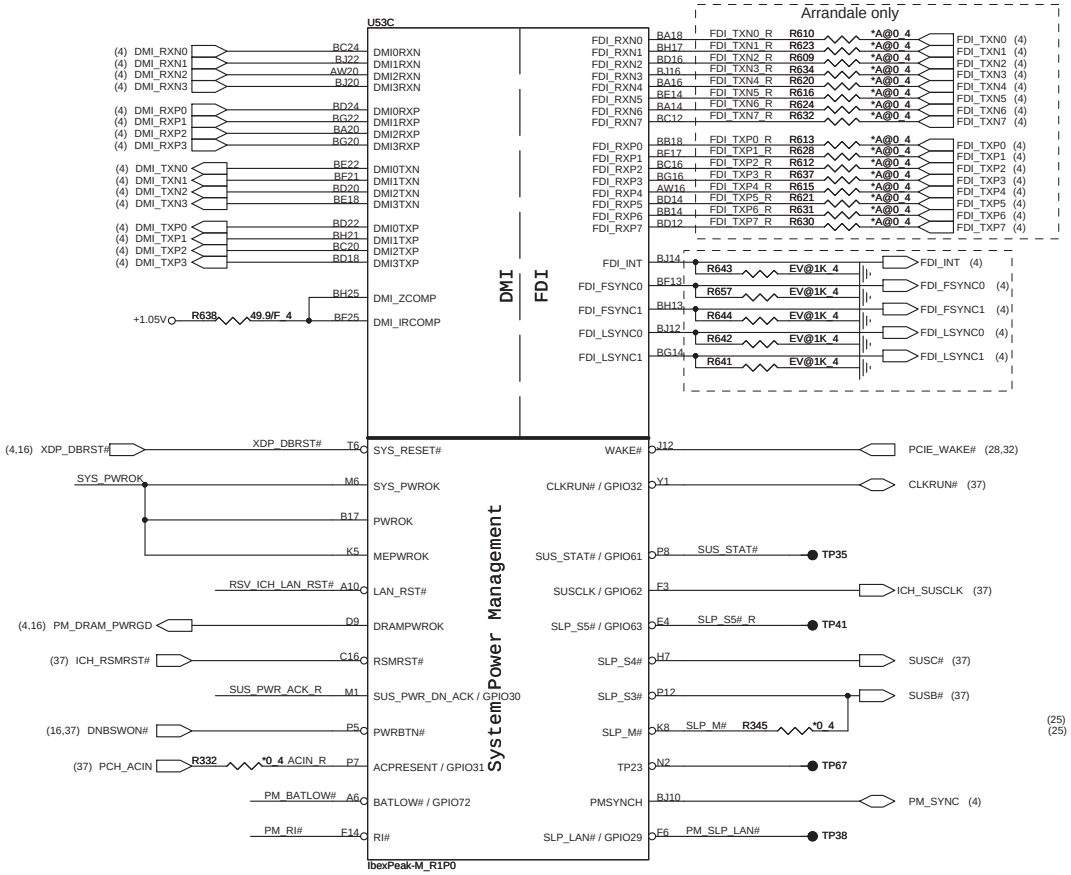
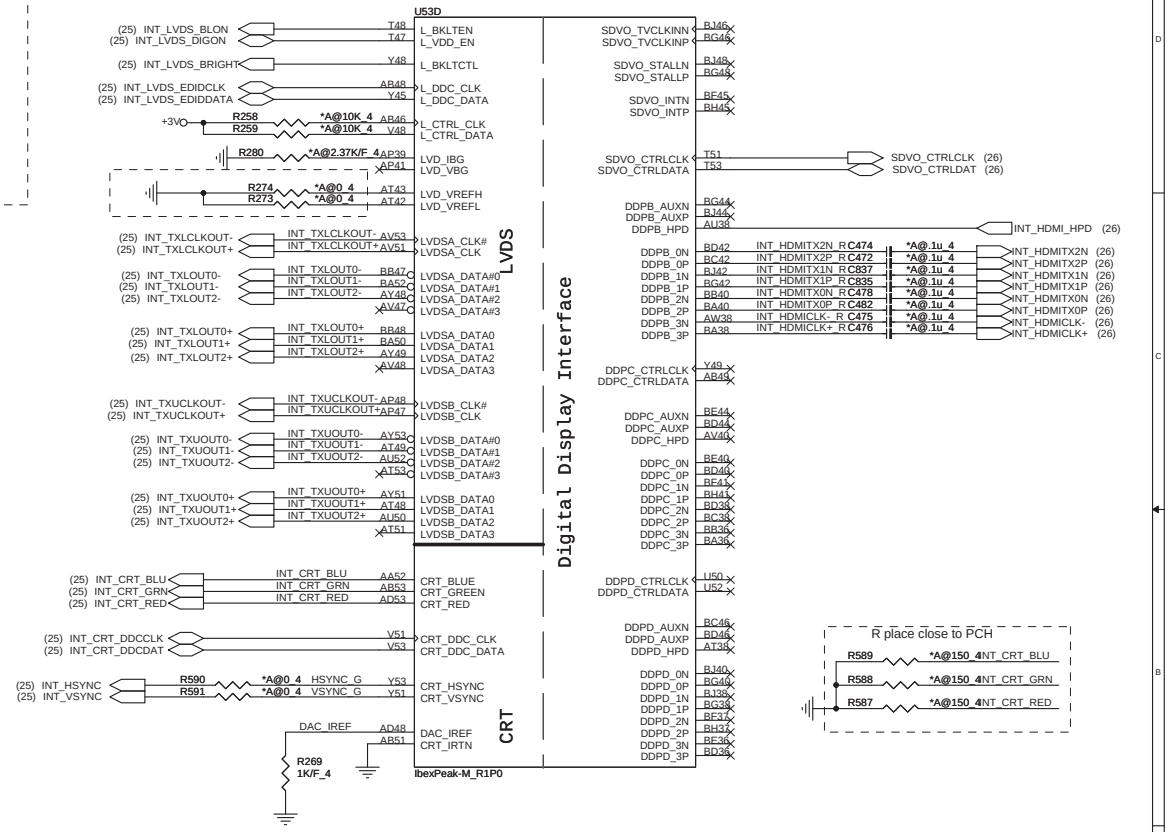
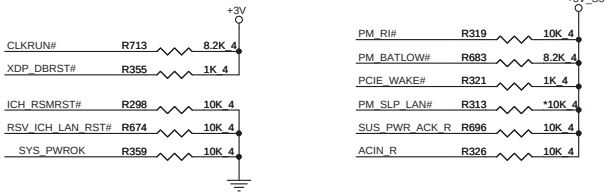
IBEX PEAK-M (DMI,FDI,GPIO)



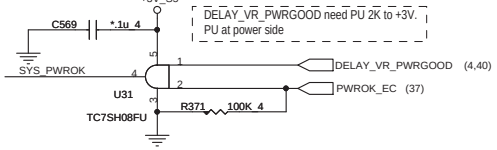
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



Quanta Computer Inc.

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	IBEX PEAK-M 1/6	1A

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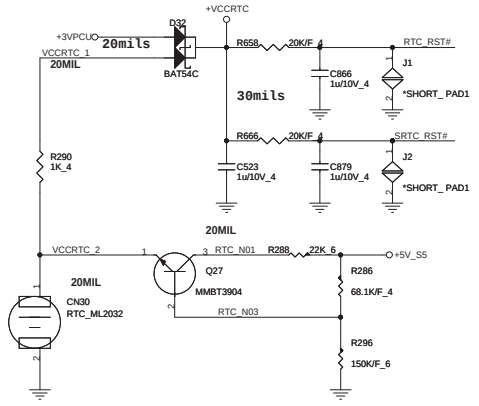
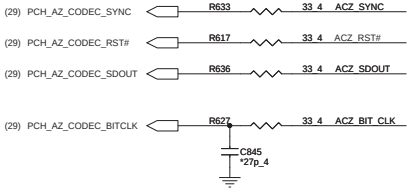
RTC Circuitry

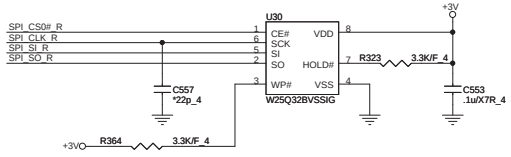


HDA Bus

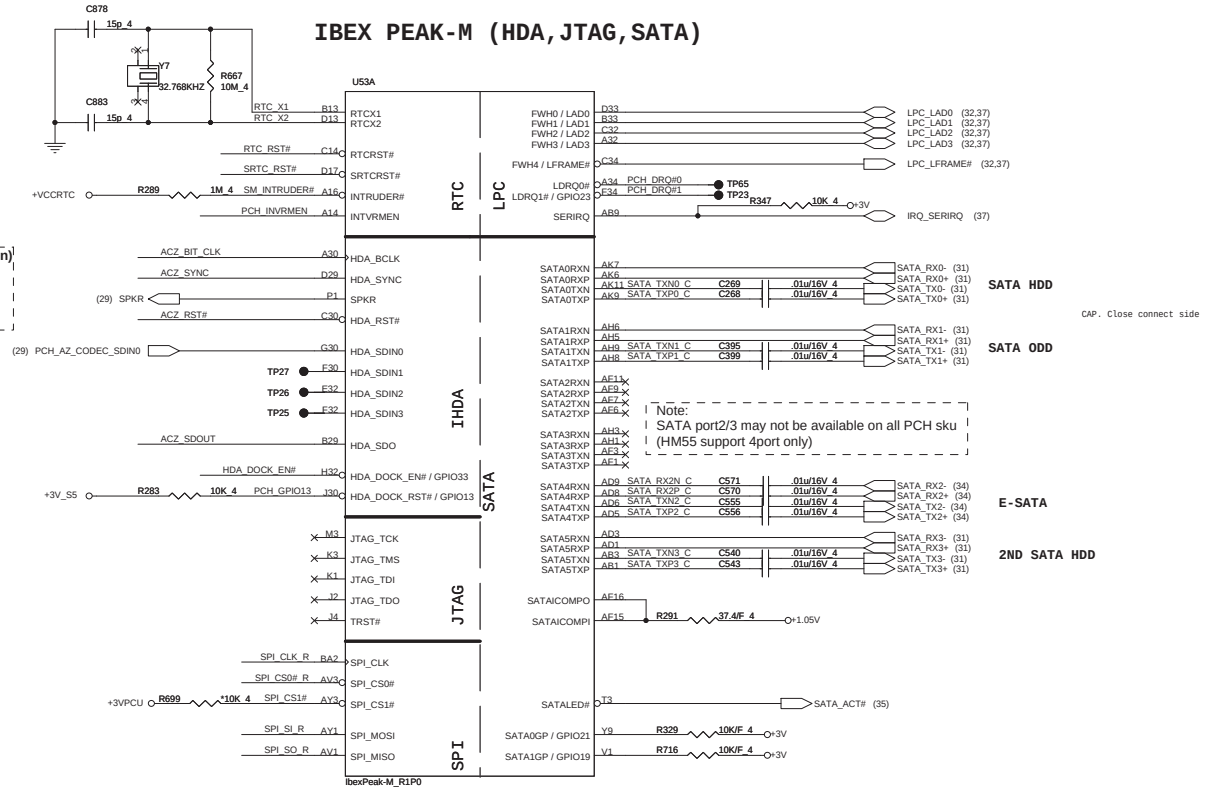


Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

PCH SPI



IBEX PEAK-M (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	ZY9B note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R702 *10K_4 SPKR
INIT3_3V	Reserved	PWROK	1 = Default (weak pull-up 20K) Should not be pull-down	
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R584 *10K_4 PCI_GNT3# (10)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+VCCRTC R662 330K_4 PCH_INVRMEN
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 / 1 / SPI 1 / 0 / PCI 0 / 0 / **LPC**	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]** +3V R270 *1K_4 R256 *1K_4 R272 1K_4 R271 1K_4 PCI_GNT0# (10) PCI_GNT1# (10)
GNT0#	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 32ohm)	+1.8V R698 *1K_4 NV_ALE NV_ALE (10,16)
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 32ohm	+1.8V R697 *1K_4 NV_CLE NV_CLE (10,16)
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V R279 *1K_4 R276 *10K_4 HDA_DOCK_EN#
SPI_MOSI	iTPM function Disable	MEPWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V R352 *1K_4 SPI_SI_R
HDA_SDO	Reserved	RSMRST#	Should not be pull-up (weak pull-down 20K)	
GPIO8	Reserved	RSMRST#	Should not be pull-down (weak pull-up 20K)	+3V_S5 R340 10K_4 RSV_GPIO8 (11)
GPIO27	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 20K)	
HDA_SYNC	On-die PLL PWR supply select	RSMRST#	0 = 1.8V supply (weak pull-down 20K) 1 = 1.5V supply	use defaul (0 = 1.8V supply)
GPIO15	Reserved	RSMRST#	0 = TLS no Confidentiality (weak pull-down 20K) 1 = TLS Confidentiality	+3V_S5 R330 1K_4 CR_WAKE# (11,27)

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	IBEX PEAK-M 2/6	1A

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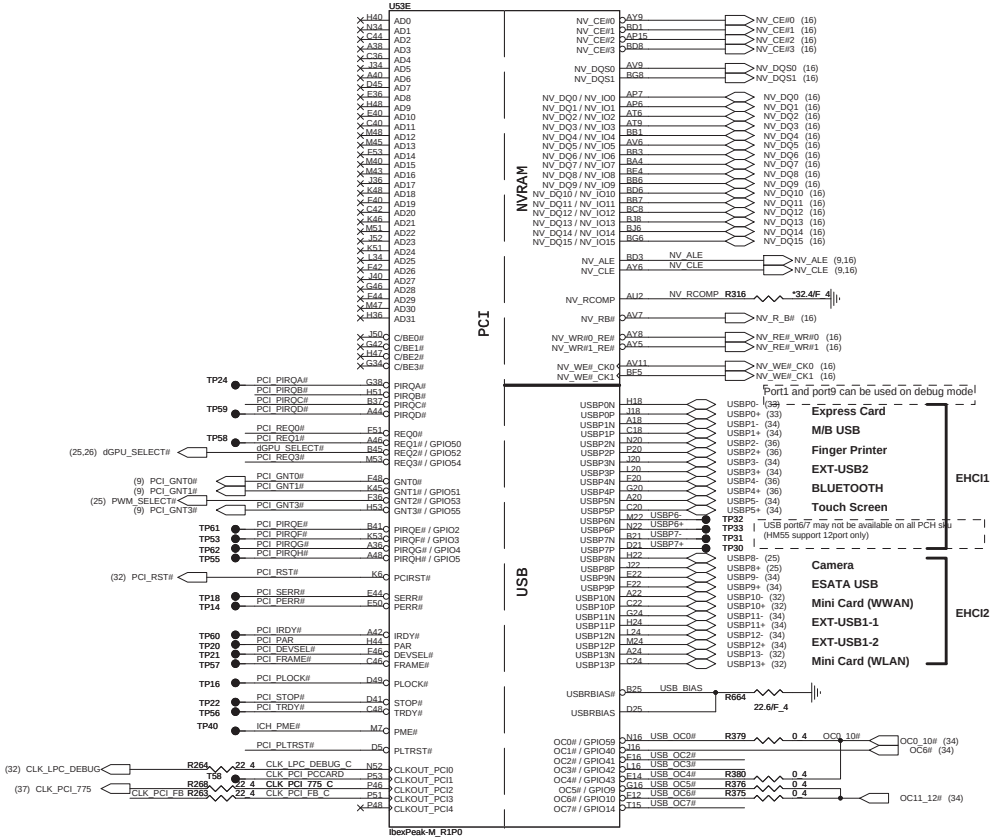
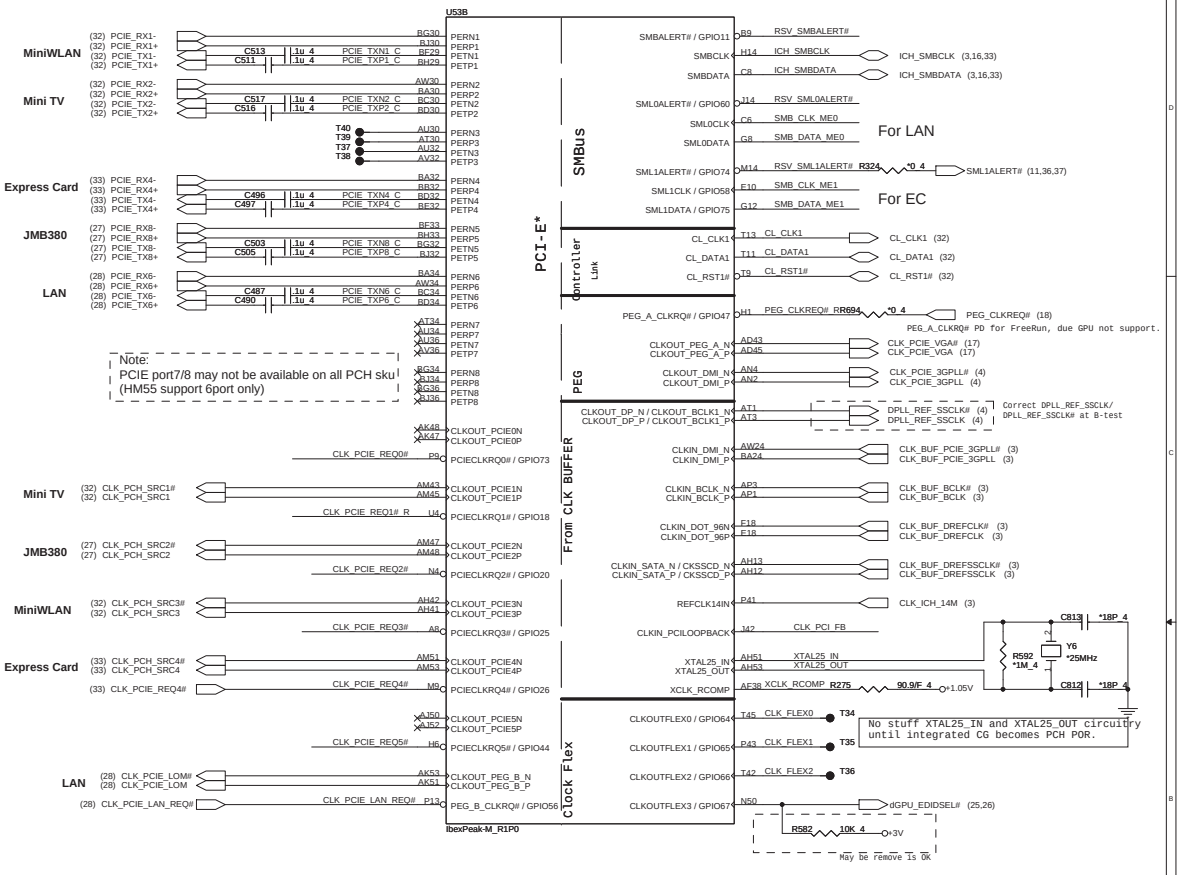
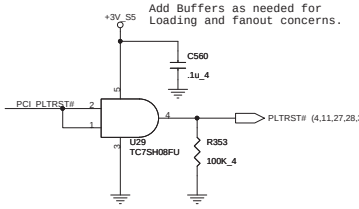
IBEX PEAK-M (PCI,USB,NVRAM)



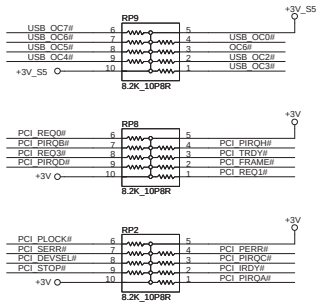
IBEX PEAK-M (PCI-E,SMBUS,CLK)



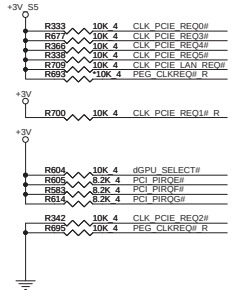
PLTRST#



PCI/USBOC# Pull-up



CLK_REQ/Strap Pin



PEG_A_CLKRQ# PD for FreeRun, due GPU not support.

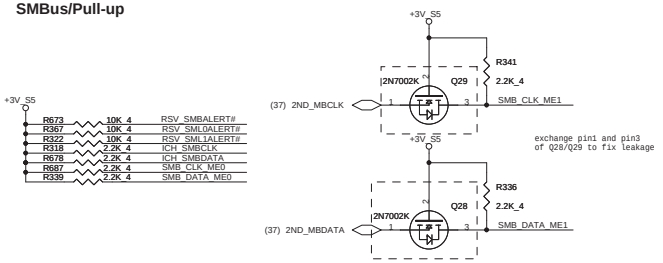
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Boot BIOS Strap		
GNT0#	GNT1#	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

SMBus/Pull-up



Quanta Computer Inc.

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Size	Document Number	Rev
	IBEX PEAK-M 3/6	1A

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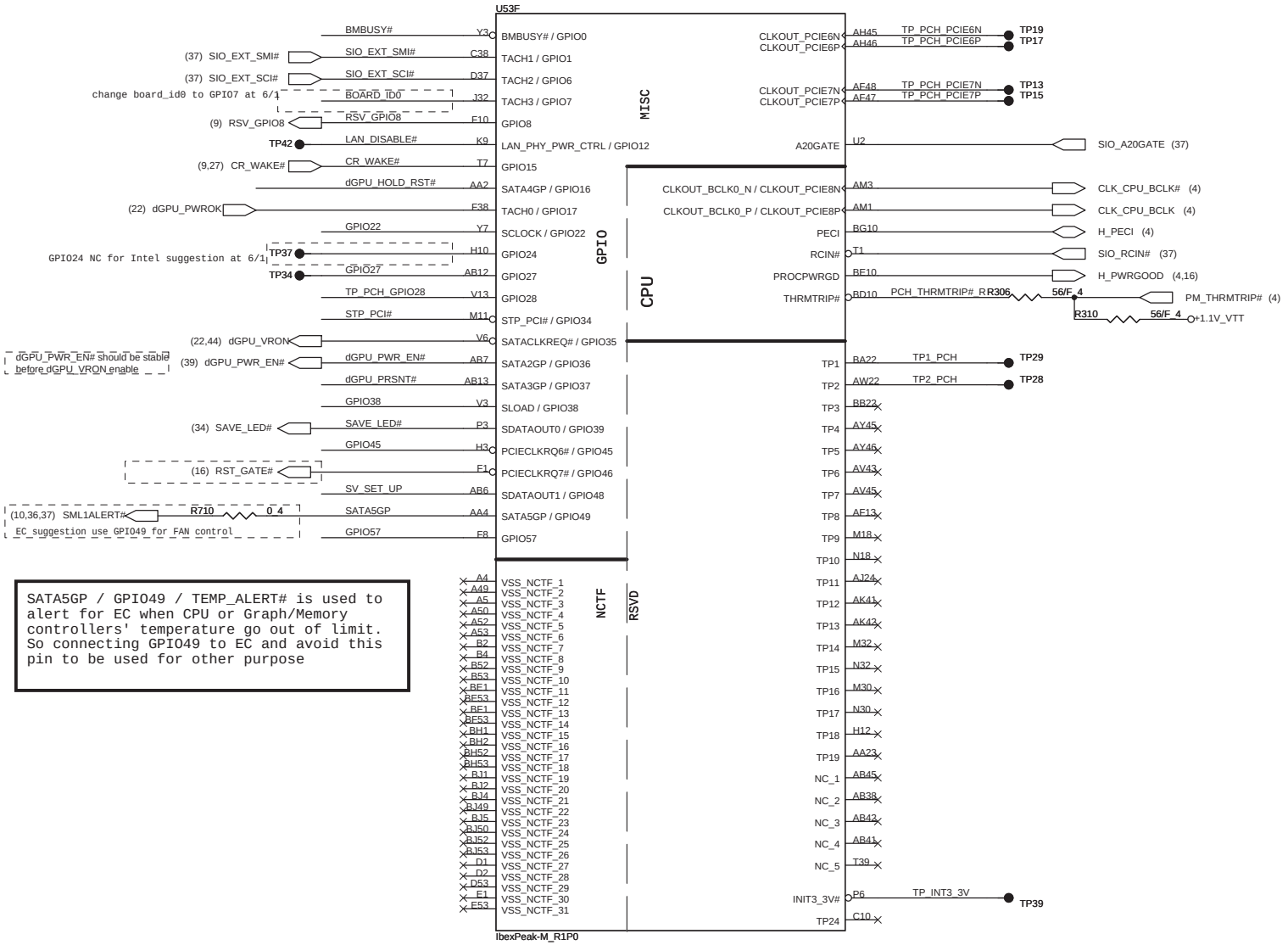
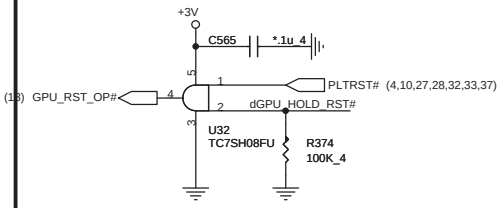
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

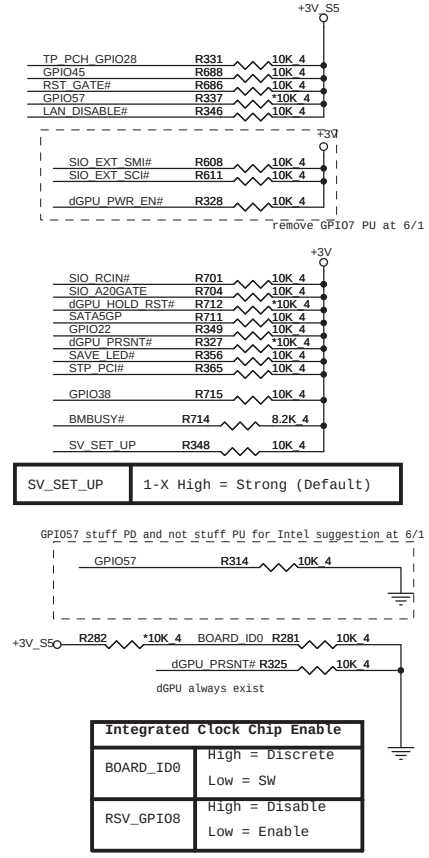


SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)

Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable

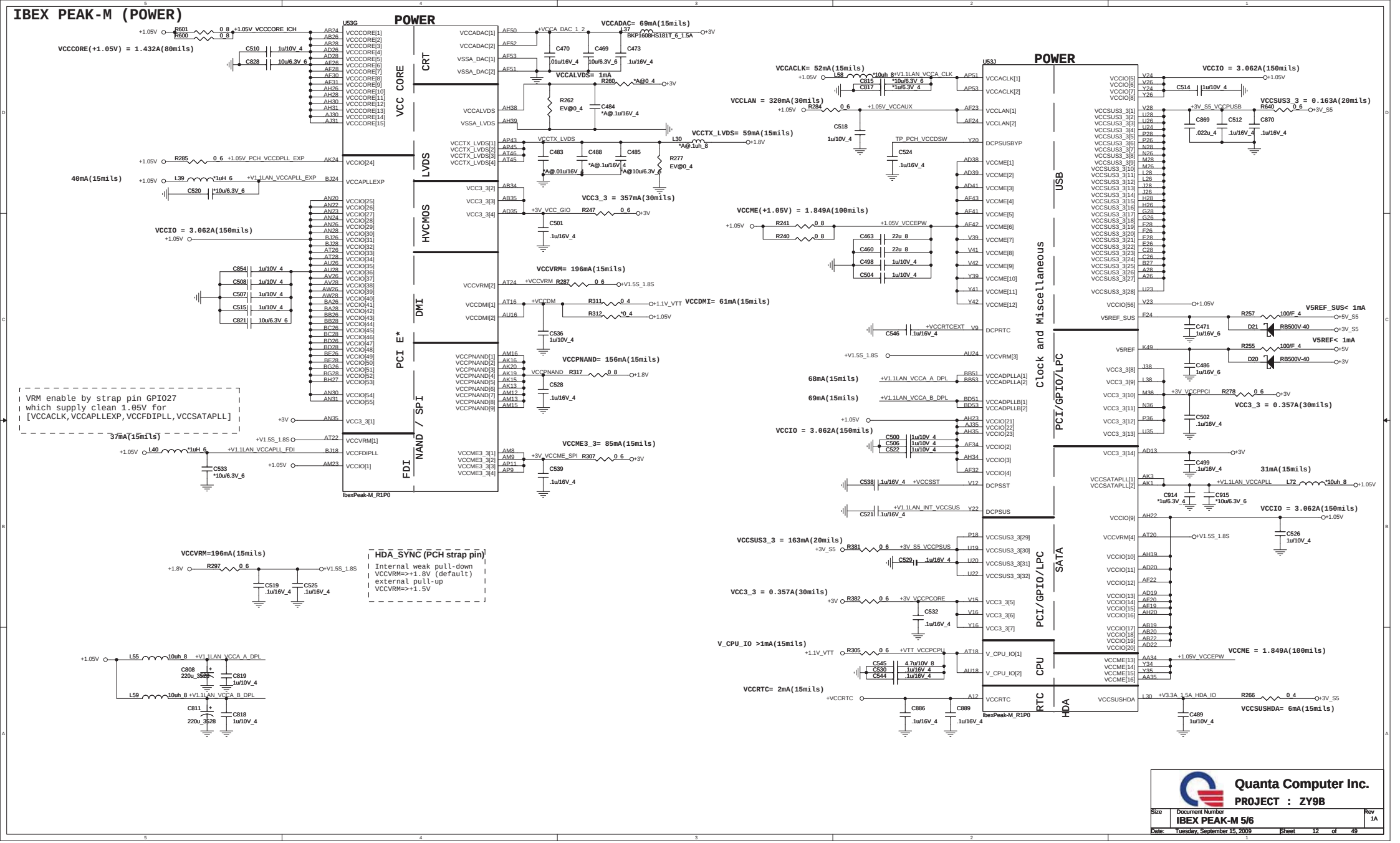
Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	IBEX PEAK-M 4/6	1A

Date: Tuesday, September 22, 2009 Sheet 11 of 49

IBEX PEAK-M (POWER)



Quanta Computer Inc.			
PROJECT : ZY9B			
Size	Document Number		Rev
	IBEX PEAK-M 5/6		1A
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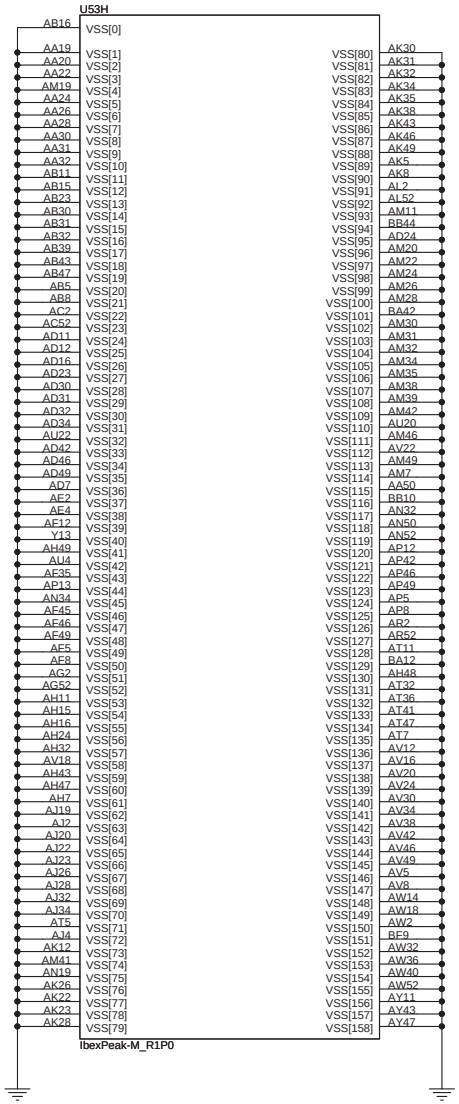
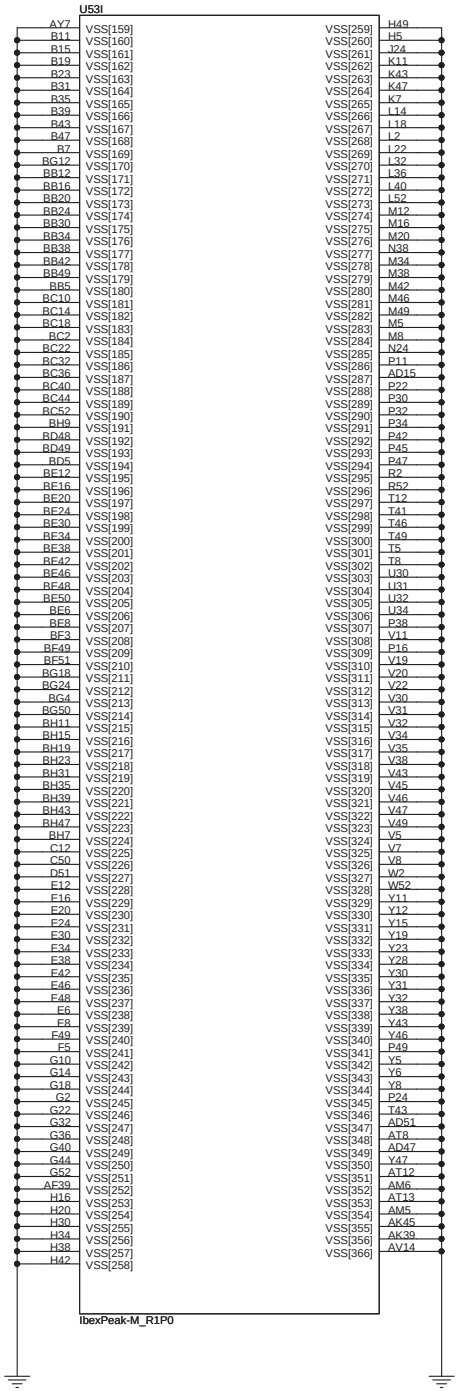
IBEX PEAK-M (GND)

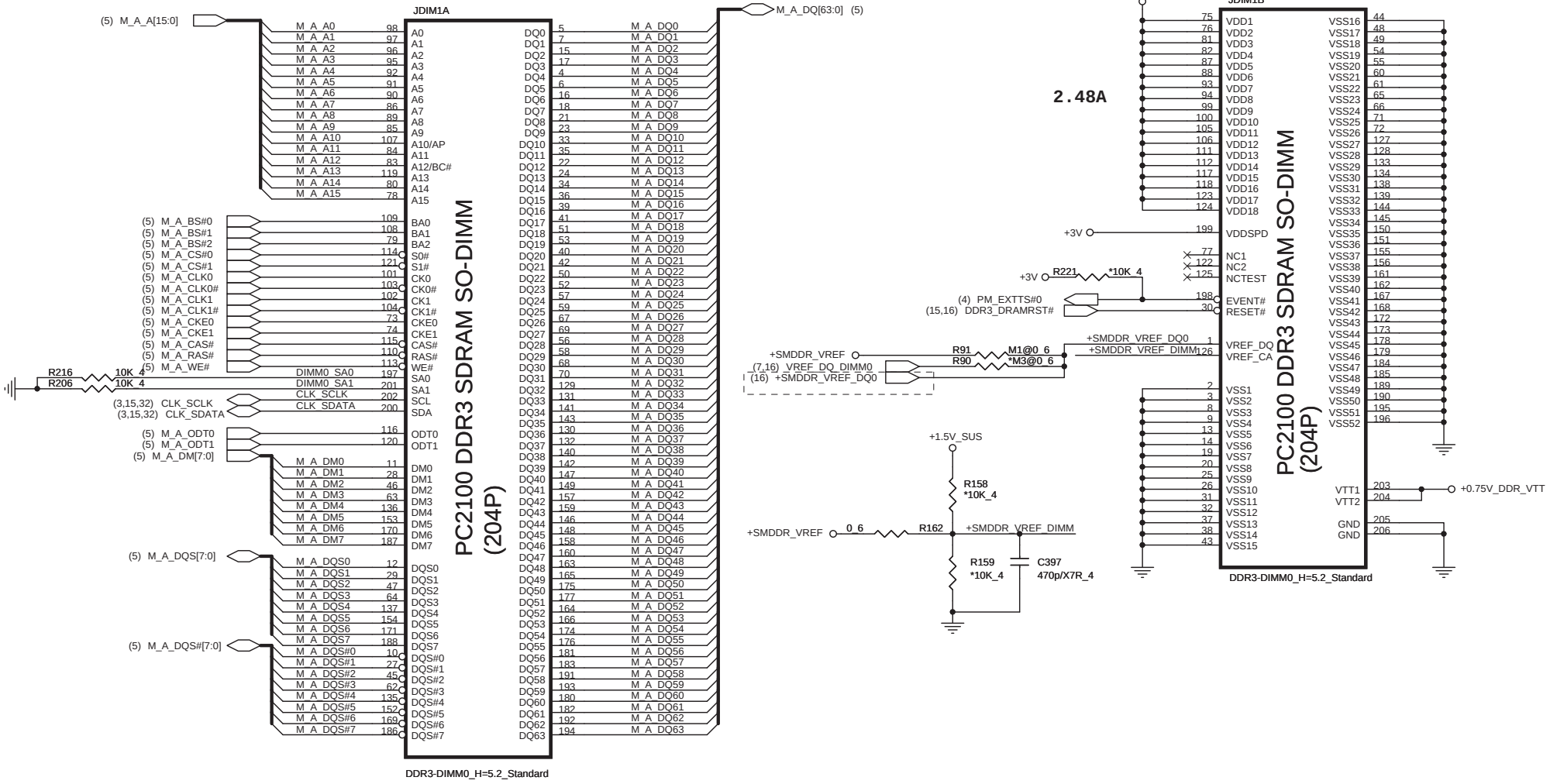




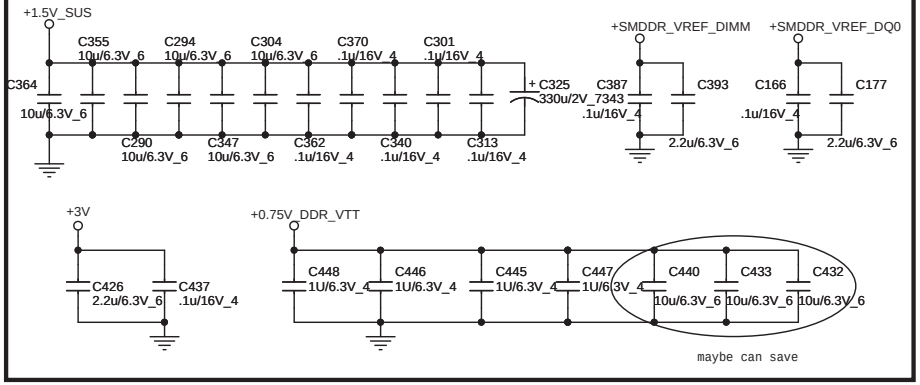
Quanta Computer Inc.

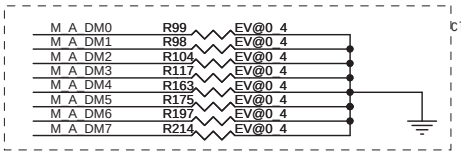
PROJECT : ZY9B

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A
Date: Thursday, June 18, 2009	Sheet 13 of 49	



Place these Caps near So-Dimm0.

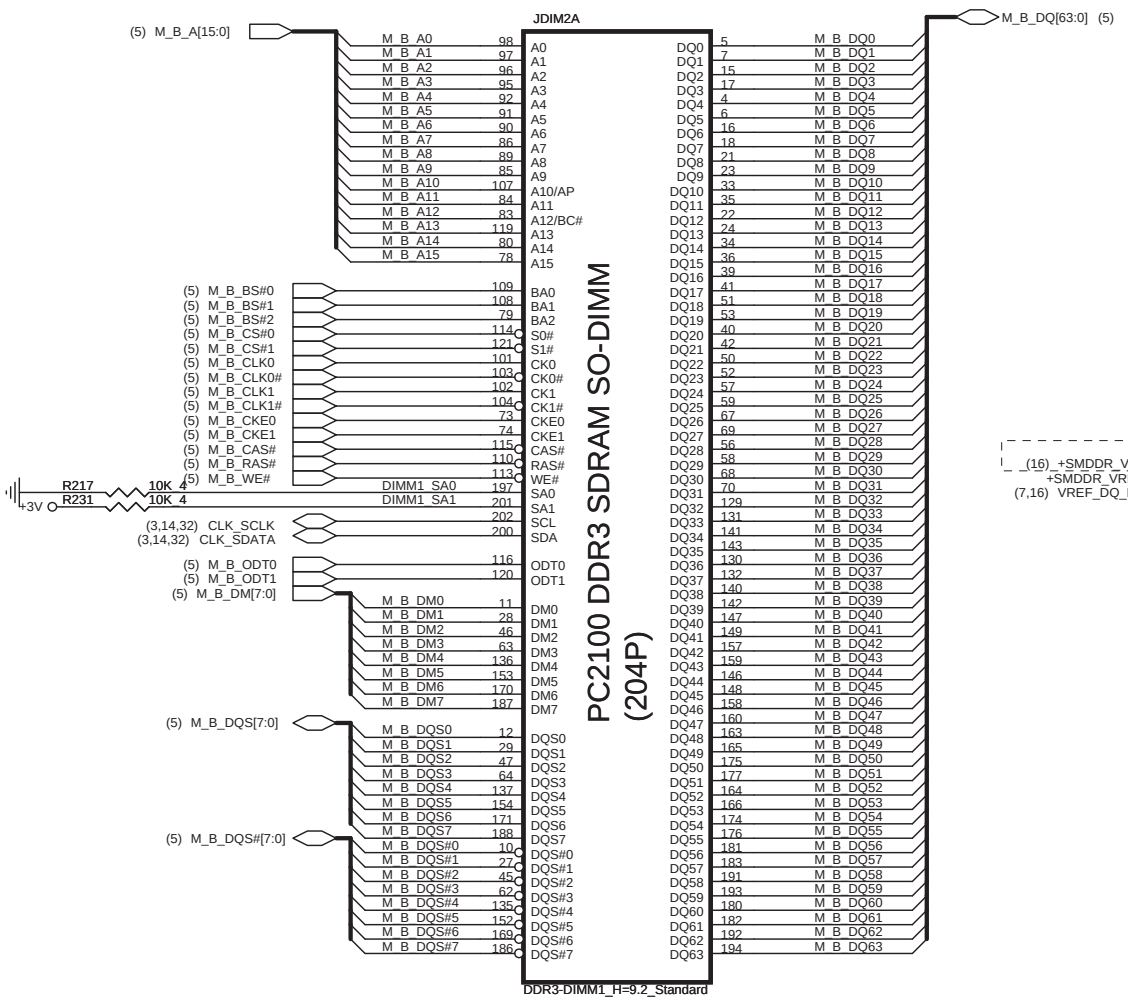


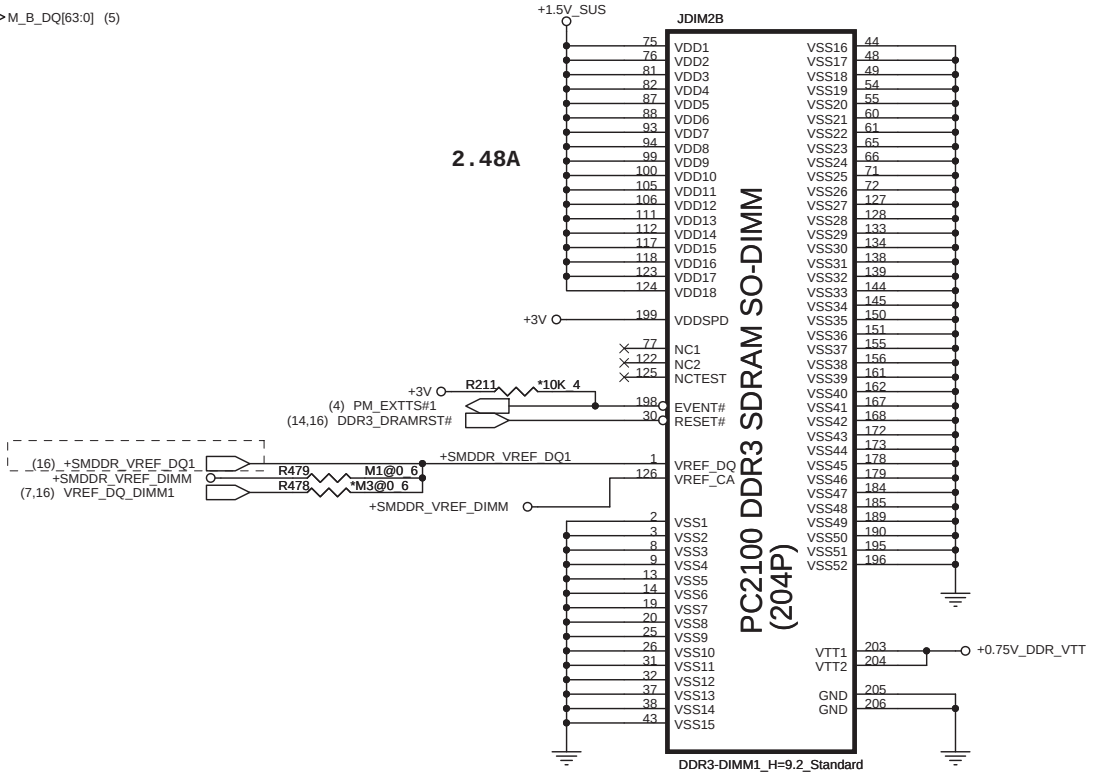


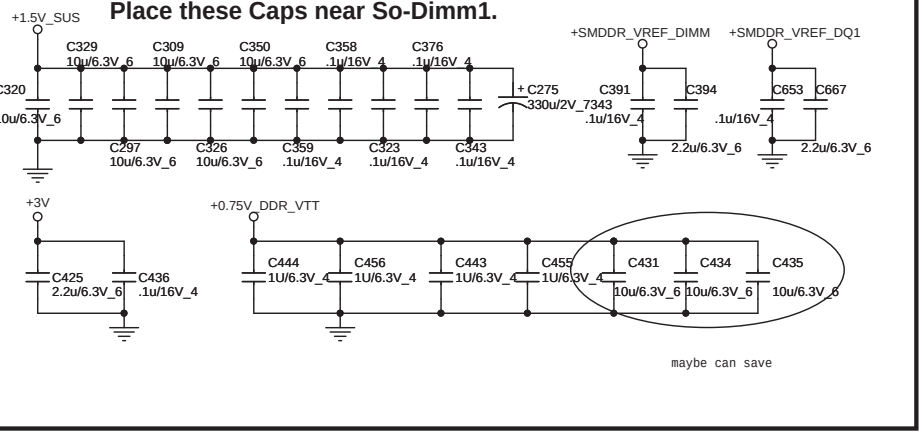
Quanta Computer Inc.

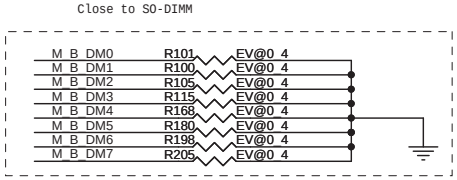
PROJECT : ZY9B

Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
Date: Thursday, September 17, 2009	Sheet 14 of 49	



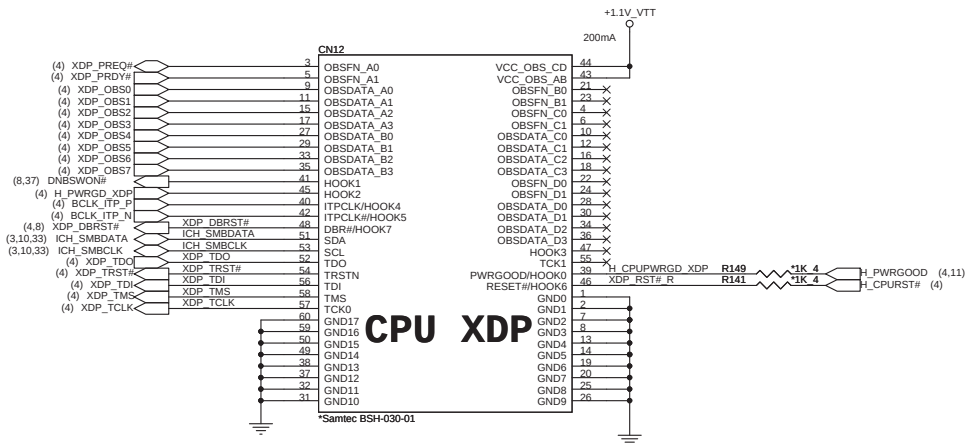




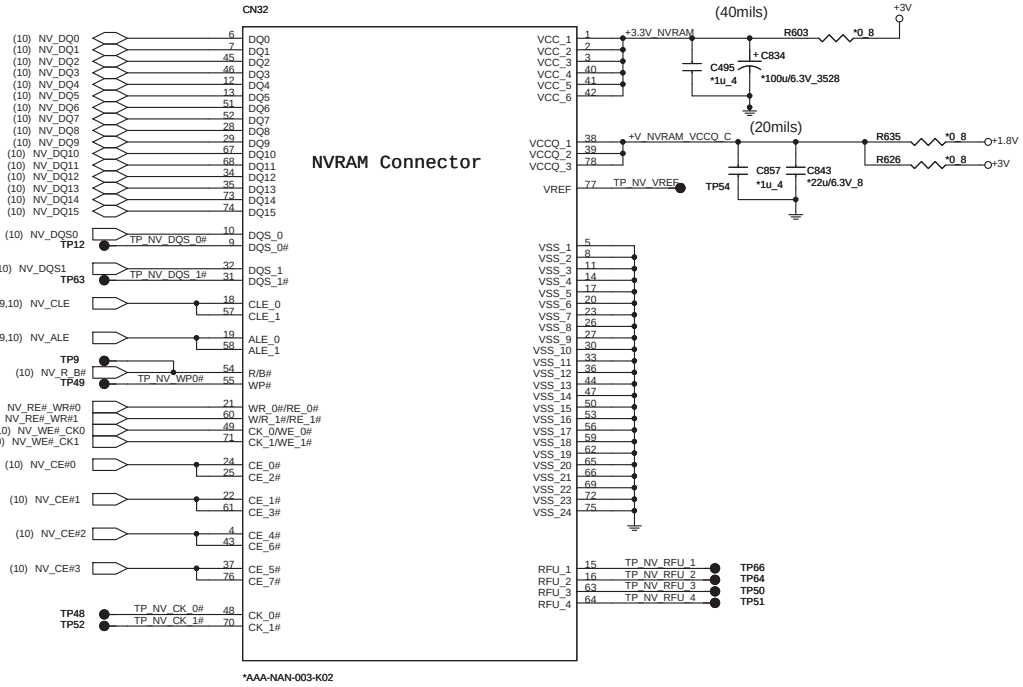


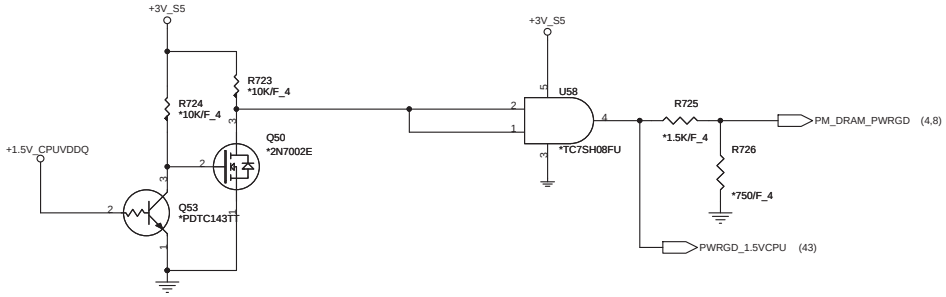
Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: DDRIII SO-DIMM-1	Rev: 1A
Date: Thursday, September 17, 2009	Sheet 15 of 49	

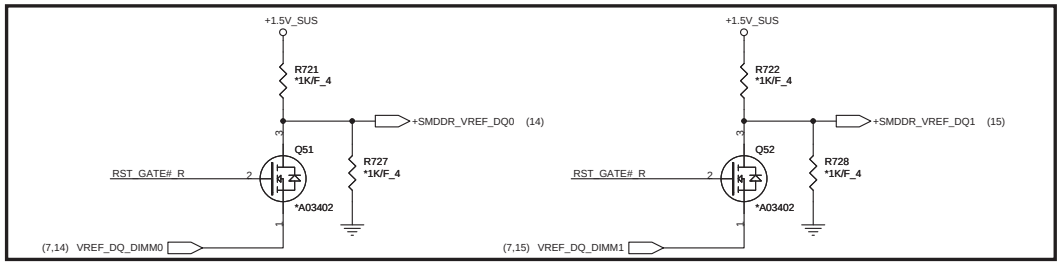
CPU XDP Connector

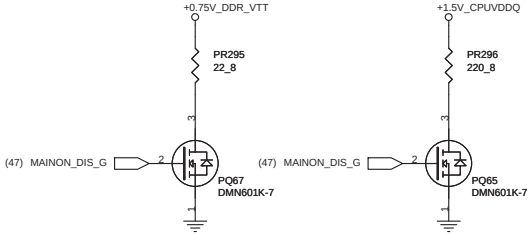


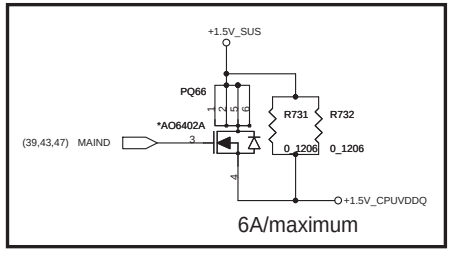
Braidwood

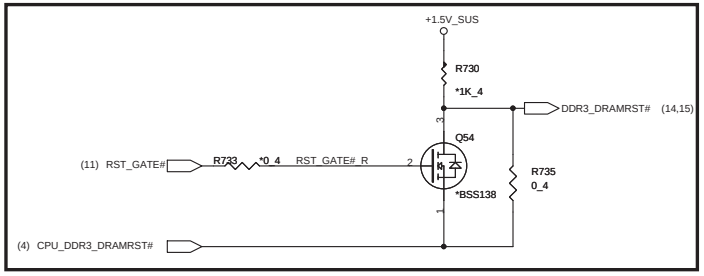


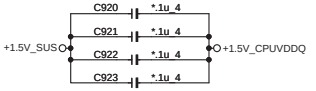












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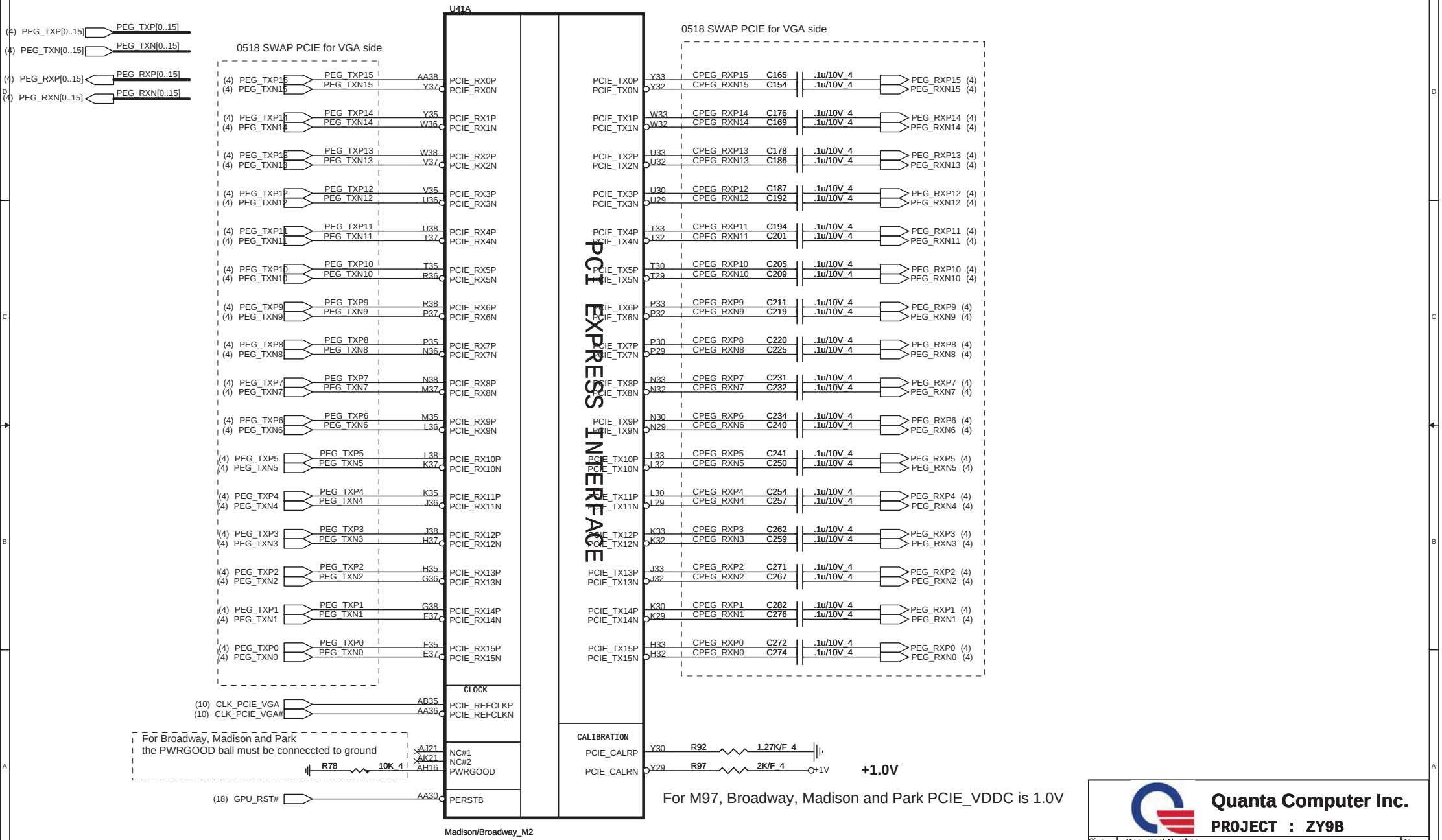
PROJECT : ZY9

Size	Document Number	Rev
	XDP/BRAIDWOOD	1A

Date: Thursday, September 17, 2009 Sheet 16 of 49



Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number	Rev
	Madison/Broadway-PCIE I/F	1A
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GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK

1.8V GPIO

3.3V GPIO

U41B

MUTI GFX

DVPCNTL_MVP_0
DVPCNTL_MVP_1
DVPCNTL_0
DVPCNTL_1
DVPCNTL_2
DVPCLK
DVPDATA_0
DVPDATA_1
DVPDATA_2
DVPDATA_3
DVPDATA_4
DVPDATA_5
DVPDATA_6
DVPDATA_7
DVPDATA_8
DVPDATA_9
DVPDATA_10
DVPDATA_11
DVPDATA_12
DVPDATA_13
DVPDATA_14
DVPDATA_15
DVPDATA_16
DVPDATA_17
DVPDATA_18
DVPDATA_19
DVPDATA_20
DVPDATA_21
DVPDATA_22
DVPDATA_23

(24) RAM_STRAP0
(24) RAM_STRAP1
(24) RAM_STRAP2
+3V_D
T51
R73 10K/F_4
R75 10K/F_4

I2C

SCL
SDA

GENERAL PURPOSE I/O

GPIO_0
GPIO_1
GPIO_2
GPIO_3_SMBDATA
GPIO_4_SMBCLK
GPIO_5_AC_BATT
GPIO_6
GPIO_7_BLON
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15_PWRCNTL_0
GPIO_16_SSIN
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20_PWRCNTL_1
GPIO_21_BB_EN
GPIO_22_ROMCSB
GPIO_23_CLKREQB
JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
GENERICF
GENERICG

(24) GPU_GPIO0
(24) GPU_GPIO1
(24) GPU_GPIO2
(24) GPIO3_SMBDAT
(24) GPIO4_SMBCLK
(44) PWR_PSI#
(45) IO_VID0
(25) EV_LVDS_BLON
(24) SOUT_GPIO8
(24) SIN_GPIO9
(24) SCLK_GPIO10
(24) GPU_GPIO11
(24) GPU_GPIO12
(24) GPU_GPIO13
(26) EXT_DP_HPD
(44) GPU_VID2
(44) GPU_VID1
(24) ALT#_GPIO17
T54
(44) GPU_VID3
T7
(24) SCS#_GPIO22
R759 10K/F_4 GPIO24_TRSTB
R761 10K/F_4
T2
(3) 27M_CLK
R760 10K/F_4
T6
(10) PEG_CLKREQ#
R430 *10K_4
R433 10K/F_4
R445 *10K/F_4
R451 *10K/F_4
(26) EXT_HDMI_HPD
HPD1

PLL/CLOCK

DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
XTALIN
XTALOUT

Change C612/C613 from 18p to 27p at B-test

C612 27p/50V_4
Y5 27MHZ
R446 1M/F_4
C613 27p/50V_4
XTALI_27M
XTALO_27M

THERMAL

DPLUS
DMINUS
(24) GPU_D+
(24) GPU_D-
T13
TS_FDO
TSVDD
TSVSS
TS_VDD

+1.8V_GPU
R31 499/F_4
R32 249/F_4
C71 .1u_4
VREFG

+1.8V(75mA)
+1.8V_GPU
120 ohm/300mA
L21 BLM15BD121SN1_4
DPLL_PVDD
C117 10u_6
C119 1u_4
C139 .1u_4

+1.0V(125mA)
+1V
120 ohm/300mA
L46 BLM15BD121SN1_4
DPLL_VDDC
C614 10u_6
C615 1u_4
C135 .1u_4

+1.8V(5mA)
+1.8V_GPU
120 ohm/300mA
L25 BLM15BD121SN1_4
TS_VDD
C138 10u_6
C137 .1u_4

DPA
TXCAP_DPA3P AU24
TXCAM_DPA3N AV23
EXT_HDMICLK+ (26)
EXT_HDMICLK- (26)
TX0P_DPA2P AT25
TX0M_DPA2N AR24
EXT_HDMITX0P (26)
EXT_HDMITX0N (26)
TX1P_DPA1P AU26
TX1M_DPA1N AV25
EXT_HDMITX1P (26)
EXT_HDMITX1N (26)
TX2P_DPA0P AT27
TX2M_DPA0N AR26
EXT_HDMITX2P (26)
EXT_HDMITX2N (26)

DPB
TXCBP_DPB3P AR30
TXCBM_DPB3N AT29
T50
T41
TX3P_DPB2P AV31
TX3M_DPB2N AU30
T55
T46
TX4P_DPB1P AR32
TX4M_DPB1N AT31
T56
T42
TX5P_DPB0P AT33
TX5M_DPB0N AU32
T5
T11

DPC
TXCCP_DPC3P AU14
TXCCM_DPC3N AV13
EXT_DP_TX3P (26)
EXT_DP_TX3N (26)
TX0P_DPC2P AT15
TX0M_DPC2N AR14
EXT_DP_TX2P (26)
EXT_DP_TX2N (26)
TX1P_DPC1P AU16
TX1M_DPC1N AV15
EXT_DP_TX1P (26)
EXT_DP_TX1N (26)
TX2P_DPC0P AT17
TX2M_DPC0N AR16
EXT_DP_TX0P (26)
EXT_DP_TX0N (26)

DPD
TXCDP_DPD3P AU20
TXCDM_DPD3N AT19
T45
T47
TX3P_DPD2P AT21
TX3M_DPD2N AR20
T43
T49
TX4P_DPD1P AU22
TX4M_DPD1N AV21
T44
T53
TX5P_DPD0P AT23
TX5M_DPD0N AR22
T48
T52

DAC1
R
RB
G
GB
B
BB
EXT_CRT_RED (25)
EXT_CRT_GRN (25)
EXT_CRT_BLU (25)
HSYNC
VSYNC
EXT_HSYNC (24,25)
EXT_VSYNC (24,25)
R463 150/F_4
R462 150/F_4
R465 150/F_4
RSET
R76 499/F_4
AVDD
AVSSQ
VDD1DI
VSS1DI

DAC2
R2
R2B
G2
G2B
B2
B2B
C
Y
COMP
H2SYNC
V2SYNC
V2SYNC (24)
VDD2DI
VSS2DI
A2VDD
A2VDDQ
A2VSSQ
R2SET
R89 715/F_4
+3V_D (3.3V@130mA A2VDD)
C153 .1u/10V_4

DDC/AUX
DDC1CLK AM26
DDC1DATA AN26
EV_HDMI_DDCCK (26)
EV_HDMI_DDCDAT (26)
HDMI
AUX1P AM27
AUX1N AL27
T12
T9
DDC2CLK AM19
DDC2DATA AL19
AUX2P AN20
AUX2N AM20
EXT_DP_AUXDP (26)
EXT_DP_AUXDN (26)
Display Port
DDCCLK_AUX3P AL30
DDCDATA_AUX3N AM30
EV_CRTDCLK (25)
EV_CRTDDAT (25)
CRT
DDCCLK_AUX4P AL29
DDCDATA_AUX4N AM29
EV_LVDS_DDCCLK (25)
EV_LVDS_DDCDAT (25)
LVDS
DDCCLK_AUX5P AN21
DDCDATA_AUX5N AM21
T14
T15
DDC6CLK AJ30
DDC6DATA AJ31
T18
T4
NC_DDCCLK_AUX7P AK30
NC_DDCDATA_AUX7N AK29
T10
T3

Madison/Broadway_M2

U41G

LVDS CONTROL

VARY_BL AK27
DIGON AJ27
EV_LVDS_BRIGHT (25)
EV_LVDS_VDDEN (25)
TXCLK_UP_DPF3P AK35
TXCLK_UN_DPF3N AL36
EV_TXUCLKOUT+ (25)
EV_TXUCLKOUT- (25)
TXOUT_U0P_DPF2P AJ38
TXOUT_U0N_DPF2N AK37
EV_TXUOUT0+ (25)
EV_TXUOUT0- (25)
TXOUT_U1P_DPF1P AH35
TXOUT_U1N_DPF1N AJ36
EV_TXUOUT1+ (25)
EV_TXUOUT1- (25)
TXOUT_U2P_DPF0P AG38
TXOUT_U2N_DPF0N AH37
EV_TXUOUT2+ (25)
EV_TXUOUT2- (25)
TXOUT_U3P AF35
TXOUT_U3N AG36

LVTMDP

TXCLK_LP_DPE3P AP34
TXCLK_LN_DPE3N AR34
EV_TXLCLKOUT+ (25)
EV_TXLCLKOUT- (25)
TXOUT_L0P_DPE2P AW37
TXOUT_L0N_DPE2N AU35
EV_TXLOUT0+ (25)
EV_TXLOUT0- (25)
TXOUT_L1P_DPE1P AR37
TXOUT_L1N_DPE1N AU39
EV_TXLOUT1+ (25)
EV_TXLOUT1- (25)
TXOUT_L2P_DPE0P AP35
TXOUT_L2N_DPE0N AR35
EV_TXLOUT2+ (25)
EV_TXLOUT2- (25)
TXOUT_L3P AN36
TXOUT_L3N AP37

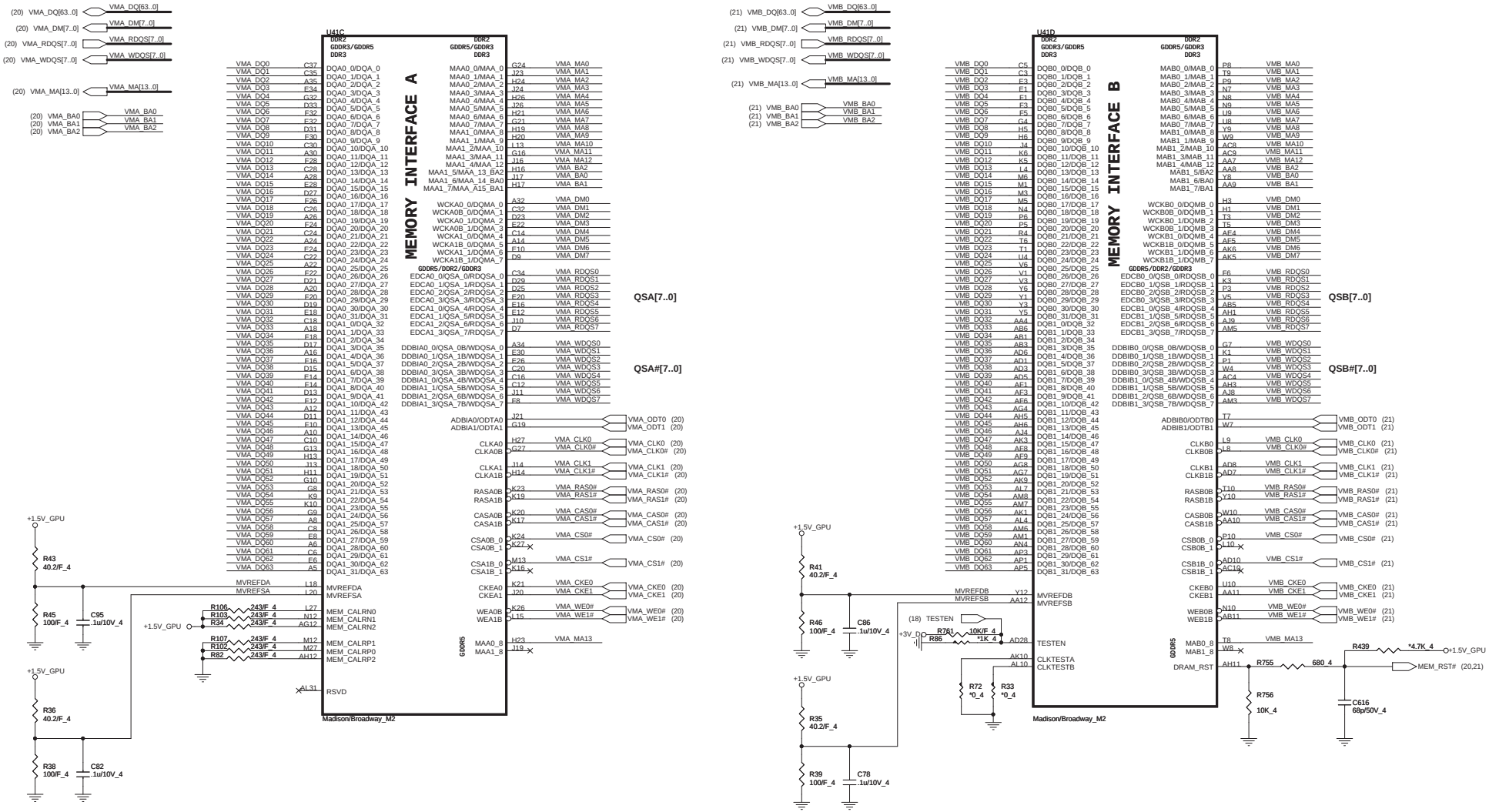
Madison/Broadway_M2

(1.8V@70mA AVDD)
+1.8V_GPU
120 ohm/300mA
L49 BLM15BD121SN1_4
AVDD
C630 .1u/10V_4
C629 1u/6.3V_4
C628 10u/6.3V_6

(1.8V@100mA VDD1DI)
120 ohm/300mA
L52 BLM15BD121SN1_4
VDD1DI
C172 .1u/10V_4
C646 1u/6.3V_4
C636 10u/6.3V_6

(1.8V@2mA A2VDDQ)
+1.8V_GPU
120 ohm/300mA
L50 BLM15BD121SN1_4
A2VDDQ
C170 .1u/10V_4
C650 1u/6.3V_4

R763 *10K/F_4 27M_CLK
+3V_D_ZY9B
C940 *.1u_4
U60
GPIO24_TRSTB
R762 *7.5K_4
C939 *100p/50V_6
C941 *100p/50V_6
R764 *7.5K_4
(11) GPU_RST_OP#
R765 0_4
(17) GPU_RST#
R766 *7.5K_4
*74AHC125PW
TESTEN (19)
C942 *100p/50V_6



Quanta Computer Inc.			
PROJECT : ZY9B			
Size	Document Number		Rev
	Madison/Broadway-MEM I/F		1A
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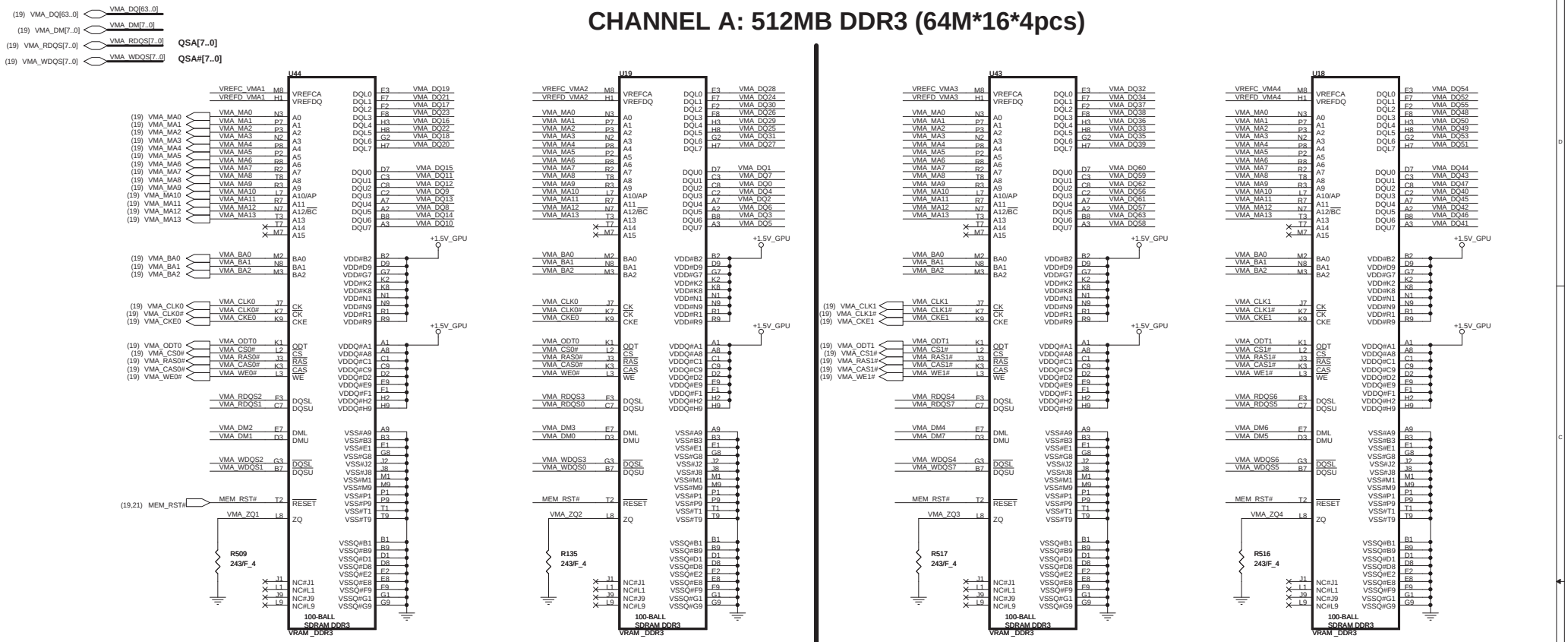
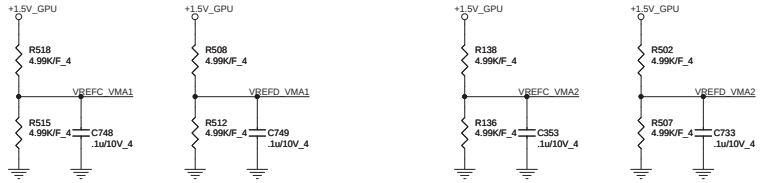
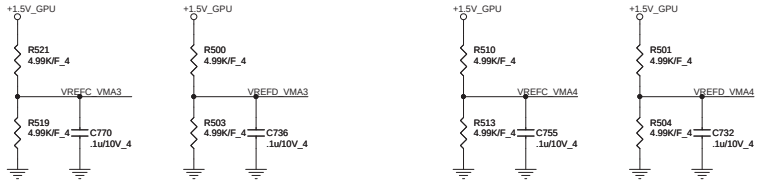
CHANNEL A: 512MB DDR3 (64M*16*4pcs)



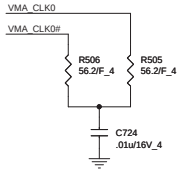
Group-A0 VREF



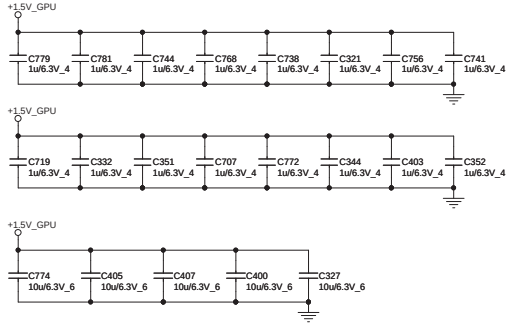
Group-A1 VREF



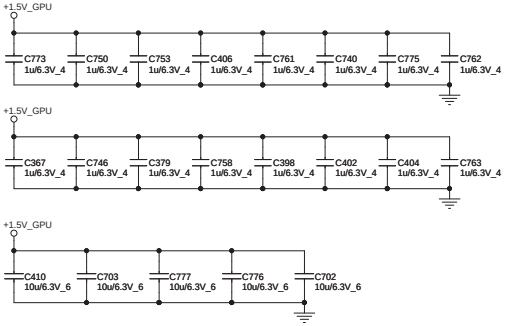
MEM_A0 CLK



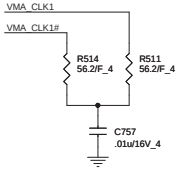
Group-A0 decoupling CAP



Group-A1 decoupling CAP



MEM_A1 CLK



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PROJECT : ZY9B

Size	Document Number	Rev
	MEMORY 1 channel A	1A

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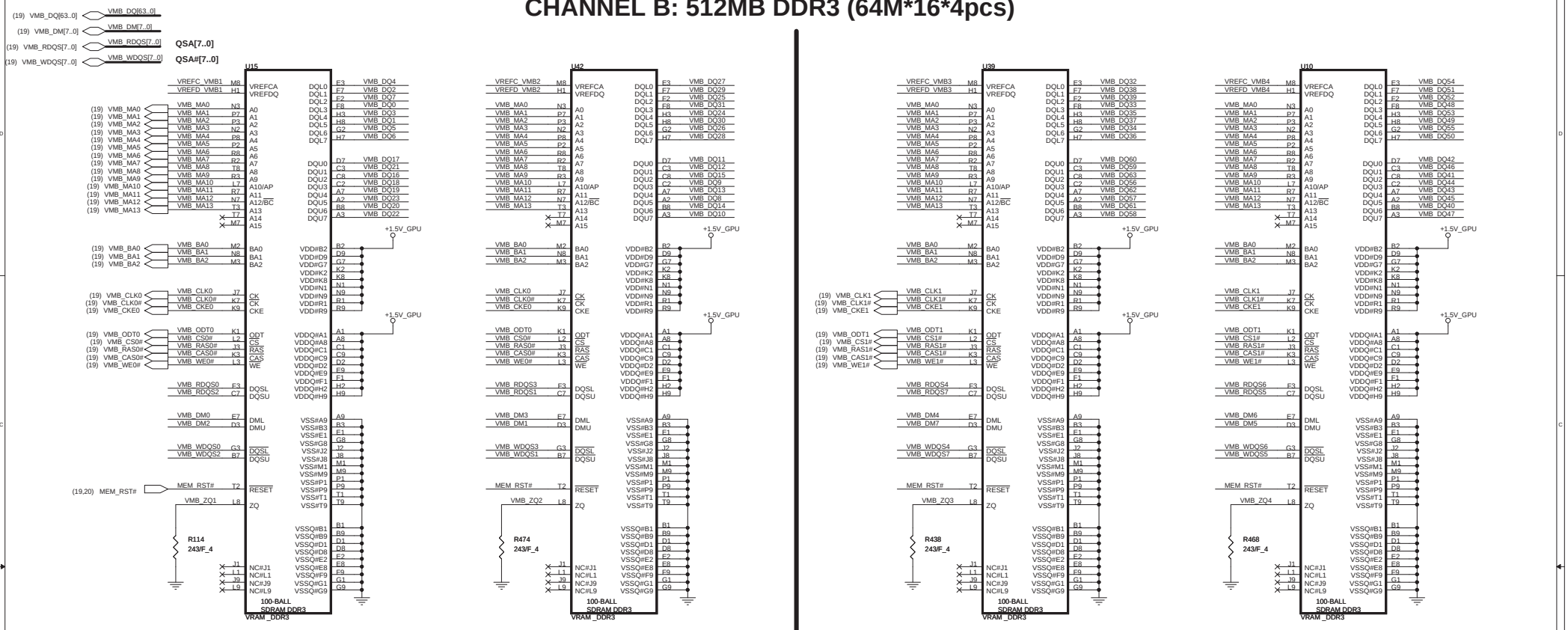
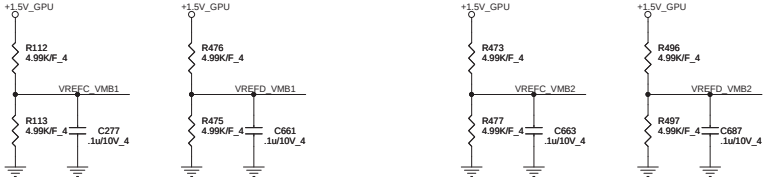
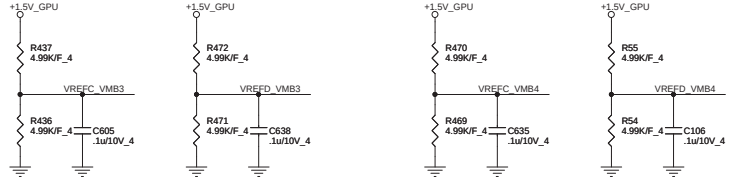
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



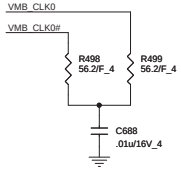
Group-B0 VREF



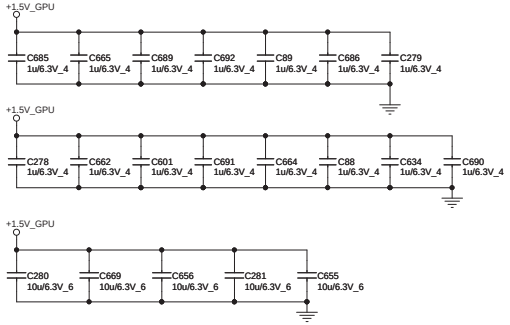
Group-B1 VREF



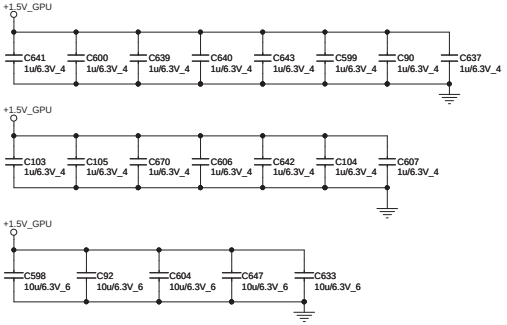
MEM_B0 CLK



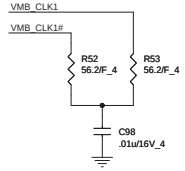
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	MEMORY 2 channel B	1A
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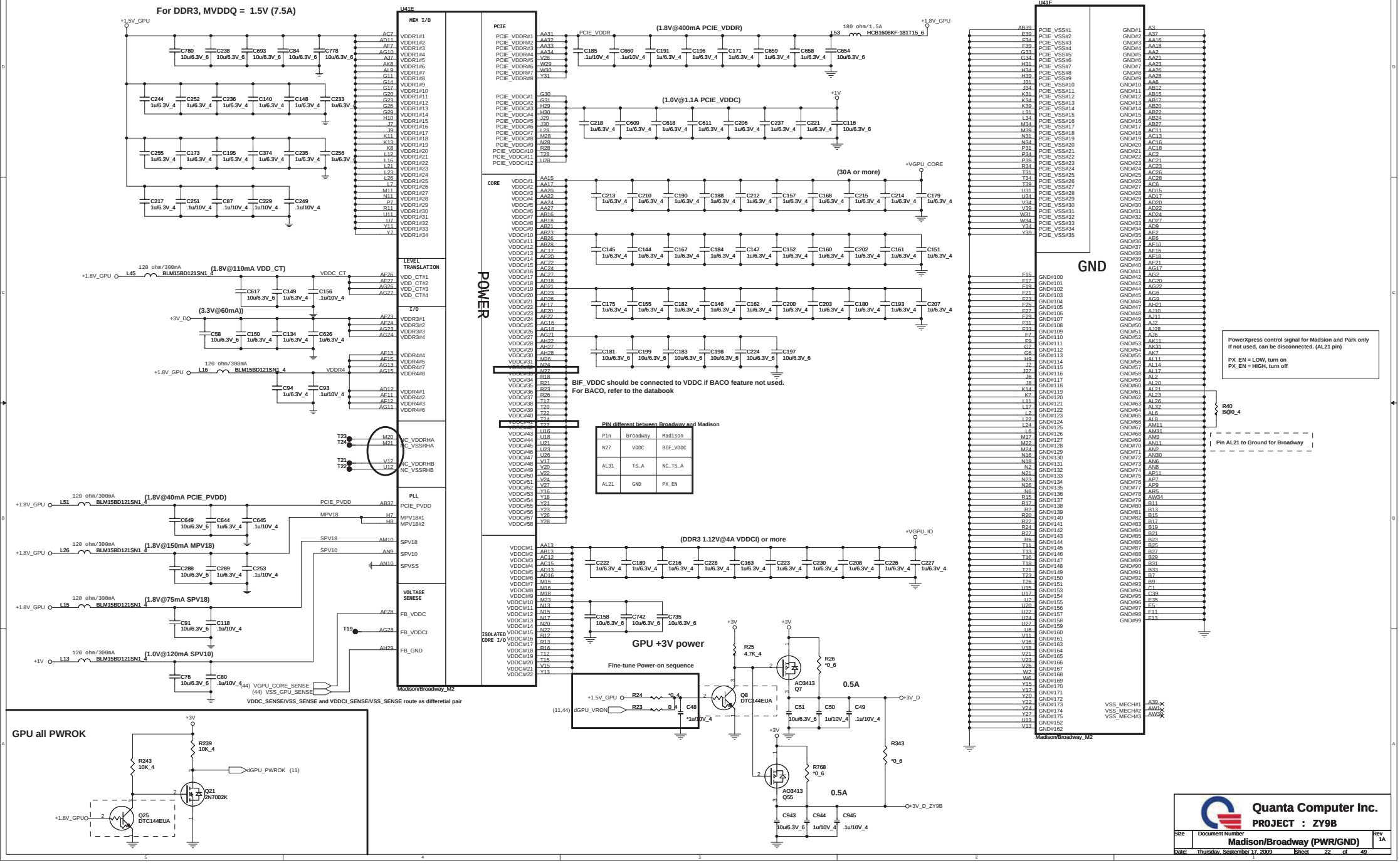
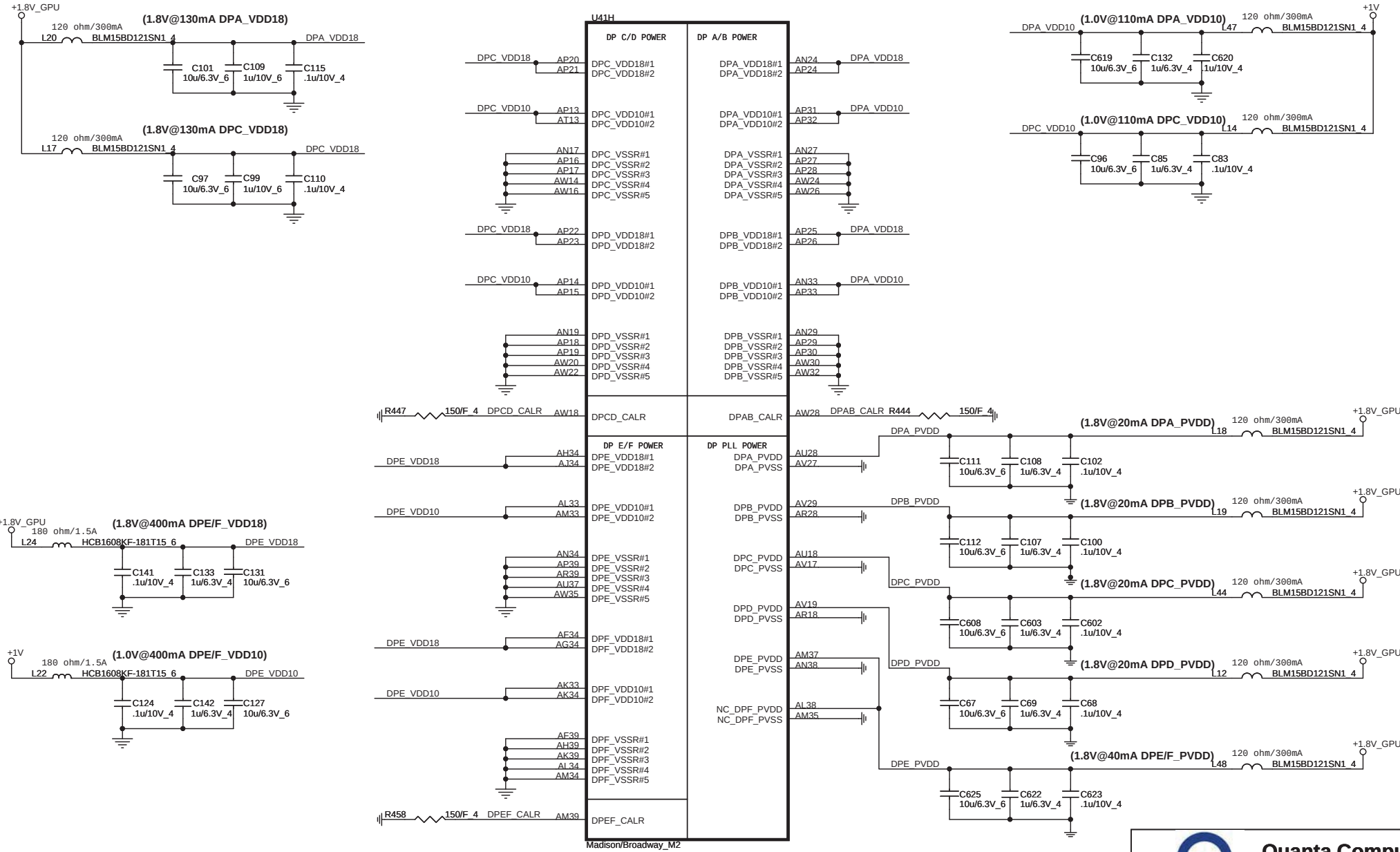
For DDR3, MVDDQ = 1.5V (7.5A)

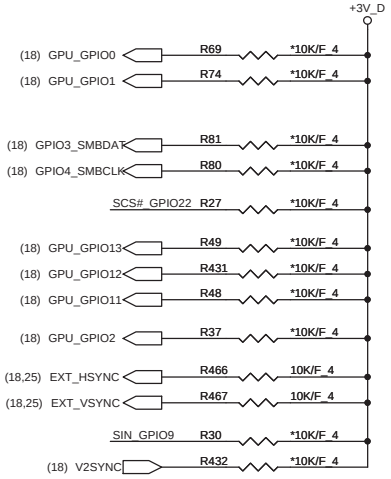


Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: Madison/Broadway (PWR/GND)	Rev: 1A
Date: Thursday, September 17, 2009	Sheet 22 of 49	



Quanta Computer Inc.			
PROJECT : ZY9B			
Size	Document Number		Rev
	Madison/Broadway (DP_PWR/GND)		1A
Date: Tuesday, September 15, 2009		Sheet 23 of 49	

PIN STRAPS



Memory Aperture size	
GPIO[13:11]	**Size**
000	**128MB**
001	256MB
010	64MB
011	32MB

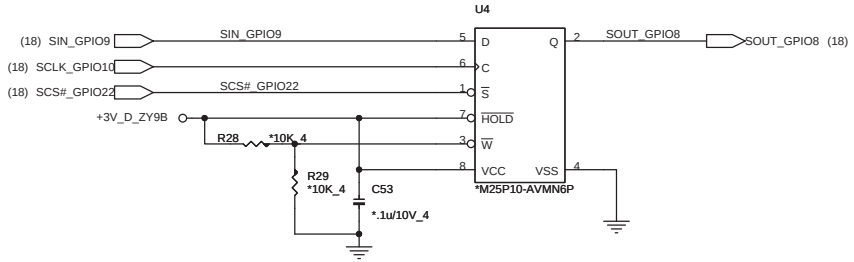
Audio Table		
EXT_HSYNC	**EXT_VSYNC**	**Discription**
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	**1**	**Both DP & HDMI**

CONFIGURATION STRAPS

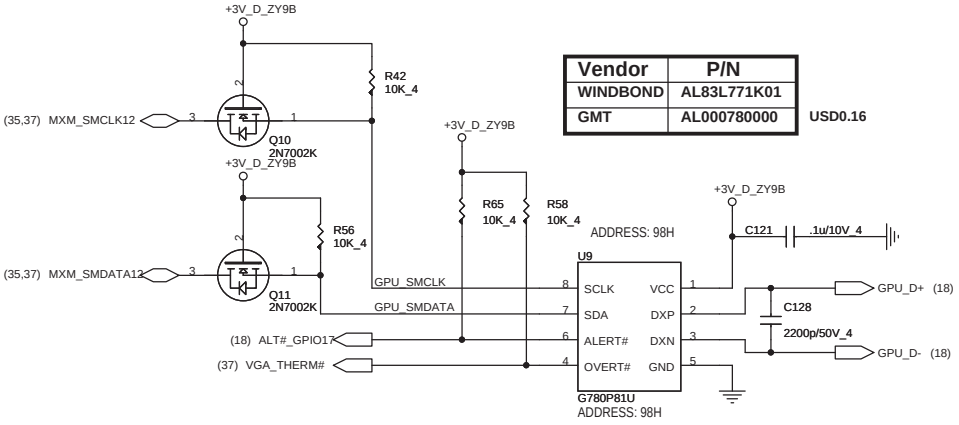
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	**0**	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	**0**	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	**0**	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	**000**	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	**0**	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	**11**	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	**0**	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	**0**	

EEPROM



Thermal Sensor



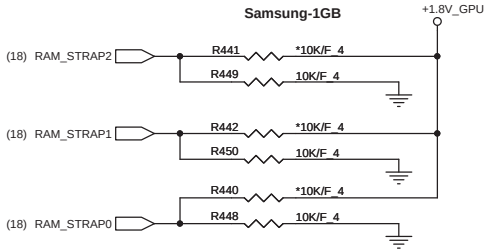
Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

USD0.16

DDR3 VRAM SIZE Strap

DDR3 VRAM size

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB			
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	512MB	0	1	0
			1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

Quanta Computer Inc.
PROJECT : ZY9B

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	Strip/Thermal	1A
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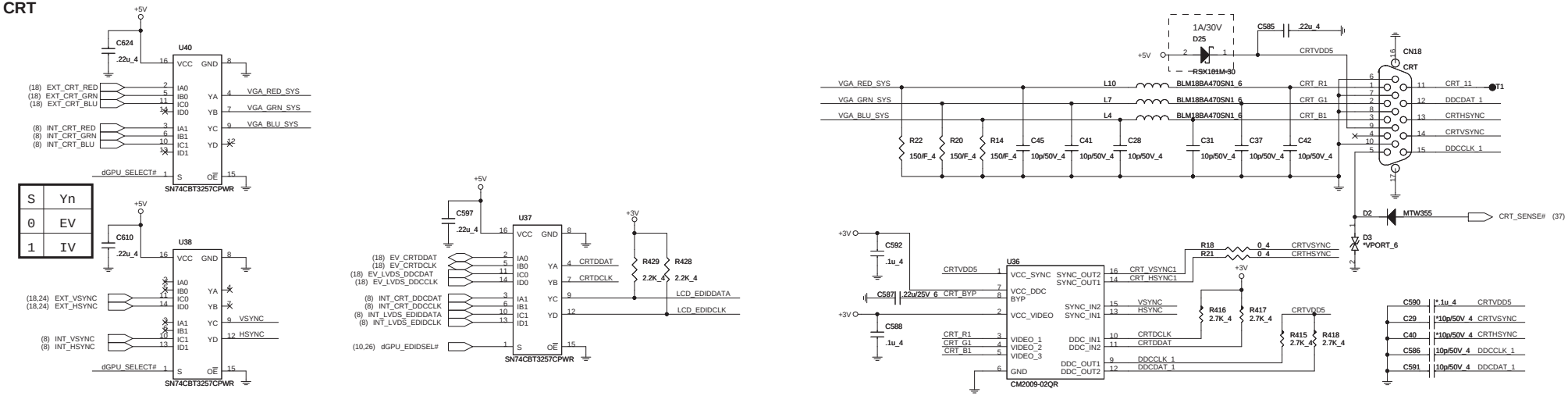
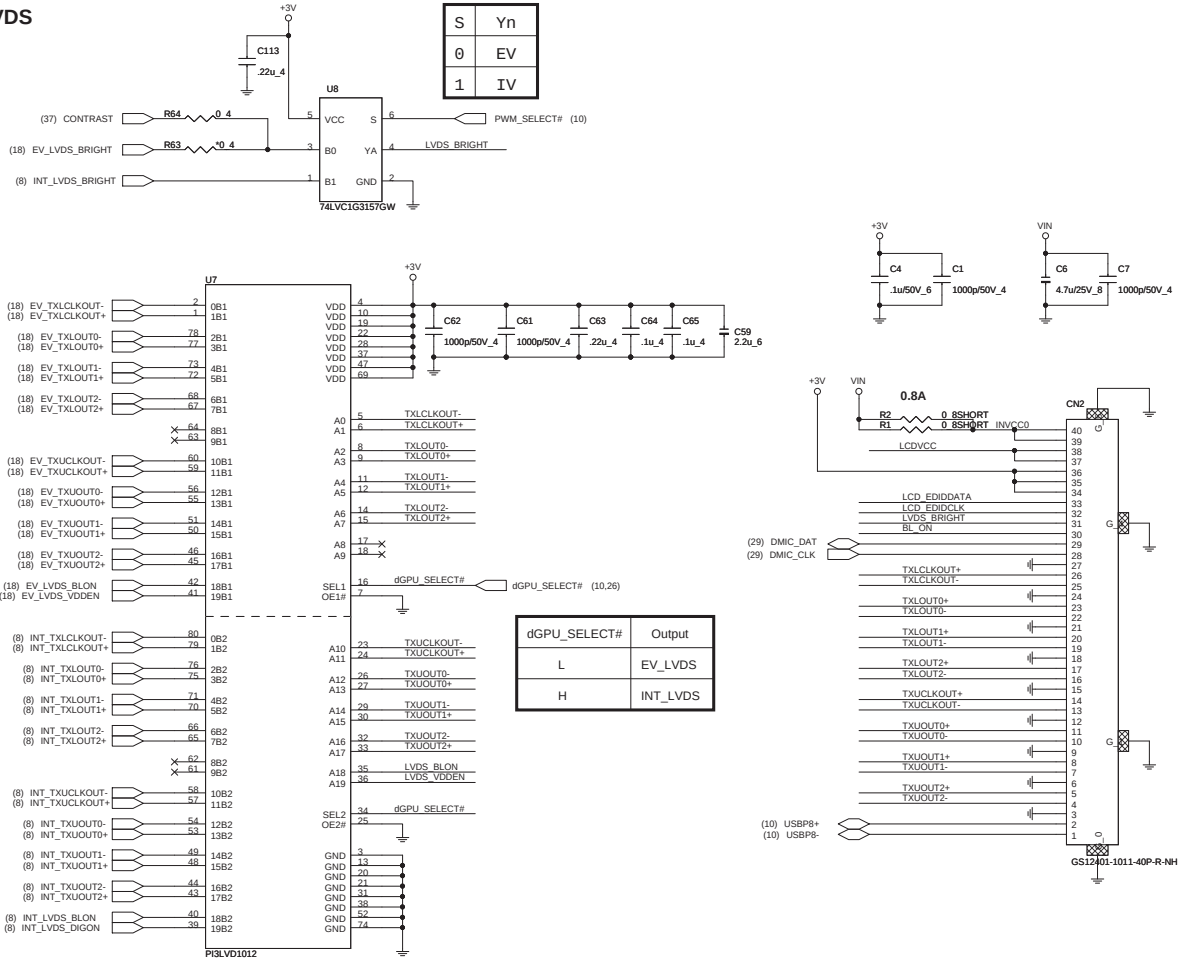
CRT



S	Yn
0	EV
1	IV

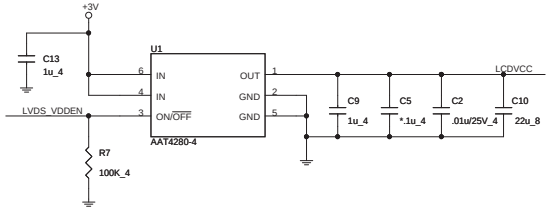
LVDS



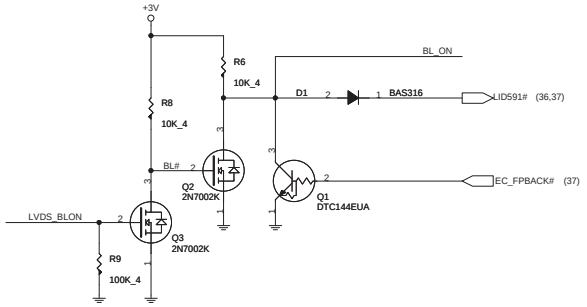
S	Yn
0	EV
1	IV

dGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

LCD Power



Backlight Control



Quanta Computer Inc.
PROJECT : ZY9B
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CRT/LVDS/LID | 1A
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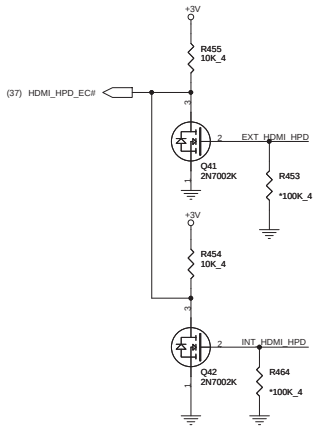
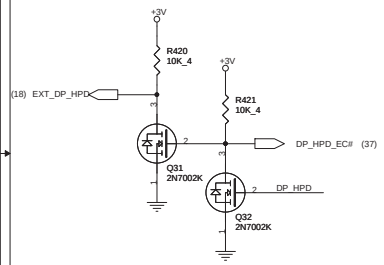
HDMI Hot-PLUG to EC and GPU

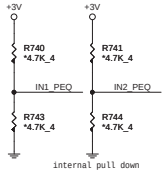


DP Hot-PLUG to EC and GPU

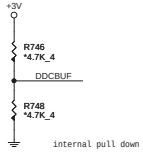


HDMI

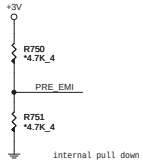
Input EQ setting	
INn_PEQ	Output
L	Middle EQ
H	High EQ
M	Low EQ



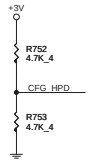
DDC Buffer setting	
DDC_BUF	Output
L	Passive DDC
H	Active Set-1
M	Active Set-2

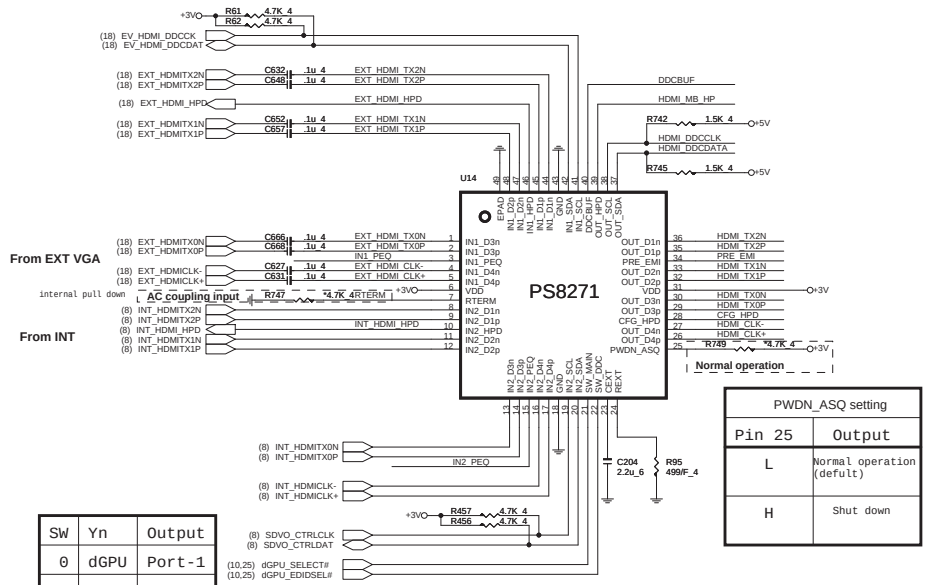


Pre-emphasis and EMI setting	
PRE_EMI	Output
L	No_PRE&EMI
H	PRE enable
M	EMI control



Hot-plug detect	
CFG_HPD	Output
L	Follow SW_MAIN
H	Follow SW_DDC
M	SW or DDC

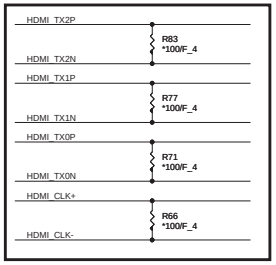




SW	Yn	Output
0	dGPU	Port-1
1	UMA	Port-2

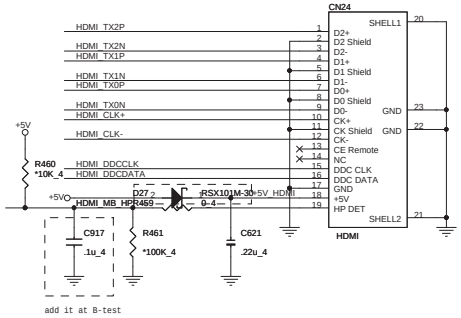
PWDN_ASQ setting	
Pin 25	Output
L	Normal operation (defult)
H	Shut down

EMI reserve for HDMI

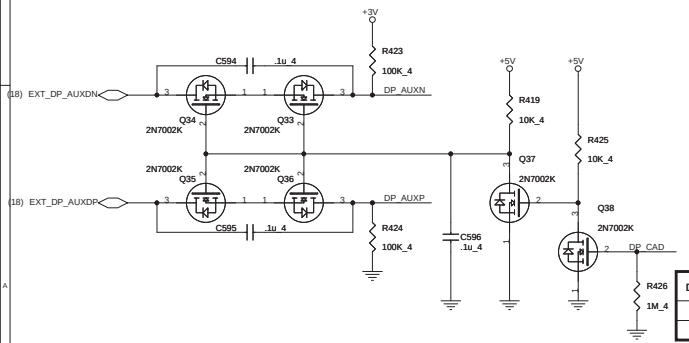


Close CN24

HDMI connector

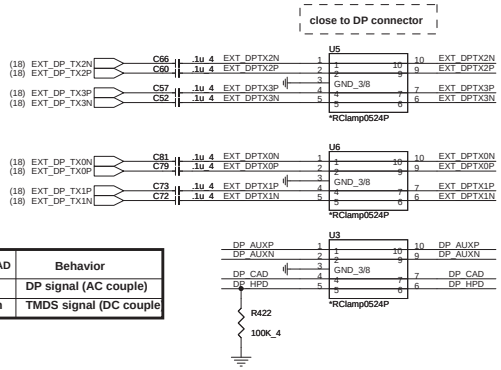


DisplayPort



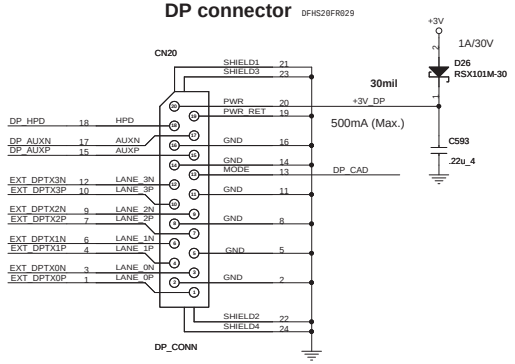
DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple

ESD Protect



DP connector

DFHS20FR029



Quanta Computer Inc.		
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	HDMI/DP	1A
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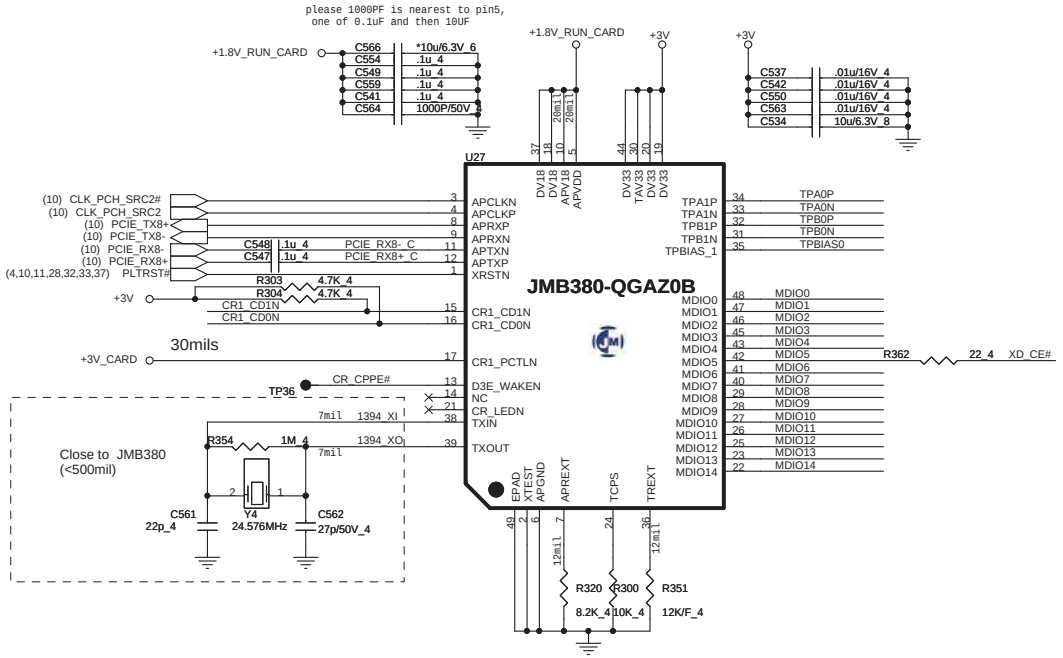
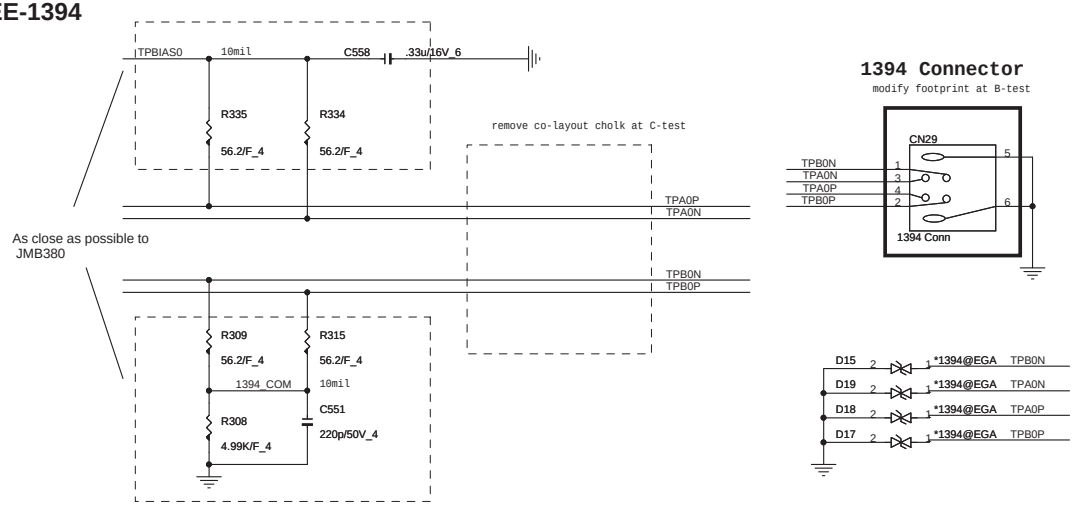
Cardreader/1394

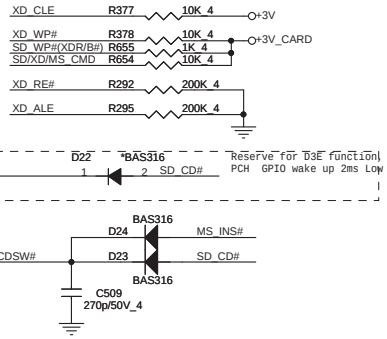


IEEE-1394



1394 Connector

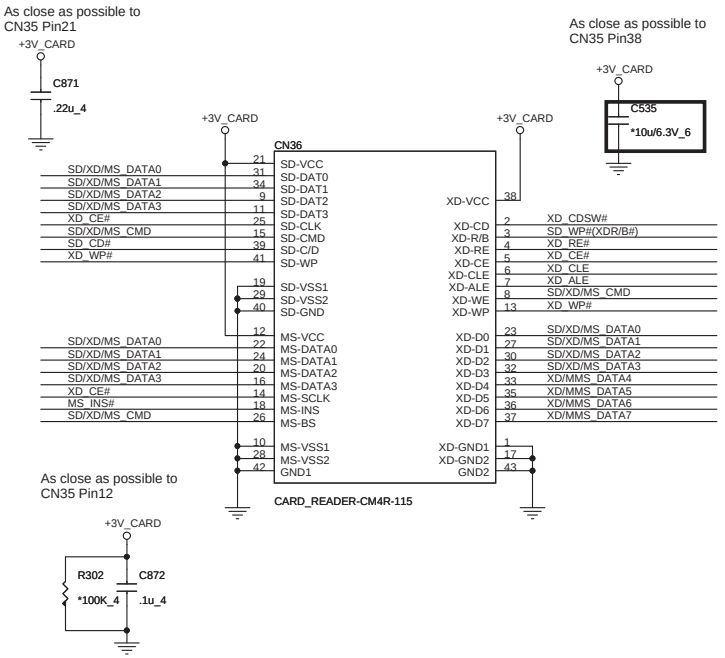
modify footprint at B-test



JMB 380 pin Note:

	SD/MMC	MS	XD
MDID0	SD_DAT0	MS_D0	XD_D0
MDID1	SD_DAT1	MS_D1	XD_D1
MDID2	SD_DAT2	MS_D2	XD_D2
MDID3	SD_DAT3	MS_D3	XD_D3
MDID4	SD_CMD	MS_BS	XD_WE#
MDID5	SD_CLK	MS_SCLK	XD_CE#
MDID6	SD_WP		XD_WP#
MDID7			XD_CLE
MDID8	SD_DAT4		XD_D4
MDID9	SD_DAT5		XD_D5
MDID10	SD_DAT6		XD_D6
MDID11	SD_DAT7		XD_D7
MDID12			XD_RE#
MDID13			XD_R/B#
MDID14			XD_ALE
CR1_LEDN	SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0	SD1_CD#		XD_CV#
CR1_CD1		MS1_CD#	XD_CD#

5 IN 1 CARD READER



EMI reserve

MDIO0	R651	0_4	SD/XD/MS_DATA0
MDIO1	R648	0_4	SD/XD/MS_DATA1
MDIO2	R652	0_4	SD/XD/MS_DATA2
MDIO3	R650	0_4	SD/XD/MS_DATA3
MDIO4	R653	0_4	SD/XD/MS_CMD
MDIO6	R361	0_4	XD_WP#
MDIO7	R360	0_4	XD_CLE
MDIO8	R649	0_4	XD/MMS_DATA4
MDIO9	R647	0_4	XD/MMS_DATA5
MDIO10	R646	0_4	XD/MMS_DATA6
MDIO11	R645	0_4	XD/MMS_DATA7
MDIO12	R299	0_4	XD_RE#
MDIO13	R656	0_4	SD_WP#(XDR/B#)
MDIO14	R301	0_4	XD_ALE
CR1_CD1N	R294	0_4	MS_INS#
CR1_CD0N	R293	0_4	SD_CD#

Quanta Computer Inc.

PROJECT : ZY9B

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	JMB380 Card Reader & 1394	1A

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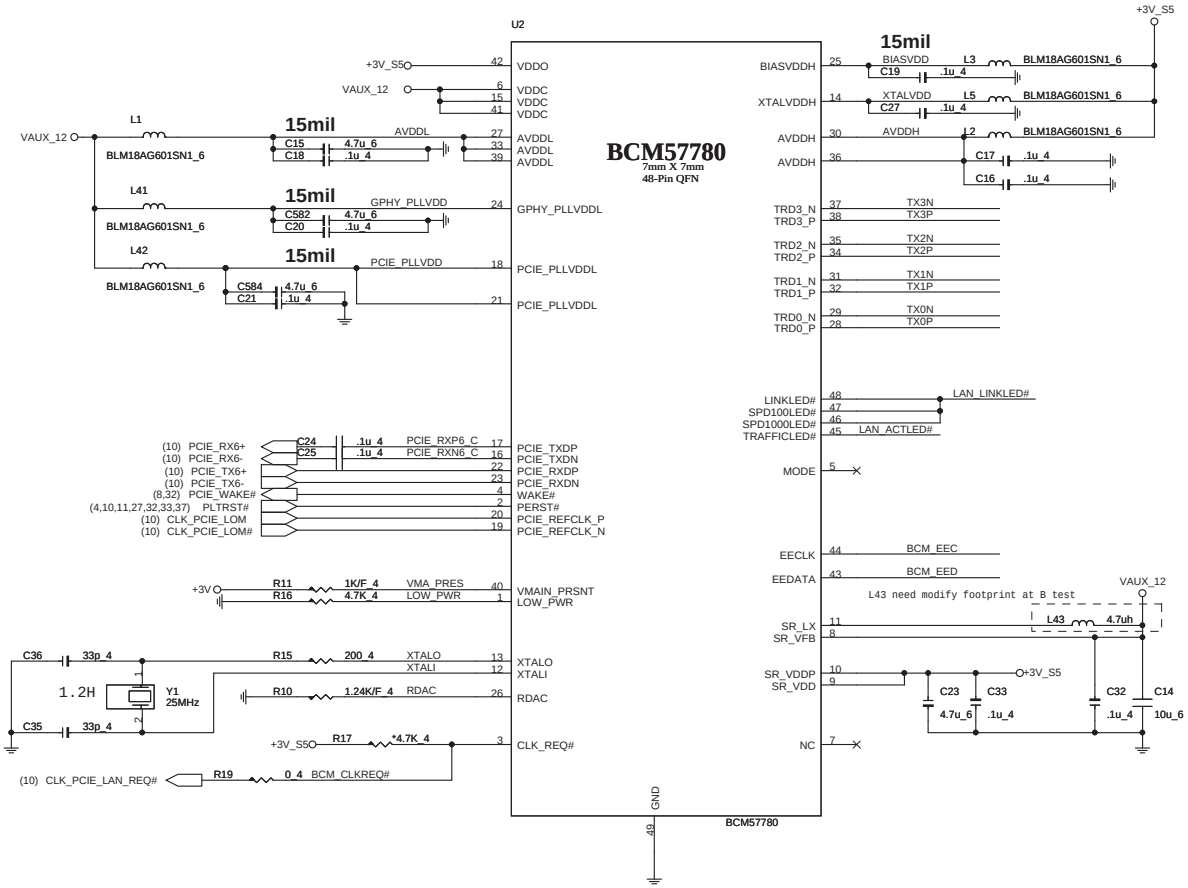
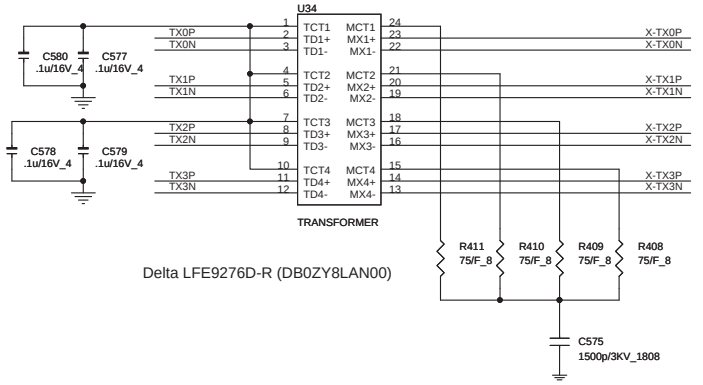
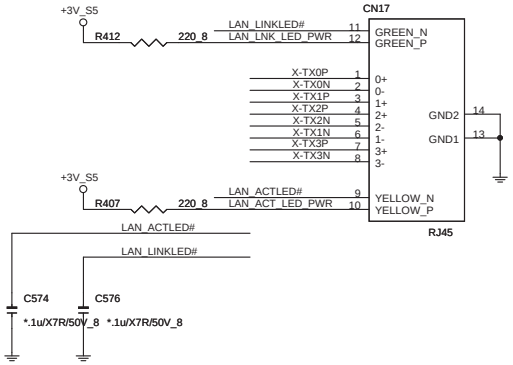
Giga-LAN BCM57780



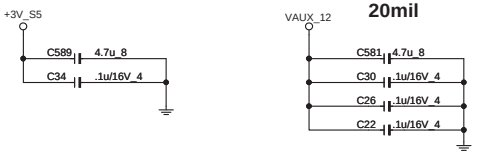
TRANSFORMER



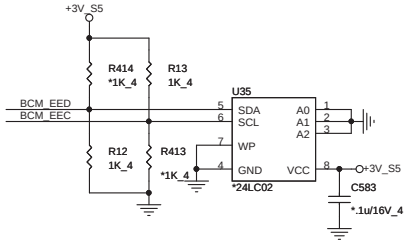
RJ45



LAN POWER



EEPROM



EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

Quanta Computer Inc.		
PROJECT : ZY9B		
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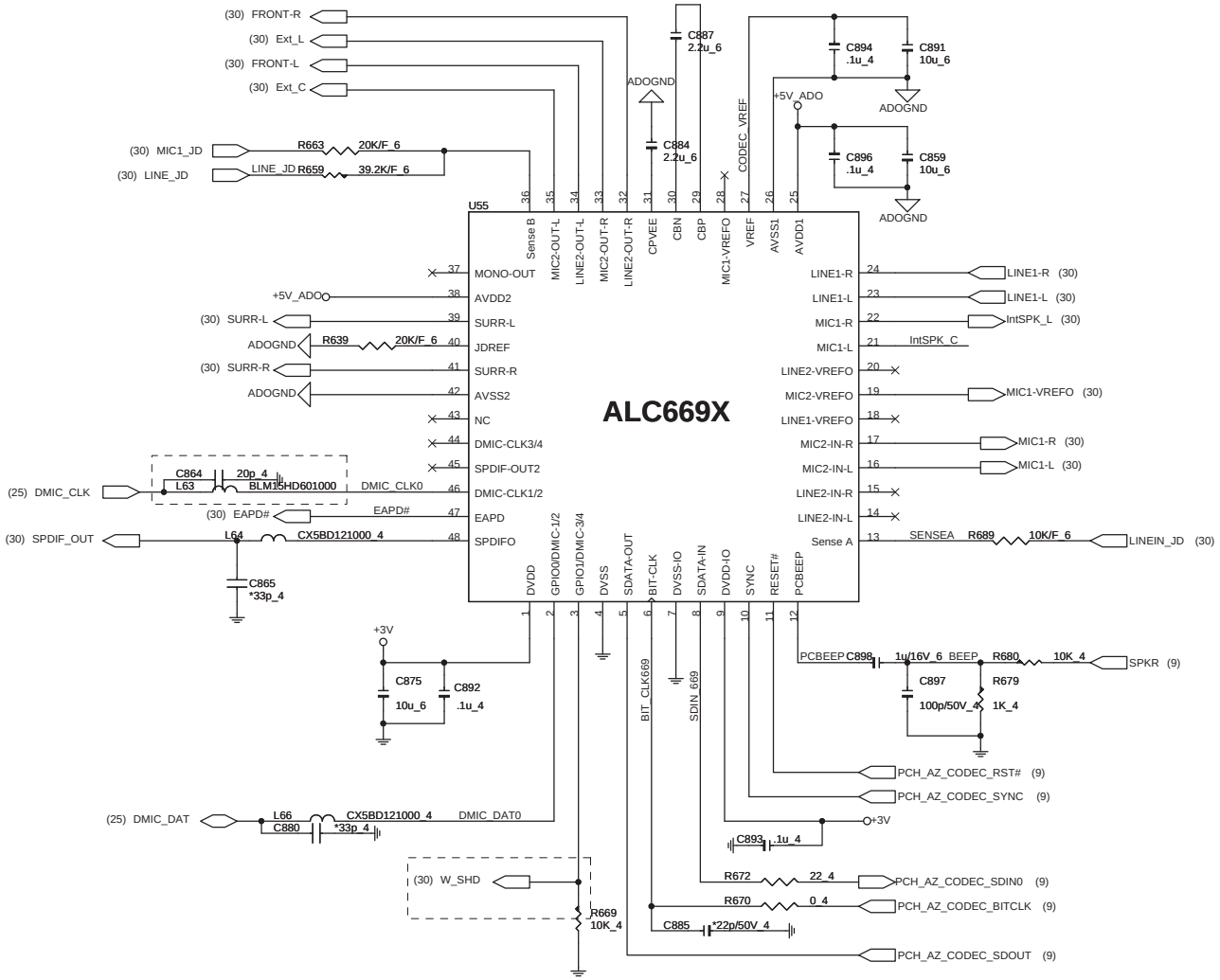
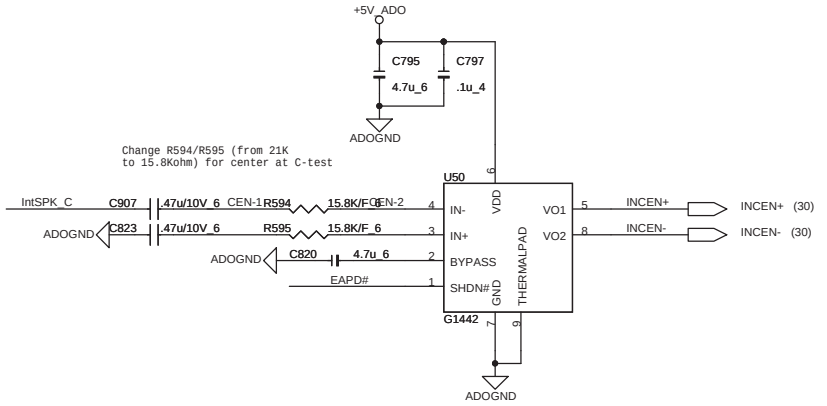
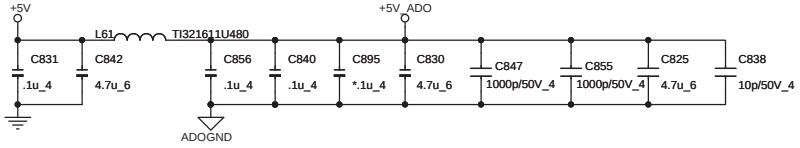
CODEC(ALC669X)



CENTER MONO



CODEC/AMP Power



Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	REALTEK ALC889X/MONO-AMP	1A
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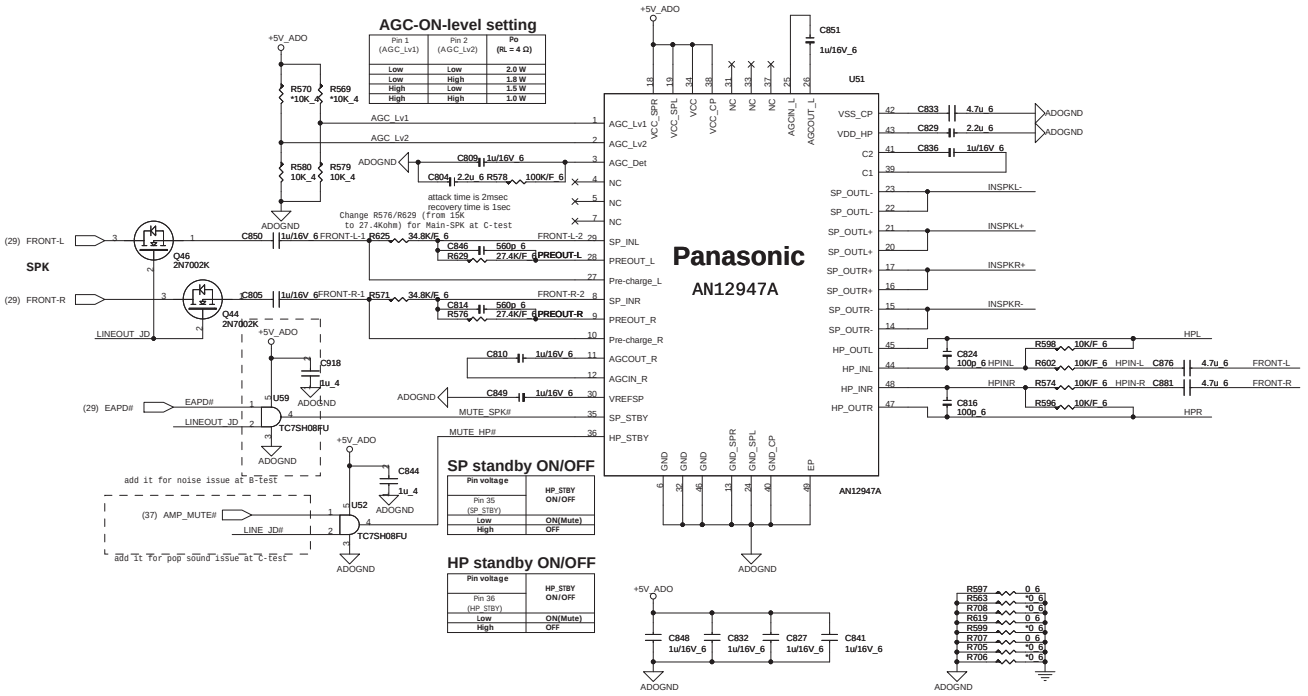
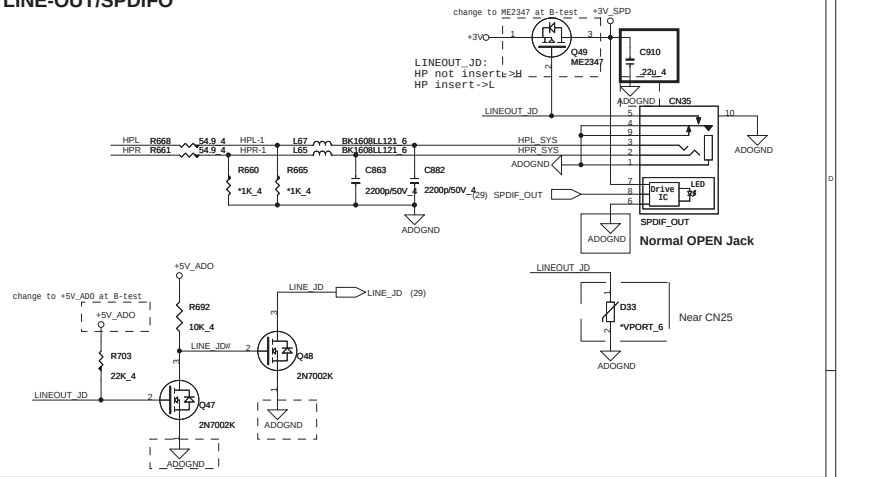
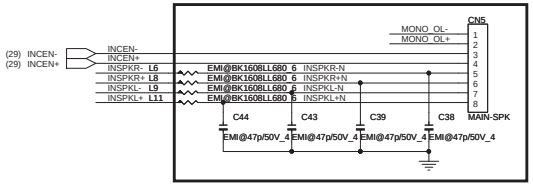
SPEAKER/HP AMP.



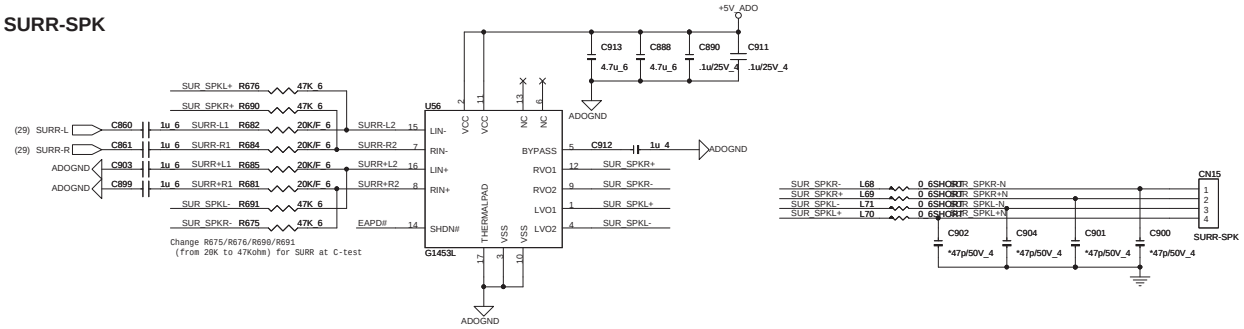
LINE-OUT/SPDIFO



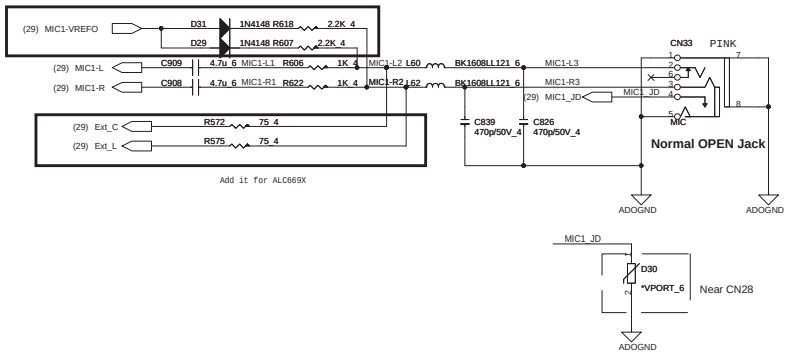
Main SPK/Center/Subwoofer EMI



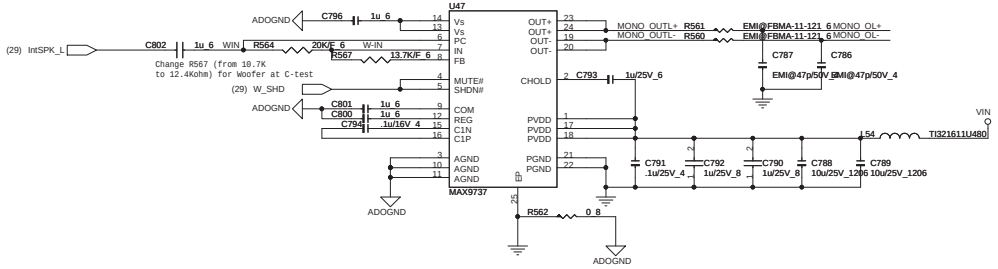
SURR-SPK



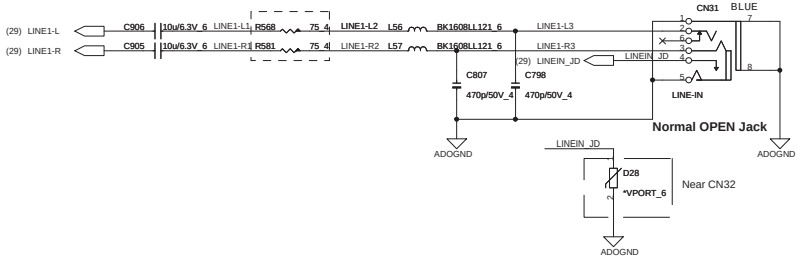
MIC



SUBWOOFER



LINE IN

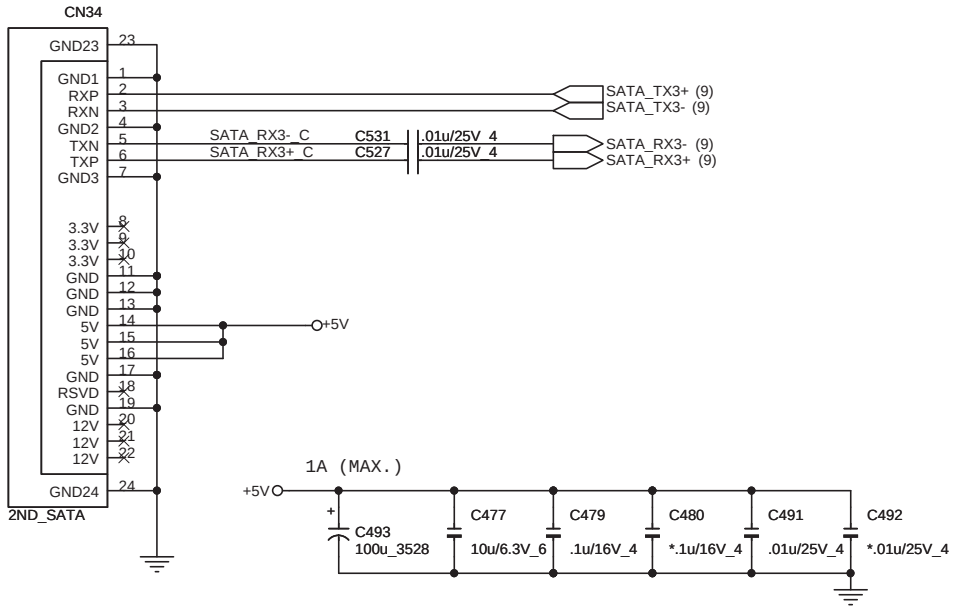


Quanta Computer Inc.
PROJECT : ZY9B

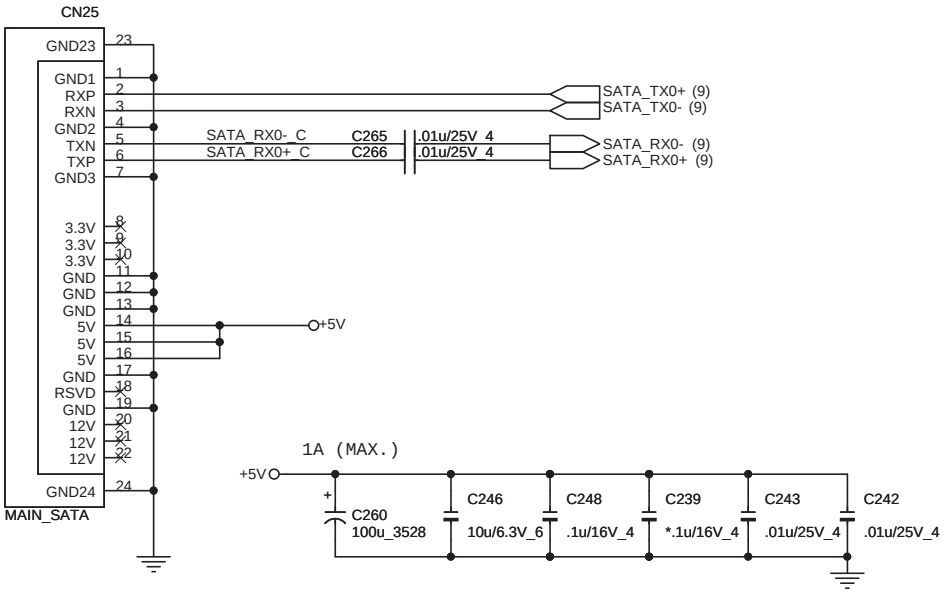
Size	Document Number	Rev
	AMP/AUDIO JACK/WOOFER	1A

Date: Thursday, September 17, 2009 Sheet 30 of 49

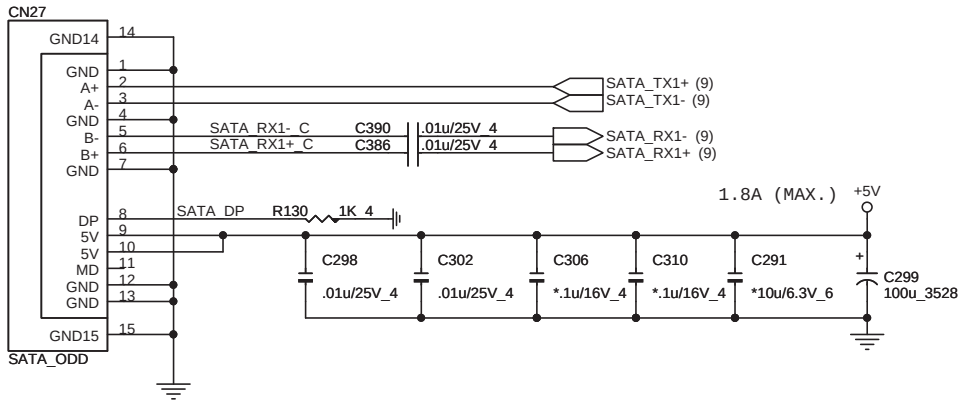
2nd SATA HDD (edge of board)



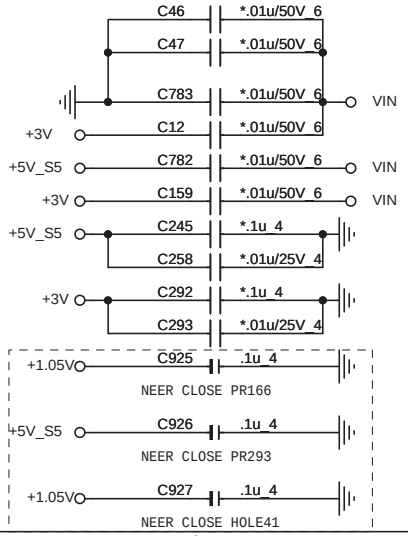
MAIN SATA HDD

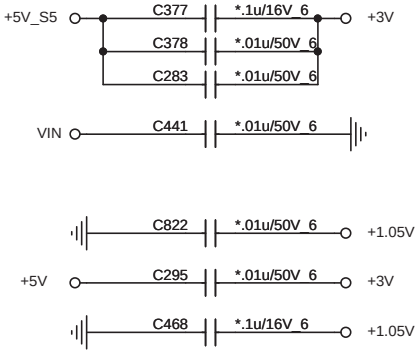


ODD (SATA)



EE RETURN-PATH CAPACITORS





Quanta Computer Inc.

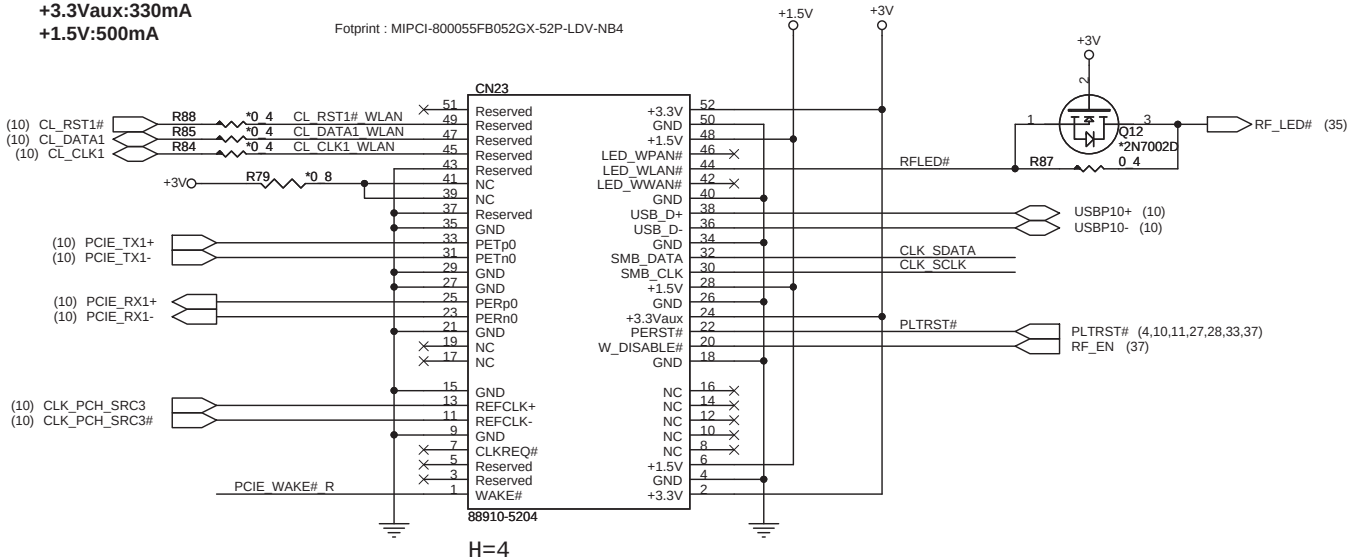
PROJECT : ZY9B

Size	Document Number	Rev
	SATA-HDD/ODD	1A
Date: Thursday, September 17, 2009	Sheet 31 of 49	

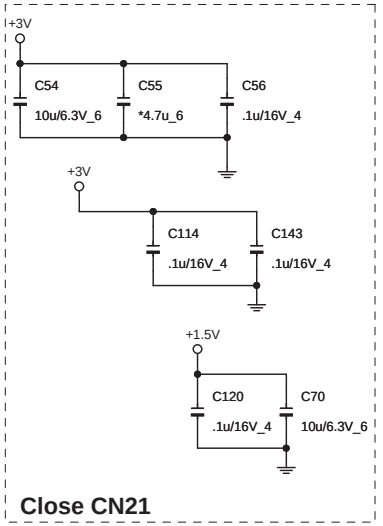
Wireless

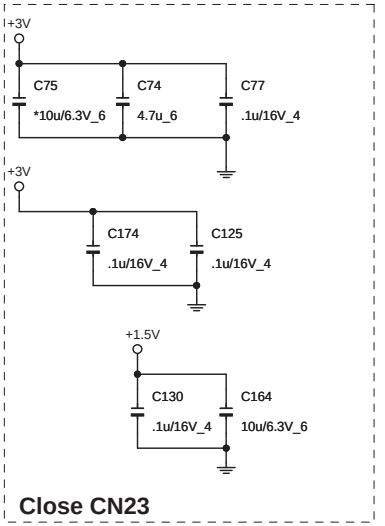
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4

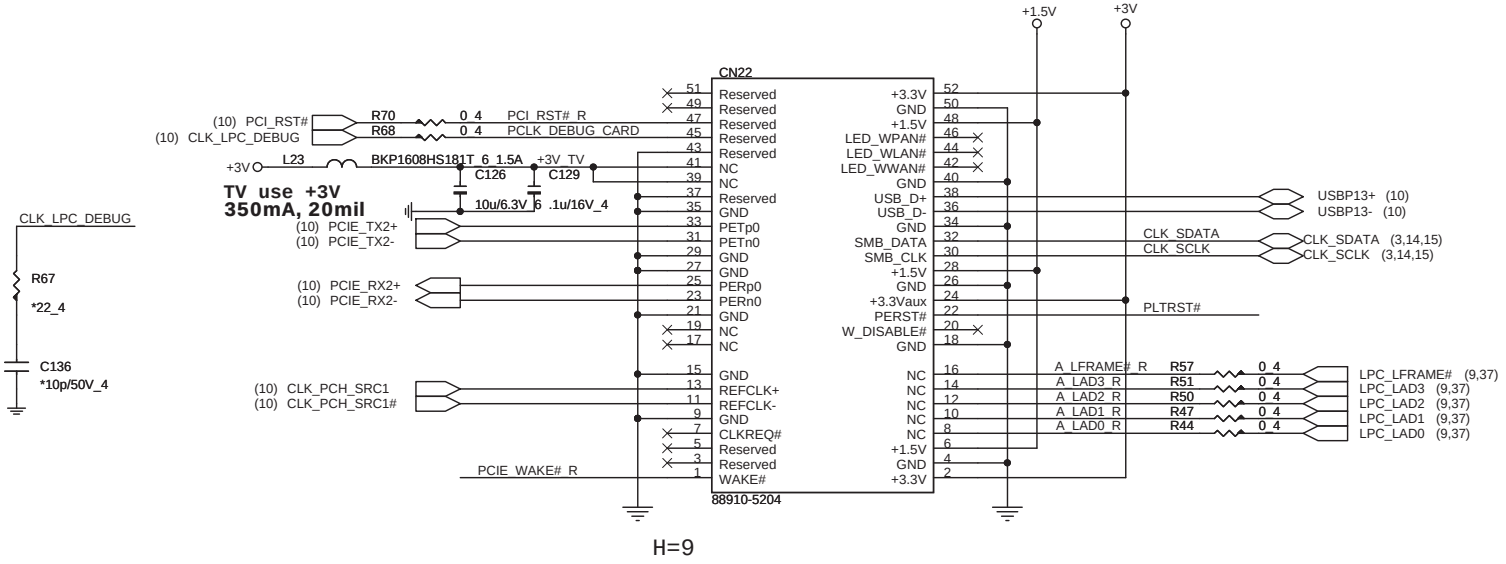


H=4

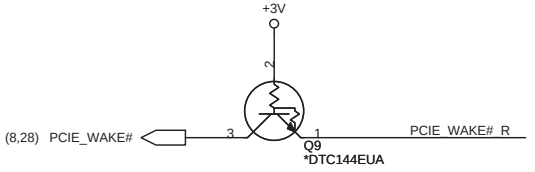




TV and Debug



H=9



Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	MINI PCI-E card/TV	1A
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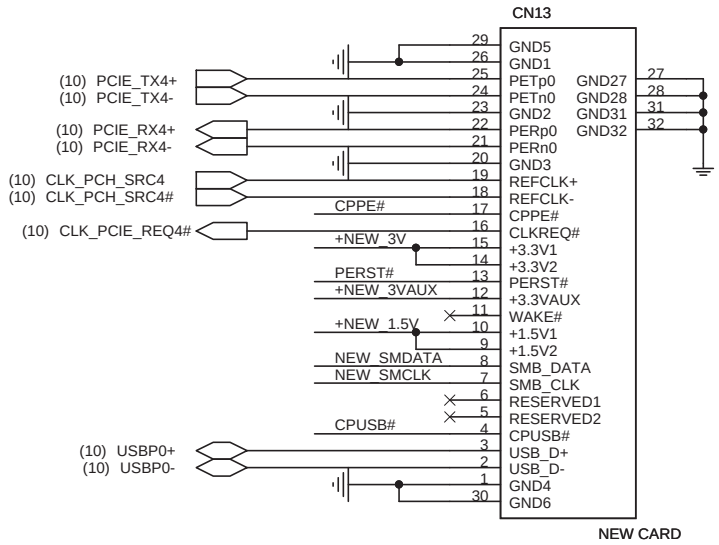
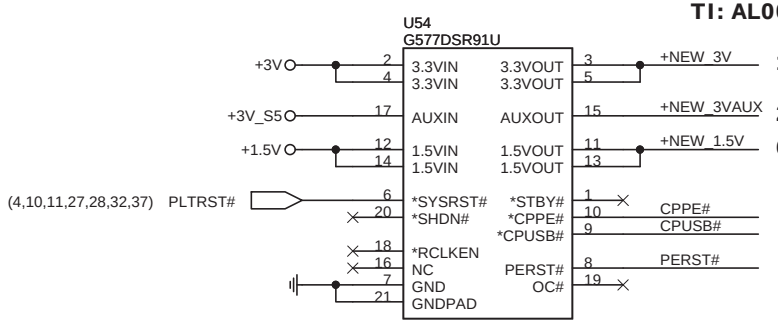
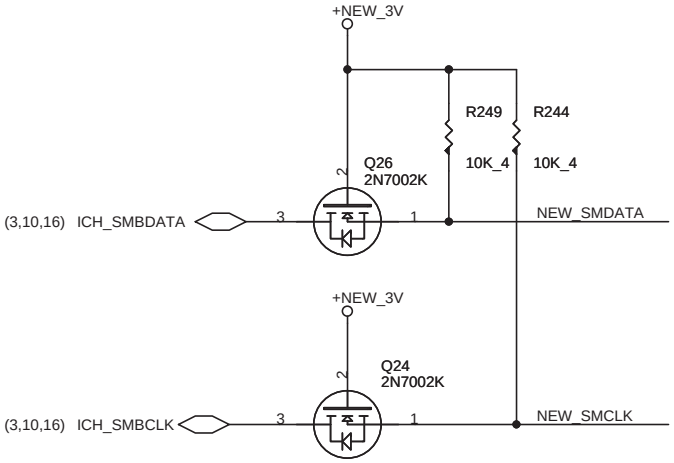
NEW CARD

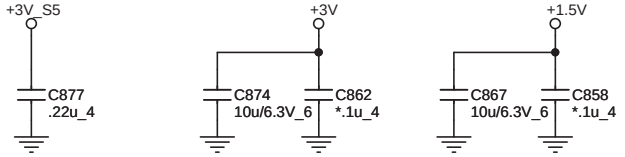


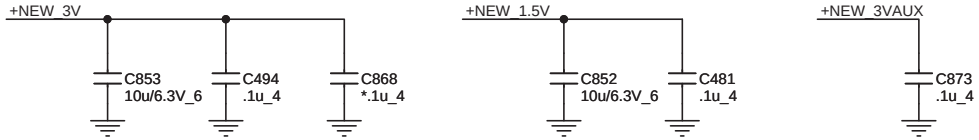
NEW CARD'S POWER SWITCH **GMT: AL000577002**

TI: AL002231000









Quanta Computer Inc.

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Size	Document Number	Rev
	NEW CARD	1A
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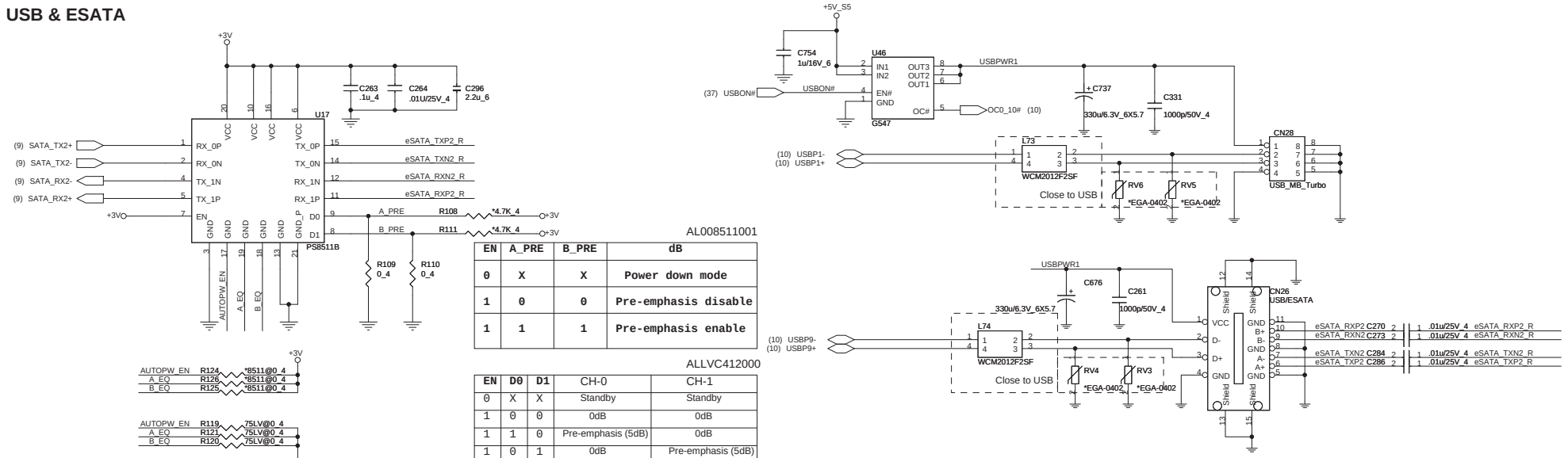
USB & ESATA



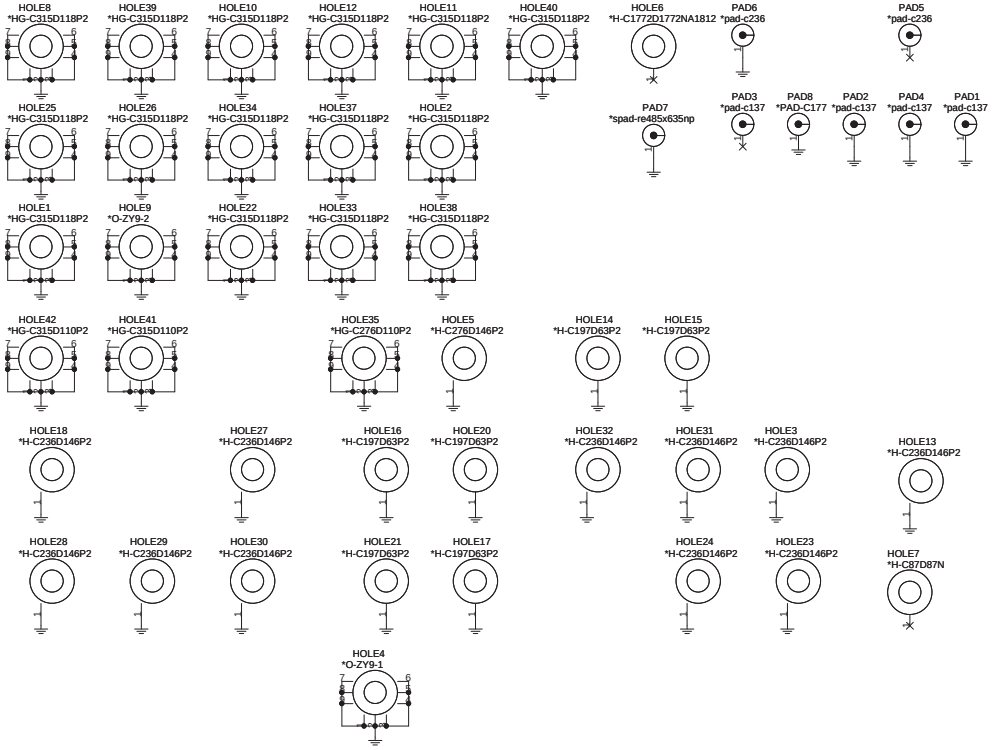
AL008511001

EN	A_PRE	B_PRE	dB
0	X	X	Power down mode
1	0	0	Pre-emphasis disable
1	1	1	Pre-emphasis enable

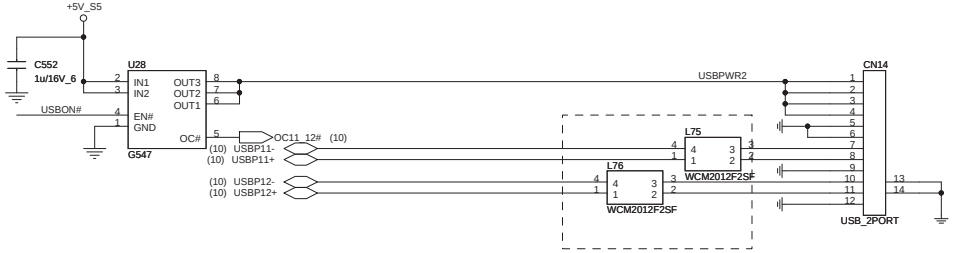
ALLVC412000

EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

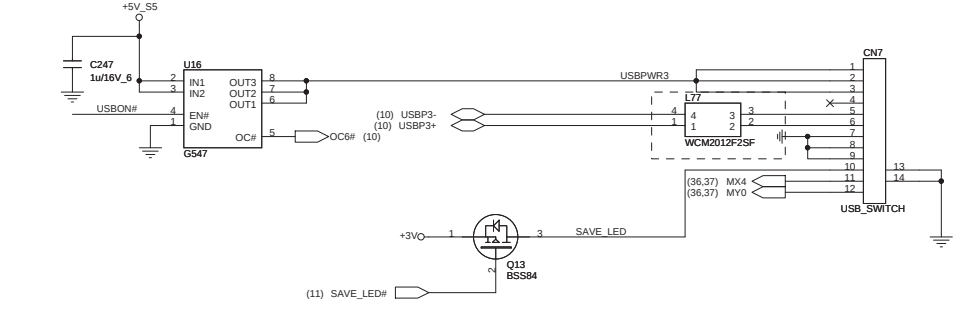
HOLES



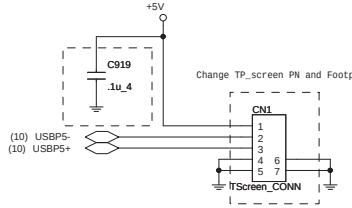
USB_2PORT/B



USB_SWITCH/B



TP_Screen



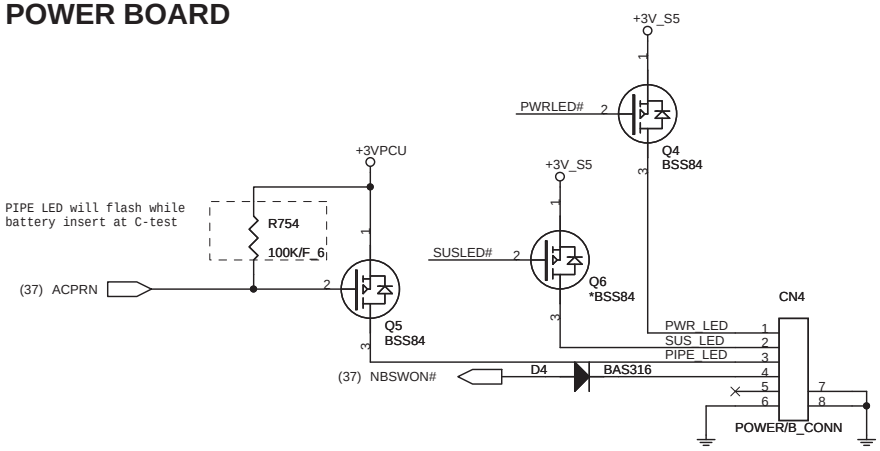
Quanta Computer Inc.

PROJECT : ZY9B

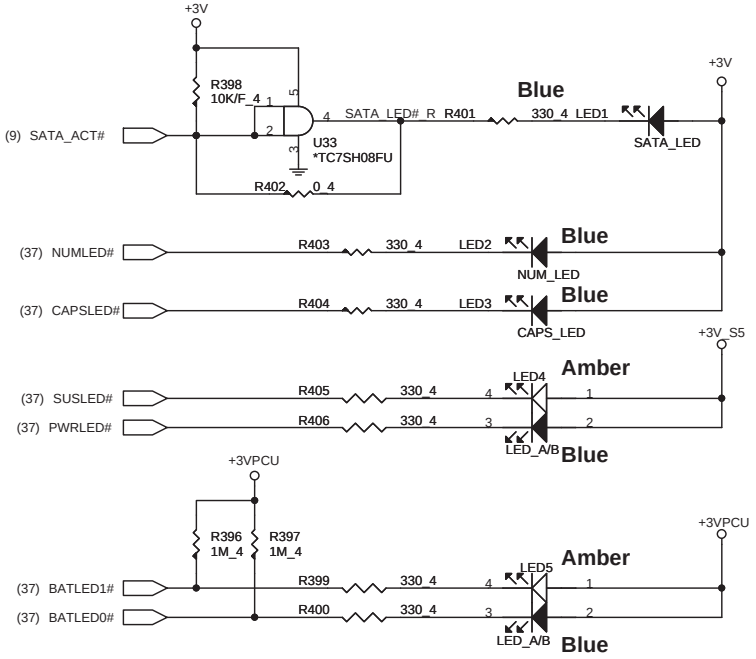
Size	Document Number	Rev
	USB/eSATA/TP_Screen	1A

Date: Thursday, September 17, 2009 Sheet 34 of 49

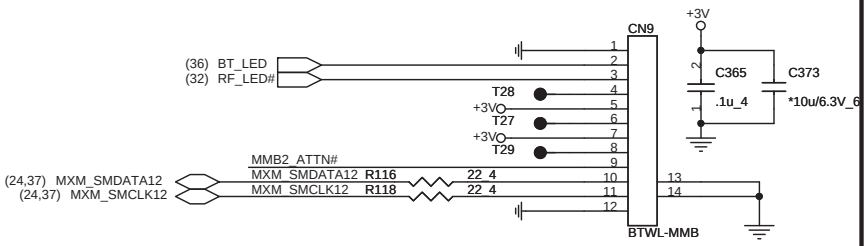
POWER BOARD



M/B LED

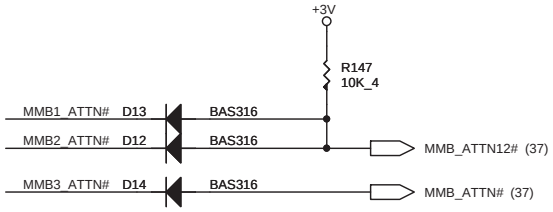


Left side MMB

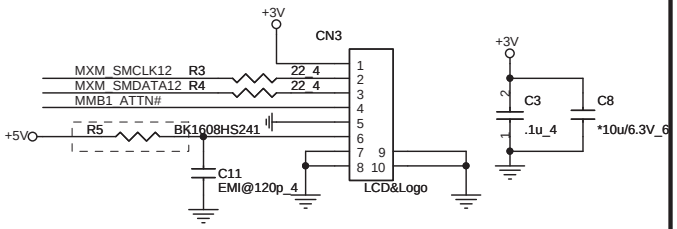


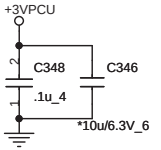
MXMCLK=MXM_SMCLK; MXMDATA=MXM_SMDATA12
MMB1 and MMB2 need add ISOLATE circuit where are on MXM page.

MMB Status

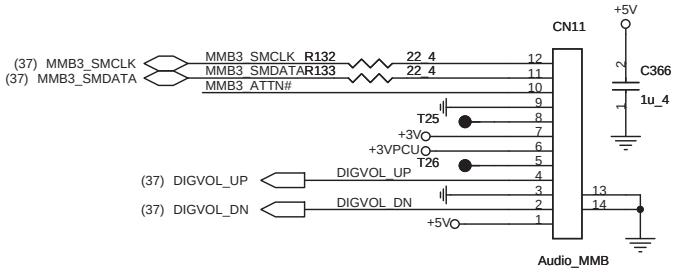


LCD BL_ON/OFF MMB & Backlight Logo LED





Right Side MMB



Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: POWER/MMB/LAUNCH/LED	Rev 1A
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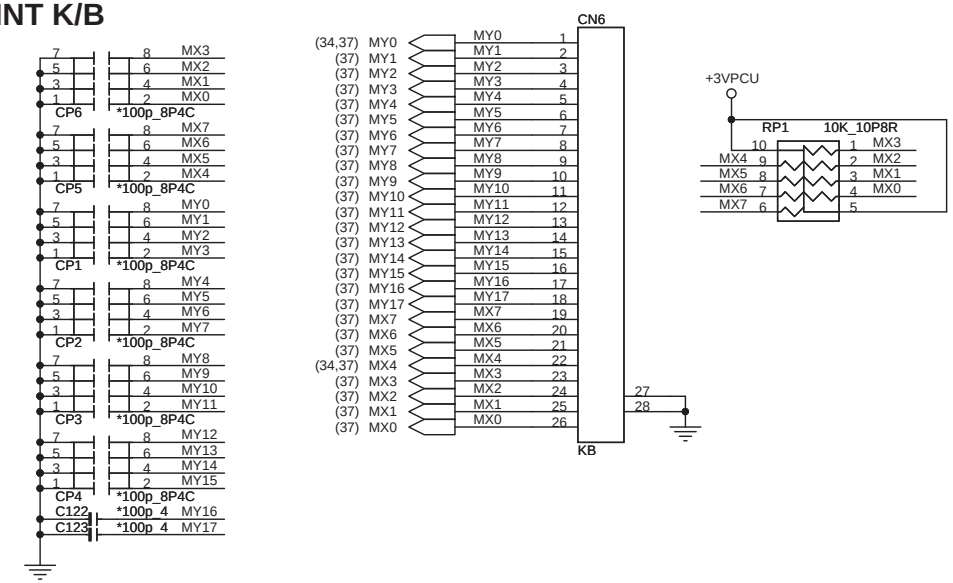
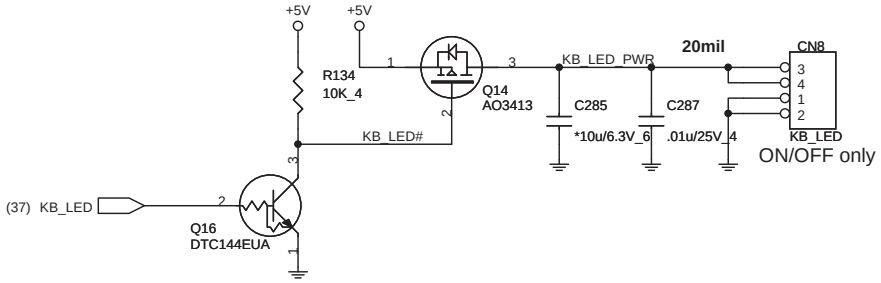
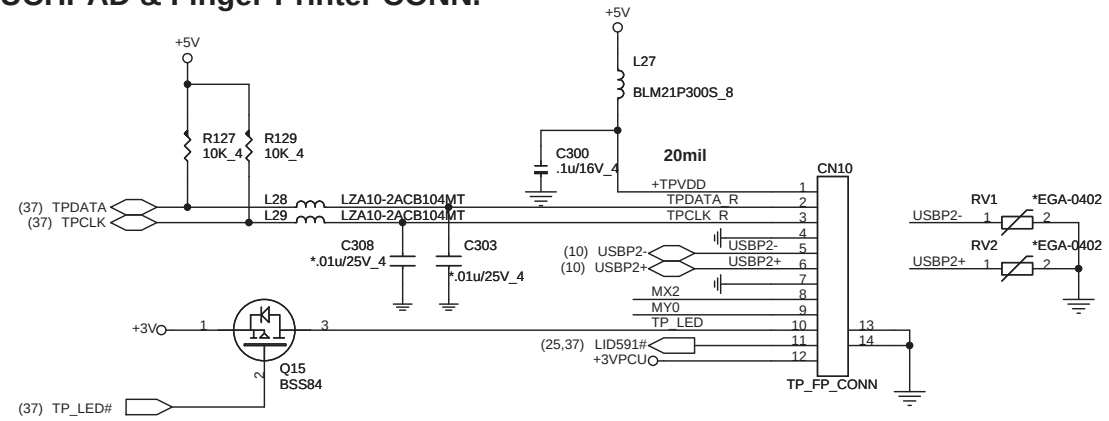
INT K/B



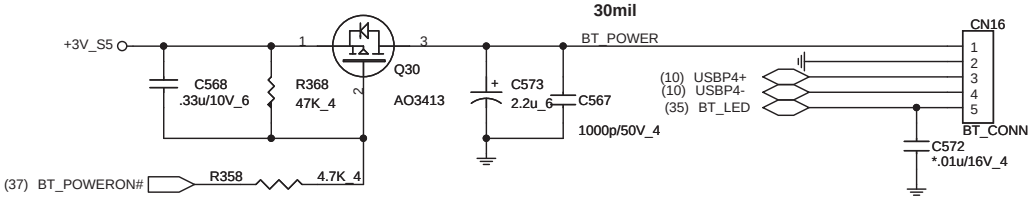
Keyboard LED control



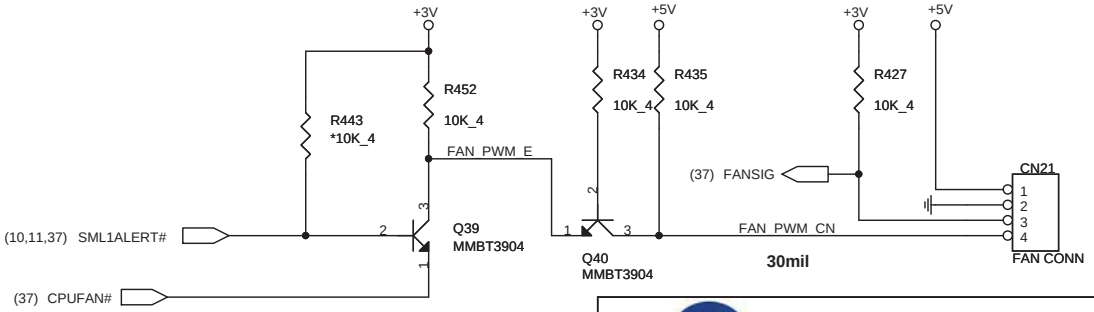
TOUCHPAD & Finger-Printer CONN.



BLUETOOTH CONNECTOR



CPU FAN



Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	KB/FAN/TP+FP/BT	1A

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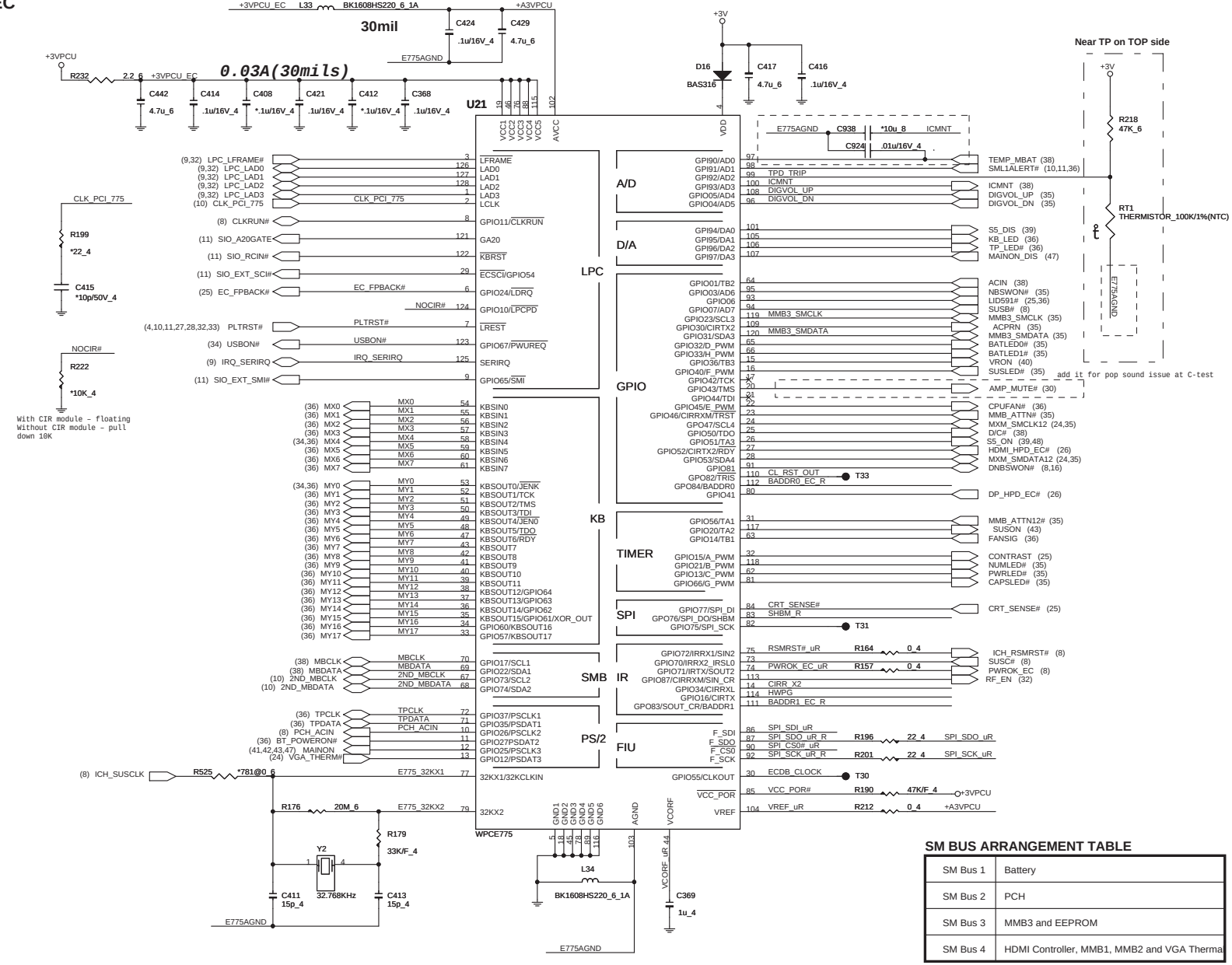
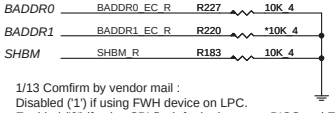
EC



I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

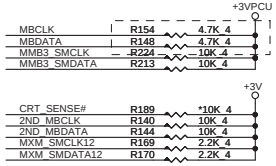
SHBM=0: Enable shared memory with host BIOS



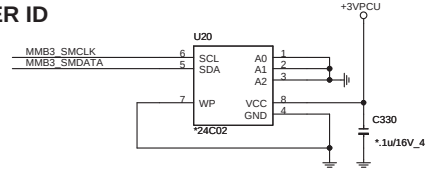
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU

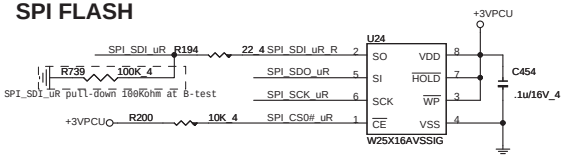
Change pull-up resistor (R148 /R154) from 10K to 4.7Kohm



ACER ID



SPI FLASH

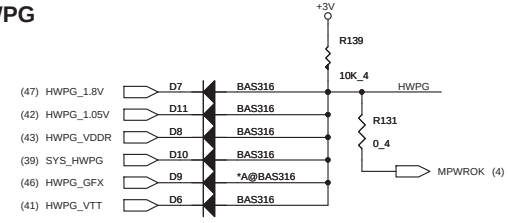


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add

Winbond	W25X16AVSSIG	AKE38ZP0N01
MXIC	MX25L1605AM2C-15G	AKE37FP0Z13
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

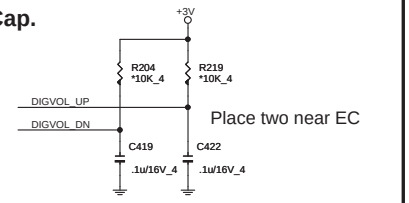
HWPG



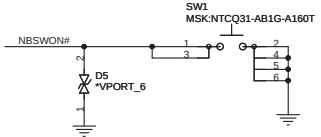
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Therma

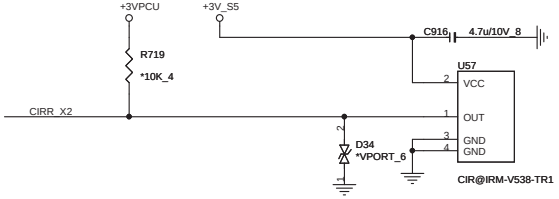
VR Cap.



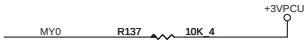
POWER-ON Switch



CIR



INTERNAL KEYBOARD STRIP SET



Quanta Computer Inc.
PROJECT : ZY9B

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A
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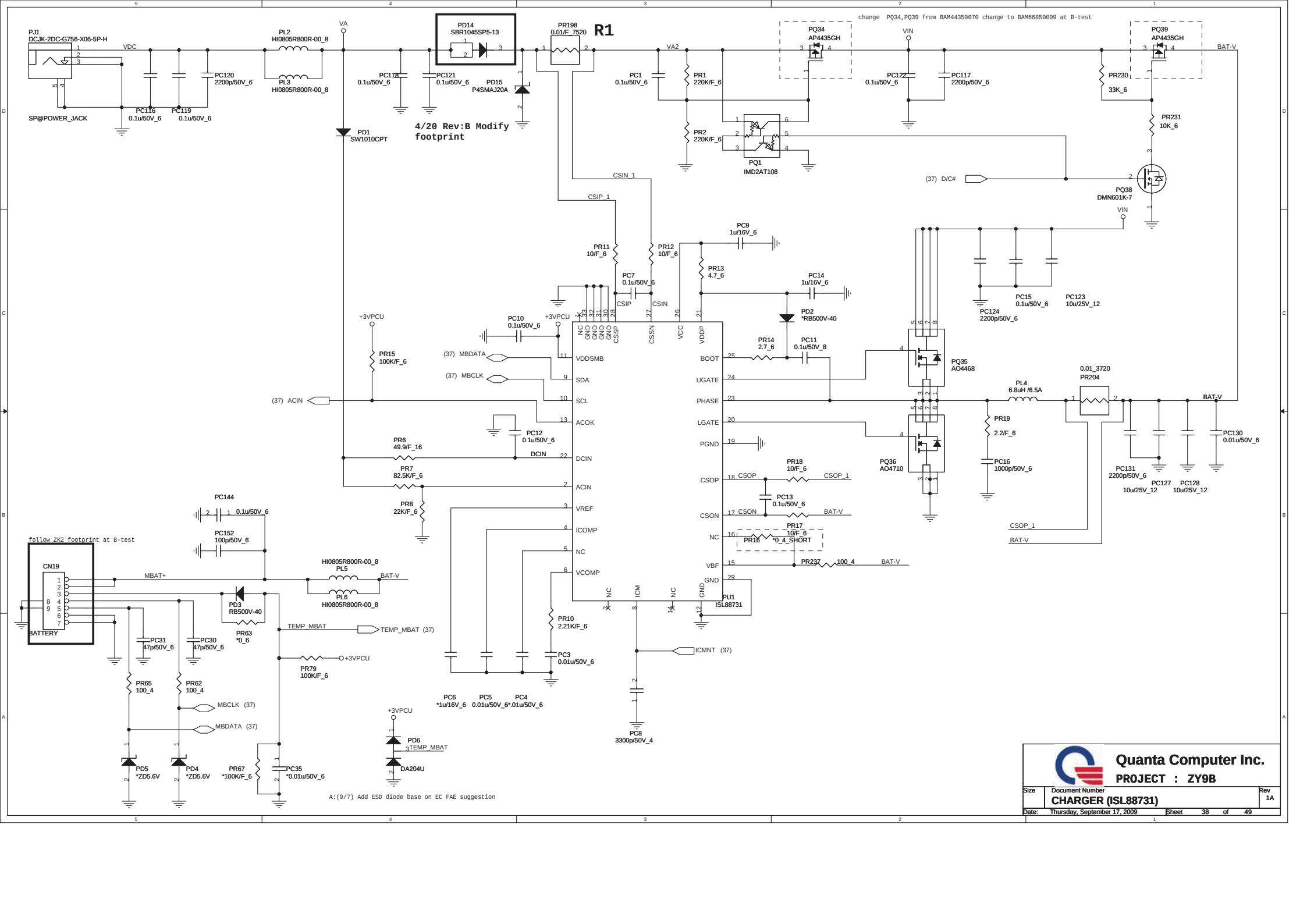
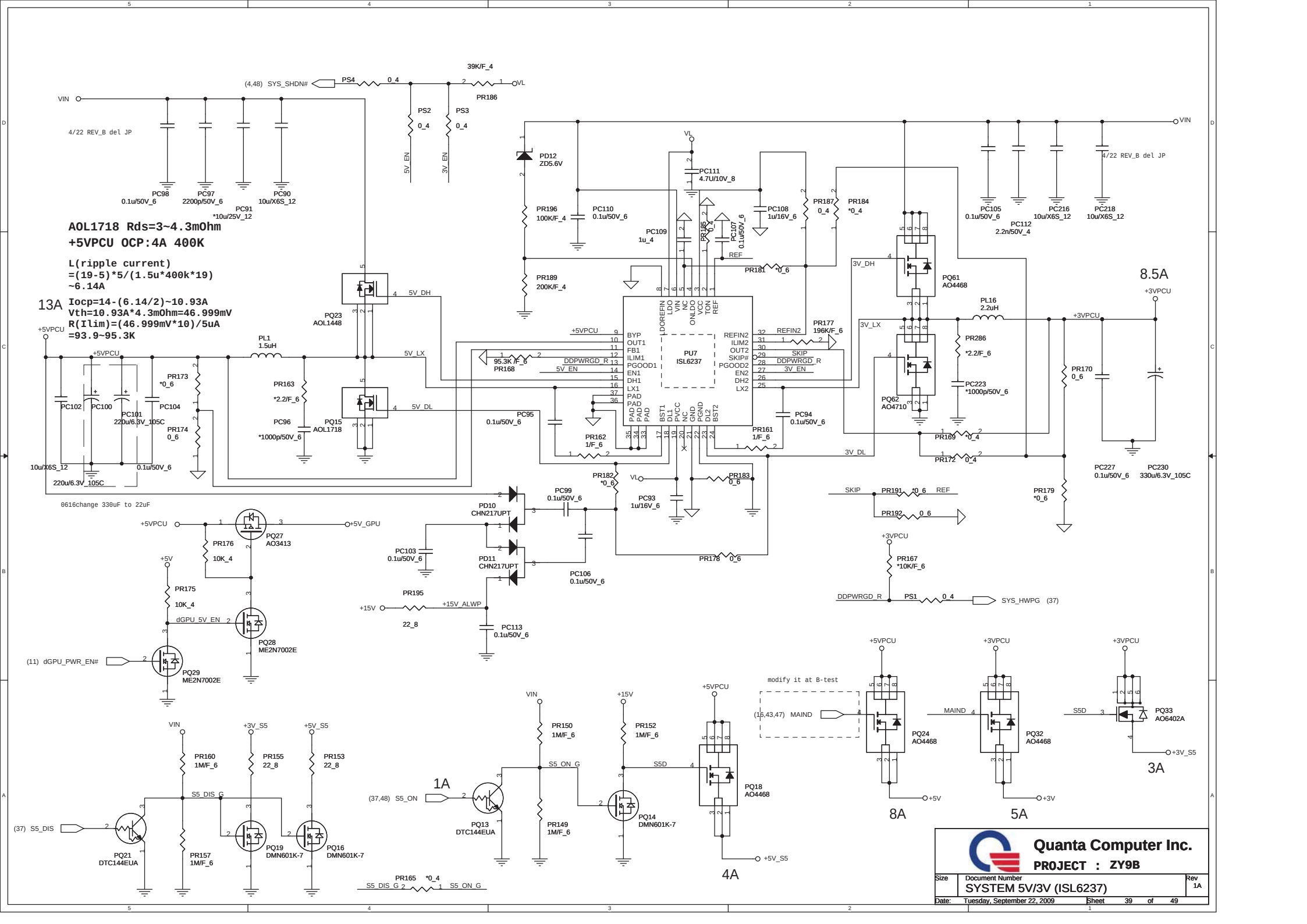
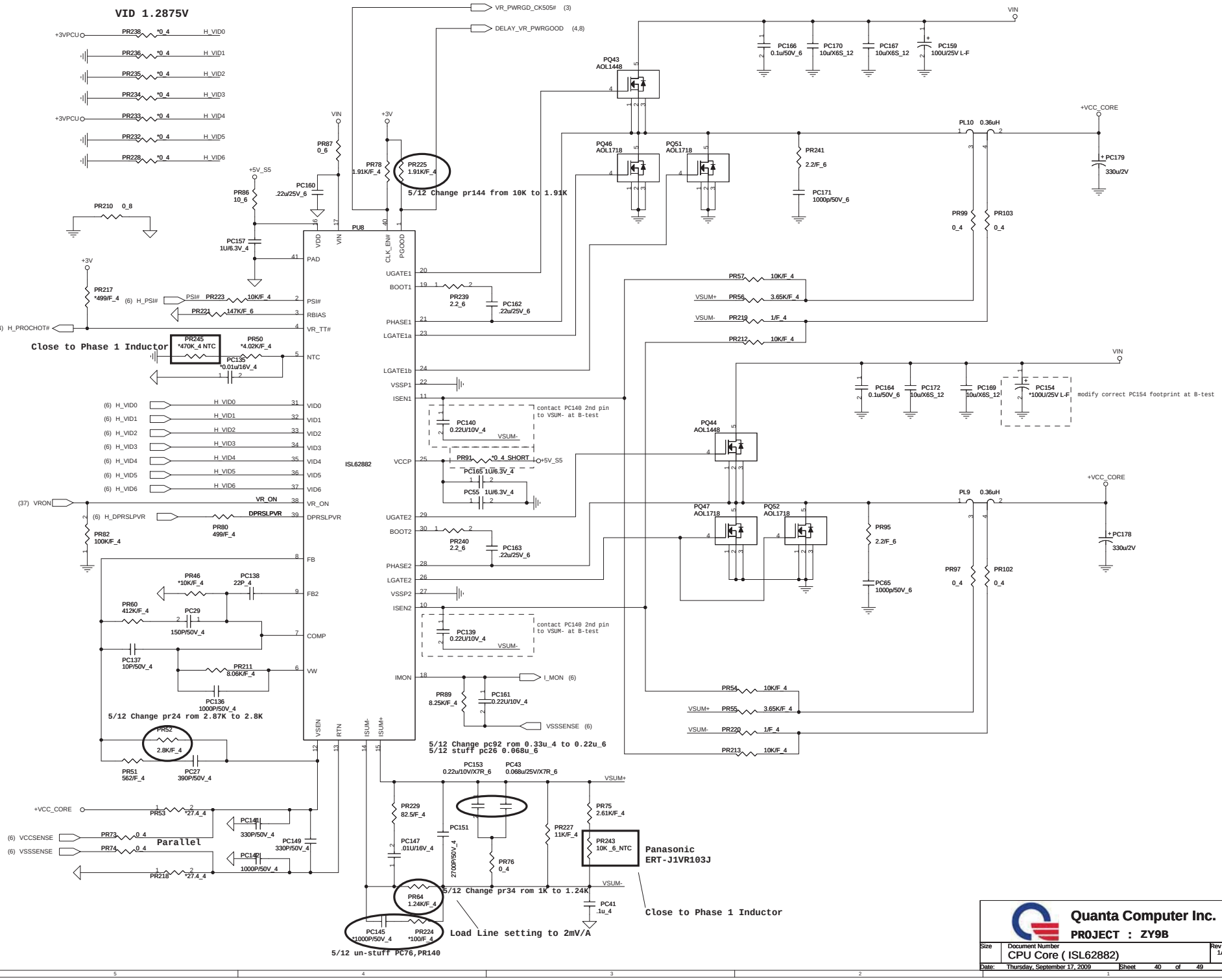

change PQ34,PQ39 from BAM44350070 change to BAM66850009 at B-test
R1
4/20 Rev:B Modify footprint
A:(9/7) Add ESD diode base on EC FAE suggestion
follow ZK2 footprint at B-test
PJ1
DCJK-2DC-G756-X06-5P-H
SP@POWER_JACK
PD1
SW1010CPT
PD14
SBR1045SP5-13
PD15
P4SMAJ20A
PL2
HI0805R800R-00_8
PL3
HI0805R800R-00_8
PR198
0.01/F_7520
PQ1
IMD2AT108
PQ34
AP4435GH
PQ39
AP4435GH
PQ38
DMN601K-7
PQ35
AO4468
PQ36
AO4710
PD2
*RB500-40
PD3
RB500-40
PD4
*ZD5.6V
PD5
*ZD5.6V
PD6
DA204U
PL4
6.8uH /6.5A
PL5
HI0805R800R-00_8
PL6
HI0805R800R-00_8
CN19
BATTERY
PU1
ISL88731
VDC
VA
VA2
VIN
BAT-V
MBAT+
+3VPCU
(37) D/C#
(37) MBDATA
(37) MBCLK
(37) ACIN
ICMNT (37)
TEMP_MBAT
TEMP_MBAT (37)
CSIN_1
CSIP_1
CSOP_1
BAT-V
DCIN
CSIP
CSIN
CSON
CSOP
PGND
VBF
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
GND
PC1 0.1u/50V_6
PC7 0.1u/50V_6
PC9 1u/16V_6
PC10 0.1u/50V_6
PC11 0.1u/50V_8
PC12 0.1u/50V_6
PC13 0.1u/50V_6
PC14 1u/16V_6
PC15 0.1u/50V_6
PC16 1000p/50V_6
PC3 0.01u/50V_6
PC4 *.01u/50V_6
PC5 0.01u/50V_6
PC6 *1u/16V_6
PC8 3300p/50V_4
PC30 47p/50V_6
PC31 47p/50V_6
PC35 *0.01u/50V_6
PC116 0.1u/50V_6
PC118 0.1u/50V_6
PC119 0.1u/50V_6
PC120 2200p/50V_6
PC121 0.1u/50V_6
PC122 0.1u/50V_6
PC123 10u/25V_12
PC124 2200p/50V_6
PC127 10u/25V_12
PC128 10u/25V_12
PC130 0.01u/50V_6
PC131 2200p/50V_6
PC144 0.1u/50V_6
PC152 100p/50V_6
PC117 2200p/50V_6
PR1 220K/F_6
PR2 220K/F_6
PR5 *0_4_SHORT
PR6 49.9/F_16
PR7 82.5K/F_6
PR8 22K/F_6
PR10 2.21K/F_6
PR11 10/F_6
PR12 10/F_6
PR13 4.7_6
PR14 2.7_6
PR15 100K/F_6
PR16 10/F_6
PR17 10/F_6
PR18 10/F_6
PR19 2.2/F_6
PR62 100_4
PR63 *0_6
PR65 100_4
PR67 *100K/F_6
PR79 100K/F_6
PR204 0.01_3720
PR230 33K_6
PR231 10K_6
PR237 100_4
Quanta Computer Inc.
PROJECT : ZY9B
Size
Document Number
CHARGER (ISL88731)
Rev
1A
Date: Thursday, September 17, 2009
Sheet 38 of 49

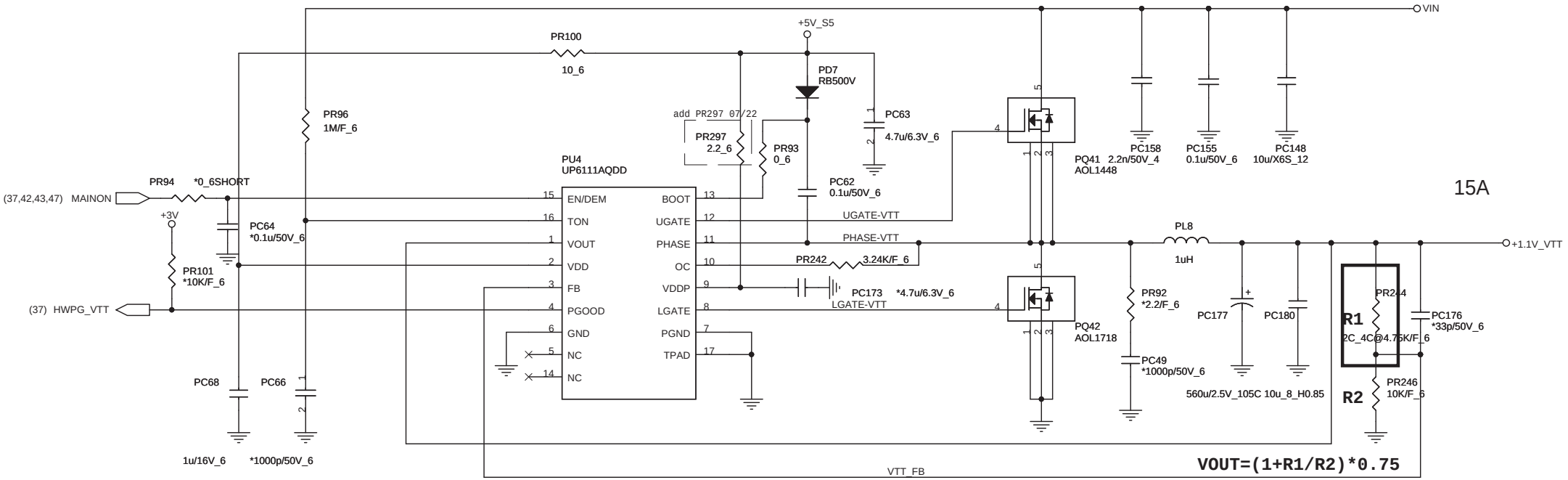

AOL1718 Rds=3~4.3mOhm
+5VPCU OCP:4A 400K
L(ripple current)
=(19-5)*5/(1.5u*400k*19)
~6.14A
13A
Iocp=14-(6.14/2)~10.93A
Vth=10.93A*4.3mOhm=46.999mV
R(Ilim)=(46.999mV*10)/5uA
=93.9~95.3K
8.5A
1A
8A
5A
4A
3A
PU7
ISL6237
PQ23 AOL1448
PQ15 AOL1718
PQ61 AO4468
PQ62 AO4710
PQ27 AO3413
PQ28 ME2N7002E
PQ29 ME2N7002E
PQ13 DTC144EUA
PQ14 DMN601K-7
PQ16 DMN601K-7
PQ18 AO4468
PQ19 DMN601K-7
PQ21 DTC144EUA
PQ24 AO4468
PQ32 AO4468
PQ33 AO6402A
PD10 CHN217UPT
PD11 CHN217UPT
PD12 ZD5.6V
PL1 1.5uH
PL16 2.2uH
VIN
+5VPCU
+3VPCU
+5V_GPU
+5V
+15V
VL
5V_DH
5V_LX
5V_DL
3V_DH
3V_LX
3V_DL
REF
REFIN2
SKIP
DDPWRGD_R
5V_EN
3V_EN
dGPU_5V_EN
dGPU_PWR_EN#
S5_DIS_G
S5_ON_G
S5D
+15V_ALWP
SYS_SHDN#
SYS_HWPG (37)
MAIND
modify it at B-test
0616change 330uF to 22uF
4/22 REV_B del JP
Quanta Computer Inc.
PROJECT : ZY9B
SYSTEM 5V/3V (ISL6237)
Size
Document Number
Rev 1A
Date: Tuesday, September 22, 2009
Sheet 39 of 49

[PWM]



Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: CPU Core (ISL62882)	Rev: 1A
Date: Thursday, September 17, 2009	Sheet 40 of 49	

[PWM]



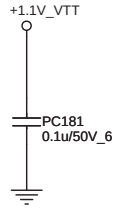
5/4
PR157 change to 4.75K

AO1718 Rdson=3~4.3mOhm

BOM change notice
Arrandale (1.05V) R1 = 4.02K (CS24023F928)
Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.64A

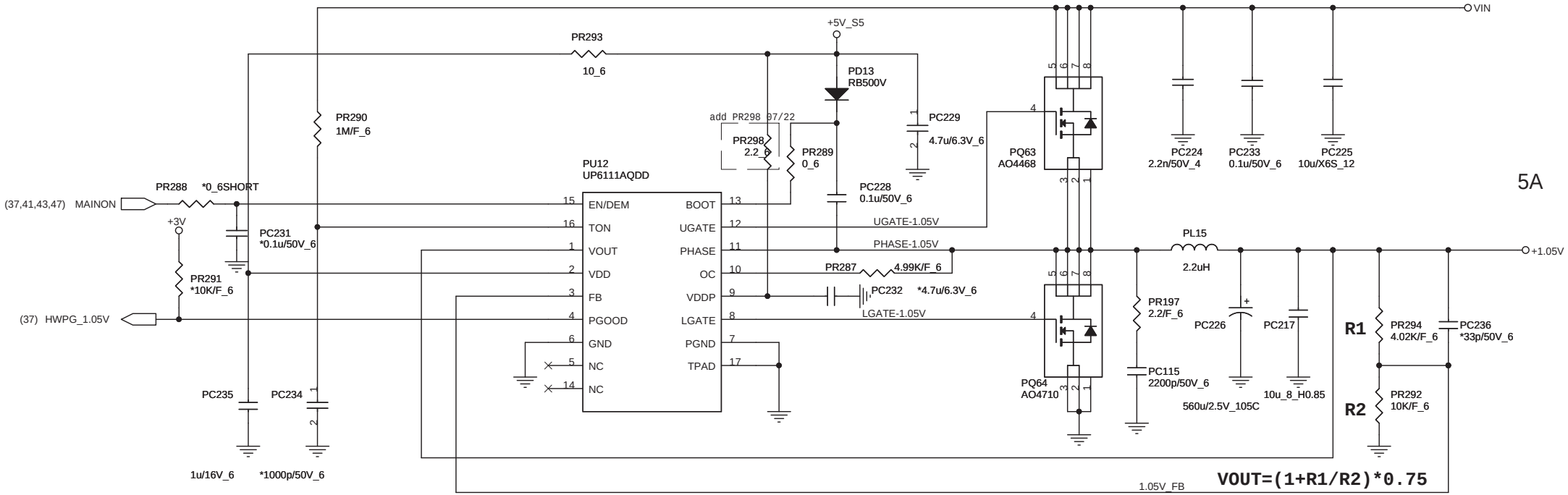
4.3m*15=RILIM*20uA
RILIM=3.24K(3.22K)



Quanta Computer Inc.
PROJECT : ZY9B

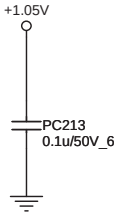
Size	Document Number	Rev
	+VTT (UP6111A)	1A
Date: Thursday, September 17, 2009	Sheet 41 of 49	

[PWM]



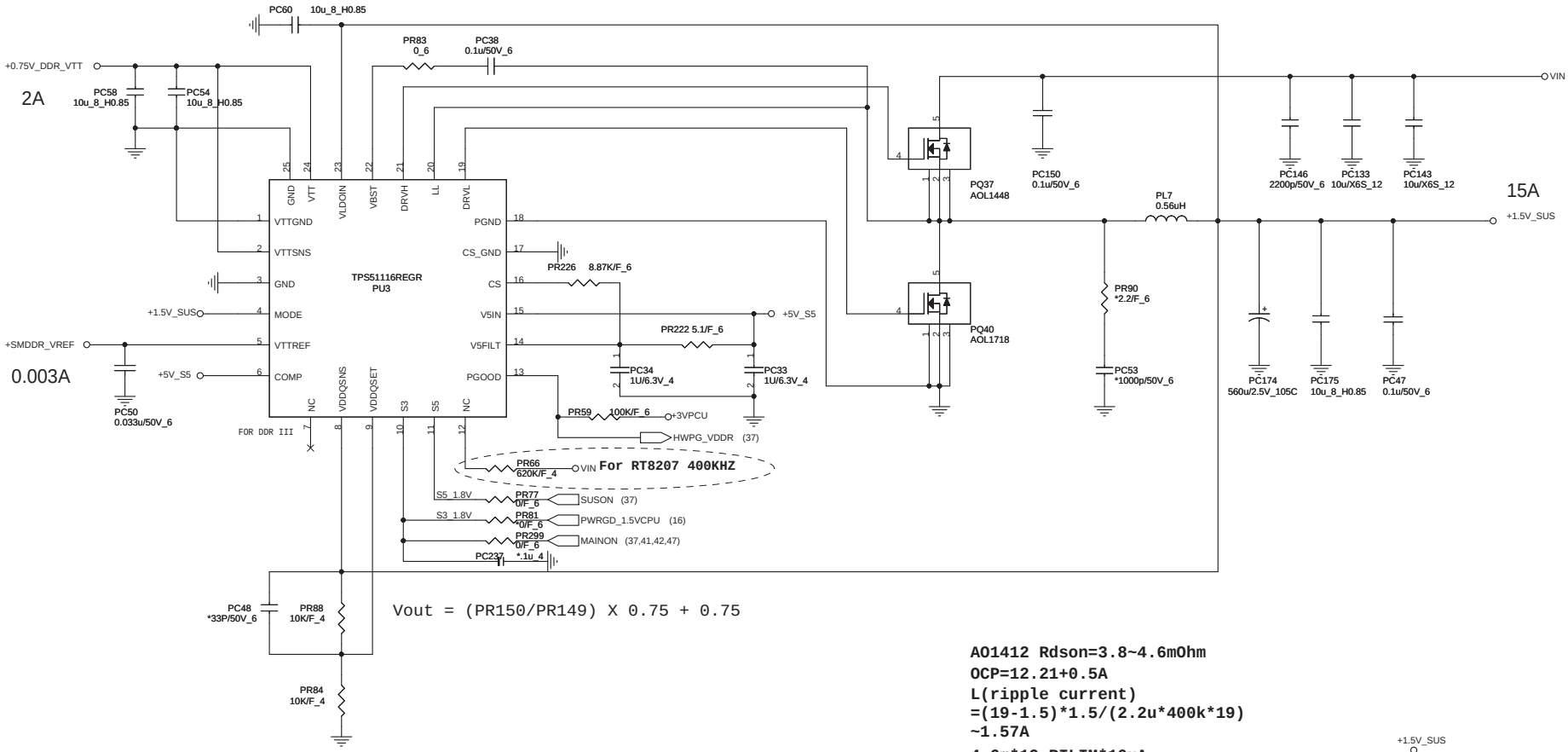
AO4710 Rdson=11.8~14.2mOhm
OCP=7.2-0.8A
L(ripple current)
=(19-1.05)*1.05/(2.2u*272k*19)
~1.6577A

14.2m*7=RILIM*20uA
RILIM=4.99K(4.97K)



Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: +1.05V(UP6111AQDD)	Rev: 1A
Date: Monday, September 21, 2009	Sheet 42 of 49	

[PWM]

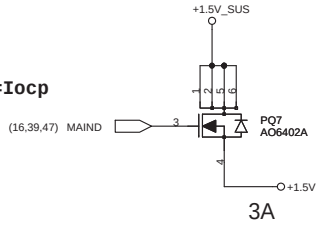


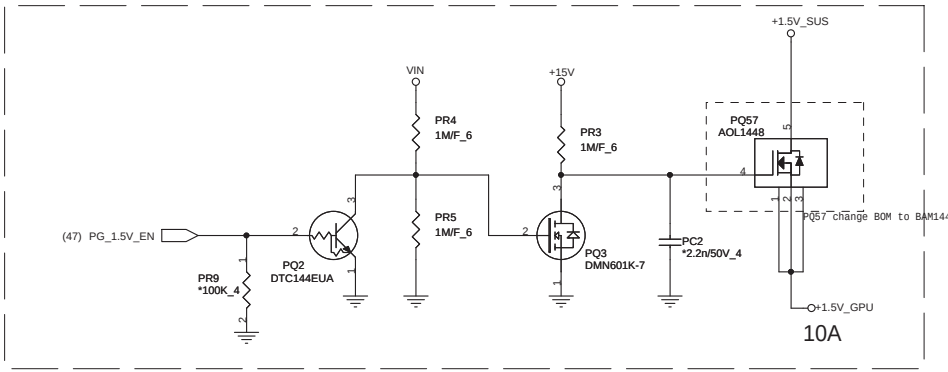
Vout = (PR150/PR149) X 0.75 + 0.75

AO1412 Rdson=3.8~4.6mOhm
OCP=12.21+0.5A
L(ripple current)
=(19-1.5)*1.5/(2.2u*400k*19)
~1.57A

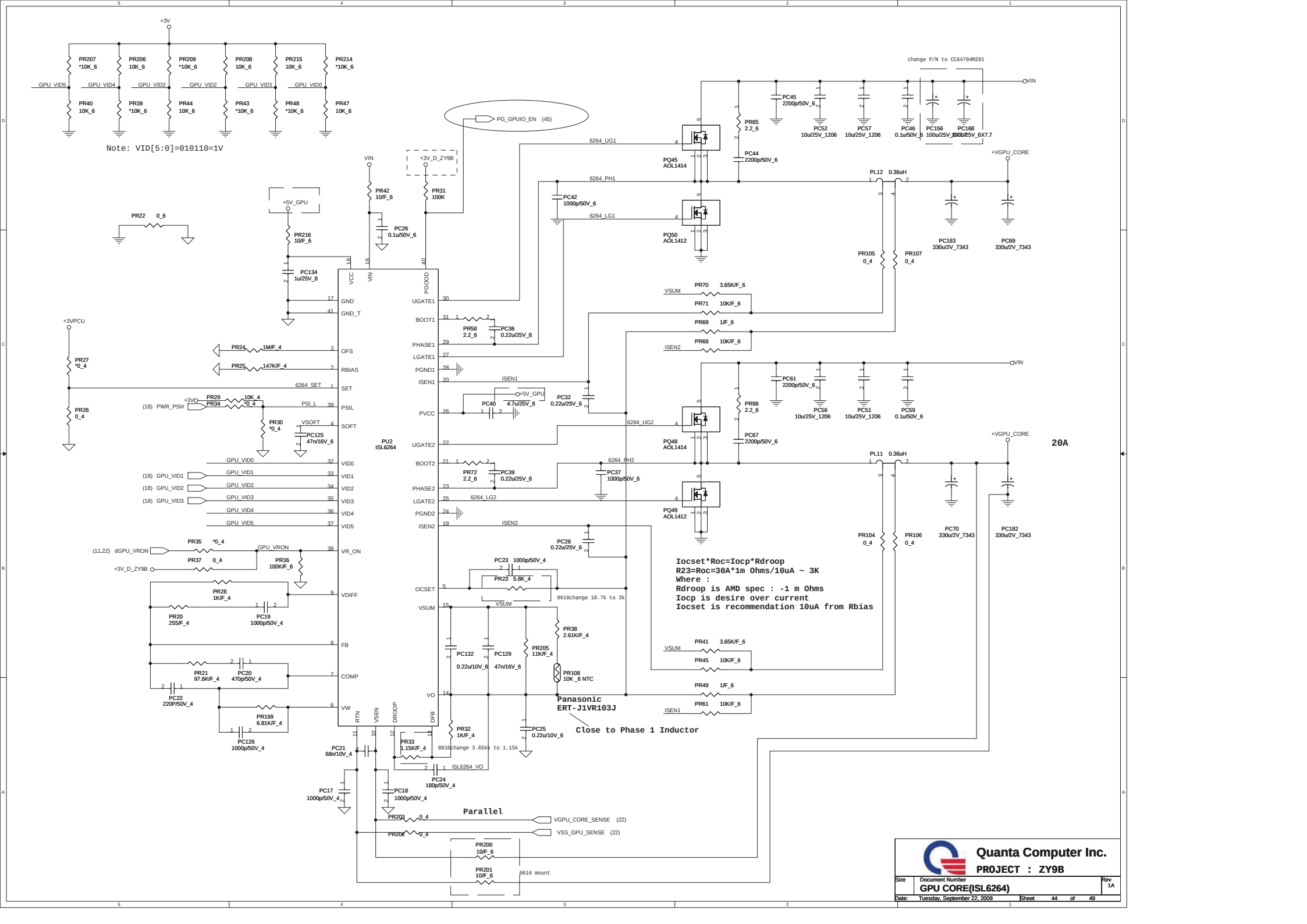
4.6m*19=RILIM*10uA
RILIM=8.74K --- 8.87K

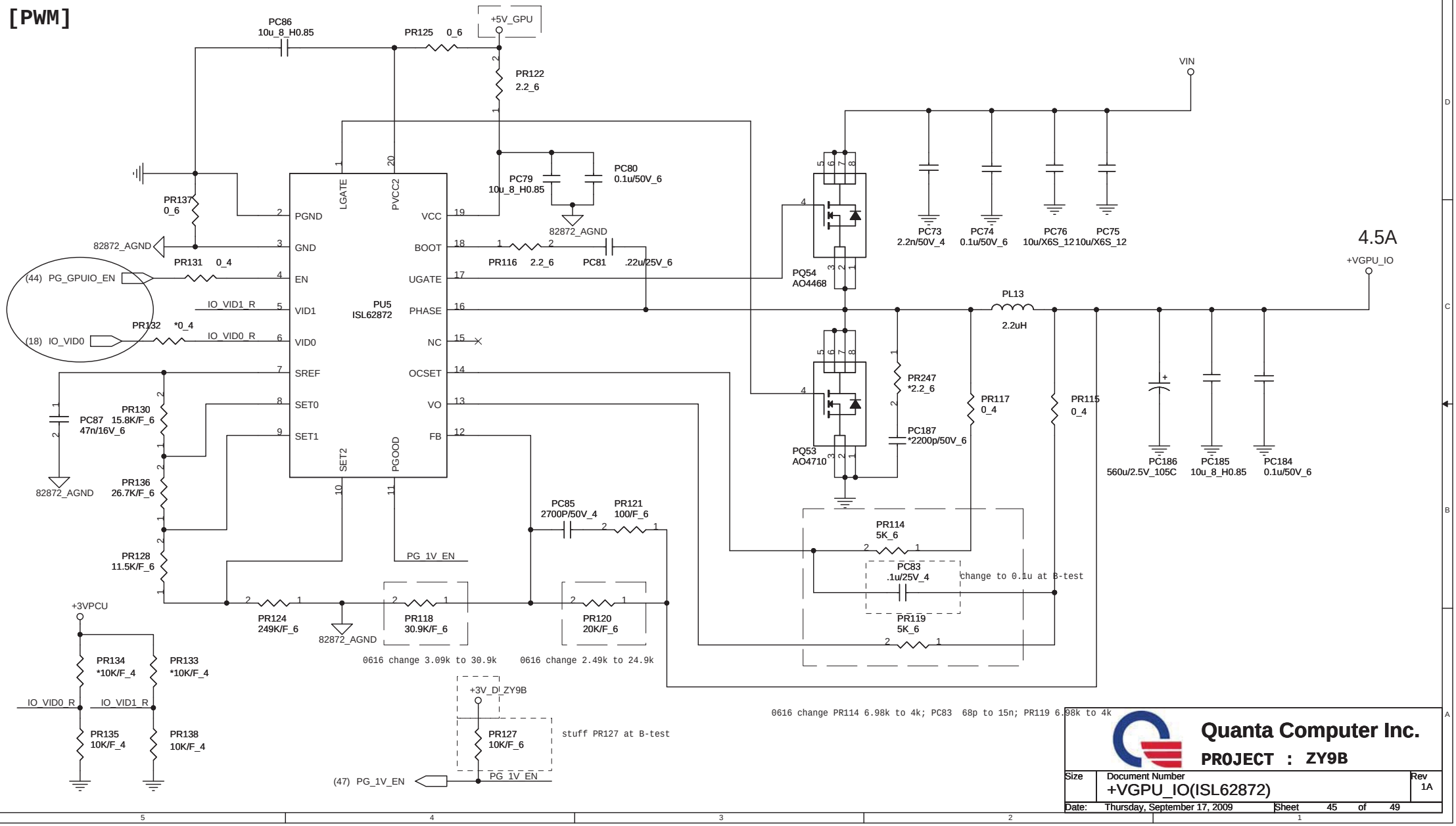
(10u*PR35)/Rdson+Delta_I/2=Iocp



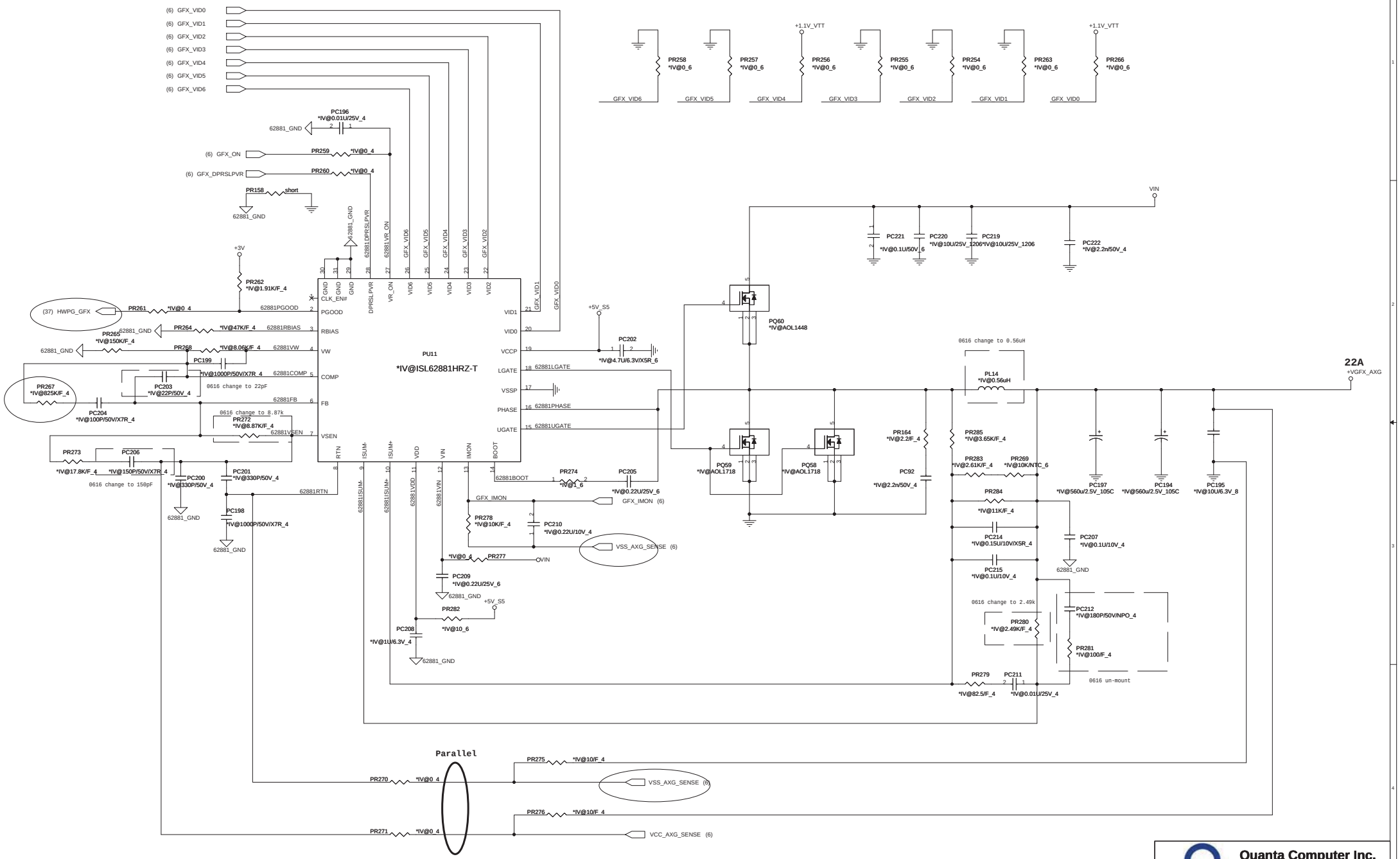


Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: DDR 1.5V(TPS51116)	Rev: 1A
Date: Thursday, September 17, 2009	Sheet 43 of 49	


+3V
PR207 *10K_6
PR206 10K_6
PR209 *10K_6
PR208 10K_6
PR215 10K_6
PR214 *10K_6
GPU_VID5
GPU_VID4
GPU_VID3
GPU_VID2
GPU_VID1
GPU_VID0
PR40 10K_6
PR39 *10K_6
PR44 10K_6
PR43 *10K_6
PR48 *10K_6
PR47 10K_6
Note: VID[5:0]=010110=1V
PG_GPUIO_EN (45)
change P/N to CC64704MZ01
VIN
+3V_D_ZY9B
PR42 10/F_6
PR31 100K
PC26 0.1u/50V_6
+5V_GPU
PR22 0_6
PR216 10/F_6
PC134 1u/25V_8
PU2 ISL6264
VCC
VIN
PGOOD
GND
GND_T
UGATE1
BOOT1
PHASE1
LGATE1
PGND1
ISEN1
PVCC
UGATE2
BOOT2
PHASE2
LGATE2
PGND2
ISEN2
OFS
RBIAS
SET
PSIL
SOFT
VID0
VID1
VID2
VID3
VID4
VID5
VR_ON
VDIFF
FB
COMP
VW
RTN
VSEN
DROOP
DFB
OCSET
VSUM
VO
6264_UG1
6264_PH1
6264_LG1
6264_UG2
6264_PH2
6264_LG2
6264_SET
ISL6264_VO
PR24 1M/F_4
PR25 147K/F_4
PR29 10K_4
PR34 *0_4
PR30 *0_4
PC125 47n/16V_6
PR26 0_4
PR27 *0_4
+3VPCU
(18) PWR_PSI#
PSI_L
VSOFT
(18) GPU_VID1
(18) GPU_VID2
(18) GPU_VID3
(11,22) dGPU_VRON
PR35 *0_4
PR37 0_4
PR36 100K/F_6
PR28 1K/F_4
PR20 255/F_4
PC19 1000p/50V_4
PR21 97.6K/F_4
PC20 470p/50V_4
PC22 220P/50V_4
PR199 6.81K/F_4
PC126 1000p/50V_4
PC21 68n/10V_4
PR33 1.15K/F_4
0616change 3.65kk to 1.15k
PC24 180p/50V_4
PC17 1000p/50V_4
PC18 1000p/50V_4
PR58 2.2_6
PC36 0.22u/25V_8
PC40 4.7u/25V_8
PC32 0.22u/25V_6
PR72 2.2_6
PC39 0.22u/25V_8
PC37 1000p/50V_6
PC28 0.22u/25V_6
PC23 1000p/50V_4
PR23 5.6K_4
0616change 10.7k to 3k
PC132 0.22u/10V_6
PC129 47n/16V_6
PR205 11K/F_4
PR38 2.61K/F_4
PR108 10K_6 NTC
PC25 0.22u/10V_6
PR32 1K/F_4
PR203 0_4
PR202 0_4
VGPU_CORE_SENSE (22)
VSS_GPU_SENSE (22)
Parallel
PR200 10/F_6
PR201 10/F_6
0616 mount
PR85 2.2_6
PC45 2200p/50V_6
PC52 10u/25V_1206
PC57 10u/25V_1206
PC46 0.1u/50V_6
PC156 100u/25V_6
PC168 100u/25V_6
PQ45 AOL1414
PC44 2200p/50V_6
PQ50 AOL1412
PC42 1000p/50V_6
PL12 0.36uH
PC183 330u/2V_7343
PC69 330u/2V_7343
+VGPU_CORE
PR105 0_4
PR107 0_4
PR70 3.65K/F_6
PR71 10K/F_6
PR69 1/F_6
PR68 10K/F_6
VSUM
ISEN2
PR98 2.2_6
PC61 2200p/50V_6
PC56 10u/25V_1206
PC51 10u/25V_1206
PC59 0.1u/50V_6
PQ48 AOL1414
PC67 2200p/50V_6
PQ49 AOL1412
PL11 0.36uH
PC70 330u/2V_7343
PC182 330u/2V_7343
PR104 0_4
PR106 0_4
PR41 3.65K/F_6
PR45 10K/F_6
PR49 1/F_6
PR61 10K/F_6
ISEN1
20A
Iocset*Roc=Iocp*Rdroop
R23=Roc=30A*1m Ohms/10uA ~ 3K
Where :
Rdroop is AMD spec : -1 m Ohms
Iocp is desire over current
Iocset is recommendation 10uA from Rbias
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Quanta Computer Inc.
PROJECT : ZY9B
Size
Document Number
GPU CORE(ISL6264)
Rev
1A
Date: Tuesday, September 22, 2009
Sheet 44 of 49


[PWM]
PC86
10u_8_H0.85
PR125 0_6
+5V_GPU
PR122
2.2_6
VIN
PC79
10u_8_H0.85
PC80
0.1u/50V_6
PR137
0_6
82872_AGND
PR131 0_4
(44) PG_GPUIO_EN
IO_VID1_R
PR132 *0_4
(18) IO_VID0
IO_VID0_R
PU5
ISL62872
PGND
GND
EN
VID1
VID0
SREF
SET0
SET1
LGATE
PVCC2
VCC
BOOT
UGATE
PHASE
NC
OCSET
VO
FB
SET2
PGOOD
PR116 2.2_6
PC81 .22u/25V_6
PQ54
AO4468
PQ53
AO4710
PC73
2.2n/50V_4
PC74
0.1u/50V_6
PC76
10u/X6S_12
PC75
10u/X6S_12
4.5A
+VGPU_IO
PL13
2.2uH
PR247
*2.2_6
PC187
*2200p/50V_6
PR117
0_4
PR115
0_4
PC186
560u/2.5V_105C
PC185
10u_8_H0.85
PC184
0.1u/50V_6
PC87
47n/16V_6
PR130
15.8K/F_6
PR136
26.7K/F_6
PR128
11.5K/F_6
PC85
2700P/50V_4
PR121
100/F_6
PG_1V_EN
PR114
5K_6
PC83
.1u/25V_4
change to 0.1u at B-test
PR119
5K_6
PR124
249K/F_6
PR118
30.9K/F_6
PR120
20K/F_6
0616 change 3.09k to 30.9k
0616 change 2.49k to 24.9k
+3VPCU
PR134
*10K/F_4
PR133
*10K/F_4
IO_VID0_R
IO_VID1_R
PR135
10K/F_4
PR138
10K/F_4
+3V_DL_ZY9B
PR127
10K/F_6
stuff PR127 at B-test
(47) PG_1V_EN
PG_1V_EN
0616 change PR114 6.98k to 4k; PC83 68p to 15n; PR119 6.98k to 4k
Quanta Computer Inc.
PROJECT : ZY9B
Size
Document Number
+VGPU_IO(ISL62872)
Rev
1A
Date: Thursday, September 17, 2009
Sheet 45 of 49

Int_VGA [PWM]



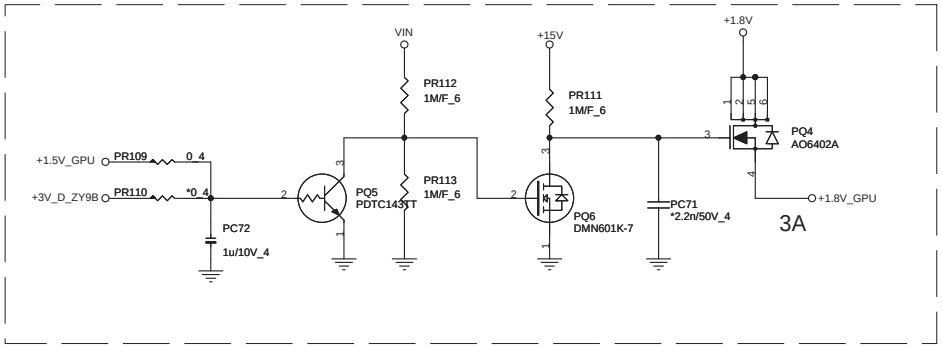
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

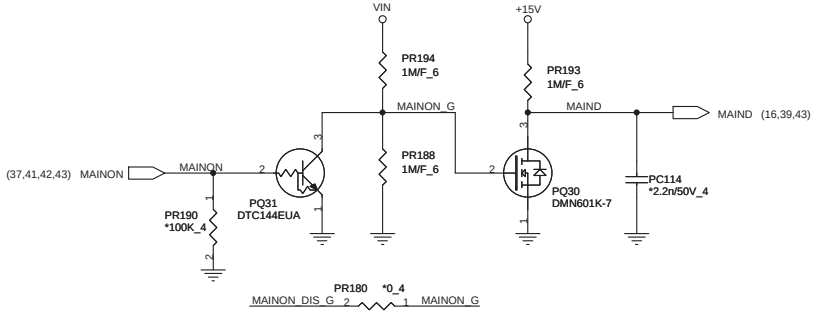
Quanta Computer Inc.
PROJECT : ZY9B

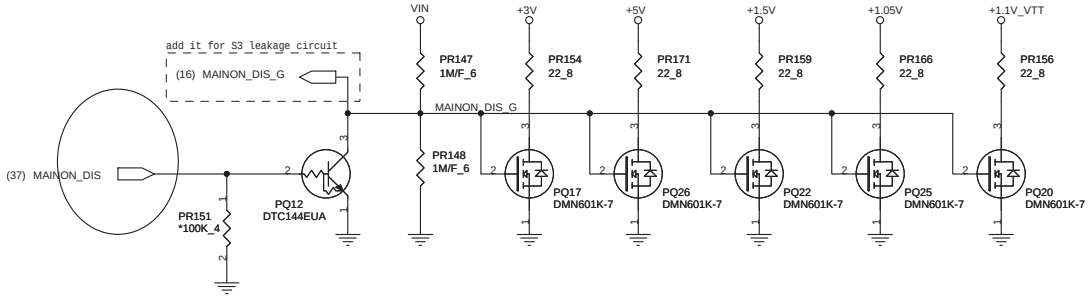
Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	1A

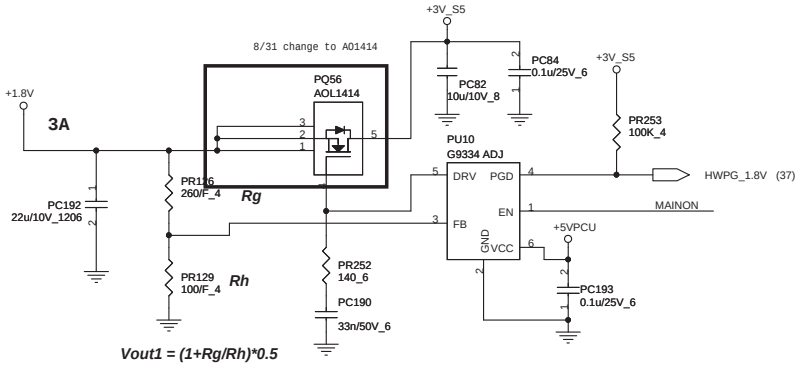
Date: Tuesday, September 22, 2009 Sheet 46 of 49

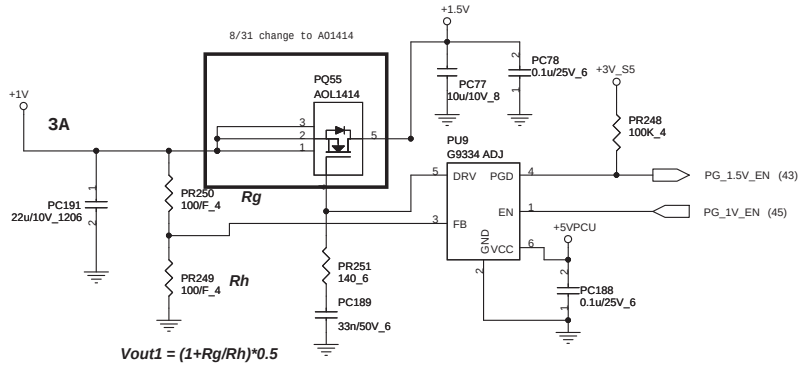
[PWM]









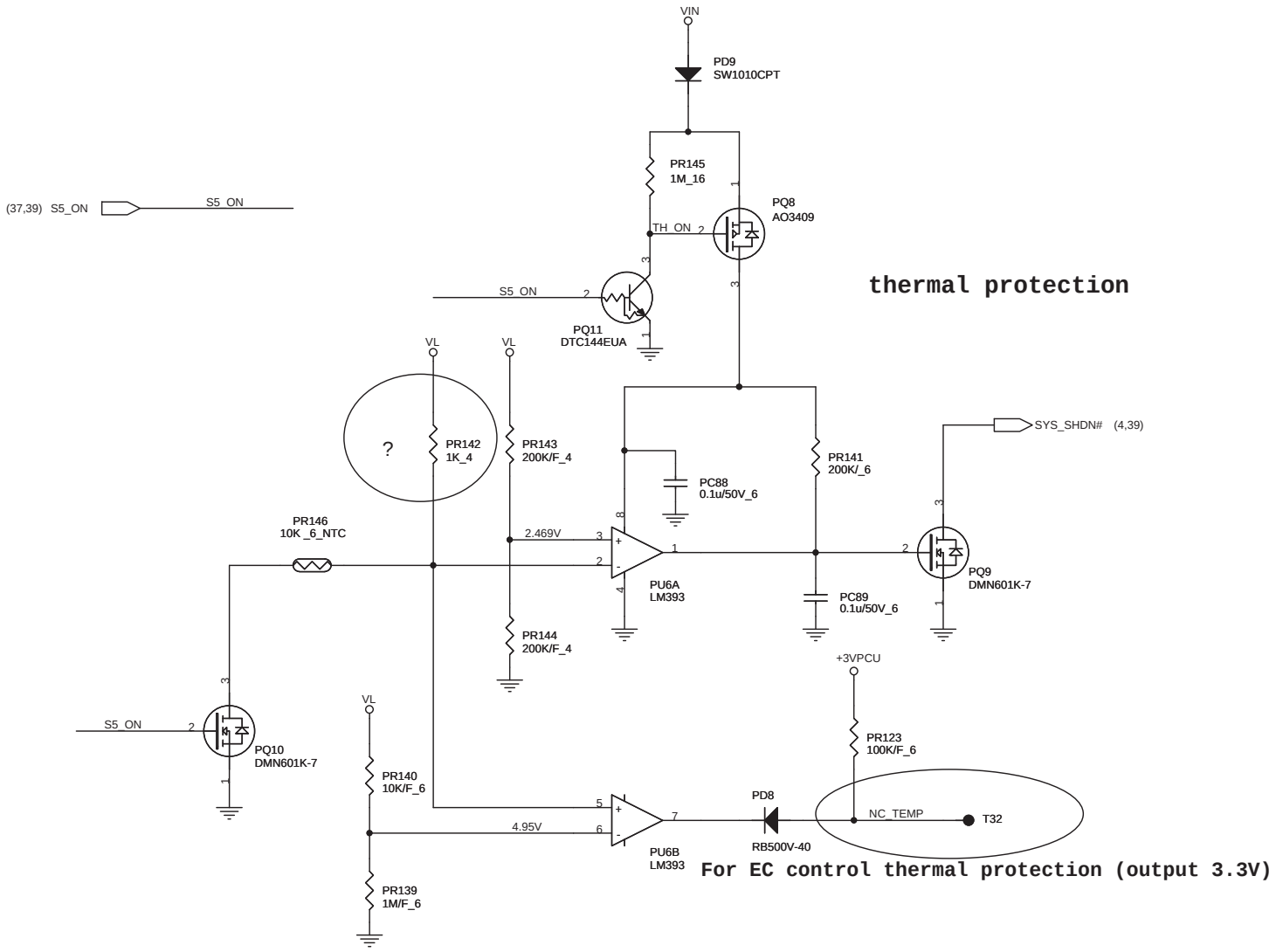


Quanta Computer Inc.

PROJECT : ZY9B

Size	Document Number	Rev
	Discharge/1V/1.8V)	1A

Date: Thursday, September 17, 2009 Sheet 47 of 49



Quanta Computer Inc.		
PROJECT : ZY9B		
Size	Document Number: Thermal Protection	Rev: 1A
Date: Thursday, September 17, 2009	Sheet 48 of 49	

Model	REV	CHANGE LIST
ZY9B MB	1A	FIRST RELEASED: E20080?-???? (PCB: DA0ZY9MB8A0)
	2A	Page4 :
	3A	
	3C	

MODEL	ZY9B	
	FROM	To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
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	1A	2A
	2A	3A
	2A	3A
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	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B
	3A	3B

DOC NO.	PROJECT MODEL :	ZY9B	APPROVED BY:		DATE:	2009/05/??
	PART NUMBER:		DRAWING BY:		REVISON:	1A