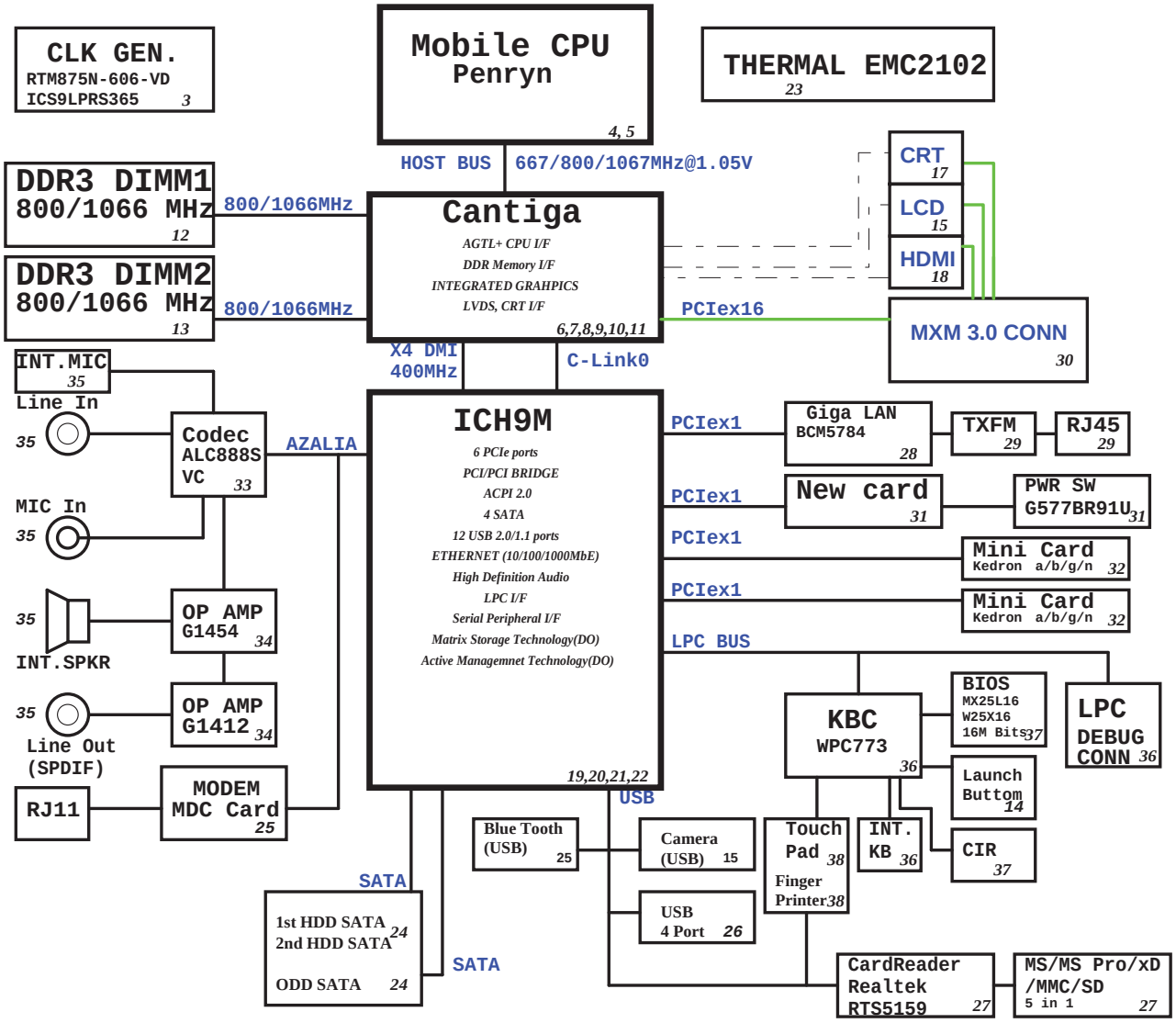
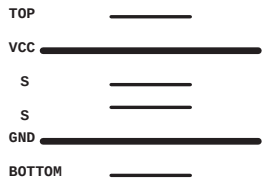
SJM80_MV/JV80_MV Block Diagram



Project code: 91.4DW01.001
PCB P/N : 48.4DW01.0SB
REVISION : 09221 -1

PCB STACKUP



SYSTEM DC/DC TPS51125 *43*

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 *45*

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D5V_S3

RT9026 *44*

1D5V_S3	DDR_VREF_S3 DDR_VREF_S3_1

AO4468 *44*

1D5V_S3	1D5V_S0

GFXCORE DC/DC ISL6263A *46*

INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V

CPU DC/DC ISL6266A *42*

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER MAX8731A *47*

INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

SJM80 UMA ONLY SB

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
Custom	SJM80/JV80	-1

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

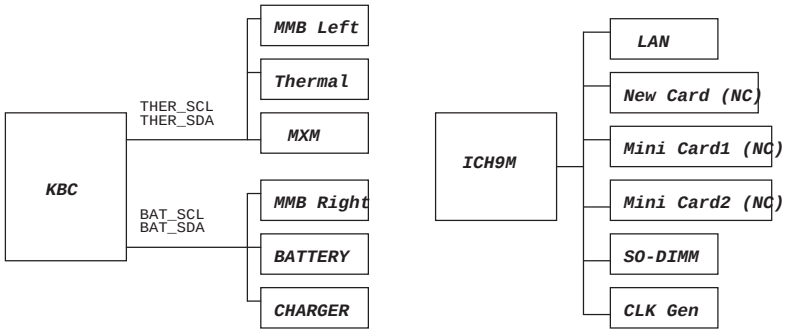
PCIE Routing

LANE1	LAN Broadcom 5784
LANE2	MiniCard WLAN
LANE3	MiniCard TV
LANE4	NC
LANE5	NewCard
LANE6	*NC*

USB Table

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINI1 (WL)
4	CCD
5	NEW CARD
6	FP
7	BT
8	NC
9	USB1
10	MINI2
11	CARD READER

SMBus



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Title: Reference

Size: A3 | Document Number: SJM80/JV80 | Rev: -1

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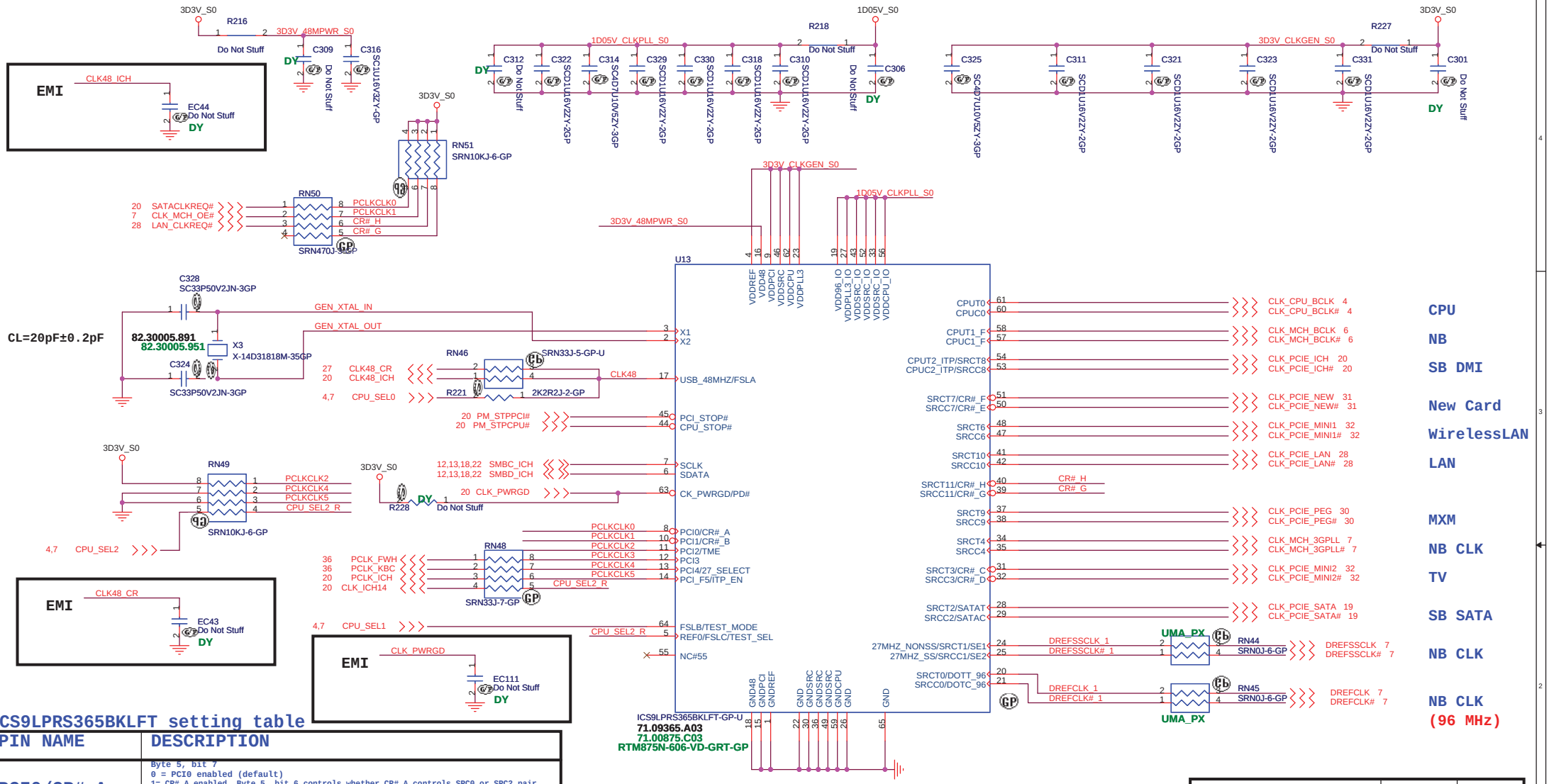

ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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Title: Clock Generator

Size	Document Number	Rev
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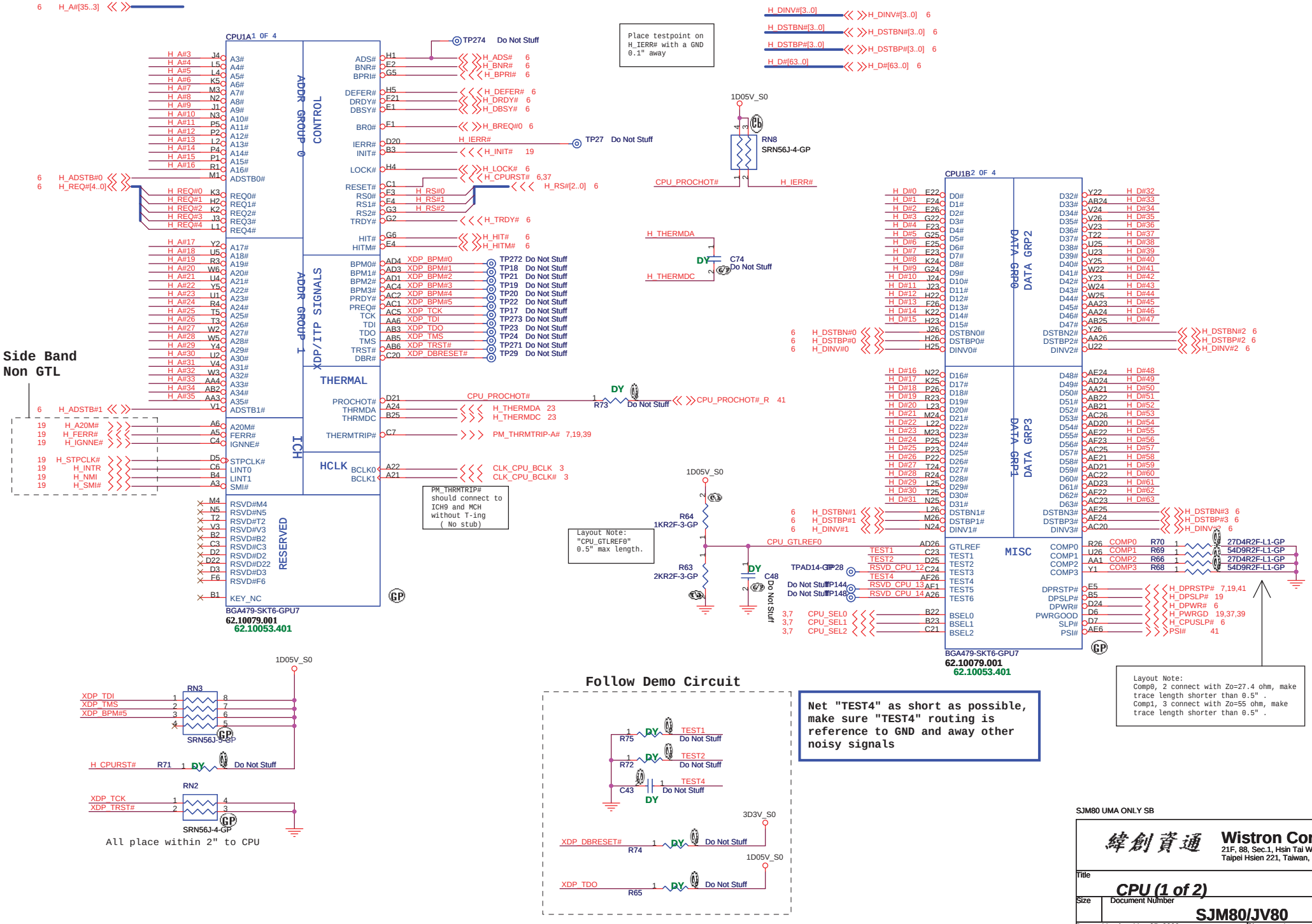
Side Band
Non GTL
CPU1A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU7
62.10079.001
62.10053.401
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
CPU1B 2 OF 4
DATA GRP0
DATA GRP1
DATA GRP2
DATA GRP3
MISC
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Follow Demo Circuit
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
All place within 2" to CPU
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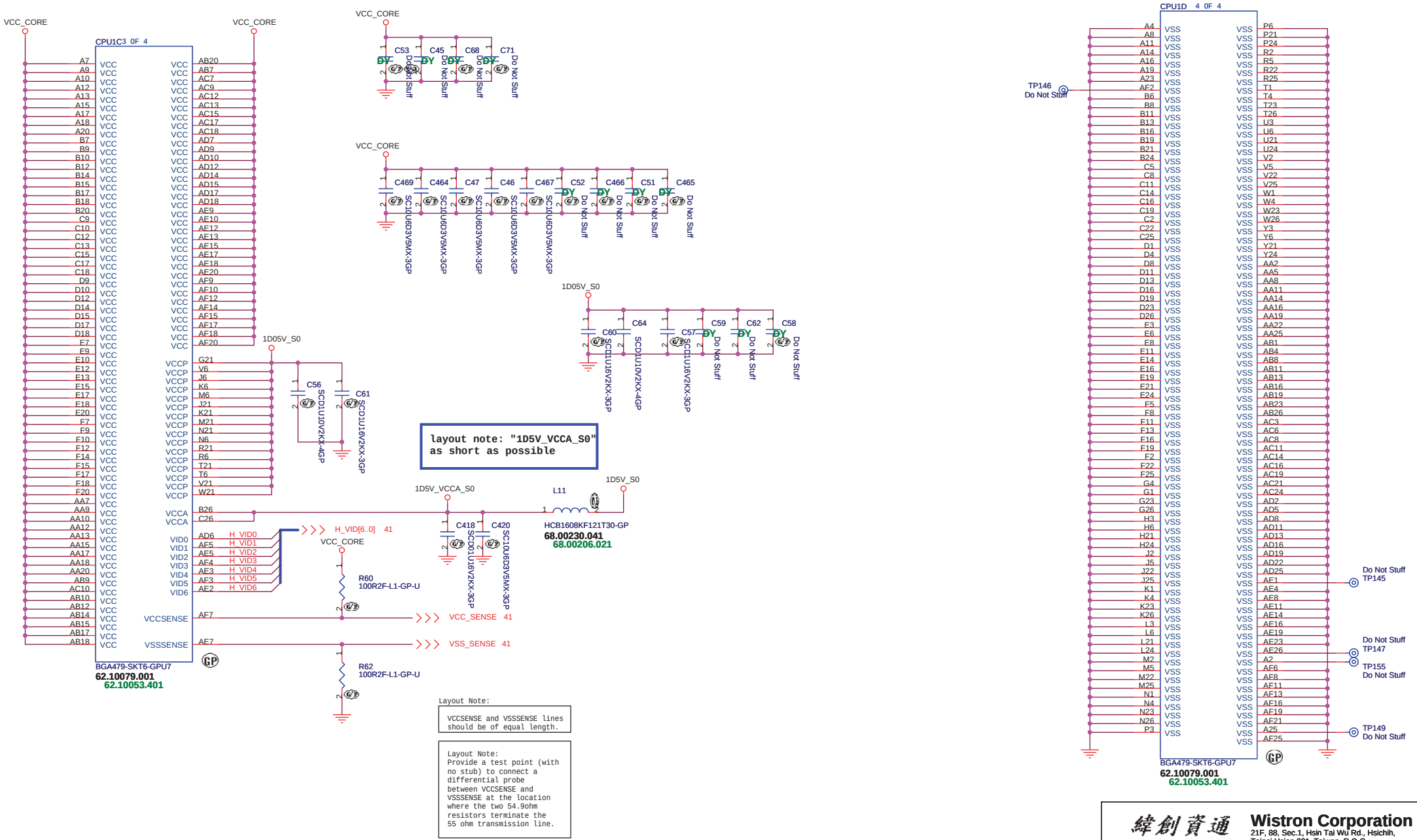

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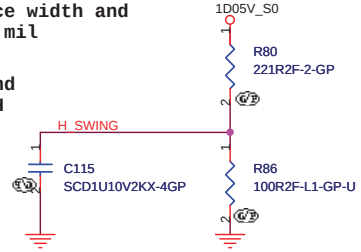
Title	CPU (2 of 2)	
Size	Document Number: SJM80/JV80	Rev: -1
Date: Monday, May 25, 2009	Sheet 5 of 51	

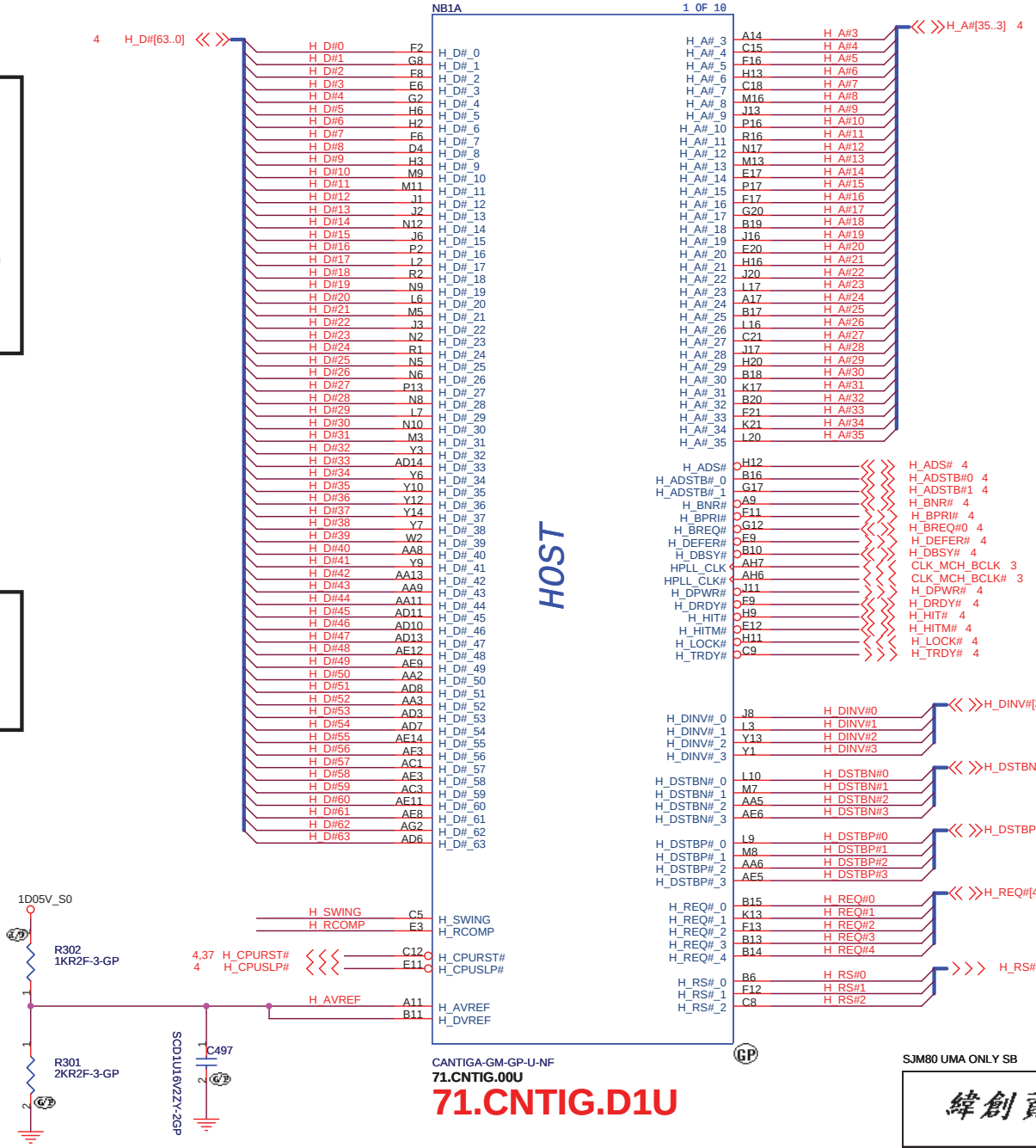
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



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Title: Cantiga (1 of 6)

Size | Document Number: SJM80/JV80 | Rev: -1

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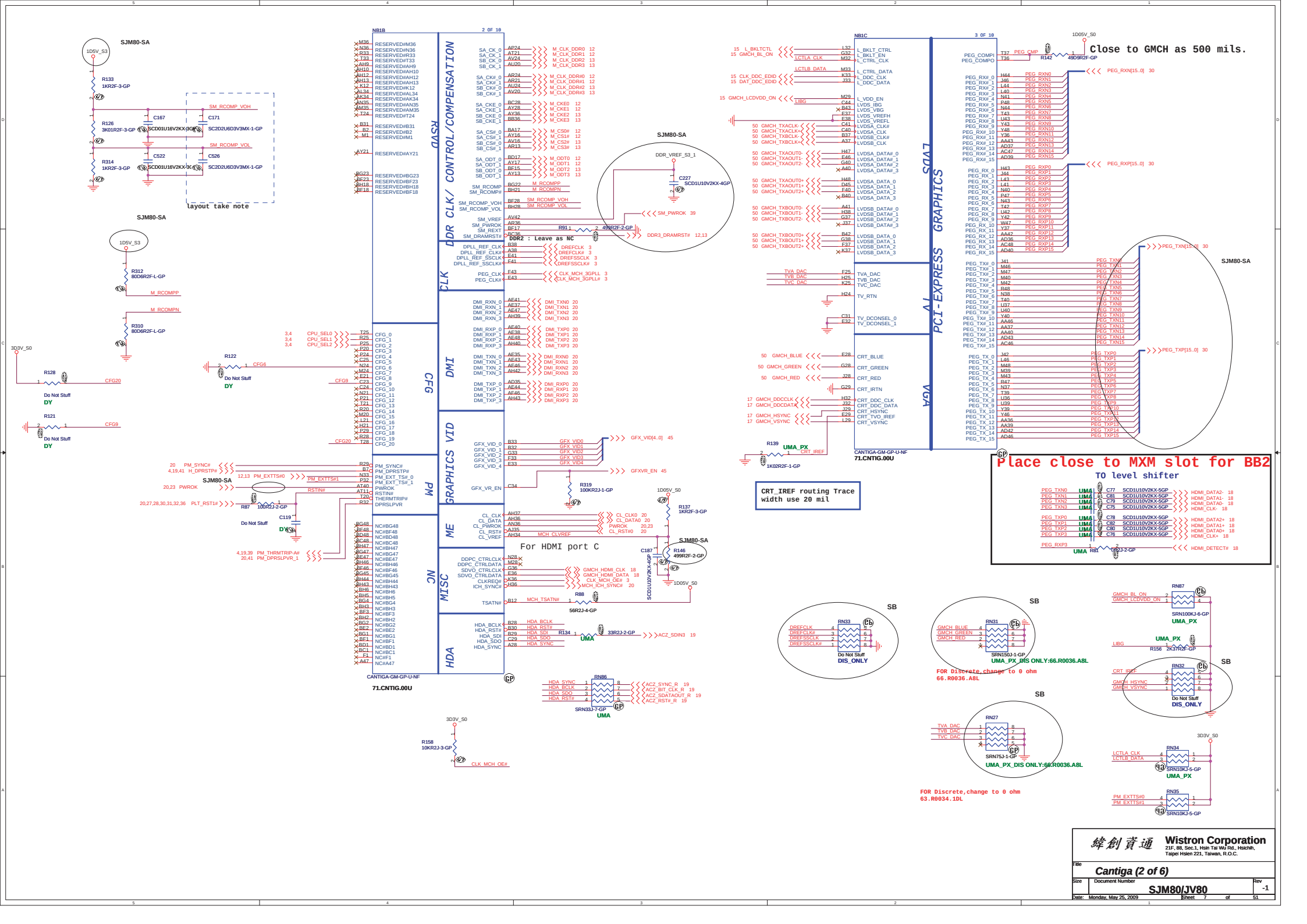
NB1B
2 OF 10
RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
HDA
SJM80-SA
layout take note
DDR2 : Leave as NC
For HDMI port C
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
NB1C
3 OF 10
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
Close to GMCH as 500 mils.
Place close to MXM slot for BB2
TO level shifter
CRT_IREF routing Trace width use 20 mil
SB
DIS_ONLY
UMA_PX_DIS ONLY:66.R0036.A8L
FOR Discrete,change to 0 ohm 66.R0036.A8L
FOR Discrete,change to 0 ohm 63.R0034.1DL
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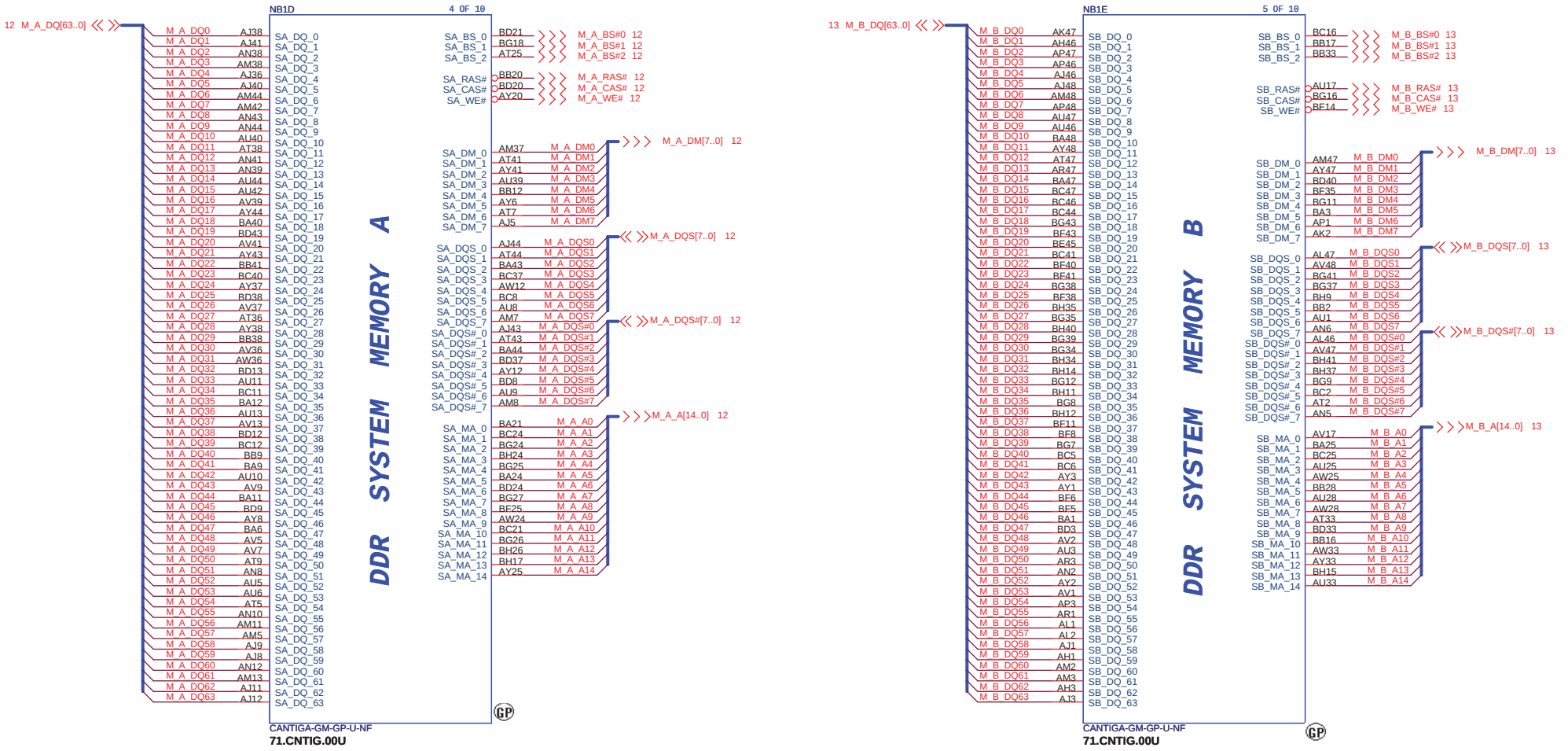
51



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Title: ***Cantiga (3 of 6)***

Size | Document Number: **SJM80/JV80** | Rev: -1

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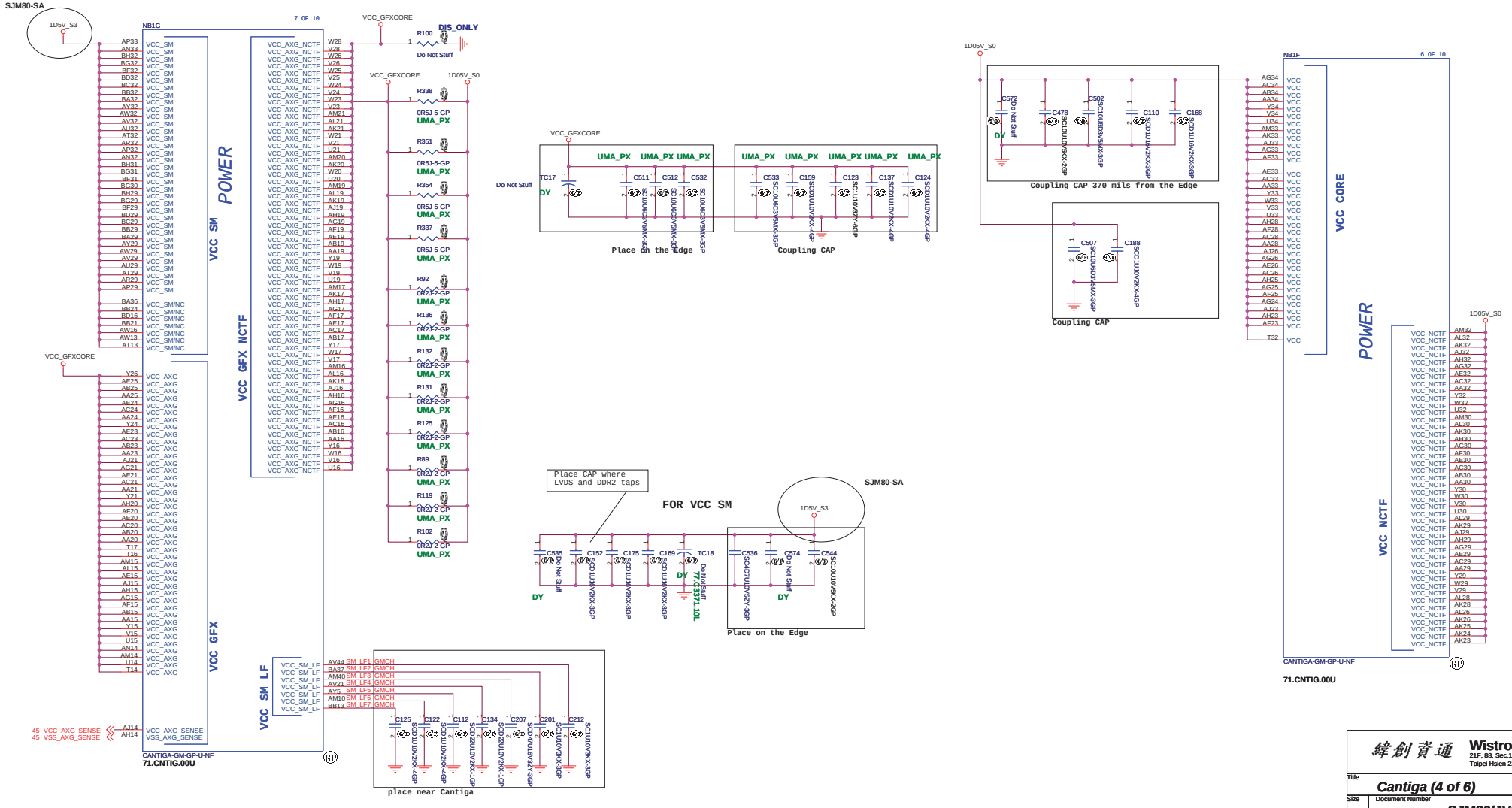

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Title	***Cantiga (4 of 6)***	
Size	Document Number: **SJM80/JV80**	Rev: -1
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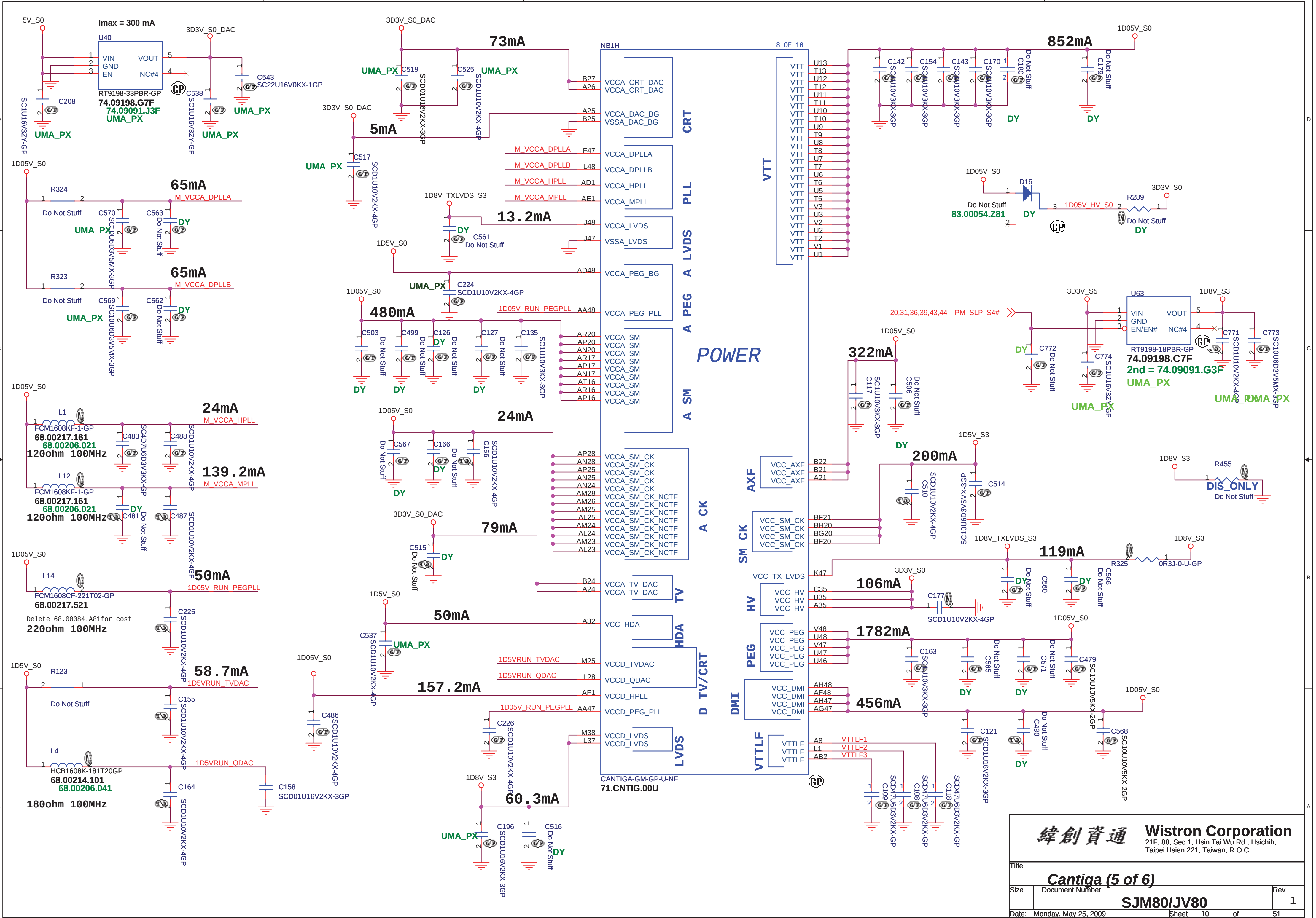

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Title: *Cantiga (5 of 6)*

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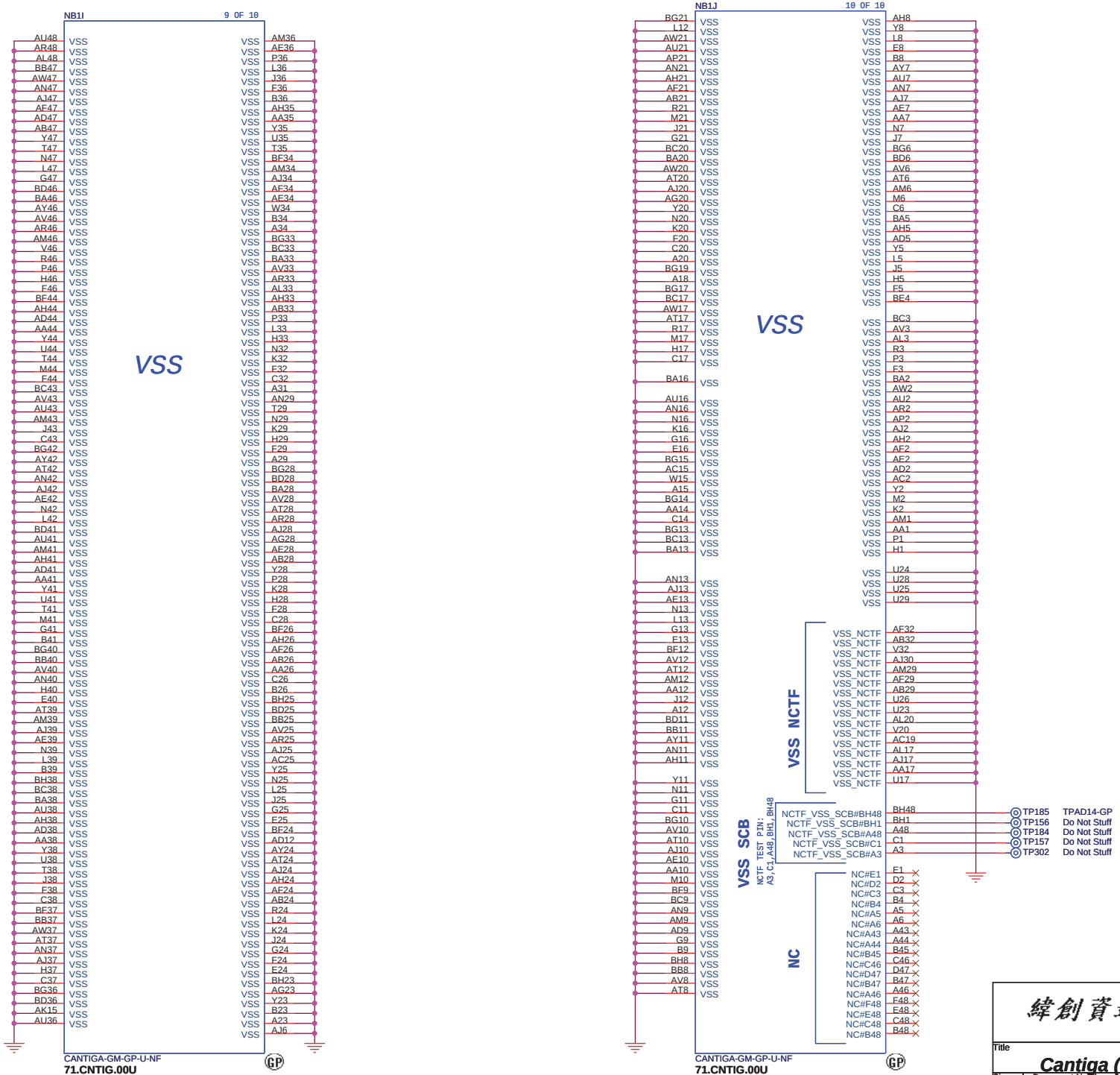

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Title: ***Cantiga (6 of 6)***

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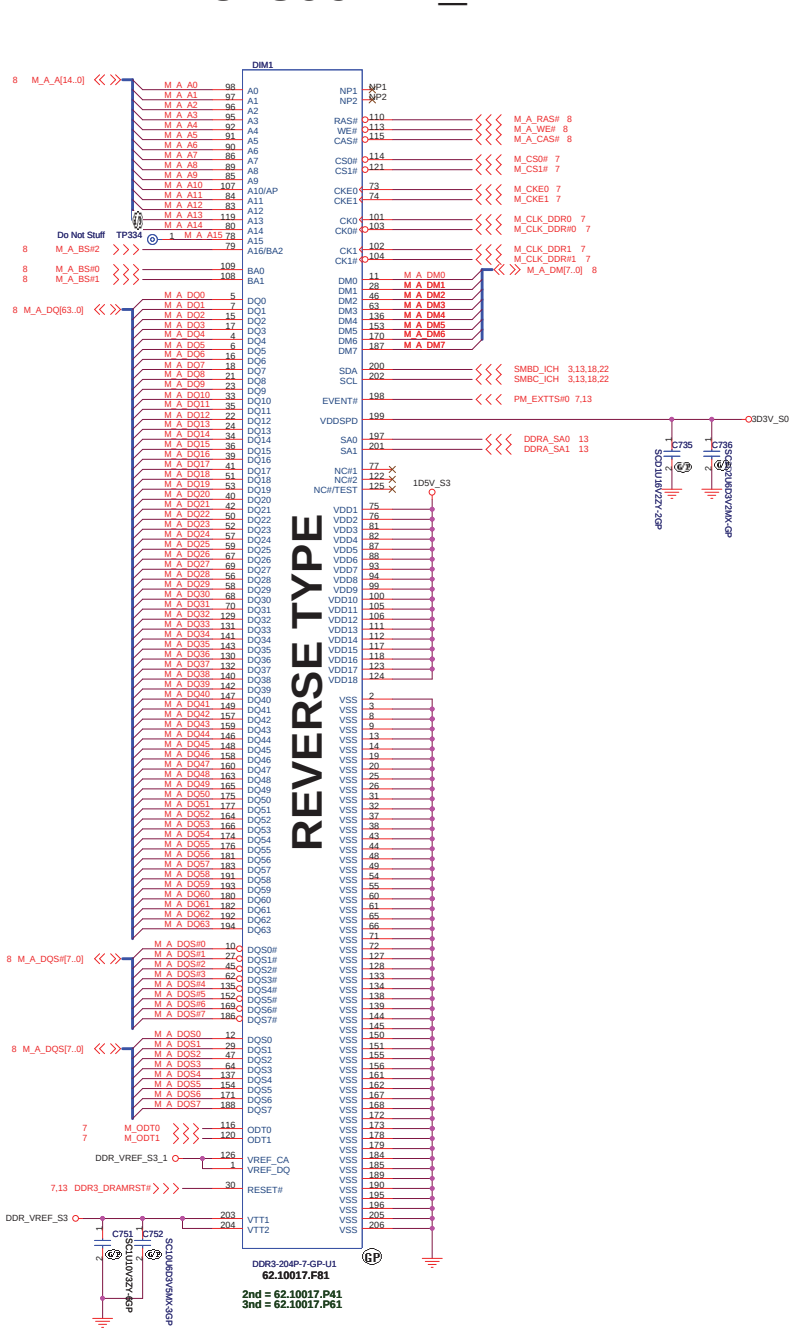
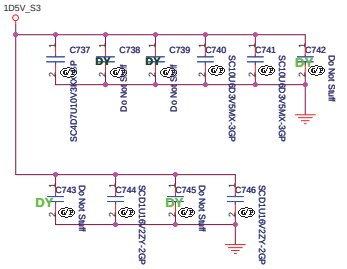
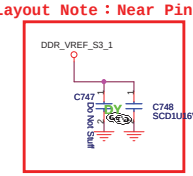
DDR3 SOCKET_1

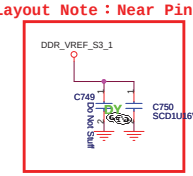




Layout Note : Near Pin 126



Layout Note : Near Pin 1



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Title	***DDR3 Socket***	
Size	Document Number **SJM80/JV80**	Rev -1
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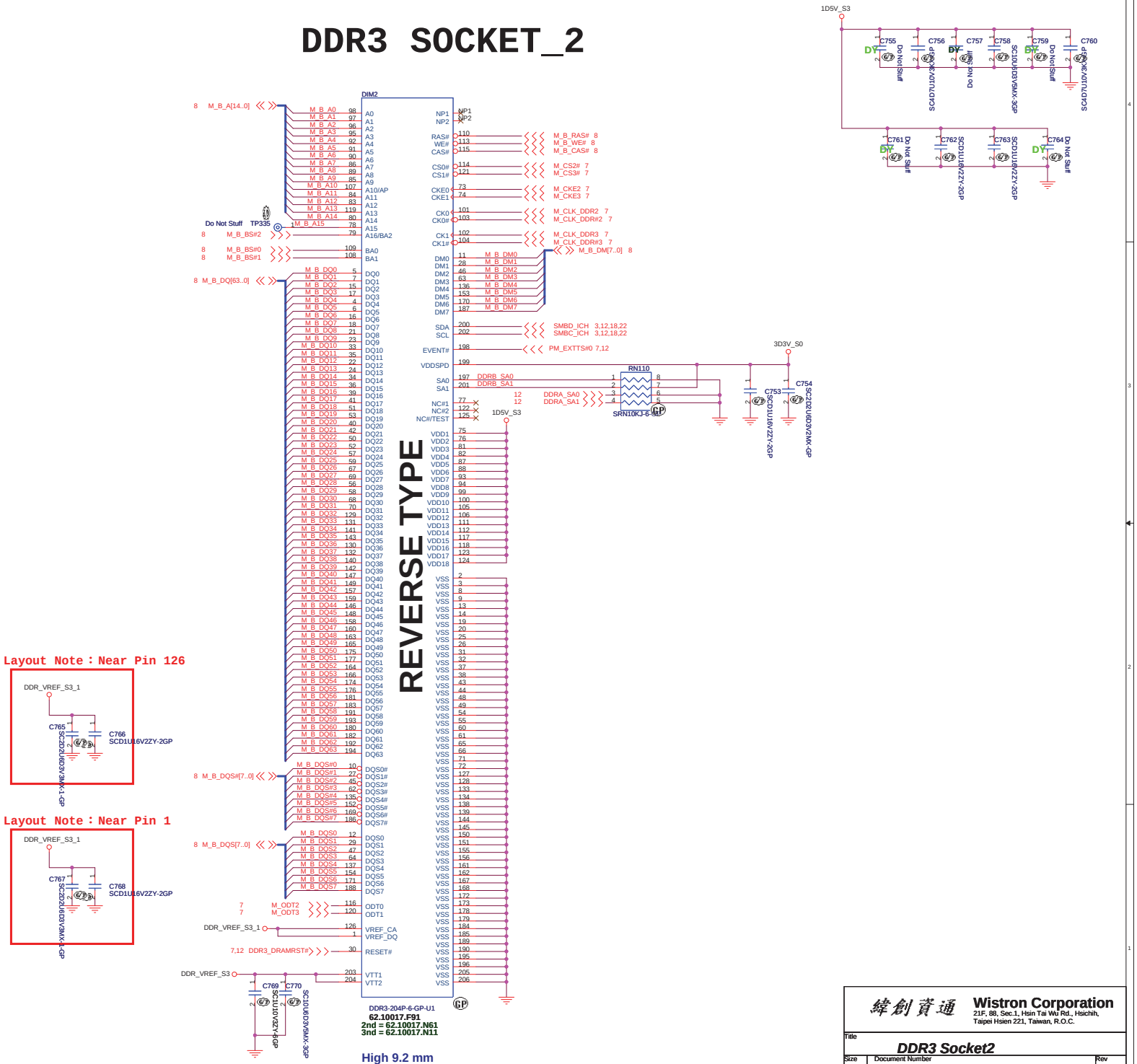
DDR3 SOCKET_2



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Title: DDR3 Socket2	
Size	Document Number: SJM80/JV80
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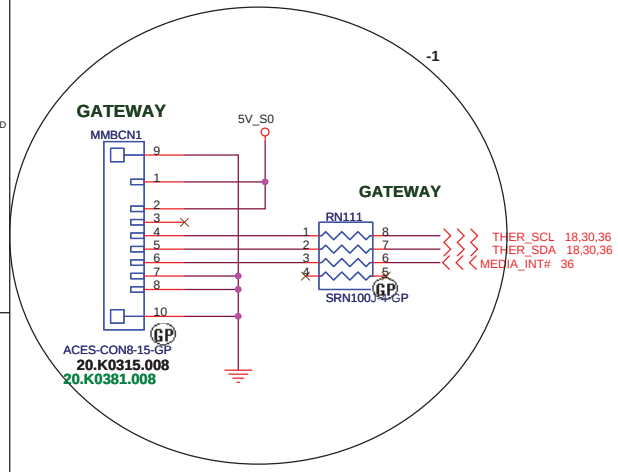
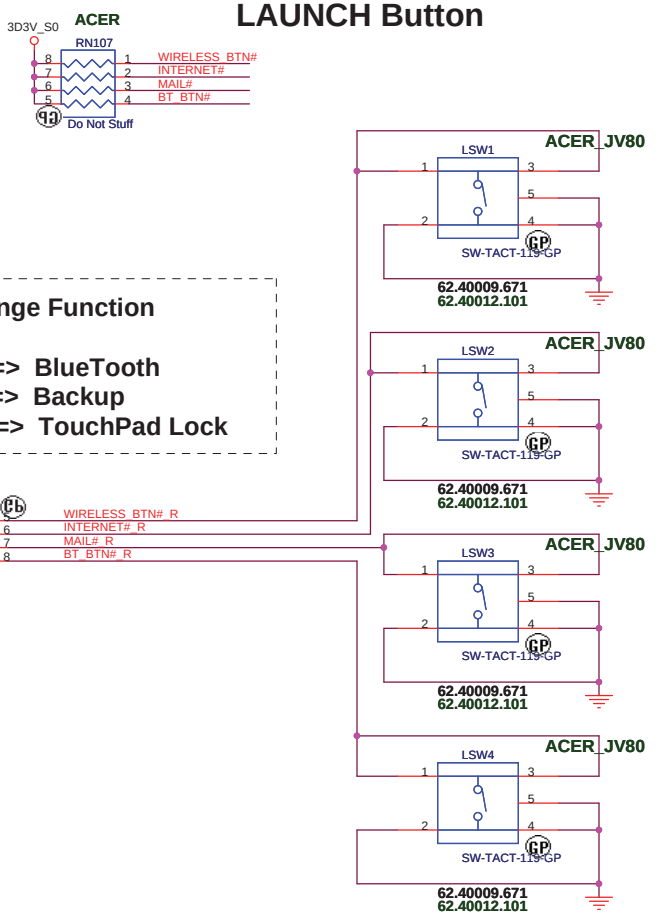
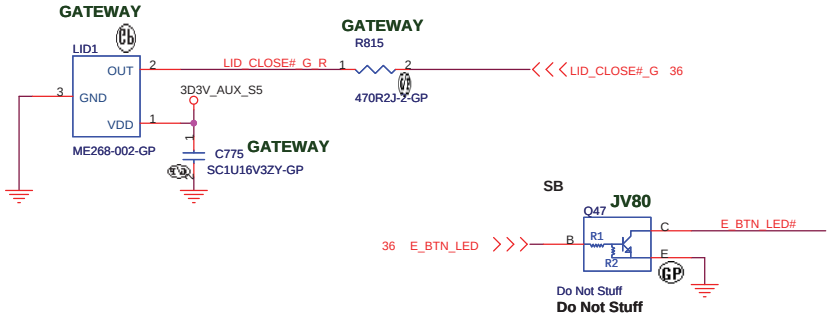
MMB Lounch For GATEWAY



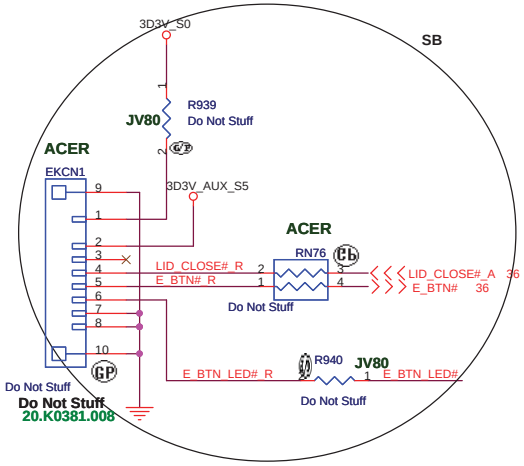
LAUNCH Button



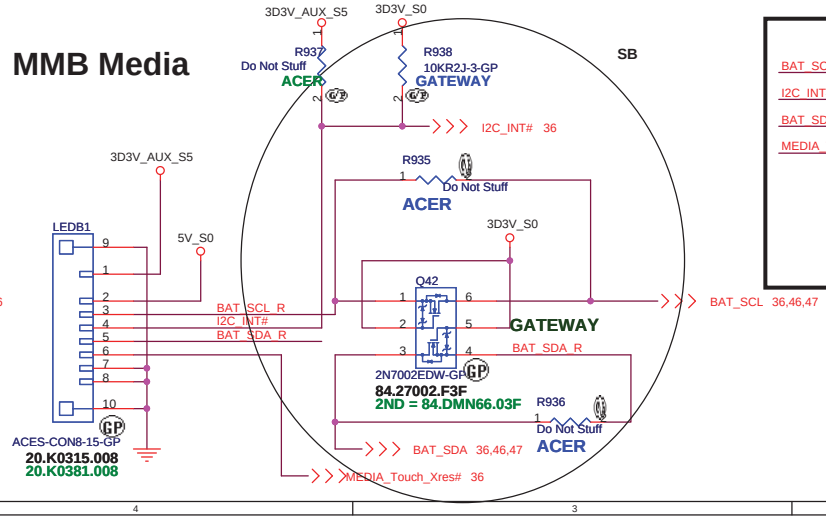
LID SWITCH

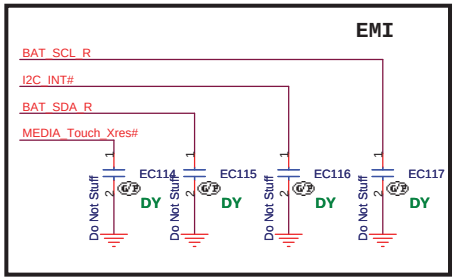


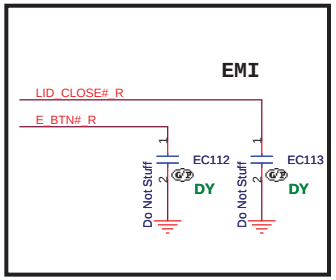
E-KEY Button



MMB Media







SJM80 UMA ONLY SB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

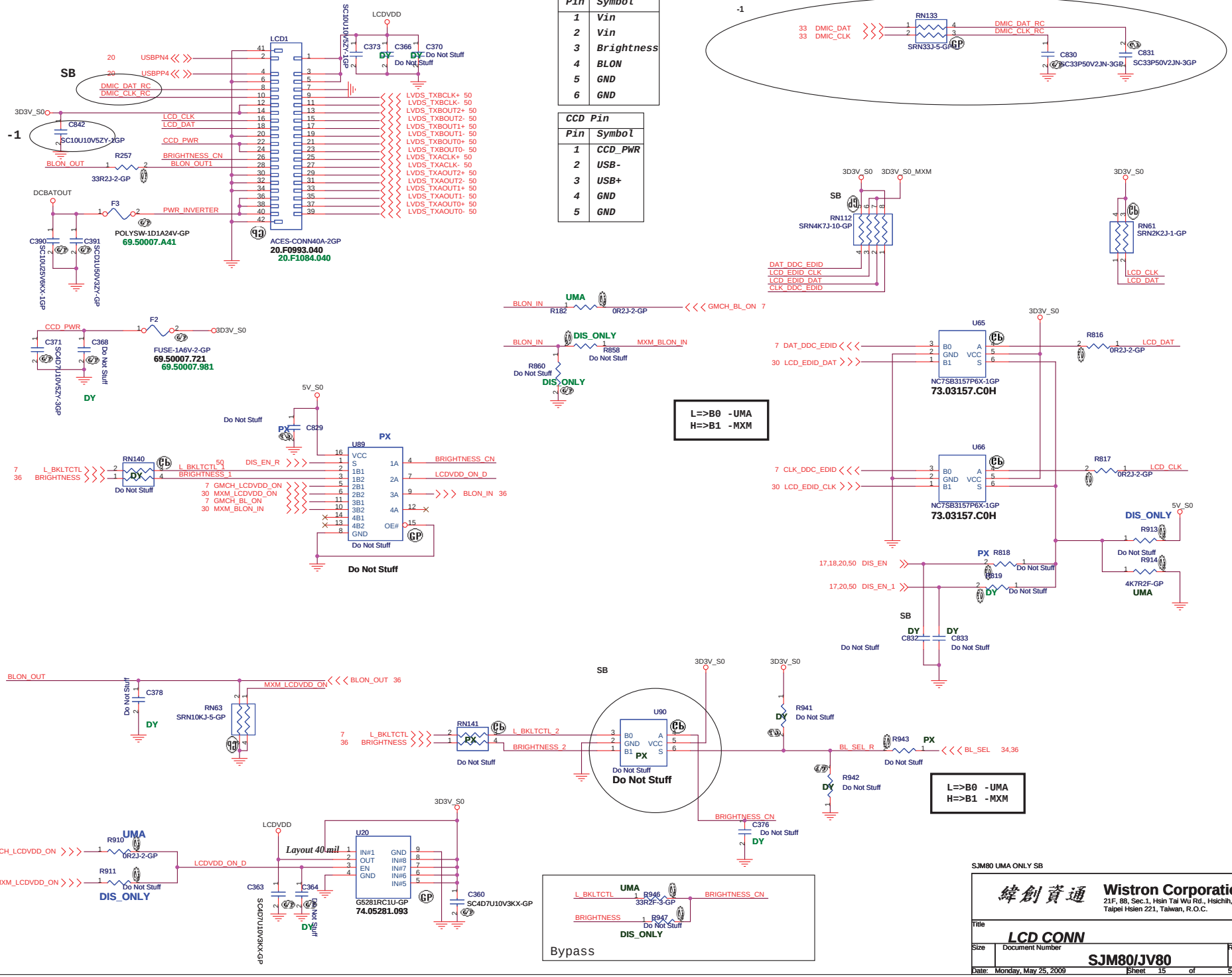
Title	**LAUNCH**	
Size	Document Number **SJM80/JV80**	Rev -1
Date: Monday, May 25, 2009	Sheet 14 of 51	

LCD/INVERTER/CCD CONN

EMI request RN133 22R change 33R
C830/C831 22P change 33P

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



SJM80 UMA ONLY SB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

Size	Document Number	Rev
	SJM80/JV80	-1

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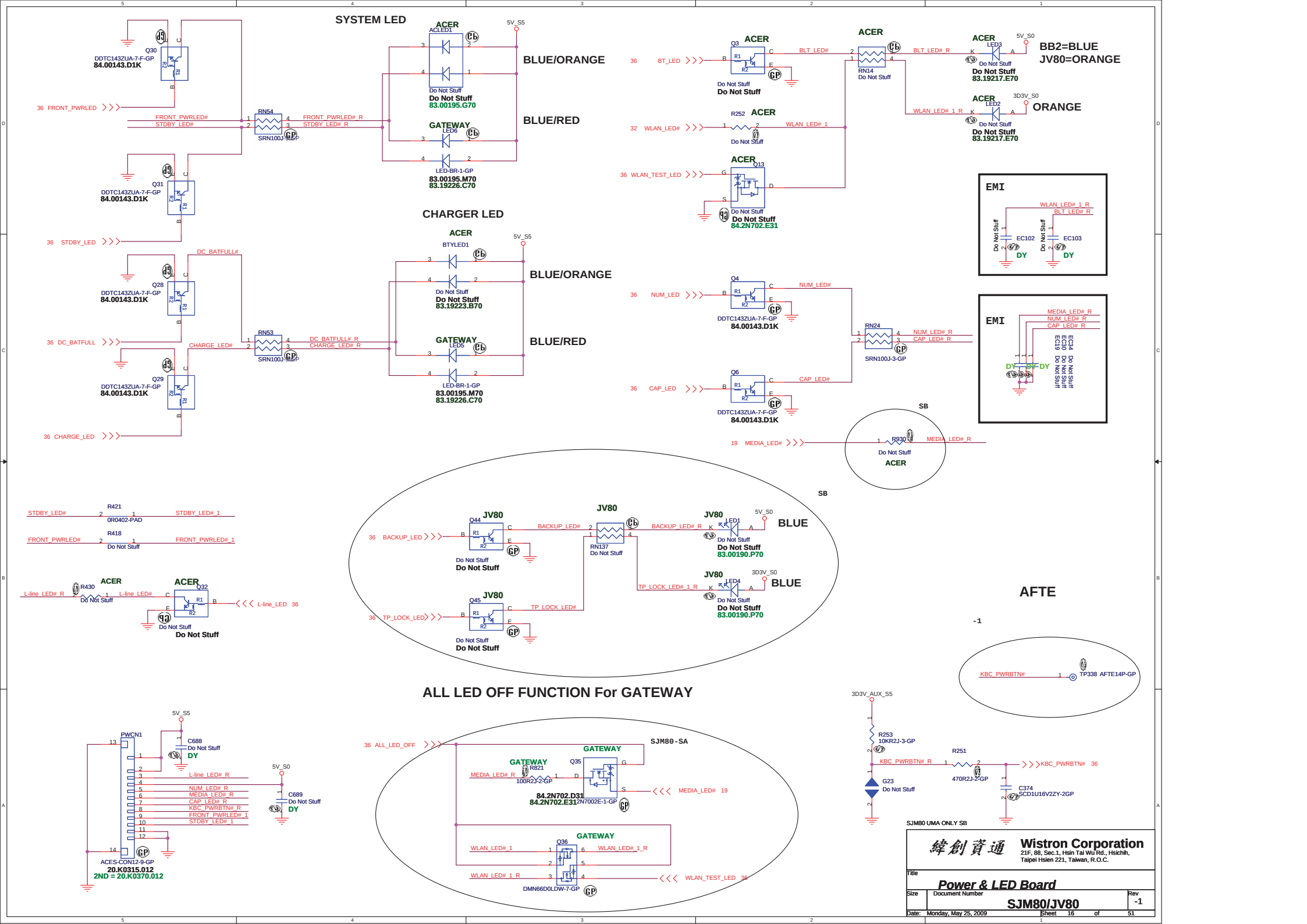

SYSTEM LED
CHARGER LED
EMI
EMI
SB
SB
ALL LED OFF FUNCTION For GATEWAY
AFTE
-1
BLUE/ORANGE
BLUE/RED
BLUE/ORANGE
BLUE/RED
BB2=BLUE
JV80=ORANGE
ORANGE
BLUE
BLUE
Do Not Stuff
DY
ACER
GATEWAY
JV80
SJM80-SA
SJM80 UMA ONLY SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Power & LED Board
SJM80/JV80
Monday, May 25, 2009

Layout Note:
Place these resistors close to the CRT-out connector

2nd =68.00119.081 source Check

Ferrite bead impedance: 10 ohm@100MHz

50 CRT_RED — L9 FCB1608CF-GP 68.00230.021 — CRT_R
50 CRT_GREEN — L8 FCB1608CF-GP 68.00230.021 — CRT_G
50 CRT_BLUE — L7 FCB1608CF-GP 68.00230.021 — CRT_B

R267 150R2J-L1-GP-U, R269 150R2J-L1-GP-U, R272 150R2J-L1-GP-U
C843 SC6D8P50V2DN-GP, C844 SC6D8P50V2DN-GP, C845 SC6D8P50V2DN-GP
C401 SC15P50V2JN-2-GP, C397 SC6D8P50V2DN-GP, C395 SC6D8P50V2DN-GP
-1
For EMI

5V_S0
D10 CRT_R — DY — Do Not Stuff / Do Not Stuff 83.00099.K11
D8 CRT_G — DY — Do Not Stuff / Do Not Stuff 83.00099.K11
D7 CRT_B — DY — Do Not Stuff / Do Not Stuff 83.00099.K11

Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

-1

15,20,50 DIS_EN_1 — DY — Do Not Stuff — R823
15,18,20,50 DIS_EN — PX — Do Not Stuff — R824

For UMA CRT

7 GMCH_HSYNC
7 GMCH_VSYNC
CRT_VSYNC1 — R826 33R2F-3-GP — SB

U68 SSLVC2G125DP-1GP 73.2G125.A07
5V_S0
DIS_ONLY
R915 Do Not Stuff
R916 4K7R2F-GP — UMA
SB — R825 33R2F-3-GP — CRT_HSYNC1

For DIS CRT

30 CRT_HSYNC
30 CRT_VSYNC
CRT_VSYNC1_OT
CRT_HSYNC_OT

U69 SSHCT2G126DP-GP 73.2G126.ABB

L=>B0 -UMA
H=>B1 -MXM

CRT I/F & CONNECTOR

CRT1 VIDEO_15P-42-GP-U1 20.20378.015
2nd :20.20775.015 暫時不用

DAT_DDC1_5
CRT_HSYNC1
CRT_VSYNC1
CLK_DDC1_5
CRT_R
CRT_G
CRT_B

C394 SC100P50V2JN-3GP — DY — Do Not Stuff
C25 — DY — Do Not Stuff
C26 — DY — Do Not Stuff
C393 SC100P50V2JN-3GP
SB

5V_CRT_S0
C27 SCD01U16V2KX-3GP

5V_S0
D5 — DY — Do Not Stuff / Do Not Stuff 83.00099.K11
CRT_IN#_R
R265 — CRT_DEC# 36
C392 470R2J-2-GP — DY

DDC_CLK & DATA level shift

DDC_CLK & DATA level shift

3D3V_S0_MXM
3D3V_S0
SB
RN113 Do Not Stuff — DY
RN114 SRN2K2J-1-GP UMA_PX

7 GMCH_DDCDATA
30 CRT_DDCDATA
U70 NC7SB3157P6X-1GP 73.03157.C0H

7 GMCH_DDCCLK
30 CRT_DDCCLK
U71 NC7SB3157P6X-1GP 73.03157.C0H

L=>B0 -UMA
H=>B1 -MXM

5V_CRT_S0
69.50007.691
69.50007.771
F4 FUSE-1D1A6V-4GP-U
5V_S0_CRT

D31 BAS16-1-GP 2nd = 83.00016.K11
RN115 Do Not Stuff — DY
RN116 4P2R-4K7R-1-GP
R931 0R0402-PAD
Q37
DY Do Not Stuff 84.DMN66.03F
R932 0R0402-PAD
CRT_IN#_R
DAT_DDC1_5
CLK_DDC1_5

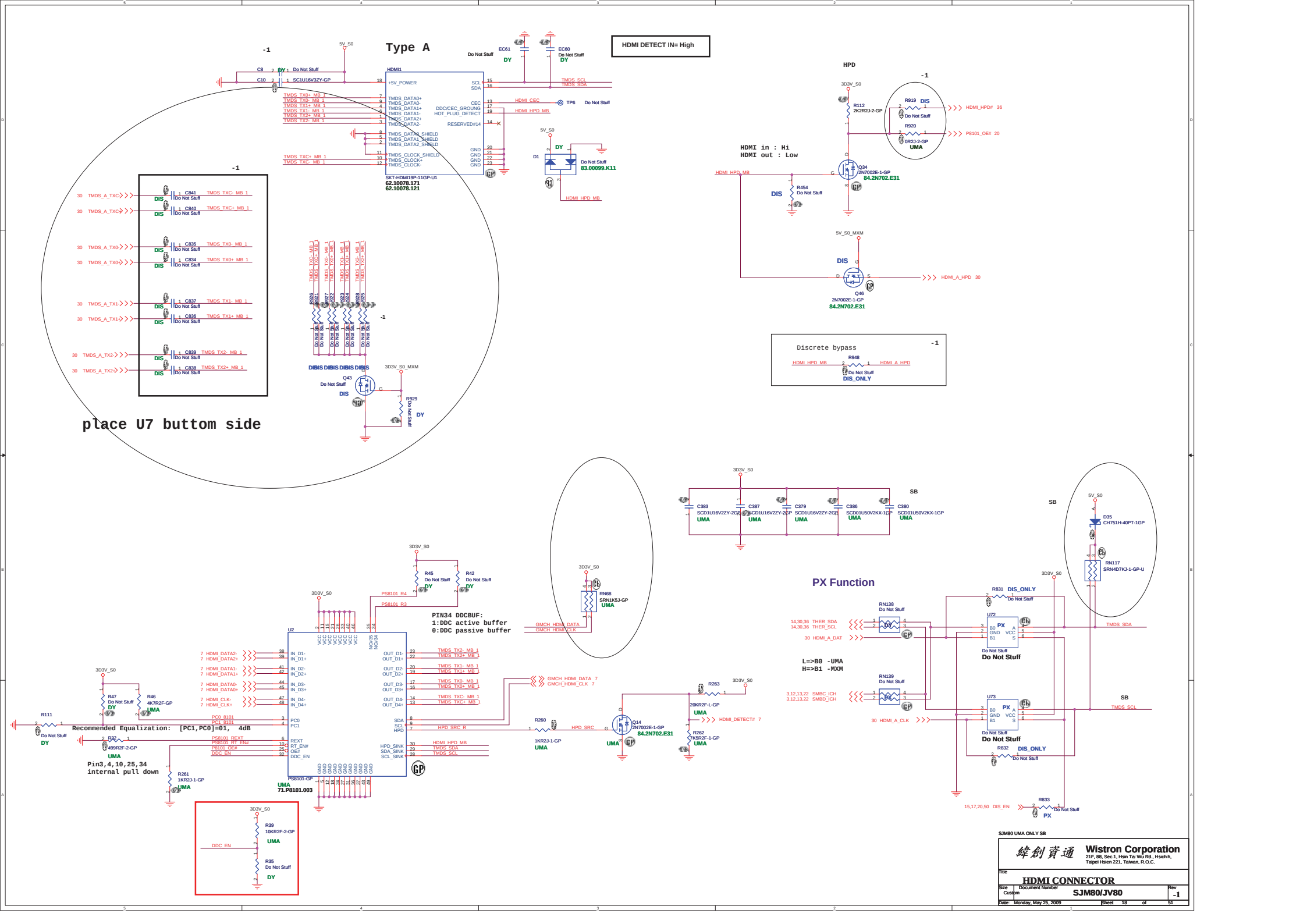
15,18,20,50 DIS_EN
R828 — PX — Do Not Stuff

5V_S0
DIS_ONLY
R917
Do Not Stuff
R918 4K7R2F-GP — UMA

SJM80 UMA ONLY SB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector
Size: Document Number: SJM80/JV80 Rev: -1
Date: Monday, May 25, 2009 Sheet 17 of 51


Type A
HDMI DETECT IN= High
HPD
HDMI in : Hi
HDMI out : Low
Discrete bypass
place U7 buttom side
PX Function
L=>B0 -UMA
H=>B1 -MXM
PIN34 DDCBUF:
1:DDC active buffer
0:DDC passive buffer
Recommended Equalization: [PC1,PC0]=01, 4dB
Pin3,4,10,25,34
internal pull down
SJM80 UMA ONLY SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
HDMI CONNECTOR
SJM80/JV80
-1
Monday, May 25, 2009
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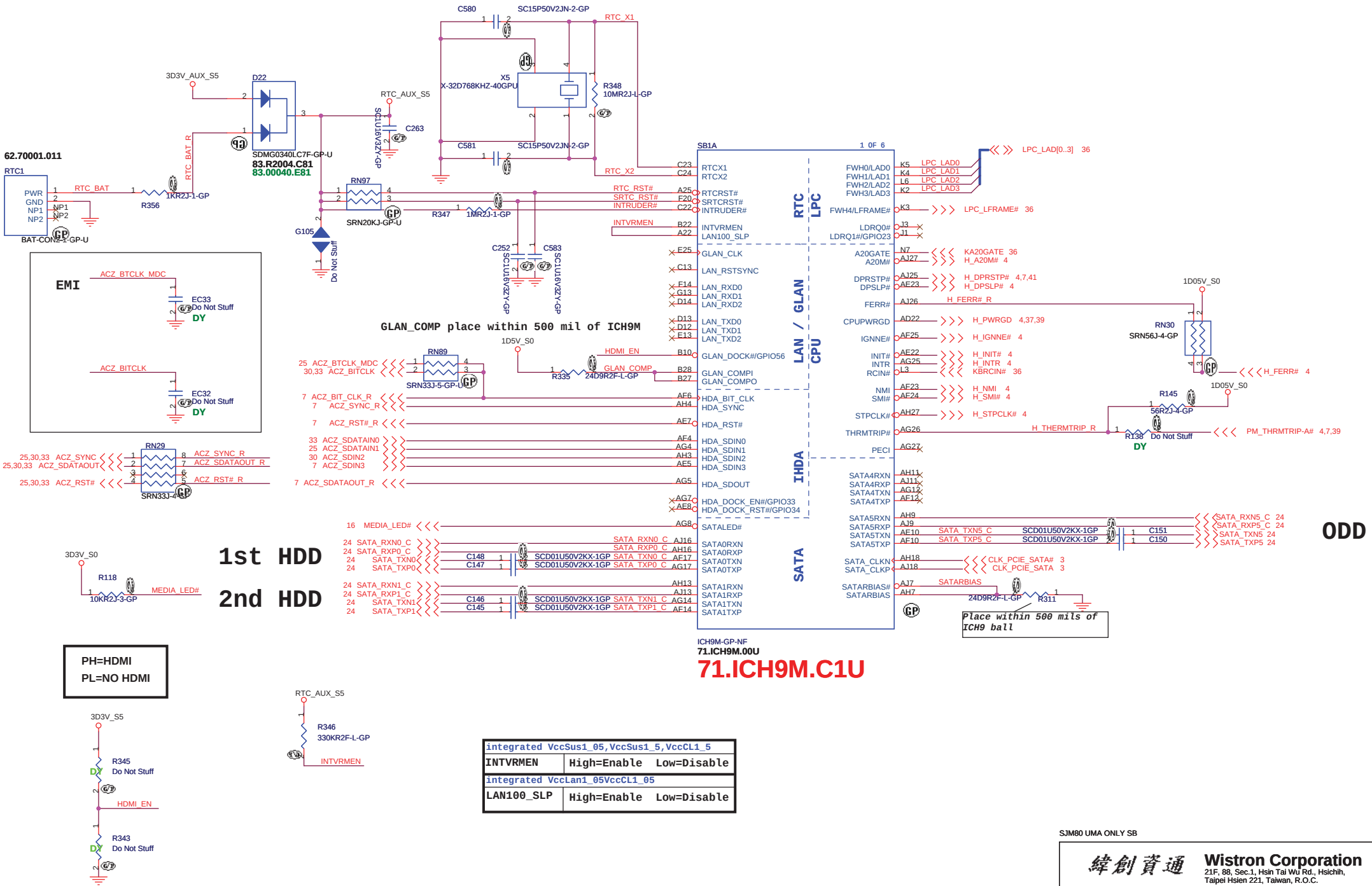
62.70001.011
RTC1
BAT-CON2-1-GP-U
RTC_BAT
R356
1KR2J-1-GP
RTC_BAT_R
D22
SDMG0340LC7F-GP-U
83.R2004.C81
83.00040.E81
3D3V_AUX_S5
RTC_AUX_S5
C263
SC1U16V3ZY-GP
C580
C581
SC15P50V2JN-2-GP
X5
X-32D768KHZ-40GPU
R348
10MR2J-L-GP
RTC_X1
RTC_X2
RN97
SRN20KJ-GP-U
RTC_RST#
SRTC_RST#
INTRUDER#
R347
1MR2J-1-GP
INTVRMEN
G105
Do Not Stuff
C252
C583
SB1A
1 OF 6
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
RTC
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
LAN / GLAN
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
IHDA
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
LPC
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
CPU
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH9M-GP-NF
71.ICH9M.00U
71.ICH9M.C1U
LPC_LAD[0..3] 36
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_LFRAME# 36
KA20GATE 36
H_A20M# 4
H_DPRSTP# 4,7,41
H_DPSLP# 4
H_FERR# R
H_PWRGD 4,37,39
H_IGNNE# 4
H_INIT# 4
H_INTR 4
KBRCIN# 36
H_NMI 4
H_SMI# 4
H_STPCLK# 4
H_THERMTRIP_R
PM_THRMTRIP-A# 4,7,39
SATA_TXN5_C
SATA_TXP5_C
SCD01U50V2KX-1GP
C151
C150
SATA_RXN5_C 24
SATA_RXP5_C 24
SATA_TXN5 24
SATA_TXP5 24
CLK_PCIE_SATA# 3
CLK_PCIE_SATA 3
SATARBIAS
24D9R2F-L-GP
R311
Place within 500 mils of ICH9 ball
1D05V_S0
RN30
SRN56J-4-GP
R145
56R2J-4-GP
R138
Do Not Stuff
DY
EMI
ACZ_BTCLK_MDC
EC33
Do Not Stuff
DY
ACZ_BITCLK
EC32
Do Not Stuff
DY
GLAN_COMP place within 500 mil of ICH9M
RN89
SRN33J-5-GP-U
HDMI_EN
GLAN_COMP
R335
24D9R2F-L-GP
25 ACZ_BTCLK_MDC
30,33 ACZ_BITCLK
7 ACZ_BIT_CLK_R
7 ACZ_SYNC_R
7 ACZ_RST#_R
33 ACZ_SDATAIN0
25 ACZ_SDATAIN1
30 ACZ_SDIN2
7 ACZ_SDIN3
7 ACZ_SDATAOUT_R
RN29
SRN33J-4-GP
25,30,33 ACZ_SYNC
25,30,33 ACZ_SDATAOUT
25,30,33 ACZ_RST#
ACZ_SYNC_R
ACZ_SDATAOUT_R
ACZ_RST#_R
3D3V_S0
R118
10KR2J-3-GP
MEDIA_LED#
16 MEDIA_LED#
1st HDD
2nd HDD
24 SATA_RXN0_C
24 SATA_RXP0_C
24 SATA_TXN0
24 SATA_TXP0
24 SATA_RXN1_C
24 SATA_RXP1_C
24 SATA_TXN1
24 SATA_TXP1
C148
C147
C146
C145
SCD01U50V2KX-1GP
SATA_TXN0_C
SATA_TXP0_C
SATA_TXN1_C
SATA_TXP1_C
ODD
PH=HDMI
PL=NO HDMI
3D3V_S5
R345
DY
Do Not Stuff
HDMI_EN
R343
DY
Do Not Stuff
RTC_AUX_S5
R346
330KR2F-L-GP
INTVRMEN
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN
High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP
High=Enable Low=Disable
SJM80 UMA ONLY SB
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
SJM80
Rev
-1
Date: Monday, May 25, 2009
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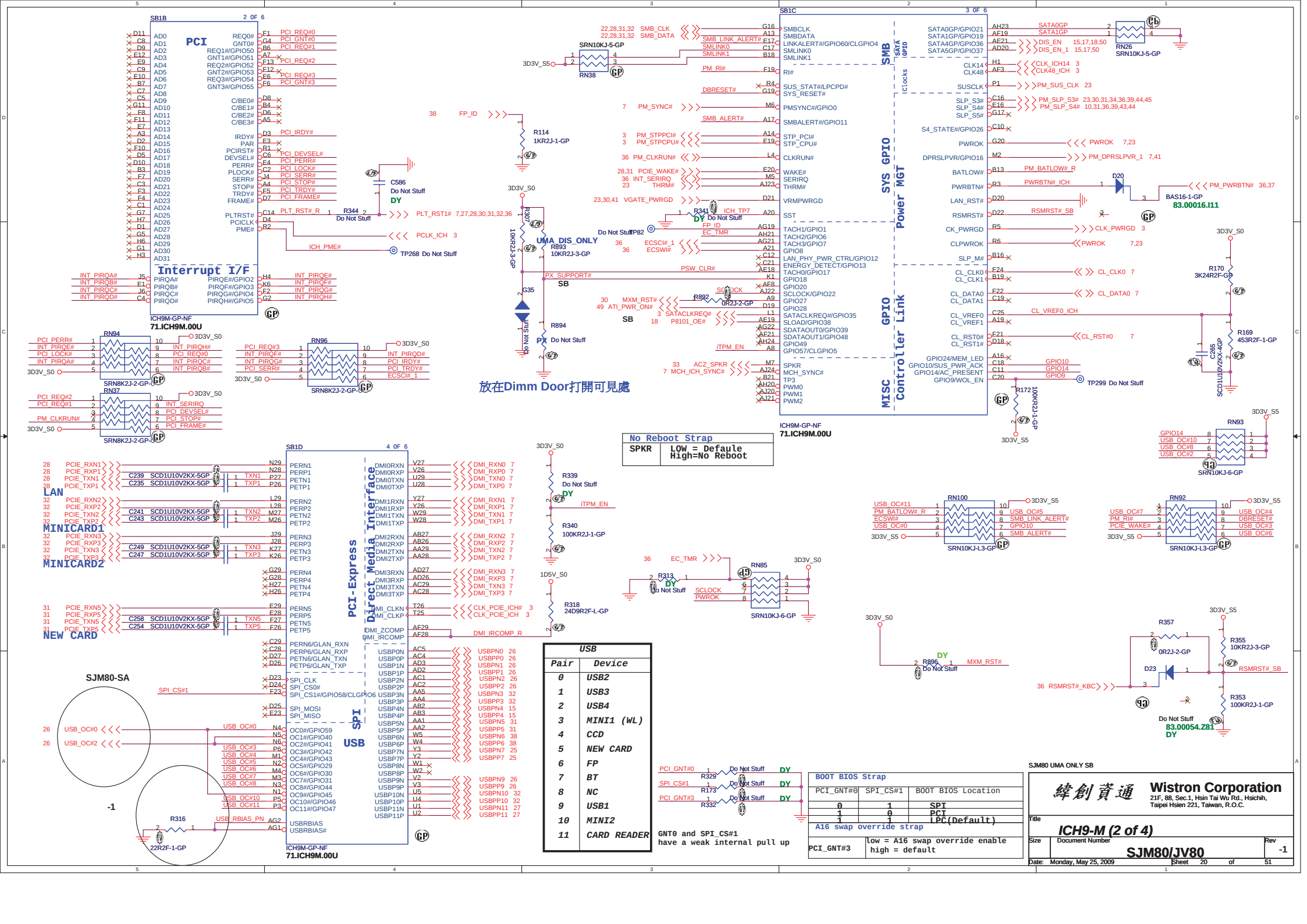
SB1B
2 0F 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB1C
3 0F 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U
SB1D
4 0F 6
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U
LAN
MINICARD1
MINICARD2
NEW CARD
SJM80-SA
放在Dimm Door打開可見處
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
USB
Pair
Device
0
USB2
1
USB3
2
USB4
3
MINI1 (WL)
4
CCD
5
NEW CARD
6
FP
7
BT
8
NC
9
USB1
10
MINI2
11
CARD READER
GNT0 and SPI_CS#1
have a weak internal pull up
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
SJM80 UMA ONLY SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
SJM80/JV80
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-1
Date: Monday, May 25, 2009
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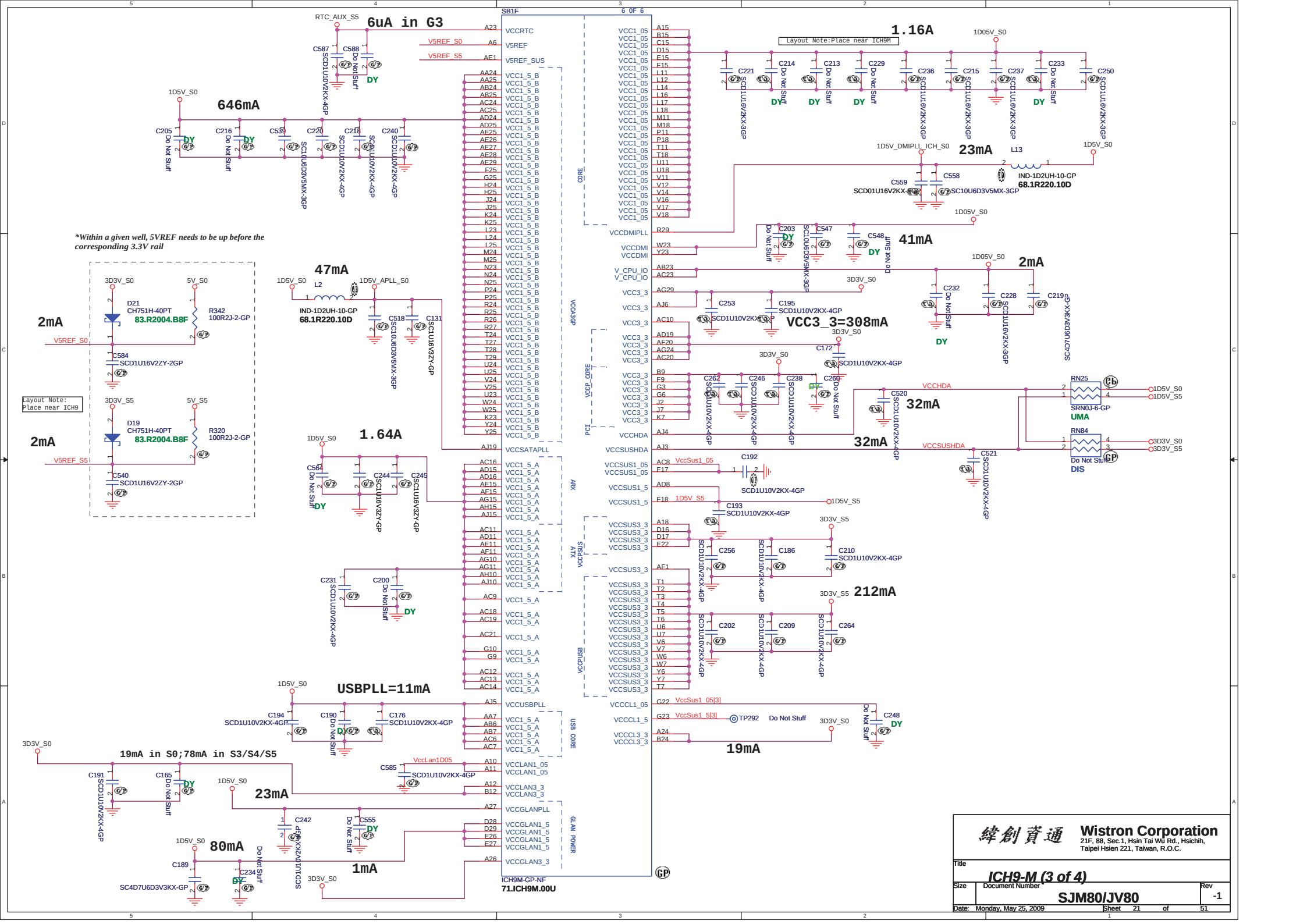
6uA in G3
646mA
1.16A
23mA
41mA
2mA
47mA
1.64A
VCC3_3=308mA
32mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
Do Not Stuff
DY
SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
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-1
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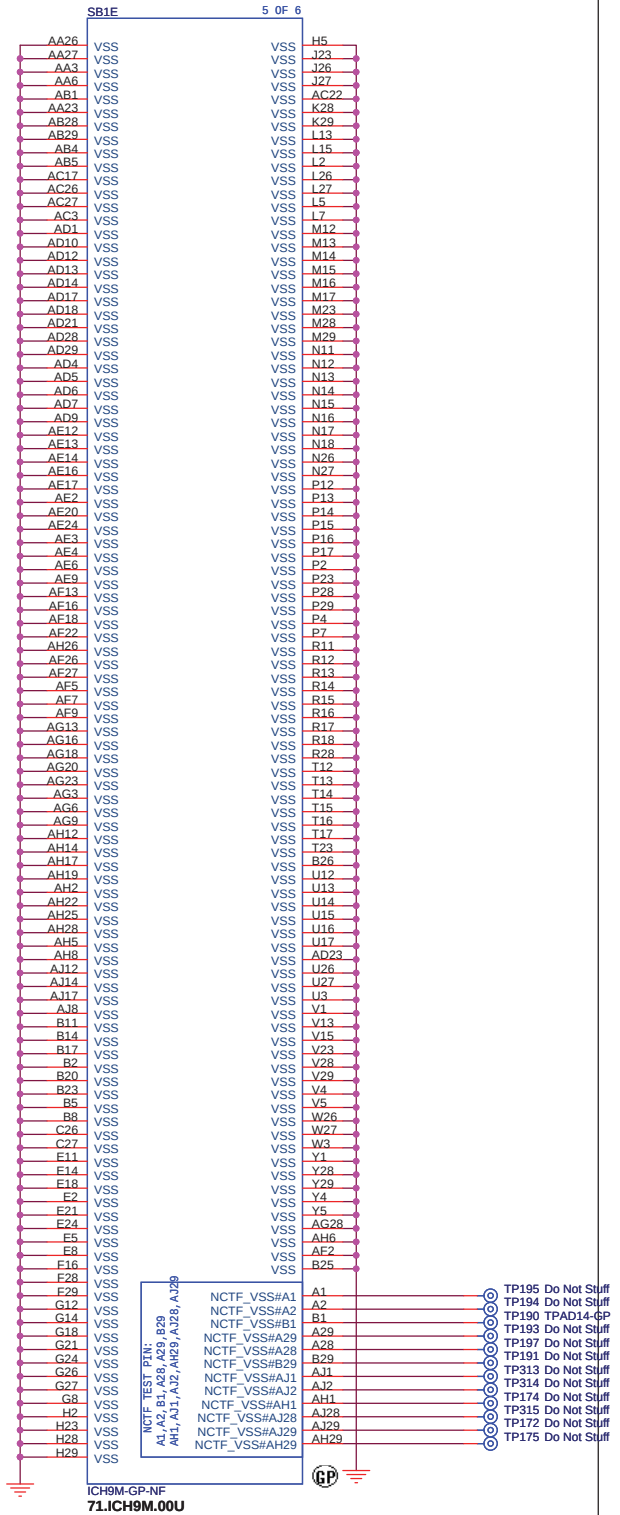

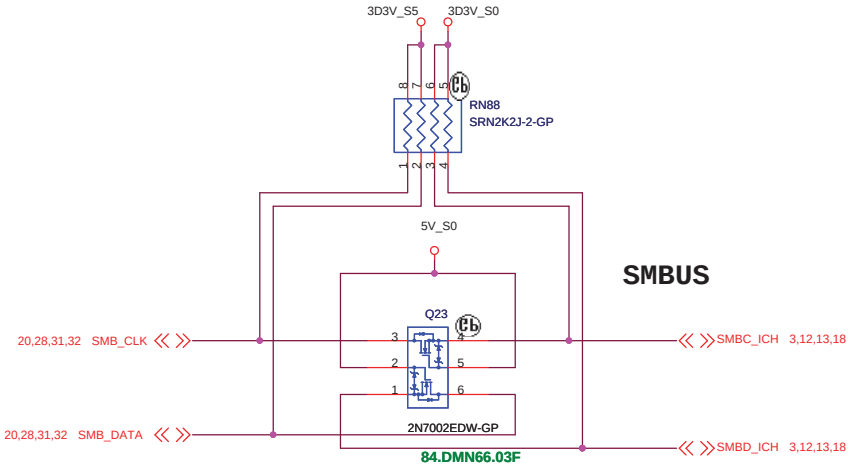

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ICH9-M (4 of 4)*

Size | Document Number: **SJM80/JV80** | Rev: -1

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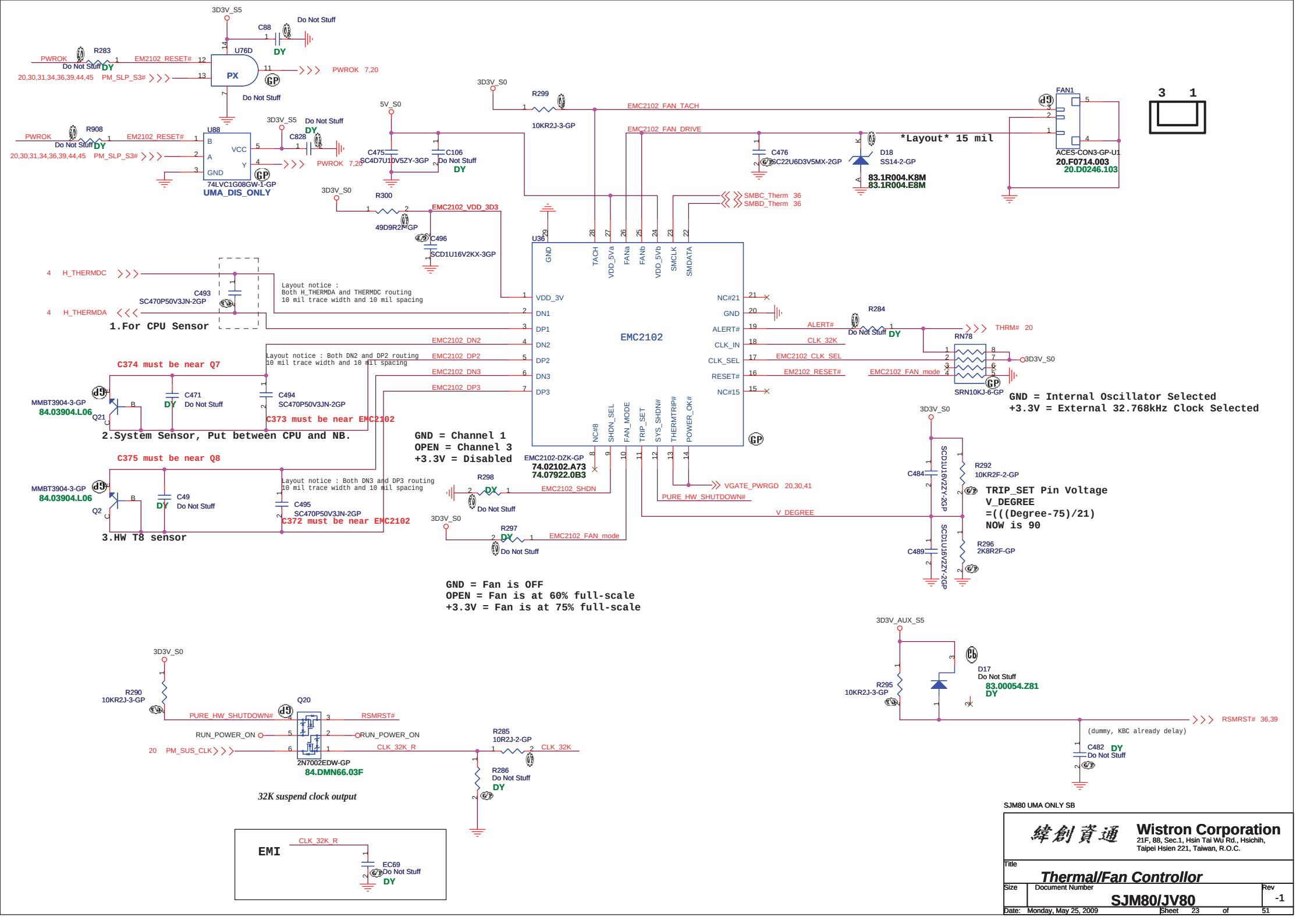
3D3V_S5
C88
Do Not Stuff
DY
U76D
PX
R283
PWROK
EM2102_RESET#
PWROK 7,20
20,30,31,34,36,39,44,45
PM_SLP_S3#
R908
U88
VCC
GND
74LVC1G08GW-1-GP
UMA_DIS_ONLY
C828
5V_S0
C475
SC4D7U10V5ZY-3GP
C106
3D3V_S0
R299
10KR2J-3-GP
EMC2102_FAN_TACH
EMC2102_FAN_DRIVE
C476
SC22U6D3V5MX-2GP
D18
SS14-2-GP
Layout 15 mil
83.1R004.K8M
83.1R004.E8M
FAN1
ACES-CON3-GP-U1
20.F0714.003
20.D0246.103
R300
49D9R2F-GP
EMC2102_VDD_3D3
C496
SCD1U16V2KX-3GP
SMBC_Therm 36
SMBD_Therm 36
U36
EMC2102
GND
TACH
VDD_5Va
FANa
FANb
VDD_5Vb
SMCLK
SMDATA
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#
EMC2102-DZK-GP
74.02102.A73
74.07922.0B3
4 H_THERMDC
4 H_THERMDA
C493
SC470P50V3JN-2GP
Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing
1.For CPU Sensor
R284
Do Not Stuff
THRM# 20
RN78
CLK_32K
EMC2102_CLK_SEL
EM2102_RESET#
EMC2102_FAN_mode
SRN10KJ-6-GP
3D3V_S0
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
EMC2102_DN2
EMC2102_DP2
EMC2102_DN3
EMC2102_DP3
Layout notice : Both DN2 and DP2 routing
10 mil trace width and 10 mil spacing
C374 must be near Q7
MMBT3904-3-GP
84.03904.L06
Q21
C471
C494
SC470P50V3JN-2GP
C373 must be near EMC2102
2.System Sensor, Put between CPU and NB.
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
C375 must be near Q8
Q2
C49
C495
C372 must be near EMC2102
Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing
3.HW T8 sensor
R298
EMC2102_SHDN
R297
EMC2102_FAN_mode
VGATE_PWRGD 20,30,41
PURE_HW_SHUTDOWN#
V_DEGREE
C484
R292
10KR2F-2-GP
C489
R296
2K8R2F-GP
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
NOW is 90
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
3D3V_AUX_S5
D17
Do Not Stuff
83.00054.Z81
R295
10KR2J-3-GP
RSMRST# 36,39
(dummy, KBC already delay)
C482
R290
10KR2J-3-GP
Q20
PURE_HW_SHUTDOWN#
RSMRST#
RUN_POWER_ON
20 PM_SUS_CLK
CLK_32K_R
2N7002EDW-GP
84.DMN66.03F
R285
10R2J-2-GP
CLK_32K
R286
32K suspend clock output
EMI
EC69
SJM80 UMA ONLY SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Document Number
SJM80/JV80
Rev
-1
Date: Monday, May 25, 2009
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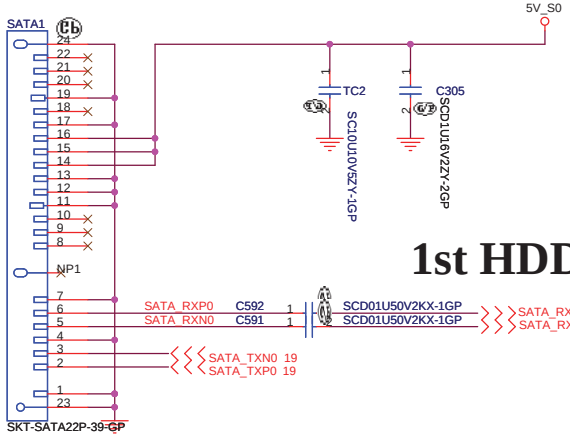
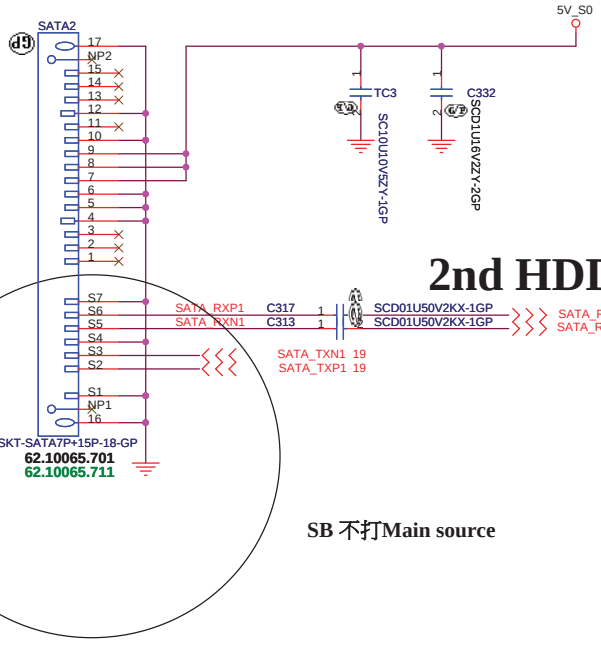


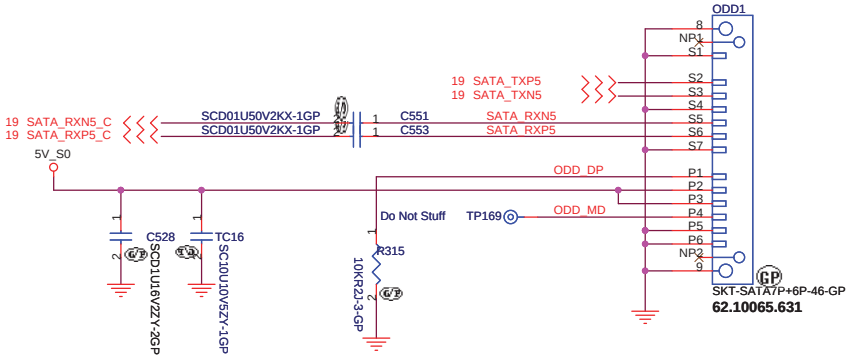
1st HDD SATA Connector



2nd HDD SATA Connector

SB 不打Main source

SATA ODD Connector



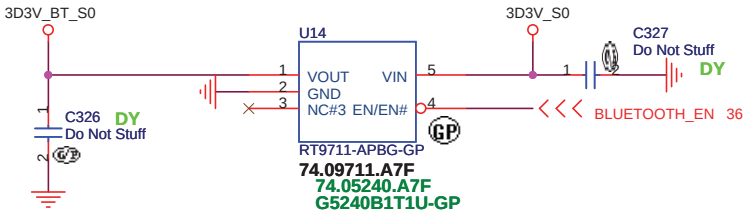
SJM80 UMA ONLY SB

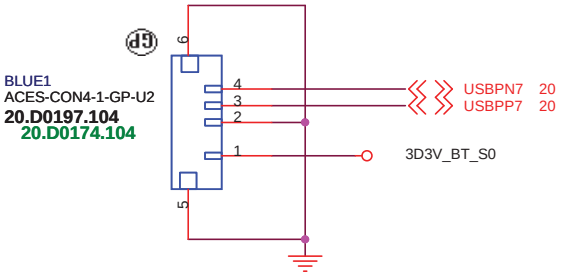
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

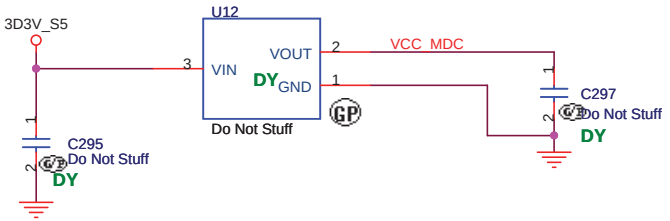
Title	***HDD & ODD***	
Size	Document Number **SJM80/JV80**	Rev -1
Date: Monday, May 25, 2009	Sheet 24 of 51	

BLUETOOTH MODULE

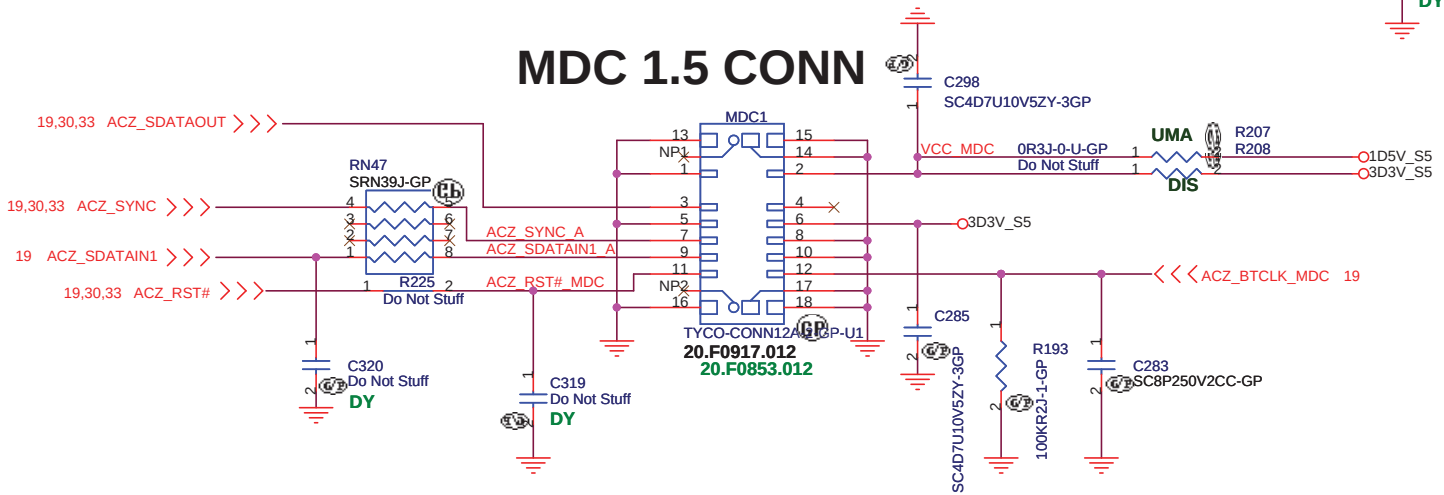
1.5A / High Active Voltage 2V

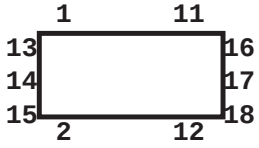






MDC 1.5 CONN





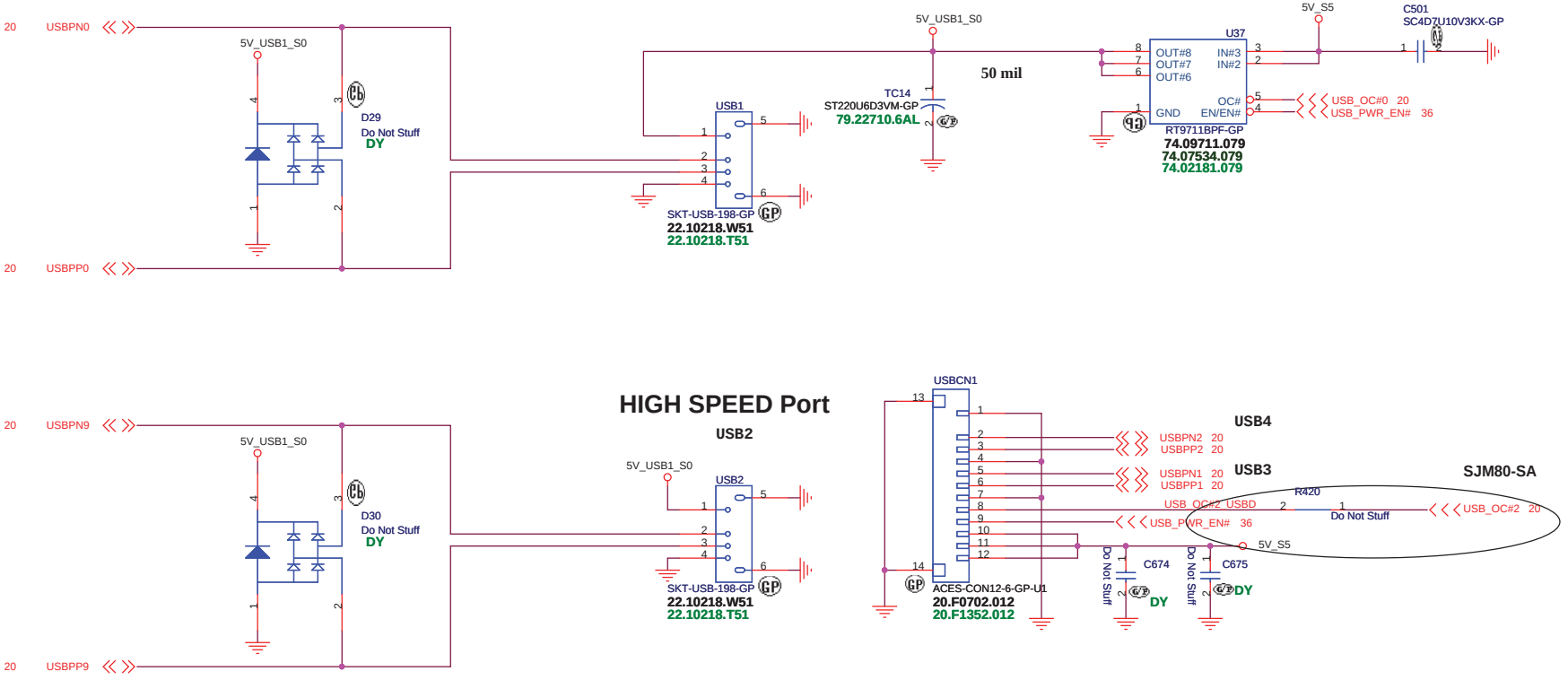
SJM80 UMA ONLY SB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLUETOOTH & MDC***

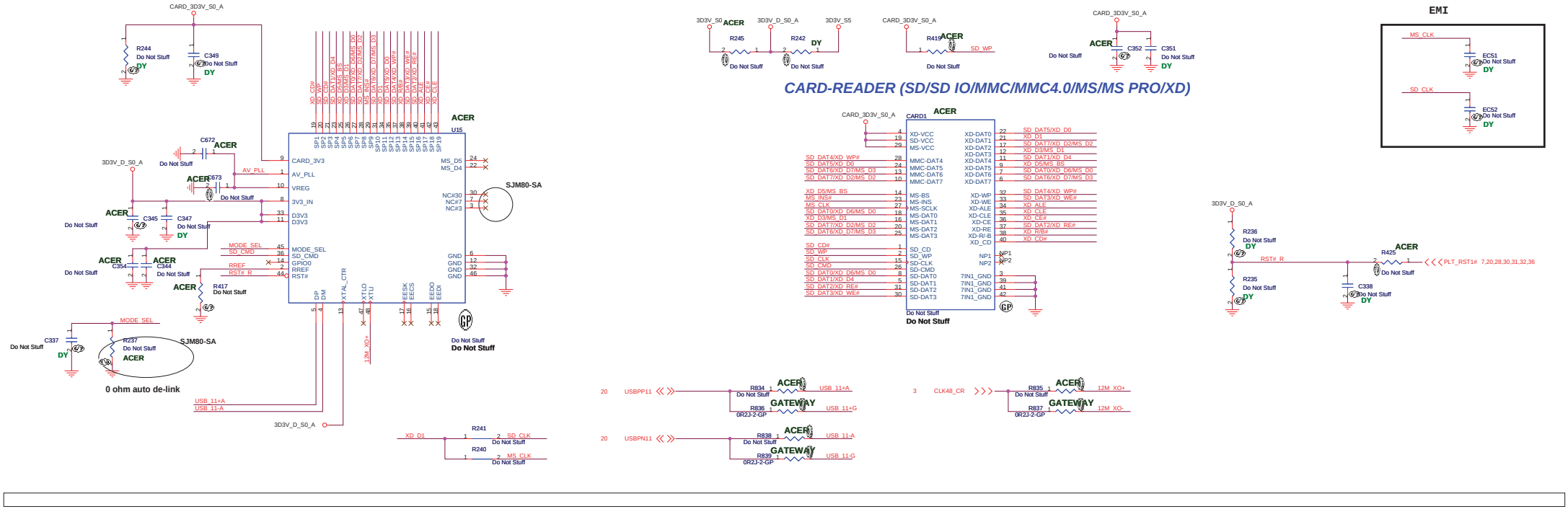
Size	Document Number	Rev
	SJM80/JV80	-1

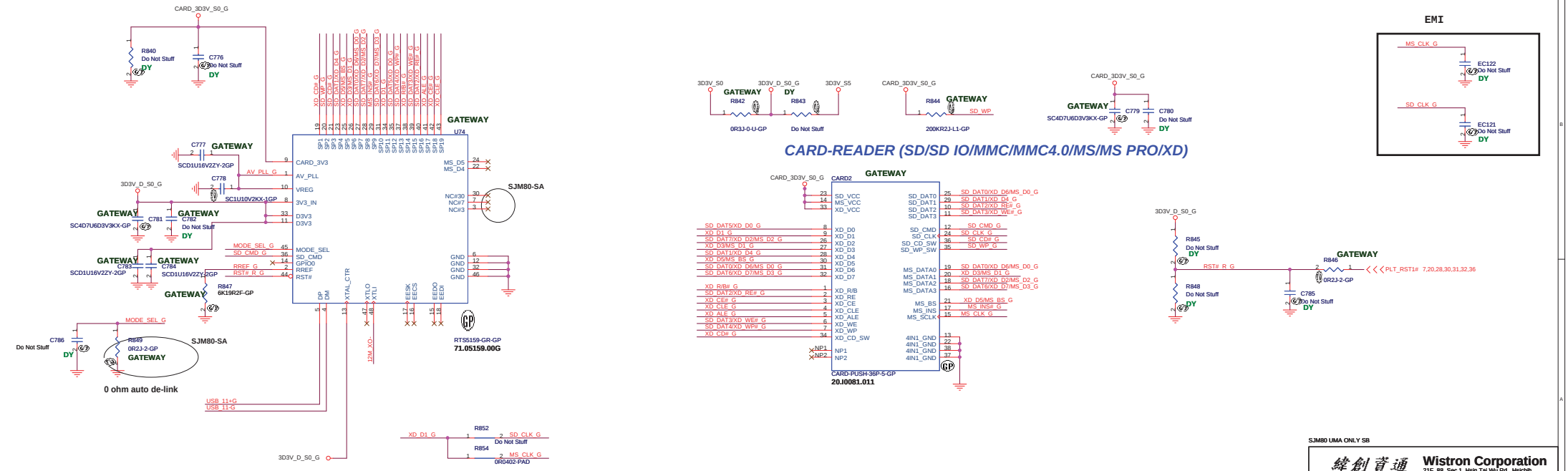
Date: Monday, May 25, 2009 Sheet 25 of 51



SJM80 UMA ONLY SB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB connector**	
Size	Document Number: SJM80/JV80	Rev: -1
Date: Monday, May 25, 2009	Sheet 26 of 51	





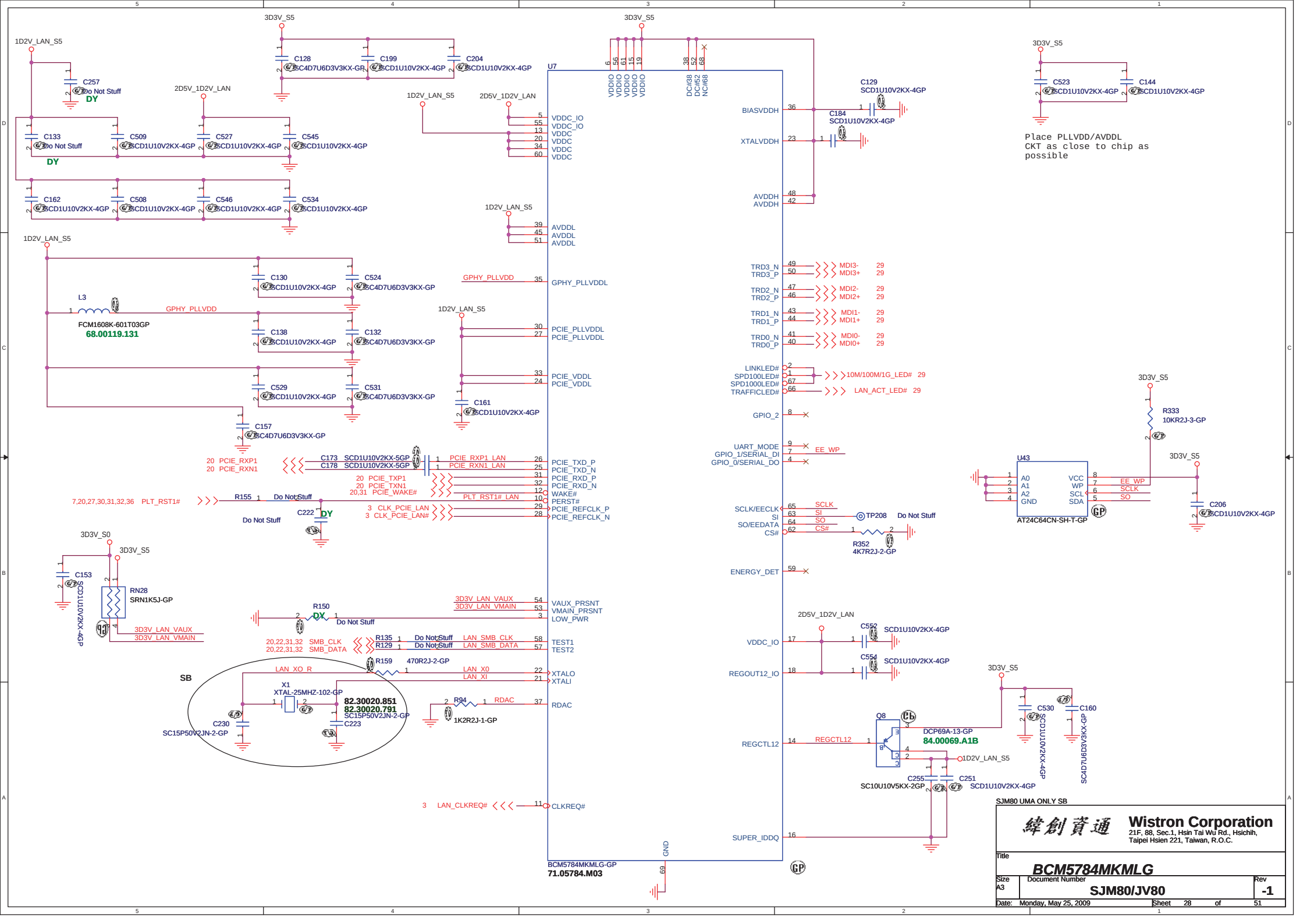
SJM80 UMA ONLY SB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Realtek Card Reader**

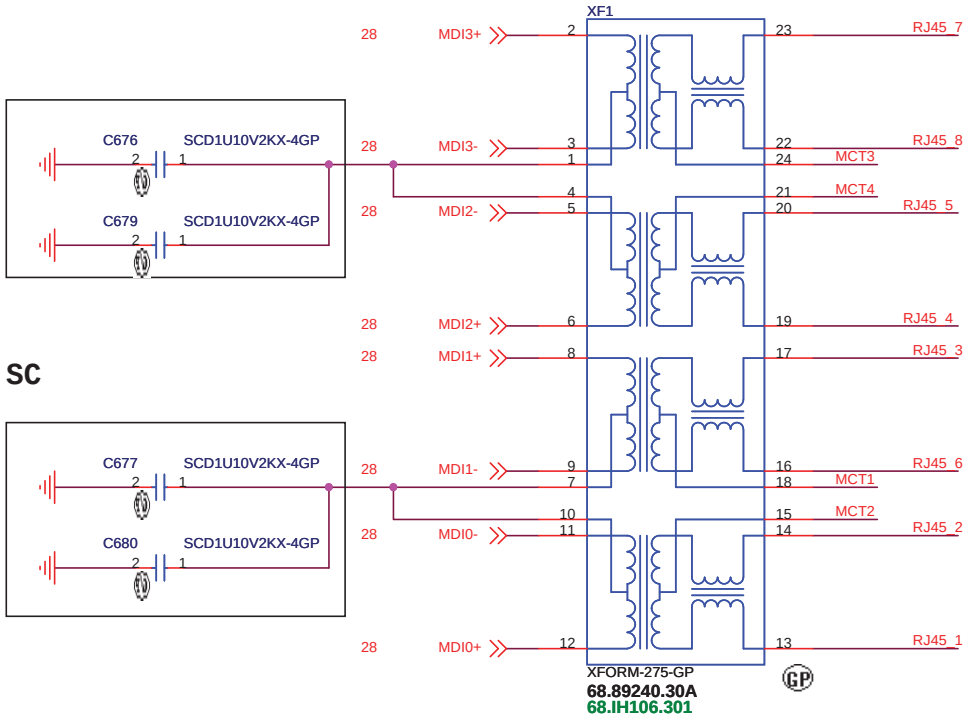
Size	Document Number	Rev
	SJM80/JV80	-1

Date: Monday, May 25, 2009 Sheet 27 of 51

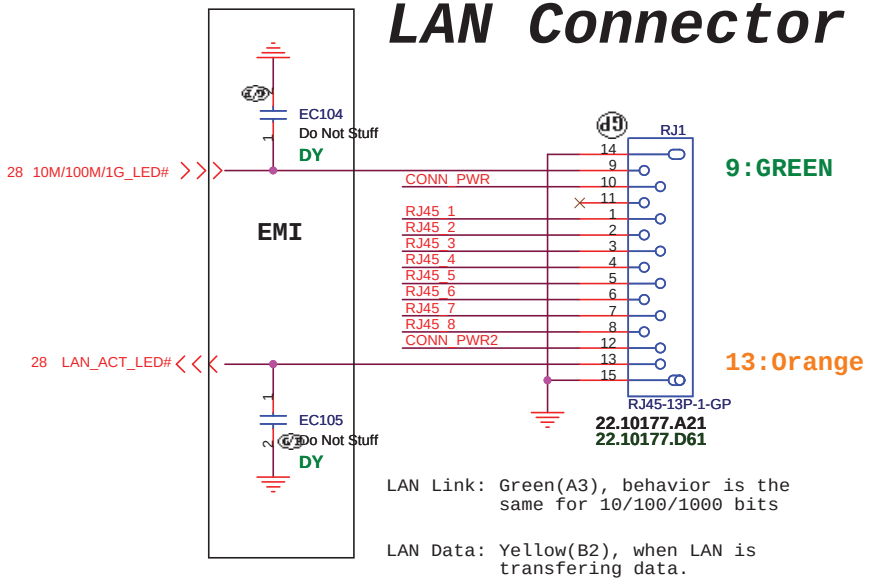

U7
BCM5784MKMLG-GP
71.05784.M03
3D3V_S5
1D2V_LAN_S5
2D5V_1D2V_LAN
3D3V_S0
C257 Do Not Stuff DY
C133 Do Not Stuff DY
C128 SC4D7U6D3V3KX-GP
C199 SCD1U10V2KX-4GP
C204 SCD1U10V2KX-4GP
C509 C527 C545 C162 C508 C546 C534 SCD1U10V2KX-4GP
C130 C524 C138 C132 C529 C531 C157
L3 FCM1608K-601T03GP 68.00119.131
C129 C184 C523 C144 SCD1U10V2KX-4GP
Place PLLVDD/AVDDL CKT as close to chip as possible
VDDC_IO VDDC VDDC VDDC VDDC VDDC
AVDDL AVDDL AVDDL
AVDDH AVDDH
BIASVDDH XTALVDDH
GPHY_PLLVDDL PCIE_PLLVDDL PCIE_VDDL
C161
TRD3_N TRD3_P TRD2_N TRD2_P TRD1_N TRD1_P TRD0_N TRD0_P
MDI3- MDI3+ MDI2- MDI2+ MDI1- MDI1+ MDI0- MDI0+
LINKLED# SPD100LED# SPD1000LED# TRAFFICLED#
10M/100M/1G_LED# LAN_ACT_LED#
GPIO_2 UART_MODE GPIO_1/SERIAL_DI GPIO_0/SERIAL_DO
EE_WP
U43 AT24C64CN-SH-T-GP
R333 10KR2J-3-GP
C206 SCD1U10V2KX-4GP
20 PCIE_RXP1 20 PCIE_RXN1
C173 C178 SCD1U10V2KX-5GP
PCIE_RXP1_LAN PCIE_RXN1_LAN
PCIE_TXD_P PCIE_TXD_N PCIE_RXD_P PCIE_RXD_N
20 PCIE_TXP1 20 PCIE_TXN1 20,31 PCIE_WAKE#
PLT_RST1# PLT_RST1# LAN
WAKE# PERST#
7,20,27,30,31,32,36 PLT_RST1#
R155 Do Not Stuff
C222 DY
3 CLK_PCIE_LAN 3 CLK_PCIE_LAN#
PCIE_REFCLK_P PCIE_REFCLK_N
SCLK/EECLK SI SO/EEDATA CS#
SCLK SI SO CS#
TP208 Do Not Stuff
R352 4K7R2J-2-GP
ENERGY_DET
C153 RN28 SRN1K5J-GP
3D3V_LAN_VAUX 3D3V_LAN_VMAIN
VAUX_PRSNT VMAIN_PRSNT LOW_PWR
R150 DY Do Not Stuff
20,22,31,32 SMB_CLK 20,22,31,32 SMB_DATA
R135 R129 Do Not Stuff
LAN_SMB_CLK LAN_SMB_DATA
TEST1 TEST2
SB
LAN_XO_R R159 470R2J-2-GP
LAN_X0 LAN_XI
XTALO XTALI
X1 XTAL-25MHZ-102-GP
82.30020.851 82.30020.791 SC15P50V2JN-2-GP
C230 SC15P50V2JN-2-GP C223
R94 RDAC 1K2R2J-1-GP
3 LAN_CLKREQ# CLKREQ#
VDDC_IO REGOUT12_IO REGCTL12 SUPER_IDDQ
C552 C554 SCD1U10V2KX-4GP
Q8 DCP69A-13-GP 84.00069.A1B
REGCTL12
C530 C160 C255 C251
SC10U10V5KX-2GP SCD1U10V2KX-4GP SC4D7U6D3V3KX-GP
SJM80 UMA ONLY SB
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title BCM5784MKMLG
Size A3 Document Number SJM80/JV80 Rev -1
Date: Monday, May 25, 2009 Sheet 28 of 51

LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

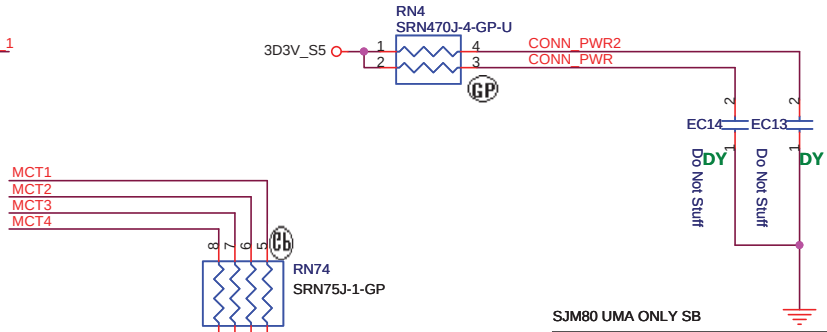


LAN Connector



LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.



SJM80 UMA ONLY SB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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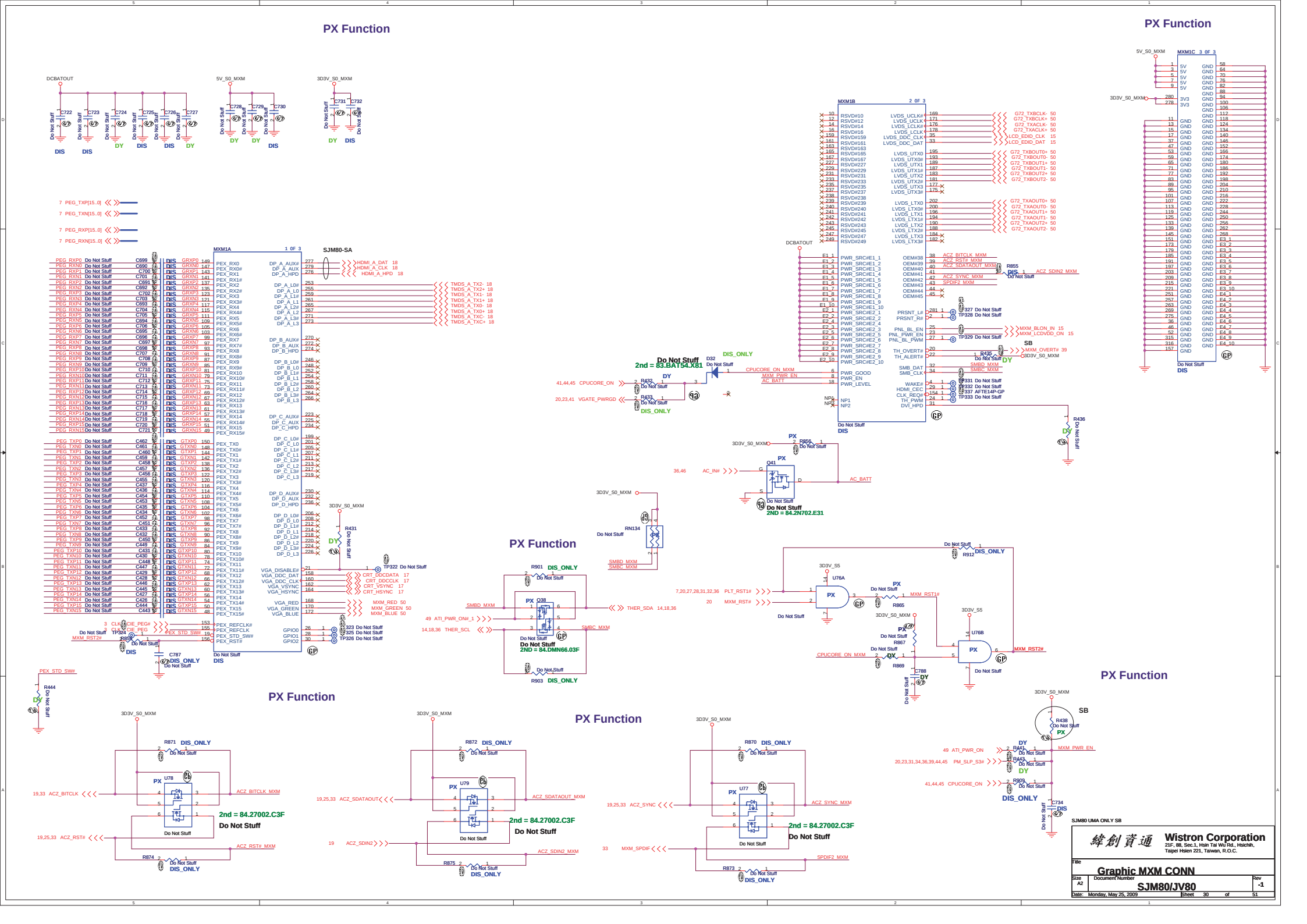
Title	LAN CONN	
Size: Custom	Document Number: SJM80/JV80	Rev: -1
Date: Monday, May 25, 2009	Sheet 29 of 51	


PX Function
PX Function
PX Function
PX Function
PX Function
PX Function
MXM1A
MXM1B
MXM1C
SJM80-SA
DCBATOUT
5V_S0_MXM
3D3V_S0_MXM
SB
DIS
DY
DIS_ONLY
Do Not Stuff
2nd = 83.BAT54.X81
2nd = 84.2N702.E31
2nd = 84.DMN66.03F
2nd = 84.27002.C3F
2nd = 84.27002.C3F
2nd = 84.27002.C3F
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Graphic MXM CONN
SJM80/JV80
Monday, May 25, 2009
30
51

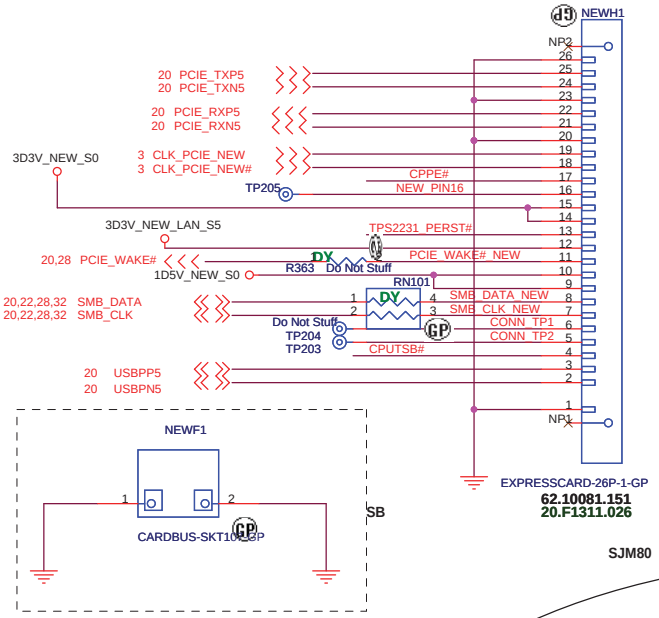
NEWCARD Connector

Reserve the symbol
for bottom side
connector

TOP VIEW

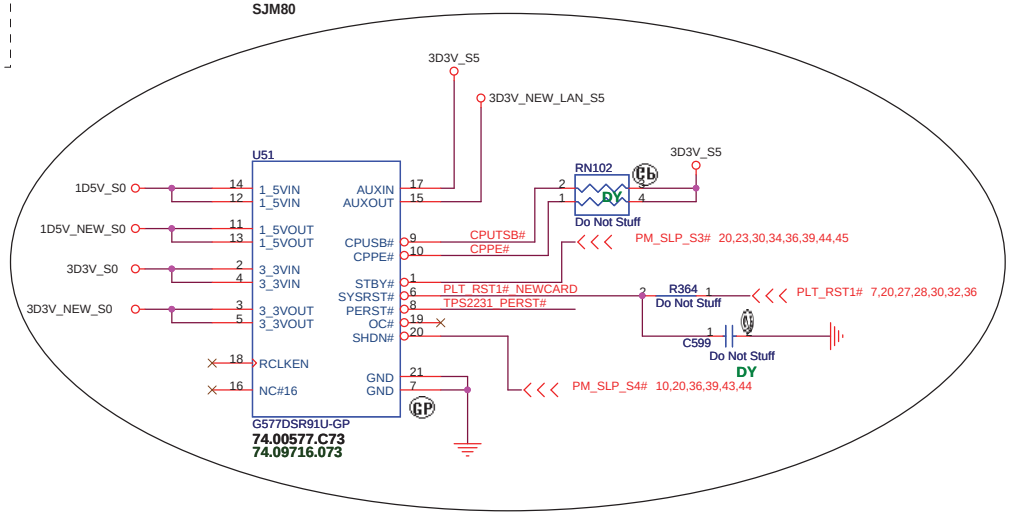
26

1

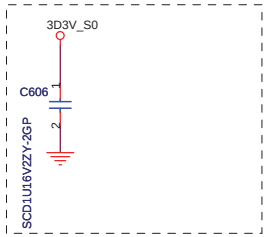


SB

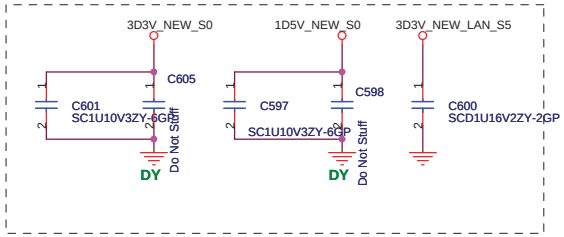
SJM80



Place them Near to Chip



Place them Near to Connector

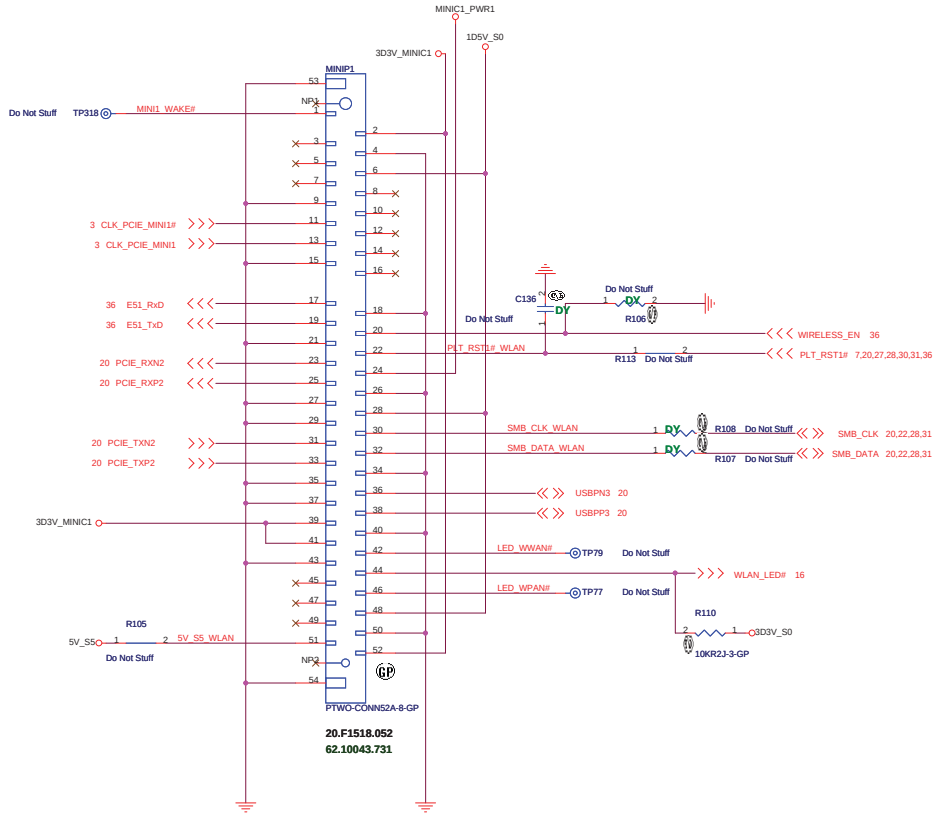


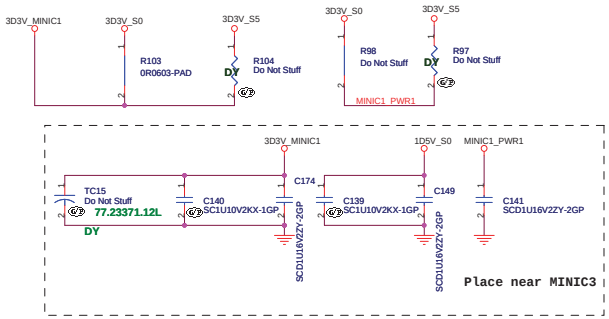
SJM80 UMA ONLY SB

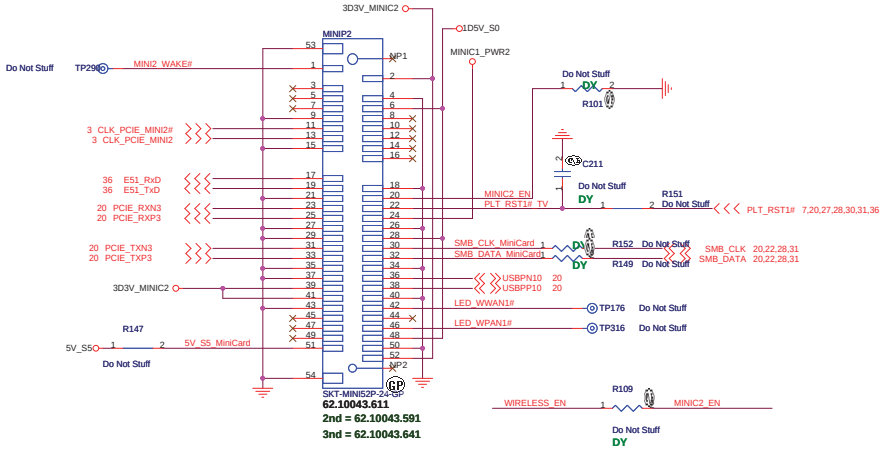
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

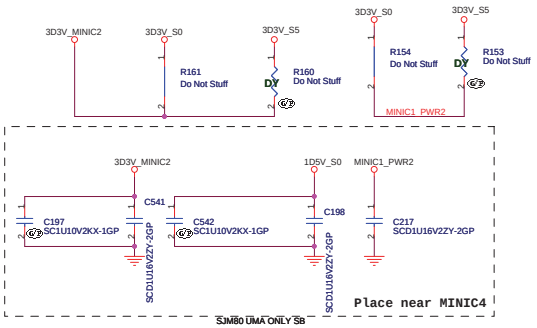
Title	NEW CARD	
Size	Document Number	Rev
	SJM80/JV80	-1
Date: Monday, May 25, 2009	Sheet 31 of 51	

Mini Card Connector(WLAN)



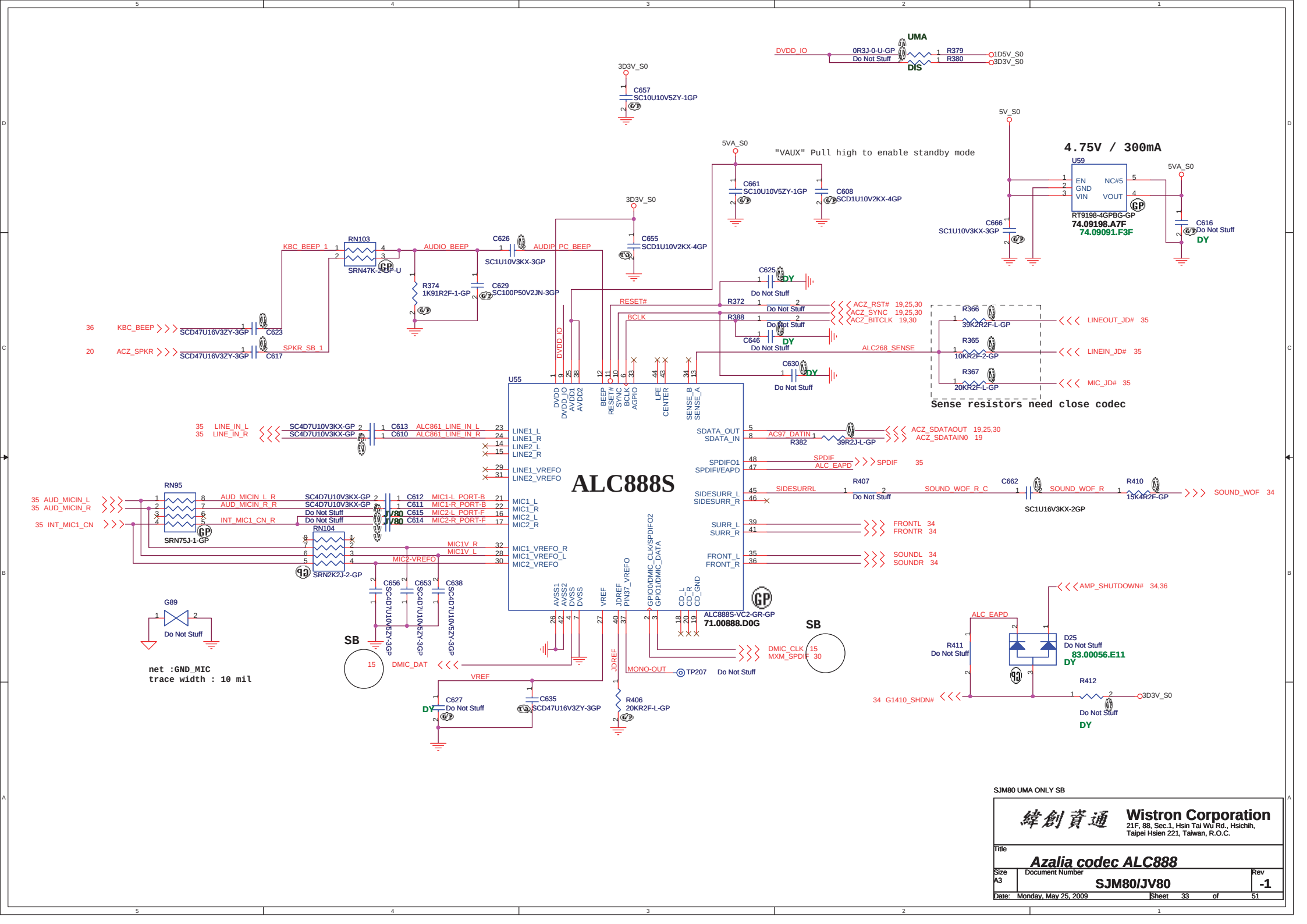






SJM80 UMA ONLY Sb

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size: Custom	Document Number: SJM80/JV80	Rev: -1
Date: Monday, May 25, 2009	Sheet 32 of 51	



SJM80 UMA ONLY SB

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Azalia codec ALC888*		
Size: A3	Document Number: SJM80/JV80	Rev: -1
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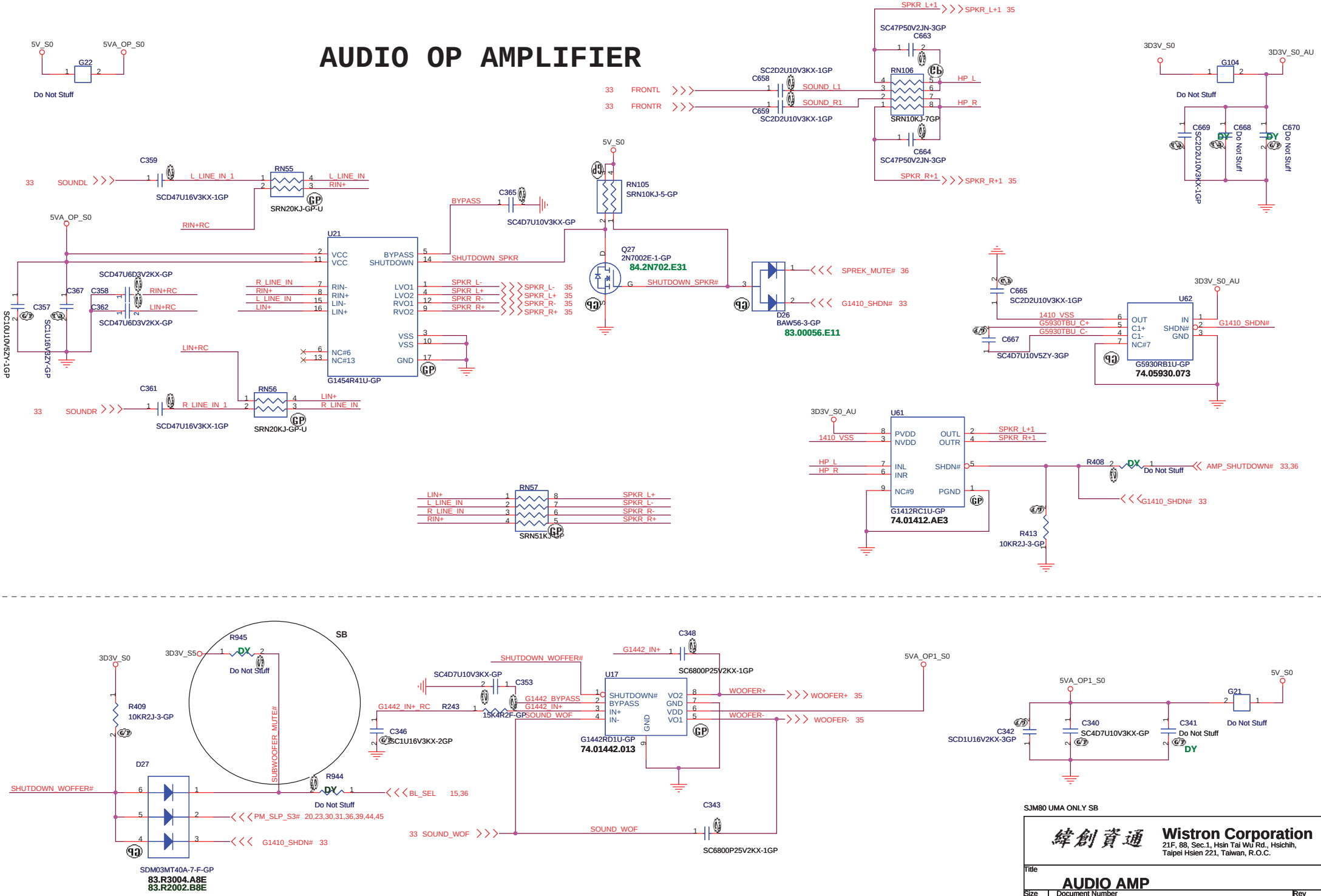
AUDIO OP AMPLIFIER



SJM80 UMA ONLY SB

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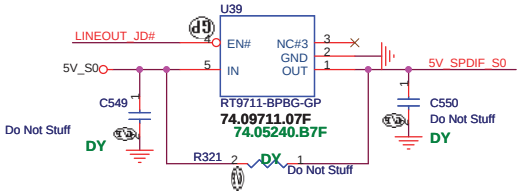
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP**

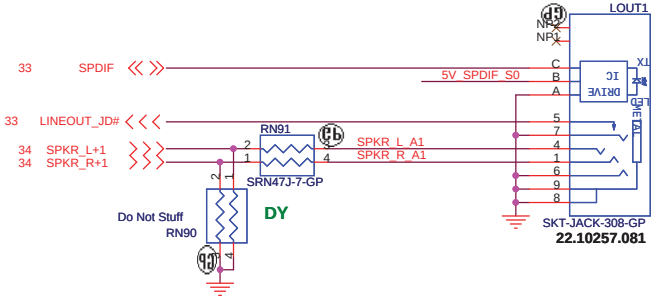
Size	Document Number	Rev
	SJM80/JV80	-1

Date: Monday, May 25, 2009 Sheet 34 of 51

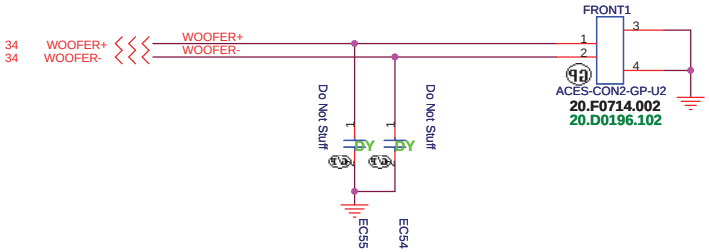


LINE OUT

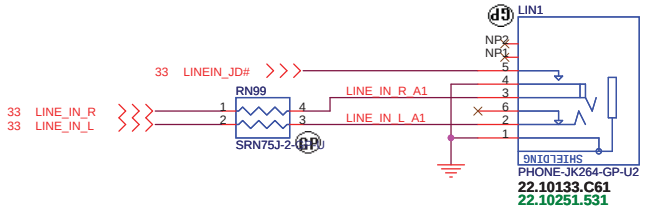
Delete 2nd source



SUBWOOFER

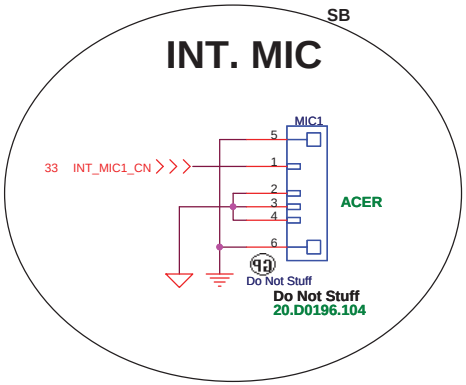


LINE IN

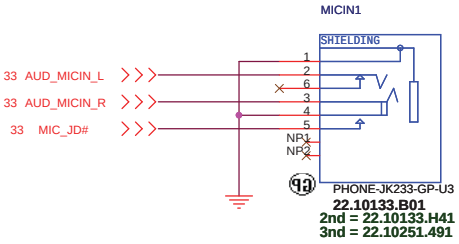


INT. MIC

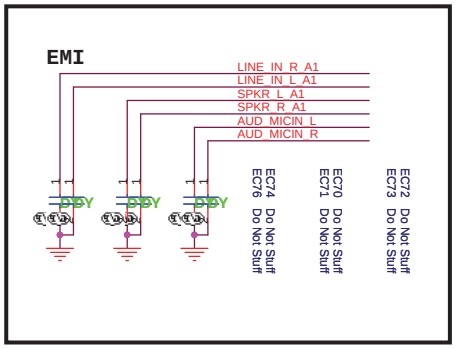
SB



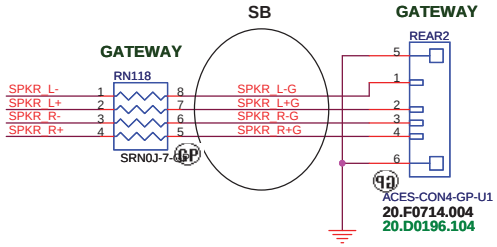
MIC IN

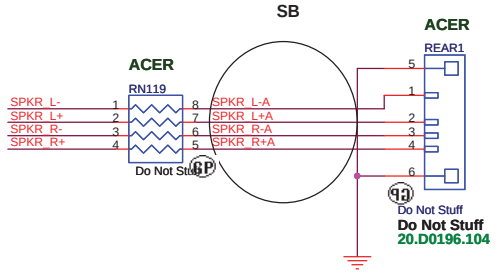


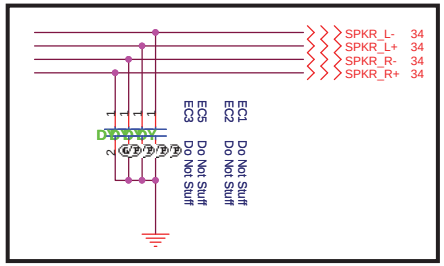
EMI



REAR Speaker







SJM80 UMA ONLY SB

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO_JACK**

Size | Document Number: SJM80/JV80 | Rev: -1

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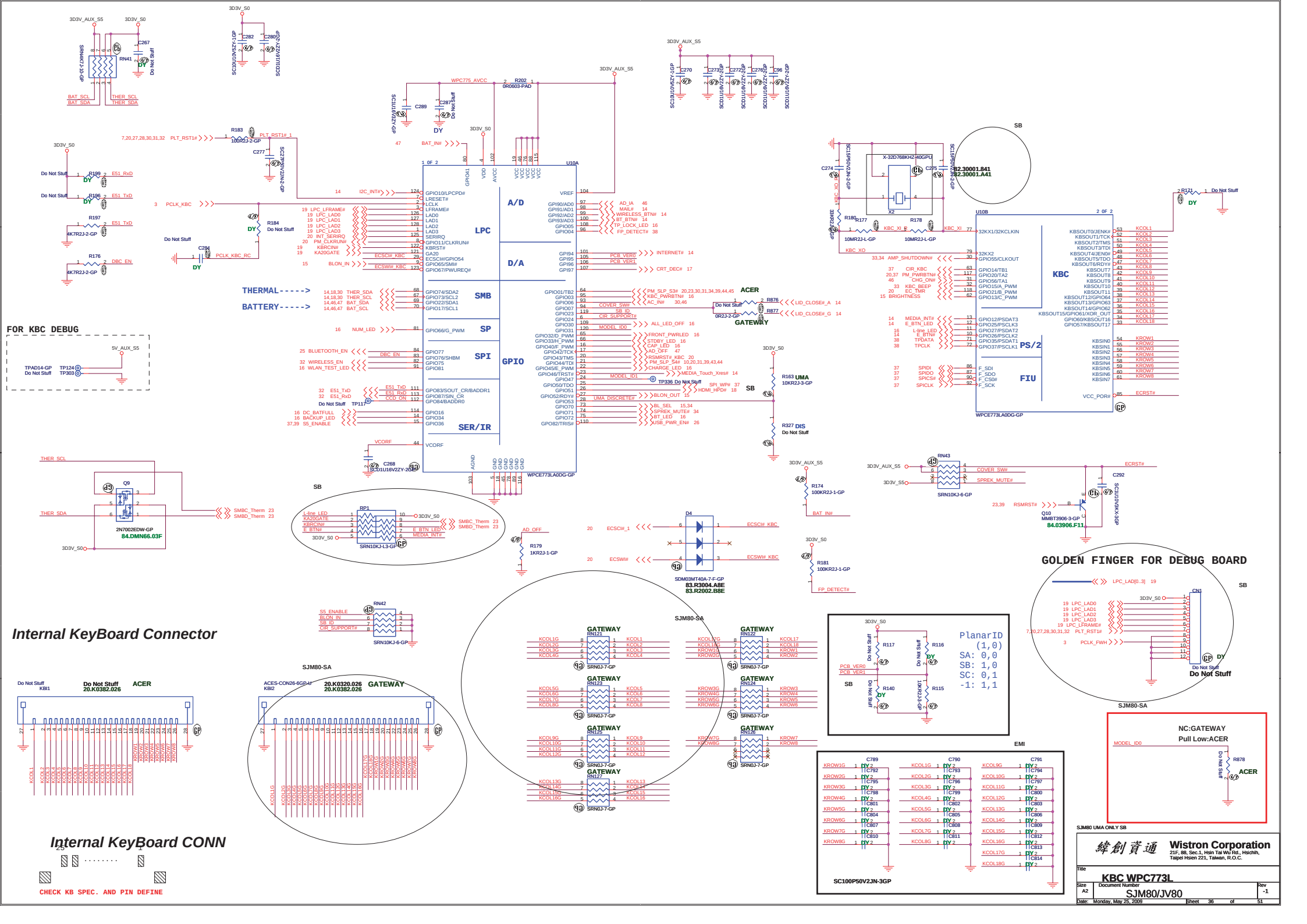
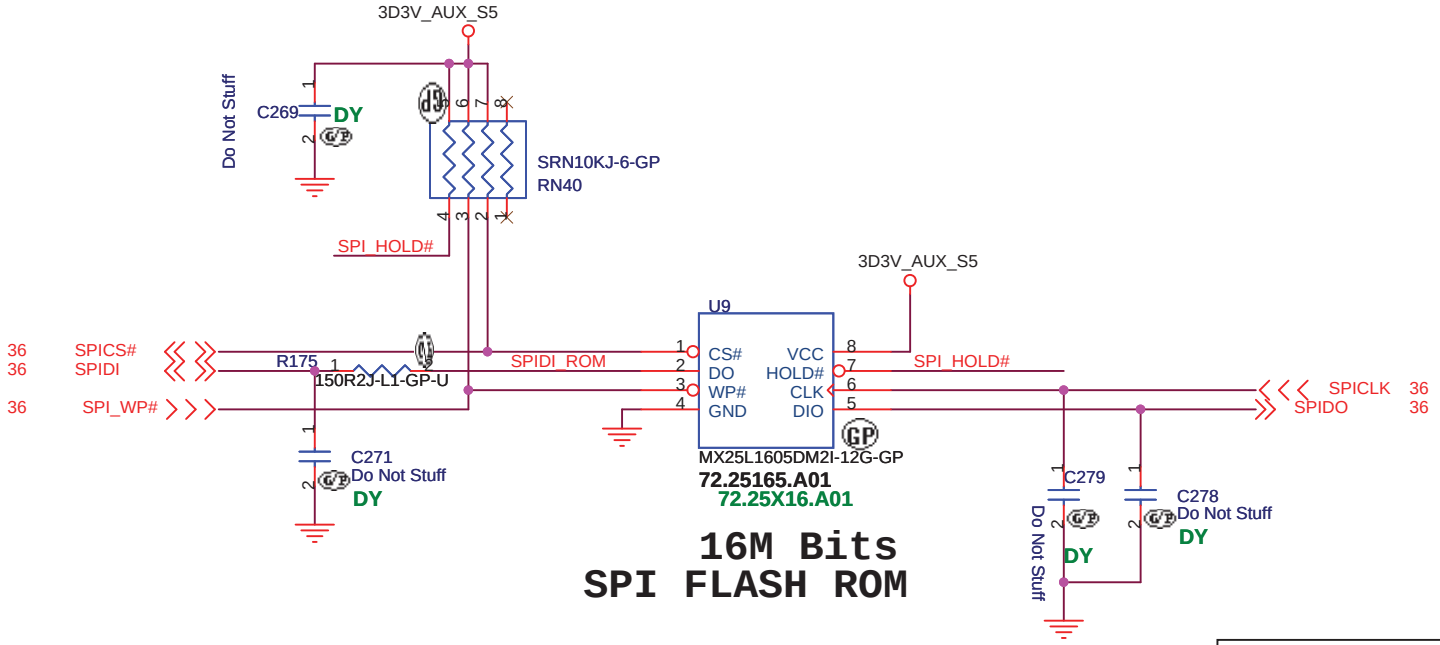
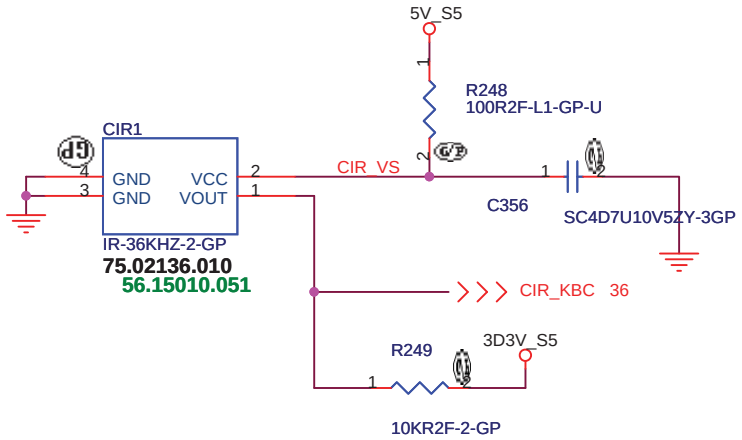

FOR KBC DEBUG
THERMAL-----> SMB
BATTERY-----> SMB
SPI
SP
SER/IR
A/D
D/A
LPC
GPIO
U10A
WPCE773LA0DG-GP
U10B
KBC
PS/2
FIU
ACER
GATEWAY
UMA
DIS
SB
Internal KeyBoard Connector
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
SJM80-SA
GOLDEN FINGER FOR DEBUG BOARD
EMI
PlanarID (1,0)
SA: 0,0
SB: 1,0
SC: 0,1
-1: 1,1
NC:GATEWAY
Pull Low:ACER
SJM80 UMA ONLY SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773L
SJM80/JV80
Monday, May 25, 2009



CIR Module



Check test point

3D3V_S0	TP202 TPAD14-GP
3D3V_AUX_S5	TP141 Do Not Stuff
3D3V_S5	TP120 Do Not Stuff
5V_S5	TP130 Do Not Stuff
20,36 PM_PWRBTN#	TP115 Do Not Stuff
4,19,39 H_PWRGD	TP320 Do Not Stuff
36,39 S5_ENABLE	TP110 Do Not Stuff
4,6 H_CPURST#	TP278 Do Not Stuff

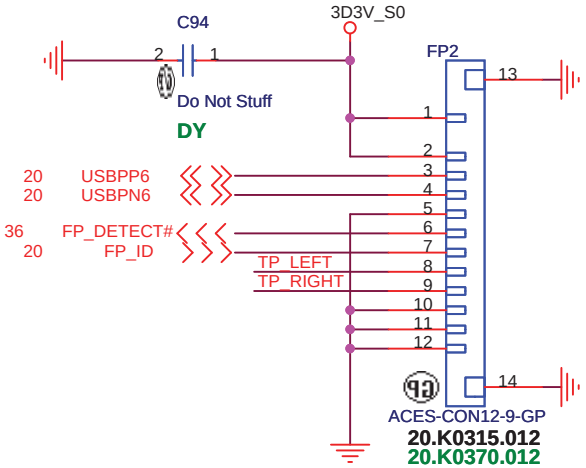
Test Point放在Dimm Door打開可量測處

SJM80 UMA ONLY SB

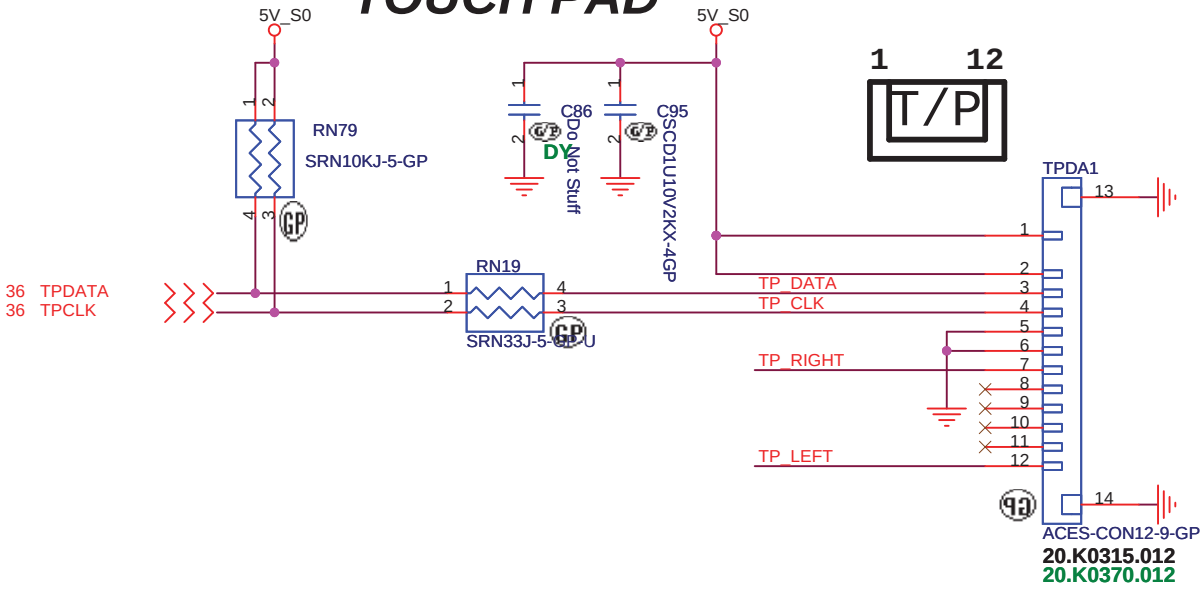
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

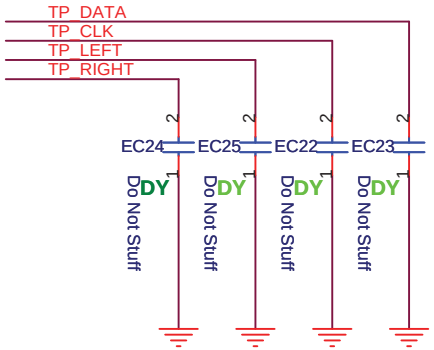
Title: BIOS		
Size	Document Number: SJM80/JV80	Rev: -1
Date: Monday, May 25, 2009	Sheet 37 of 51	

Finger printer



TOUCH PAD





SJM80 UMA ONLY SB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Finger Printer and Touch PAD**

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A4	SJM80/JV80	-1

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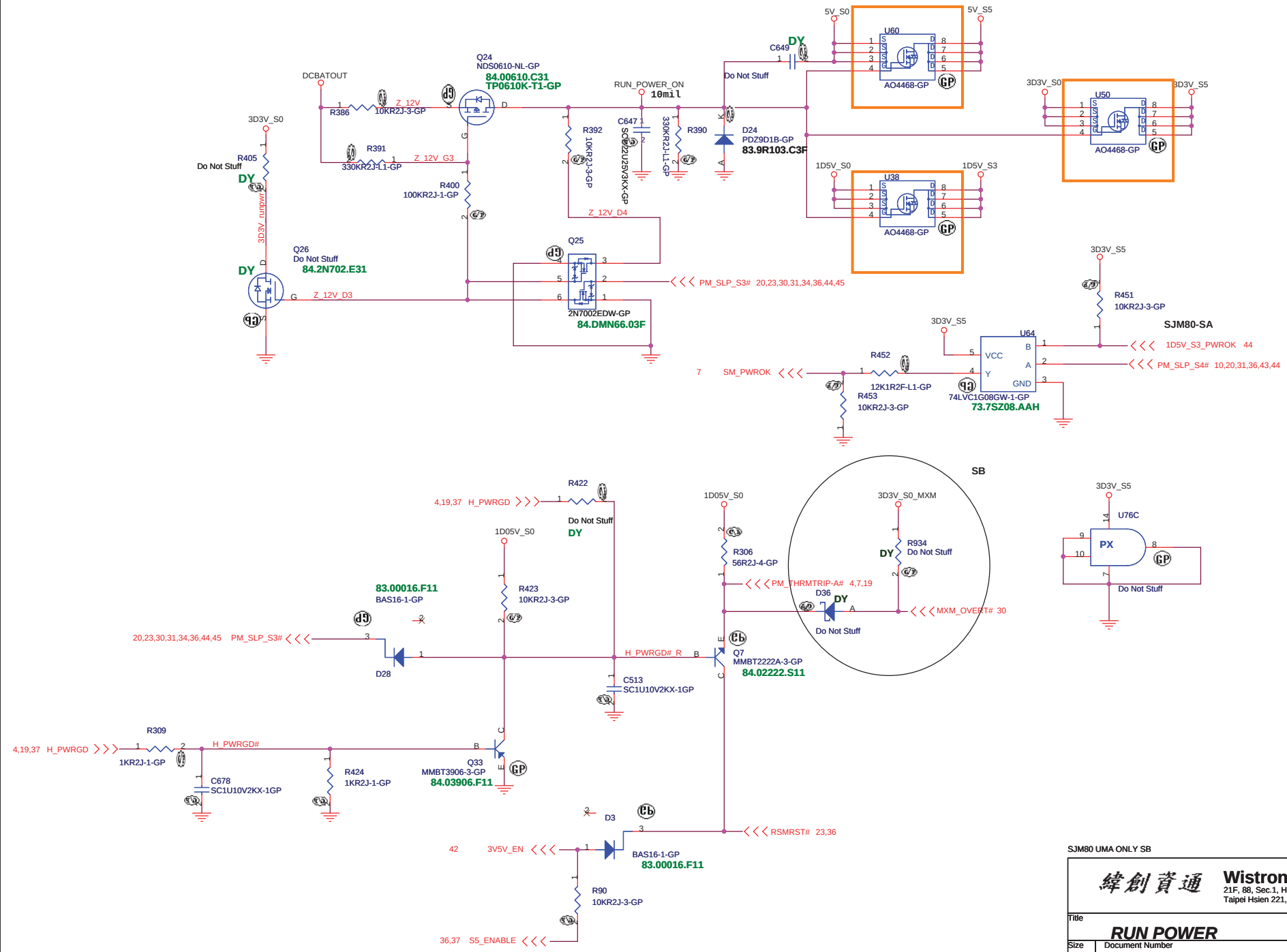
Run Power



SJM80 UMA ONLY SB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER**

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CPU_CORE
ISL6266A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

CPUCORE_ON

Input Signal
EN (I / 3.3V)

VCC_SENSE
VSS_SENSE

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT_6266A
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

VGATE_PWRGD

Output Power
VCC_CORE_PWR(O)

VCC_CORE(Imax=38A)

TPS51125
5V/3D3V

DCBATOUT_51125

PM_SLP_S4#

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

ALW_PWRGD_3V_5V

Output Power
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (6A)

TPS51124
1D5V_S0

1D5V_S3
PM_SLP_S3#

VIN
EN

1D5V(O)
PGOOD

1D5V_S0 (2.5A)
CPUCORE_ON

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

5V_S0
DCBATOUT

Input Power
VDD
VIN

PM_SLP_S3#
GFXVR_EN

Input Signal
VR_ON

VCC_AXG_SENSE
VSS_AXG_SENSE

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

CPUCORE_ON

Output Power
VGFXCORE (O)

VCC_GFXCORE(5.5A)

RT9026
0D75V_S0

5V_S5
1D5V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5

VTT
VTTREF

0D75V_S3 (1A)
0D75V_S3_1

MAX8731A

CHG_ON#
24750_CELLS

Input Signal
CHGEN#
CELLS

Output Signal
ACGOOD#
SRSET

AC_IN#
AD_IA

AD+

Input Power
ACN

Output Power
VOUT (O)
VOUT (O)

BT+
DCBATOUT

TPS51124
1D8V/1D05V

5V_S5
DCBATOUT_51124

Input Power
VDD
VCC

Output Power
1D8V (O)
1D05V(O)

1D5V_S3 (10A)
1D05V_S0 (15A)

PM_SLP_S4#
PM_SLP_S3#

Input Signal
EN1
EN2

CPUCORE_ON

Output Signal
PGOOD1
PGOOD2

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

SJM80 UMA ONLY SB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Sequence Logic**

Size: B | Document Number: SJM80/JV80 | Rev: -1

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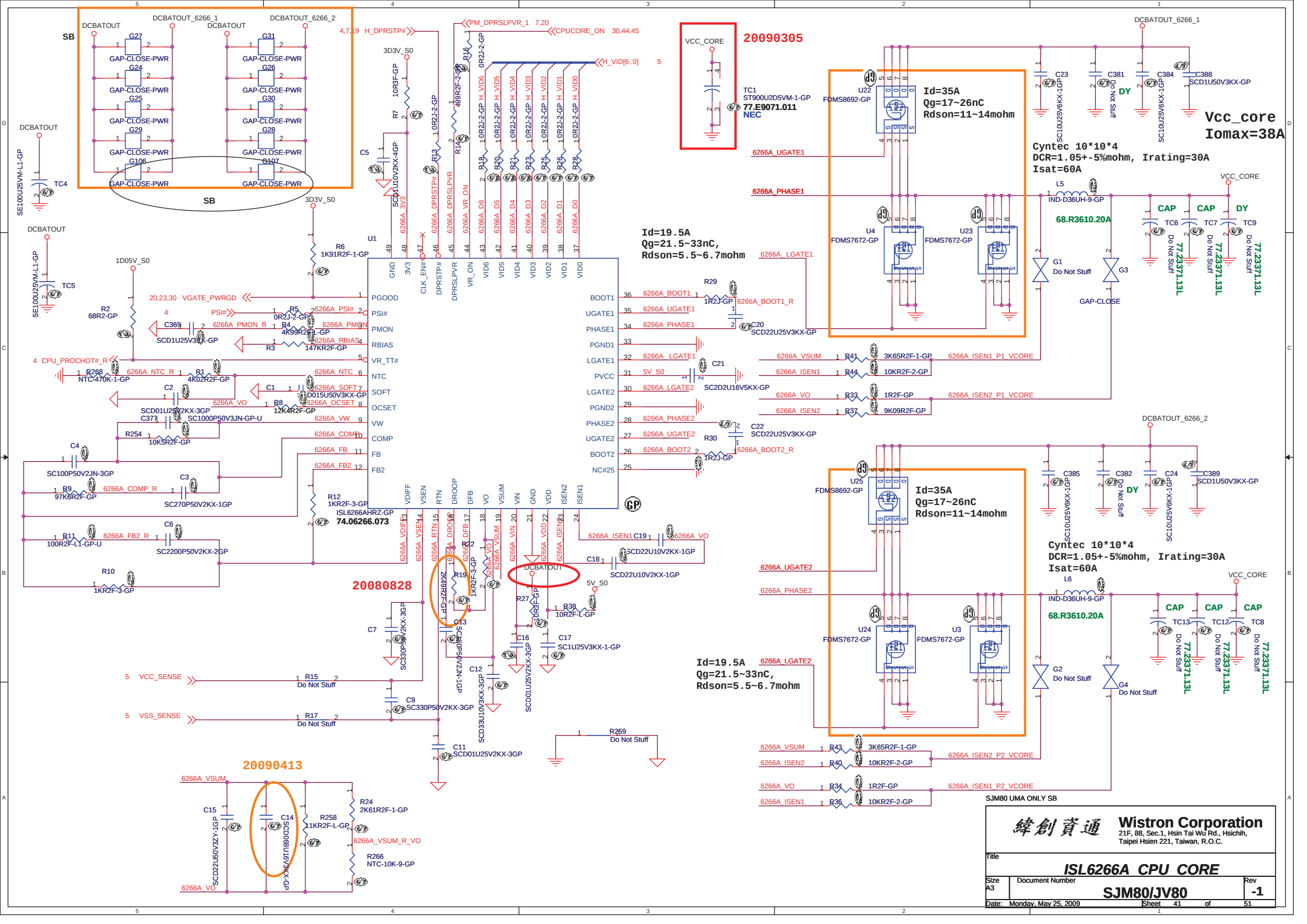
SB
DCBATOUT_6266_1
DCBATOUT_6266_2
GAP-CLOSE-PWR
20090305
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
20080828
20090413
SJM80 UMA ONLY SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A CPU CORE
SJM80/JV80
-1
Monday, May 25, 2009
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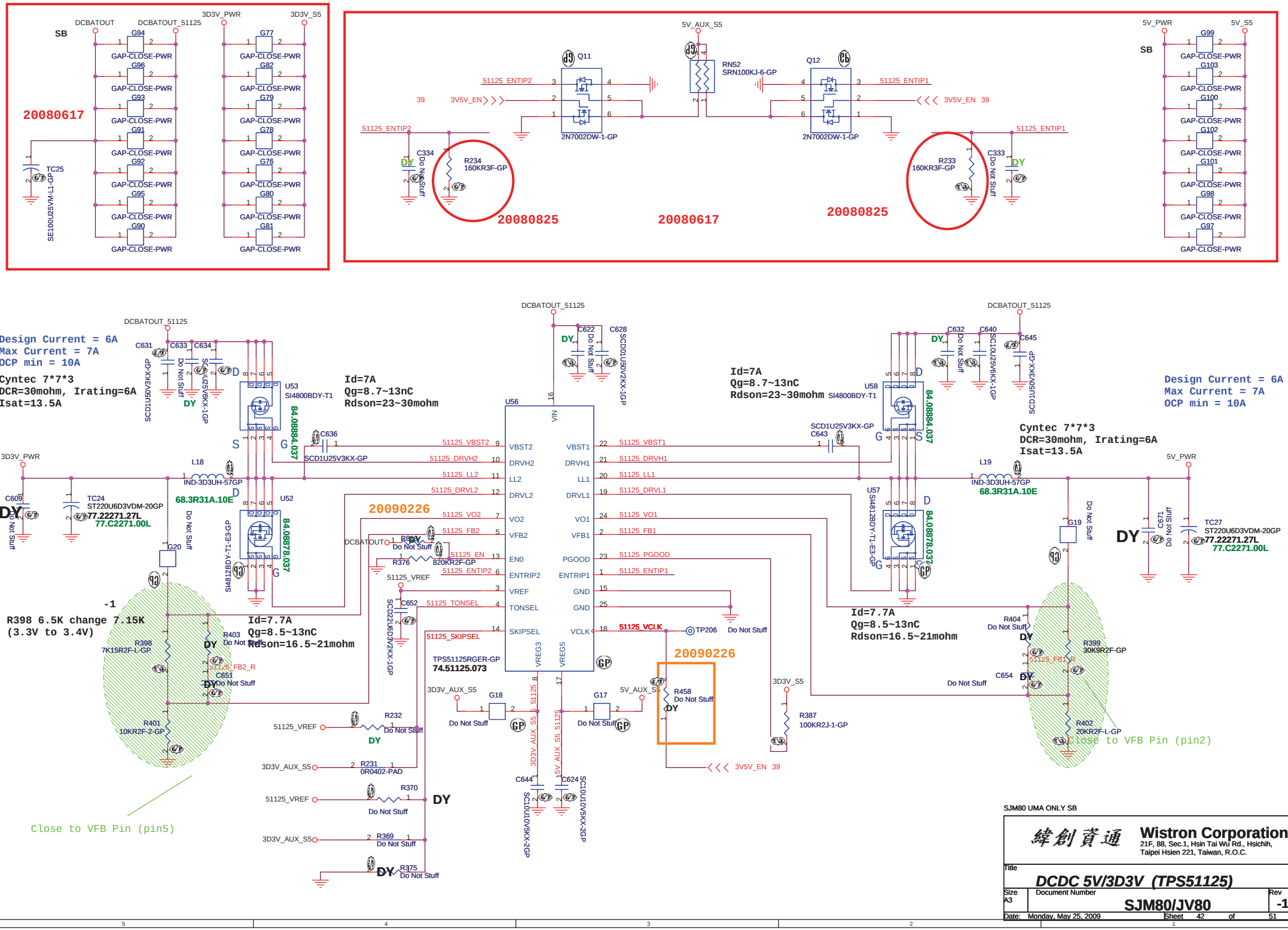
SB
DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
20080617
TC25
SE100U025VM-T1-GP
GAP-CLOSE-PWR
5V_AUX_S5
Q11
Q12
RN52
SRN100KJ-6-GP
2N7002DW-1-GP
51125_ENTIP2
51125_ENTIP1
3V5V_EN
R234
160KR3F-GP
R233
C334
C333
Do Not Stuff
DY
20080825
5V_PWR
5V_S5
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
U53
SI4800BDY-T1
84.08884.037
U58
U56
TPS51125RGER-GP
74.51125.073
VIN
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VREG3
VREG5
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
ENTRIP1
GND
VCLK
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_VREF
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_PGOOD
51125_ENTIP1
51125_VCLK
L18
L19
IND-3D3UH-57GP
68.3R31A.10E
TC24
TC27
ST220U6D3VDM-20GP
77.22271.27L
77.C2271.00L
U52
U57
SI4812BDY-T1-E3-GP
84.08878.037
20090226
R398
7K15R2F-L-GP
R403
R401
10KR2F-2-GP
R404
R399
30K9R2F-GP
R402
20KR2F-L-GP
R376
820KR2F-GP
R458
R387
100KR2J-1-GP
R232
R231
0R0402-PAD
R370
R369
R375
C652
SCD22U6D3V2KX-1GP
C644
C624
SCD10U10V5KX-2GP
C622
C628
SCD01U50V2KX-1GP
C632
C640
C645
SCD10U25V6KX-1GP
SCD1U50V3KX-1GP
SCD1U25V3KX-GP
SCD1U25V6KX-1GP
C609
C631
C633
C634
C636
C643
C671
G17
G18
G19
G20
TP206
-1
R398 6.5K change 7.15K
(3.3V to 3.4V)
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
SJM80 UMA ONLY SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (TPS51125)
Size
A3
Document Number
SJM80/JV80
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-1
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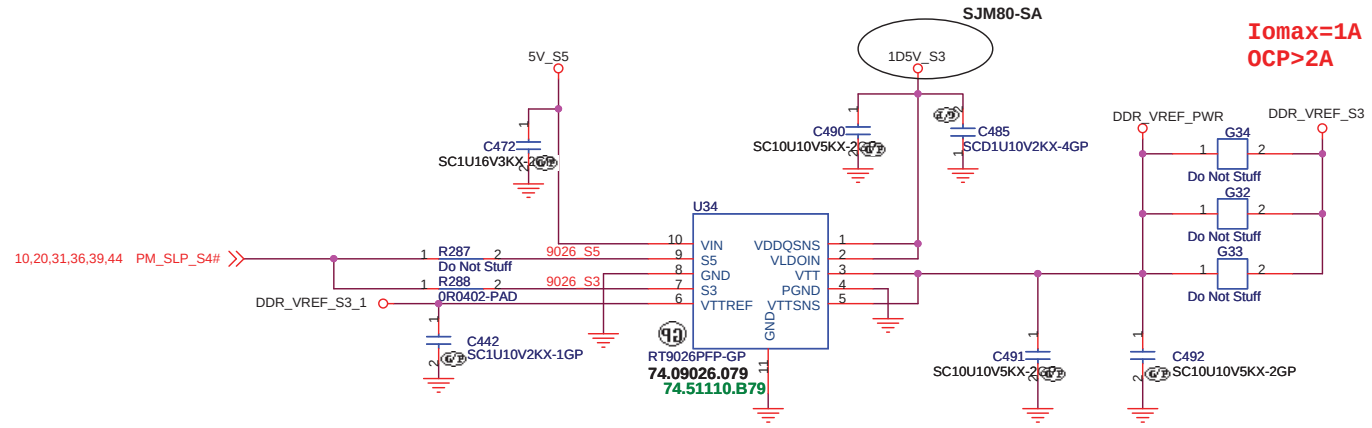
SJM80-SA



SJM80 UMA ONLY SB

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***1D5V & 0D75V***

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Custom	SJM80/JV80	-1

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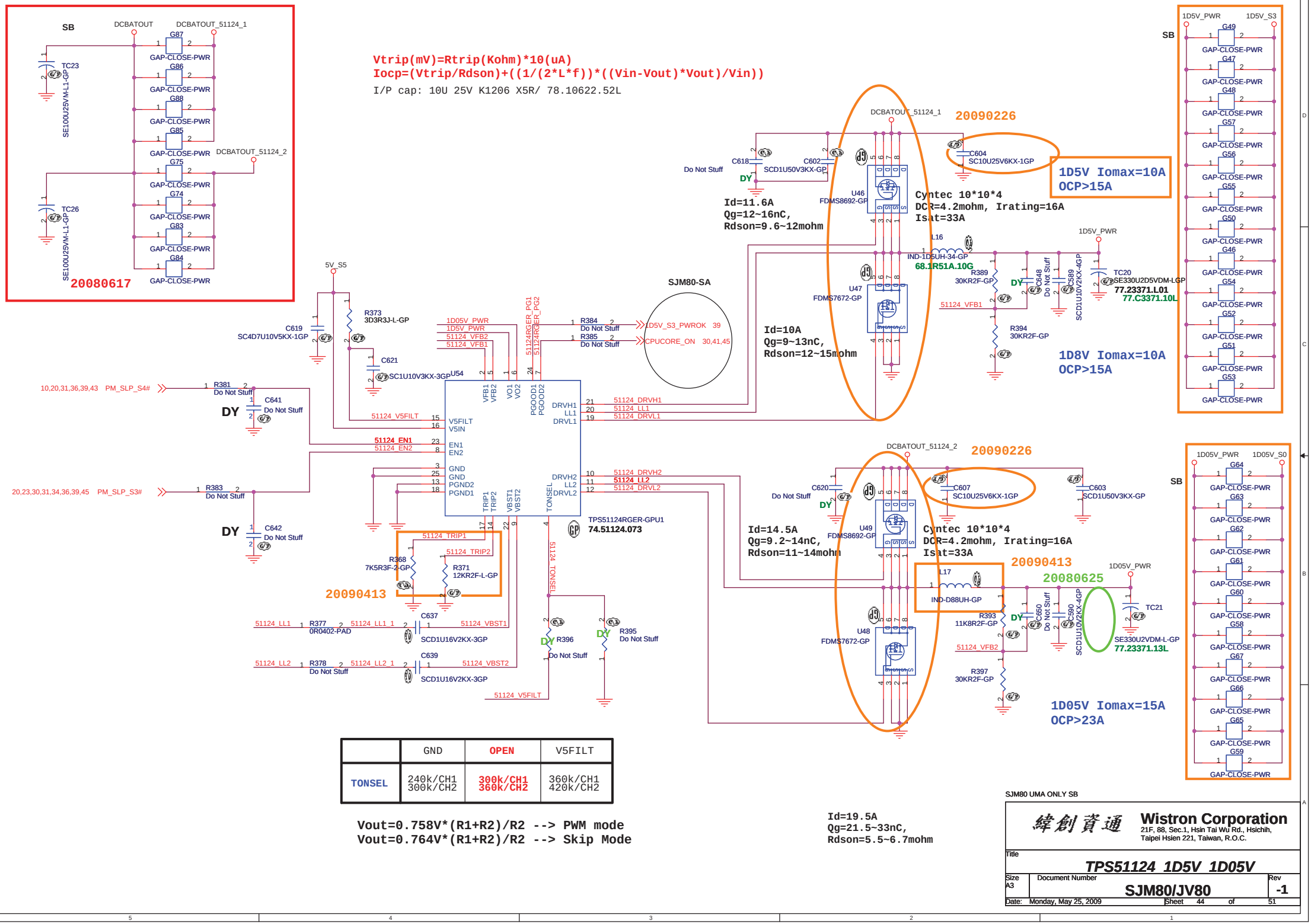
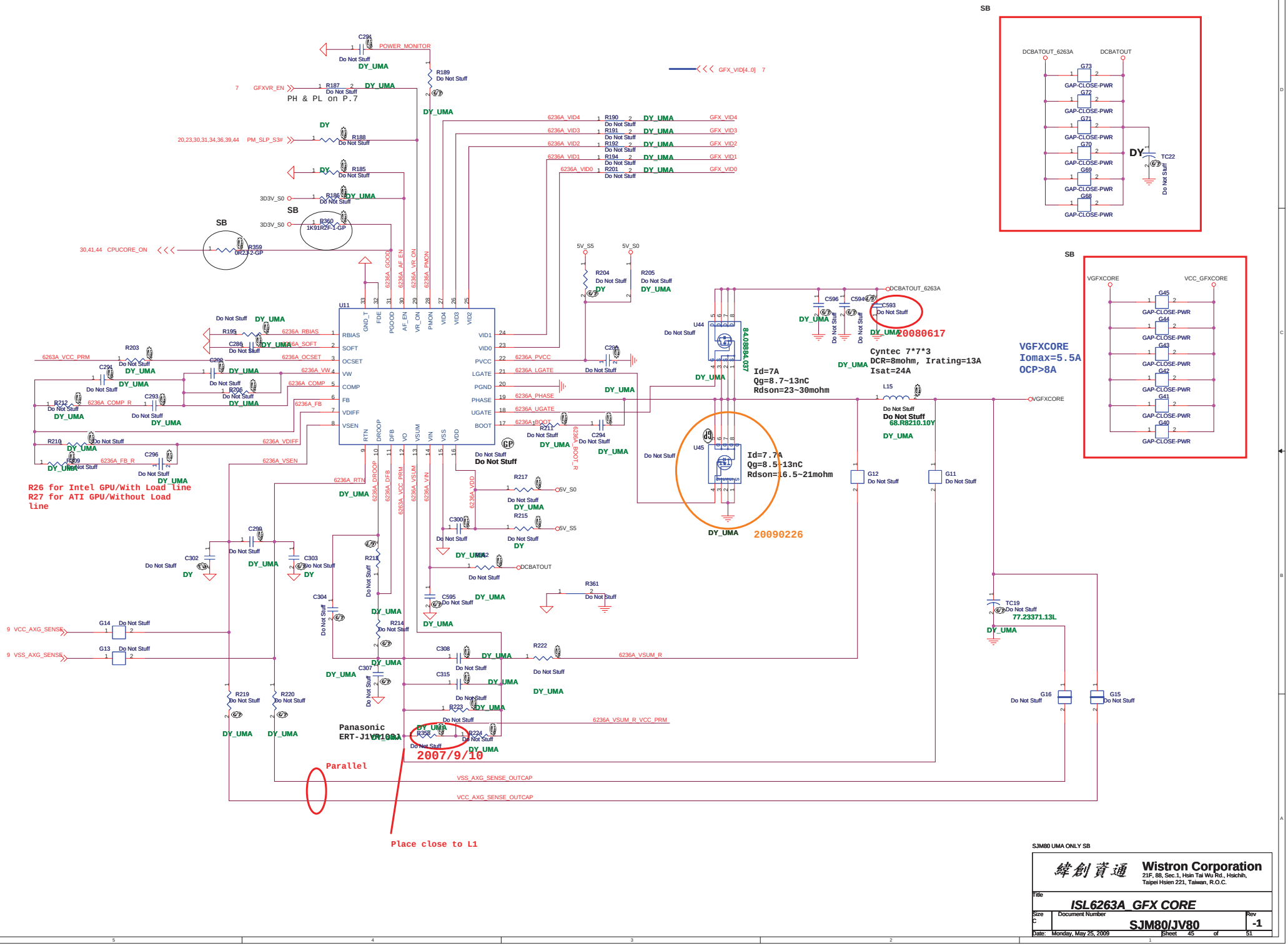


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2


SB
DCBATOUT_6263A
DCBATOUT
GAP-CLOSE-PWR
DY
TC22
Do Not Stuff
VGFXCORE
VCC_GFXCORE
U11
RBIAS
SOFT
OCSET
VW
COMP
FB
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
VSS
VDD
VID1
VID0
PVCC
LGATE
PGND
PHASE
UGATE
BOOT
GND_T
FDE
PGOOD
AF_EN
VR_ON
PMON
VID4
VID3
VID2
U44
U45
84808AA037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
20080617
Cyntec 7*7*3
DCR=8mohm, Irating=13A
Isat=24A
VGFXCORE
Iomax=5.5A
OCP>8A
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
20090226
L15
68.R8210.10Y
G11
G12
TC19
77.23371.13L
G15
G16
R26 for Intel GPU/With Load line
R27 for ATI GPU/Without Load line
Panasonic
ERT-J1VR103J
2007/9/10
Parallel
Place close to L1
PH & PL on P.7
POWER_MONITOR
GFX_VID[4..0]
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
SJM80 UMA ONLY SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ISL6263A_GFX CORE
SJM80/JV80
-1
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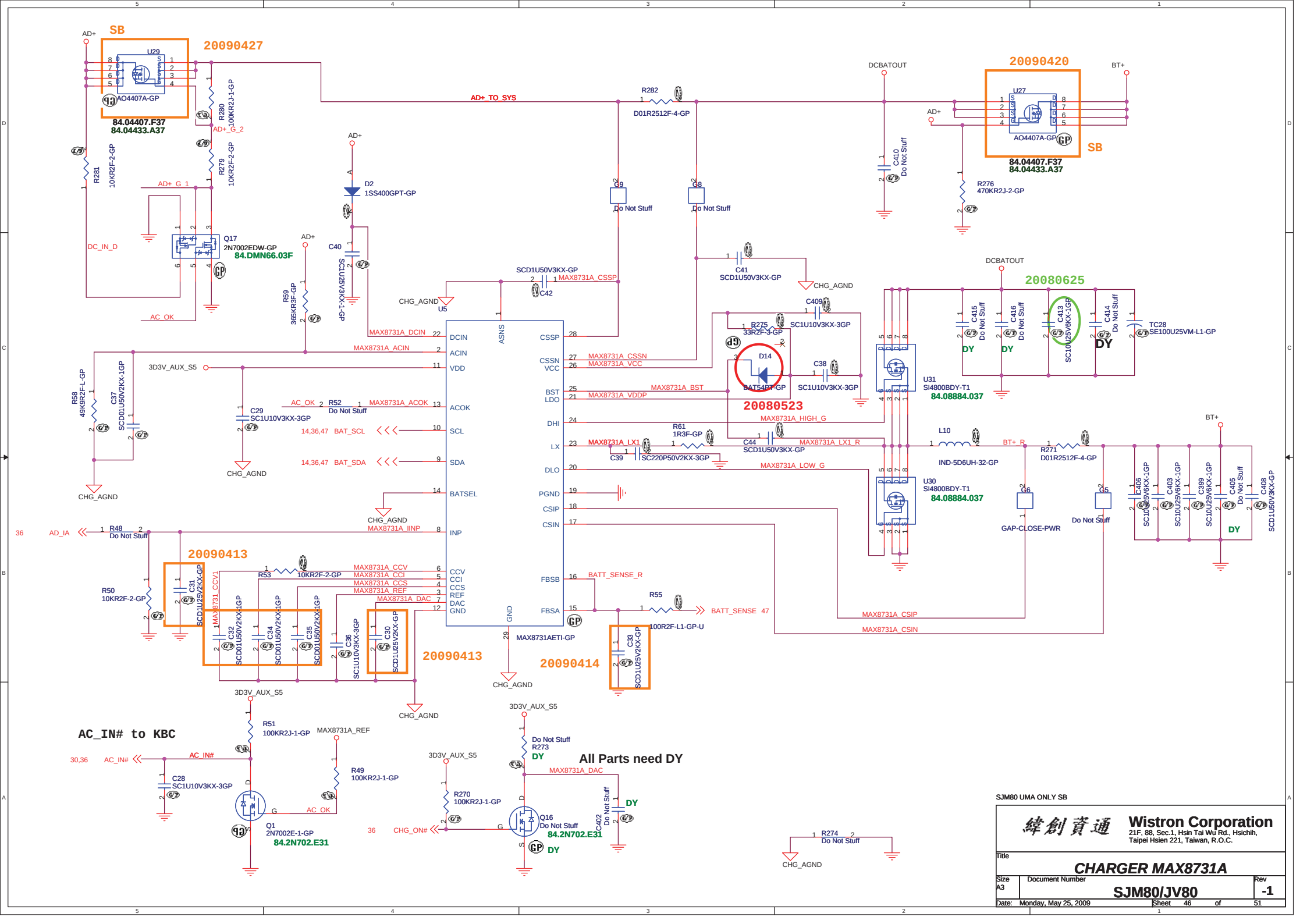
SB
20090427
U29
AO4407A-GP
84.04407.F37
84.04433.A37
AD+
AD+_TO_SYS
R282
D01R2512F-4-GP
DCBATOUT
20090420
U27
AO4407A-GP
SB
84.04407.F37
84.04433.A37
BT+
R276
470KR2J-2-GP
C410
Do Not Stuff
R280
100KR2J-1-GP
AD+_G_2
R279
10KR2F-2-GP
R281
10KR2F-2-GP
AD+_G_1
DC_IN_D
Q17
2N7002EDW-GP
84.DMN66.03F
AC_OK
D2
1SS400GPT-GP
C40
SCD1U25V3KX-1-GP
R59
365KR3F-GP
G9
Do Not Stuff
G8
Do Not Stuff
C41
SCD1U50V3KX-GP
CHG_AGND
U5
SCD1U50V3KX-GP
C42
MAX8731A_CSSP
C409
R275
33R2F-3-GP
SC1U10V3KX-3GP
D14
BAT54PT-GP
C38
SC1U10V3KX-3GP
20080523
DCBATOUT
20080625
C415
Do Not Stuff
C416
Do Not Stuff
C413
SC10U25V6KX-1GP
C414
Do Not Stuff
DY
TC28
SE100U25VM-L1-GP
U31
SI4800BDY-T1
84.08884.037
U30
SI4800BDY-T1
84.08884.037
L10
IND-5D6UH-32-GP
BT+_R
R271
D01R2512F-4-GP
G6
GAP-CLOSE-PWR
G5
Do Not Stuff
C406
C403
C399
C405
Do Not Stuff
C408
SCD1U50V3KX-GP
MAX8731A_DCIN
MAX8731A_ACIN
3D3V_AUX_S5
R58
49K9R2F-L-GP
C37
SCD01U50V2KX-1GP
C29
SC1U10V3KX-3GP
AC_OK
R52
Do Not Stuff
MAX8731A_ACOK
14,36,47 BAT_SCL
14,36,47 BAT_SDA
CHG_AGND
MAX8731A_IINP
36 AD_IA
R48
Do Not Stuff
20090413
R50
10KR2F-2-GP
C31
SCD1U25V2KX-GP
MAX8731_CCV1
R53
10KR2F-2-GP
C32
C34
C35
SCD01U50V2KX1GP
C36
SC1U10V3KX-3GP
C30
SCD1U25V2KX-GP
20090413
MAX8731A_CCV
MAX8731A_CCI
MAX8731A_CCS
MAX8731A_REF
MAX8731A_DAC
MAX8731AETI-GP
20090414
C33
SCD1U25V2KX-GP
R61
1R3F-GP
C44
SCD1U50V3KX-GP
C39
SC220P50V2KX-3GP
MAX8731A_HIGH_G
MAX8731A_LX1
MAX8731A_LX1_R
MAX8731A_LOW_G
MAX8731A_VDDP
MAX8731A_BST
MAX8731A_CSSN
MAX8731A_VCC
BATT_SENSE_R
R55
100R2F-L1-GP-U
BATT_SENSE 47
MAX8731A_CSIP
MAX8731A_CSIN
DCIN
ACIN
VDD
ACOK
SCL
SDA
BATSEL
INP
CCV
CCI
CCS
REF
DAC
GND
CSSP
CSSN
VCC
BST
LDO
DHI
LX
DLO
PGND
CSIP
CSIN
FBSB
FBSA
ASNS
AC_IN# to KBC
30,36 AC_IN#
R51
100KR2J-1-GP
C28
SC1U10V3KX-3GP
R49
100KR2J-1-GP
Q1
2N7002E-1-GP
84.2N702.E31
R270
100KR2J-1-GP
36 CHG_ON#
Q16
Do Not Stuff
84.2N702.E31
C402
Do Not Stuff
DY
Do Not Stuff
R273
DY
All Parts need DY
R274
Do Not Stuff
SJM80 UMA ONLY SB
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER MAX8731A
Size A3
Document Number
SJM80/JV80
Rev -1
Date: Monday, May 25, 2009
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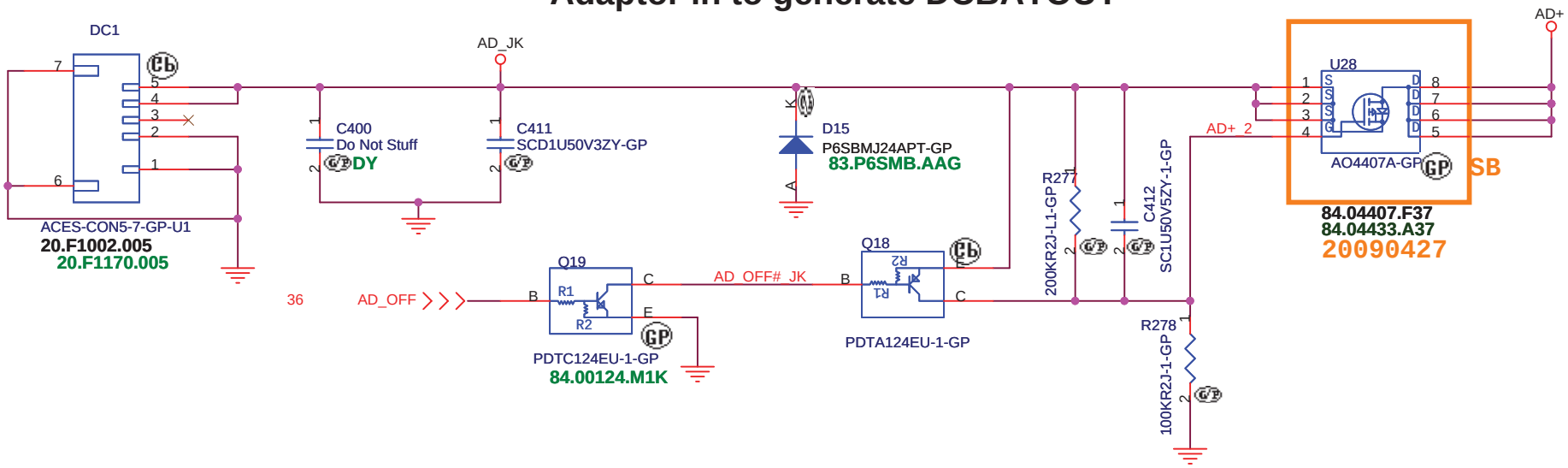
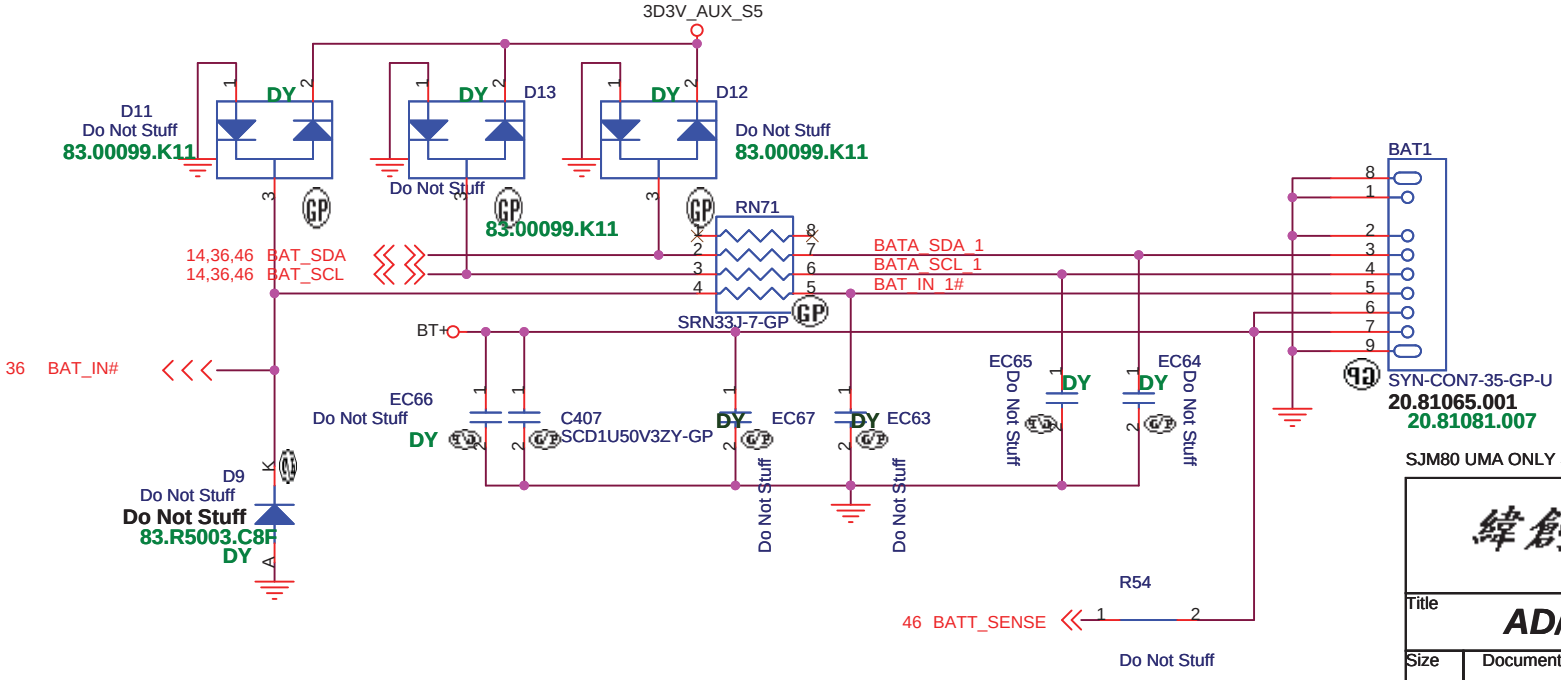
Adaptor in to generate DCBATOUT

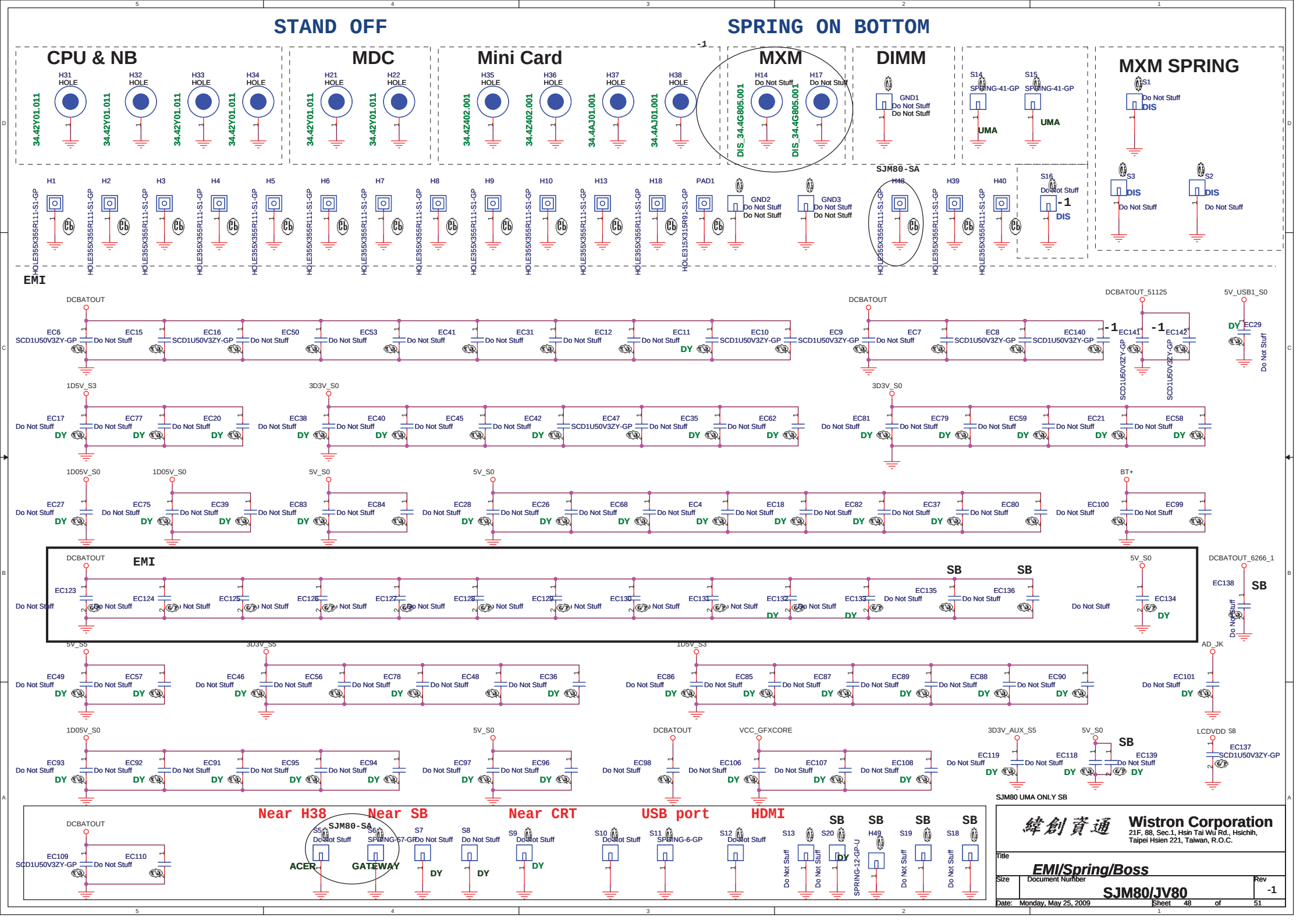


BATTERY CONNECTOR



SJM80 UMA ONLY SB

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AD/BATT CONN***	
Size	Document Number **SJM80/JV80**	Rev -1
Date: Monday, May 25, 2009	Sheet 47 of 51	


STAND OFF
SPRING ON BOTTOM
CPU & NB
MDC
Mini Card
MXM
DIMM
MXM SPRING
H31 HOLE
H32 HOLE
H33 HOLE
H34 HOLE
H21 HOLE
H22 HOLE
H35 HOLE
H36 HOLE
H37 HOLE
H38 HOLE
H14 Do Not Stuff
H17 Do Not Stuff
GND1 Do Not Stuff Do Not Stuff
S14 SPRING-41-GP
S15 SPRING-41-GP
UMA
S1 Do Not Stuff DIS
S3 DIS Do Not Stuff
S2 DIS Do Not Stuff
H1
H2
H3
H4
H5
H6
H7
H8
H9
H10
H13
H18
PAD1
GND2 Do Not Stuff Do Not Stuff
GND3 Do Not Stuff Do Not Stuff
SJM80-SA
H48
H39
H40
S16 Do Not Stuff
DIS
EMI
DCBATOUT
DCBATOUT_51125
5V_USB1_S0
1D5V_S3
3D3V_S0
1D05V_S0
5V_S0
BT+
SB
5V_S5
3D3V_S5
1D5V_S5
AD_JK
DCBATOUT_6266_1
VCC_GFXCORE
3D3V_AUX_S5
LCDVDD SB
SJM80 UMA ONLY SB
Near H38
Near SB
Near CRT
USB port
HDMI
ACER
GATEWAY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
SJM80/JV80
Rev
-1
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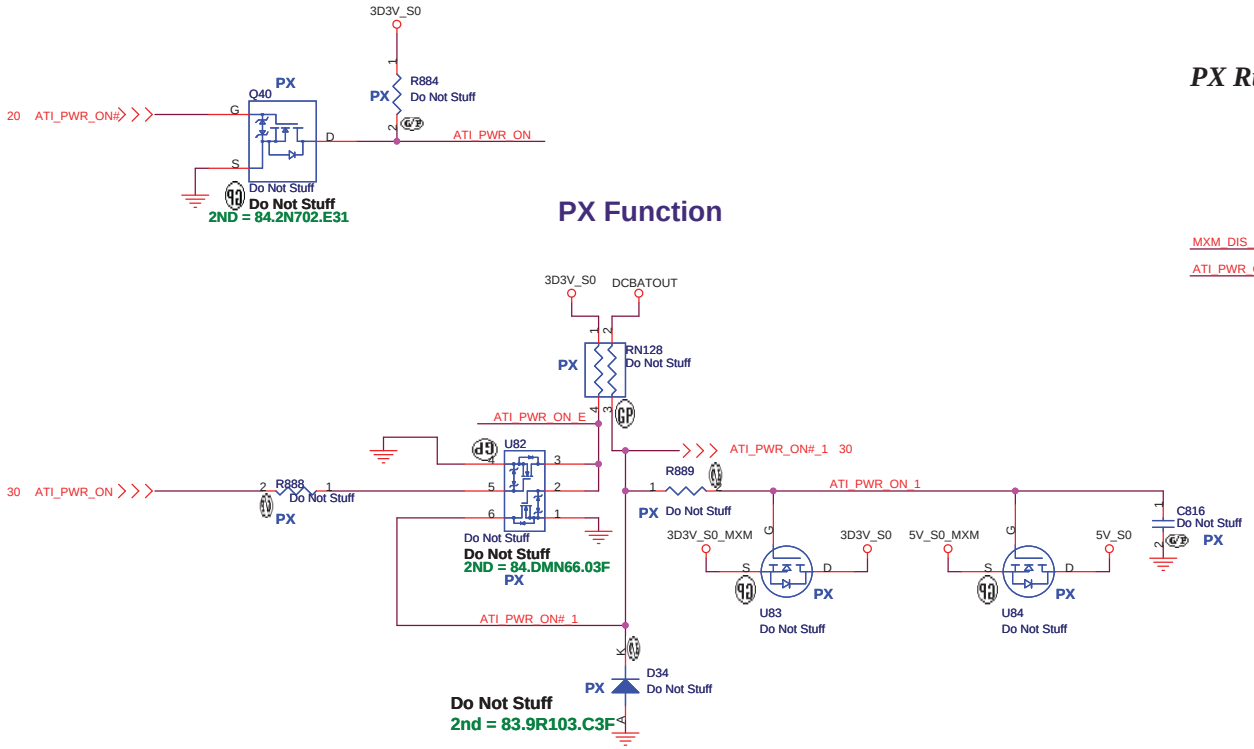

SJM80 UMA ONLY SB

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Title	***PX Run Power***	
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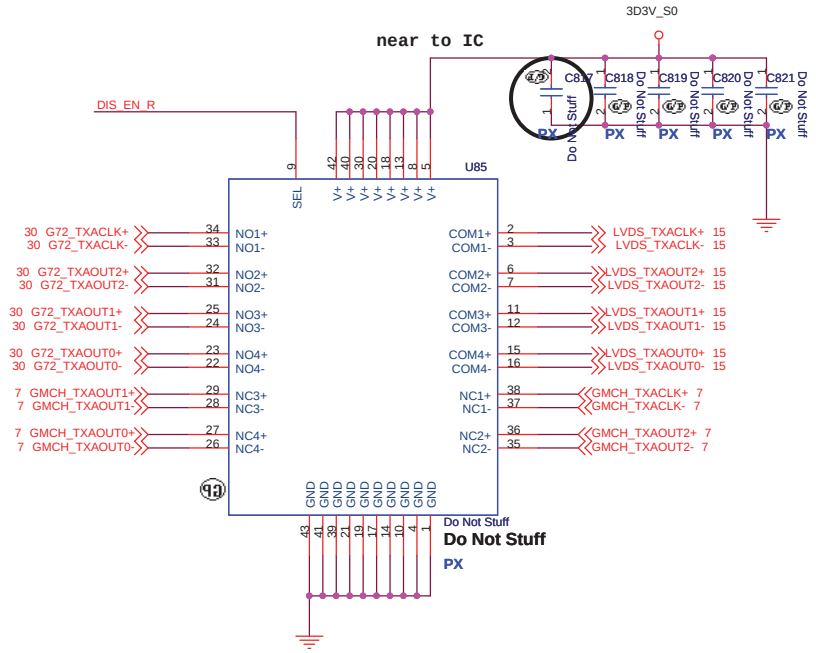
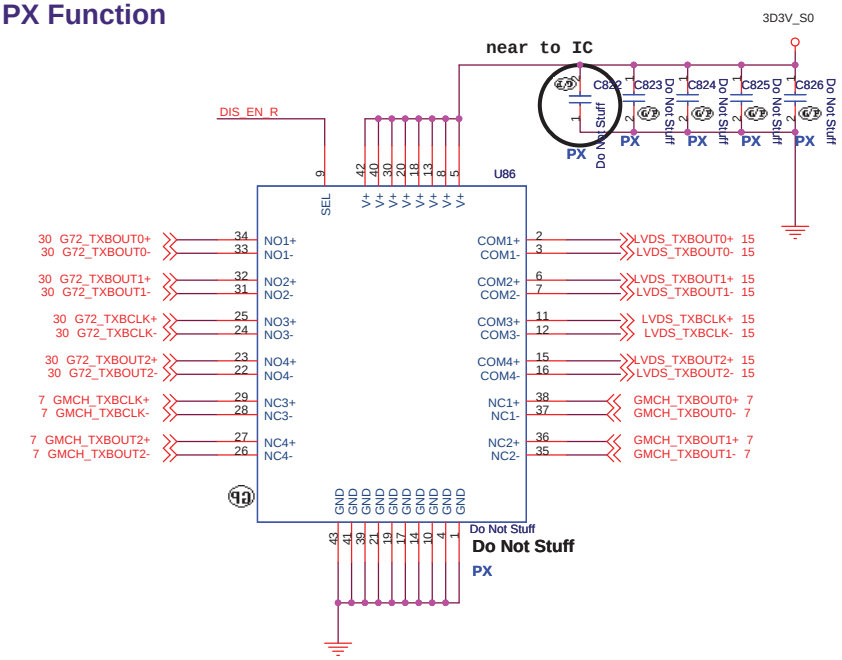
PX Function

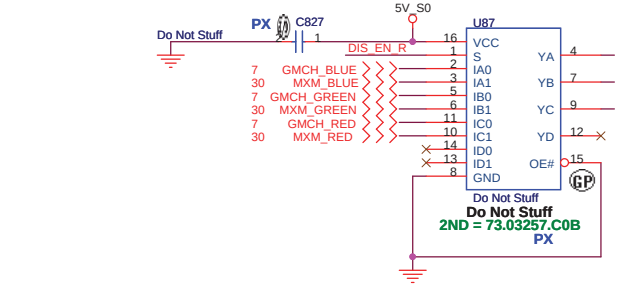


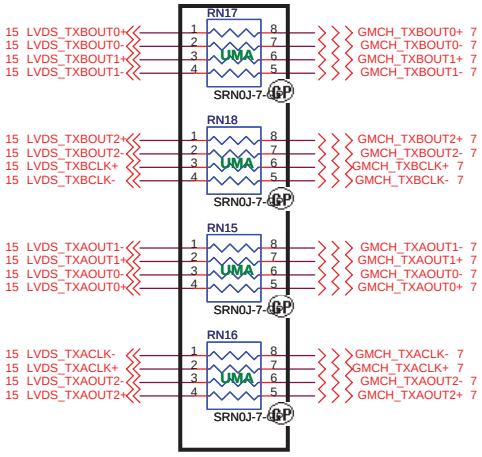


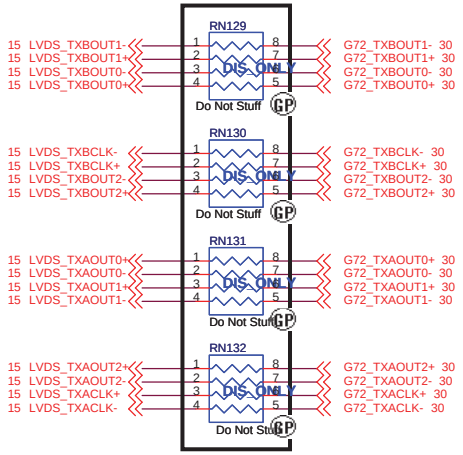
$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

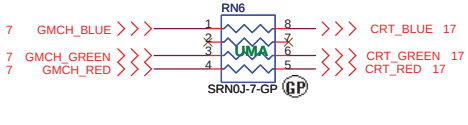
DIS_EN_R Low = UMA
DIS_EN_R High = DIS

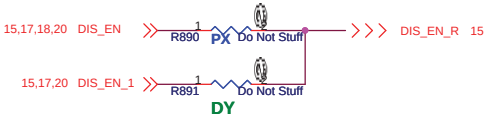
PX Function











SJM80 UMA ONLY SB

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Title: **PX Switch**

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SJM80 Schematic EC Tracking Record LAB 0325 , 2009
EC #/ Page / Description / Part Affected

EC SB03/26/change R359 R360 上件(for PX function)
EC SB03/26/change RN27 RN31 RN32 RN33 上件(for PX function)
EC SC03/30 change REAR1,REAR2 Net name
EC SB03/31 add digital Mic function
EC SB04/03 change Brightness setting from NB
EC SB04/03 modify MMB BD add switch
EC SB04/06 Change LAN Crystal setting
EC SB04/07 Close Power GAP
EC SB04/07 Change PCB Version
EC SB04/13 Keep JV80 GPIO and Function Key
EC SB04/20 add R946 R947 for BRIGHTNESS Bypass
EC -105/03 change C834~C841 to 0 ohm for HDMI no display design
EC -105/03 add R948 for DIS ONLY HDP
EC -105/03 change R823 to R824 for CRT no display
EC -105/13 change MXM Card Stand off part number
EC -105/19 MMBCN1 power 3D3V change 5V (for MMB LED light display)
EC -105/19 Modify HDMI hot plug schematic Location Q46
EC -105/20 change R316 to 22R2 (For USB eye diagram)
EC -105/20 change R398 6.5k to 7.1K increase 3.3V to 3.4V
EC -105/21 Q46 HDMI hot plug change power 3D3V_S0_MXM to 5V_S0
EC -105/22 add Cap for EMI at CRT RGB

EC -1 01/20/Change R316 to 22D6R2F(For USB eye diagram)

SJM80 UMA ONLY SB

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Title: EC Tracking Record

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