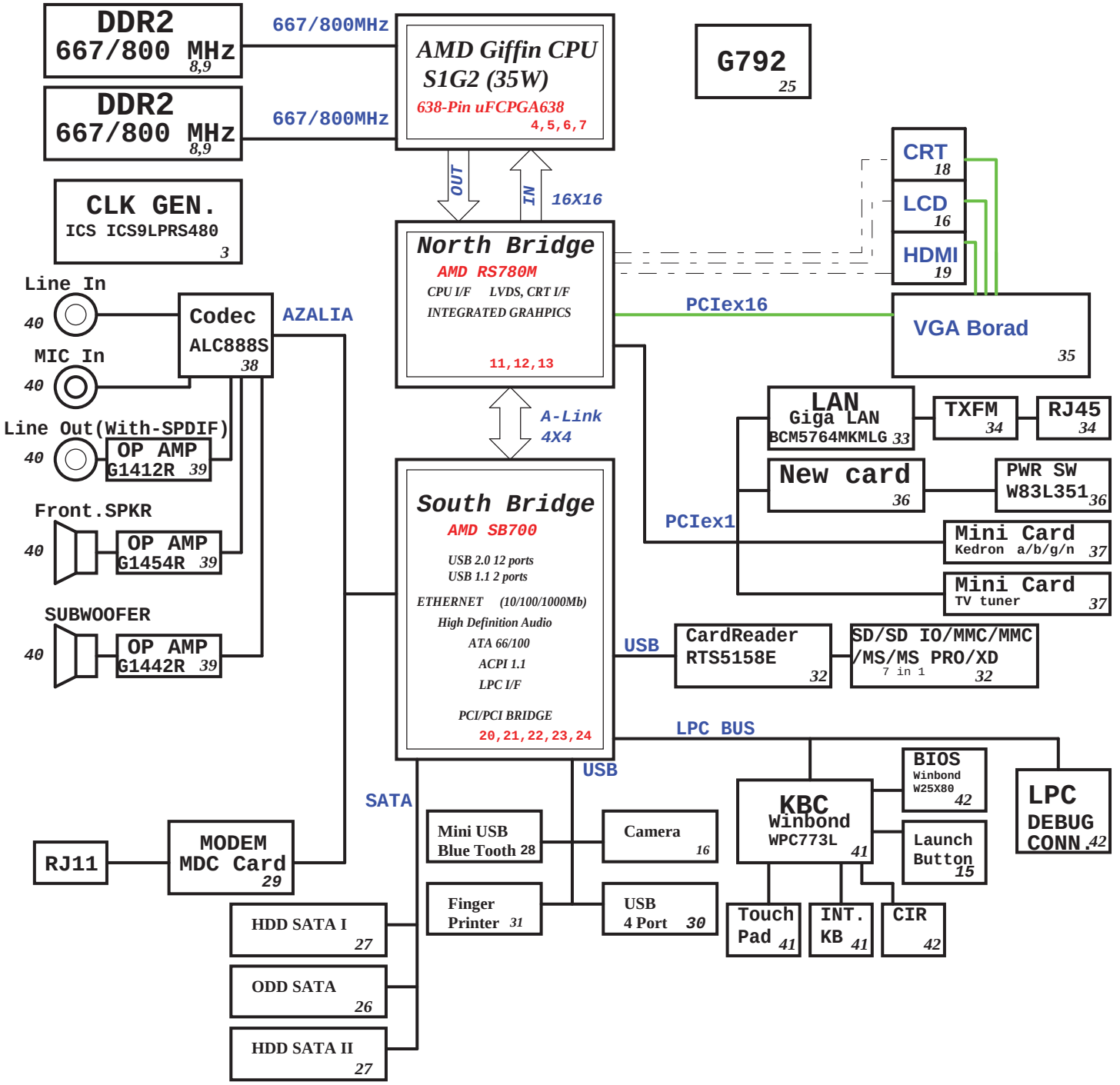
Big Bear 2A (AS 18") Block Diagram

Project code: 91.4AJ01.001
PCB P/N : 48.4AJ01.001
REVISION : 08208-1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 47	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)

SYSTEM DC/DC TPS51124 48	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(8A) 1D2V_S0(5A)

SYSTEM DC/DC TPS51117 49	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(10A)
RT9026PFP 50	
1D8V_S3	DDR_VREF_S3 0D9V_S3(1A)
RT9166 50	
3D3V_S0	2D5V_S0 (300mA)
G957 50	
3D3V_S0	1D5V_S0(1A)
G9161 50	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731A 51	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	Big Bear 2A	SC

Date: Monday, October 27, 2008 Sheet 1 of 55

<Core Design>

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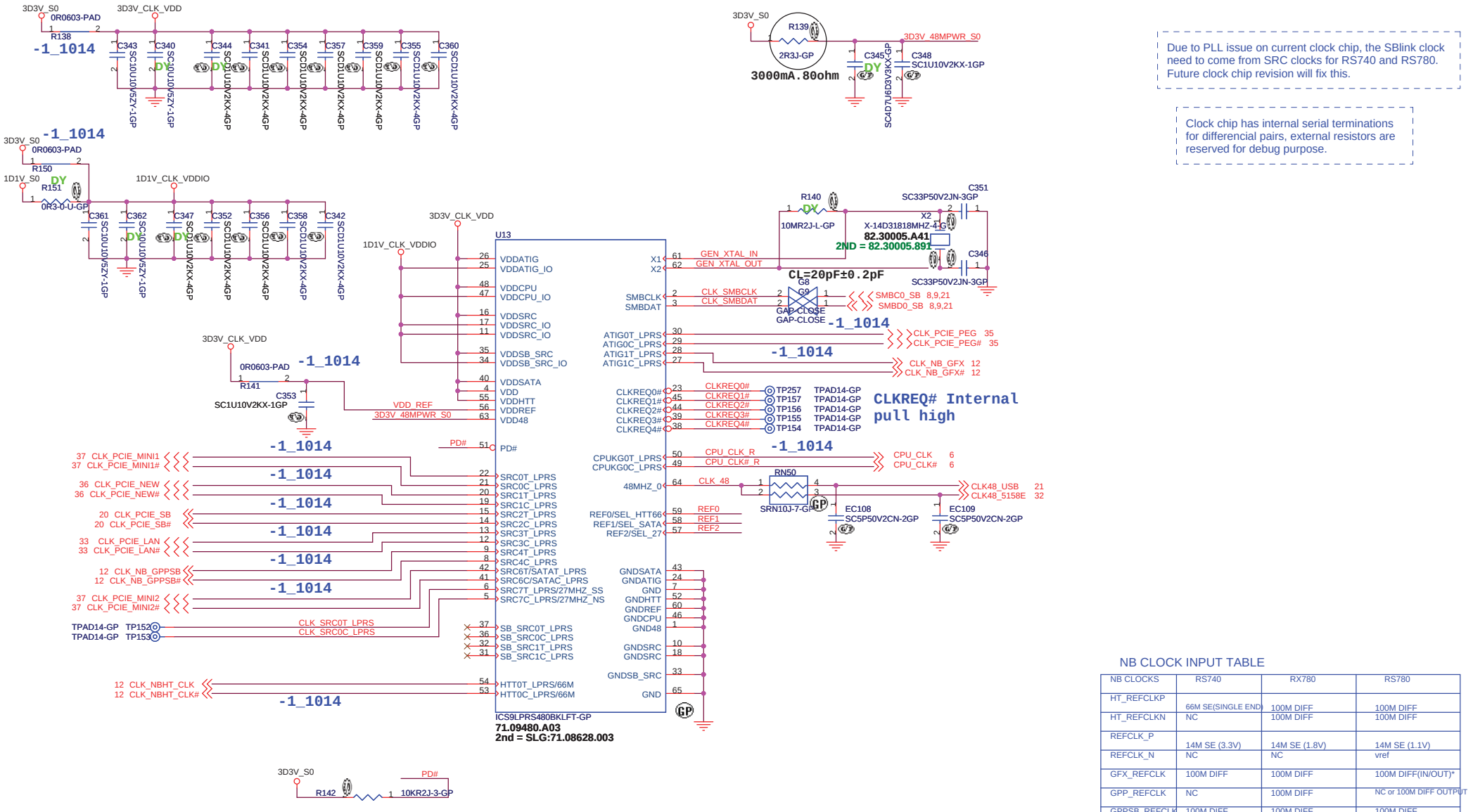
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
HISTORY

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 2 of 55



SEL_27 REF2		
	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0*	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0 *	100MHz differential HTT clock

* default

CPU_CLK(200MHz)

	OSC_14M_NB
RS780M	1.1V 158R/90.9R

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

<Core Design>

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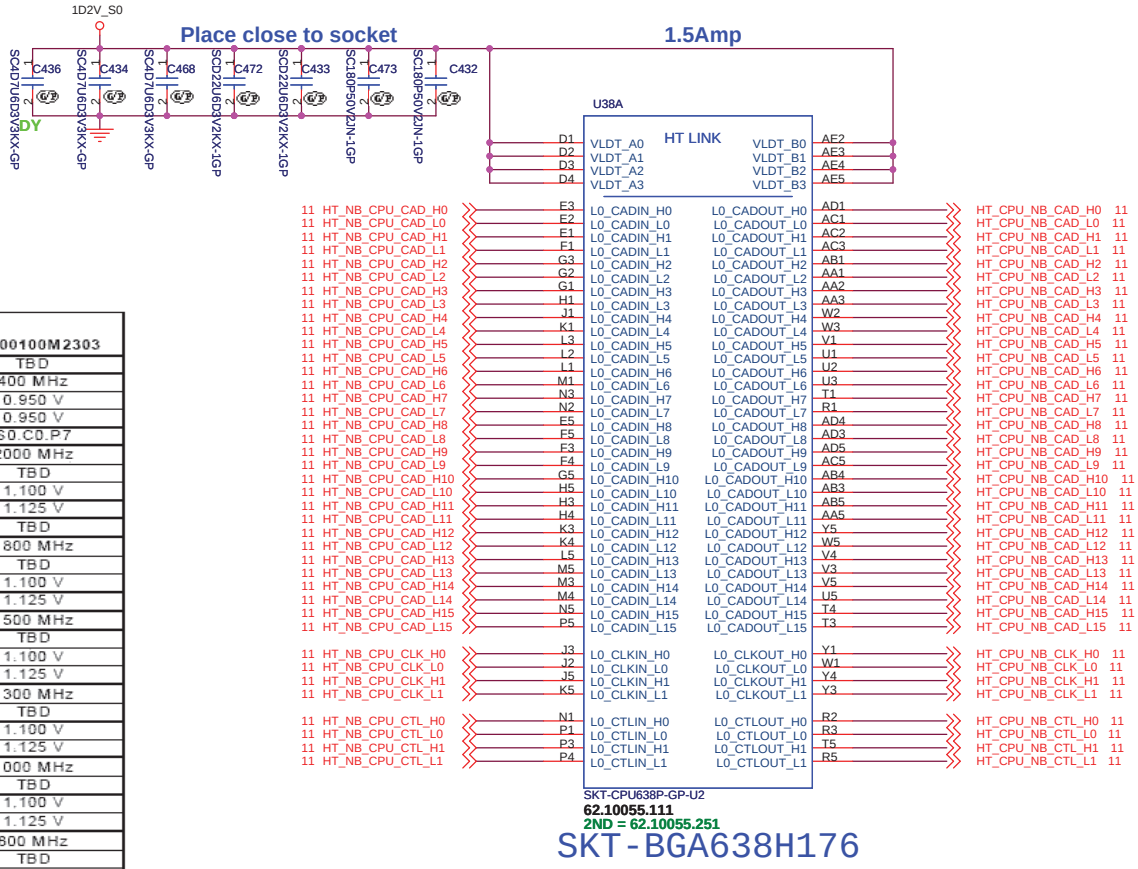
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS9LPRS480

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 3 of 55



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_HT_LINK I/F_(1/4)

Size: A3 | Document Number: Big Bear 2A | Rev: SA

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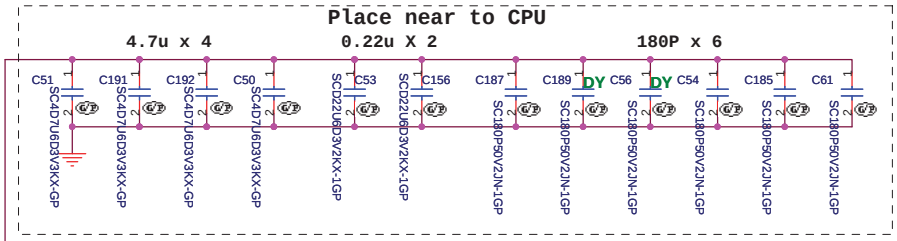
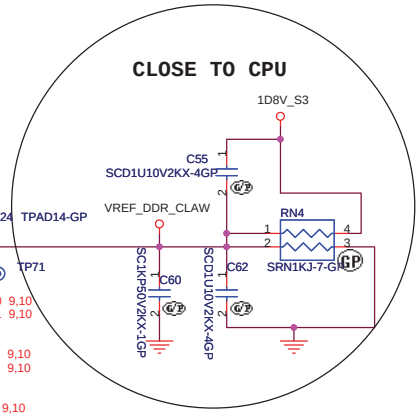




0D9V_S3

1D8V_S3 R221 39D2R2F-L-GP

R225 39D2R2F-L-GPTP48

MEM_RSVD_M1

TP24 TPAD14-GP

TP71

U38B

MEM:CMD/CTRL/CLK

	D10	VTT1		VTT5	W10
	C10	VTT2		VTT6	AC10
	B10	VTT3		VTT7	AB10
	AD10	VTT4		VTT8	AA10
				VTT9	A10
MEMZP	AE10	MEMZP			
MEMZN	AE10	MEMZN		VTT_SENSE	Y10
	H16	RSVD_M1		MEMVREF	W17
8,10 MEM_MA0_ODT0	T19	MA0_ODT0		RSVD_M2	B18
8,10 MEM_MA0_ODT1	V22	MA0_ODT1			
	U21	MA1_ODT0		MB0_ODT0	W26
	V19	MA1_ODT1		MB0_ODT1	W23
				MB1_ODT0	Y26
8,10 MEM_MA0_CS#0	T20	MA0_CS_L0			
8,10 MEM_MA0_CS#1	U19	MA0_CS_L1		MB0_CS_L0	V26
	U20	MA1_CS_L0		MB0_CS_L1	W25
	V20	MA1_CS_L1		MB1_CS_L0	U22
8,10 MEM_MA_CKE0	J22	MA_CKE0		MB_CKE0	J25
8,10 MEM_MA_CKE1	J20	MA_CKE1		MB_CKE1	H26
	N19	MA_CLK_H5		MB_CLK_H5	P22
	N20	MA_CLK_L5		MB_CLK_L5	R22
8 MEM_MA_CLK0_P	E16	MA_CLK_H1		MB_CLK_H1	A17
8 MEM_MA_CLK0_N	F16	MA_CLK_L1		MB_CLK_L1	A18
8 MEM_MA_CLK1_P	Y16	MA_CLK_H7		MB_CLK_H7	AF18
8 MEM_MA_CLK1_N	AA16	MA_CLK_L7		MB_CLK_L7	AF17
	P19	MA_CLK_H4		MB_CLK_H4	R26
	P20	MA_CLK_L4		MB_CLK_L4	R25
8,10 MEM_MA_ADD0	N21	MA_ADD0		MB_ADD0	P24
8,10 MEM_MA_ADD1	M20	MA_ADD1		MB_ADD1	N24
8,10 MEM_MA_ADD2	N22	MA_ADD2		MB_ADD2	P26
8,10 MEM_MA_ADD3	M19	MA_ADD3		MB_ADD3	N23
8,10 MEM_MA_ADD4	M22	MA_ADD4		MB_ADD4	N26
8,10 MEM_MA_ADD5	L20	MA_ADD5		MB_ADD5	L23
8,10 MEM_MA_ADD6	M24	MA_ADD6		MB_ADD6	N25
8,10 MEM_MA_ADD7	L21	MA_ADD7		MB_ADD7	L24
8,10 MEM_MA_ADD8	L19	MA_ADD8		MB_ADD8	M26
8,10 MEM_MA_ADD9	K22	MA_ADD9		MB_ADD9	K26
8,10 MEM_MA_ADD10	R21	MA_ADD10		MB_ADD10	T26
8,10 MEM_MA_ADD11	L22	MA_ADD11		MB_ADD11	L26
8,10 MEM_MA_ADD12	K20	MA_ADD12		MB_ADD12	L25
8,10 MEM_MA_ADD13	V24	MA_ADD13		MB_ADD13	W24
8,10 MEM_MA_ADD14	K24	MA_ADD14		MB_ADD14	J23
8,10 MEM_MA_ADD15	K19	MA_ADD15		MB_ADD15	J24
8,10 MEM_MA_BANK0	R20	MA_BANK0		MB_BANK0	R24
8,10 MEM_MA_BANK1	R23	MA_BANK1		MB_BANK1	U26
8,10 MEM_MA_BANK2	J21	MA_BANK2		MB_BANK2	J26
8,10 MEM_MA_RAS#	R19	MA_RAS_L		MB_RAS_L	U25
8,10 MEM_MA_CAS#	T22	MA_CAS_L		MB_CAS_L	U24
8,10 MEM_MA_WE#	T24	MA_WE_L		MB_WE_L	U23

SKT-CPU638P-GP-U2

62.10055.111

2ND = 62.10055.251

U38C

MEM:DATA

8 MEM_MA_DATA0	G12	MA_DATA0	MB_DATA0	C11
8 MEM_MA_DATA1	F12	MA_DATA1	MB_DATA1	A11
8 MEM_MA_DATA2	H14	MA_DATA2	MB_DATA2	A14
8 MEM_MA_DATA3	G14	MA_DATA3	MB_DATA3	B14
8 MEM_MA_DATA4	H11	MA_DATA4	MB_DATA4	G11
8 MEM_MA_DATA5	H12	MA_DATA5	MB_DATA5	E11
8 MEM_MA_DATA6	C13	MA_DATA6	MB_DATA6	D12
8 MEM_MA_DATA7	E13	MA_DATA7	MB_DATA7	A13
8 MEM_MA_DATA8	H15	MA_DATA8	MB_DATA8	A15
8 MEM_MA_DATA9	E15	MA_DATA9	MB_DATA9	A16
8 MEM_MA_DATA10	E17	MA_DATA10	MB_DATA10	A19
8 MEM_MA_DATA11	H17	MA_DATA11	MB_DATA11	A20
8 MEM_MA_DATA12	E14	MA_DATA12	MB_DATA12	C14
8 MEM_MA_DATA13	F14	MA_DATA13	MB_DATA13	D14
8 MEM_MA_DATA14	C17	MA_DATA14	MB_DATA14	C18
8 MEM_MA_DATA15	G17	MA_DATA15	MB_DATA15	D18
8 MEM_MA_DATA16	G18	MA_DATA16	MB_DATA16	D20
8 MEM_MA_DATA17	C19	MA_DATA17	MB_DATA17	A21
8 MEM_MA_DATA18	D22	MA_DATA18	MB_DATA18	D24
8 MEM_MA_DATA19	E20	MA_DATA19	MB_DATA19	C25
8 MEM_MA_DATA20	E18	MA_DATA20	MB_DATA20	B20
8 MEM_MA_DATA21	F18	MA_DATA21	MB_DATA21	C20
8 MEM_MA_DATA22	B22	MA_DATA22	MB_DATA22	B24
8 MEM_MA_DATA23	C23	MA_DATA23	MB_DATA23	C24
8 MEM_MA_DATA24	F20	MA_DATA24	MB_DATA24	E23
8 MEM_MA_DATA25	F22	MA_DATA25	MB_DATA25	E24
8 MEM_MA_DATA26	H24	MA_DATA26	MB_DATA26	G25
8 MEM_MA_DATA27	J19	MA_DATA27	MB_DATA27	G26
8 MEM_MA_DATA28	E21	MA_DATA28	MB_DATA28	C26
8 MEM_MA_DATA29	E22	MA_DATA29	MB_DATA29	D26
8 MEM_MA_DATA30	H20	MA_DATA30	MB_DATA30	G23
8 MEM_MA_DATA31	H22	MA_DATA31	MB_DATA31	G24
8 MEM_MA_DATA32	Y24	MA_DATA32	MB_DATA32	AA24
8 MEM_MA_DATA33	AB24	MA_DATA33	MB_DATA33	AA23
8 MEM_MA_DATA34	AB22	MA_DATA34	MB_DATA34	AD24
8 MEM_MA_DATA35	AA21	MA_DATA35	MB_DATA35	AE24
8 MEM_MA_DATA36	W22	MA_DATA36	MB_DATA36	AA26
8 MEM_MA_DATA37	W21	MA_DATA37	MB_DATA37	AA25
8 MEM_MA_DATA38	Y22	MA_DATA38	MB_DATA38	AD26
8 MEM_MA_DATA39	AA22	MA_DATA39	MB_DATA39	AE25
8 MEM_MA_DATA40	Y20	MA_DATA40	MB_DATA40	AC22
8 MEM_MA_DATA41	AA20	MA_DATA41	MB_DATA41	AD22
8 MEM_MA_DATA42	AA18	MA_DATA42	MB_DATA42	AE20
8 MEM_MA_DATA43	AB18	MA_DATA43	MB_DATA43	AF20
8 MEM_MA_DATA44	AB21	MA_DATA44	MB_DATA44	AF24
8 MEM_MA_DATA45	AD21	MA_DATA45	MB_DATA45	AF23
8 MEM_MA_DATA46	AD19	MA_DATA46	MB_DATA46	AC20
8 MEM_MA_DATA47	Y18	MA_DATA47	MB_DATA47	AD20
8 MEM_MA_DATA48	AD17	MA_DATA48	MB_DATA48	AD18
8 MEM_MA_DATA49	W16	MA_DATA49	MB_DATA49	AE18
8 MEM_MA_DATA50	W14	MA_DATA50	MB_DATA50	AC14
8 MEM_MA_DATA51	Y14	MA_DATA51	MB_DATA51	AD14
8 MEM_MA_DATA52	Y17	MA_DATA52	MB_DATA52	AF19
8 MEM_MA_DATA53	AB17	MA_DATA53	MB_DATA53	AC18
8 MEM_MA_DATA54	AB15	MA_DATA54	MB_DATA54	AF16
8 MEM_MA_DATA55	AD15	MA_DATA55	MB_DATA55	AF15
8 MEM_MA_DATA56	AB13	MA_DATA56	MB_DATA56	AF13
8 MEM_MA_DATA57	AD13	MA_DATA57	MB_DATA57	AC12
8 MEM_MA_DATA58	Y12	MA_DATA58	MB_DATA58	AB11
8 MEM_MA_DATA59	W11	MA_DATA59	MB_DATA59	Y11
8 MEM_MA_DATA60	AB14	MA_DATA60	MB_DATA60	AE14
8 MEM_MA_DATA61	AA14	MA_DATA61	MB_DATA61	AE14
8 MEM_MA_DATA62	AB12	MA_DATA62	MB_DATA62	AF11
8 MEM_MA_DATA63	AA12	MA_DATA63	MB_DATA63	AD11
8 MEM_MA_DM0	E12	MA_DM0	MB_DM0	A12
8 MEM_MA_DM1	C15	MA_DM1	MB_DM1	B16
8 MEM_MA_DM2	E19	MA_DM2	MB_DM2	A22
8 MEM_MA_DM3	F24	MA_DM3	MB_DM3	E25
8 MEM_MA_DM4	AC24	MA_DM4	MB_DM4	AB26
8 MEM_MA_DM5	Y19	MA_DM5	MB_DM5	AE22
8 MEM_MA_DM6	AB16	MA_DM6	MB_DM6	AC16
8 MEM_MA_DM7	Y13	MA_DM7	MB_DM7	AD12
8 MEM_MA_DQS0_P	G13	MA_DQS_H0	MB_DQS_H0	C12
8 MEM_MA_DQS0_N	H13	MA_DQS_L0	MB_DQS_L0	B12
8 MEM_MA_DQS1_P	G16	MA_DQS_H1	MB_DQS_H1	D16
8 MEM_MA_DQS1_N	G15	MA_DQS_L1	MB_DQS_L1	C16
8 MEM_MA_DQS2_P	C22	MA_DQS_H2	MB_DQS_H2	A24
8 MEM_MA_DQS2_N	C21	MA_DQS_L2	MB_DQS_L2	A23
8 MEM_MA_DQS3_P	G22	MA_DQS_H3	MB_DQS_H3	F26
8 MEM_MA_DQS3_N	G21	MA_DQS_L3	MB_DQS_L3	E26
8 MEM_MA_DQS4_P	AD23	MA_DQS_H4	MB_DQS_H4	AC25
8 MEM_MA_DQS4_N	AC23	MA_DQS_L4	MB_DQS_L4	AC26
8 MEM_MA_DQS5_P	AB19	MA_DQS_H5	MB_DQS_H5	AF21
8 MEM_MA_DQS5_N	AB20	MA_DQS_L5	MB_DQS_L5	AF22
8 MEM_MA_DQS6_P	Y15	MA_DQS_H6	MB_DQS_H6	AE16
8 MEM_MA_DQS6_N	W15	MA_DQS_L6	MB_DQS_L6	AD16
8 MEM_MA_DQS7_P	W12	MA_DQS_H7	MB_DQS_H7	AE12
8 MEM_MA_DQS7_N	W13	MA_DQS_L7	MB_DQS_L7	AE12

SKT-CPU638P-GP-U2

62.10055.111

2ND = 62.10055.251

<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 5 of 55

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

1D8V_S0
RN31
SRN300J-1-GP
-1_1014
20,53 CPU_LDT_RST# — R257 0R0402-PAD — LDT_RST#_CPU
20,53 CPU_PWRGD — R258 0R0402-PAD — LDT_PWROK
20 CPU_LDT_STOP# — R62 0R0402-PAD — LDT_STP#_CPU 12
12,20 ALLOW_LDTSTOP — R255 0R0402-PAD — CPU_LDT_REQ#_CPU
SB with 0402 PAD

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491
LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.
2D5V_S0 — R55 0R3-0-U-GP — 2D5V_VDDA_S0
C162 DY SC10U10V5ZY-1GP
C163 SC4D7U6D3V3KX-GP
C153 SC3300P50V2KX-1GP
C164 SC10U10V5ZY-1GP
C161 SCD22U10V3KX-2GP
Cloce To CPU

U38D

CPU_CLK / CPU_CLK# — C481 / C488 SC3900P50V2KX-2GP — R263 169R2F-GP — CLKCPU_IN / CLKCPU# IN
LDT_RST# CPU
HDT_RST# — R256 0R0402-PAD
For HDT DBG
LDT_PWROK
LDT_STP# CPU
CPU_LDT_REQ# CPU
TPAD14-GP TP180 CPU_SIC
TPAD14-GP TP175 CPU_SID
TPAD14-GP TP174 CPU_ALERT#
1D2V_S0 — R48 / R49 44D2R2F-GP
CPU_HTREF0
CPU_HTREF1
46 CPU_VDD0_RUN_FB_H
46 CPU_VDD0_RUN_FB_L
46 CPU_VDD1_RUN_FB_H
46 CPU_VDD1_RUN_FB_L
CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
TP69 CPU_TEST23
CPU_TEST18
CPU_TEST19
TP65 CPU_TEST25_H
TP64 CPU_TEST25_L
CPU_TEST21
TP176 CPU_TEST20
CPU_TEST24
CPU_TEST22
CPU_TEST12
CPU_TEST27
RN84 SRN300J-1-GP — R254 0R0402-PAD — CPU_TEST9
CLKIN_H / CLKIN_L
RESET_L / PWROK / LDTSTOP_L / LDTREQ_L
SIC / SID / ALERT_L
HT_REF0 / HT_REF1
VDD0_FB_H / VDD0_FB_L
VDD1_FB_H / VDD1_FB_L
DBRDY / TMS / TCK / TRST_L / TDI
TEST23 / TEST18 / TEST19 / TEST25_H / TEST25_L
TEST21 / TEST20 / TEST24 / TEST22 / TEST12 / TEST27 / TEST9 / TEST6
RSVD1 / RSVD2 / RSVD3 / RSVD4 / RSVD5
KEY1 / KEY2
SVC / SVD
THERMTRIP_L / PROCHOT_L / MEMHOT_L
THERMDC / THERMDA
VDDIO_FB_H / VDDIO_FB_L
VDDNB_FB_H / VDDNB_FB_L
DBREQ_L
TDO
TEST28_H / TEST28_L
TEST17 / TEST16 / TEST15 / TEST14
TEST7 / TEST10 / TEST8
TEST29_H / TEST29_L
RSVD10 / RSVD9 / RSVD8 / RSVD7 / RSVD6
SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10055.251

1D8V_S3
RN30 SRN1KJ-7-GP
CPU_SVC 46
CPU_SVD 46
RN65 SRN300J-1-GP
CPU_TEST27
CPU_DBREQ#
R433 300R2J-4-GP DY
-1_1014
THERMTRIP#
PROCHOT#
CPU_MEMHOT#
R227 0R0402-PAD — PROCHOT#_SB 20
internal pull high 300 ohm
H_THERMDC 25
H_THERMDA 25
C58 DY SC100P50V2JN-3GP
CPU_VDDIO_SUS_FB_H — TP28
CPU_VDDIO_SUS_FB_L — TP27
CPU_VDDNB_RUN_FB_H 46
CPU_VDDNB_RUN_FB_L 46
CPU_DBREQ#
CPU_TDO
CPU_TEST28_H — TP52
CPU_TEST28_L — TP54
CPU_TEST17 — TP68
CPU_TEST16 — TP63
CPU_TEST15
CPU_TEST14
CPU_TEST29H — TP184
CPU_TEST29L — TP185

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

-1_1014
46 CPU_PWRGD_SVID_REG — R259 0R0402-PAD — LDT_PWROK
C483 DY SCD1U16V2ZY-2GP
Near CPU PIN

LDT_PWROK
R261 2K2R2J-2-GP
C482 1D8V_SUS_Q2 SCD1U16V2ZY-2GP
Q21 MMBT3904-4-GP
THERMTRIP# — KBC_THERMTRIP# 25,41
84.T3904.C11
2ND = 84.03904.T11
CPU exceeds to 125℃

CPU_TEST19 — R226 300R2J-4-GP DY
CPU_TEST18 — R45 300R2J-4-GP DY
CPU_TEST14 — R431 300R2J-4-GP DY
CPU_TEST15 — R432 300R2J-4-GP DY

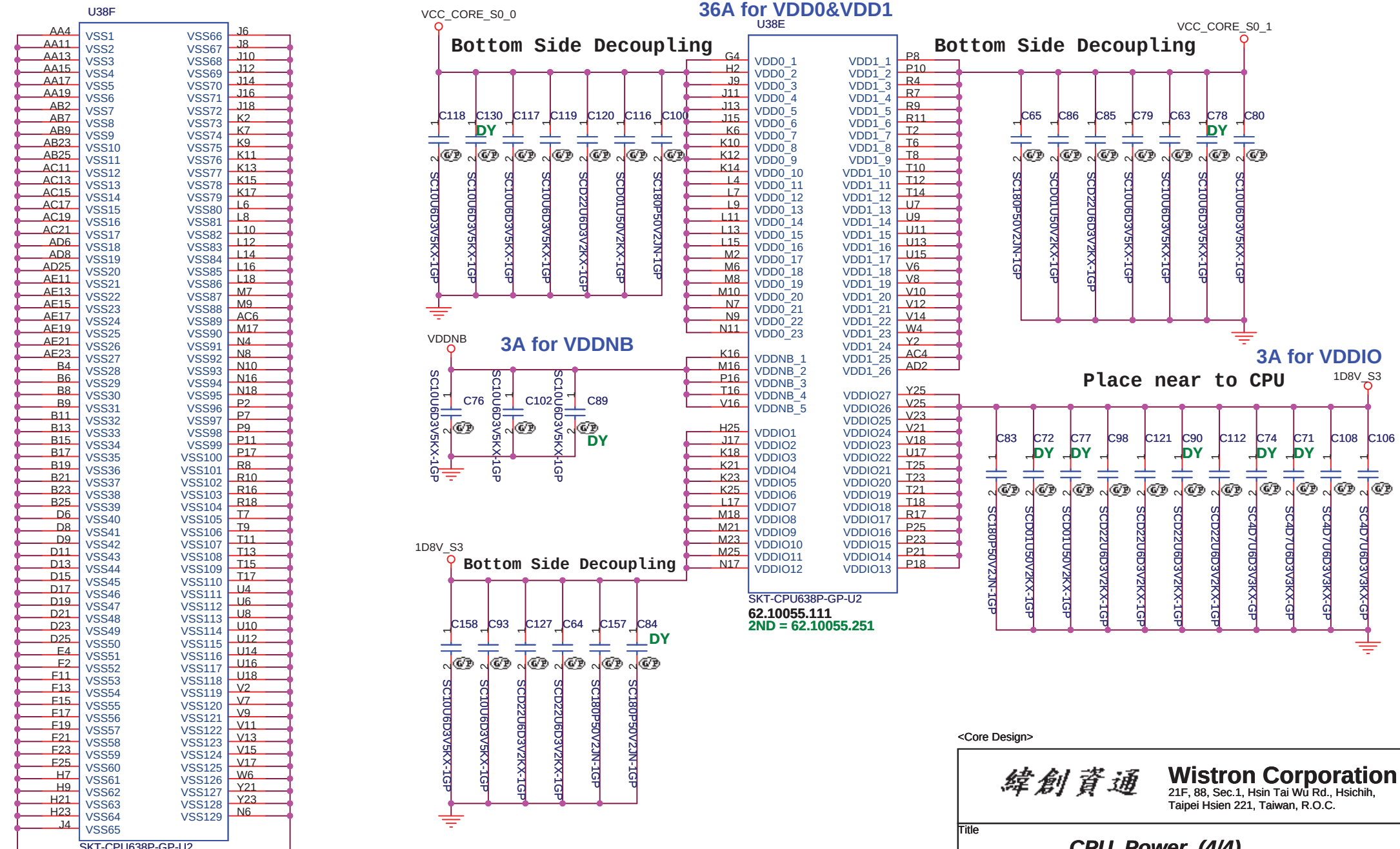
HDT Connectors

CPU_DBREQ#	TP17	TPAD14-GP
CPU_DBRDY	TP50	TPAD14-GP
CPU_TCK	TP21	TPAD14-GP
CPU_TMS	TP23	TPAD14-GP
CPU_TDI	TP20	TPAD14-GP
CPU_TRST#	TP19	TPAD14-GP
CPU_TDO	TP18	TPAD14-GP
1D8V_S3	TP29	TPAD14-GP
HDT_RST#	TP183	TPAD14-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)
Size: A3 | Document Number: Big Bear 2A | Rev: SC
Date: Monday, October 27, 2008 | Sheet 6 of 55



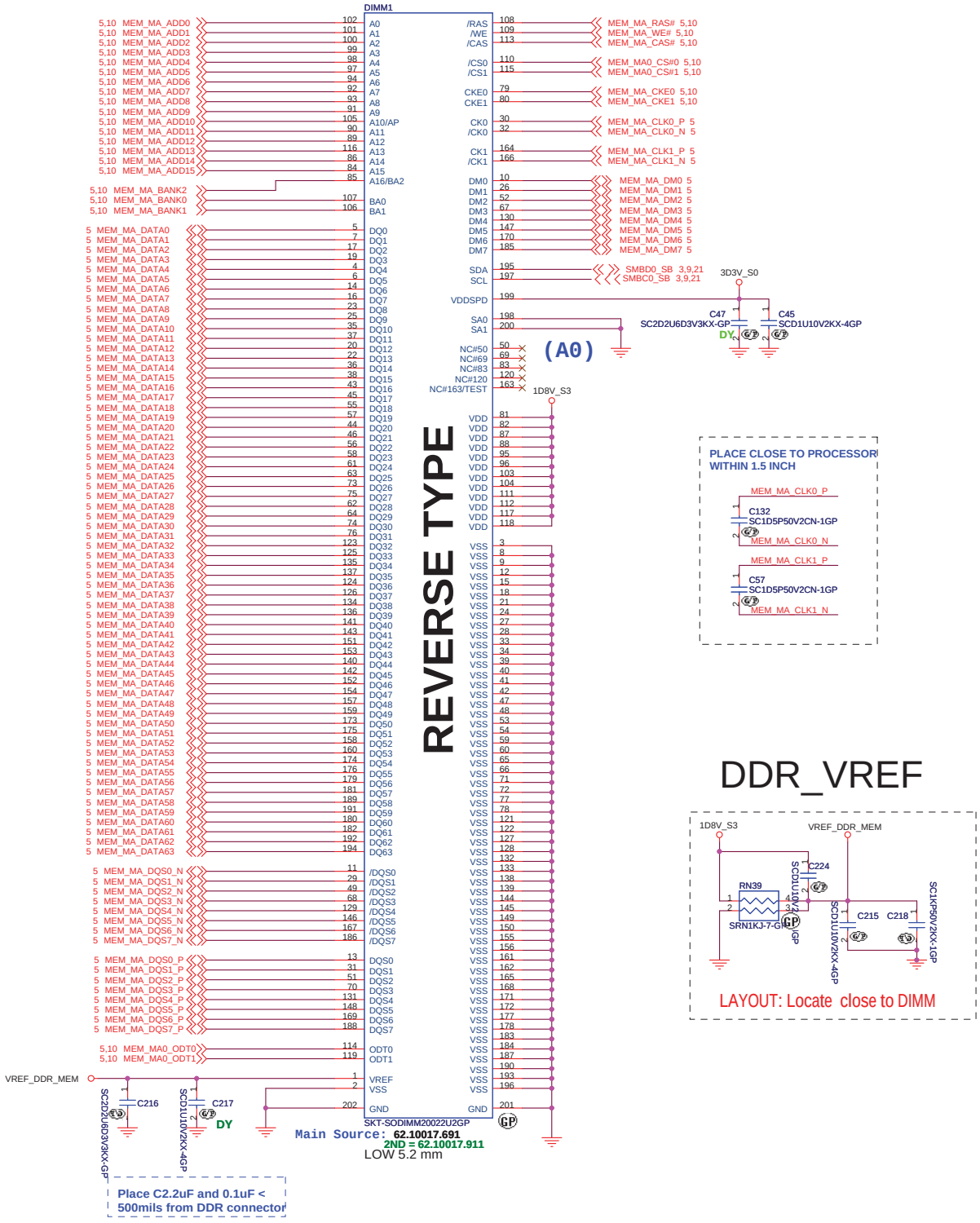
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_Power_(4/4)***

Size	Document Number	Rev
A4	**Big Bear 2A**	SA

Date: Monday, October 27, 2008 Sheet 7 of 55



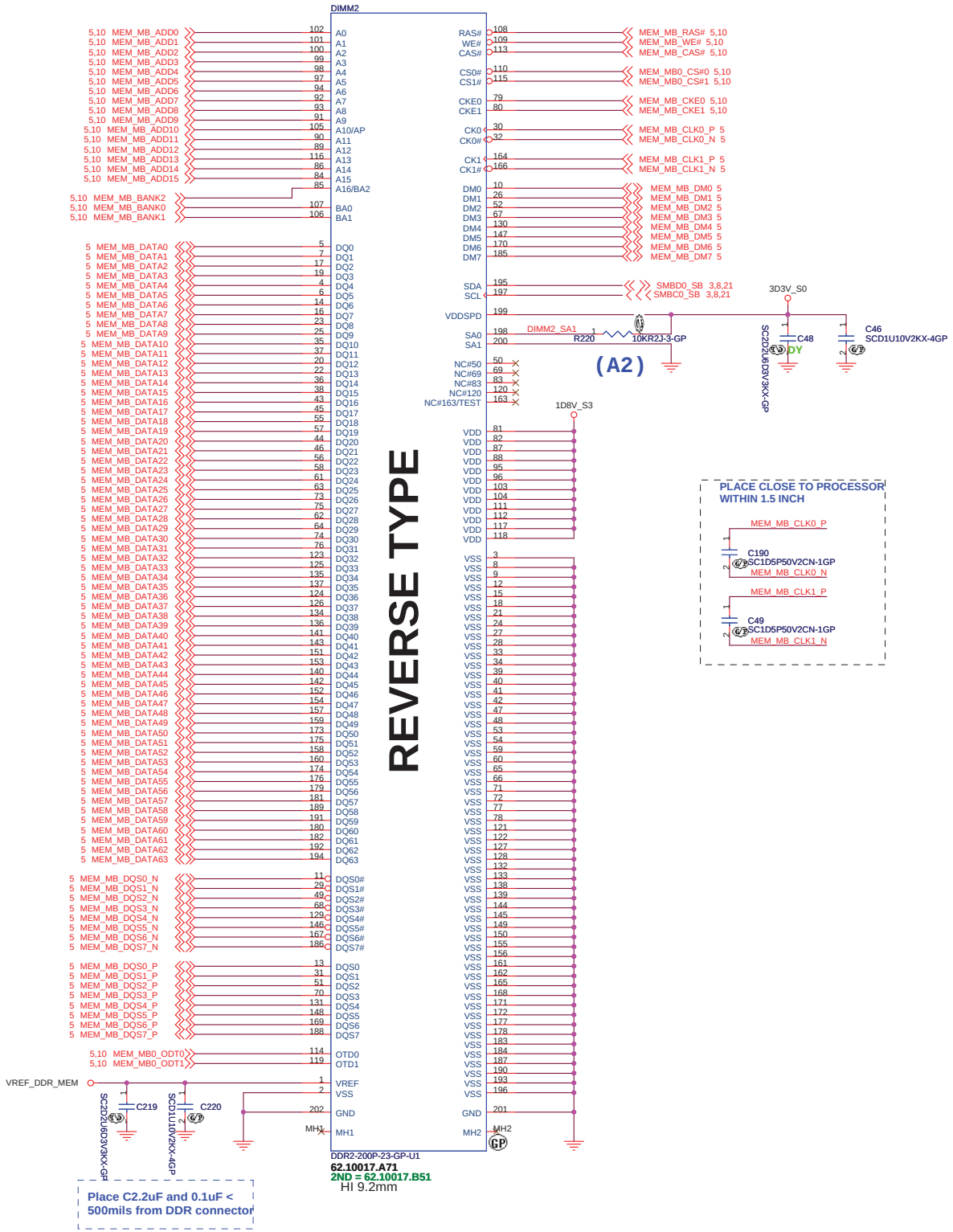
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 8 of 55



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

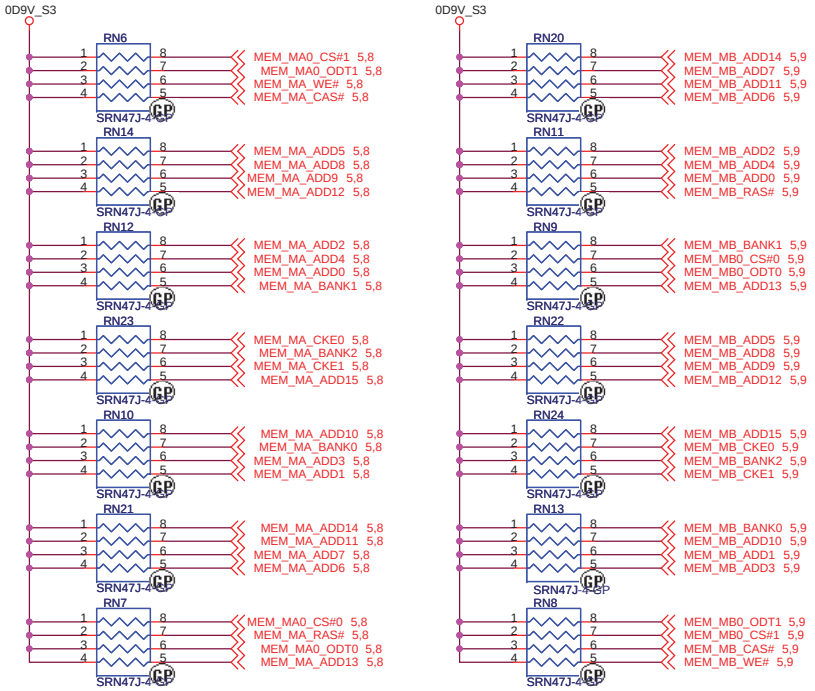
Title: DDR_SO-DIMM SKT_2

Size: Custom | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 9 of 55

PARALLEL TERMINATION

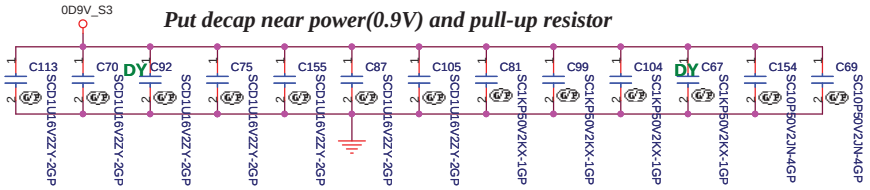
Put decap near power(0.9V) and pull-up resistor



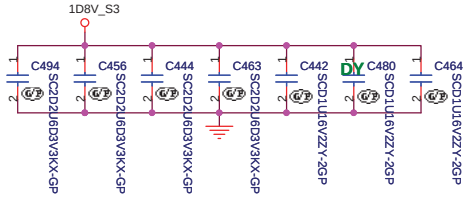
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

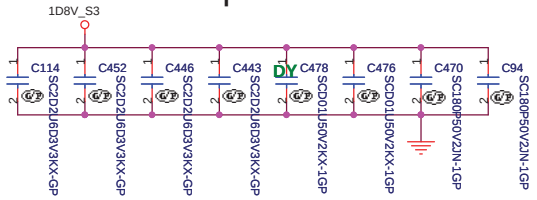


Place these Caps near DM1



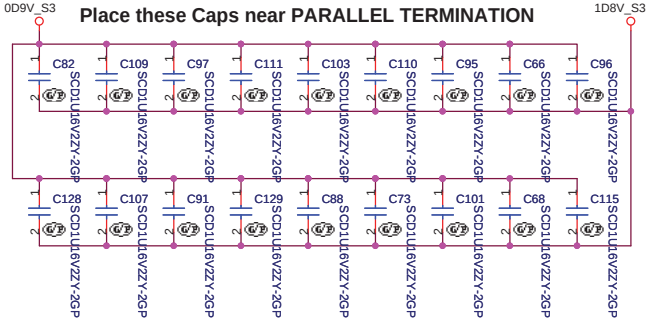
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



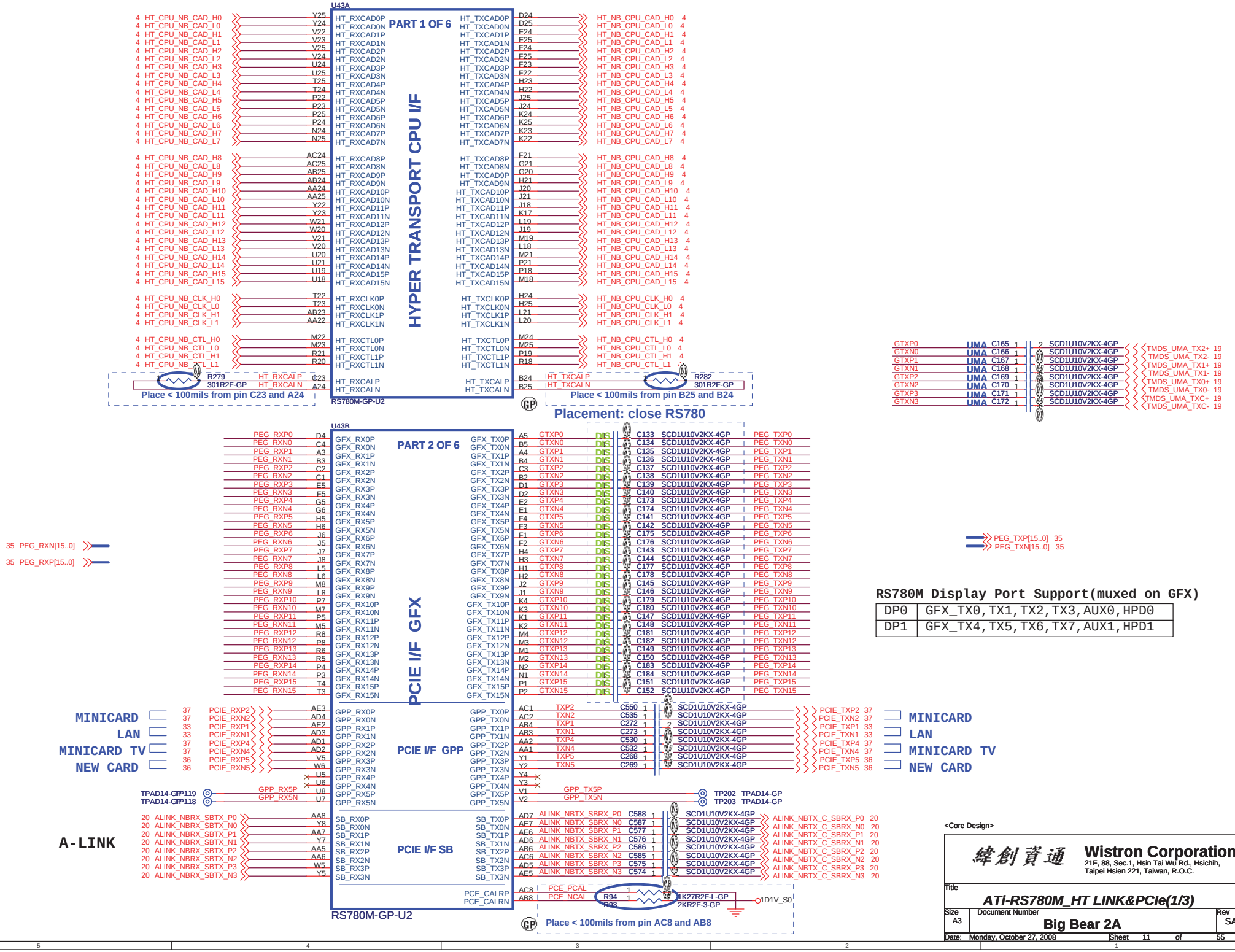
<Core Design>

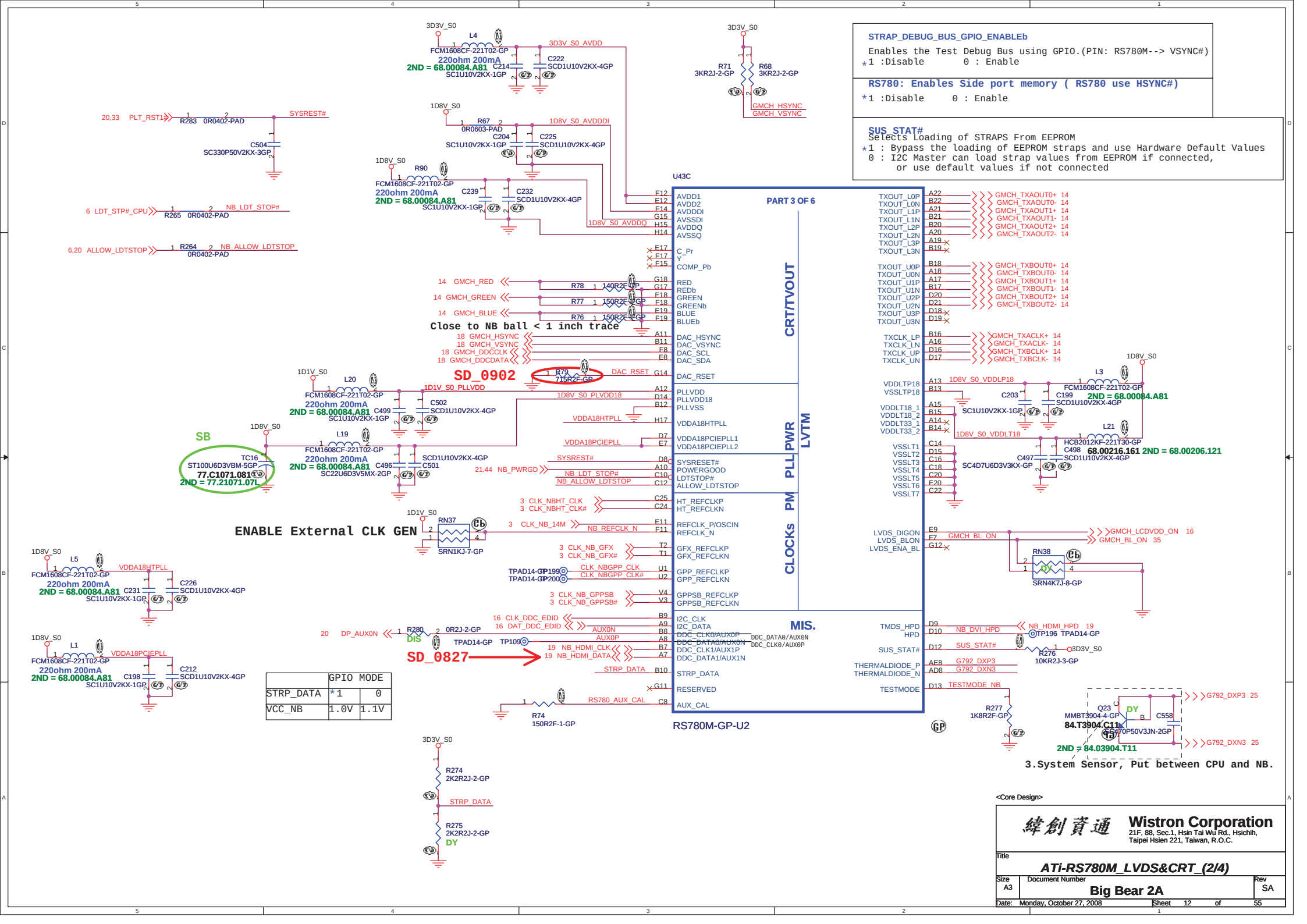
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

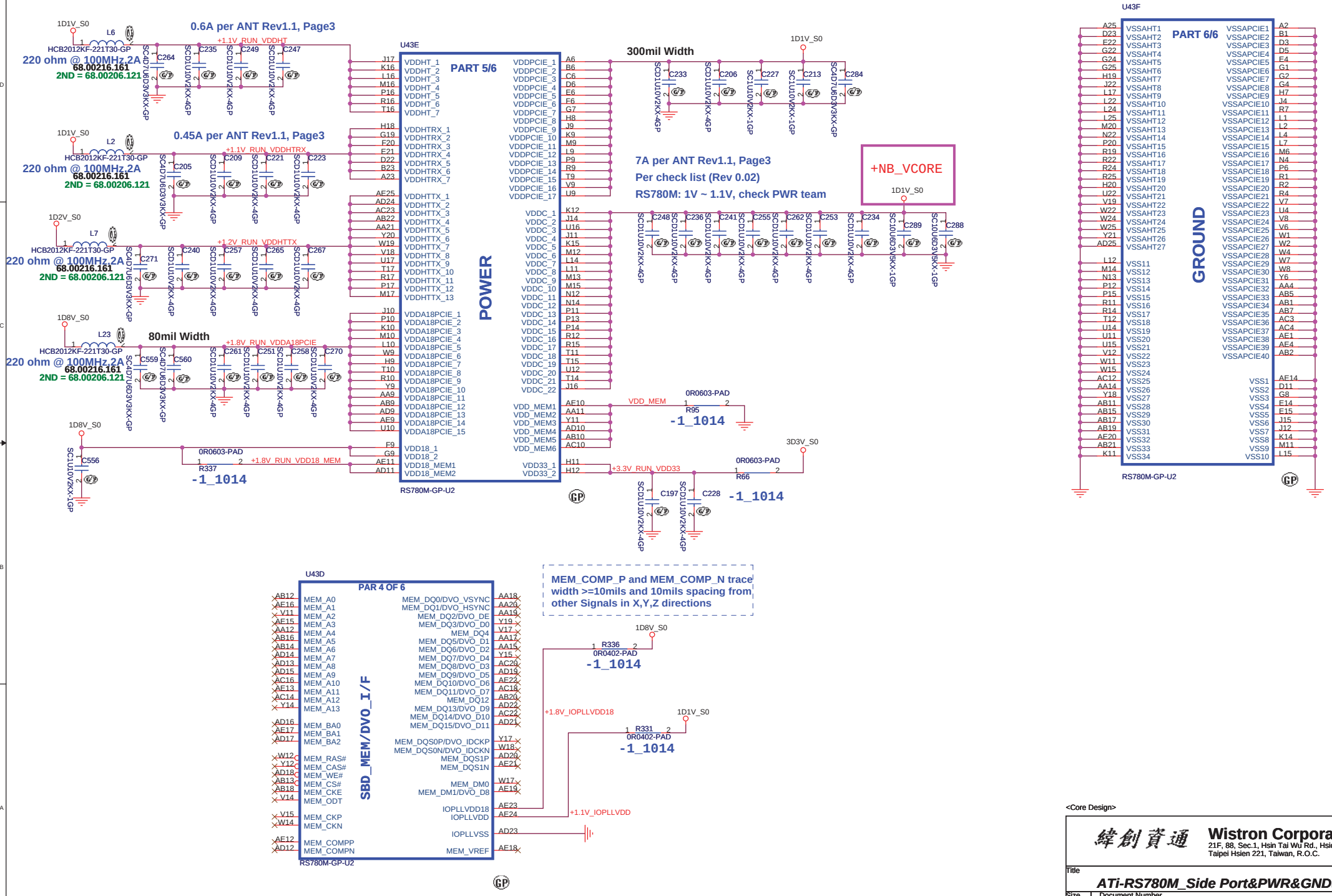
Title: ***DDR_DAMPING & TERMINATION***

Size	Document Number	Rev
A3	Big Bear 2A	SA

Date: Monday, October 27, 2008 Sheet 10 of 55


U43A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
Placement: close RS780
U43B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
Place < 100mils from pin AC8 and AB8
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
MINICARD
LAN
MINICARD TV
NEW CARD
A-LINK
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_HT LINK&PCIe(1/3)
Size A3
Document Number Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 11 of 55


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
U43C
PART 3 OF 6
RS780M-GP-U2
Close to NB ball < 1 inch trace
SD_0902
SD_0827
ENABLE External CLK GEN
SB
DIS
3.System Sensor, Put between CPU and NB.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_LVDS&CRT_(2/4)
Big Bear 2A
Monday, October 27, 2008

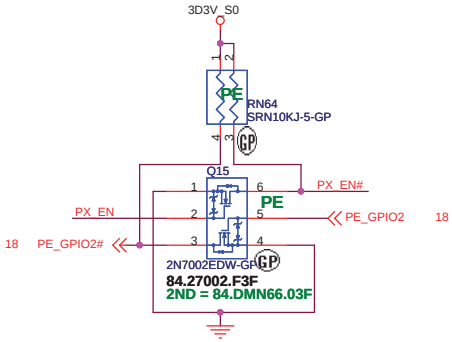


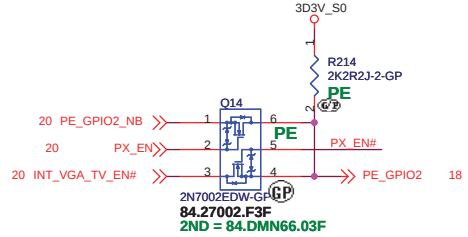
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_Side Port&PWR&GND(3/3)

Size: A3 | Document Number: Big Bear 2A | Rev: SA

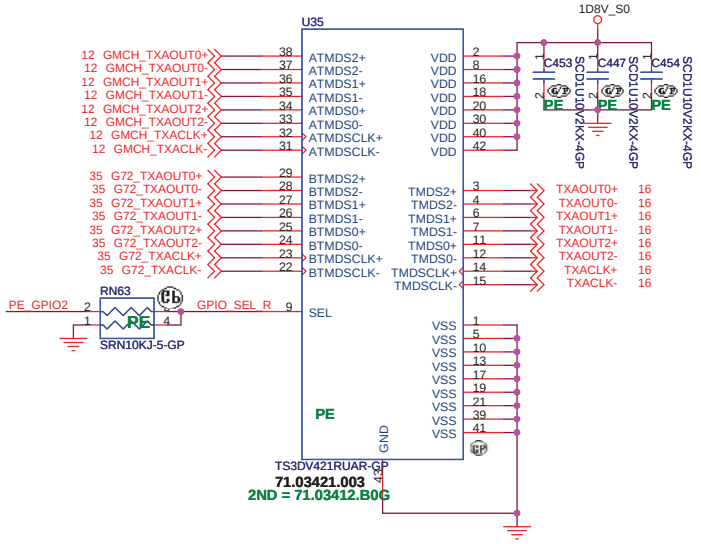
Date: Monday, October 27, 2008 | Sheet 13 of 55

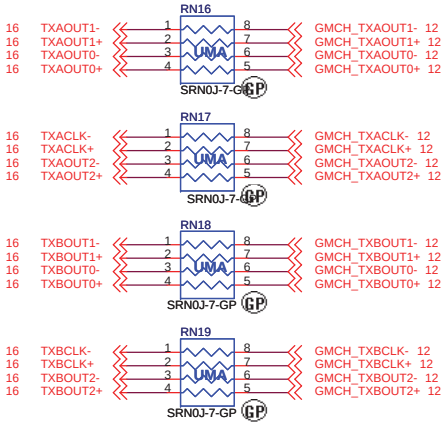


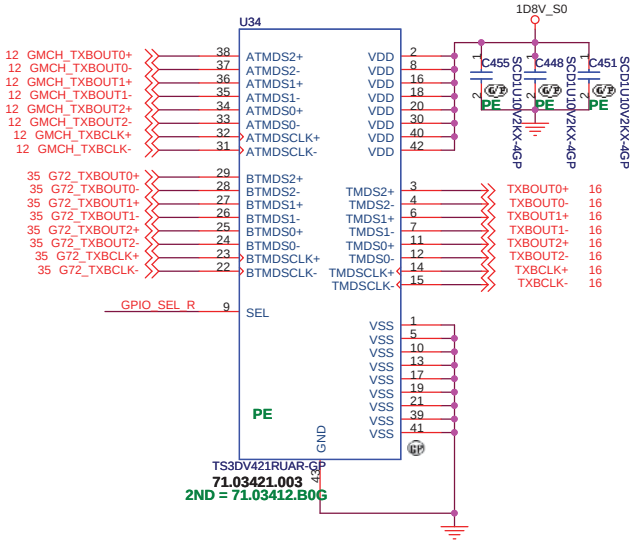


FUNCTION TABLE

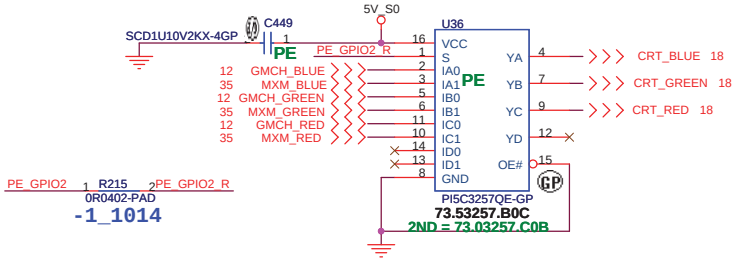
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

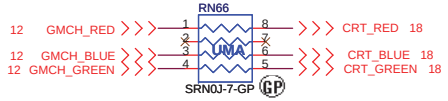






$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SWITCH**

Size: A3 | Document Number: **Big Bear 2A** | Rev: SB

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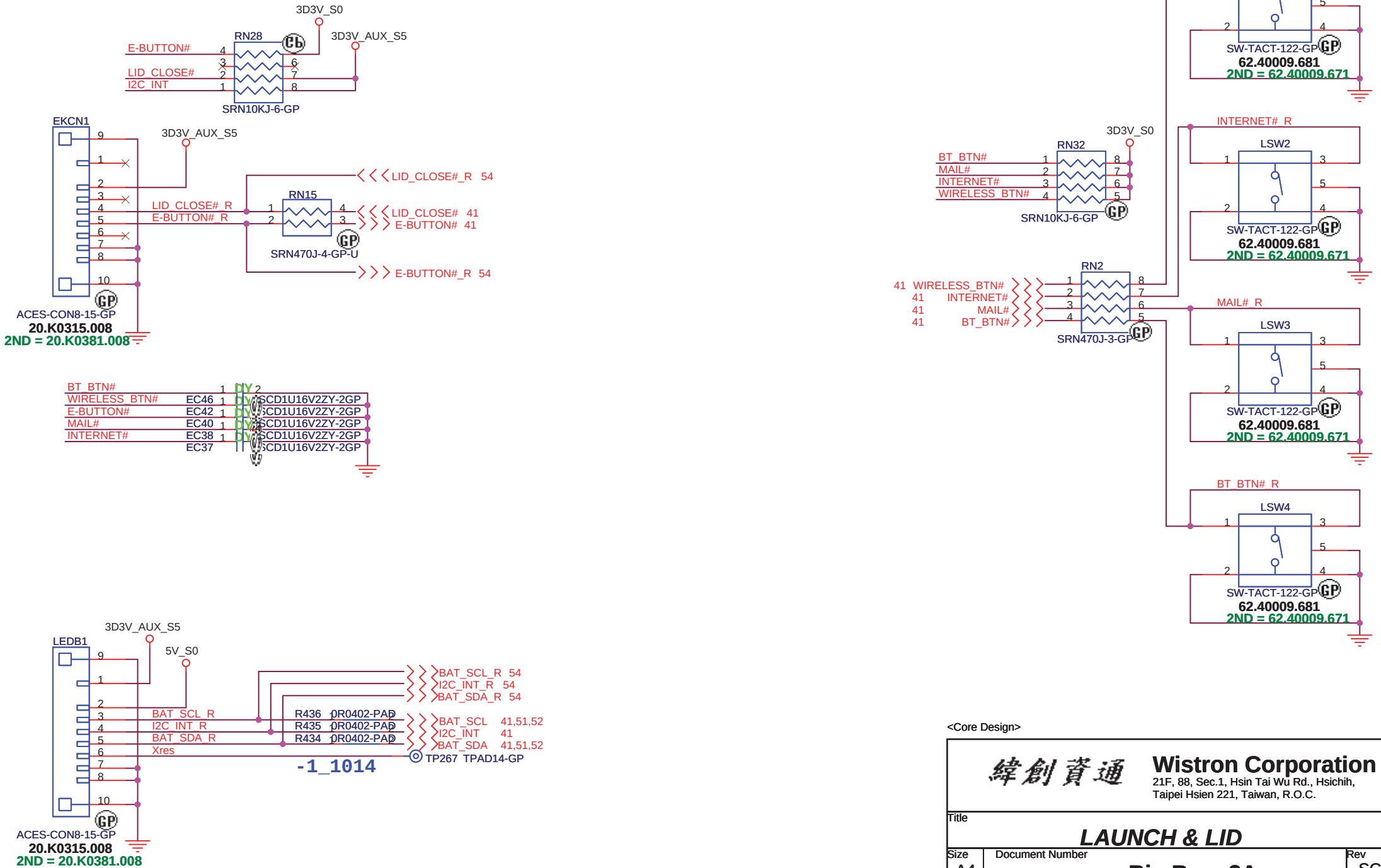
LAUNCH



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAUNCH & LID**

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A4	Big Bear 2A	SC

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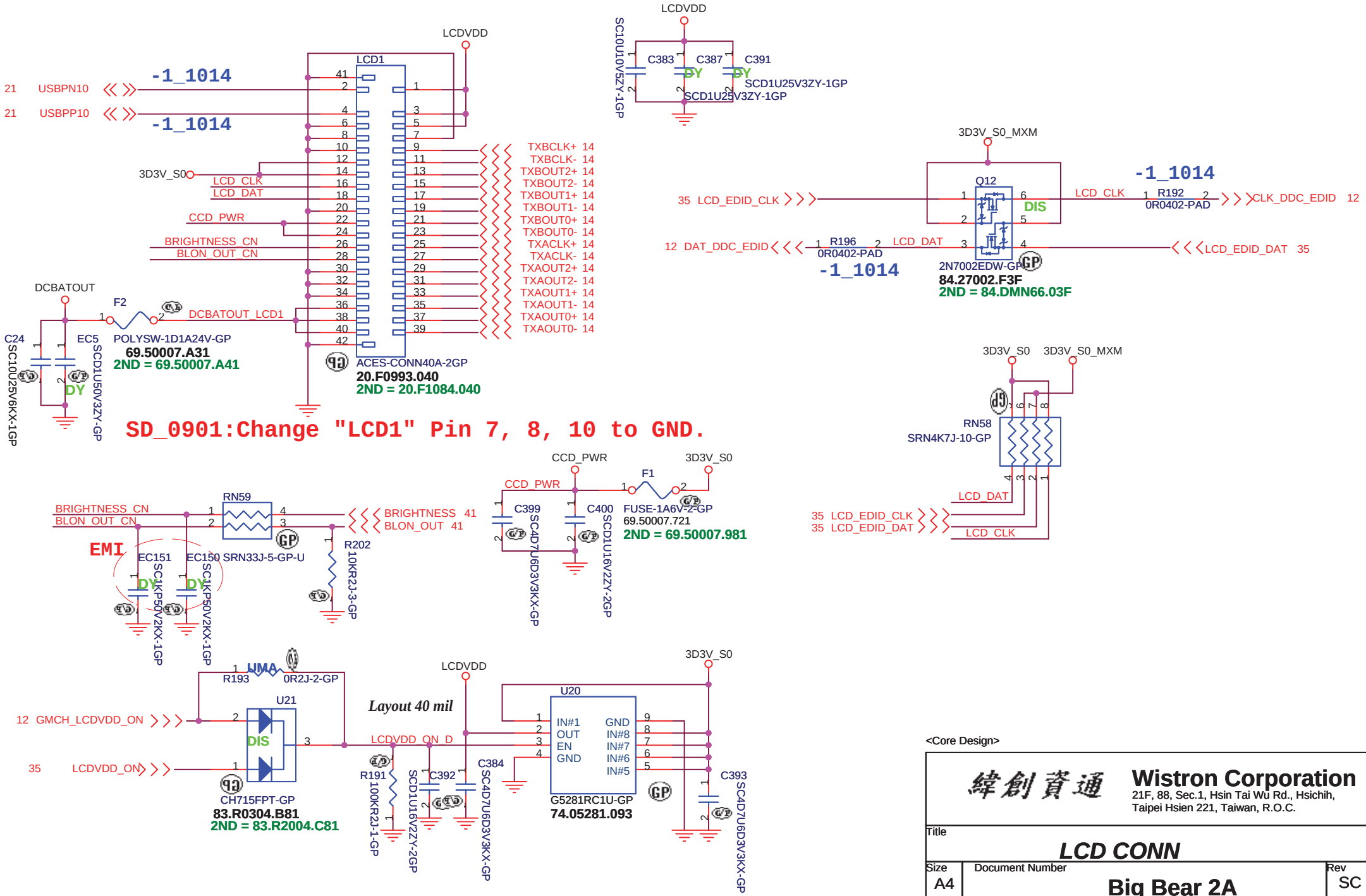
LCD/INVERTER/CCD CONN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN**

Size	Document Number	Rev
A4	Big Bear 2A	SC

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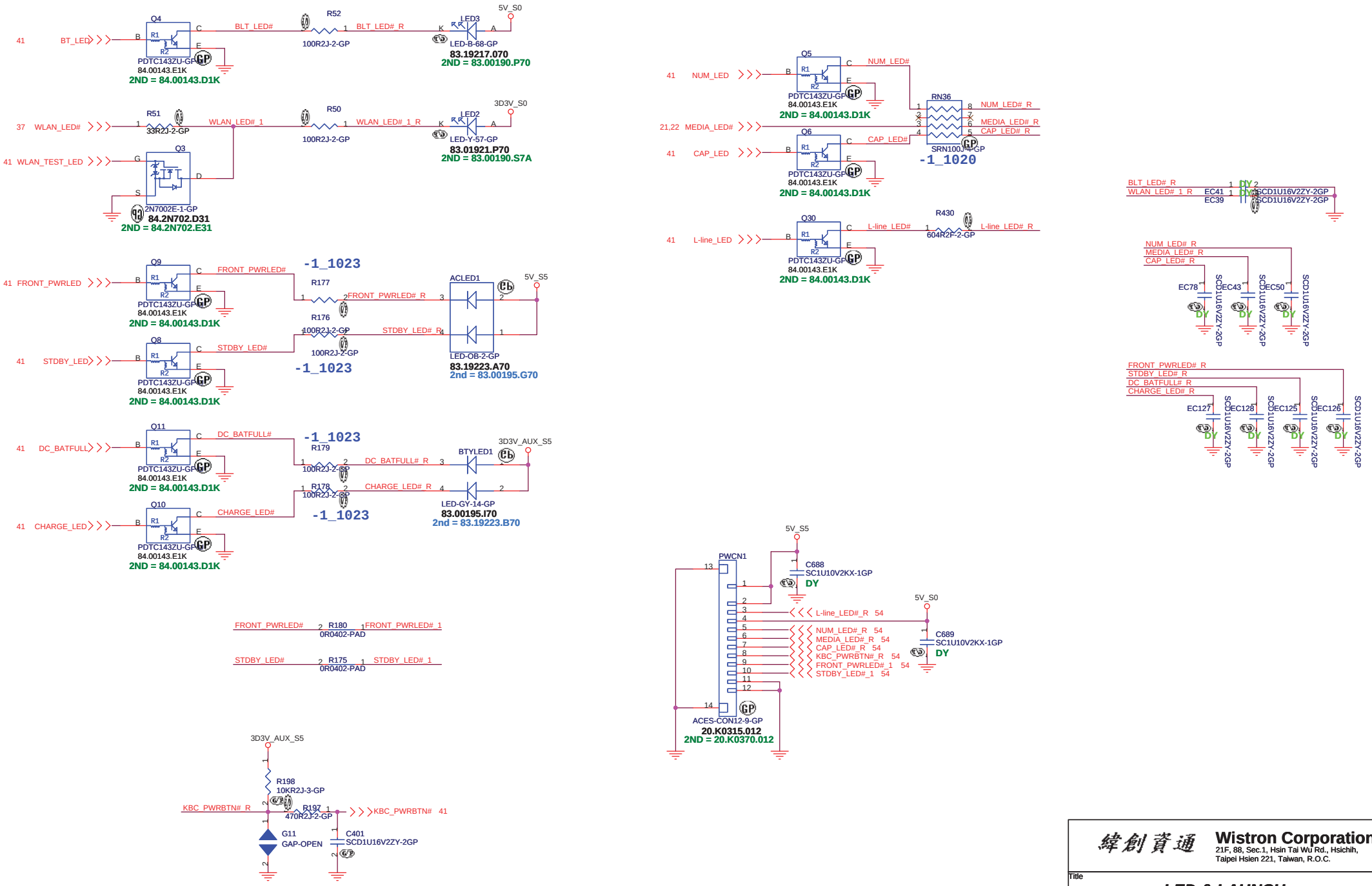
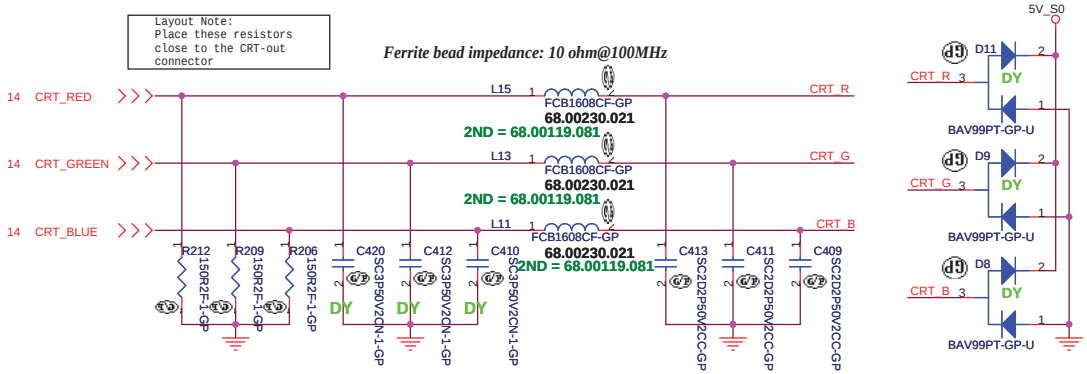
LED



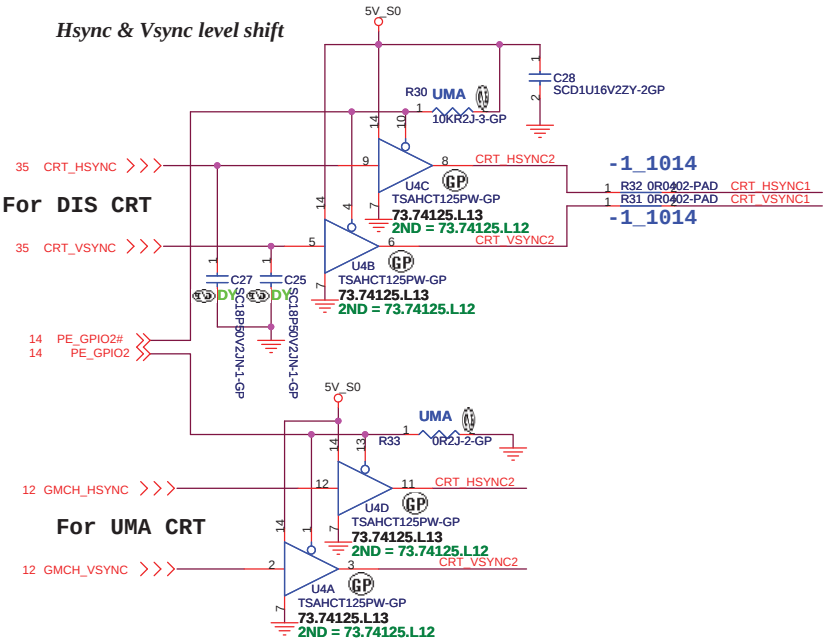
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED & LAUNCH	
Size: A3	Document Number: Big Bear 2A	Rev: SC
Date: Monday, October 27, 2008	Sheet 17 of 55	

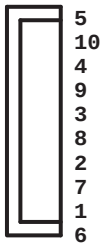


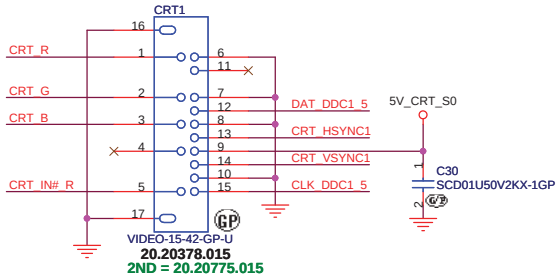
Change C409; C411, C413 to 1.5pF (78.1R574.1FL) in UMA

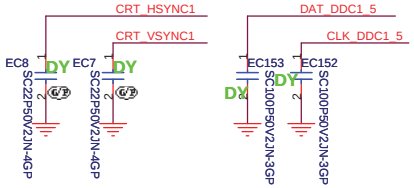
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

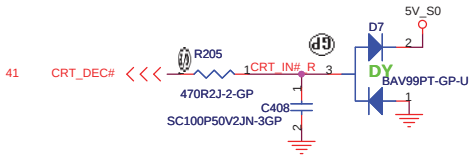


CRT I/F & CONNECTOR

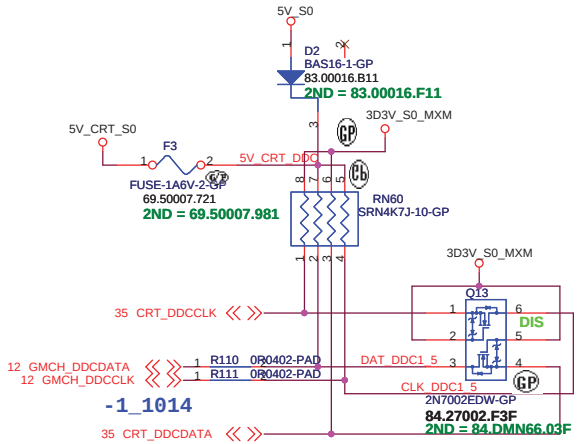








DDC_CLK & DATA level shift



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size | Document Number: **Big Bear 2A** | Rev: SA

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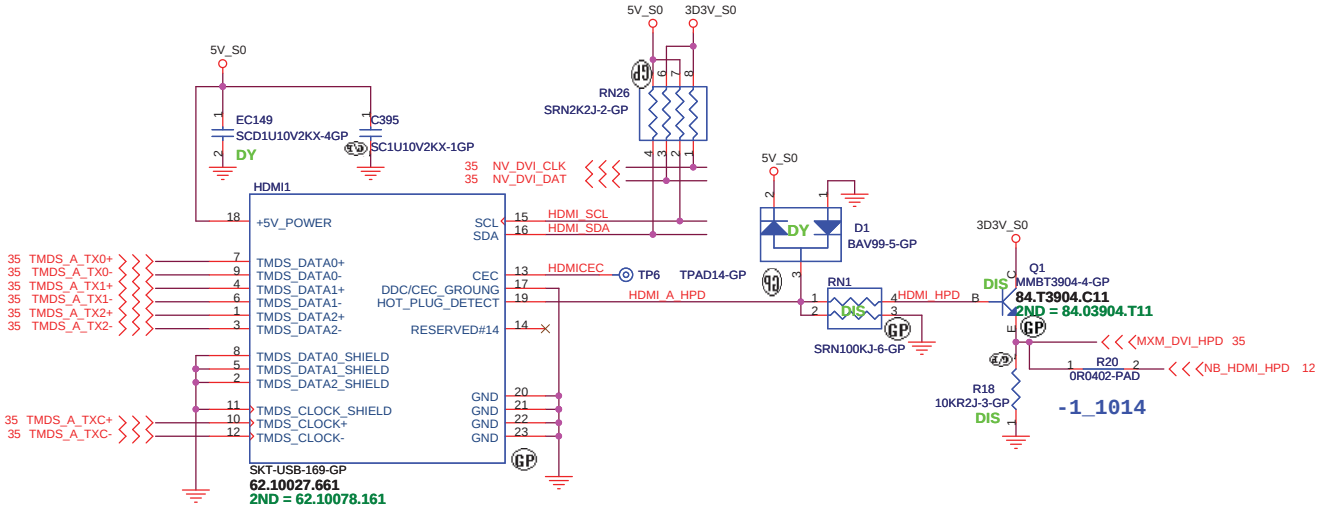
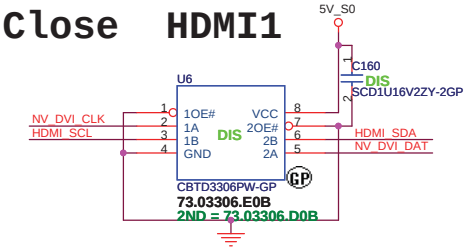
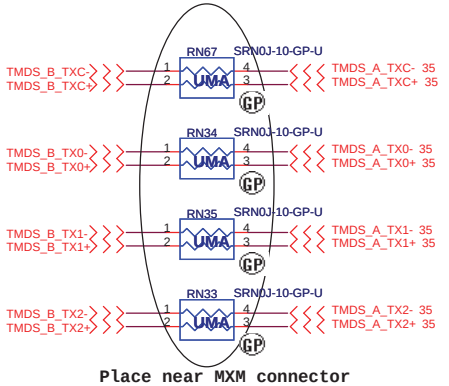
HDMI SM BUS LEVEL shifter

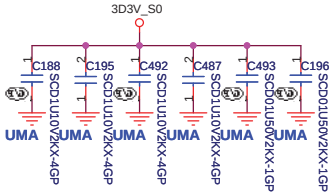
Close HDMI1

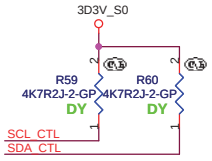


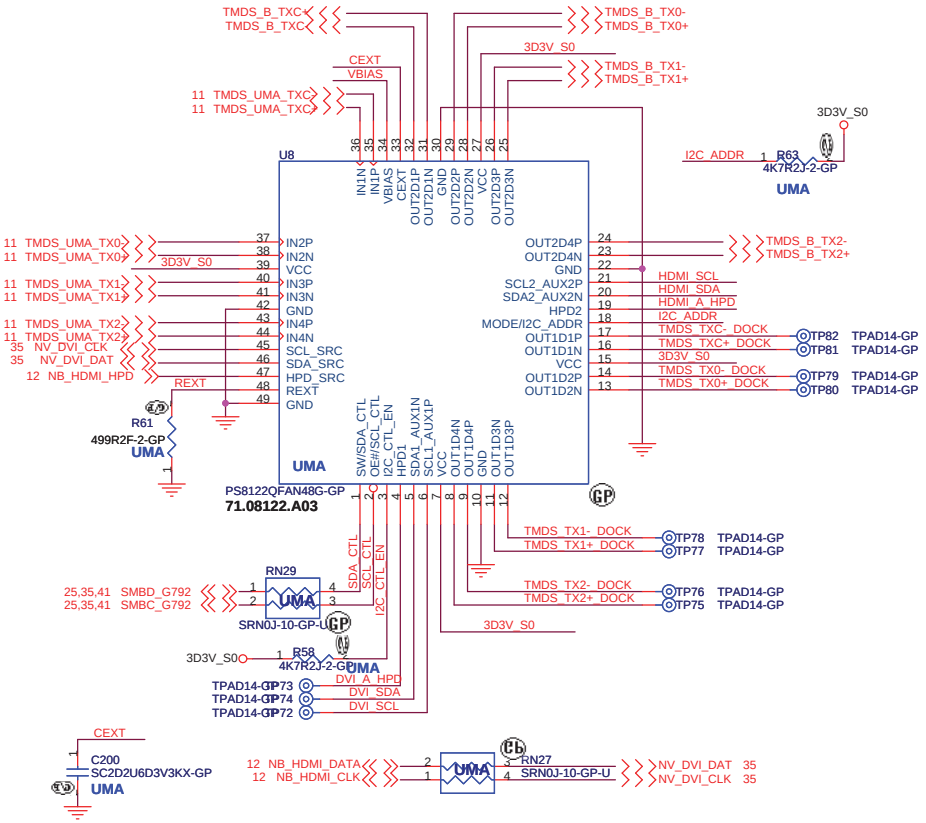




Place near MXM connector







<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI CONNECTOR

Size	Document Number	Rev
A3	Big Bear 2A	SD

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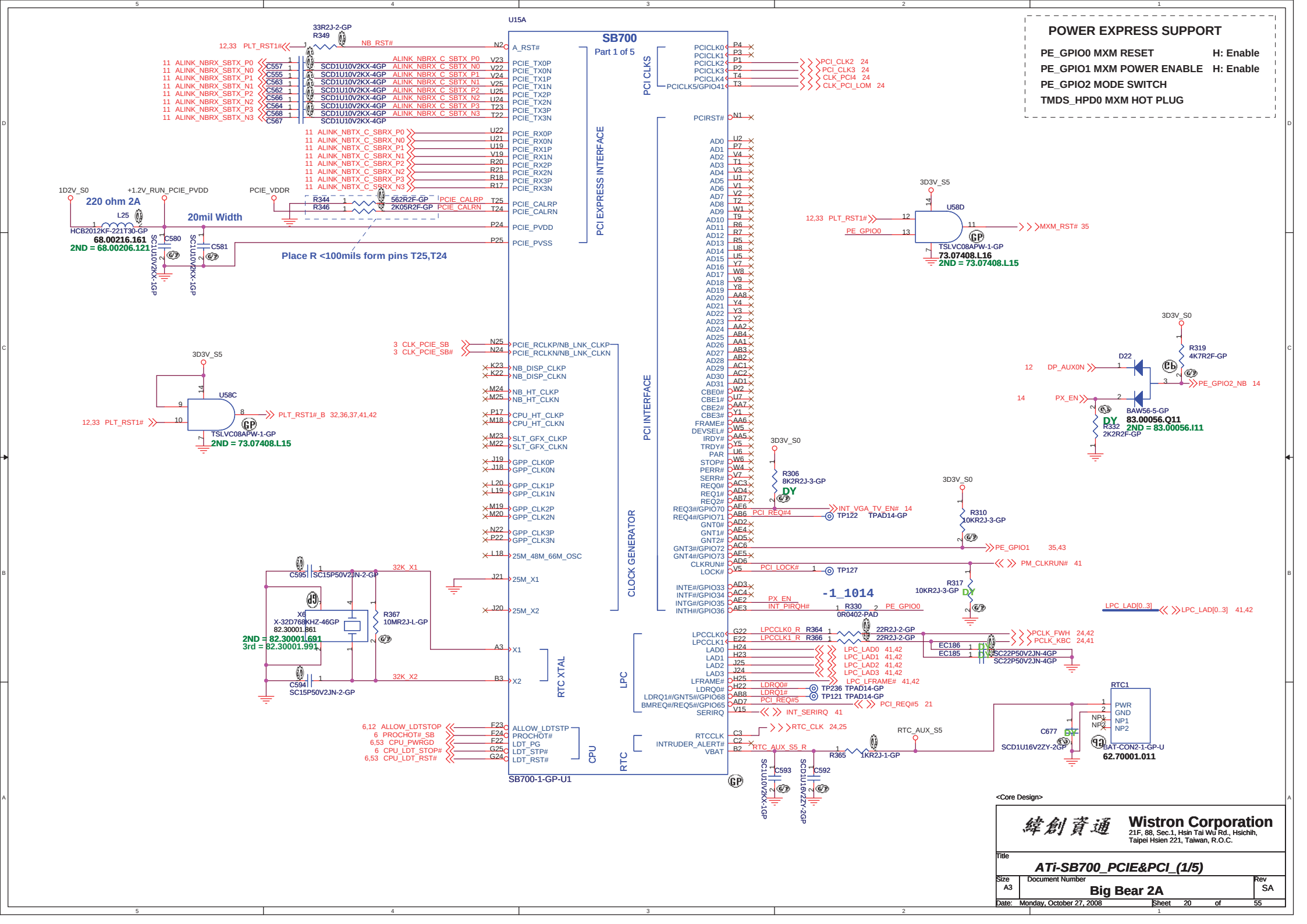
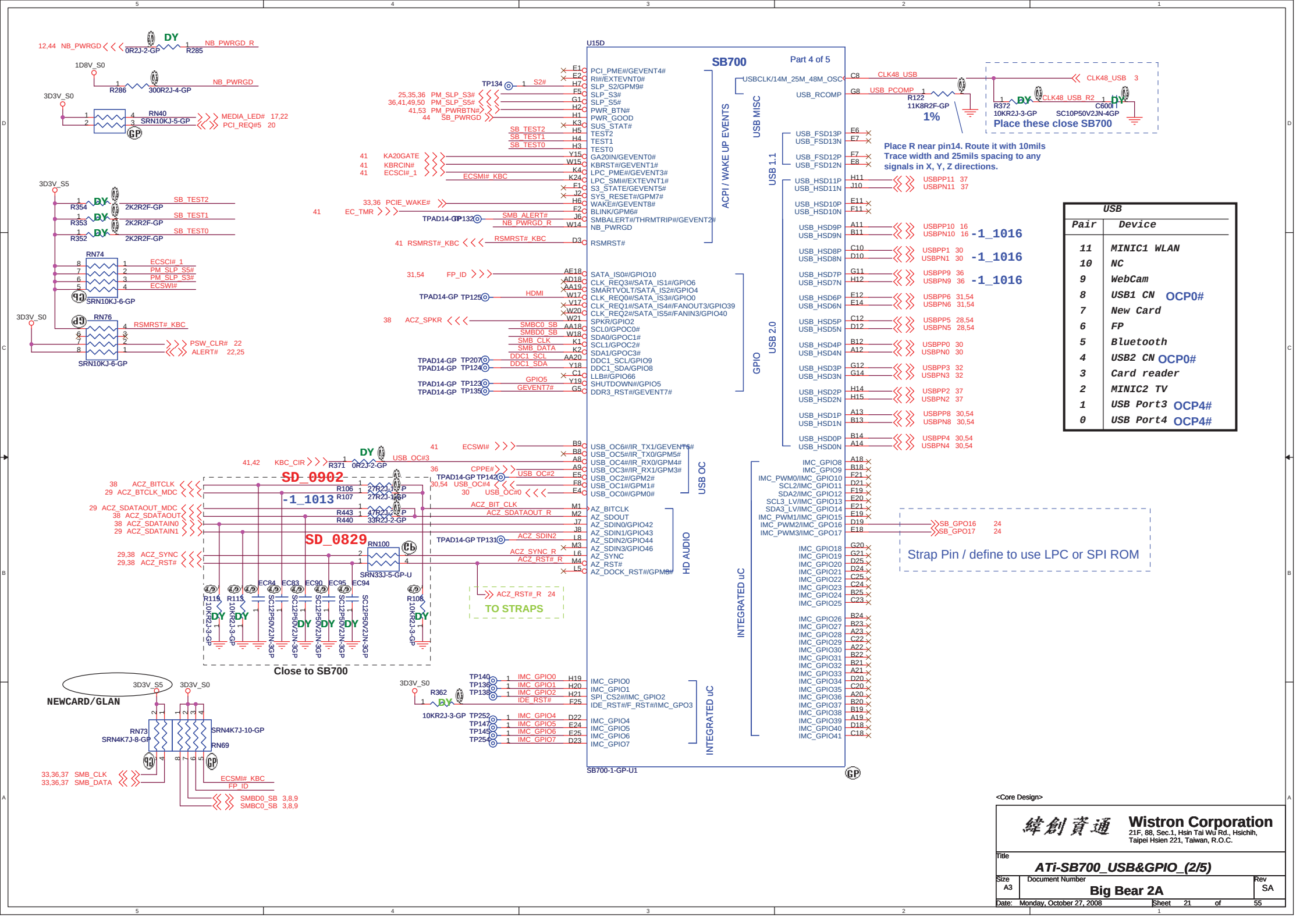
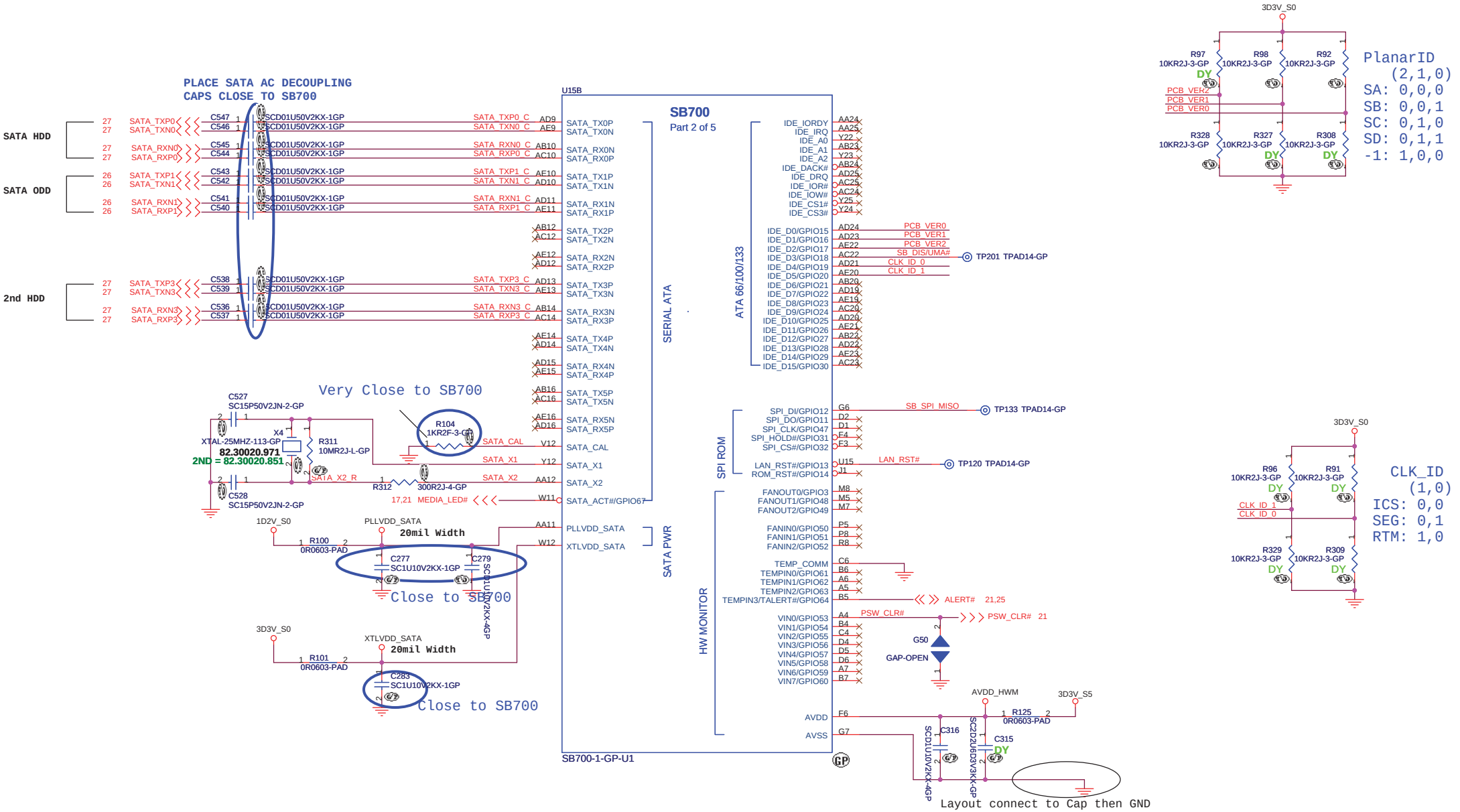

POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMDS_HPD0 MXM HOT PLUG
U15A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB700-1-GP-U1
33R2J-2-GP
R349
NB_RST#
12,33 PLT_RST1#
ALINK_NBRX_SBTX_P0
ALINK_NBRX_SBTX_N0
ALINK_NBRX_SBTX_P1
ALINK_NBRX_SBTX_N1
ALINK_NBRX_SBTX_P2
ALINK_NBRX_SBTX_N2
ALINK_NBRX_SBTX_P3
ALINK_NBRX_SBTX_N3
SCD1U10V2KX-4GP
ALINK_NBRX_C_SBTX_P0
ALINK_NBRX_C_SBTX_N0
ALINK_NBRX_C_SBTX_P1
ALINK_NBRX_C_SBTX_N1
ALINK_NBRX_C_SBTX_P2
ALINK_NBRX_C_SBTX_N2
ALINK_NBRX_C_SBTX_P3
ALINK_NBRX_C_SBTX_N3
ALINK_NBTX_C_SBRX_P0
ALINK_NBTX_C_SBRX_N0
ALINK_NBTX_C_SBRX_P1
ALINK_NBTX_C_SBRX_N1
ALINK_NBTX_C_SBRX_P2
ALINK_NBTX_C_SBRX_N2
ALINK_NBTX_C_SBRX_P3
ALINK_NBTX_C_SBRX_N3
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
1D2V_S0
220 ohm 2A
L25
HCB2012KF-221T30-GP
68.00216.161
2ND = 68.00206.121
+1.2V_RUN_PCIE_PVDD
20mil Width
C580
C581
SC1U10V2KX-1GP
PCIE_VDDR
R344
562R2F-GP
R346
2K05R2F-GP
PCIE_CALRP
PCIE_CALRN
Place R <100mils form pins T25,T24
PCIE_PVDD
PCIE_PVSS
A_RST#
PCIRST#
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCI_CLK2 24
PCI_CLK3 24
CLK_PCI4 24
CLK_PCI_LOM 24
3D3V_S5
U58D
TSLVC08APW-1GP
73.07408.L16
2ND = 73.07408.L15
PE_GPIO0
MXM_RST# 35
3D3V_S0
R319
4K7R2F-GP
D22
BAW56-5-GP
83.00056.Q11
2ND = 83.00056.I11
R332
2K2R2F-GP
DP_AUX0N
PE_GPIO2_NB 14
PX_EN
U58C
TSLVC08APW-1GP
73.07408.L15
PLT_RST1#_B 32,36,37,41,42
3 CLK_PCIE_SB
3 CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
25M_48M_66M_OSC
25M_X1
25M_X2
32K_X1
32K_X2
X6
X-32D768KHZ-46GP
82.30001.861
2ND = 82.30001.691
3rd = 82.30001.991
R367
10MR2J-L-GP
C595
C594
SC15P50V2JN-2-GP
X1
X2
ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
6,12 ALLOW_LDTSTOP
6 PROCHOT#_SB
6,53 CPU_PWRGD
6 CPU_LDT_STOP#
6,53 CPU_LDT_RST#
REQ3#/GPIO70
REQ4#/GPIO71
GNT0#
GNT1#
GNT2#
GNT3#/GPIO72
GNT4#/GPIO73
CLKRUN#
LOCK#
INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
PCI_REQ#4
INT_VGA_TV_EN# 14
TP122
TPAD14-GP
R306
8K2R2J-3-GP
DY
PCI_LOCK#
TP127
PX_EN
INT_PIRQH#
R330
0R0402-PAD
PE_GPIO0
R310
10KR2J-3-GP
PE_GPIO1 35,43
PM_CLKRUN# 41
R317
10KR2J-3-GP
-1_1014
LPC_LAD[0..3]
LPC_LAD[0..3] 41,42
LPCCLK0
LPCCLK1
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#/GNT5#/GPIO68
BMREQ#/REQ5#/GPIO65
SERIRQ
LPCCLK0_R R364
LPCCLK1_R R366
22R2J-2-GP
PCLK_FWH 24,42
PCLK_KBC 24,41
EC186
EC185
SC22P50V2JN-4GP
LPC_LAD0 41,42
LPC_LAD1 41,42
LPC_LAD2 41,42
LPC_LAD3 41,42
LPC_LFRAME# 41,42
LDRQ0#
LDRQ1#
TP236 TPAD14-GP
TP121 TPAD14-GP
PCI_REQ#5
PCI_REQ#5 21
INT_SERIRQ 41
RTCCLK
INTRUDER_ALERT#
VBAT
RTC_CLK 24,25
RTC_AUX_S5_R
RTC_AUX_S5
R365
1KR2J-1-GP
C593
C592
SC1U10V2KX-1GP
SCD1U16V2ZY-2GP
C677
SCD1U16V2ZY-2GP
RTC1
PWR
GND
NP1
NP2
BAT-CON2-1-GP-U
62.70001.011
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_PCIE&PCI_(1/5)
Size A3
Document Number
Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 20 of 55


SB700
Part 4 of 5
U15D
SB700-1-GP-U1
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPIO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
CLK48_USB
USB_PCOMP
R122
11K8R2F-GP
1%
R372
10KR2J-3-GP
CLK48_USB_R2
C600
SC10P50V2JN-4GP
Place these close SB700
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
-1_1016
-1_1013
SD_0902
SD_0829
Close to SB700
TO STRAPS
Strap Pin / define to use LPC or SPI ROM
NEWCARD/GLAN
USB
Pair Device
11 MINIC1 WLAN
10 NC
9 WebCam
8 USB1 CN OCP0#
7 New Card
6 FP
5 Bluetooth
4 USB2 CN OCP0#
3 Card reader
2 MINIC2 TV
1 USB Port3 OCP4#
0 USB Port4 OCP4#
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_USB&GPIO_(2/5)
Size A3
Document Number
Big Bear 2A
Rev SA
Date: Monday, October 27, 2008
Sheet 21 of 55


PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700
SATA HDD
SATA ODD
2nd HDD
U15B
SB700
Part 2 of 5
SERIAL ATA
SATA PWR
ATA 66/100/133
SPI ROM
HW MONITOR
SB700-1-GP-U1
Very Close to SB700
Close to SB700
Close to SB700
20mil Width
20mil Width
82.30020.971
2ND = 82.30020.851
PlanarID
(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
SD: 0,1,1
-1: 1,0,0
CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0
Layout connect to Cap then GND
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_SATA-IDE_(3/5)
Size
A3
Document Number
Big Bear 2A
Rev
SB
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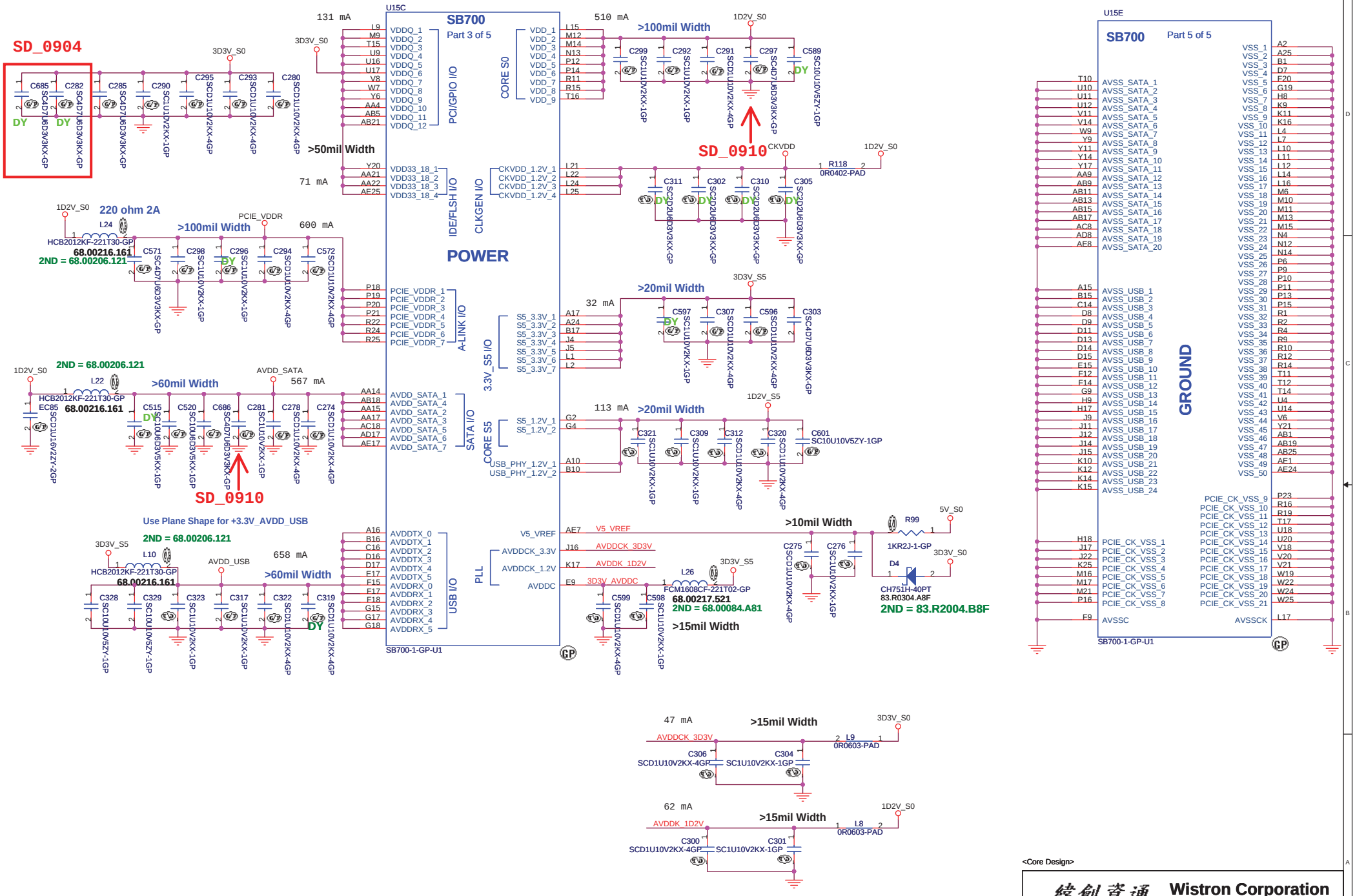
SD_0904
SB700
Part 3 of 5
U15C
131 mA
510 mA
>100mil Width
>50mil Width
71 mA
SD_0910
POWER
220 ohm 2A
>100mil Width
600 mA
2ND = 68.00206.121
68.00216.161
>60mil Width
567 mA
32 mA
>20mil Width
113 mA
Use Plane Shape for +3.3V_AVDD_USB
658 mA
>10mil Width
2ND = 83.R2004.B8F
68.00217.521
2ND = 68.00084.A81
>15mil Width
47 mA
62 mA
SB700-1-GP-U1
U15E
Part 5 of 5
GROUND
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_POWER&GND_(4/5)
Big Bear 2A
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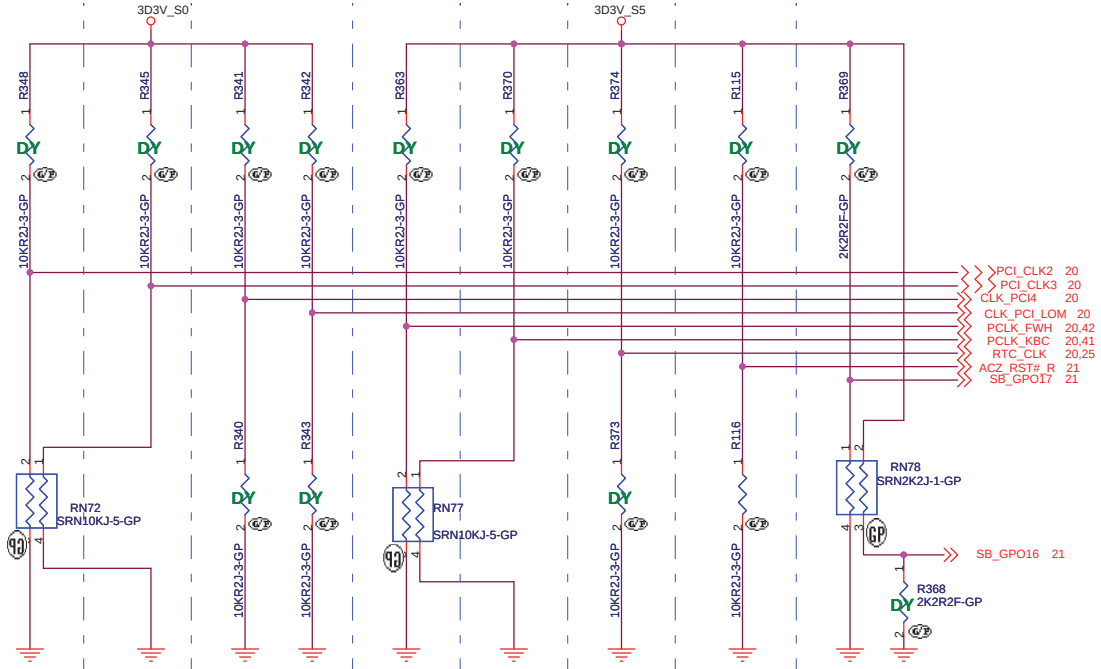
REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

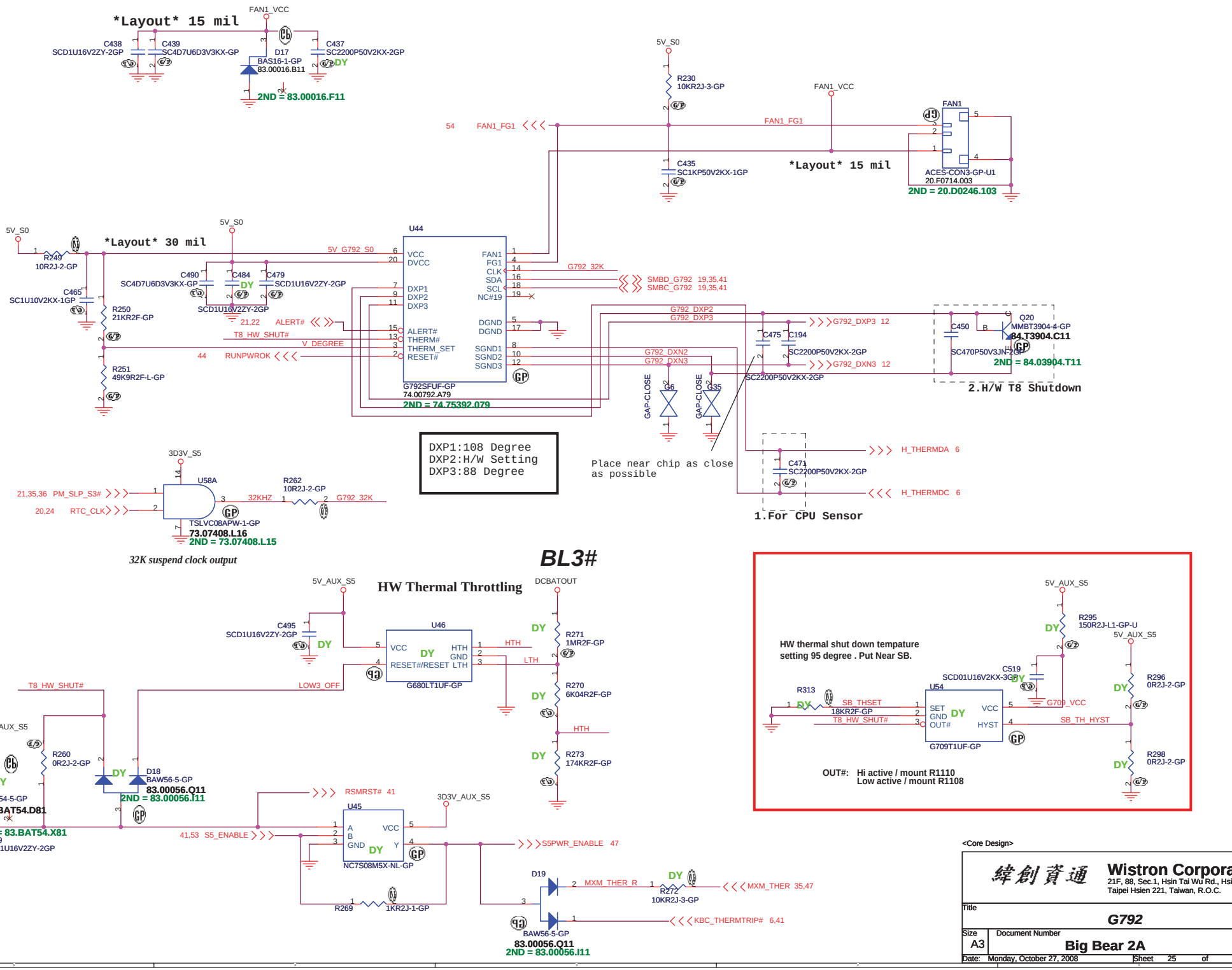
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: Big Bear 2A | Rev: SA

Date: Monday, October 27, 2008 | Sheet 24 of 55



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G792	
Size A3	Document Number Big Bear 2A	Rev SA
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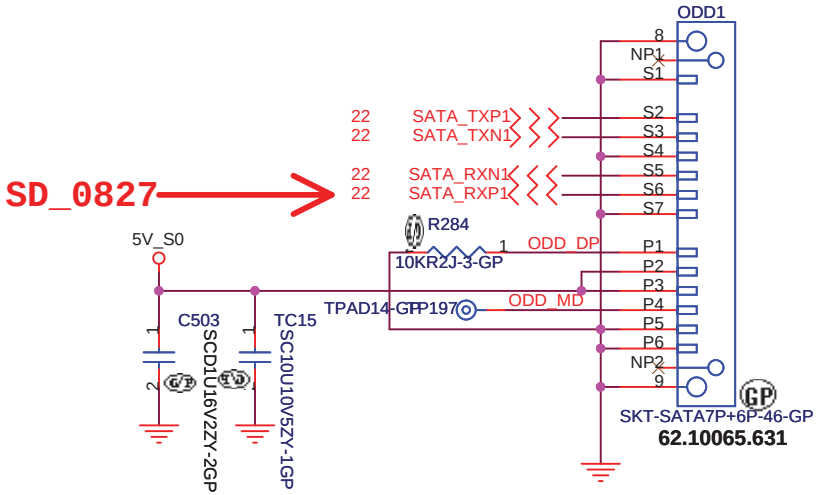
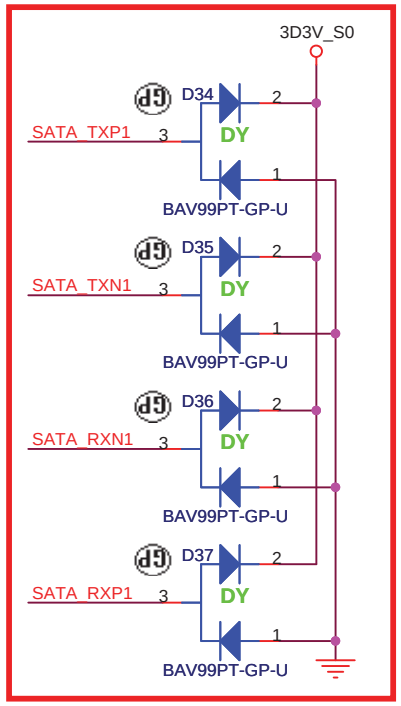
ODD Connector



SD_0828



<Core Design>

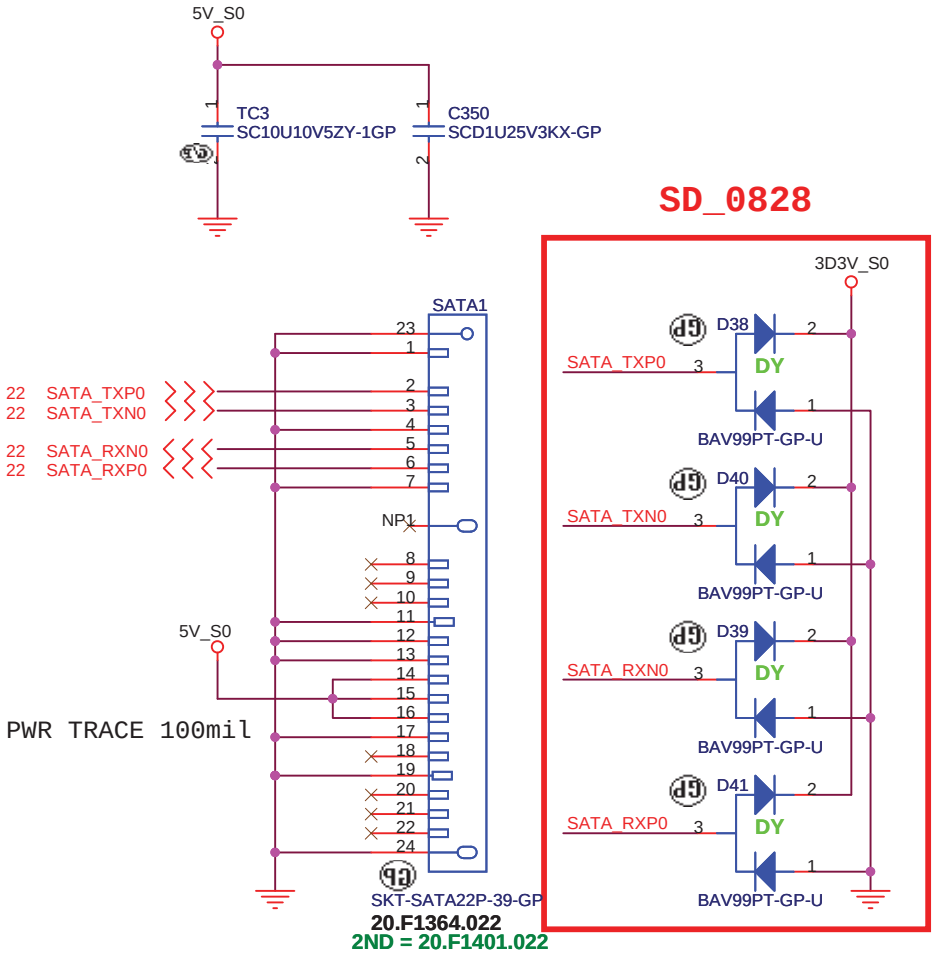
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CDROM

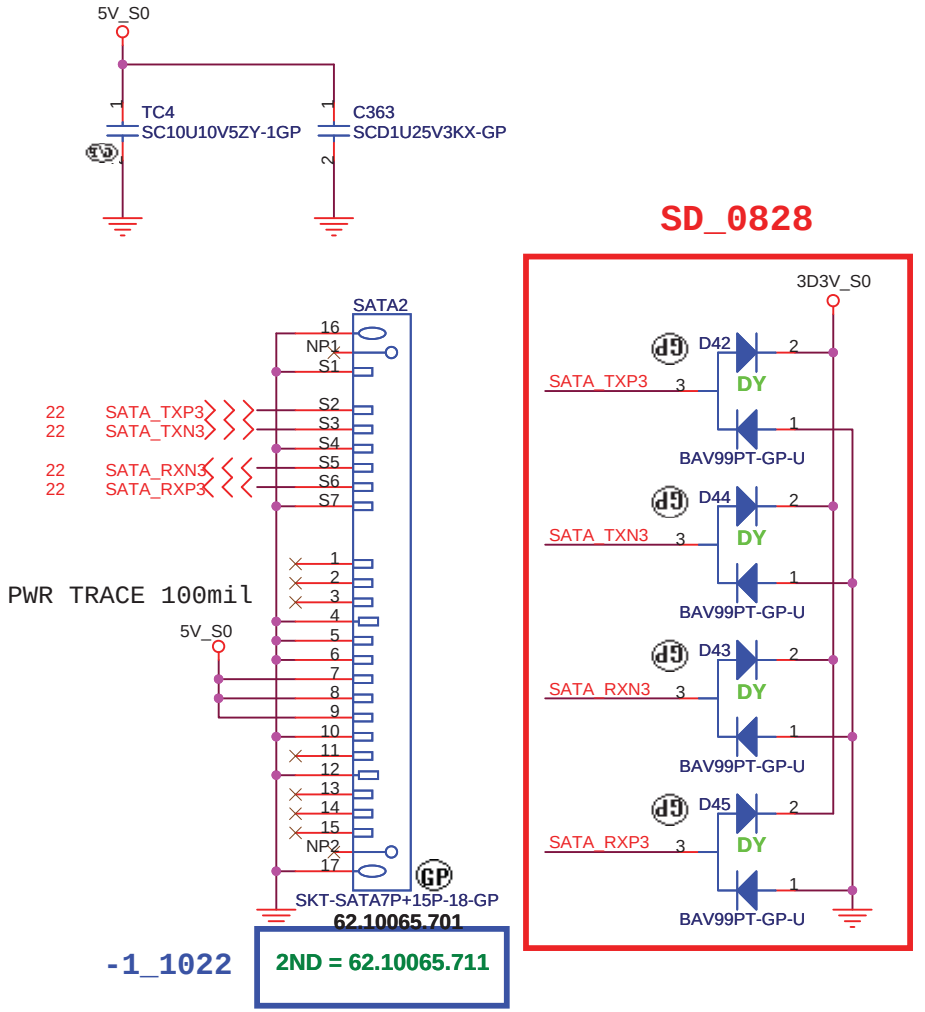
Size	Document Number	Rev
A4	Big Bear 2A	SD

Date: Monday, October 27, 2008 Sheet 26 of 55

SATA HDD Connector



2ND SATA HDD Connector



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD	
Size: A4	Document Number: Big Bear 2A	Rev: SD
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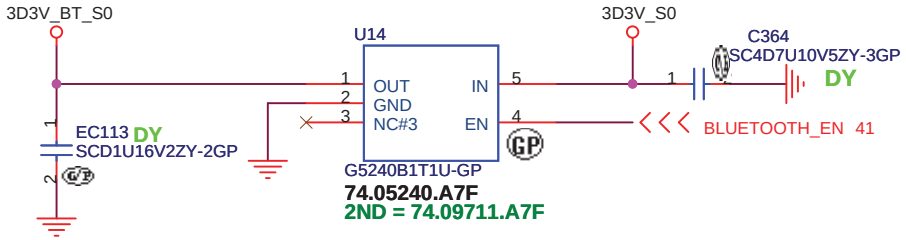
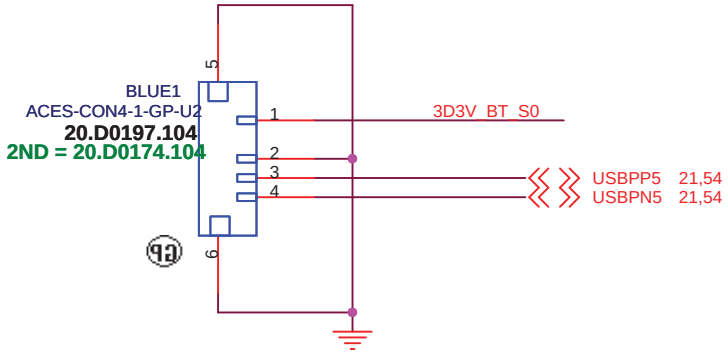
BLUETOOTH MODULE



EC40 put near BLUE1 / all USB put one choke near connector by EMI request



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLUETOOTH***

Size	Document Number	Rev
A4	Big Bear 2A	SA

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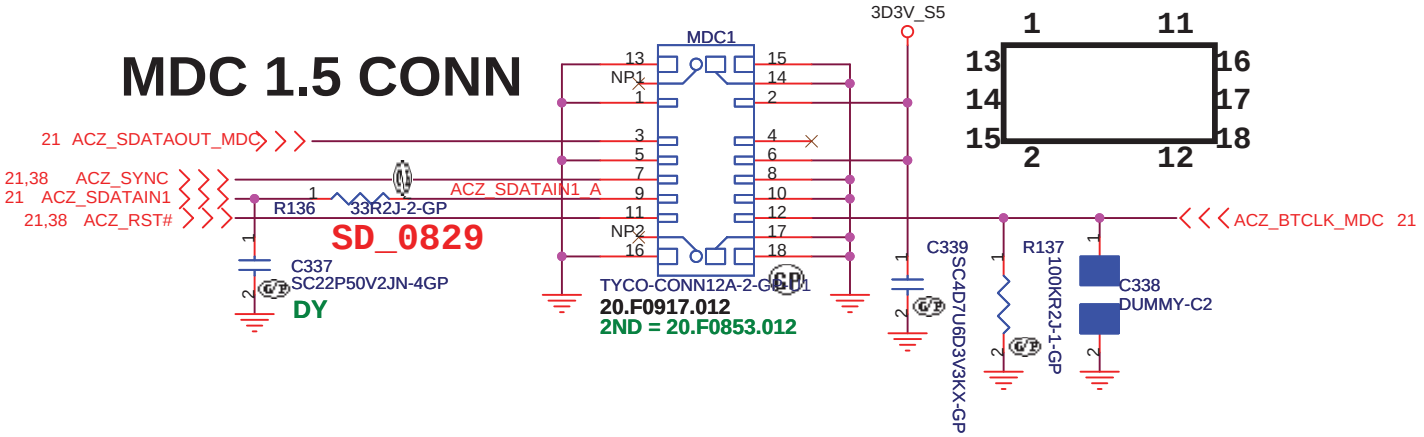
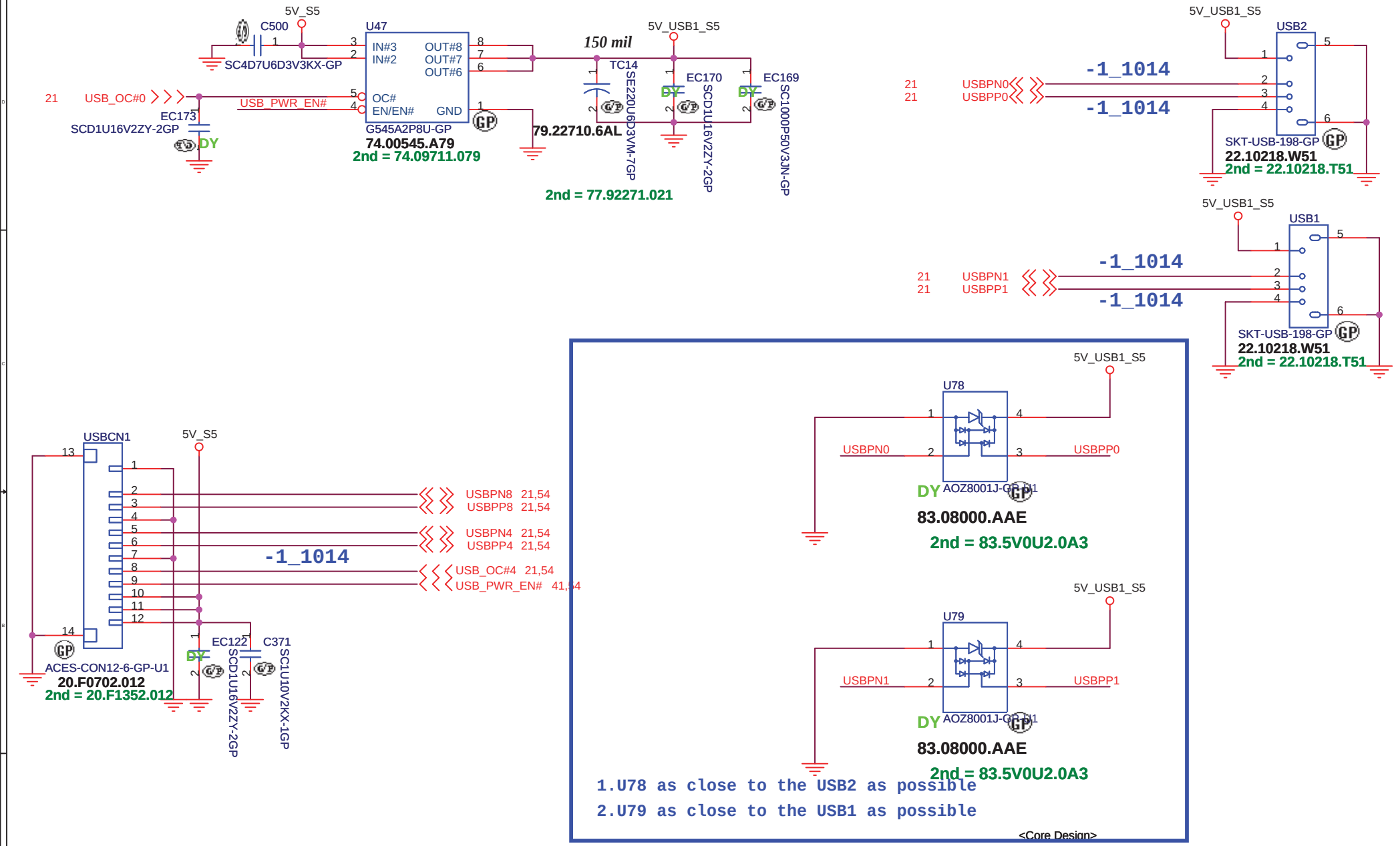
MDC 1.5 CONN



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MDC***
Size: A4	Document Number: **Big Bear 2A**
Rev: SA	
Date: Monday, October 27, 2008	Sheet 29 of 55



ESD Protection

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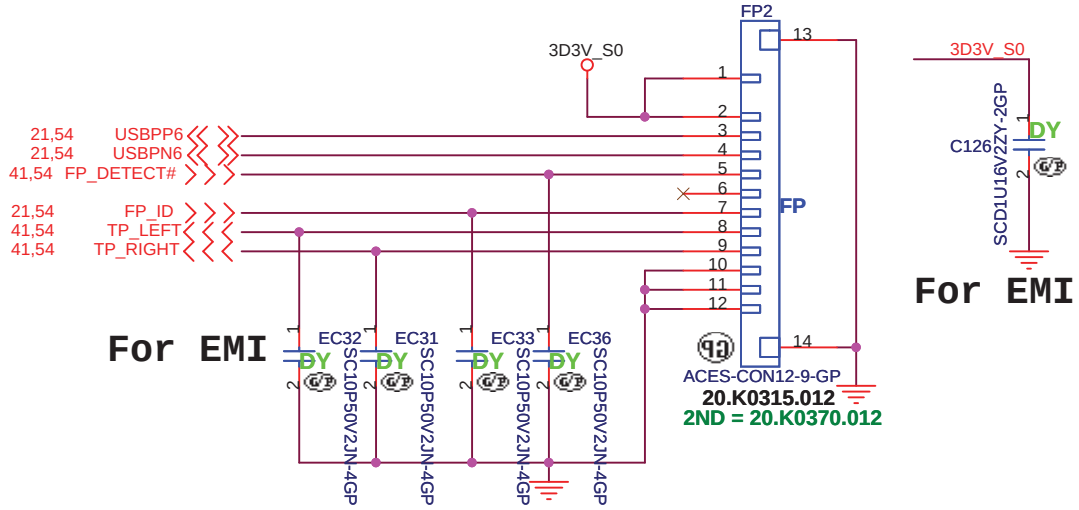
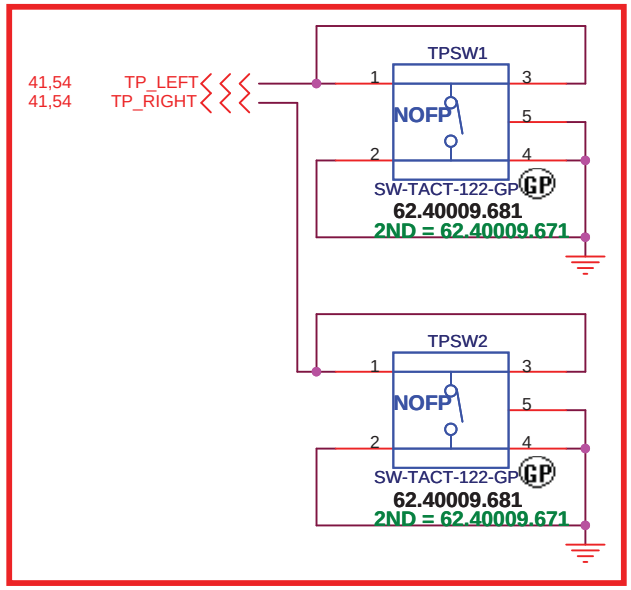
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB	
Size: A4	Document Number: Big Bear 2A	Rev: SB
Date: Monday, October 27, 2008	Sheet 30 of 55	

Finger printer



SD_0903



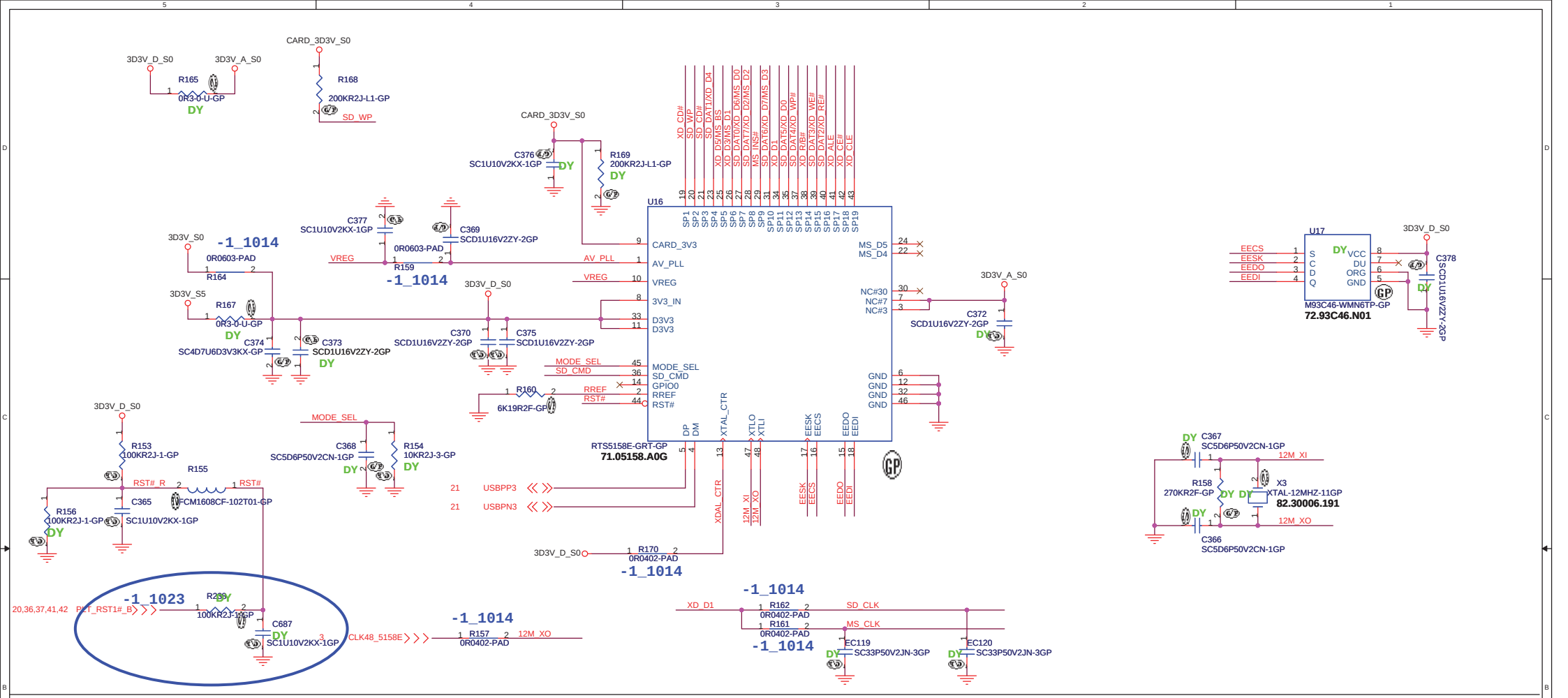
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

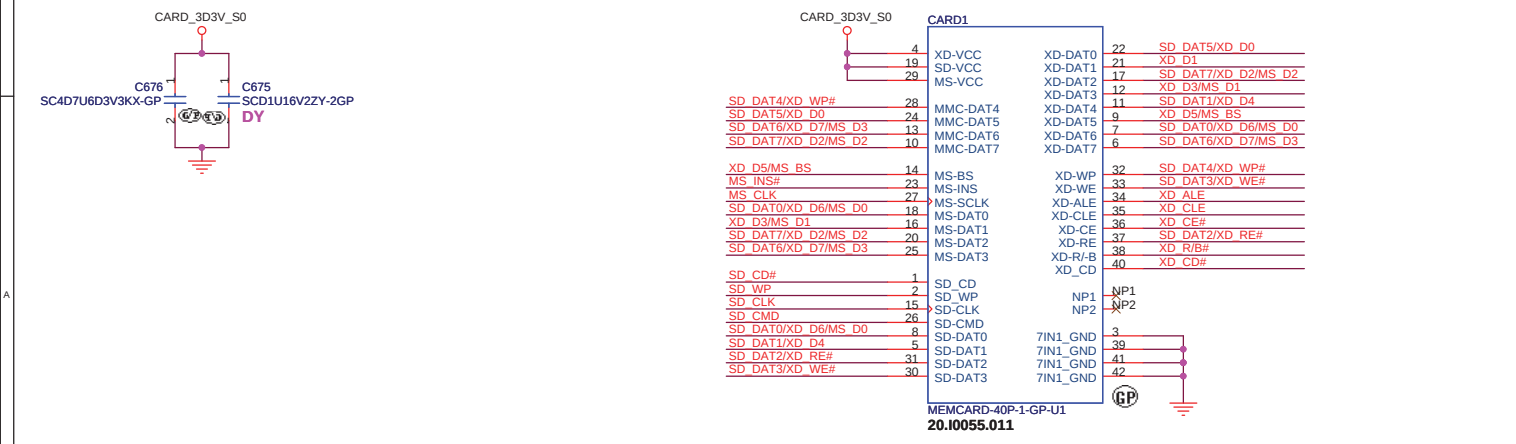
Title: *Finger Printer*

Size	Document Number	Rev
A4	Big Bear 2A	SD

Date: Monday, October 27, 2008 Sheet 31 of 55



7 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader Connector

Size	Document Number	Rev
A3	Big Bear 2A	SD

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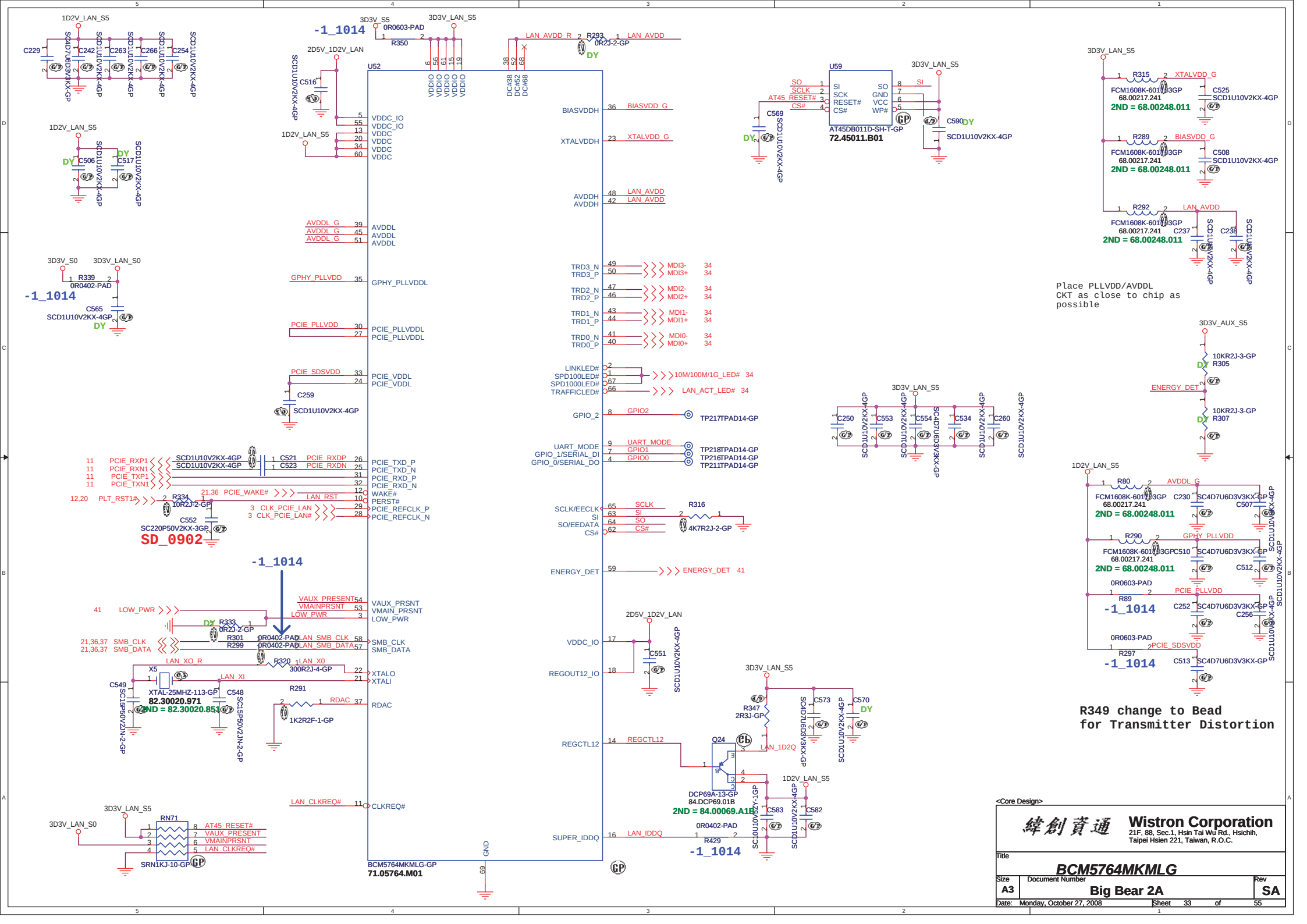
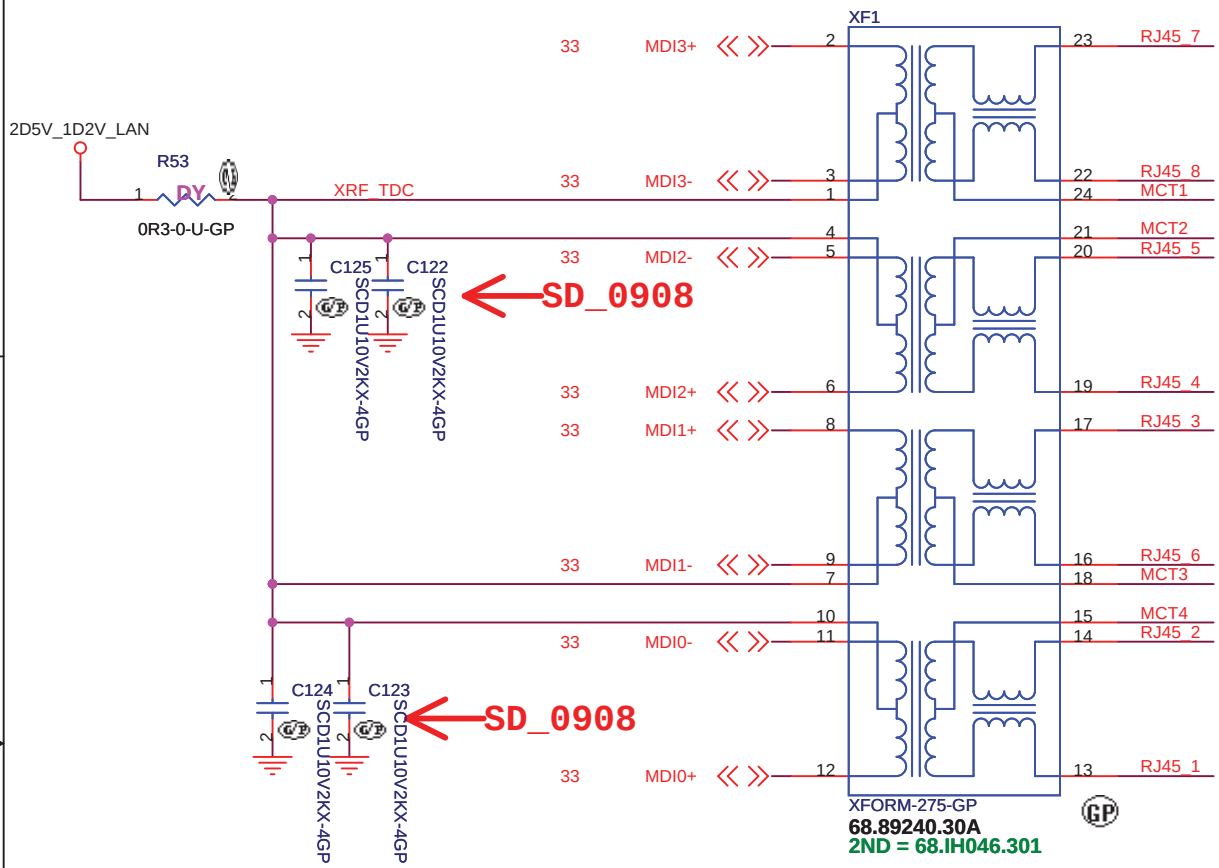
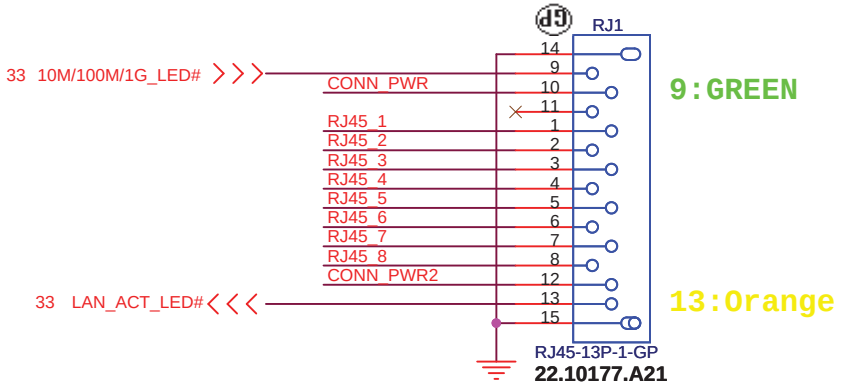

U52
BCM5764MKMLG-GP
71.05764.M01
-1_1014
SD_0902
Place PLLVDD/AVDDL
CKT as close to chip as
possible
R349 change to Bead
for Transmitter Distortion
U59
AT45DB011D-SH-T-GP
72.45011.B01
DCP69A-13-GP
84.DCP69.01B
2ND = 84.00069.A1B
2ND = 82.30020.851
82.30020.971
XTAL-25MHZ-113-GP
SRN1KJ-10-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5764MKMLG
Size
A3
Document Number
Big Bear 2A
Rev
SA
Date: Monday, October 27, 2008
Sheet 33 of 55

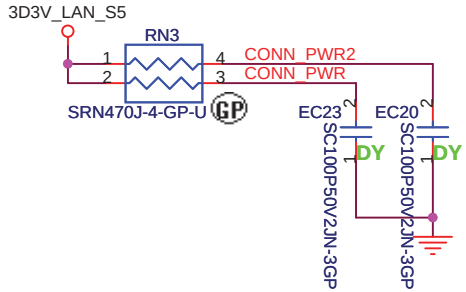
LAN Connector

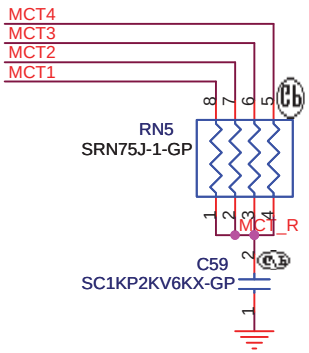




LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

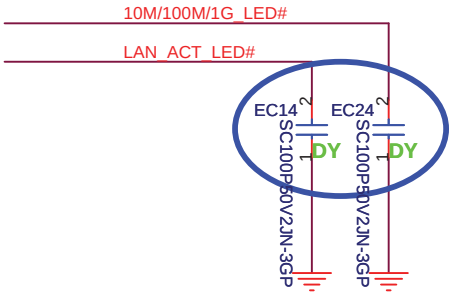
LAN Data: Yellow(B2), when LAN is transfering data.





1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

For EMI Near LAN1 CONN



<Core Design>

緯創資通 **Wistron Corporation**
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Title: **LAN CONN**		
Size: A4	Document Number: Big Bear 2A	Rev: SB
Date: Monday, October 27, 2008	Sheet 34 of 55	

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector

-1_1022

-1_1016

-1_1014

SD_0902

MXM1 DIS
SPD-CONN230A-4-GP-U3
20.F1031.230
2ND = 20.F1384.230

BAS16-1-GP
83.00016.B11
2ND = 83.00016.F11

79.10712.L02
2ND = 79.10712.6JL

2N7002EDW-GP
84.27002.F3F
2ND = 84.DMN66.03F

CH715FPT-GP
83.R0304.B81
2ND = 83.R2004.C8

<Core Design>

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Title: Graphic MXM CONN

Size: A3 | Document Number: Big Bear 2A | Rev: SD

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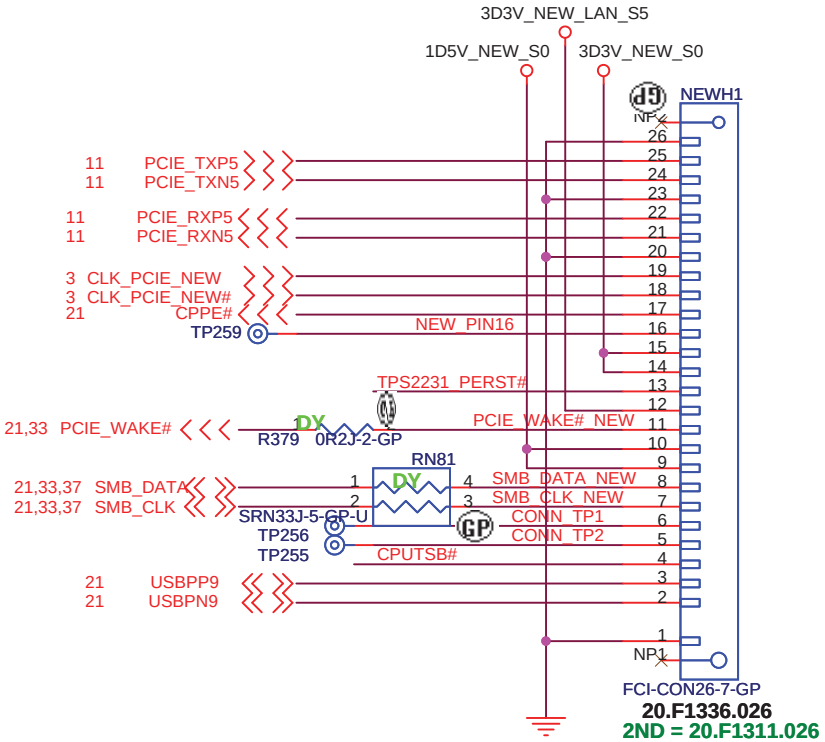
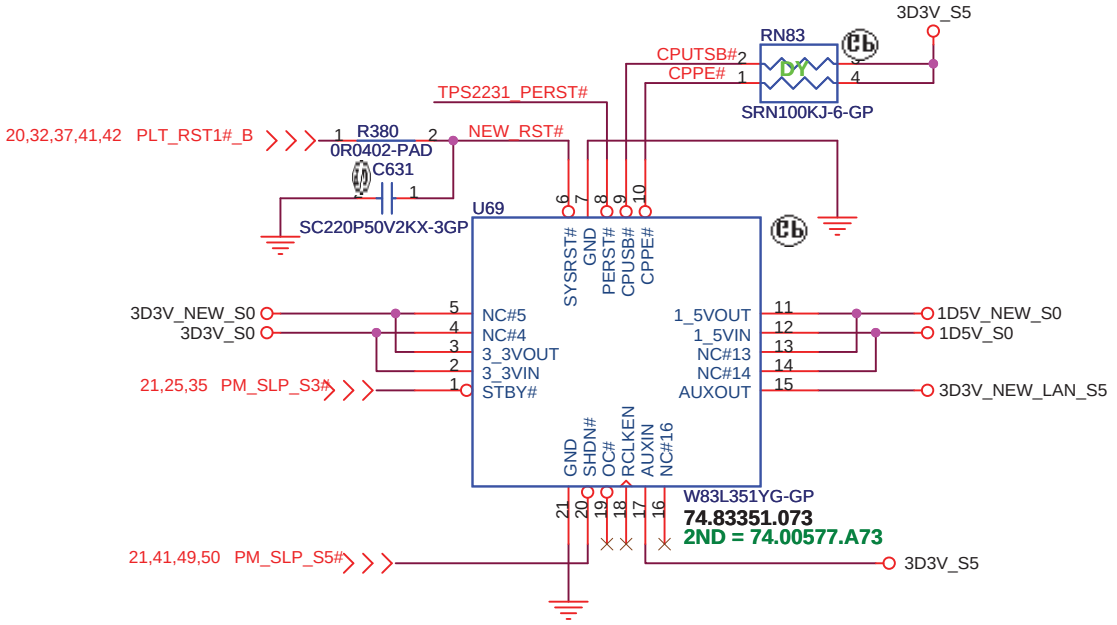
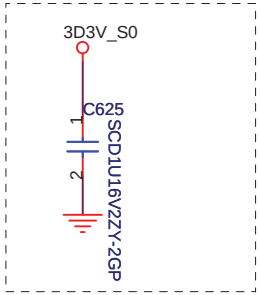
NEWCARD Connector

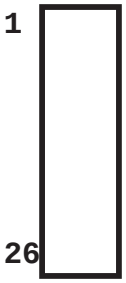


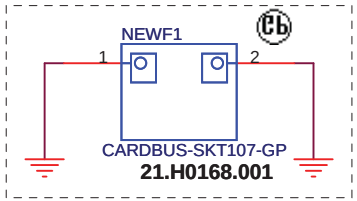


Place them Near to Chip

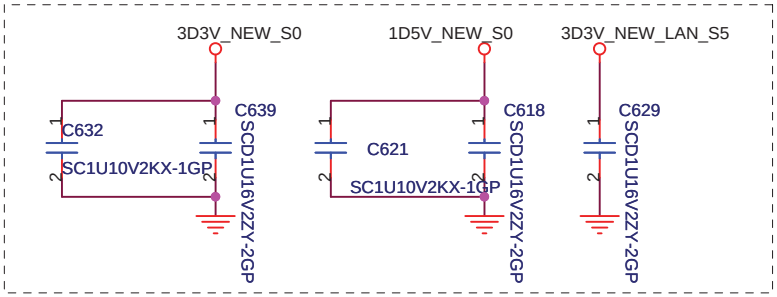


TOP VIEW





Place them Near to Connector



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: NEW CARD		
Size: A4	Document Number: Big Bear 2A	Rev: SC
Date: Monday, October 27, 2008	Sheet 36 of 55	

Mini Card Connector(TV) UPPER SLOT
Mini Card Connector(WLAN) LOWER SLOT

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini Card

Size	Document Number	Rev
A3	Big Bear 2A	SA

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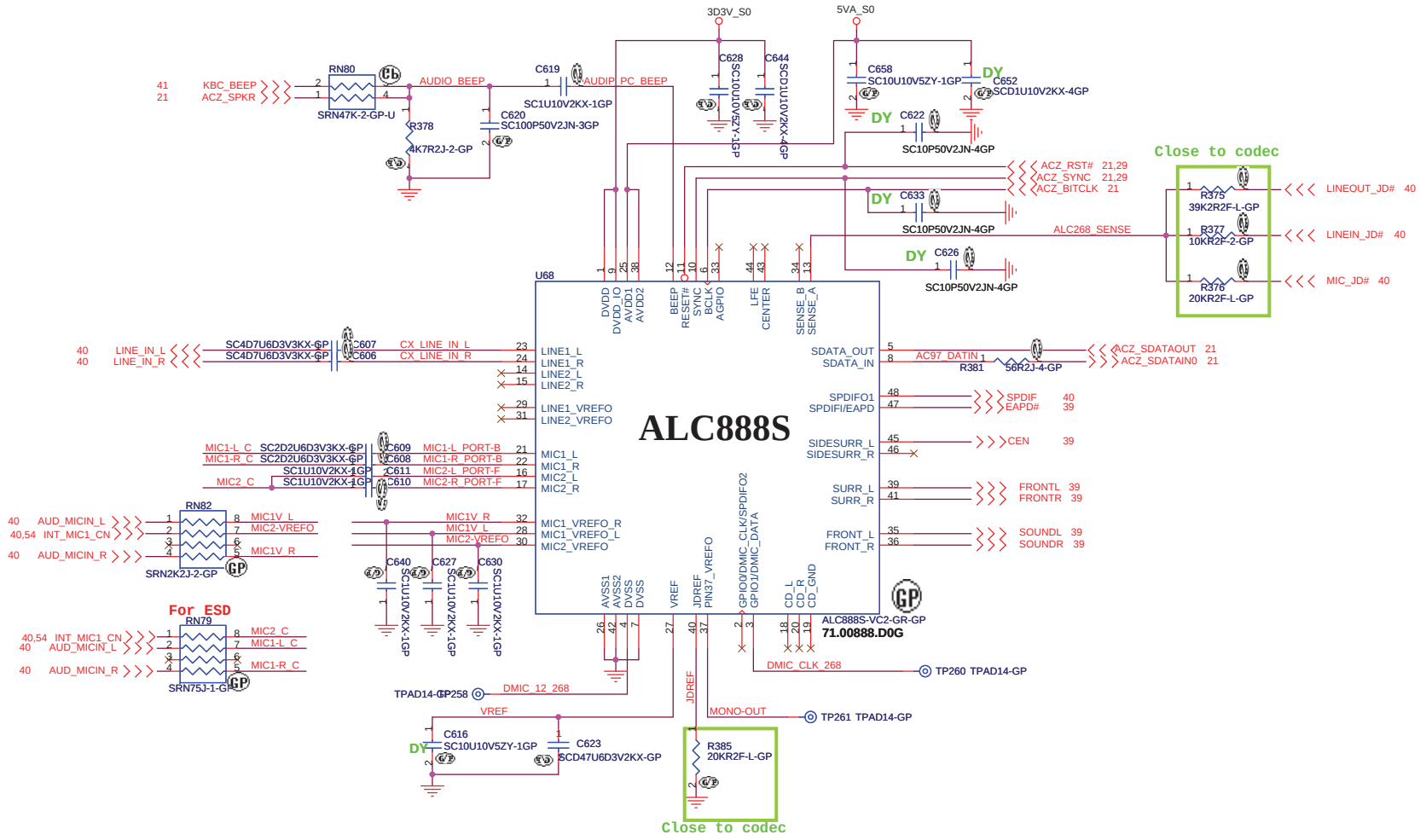

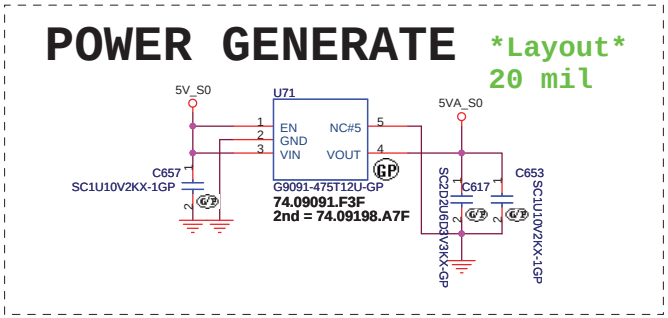

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Azalia codec ALC268***

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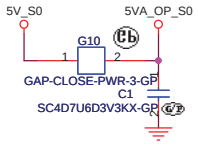
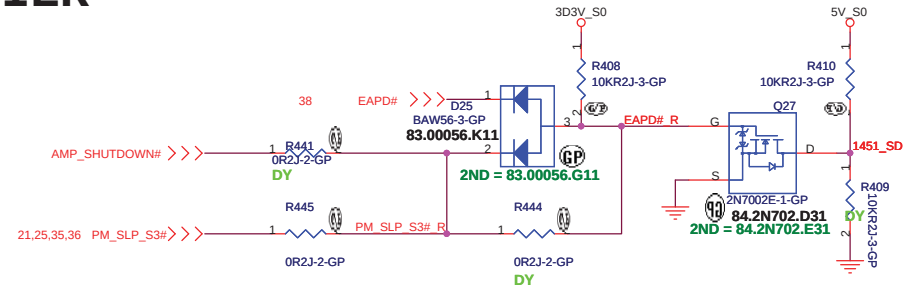
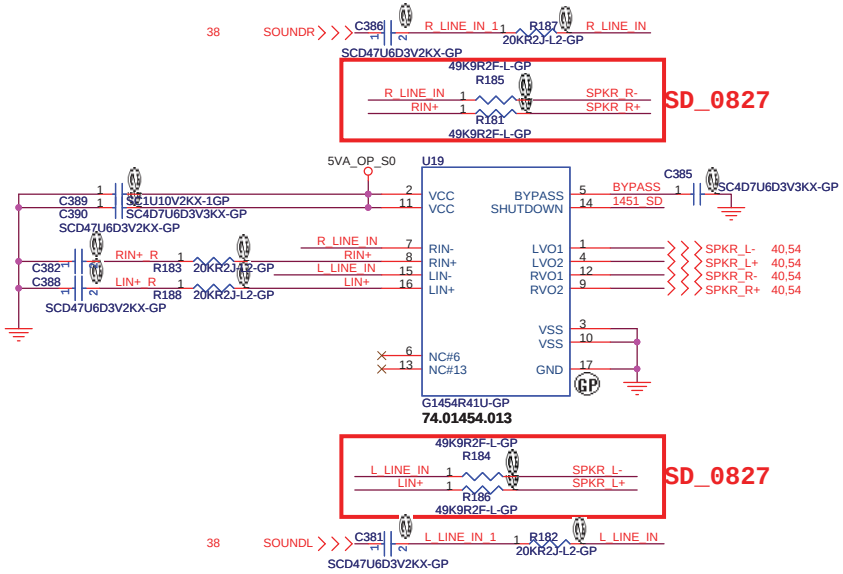
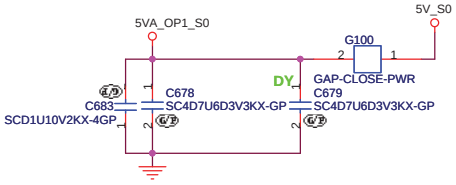
AUDIO OP AMPLIFIER

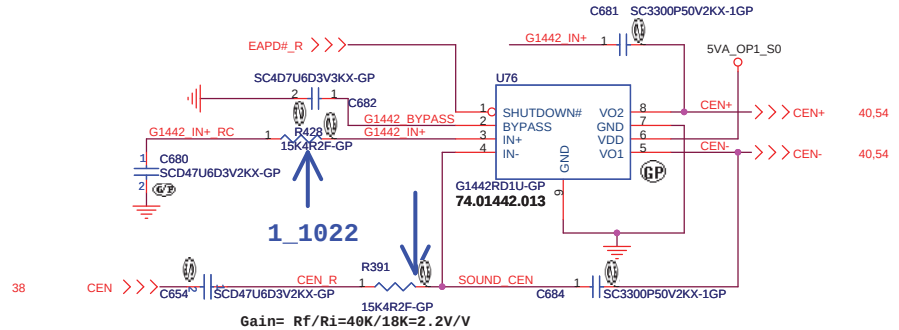






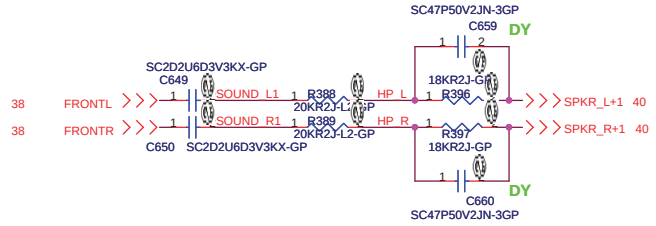
Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W



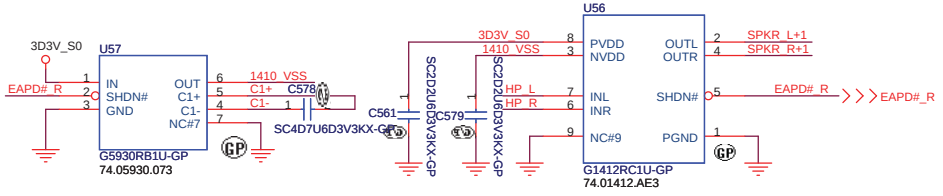


Gain= Rf/Ri=40K/18K=2.2V/V
f(HP)=1/(2 Pi*18K*0.47uf)=18Hz
If VIN= 1.54V Gain=2.2V/V RL=4Ω VO(peak) =3.38V V(rms)=2.390V
Power= 2.390^2/4=1.428W

KBC_MUTE_GPIO8



Gain= Rf/Ri=20K/18K=0.9V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=0.9V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= ?



<Core Design>

緯創資通 **Wistron Corporation**
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Title: AUDIO AMP

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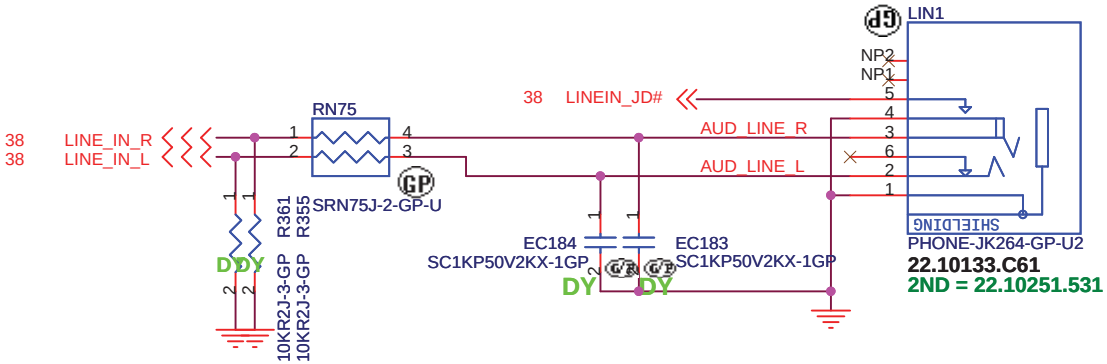
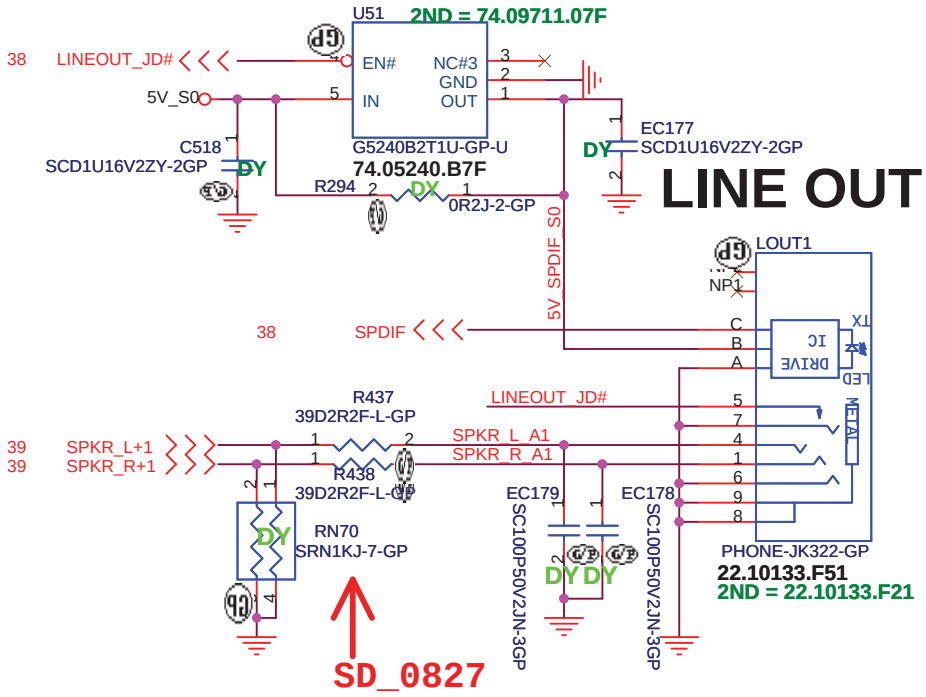
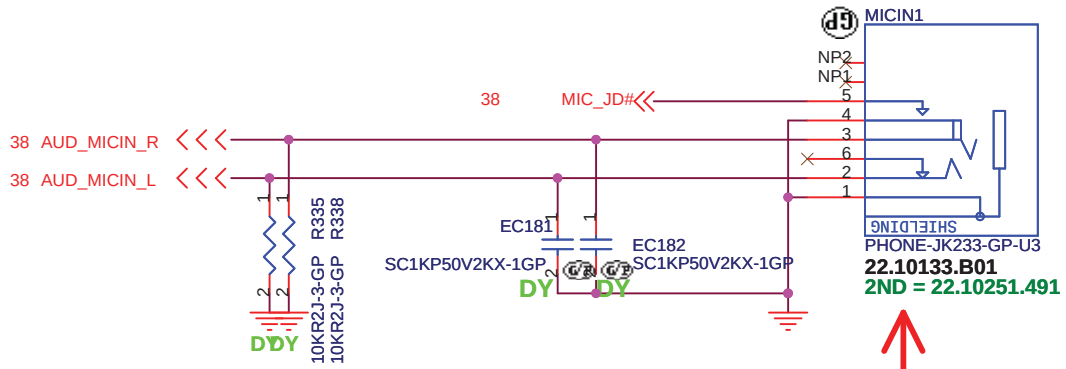
LINE IN



LINE OUT

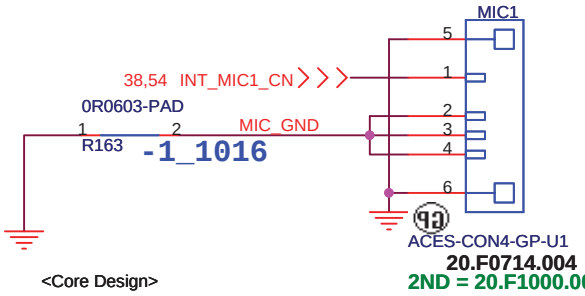


MIC IN



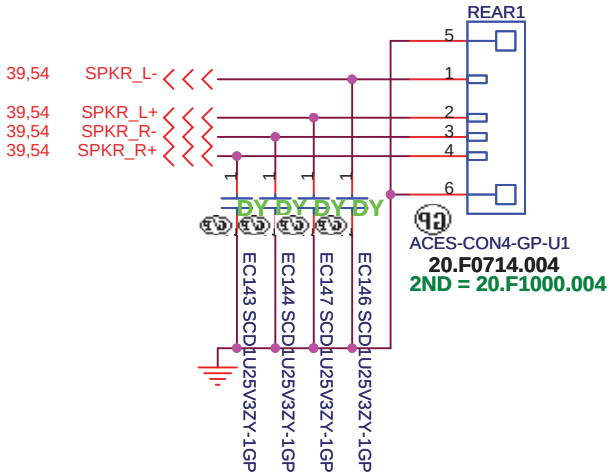
SD_0912 change 2nd

INT. MIC

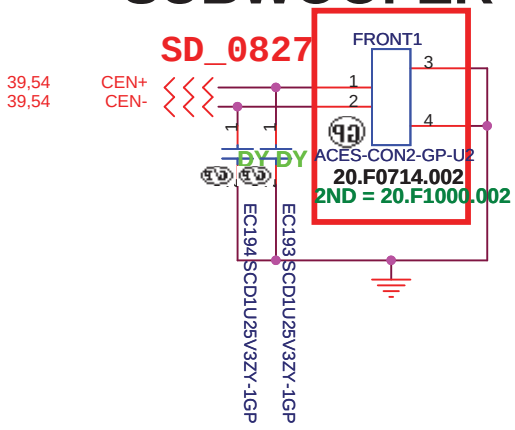


<Core Design>

REAR Speaker



SUBWOOFER



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO JACK*	
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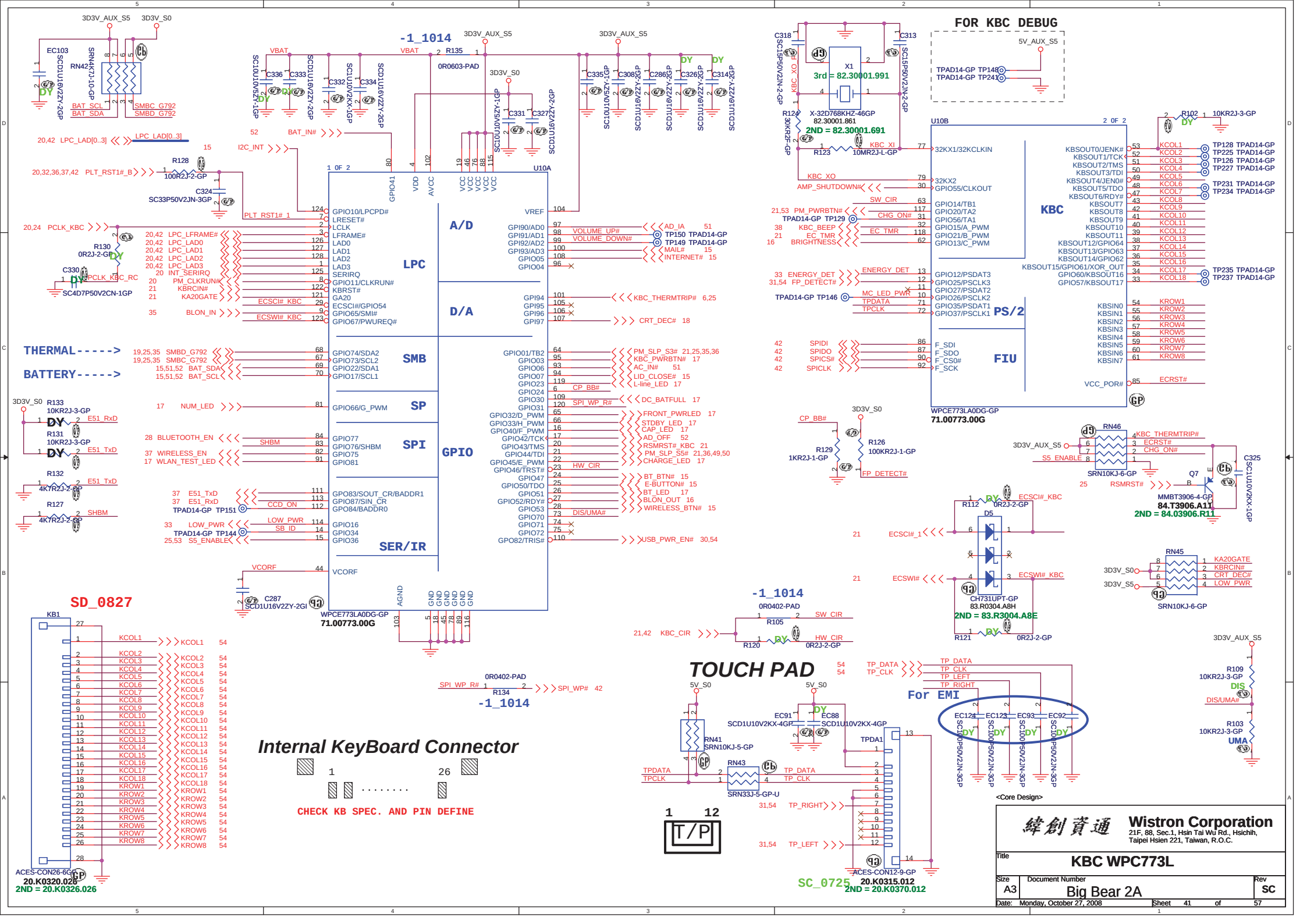
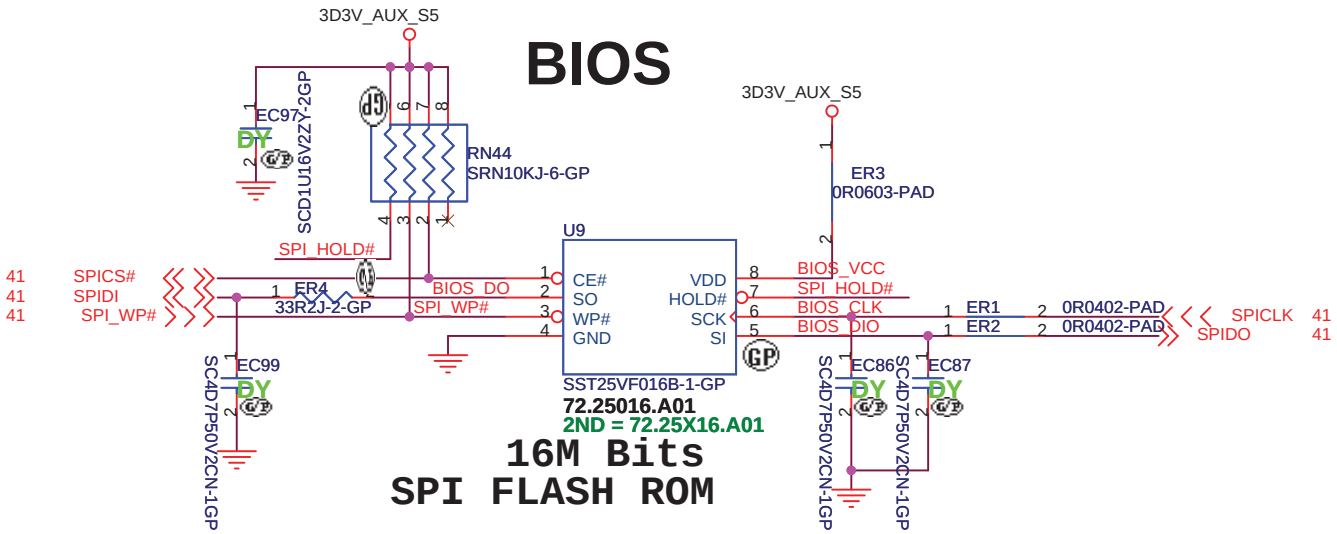
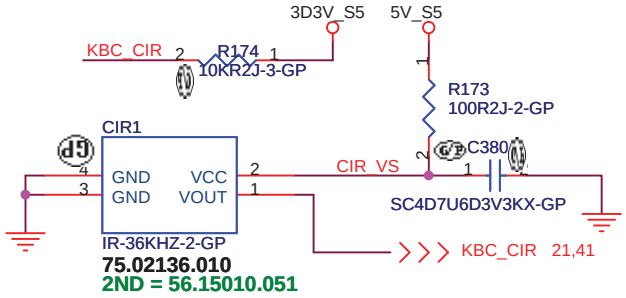

FOR KBC DEBUG
-1_1014
KBC
PS/2
FIU
GPIO
LPC
A/D
D/A
SMB
SP
SPI
SER/IR
THERMAL----->
BATTERY----->
SD_0827
Internal KeyBoard Connector
CHECK KB SPEC. AND PIN DEFINE
TOUCH PAD
For EMI
T/P
WPCE773LA0DG-GP
71.00773.00G
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773L
Big Bear 2A
Monday, October 27, 2008

BIOS



16M Bits
SPI FLASH ROM

CIR Module

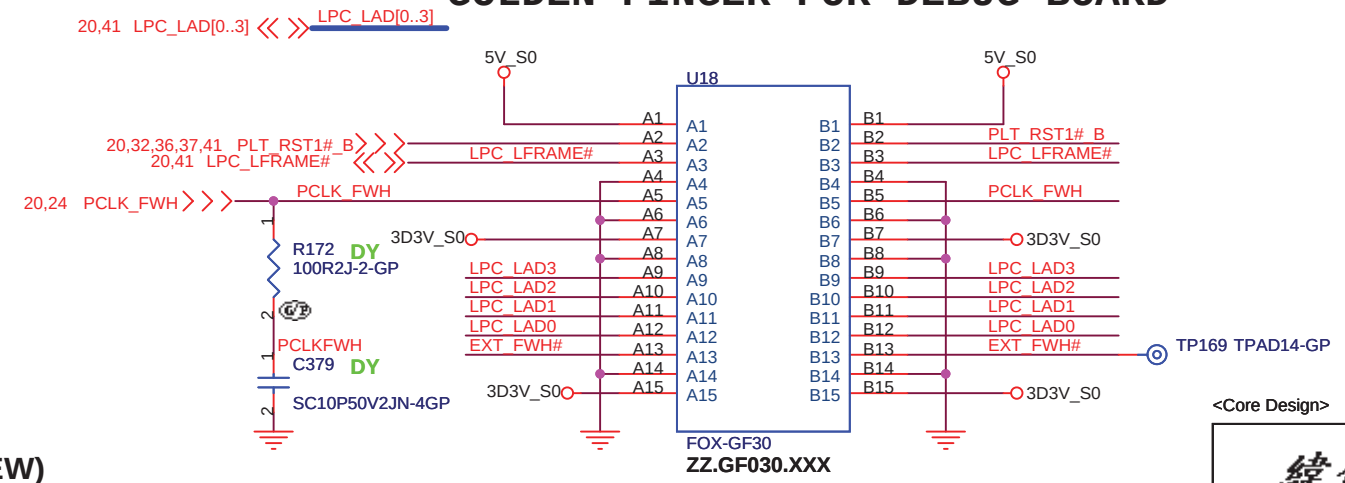


GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)



<Core Design>

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Title	BIOS & CIR	
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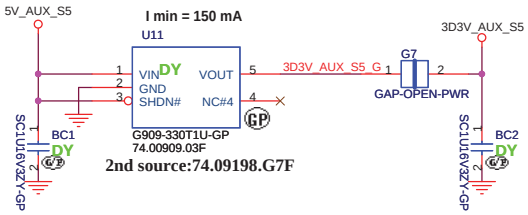
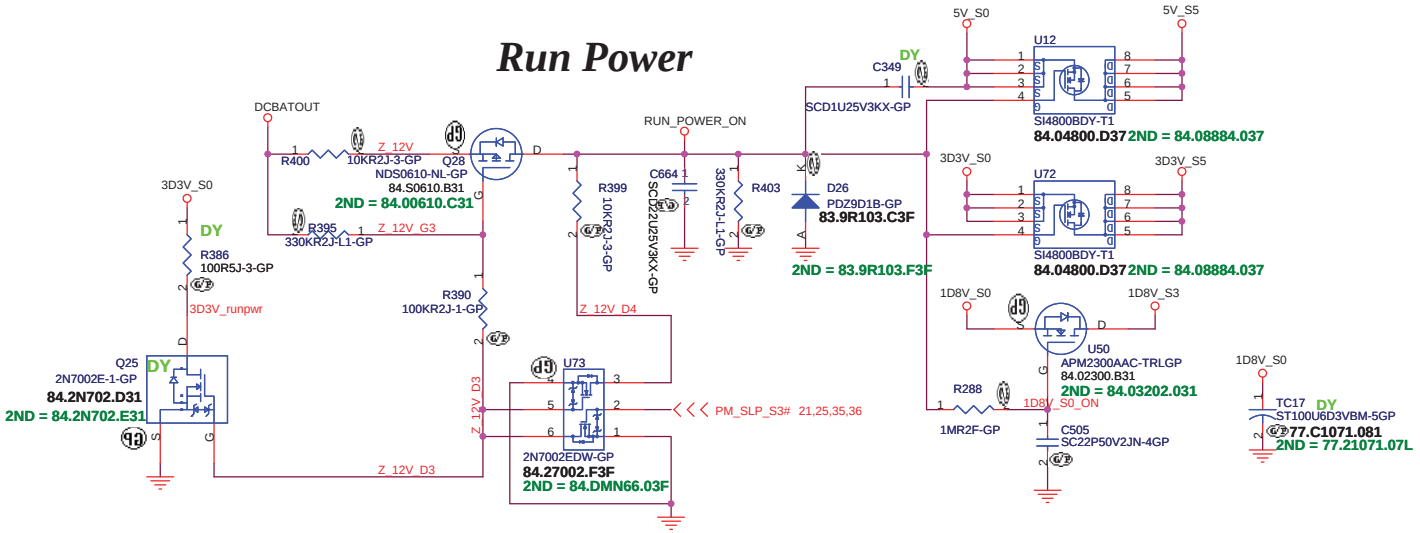
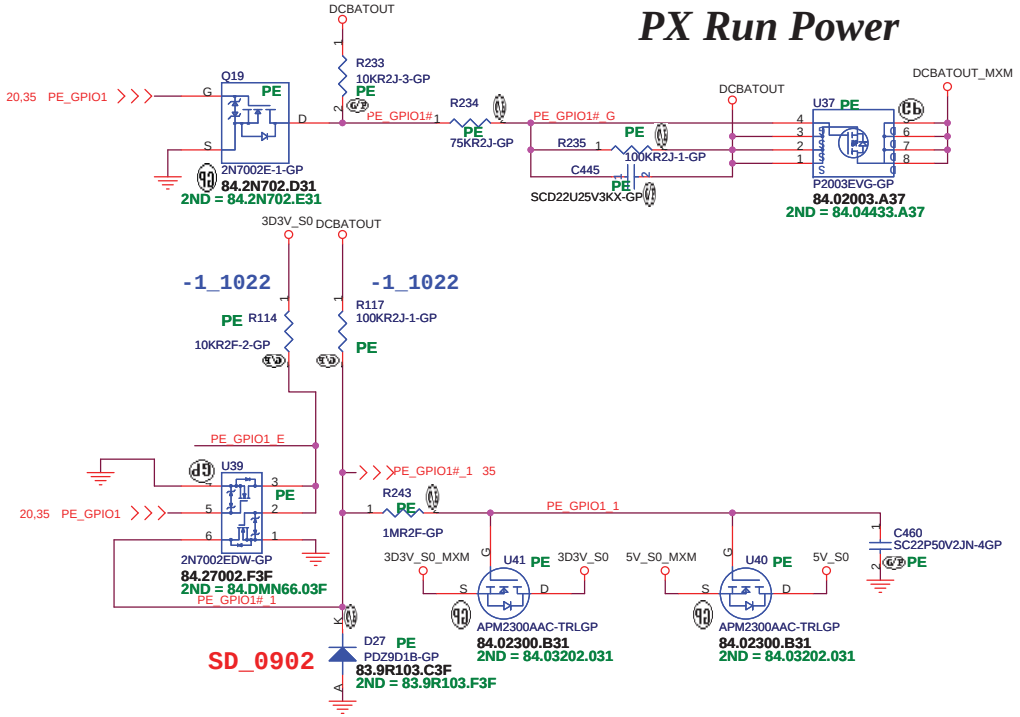
Aux Power 3D3V_AUX_S5



Run Power

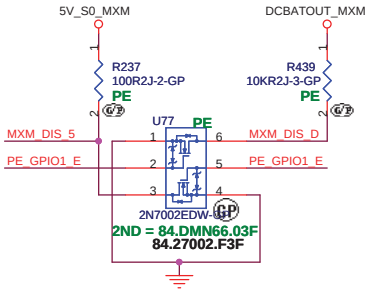


PX Run Power



SD_0902

PX Run Power Discharge circuit



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RUN POWER and 3D3V_AUX_S5		
Size: A3	Document Number: Big Bear 2A	Rev: SD
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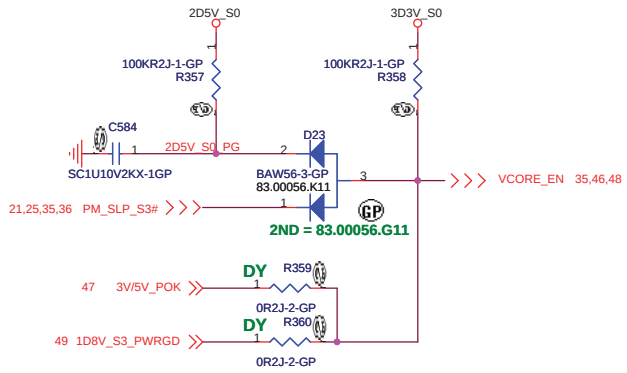
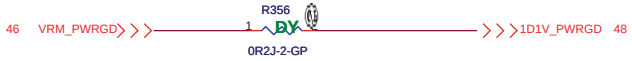
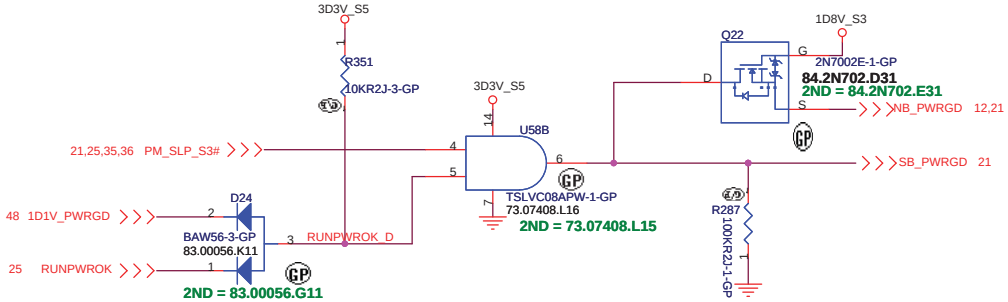


P/H @ 1D8V_S3 PAGE



Reference schematic recommend



<Core Design>

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Title: ***POWER ON LOGIC***

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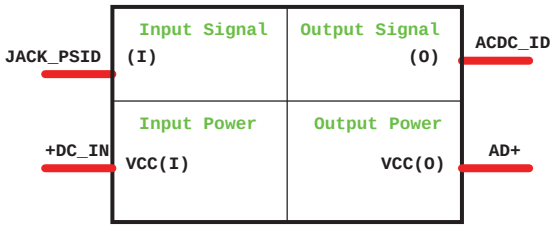
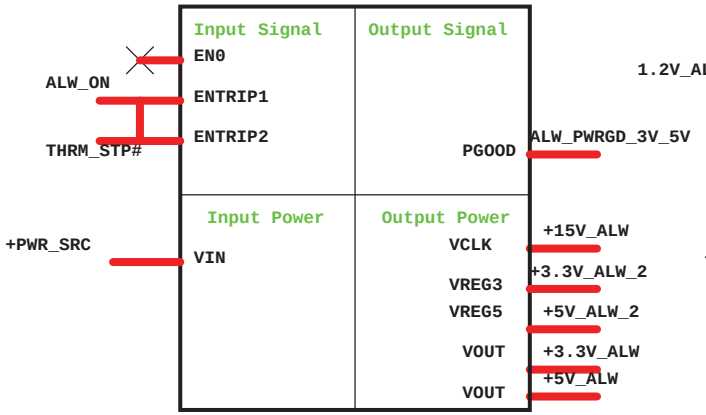
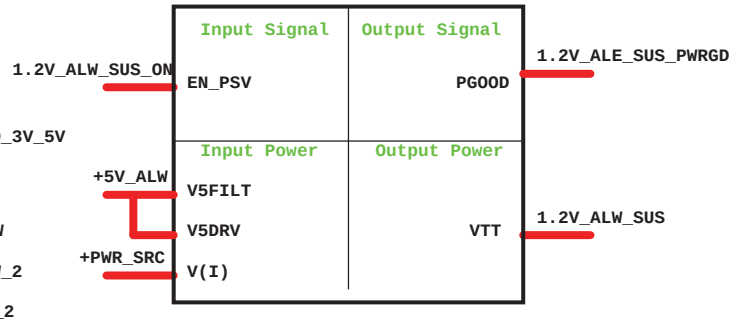
Adapter



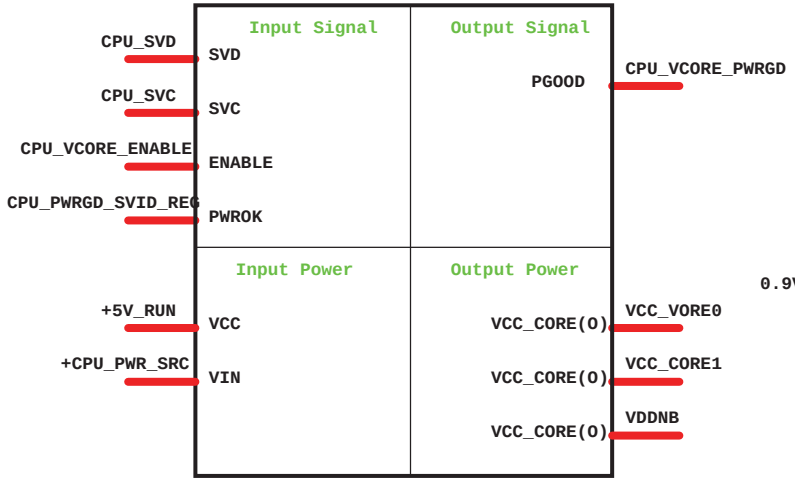
SN0608098



DCDC 1D2V(TPS5117)

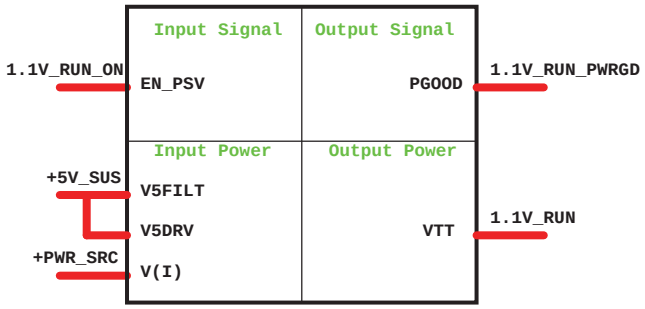


CPU_CORE
ISL6265HRTZ

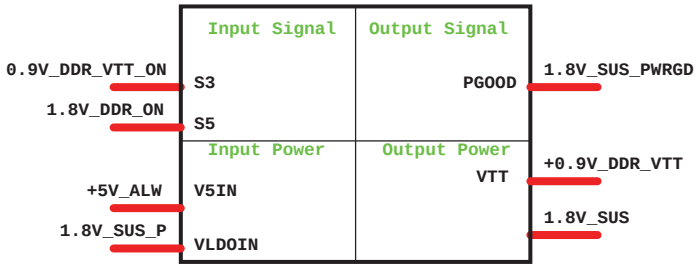


	S3	S5	VDDQ	VTTREF	VTT
S0 S3	1	1	1	1	1
S4 S5	0	0	0	0	0

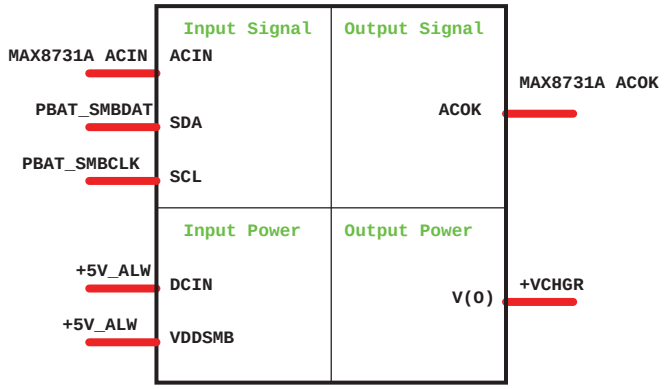
1D1V(TPS5117)



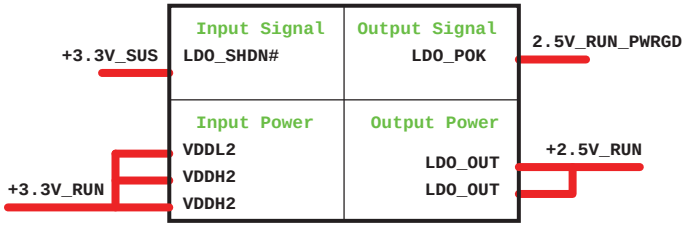
1D8V/0D9V(TPS5116)



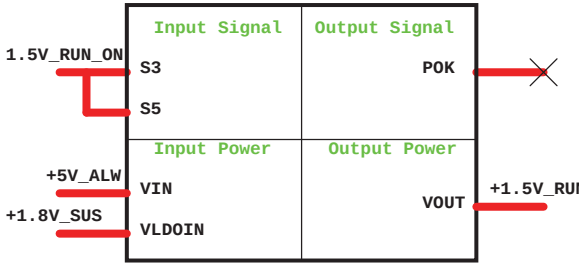
CHARGER BQ24745



2.5V LDO
EMC4002



1.5V_LDO



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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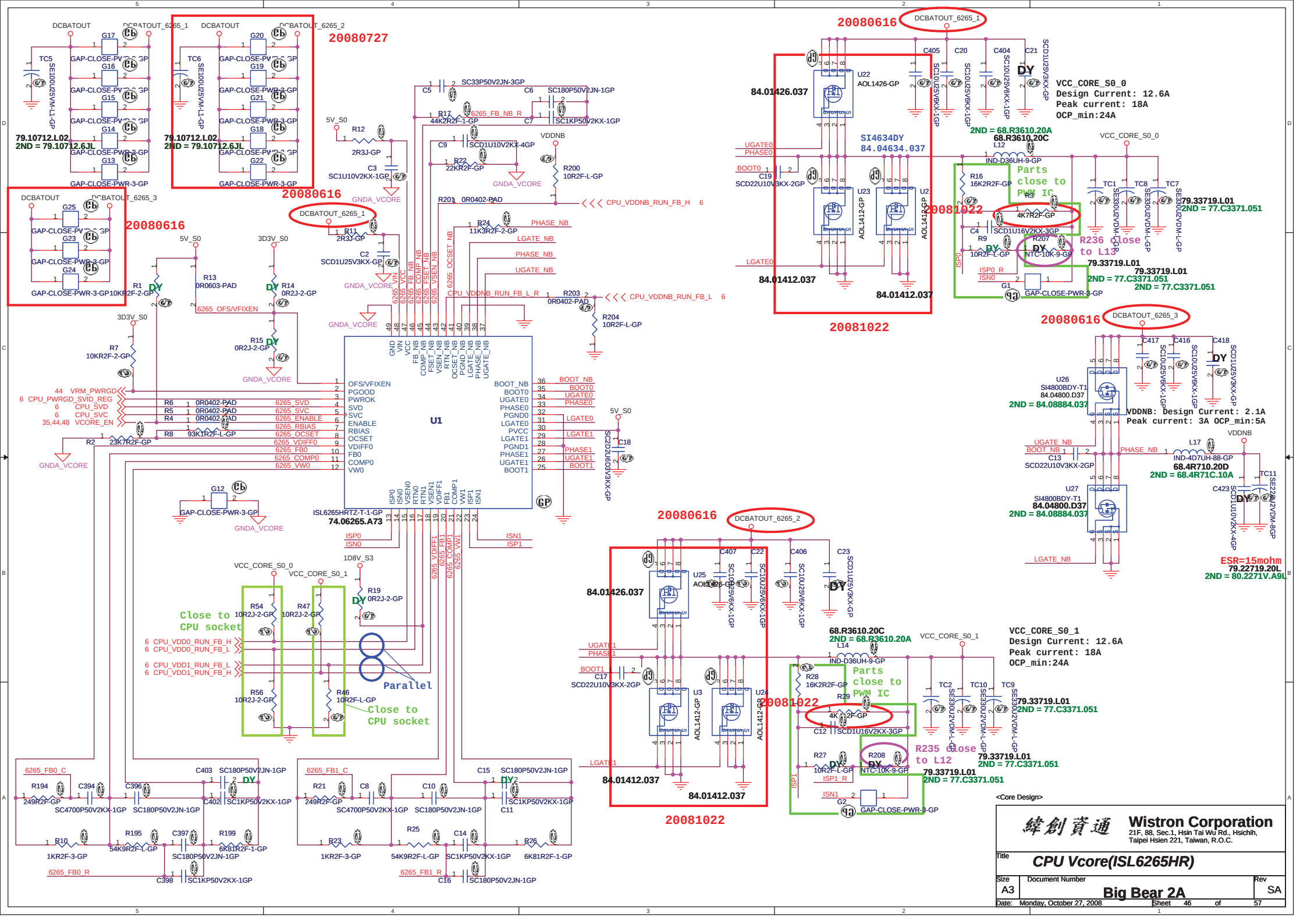
20080727
20080616
20081022
U1
ISL6265HRTZ-T-1-GP
74.06265.A73
U22
AOL1426-GP
84.01426.037
U23
AOL1412-GP
84.01412.037
U2
AOL1412-GP
SI4634DY
84.04634.037
U26
SI4800BDY-T1
84.04800.D37
U27
SI4800BDY-T1
84.04800.D37
U25
AOL1426-GP
U3
AOL1412-GP
U24
AOL1412-GP
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
Parts close to PWM IC
R236 Close to L13
R235 Close to L12
Close to CPU socket
Parallel
ESR=15mohm
79.22719.20L
2ND = 80.2271V.A9L
79.10712.L02
2ND = 79.10712.6JL
79.33719.L01
2ND = 77.C3371.051
68.R3610.20C
2ND = 68.R3610.20A
68.4R710.20D
2ND = 68.4R71C.10A
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
Big Bear 2A
Size A3
Rev SA
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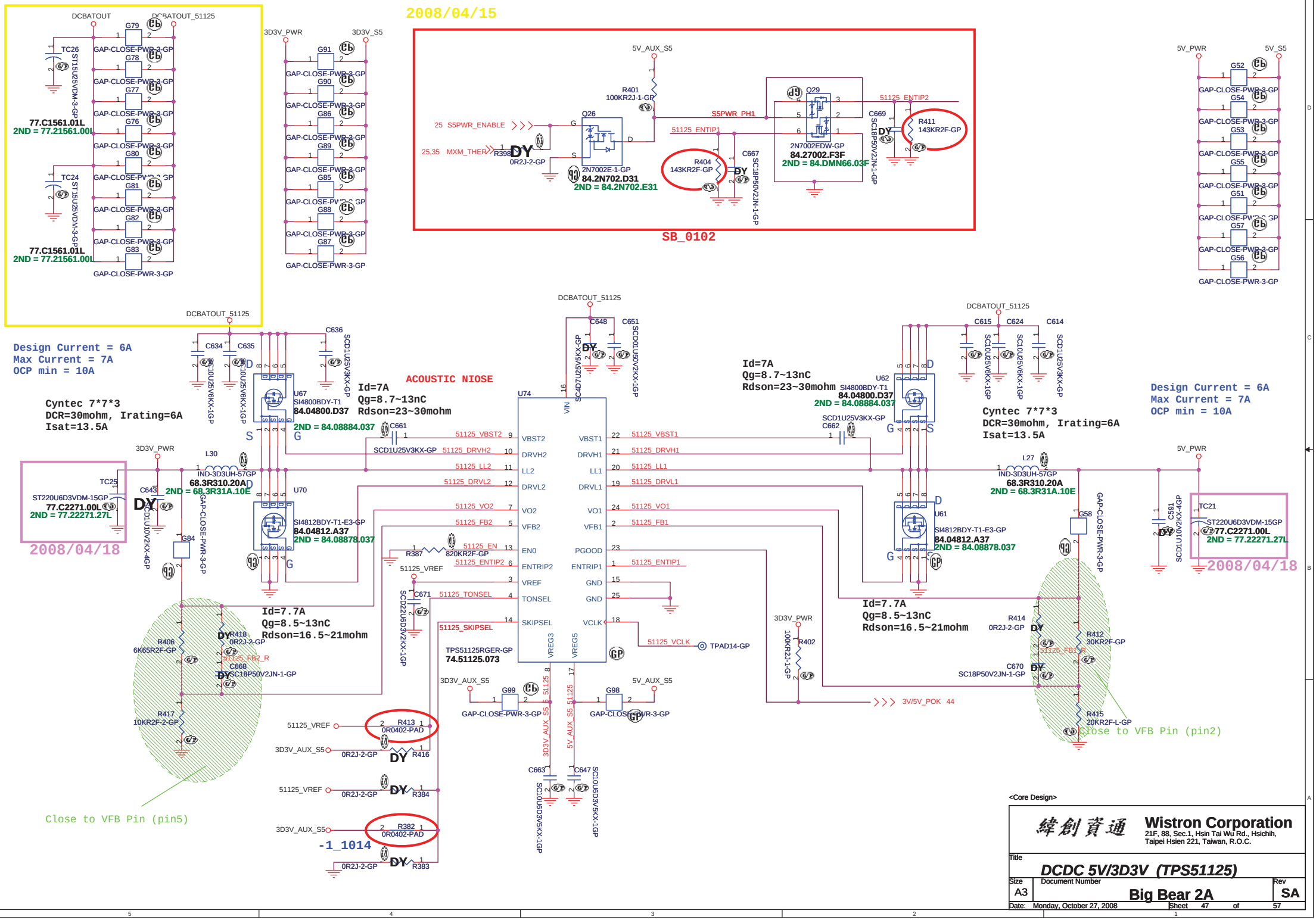
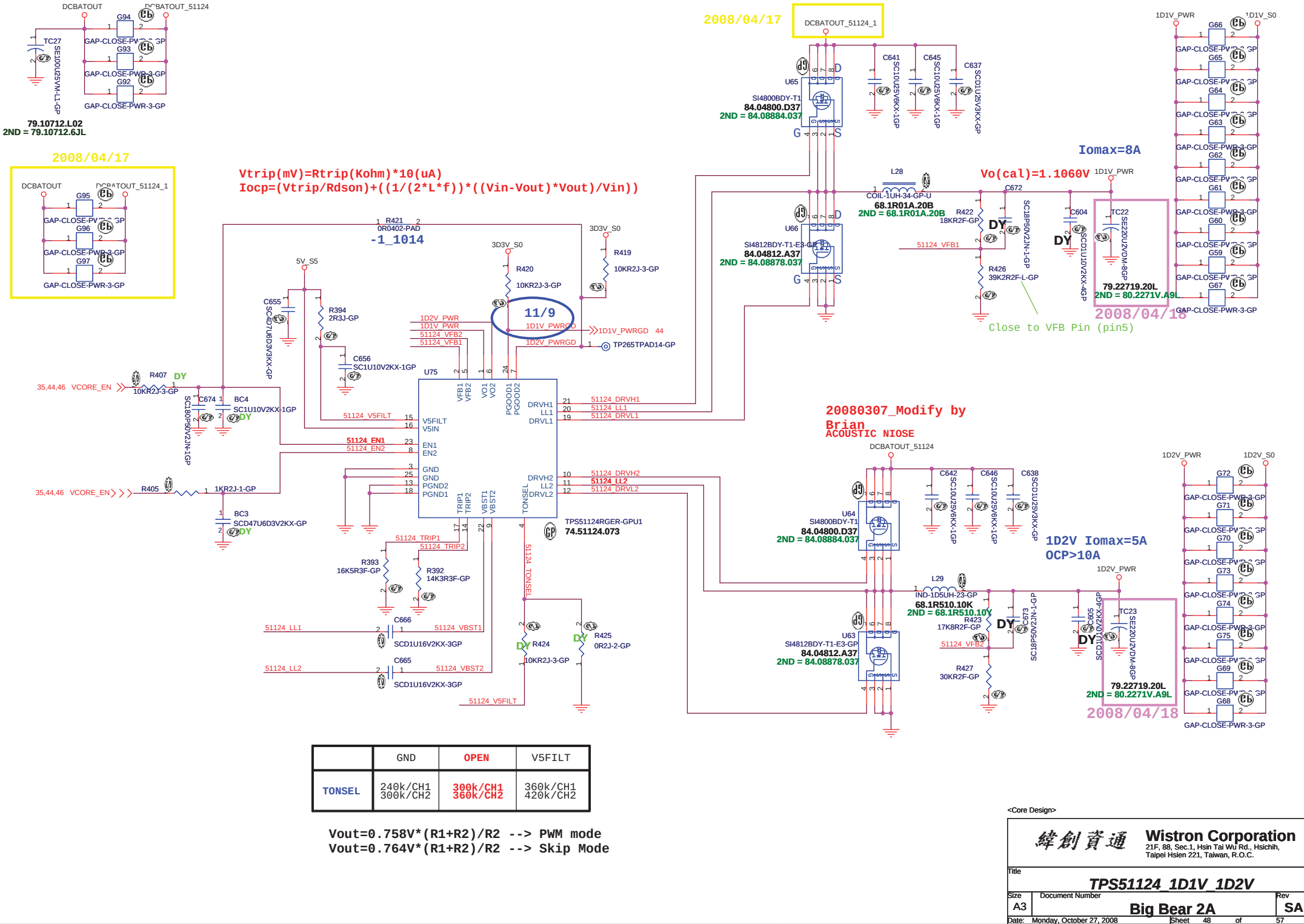

2008/04/15
SB_0102
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
ACOUSTIC NIOSE
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
TPS51125RGER-GP
74.51125.073
2008/04/18
-1_1014
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
Wistron Corporation
DCDC 5V/3D3V (TPS51125)
Big Bear 2A
Monday, October 27, 2008



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

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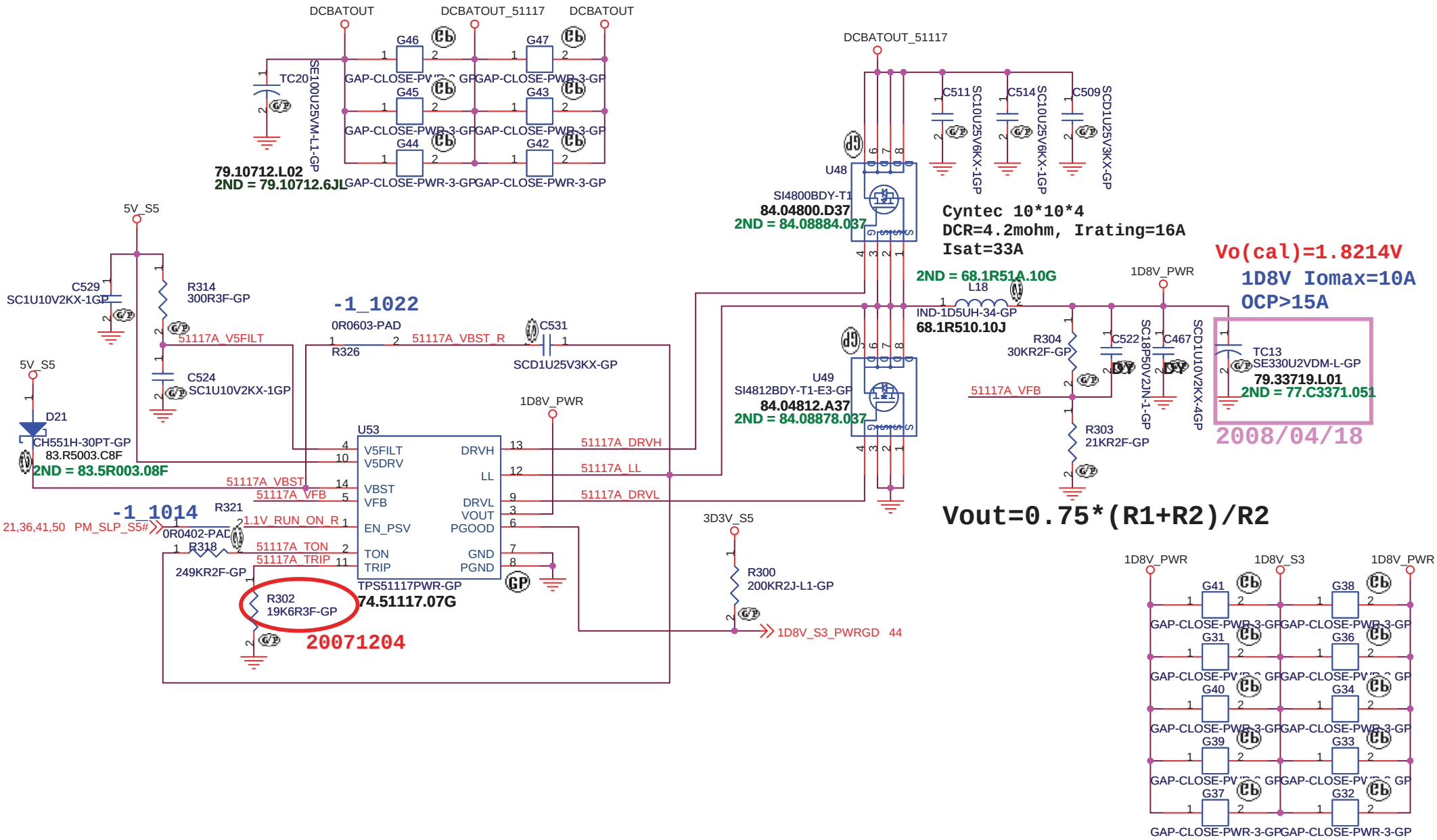

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *1D8V(TPS5117)*

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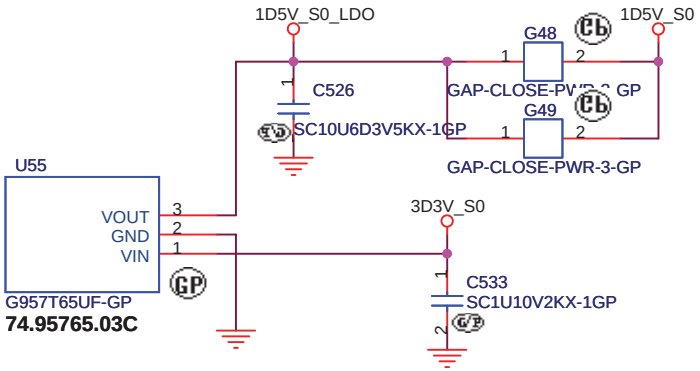
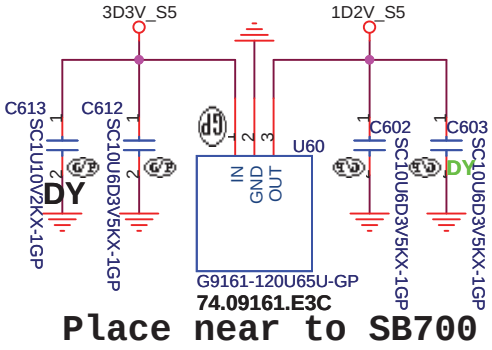
G957

1D5V_S0
Iomax=1A

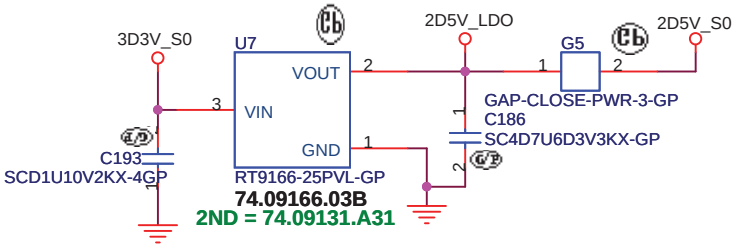


1D2V_S5
Iomax=400mA

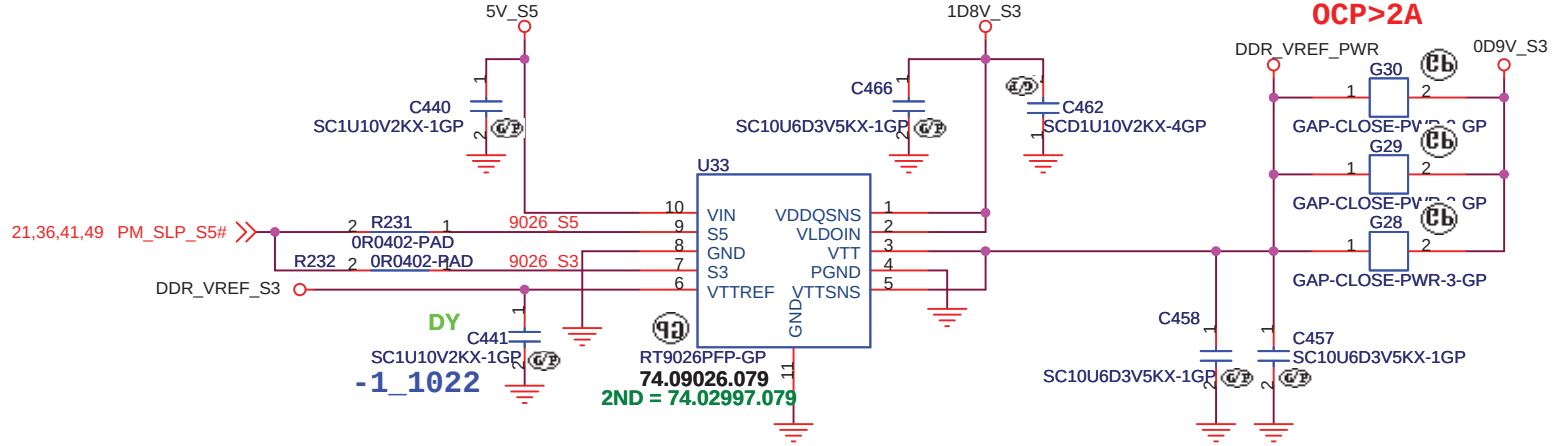


Place near to SB700

2D5V_S0
Iomax=0.3A 2D5V/300mA



Iomax=1A
OCP>2A



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *0D9V&2D5V&1D25V&1D5V*		
Size: A4	Document Number: Big Bear 2A	Rev: SB
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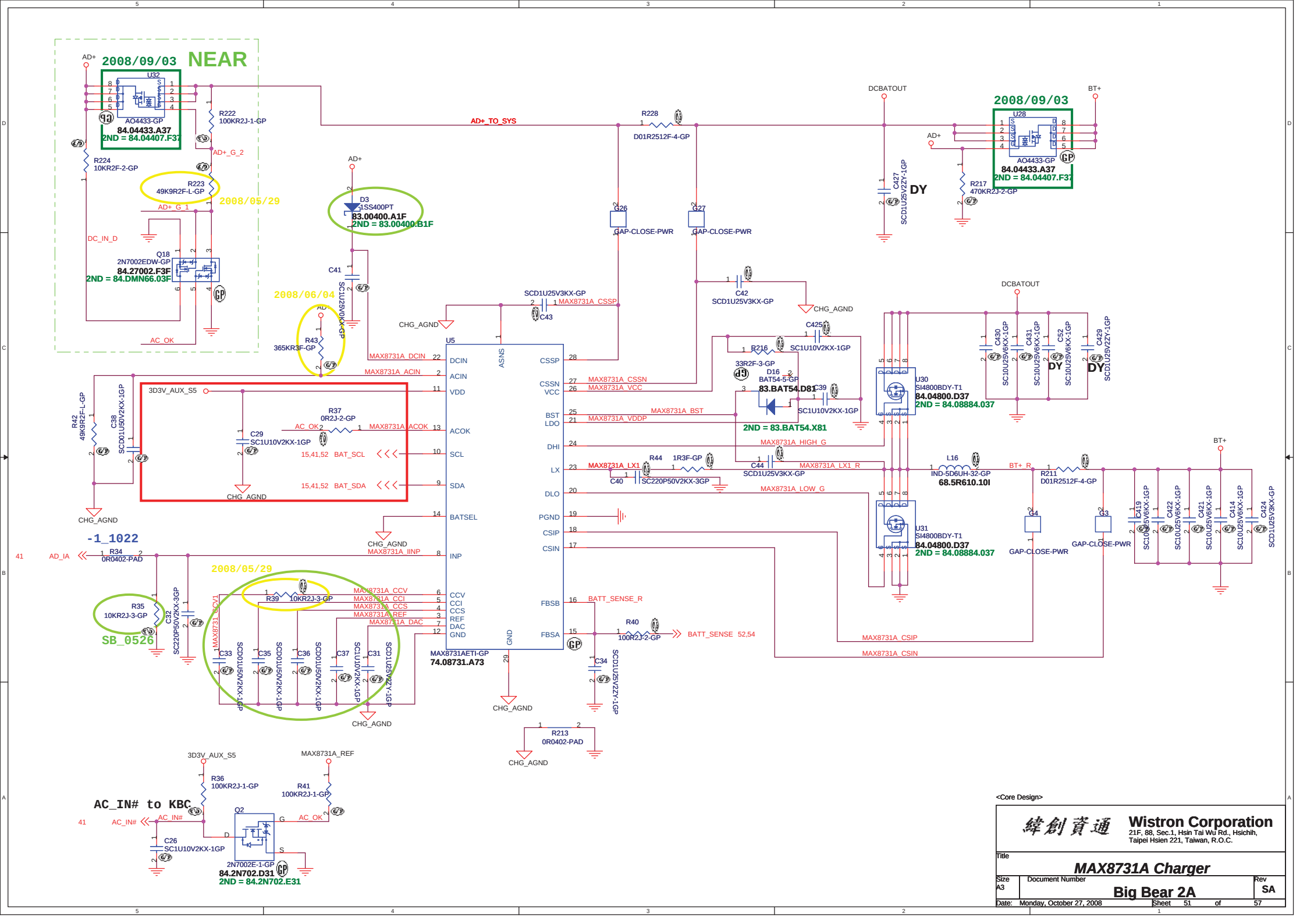
2008/09/03 NEAR
U32
AO4433-GP
84.04433.A37
2ND = 84.04407.F37
R222 100KR2J-1-GP
AD+_G_2
R224 10KR2F-2-GP
R223 49K9R2F-L-GP
2008/05/29
AD+_G_1
DC_IN_D
Q18
2N7002EDW-GP
84.27002.F3F
2ND = 84.DMN66.03F
AC_OK
AD+
AD+_TO_SYS
R228 D01R2512F-4-GP
DCBATOUT
BT+
2008/09/03
U28
AO4433-GP
84.04433.A37
2ND = 84.04407.F37
R217 470KR2J-2-GP
C427 SCD1U25V2ZY-1GP
DY
D3
1SS400PT
83.00400.A1F
2ND = 83.00400.B1F
2008/06/04
C41 SCD1U25V3KX-GP
R43 365KR3F-GP
G26 GAP-CLOSE-PWR
G27 GAP-CLOSE-PWR
C42 SCD1U25V3KX-GP
C43 SCD1U25V3KX-GP
MAX8731A_CSSP
CHG_AGND
U5
MAX8731AETI-GP
74.08731.A73
DCIN
ACIN
VDD
ACOK
SCL
SDA
BATSEL
INP
CCV
CCI
CCS
REF
DAC
GND
CSSP
CSSN
VCC
BST
LDO
DHI
LX
DLO
PGND
CSIP
CSIN
FBSB
FBSA
ASNS
MAX8731A_DCIN
MAX8731A_ACIN
MAX8731A_CSSN
MAX8731A_VCC
MAX8731A_VDDP
MAX8731A_BST
MAX8731A_HIGH_G
MAX8731A_LX1
MAX8731A_LOW_G
MAX8731A_IINP
MAX8731A_CCV
MAX8731A_CCI
MAX8731A_CCS
MAX8731A_REF
MAX8731A_DAC
BATT_SENSE_R
3D3V_AUX_S5
R37 0R2J-2-GP
AC_OK
MAX8731A_ACOK
C29 SC1U10V2KX-1GP
15,41,52 BAT_SCL
15,41,52 BAT_SDA
R42 49K9R2F-L-GP
C38 SCD01U50V2KX-1GP
R216 33R2F-3-GP
C425 SC1U10V2KX-1GP
D16 BAT54-5-GP
83.BAT54.D81
2ND = 83.BAT54.X81
C39 SC1U10V2KX-1GP
R44 1R3F-GP
C44 SCD1U25V3KX-GP
C40 SC220P50V2KX-3GP
L16 IND-5D6UH-32-GP
68.5R610.10I
R211 D01R2512F-4-GP
BT+_R
U30
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
U31
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
C430 SC10U25V6KX-1GP
C431 SC10U25V6KX-1GP
C52 SC10U25V6KX-1GP
C429 SCD1U25V2ZY-1GP
C419 SC10U25V6KX-1GP
C422 SC10U25V6KX-1GP
C421 SC10U25V6KX-1GP
C414 SC10U25V6KX-1GP
C424 SCD1U25V3KX-GP
G4 GAP-CLOSE-PWR
G3 GAP-CLOSE-PWR
-1_1022
AD_IA
R34 0R0402-PAD
R35 10KR2J-3-GP
SB_0526
C32 SC220P50V2KX-3GP
R39 10KR2J-3-GP
C33 C35 C36 C37 C31
SCD01U50V2KX-1GP
SCD1U25V2ZY-1GP
R40 100R2J-2-GP
BATT_SENSE 52,54
C34 SCD1U25V2ZY-1GP
R213 0R0402-PAD
MAX8731A_CSIP
MAX8731A_CSIN
AC_IN# to KBC
3D3V_AUX_S5
MAX8731A_REF
R36 100KR2J-1-GP
R41 100KR2J-1-GP
Q2
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
C26 SC1U10V2KX-1GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MAX8731A Charger
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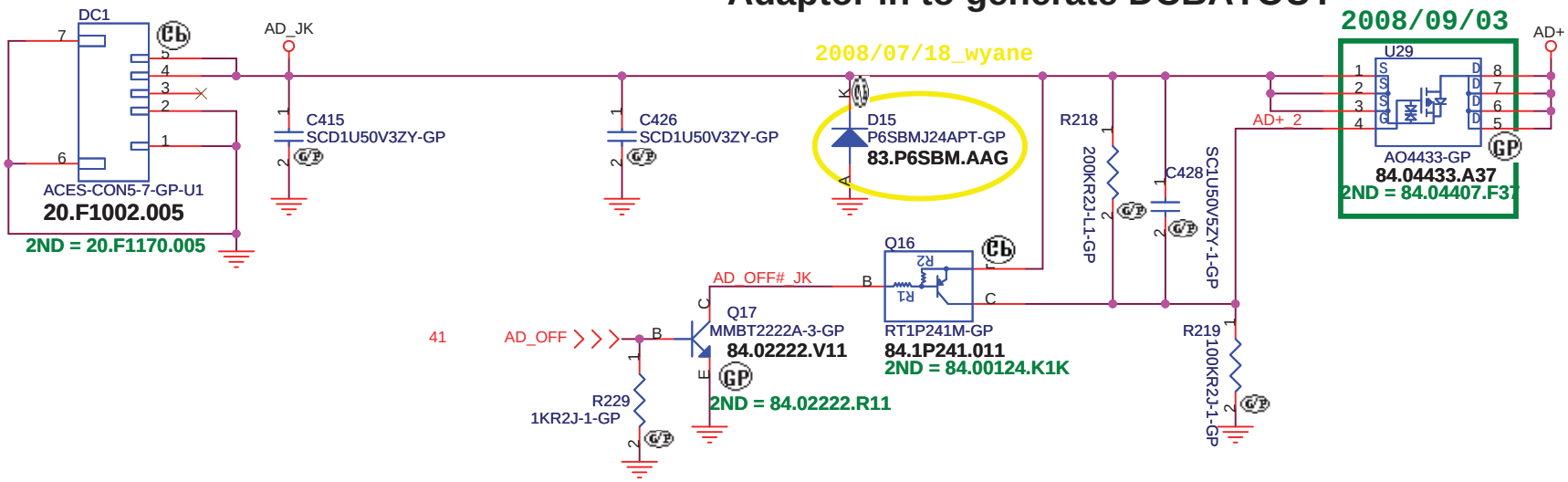
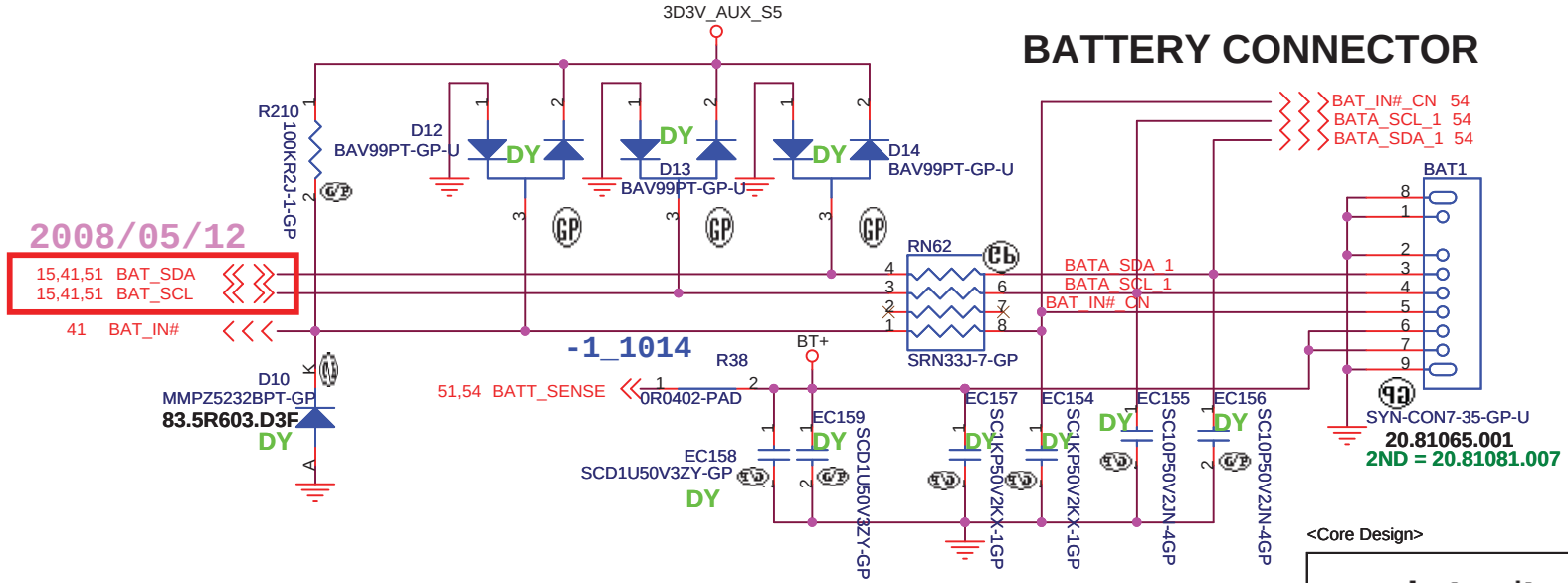
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AD/BATT CONN***

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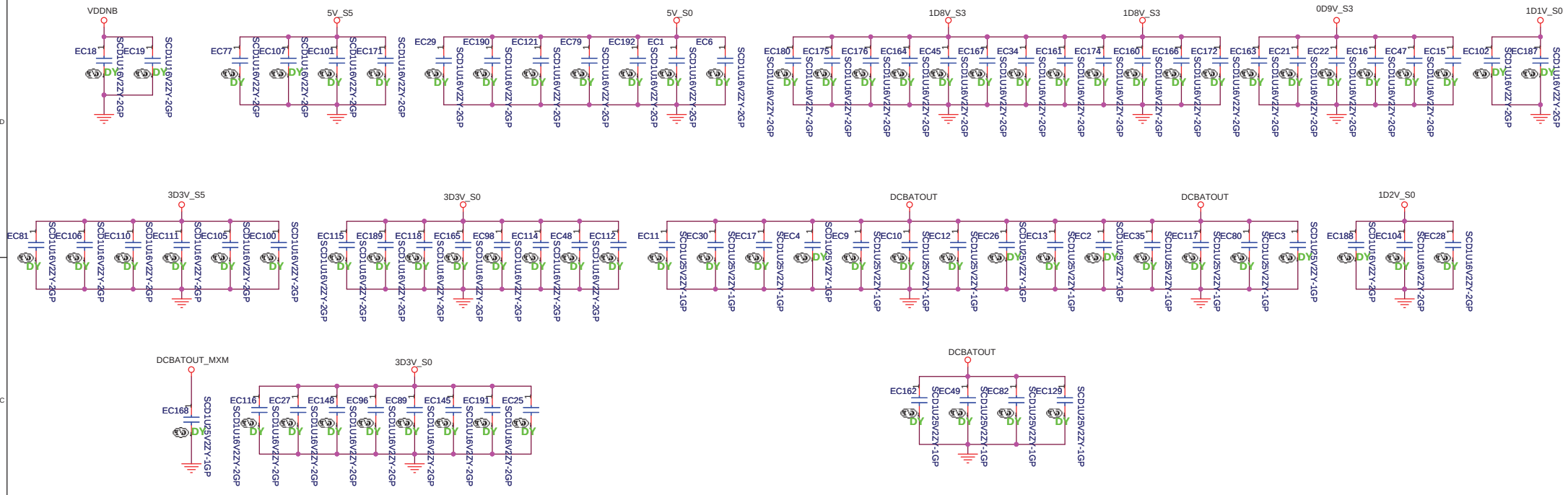

SPRING ON BOTTOM

DIMM

GND3 SPRING-62-GP 34.39S07.003 DY

GND1 SPRING-62-GP 34.39S07.003 DY

MXM

S1 SPRING-37-GP-U 34.15F09.001 DY

S2 SPRING-37-GP-U 34.15F09.001 DY

S3 SPRING-37-GP-U 34.15F09.001 DY

SPRING ON TOP

SD_0903

Touch Pad

H30 SPRING-57-GP 34.42T14.002

HDMI

SW2 SPRING-15-GP DY

SB-U15

SW3 SPRING-7 DY

SW4 SPRING-7 DY

SW5 SPRING-7 DY

USB

SW6 SPRING-6 DY

SW7 SPRING-6 DY

Jack

SW8 SPRING-15-GP DY

RN24

SW9 SPRING-7 DY

STAND OFF ON BOTTOM

CPU & NB

H31 HOLE 34.42Y01.011

H32 HOLE 34.42Y01.011

H33 HOLE 34.42Y01.011

H34 HOLE 34.42Y01.011

Mini Card

H19 HOLE 34.4Z402.001

H20 HOLE 34.4Z402.001

MXM

H14 HOLE DIS 34.4Z401.001

H17 HOLE DIS 34.4Z401.001

STAND OFF ON TOP

MDC

H21 HOLE 34.42Y01.011

H22 HOLE 34.42Y01.011

H1 PAD-1P-3-GP

H2 PAD-1P-3-GP

H3 PAD-1P-3-GP

H4 PAD-1P-3-GP

H5 PAD-1P-3-GP

H6 PAD-1P-3-GP

H7 PAD-1P-3-GP

H8 PAD-1P-3-GP

H9 PAD-1P-3-GP

H10 PAD-1P-3-GP

H13 PAD-1P-3-GP

H18 PAD-1P-3-GP

PAD1 PAD-1P-4-GP

H39 PAD-1P-3-GP

H40 PAD-1P-3-GP

Check test point

3D3V_S0	TP263 TPAD14-GP
3D3V_AUX_S5	TP226 TPAD14-GP
3D3V_S5	TP262 TPAD14-GP
5V_S5	TP246 TPAD14-GP
21,41 PM_PWRBTN#	TP253 TPAD14-GP
6,20 CPU_PWRGD	TP141 TPAD14-GP
25,41 S5_ENABLE	TP143 TPAD14-GP
6,20 CPU_LDT_RST#	TP238 TPAD14-GP

Test Point放在Dimm Door打開可量測處

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size: A3 | Document Number: Big Bear 2A | Rev: SD

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***EMI/Spring/Boss***

Size	Document Number	Rev
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