

Compal Confidential

Model Name : P7YE0/P7YH0/P7YS0

File Name : LA-6911P

BOM P/N:43

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P7YE0/P7YH0/P7YS0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH  
ATI Seymour/Whistler/Granville

2010-11-01

REV:0.3

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                    |                 |            |                          |                            |               |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|--------------------------|----------------------------|---------------|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Compal Secret Data |                 |            | Compal Electronics, Inc. |                            |               |
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 2010/07/12         | Deciphered Date | 2012/07/12 | Title                    | SCHEMATIC,MB A6911         |               |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                    |                 |            | Custom                   | 4019A9                     | B             |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                    |                 |            | Date:                    | Tuesday, November 09, 2010 | Sheet 1 of 60 |



Voltage Rails

| Power Plane                                                                                     | Description                                                 | S1  | S3  | S5  |
|-------------------------------------------------------------------------------------------------|-------------------------------------------------------------|-----|-----|-----|
| VIN                                                                                             | Adapter power supply (19V)                                  | N/A | N/A | N/A |
| BATT+                                                                                           | Battery power supply (12.6V)                                | N/A | N/A | N/A |
| B+                                                                                              | AC or battery power rail for power circuit.                 | N/A | N/A | N/A |
| +CPU_CORE                                                                                       | Core voltage for CPU                                        | ON  | OFF | OFF |
| +VGA_CORE                                                                                       | Core voltage for GPU                                        | ON  | OFF | OFF |
| +VGFX_CORE                                                                                      | Core voltage for UMA graphic                                | ON  | OFF | OFF |
| +0.75VS                                                                                         | +0.75VP to +0.75VS switched power rail for DDR terminator   | ON  | OFF | OFF |
| +1.0VSDGPU                                                                                      | +1.0VSDGPU switched power rail for GPU                      | ON  | OFF | OFF |
| +1.05VS_VTT                                                                                     | +1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU     | ON  | OFF | OFF |
| +1.05VS_PCH                                                                                     | +1.05VS_VTT to +1.05VS_PCH power for PCH                    | ON  | OFF | OFF |
| +1.5V                                                                                           | +1.5VP to +1.5V power rail for DDRIII                       | ON  | ON  | OFF |
| +1.5VS                                                                                          | +1.5V to +1.5VS switched power rail                         | ON  | OFF | OFF |
| +1.5VSDGPU                                                                                      | +1.5V to +1.5VSDGPU switched power rail for GPU             | ON  | OFF | OFF |
| +1.8VS                                                                                          | (+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU | ON  | OFF | OFF |
| +3VALW                                                                                          | +3VALW always on power rail                                 | ON  | ON  | ON* |
| +3VALW_PCH                                                                                      | +3VALW to +3VALW_PCH power rail for PCH (Short Jumper)      | ON  | ON  | ON* |
| +3VS                                                                                            | +3VALW to +3VS power rail                                   | ON  | OFF | OFF |
| +5VALW                                                                                          | +5VALWP to +5VALW power rail                                | ON  | ON  | ON* |
| +5VALW_PCH                                                                                      | +5VALW to +5VALW_PCH power rail for PCH (Short resister)    | ON  | ON  | ON* |
| +5VS                                                                                            | +5VALW to +5VS switched power rail                          | ON  | OFF | OFF |
| +VSB                                                                                            | +VSBP to +VSB always on power rail for sequence control     | ON  | ON  | ON* |
| +RTCVCC                                                                                         | RTC power                                                   | ON  | ON  | ON  |
|                                                                                                 |                                                             |     |     |     |
|                                                                                                 |                                                             |     |     |     |
| Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF. |                                                             |     |     |     |

EC SM Bus1 address

| Device        | Address     | Device | Address |
|---------------|-------------|--------|---------|
| Smart Battery | 0001 011X b |        |         |

EC SM Bus2 address

PCH SM Bus address

| Device            | Address   | VRAM P/N |
|-------------------|-----------|----------|
| ChannelA DIMM0 A0 | 1010 000X | JDIMM1   |
| DIMM1 A2          | 1010 001X | JDIMM3   |
| ChannelB DIMM0 A4 | 1010 010X | JDIMM2   |
| DIMM1 A6          | 1010 011X | JDIMM4   |

SAM 64\*16 900M SA00004GS10(S IC D3 64M16 K4W1G1646G-BC11 FBGA ABOI)

SAM 64\*16 800M SA000035720(S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABOI)

SAM 128\*16 800M SA00003MQ60(S IC D3 128M16 K4W2G1646C-HC12 FBGA ABOI)

HYN 64\*16 900M SA000041S40(S IC D3 64MX16 H5TQ1G63DPR-11C FBGA ABOI)

HYN 64\*16 800M SA000032420(S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABOI)

HYN 128\*16 800M SA00003VS10(S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABOI)

HYN 64\*16 800M SA0000324G0(S IC D3 64M16 H5TQ1G63DPR-12C FBGA ABOI)

| BT Config        | GPU config                       | BACO config                                         |
|------------------|----------------------------------|-----------------------------------------------------|
| BT SKU: BT@      | Whistler: WHIS@                  | BACO: BACO@                                         |
| 4DIMM config     | Seymour: SEYM@                   | nonBACO: NOBACO@                                    |
| 4 DIMM: 4DIMM@   | Granville: GRAN@                 | Muxless config                                      |
| LVDS/eDP config  | Granville config                 | Muxless: MUXL@                                      |
| UMA LVDS: ULVDS@ | Granville: GRAN@ (VDDCI)         | nonMuxless: NOMUXL@ (DISO,UMA0)                     |
| DIS LVDS: DLVDS@ | nonGranville: NOGRAN@ (VGA_CORE) |                                                     |
| DIS eDP: DEDP@   | GPU Frame config                 |                                                     |
|                  | 128bit: 128@ (WHIS,GRAN)         |                                                     |
|                  |                                  | VRAM BOM Config                                     |
|                  |                                  | X76264BOL01: 64Mx16x4 Seymour 512M HYN NEW          |
|                  |                                  | X76264BOL02: 64Mx16x4 Seymour 512M HYN OLD          |
|                  |                                  | X76264BOL03: 64Mx16x8 Whistler/Granville 1G HYN NEW |
|                  |                                  | X76264BOL04: 64Mx16x8 Whistler/Granville 1G HYN OLD |
|                  |                                  | X76264BOL05: 128Mx16x8 Whistler/Granville 2G HYN    |
|                  |                                  | X76264BOL06: 128Mx16x8 Whistler/Granville 2G SAM    |
|                  |                                  | X76264BOL07: 128Mx16x4 Seymour 1G SAM               |
|                  |                                  | X76264BOL08: 128Mx16x4 Seymour 1G HYN               |

| BOM Config                    |                                         |                                |
|-------------------------------|-----------------------------------------|--------------------------------|
| * UMA Only LVDS Panel:        | BT@/UMA0@/UMA@/ULVDS@/NOMUXL@           | +DIMM,USB option               |
| * DIS Only LVDS Panel:        | BT@/DIS@/VGA@/DISO@/DLVDS@/NOMUXL@      | +X76+GPU +DIMM,USB option      |
| * DIS Only EDP Panel:         | BT@/DIS@/VGA@/DISO@/DEDP@/NOMUXL@       | +X76+GPU +DIMM,USB option      |
| * Muxless BACO LVDS Panel:    | BT@/UMA@/DIS@/VGA@/ULVDS@/BACO@/MUXL@   | +X76+GPU(S,W) +DIMM,USB option |
| * Muxless nonBACO LVDS Panel: | BT@/UMA@/DIS@/VGA@/ULVDS@/NOBACO@/MUXL@ | +X76+GPU(G) +DIMM,USB option   |

| STATE                | SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V  | +VS | Clock |
|----------------------|--------|---------|---------|---------|---------|-------|-----|-----|-------|
| Full ON              |        | HIGH    | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | ON    |
| S1(Power On Suspend) |        | LOW     | HIGH    | HIGH    | HIGH    | ON    | ON  | ON  | LOW   |
| S3 (Suspend to RAM)  |        | LOW     | LOW     | HIGH    | HIGH    | ON    | ON  | OFF | OFF   |
| S4 (Suspend to Disk) |        | LOW     | LOW     | LOW     | HIGH    | ON    | OFF | OFF | OFF   |
| S5 (Soft OFF)        |        | LOW     | LOW     | LOW     | LOW     | ON    | OFF | OFF | OFF   |

Board ID / SKU ID Table for AD channel

| Vcc      | 3.3V +/- 5%  |                         |                         |                         |
|----------|--------------|-------------------------|-------------------------|-------------------------|
| Ra/Rc/Re | 100K +/- 5%  |                         |                         |                         |
| Board ID | Rb / Rd / Rf | V <sub>AD_BID</sub> min | V <sub>AD_BID</sub> typ | V <sub>AD_BID</sub> max |
| 0        | 0            | 0 V                     | 0 V                     | 0 V                     |
| 1        | 8.2K +/- 5%  | 0.216 V                 | 0.250 V                 | 0.289 V                 |
| 2        | 18K +/- 5%   | 0.436 V                 | 0.503 V                 | 0.538 V                 |
| 3        | 33K +/- 5%   | 0.712 V                 | 0.819 V                 | 0.875 V                 |
| 4        | 56K +/- 5%   | 1.036 V                 | 1.185 V                 | 1.264 V                 |
| 5        | 100K +/- 5%  | 1.453 V                 | 1.650 V                 | 1.759 V                 |
| 6        | 200K +/- 5%  | 1.935 V                 | 2.200 V                 | 2.341 V                 |
| 7        | NC           | 2.500 V                 | 3.300 V                 | 3.300 V                 |

BOARD ID Table

| Board ID | PCB Revision |
|----------|--------------|
| 0        | 0.1          |
| 1        | 0.2          |
| 2        | 0.3          |
| 3        | 1.0          |
| 4        |              |
| 5        |              |
| 6        |              |
| 7        |              |

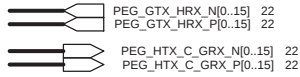
USB Port Table

| USB 2.0 | USB 1.1 | Port | 3 External USB Port          |
|---------|---------|------|------------------------------|
| EHCI1   | UHCI0   | 0    | USB/B(Right side 2.0 option) |
|         |         | 1    | USB/B(Right side 2.0 option) |
|         |         | 2    | USB port(left side 2.0)      |
|         | UHCI1   | 3    | USB/B(Right side 3.0 option) |
|         |         | 4    |                              |
|         |         | 5    |                              |
|         | UHCI2   | 6    |                              |
|         |         | 7    |                              |
|         |         | 8    | Mini Card(WLAN)              |
|         | UHCI4   | 9    | Mini Card                    |
|         |         | 10   | Camera                       |
|         |         | 11   | Card Reader                  |
| EHCI2   | UHC15   | 12   |                              |
|         |         | 13   | Blue Tooth                   |
|         |         |      |                              |

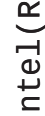
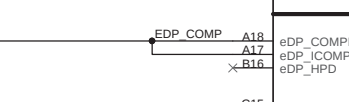
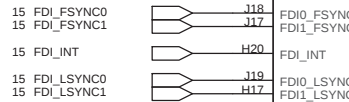
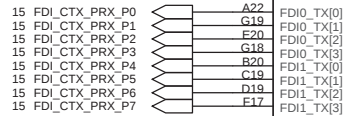
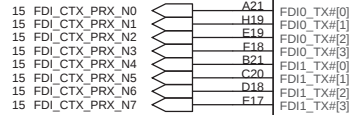
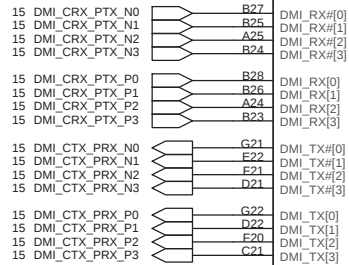
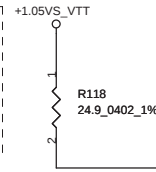
| BTO Option Table  |               |
|-------------------|---------------|
| BTO Item          | BOM Structure |
| UMA Only          | UMA0@         |
| Muxless/UMA       | UMA@          |
| DIS Only          | DIS0@         |
| Muxless/DIS       | DIS@          |
| Muxless/DIS       | VGA@          |
| BACO mode         | BACO@         |
| nonBACO mode      | NOBACO@       |
| VRAM              | X76@          |
| 128bit VRAM       | 128@          |
| Granville GPU     | GRAN@         |
| Whistler GPU      | WHIS@         |
| Seymour GPU       | SEYM@         |
| non Granville GPU | NOGRAN@       |
| Blue Tooth        | BT@           |
| Connector         | CONN@         |
| Unpop             | @             |
|                   |               |
| DIS eDP           | DEDP@         |
| UMA LVDS          | ULVDS@        |
| DIS LVDS          | DLVDS@        |
| Muxless           | MUXL@         |
| non Muxless       | NOMUXL@       |
| USB2.0 Conn       | USB2@         |
| USB3.0 Conn       | USB3@         |
| 4 Dimm            | 4DIMM@        |
|                   |               |
|                   |               |

| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                                 | Compal Secret Data |                 |            | Compal Electronics, Inc. |                            |               |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|--------------------------|----------------------------|---------------|
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 2010/07/12         | Deciphered Date | 2012/07/12 | Title                    | SCHEMATIC,MB A6911         |               |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                    |                 |            | Date:                    | Tuesday, November 09, 2010 | Sheet 3 of 60 |

PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



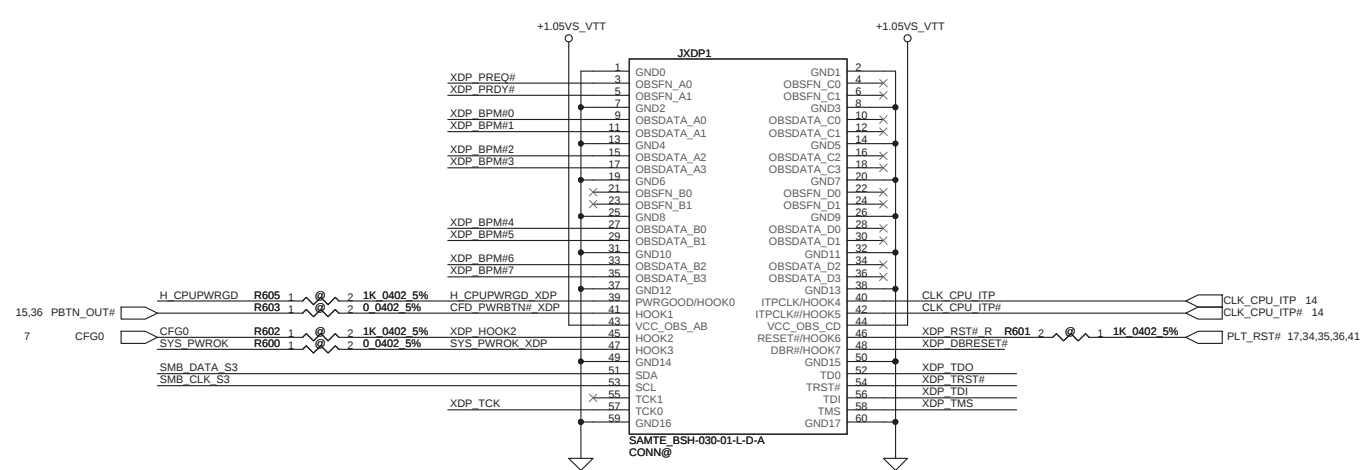
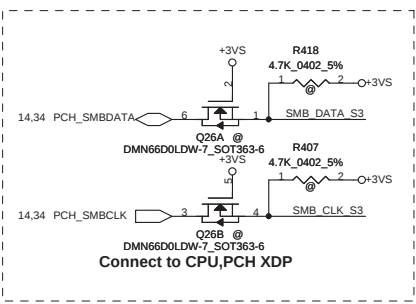
eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms should not be left floating ,even if disable eDP function...



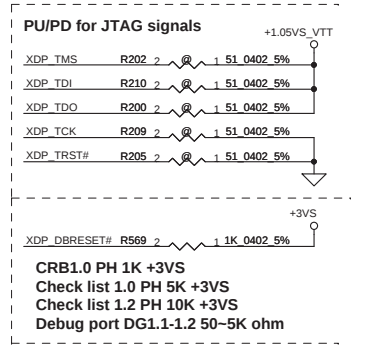
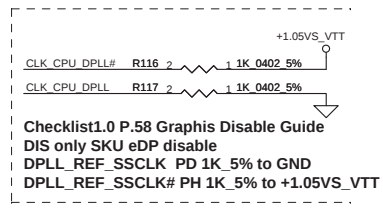
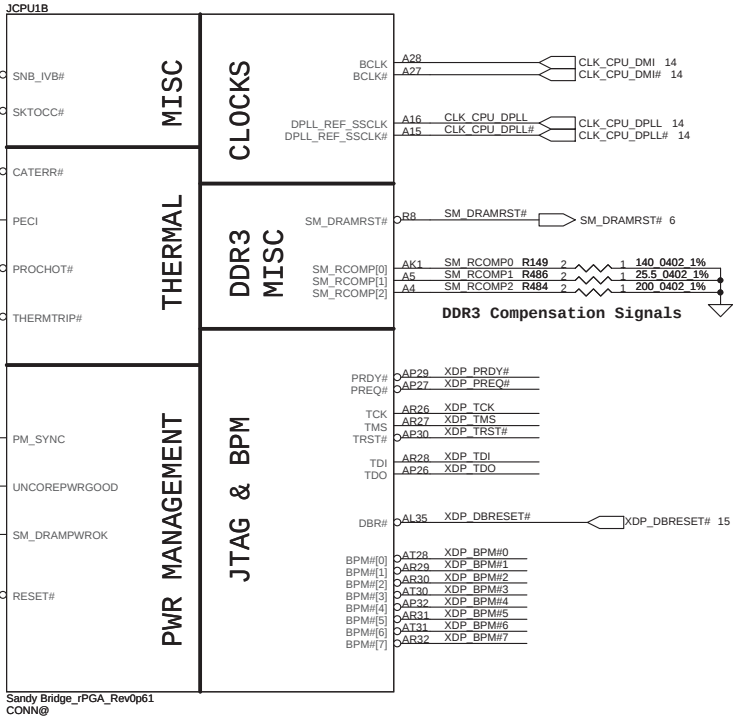
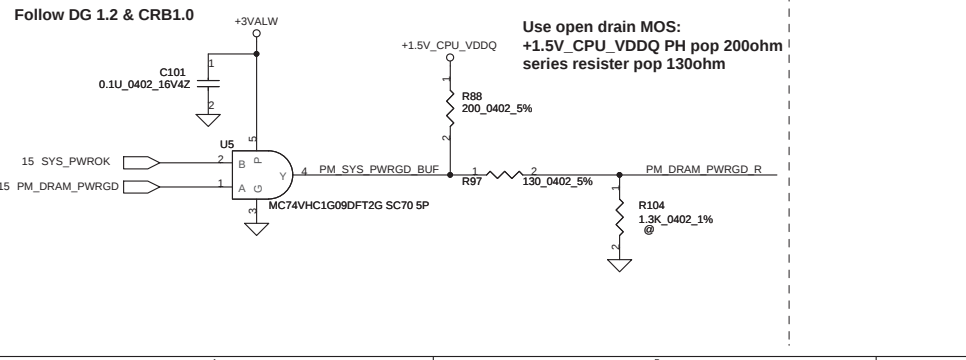
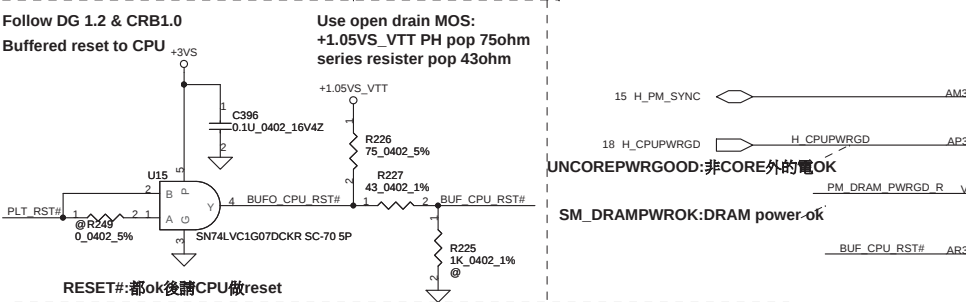
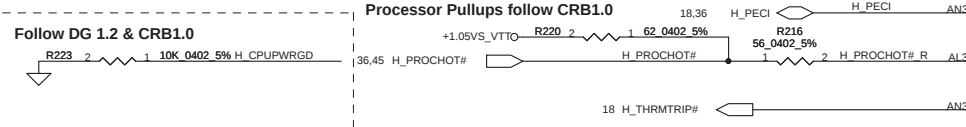
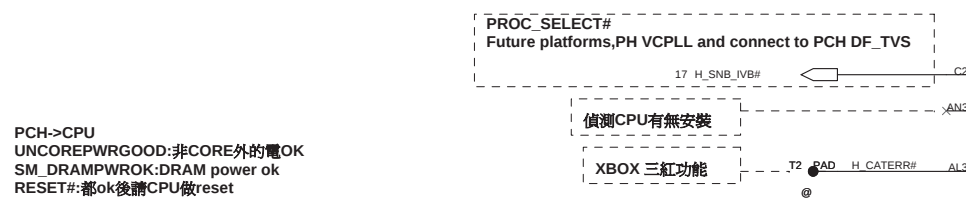
PCI EXPRESS\* - GRAPHICS

|            |     |                   |            |      |                                            |
|------------|-----|-------------------|------------|------|--------------------------------------------|
| PEG_ICOMPI | J22 | PEG_COMP          | 1.05VS_VTT | R532 | 24.9_0402_1%                               |
| PEG_ICOMPO | J21 |                   |            |      |                                            |
| PEG_RCOMPO | H22 |                   |            |      |                                            |
| PEG_RX#0   | K33 | PEG GTX C HRX N15 | C320       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N15   |
| PEG_RX#1   | M35 | PEG GTX C HRX N14 | C316       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N14   |
| PEG_RX#2   | L34 | PEG GTX C HRX N13 | C313       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N13   |
| PEG_RX#3   | J35 | PEG GTX C HRX N12 | C308       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N12   |
| PEG_RX#4   | J32 | PEG GTX C HRX N11 | C300       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N11   |
| PEG_RX#5   | H34 | PEG GTX C HRX N10 | C297       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N10   |
| PEG_RX#6   | H31 | PEG GTX C HRX N9  | C287       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N9    |
| PEG_RX#7   | G33 | PEG GTX C HRX N8  | C275       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N8    |
| PEG_RX#8   | G30 | PEG GTX C HRX N7  | C262       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N7    |
| PEG_RX#9   | E35 | PEG GTX C HRX N6  | C249       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N6    |
| PEG_RX#10  | E32 | PEG GTX C HRX N5  | C244       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N5    |
| PEG_RX#11  | D33 | PEG GTX C HRX N4  | C233       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N4    |
| PEG_RX#12  | D31 | PEG GTX C HRX N3  | C224       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N3    |
| PEG_RX#13  | D31 | PEG GTX C HRX N2  | C207       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N2    |
| PEG_RX#14  | B33 | PEG GTX C HRX N1  | C206       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N1    |
| PEG_RX#15  | C32 | PEG GTX C HRX N0  | C194       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX N0    |
| PEG_RX#16  | J33 | PEG GTX C HRX P15 | C318       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P15   |
| PEG_RX#17  | L35 | PEG GTX C HRX P14 | C314       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P14   |
| PEG_RX#18  | K34 | PEG GTX C HRX P13 | C309       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P13   |
| PEG_RX#19  | H35 | PEG GTX C HRX P12 | C303       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P12   |
| PEG_RX#20  | H32 | PEG GTX C HRX P11 | C298       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P11   |
| PEG_RX#21  | G34 | PEG GTX C HRX P10 | C288       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P10   |
| PEG_RX#22  | G31 | PEG GTX C HRX P9  | C278       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P9    |
| PEG_RX#23  | F33 | PEG GTX C HRX P8  | C265       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P8    |
| PEG_RX#24  | F30 | PEG GTX C HRX P7  | C255       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P7    |
| PEG_RX#25  | E35 | PEG GTX C HRX P6  | C246       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P6    |
| PEG_RX#26  | E33 | PEG GTX C HRX P5  | C235       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P5    |
| PEG_RX#27  | F32 | PEG GTX C HRX P4  | C226       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P4    |
| PEG_RX#28  | D34 | PEG GTX C HRX P3  | C214       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P3    |
| PEG_RX#29  | E31 | PEG GTX C HRX P2  | C210       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P2    |
| PEG_RX#30  | C33 | PEG GTX C HRX P1  | C196       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P1    |
| PEG_RX#31  | B32 | PEG GTX C HRX P0  | C190       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG GTX HRX P0    |
| PEG_TX#0   | M29 | PEG HTX GRX N15   | C885       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N15 |
| PEG_TX#1   | M32 | PEG HTX GRX N14   | C883       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N14 |
| PEG_TX#2   | M31 | PEG HTX GRX N13   | C880       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N13 |
| PEG_TX#3   | L32 | PEG HTX GRX N12   | C676       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N12 |
| PEG_TX#4   | L29 | PEG HTX GRX N11   | C673       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N11 |
| PEG_TX#5   | K31 | PEG HTX GRX N10   | C671       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N10 |
| PEG_TX#6   | K28 | PEG HTX GRX N9    | C667       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N9  |
| PEG_TX#7   | J30 | PEG HTX GRX N8    | C663       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N8  |
| PEG_TX#8   | J28 | PEG HTX GRX N7    | C661       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N7  |
| PEG_TX#9   | H29 | PEG HTX GRX N6    | C659       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N6  |
| PEG_TX#10  | G27 | PEG HTX GRX N5    | C654       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N5  |
| PEG_TX#11  | E29 | PEG HTX GRX N4    | C648       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N4  |
| PEG_TX#12  | E27 | PEG HTX GRX N3    | C644       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N3  |
| PEG_TX#13  | D28 | PEG HTX GRX N2    | C640       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N2  |
| PEG_TX#14  | E26 | PEG HTX GRX N1    | C637       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N1  |
| PEG_TX#15  | E25 | PEG HTX GRX N0    | C631       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX N0  |
| PEG_TX#16  | M28 | PEG HTX GRX P15   | C684       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P15 |
| PEG_TX#17  | M33 | PEG HTX GRX P14   | C681       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P14 |
| PEG_TX#18  | M30 | PEG HTX GRX P13   | C677       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P13 |
| PEG_TX#19  | L31 | PEG HTX GRX P12   | C674       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P12 |
| PEG_TX#20  | L28 | PEG HTX GRX P11   | C670       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P11 |
| PEG_TX#21  | K30 | PEG HTX GRX P10   | C668       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P10 |
| PEG_TX#22  | K27 | PEG HTX GRX P9    | C664       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P9  |
| PEG_TX#23  | J29 | PEG HTX GRX P8    | C662       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P8  |
| PEG_TX#24  | J27 | PEG HTX GRX P7    | C658       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P7  |
| PEG_TX#25  | H28 | PEG HTX GRX P6    | C657       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P6  |
| PEG_TX#26  | G28 | PEG HTX GRX P5    | C650       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P5  |
| PEG_TX#27  | E28 | PEG HTX GRX P4    | C645       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P4  |
| PEG_TX#28  | E28 | PEG HTX GRX P3    | C641       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P3  |
| PEG_TX#29  | D27 | PEG HTX GRX P2    | C636       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P2  |
| PEG_TX#30  | E26 | PEG HTX GRX P1    | C635       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P1  |
| PEG_TX#31  | D25 | PEG HTX GRX P0    | C626       | 1    | 2 DIS@ 0.22U 0402 6.3V6K PEG HTX C GRX P0  |

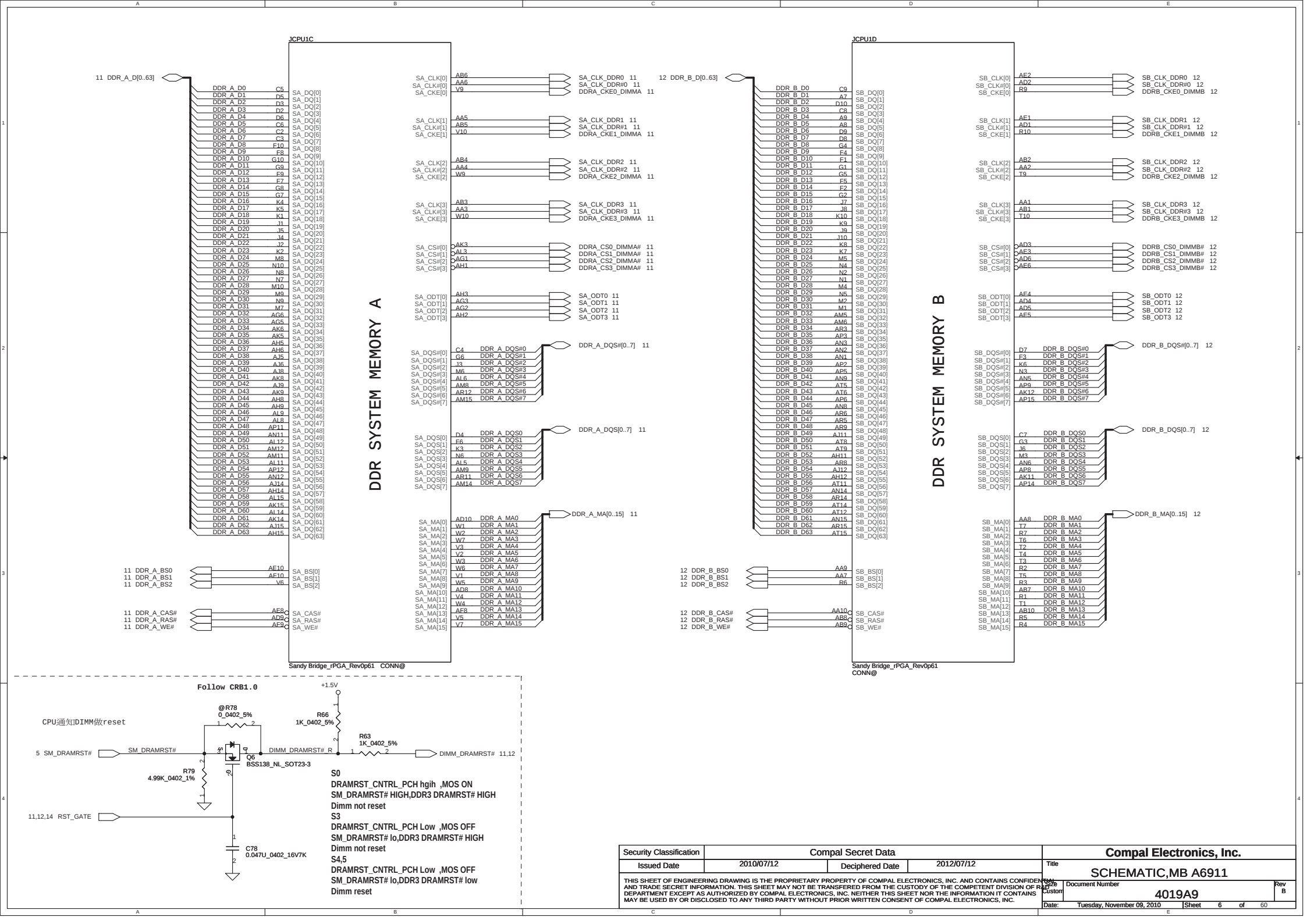
Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)



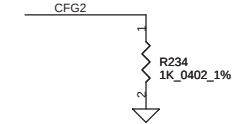
Debug port DG 0.65--  
Note: 1. These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed



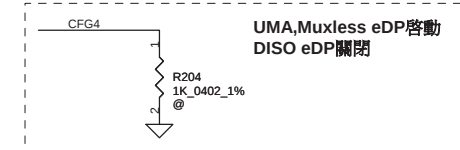
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            |                            |               |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|----------------------------|---------------|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       | Compal Secret Data |                 |            | Compal Electronics, Inc.   |               |
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 2010/07/12         | Deciphered Date | 2012/07/12 | SHEMATIC,MB A6911          |               |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | 4019A9                     |               |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Tuesday, November 09, 2010 | Sheet 5 of 60 |



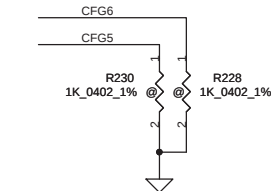
## CFG Straps for Processor



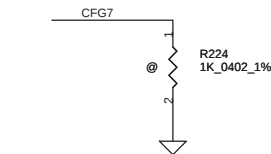
| PEG Static Lane Reversal - CFG2 is for the 16x |                                                                                                              |
|------------------------------------------------|--------------------------------------------------------------------------------------------------------------|
| CFG2                                           | <b>1: Normal Operation; Lane # definition matches socket pin map definition</b><br><b>★ 0: Lane Reversed</b> |



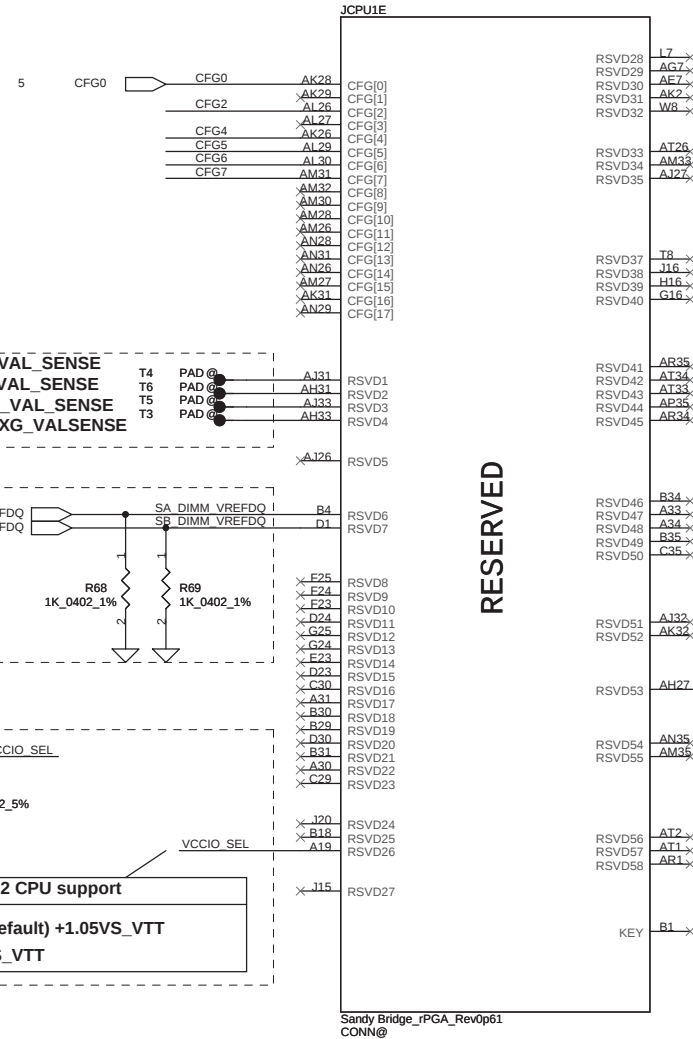
| eDP enable |                                         |
|------------|-----------------------------------------|
| CFG4       | <b>★ 1: Disable</b><br><b>0: Enable</b> |



| PCIe Port Bifurcation Straps |                                                                                                                                |
|------------------------------|--------------------------------------------------------------------------------------------------------------------------------|
| CFG[6:5]                     | <b>★11: (Default) 1x16 PCI Express</b><br><b>10: 2x8 PCI Express</b><br><b>01: Reserved</b><br><b>00: 1x8, 2x4 PCI Express</b> |

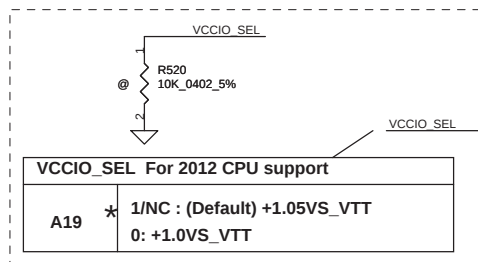
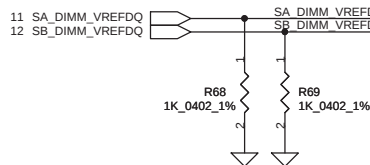


| PEG DEFER TRAINING |                                                                                                                       |
|--------------------|-----------------------------------------------------------------------------------------------------------------------|
| CFG7               | <b>1: (Default) PEG Train immediately following xxRESETB de assertion</b><br><b>0: PEG Wait for BIOS for training</b> |



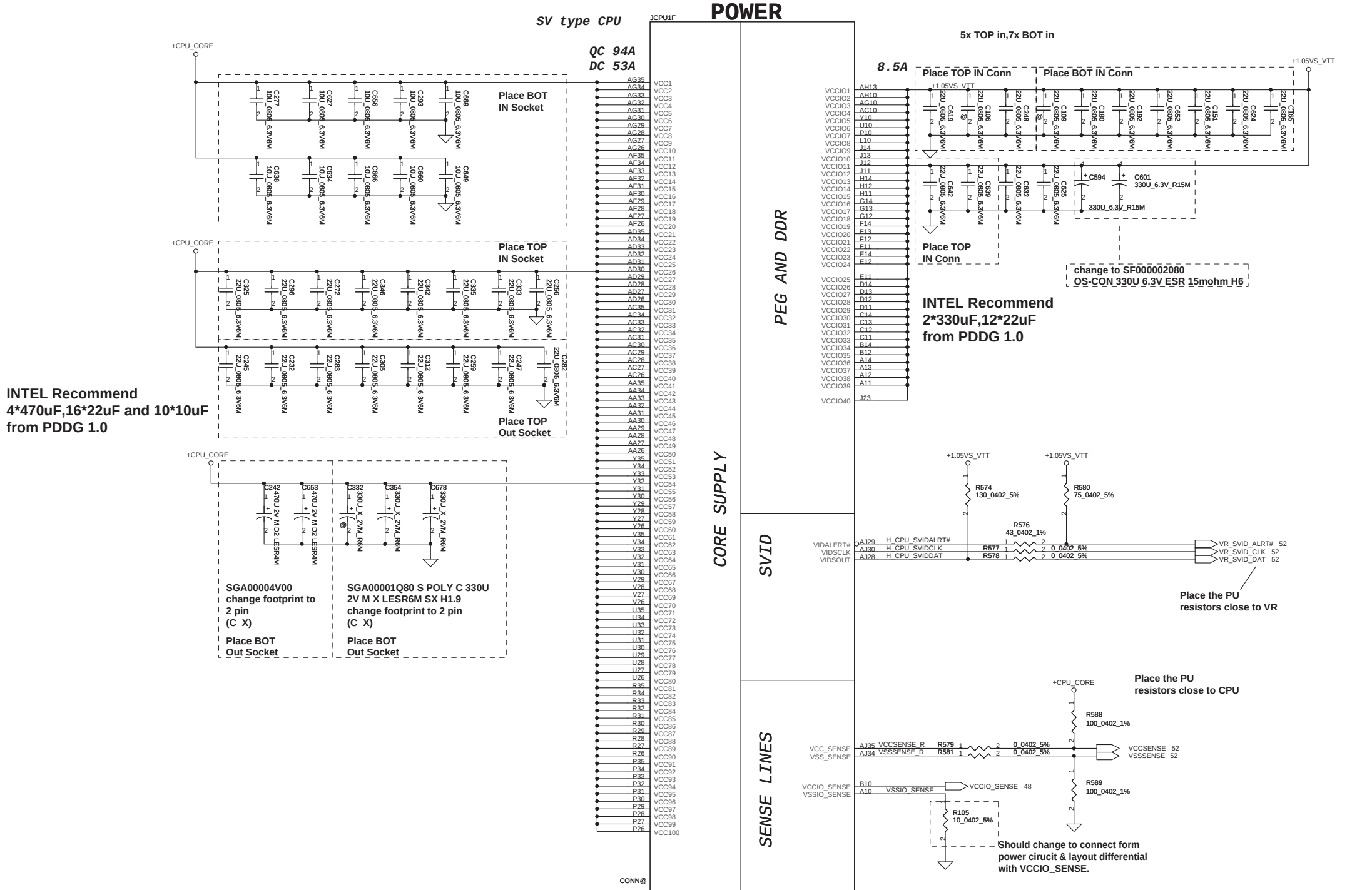
Sandy Bridge\_rPGA\_Rev0p61  
CONN@

**SA\_DIMM\_VREFDQ**  
**SB\_DIMM\_VREFDQ**  
 For Future CPU M3 support,  
 Sandey bridge not support M3,  
 Check list1.0&CRB say can NC



| VCCIO_SEL For 2012 CPU support |                                                               |
|--------------------------------|---------------------------------------------------------------|
| A19                            | <b>★ 1/NC : (Default) +1.05VS_VTT</b><br><b>0: +1.0VS_VTT</b> |

| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |            | Compal Secret Data |            | Compal Electronics, Inc. |                            |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Date:                    | Tuesday, November 09, 2010 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Sheet                    | 7 of 60                    |



INTEL Recommend  
2\*470uF,12\*22uF  
from PDDG 1.0

SGA00001Q80 S POLY C 330U  
2V M X LESR6M SX H1.9

- Vaxg**
- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
  - VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

change to SF000002080  
OS-CON 330U 6.3V ESR 15mohm H6

INTEL Recommend  
1\*330uF,1\*10uF and 2\*1uF(0402)  
from PDDG 1.0

## POWER

### GRAPHICS

#### SENSE LINES

#### VREF

#### DDR3 -1.5V RAILS

#### SA RAIL

#### MISC

QC 33A  
DC 26A

JCPU1G

Sandy Bridge\_rPGA\_Rev0p61  
CONN@

### 1.8V RAIL

VAXG\_SENSE  
VSSAXG\_SENSE

SM\_VREF

VDDQ1  
VDDQ2  
VDDQ3  
VDDQ4  
VDDQ5  
VDDQ6  
VDDQ7  
VDDQ8  
VDDQ9  
VDDQ10  
VDDQ11  
VDDQ12  
VDDQ13  
VDDQ14  
VDDQ15

VCCSA1  
VCCSA2  
VCCSA3  
VCCSA4  
VCCSA5  
VCCSA6  
VCCSA7  
VCCSA8

VCCPLL1  
VCCPLL2  
VCCPLL3

VCCSA\_SENSE  
FC\_C22  
VCCSA\_VID1

VCC\_AXG\_SENSE 52  
VSS\_AXG\_SENSE 52

+V SM\_VREF should  
have 20 mil trace width

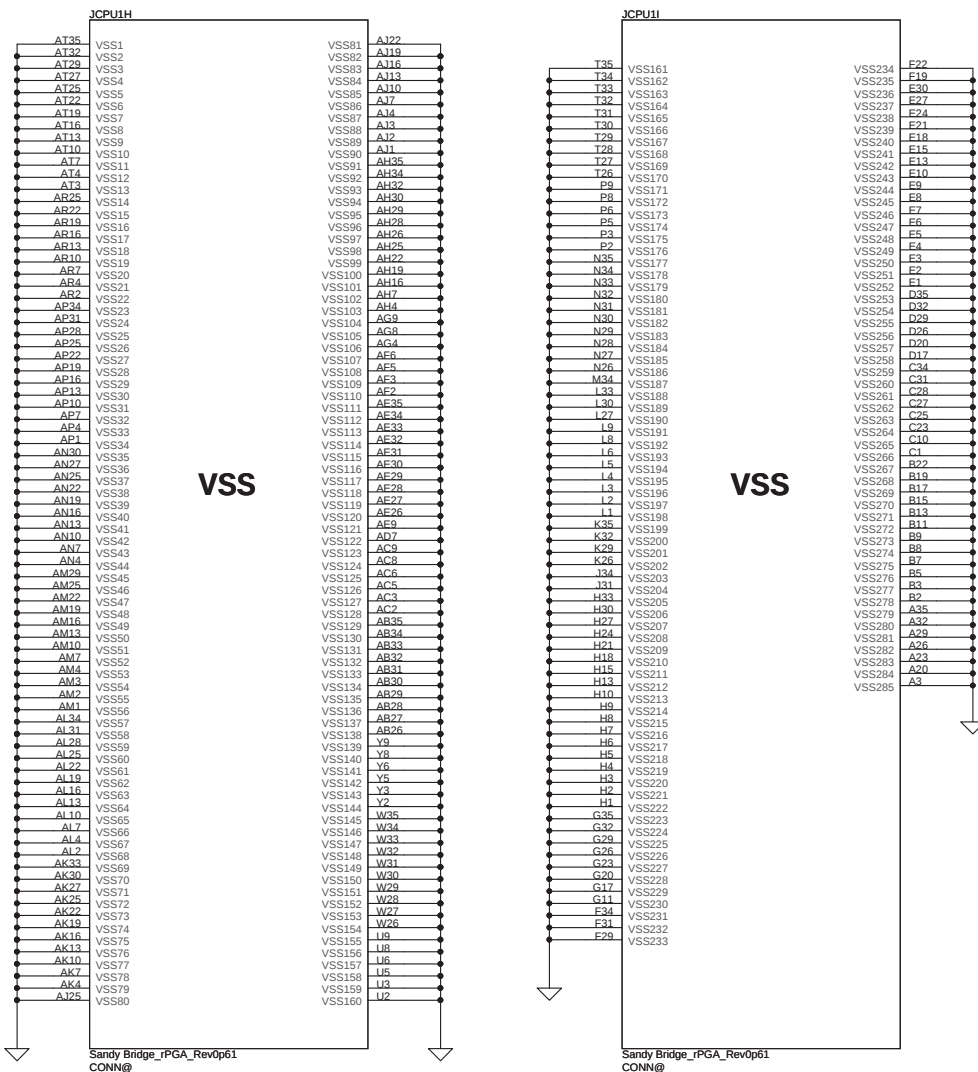
10A

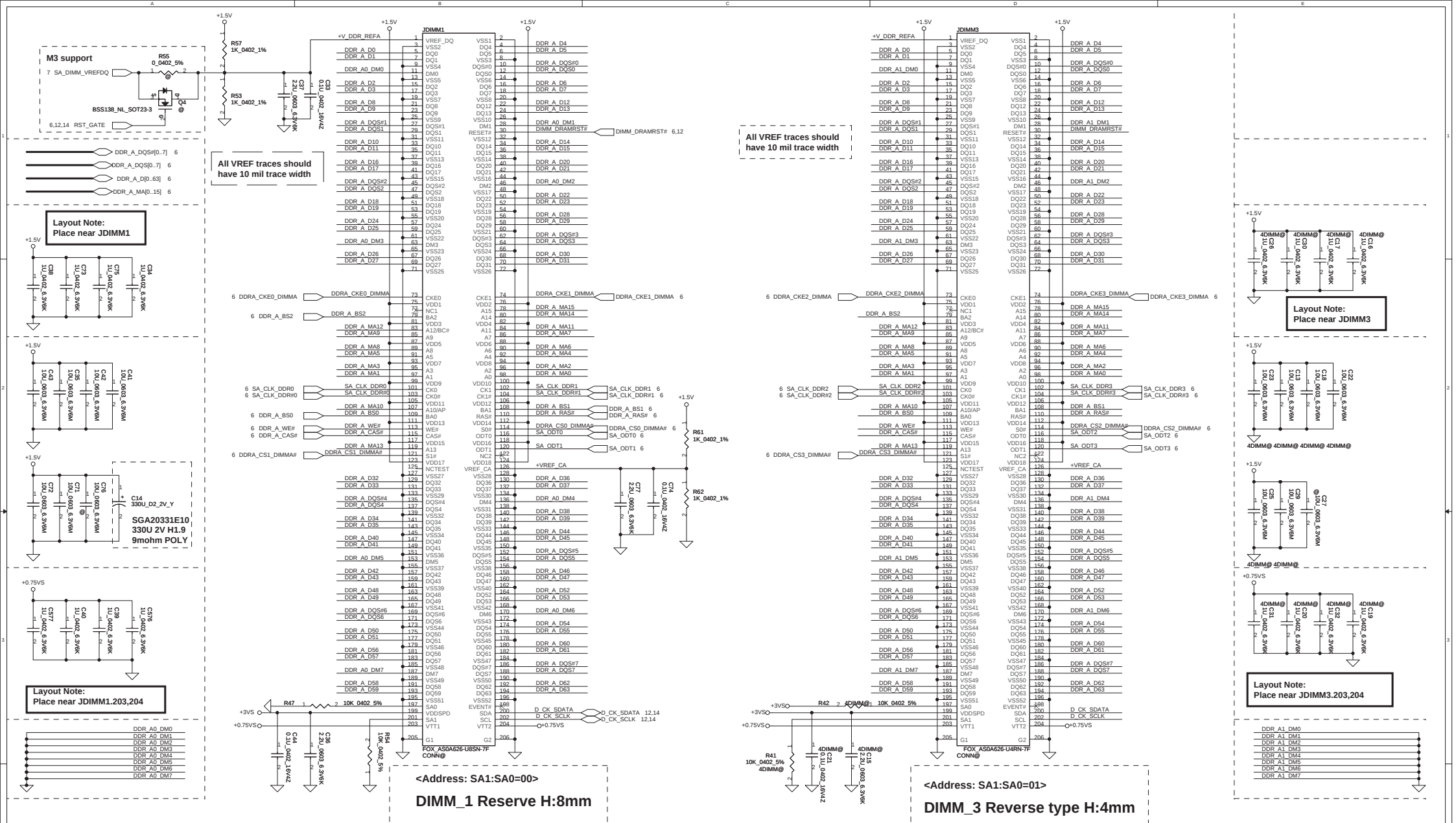
6A

CPU EDS1.3 P.93  
VCCSA\_VID0 Must PD

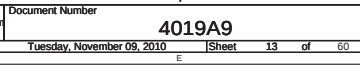
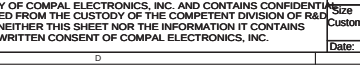
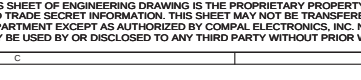
VCCSA\_VID0  
For 2012 future CPU  
VCCSA voltage select

| VCCSA |      |        |         |         |
|-------|------|--------|---------|---------|
| VID0  | VID1 | Vout   | 2011CPU | 2012CPU |
| 0     | 0    | 0.9V   | V       | V       |
| 0     | 1    | 0.8V   | V       | V       |
| 1     | 0    | 0.725V | X       | V       |
| 1     | 1    | 0.675V | X       | V       |

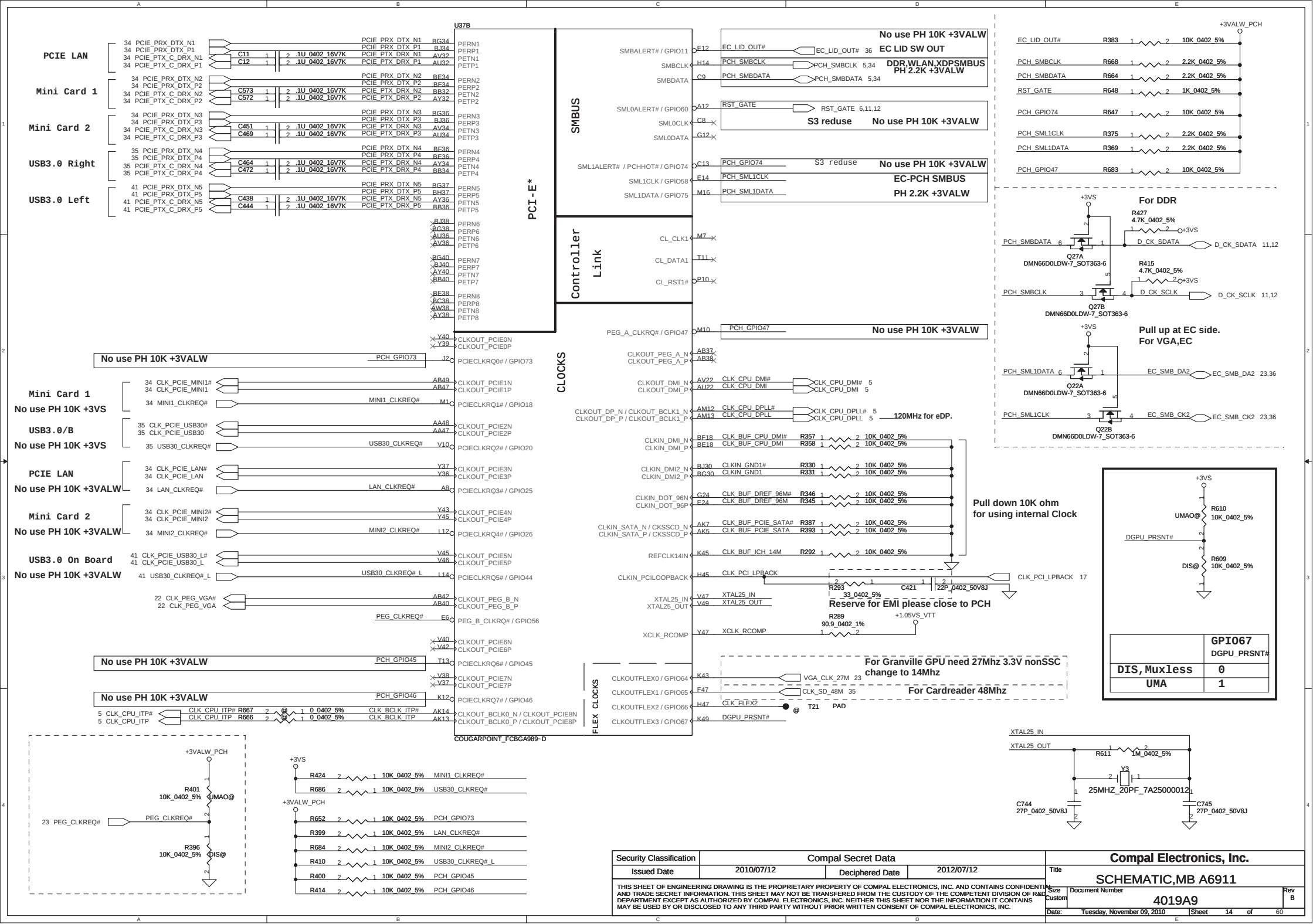


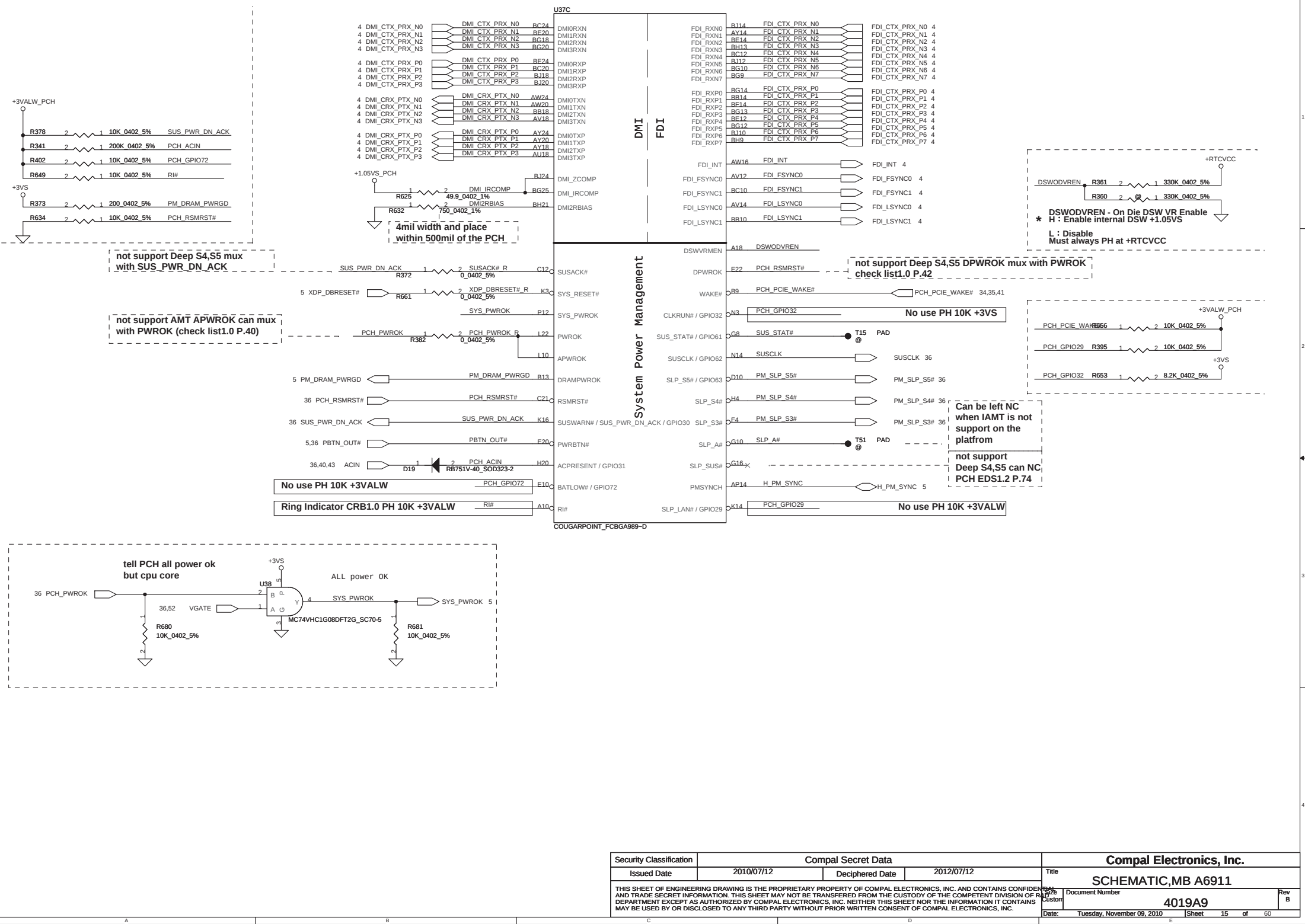




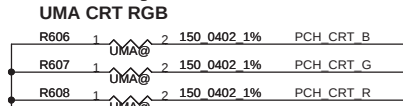
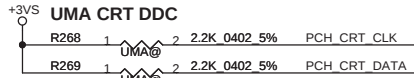
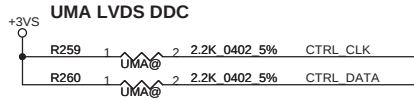
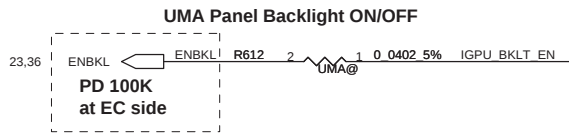


|       |                                 |  |
|-------|---------------------------------|--|
|       | <b>Compal Electronics, Inc.</b> |  |
| Title |                                 |  |





|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            |                          |                            |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Sheet                    | 15 of 60                   |

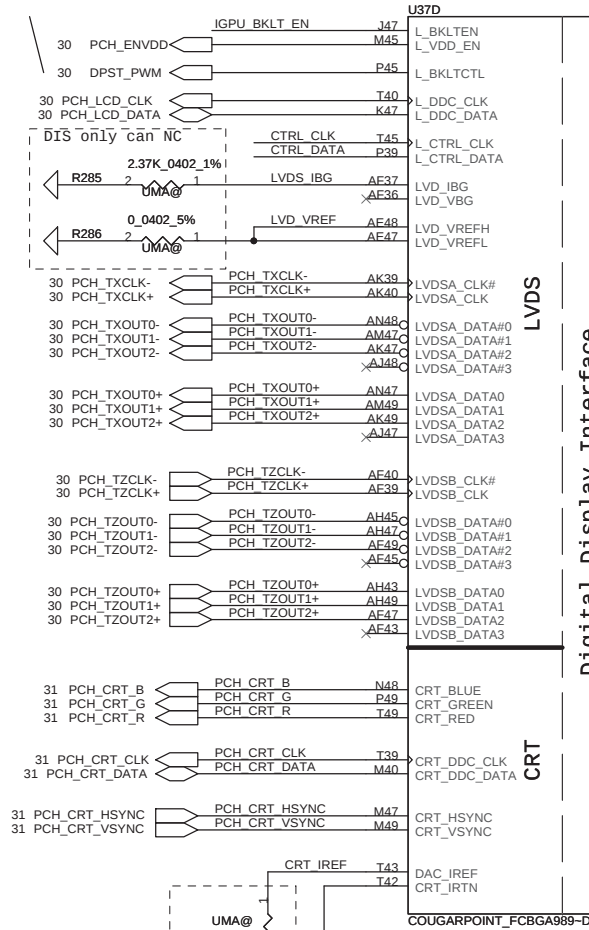


Check list1.0 P.55 disable Graphics  
ALL Can NC  
but DAC\_IREF still need PD

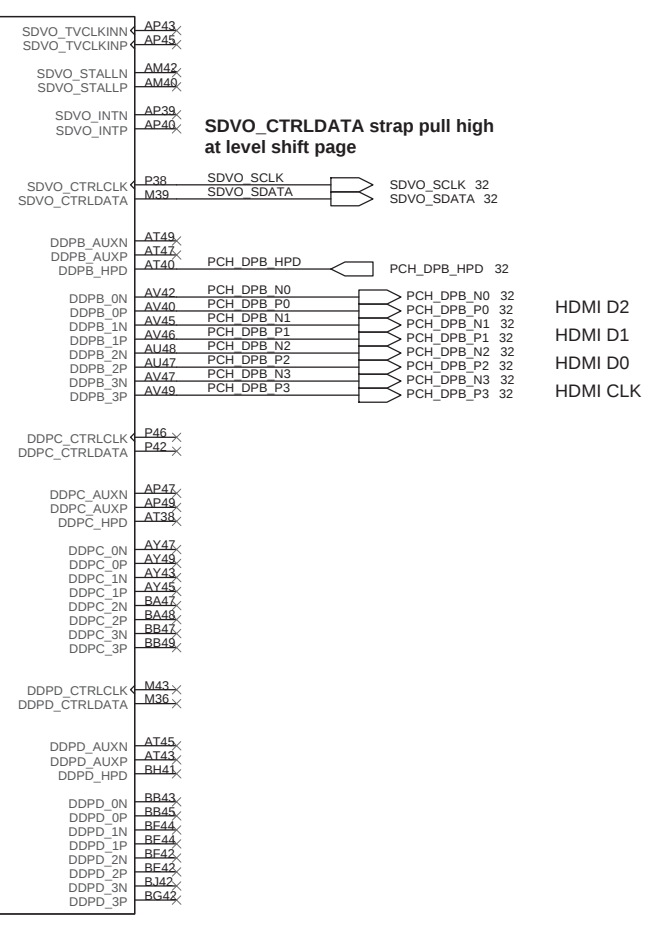
LVDS disable:  
DATA/Clock/Control an NC  
VCC\_TX\_LVDS,VCCA\_LVDS PD to GND

CRT disable:  
DATA/Clock/Control an NC  
VCCADAC connect to +3VS

Pull high at LVDS conn side.

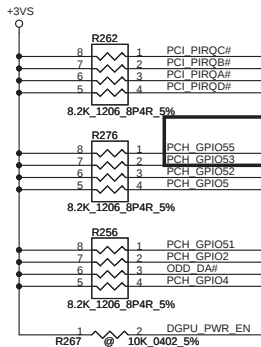


Digital Display Interface

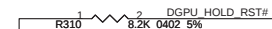


DIS only sku can use 1K\_0402\_5% to GND

|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            |                          |                            |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Sheet                    | 16 of 60                   |



可以不用PH,如做GPIO使用PH+3VS

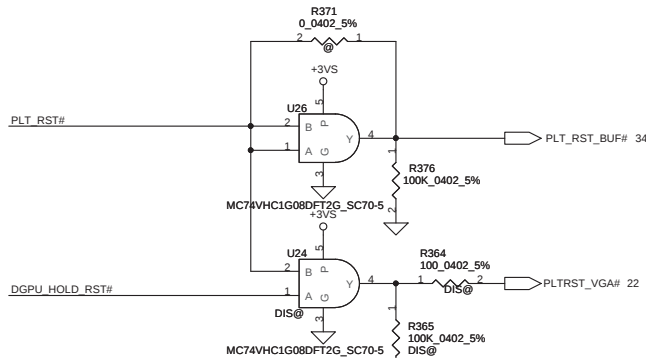
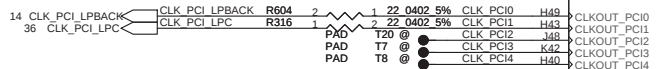
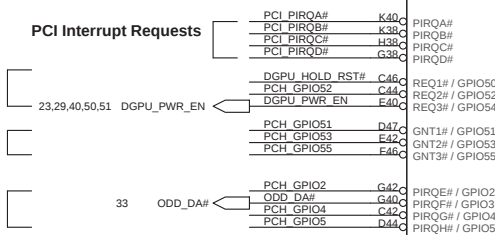


| Boot BIOS Strap  |                         |       |             |
|------------------|-------------------------|-------|-------------|
| GNT1#/<br>GPIO51 | GPIO19 GPIO51 Boot BIOS |       | Destination |
|                  | Bit11                   | Bit10 |             |
| Internal         | 0                       | 1     | Reserved    |
| PH               | 1                       | 0     | PCI         |
|                  | 0                       | 0     | LPC         |

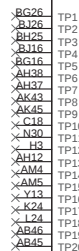
只剩GPIO的功能没有strap function  
不做GPIO要PH +3VS,如做GPIO PH +3VS

只剩GPIO的功能没有strap function  
無須PH(Internal PH),如做GPIO PH +3VS

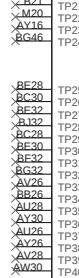
#### PCI Interrupt Requests



#### U37E



#### RSVD



#### PCI

#### USB



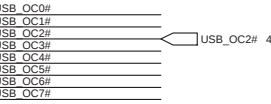
#### COUGARPOINT\_FCBGA989-D



Some PCH config not support USB port 6 & 7.

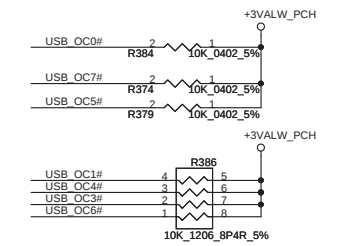
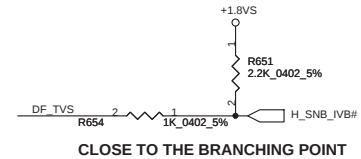
- Mini Card (WLAN)
- Mini Card (WWAN)
- CMOS Camera (LVDS)
- Card Reader
- Mini Card (SIM card)
- Bluetooth

Within 500 mils



| DMI,FDI Termination Voltage |                                             |
|-----------------------------|---------------------------------------------|
| DF_TVSS                     | Set to Vcc when HIGH<br>Set to Vss when LOW |

DG1.2 CRB1.0 PH 2.2K series 1K  
For 2012 support

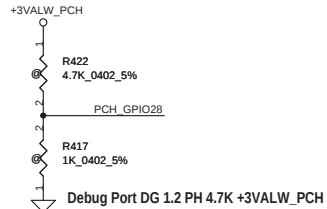


## HDA\_SYNC PH(PLL =+1.5VS)

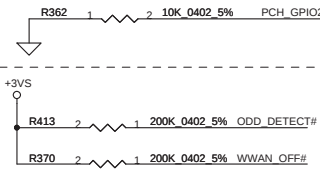
## GPIO28

## On-Die PLL Voltage Regulator

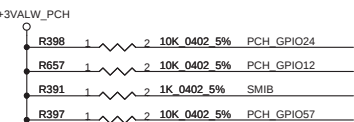
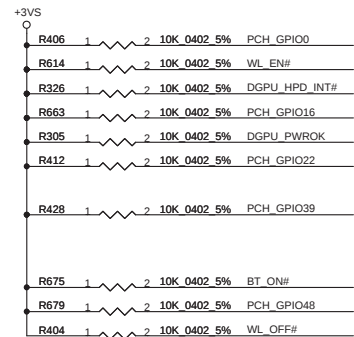
This signal has a weak internal pull up  
\* H : On-Die PLL voltage regulator enable  
L : On-Die PLL Voltage Regulator disable



Deep S4,S5 wake event signal  
RTC alarm,Power BTN,GPIO27  
PCH\_GPIO27 (Have internal Pull-High)  
Deep S4,S5 wake event signal  
No use PD to GND Check list1.0 P.70



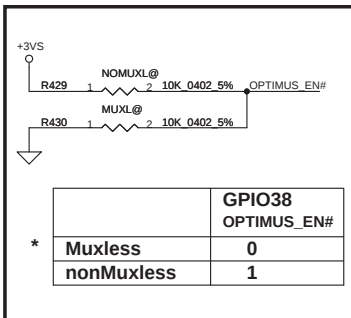
SATA2GP/GPIO36 & SATA3GP/GPIO37  
Sampled at Rising edge of PWROK.  
Weak internal pull-down.  
(weak internal pull-down is disabled  
after PLTRST# de-asserts)  
NOTE: This signal should NOT be  
pulled high when strap is sampled



|                    |                  |     |
|--------------------|------------------|-----|
| No use PH 10K +3VS | PCH_GPIO0        | T7  |
| No use PH 10K +3VS | 35 WL_EN#        | A42 |
| No use PH 10K +3VS | 32 DGPU_HPD_INT# | H36 |
|                    | 36 EC_SC#        | E38 |
|                    | 36 EC_SMI#       | C10 |

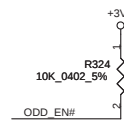
|                                                      |            |    |
|------------------------------------------------------|------------|----|
| No use PH +3VALW                                     | PCH_GPIO12 | C4 |
| USB3.0 System management<br>Interrupt signal "SMI#". | 35,41 SMIB | G2 |
| No use PH +3VS                                       | PCH_GPIO16 | U2 |

|                                               |                |     |
|-----------------------------------------------|----------------|-----|
| No use PH 10K +3VS                            | PCH_GPIO22     | T5  |
| CRB1.0 PH 10K +3VALW                          | PCH_GPIO24     | E8  |
| No use PD 10K to GND                          | PCH_GPIO27     | F16 |
| No use PH 10K +3VALW                          | PCH_GPIO28     | P8  |
| No use PH 10K +3VS BT ON/OFF                  | 34,35 BT_ON#   | K1  |
| No use can NC                                 | PAD T16 @      | K4  |
| Can't PH                                      | 33 ODD_DETECT# | V8  |
| Can't PH                                      | 34 WWAN_OFF#   | M5  |
| No use PH 10K +3VS Optimus(L)/ non optimus(H) | OPTIMUS_EN#    | N2  |
| No use PH 10K +3VS                            | PCH_GPIO39     | M3  |
| No use PH 10K +3VS                            | PCH_GPIO48     | V13 |
| SATA5GP&TEMP_ALERT# CRB PH 10K +3VSWL_OFF#    | WL_OFF#        | V3  |
| No use PH +3VALW or PD to GND                 | PCH_GPIO57     | D6  |

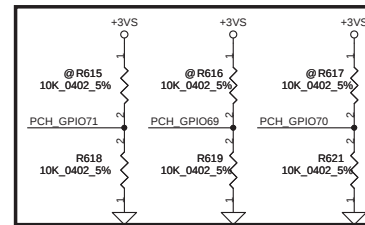


|            | GPIO38<br>OPTIMUS_EN# |
|------------|-----------------------|
| * Muxless  | 0                     |
| nonMuxless | 1                     |

GPIO24 Unmultiplexed  
NOTE: GPIO24 configuration  
register bits are not cleared by  
CF9h reset event.  
CRB1.0 PH10K to +3VALW



Fan Tachometer Inputs  
TACH1-7 only on server  
can insted to GPIO



| Project ID | GPIO69 | GPIO70 | GPIO71 |
|------------|--------|--------|--------|
| * P7YE0    | 0      | 0      | 0      |
| X          | 0      | 0      | 1      |
| X          | 0      | 1      | 0      |
| X          | 0      | 1      | 1      |
| X          | 1      | 0      | 0      |
| X          | 0      | 0      | 1      |
| X          | 0      | 1      | 0      |
| X          | 0      | 1      | 1      |
| X          | 1      | 0      | 0      |
| X          | 1      | 0      | 1      |
| X          | 1      | 1      | 0      |
| X          | 1      | 1      | 1      |

GPIO

CPU/MISC

NCTF

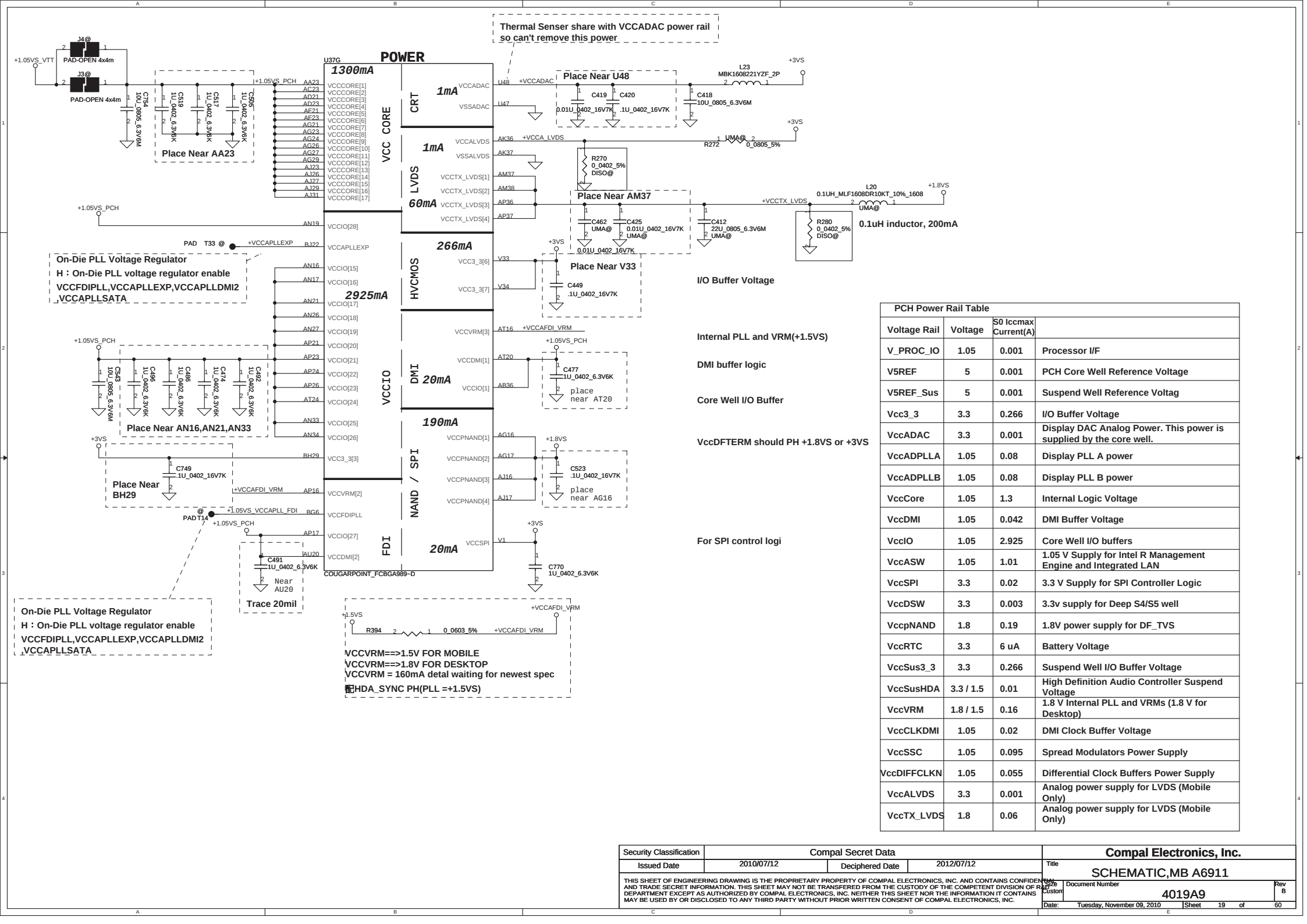
|      |                           |                |
|------|---------------------------|----------------|
| U37F | BMBUSY# / GPIO0           | TACH4 / GPIO68 |
|      | TACH1 / GPIO1             | TACH5 / GPIO69 |
|      | TACH2 / GPIO6             | TACH6 / GPIO70 |
|      | TACH3 / GPIO7             | TACH7 / GPIO71 |
|      | GPIO8                     |                |
|      | LAN_PHY_PWR_CTRL / GPIO12 |                |
|      | GPIO15                    |                |
|      | SATA4GP / GPIO16          |                |
|      | TACH0 / GPIO17            |                |
|      | SCLOCK / GPIO22           |                |
|      | GPIO24 / MEM_LED          |                |
|      | GPIO27                    |                |
|      | GPIO28                    |                |
|      | STP_PC# / GPIO34          |                |
|      | GPIO35                    |                |
|      | SATA2GP / GPIO36          |                |
|      | SATA3GP / GPIO37          |                |
|      | SLOAD / GPIO38            |                |
|      | SDATAOUT0 / GPIO39        |                |
|      | SDATAOUT1 / GPIO48        |                |
|      | SATA5GP / GPIO49          |                |
|      | GPIO57                    |                |

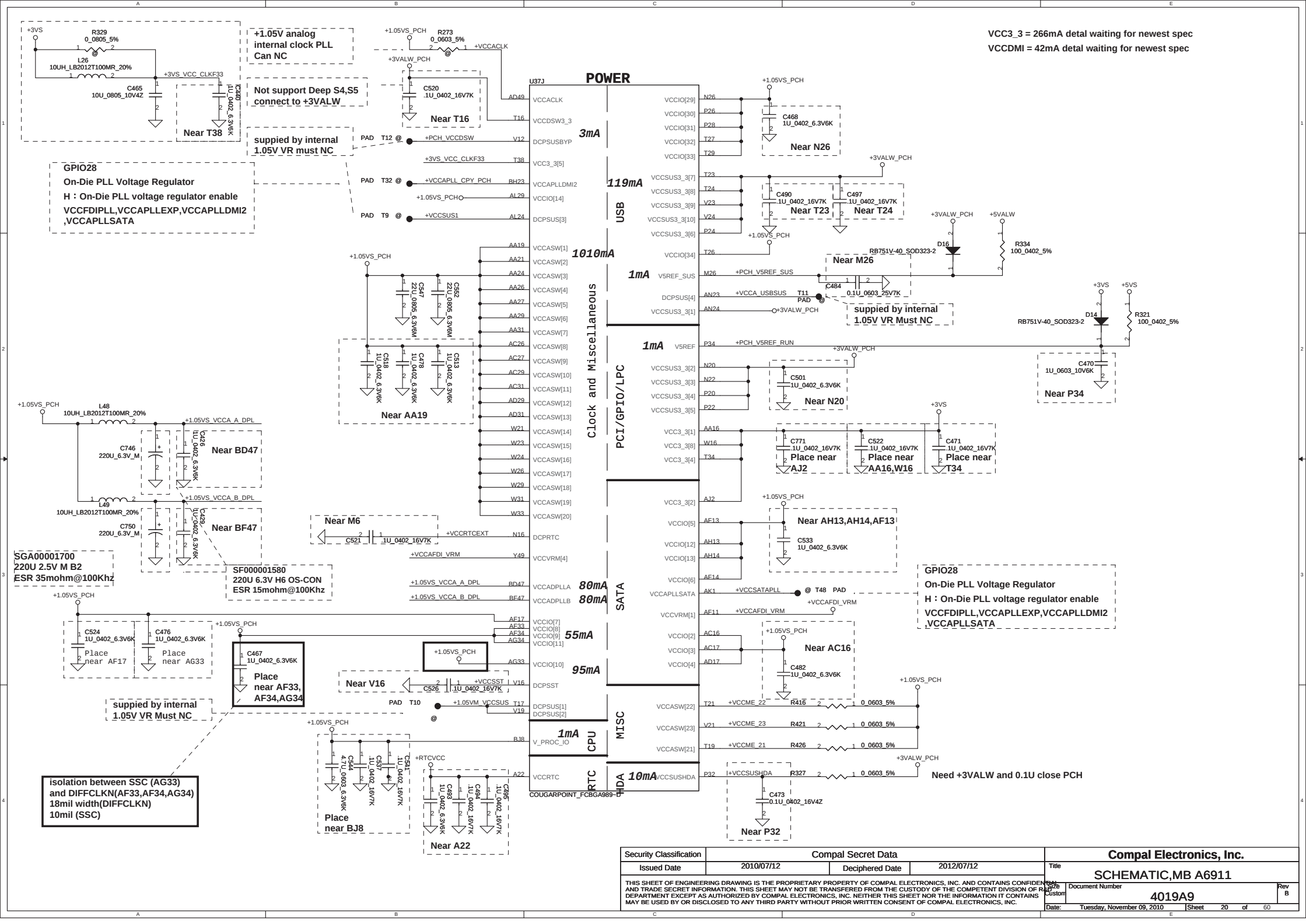
|                |     |      |
|----------------|-----|------|
| TACH4 / GPIO68 | NC1 | AH8  |
| TACH5 / GPIO69 | NC2 | AK11 |
| TACH6 / GPIO70 | NC3 | AH10 |
| TACH7 / GPIO71 | NC4 | AK10 |
|                | NC5 | P37  |

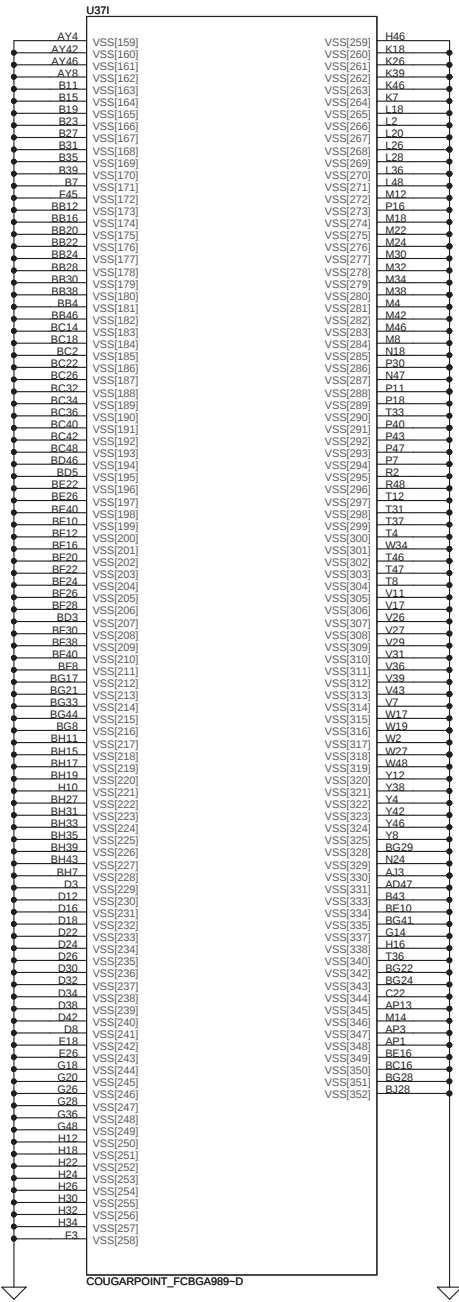
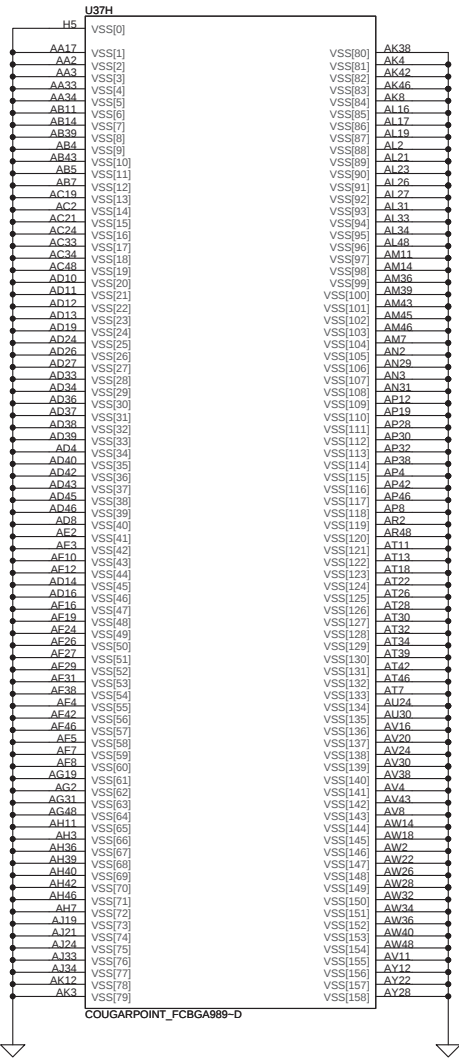
|             |      |      |     |
|-------------|------|------|-----|
| VSS_NCTF_15 | BG2  | @T38 | PAD |
| VSS_NCTF_16 | BG48 | @T24 | PAD |
| VSS_NCTF_17 | BH3  | @T37 | PAD |
| VSS_NCTF_18 | BH47 | @T19 | PAD |
| VSS_NCTF_19 | B14  | @T36 | PAD |
| VSS_NCTF_20 | B144 | @T31 | PAD |
| VSS_NCTF_21 | B145 | @T29 | PAD |
| VSS_NCTF_22 | B146 | @T25 | PAD |
| VSS_NCTF_23 | B15  | @T35 | PAD |
| VSS_NCTF_24 | B16  | @T34 | PAD |
| VSS_NCTF_25 | C2   | @T39 | PAD |
| VSS_NCTF_26 | C48  |      |     |
| VSS_NCTF_27 | D1   | @T40 | PAD |
| VSS_NCTF_28 | D49  | @T22 | PAD |
| VSS_NCTF_29 | F1   | @T41 | PAD |
| VSS_NCTF_30 | F49  |      |     |
| VSS_NCTF_31 | F1   | @T42 | PAD |
| VSS_NCTF_32 | F49  |      |     |

COUGARPOINT\_FCBGA989-D

| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       | Compal Secret Data |                 |            | Compal Electronics, Inc. |                            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|--------------------------|----------------------------|
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 2010/07/12         | Deciphered Date | 2012/07/12 | Title                    | SCHMATIC,MB A6911          |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Date:                    | Tuesday, November 09, 2010 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Sheet                    | 18 of 60                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Rev                      | B                          |







# GFX PCIE LANE REVERSAL

4 PEG\_GTX\_HRX\_N[0..15]  
4 PEG\_GTX\_HRX\_P[0..15]

4 PEG\_HTX\_C\_GRX\_N[0..15]  
4 PEG\_HTX\_C\_GRX\_P[0..15]



LCD PWM (pulse width modulated)  
output to adjust LCD brightness  
Active High ,external PD need

Controls panel digital power on/off.  
Active High ,external PD need

Display Port F config

Display Port E config

eDP  
DP3  
DP2  
DP1  
DP0

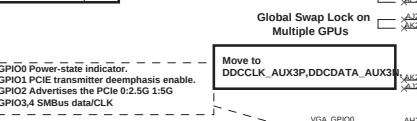
For M96, AH16 is NC  
For Boardway,Madison,Park, AH16 must connect to GND

17 PLTRST\_VGA#

SEYM@  
Park XT P/N : SA00003M570 (S IC 216-0774009 A11 PARK XT S3 631P C38)  
Madison Pro P/N : SA00003M360 ( S IC 216-0772000 MADISON PRO FCBGA 0FA)  
Seymour XT P/N: SA000047H00 (S IC 216-0809000 A11 SEYMOUR XT M2 0FH)

| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |  |  |  | Compal Secret Data         |  |                 |  | Compal Electronics, Inc. |  |       |  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|----------------------------|--|-----------------|--|--------------------------|--|-------|--|
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                   |  |  |  | 2010/07/12                 |  | Deciphered Date |  | 2012/07/12               |  | Title |  |
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| Date:                                                                                                                                                                                                                                                                                                                                                                                                                                                         |  |  |  | Tuesday, November 09, 2010 |  | Sheet           |  | 22                       |  | of 60 |  |

|                                                  |         |         |
|--------------------------------------------------|---------|---------|
| Don't have this strap on<br>Whistler and Seymour |         |         |
| NC on Park,<br>Robson and Seymour                |         |         |
| NC on Park, Robson                               |         |         |
|                                                  | VRAM B0 | VRAM B0 |
|                                                  | VRAM B1 | VRAM B1 |
|                                                  | VRAM B2 | VRAM B2 |
|                                                  | VRAM B3 | VRAM B3 |
| NC on Park,<br>Robson and Seymour                |         |         |



|  |                                             |               |     |
|--|---------------------------------------------|---------------|-----|
|  | GPIOs fast-power reduction:                 | VGA GPIO1     | A0  |
|  | HW control will cause display disturb       | VGA GPIO3     | A2  |
|  | should use SW method control                | VGA GPIO2     | A1  |
|  | GPIO6 voltage control signal. No use can NC | VGA GPIO4     | A3  |
|  | GPIO7 Controls backlight on/off             | DSP0 BK1-EN   | A4  |
|  | Active High, need external PD               | GPIO 0 ROMSS0 | A5  |
|  | GPIO12 High, GPIO 11:13-3-Config[2]         | GPIO 1 ROMSS1 | A6  |
|  | Config ROM type. GPIO has internal PD       | GPIO 2 ROMSS2 | A7  |
|  | GPIO6,15,16,20                              | GPIO 3 ROMSS3 | A8  |
|  | Voltage control signal                      | VGA GPIO23    | A9  |
|  | GPIO15 is no use can NC                     | GPIO VDD      | HPD |
|  | Thermal monitor interrupt                   | GPIO VDD      | AL  |
|  | Critical temperature fault                  | GPIO VDD      | AL  |
|  | Reserved                                    | GPIO VDD      | AL  |
|  | GPIO22 ROMSS4                               | GPIO VDD      | AL  |
|  | External BIOS/ODT inter PD                  | GPIO VDD      | AL  |
|  | Internal BIOS/ODT inter PD                  | GPIO VDD      | AL  |
|  | Internal Debug                              | GPIO VDD      | AL  |
|  | no use can floating                         | GPIO VDD      | AL  |

32 VGA, HDMI, DET

VGA, HDMI, DET HPD\_AK

1.8VSDGPU

R495 1V8V 2 499 0402 1%

R496 1V8V 2 249 0402 1%

C986 0.1uF 0402 16V47

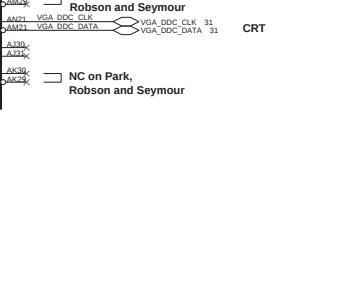
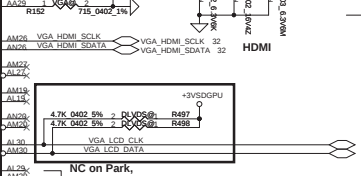
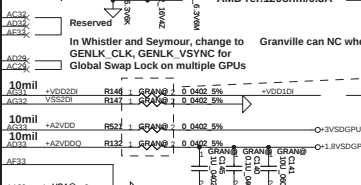
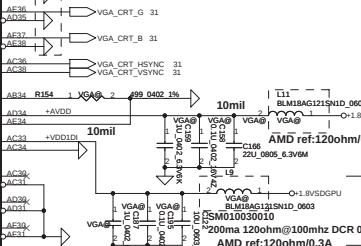
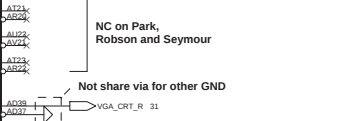
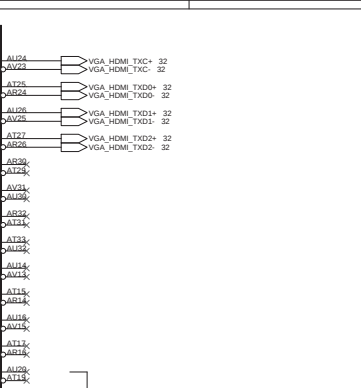
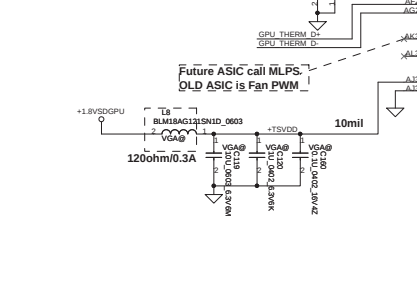
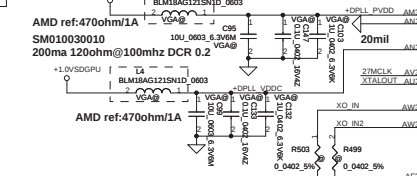
VGA\_B

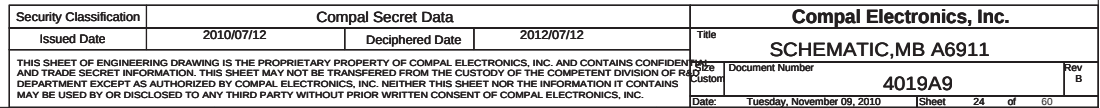
VGA\_VREF\_AH

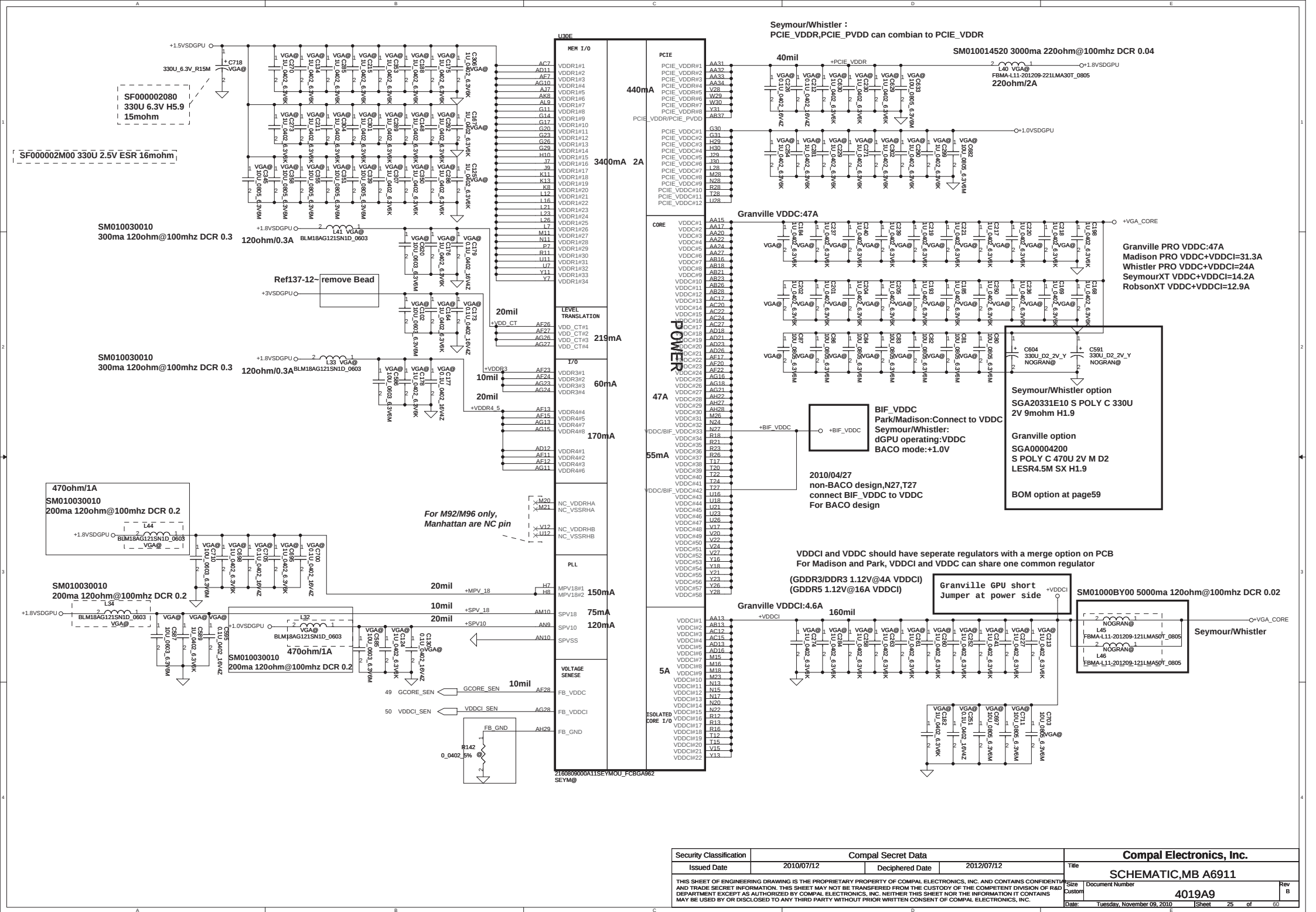
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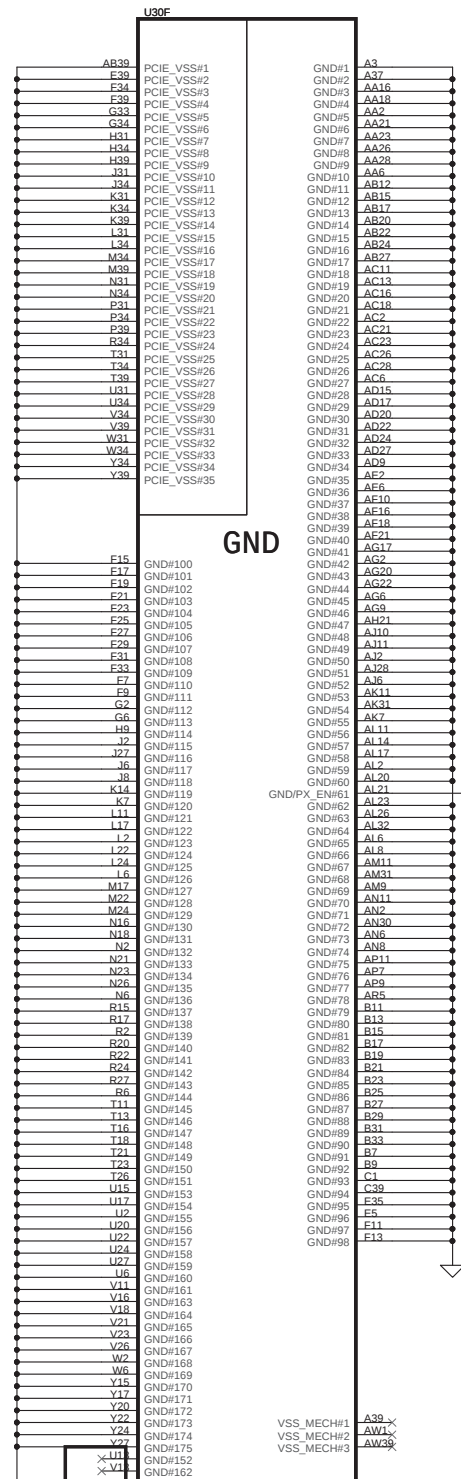
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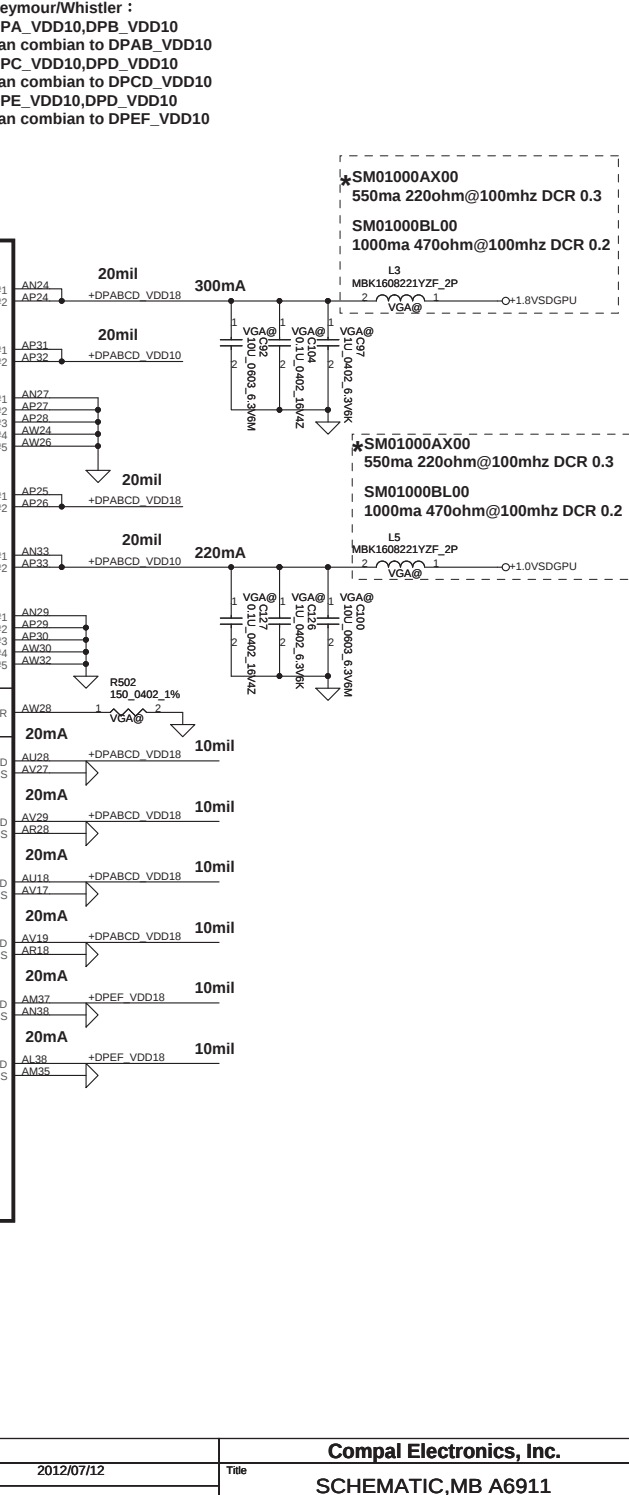
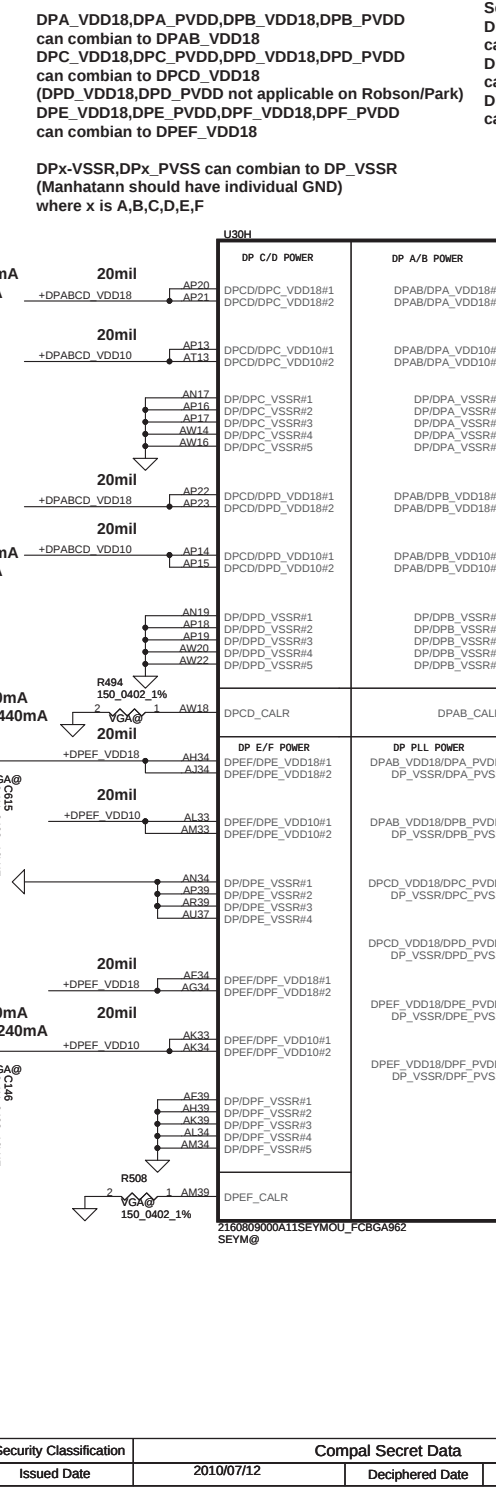
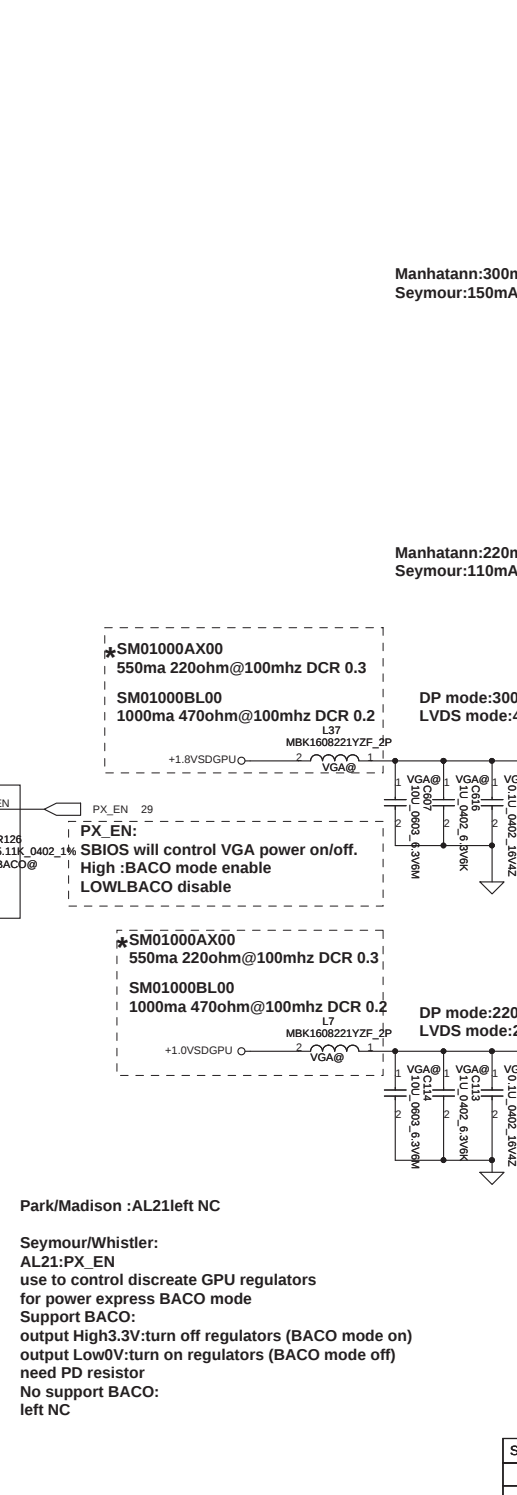




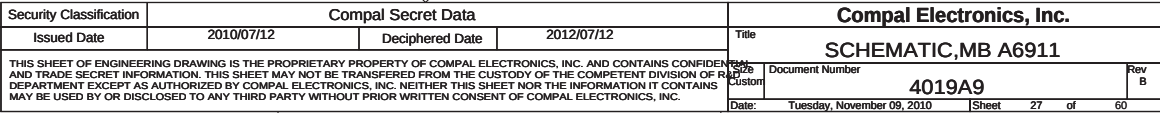


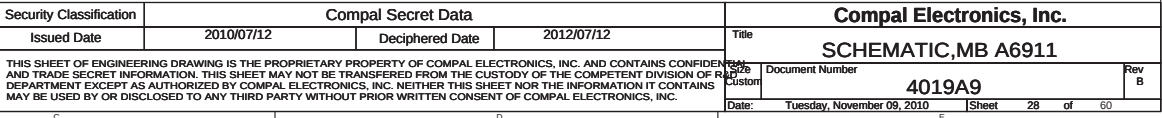


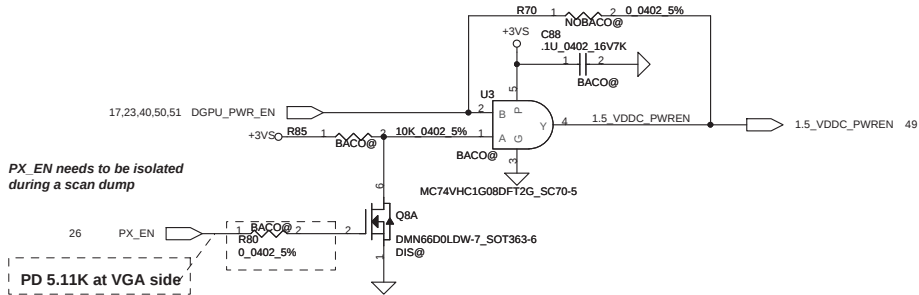
2160809000A11SEYMOU\_FCBGA962  
SEYM@  
REF137-13 update



| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                             |            | Compal Secret Data |            | Title                      |                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------|------------|----------------------------|----------------|
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 2010/07/12 | Deciphered Date    | 2012/07/12 | Compal Electronics, Inc.   |                |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |            |                    |            | 4019A9                     |                |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |            |                    |            | Tuesday, November 09, 2010 | Sheet 26 of 60 |



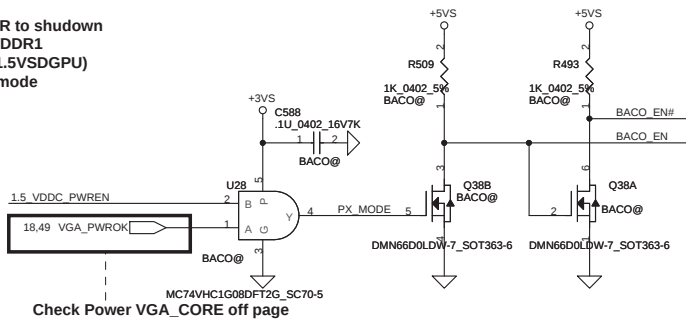




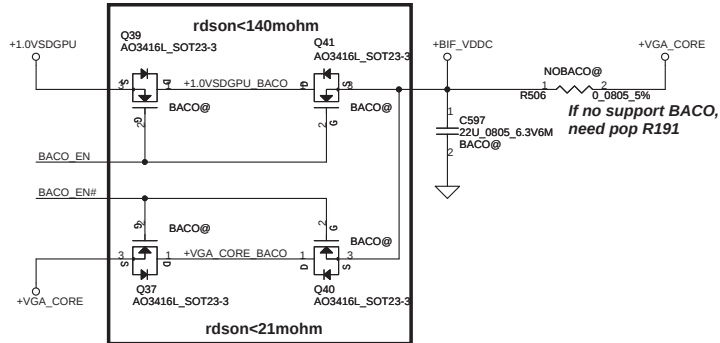
PX\_EN needs to be isolated during a scan dump

PX\_EN = 1, For BACO Mode  
PX\_EN = 0, For Normal Mode

PX\_EN:  
Connect to PWR to shutdown  
VDDC/VDDCI/VDDR1  
(VGA\_CORE, +1.5VSDGPU)  
High in BACO mode



Check Power VGA\_CORE off page



PX\_EN = 1, For BACO Mode  
BACO\_EN=0  
BACO\_EN#=1(5V)==> BIF\_VDDC=+1.0VSDGPU  
PX\_EN = 0, For Normal Mode  
BACO\_EN=1(5V) ==> BIF\_VDDC=VGA\_CORE  
BACO\_EN#=0

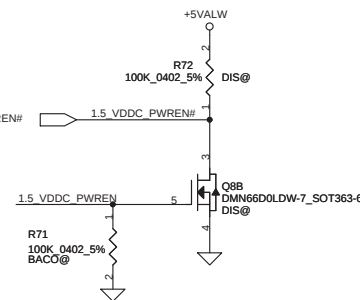
For the MOSFETs on the path of delivering  
PCIE\_VDDC(+1.0VSDGPU) to  
BIF\_VDDC Rds on of 140 mOhms or less is required.

For the MOSFETs on the path of delivering VGA\_CORE to  
BIF\_VDDC, Rds on of 21 mOhms or less is required.

BACO\_EN/BACO\_EN#:  
0: BACO Mode->BACO\_EN High->  
BIF\_VDDC=+1.0VSDGPU(N-MOS),VGA\_CORE(P-MOS)

1: Normal mode->BACO\_EN# High->  
BIF\_VDDC=+VGA\_CORE(N-MOS),VGA\_CORE(N-MOS)

BACO\_EN#=1 (BACO mode)  
BACO\_EN#=0 (Normal mode)  
BACO\_EN=0 (BACO mode)  
BACO\_EN=1 (Normal mode)



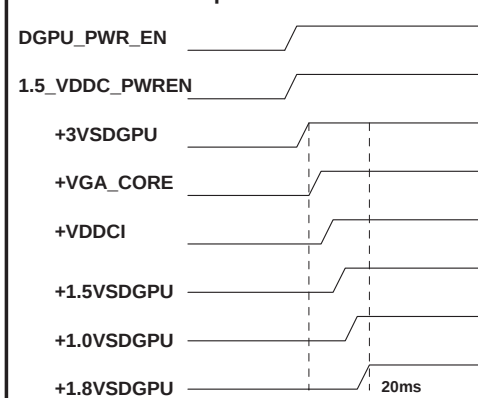
VGA Status Mapping table

|                | Normal mode | BACO mode  |
|----------------|-------------|------------|
| PX_EN          | 0           | 1          |
| 1.5_VDDC_PWREN | 1           | 0          |
| BACO_EN#       | 1           | 0          |
| BACO_EN        | 0           | 1          |
| +3VSDGPU       | ON          | ON         |
| +1.8VSDGPU     | ON          | ON         |
| +1.0VSDGPU     | ON          | ON         |
| +VGA_CORE      | ON          | OFF        |
| +1.5VSDGPU     | ON          | OFF        |
| +BIF_VDDC      | +VGA_CORE   | +1.0VSDGPU |

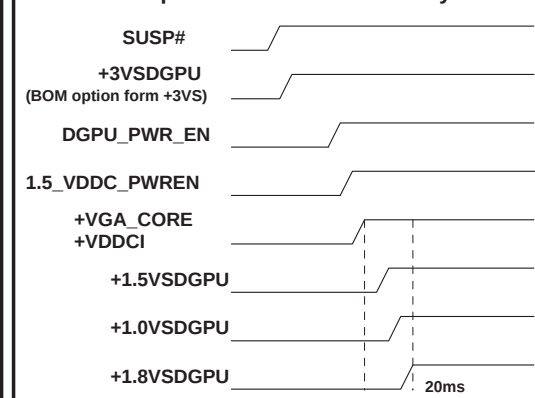
VGA Power Enable Signal Mapping table

|            | Graville    | Whistler and Seymour   |
|------------|-------------|------------------------|
| +3VSDGPU   | DGPU_PWR_EN | SUSP#                  |
| +1.8VSDGPU | DGPU_PWR_EN | DGPU_PWR_EN            |
| +1.0VSDGPU | DGPU_PWR_EN | DGPU_PWR_EN            |
| +VDDCI     | DGPU_PWR_EN | Combine with +VGA_CORE |
| +VGA_CORE  | DGPU_PWR_EN | 1.5_VDDC_PWREN         |
| +1.5VSDGPU | DGPU_PWR_EN | 1.5_VDDC_PWREN         |

Power Sequence of Graville

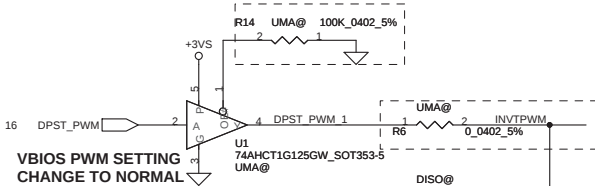
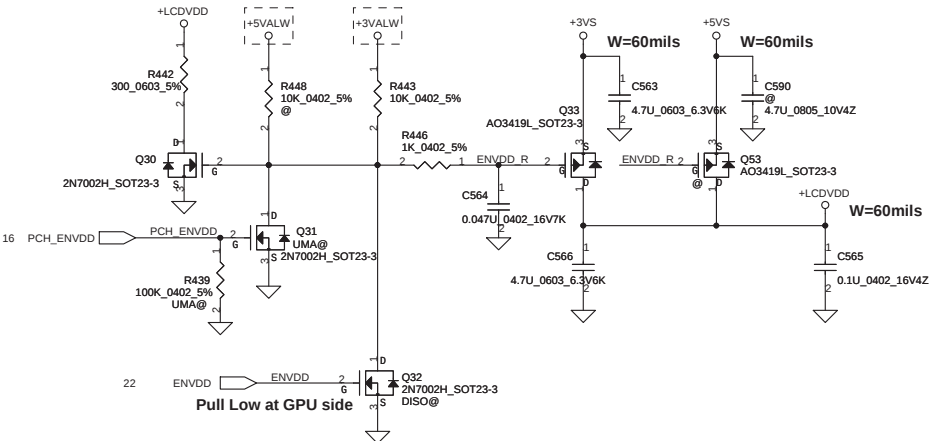


Power Sequence of Whistler and Seymour



100505 change to +3VALW  
101029 add +5VALW

## LCD POWER CIRCUIT



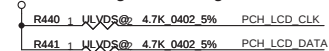
| UMA/DIS LVDS/eDP Mapping table |          |              |      | Panel Conn. |
|--------------------------------|----------|--------------|------|-------------|
| UMA                            | eDP      | DIS          | eDP  |             |
| LVDS                           |          | LVDS         |      |             |
| PCH_TXOUT0+                    |          | VGA_TXOUT0+  |      | TXOUT0+     |
| PCH_TXOUT0-                    |          | VGA_TXOUT0-  |      | TXOUT0-     |
| PCH_TXOUT1+                    | EDP_TXP1 | VGA_TXOUT1+  | DP1P | TXOUT1+     |
| PCH_TXOUT1-                    | EDP_TXN1 | VGA_TXOUT1-  | DP1N | TXOUT1-     |
| PCH_TXOUT2+                    | EDP_TXP0 | VGA_TXOUT2+  | DP0P | TXOUT2+     |
| PCH_TXOUT2-                    | EDP_TXN0 | VGA_TXOUT2-  | DP0N | TXOUT2-     |
| PCH_TXCLK+                     |          | VGA_TXCLK+   |      | TXCLK+      |
| PCH_TXCLK-                     |          | VGA_TXCLK-   |      | TXCLK-      |
| PCH_TZOUT0+                    |          | VGA_TZOUT0+  |      | TZOUT0+     |
| PCH_TZOUT0-                    |          | VGA_TZOUT0-  |      | TZOUT0-     |
| PCH_TZOUT1+                    |          | VGA_TZOUT1+  |      | TZOUT1+     |
| PCH_TZOUT1-                    |          | VGA_TZOUT1-  |      | TZOUT1-     |
| PCH_TZOUT2+                    |          | VGA_TZOUT2+  |      | TZOUT2+     |
| PCH_TZOUT2-                    |          | VGA_TZOUT2-  |      | TZOUT2-     |
| PCH_TZCLK+                     |          | VGA_TZCLK+   |      | TZCLK+      |
| PCH_TZCLK-                     |          | VGA_TZCLK-   |      | TZCLK-      |
| PCH_I2CC_SCL                   | EDP_AUXP | VGA_LCD_CLK  | AUXP | I2CC_SCL    |
| PCH_I2CC_SDA                   | EDP_AUXN | VGA_LCD_DATA | AUXN | I2CC_SDA    |

## UMA ONLY/Muxless

|                 |              |      |   |        |           |          |
|-----------------|--------------|------|---|--------|-----------|----------|
| 16 PCH_TXOUT0+  | PCH_TXOUT0+  | R452 | 1 | ULVDS@ | 0.0402 5% | TXOUT0+  |
| 16 PCH_TXOUT0-  | PCH_TXOUT0-  | R450 | 1 | ULVDS@ | 0.0402 5% | TXOUT0-  |
| 16 PCH_TXOUT1+  | PCH_TXOUT1+  | R455 | 1 | ULVDS@ | 0.0402 5% | TXOUT1+  |
| 16 PCH_TXOUT1-  | PCH_TXOUT1-  | R453 | 1 | ULVDS@ | 0.0402 5% | TXOUT1-  |
| 16 PCH_TXOUT2+  | PCH_TXOUT2+  | R456 | 1 | ULVDS@ | 0.0402 5% | TXOUT2+  |
| 16 PCH_TXOUT2-  | PCH_TXOUT2-  | R454 | 1 | ULVDS@ | 0.0402 5% | TXOUT2-  |
| 16 PCH_TXCLK+   | PCH_TXCLK+   | R458 | 1 | ULVDS@ | 0.0402 5% | TXCLK+   |
| 16 PCH_TXCLK-   | PCH_TXCLK-   | R457 | 1 | ULVDS@ | 0.0402 5% | TXCLK-   |
| 16 PCH_TZOUT0+  | PCH_TZOUT0+  | R460 | 1 | ULVDS@ | 0.0402 5% | TZOUT0+  |
| 16 PCH_TZOUT0-  | PCH_TZOUT0-  | R459 | 1 | ULVDS@ | 0.0402 5% | TZOUT0-  |
| 16 PCH_TZOUT1+  | PCH_TZOUT1+  | R462 | 1 | ULVDS@ | 0.0402 5% | TZOUT1+  |
| 16 PCH_TZOUT1-  | PCH_TZOUT1-  | R461 | 1 | ULVDS@ | 0.0402 5% | TZOUT1-  |
| 16 PCH_TZOUT2+  | PCH_TZOUT2+  | R465 | 1 | ULVDS@ | 0.0402 5% | TZOUT2+  |
| 16 PCH_TZOUT2-  | PCH_TZOUT2-  | R463 | 1 | ULVDS@ | 0.0402 5% | TZOUT2-  |
| 16 PCH_TZCLK+   | PCH_TZCLK+   | R467 | 1 | ULVDS@ | 0.0402 5% | TZCLK+   |
| 16 PCH_TZCLK-   | PCH_TZCLK-   | R466 | 1 | ULVDS@ | 0.0402 5% | TZCLK-   |
| 16 PCH_LCD_CLK  | PCH_LCD_CLK  | R444 | 1 | ULVDS@ | 0.0402 5% | I2CC_SCL |
| 16 PCH_LCD_DATA | PCH_LCD_DATA | R445 | 1 | ULVDS@ | 0.0402 5% | I2CC_SDA |

5/4 PCH\_LCD\_CLK & PCH\_LCD\_DATA

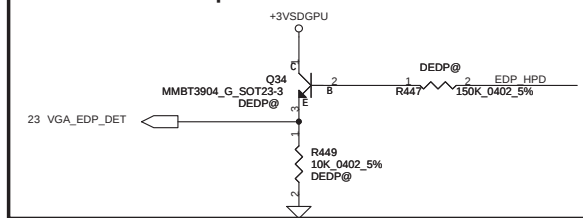
Pull high 2.2K change to 4.7K



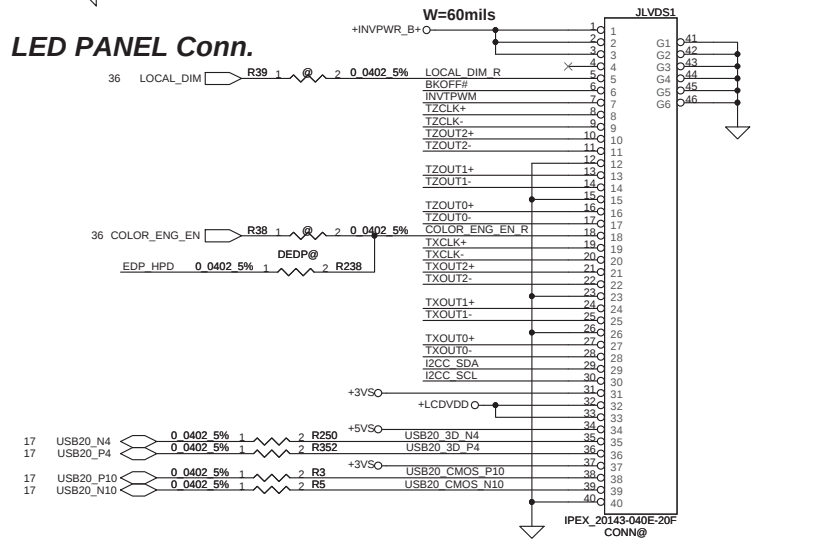
## Discrete ONLY

|                 |              |     |   |        |           |          |
|-----------------|--------------|-----|---|--------|-----------|----------|
| 22 VGA_TXOUT0+  | VGA_TXOUT0+  | R13 | 1 | ULVDS@ | 0.0402 5% | TXOUT0+  |
| 22 VGA_TXOUT0-  | VGA_TXOUT0-  | R12 | 1 | ULVDS@ | 0.0402 5% | TXOUT0-  |
| 22 VGA_TXOUT1+  | VGA_TXOUT1+  | R23 | 1 | ULVDS@ | 0.0402 5% | TXOUT1+  |
| 22 VGA_TXOUT1-  | VGA_TXOUT1-  | R17 | 1 | ULVDS@ | 0.0402 5% | TXOUT1-  |
| 22 VGA_TXOUT2+  | VGA_TXOUT2+  | R24 | 1 | ULVDS@ | 0.0402 5% | TXOUT2+  |
| 22 VGA_TXOUT2-  | VGA_TXOUT2-  | R22 | 1 | ULVDS@ | 0.0402 5% | TXOUT2-  |
| 22 VGA_TXCLK+   | VGA_TXCLK+   | R26 | 1 | ULVDS@ | 0.0402 5% | TXCLK+   |
| 22 VGA_TXCLK-   | VGA_TXCLK-   | R25 | 1 | ULVDS@ | 0.0402 5% | TXCLK-   |
| 22 VGA_TZOUT0+  | VGA_TZOUT0+  | R28 | 1 | ULVDS@ | 0.0402 5% | TZOUT0+  |
| 22 VGA_TZOUT0-  | VGA_TZOUT0-  | R27 | 1 | ULVDS@ | 0.0402 5% | TZOUT0-  |
| 22 VGA_TZOUT1+  | VGA_TZOUT1+  | R30 | 1 | ULVDS@ | 0.0402 5% | TZOUT1+  |
| 22 VGA_TZOUT1-  | VGA_TZOUT1-  | R29 | 1 | ULVDS@ | 0.0402 5% | TZOUT1-  |
| 22 VGA_TZOUT2+  | VGA_TZOUT2+  | R32 | 1 | ULVDS@ | 0.0402 5% | TZOUT2+  |
| 22 VGA_TZOUT2-  | VGA_TZOUT2-  | R31 | 1 | ULVDS@ | 0.0402 5% | TZOUT2-  |
| 22 VGA_TZCLK+   | VGA_TZCLK+   | R34 | 1 | ULVDS@ | 0.0402 5% | TZCLK+   |
| 22 VGA_TZCLK-   | VGA_TZCLK-   | R33 | 1 | ULVDS@ | 0.0402 5% | TZCLK-   |
| 23 VGA_LCD_CLK  | VGA_LCD_CLK  | R9  | 1 | ULVDS@ | 0.0402 5% | I2CC_SCL |
| 23 VGA_LCD_DATA | VGA_LCD_DATA | R7  | 1 | ULVDS@ | 0.0402 5% | I2CC_SDA |

## BOM option for Discrete eDP

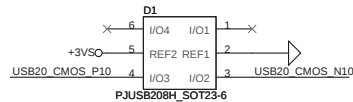
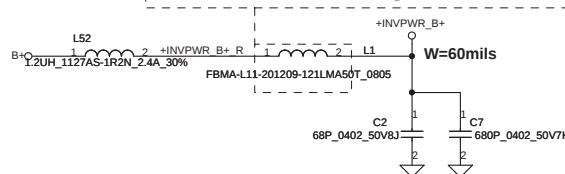


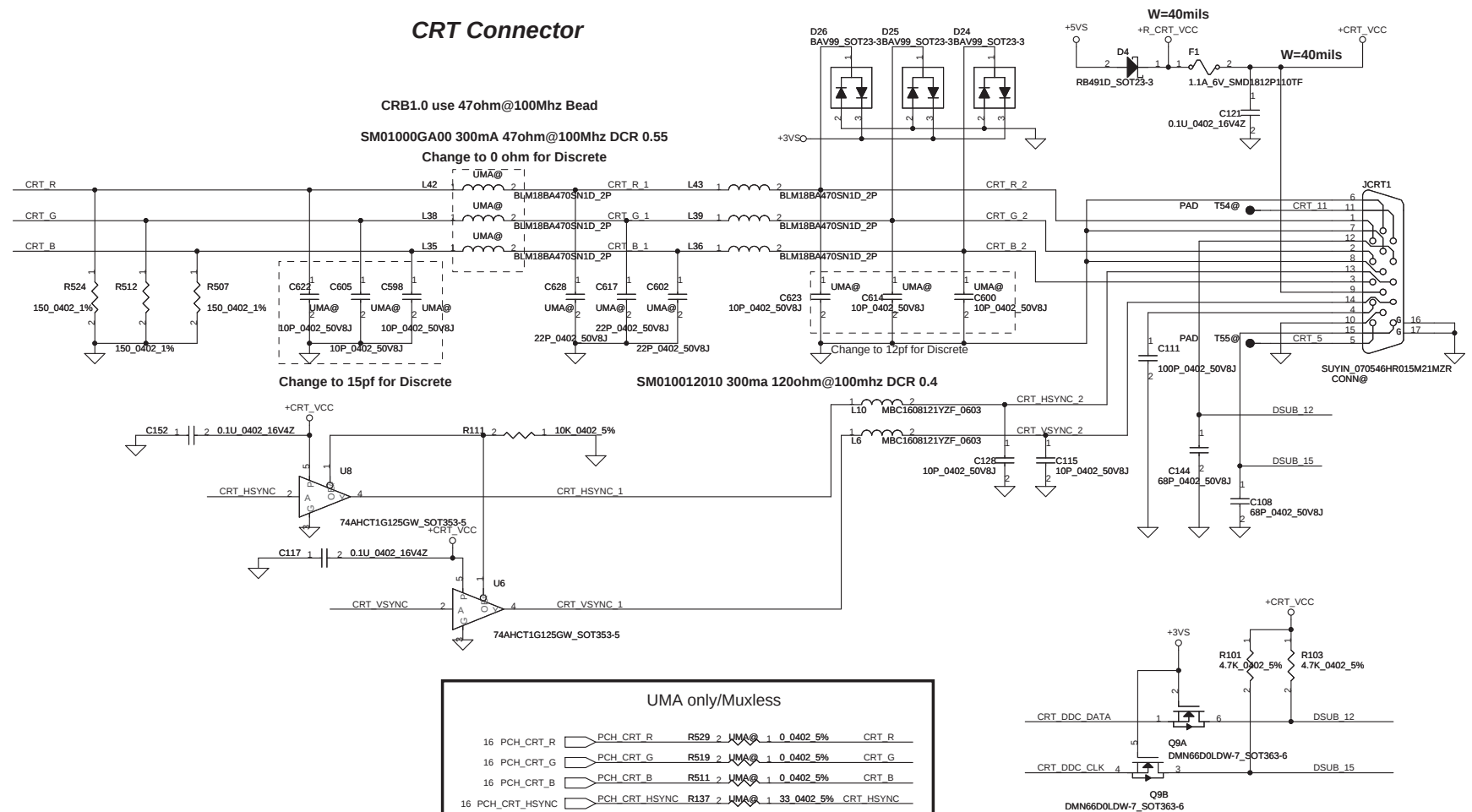
## LED PANEL Conn.

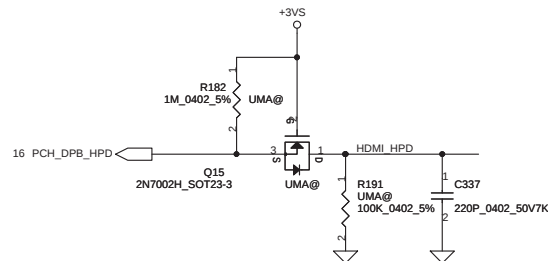
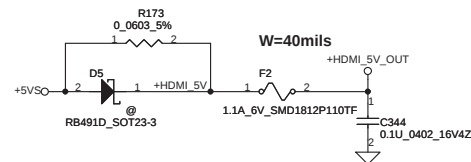


SM010014520 3000ma 220ohm@100mhz DCR 0.04

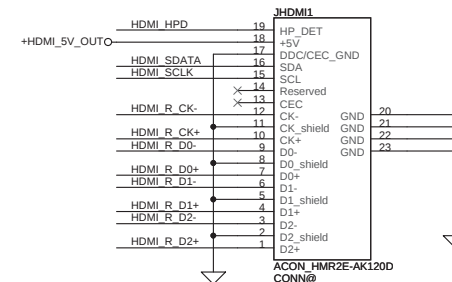
SM01000BY00 5000ma 120ohm@100mhz DCR 0.02



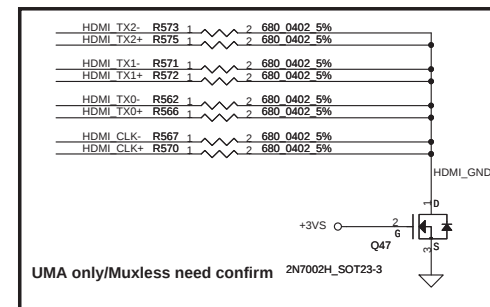
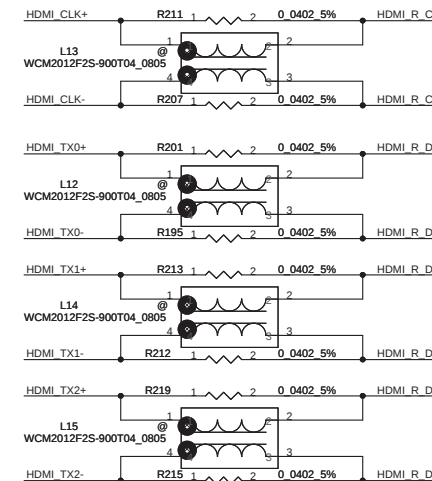




### HDMI connector

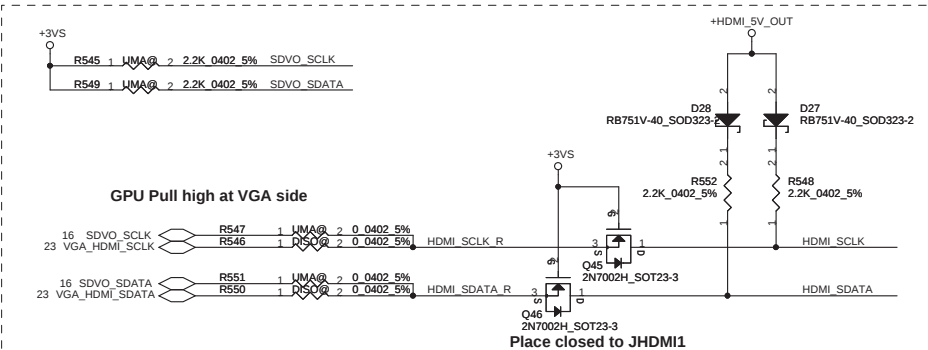
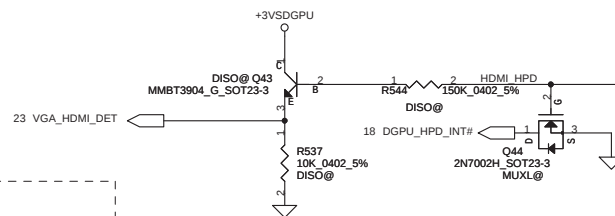


SM070001310 400ma 90ohm@100mhz DCR 0.3



|             |  |               |             |                  |           |
|-------------|--|---------------|-------------|------------------|-----------|
| UMA/Muxless |  | 16 PCH_DPB_N0 | C364 UMA@ 2 | 1 .1U 0402 16V7K | HDMI TX2- |
|             |  | 16 PCH_DPB_P0 | C368 UMA@ 2 | 1 .1U 0402 16V7K | HDMI TX2+ |
|             |  | 16 PCH_DPB_N1 | C357 UMA@ 2 | 1 .1U 0402 16V7K | HDMI TX1- |
|             |  | 16 PCH_DPB_P1 | C359 UMA@ 2 | 1 .1U 0402 16V7K | HDMI TX1+ |
|             |  | 16 PCH_DPB_N2 | C347 UMA@ 2 | 1 .1U 0402 16V7K | HDMI TX0- |
|             |  | 16 PCH_DPB_P2 | C349 UMA@ 2 | 1 .1U 0402 16V7K | HDMI TX0+ |
|             |  | 16 PCH_DPB_N3 | C352 UMA@ 2 | 1 .1U 0402 16V7K | HDMI CLK- |
|             |  | 16 PCH_DPB_P3 | C356 UMA@ 2 | 1 .1U 0402 16V7K | HDMI CLK+ |

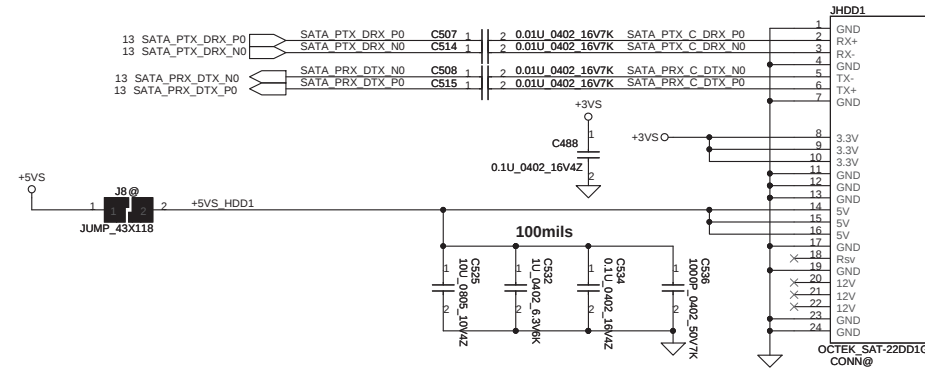
|          |  |                   |              |                  |           |
|----------|--|-------------------|--------------|------------------|-----------|
| DIS Only |  | 23 VGA_HDMI_TXD2- | C716 DISO@ 2 | 1 .1U 0402 16V7K | HDMI TX2- |
|          |  | 23 VGA_HDMI_TXD2+ | C717 DISO@ 2 | 1 .1U 0402 16V7K | HDMI TX2+ |
|          |  | 23 VGA_HDMI_TXD1- | C714 DISO@ 2 | 1 .1U 0402 16V7K | HDMI TX1- |
|          |  | 23 VGA_HDMI_TXD1+ | C715 DISO@ 2 | 1 .1U 0402 16V7K | HDMI TX1+ |
|          |  | 23 VGA_HDMI_TXD0- | C704 DISO@ 2 | 1 .1U 0402 16V7K | HDMI TX0- |
|          |  | 23 VGA_HDMI_TXD0+ | C709 DISO@ 2 | 1 .1U 0402 16V7K | HDMI TX0+ |
|          |  | 23 VGA_HDMI_TXC-  | C712 DISO@ 2 | 1 .1U 0402 16V7K | HDMI CLK- |
|          |  | 23 VGA_HDMI_TXC+  | C713 DISO@ 2 | 1 .1U 0402 16V7K | HDMI CLK+ |



|                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |                    |            |                          |                            |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------|------------|--------------------------|----------------------------|
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| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 2010/07/12 | Deciphered Date    | 2012/07/12 | Title                    | SCHEMATIC,MB A6911         |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |                    |            | Date:                    | Tuesday, November 09, 2010 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |                    |            | Sheet                    | 32 of 60                   |

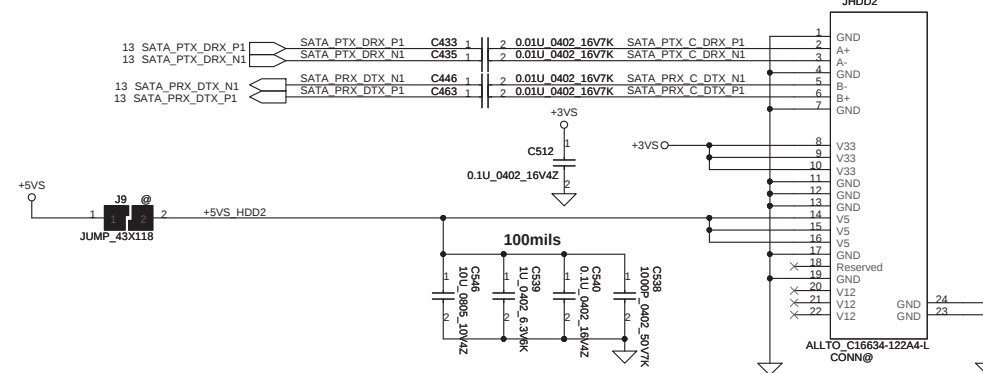
## SATA HDD1 Conn.

CL 2.9 mm

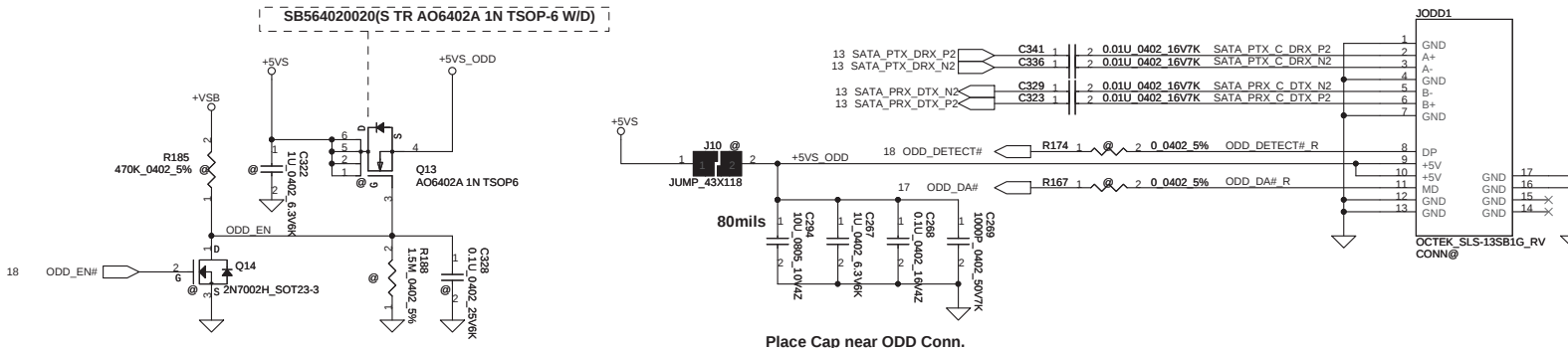


## SATA HDD2 Conn.

CL 4.4 mm



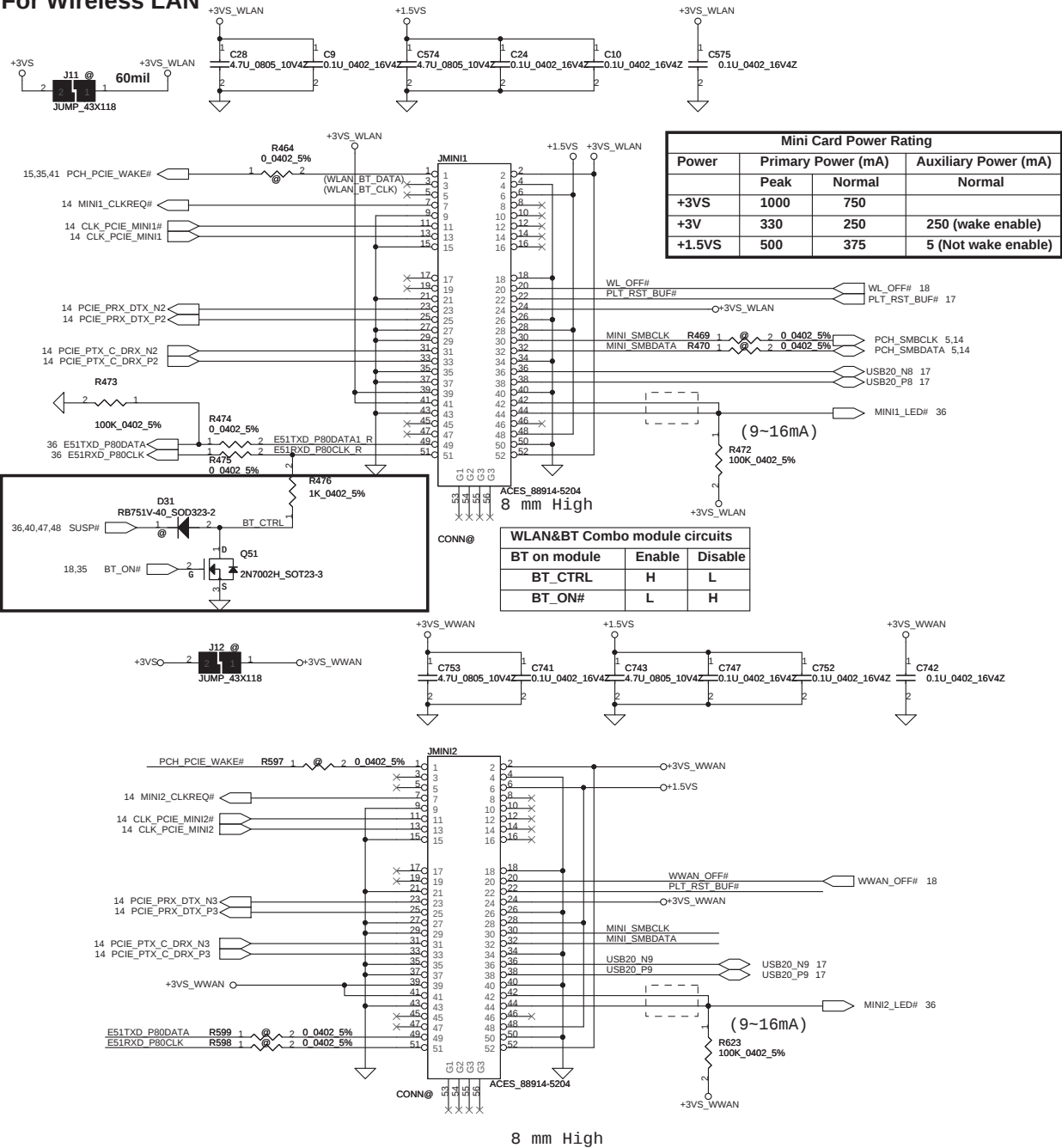
## SATA ODD Conn.



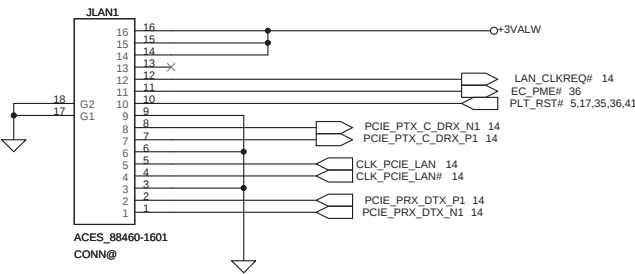
Place Cap near ODD Conn.

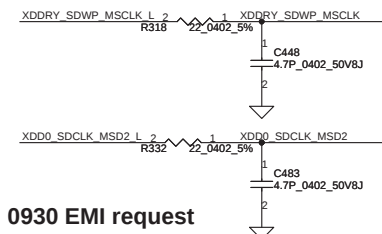
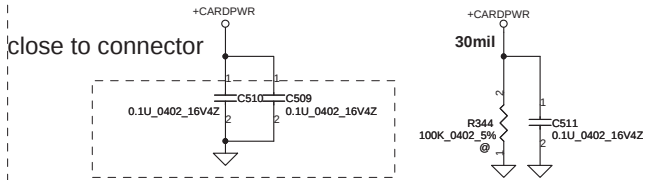
| Security Classification                                                                                                                                                                                                                                                               |            | Compal Secret Data |            | Compal Electronics, Inc. |                            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------|------------|--------------------------|----------------------------|
| Issued Date                                                                                                                                                                                                                                                                           | 2010/07/12 | Deciphered Date    | 2012/07/12 | Title                    | SCHEMATIC,MB A6911         |
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|                                                                                                                                                                                                                                                                                       |            |                    |            | Date:                    | Tuesday, November 09, 2010 |
|                                                                                                                                                                                                                                                                                       |            |                    |            | Sheet                    | 33 of 60                   |
|                                                                                                                                                                                                                                                                                       |            |                    |            | Rev                      | B                          |

For Wireless LAN

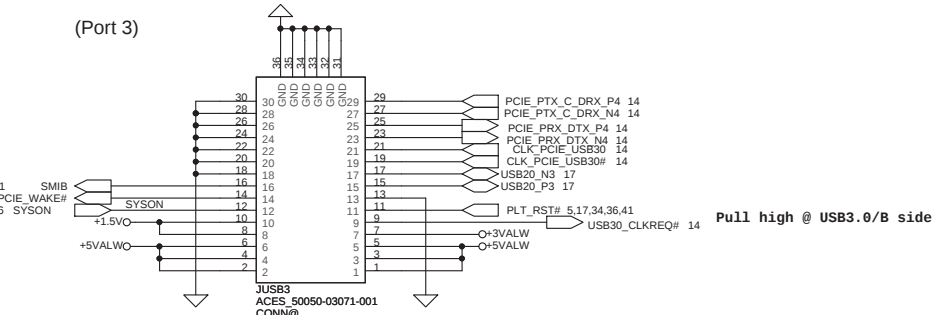
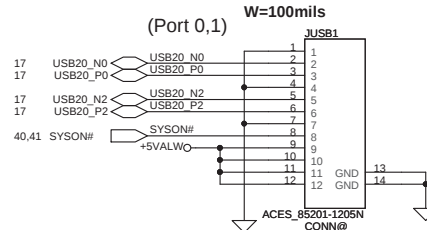


LAN CONN. LS-6912P

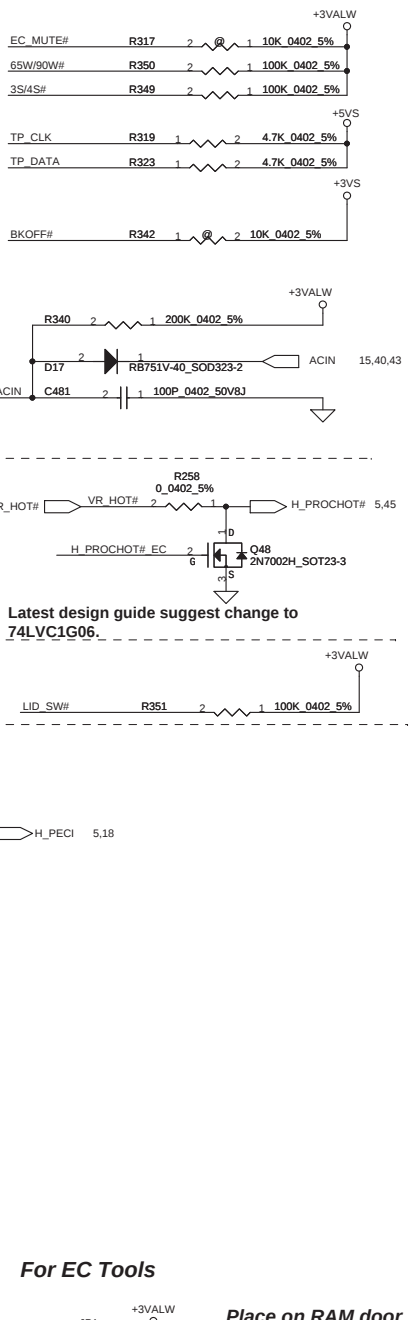
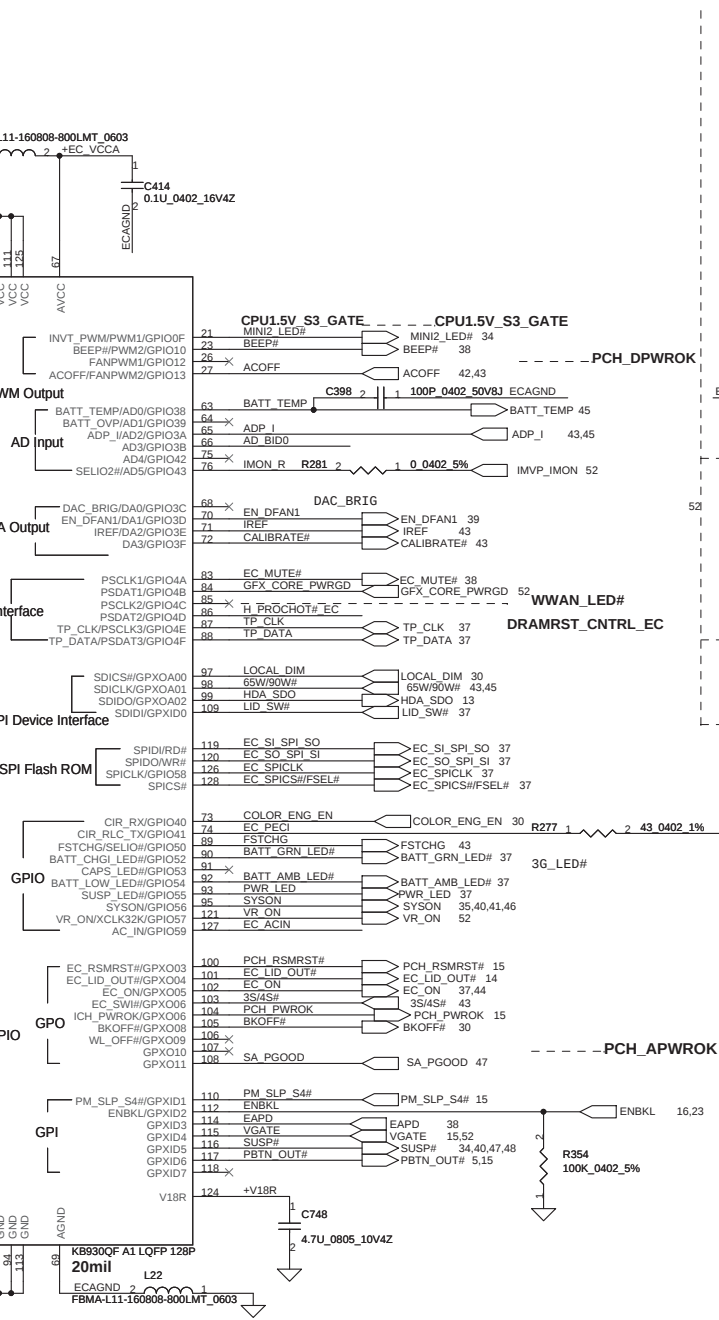
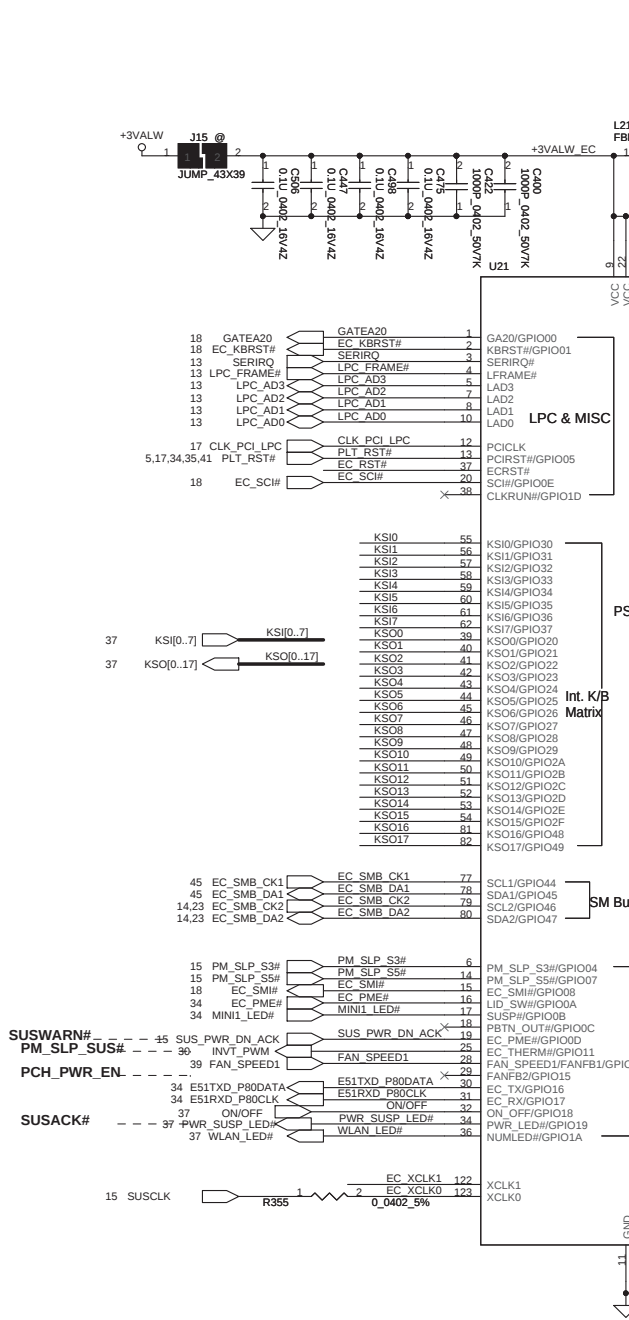
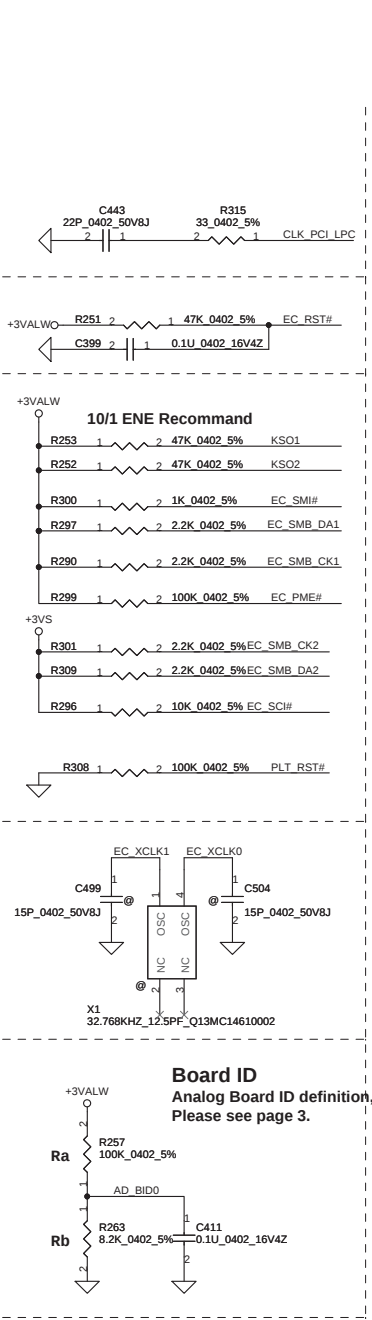


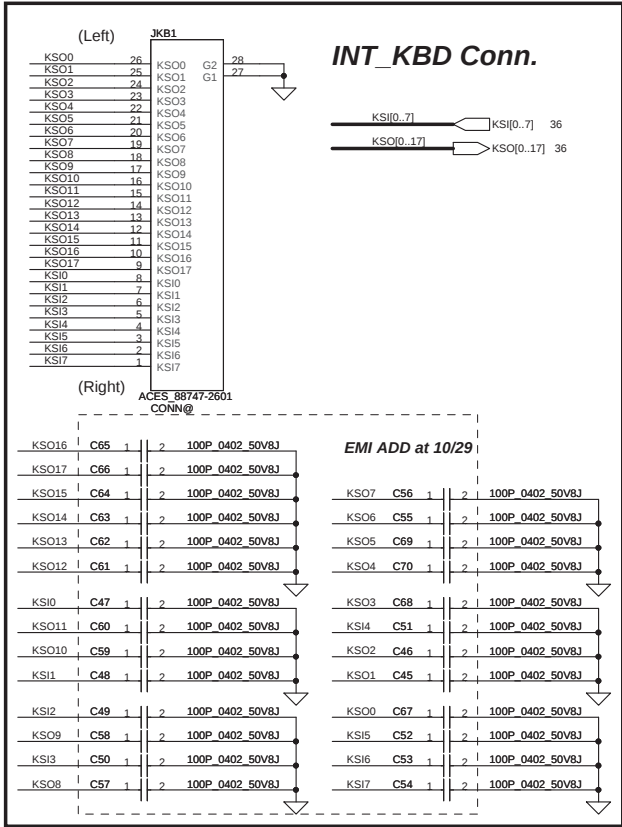
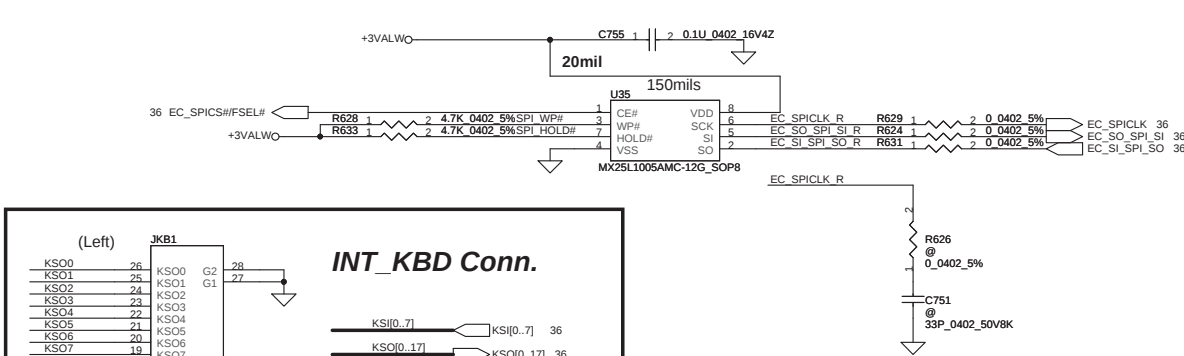


## Share Pin

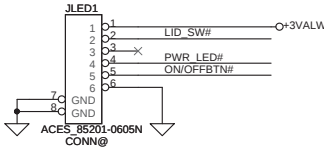


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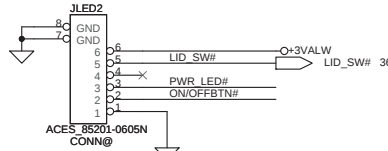




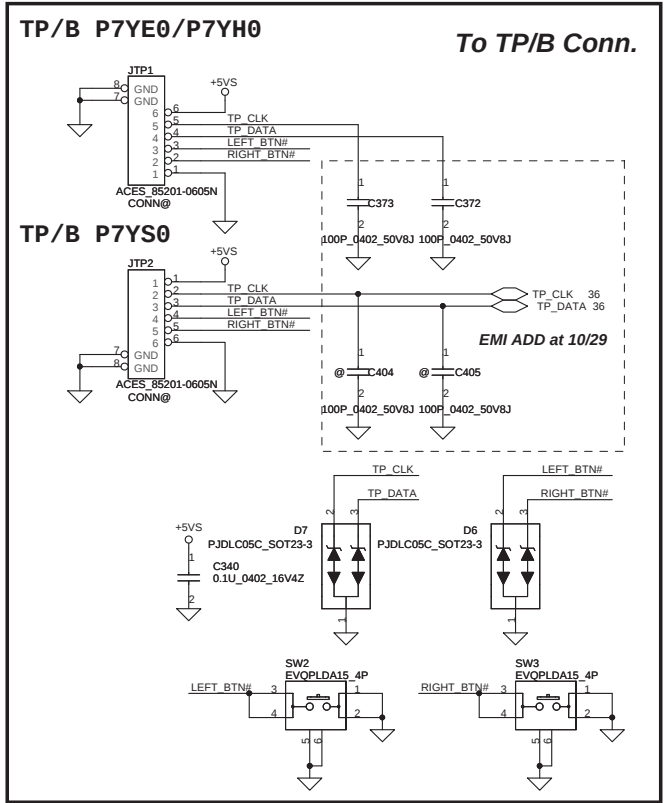
### LED/B P7YE0/P7YH0 LS-6913P



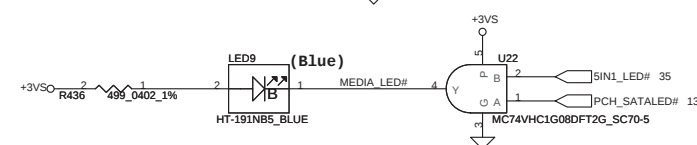
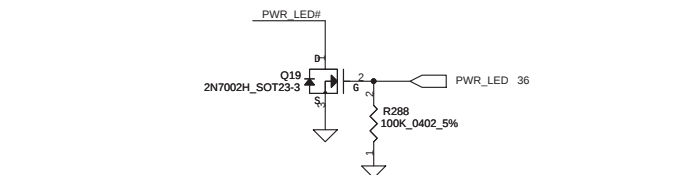
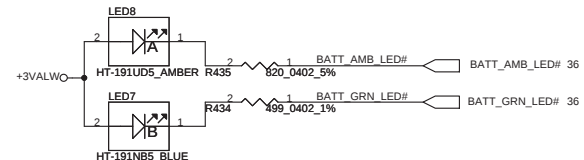
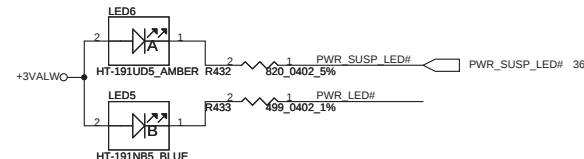
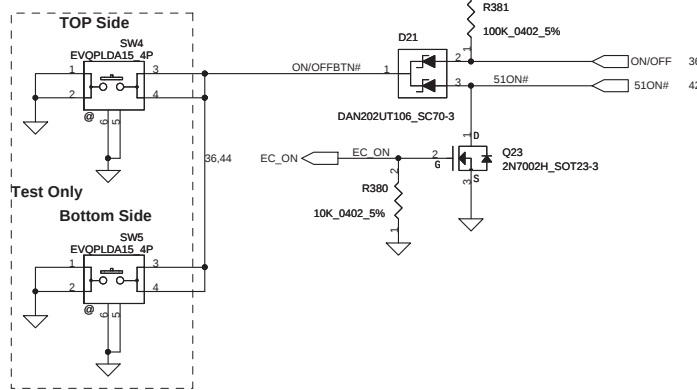
### LED/B P7YS0 LS-6913P



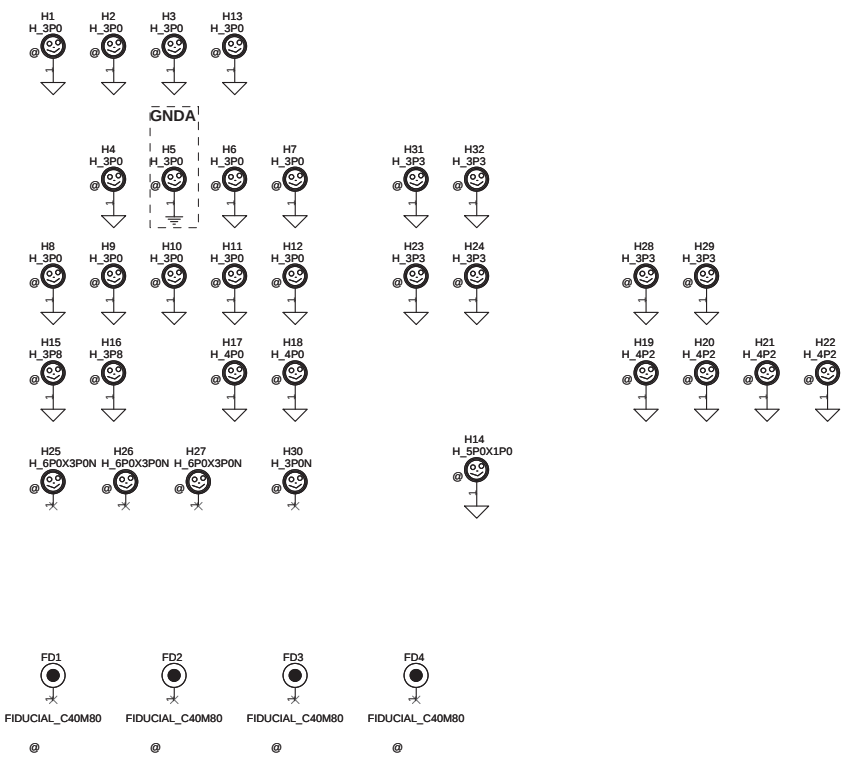
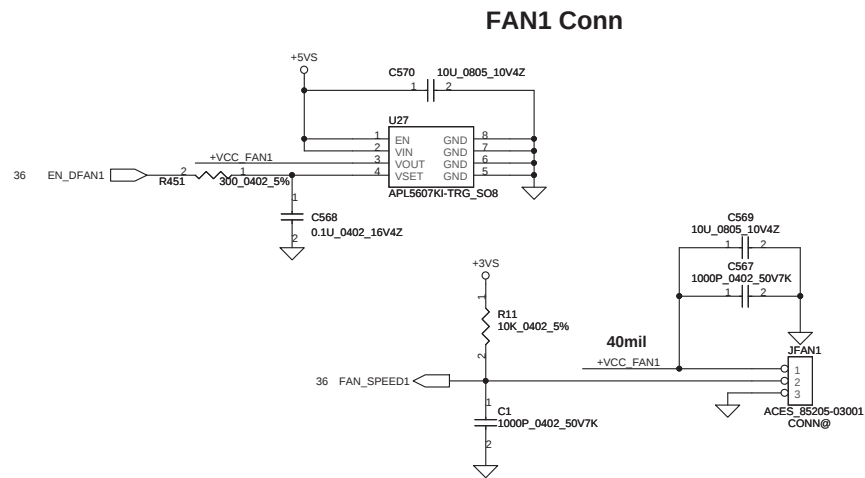
| LED Status  | Power/SUS |       | Battery |        | 3G/WLAN |       | BlueTooth | ACIN |
|-------------|-----------|-------|---------|--------|---------|-------|-----------|------|
|             | ON        | SUS   | Full    | Charge | 3G      | WLAN  |           |      |
| NEW70/80/90 | Blue      | Amber | Blue    |        | Blue    | Amber |           |      |



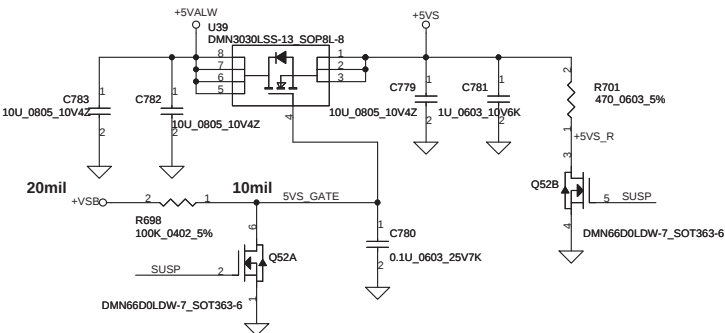
### Power Button ON/OFF switch



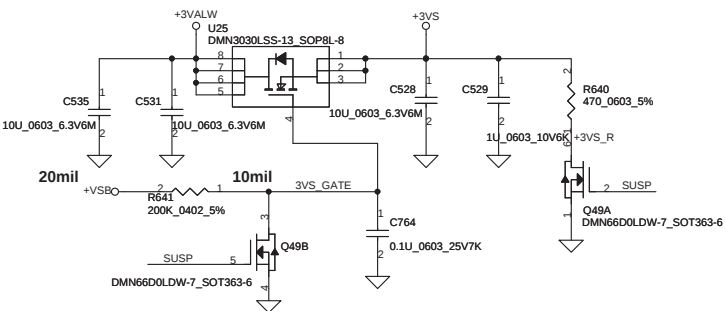




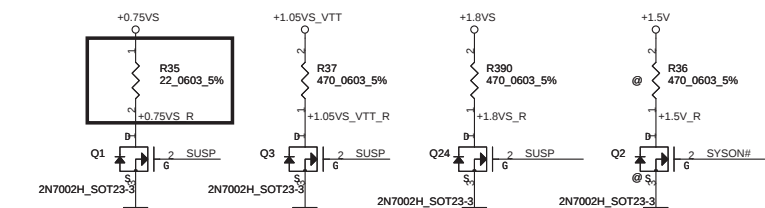
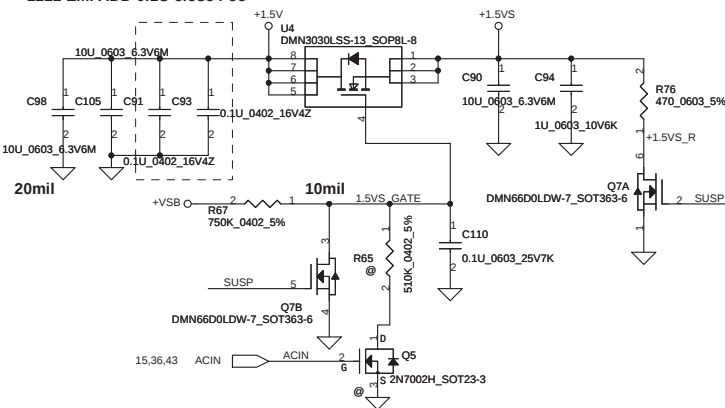
### +5VALW TO +5VS



### +3VALW TO +3VS

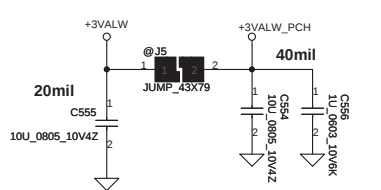


### +1.5V to +1.5VS

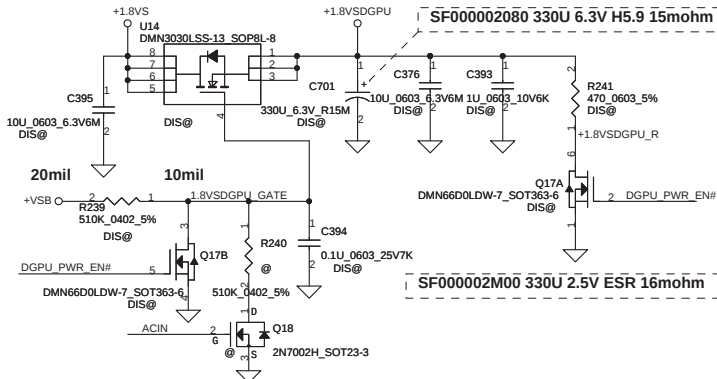


2009/08/14  
CP\_S3PowerReduction  
WhitePaper\_Rev0.9  
0.75VS speed up discharge

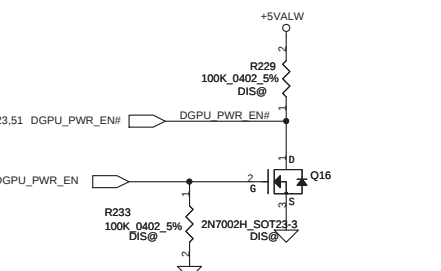
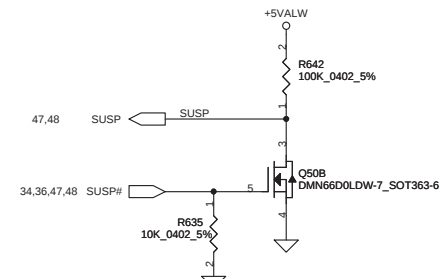
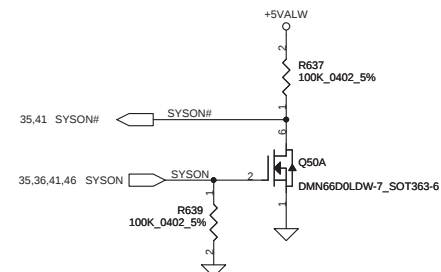
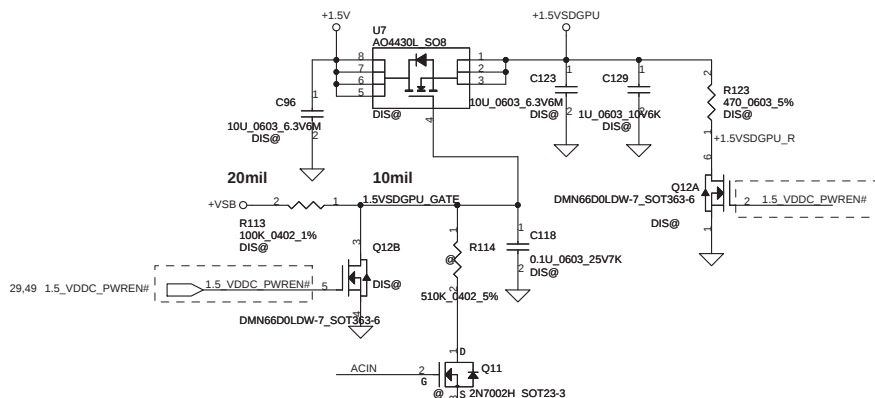
### +3VALW TO +3VALW(PCH AUX Power)



### +1.8VS to +1.8VSDGPU for GPU

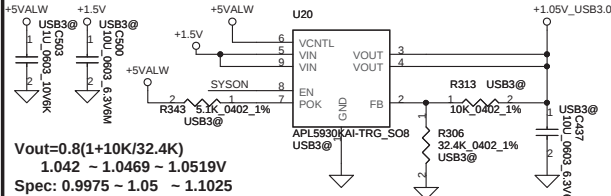


### +1.5V to +1.5VSDGPU for GPU

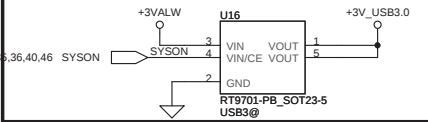


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|                         |  |  |  |                    |  |                 |  |                          |  | 4019A9                           |  |
|                         |  |  |  |                    |  |                 |  |                          |  | Rev B                            |  |
|                         |  |  |  |                    |  |                 |  |                          |  | Date: Tuesday, November 09, 2010 |  |
|                         |  |  |  |                    |  |                 |  |                          |  | Sheet 40 of 60                   |  |

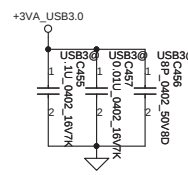
## +1.5V to +1.05V Transfer



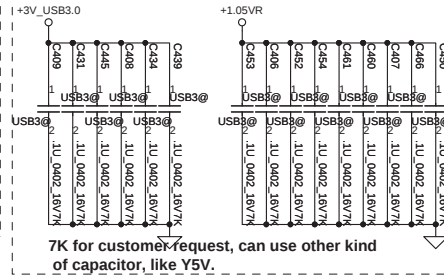
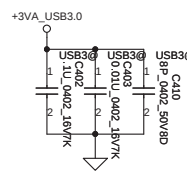
## +3VALW to +3V Transfer



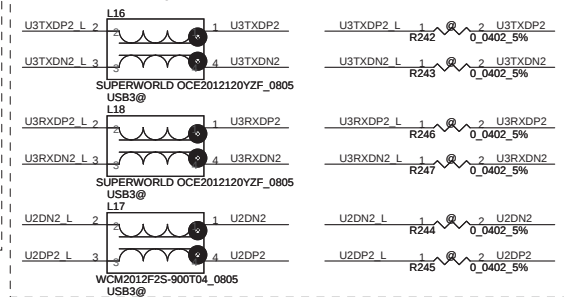
## Close to U41.D7



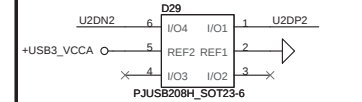
## Close to U41.P13



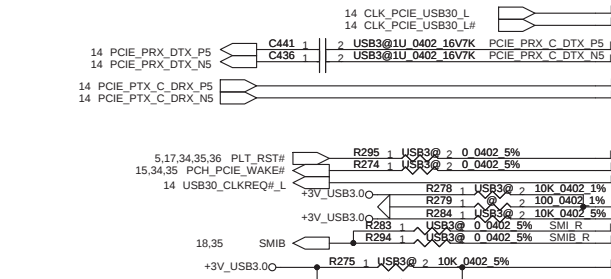
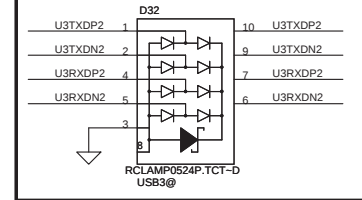
## For EMI request



## For USB2.0 ESD diode



## For USB3.0 ESD diode



SPEC Max: +3V---200mA; +1.05V---800mA

Idle mode: 0.489W

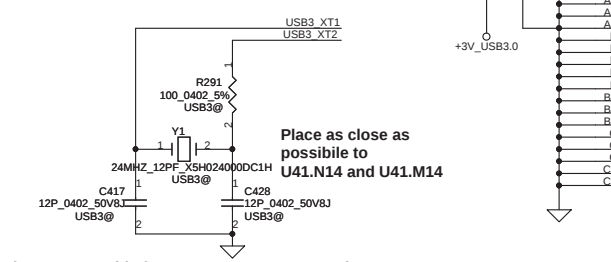
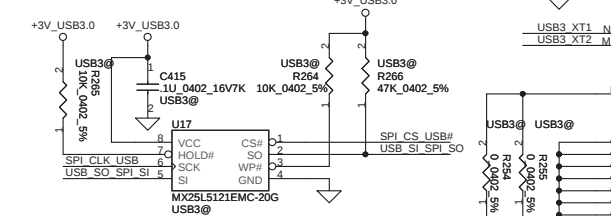
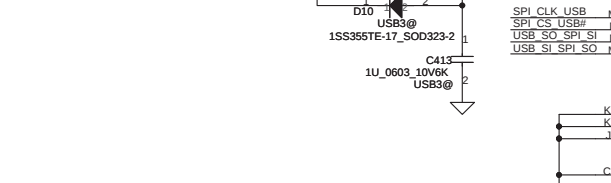
+3V---43mA; +1.05V---328mA

D3 mode: 0.066W

+3V---5.4mA; +1.05V---45mA

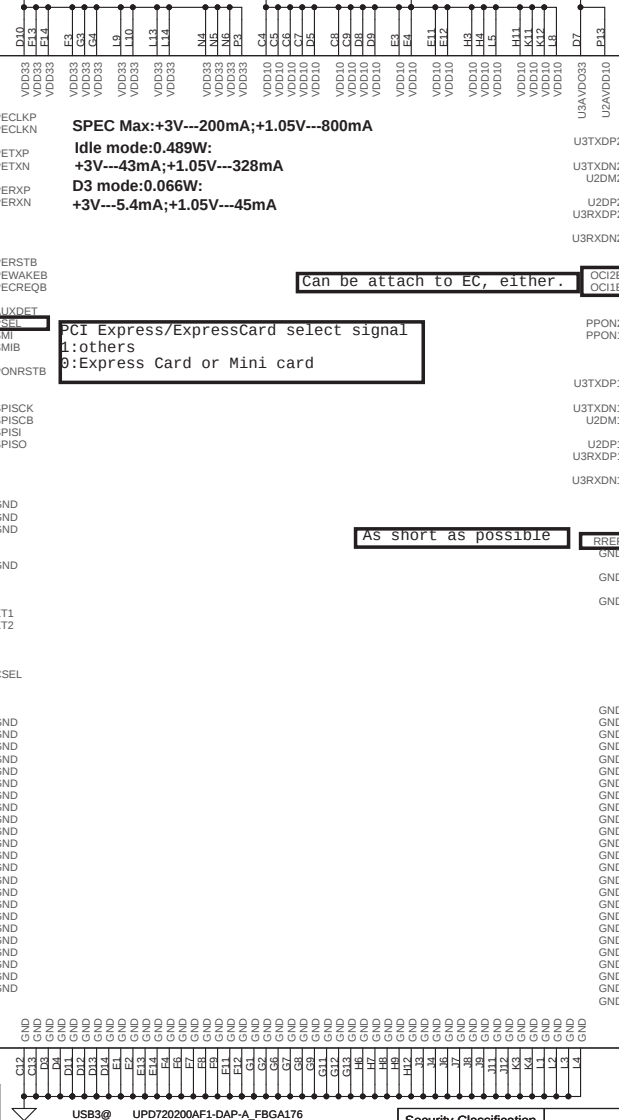
Can be attach to EC, either.

PCI Express/ExpressCard select signal  
1: others  
0: Express Card or Mini card

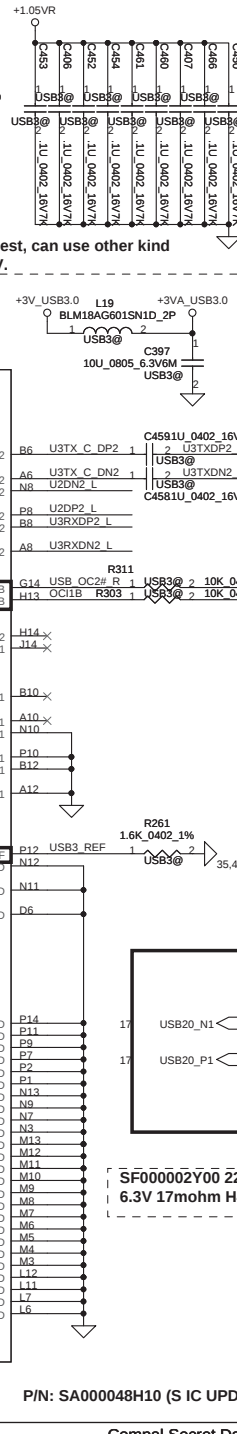


Pin compare table for support USB remote wakeup or not

|                               | AUXDET(Pin J2)         | CSEL(Pin P6)       | CLK                                                               |
|-------------------------------|------------------------|--------------------|-------------------------------------------------------------------|
| Support USB remote wakeup     | pull high 10k to VDD33 | Tied to GND        | Must use 24MHz crystal: mount Y5,R816,C879,C880                   |
| Not support USB remote wakeup | Tied to GND            | pull high to VDD33 | Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25 |



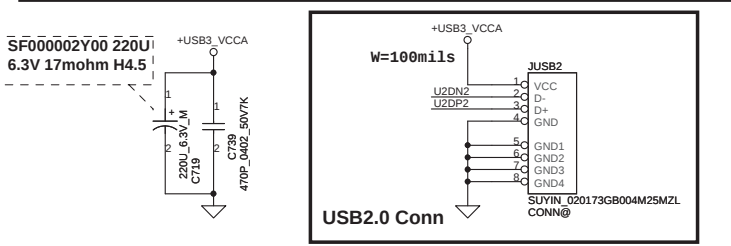
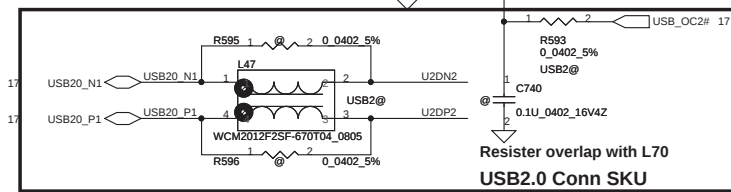
As short as possible



SF000002Y00 220u  
6.3V 17mohm H4.5

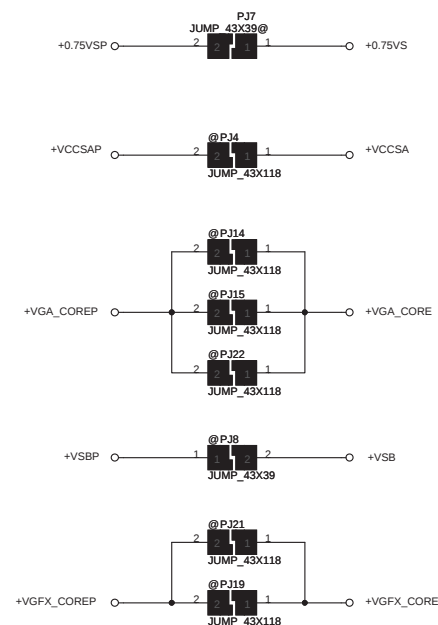
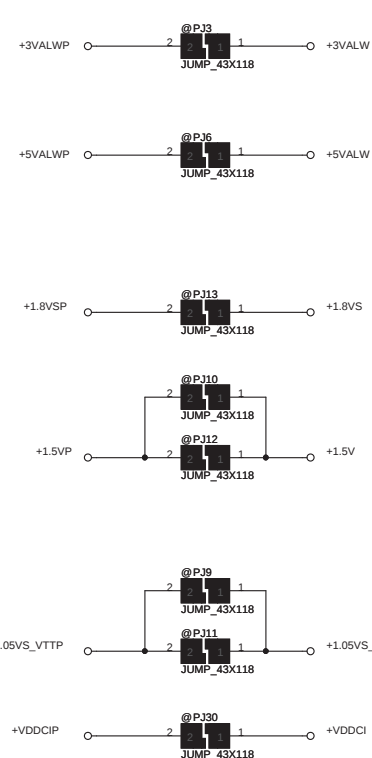
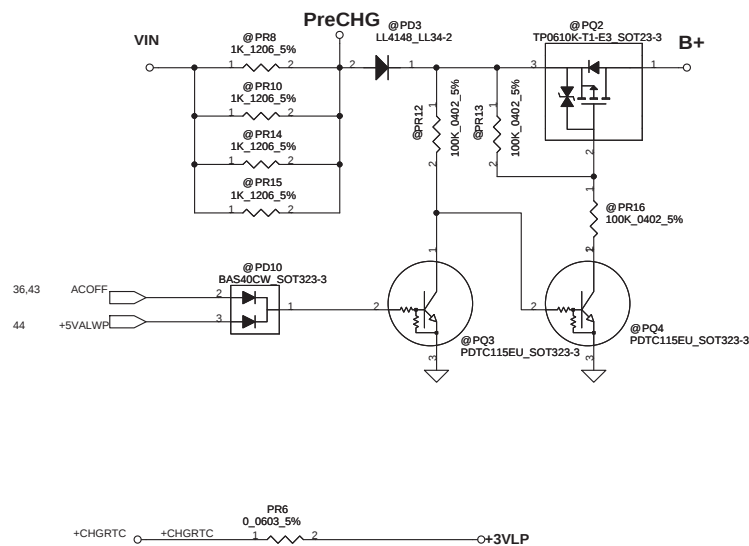
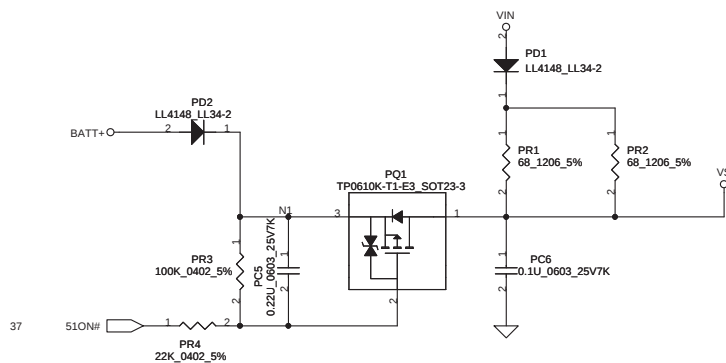
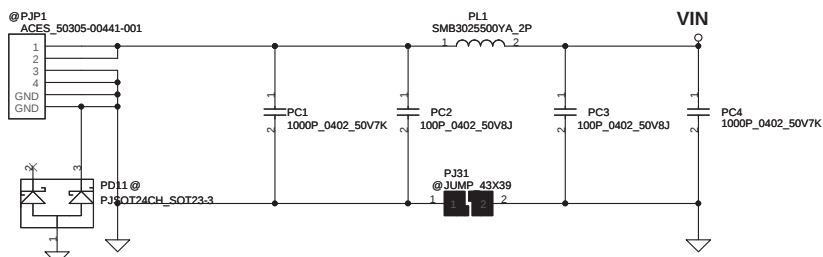


P/N: SA000048H10 (S IC UPD720200AF1-DAP-SSA-A FBGA USB3.0)



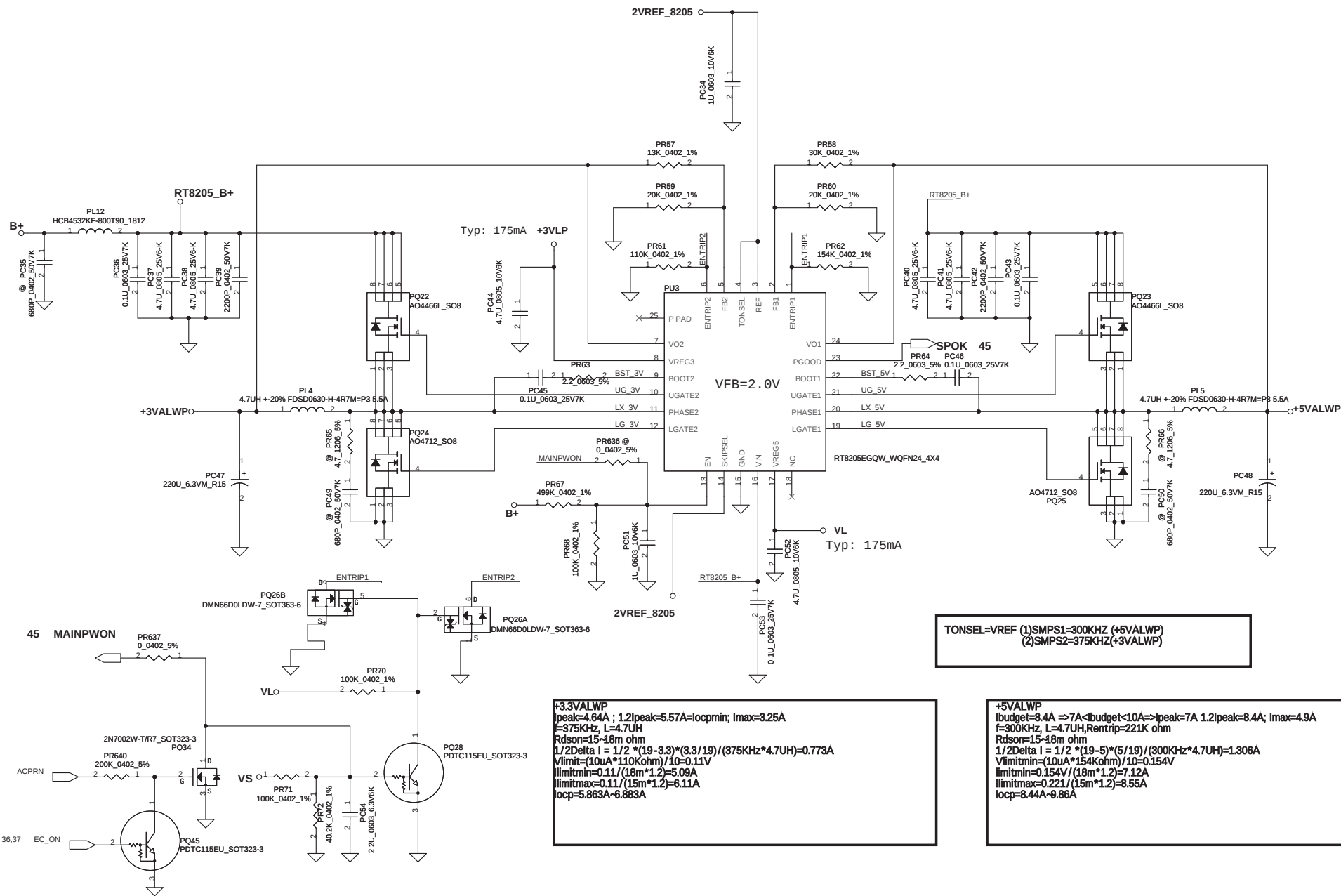
USB2.0 Conn

| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       | Compal Secret Data | Document Number | Rev B      |
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| Date: Tuesday, November 09, 2010                                                                                                                                                                                                                                                                                                                                                                                                                              |                    |                 |            |
| Sheet 41 of 60                                                                                                                                                                                                                                                                                                                                                                                                                                                |                    |                 |            |



|                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            |                          |                            |       |          |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Date:                    | Tuesday, November 09, 2010 | Sheet | 42 of 60 |





TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)  
(2)SMPS2=375KHZ(+3VALWP)

**+3.3VALWP**  
I<sub>peak</sub>=4.64A ; I<sub>2peak</sub>=5.57A=I<sub>ocpmin</sub>; I<sub>max</sub>=3.25A  
f=375KHz, L=4.7UH  
R<sub>ds(on)</sub>=15-18m ohm  
1/2Delta I = 1/2 \* (19-3.3)\*(3.3/19)/(375KHz\*4.7UH)=0.773A  
V<sub>limitmin</sub>=(10uA\*110Kohm)/10=0.11V  
I<sub>limitmin</sub>=0.11/(18m\*1.2)=5.09A  
I<sub>limitmax</sub>=0.11/(15m\*1.2)=6.11A  
I<sub>ocp</sub>=5.863A-6.883A

**+5VALWP**  
I<sub>budget</sub>=8.4A =>7A<I<sub>budget</sub><10A=>I<sub>peak</sub>=7A I<sub>2peak</sub>=8.4A; I<sub>max</sub>=4.9A  
f=300KHz, L=4.7UH, R<sub>entrip</sub>=221K ohm  
R<sub>ds(on)</sub>=15-18m ohm  
1/2Delta I = 1/2 \* (19-5)\*(5/19)/(300KHz\*4.7UH)=1.306A  
V<sub>limitmin</sub>=(10uA\*154Kohm)/10=0.154V  
I<sub>limitmin</sub>=0.154V/(18m\*1.2)=7.12A  
I<sub>limitmax</sub>=0.221/(15m\*1.2)=8.55A  
I<sub>ocp</sub>=8.44A-9.86A



35,36,40,41 SYSON

+5VALW

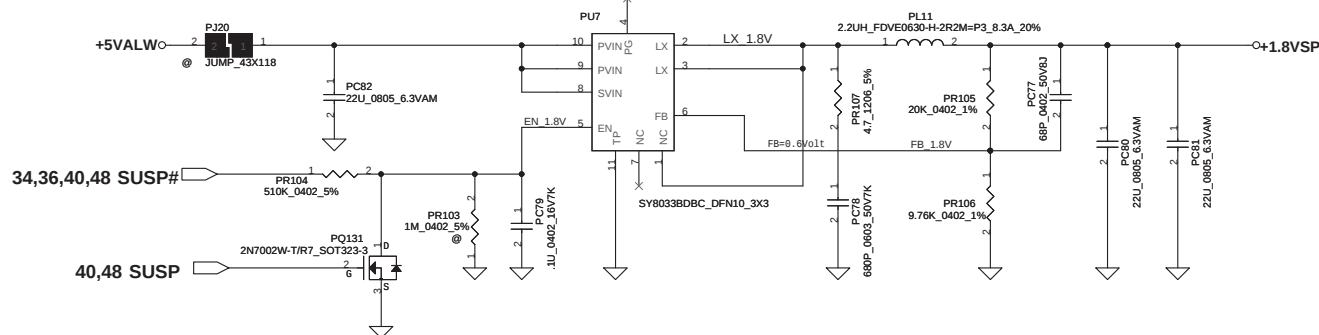
+5VALW

B+

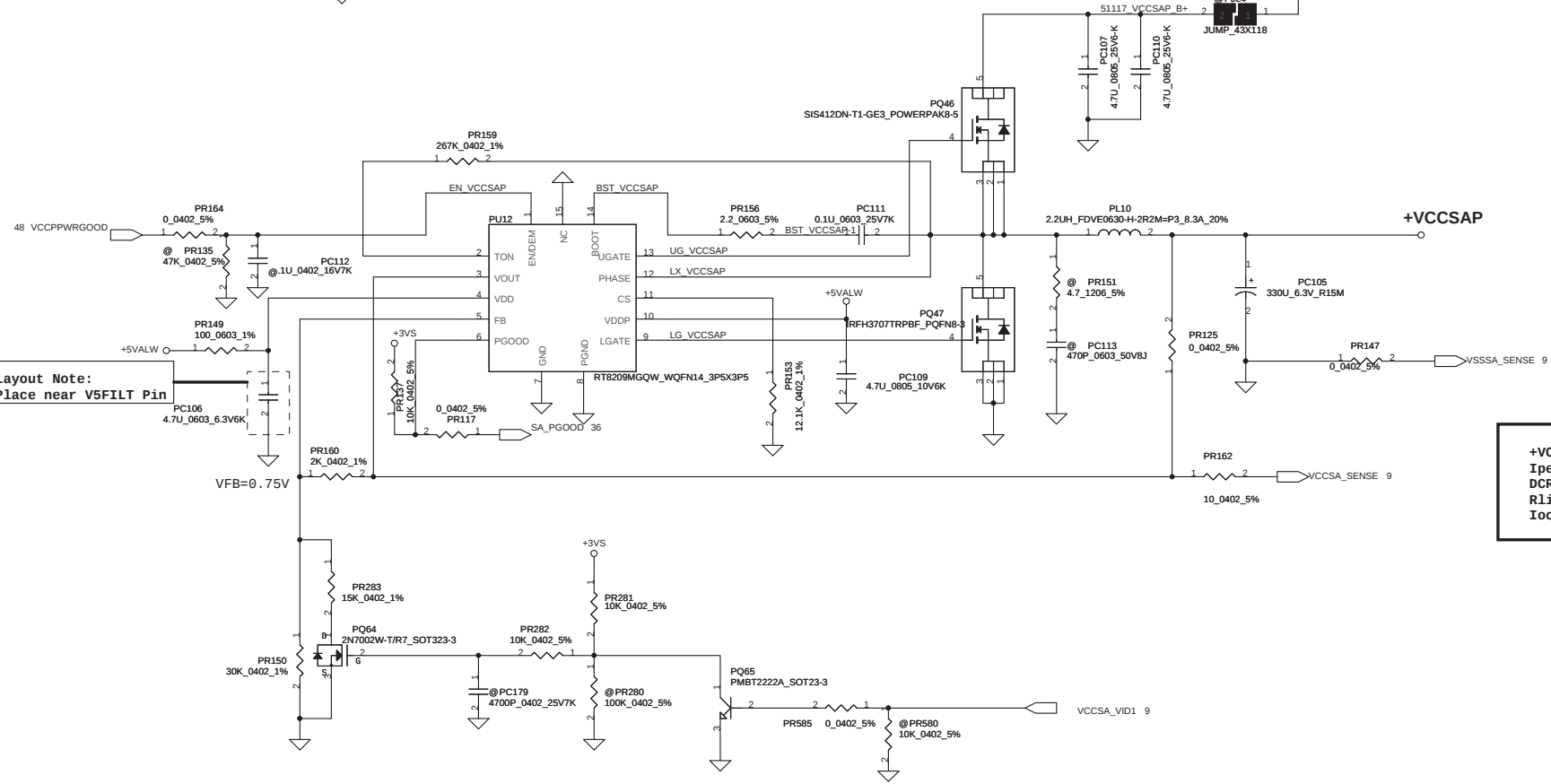
+1.5VP

+1.5VP  
Ipeak=21.56A;1.2Ipeak=25.87A ;Imax=15.09A  
Rton=267K, Fsw=298KHz ,Rdson=4.5~5.6mohm  
Rtrip=16.5K  
Iocp=25.97A~42.41A

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                    |                 |            |                          |                            |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|--------------------------|----------------------------|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                         | Compal Secret Data |                 |            | Compal Electronics, Inc. |                            |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                    |                 |            | Date:                    | Tuesday, November 09, 2010 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                    |                 |            | Sheet                    | 46 of 60                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                    |                 |            | Rev                      | B                          |



1.8VSP  
 Ipeak=3.35A ; 1.2Ipeak=4.02 ; Imax=2.345A  
 Vout=0.6\*(1+(20K/10K))=1.8V  
 -DVT-



+VCCSAP  
 Ipeak=6A , Imax=4.2A, 1.2Ipeak=7.2A  
 DCR= 9 m(typ)-10 m(max)  
 Rlimit=12.1K, Rds(on)=14.5-17.9mohm  
 Iocp=7.24A-12.59A

Layout Note:  
 Place near V5FILT Pin

| VID[0] | VID[1] | VCCSA Vout | Require on 2011/ 2012 | Required |
|--------|--------|------------|-----------------------|----------|
| 0      | 0      | 0.9 V      | Yes/Yes               |          |
| 0      | 1      | 0.8 V      | Yes/Yes               |          |
| 1      | 1      | 0.75V      | No/Yes                |          |
| 1      | 1      | 0.65V      | No/Yes                |          |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            |                          |                            |                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|--------------------------|----------------------------|----------------|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       | Compal Secret Data |                 |            | Compal Electronics, Inc. |                            |                |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Date:                    | Tuesday, November 09, 2010 | Sheet 47 of 60 |

Note: Use VCCSA\_SEL to switch High & Low Level for VID[1]



**Ipeak**  
**Granville(35W) 47A**  
**Whistler(25W) 27A(VDDC+VDDCI)**  
**Seymour(15W) 14.2A(VDDC+VDDCI)**

Switch freq. (RF pin setting)  
 47K ==>450KHZ  
 100K ==>390KHZ  
 200K ==>350KHZ (Currently setting)  
 470K ==>300KHZ

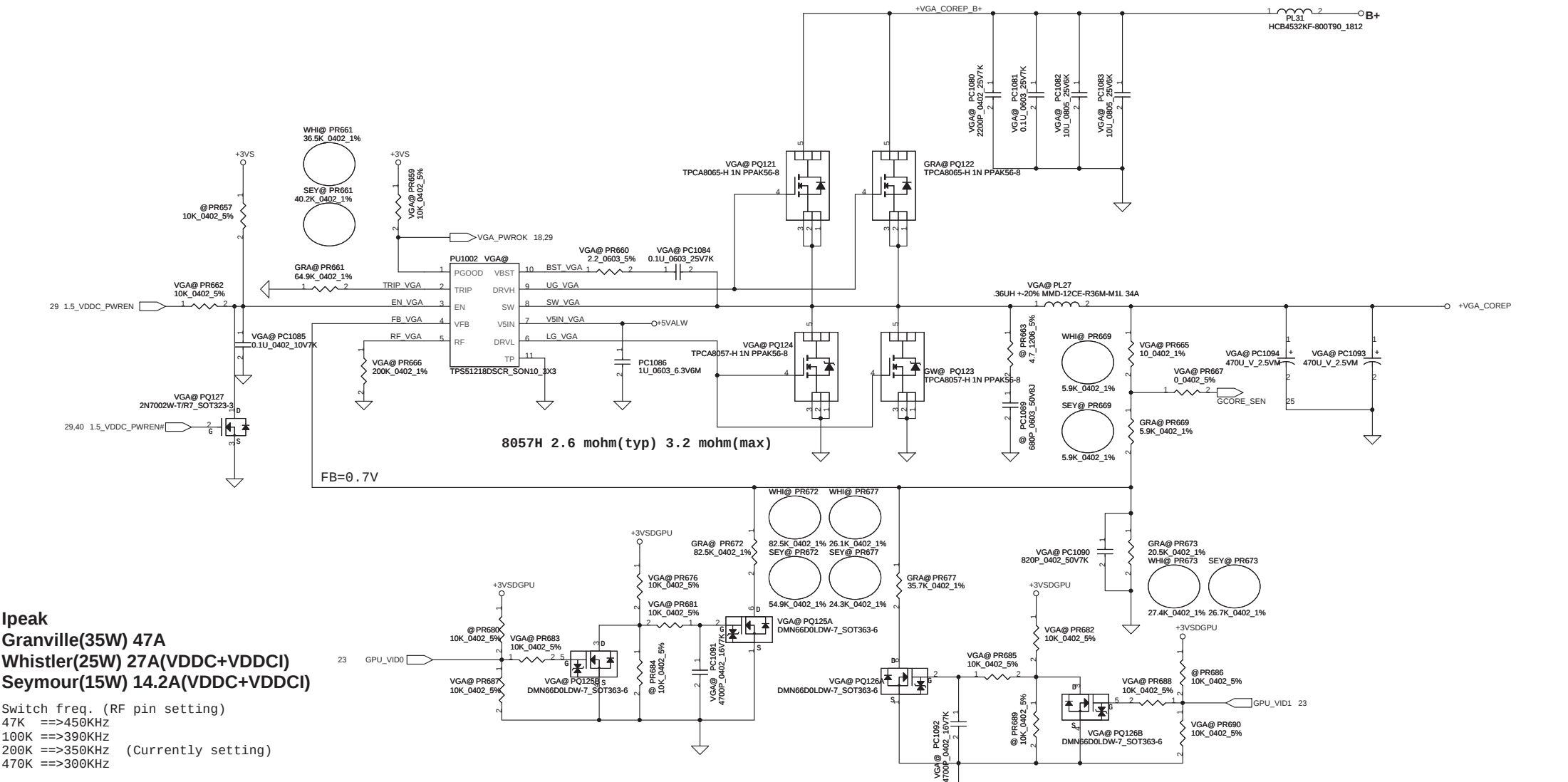
| GPIO 15  | GPIO 20  | Whistler           | Seymour            | Granville          |
|----------|----------|--------------------|--------------------|--------------------|
| GPU_VID0 | GPU_VID1 | Core Voltage Level | Core Voltage Level | Core Voltage Level |
| 1        | 1        | 0.85V              | 0.85V(0.855V)      | 0.90V              |
| 0        | 1        | 0.9V               | 0.9V(0.930V)       | 0.95V              |
| 1        | 0        | 1.00V              | 1.00V(1.025V)      | 1.00V              |
| 0        | 0        |                    | 1.1V(1.100V)       | 1.05V              |

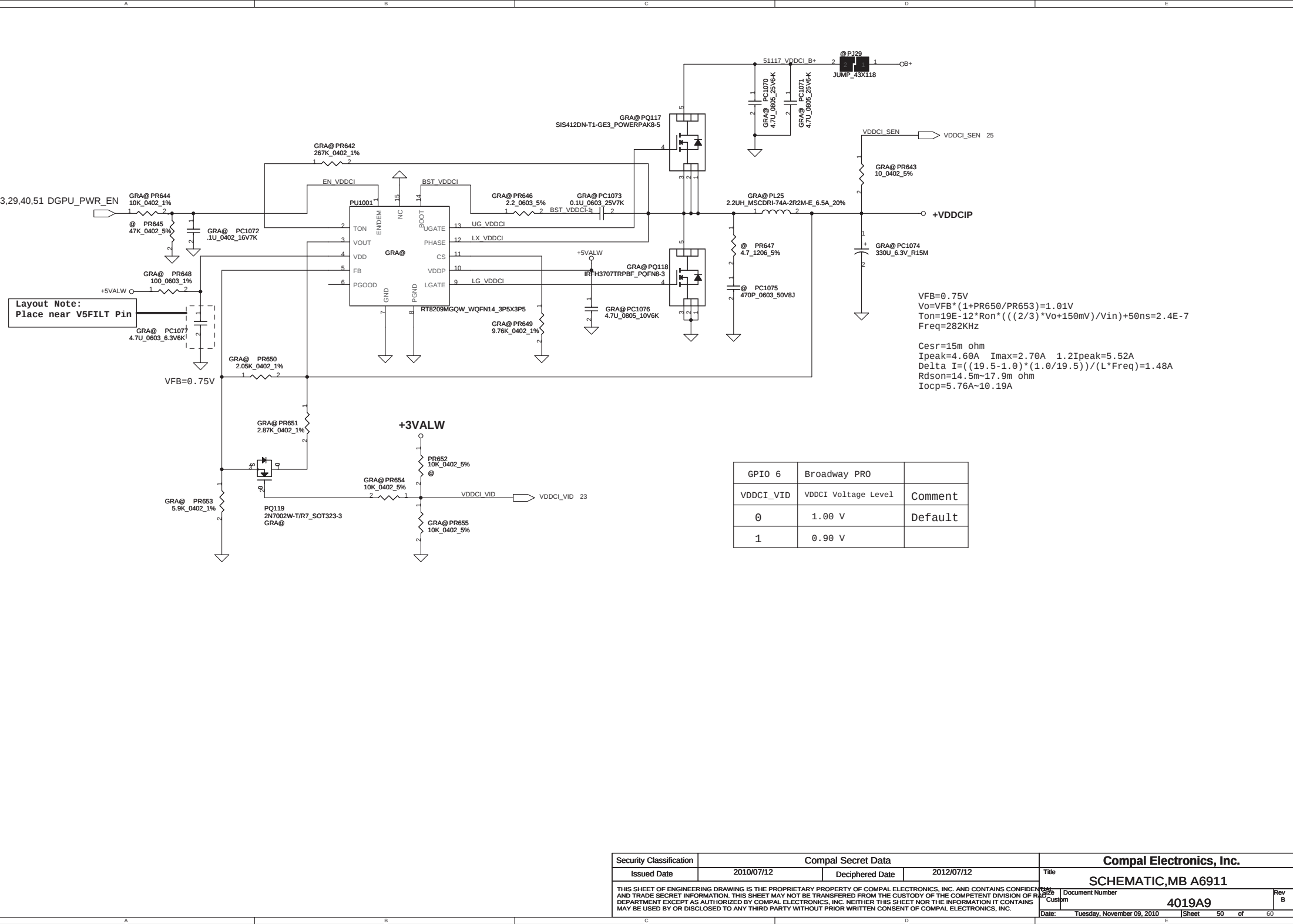
For Granville  
 1/2Delta I=4.05A  
 Vtrip=Rtrip\*Itrip=64.9K\*10uA=0.649V  
 Iocpmin=(Vtrip/8\*Rdson)+1/2Delta  
 =(0.649V/(8\*1.6m ohm))+4.502A  
 =50.7A+4.05A=54.75A

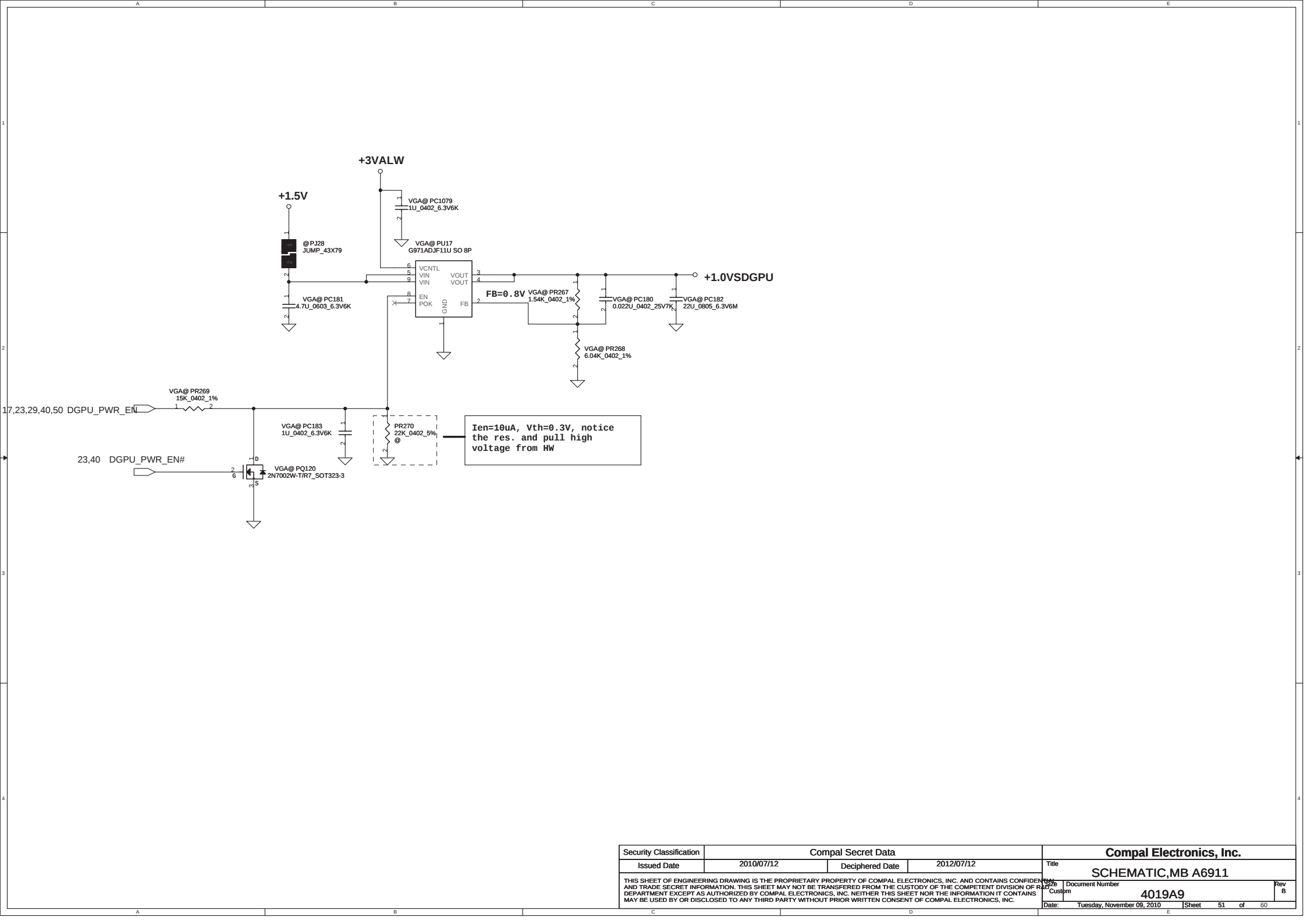
For Seymour  
 1/2Delta I=4.31A  
 Vtrip=40.2K\*10uA=0.402V  
 Iocp=0.402V/(8\*3.2m)+1/2Delta I  
 =15.70A+4.31A=20.01A

For Whistler  
 1/2Delta I=4.05A  
 Vtrip=36.5K\*10uA=0.365V  
 Iocpmin=0.365V/(8\*1.6m)+1/2Delta I=28.51A+4.05A  
 =32.56A

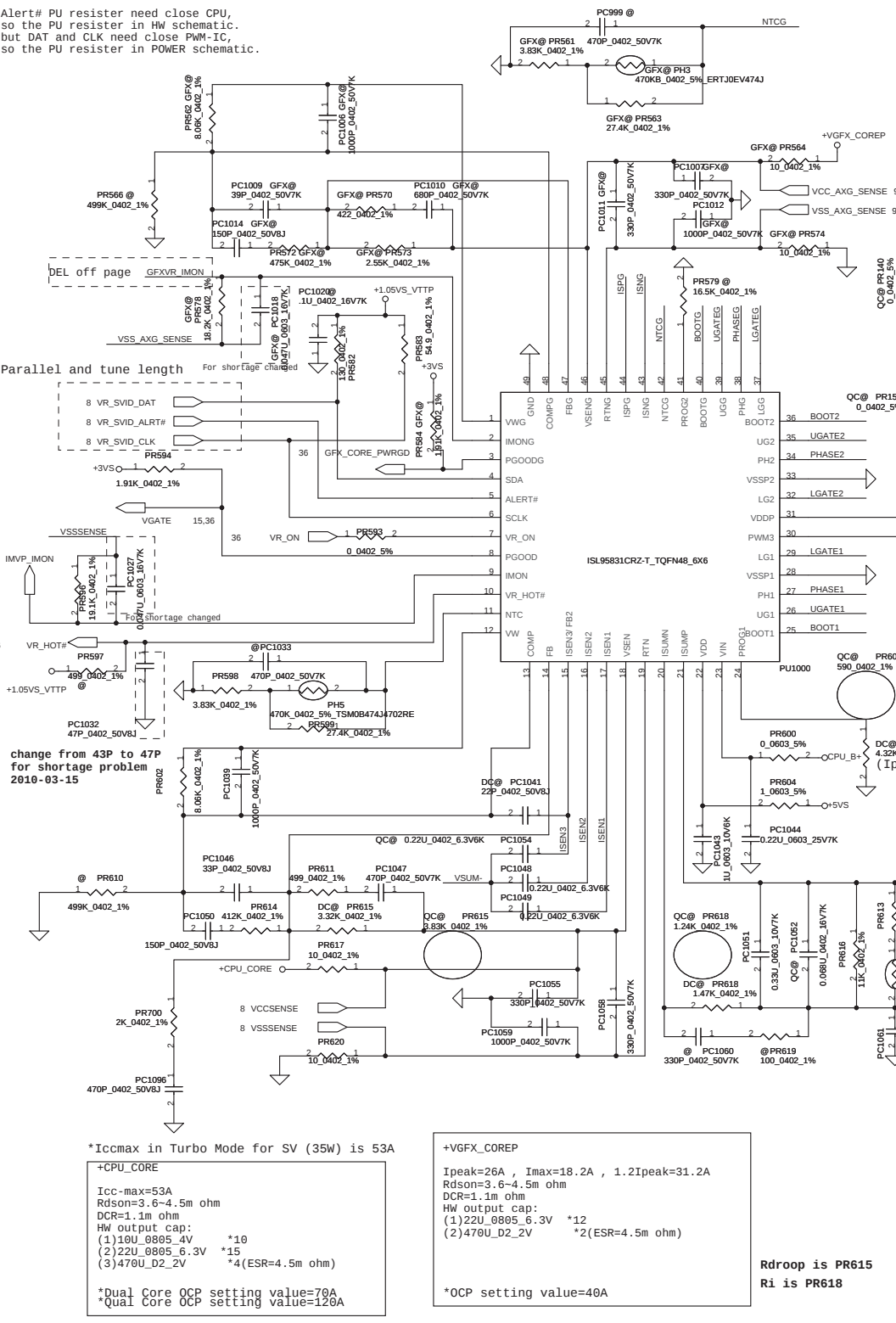
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |            | Compal Secret Data |            | Compal Electronics, Inc. |                            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------|------------|--------------------------|----------------------------|
| Issued Date                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 2010/07/12 | Deciphered Date    | 2012/07/12 | Title                    | SCHEMATIC,MB A6911         |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Date:                    | Tuesday, November 09, 2010 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Sheet                    | 49 of 60                   |







|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            |                          |                            |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|--------------------------|----------------------------|
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       | Compal Secret Data |                 |            | Compal Electronics, Inc. |                            |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Sheet                    | 51 of 60                   |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Rev                      | B                          |



Alert# PU resistor need close CPU,  
so the PU resistor in HW schematic.  
but DAT and CLK need close PWM-IC,  
so the PU resistor in POWER schematic.

DEL off page

Parallel and tune length

change from 43P to 47P  
for shortage problem  
2010-03-15

\*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU\_CORE

Icc-max=53A  
Rdson=3.6-4.5m ohm  
DCR=1.1m ohm  
HW output cap:  
(1)10U\_0805\_4V \*10  
(2)22U\_0805\_6.3V \*15  
(3)470U\_D2\_2V \*4(ESR=4.5m ohm)

+VGFX\_COREP

Ipeak=26A, Imax=18.2A, 1.2Ipeak=31.2A  
Rdson=3.6-4.5m ohm  
DCR=1.1m ohm  
HW output cap:  
(1)22U\_0805\_6.3V \*12  
(2)470U\_D2\_2V \*2(ESR=4.5m ohm)

Rdroop is PR615  
Ri is PR618

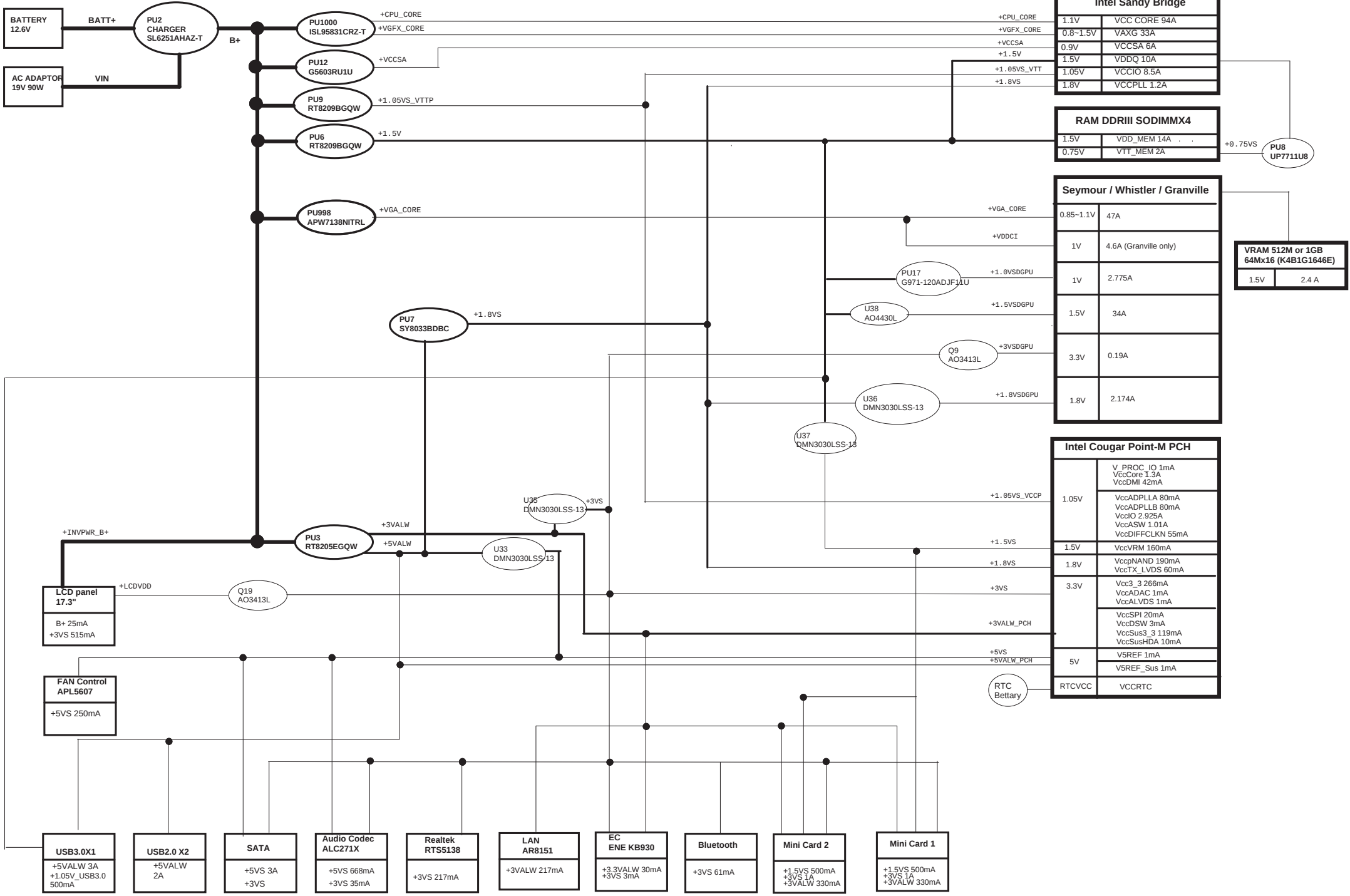
| Security Classification                                                                                                                                                                                                                                                                                                                                                                                                                                       |            | Compal Secret Data |            | Compal Electronics, Inc. |                    |
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| Document Number                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | 4019A9                   | Rev B              |
| Date: Tuesday, November 09, 2010                                                                                                                                                                                                                                                                                                                                                                                                                              |            |                    |            | Sheet 52                 | of 60              |

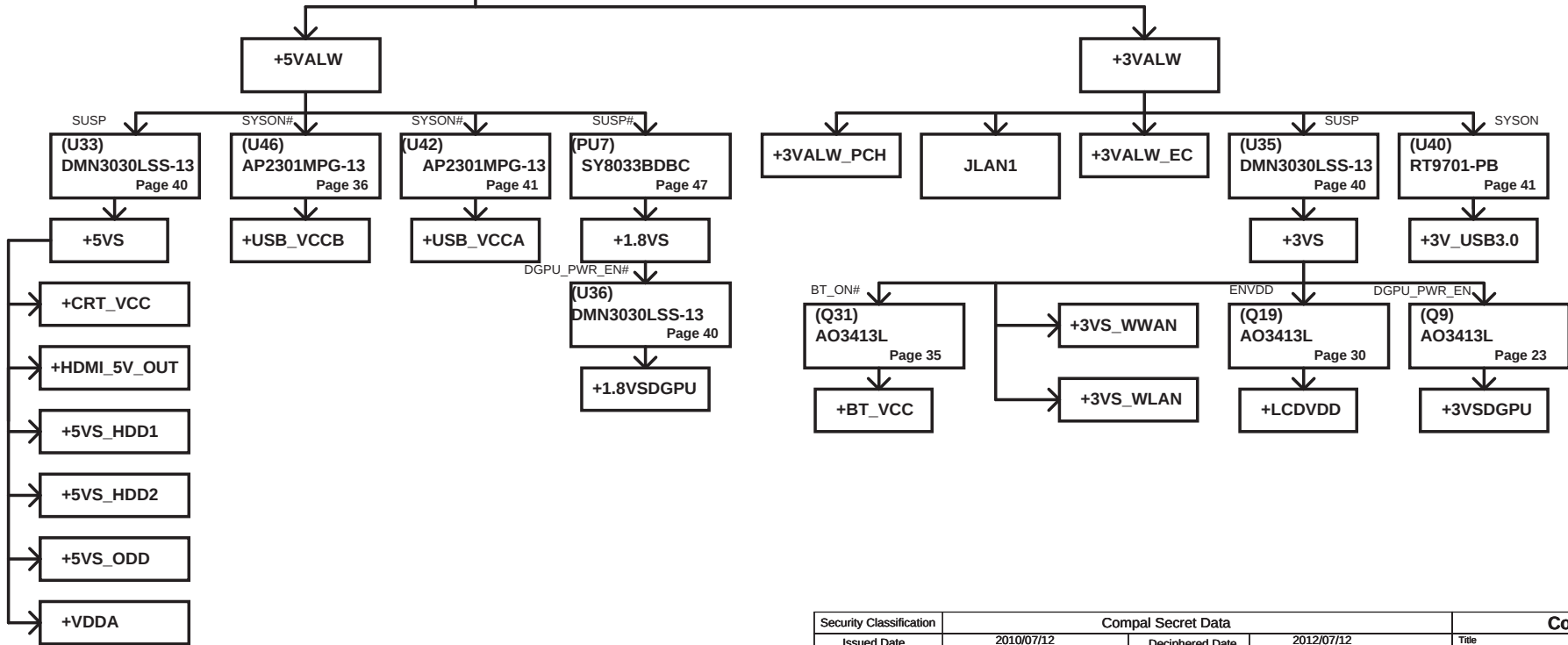
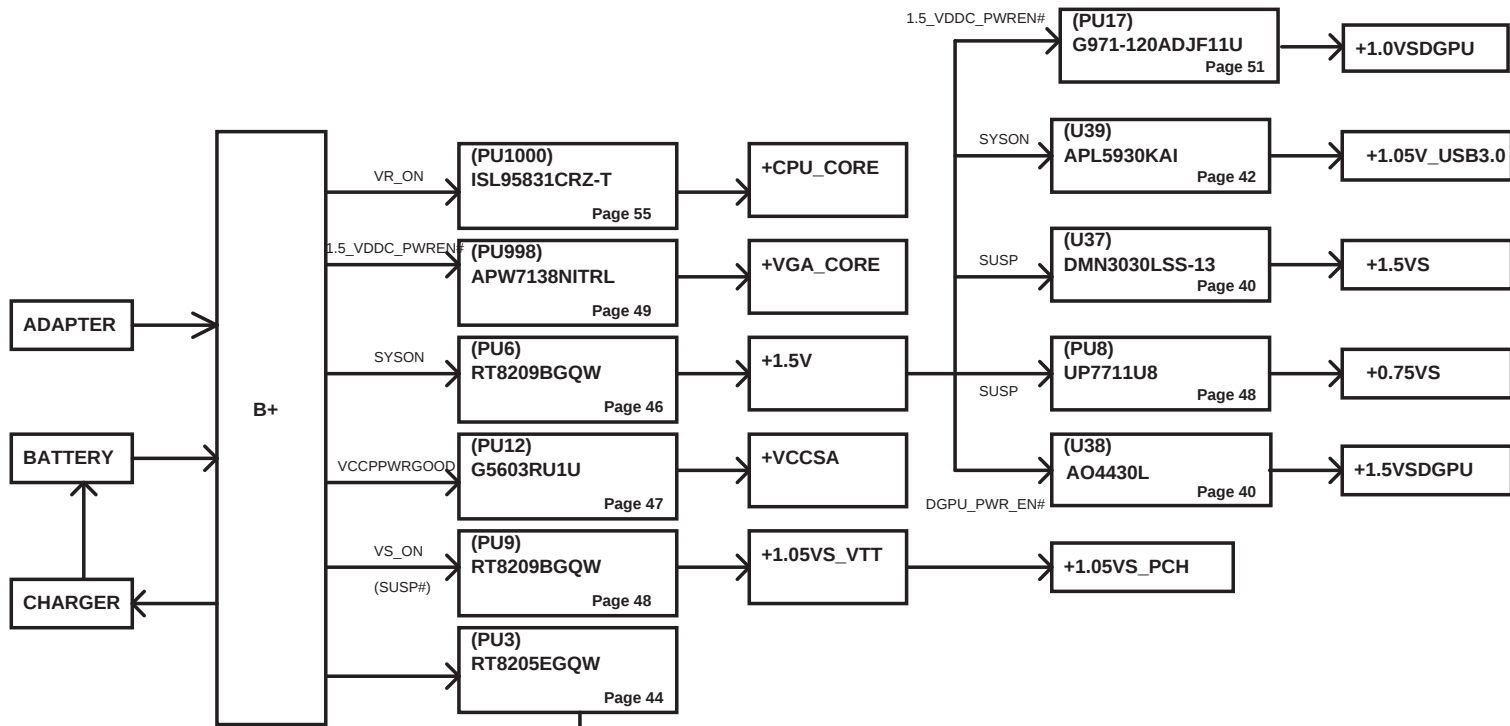
## Version change list (P.I.R. List)

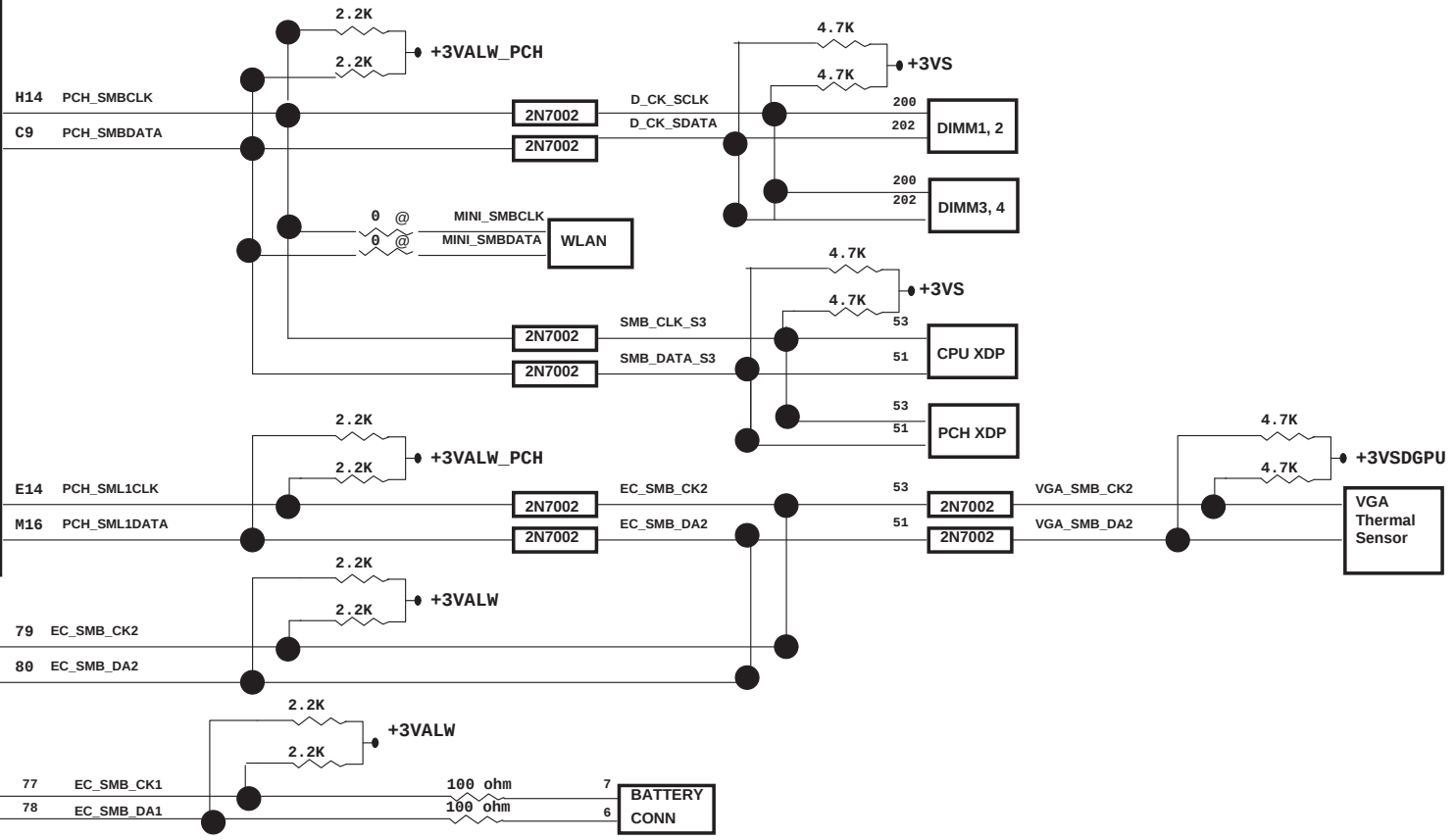
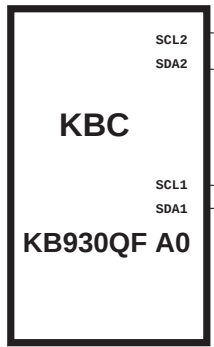
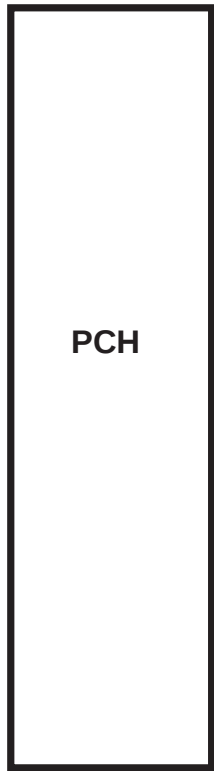
Page 1 of 1 for PWR

| Item | Fixed Issue                                            | Reason for change                                                                                                                                                | Rev. PG# |          | Modify List                                                                                      | Date       | Phase |
|------|--------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|----------|--------------------------------------------------------------------------------------------------|------------|-------|
| 1    | HW increase 1.8V voltage.                              | HW need to increase 1.8V voltage.                                                                                                                                | 0.1      | 47       | Change PR106 from SD034100280 to SD034976180.                                                    | 2010/09/23 | DVT   |
| 2    | VGA Granville OVP issue.                               | Because VGA has happened OVP issue in Granville SKU, that is caused by output capacitor too small. change PC1094 to SGA00004200 to solve it. PC1088 must remove. | 0.1      | 49       | Add PC1094 to SGA00004200 and delete PC1088 SF000002000.                                         | 2010/09/23 | DVT   |
| 3    | 1.8V Power sequence adjust.                            | HW adjust 1.8V power sequence.                                                                                                                                   | 0.1      | 47       | change PR104 from SD028100380 to SD028150380.                                                    | 2010/09/23 | DVT   |
| 4    | 0.75V Power sequence adjust.                           | HW adjust 0.75V power sequence.                                                                                                                                  | 0.1      | 48       | Change PR127 from SD028150380 to SD034267380.                                                    | 2010/09/23 | DVT   |
| 5    | adjust +1.05VS_VTT power sequence                      | HW adjust +1.05VS_VTT power sequence                                                                                                                             | 0.1      | 48       | Change PC99 from SE107475K80 to SE076104K80.                                                     | 2010/09/23 | DVT   |
| 6    | adjust +VDDCI power sequence                           | HW adjust +VDDCI power sequence                                                                                                                                  | 0.1      | 50       | Change PR644 from SD034301380 to SD034100280.                                                    | 2010/09/23 | DVT   |
| 7    | HW request to delete PR103.                            | HW request to delete PR103.                                                                                                                                      | 0.2      | 47       | Delete PR103 SD028100480.                                                                        | 2010/09/28 | DVT   |
| 8    | PR104 BOM error.                                       | PR104 BOM error for power sequence.                                                                                                                              | 0.2      | 47       | Change PR104 from SD034150380 to SD034510380.                                                    | 2010/09/28 | DVT   |
| 9    | PR669 BOM error for Seymour only.                      | PR669 BOM error for Seymour only.                                                                                                                                | 0.2      | 49       | Chnage PR669 from SD034681180 to SD034590180.                                                    | 2010/09/28 | DVT   |
| 10   | To same as P5WE0 VCCSAP choke.                         | To same as P5WE0 VCCSAP choke.                                                                                                                                   | 0.2      | 47       | Change PL10 from SH000009Q00 to SH00000M700.                                                     | 2010/09/28 | DVT   |
| 11   | HW request to add PQ130 and PQ131 to speed up to 放电.   | HW request to add PQ130 and PQ131 to speed up to 放电.                                                                                                             | 0.3      | 47<br>48 | Add PQ130 and PQ131 SB000006800.                                                                 | 2010/10/05 | DVT   |
| 12   | Remove chargeable RTC battery.                         | We reserve chargeable RTC battery to prevent over heat issue, Thermal team result is pass, so remove chargeable RTC battery.                                     | 0.3      | 42       | Delete PR691 SD013000080<br>Change PR6 from SD013560080 to SD013000080.                          | 2010/10/05 | DVT   |
| 13   | Chnage PL4 and PL5 to TOKO new part.                   | Chnage PL4 and PL5 to TOKO new part.                                                                                                                             | 0.3      | 44       | Change PL4 and PL5 from SH000006J80 to SH00000MB00                                               | 2010/10/05 | DVT   |
| 14   | for ISN issue.                                         | for ISN issue.                                                                                                                                                   | 0.3      | 43       | Add PL30 SH000009Q00.<br>Delete PL28 SM010018210                                                 | 2010/10/05 | DVT   |
| 15   | to same as P5WE0 choke.                                | to same as P5WE0 choke.                                                                                                                                          | 0.3      | 47       | Change PL10 and PL11 from SH000009Q00 to SH00000F800                                             | 2010/10/05 | DVT   |
| 16   | for QC+25WGPU and QC+35W GPU change CP point.          | Because Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.                                                                     | 0.3      | 43       | Delete PQ20 SB000006800. Delete PR48 SD034255180<br>Change PR22 from SD000001F00 to SD021100b80. | 2010/10/05 | DVT   |
| 17   | for QC+25WGPU and QC+35W GPU change CP point.          | Because Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.                                                                     | 0.3      | 43       | Change PR47 from SD034121280 to SD034100180<br>Change PR50 from SD034200280 to SD034511280       | 2010/10/05 | DVT   |
| 18   | Modify adapter throttling at turbo mode setting point. | Modify adapter throttling at turbo mode setting point.                                                                                                           | 0.3      | 45       | Add PR695 SD034154280<br>Add PR697 SD034174280                                                   | 2010/10/05 | DVT   |
| 19   | CPU Transient responds issue.                          | Change CPU transient reponds RC time constant.                                                                                                                   | 0.4      | 52       | Add PC1052 SE000003J80. Add PC1096 SE071471J80. Add PR700 SD034200180.                           | 2010/10/07 | DVT   |
| 20   | for ISN issue.                                         | for ISN issue.                                                                                                                                                   | 0.4      | 43       | Change PL30 from SH000009Q00 to SH00000M700.                                                     | 2010/10/07 | DVT   |
| 21   | Make BOM same as P5WE0.                                | Make BOM same as P5WE0.                                                                                                                                          | 0.4      | 52       | Change PL21,PL23,PL24 from SH000005680 to SH00000HK00.                                           | 2010/10/07 | DVT   |
| 22   | BOM loss.                                              | Because BOM Config loss 65@ and 90W@, so miss PR695 and PR697.                                                                                                   | 0.5      | 45       | Add PR695 SD034909180 9.09K_0402_1%<br>ADD PR697 SD034162280 16.2K_0402_1%                       | 2010/10/26 | PVT   |
| 23   | Modify CPU OCP.                                        | Beuase original design is for 3 phase DC, now change to 2 phase DC, so modify OCP.                                                                               | 0.5      | 52       | Chnage PR618 from SD034698080 to SD000009480                                                     | 2010/10/26 | PVT   |
| 24   | Modify DC LL.                                          | Because DC OCP was modified, must also update LL of DC.                                                                                                          | 0.5      | 52       | Chnage PR615 from SD034215180 to SD034332180                                                     | 2010/10/26 | PVT   |

|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            |                          |                            |                |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|------------|--------------------------|----------------------------|----------------|
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Date:                    | Tuesday, November 09, 2010 | Sheet 53 of 60 |

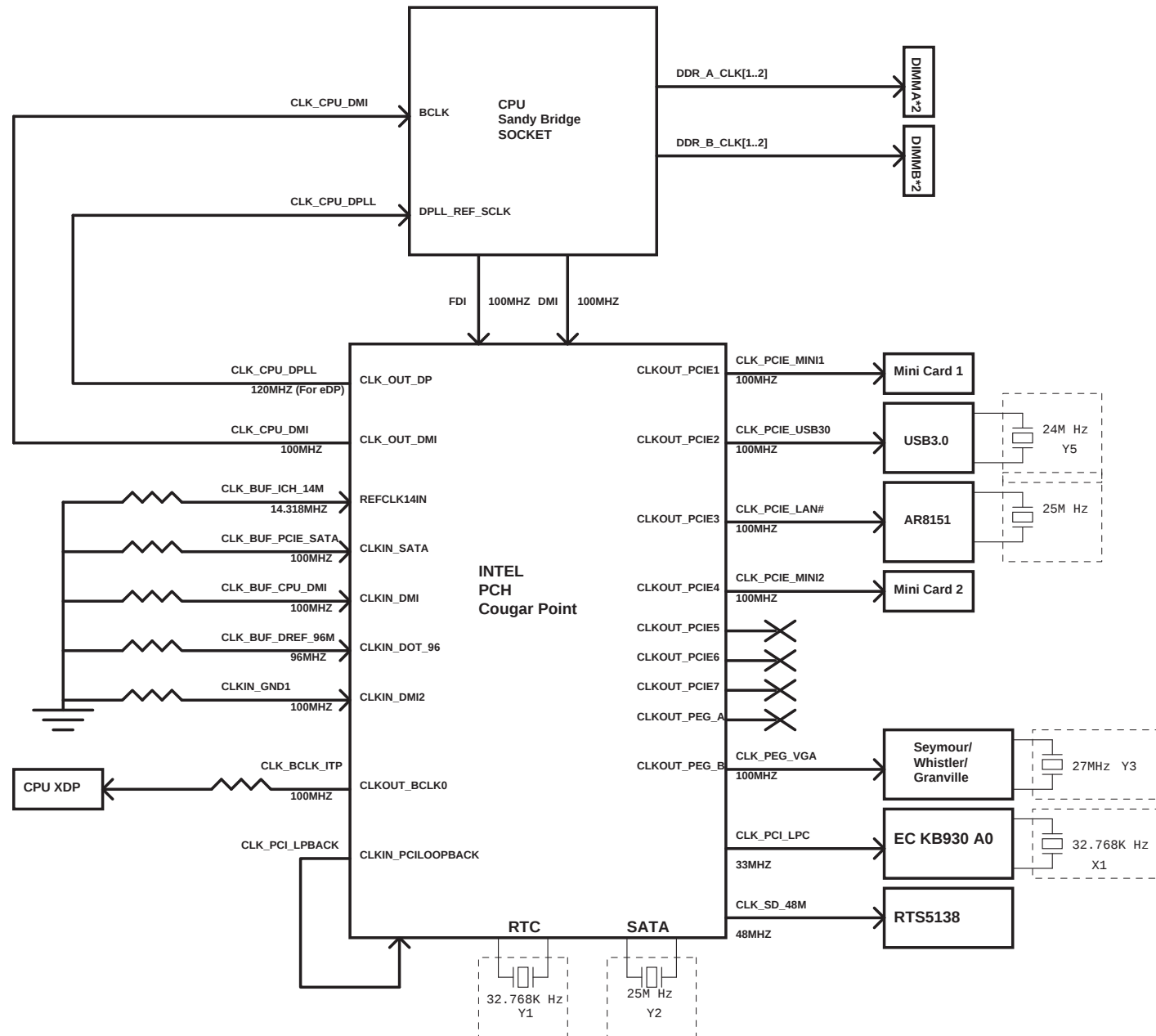




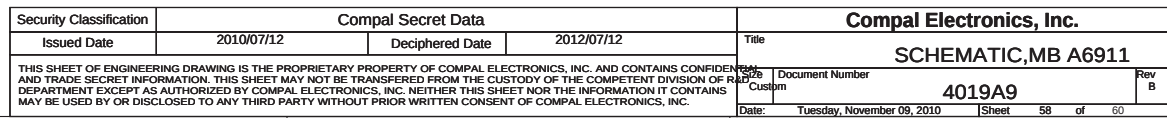


PCH SM Bus address

| Device            | Address   |
|-------------------|-----------|
| ChannelA DIMM0 A0 | 1010 000X |
| DIMM1 A2          | 1010 001X |
| ChannelB DIMM0 A4 | 1010 010X |
| DIMM1 A6          | 1010 011X |



|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            |                          |                            |
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Date:                    | Tuesday, November 09, 2010 |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                    |                 |            | Sheet                    | 57 of 60                   |



PCB

LA-6911P MB Rev0: DA80000LC00  
LA-6911P MB Rev1: DA80000LC10  
LA-6911P MB with Small Board Rev1: DAZ  
LA-69111P REV0 MB

VGA

Granville PRO M2 A12:  
SA00004C820(S IC 216-0769024 A12 GRANVILLE PRO ABO!)

WHISLER PRO M2 A11:  
SA00004C720(S IC 216-0810005 A11 WHISTLER PRO FCBGA 962P ABO !)

X76

X761@ X76264BOL01 VRAM 512M SAM P7YE0  
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)

X762@ X76264BOL02 VRAM 512M HYN P7YE0  
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

X763@ X76264BOL03 VRAM 1G SAM P7YE0  
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)

X764@ X76264BOL04 VRAM 1G HYN P7YE0  
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

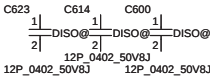
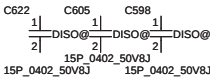
X765@ X76264BOL05 VRAM 2G HYN P7YE0  
Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)

X766@ X76264BOL06 VRAM 2G SAM P7YE0  
Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)

X767@ X76264BOL07 VRAM 1G SAM P7YE0  
Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)

X768@ X76264BOL08 VRAM 1G HYN P7YE0  
Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)

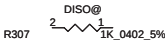
CRT Option Components



15P\_0402\_50V8J: SE071150J80  
12P\_0402\_50V8J: SE071120J80

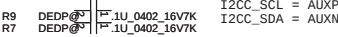
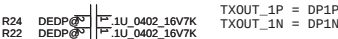
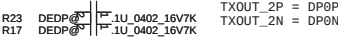


0\_0805\_5%: SD002000080

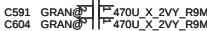


DIS only PCH DAC\_IREF  
can use 1K\_0402\_5% PD to GND

DIS EDP Option Components



Granville VGA\_CORE CAP Option



SGA00003N00  
S POLY C 470U 2V Y X  
LESR9M S H1.9

EC susclk/crystal  
Option Components



|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            |                          |                            |                |  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------------|------------|--------------------------|----------------------------|----------------|--|
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|                                                                                                                                                                                                                                                                                                                                                                                                                                                               |            |                    |            | Docu                     | ment Number                | Rev            |  |
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| 1 | 2 | 3 | 4 | <div>0923:<br/>  rework<br/>  ADD Q8 DMN66D0LDW-7(SB00000D000) &amp; change BOM structure to DIS0(DIS0 Granville can't power on issue)<br/>  R72 100K_0402_5%(SD028100380)change BOM structure to DIS0(DIS0 Granville can't power on issue)<br/>  R674 4.7K PH change BOM structure to @(+3VS GPIO19 leakage)<br/>  D31 change BOM structure to @(EC debug CLK leakage)<br/>  R531,R530 change BOM structure to DIS0@ (HSYN:VSYNC 11: Audio for both DisplayPort and HDMI)<br/>  ADD C591 C604 BOM option<br/>  (Seymour/Whistler option NOGRAN@ SGA20331E10 S POLY C 330U 2V 9mohm H1.9)<br/>  (Granville option GRAN@ SGA00004200 S POLY C 470U 2V M D2 LESR4.5M SX H1.9)<br/>  C746,C750 change from SF000001500 to SF000001580<br/><br/>Power sequence:<br/>  1. BOT (adjust +5VS power sequence)<br/>    R698 change from 200K to 100K_0402_5% (SD028100380)<br/>  2. BOT (adjust +1.8VS power sequence)<br/>    PR104 change from 100K to 510K_0402_5%(SD028510380)<br/>    remove PR103 1M_0402_5%<br/>  3. TOP (adjust +1.5VS power sequence)<br/>    R67 change from 510K_0402_5% to 750K_0402_5%(SD028750380)<br/>  4. TOP (adjust +0.75VS power sequence)<br/>    PR127 change from 150K_0402_5% to 267K_0402_1%(SD034267380)<br/>  5. TOP (adjust +1.05VS_VTT power sequence)<br/>    PC99 change from 4.7U to .1U_0402_16V7K (SE076104K00)<br/>  6. TOP (adjust +1.5VSDGPU power sequence)<br/>    R113 510K change to 100K_0402_1% (SD034100380)<br/>  7. BOT (adjust +VDDCI power sequence)<br/>  PR644 301K change to 10K_0402_1% (SD034100280)<br/><br/>Power:<br/>  PR101 change from 10K to 9.53K (adjust +1.5V power)<br/>  PR106 change from 10K to 9.76K (adjust +1.8VS power)<br/>Layout:<br/>  D21 channgce to SC600000B00 (for sourcer 2nd source)<br/>  DEL C590,C603 (DEL colay Cap)<br/>  L24,25,27,30,31 change from SM010004010 to SM010015410<br/>  BATT Blue light place at front side<br/>  H1 change H3P0 to H4P6<br/>  DEL LED1,LED2,LED3,LED4<br/><br/>0924:<br/>  Q37,Q39,Q40,Q41, change from SB00000FG00 to SB00000FG10<br/>  U7 change from SB000007000 to SB000007010<br/>  USB3.0 schmetic change to unpop<br/>  XDP change to unpop<br/>  U19 A10,N10,P10,B12 connect to GND<br/><br/>0925:<br/>  R249 change from U15.2 to U15.1(footprint issue)<br/>  R105 change form 10K to 10_0402_5%(SD028100A80)<br/>  R422 change BOM structure to @(crystal issue debug port1.2)<br/>  R422 change +3VS to +3VALW_PCH (GPIO28)<br/>  R674 change BOM structure to @(leakage issue debug port1.2)<br/>  R674 change +3VALW_PCH to +3VS (GPIO19)<br/>  ADD LED11 pop WLAN_LED#(SC500007700),LED12 @ MEDIA_LED#(SC591NB5A30)<br/>  LED10 WLAN_LED#(SC500007700) change BOM struture to @<br/>  DEL D9,D10 USB3.0 old ESD diode<br/>  ADD D32 new USB3.0 ESD diode (SC300001D00)<br/>  DEL R238,R250,C401 USB3.0 conn PD resistor &amp; CAP<br/>  EMI request:<br/>  R595,R596 change to @ L47 change to POP(USB2.0 common mode choke)<br/><br/>0927:<br/>  Audio vender suggest:<br/>  C913 change BOM structure to @<br/>  ADD C702 22K_0402_5%(SD028220280)<br/>  change USB conn to USB2.0(SUYIN_020133GB004M25MZL_4P-T)<br/>  modify Debug port note(GPIO19 PH +3VS GPIO28 PH +3VALW_PCH)<br/>  R667,R666 change BOM structure to @(XDP CLK source)<br/>  change SW4,SW5 BOM structure to @ (debug PWRBTN)<br/>  change R432,R435,R437 from 1K_0402_5% to 300_0402_5%(orange LED resistor)<br/>  change USB3.0 schmetic BOM structure back to USB30<br/>  C746,C750 change from SF000001500 to SF000001580<br/>  D4,D5 change from SCSH491D010(S SCH DIO CH491DPT SOT-23) to SCS00002000(S SCH DIO RB491D SOT-23 PANJIT)<br/>  Q29,Q33,Q36 change from SB934130020(S TR A03413L 1P SOT23-3) to SB0000006R10(S TR A03419L 1P SOT23-3)<br/><br/>0928:<br/>  DEL R468<br/>  JMINI1.24 change power source from +3VS to +3VS_WLAN<br/>  DEL R613<br/>  JMINI2.24change power source from +3VS to +3VS_WMAN<br/>  DEL R352<br/>  change power source from +XDPWR_SDPWR MSPWR to +CARDPWR<br/>  Q21 change from SB324110080(2SC2411K) to SB039040020(MMBT3904)<br/>  Change JUSB2 footprint to "SUYIN_020173GB004M25MZL_4P"<br/>  ADD R613 1M PD to GND(HDA_SYNC_PCH_R)<br/>  ADD SLP_A# at U37.G10 test point(for DFT request)<br/>  ADD JTAG_TDI at U30.AN23 test point(for DFT request)<br/>  ADD JTAG_TDO at U30.AM24 test point(for DFT request)<br/>  JREA01 change conn from TAITW_R013-P12-HM_44P_NR to TAITW_R013-P17-HM_40P_NR</div> | <div>0929:<br/>  DEL Rechargeable RTC schematic D21,R425,C551<br/><br/>0930:<br/>  R534,R540 change from 100_0402_1% to 1K_0402_5%(SD028100180)(DG1.5 change save cost)<br/>  C744,C745 change from 18P_0402_50V8J to 27P_0402_50V8J(SE071270J80)(25Mhz Crystal modify)<br/>  R357,R358,R330,R331,R345,R346,R387,R393,R292 change BOM structure to @ (10K_0402_5%)PD to GND(DG1.5 unuse CLK NC)<br/>  R666,R667 change BOM structure to @(XDP unuse)<br/>  R573,R575,R571,R572,R562,R566,R567,R570 DEL option 499_0402_1% leave 680_0402_5%<br/>  R318,R332 change from 00hm to 22_0402_5%(SD028220A80)<br/>  C448,C483 change to 4.7P_0402_50V8J(SE07147AC80)<br/>  L47 change to 670hm common mode choke CHENG HANN WCM2012F2SF-670T04(SM070000S80)<br/>  -----<br/><br/>1025:<br/>  R370,R413 change from SD028100380(100K_0402_5%) to SD028200380(200K_0402_5%)<br/>  PCH_GPIO1 change net to WL_EN#<br/>  LVDS<br/>  Add +5VS (Pin34) &amp; USB20_N4/P4 (Pin35, 36)<br/>  change EDP_HP0 to Pin18<br/>  PCH side add USB20_N4/P4 (Pin35, 36)<br/><br/>For eDP interface AUX channel, please request Layout routing as differential signal to follow eDP Layout Guide.<br/>(VGA_LCD_CLK &amp; VGA_LCD_DATA / I2CC_SCL &amp; I2CC_SDA)<br/><br/>DEL DDR DM<br/>  R50,R58,R59,R48,R56,R51,R60,R49 DIMMA<br/>  R39,R52,R44,R43,R46,R38,R45,R40 DIMMA<br/>  R77,R73,R109,R112,R180,R181,R192,R206 DIMMB<br/>  R64,R83,R108,R115,R179,R183,R189,R208 DIMMM<br/><br/>1026:<br/>  C604,C591 change from SGA00004200(470 4.5mohm)to SGA00003N00(470 9mohm)<br/>  Pop R257(SD028100380 100K_0402_5%),R622(SD028820180 8.2K_0402_5%) Board ID<br/>  R443 change from 100K_0402_5% to 10K_0402_5% (SD028100280)<br/><br/>remove R471,R622(JMINI1,JMINI2 Pin42 0ohm series resistor)<br/>  J1,J2 change location to J6,J7<br/>  remove R222 0ohm_0402 (H_CPUWPWRGD_R)<br/>  remove R423,0ohm_0402 (MINI1_CLKREQ#_R)<br/>  remove R392 0ohm_0402 (LAN_CLKREQ#_R)<br/>  remove R685 0ohm_0402 (MINI2_CLKREQ#_R)<br/>  remove R655 0ohm_0402 (WAKE#)<br/>  remove R636 0ohm_0402 (PCH_RSMRST#)<br/>  remove R377 0ohm_0402 (SUS_PWR_DM_ACK)<br/>  remove R339 0ohm_0402 (PBTN_OUT#)<br/>  remove R359 0ohm_0402 (DGPU_HOLD_RST#)<br/>  remove R16 0ohm_0402 (BKOFF#)<br/>  remove R448 0ohm_0402 (VGA_EDP_DET)<br/>  remove R533 0ohm_0402 (VGA_HDMI_DET)<br/>  remove R627 0ohm_0603 (+SPT_VCC)<br/><br/>ADD R39 0ohm_0402 LOCAL_DIM<br/>ADD R38 0ohm_0402 COLOR_ENG_EN<br/><br/>C242,C653,C332,C354,C678 change footprint to C_X(2pin)</div> | <div>E</div> <div>Compal Secret Data</div> <div>Compal Electronics, Inc.</div> <div>SCHEMATIC,MB A6911</div> <div>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. 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