# ZYB & ZYBA SYSTEM BLOCK DIAGRAM

A@ --> Arrandale use
E@ --> Discrete use
SW@ --> Switch use
IV@ --> UMA use

| | |
|---|---|
| GPU CORE PWR ISL6264 P44 | CHARGER ISL88731 P38 |
| GPU IO PWR ISL62827 P45 | 3/5V SYS PWR ISL6237 P39 |
| DISCHARGER +3V,+5V,+1.5V,+1.05V,+1.1V_VTT P47 | CPU CORE PWR ISL62882 P40 |
| +1.0V/+1.5V G93334 + Linear P47 | CPU VTT ARD: 1.05V CFD: 1.1V UP61111AQDD P41 |
| CPU VGFX_AXG ISL62881 P46 | VTT 1.05V UP61111AQDD P42 |
| THERMAL PROTECTION P48 | DDR3 PWR TPS5116 P43 |

CLOCK GENERATOR
SELGO: SLG8SP595V P3
X'TAL 14.318MHz

BCLK: 133MHz
PEG_CLK: 100MHz
DPLL_REF_SSCLK: 120MHz

DDR III
SO-DIMM 0
SO-DIMM 1
SO-DIMM 2
SO-DIMM 3 P14, 15 .16. 17

Dual Channel
800/ 1066 MHz
800 MT/s 1066 MT/s

DDR SYSTEM MEMORY

intel
<MCH Processor>
Clarksfield <Discrete only w/4 DIMM>*
Arrandale <UMA only>
Auburndale <UMA/SG>
rPGA 989
(37.5mm X 37.5mm)
P4.5.6.7
PCI-E X16
FDI
DMI

Fan Driver
(PWM Type) P36

CPU & PCH XDP Conn. P16

PCIE
2.5GT/s

AMD GPU
Broadway-Pro / Madison-Pro 1GB
P19,20,21,22,23,24,25,26

HDMI
CRT
LVDS

X'TAL 27.0MHz

*[Arrandale Only]

X4 DMI interface

LVDS_CRT_HDMI Switch Graphics
P25, 26

HDMI P26
CRT P25
LVDS P25

INT_HDMI *[Arrandale Only]
INT_CRT *[Arrandale Only]
INT_LVDS *[Arrandale Only]

Note:
HM55 does not support USB 6 & 7
HM55 does not support SATA 2 & 3

intel
<PCH>
Graphics Interfaces
SATA
3.0 GT/s
Ibex Peak_M
PCI-E
USB
mBGA 676
(27mm X 25mm)
P8.9.10.11.12.13
HDA
RTC P9
SPI
LPC

X'TAL 32.768KHz

HDD (SATA) *2
P31
SATA0
SATA5

ODD (SATA)
P31
SATA1

SATA4

PS8101 LS

PCI-Express
2.5GT/s

USB Port x 4
USB 1, 3, 11, 12 P34
USB 2.0

Bluetooth
USB 4 P36

CCD
USB 8 P29

Azalia

PCIE-1 & 2
CLKOUT_PEG_1&3

PCIE-6
CLKOUT_PEG_B

Mini Card WLAN / 2
USB 10 & 13 P32

USB10 & 13

Lan/B

Atheros
Giga-LAN
AR8151
P28

X'TAL 25MHz

Transformer P28

RJ45 Connector P28

Alcor
CardReader
AU6437

P26
Card Reader Connector

Relteak
Audio CODEC
ALC669X P29

SPI ROM
4MB x1 (Basic ME+Braidwood)
P9

Winbond
EC (WPC781) P37

SPI ROM P37

Touch Pad P36

Sub-Amplifier (TPA3111D1)

Rear Audio Amp & Head phone
GMT G1453L P30

SUBWOOFER P30
Main SPK P30
S/PDIF P30
Line in P30
MIC Jack P30
Int. D-MIC P125 P30
K/B COON. P36

SSID: DISCRETE: 030A
SSID: SWITCH GFX: 0308

SVID: 1025

PROJECT : ZYB & ZYBA
Quanta Computer Inc.

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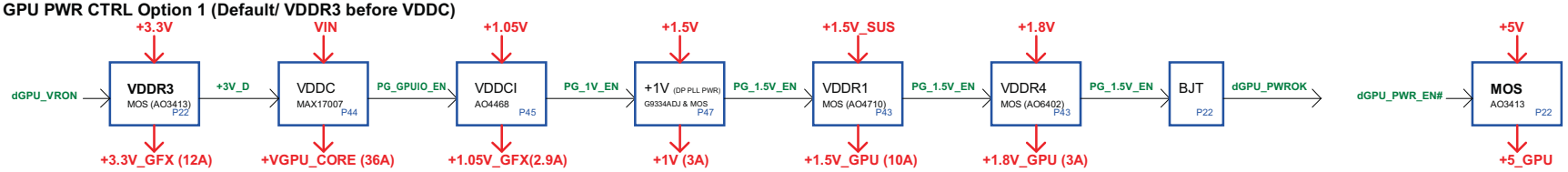
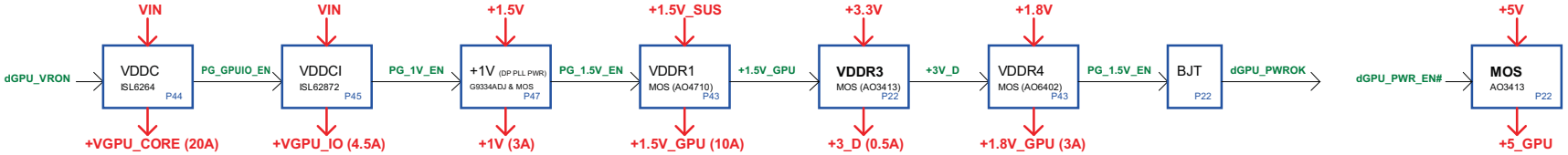
|---|---|---|
| | ZYB Block Diagram | 1A |
| Date: Tuesday, January 12, 2010 | Sheet 1 of 51 | |

## GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



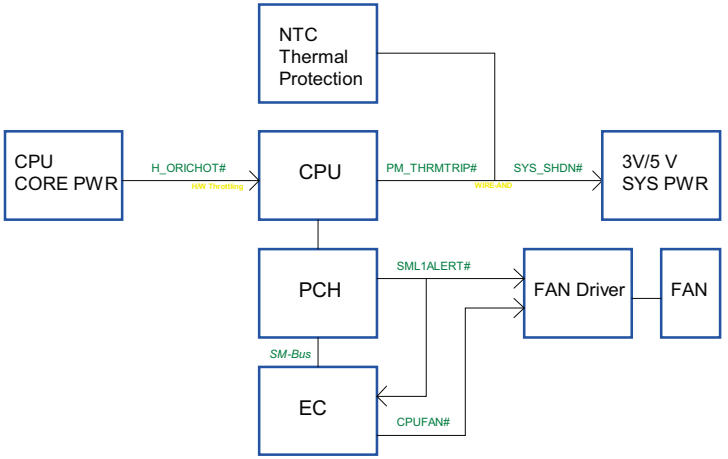

## GPU PWR CTRL Option 2 (VDDR3 after VDDR1)




### Power States

| POWER PLANE | VOLTAGE | DESCRIPTION | CONTROL SIGNAL | ACTIVE IN |
|---|---|---|---|---|
| VIN | +10V~+19V | MAIN POWER | ALWAYS | ALWAYS |
| +VCCRTC | +3V~+3.3V | RTC POWER | ALWAYS | ALWAYS |
| +3VPCU | +3.3V | EC POWER | ALWAYS | ALWAYS |
| +5VPCU | +5V | CHARGE POWER | ALWAYS | ALWAYS |
| +15V | +15V | CHARGE PUMP POWER | ALWAYS | ALWAYS |
| +3V_S5 | +3.3V | LAN/BT/CIR POWER | S5_ON | S0-S5 |
| +5V_S5 | +5V | USB POWER | S5_ON | S0-S5 |
| +5V | +5V | HDD/ODD/Codec/TP/CRT/HDMI POWER | MAINON | S0 |
| +3V | +3.3V | PCH/GPU/Peripheral component POWER | MAINON | S0 |
| +1.5V_SUS | +1.5V | CPU/SODIMM CORE POWER | SUSON | S0-S3 |
| +0.75V_DDR_VTT | +0.75V | SODIMM Termination POWER | MAINON | S0 |
| +VGFX_AXG | variation | Internal GPU POWER | GFX_ON | S0 |
| +1.8V | +1.8V | CPU/PCH/Braidwood POWER | MAINON | S0 |
| +1.5V | +1.5V | MINI CARD/NEW CARD POWER | MAINON | S0 |
| +1.1V_VTT | +1.05V or +1.1V | CPU VTT POWER | MAINON | S0 |
| +1.05V | +1.05V | PCH CORE POWER | MAINON | S0 |
| +VCC_CORE | variation | CPU CORE POWER | VRON | S0 |
| LCDVCC | +3.3V | LCD POWER | LVDS_VDDEN | S0 |
| +VGPUCORE | +0.9V~+1.1V | GPU CORE POWER | dGPU_VRON | Discrete enable |
| +1.05V_GFX | +0.9V~+1.1V | GPU I/O POWER | dGPU_VRON | Discrete enable |
| +1.5V_GFX | +1.5V | VRAM CORE POWER | dGPU_VRON | Discrete enable |
| +1.8V_VGA | +1.8V | LVDS/PLL POWER | dGPU_VRON | Discrete enable |
| +3.3V_GFX | +3.3V | PEG/HDMI/CRT POWER | dGPU_VRON | Discrete enable |
| | | | | |

### Thermal Follow Chart

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| Size | Document Number | Rev |
|---|---|---|
| | PWR Status & GPU PWR CRL & THRM | 1A |

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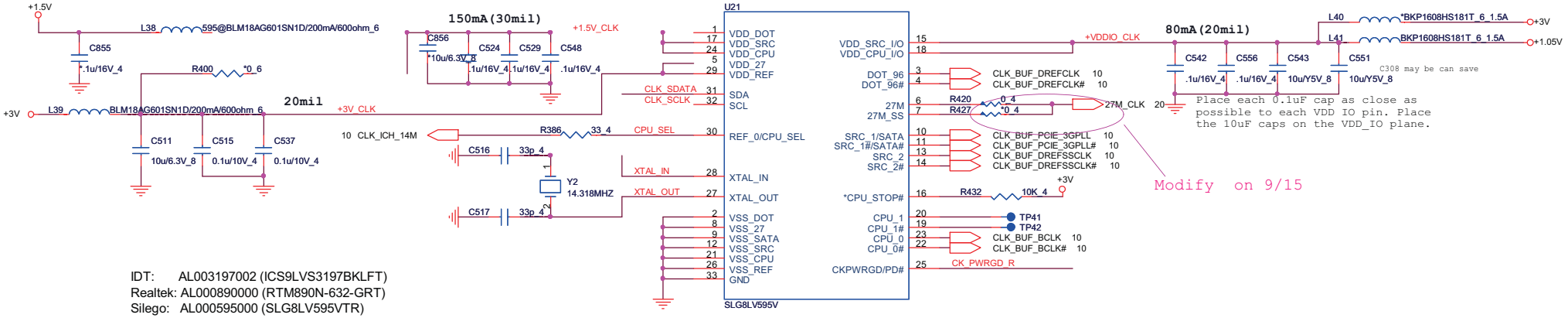
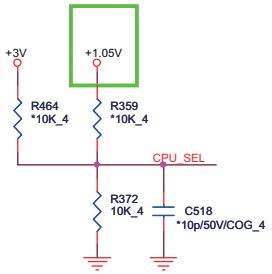


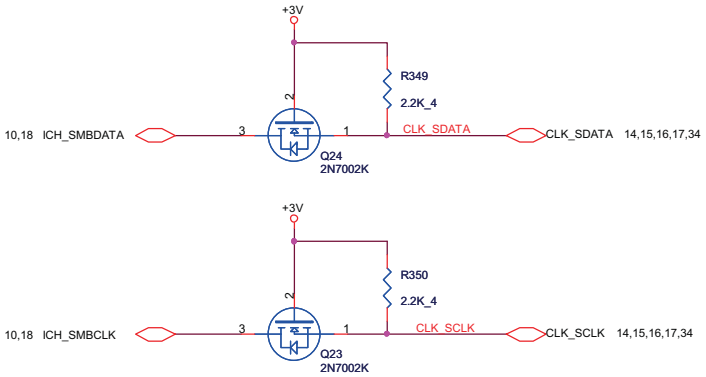

IDT: AL003197002 (ICS9LVS3197BKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

## CPU_CLK select

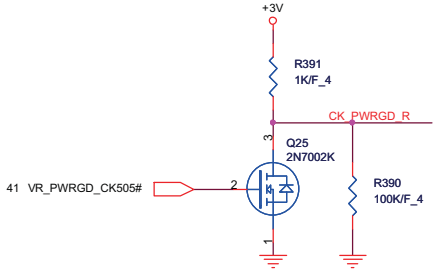



| | 0 | 1 |
|---|---|---|
| CPU_SEL | CPU0/1=133MHz (default) | CPU0/1=100MHz |

## SMBus




## CLK Enable

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| Size | Document Number | Rev |
|---|---|---|
| | Clock Generator | 1A |
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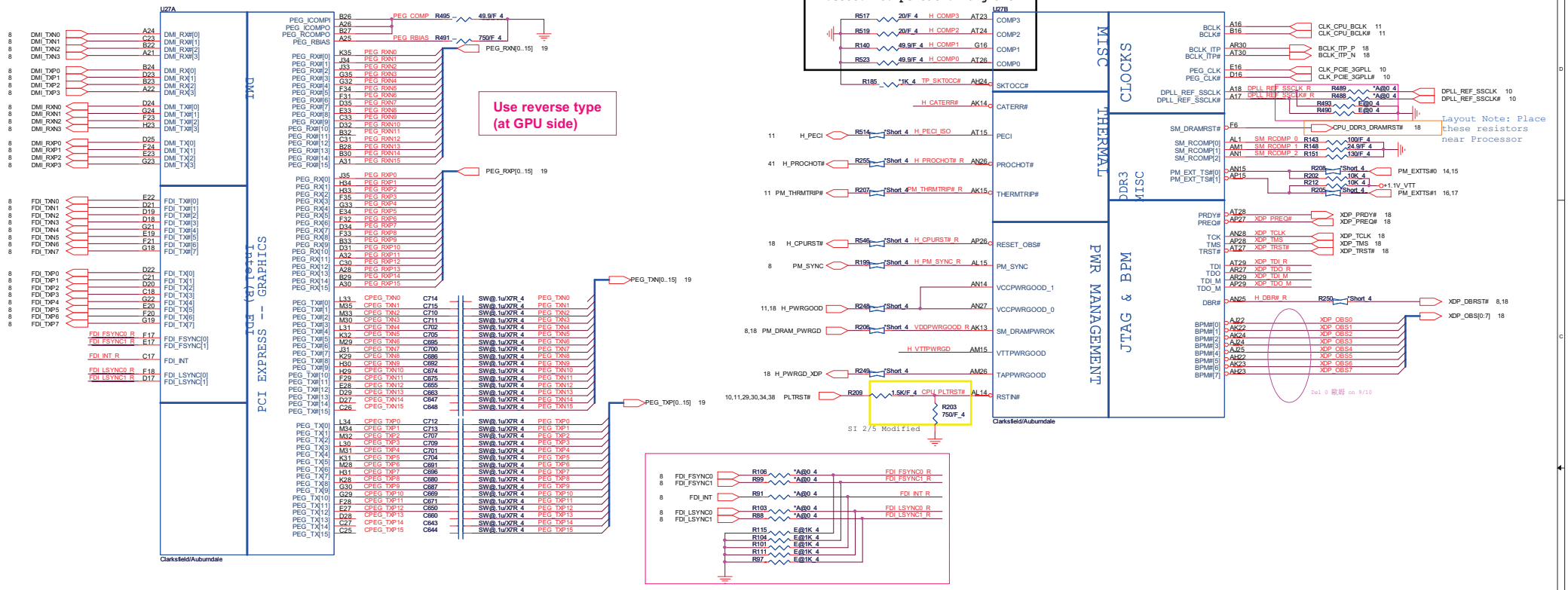
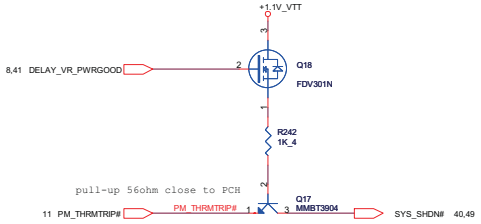
# AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

# AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

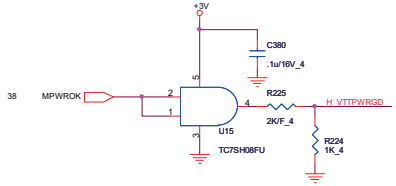
4



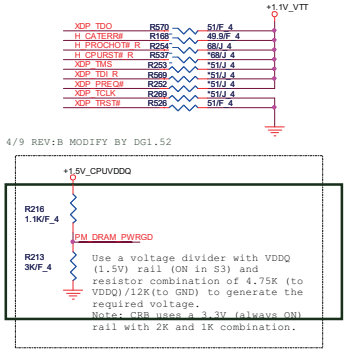

## Thermaltrip protect



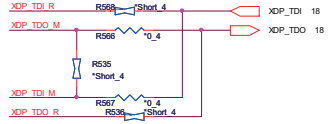

## VTT PWR_Good




## Processor pull-up




## JTAG MAPPING




| | |
|---|---|
| Scan Chain (Default) | STUFF -> R469, R491, R507<br>NO STUFF -> R489, R490 |
| CPU Only | STUFF -> R490, R491<br>NO STUFF -> R469, R489, R507 |
| GMCH Only | STUFF -> R489, R507<br>NO STUFF -> R491, R490, R469 |

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| | AUBURNDA 1/4 | 1A |
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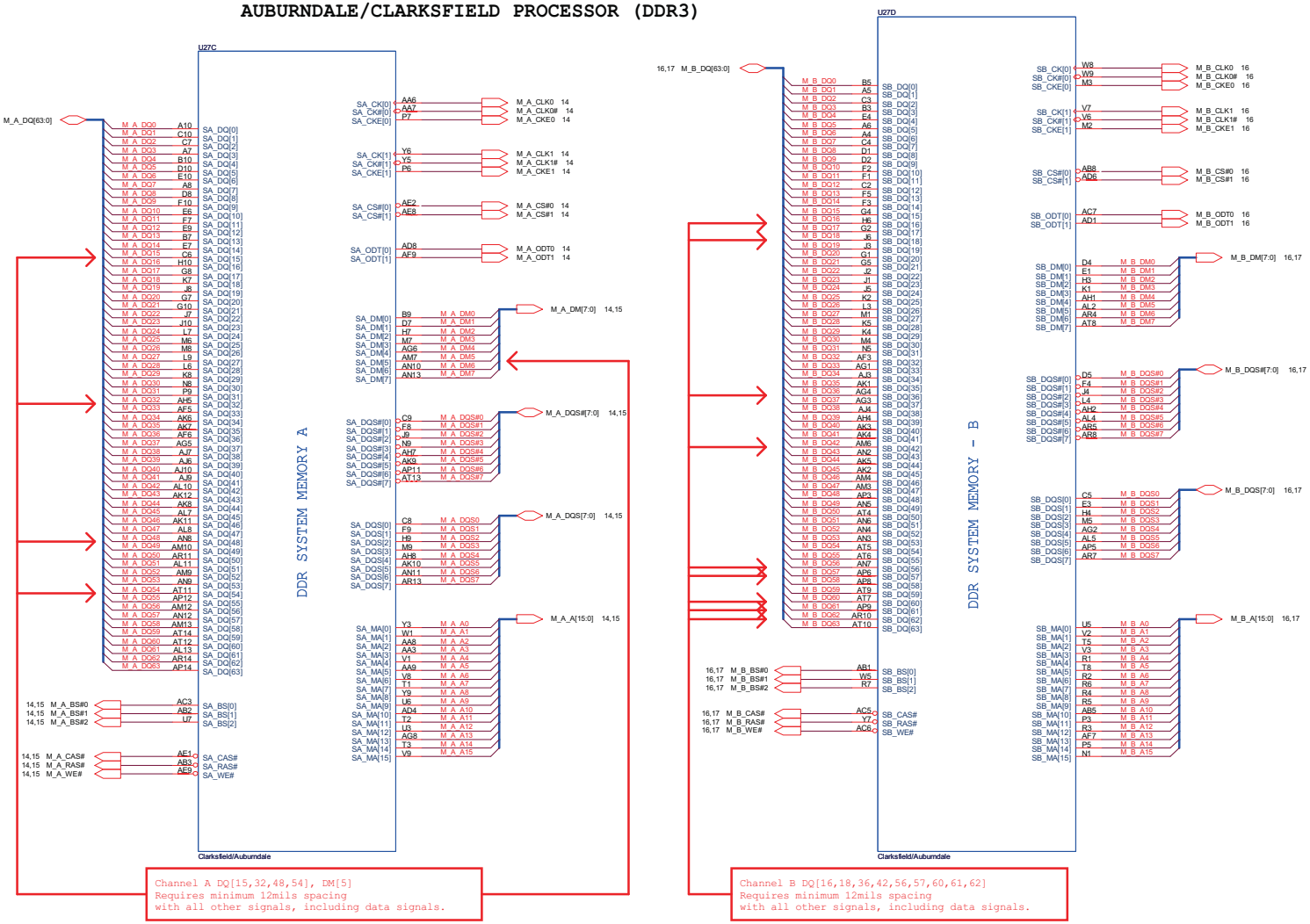
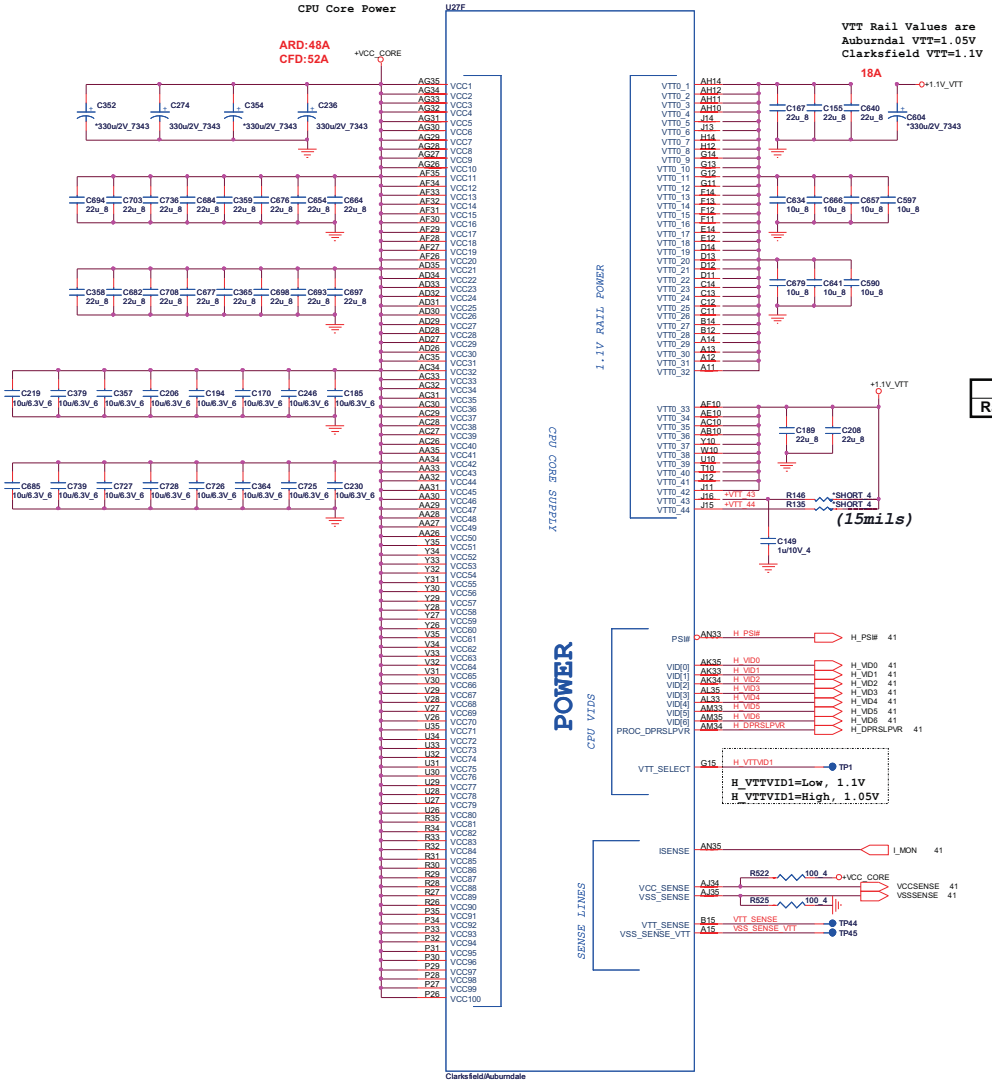
# AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

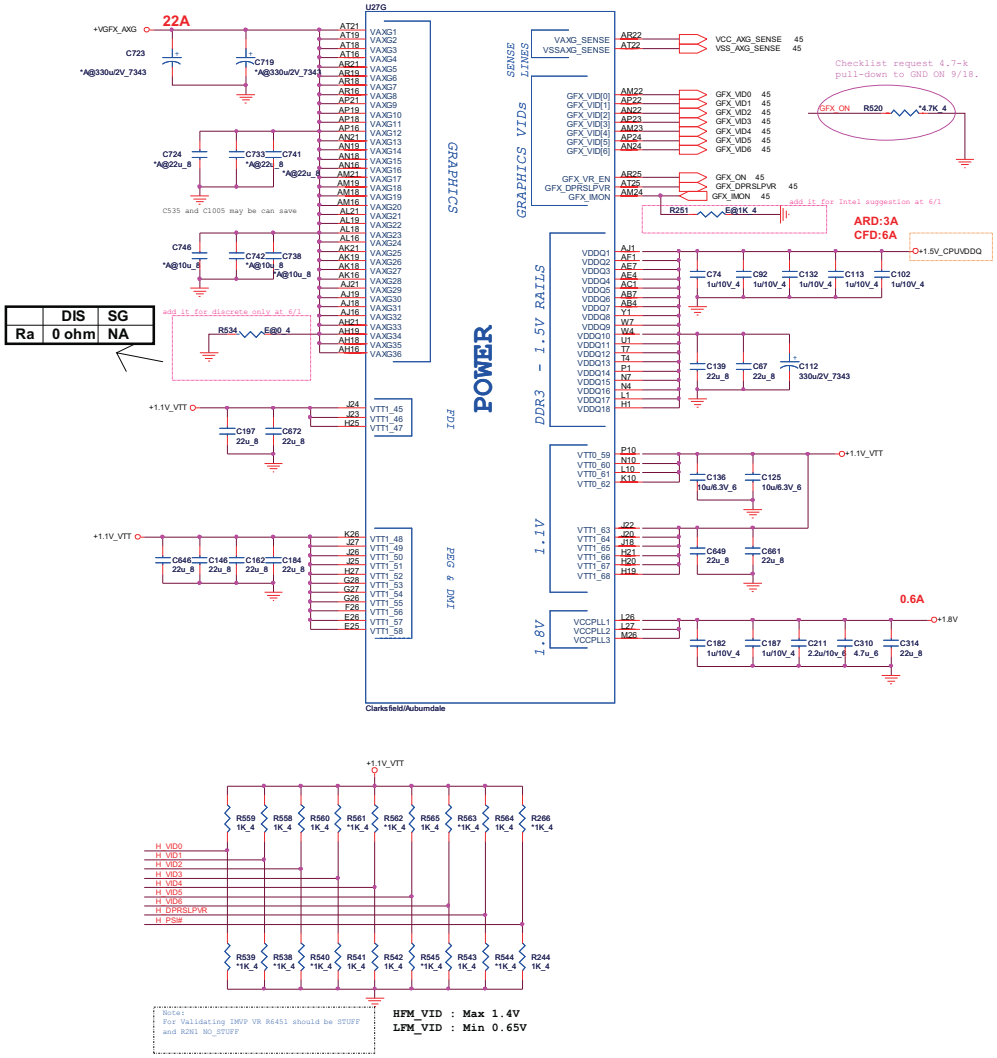



| | | |
|---|---|---|
| Quanta Computer Inc. | PROJECT : ZYB & ZYBA | |
| Size | Document Number: AUBURNDA 2/4 | Rev: 1A |
| Date: Tuesday, January 19, 2010 | Sheet 5 of 51 | |

# AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)




# AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)





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Document Number
AUBURNDA 3/4 (PWR)
Rev
1A
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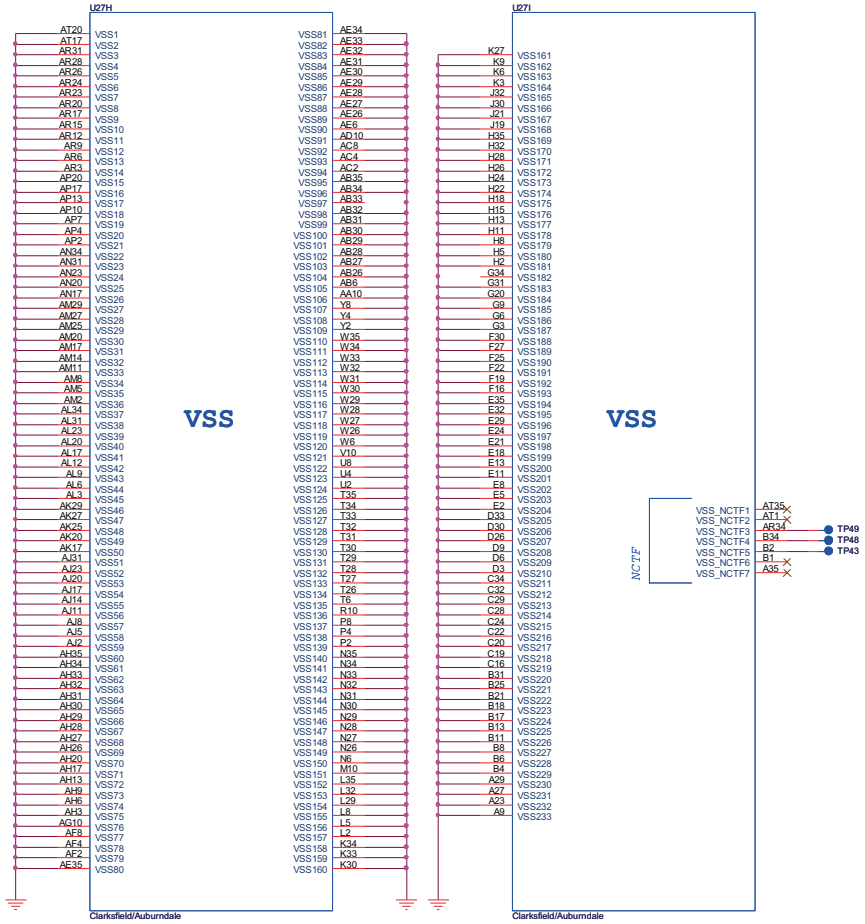
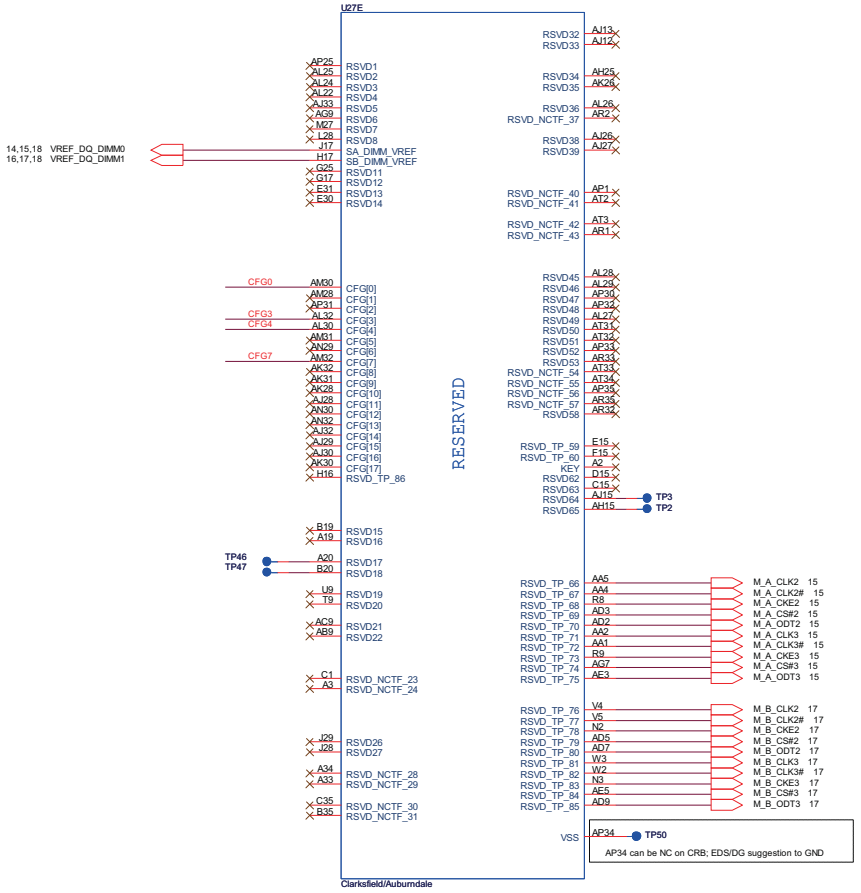
## AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

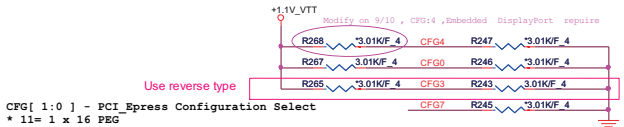



## AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)




### Processor Strapping

| | 1 | 0 |
|---|---|---|
| CFG4 (Display Port Presence) | Disabled; No Physical Display Port attached to Embedded Diplay Port | Enabled; An external Display port device is connected to the Embedded Display port |
| CFG0 (PCI-Epress Configuration Select) | Single PEG | Bifurcation enabled |
| CFG3 (PCI-Epress Static Lane Reversal) | Normal Operation | Lane Numbers Reversed |




CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.(ES1 only)

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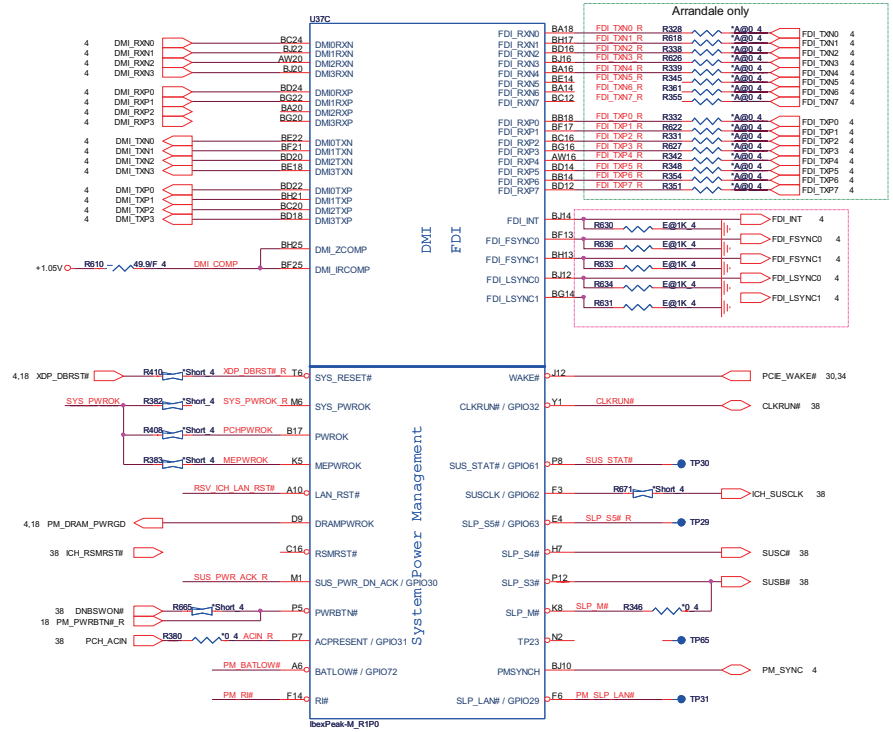
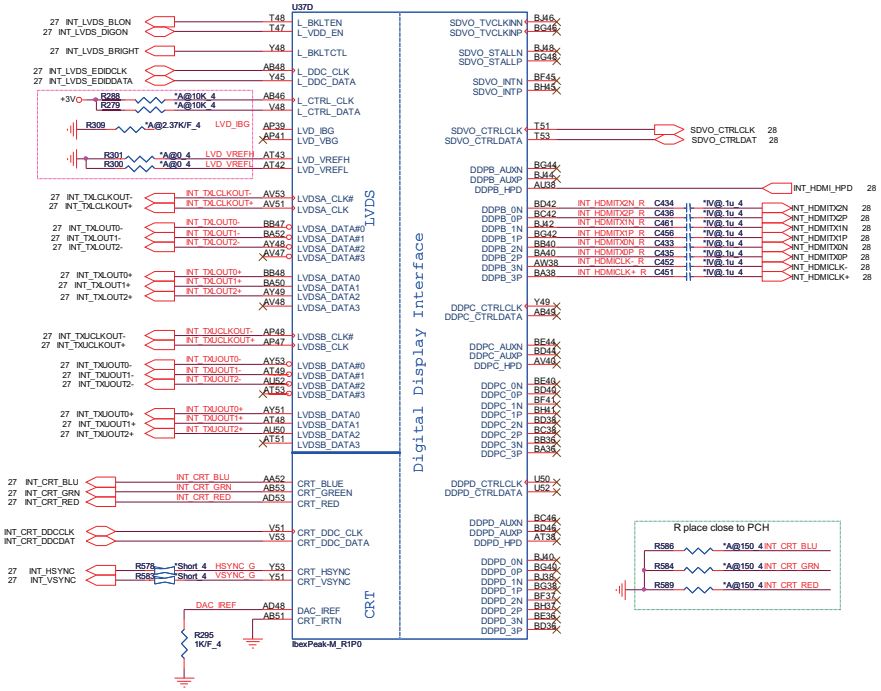
|---|---|---|
| | AUBURNDA 4/4 | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 7 of 51 | |

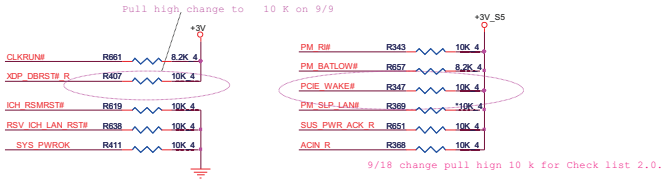
# IBEX PEAK-M (DMI,FDI,GPIO)



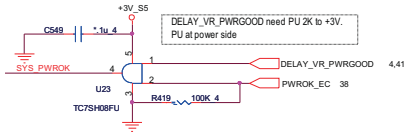



## PCH Pull-high/low




## System PWR_OK

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| Size | Document Number | Rev |
|---|---|---|
| | IBEX PEAK-M 1/6 | 1A |
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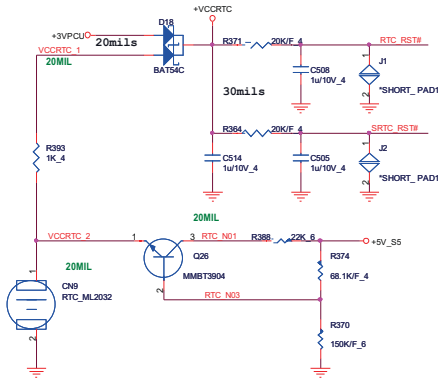
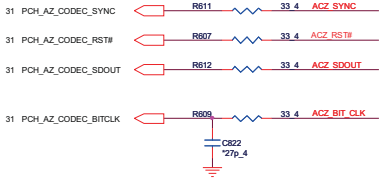
# IBEX PEAK-M (HDA,JTAG,SATA)

## RTC Circuitry




## HDA Bus

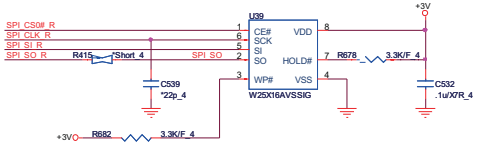


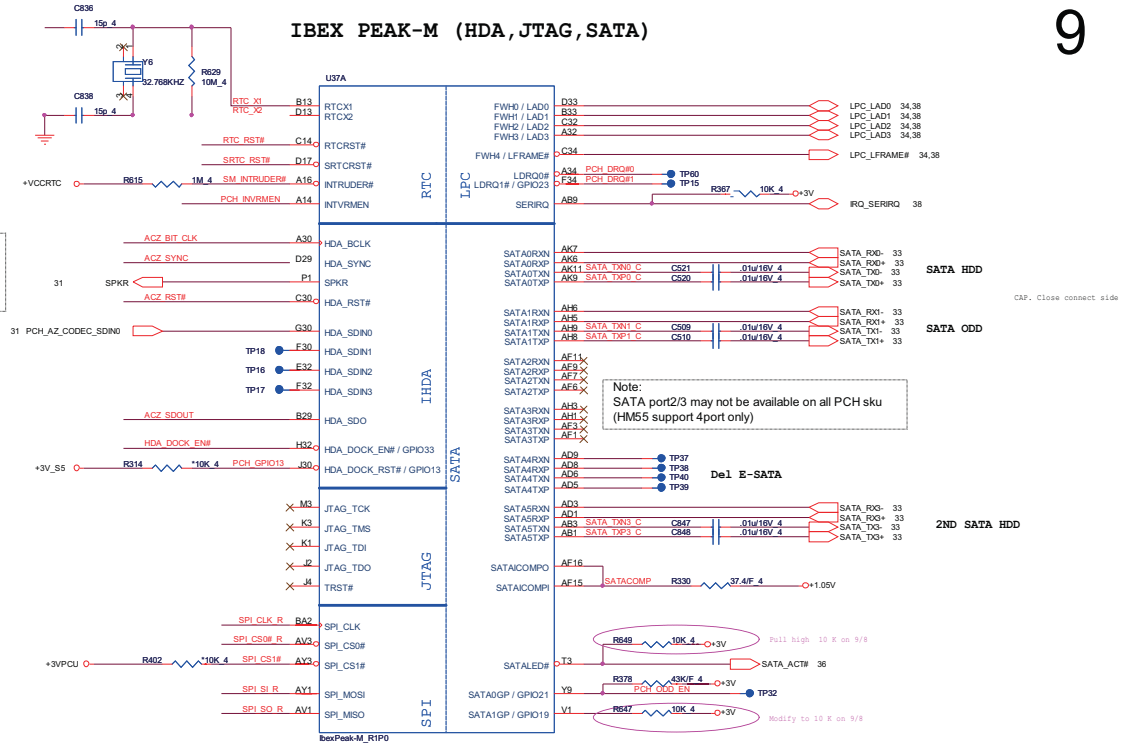

Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

## HDA Bus for Modem(CLG)

HDA Bus for Modem(CLG)

## PCH SPI




## PCH Strap Table

| Pin Name | Strap description | Sampled | Configuration | ZY9B note |
|---|---|---|---|---|
| SPKR | No reboot mode setting | PWROK | 0 = Default (weak pull-down 20K)<br>1 = Setting to No-Reboot mode | +3V R650 *10K_4 SPKR |
| INIT3_3V | Reserved | PWROK | 1 = Default (weak pull-up 20K)<br>Should not be pull-down | |
| GNT3# / GPIO55 | Top-Block Swap Override | PWROK | 0 = "top-block swap" mode<br>1 = Default (weak pull-up 20K) | R582 *10K_4 PCI_GNT3# 10 |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | Should be always pull-up | +VCCRTC R625 330K_4 PCH_INVRMEN |
| GNT1# / GPIO51 | Boot BIOS Selection 1 [bit-1] | PWROK | GNT1# / GNT0# / Boot Location<br>1 / 1 / SPI<br>1 / 0 / PCI<br>0 / 0 / LPC | Default weak pull-up on GNT0/1#<br>[Need external pull-down for LPC BIOS]<br>+3V R293 *1K_4 R305 *1K_4<br>R298 1K_4 R299 1K_4<br>PCI_GNT0# 10<br>PCI_GNT1# 10 |
| GNT0# | Boot BIOS Selection 0 [bit-0] | PWROK | | |
| GNT2# / GPIO53 | ESI strap (Server only) | PWROK | Should not be pull-down<br>(weak pull-up 20K) | USE GPIO PIN |
| NV_ALE | Intel Anti-Theft HDD protection | PWROK | 0 = Disable (Internal pull-down 32ohm) | +1.8V R373 *1K_4 NV_ALE NV_ALE 10 |
| NV_CLE | DMI Termination voltage | PWROK | weak pull-down 32ohm | +1.8V R366 *1K_4 NV_CLE NV_CLE 10 |
| HDA_DOCK_EN#/GPIO33 | Flash Descriptor Security | PWROK | 0 = Override<br>1 = Default (weak pull-up 20K) | +3V R307 *1K_4 R303 *10K_4 HDA_DOCK_EN# |
| SPI_MOSI | iTPM function Disable | MEPWROK | 0 = Default (weak pull-down 20K)<br>1 = Enable | +3V R392 *1K_4 SPI_SI_R |
| HDA_SDO | Reserved | RSMRST# | Should not be pull-up<br>(weak pull-down 20K) | |
| GPIO8 | Reserved | RSMRST# | Should not be pull-down<br>(weak pull-up 20K) | +3V_S5 R357 10K_4 RSV_GPIO8 11 |
| GPIO27 | On-die PLL Voltage Regulator | RSMRST# | 0 = Disable<br>1 = Enable (weak pull-up 20K) | |
| HDA_SYNC | On-die PLL PWR supply select | RSMRST# | 0 = 1.8V supply (weak pull-down 20K)<br>1 = 1.5V supply | use defaul (0 = 1.8V supply) |
| GPIO15 | Reserved | RSMRST# | 0 = TLS no Confidentiality<br>(weak pull-down 20K)<br>1 = TLS Confidentiality | +3V_S5 R365 1K_4 CR_WAKE# 11 |

| | |
|---|---|
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| Quanta Computer Inc. | |
| Size | Document Number: IBEX PEAK-M 2/6 — Rev: 1A |
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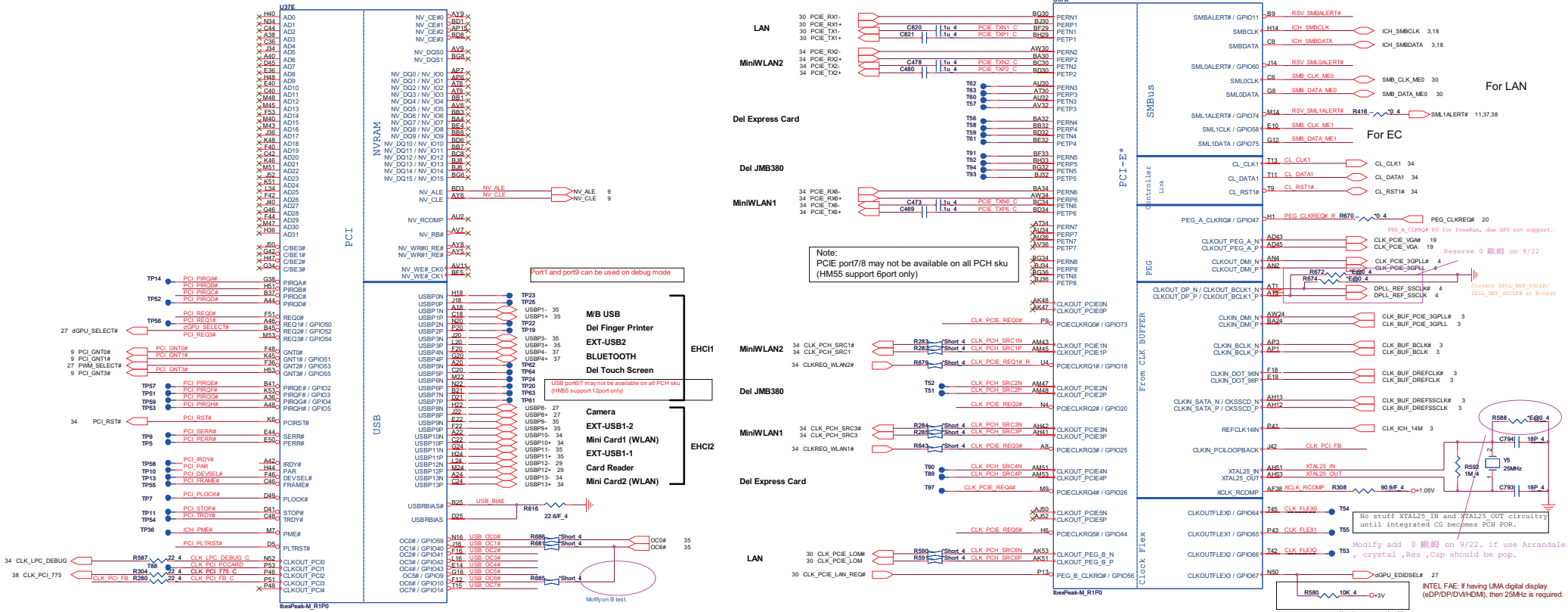
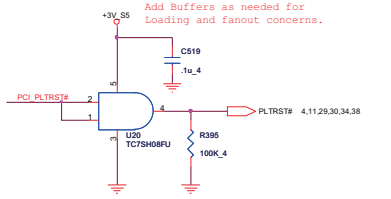
# IBEX PEAK-M (PCI,USB,NVRAM)

# IBEX PEAK-M (PCI-E,SMBUS,CLK)

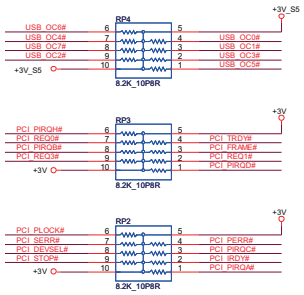




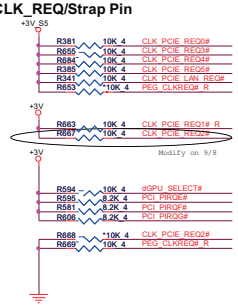

## PLTRST#




## PCI/USBOC# Pull-up




## CLK_REQ/Strap Pin




PEG_A_CLKRQ# PD for FreeRun, due GPU not support.

**A16 swap override Strap/Top-Block Swap Override jumper**

| | |
|---|---|
| PCI_GNT3# | Low = A16 swap override/Top-Block Swap Override enabled<br>High = Default |

**Boot BIOS Strap**

| GNT0# | GNT1# | Boot BIOS Location |
|---|---|---|
| 0 | 0 | LPC |
| 0 | 1 | Reserved (NAND) |
| 1 | 0 | PCI |
| 1 | 1 | SPI |

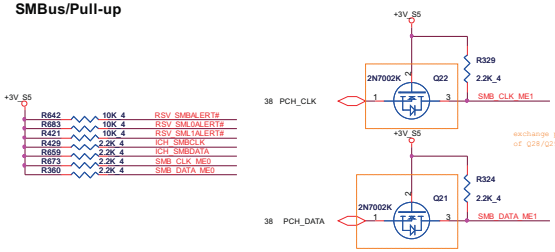
**Danbury Technology Enabled**

| | |
|---|---|
| NV_ALE | High = Enable<br>Low = Disable |

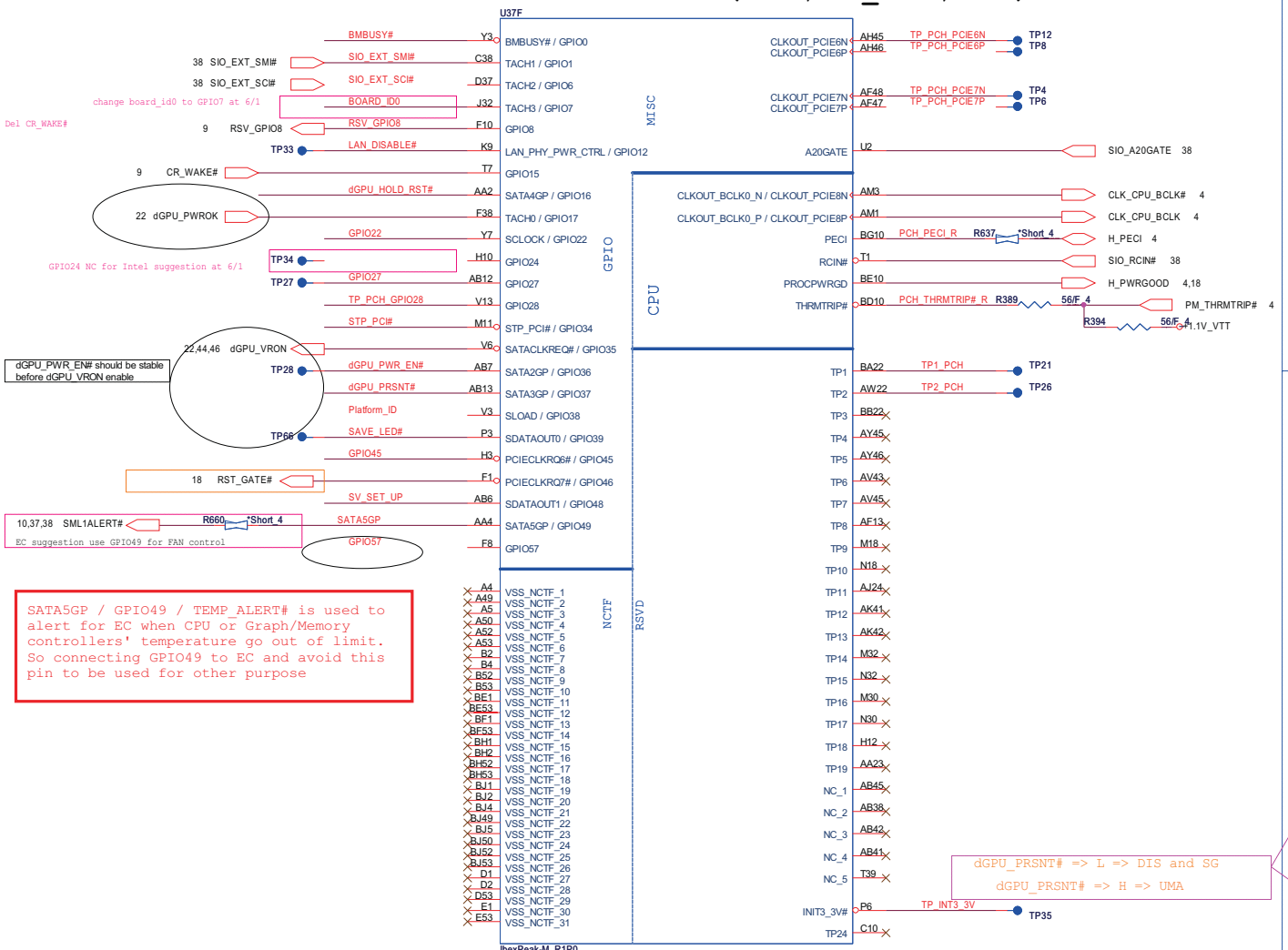
**DMI Termination Voltage**

| | |
|---|---|
| NV_CLE | Set to Vcc when LOW<br>Set to Vcc/2 when HIGH |

## SMBus/Pull-up

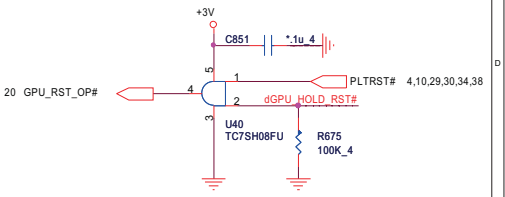


# IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

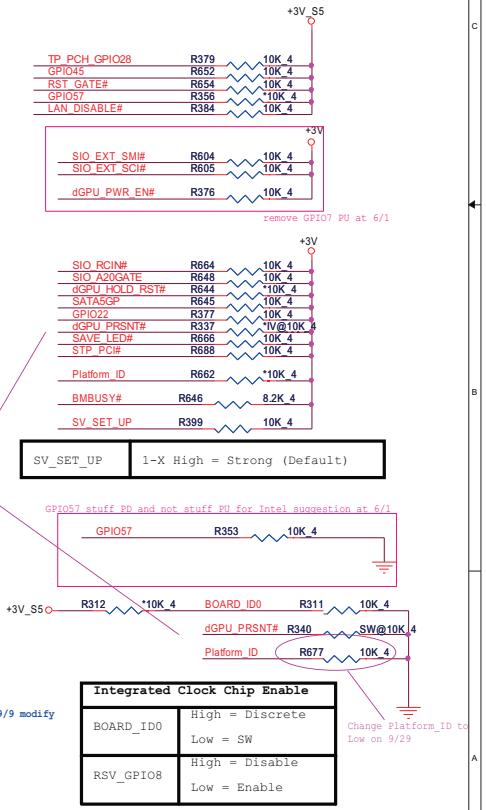



SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

## GPU RST#




## GPIO Pull-up/Pull-down




| SV_SET_UP | 1-X High = Strong (Default) |
|---|---|

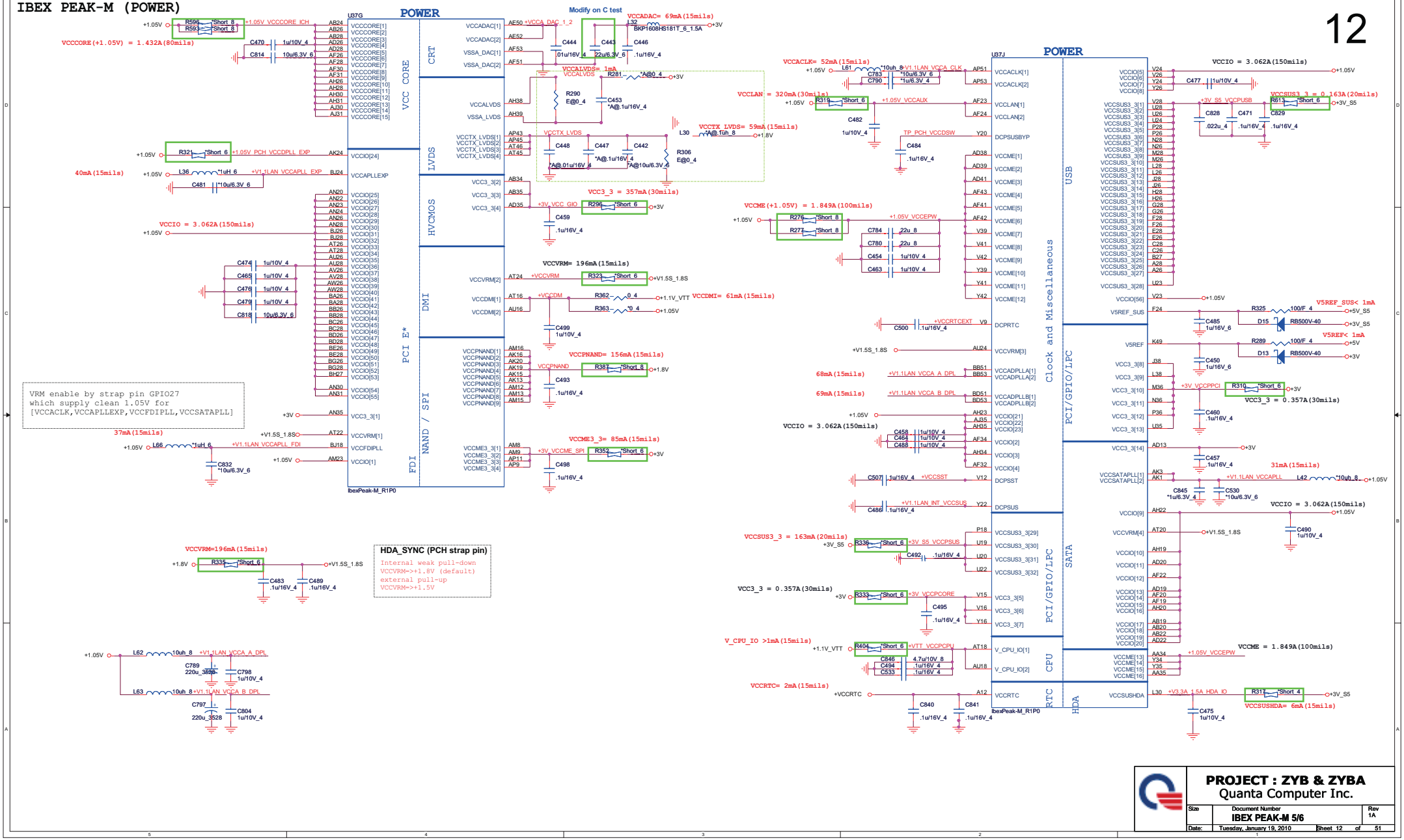
| Integrated Clock Chip Enable | |
|---|---|
| BOARD_ID0 | High = Discrete<br>Low = SW |
| RSV_GPIO8 | High = Disable<br>Low = Enable |

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | IBEX PEAK-M 4/6 | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 11 of 51 | |

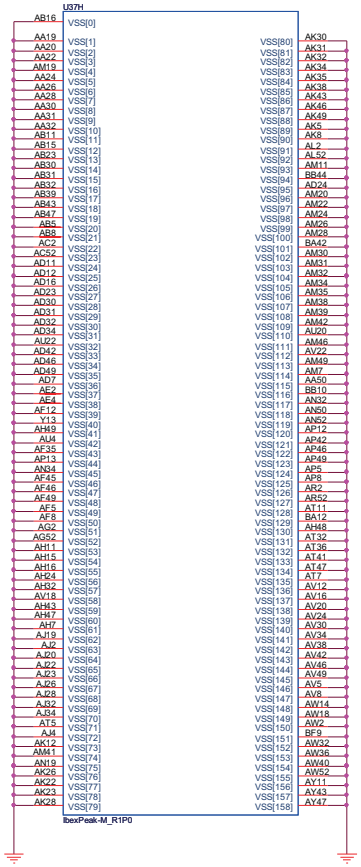
# IBEX PEAK-M (POWER)

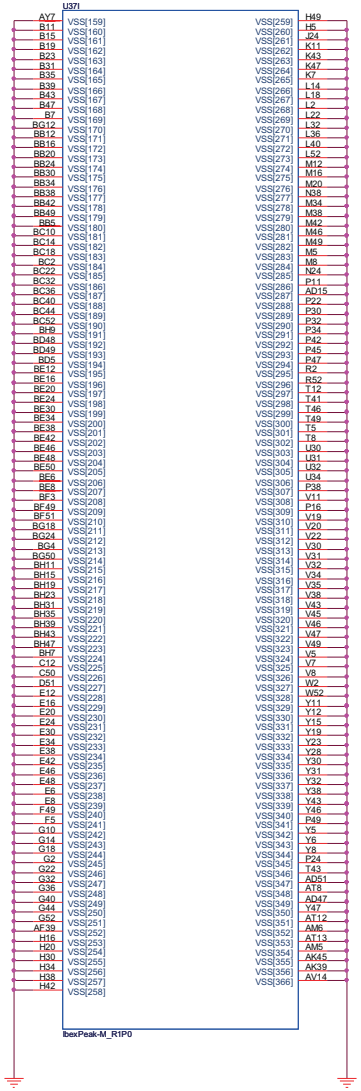





| | | | |
|---|---|---|---|
| PROJECT : ZYB & ZYBA<br>Quanta Computer Inc. | | | |
| Size | Document Number<br>IBEX PEAK-M 5/6 | | Rev<br>1A |
| Date: Tuesday, January 19, 2010 | Sheet 12 | of | 51 |

# IBEX PEAK-M (GND)



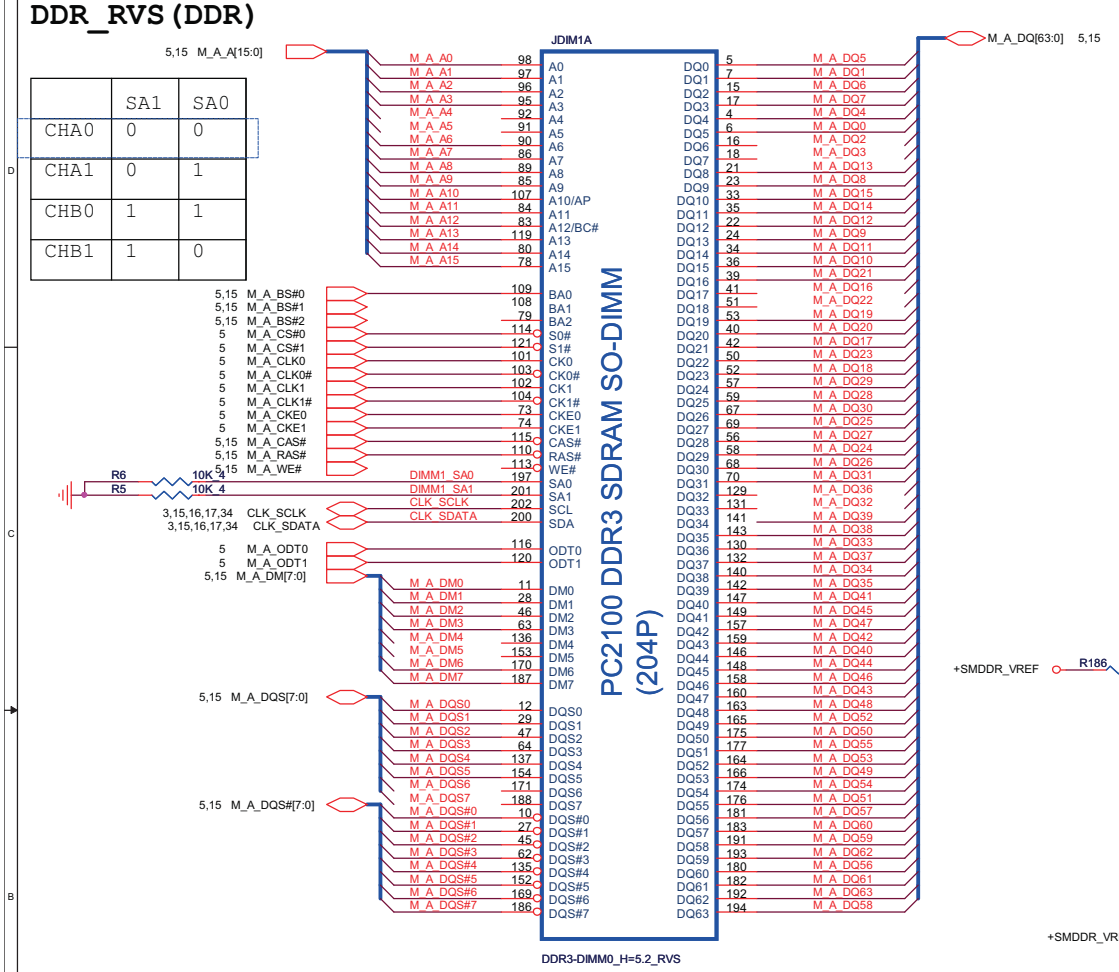

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

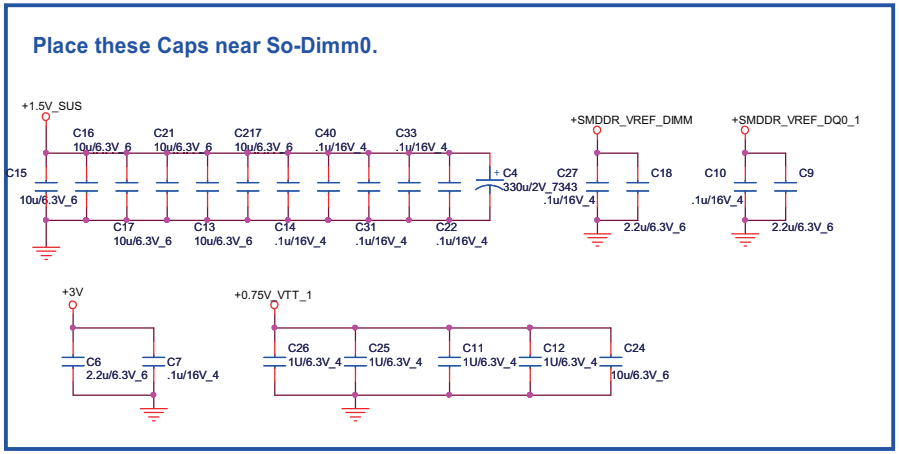
| Size | Document Number | Rev |
|---|---|---|
| | IBEX PEAK-M 6/6 | 1A |
| Date: Tuesday, January 12, 2010 | Sheet 13 of 51 | |

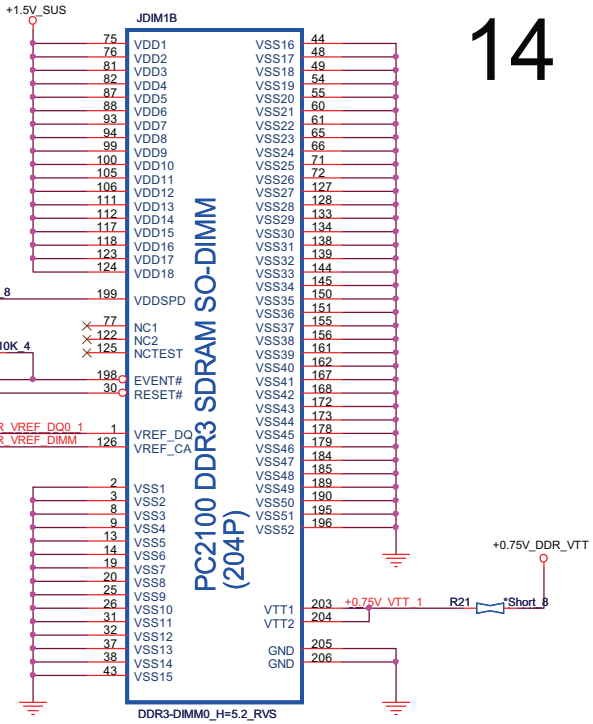
# DDR_RVS (DDR)

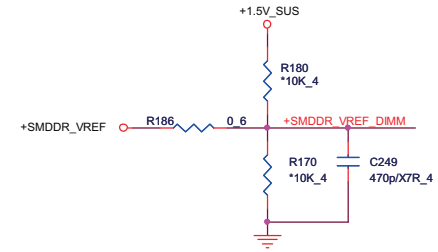


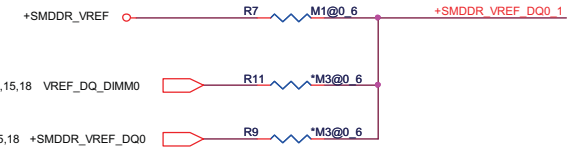
| | SA1 | SA0 |
|---|---|---|
| CHA0 | 0 | 0 |
| CHA1 | 0 | 1 |
| CHB0 | 1 | 1 |
| CHB1 | 1 | 0 |




DM signals are not present on Clarksfield processor. All DM signals can be left as No Connect on Clarksfield and connected directly to GND on SO-DIMM side for Clarksfield only designs.

15,16,17,18,44 +0.75V_DDR_VTT
15,16,17,18,44 +1.5V_SUS
15,16,17,44 +SMDDR_VREF
3,4,8,9,10,11,12,15,16,17,22,27,28,29,31,32,34,36,37,38,40,41,46,48 +3V

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-0 | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 14 of 51 | |

# DDR_RVS (DDR)



| | SA1 | SA0 |
|---|---|---|
| CHA0 | 0 | 0 |
| CHA1 | 0 | 1 |
| CHB0 | 1 | 1 |
| CHB1 | 1 | 0 |

JDIM2A

PC2100 DDR3 SDRAM SO-DIMM (204P)

E@DDR3-DIMM0_H=9.2_RVS

JDIM2B

PC2100 DDR3 SDRAM SO-DIMM (204P)

2.48A

E@DDR3-DIMM0_H=9.2_RVS

## Place these Caps near So-Dimm0.

maybe can save

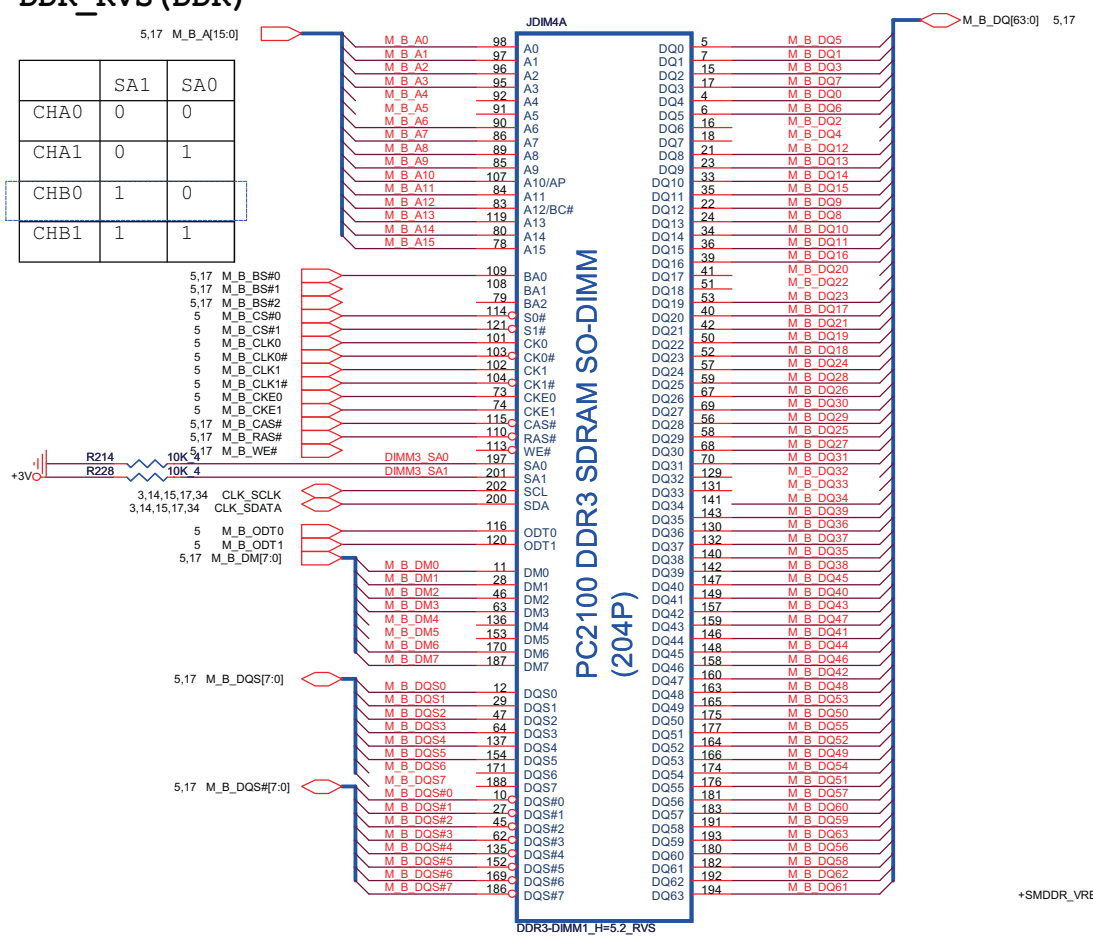
Close to SO-DIMM

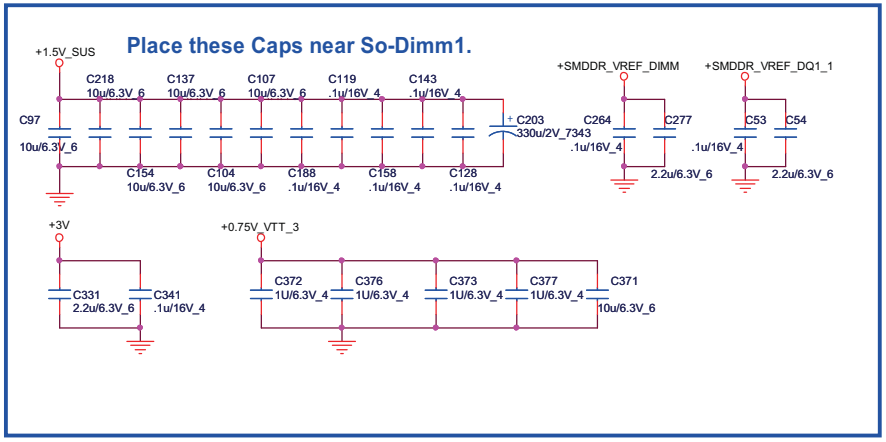
| | |
|---|---|
| PROJECT : | ZYB & ZYBA |
| Quanta Computer Inc. | |
| Size | Document Number: DDRIII SO-DIMM-0 |
| Rev | 1A |
| Date: | Tuesday, January 19, 2010 |
| Sheet | 15 of 51 |

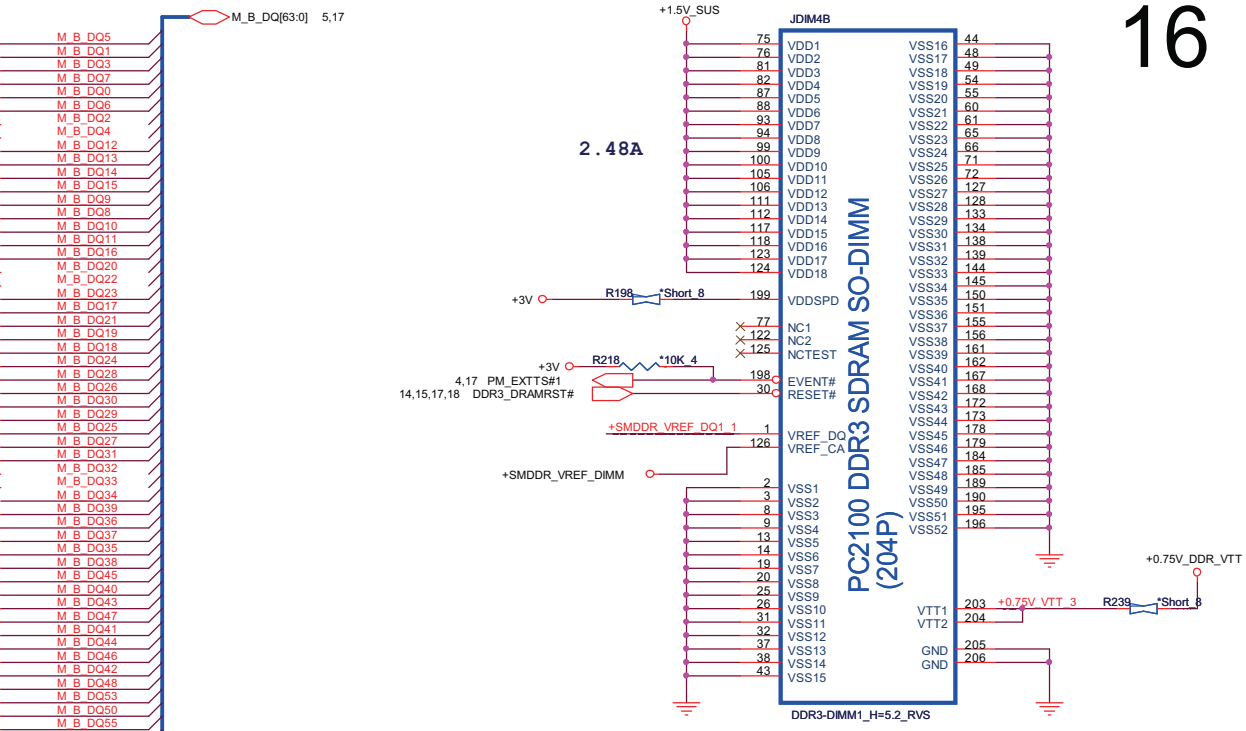
# DDR_RVS (DDR)

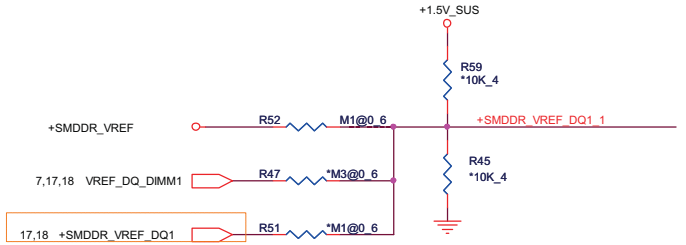


| | SA1 | SA0 |
|---|---|---|
| CHA0 | 0 | 0 |
| CHA1 | 0 | 1 |
| CHB0 | 1 | 0 |
| CHB1 | 1 | 1 |




14,15,17,18,44 +0.75V_DDR_VTT
14,15,17,18,44 +1.5V_SUS
14,15,17,44 +SMDDR_VREF
3,4,8,9,10,11,12,14,15,17,22,27,28,29,31,32,34,36,37,38,40,41,46,48 +3V

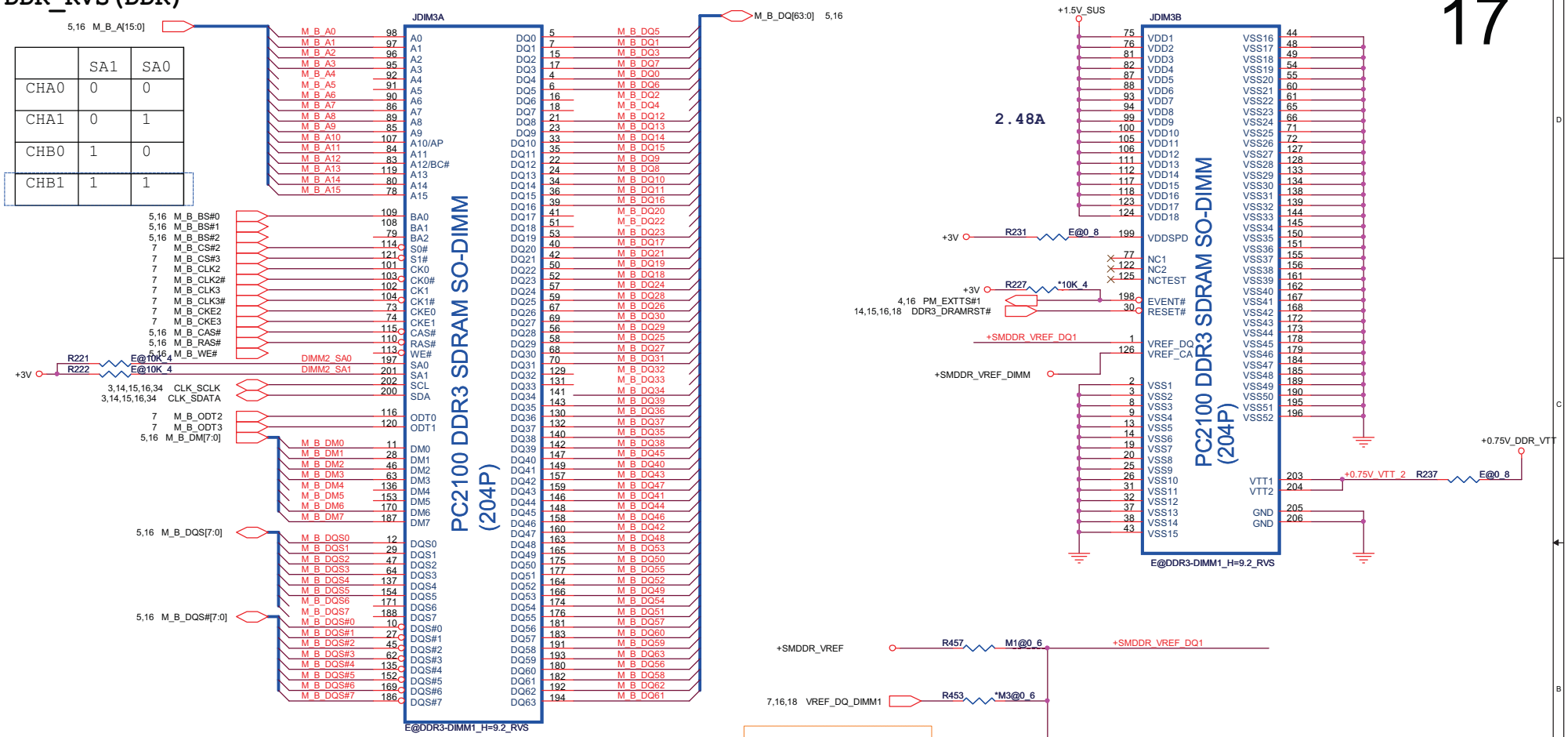
**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-1 | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 16 of 51 | |

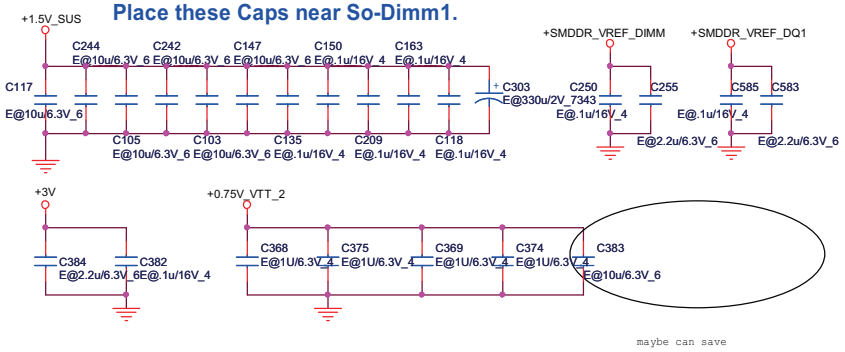
# DDR_RVS (DDR)



| | SA1 | SA0 |
|---|---|---|
| CHA0 | 0 | 0 |
| CHA1 | 0 | 1 |
| CHB0 | 1 | 0 |
| CHB1 | 1 | 1 |




## Place these Caps near So-Dimm1.

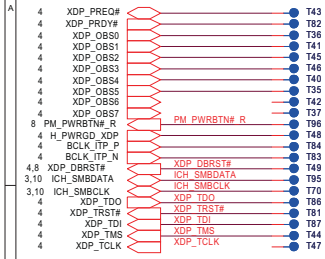



14,15,16,18,44 +0.75V_DDR_VTT
14,15,16,18,44 +1.5V_SUS
14,15,16,44 +SMDDR_VREF
3,4,8,9,10,11,12,14,15,16,22,27,28,29,31,32,34,36,37,38,40,41,46,48 +3V

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | DDRIII SO-DIMM-1 | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 17 of 51 | |

## Del CPU XDP Connector

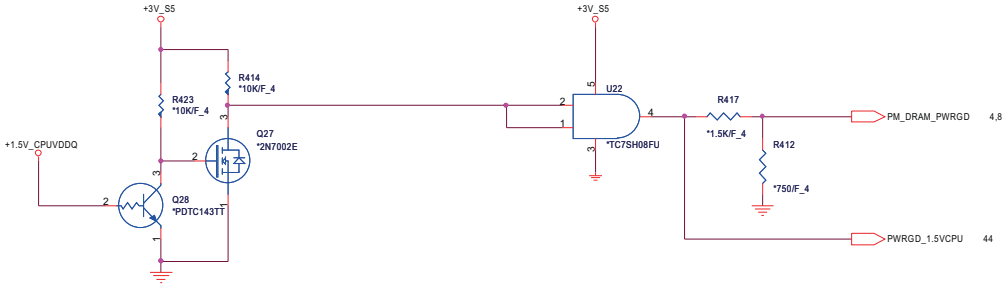


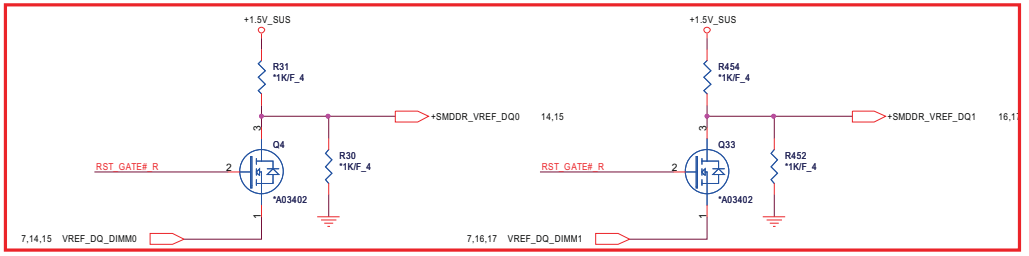


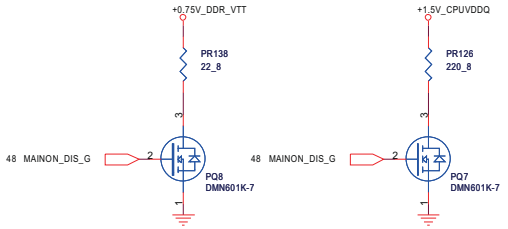
## Del Braidwood

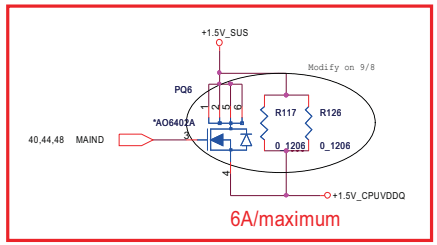


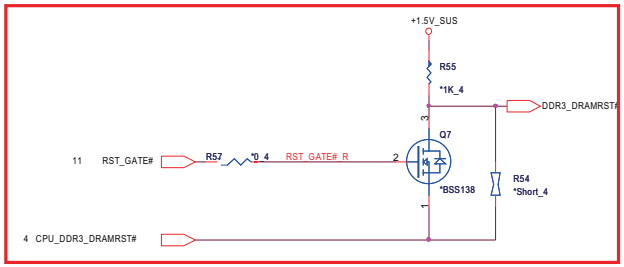
## S3 leakage solution(CLG)



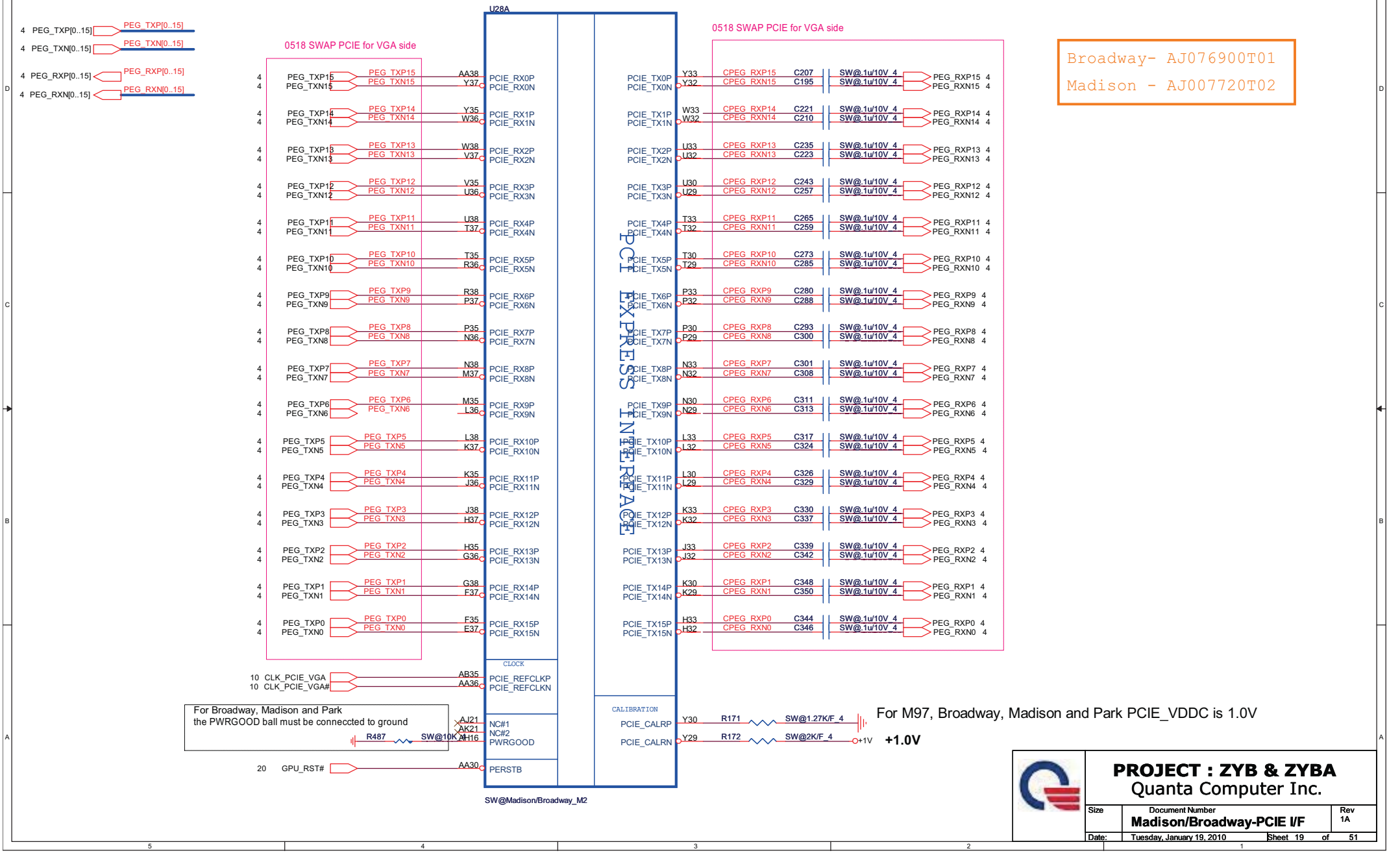





**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | XDP | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 18 of 51 | |


U28A
0518 SWAP PCIE for VGA side
0518 SWAP PCIE for VGA side
PCI EXPRESS INTERFACE
CLOCK
CALIBRATION
SW@Madison/Broadway_M2
For Broadway, Madison and Park
the PWRGOOD ball must be connecctd to ground
For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V
+1.0V
Broadway- AJ076900T01
Madison - AJ007720T02
PROJECT : ZYB & ZYBA
Quanta Computer Inc.
Madison/Broadway-PCIE I/F
Tuesday, January 19, 2010
Sheet 19 of 51

## GPU Power-on sequence

1 => +VGPU_CORE
2 => +VGPU_IO
3 => +1V
4 => +1.5V_GPU
5 => +3V_D
6 => +1.8V_GPU
7 => dGPU_PWROK

1.8V GPIO

3.3V GPIO

U28B

U28G

SW@Madison/Broadway_M2

SW@Madison/Broadway_M2

For EMI

(1.8V@70mA AVDD)

(1.8V@100mA VDD1DI)

(1.8V@2mA A2VDDQ)

(3.3V@130mA A2VDD)

HDMI

Display Port

LVDS

CRT

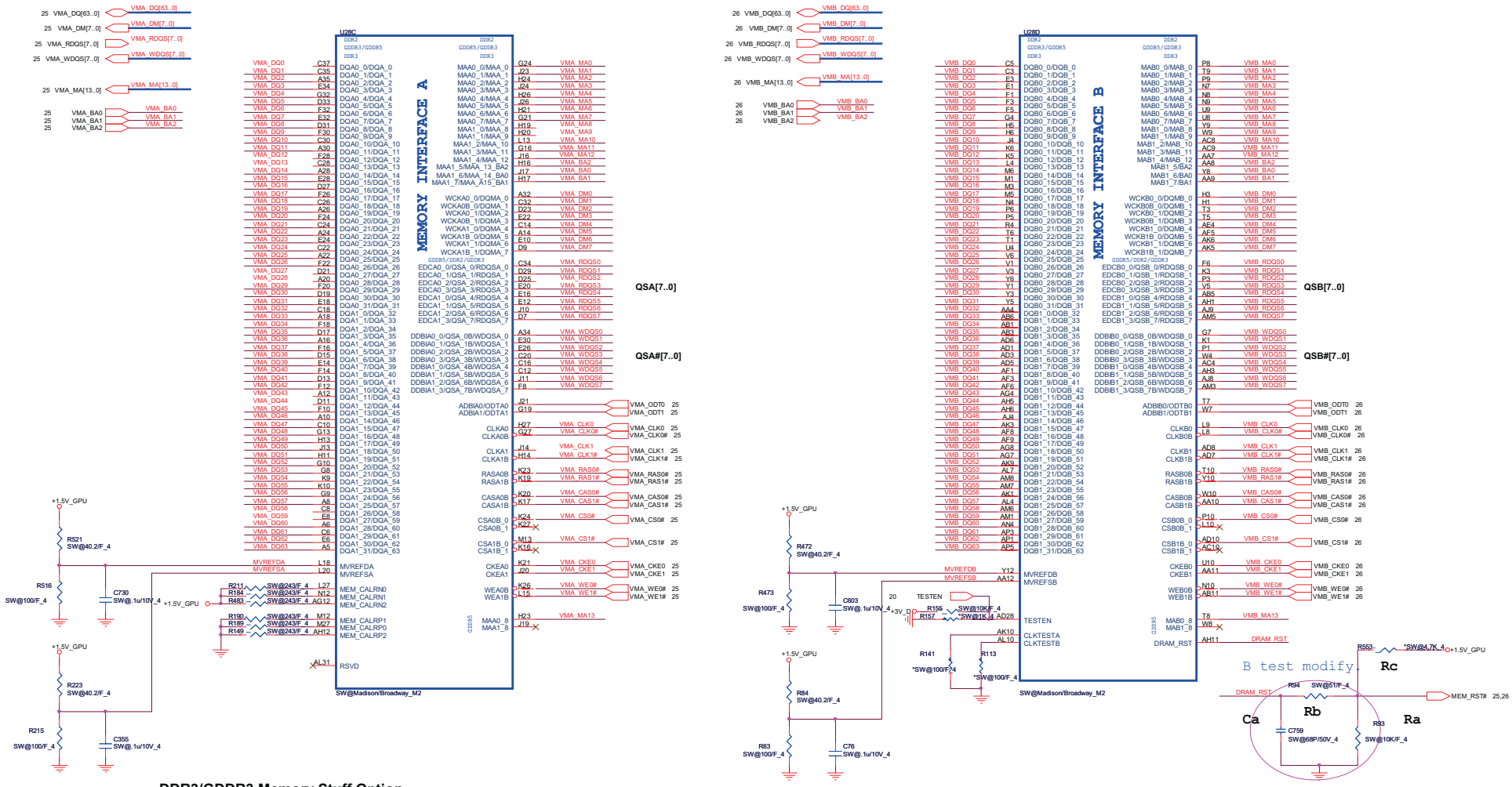
+1.8V(75mA)

+1.0V(125mA)

+1.8V(5mA)

PROJECT : ZYB & ZYBA
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | Madison/Broadway-HOST I/F | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 20 of 51 | |



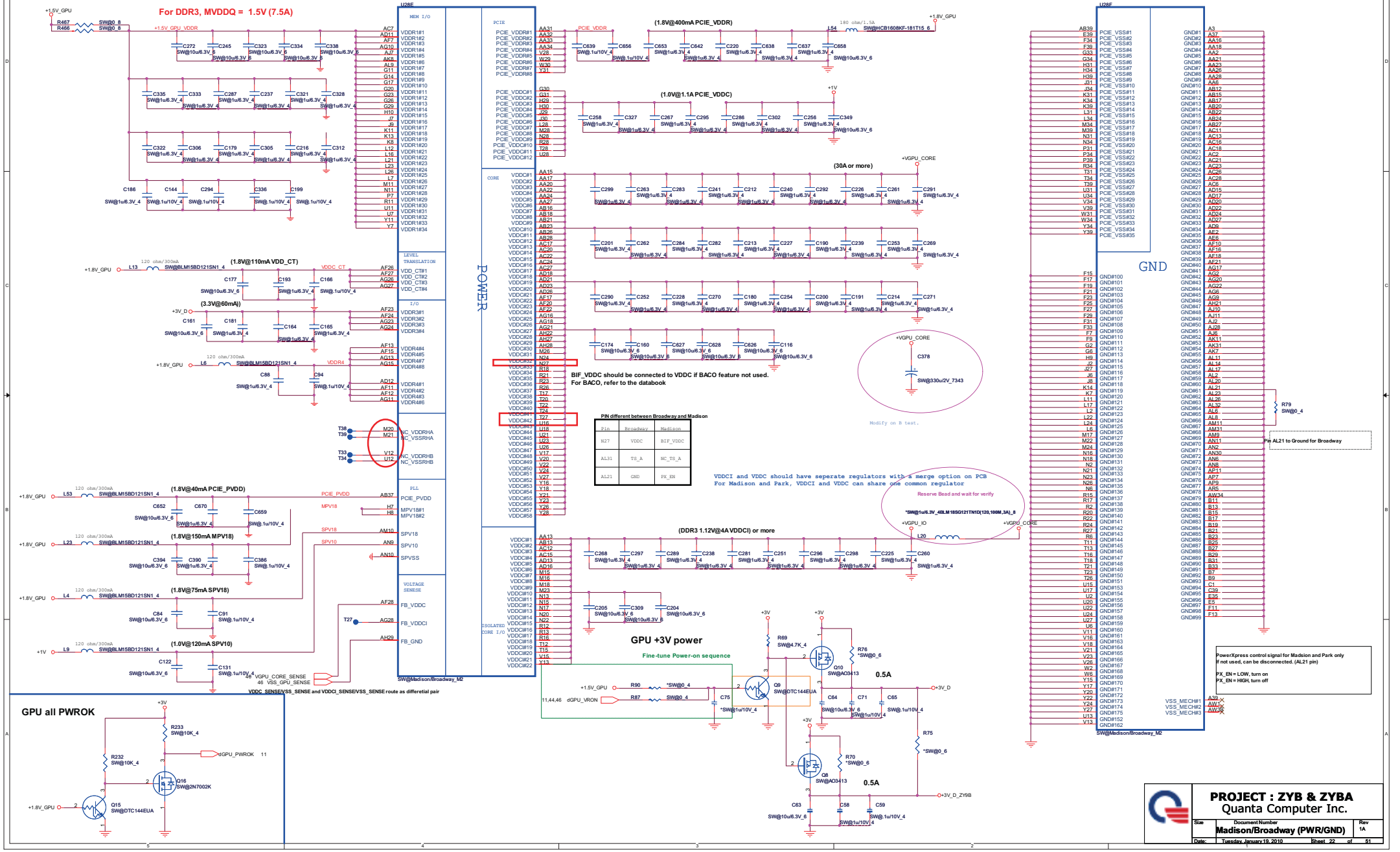

## DDR3/GDDR3 Memory Stuff Option

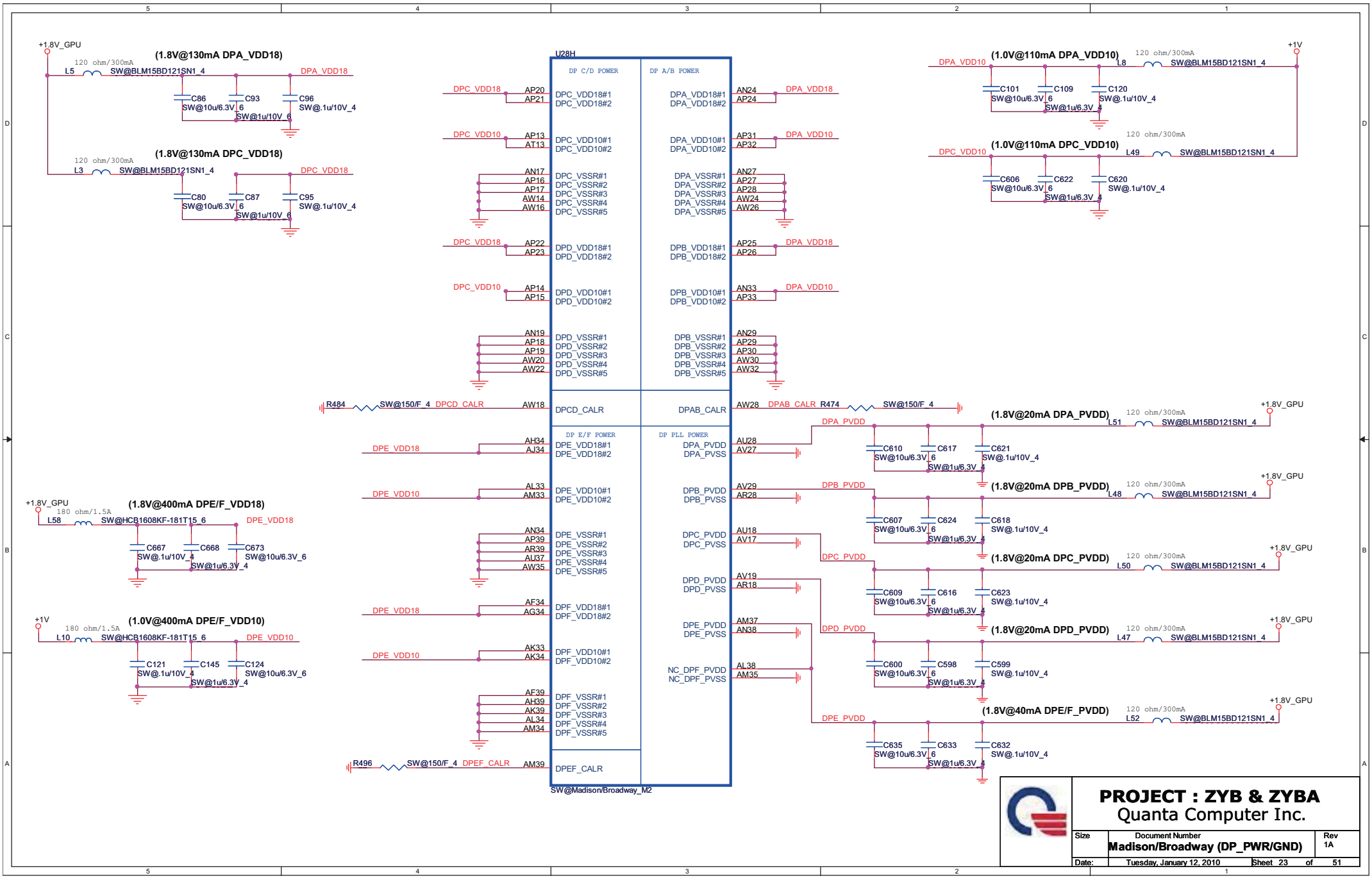
| | GDDR5 | GDDR3 | DDR3 |
|---|---|---|---|
| +1.5V_VGA | 1.5V | 1.8V/1.5V | 1.5V |
| Ra | 40.2R | 40.2R | 40.2R |
| Rb | 100R | 100R | 100R |

| Designator | For M97-M2 | For Mannhatton |
|---|---|---|
| Ra | 10K | 10K |
| Rb | 0R/Short | 51R |
| Rc | DNI | DNI |
| Ca | 2.2nF | 68pF |

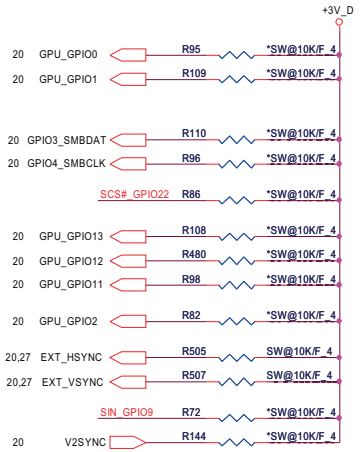
**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | Madison/Broadway-MEM I/F | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 21 of 51 | |


For DDR3, MVDDQ = 1.5V (7.5A)
U28F
MEM I/O
POWER
PCIE
CORE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENSE
ISOLATED CORE I/O
(1.8V@400mA PCIE_VDDR)
(1.0V@1.1A PCIE_VDDC)
(30A or more)
(1.8V@110mA VDD_CT)
(3.3V@60mA))
(1.8V@40mA PCIE_PVDD)
(1.8V@150mA MPV18)
(1.8V@75mA SPV18)
(1.0V@120mA SPV10)
(DDR3 1.12V@4A VDDCI) or more
BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
PIN different between Broadway and Madison
VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison and Park, VDDCI and VDDC can share one common regulator
GPU +3V power
Fine-tune Power-on sequence
GPU all PWROK
GND
PowerXpress control signal for Madison and Park only
If not used, can be disconnected. (AL21 pin)
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
Pin AL21 to Ground for Broadway
VDDC_SENSE/VSS_SENSE and VDDCI_SENSE/VSS_SENSE route as differetial pair
PROJECT : ZYB & ZYBA
Quanta Computer Inc.
Madison/Broadway (PWR/GND)
Tuesday, January 19, 2010
Sheet 22 of 51


+1.8V_GPU
(1.8V@130mA DPA_VDD18)
120 ohm/300mA
L5 SW@BLM15BD121SN1_4
DPA_VDD18
C86 SW@10u/6.3V_6
C93 SW@1u/10V_6
C96 SW@.1u/10V_4
(1.8V@130mA DPC_VDD18)
120 ohm/300mA
L3 SW@BLM15BD121SN1_4
DPC_VDD18
C80 SW@10u/6.3V_6
C87 SW@1u/10V_6
C95 SW@.1u/10V_4
U28H
DP C/D POWER
DP A/B POWER
DPC_VDD18
AP20 AP21
DPC_VDD18#1 DPC_VDD18#2
DPA_VDD18#1 DPA_VDD18#2
AN24 AP24
DPA_VDD18
DPC_VDD10
AP13 AT13
DPC_VDD10#1 DPC_VDD10#2
DPA_VDD10#1 DPA_VDD10#2
AP31 AP32
DPA_VDD10
AN17 AP16 AP17 AW14 AW16
DPC_VSSR#1 DPC_VSSR#2 DPC_VSSR#3 DPC_VSSR#4 DPC_VSSR#5
DPA_VSSR#1 DPA_VSSR#2 DPA_VSSR#3 DPA_VSSR#4 DPA_VSSR#5
AN27 AP27 AP28 AW24 AW26
DPC_VDD18
AP22 AP23
DPD_VDD18#1 DPD_VDD18#2
DPB_VDD18#1 DPB_VDD18#2
AP25 AP26
DPA_VDD18
DPC_VDD10
AP14 AP15
DPD_VDD10#1 DPD_VDD10#2
DPB_VDD10#1 DPB_VDD10#2
AN33 AP33
DPA_VDD10
AN19 AP18 AP19 AW20 AW22
DPD_VSSR#1 DPD_VSSR#2 DPD_VSSR#3 DPD_VSSR#4 DPD_VSSR#5
DPB_VSSR#1 DPB_VSSR#2 DPB_VSSR#3 DPB_VSSR#4 DPB_VSSR#5
AN29 AP29 AP30 AW30 AW32
R484 SW@150/F_4 DPCD_CALR
AW18
DPCD_CALR
DPAB_CALR
AW28 DPAB_CALR R474 SW@150/F_4
DP E/F POWER
DP PLL POWER
DPE_VDD18
AH34 AJ34
DPE_VDD18#1 DPE_VDD18#2
DPA_PVDD DPA_PVSS
AU28 AV27
DPE_VDD10
AL33 AM33
DPE_VDD10#1 DPE_VDD10#2
DPB_PVDD DPB_PVSS
AV29 AR28
AN34 AP39 AR39 AU37 AW35
DPE_VSSR#1 DPE_VSSR#2 DPE_VSSR#3 DPE_VSSR#4 DPE_VSSR#5
DPC_PVDD DPC_PVSS
AU18 AV17
DPD_PVDD DPD_PVSS
AV19 AR18
DPE_VDD18
AF34 AG34
DPF_VDD18#1 DPF_VDD18#2
DPE_PVDD DPE_PVSS
AM37 AN38
DPE_VDD10
AK33 AK34
DPF_VDD10#1 DPF_VDD10#2
NC_DPF_PVDD NC_DPF_PVSS
AL38 AM35
AF39 AH39 AK39 AL34 AM34
DPF_VSSR#1 DPF_VSSR#2 DPF_VSSR#3 DPF_VSSR#4 DPF_VSSR#5
R496 SW@150/F_4 DPEF_CALR
AM39
DPEF_CALR
SW@Madison/Broadway_M2
+1V
(1.0V@110mA DPA_VDD10)
120 ohm/300mA
DPA_VDD10
L8 SW@BLM15BD121SN1_4
C101 SW@10u/6.3V_6
C109 SW@1u/6.3V_4
C120 SW@.1u/10V_4
(1.0V@110mA DPC_VDD10)
120 ohm/300mA
DPC_VDD10
L49 SW@BLM15BD121SN1_4
C606 SW@10u/6.3V_6
C622 SW@1u/6.3V_4
C620 SW@.1u/10V_4
+1.8V_GPU
(1.8V@20mA DPA_PVDD)
120 ohm/300mA
DPA_PVDD
L51 SW@BLM15BD121SN1_4
C610 SW@10u/6.3V_6
C617 SW@1u/6.3V_4
C621 SW@.1u/10V_4
(1.8V@20mA DPB_PVDD)
120 ohm/300mA
DPB_PVDD
L48 SW@BLM15BD121SN1_4
C607 SW@10u/6.3V_6
C624 SW@1u/6.3V_4
C618 SW@.1u/10V_4
(1.8V@20mA DPC_PVDD)
120 ohm/300mA
DPC_PVDD
L50 SW@BLM15BD121SN1_4
C609 SW@10u/6.3V_6
C616 SW@1u/6.3V_4
C623 SW@.1u/10V_4
(1.8V@20mA DPD_PVDD)
120 ohm/300mA
DPD_PVDD
L47 SW@BLM15BD121SN1_4
C600 SW@10u/6.3V_6
C598 SW@1u/6.3V_4
C599 SW@.1u/10V_4
(1.8V@40mA DPE/F_PVDD)
120 ohm/300mA
DPE_PVDD
L52 SW@BLM15BD121SN1_4
C635 SW@10u/6.3V_6
C633 SW@1u/6.3V_4
C632 SW@.1u/10V_4
(1.8V@400mA DPE/F_VDD18)
180 ohm/1.5A
L58 SW@HCB1608KF-181T15_6
DPE_VDD18
C667 SW@.1u/10V_4
C668 SW@1u/6.3V_4
C673 SW@10u/6.3V_6
(1.0V@400mA DPE/F_VDD10)
180 ohm/1.5A
L10 SW@HCB1608KF-181T15_6
DPE_VDD10
C121 SW@.1u/10V_4
C145 SW@1u/6.3V_4
C124 SW@10u/6.3V_6
PROJECT : ZYB & ZYBA
Quanta Computer Inc.
Size
Document Number
Madison/Broadway (DP_PWR/GND)
Rev
1A
Date:
Tuesday, January 12, 2010
Sheet 23 of 51

## PIN STRAPS




| Memory Aperture size | |
|---|---|
| GPIO[13:11] | Size |
| 000 | 128MB |
| 001 | 256MB |
| 010 | 64MB |
| 011 | 32MB |

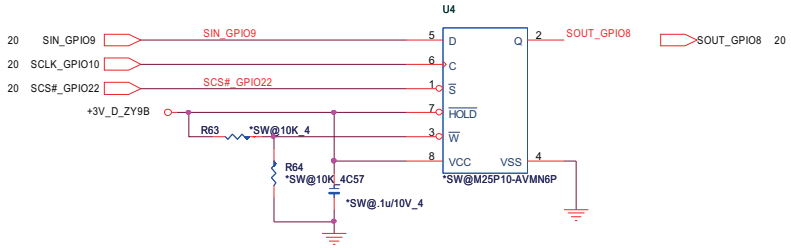
| Audio Table | | |
|---|---|---|
| EXT_HSYNC | EXT_VSYNC | Discription |
| 0 | 0 | No Audio |
| 0 | 1 | Any one by dectec |
| 1 | 0 | DP only |
| 1 | 1 | Both DP & HDMI |

## CONFIGURATION STRAPS

**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET**

| STRAPS | PIN | DESCRIPTION OF DEFAULT SETTINGS | DEFAULT | REMARK |
|---|---|---|---|---|
| TX_PWRS_ENB | GPIO0 | 0 = 50% TX OUTPUT SWING<br>1 = FULL TX OUTPUT SWING | 0 | |
| TX_DEEMPH_EN | GPIO1 | PCIE TRANSMITTER DE-EMPHASIS ENABLED<br>0 = TX DE-EMPHASIS DISABLED<br>1 = TX DE-EMPHASIS ENABLED | 0 | |
| BIOS_ROM_EN | GPIO_22_ROMCSB | ENABLE EXTERNAL BIOS ROM<br>0 = DISABLE<br>1 = ENABLE | 0 | |
| ROMIDCFG(2:0) | GPIO[13:11] | SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT | 000 | See Memory Aperture size |
| BIF_GEN2_EN_A | GPIO2 | 0 = PCIE DEVICE AS 2.5GT/S CAPABLE<br>1 = PCIE DEVICE AS 5GT/S CAPABLE | 0 | |
| GPIO_8_ROMSO<br>H2SYNC<br>GPIO_21_BB_EN | GPIO8<br>H2SYNC<br>GPIO21 | Reserved Only | 0 | |
| AUD[1]<br>AUD[0] | HSYNC<br>VSYNC | AUD[1:0]<br>00: NO AUDIO FUNCTION.<br>01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED.<br>10: AUDIO FOR DISPLAYPORT ONLY.<br>11: AUDIO FOR BOTH DISPLAYPORT AND HDMI. | 11 | See Audio table |
| GPIO_9_ROMSI | GPIO9 | 0 = VGA controller capacity enable | 0 | |
| VIP_DEVICE_STRAP_ENA | V2SYNC | 0 = DRIVER would ignore the value sample on VHAD_0 during RESET. | 0 | |

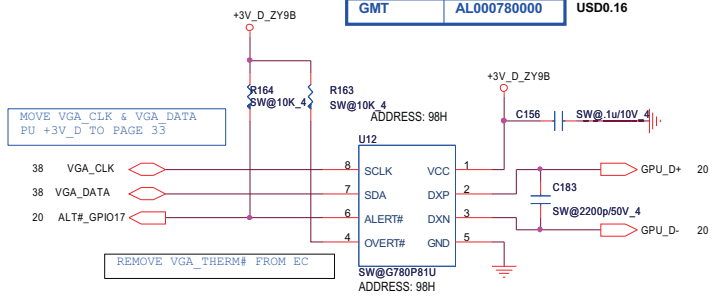
## EEPROM




## Thermal Sensor

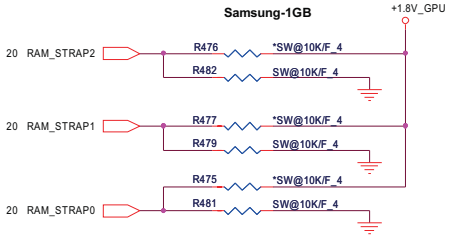
| Vendor | P/N |
|---|---|
| WINDBOND | AL83L771K01 |
| GMT | AL000780000 |

USD0.16




## DDR3 VRAM SIZE Strap

| DDR3 VRAM size | | | | | | |
|---|---|---|---|---|---|---|
| Vendor | Vendor P/N | STN B/S P/N | Size | RAM_STRAP2 DVPDATA_2 | RAM_STRAP1 DVPDATA_1 | RAM_STRAP0 DVPDATA_0 |
| Hynix | | | 512MB | 1 | 1 | 0 |
| | H5TQ1G63BFR-12C | AKD5LZGTW04 (64M*16) | 1GB | 1 | 0 | 0 |
| | | | 2GB | 1 | 0 | 1 |
| Samsung | | | 512MB | 0 | 1 | 0 |
| | K4W1G1646E-HC12 | AKD5LGGT506 (64M*16) | 1GB | 0 | 0 | 0 |
| | K4W2G1646B-HC12 | AKD5MGGT500 | 2GB | 0 | 0 | 1 |
| AMD | 23EY2387MA-12 | AKD5LGGT700 | | 0 | 1 | 0 |




RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | Strip/Thermal | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 24 of 51 | |

# CHANNEL A: 512MB DDR3 (64M*16*4pcs)

Park, M92M Use Channel B Memory Interface Only

SAMSUNG - AKD5LGGT506
HYNIX - AKD5LZGTW04

TOP Left

BOT Left

BOT Right

TOP Right

## Group-A0 VREF

## Group-A1 VREF

## MEM_A0 CLK

## Group-A0 decoupling CAP

## Group-A1 decoupling CAP

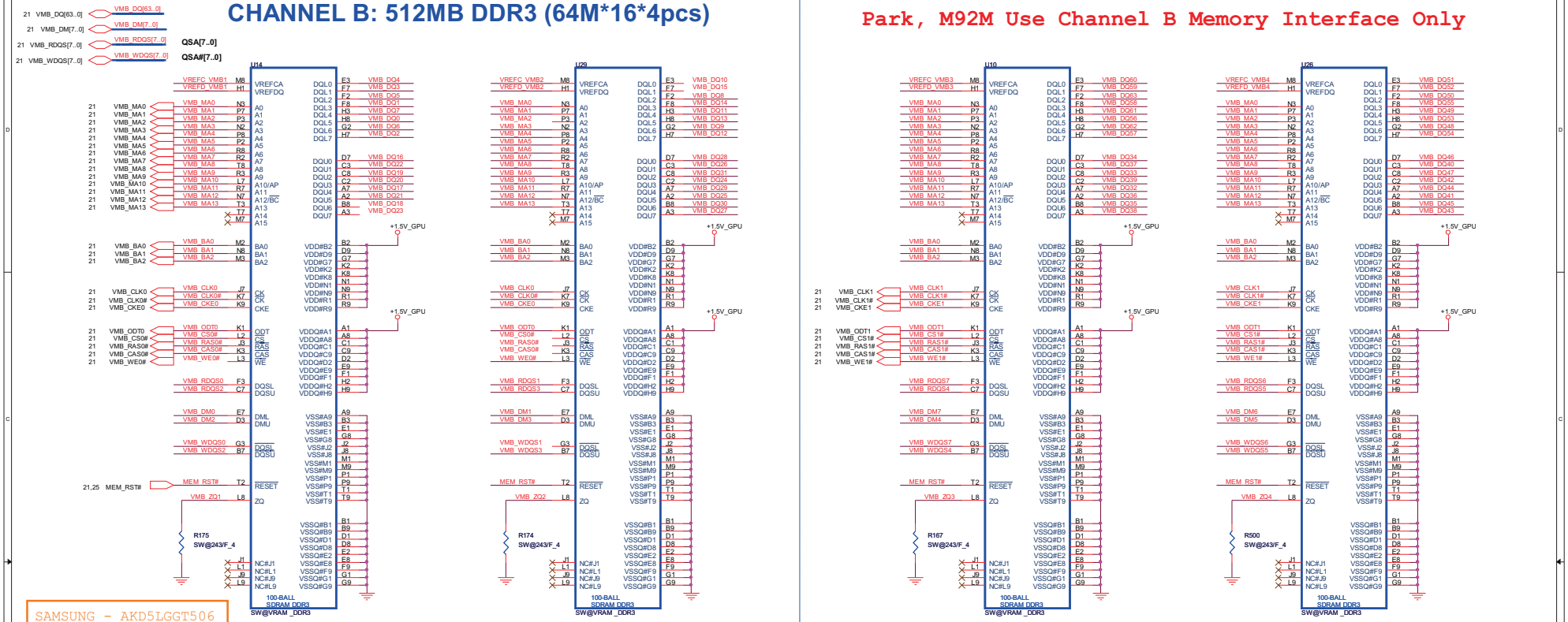
## MEM_A1 CLK

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

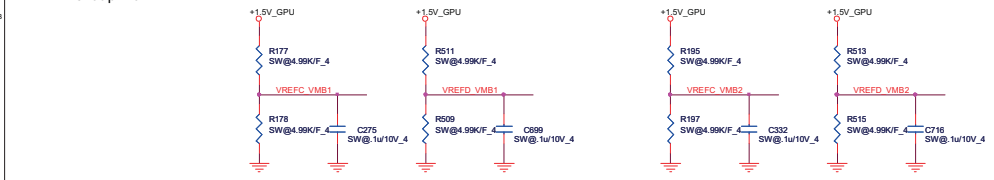
| Size | Document Number | Rev |
|---|---|---|
| | MEMORY 1 channel A | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 25 of 51 | |

# CHANNEL B: 512MB DDR3 (64M*16*4pcs)

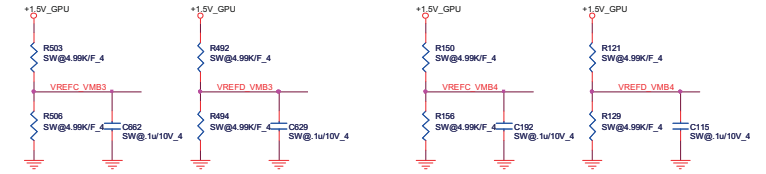
## Park, M92M Use Channel B Memory Interface Only



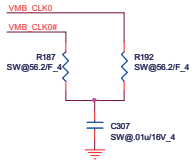

## Group-B0 VREF



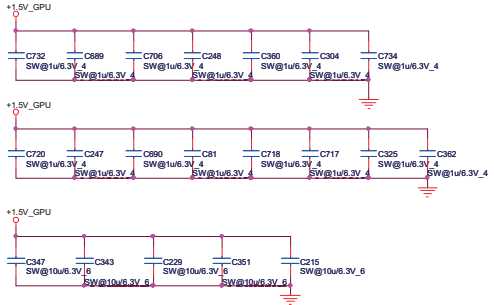

## Group-B1 VREF



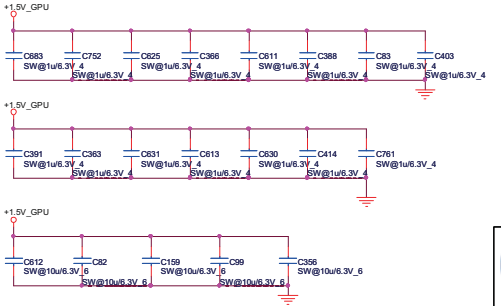

## MEM_B0 CLK



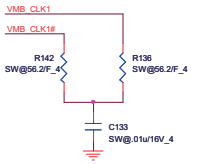

## Group-B0 decoupling CAP




## Group-B1 decoupling CAP

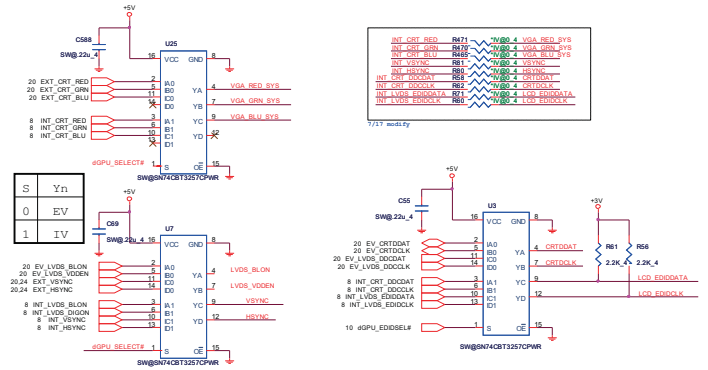



## MEM_B1 CLK

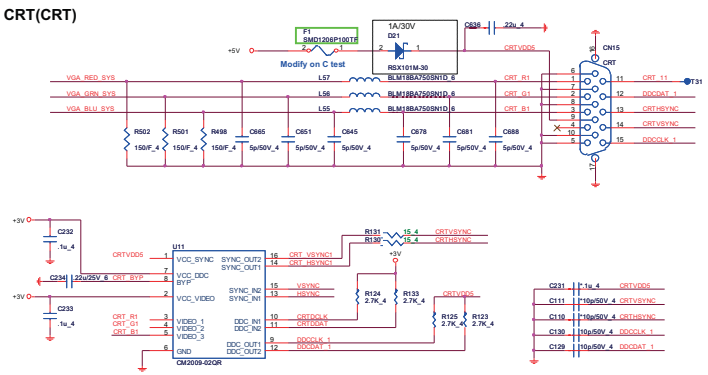



| | | |
|---|---|---|
| PROJECT : ZYB & ZYBA | | |
| Quanta Computer Inc. | | |
| Size | Document Number: MEMORY 2 channel B | Rev: 1A |
| Date: Tuesday, January 19, 2010 | Sheet 26 of 51 | |

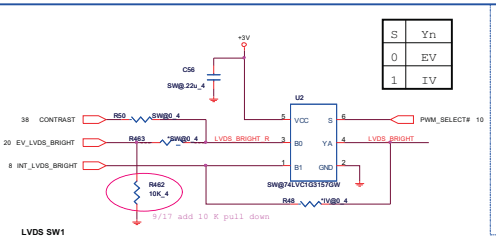
## CRT SWITCH(CRT)



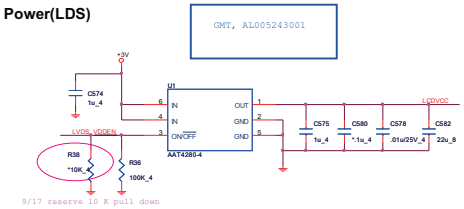

## CRT(CRT)



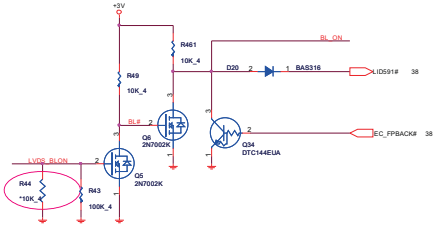

## LVDS(LDS)



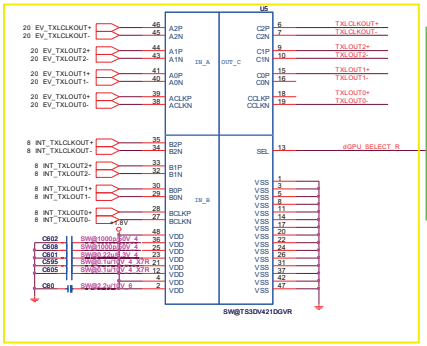

## LCD Power(LDS)

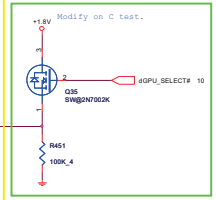


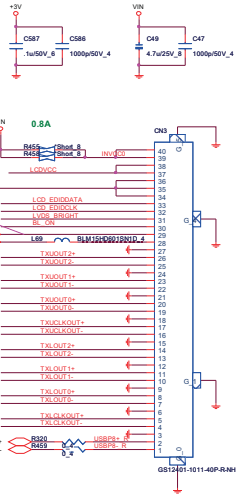

## Backlight Control(LDS)



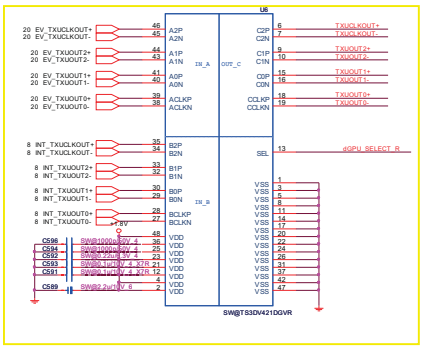

## LVDS SW1



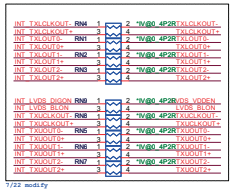



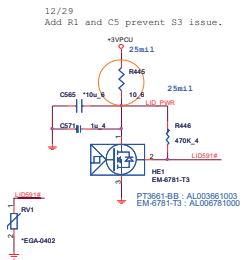

## LVDS SW2




| dGPU_SELECT# | Output |
|---|---|
| L | EV_LVDS |
| H | INT_LVDS |




## Lid Switch (HSR)

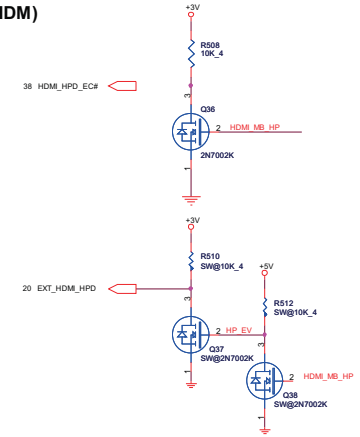



**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | CRT/LVDS/LID | 1A |

Date: Tuesday, January 19, 2010 Sheet 27 of 51

## HDMI HPD(HDM)



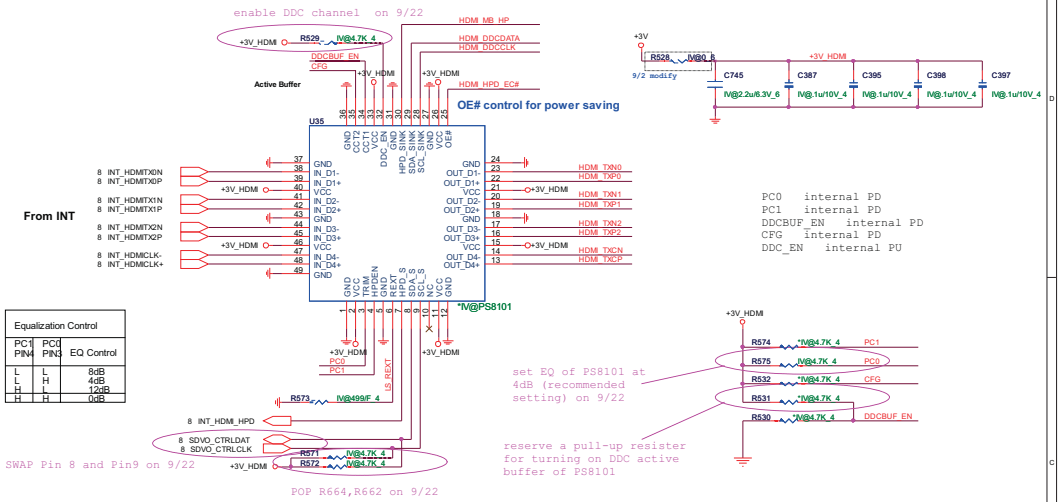

## (HDM)

## HDMI LEVEL SHIFTER(HDM)

PS8101 :: AL008101000

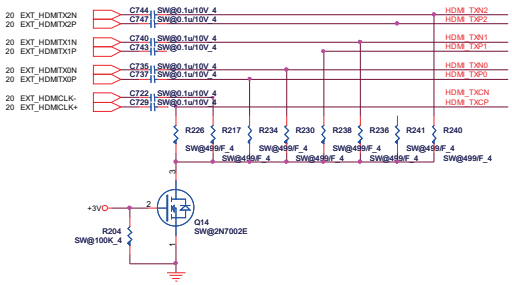
UMA => PS8101 Exist
SG and Dis only => PS8101 del

28




| Equalization Control | | |
|---|---|---|
| PC1 PIN4 | PC0 PIN3 | EQ Control |
| L | L | 8dB |
| L | H | 4dB |
| H | L | 12dB |
| H | H | 0dB |

## From EXT VGA

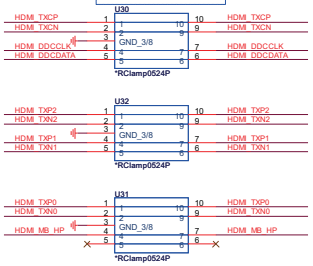



## EMI reserve for HDMI(HDM)

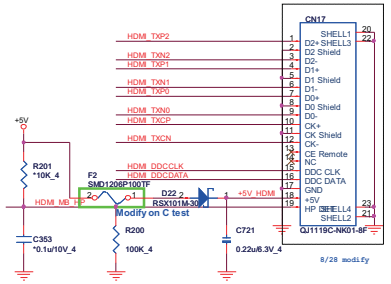

Close connector

### ESD Protect

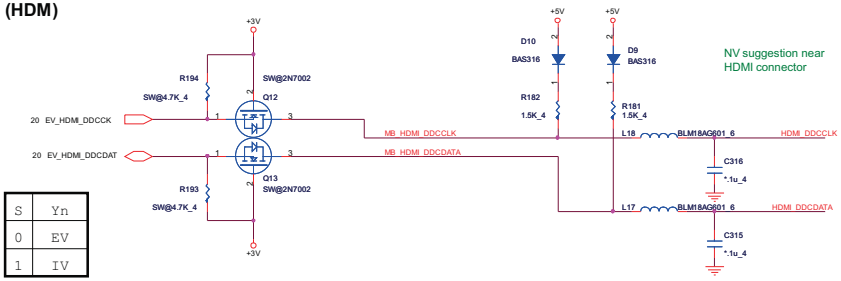
close to HDMI connector




## HDMI connector(HDM)




## (HDM)

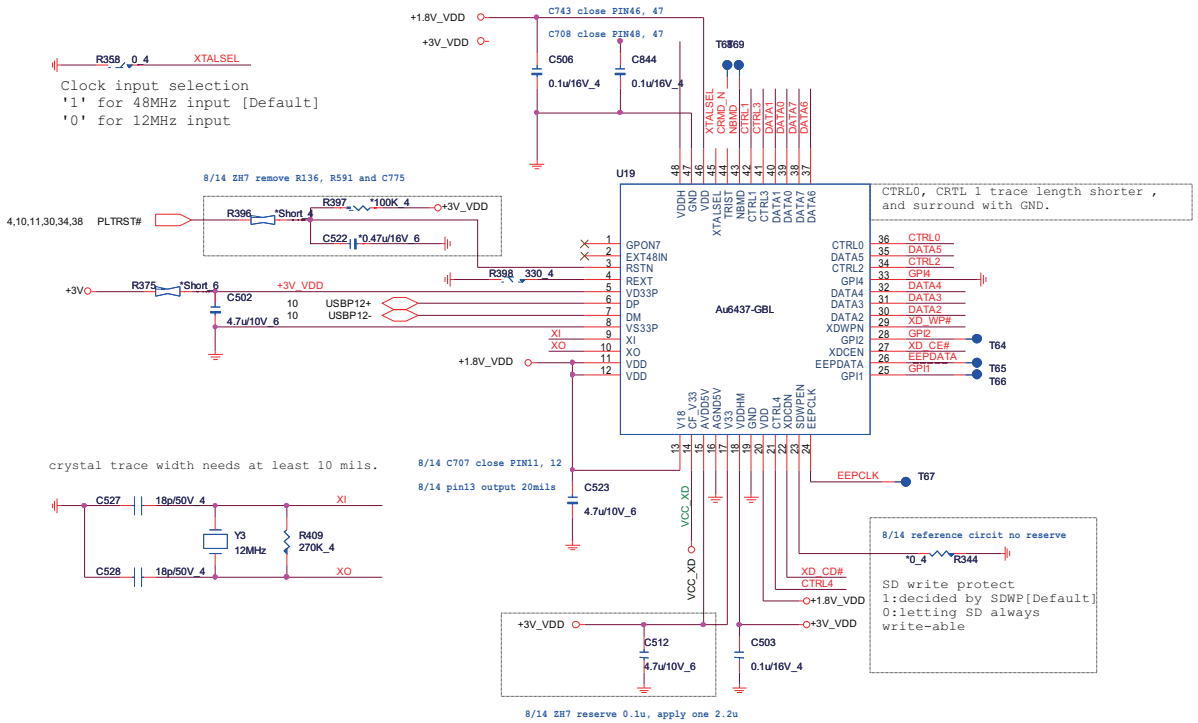



| S | Yn |
|---|---|
| 0 | EV |
| 1 | IV |

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

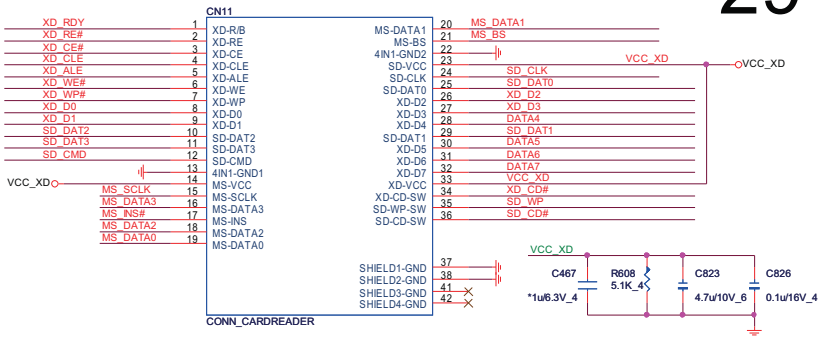
| Size | Document Number | Rev |
|---|---|---|
| | HDMI/DP | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 28 of 51 | |

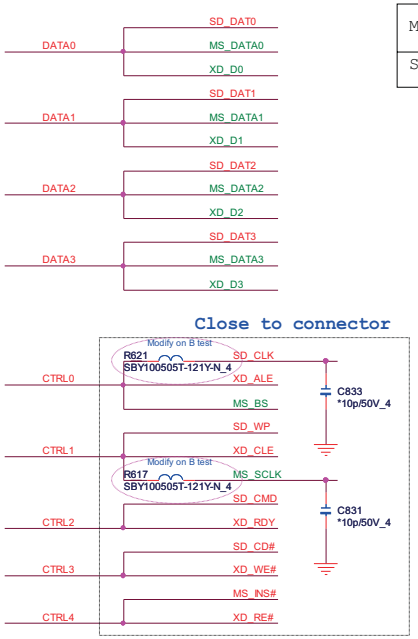
## AU6433 CardReader(MMC)




## 4 IN 1 CARD READER (MMC)

29

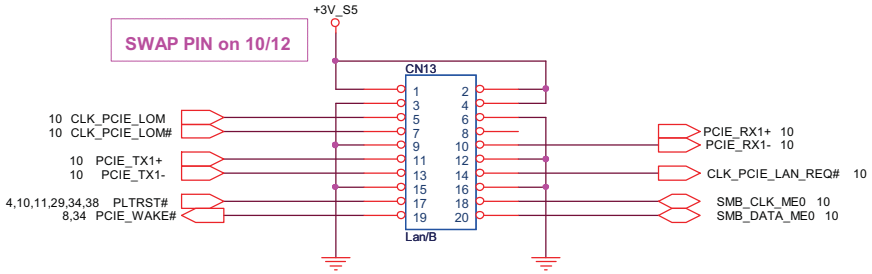


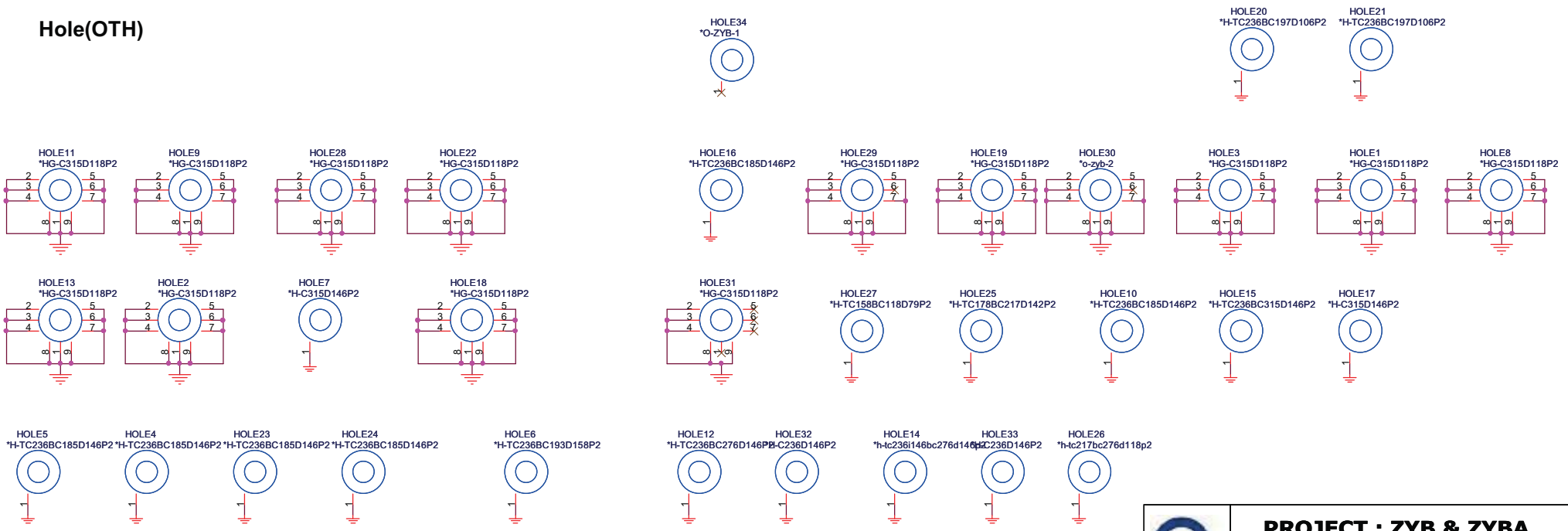

| | |
|---|---|
| Main | DFHD36MS017 |
| Second | DFHD38MS013 |

| | |
|---|---|
| PROJECT : | ZYB & ZYBA |
| Quanta Computer Inc. | |
| Size | Document Number: AU6433 CardReader |
| Rev | 1A |
| Date: | Tuesday, January 19, 2010 |
| Sheet | 29 of 51 |

## Lan/B(LAN)



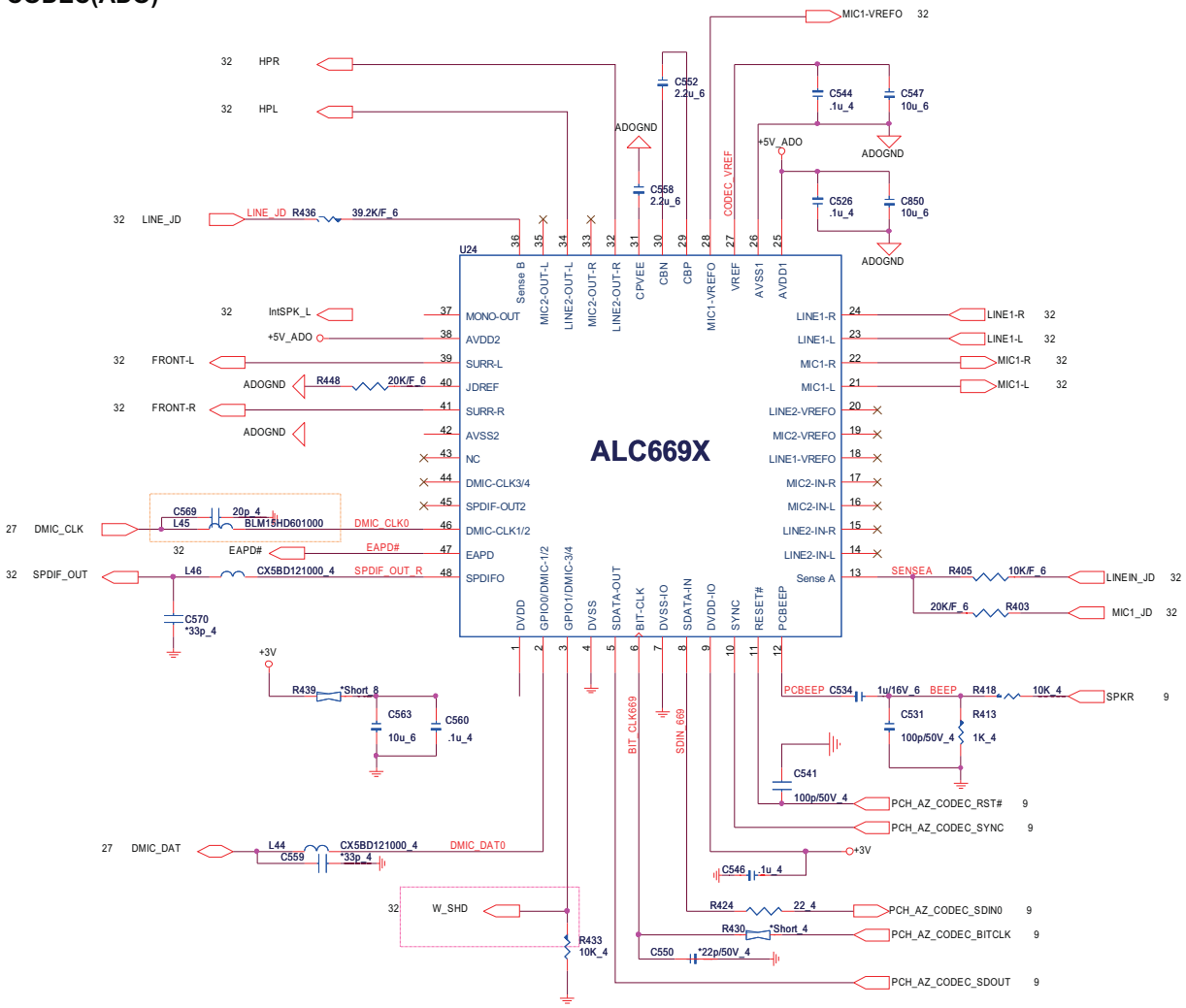

## Hole(OTH)



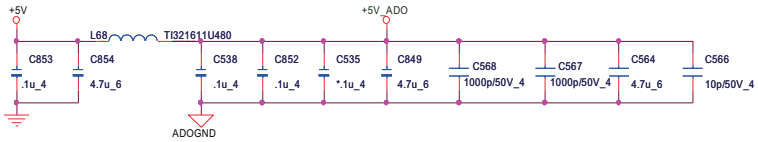

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | **Lan/B & Hole** | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 30 of 51 | |

## CODEC(ADO)

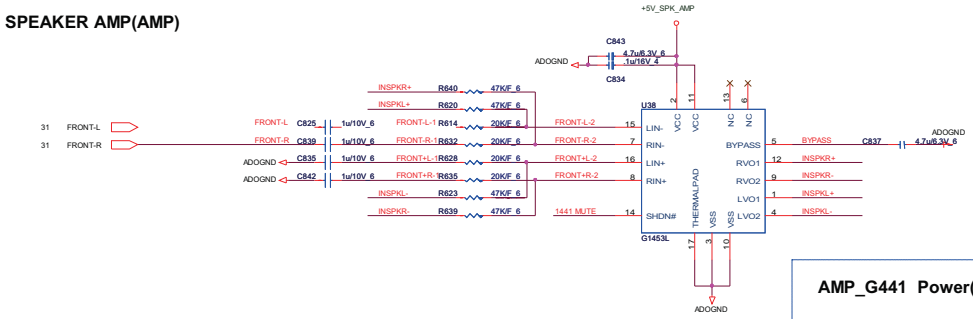



## CODEC/AMP Power(ADO)

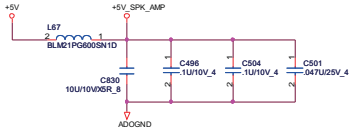



| | | |
|---|---|---|
| **PROJECT : ZYB & ZYBA** | | |
| Quanta Computer Inc. | | |
| Size | Document Number | Rev |
| | REALTEK ALC669X | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 31 of 51 | |

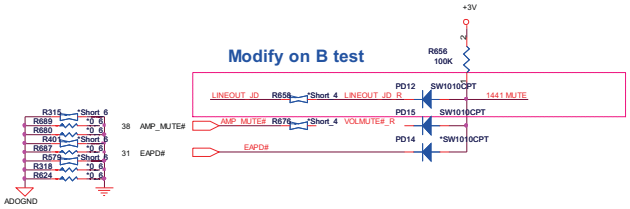
## SPEAKER AMP(AMP)



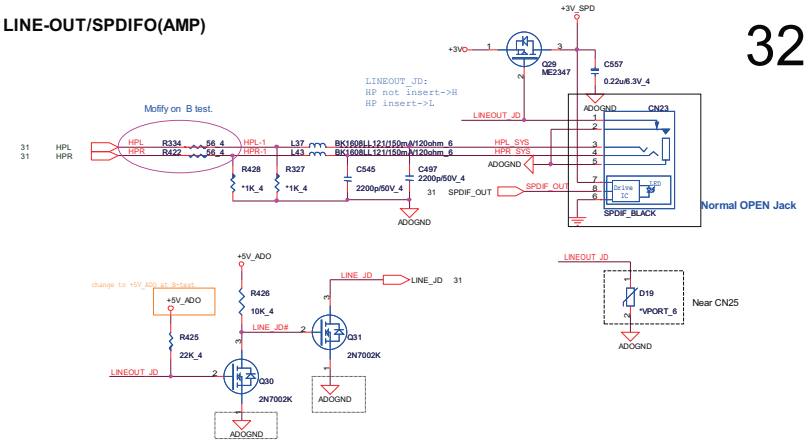

## AMP_G441 Power(ADO)



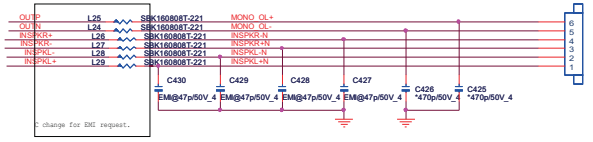

## Modify on B test




## LINE-OUT/SPDIFO(AMP)




## Main SPK and SUBWOOFER(AMP)

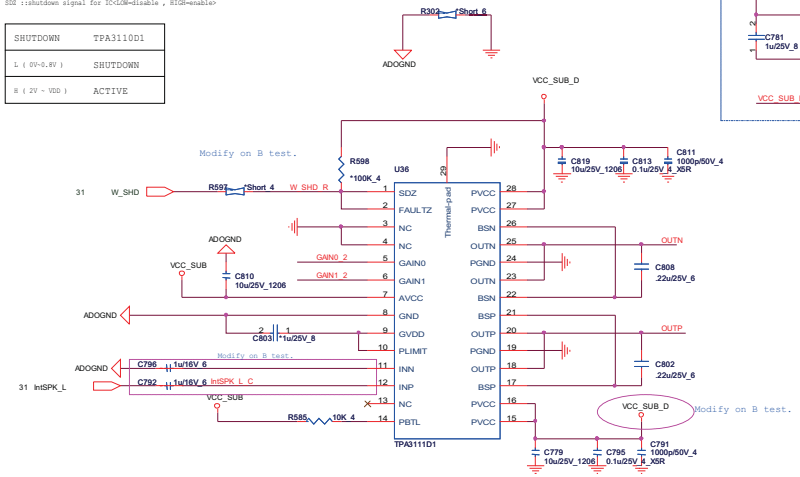



## SUBWOOFER(AMP)

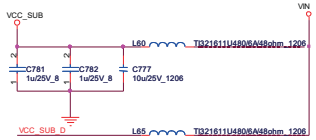
LPF for fc(-3dB)=500Hz

SDZ ::shutdown signal for IC<LOW-disable , HIGH-enable>

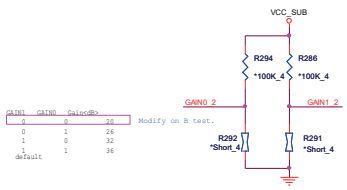
| | |
|---|---|
| SHUTDOWN | TPA3110D1 |
| L ( 0V~0.8V ) | SHUTDOWN |
| H ( 2V ~ VDD ) | ACTIVE |



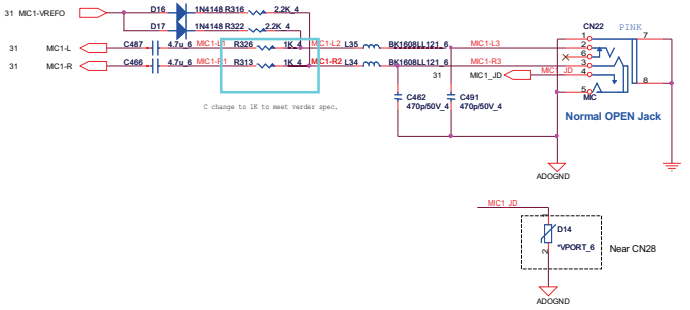

## SUBWOOFER Power(AMP)



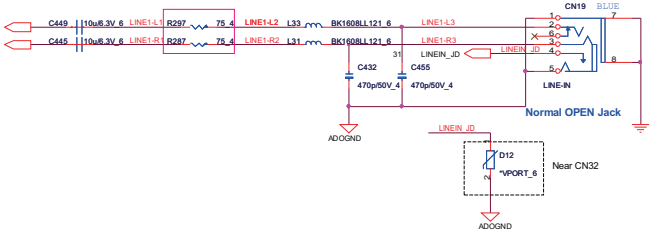

## AMO GAIN(AMP)




## MIC(AMP)



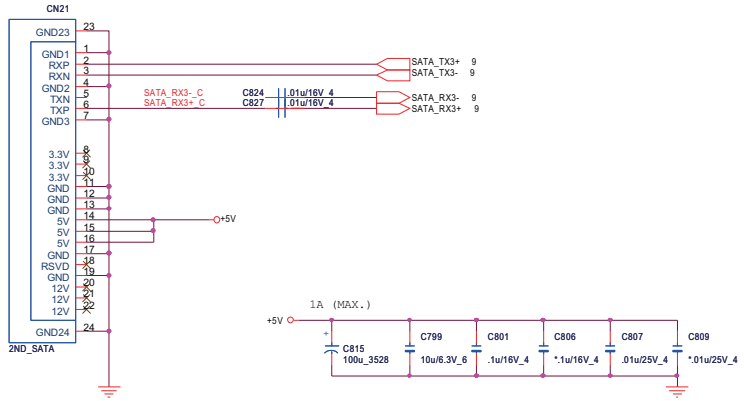

## LINE IN(AMP)



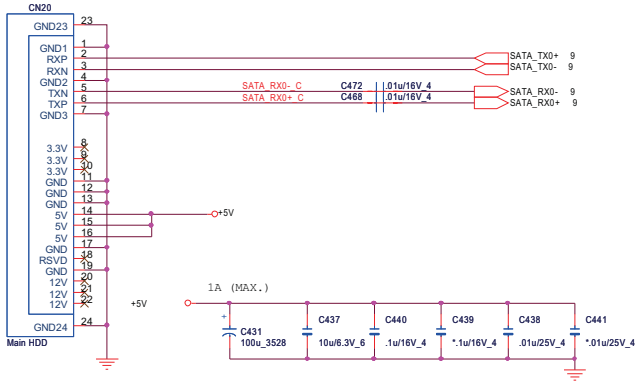

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | AMP/AUDIO JACK/WOOFER | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 32 of 51 | |

## 2nd SATA HDD (HDD)

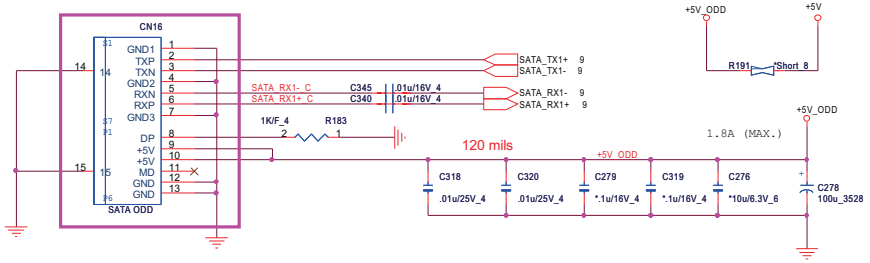



## MAIN SATA HDD(HDD)




## ODD SATA(ODD)

**This ODD must be use eSATA Port**



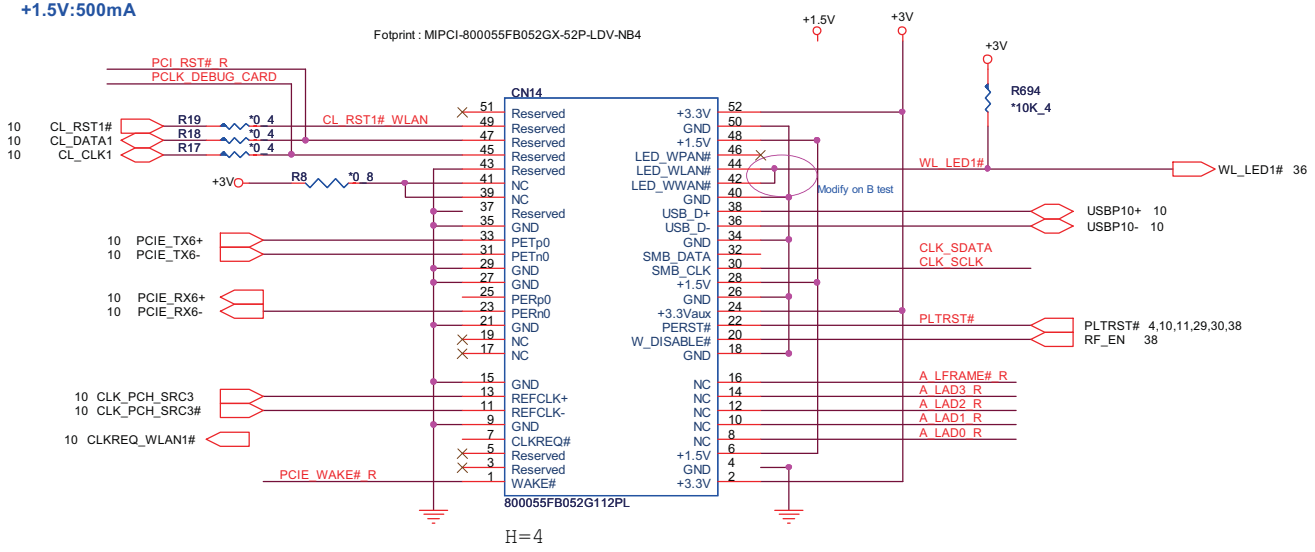

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

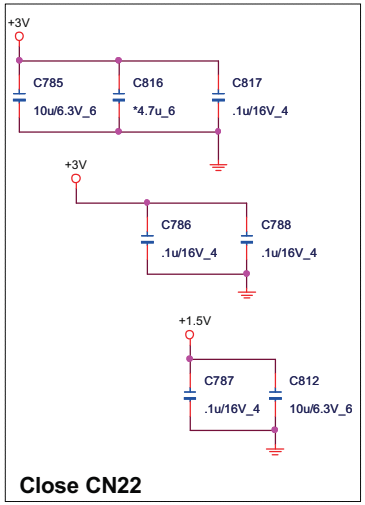
| Size | Document Number | Rev |
|---|---|---|
| | SATA-HDD/ODD | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 33 of 51 | |

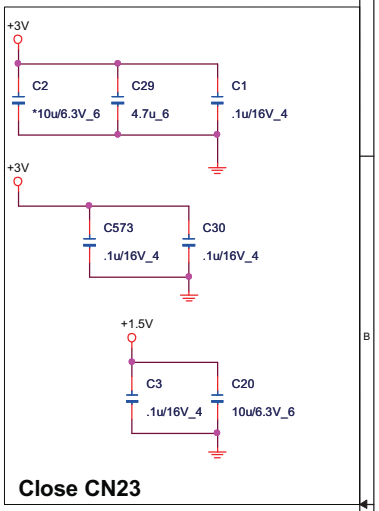
# Wireless 1(MPC)



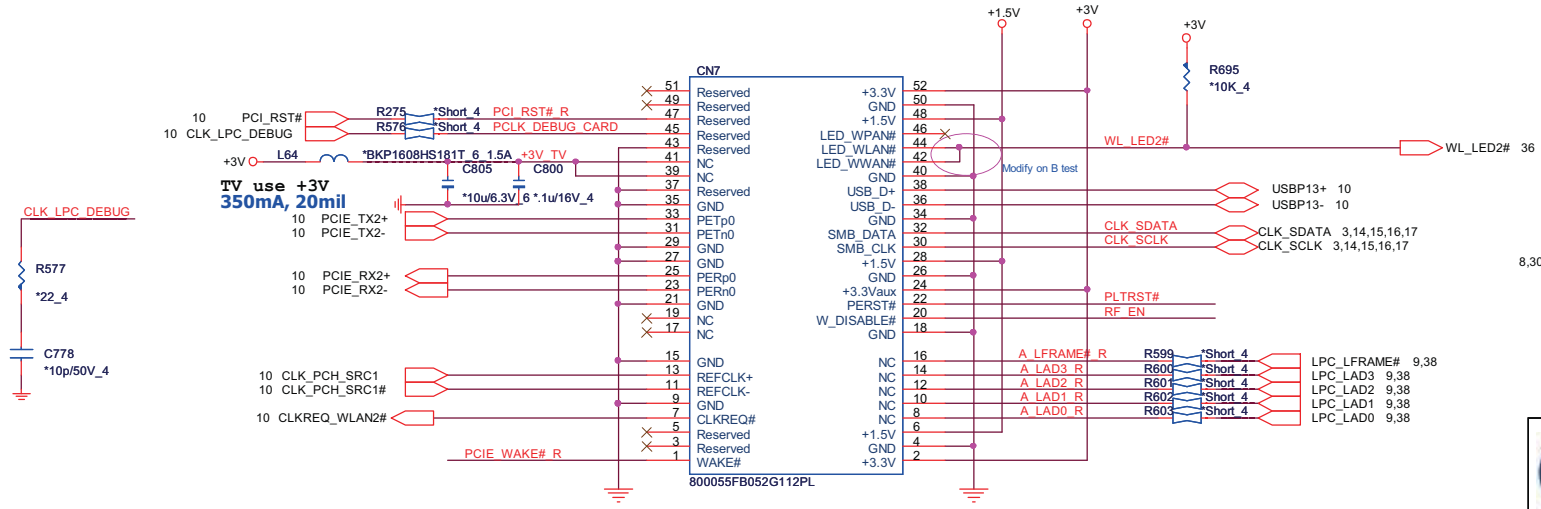
**+3.3V: 1000mA**
**+3.3Vaux:330mA**
**+1.5V:500mA**

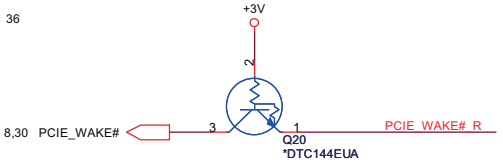



# Wireless 2 (MPC)



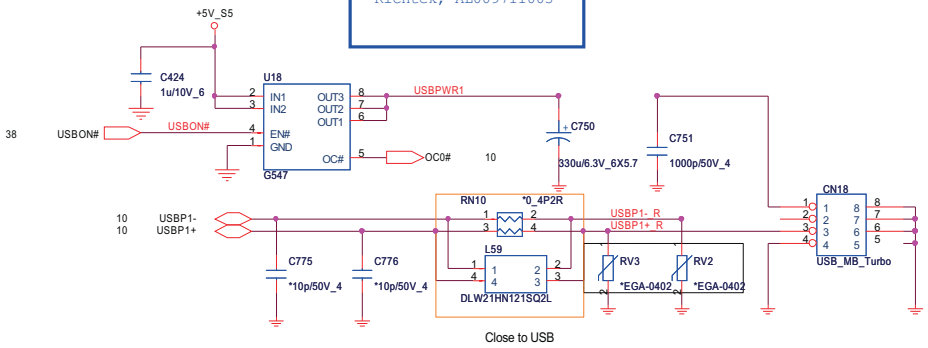




**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

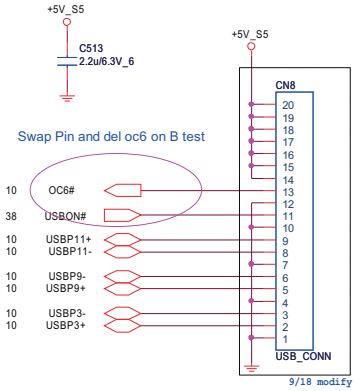
| Size | Document Number | Rev |
|---|---|---|
| | MINI PCI-E card | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 34 of 51 | |

## USB(USB)

GMT, AL000547000
Richtek, AL009711003

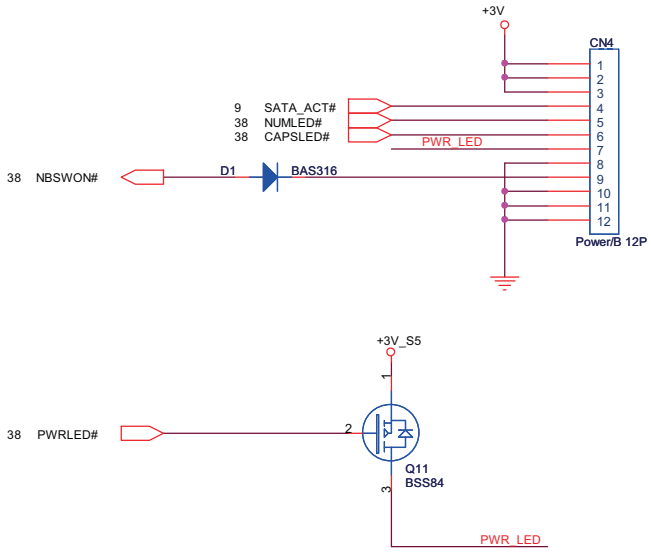



## USB/B

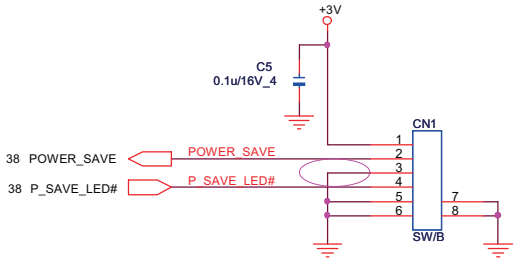



| | | |
|---|---|---|
| PROJECT : ZYB & ZYBA<br>Quanta Computer Inc. | | |
| Size | Document Number<br>INT USB/ EXT USB | Rev<br>1A |
| Date: Tuesday, January 19, 2010 | Sheet 35 of 51 | |

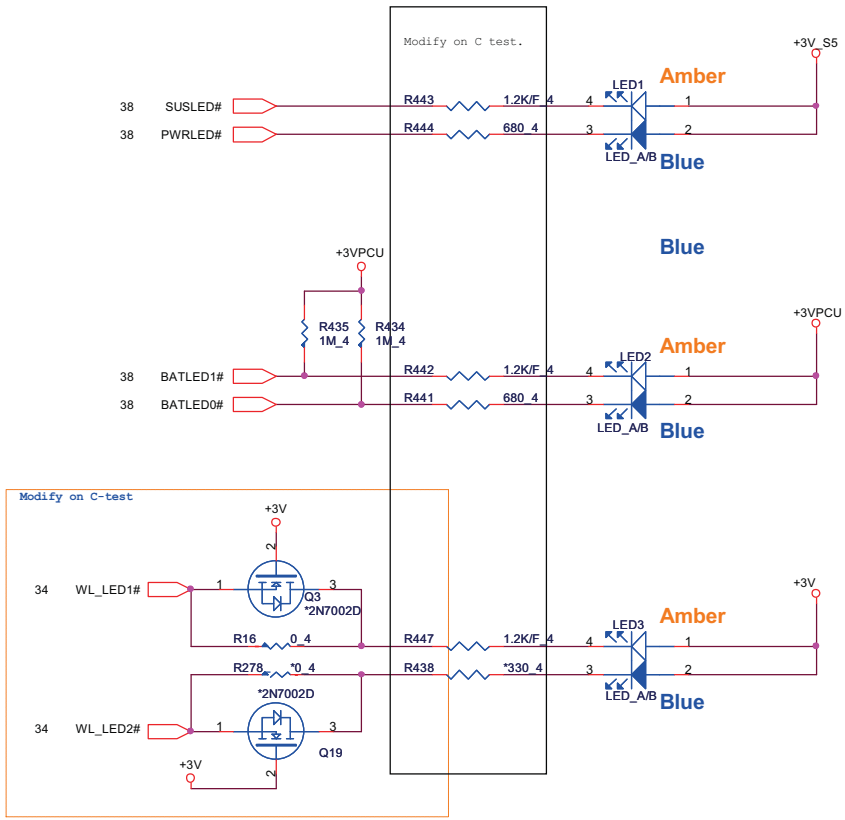
## POWER BOARD(UIF)




## SW/B(UIF)

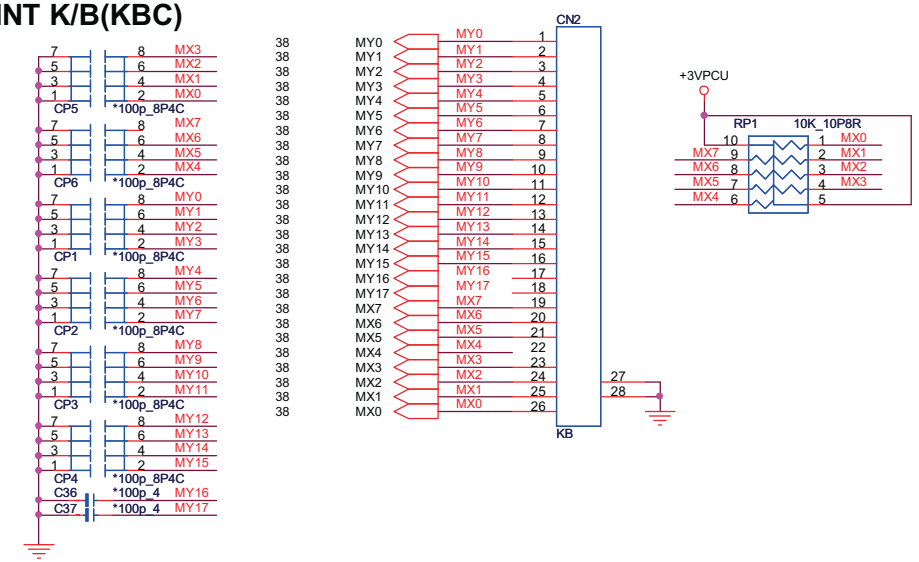



## M/B(Battery) LED(uif)

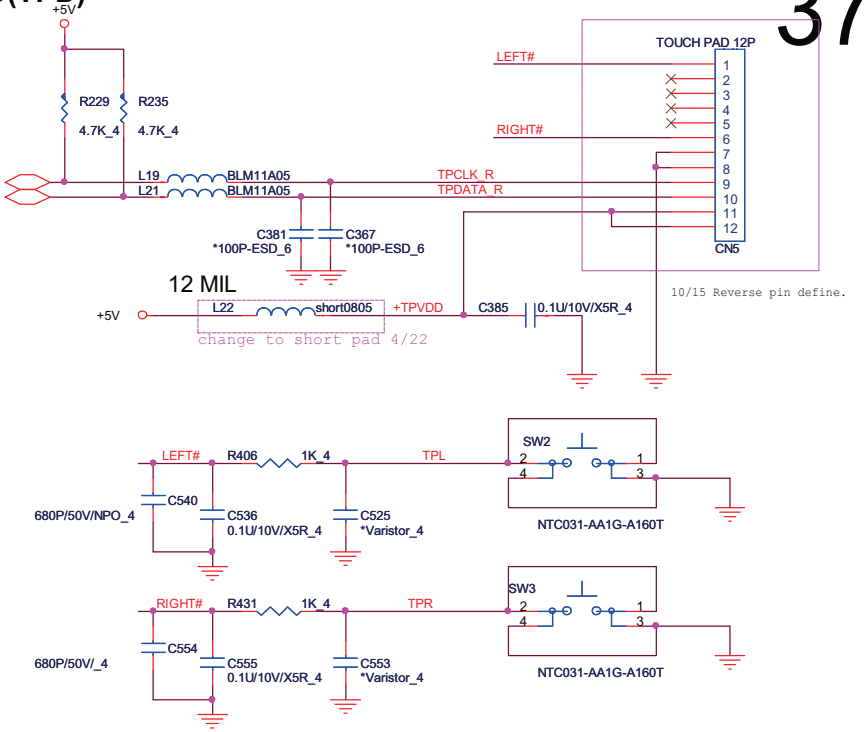



| | | |
|---|---|---|
| PROJECT : ZYB & ZYBA<br>Quanta Computer Inc. | | |
| Size | Document Number<br>POWER/LAUNCH/LED | Rev<br>1A |
| Date: Tuesday, January 19, 2010 | Sheet 36 of 51 | |

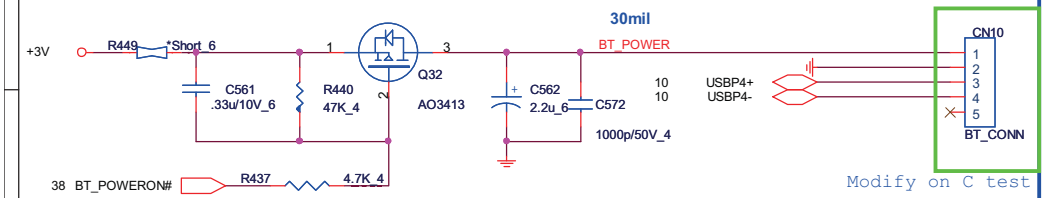
## INT K/B(KBC)



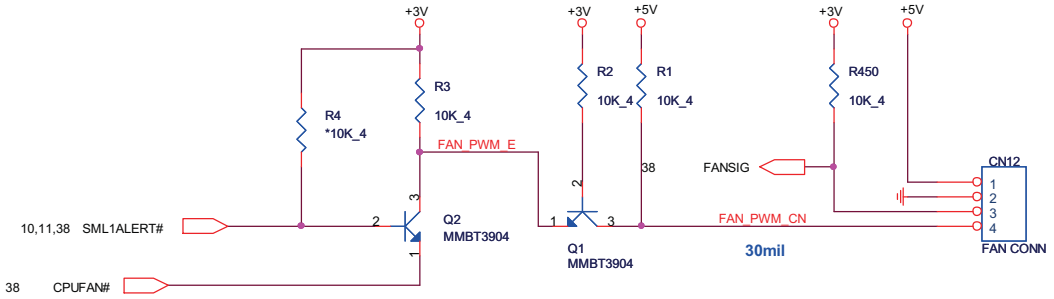

## TOUCHPAD(TPD)




## BLUETOOTH CONNECTOR(BTM)



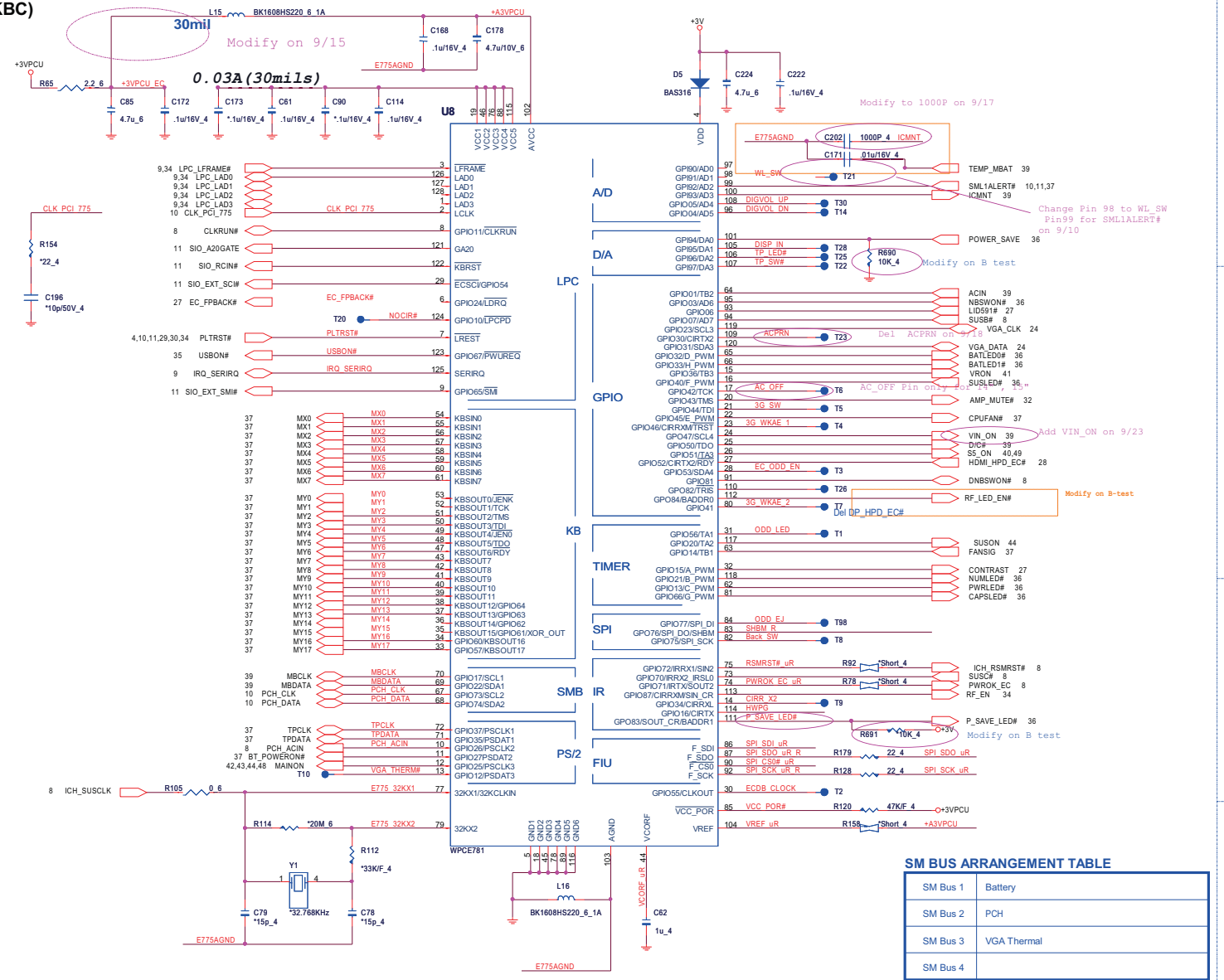

## CPU FAN(THM)




**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | KB/FAN/TP/BT | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 37 of 51 | |

## EC(KBC)




## I/O ADDRESS SETTING

SHBM=0: Enable shared memory with host BIOS

SHBM

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

## SM BUS PU

Change pull-up resistor (R148 /R154) from 10K to 4.7Kohm

## SPI FLASH

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

At 11/24 add

| | | |
|---|---|---|
| Winbond | W25X16AVSSIG | AKE38FP0N01 |
| MXIC | MX25L1605DM2I-12G | AKE38FP0Z00 |
| AMIC | A25L016M-F | AKE38ZN0800 |

## HWPG

## SM BUS ARRANGEMENT TABLE

| | |
|---|---|
| SM Bus 1 | Battery |
| SM Bus 2 | PCH |
| SM Bus 3 | VGA Thermal |
| SM Bus 4 | |

## VR Cap.

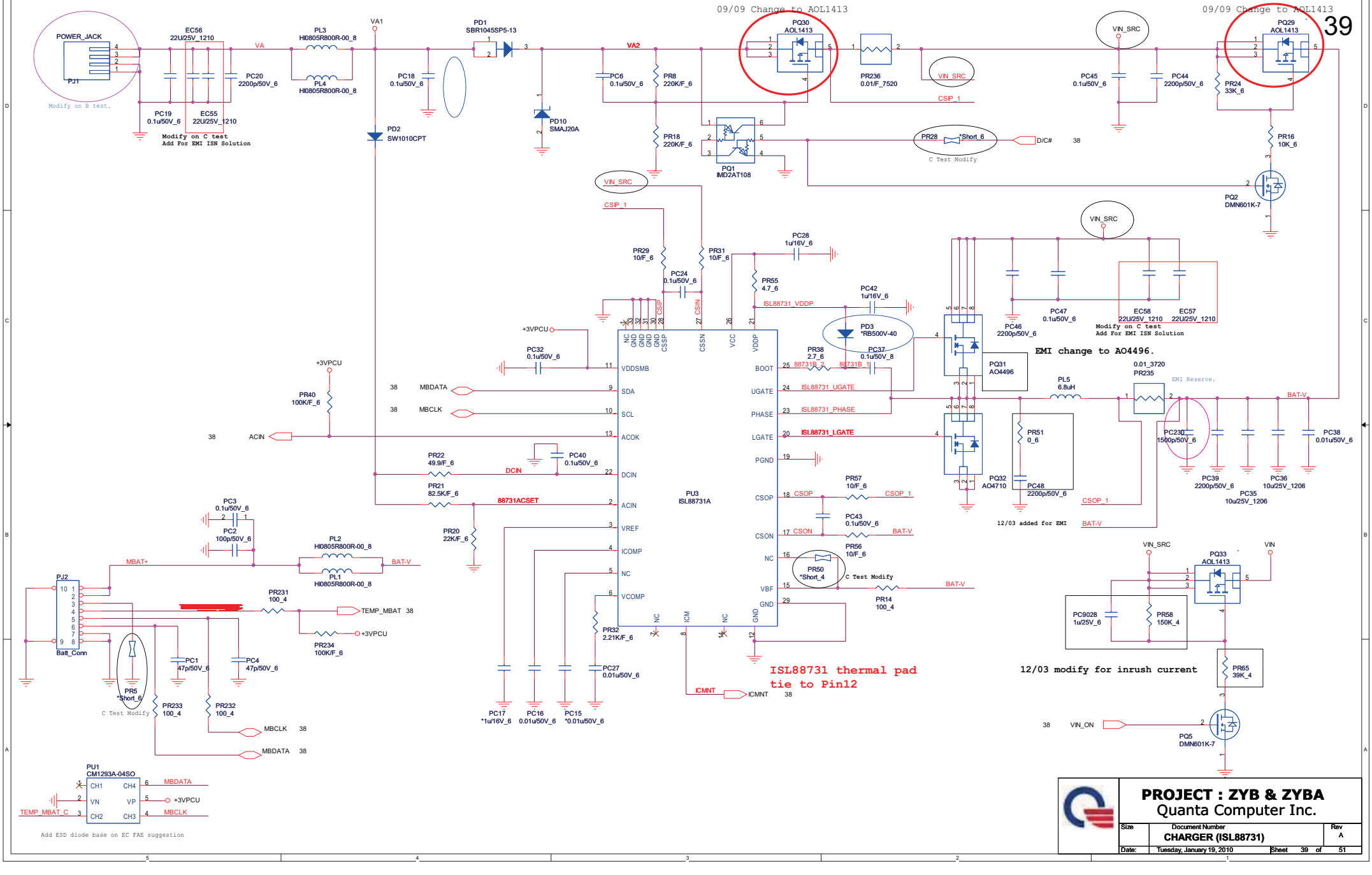
## POWER-ON Switch

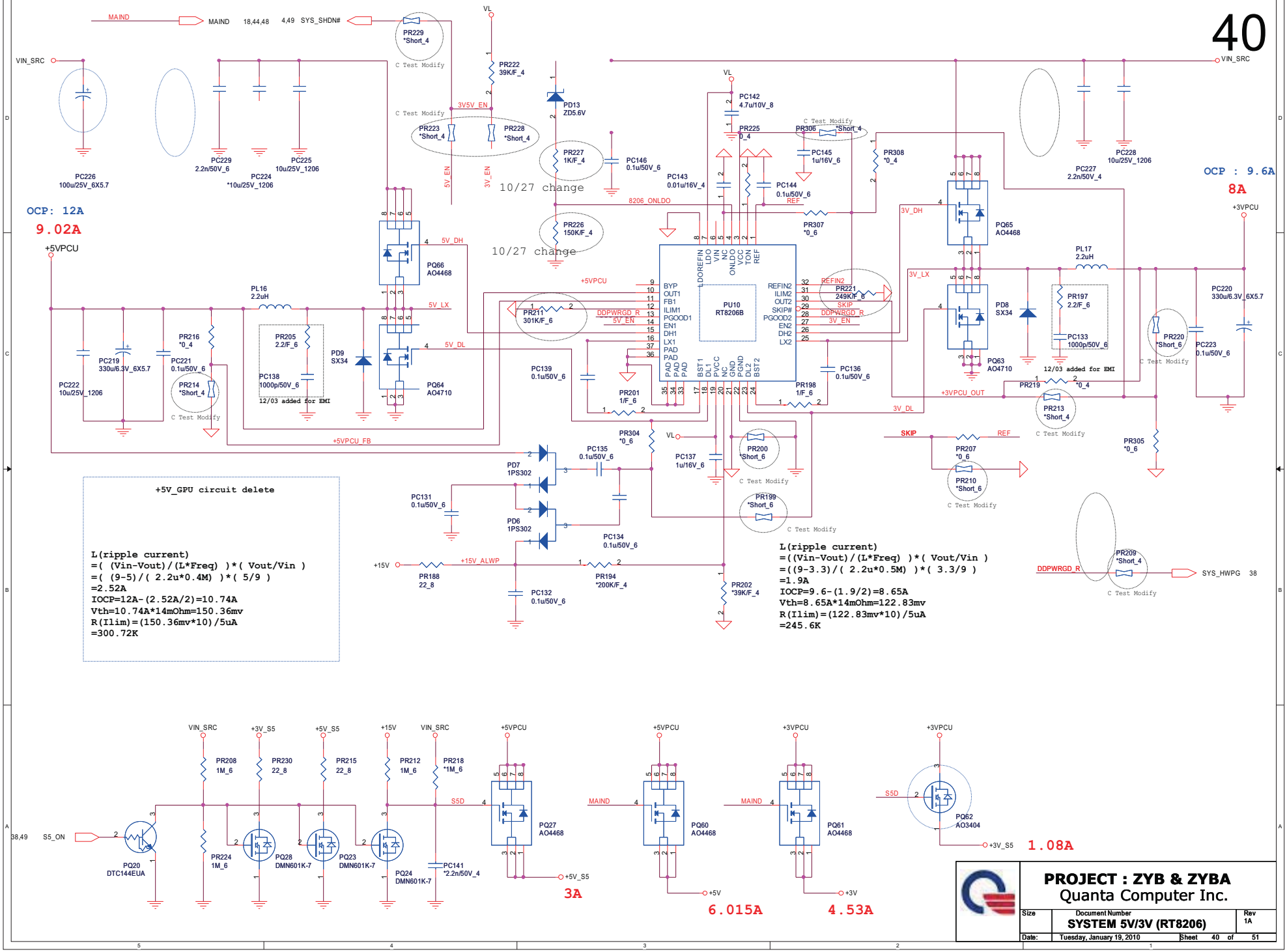
SW1
MSK:NTCQ31-AB1G-A160T

## INTERNAL KEYBOARD STRIP SET

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

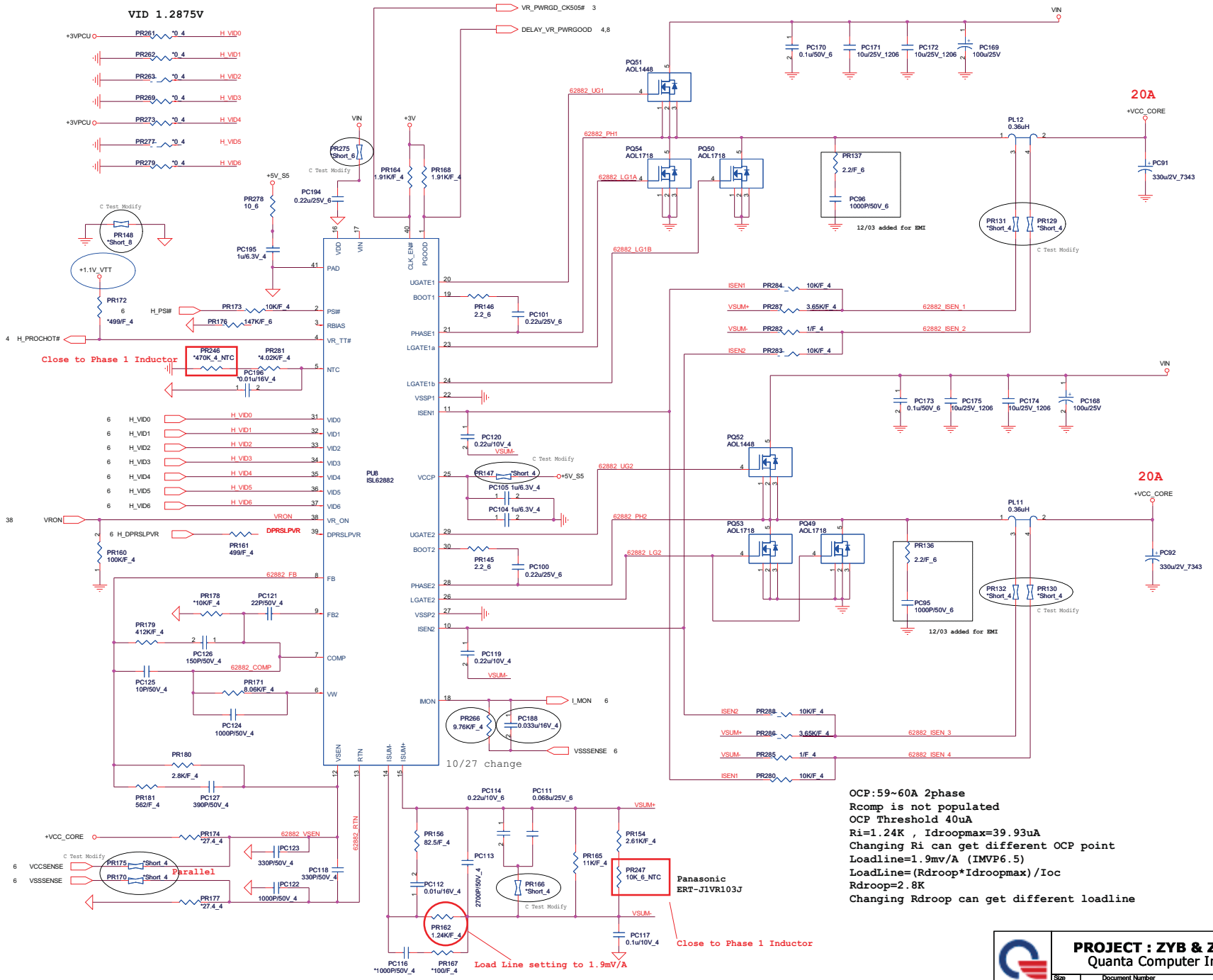
| Size | Document Number | Rev |
|---|---|---|
| | WPCE81 & FLASH | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 38 of 51 | |


09/09 Change to AOL1413
09/09 Change to AOL1413
39
POWER_JACK
PJ1
Modify on B test.
EC56 22U/25V_1210
PC19 0.1u/50V_6
EC55 22U/25V_1210
PC20 2200p/50V_6
Modify on C test
Add For EMI ISN Solution
VA
PL3 HI0805R800R-00_8
PL4 HI0805R800R-00_8
VA1
PC18 0.1u/50V_6
PD2 SW1010CPT
PD1 SBR1045SP5-13
PD10 SMAJ20A
VA2
PC6 0.1u/50V_6
PR8 220K/F_6
PR18 220K/F_6
PQ30 AOL1413
PR236 0.01/F_7520
VIN_SRC
CSIP_1
PQ1 IMD2AT108
PR28 *Short_6
C Test Modify
D/C#
38
PC45 0.1u/50V_6
PC44 2200p/50V_6
PQ29 AOL1413
PR24 33K_6
PR16 10K_6
PQ2 DMN601K-7
PC28 1u/16V_6
PR29 10/F_6
PR31 10/F_6
PC24 0.1u/50V_6
PR55 4.7_6
ISL88731_VDDP
PC42 1u/16V_6
PD3 *RB500V-40
PC37 0.1u/50V_8
+3VPCU
PC32 0.1u/50V_6
PR40 100K/F_6
38 MBDATA
38 MBCLK
38 ACIN
PR22 49.9/F_6
DCIN
PC40 0.1u/50V_6
PR21 82.5K/F_6
88731ACSET
PR20 22K/F_6
PU3 ISL88731A
NC GND GND GND GND CSSP CSSN VCC VDDP
VDDSMB SDA SCL ACOK DCIN ACIN VREF ICOMP NC VCOMP
BOOT UGATE PHASE LGATE PGND CSOP CSON NC VBF GND
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
PR38 2.7_6
88731B_2
88731B_1
PR57 10/F_6
PC43 0.1u/50V_6
PR56 10/F_6
PR50 *Short_4
C Test Modify
PR14 100_4
BAT-V
PR32 2.21K/F_6
PC27 0.01u/50V_6
PC17 *1u/16V_6
PC16 0.01u/50V_6
PC15 *0.01u/50V_6
ICMNT
38
ISL88731 thermal pad tie to Pin12
PC3 0.1u/50V_6
PC2 100p/50V_6
PL2 HI0805R800R-00_8
PL1 HI0805R800R-00_8
MBAT+
PJ2
Batt_Conn
PR231 100_4
TEMP_MBAT 38
PR234 100K/F_6
PC1 47p/50V_6
PC4 47p/50V_6
PR5 *Short_6
C Test Modify
PR233 100_4
PR232 100_4
MBCLK 38
MBDATA 38
PU1 CM1293A-04SO
CH1 CH2 CH3 CH4 VN VP
MBDATA
+3VPCU
MBCLK
TEMP_MBAT_C
Add ESD diode base on EC FAE suggestion
PC46 2200p/50V_6
PC47 0.1u/50V_6
EC58 22U/25V_1210
EC57 22U/25V_1210
Modify on C test
Add For EMI ISN Solution
EMI change to AO4496.
PQ31 AO4496
PQ32 AO4710
PL5 6.8uH
0.01_3720
PR235
EMI Reserve.
PR51 0_6
PC48 2200p/50V_6
12/03 added for EMI
PC230 1500p/50V_6
PC39 2200p/50V_6
PC36 10u/25V_1206
PC35 10u/25V_1206
PC38 0.01u/50V_6
PQ33 AOL1413
PC9028 1u/25V_6
PR58 150K_4
PR65 39K_4
12/03 modify for inrush current
VIN_ON
PQ5 DMN601K-7
PROJECT : ZYB & ZYBA
Quanta Computer Inc.
Size
Document Number
CHARGER (ISL88731)
Rev A
Date: Tuesday, January 19, 2010
Sheet 39 of 51



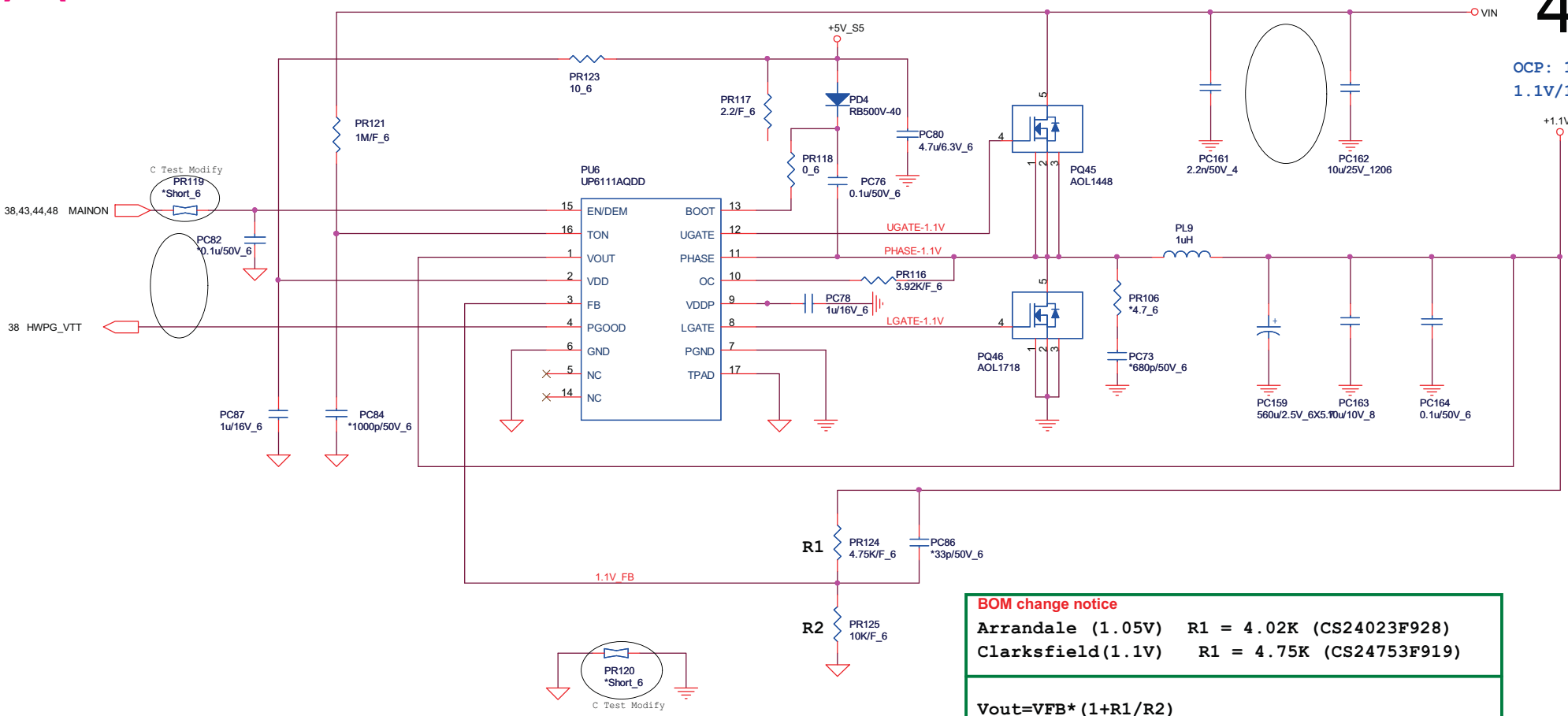

| | | |
|---|---|---|
| PROJECT : ZYB & ZYBA | | |
| Quanta Computer Inc. | | |
| Size | Document Number: SYSTEM 5V/3V (RT8206) | Rev: 1A |
| Date: Tuesday, January 19, 2010 | Sheet 40 of 51 | |

[PWM]




| | |
|---|---|
| PROJECT : ZYB & ZYBA | |
| Quanta Computer Inc. | |
| Size | Document Number: CPU Core ( ISL62882) — Rev: 1A |
| Date: Tuesday, January 19, 2010 | Sheet 41 of 51 |

OCP: 18A
1.1V/13.5A




**BOM change notice**

Arrandale (1.05V) R1 = 4.02K (CS24023F928)
Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

Vout=VFB*(1+R1/R2)
VFB=0.75V

TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

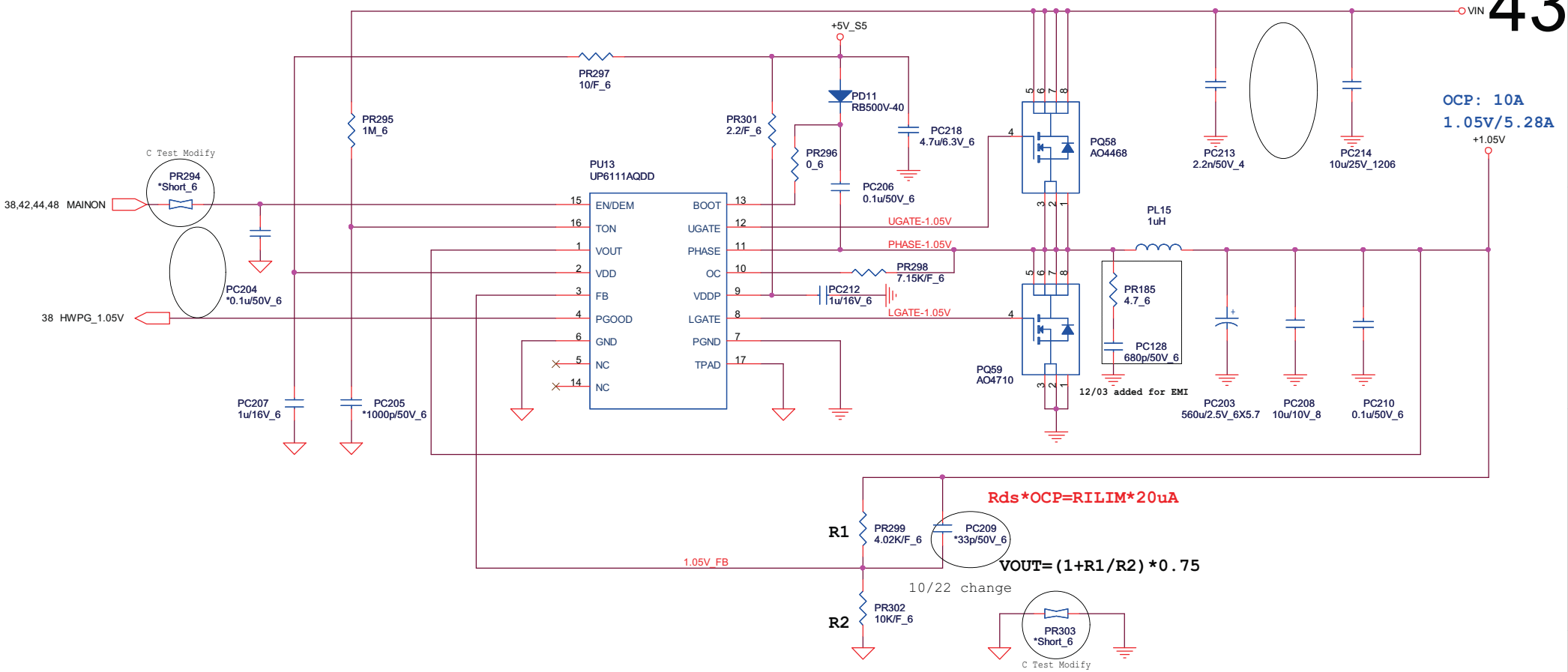
TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm
L(ripple current)
=(19-1.1)*1.1(1u*272k*19)
~3.81A

4.3m*18=RILIM*20uA
RILIM=3.87K --- 3.92K

| | | |
|---|---|---|
| | **PROJECT : ZYB & ZYBA**<br>Quanta Computer Inc. | |
| Size | Document Number<br>+VTT (UP6111A) | Rev<br>1A |
| Date: Tuesday, January 19, 2010 | Sheet 42 of 51 | |




TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

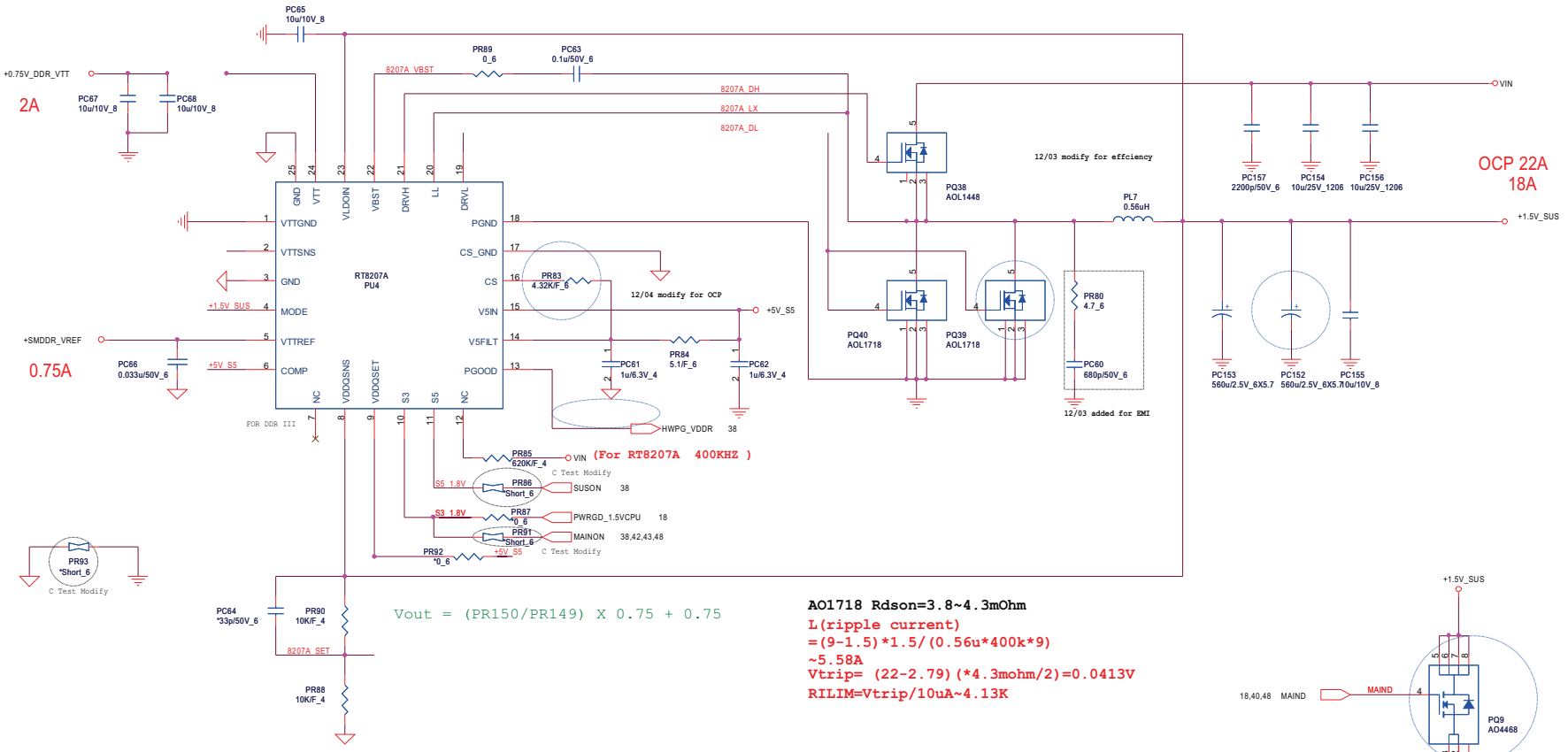
AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

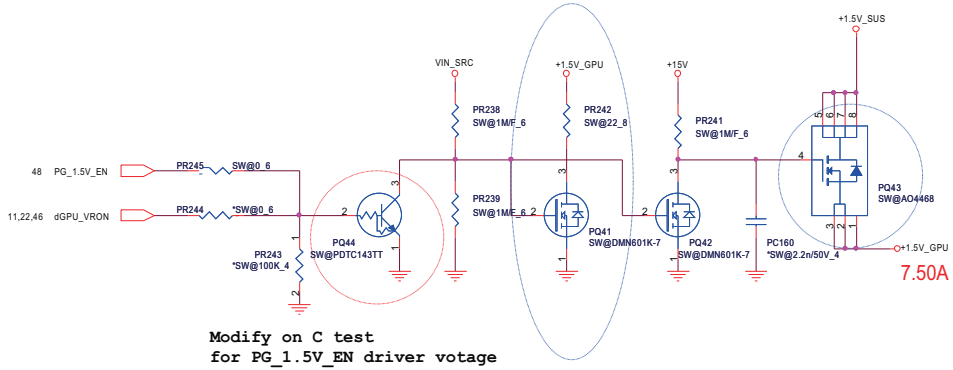
| Size | Document Number | Rev |
|---|---|---|
| | VCCP +1.05V (UP6111A) | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 43 of 51 | |




**AO1718 Rdson=3.8~4.3mOhm**

**L(ripple current)**
**=(9-1.5)*1.5/(0.56u*400k*9)**
**~5.58A**
**Vtrip= (22-2.79)(*4.3mohm/2)=0.0413V**
**RILIM=Vtrip/10uA~4.13K**




**Modify on C test**
**for PG_1.5V_EN driver votage**

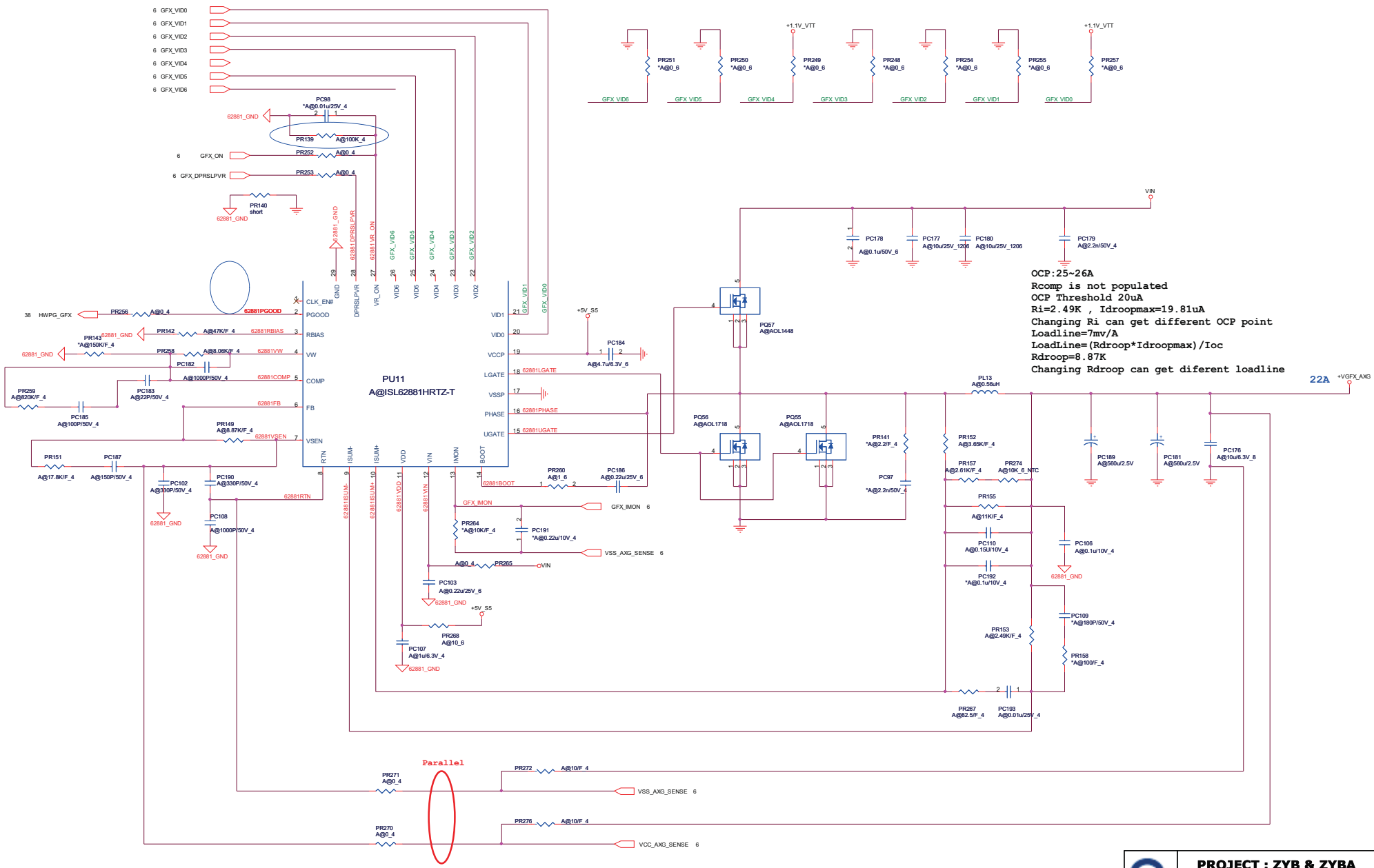
**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | DDR 1.5V(TPS51116) | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 44 of 51 | |

# Int_VGA [PWM]

UMA &SG => +VGFX_AXG Exist
Discrete =>+VGFX_AXG del








**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | +VGFX_AXG (ISL62881) | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 45 of 51 | |

| GPU_VID1 | GPU_VID2 | GPU_VID3 | +VGPU_Core |
|---|---|---|---|
| 0 | 0 | 0 | 1.15V |
| 1 | 0 | 0 | 1.1V |
| 1 | 1 | 0 | 1.0V |
| 0 | 0 | 1 | 0.95V |
| 1 | 0 | 1 | 0.9V |
| 0 | 1 | 1 | 0.85V |
| 1 | 1 | 1 | 0.8V |

12/03 modify for VID0

Note: VID[5:0]=011010=0.9V
VID[5:0]=010110=1.0V

Iocset*Roc=Iocp*Rdroop
OFFSET=1.2V*RCIN/ROFS=30.6mv
Where :
ROFS=39.2K , RCIN=1K
Roc=1.82K
Rdroop =0.44mv/A for Rs=10K,Rdrp2=348 Ohm
T=25 degree C
Iocp is desire max over current 40A
Iocset is recommendation 10uA from Rbias

Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor

Parallel

10/27 change
10/27 change to ESR 6mohm
10/28 change for load line and ocp

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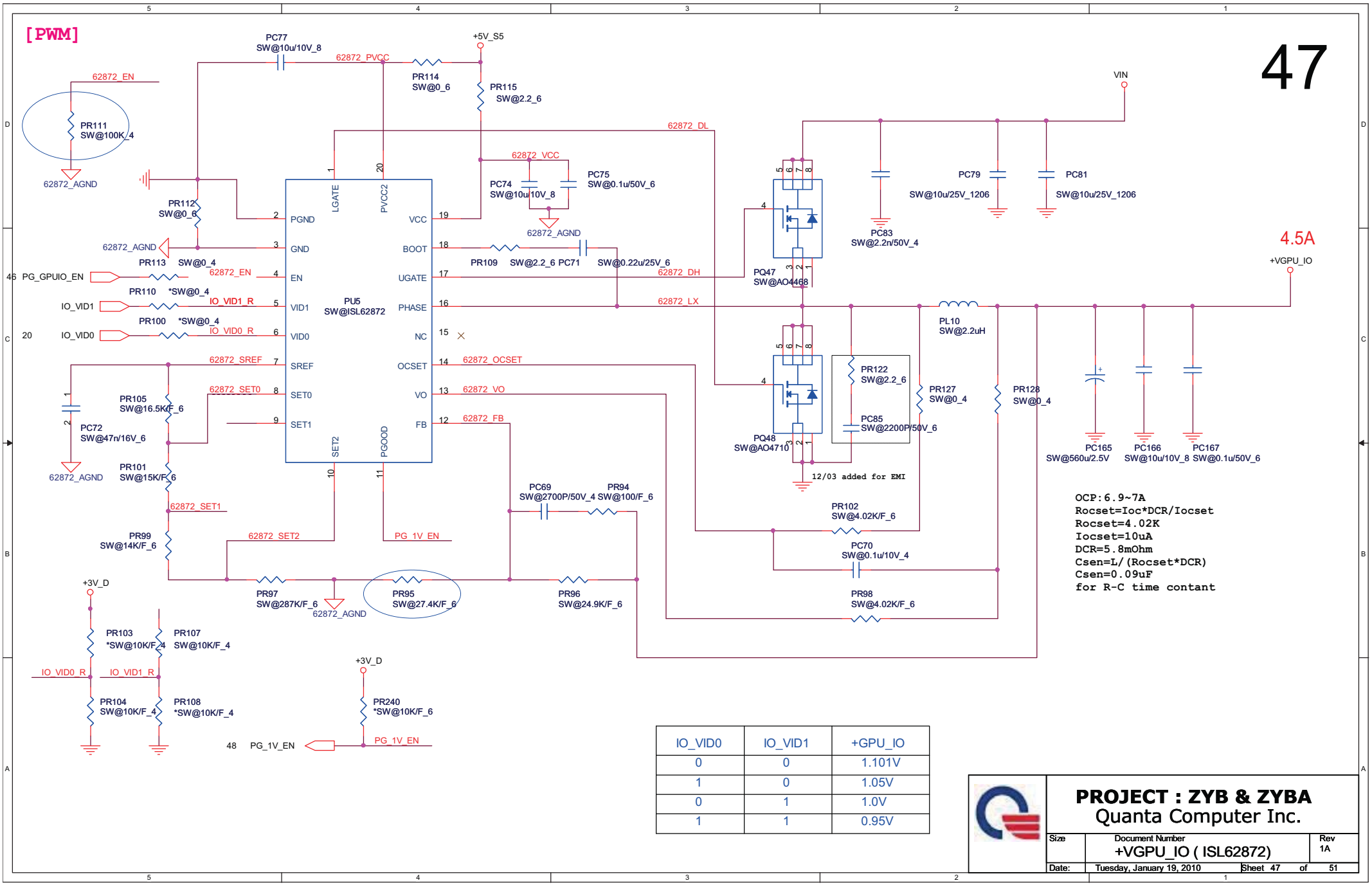
Quanta Computer Inc.
Size | Document Number: +VGPU_Core (ISL6264) | Rev: 1A
Date: Tuesday, January 19, 2010 | Sheet 46 of 51




| IO_VID0 | IO_VID1 | +GPU_IO |
|---|---|---|
| 0 | 0 | 1.101V |
| 1 | 0 | 1.05V |
| 0 | 1 | 1.0V |
| 1 | 1 | 0.95V |

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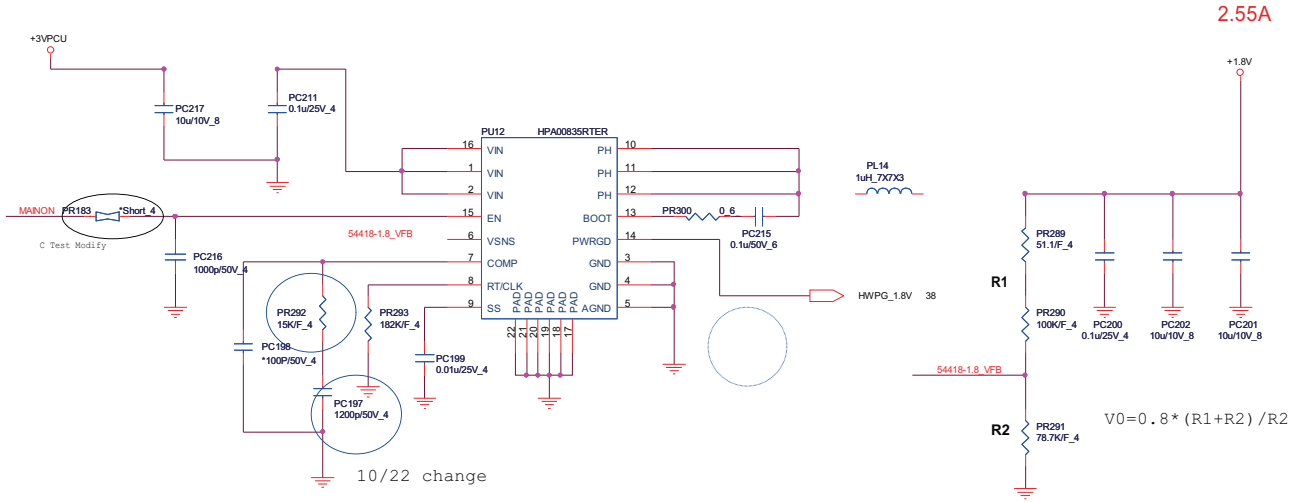
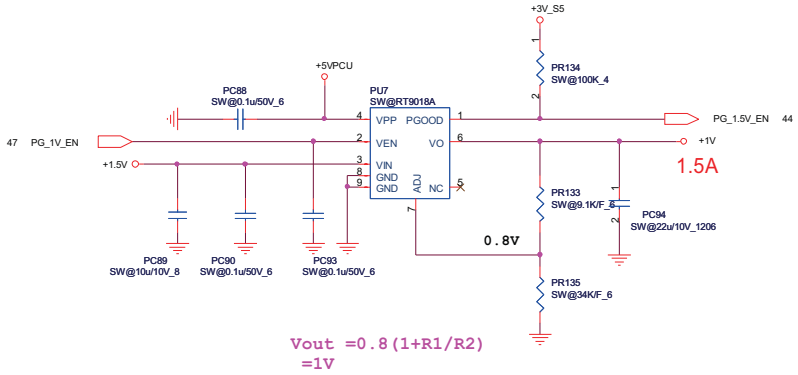
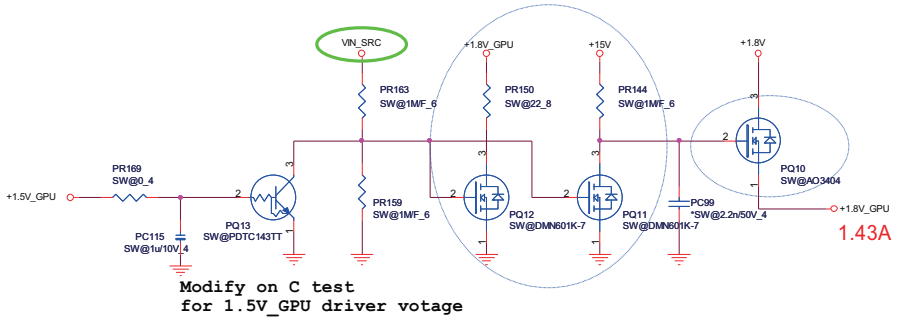
Quanta Computer Inc.

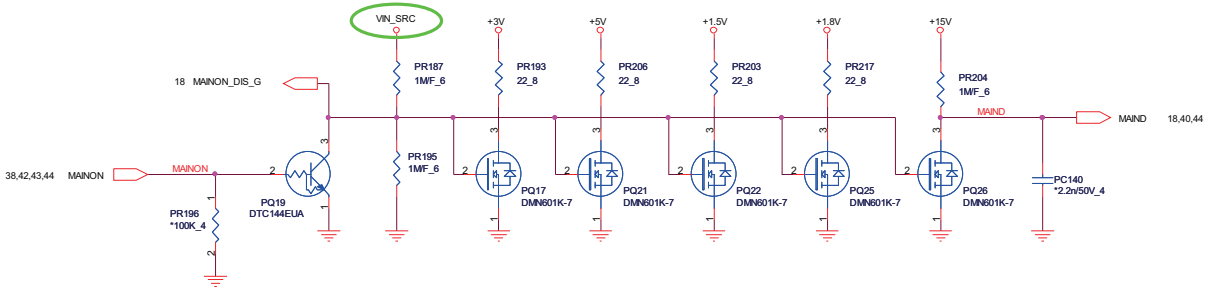
| Size | Document Number | Rev |
|---|---|---|
| | +VGPU_IO ( ISL62872) | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 47 of 51 | |




9/7 change

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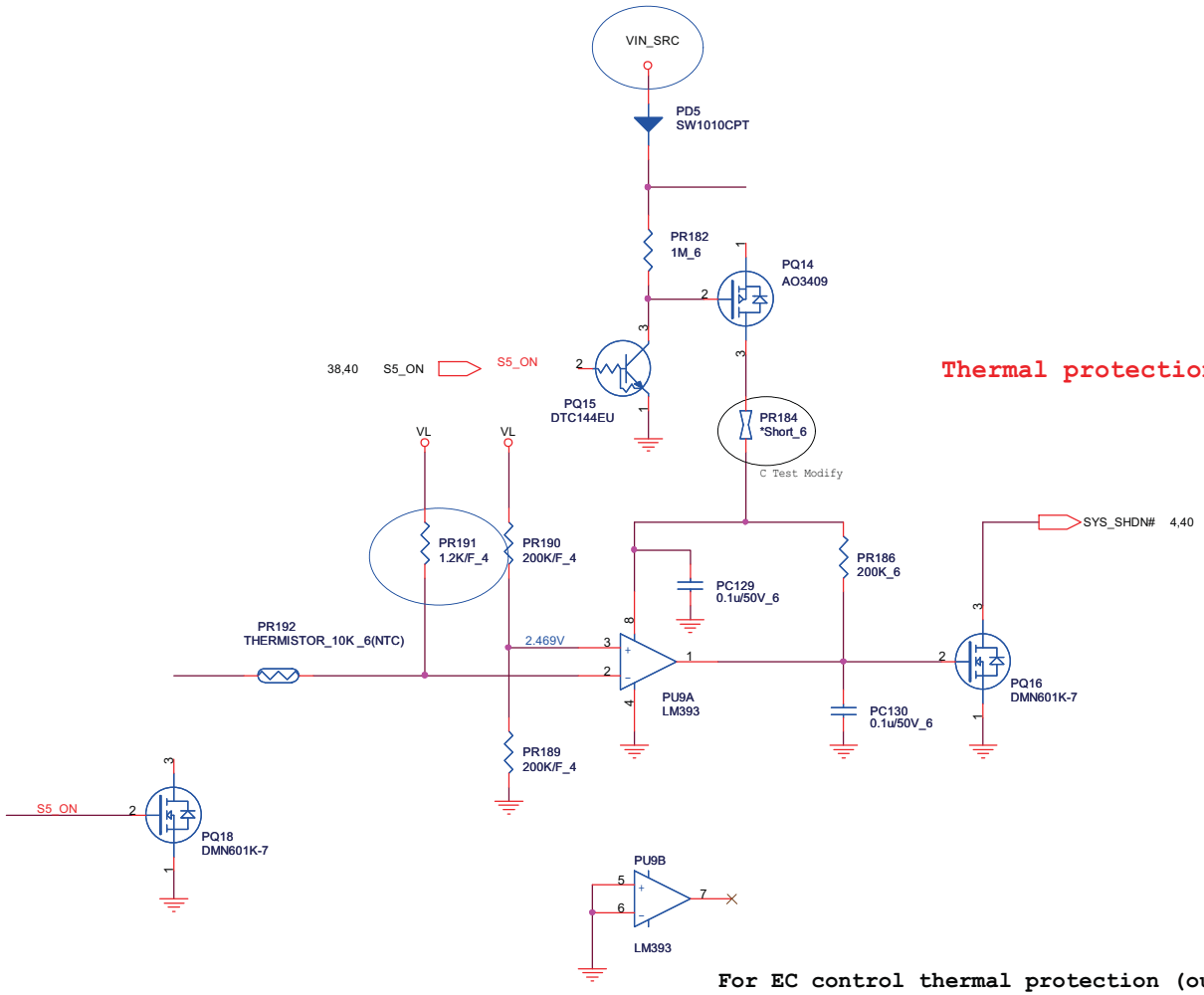
| Size | Document Number | Rev |
|---|---|---|
| | Discharge/1.8V) | 1A |
| Date: Tuesday, January 19, 2010 | Sheet 48 of 51 | |




Thermal protection

For EC control thermal protection (output 3.3V)

| | | |
|---|---|---|
| PROJECT : ZYB & ZYBA<br>Quanta Computer Inc. | | |
| Size | Document Number<br>Thermal protect | Rev<br>1A |
| Date: Tuesday, January 19, 2010 | Sheet 49 of 51 | |

| MODEL: | REV | CHANGE LIST |
|---|---|---|
| ZYB MB | A | ***First release*** |
| | B | ***Page10: USB_OC6# connect to OC1.***<br>***Page21: Change R94 from 680ohm => 51ohm(CS05102FB09) for AMD suggestion.***<br>***Page32: Modify Audio LINE_JD# circuit ,ADD R658 -shot pad and PD12(BC001010Z17) , and del R641 , Q39 .***<br>***Page27: Change R130,R131 from 0 ohm => 15 ohm(CS01502JB12).***<br>***Page28: Change Q14 footprint => UMT_213-3-1_3***<br>***Page29: Change R617 and R621 from 0 ohm => 120 ohm Bead(CX05T121000) for SD card EMI issue.***<br>***Page35: Swap CN32 Pin define and del oc6 on B test***<br>***Page32:Change R334 and R422 from 47ohm => 56ohm(CS05602JB17) for Audio suggestion on B test..***<br>***Page38:add R690(CS31002JB28) pull low for power saving and reserve R691 for LED pin.***<br>***Page34:CN7 and CN14 Pin42 connect to RFLED#***<br>***Page34:Change 2nd HDD conn footprint (sata-ld2822f-saq16-22p-r)and P/N(DFHS22FR239 ).***<br>***Page36:Reserve Q3 , Q19(BAM00840001) and pop R16 ,depop R278 (CS00002JB38) to meet acer 2010 spec , only EC control.***<br>***Page32:Del R598(CS41002JB20) PU Res for AMP.***<br>***Page32:Tune SUB AMP Gain to 20 db => del R286 , add R291 , and add R320 ,R696 to 0 ohm(CS00003J951) on AMP Pin 11 and 12,***<br>***Page22: POP C378 330U(CH733RM8831) fot +VGPU_CORE.***<br>***Page03: Reserve C855(CH41003ZB35) and C856(CH61001ME96) on U21 Clock Gen 1.5V .***<br>***Page :0 ohm short for cost down***<br>***R78,R92,R158,R160,R199,R205,R206,R207,R208,R248,R249,R250,R255,R275,R282,R283,***<br>***R284,R285,R382,R383,R396,R408,R410,R415,R430,R514,R546,R576,R578,R583,R590,R591,R599,R600,R601.R602,R603,***<br>***R637,R643,R658,R660,R665,R671,R676,R679,R681,R685,R686***<br>***Page35: Change C424 p/n => CH51002M930.***<br>***Page39: Add PC9028(CH5104K9906) , change PR58 from 33k => 150k(CS41502JB10) and change PR65 from 10k => 39K(CS33902JB01) for inrush current issue.***<br>***Page39: Add PR51/ 0ohm(CS00003J951) and PC48/2200p(CH22206K917) for EMI suggestion.***<br>***Page39:Change PJ1 pin define , Pin1, 2 =>GND , Pin3, 4=>Vin .***<br>***Page39: Change PQ31 from P/N BAM44680003 =>BAM44960000.***<br>***Page39: Reserve PC230/1000p(CH21006K917)for EMI suggestion.***<br>***Page40: Add PR197,PR205 2.2ohm(CS-2203F911) and PC133 ,PC138 1000p(CH21006K917) for EMI suggestion.***<br>***Page41: Add PR137,PR136 /2.2ohm(CS-2203F911) and PC96,PC95/1000p(CH21006K917) for EMI suggestion.***<br>***Page41: Change PU8 footprint QFN40-5X5-4-41P-0_75H => qfn40-5x5-4-41p-0_75h-smt .***<br>***Page43: Add PR185 /4.7ohm(CS-4703J917) and PC128/680p(CH16806J911) for EMI suggestion.***<br>***Page44: Add PR80 /4.7ohm(CS-4703J917) and PC60/680p(CH16806J911) for EMI suggestion.***<br>***Page44: Change PR83 from 4.02k=>4.32k(CS24323F911) to modify OCP.***<br>***Page46: POP PR70(CS31003J941) and depop PR59 for VGPUCORE VID0.***<br>***Page46: Change PR41 PN from 39.2k => 60.4K(CS36042FB10).***<br>***Page47: Add PR122(CS-2203J913) and PC85(CH22206K917) for EMI issue.***<br>***Page48: Change PU12 PN from AL054418000 => AL000835000.*** |

| MODEL / PAGE | ZR6 MB FROM | ZR6 MB TO |
|---|---|---|
| 1 | 1A | |
| 2 | 1A | 3B |
| 3 | 1A | |
| 4 | 1A | |
| 5 | 2A | |
| 6 | 1A | |
| 7 | 1A | |
| 8 | 1A | |
| 9 | 3A | |
| 10 | 3A | |
| 11 | 1A | 3B |
| 12 | 1A | |
| 13 | 1A | |
| 14 | 3A | |
| 15 | 2A | |
| 16 | 1A | |
| 17 | 3A | 3B |
| 18 | 2A | |
| 19 | 3A | |
| 20 | 1A | |
| 21 | 3A | |
| 22 | 1A | |
| 23 | 3A | |
| 24 | 3A | |
| 25 | 2A | |
| 26 | 3A | |
| 27 | 2A | |
| 28 | 3A | |
| 29 | 3A | 3B |
| 30 | 1A | |
| 31 | 3A | |
| 32 | 2A | |
| 33 | 2A | |
| 34 | 2A | |
| 35 | 2A | 3B |
| 36 | 2A | |
| 37 | 2A | |
| 38 | 2A | |
| 39 | 3A | 3B |
| 40 | | |

| | | |
|---|---|---|
| MB Assy' P/N: 31ZYBMB0000/10/80 | Project :ZYB MB | Document No.: |
| Approved by : J. C | Drawing by :Jason Twu | DATE: 2009/10/20 |

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | Change list | 1A |
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| MODEL: | REV |
|---|---|
| ZYB MB | C |

# CHANGE LIST

*Page12: Change C443 from 10u/0603 =>22u/0603(CH6221M9900) for CRT Flicker issue.*
*Page20 : Change C169,C66 from 10u/0603 =>22u/0603(CH6221M9900) for CRT Flicker issue.*

*Page27: Del R459,R460 Add L69 for Mic EMI issue.*

*Page03: Add R464 Reserve CPU_SEL PIN PU to +3V.*

*Page08,21:Change R309 C759 Footprint from RC0402-C , CC0402-C =>RC0402 , CC0402*

*Page29:Change CN11 => DFHD36MS012(4in1-r015-212-lm-42p-h-nb4).*

*Page27:Add Fuse F1(DK100TPU028) on CRT VCC for safty requirement.*

*Page28:Add Fuse F2(DK100TPU028) on HDMI VCC for safty requirement.*

*Page:0805- R596,R593,R387,R276,R277,R10,R21,R191,R198,R239,R439,R455,R458*
*0603- R321,R335,R296,R323,R352,R319,R333,R336,R404,R310,R613,R302,R315,R401,R579,R449,R375*
*0402- R317,R597,R568,R536,R535,R291,R292,R54*

*Page37:Change CN10 => DFWF05MR027 (87213-05XX-5P-L)*

*Page27:Reserve 2 varistor(RV4,RV5) for DMIC_CLK , DMIC_DATA to solve ESD, Add R320,R459 for EMI request.*

*Page27:Change LvdS SW circuit to solve leakage current , del R464 and PD R451 100K/0402(CS41002JB20).*

*Page32 : remove R320,R696 cost down , change R326 and R313 to 1K_4(CS21002JB34) to meet vender spec.*

*Page32 : Change L24~L29 to CX60808T012 EMI FILTER SBK160808T-221Y-N(200MA) for EMI Request.*

*Page36 : Change Q3,Q19 connector to WLAN For Acer LES spec V3.4*

*Page36 : Change Q3,Q19 connector to WLAN For Acer LES spec V3.4*
*Page39:Change R443,R442,R447 to 1.2K(CS21202FB13) and R444,R441 to 680(CS16802JB27) ohm to meet Acer LED Spec.*

*Page39:Add EC55,EC56,EC57,EC58 22u/25V 1210(CH6224K9300) for EMI ISN solution*

*Page39:Change PC147 to EC58*

*Page39:Change PU3 footprint QFN28-5X5-5-33P => QFN28-5X5-5-33P-SMT*

*Page44:Change PQ44 PN from BA144EUAZ04 to BA001430Z49.*

*Page45:Change PU11 footprint qfn28-4x4-4-31p => QFN28-4X4-4-29P-SMT*

*Page48:Change PQ13 PN from BA144EUAZ04 to BA001430Z49*

*Page:0805- PR148*
*0603- PR28,PR5,PR220,PR210,PR200,PR199,PR275,PR119,PR120,PR294,PR303,PR93,PR86,PR91,PR184*
*0402- PR50,PR213,PR209,PR306,PR228,PR223,PR229,PR214,PR131,PR129,PR132,PR130,PR147,PR175,PR170,PR166,PR183,PR166*

| MODEL | ZR6 MB | |
|---|---|---|
| PAGE | FROM | TO |
| 1 | 1A | |
| 2 | 1A | 3B |
| 3 | 1A | |
| 4 | 1A | |
| 5 | 2A | |
| 6 | 1A | |
| 7 | 1A | |
| 8 | 1A | |
| 9 | 3A | |
| 10 | 3A | |
| 11 | 1A | 3B |
| 12 | 1A | |
| 13 | 1A | |
| 14 | 3A | |
| 15 | 2A | |
| 16 | 1A | |
| 17 | 3A | 3B |
| 18 | 2A | |
| 19 | 3A | |
| 20 | 1A | |
| 21 | 3A | |
| 22 | 1A | |
| 23 | 3A | |
| 24 | 3A | |
| 25 | 2A | |
| 26 | 3A | |
| 27 | 2A | |
| 28 | 3A | |
| 29 | 3A | 3B |
| 30 | 1A | |
| 31 | 3A | |
| 32 | 2A | |
| 33 | 2A | |
| 34 | 2A | |
| 35 | 2A | 3B |
| 36 | 2A | |
| 37 | 2A | |
| 38 | 2A | |
| 39 | 3A | 3B |
| 40 | | |

| | | |
|---|---|---|
| MB Assy' P/N: 31ZYBMB0000/10/80 | Project :ZYB MB | Document No.: |
| Approved by : J. C | Drawing by :Jason Twu | DATE: 2009/10/20 |

**PROJECT : ZYB & ZYBA**
Quanta Computer Inc.

| Size | Document Number | Rev |
|---|---|---|
| | Change list | 1A |
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