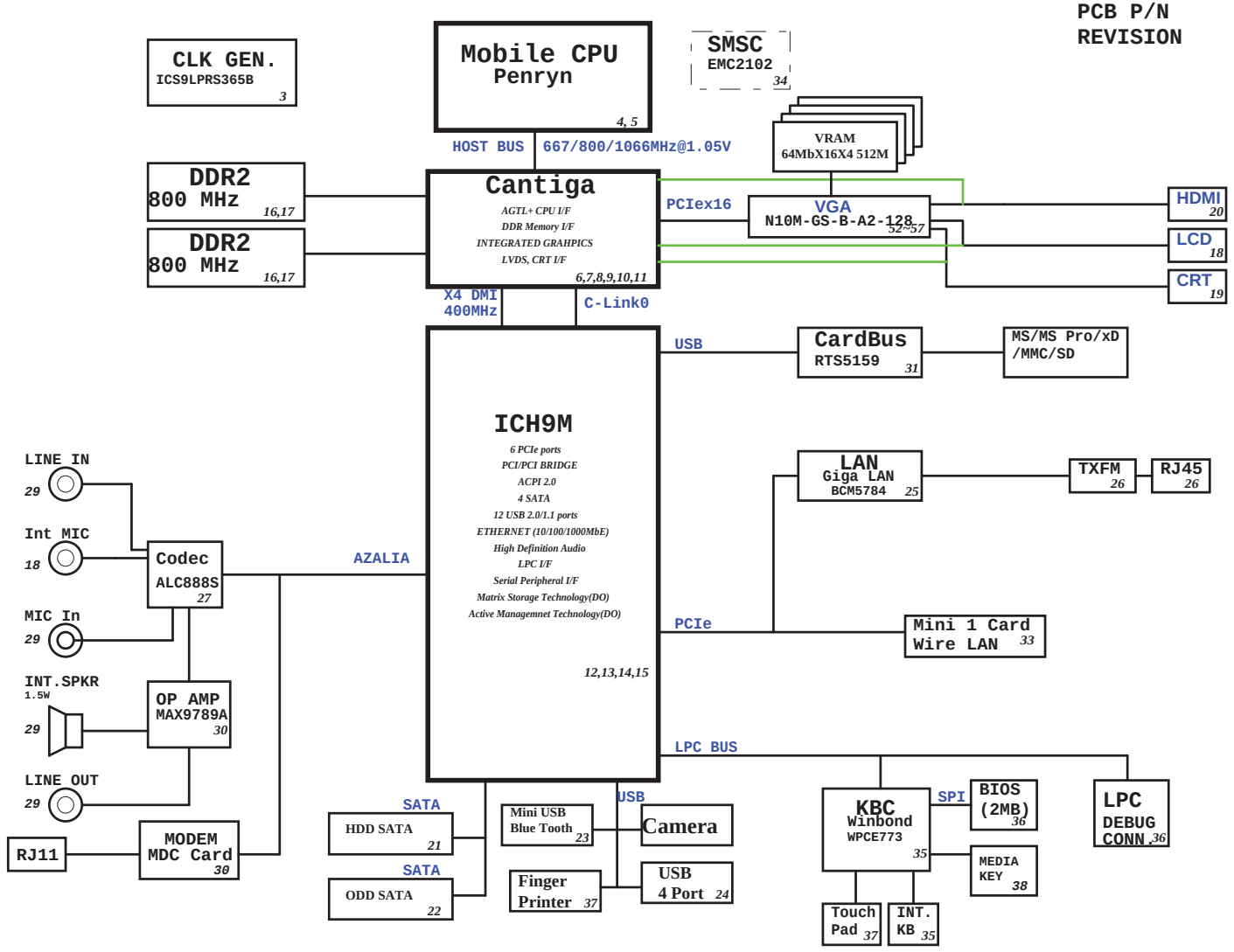
# JV71-MV Block Diagram

Project code: 91.4FX01.001
PCB P/N : 48.4FX01.0SA
REVISION : 09242 -1




**SYSTEM DC/DC** ISL62392 *42*

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | 5V_S5(6A)<br>3D3V_S5(7A)<br>5V_AUX_S5<br>3D3V_AUX_S5 |

**SYSTEM DC/DC** TPS51124 *43*

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | 1D05V_S0(9A)<br>1D5V_S3(12A) |

**RT9026** *44*

| | |
|---|---|
| 1D5V_S3 | DDR_VREF_S3 (1.2A) |

**RT9018** *44*

| | |
|---|---|
| 1D5V_S3 | 1D1V_S0(2A) |

**TPS51117** *45*

| | |
|---|---|
| DCBATOUT | FBVDD(4A) |

**CHARGER** ISL88731A *47*

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | BT+ |

**CPU DC/DC** ISL6266A *41*

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | VCC_CORE 38A |

**VGA_CORE** RT8202A *47*

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | VGA_CORE 13A |

**GFXCORE** ISL6263A *46*

| INPUTS | OUTPUTS |
|---|---|
| DCBATOUT | VCC_GFXCORE (7A) |

**PCB STACKUP**

| | |
|---|---|
| TOP | L1 |
| GND | L2 |
| S | L3 |
| S | L4 |
| GND | L5 |
| BOTTOM | L6 |

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

| Size | Document Number | Rev |
|---|---|---|
| A2 | JV71 | -2 |

Date: Thursday, July 02, 2009 Sheet 1 of 60

# ICH9M Functional Strap Definitions

| Signal | Usage/When Sampled | Comment |
|---|---|---|
| HDA_SDOUT | XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK | Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down |
| HDA_SYNC | PCIE config1 bit0, Rising Edge of PWROK. | This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h) |
| GNT2#/ GPIO53 | PCIE config2 bit2, Rising Edge of PWROK. | This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h) |
| GPIO20 | Reserved | This signal should not be pulled high. |
| GNT1#/ GPIO51 | ESI Strap (Server Only) Rising Edge of PWROK | ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile. |
| GNT3#/ GPIO55 | Top-Block Swap Override. Rising Edge of PWROK. | Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT0#: SPI_CS1#/ GPIO58 | Boot BIOS Destination Selection 0:1. Rising Edge of PWROK. | Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC. |
| SPI_MOSI | Integrated TPM Enable, Rising Edge of CLPWROK | Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable. |
| GPIO49 | DMI Termination Voltage, Rising Edge of PWROK. | The signal is required to be low for desktop applications and required to be high for mobile applications. |
| SATALED# | PCI Express Lane Reversal. Rising Edge of PWROK. | Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8) |
| SPKR | No Reboot. Rising Edge of PWROK. | If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit. |
| TP3 | XOR Chain Entrance. Rising Edge of PWROK. | This signal should not be pull low unless using XOR Chain testing. |
| GPIO33/ HDA_DOCK _EN# | Flash Descriptor Security Override Strap Rising Edge of PWROK | Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister. |

# ICH9M Integrated Pull-up and Pull-down Resistors



| SIGNAL | Resistor Type/Value |
|---|---|
| CL_CLK[1:0] | PULL-UP 20K |
| CL_DATA[1:0] | PULL-UP 20K |
| CL_RST0# | PULL-UP 20K |
| DPRSLPVR/GPIO16 | PULL-DOWN 20K |
| ENERGY_DETECT | PULL-UP 20K |
| HDA_BIT_CLK | PULL-DOWN 20K |
| HDA_DOCK_EN#/GPIO33 | PULL-UP 20K |
| HDA_RST# | PULL-DOWN 20K |
| HDA_SDIN[3:0] | PULL-DOWN 20K |
| HDA_SDOUT | PULL-DOWN 20K |
| HDA_SYNC | PULL-DOWN 20K |
| GLAN_DOCK# | The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller |
| GNT[3:0]#/GPIO[55,53,51] | PULL-UP 20K |
| GPIO[20] | PULL-DOWN 20K |
| GPIO[49] | PULL-UP 20K |
| LDA[3:0]#/FHW[3:0]# | PULL-UP 20K |
| LAN_RXD[2:0] | PULL-UP 20K |
| LDRQ[0] | PULL-UP 20K |
| LDRQ[1]/GPIO23 | PULL-UP 20K |
| PME# | PULL-UP 20K |
| PWRBTN# | PULL-UP 20K |
| SATALED# | PULL-UP 15K |
| SPI_CS1#/GPIO58/CLGPIO6 | PULL-UP 20K |
| SPI_MOSI | PULL-DOWN 20K |
| SPI_MISO | PULL-UP 20K |
| SPKR | PULL-DOWN 20K |
| TACH_[3:0] | PULL-UP 20K |
| TP[3] | PULL-UP 20K |
| USB[11:0][P,N] | PULL-DOWN 15K |

# Cantiga chipset and ICH9M I/O controller Hub strapping configuration



| Pin Name | Strap Description | Configuration |
|---|---|---|
| CFG[2:0] | FSB Frequency Select | 000 = FSB1067<br>011 = FSB667<br>010 = FSB800<br>others = Reserved |
| CFG[4:3]<br>CFG8<br>CFG[15:14]<br>CFG[18:17] | Reserved | |
| CFG5 | DMI x2 Select | 0 = DMI x2<br>1 = DMI x4 (Default) |
| CFG6 | iTPM Host Interface | 0= The iTPM Host Interface is enabled(Note2)<br>**1=The iTPM Host Interface is disalbed(default)** |
| CFG7 | Intel Management engine Crypto strap | 0 = Transport Layer Security (TLS) cipher suite with no confidentiality<br>**1 = TLS cipher suite with confidentiality (default)** |
| CFG9 | PCIE Graphics Lane | 0 = Reverse Lanes,15->0,14->1 ect..<br>**1= Normal operation(Default):Lane Numbered in order** |
| CFG10 | PCIE Loopback enable | 0 = Enable (Note 3)<br>**1= Disabled (default)** |
| CFG[13:12] | XOR/ALL | 00 = Reserve<br>10 = XOR mode Enabled<br>01 = ALLZ mode Enabled (Note 3)<br>**11 = Disabled (default)** |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT Disabled<br>**1 = Dynamic ODT Enabled (Default)** |
| CFG19 | DMI Lane Reversal | **0 = Normal operation(Default): Lane Numbered in Order**<br>1 = Reverse Lanes<br>DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3)<br>DMI x2 mode[MCH -> ICH]:(3->0,2->1) |
| CFG20 | Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe | **0 = Only Digital Display Port or PCIE is operational (Default)**<br>1 =Digital display Port and PCIe are operting simulataneously via the PEG port |
| SDVO_CTRLDATA | SDVO Present | **0 =No SDVO Card Present (Default)**<br>1 = SDVO Card Present |
| L_DDC_DATA | Local Flat Panel (LFP) Present | **0 = LFP Disabled (Default)**<br>1= LFP Card Present; PCIE disabled |

**NOTE:**
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.



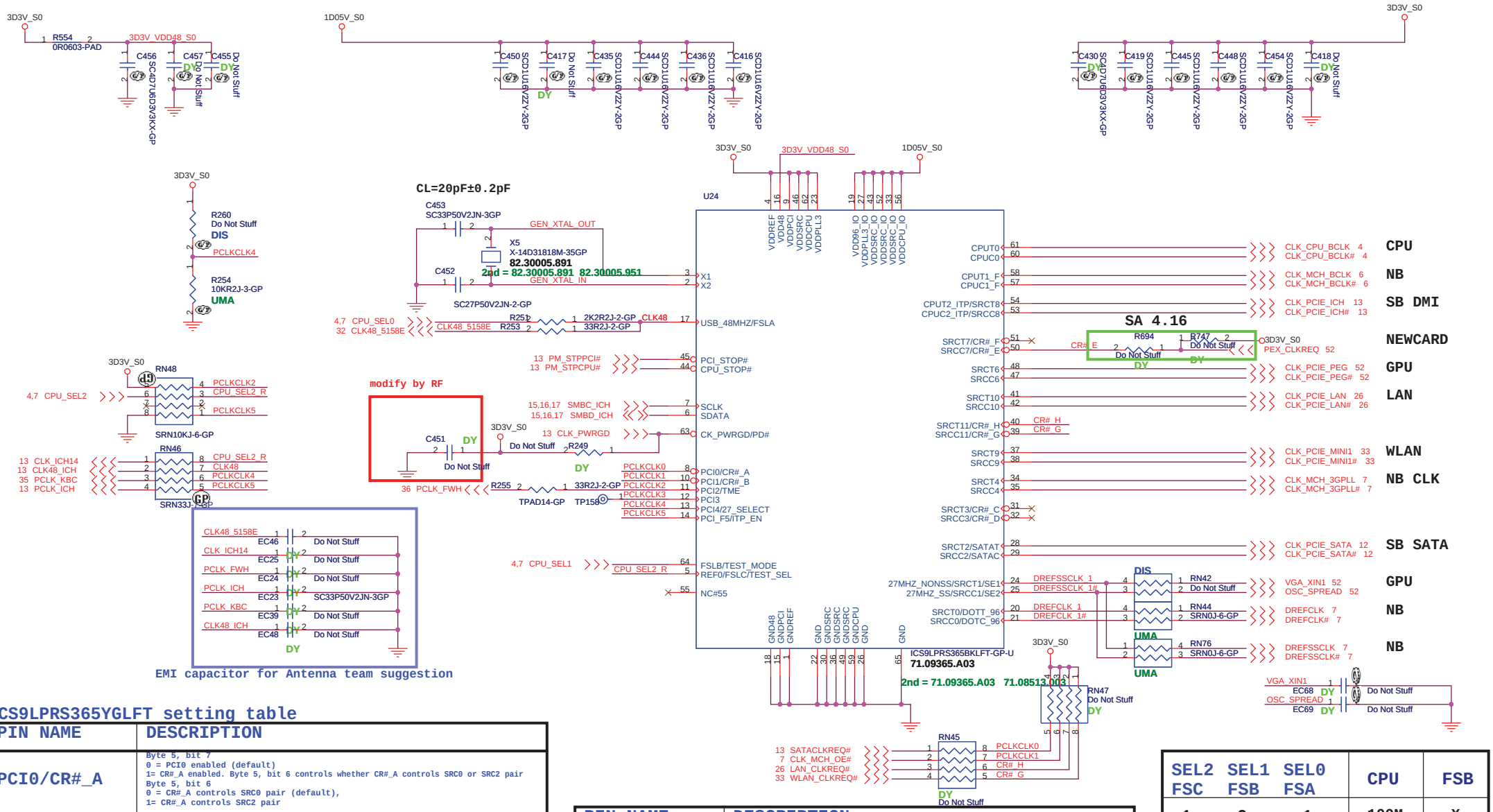
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reference

Size: A3 | Document Number: JV71 | Rev: -2

Date: Thursday, July 02, 2009 | Sheet 2 of 60




## ICS9LPRS365YGLFT setting table

| PIN NAME | DESCRIPTION |
|---|---|
| PCI0/CR#_A | Byte 5, bit 7<br>0 = PCI0 enabled (default)<br>1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair<br>Byte 5, bit 6<br>0 = CR#_A controls SRC0 pair (default),<br>1= CR#_A controls SRC2 pair |
| PCI1/CR#_B | Byte 5, bit 5<br>0 = PCI1 enabled (default)<br>1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair<br>Byte 5, bit 4<br>0 = CR#_B controls SRC1 pair (default)<br>1= CR#_B controls SRC4 pair |
| PCI2/TME | 0 = Overclocking of CPU and SRC Allowed<br>1 = Overclocking of CPU and SRC NOT allowed |
| PCI3 | |
| PCI4/27M_SEL | 0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96#<br>1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0# |
| PCI_F5/ITP_EN | 0 =SRC8/SRC8#<br>1 = ITP/ITP# |
| SRCT3/CR#_C | Byte 5, bit 3<br>0 = SRC3 enabled (default)<br>1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair<br>Byte 5, bit 2<br>0 = CR#_C controls SRC0 pair (default),<br>1= CR#_C controls SRC2 pair |

| PIN NAME | DESCRIPTION |
|---|---|
| SRCC3/CR#_D | Byte 5, bit 1<br>0 = SRC3 enabled (default)<br>1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair<br>Byte 5, bit 0<br>0 = CR#_D controls SRC1 pair (default)<br>1= CR#_D controls SRC4 pair |
| SRCC7/CR#_E | Byte 6, bit 7<br>0 = SRC7# enabled (default)<br>1= CR#_F controls SRC6 |
| SRCT7/CR#_F | Byte 6, bit 6<br>0 = SRC7 enabled (default)<br>1= CR#_F controls SRC8 |
| SRCC11/CR#_G | Byte 6, bit 5<br>0 = SRC11# enabled (default)<br>1= CR#_G controls SRC9 |
| SRCT11/CR#_H | Byte 6, bit 4<br>0 = SRC11 enabled (default)<br>1= CR#_H controls SRC8 |

| SEL2 FSC | SEL1 FSB | SEL0 FSA | CPU | FSB |
|---|---|---|---|---|
| 1 | 0 | 1 | 100M | X |
| 0 | 0 | 1 | 133M | 533M |
| 0 | 1 | 1 | 166M | 667M |
| 0 | 1 | 0 | 200M | 800M |
| 0 | 0 | 0 | 266M | 1067M |

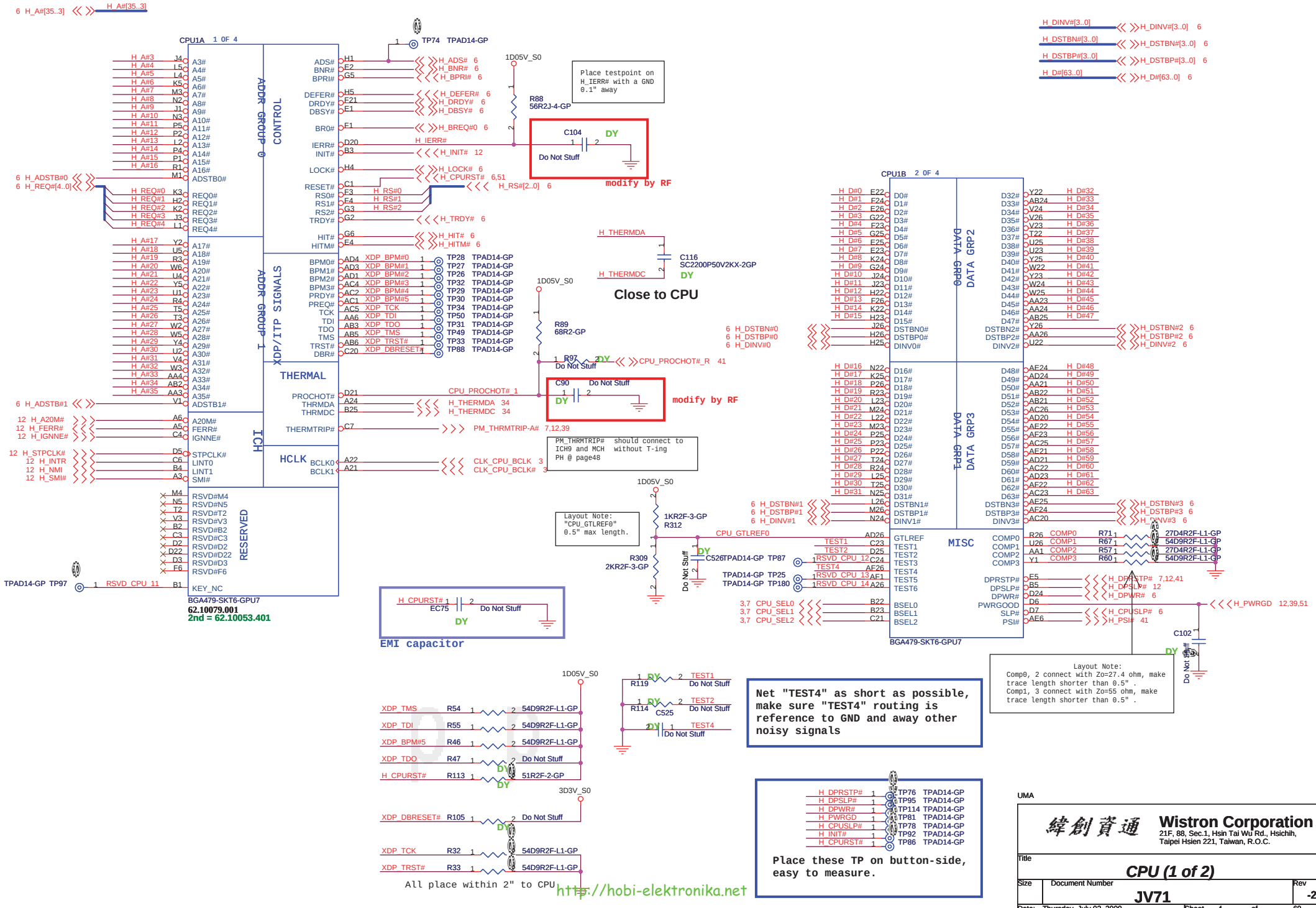
UMA

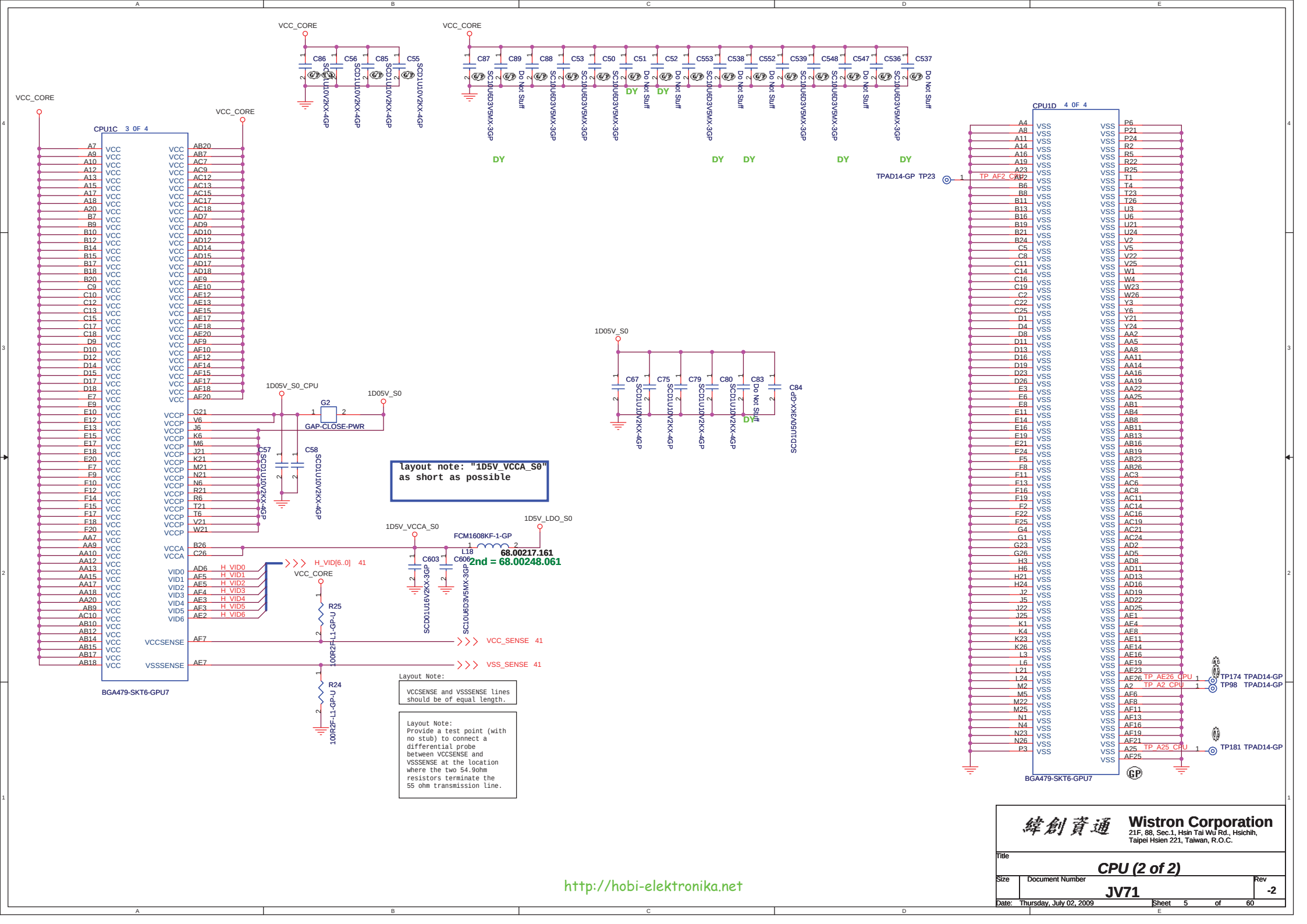
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Clock Generator

Size | Document Number: JV71 | Rev: -2

Date: Thursday, July 02, 2009 | Sheet 3 of 60


CPU1A 1 0F 4
ADDR GROUP 0
CONTROL
ADDR GROUP 1
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU7
62.10079.001
2nd = 62.10053.401
CPU1B 2 0F 4
DATA GRP2
DATA GRP0
DATA GRP3
DATA GRP1
MISC
BGA479-SKT6-GPU7
Close to CPU
modify by RF
EMI capacitor
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Place these TP on button-side, easy to measure.
All place within 2" to CPU
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CPU (1 of 2)
JV71
-2
Thursday, July 02, 2009
Sheet 4 of 60



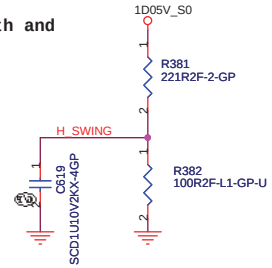

http://hobi-elektronika.net

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | CPU (2 of 2) | |
| Size | Document Number JV71 | Rev -2 |
| Date: Thursday, July 02, 2009 | Sheet 5 of 60 | |

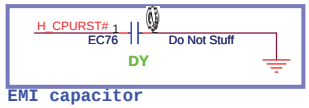
**H_SWING routing Trace width and Spacing use 10 / 20 mil**

**H_SWING Resistors and Capacitors close MCH 500 mil ( MAX )**

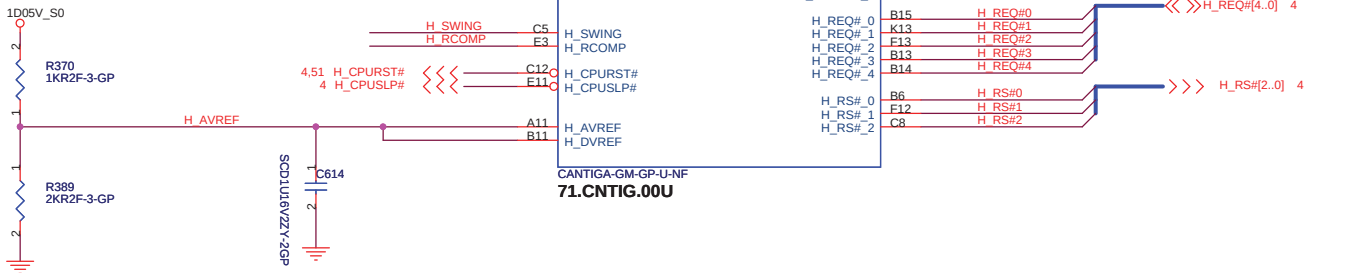



**H_RCOMP routing Trace width and Spacing use 10 / 20 mil**


**Place them near to the chip ( < 0.5")**




**EMI capacitor**

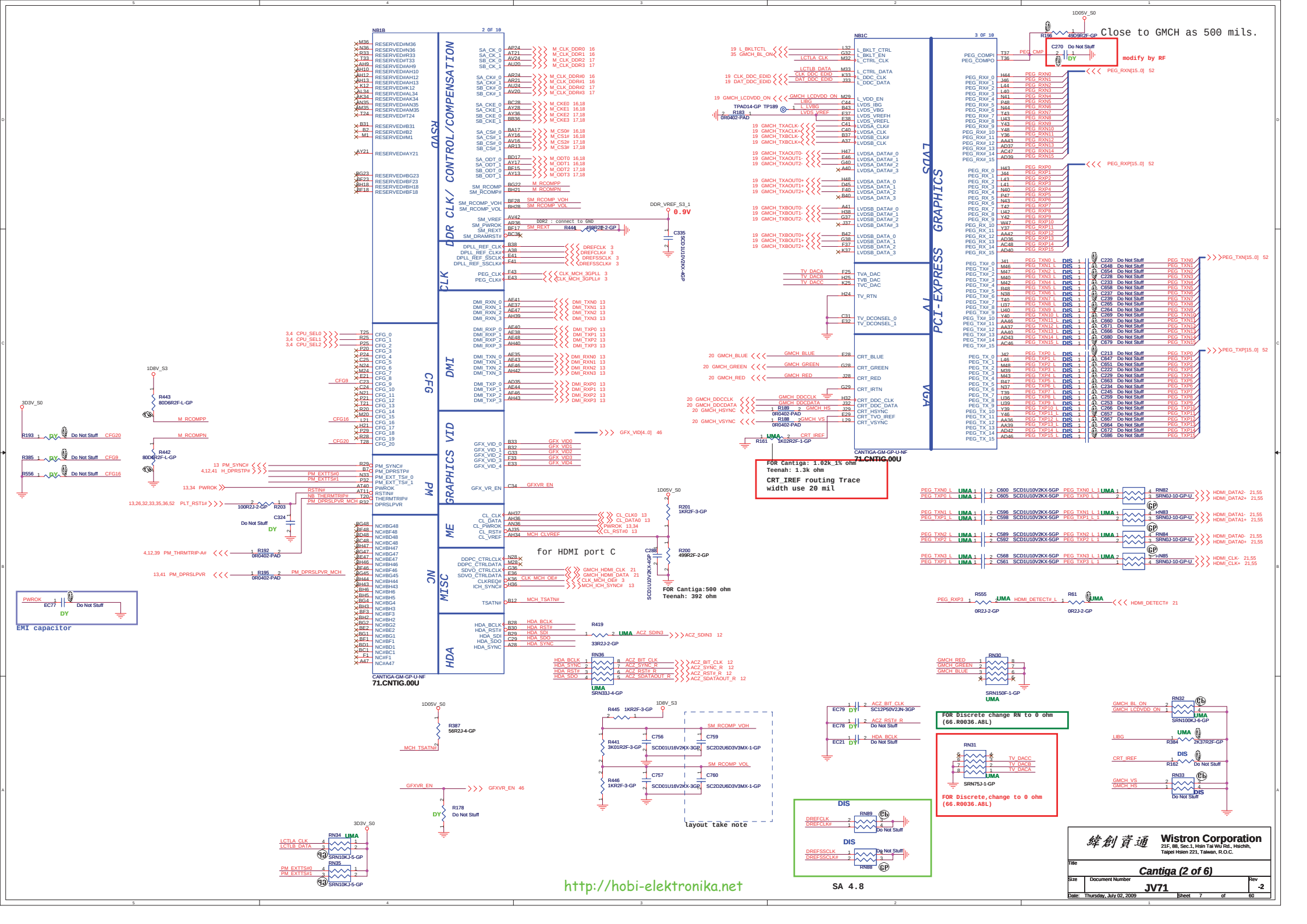


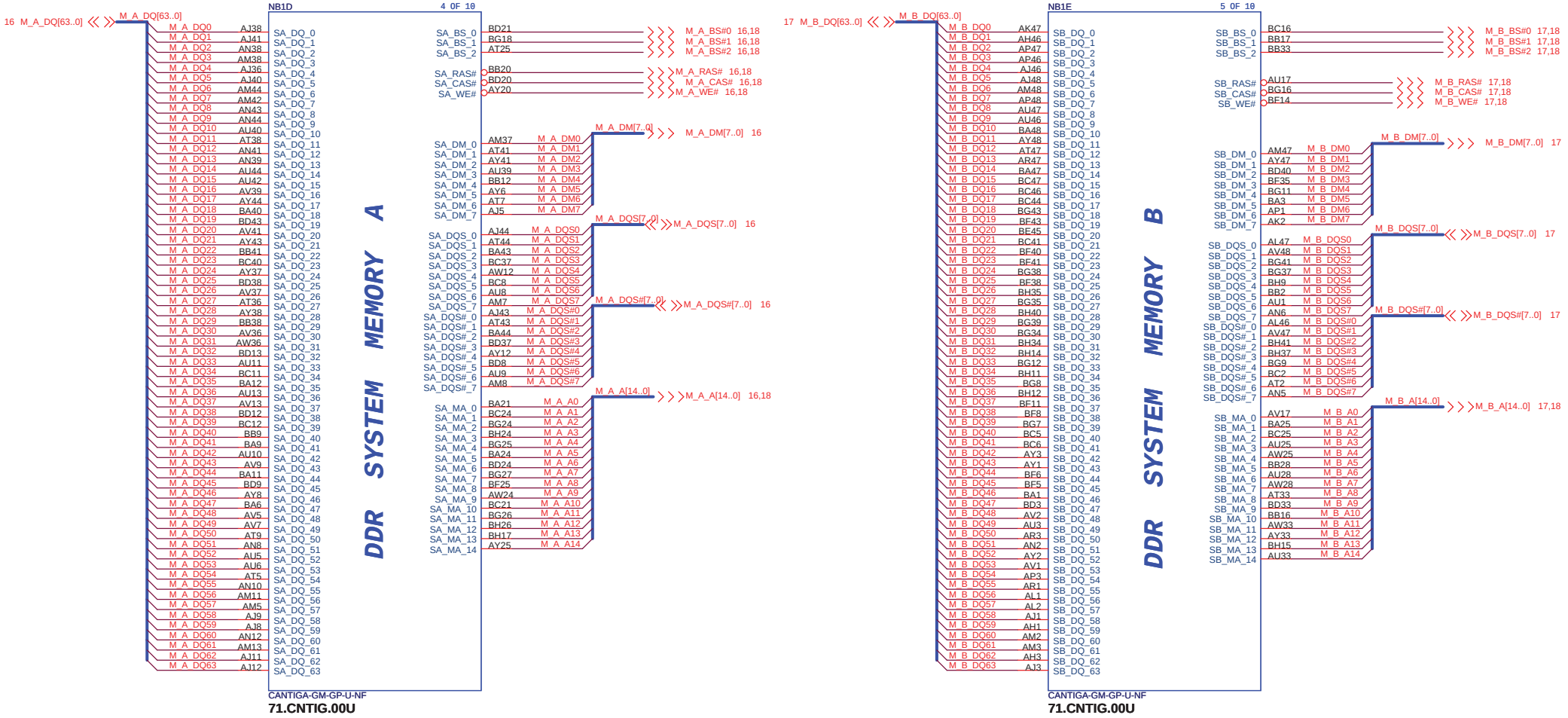



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | *Cantiga (1 of 6)* | |
| Size | Document Number: JV71 | Rev: -2 |
| Date: Thursday, July 02, 2009 | Sheet 6 of 60 | |


Close to GMCH as 500 mils.
modify by RF
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
for HDMI port C
FOR Cantiga:500 ohm
Teenah: 392 ohm
EMI capacitor
layout take note
FOR Discrete change RN to 0 ohm (66.R0036.A8L)
FOR Discrete,change to 0 ohm (66.R0036.A8L)
http://hobi-elektronika.net
SA 4.8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Cantiga (2 of 6)
JV71
-2
Thursday, July 02, 2009



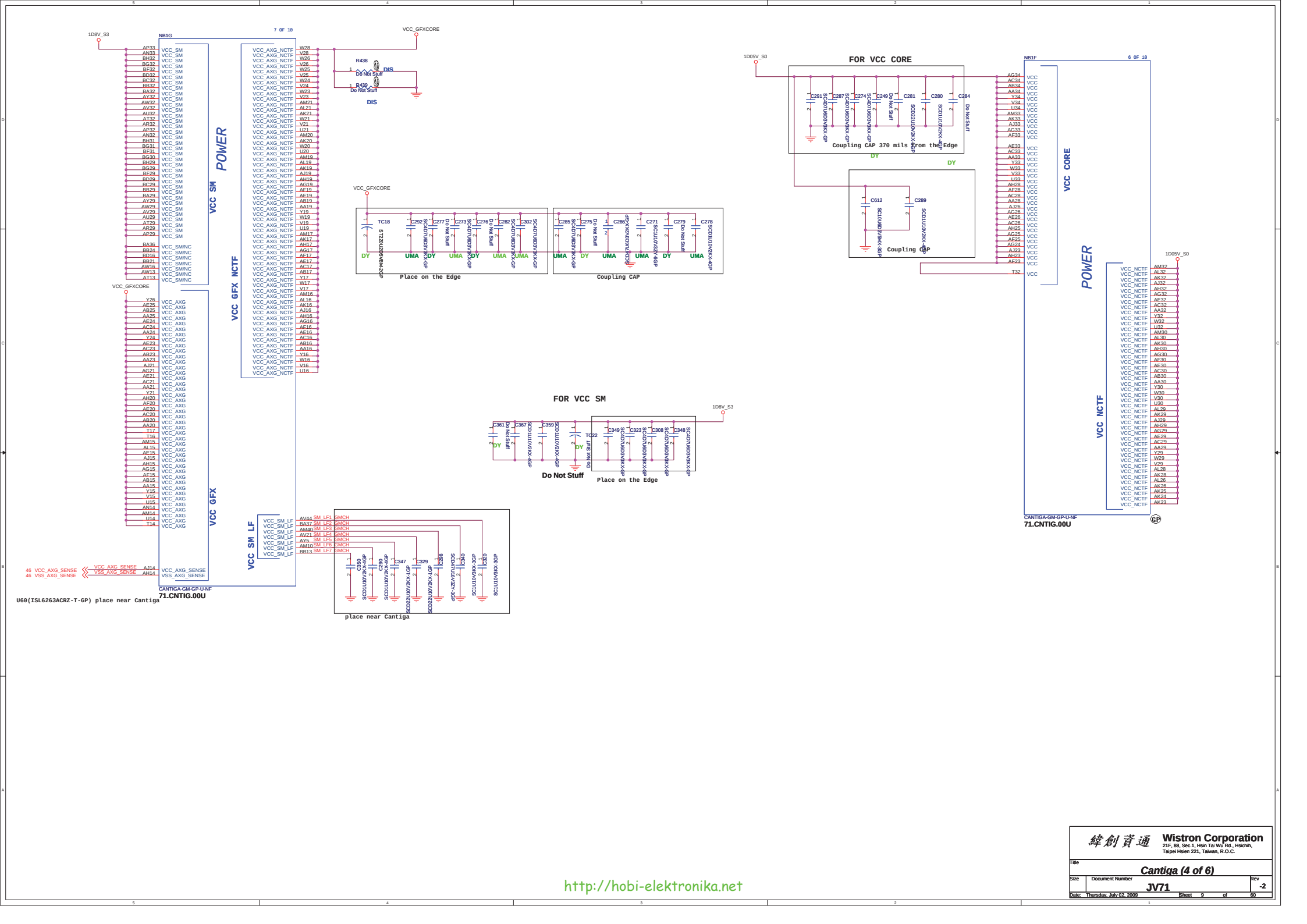



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Cantiga (3 of 6)***

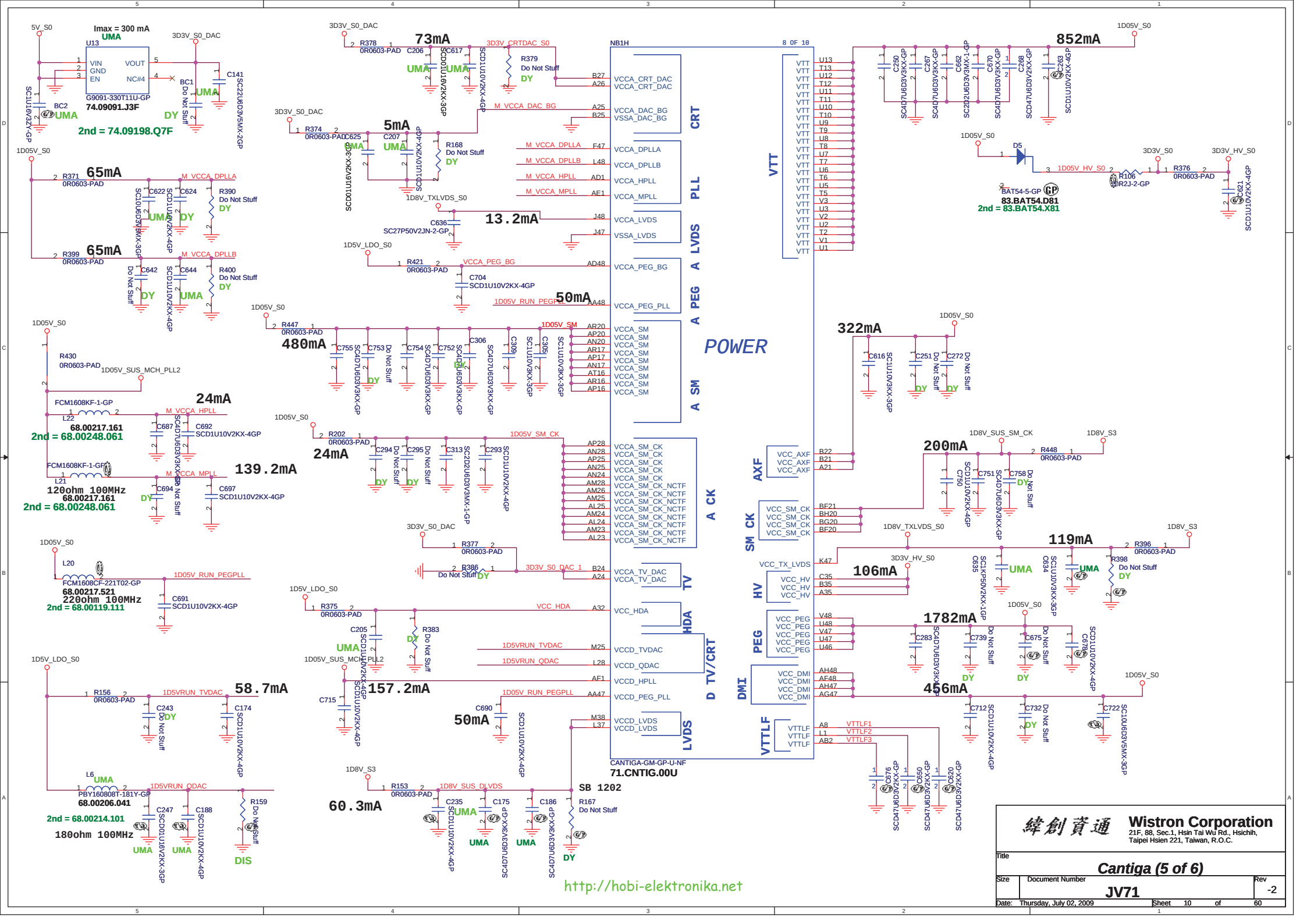
| Size | Document Number | Rev |
|---|---|---|
| | JV71 | -2 |

Date: Thursday, July 02, 2009 Sheet 8 of 60



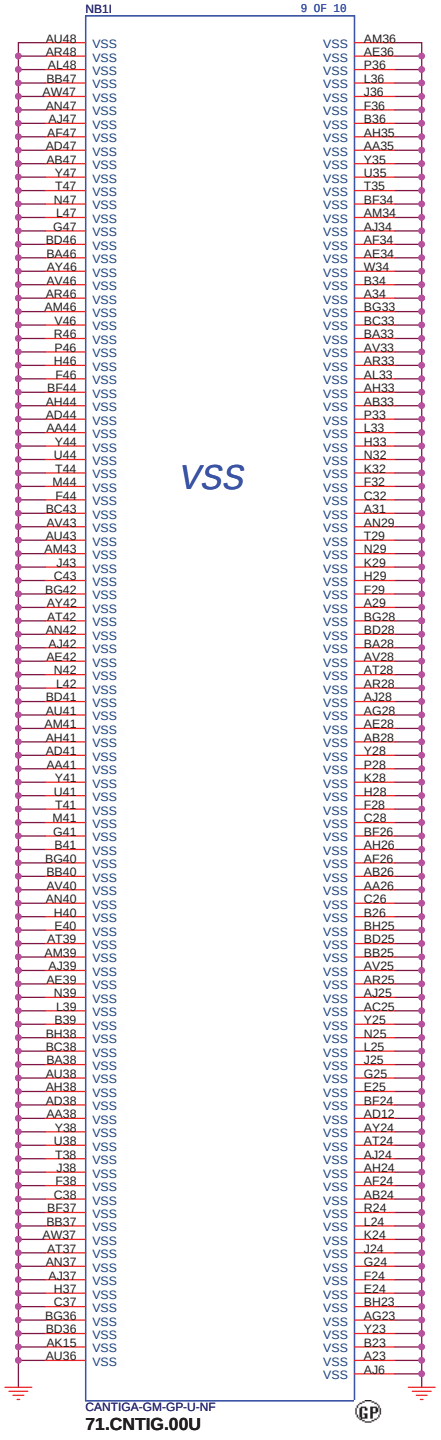


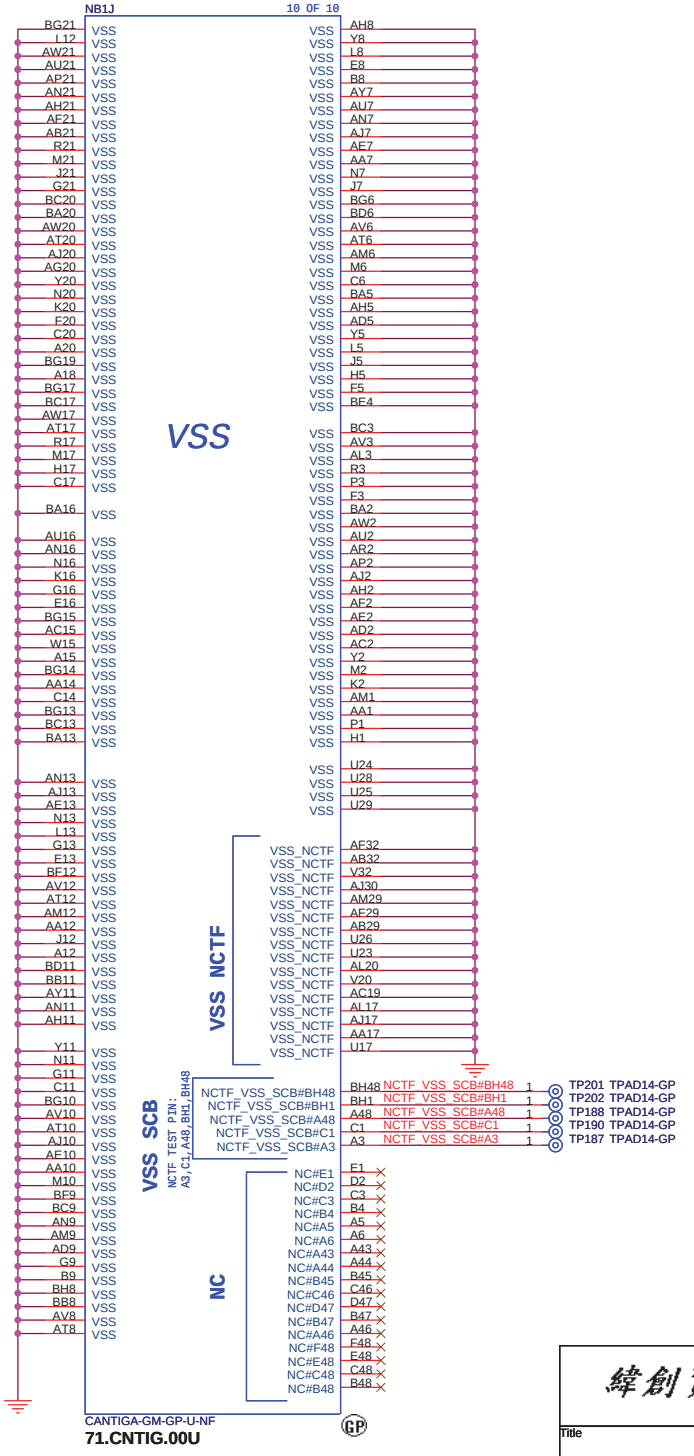

| | | |
|---|---|---|
| 緯創資通 | Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | Cantiga (4 of 6) | |
| Size | Document Number: JV71 | Rev: -2 |
| Date: Thursday, July 02, 2009 | Sheet 9 of 60 | |




緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | Cantiga (5 of 6) | |
| Size | Document Number JV71 | Rev -2 |
| Date: Thursday, July 02, 2009 | Sheet 10 of 60 | |

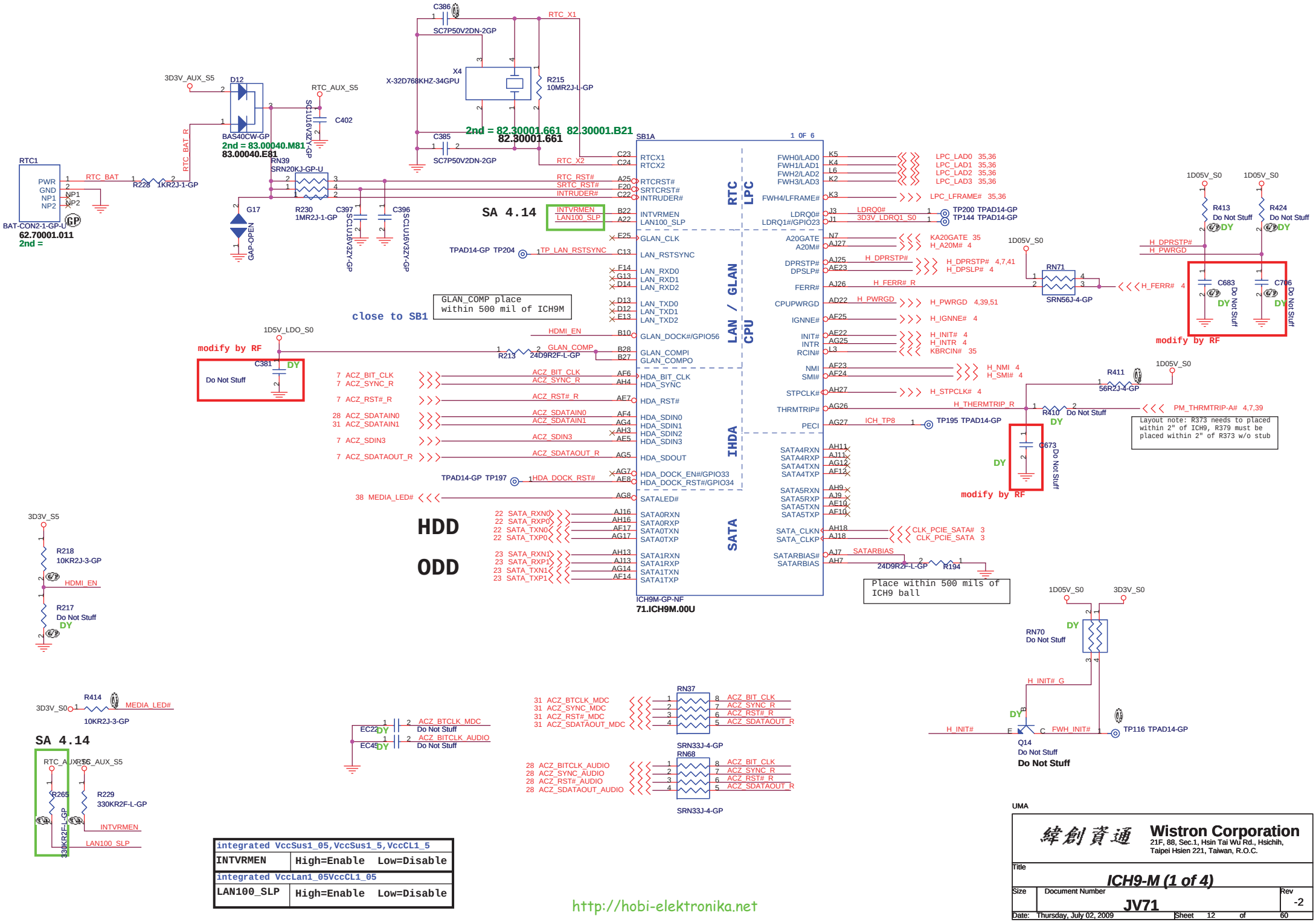





緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | *Cantiga (6 of 6)* | |
| Size | Document Number: JV71 | Rev: -2 |
| Date: Thursday, July 02, 2009 | Sheet 11 of 60 | |


SB1A
1 0F 6
ICH9M-GP-NF
71.ICH9M.00U
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
HDD
ODD
SA 4.14
close to SB1
GLAN_COMP place within 500 mil of ICH9M
modify by RF
Do Not Stuff
Place within 500 mils of ICH9 ball
Layout note: R373 needs to placed within 2" of R373 w/o stub
2nd = 82.30001.661 82.30001.B21
82.30001.661
2nd = 83.00040.M81
83.00040.E81
62.70001.011
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (1 of 4)
JV71
Thursday, July 02, 2009

PCI_GNT#0 and SPI_CS1#
have weak internal Pull up

GPIO049 should be pulled down to
GND only when using Teenah. When
using Cantiga, this ball should
be left as No Connect.

These R need close SB
within 600 mils

SA 4.14

SA 4.14

SA 4.14

| USB | |
|---|---|
| Pair | Device |
| 0 | USB2 |
| 1 | USB3 |
| 2 | USB4 |
| 3 | MINI1 |
| 4 | CCD |
| 5 | NC |
| 6 | Finger Print |
| 7 | Blue Tooth |
| 8 | NC |
| 9 | USB1 |
| 10 | NC |
| 11 | Cardreader |

| No Reboot Strap | |
|---|---|
| SPKR | LOW = Defaule<br>High=No Reboot |

| BOOT BIOS Strap | | |
|---|---|---|
| PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location |
| 0 | 1 | SPI |
| 1 | 0 | PCI |
| 1 | 1 | LPC(Default) |

| A16 swap override strap | |
|---|---|
| PCI_GNT#3 | low = A16 swap override enable<br>high = default |

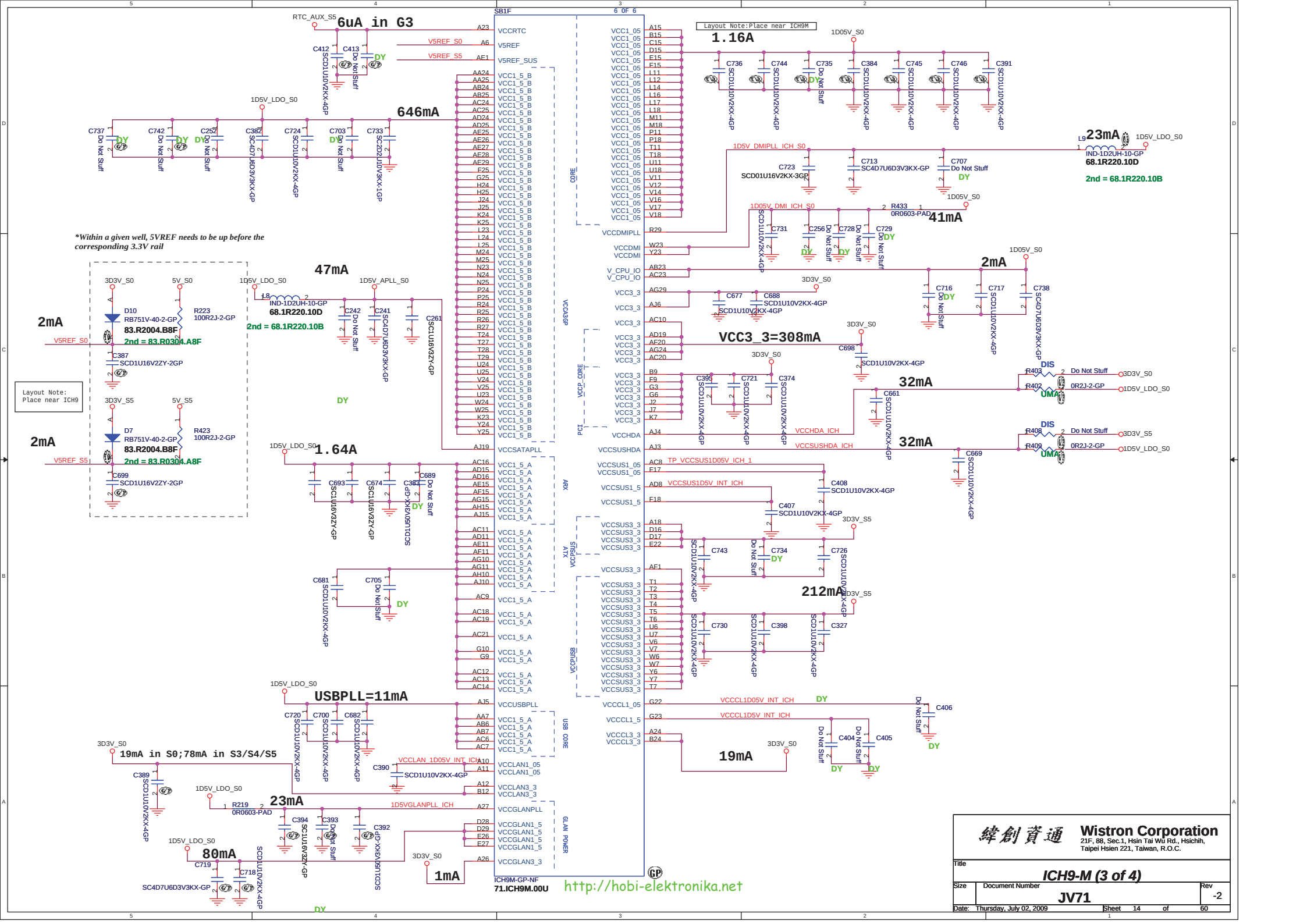
UMA

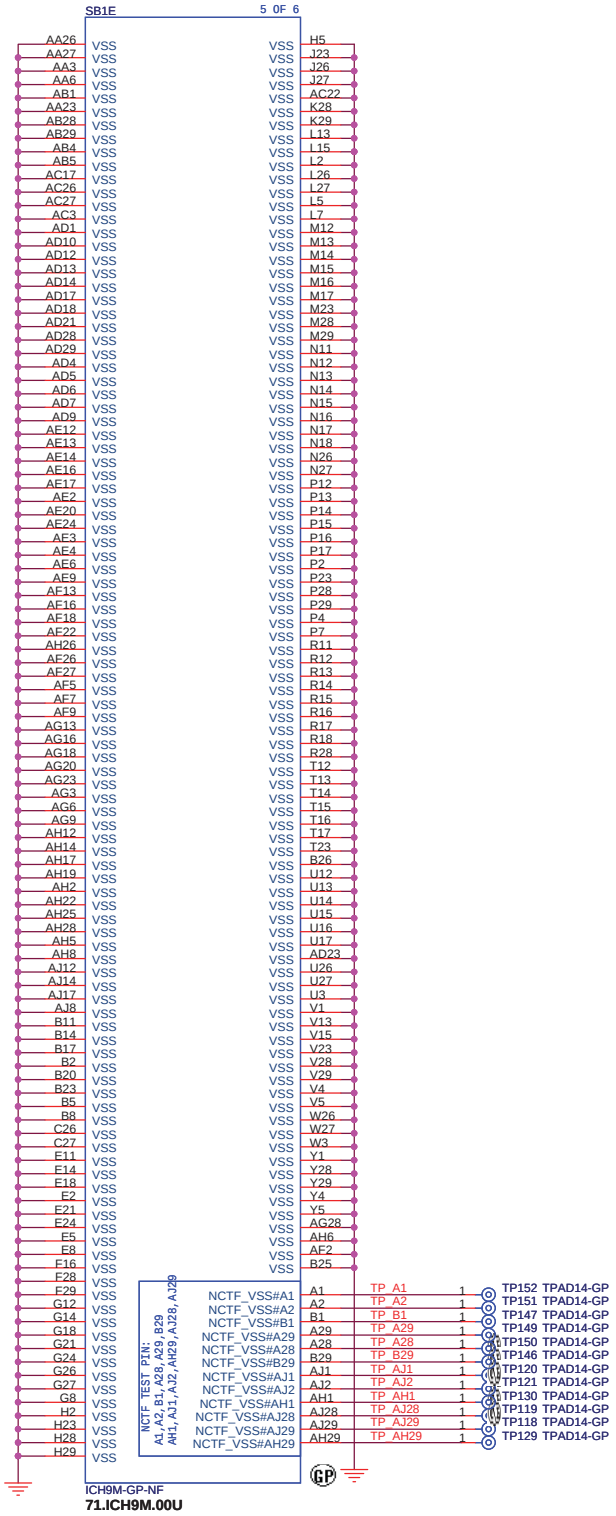
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

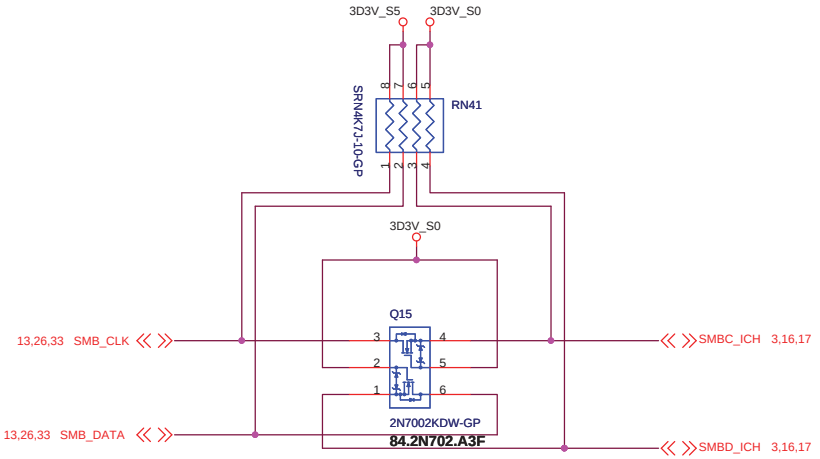
Title: ICH9-M (2 of 4)

Size | Document Number: JV71 | Rev: -2

Date: Thursday, July 02, 2009 | Sheet 13 of 60


SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
RTC_AUX_S5
6uA in G3
V5REF_S0
V5REF_S5
1D5V_LDO_S0
646mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
47mA
1D5V_APLL_S0
IND-1D2UH-10-GP
68.1R220.10D
2nd = 68.1R220.10B
3D3V_S0
5V_S0
2mA
D10
RB751V-40-2-GP
83.R2004.B8F
2nd = 83.R0304.A8F
R223
100R2J-2-GP
C387
SCD1U16V2ZY-2GP
Layout Note:
Place near ICH9
3D3V_S5
5V_S5
D7
R423
C699
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
VCCLAN_1D05V_INT_ICH
23mA
1D5VGLANPLL_ICH
R219
0R0603-PAD
80mA
1mA
SC4D7U6D3V3KX-GP
Layout Note:Place near ICH9M
1.16A
C736
C744
C735
C384
C745
C746
C391
SCD1U10V2KX-4GP
Do Not Stuff
1D5V_DMIPLL_ICH_S0
C723
SCD01U16V2KX-3GP
C713
SC4D7U6D3V3KX-GP
C707
1D5V_DMI_ICH_S0
R433
0R0603-PAD
41mA
C731
C256
C728
C729
SCD1U10V2KX-4GP
2mA
C716
C717
C738
SC4D7U6D3V3KX-GP
VCC3_3=308mA
C698
C677
C688
C395
C721
C374
C661
32mA
DIS
UMA
R403
R402
R408
R409
0R2J-2-GP
C669
C408
C407
212mA
C743
C734
C726
C730
C398
C327
C406
C404
C405
19mA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (3 of 4)
Size
Document Number
JV71
Rev
-2
Date: Thursday, July 02, 2009
Sheet 14 of 60
http://hobi-elektronika.net



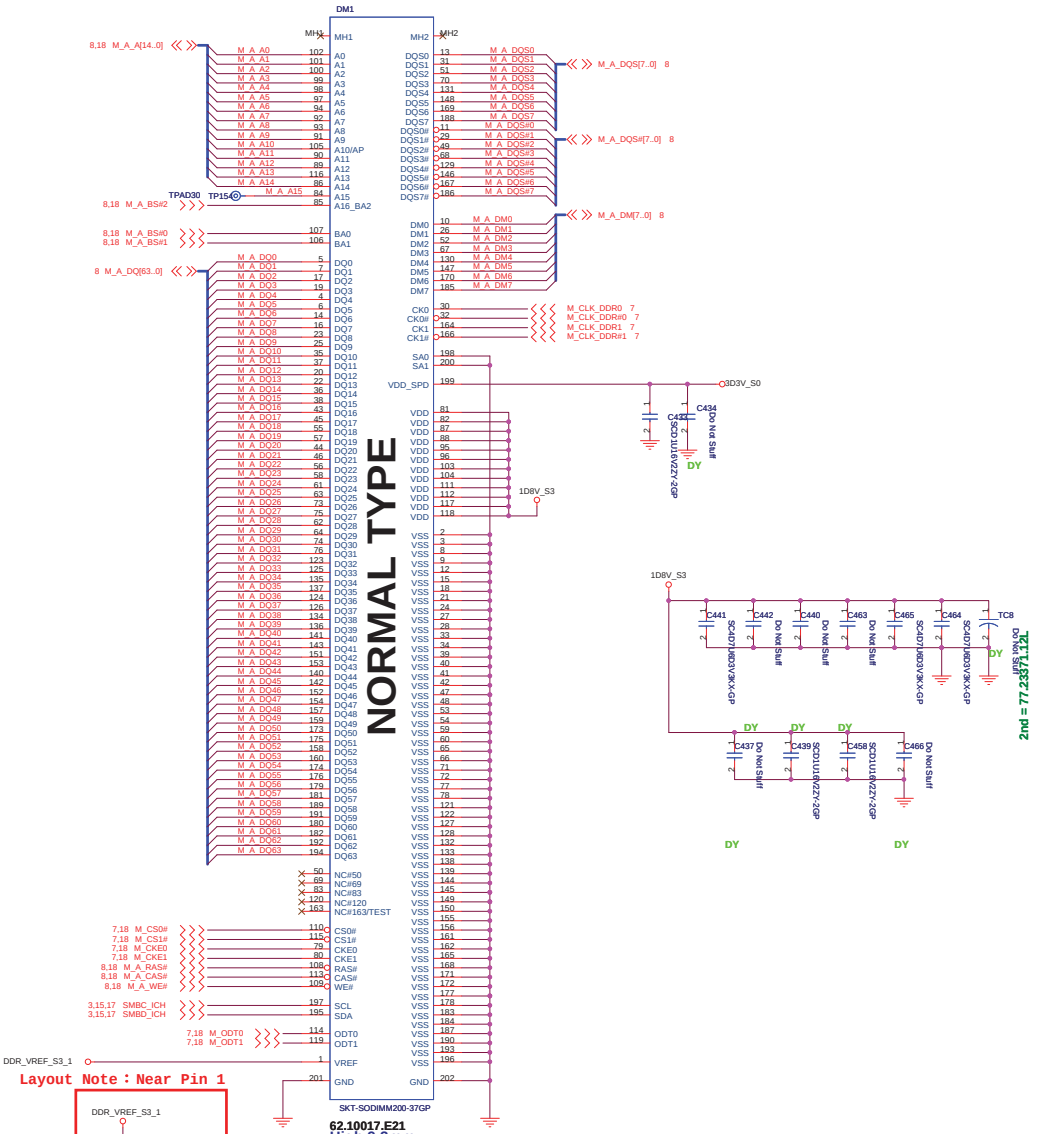

## SMBUS



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | *ICH9-M (4 of 4)* | |
| Size | Document Number: JV71 | Rev: -2 |
| Date: Thursday, July 02, 2009 | Sheet 15 of 60 | |

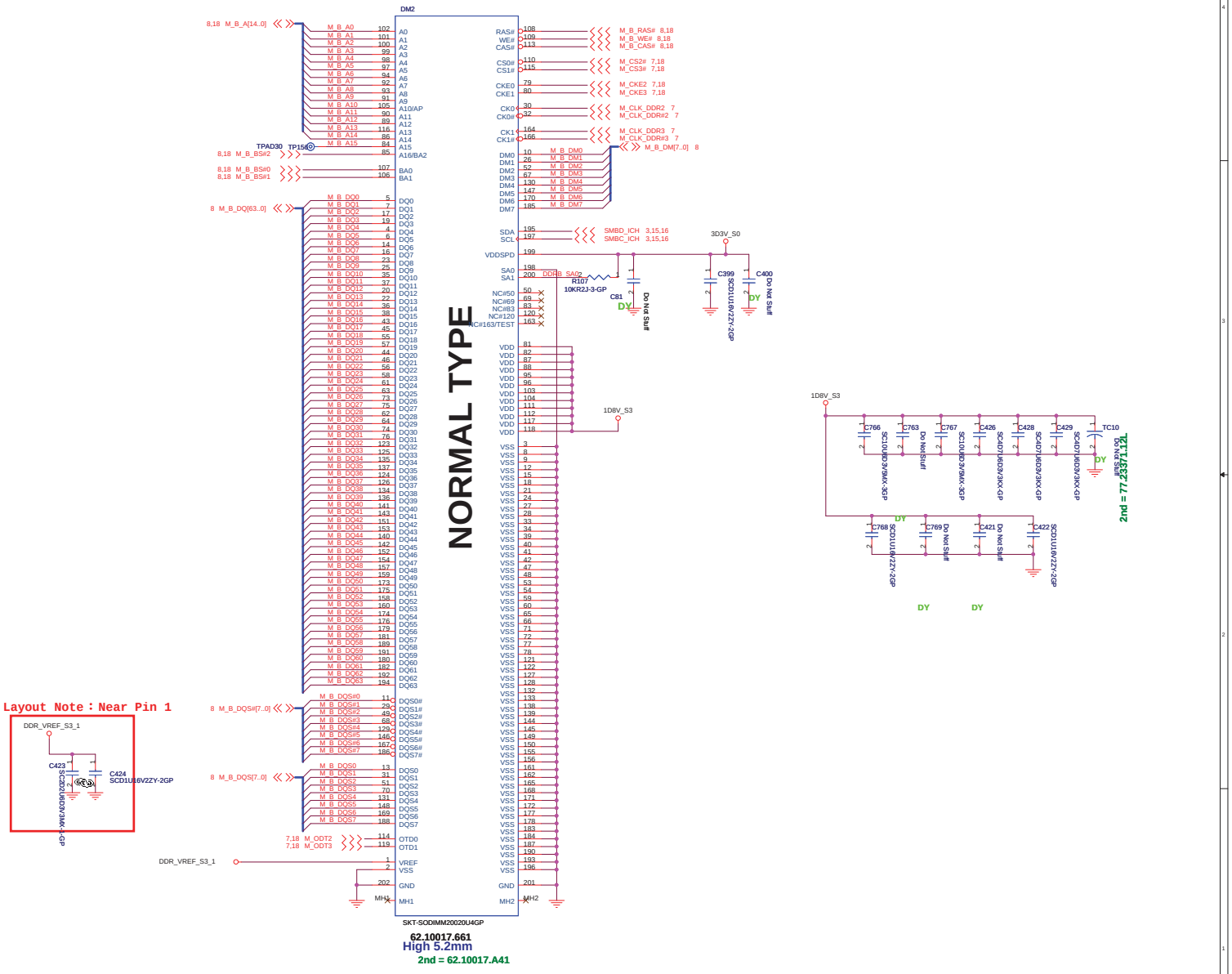
# DDR2 SOCKET_1






| | | |
|---|---|---|
| 緯創資通 Wistron Corporation | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: DDR3 Socket | | |
| Size | Document Number: JV71 | Rev: -2 |
| Date: Thursday, July 02, 2009 | Sheet 16 of 60 | |

# DDR2 SOCKET_2

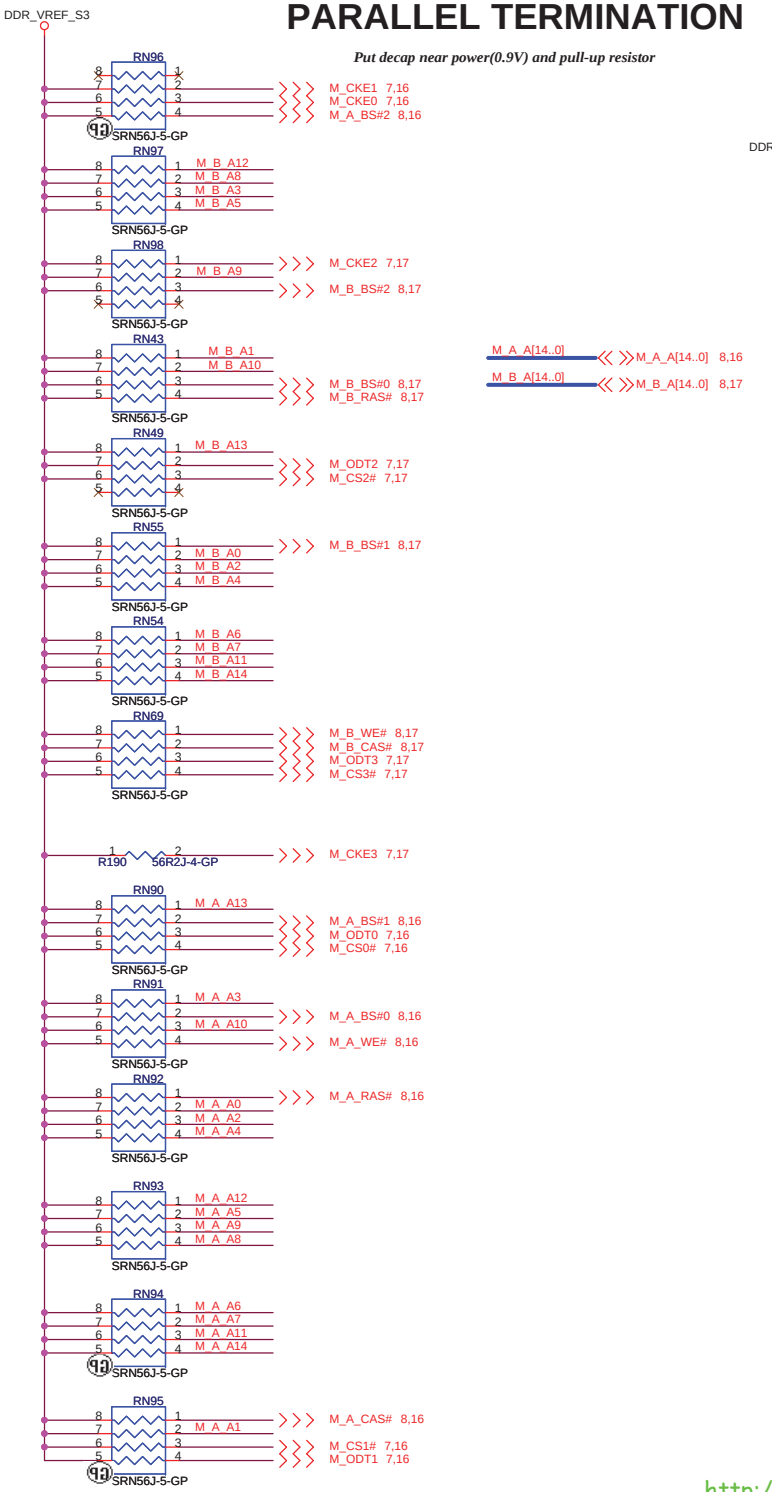





| | | |
|---|---|---|
| 緯創資通 | Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title: DDR3 Socket2 | | |
| Size | Document Number: JV71 | Rev: -2 |
| Date: Thursday, July 02, 2009 | Sheet 17 of 60 | |

# PARALLEL TERMINATION

*Put decap near power(0.9V) and pull-up resistor*

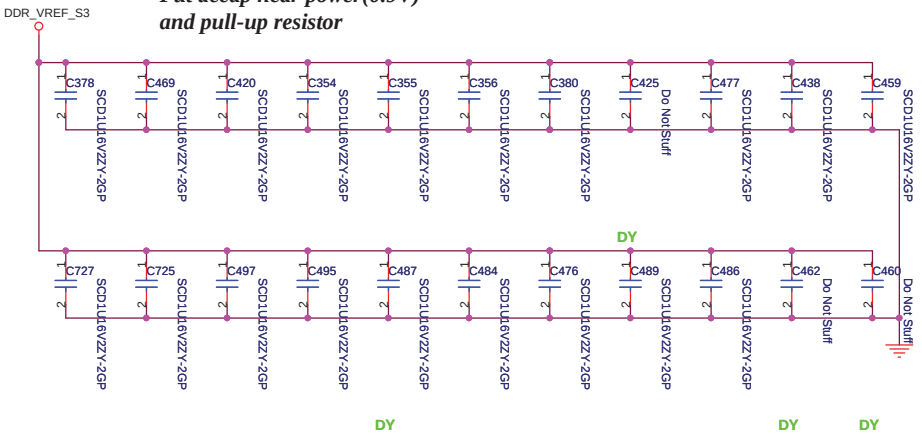






# Decoupling Capacitor

*Put decap near power(0.9V) and pull-up resistor*






UMA

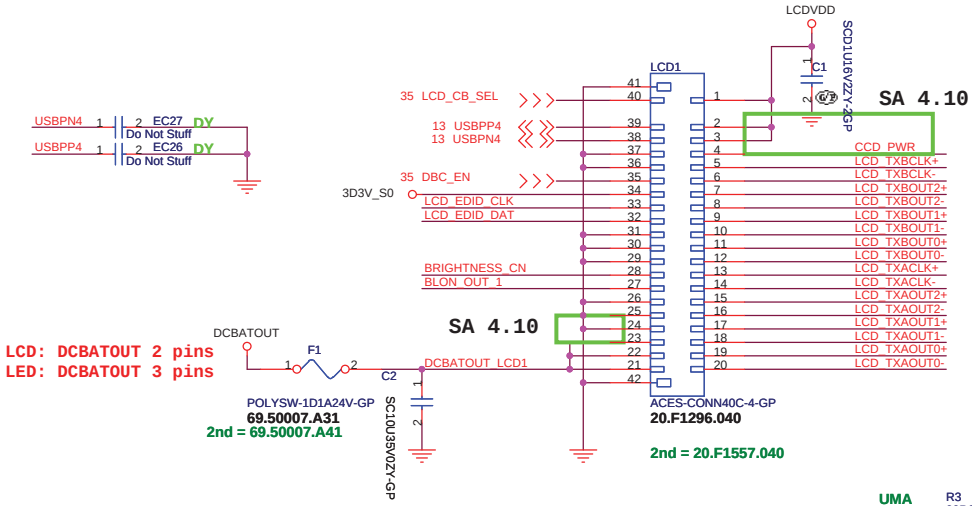
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

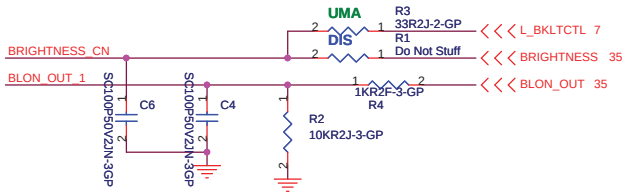
Title: ***DDR 2 Termination Resistor***

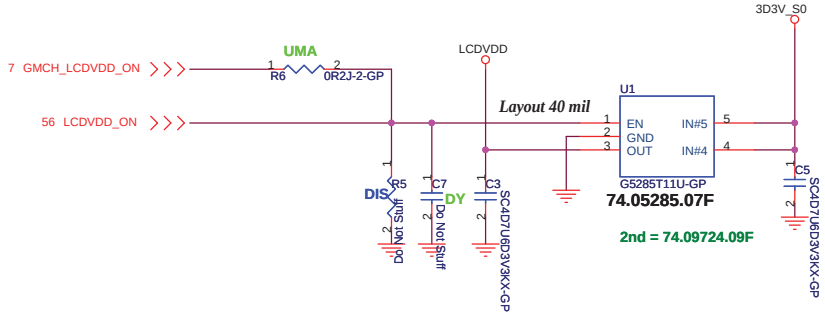
| Size | Document Number | Rev |
|---|---|---|
| | JV71 | -2 |

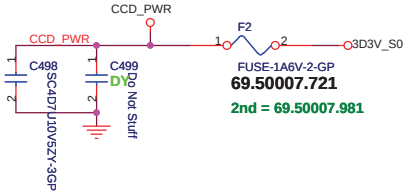
Date: Thursday, July 02, 2009 Sheet 18 of 60

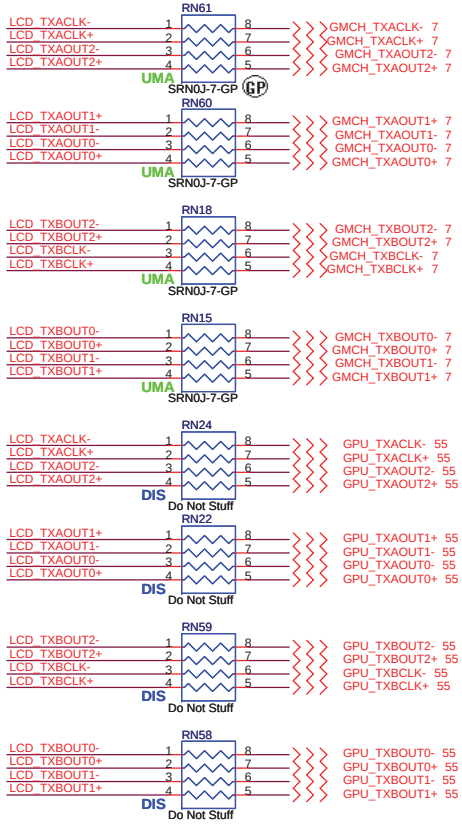
# LCD/INVERTER/CCD CONN

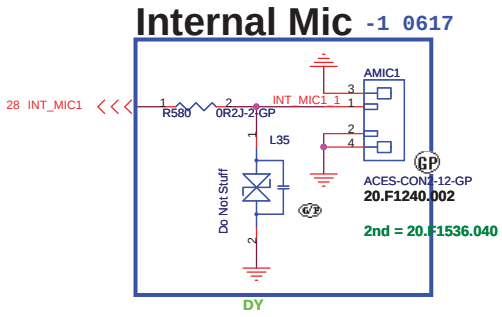


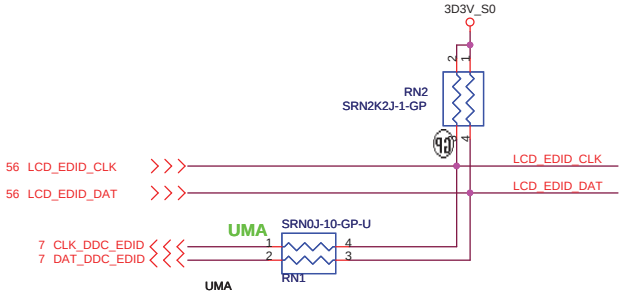



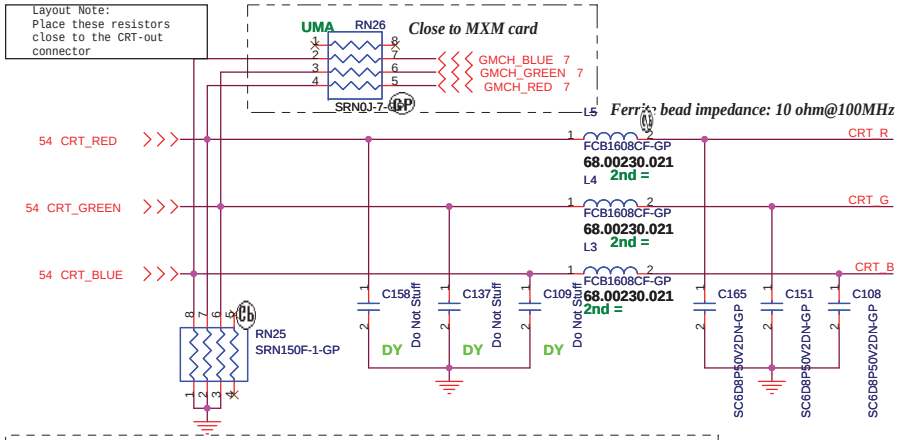




UMA

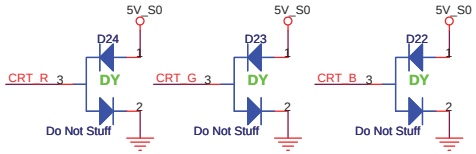
http://hobi-elektronika.net

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

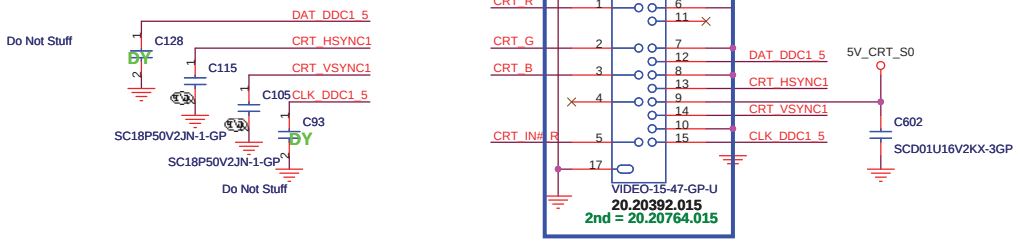
| | | |
|---|---|---|
| Title | LCD CONN | |
| Size | Document Number JV71 | Rev -2 |
| Date: Thursday, July 02, 2009 | Sheet 19 of 60 | |

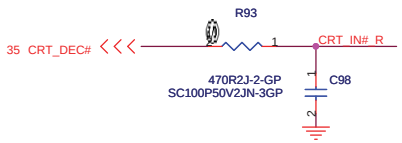


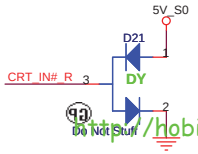

***Layout Note:***
**** Must be a ground return path between this ground and the ground on the VGA connector.***
***Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.***



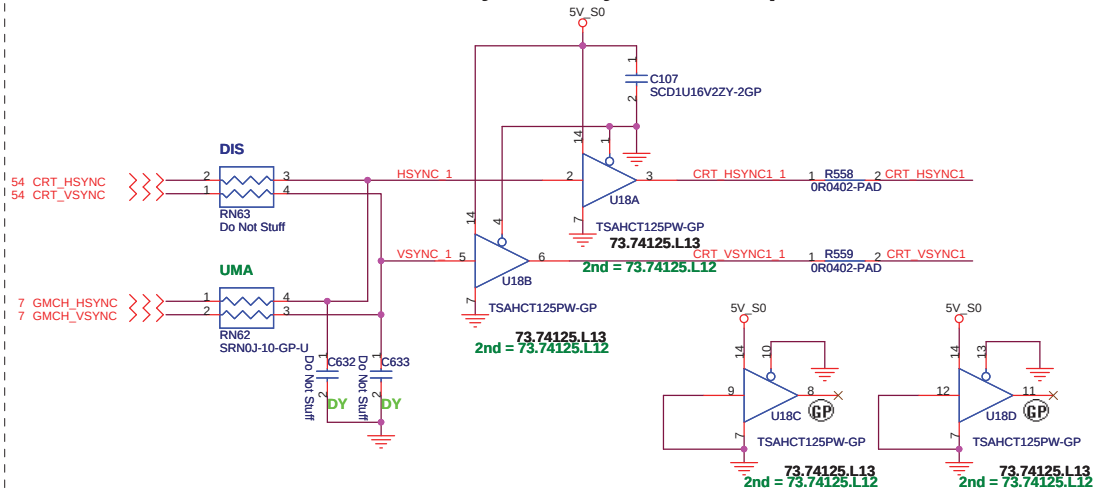

# CRT I/F & CONNECTOR



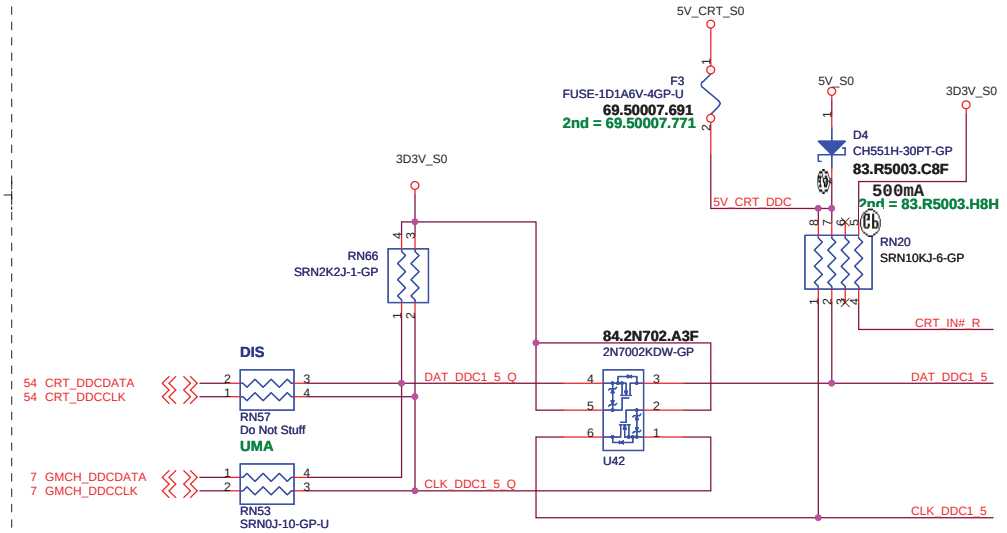




## Hsync & Vsync level shift




## DDC_CLK & DATA level shift



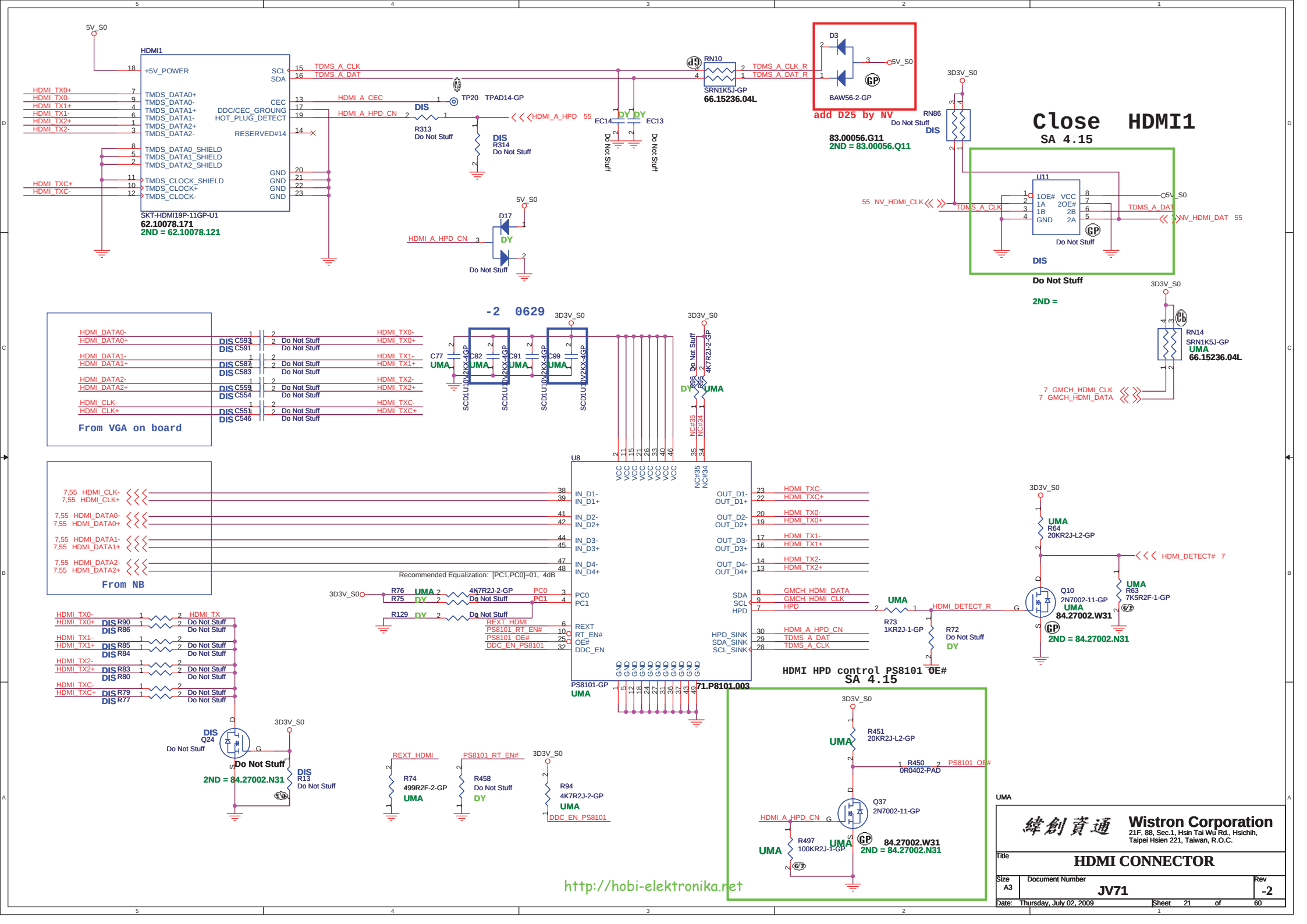



UMA

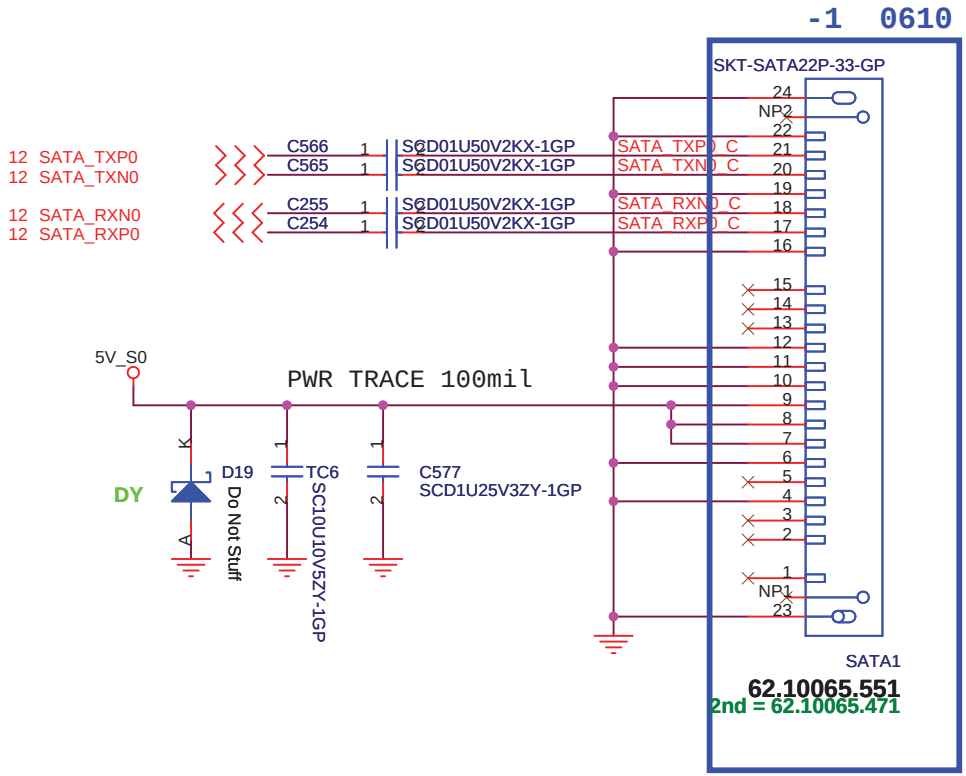
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | **CRT CONN** | |
| Size | Document Number **JV71** | Rev -2 |
| Date: Thursday, July 02, 2009 | Sheet 20 of 60 | |

6 1 7 2 8 3 9 4 10 5


HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
2ND = 62.10078.121
TP20 TPAD14-GP
RN10
SRN1K5J-GP
66.15236.04L
D3
BAW56-2-GP
add D25 by NV
83.00056.G11
2ND = 83.00056.Q11
RN86
Do Not Stuff
DIS
Close HDMI1
SA 4.15
U11
Do Not Stuff
DIS
Do Not Stuff
2ND =
RN14
SRN1K5J-GP
UMA
66.15236.04L
-2 0629
From VGA on board
From NB
U8
PS8101-GP
UMA
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
HDMI HPD control PS8101 OE#
SA 4.15
Q24
Do Not Stuff
2ND = 84.27002.N31
Q10
2N7002-11-GP
UMA
84.27002.W31
2ND = 84.27002.N31
Q37
2N7002-11-GP
UMA
84.27002.W31
2ND = 84.27002.N31
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI CONNECTOR
Size A3
Document Number JV71
Rev -2
Date: Thursday, July 02, 2009
Sheet 21 of 60

# SATA Connector



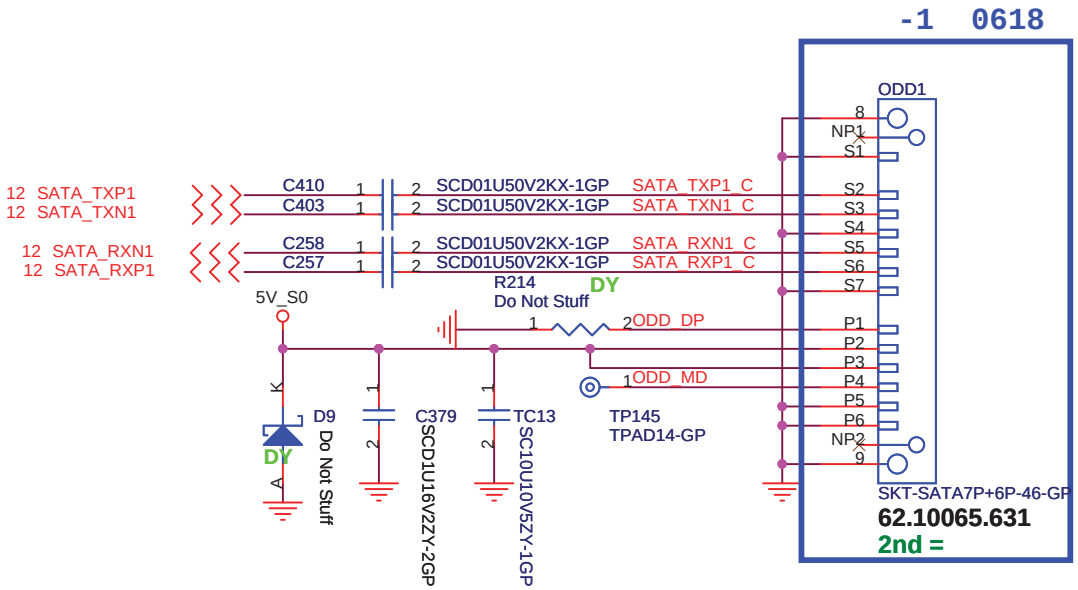



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | ***HDD CONN*** | |
| Size | Document Number **JV71** | Rev -2 |
| Date: Thursday, July 02, 2009 | Sheet 22 of 60 | |

# ODD Connector



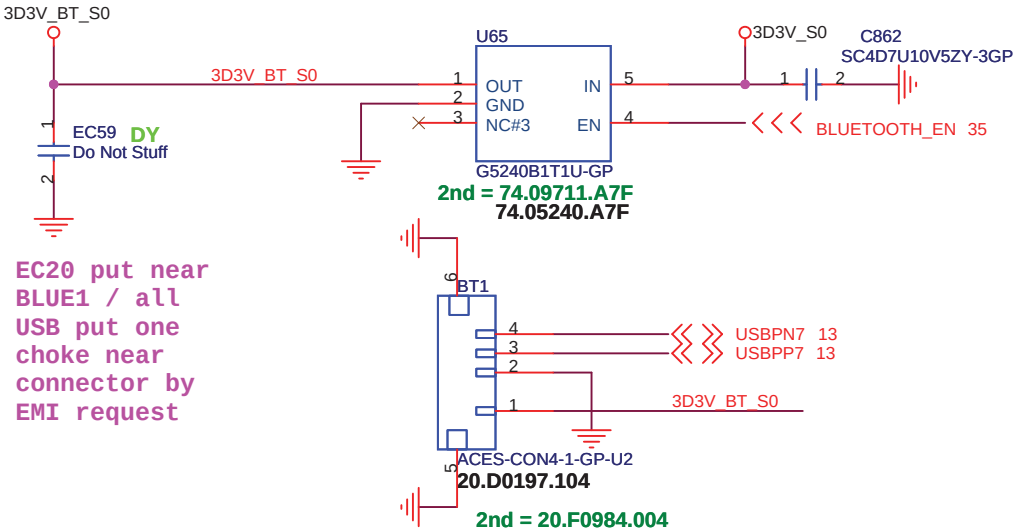

http://hobi-elektronika.net

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title: ODD | | |
| Size | Document Number: JV71 | Rev: -2 |
| Date: Thursday, July 02, 2009 | Sheet 23 of 60 | |

# BLUETOOTH MODULE

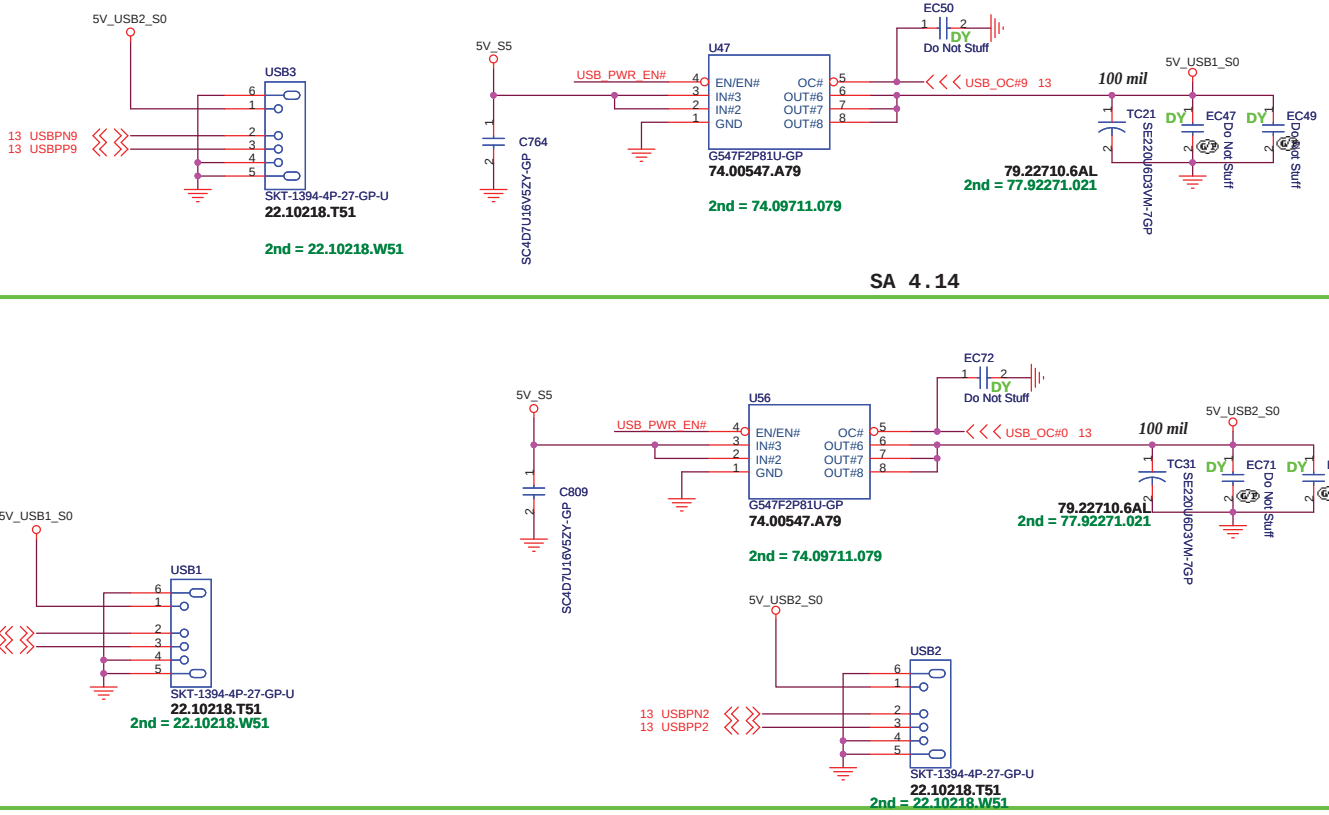





UMA

**Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title: BLUETOOTH | | |
| Size | Document Number: JV71 | Rev: -2 |
| Date: Thursday, July 02, 2009 | Sheet 24 of 60 | |

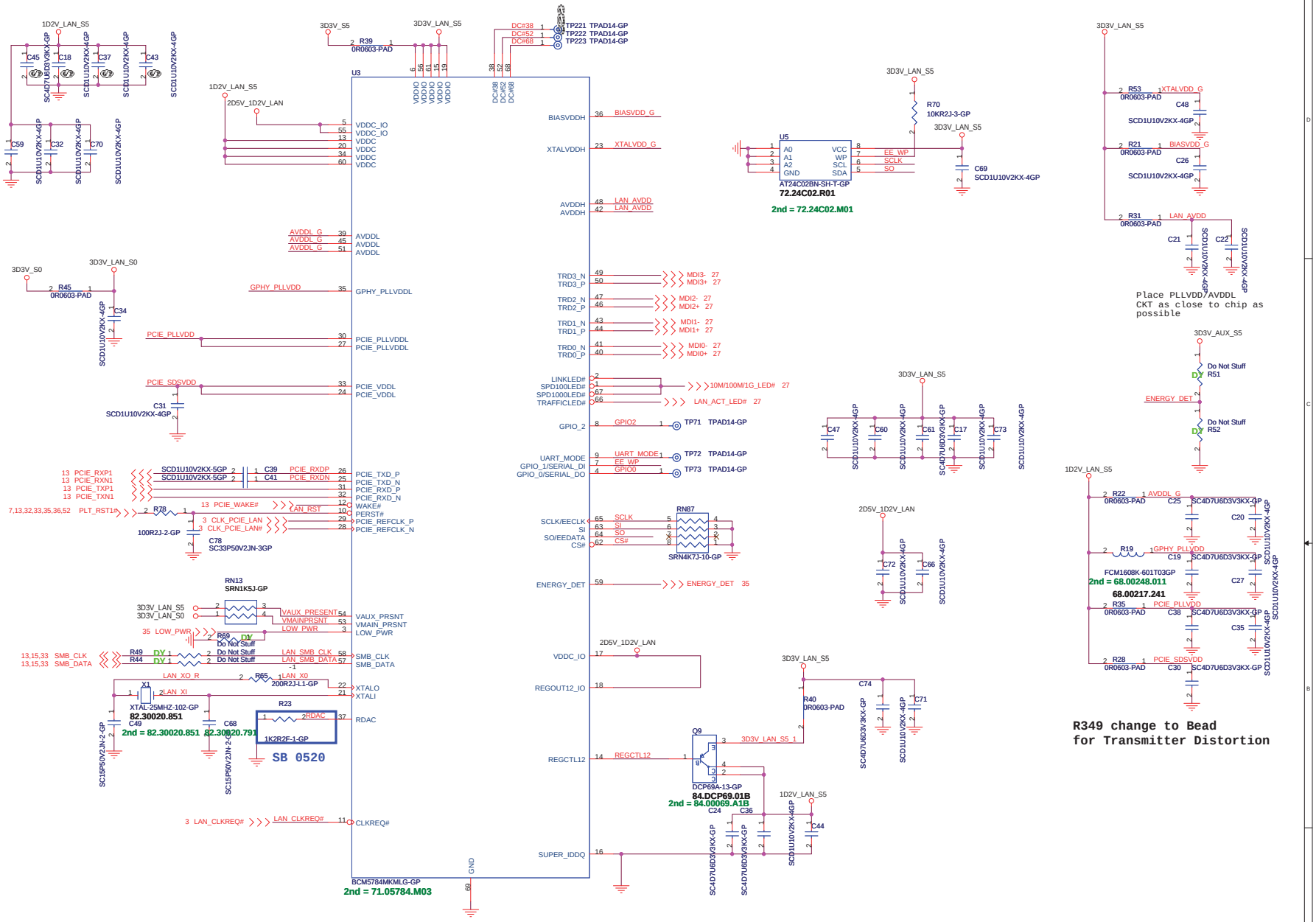



http://hobi-elektronika.net

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | *USB CONN* | |
| Size | Document Number JV71 | Rev -2 |
| Date: Thursday, July 02, 2009 | Sheet 25 of 60 | |




UMA

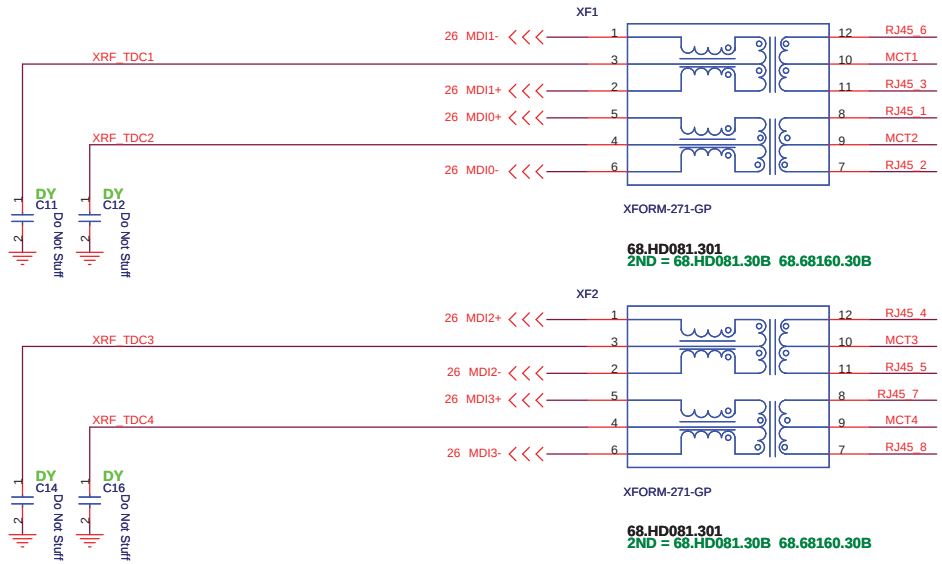
| | | |
|---|---|---|
| 緯創資通 | **Wistron Corporation**<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | ***BCM5764*** | |
| Size<br>Custom | Document Number<br>**JV71** | Rev<br>**-2** |
| Date: Thursday, July 02, 2009 | Sheet 26 of 60 | |

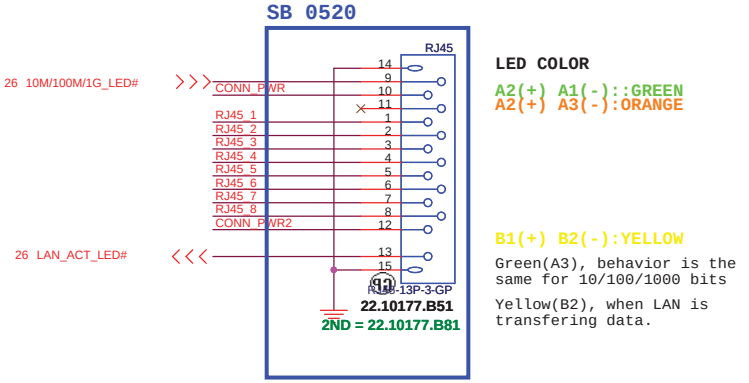
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

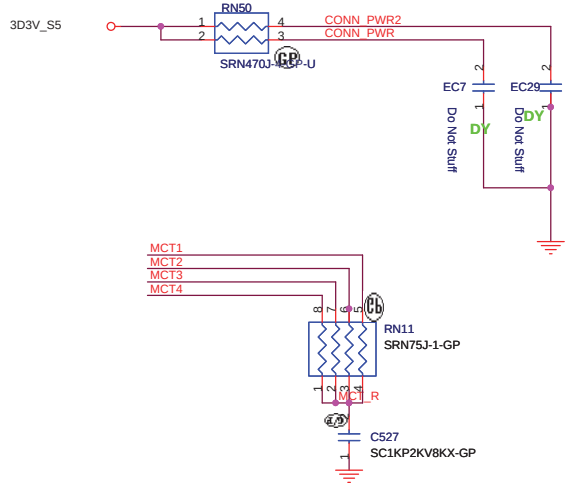
# LAN Connector

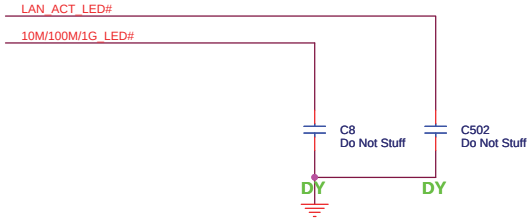
LAN Connector

*GIGA Lan Transformer*



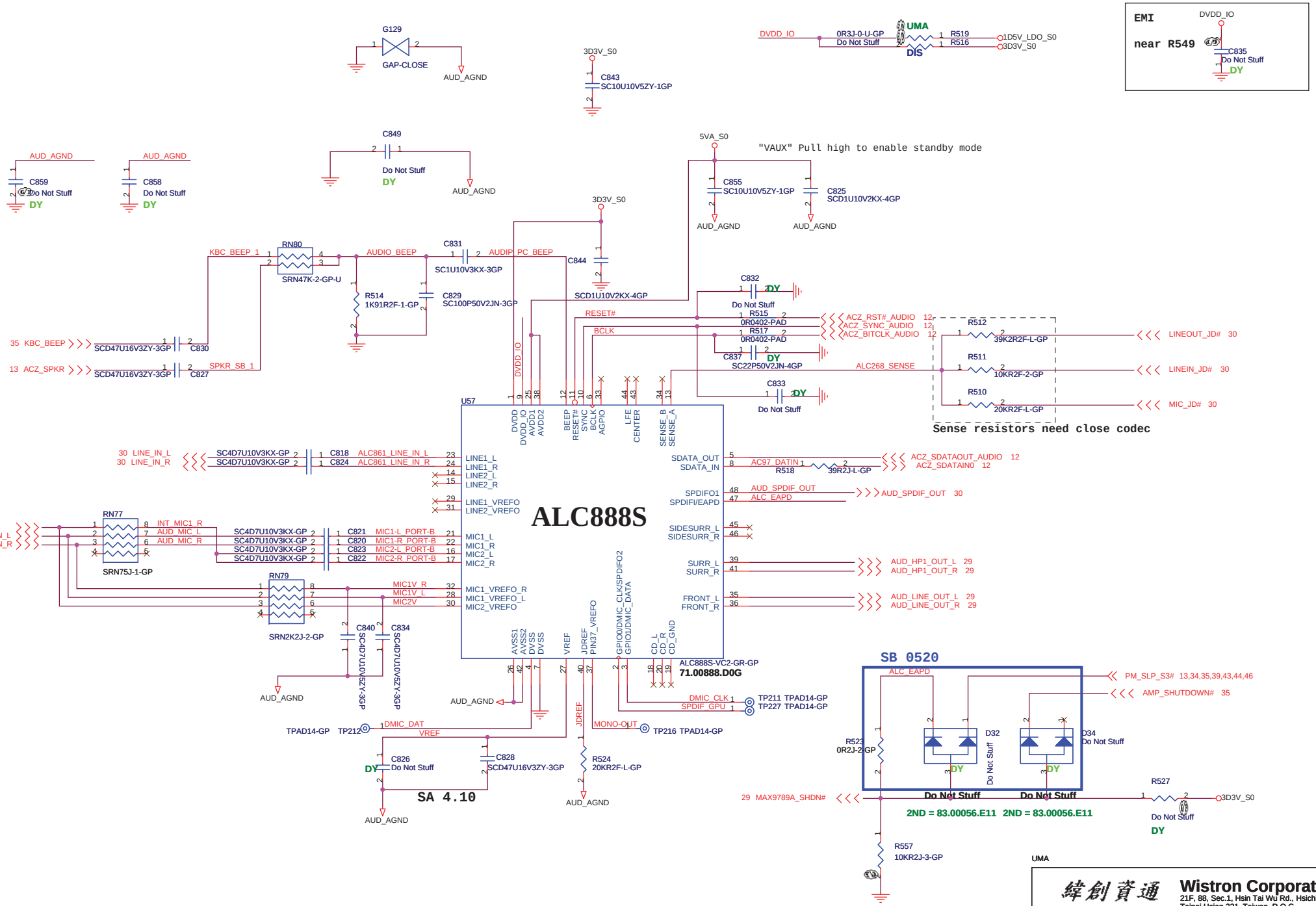



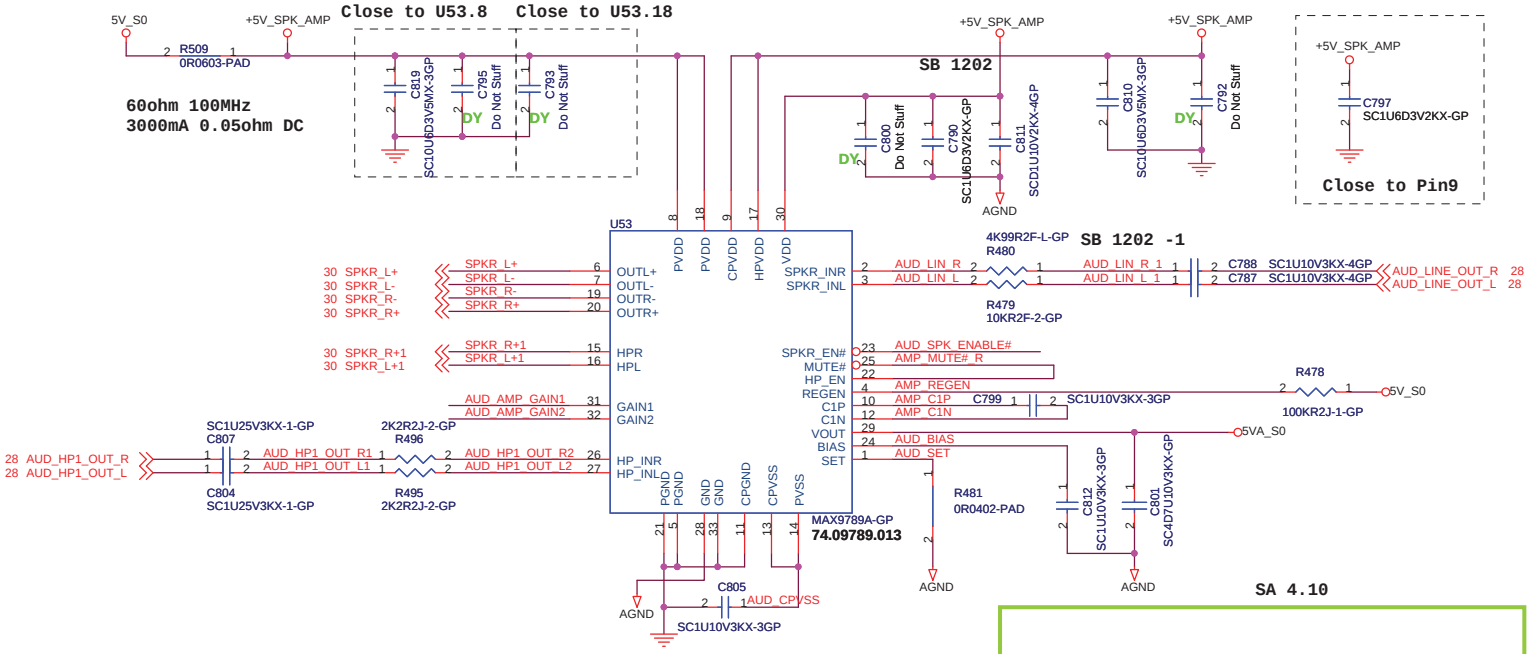



UMA

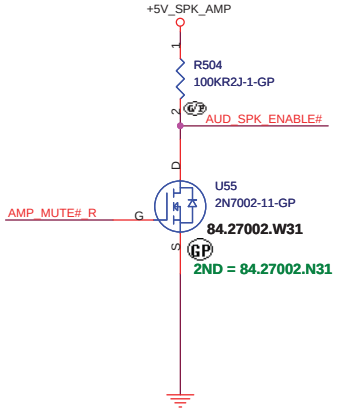
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | LAN CONN | |
| Size A3 | Document Number JV71 | Rev -2 |
| Date: Thursday, July 02, 2009 | Sheet 27 of 60 | |

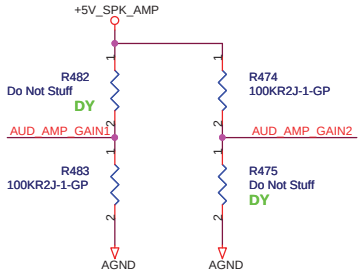




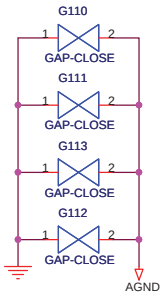

## Signal inverter for speaker shutdown




## GAIN SETTING




| GAIN1 | GAIN2 | GAIN |
|---|---|---|
| 0 | 0 | 6dB |
| 0 | 1 | 10dB |
| 1 | 0 | 15.6dB |
| 1 | 1 | 21.6dB |



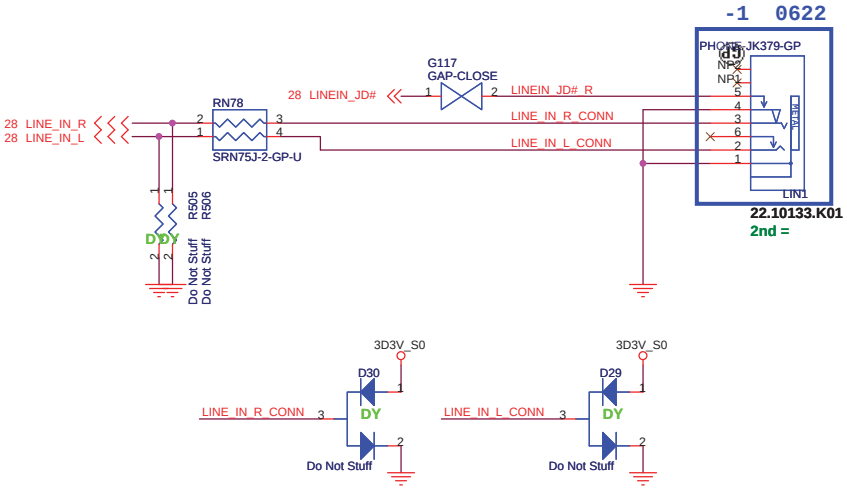



UMA

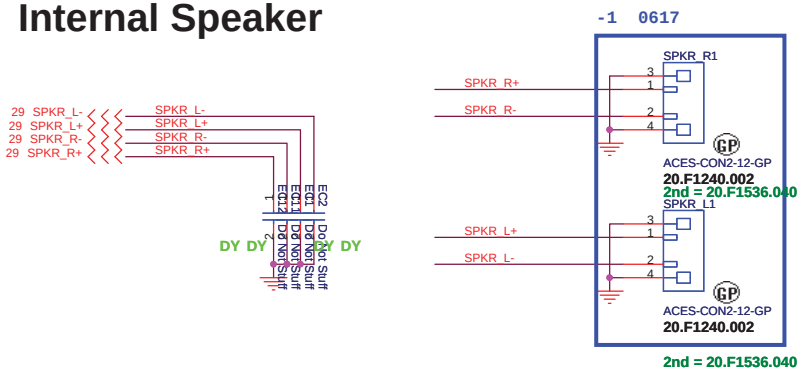
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | *AUDIO AMP* | |
| Size | Document Number JV71 | Rev -2 |
| Date: Thursday, July 02, 2009 | Sheet 29 of 60 | |

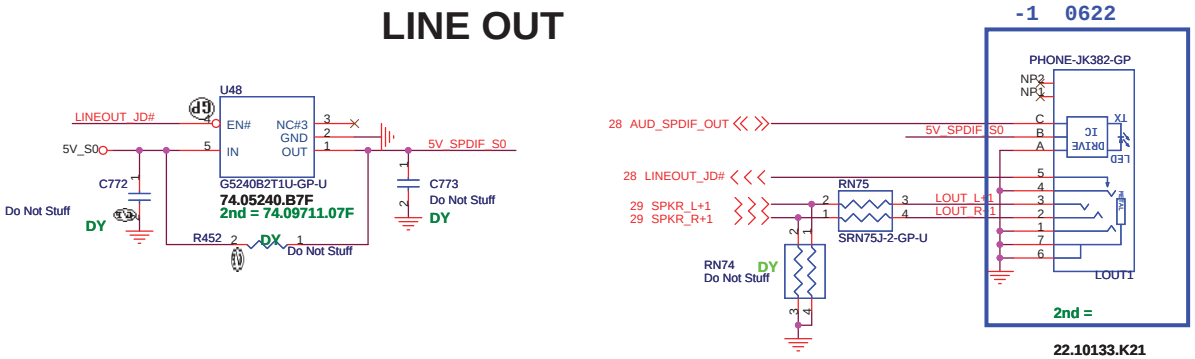
# LINE IN

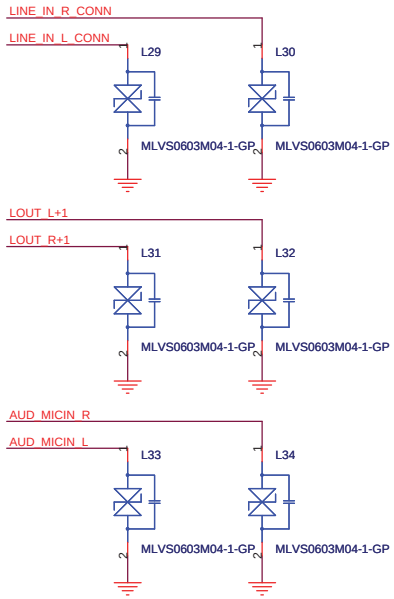



# Internal Speaker

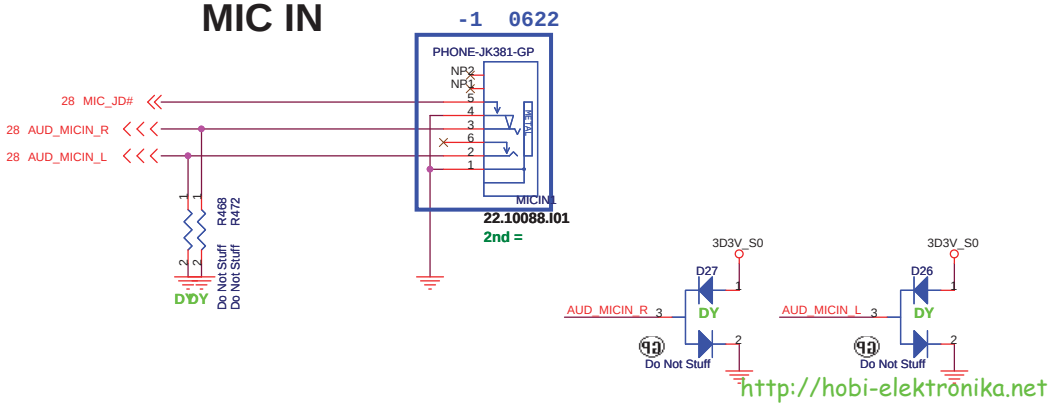



# LINE OUT




# MIC IN






UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

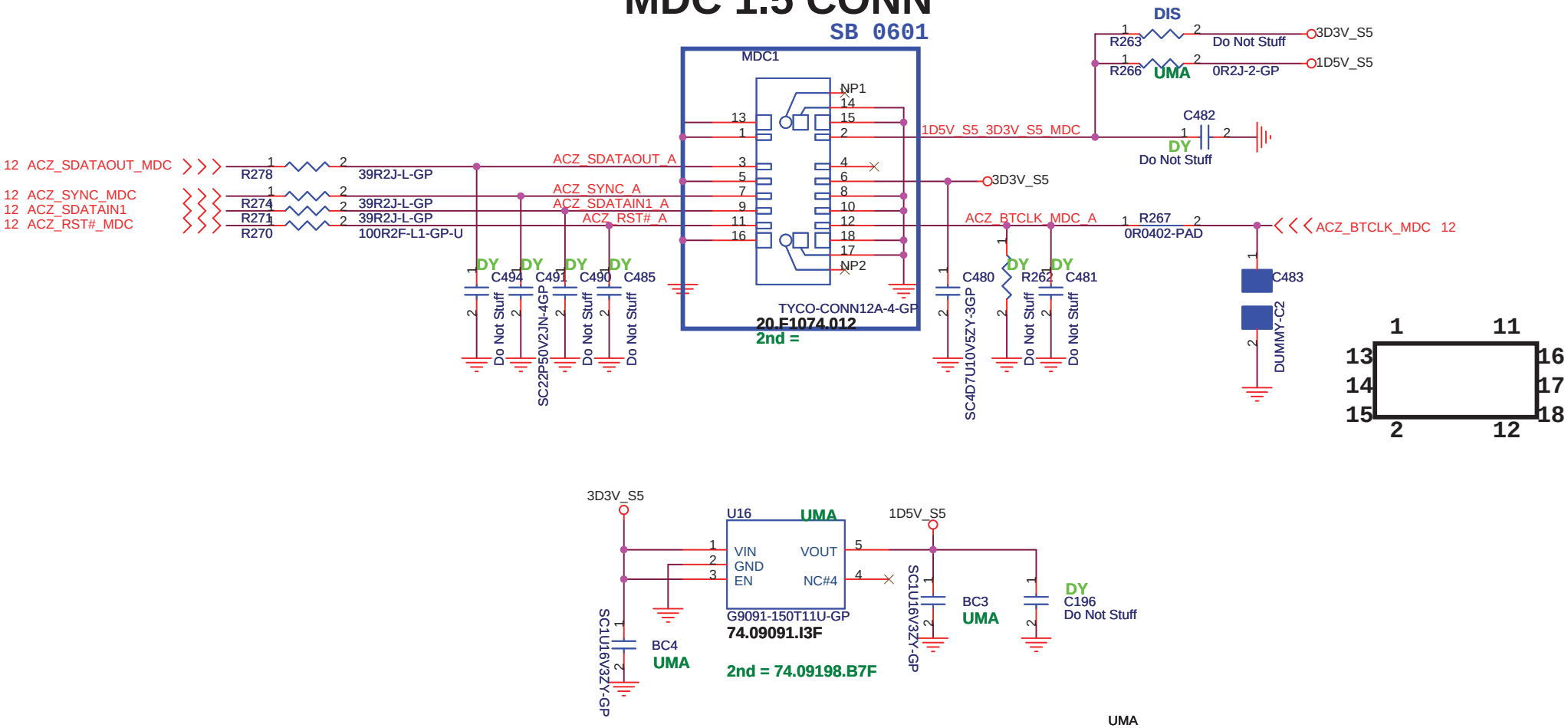
Title: AUDIO jack

Size | Document Number: JV71 | Rev: -2

Date: Thursday, July 02, 2009 | Sheet 30 of 60

# MDC 1.5 CONN

SB 0601





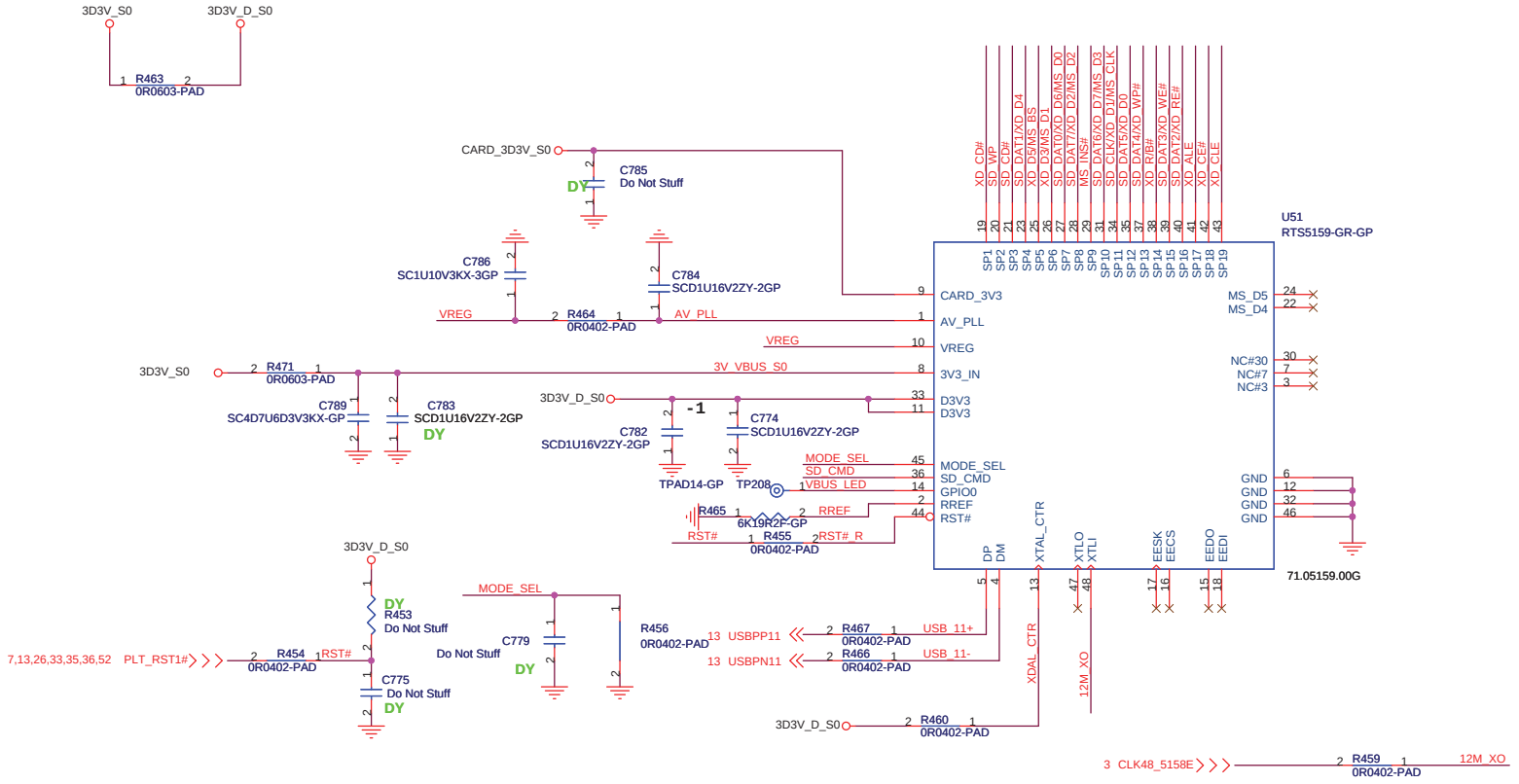


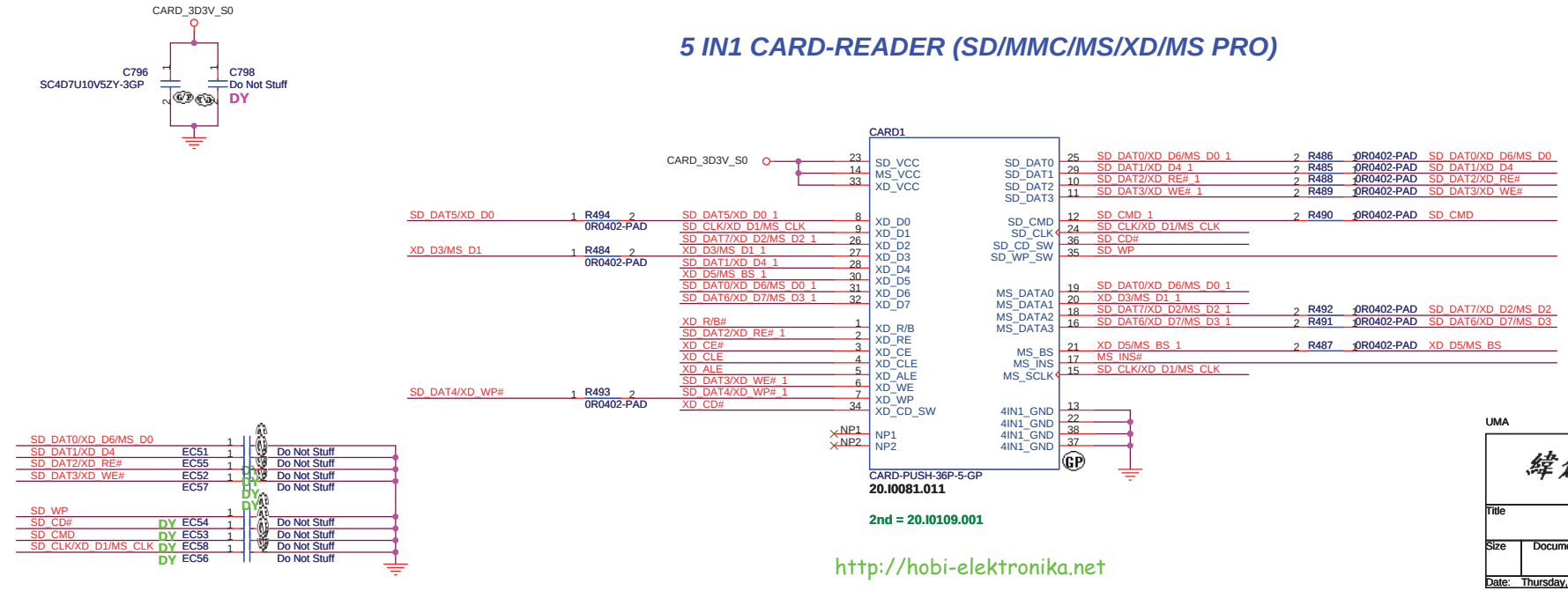


UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | MDC | |
| Size | Document Number JV71 | Rev -2 |
| Date: Thursday, July 02, 2009 | Sheet 31 of 60 | |



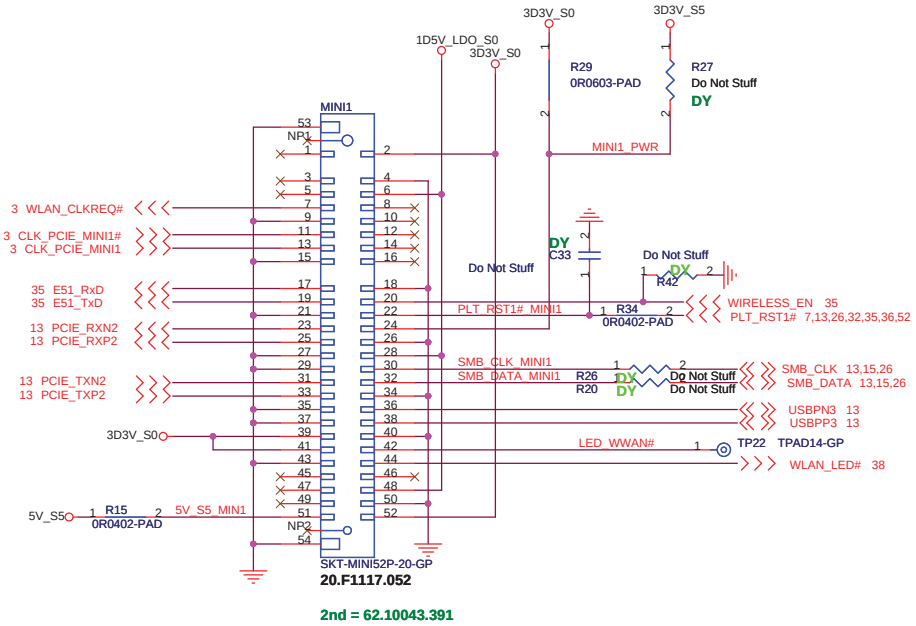



UMA

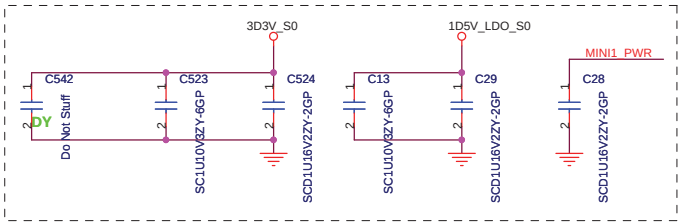
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | Cardreader RTS5159 | |
| Size | Document Number JV71 | Rev -2 |
| Date: Thursday, July 02, 2009 | Sheet 32 of 60 | |

# Mini Card Connector(WLAN)
# Support debug-card




Place near MINI1

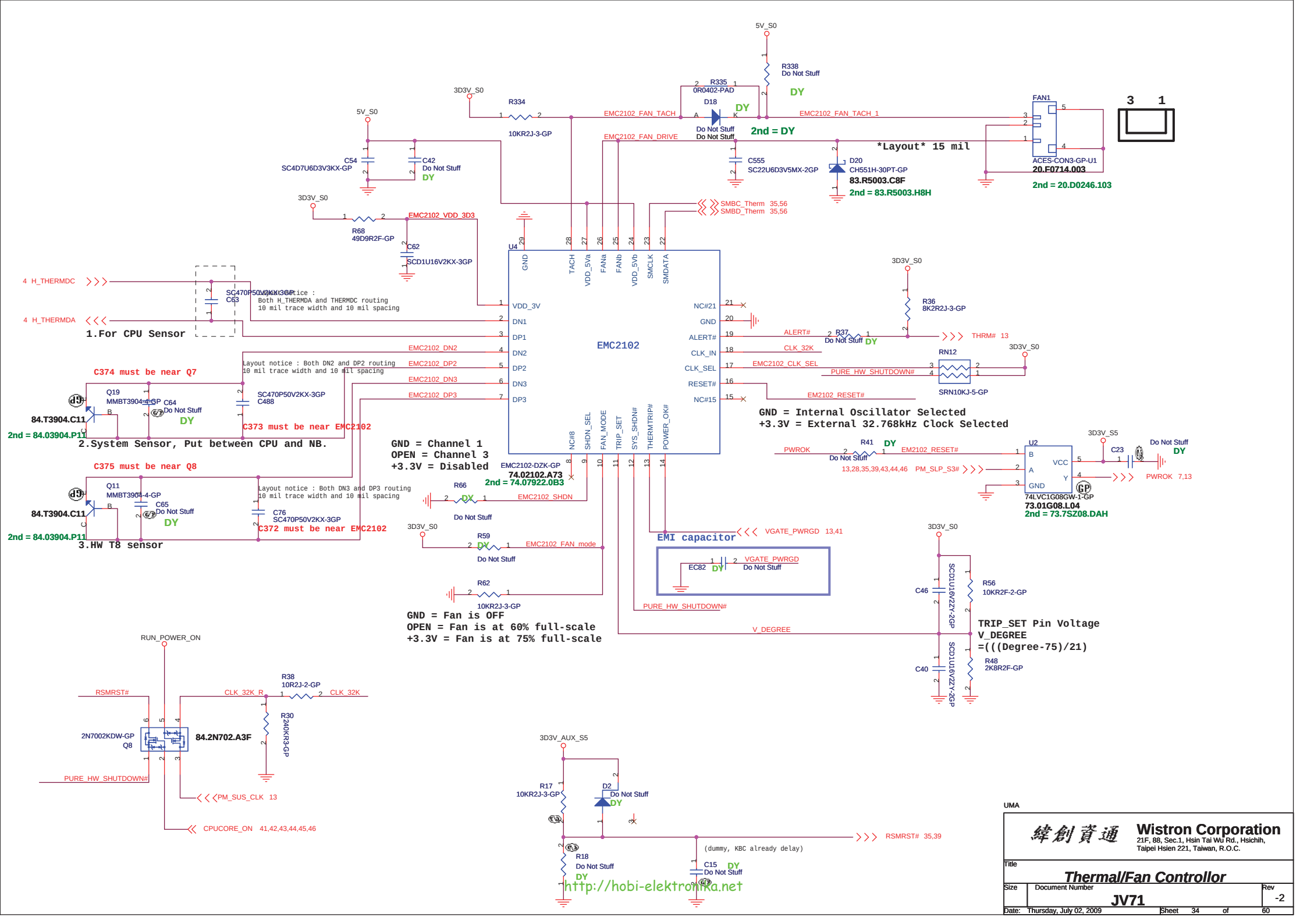


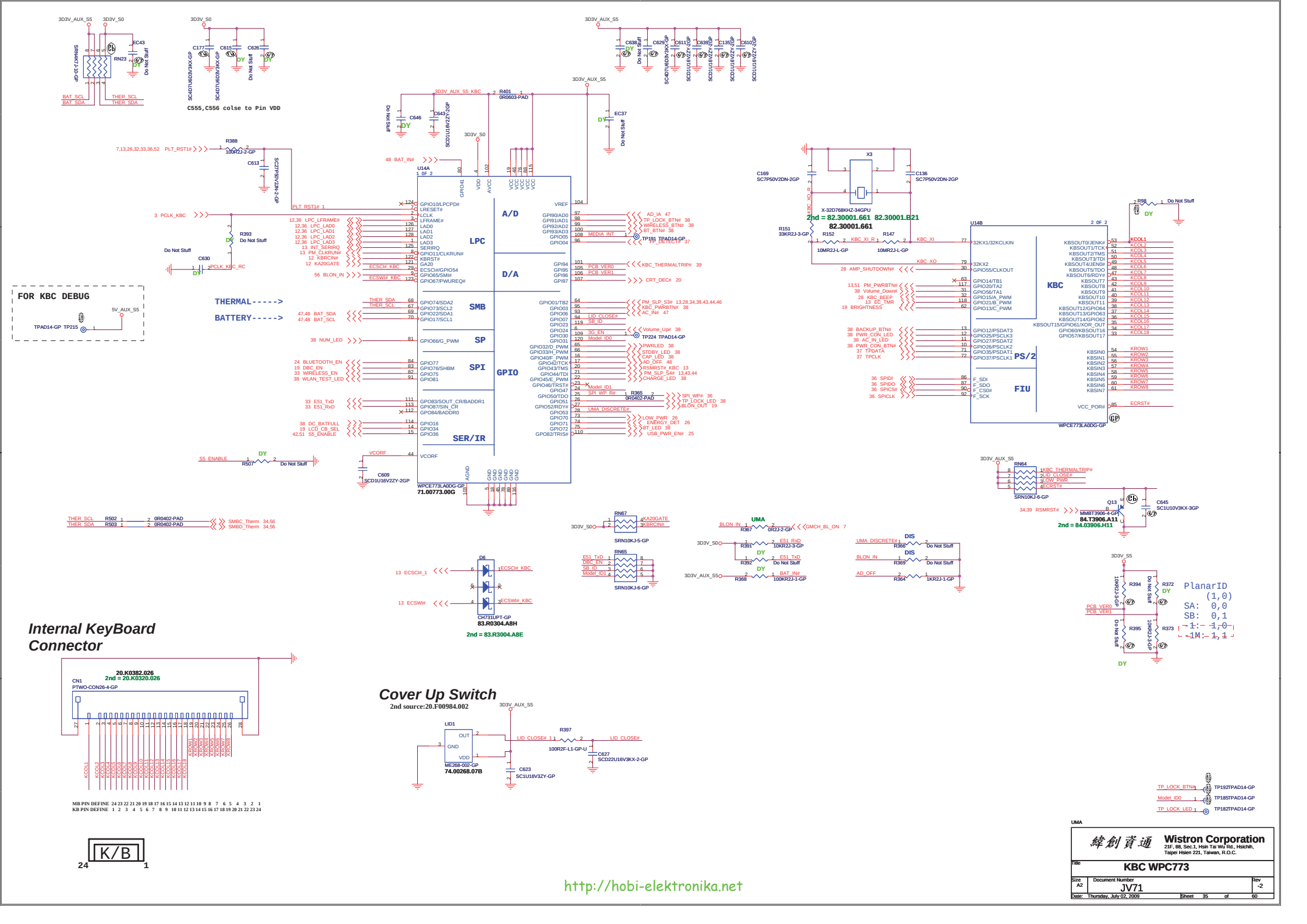

# Mini Card Connector

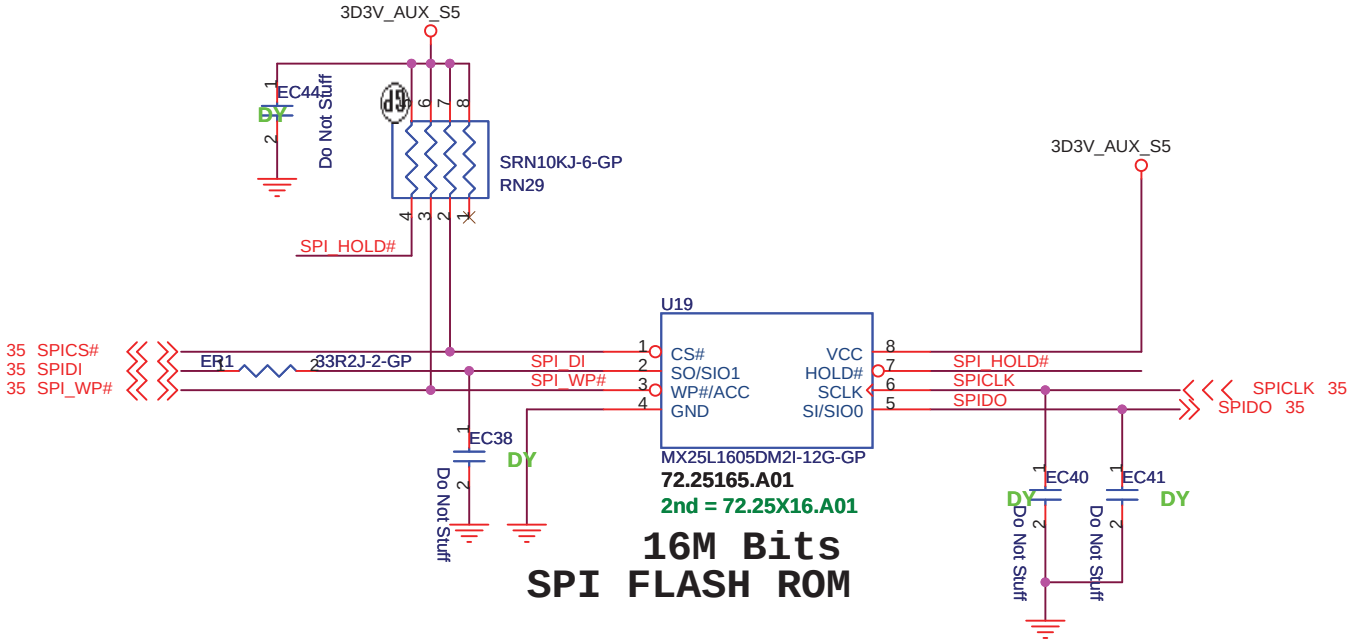
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

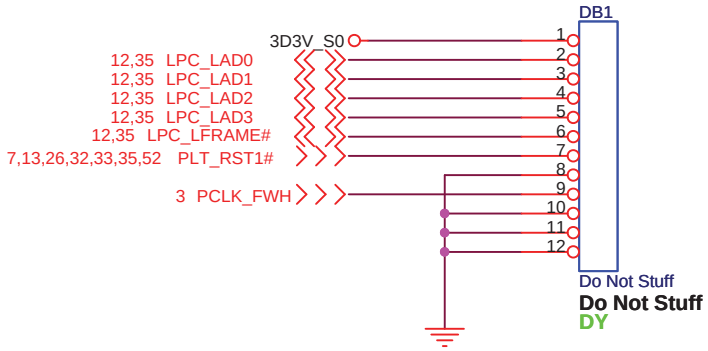
| Title | | |
|---|---|---|
| MINI CARD | | |
| Size: A3 | Document Number: JV71 | Rev: -2 |
| Date: Thursday, July 02, 2009 | Sheet 33 of 60 | |


5V_S0
R338
Do Not Stuff
DY
3D3V_S0
R335
0R0402-PAD
R334
D18
DY
EMC2102_FAN_TACH
EMC2102_FAN_TACH_1
FAN1
10KR2J-3-GP
Do Not Stuff
Do Not Stuff
2nd = DY
EMC2102_FAN_DRIVE
*Layout* 15 mil
C54
SC4D7U6D3V3KX-GP
C42
Do Not Stuff
DY
C555
SC22U6D3V5MX-2GP
D20
CH551H-30PT-GP
83.R5003.C8F
2nd = 83.R5003.H8H
ACES-CON3-GP-U1
20.F0714.003
2nd = 20.D0246.103
3 1
3D3V_S0
R68
49D9R2F-GP
EMC2102_VDD_3D3
C62
SCD1U16V2KX-3GP
SMBC_Therm 35,56
SMBD_Therm 35,56
U4
GND
TACH
VDD_5Va
FANa
FANb
VDD_5Vb
SMCLK
SMDATA
4 H_THERMDC
4 H_THERMDA
SC470P50V2KX-3GP
C63
Layout notice :
Both H_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing
1.For CPU Sensor
VDD_3V
DN1
DP1
DN2
DP2
DN3
DP3
EMC2102
NC#21
GND
ALERT#
CLK_IN
CLK_SEL
RESET#
NC#15
3D3V_S0
R36
8K2R2J-3-GP
R37
Do Not Stuff
DY
ALERT#
THRM# 13
CLK_32K
EMC2102_CLK_SEL
PURE_HW_SHUTDOWN#
RN12
SRN10KJ-5-GP
3D3V_S0
EM2102_RESET#
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
EMC2102_DN2
EMC2102_DP2
EMC2102_DN3
EMC2102_DP3
Layout notice : Both DN2 and DP2 routing
10 mil trace width and 10 mil spacing
C374 must be near Q7
Q19
MMBT3904-4-GP
C64
Do Not Stuff
DY
84.T3904.C11
2nd = 84.03904.P11
SC470P50V2KX-3GP
C488
C373 must be near EMC2102
2.System Sensor, Put between CPU and NB.
C375 must be near Q8
Q11
MMBT3904-4-GP
C65
Do Not Stuff
DY
84.T3904.C11
2nd = 84.03904.P11
Layout notice : Both DN3 and DP3 routing
10 mil trace width and 10 mil spacing
C76
SC470P50V2KX-3GP
C372 must be near EMC2102
3.HW T8 sensor
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
NC#8
SHDN_SEL
FAN_MODE
TRIP_SET
SYS_SHDN#
THERMTRIP#
POWER_OK#
EMC2102-DZK-GP
74.02102.A73
2nd = 74.07922.0B3
R66
DY
Do Not Stuff
EMC2102_SHDN
3D3V_S0
R59
DY
Do Not Stuff
EMC2102_FAN_mode
R62
10KR2J-3-GP
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
EMI capacitor
VGATE_PWRGD 13,41
EC82
DY
VGATE_PWRGD
Do Not Stuff
PURE_HW_SHUTDOWN#
V_DEGREE
PWROK
R41
DY
Do Not Stuff
EM2102_RESET#
13,28,35,39,43,44,46 PM_SLP_S3#
U2
B
A
GND
VCC
Y
74LVC1G08GW-1-GP
73.01G08.L04
2nd = 73.7S08.DAH
3D3V_S5
C23
Do Not Stuff
DY
PWROK 7,13
3D3V_S0
C46
SCD1U16V2ZY-2GP
R56
10KR2F-2-GP
C40
SCD1U16V2ZY-2GP
R48
2K8R2F-GP
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
RUN_POWER_ON
RSMRST#
R38
10R2J-2-GP
CLK_32K_R
CLK_32K
2N7002KDW-GP
Q8
84.2N702.A3F
R30
240KR3-GP
PURE_HW_SHUTDOWN#
PM_SUS_CLK 13
CPUCORE_ON 41,42,43,44,45,46
3D3V_AUX_S5
R17
10KR2J-3-GP
D2
Do Not Stuff
DY
RSMRST# 35,39
(dummy, KBC already delay)
R18
Do Not Stuff
DY
C15
Do Not Stuff
DY
http://hobi-elektronika.net
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Thermal/Fan Controllor
Size
Document Number
JV71
Rev
-2
Date: Thursday, July 02, 2009
Sheet 34 of 60


FOR KBC DEBUG
THERMAL----->
BATTERY----->
U14A
WPCE773LA0DG-GP
71.00773.00G
KBC
PS/2
FIU
Internal KeyBoard Connector
Cover Up Switch
2nd source:20.F00984.002
20.K0382.026
2nd = 20.K0320.026
PTWO-CON24-4-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773
JV71
Thursday, July 02, 2009
http://hobi-elektronika.net




## GOLDEN FINGER FOR DEBUG BOARD

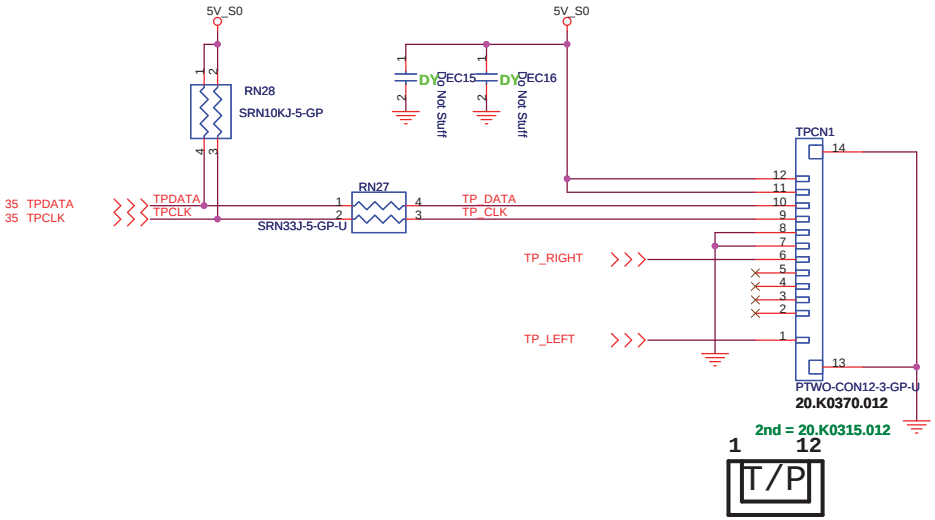




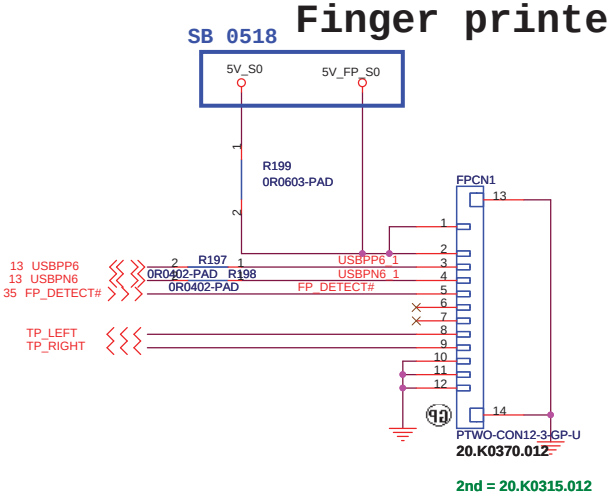

UMA

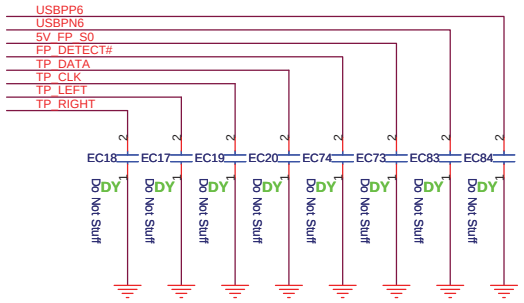
| | | |
|---|---|---|
| 緯創資通 Wistron Corporation<br>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,<br>Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title: **BIOS** | | |
| Size | Document Number: **JV71** | Rev: -2 |
| Date: Thursday, July 02, 2009 | Sheet 36 of 60 | |

# TOUCH PAD




# Finger printer



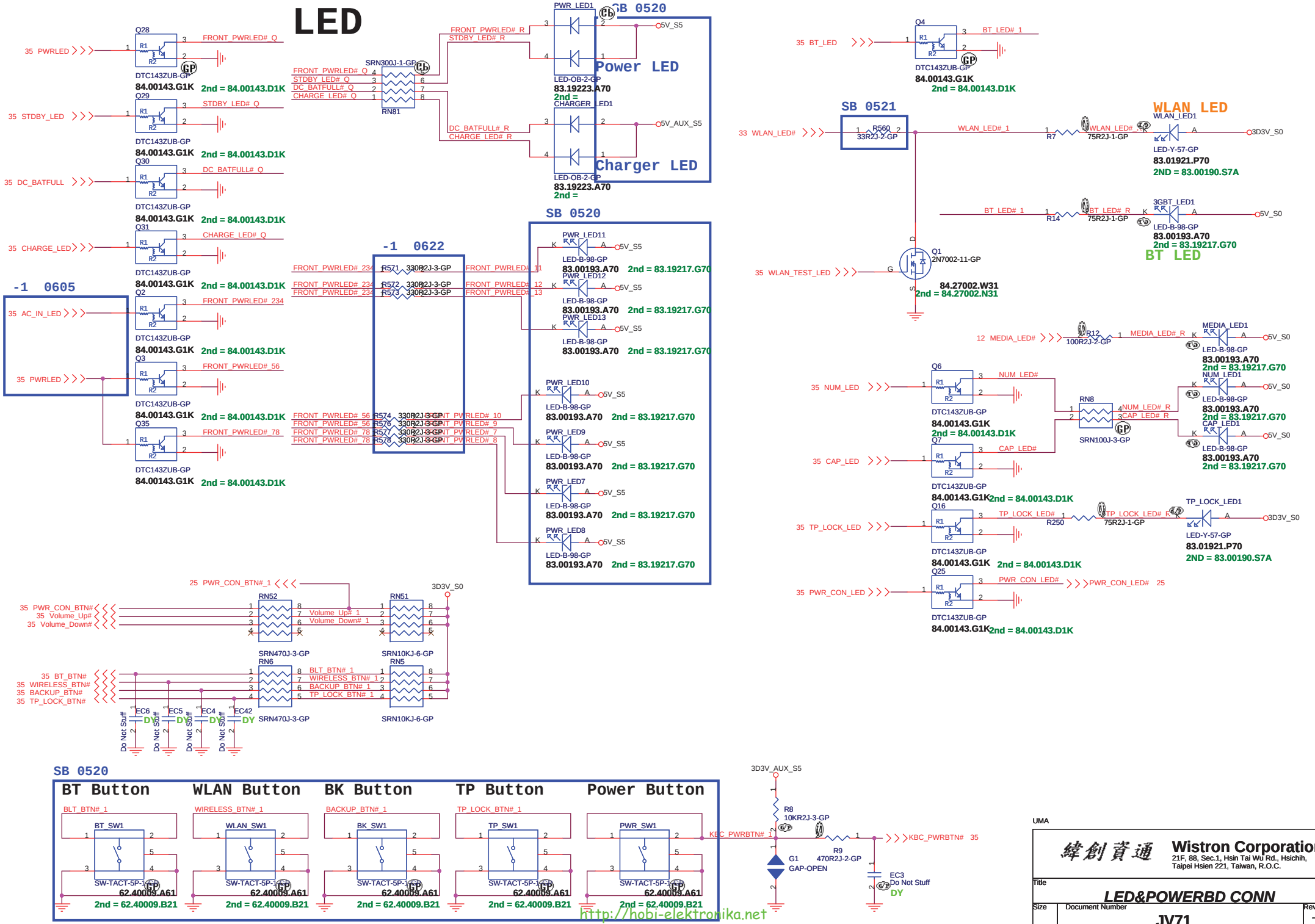



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title: Touch PAD and FP | | |
| Size | Document Number: JV71 | Rev: -2 |
| Date: Thursday, July 02, 2009 | Sheet 37 of 60 | |

# LED




UMA

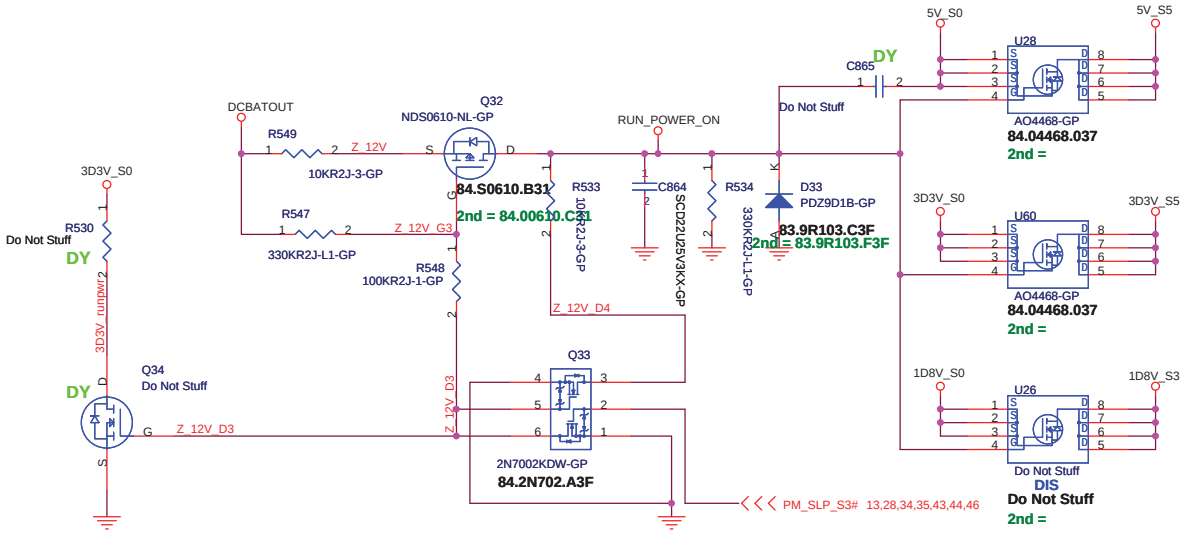
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

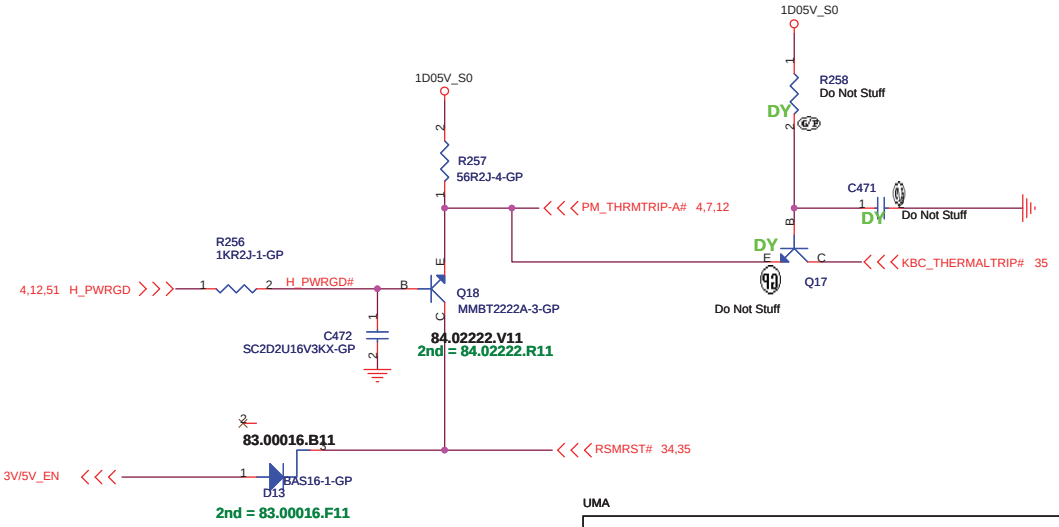
Title: LED&POWERBD CONN

Size | Document Number: JV71 | Rev: -2

Date: Thursday, July 02, 2009 | Sheet 38 of 60

# Run Power





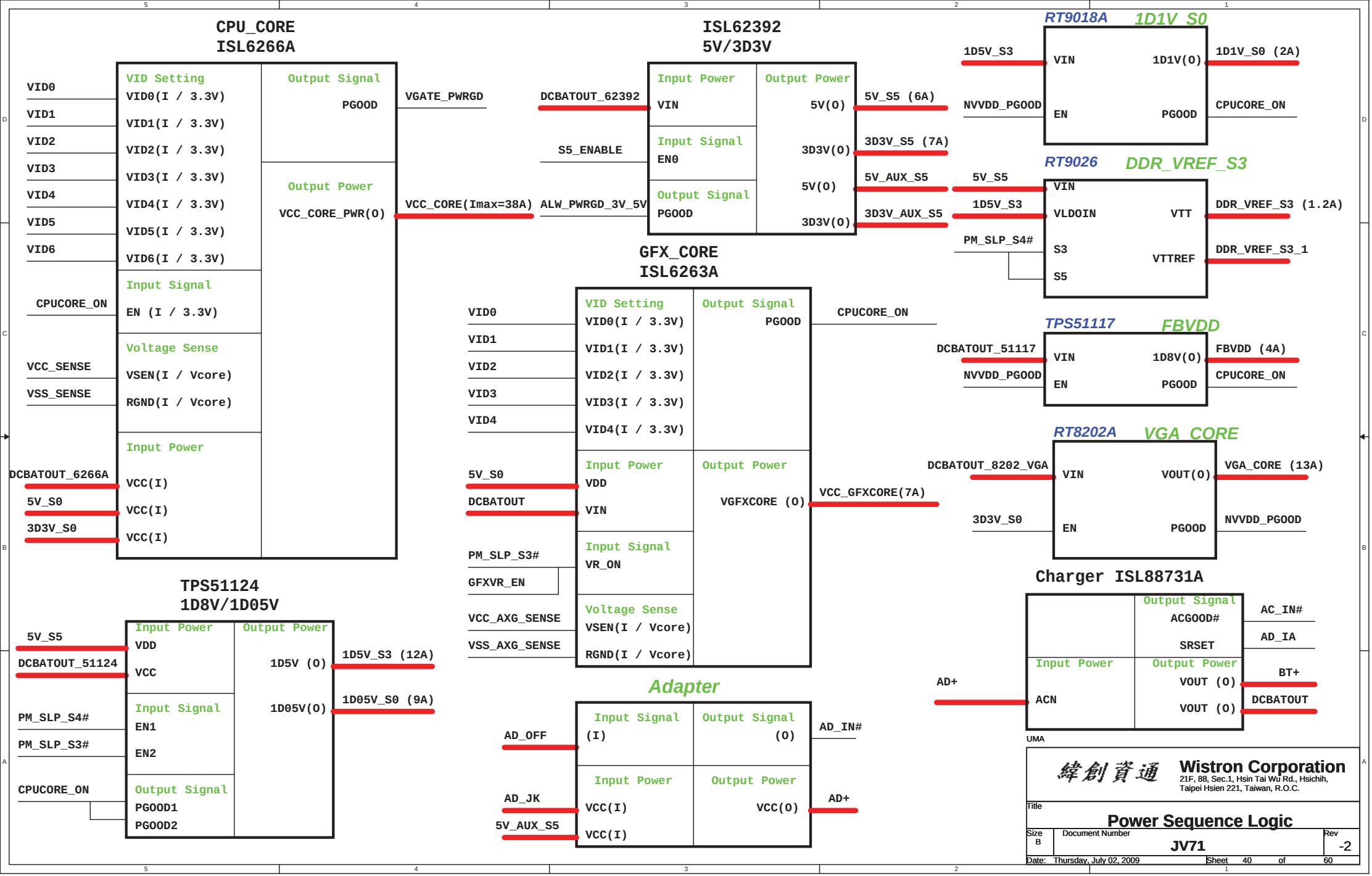

UMA

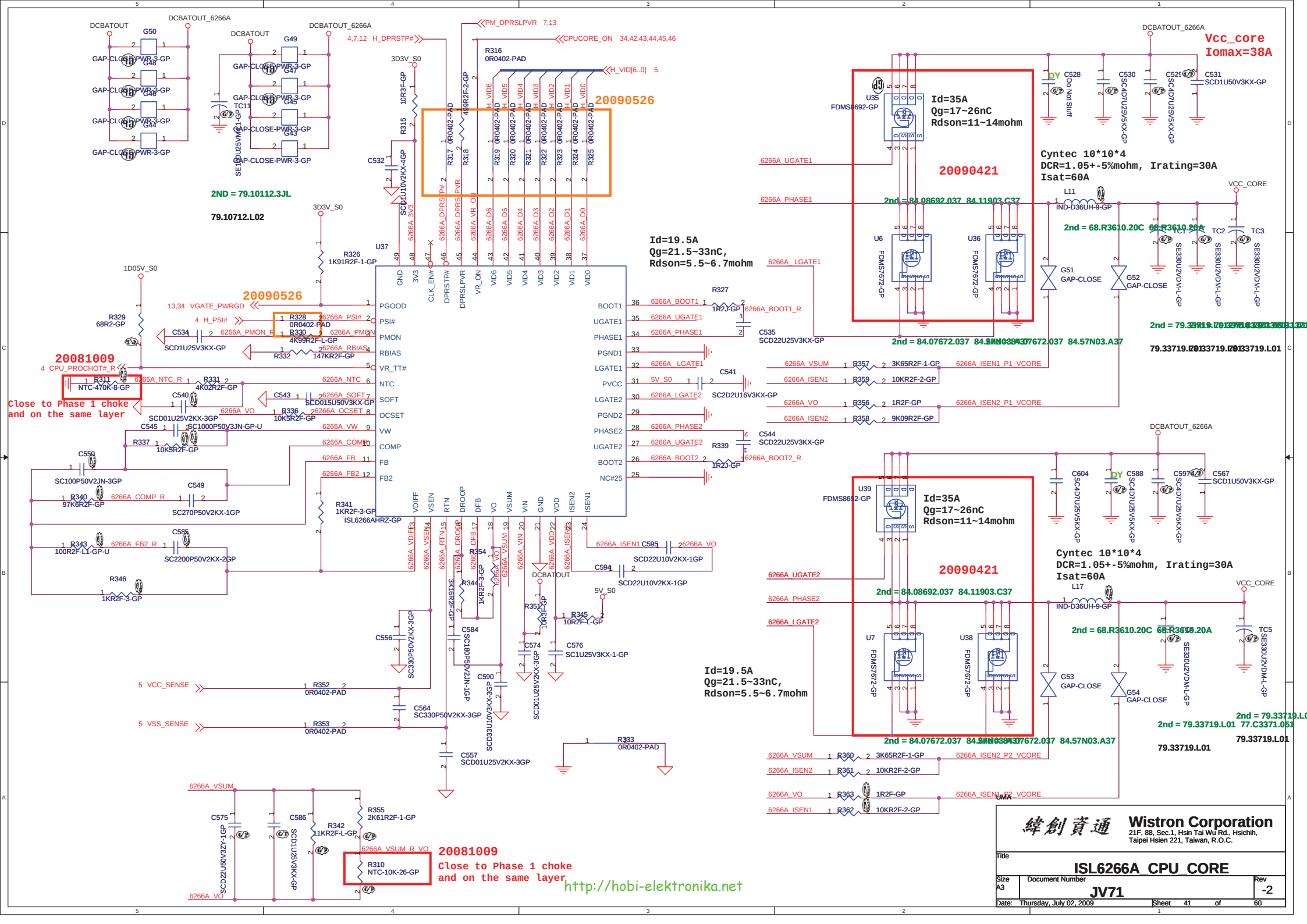
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

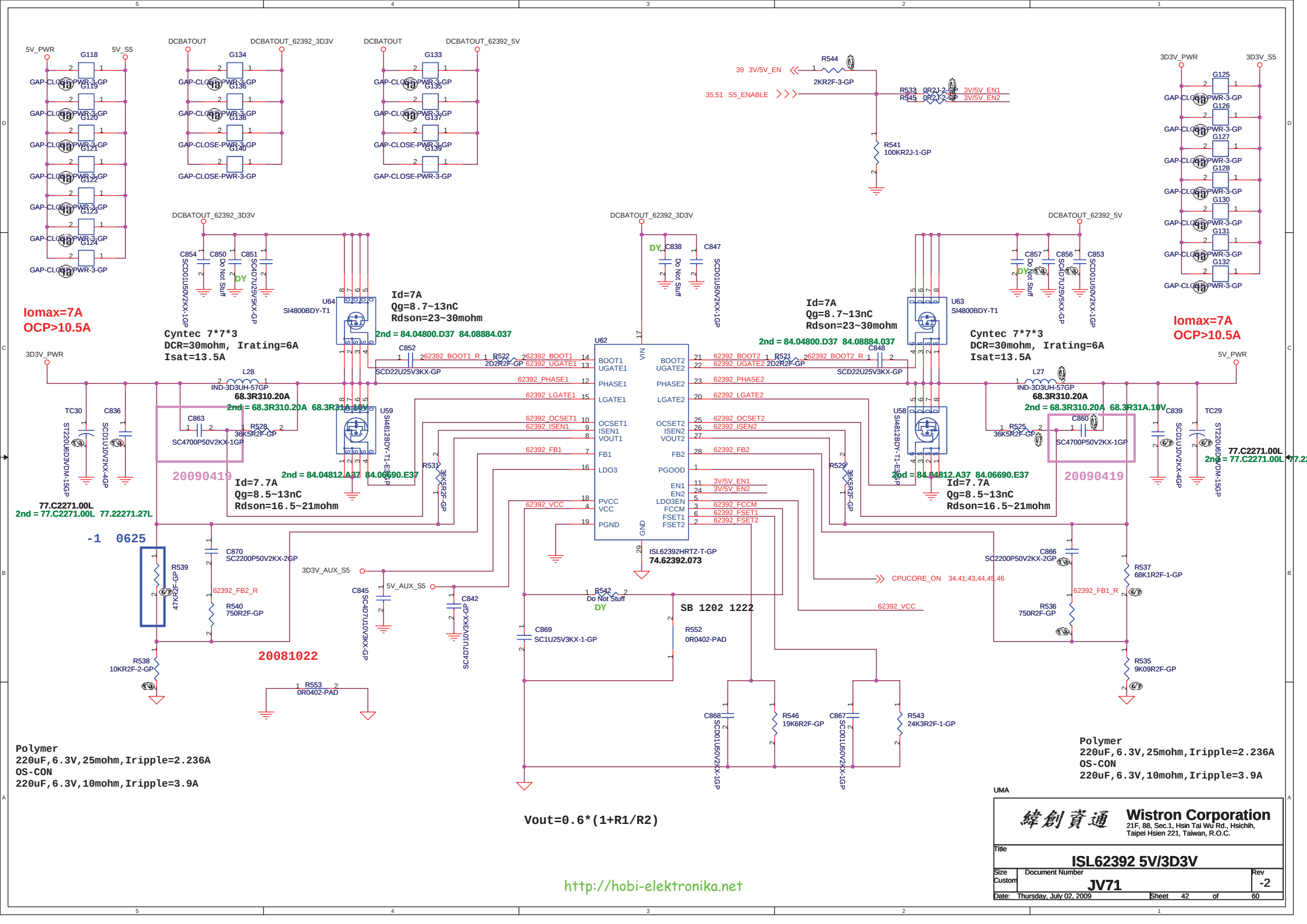
Title: **RUN POWER and 3D3V_AUX_S5**

| Size | Document Number | Rev |
|---|---|---|
| | JV71 | -2 |

Date: Thursday, July 02, 2009 Sheet 39 of 60




Vcc_core
Iomax=38A
Id=35A
Qg=17~26nC
Rdson=11~14mohm
FDMS8692-GP
FDMS7672-GP
20090421
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
IND-D36UH-9-GP
VCC_CORE
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
ISL6266AHRZ-GP
20090526
20081009
Close to Phase 1 choke
and on the same layer
2ND = 79.10112.3JL
79.10712.L02
2nd = 84.08692.037 84.11903.C37
2nd = 84.07672.037 84.57N03.A37
79.33719.L01
2nd = 68.R3610.20C
GAP-CLOSE
DCBATOUT
DCBATOUT_6266A
3D3V_S0
1D05V_S0
5V_S0
UMA
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A_CPU_CORE
Size A3
Document Number JV71
Rev -2
Date: Thursday, July 02, 2009
Sheet 41 of 60



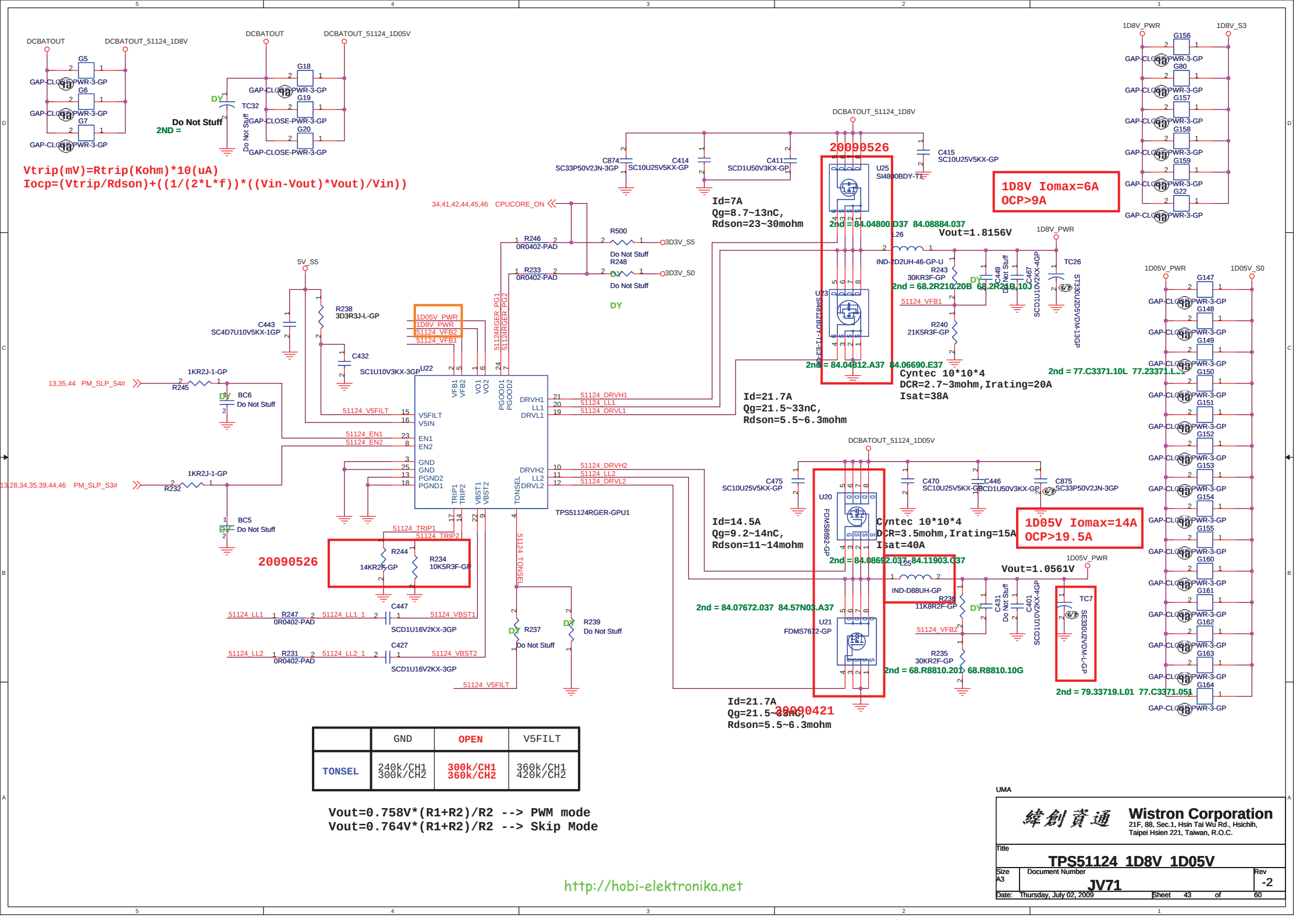

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

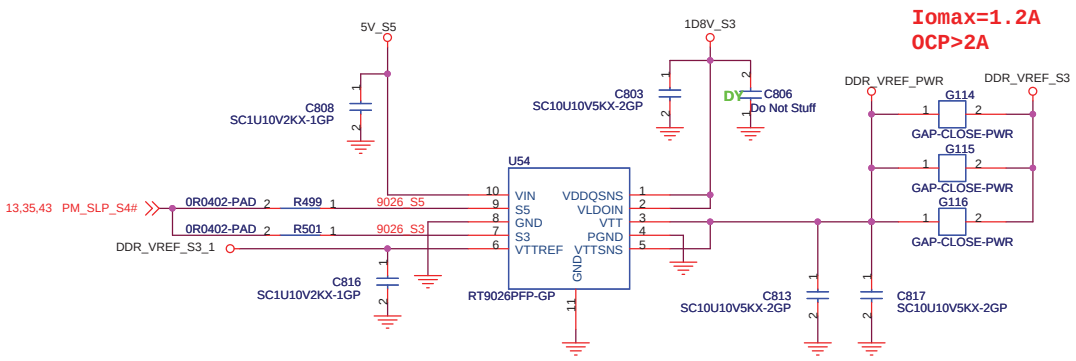
Title: ISL62392 5V/3D3V

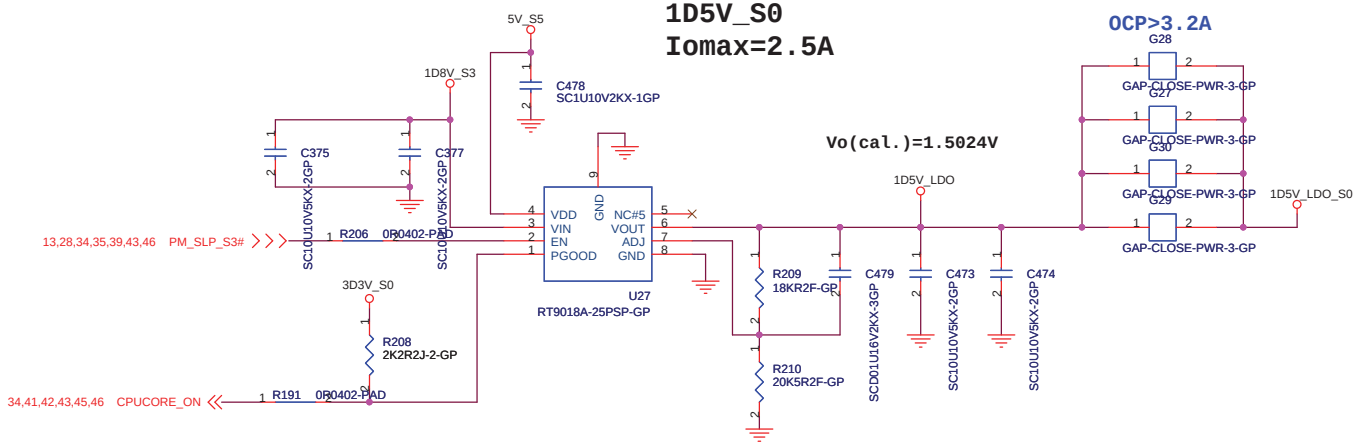
| Size | Document Number | Rev |
|---|---|---|
| Custom | JV71 | -2 |

Date: Thursday, July 02, 2009 Sheet 42 of 60




| | GND | OPEN | V5FILT |
|---|---|---|---|
| TONSEL | 240k/CH1<br>300k/CH2 | 300k/CH1<br>360k/CH2 | 360k/CH1<br>420k/CH2 |





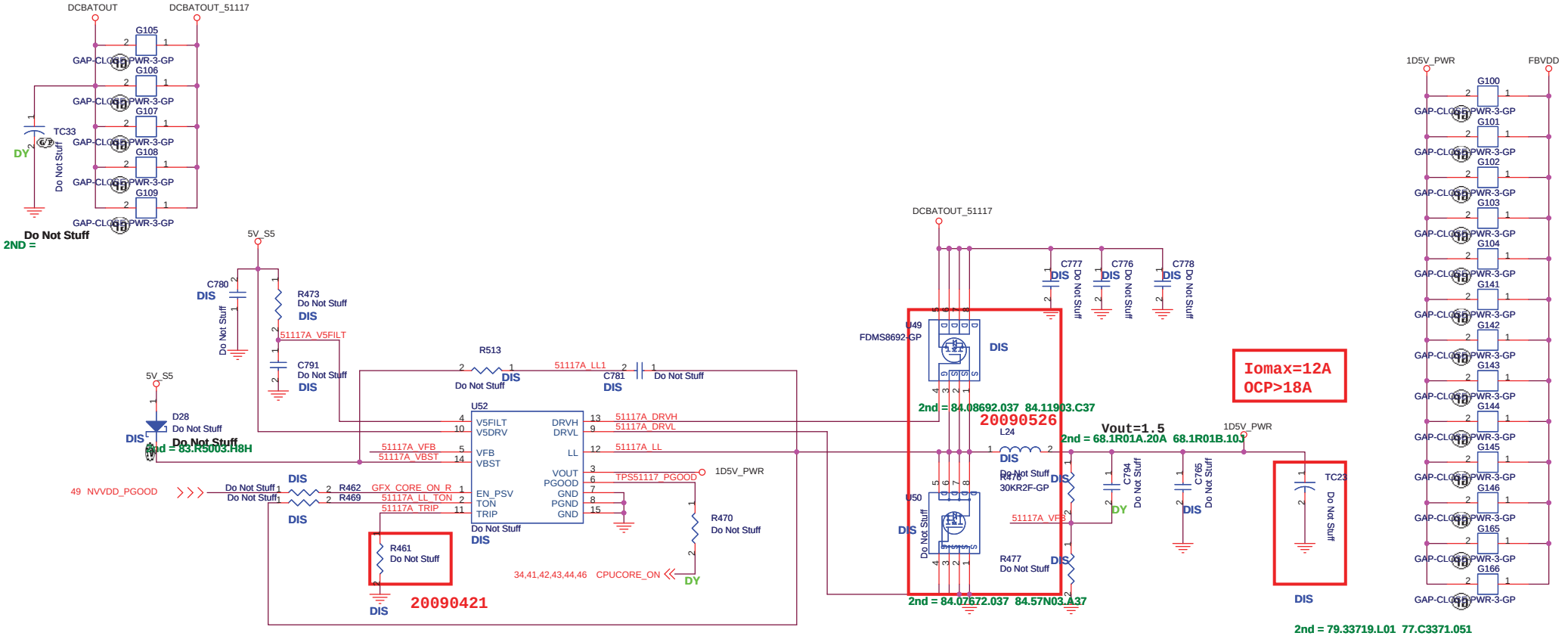

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 0D75V

| Size | Document Number | Rev |
|---|---|---|
| A3 | JV71 | -2 |

Date: Thursday, July 02, 2009 Sheet 44 of 60



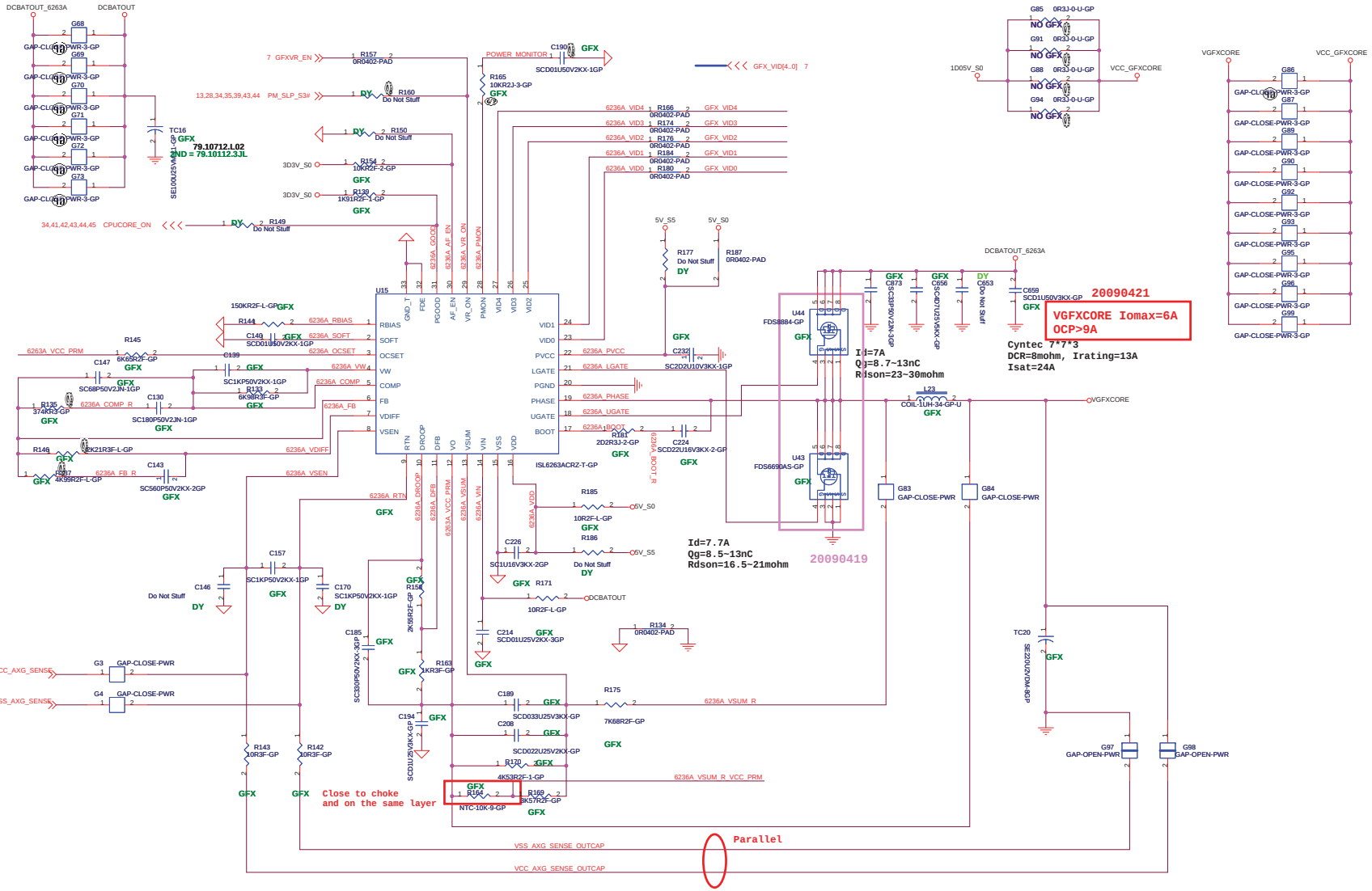

Vout=0.75V*(R1+R2)/R2



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|---|---|---|
| Title | TPS51117_1D8V | |
| Size A3 | Document Number JV71 | Rev -2 |
| Date: Thursday, July 02, 2009 | Sheet 45 of 60 | |





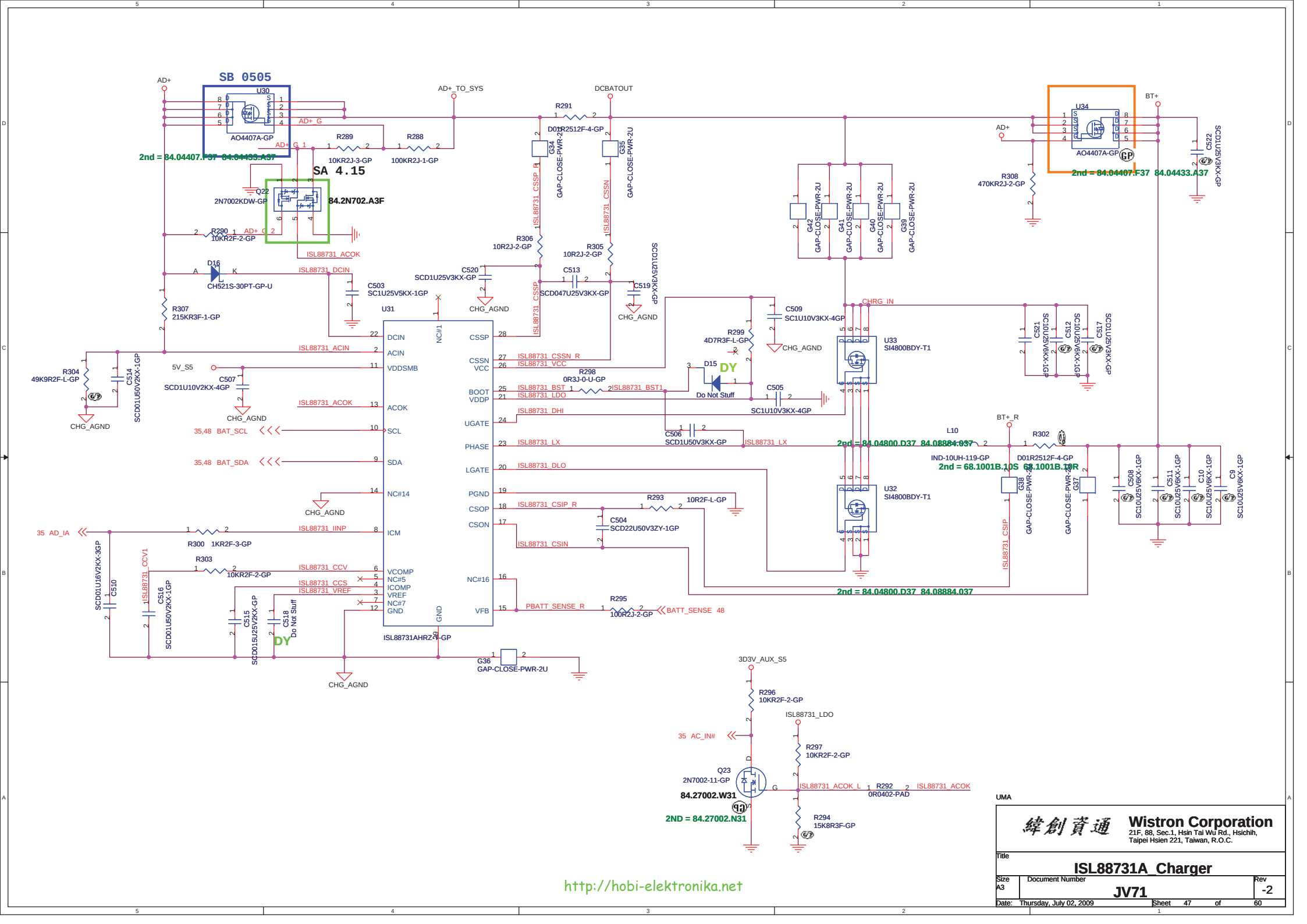

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

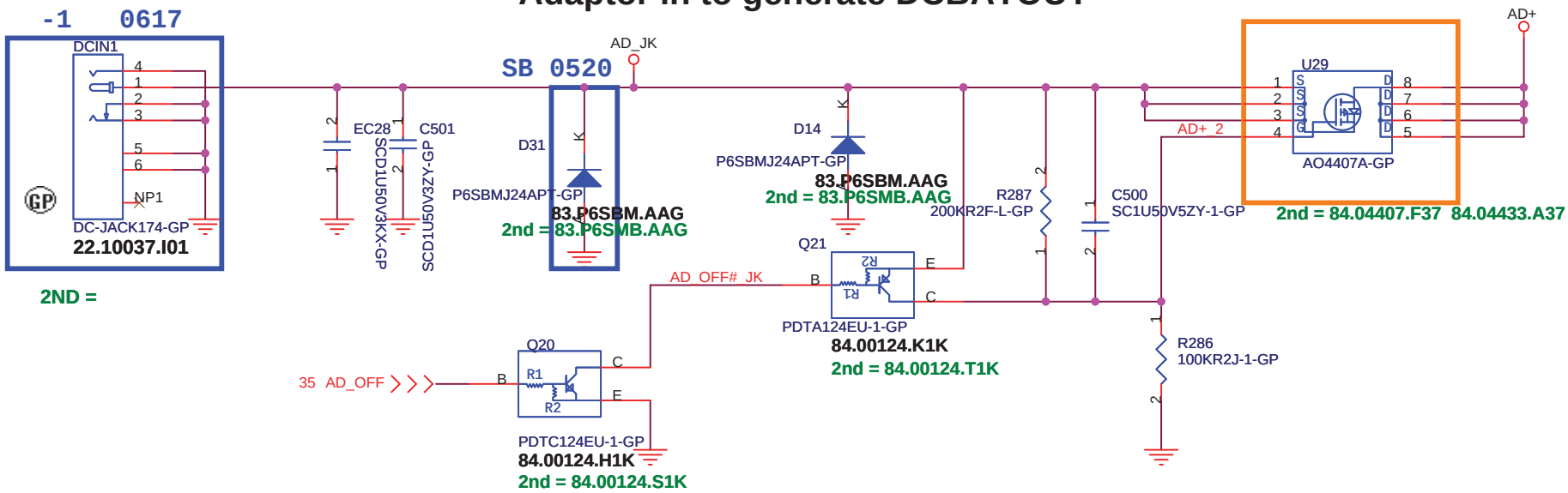
Title: ISL6263A_GFX CORE

| Size | Document Number | Rev |
|---|---|---|
| Custom | JV71 | -2 |

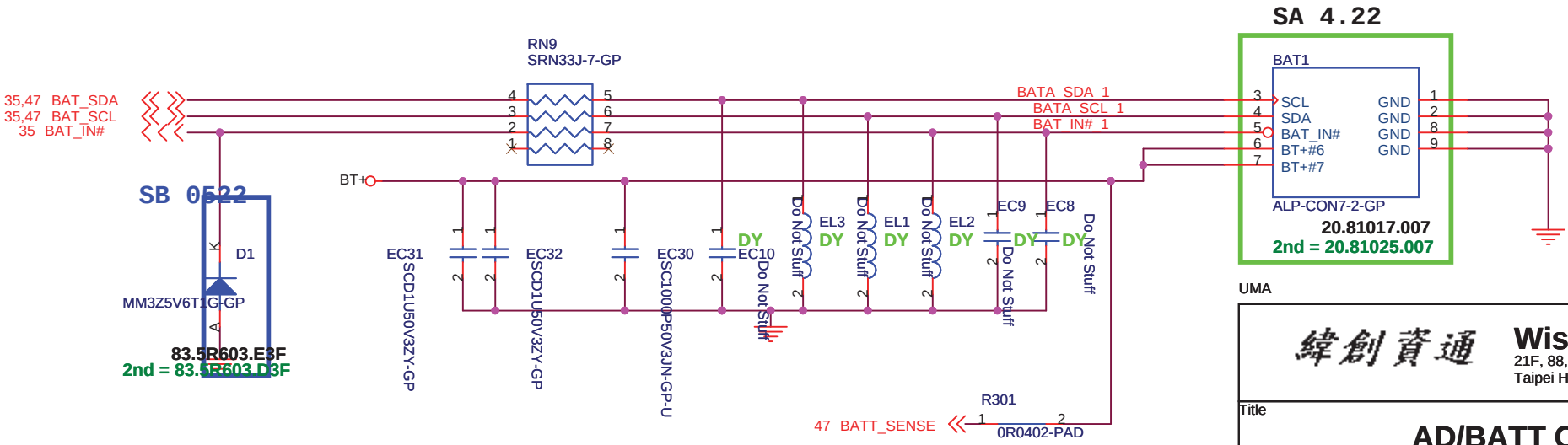
Date: Thursday, July 02, 2009 Sheet 46 of 60


SB 0505
SA 4.15
84.2N702.A3F
2nd = 84.04407.F37 84.04433.A37
2nd = 84.04800.D37 84.08884.037
2nd = 68.1001B.10S 68.1001B.10R
2ND = 84.27002.N31
U30
AO4407A-GP
U34
AO4407A-GP
Q22
2N7002KDW-GP
Q23
2N7002-11-GP
84.27002.W31
U31
ISL88731AHRZ-T-GP
U33
SI4800BDY-T1
U32
SI4800BDY-T1
D16
CH521S-30PT-GP-U
D15
Do Not Stuff
DY
L10
IND-10UH-119-GP
D01R2512F-4-GP
AD+
AD+_TO_SYS
DCBATOUT
BT+
BT+_R
CHRG_IN
3D3V_AUX_S5
5V_S5
CHG_AGND
GAP-CLOSE-PWR-2U
35 AD_IA
35 AC_IN#
35,48 BAT_SCL
35,48 BAT_SDA
BATT_SENSE 48
ISL88731_ACOK
ISL88731_DCIN
ISL88731_ACIN
ISL88731_VCC
ISL88731_BST
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
ISL88731_IINP
ISL88731_CCV
ISL88731_CCS
ISL88731_VREF
PBATT_SENSE_R
ISL88731_ACOK_L
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
NC#1
R307 215KR3F-1-GP
R306 10R2J-2-GP
R305 10R2J-2-GP
R304 49K9R2F-L-GP
R300 1KR2F-3-GP
R303 10KR2F-2-GP
R290 10KR2F-2-GP
R289 10KR2J-3-GP
R288 100KR2J-1-GP
R291 0R2512F-4-GP
R298 0R3J-0-U-GP
R299 4D7R3F-L-GP
R293 10R2F-L-GP
R295 100R2J-2-GP
R296 10KR2F-2-GP
R297 10KR2F-2-GP
R294 15K8R3F-GP
R292 0R0402-PAD
R308 470KR2J-2-GP
R302
C503 SC1U25V5KX-1GP
C504 SCD22U50V3ZY-1GP
C505 SC1U10V3KX-4GP
C506 SCD1U50V3KX-GP
C507 SCD1U10V2KX-4GP
C508 SC10U25V6KX-1GP
C509 SC1U10V3KX-4GP
C510 SCD01U16V2KX-3GP
C511 SC10U25V6KX-1GP
C512 SC10U25V6KX-1GP
C513 SCD047U25V3KX-GP
C514 SCD01U50V2KX-1GP
C515 SCD015U25V2KX-GP
C516 SCD01U50V2KX-1GP
C517 SCD1U25V6KX-GP
C518 Do Not Stuff
C519 SCD1U25V3KX-GP
C520 SCD1U25V3KX-GP
C521 SCD1U25V6KX-1GP
C522 SCD1U25V3KX-GP
C9 SC10U25V6KX-1GP
C10 SC10U25V6KX-1GP
G34 GAP-CLOSE-PWR-2U
G35 GAP-CLOSE-PWR-2U
G36 GAP-CLOSE-PWR-2U
G38 GAP-CLOSE-PWR-2U
G39 GAP-CLOSE-PWR-2U
G40 GAP-CLOSE-PWR-2U
G41 GAP-CLOSE-PWR-2U
G42 GAP-CLOSE-PWR-2U
G37 GAP-CLOSE-PWR-2U
http://hobi-elektronika.net
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A_Charger
Size A3
Document Number
JV71
Rev -2
Date: Thursday, July 02, 2009
Sheet 47 of 60

# Adaptor in to generate DCBATOUT




# BATTERY CONNECTOR



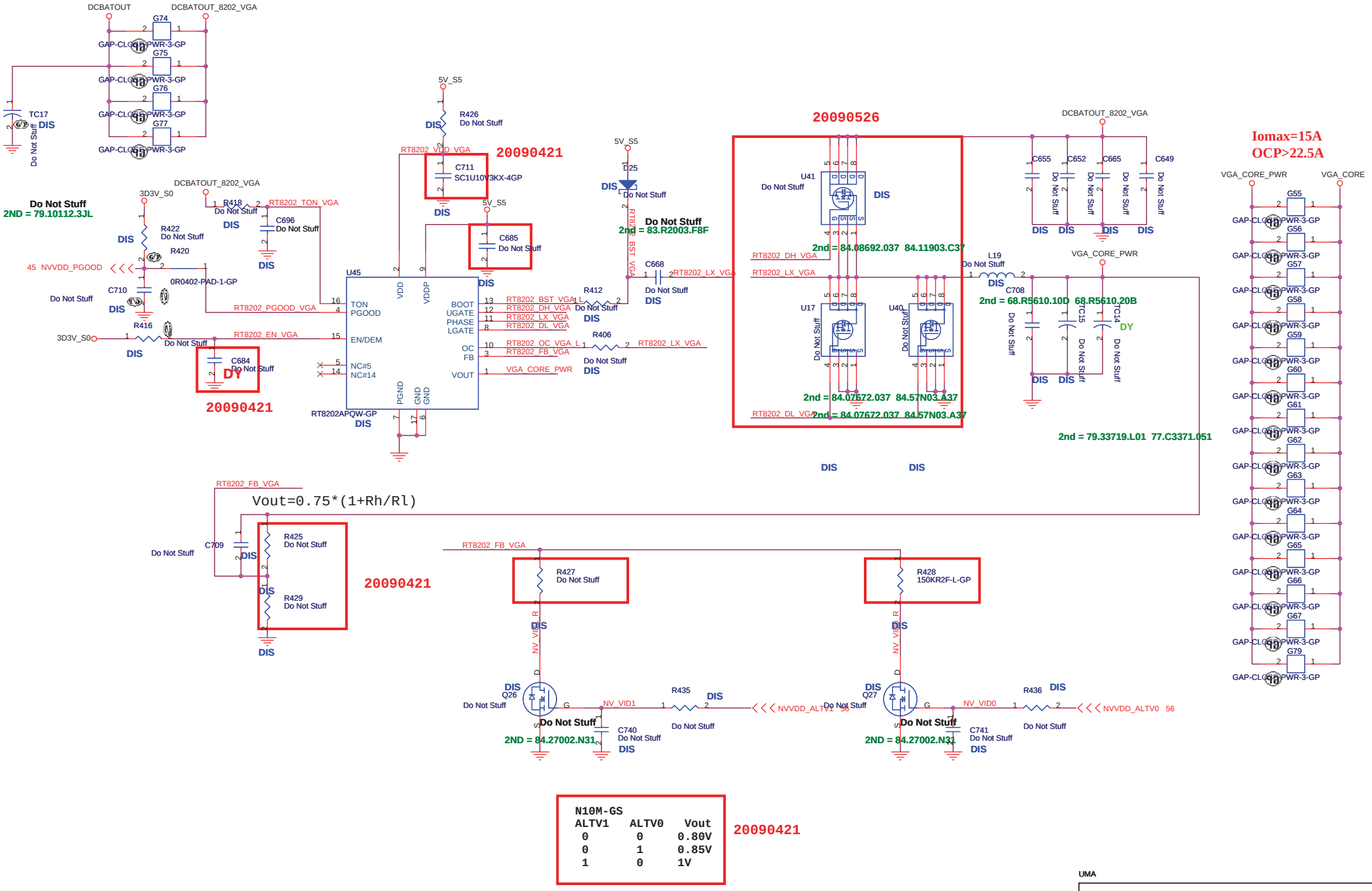

UMA

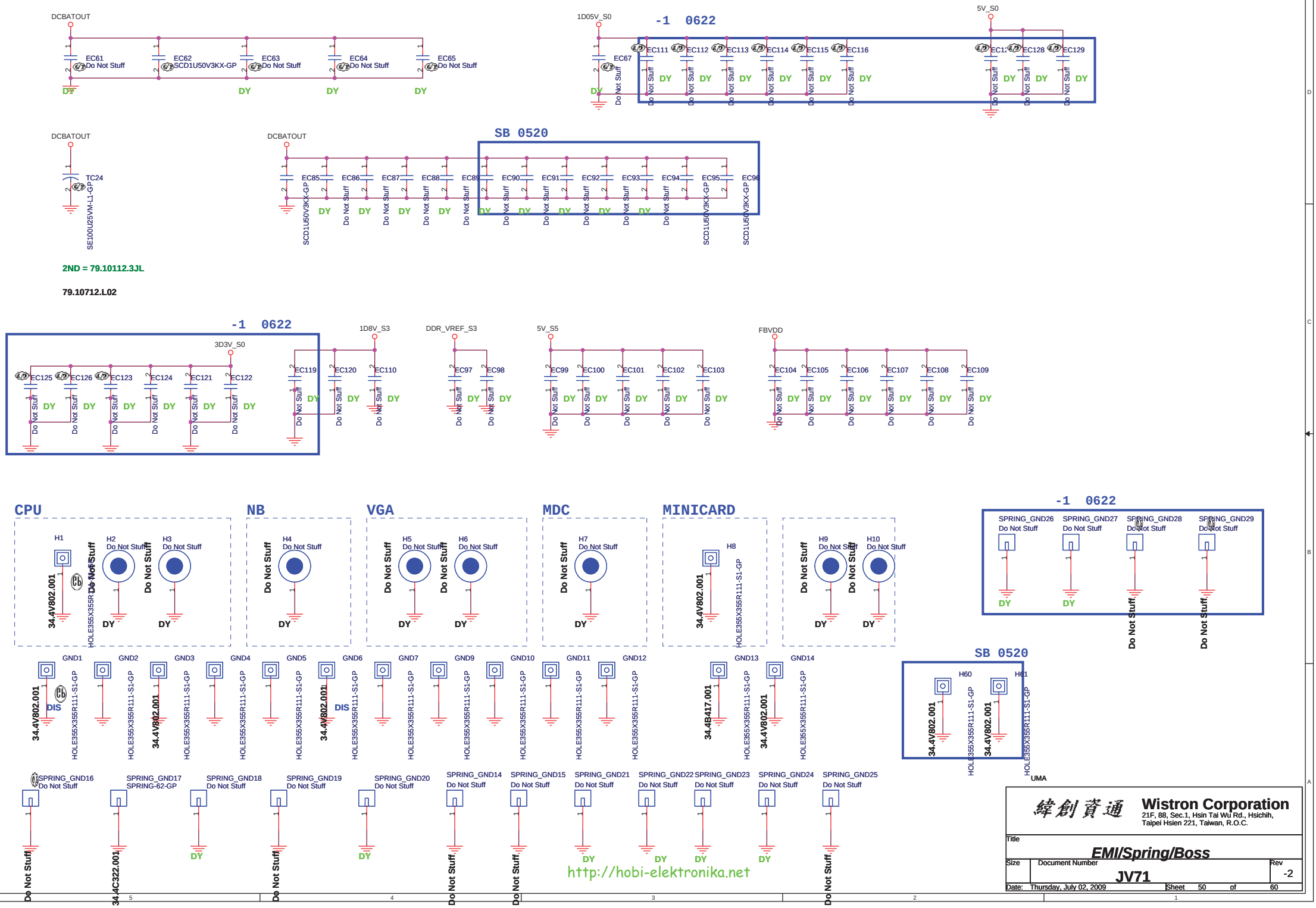

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: AD/BATT CONN

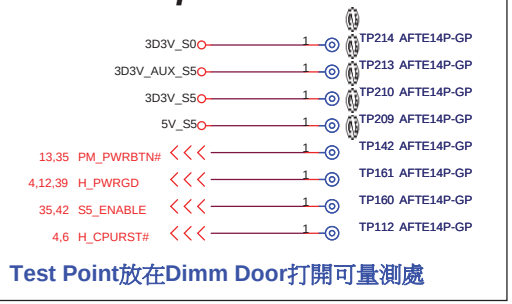
| Size | Document Number | Rev |
|---|---|---|
| | JV71 | -2 |

Date: Thursday, July 02, 2009 Sheet 48 of 60


DCBATOUT
DCBATOUT_8202_VGA
G74
G75
G76
G77
GAP-CLOSE-PWR-3-GP
TC17
DIS
Do Not Stuff
5V_S5
R426
Do Not Stuff
RT8202_VDD_VGA
20090421
C711
SC1U10V3KX-4GP
C685
Do Not Stuff
3D3V_S0
R418
R422
R420
0R0402-PAD-1-GP
C710
C696
45 NVVDD_PGOOD
RT8202_TON_VGA
RT8202_PGOOD_VGA
RT8202_EN_VGA
R416
C684
DY
20090421
U45
TON
PGOOD
EN/DEM
NC#5
NC#14
VDD
VDDP
PGND
GND
BOOT
UGATE
PHASE
LGATE
OC
FB
VOUT
RT8202_BST_VGA_L
RT8202_DH_VGA
RT8202_LX_VGA
RT8202_DL_VGA
RT8202_OC_VGA_L
RT8202_FB_VGA
VGA_CORE_PWR
RT8202APQW-GP
Do Not Stuff
2nd = 83.R2003.F8F
D25
C668
R412
R406
20090526
U41
U17
U40
2nd = 84.08692.037 84.11903.C37
2nd = 84.07672.037 84.57N03.A37
L19
C708
2nd = 68.R5610.10D 68.R5610.20B
TC15
TC14
C655
C652
C665
C649
2nd = 79.33719.L01 77.C3371.051
Iomax=15A
OCP>22.5A
VGA_CORE_PWR
VGA_CORE
G55
G56
G57
G58
G59
G60
G61
G62
G63
G64
G65
G66
G67
G79
Vout=0.75*(1+Rh/Rl)
C709
R425
R429
20090421
R427
R428
150KR2F-L-GP
NV_VID1_R
NV_VID0_R
Q26
Q27
NV_VID1
NV_VID0
R435
R436
NVVDD_ALTV1 56
NVVDD_ALTV0 56
C740
C741
2ND = 84.27002.N31
N10M-GS
ALTV1 ALTV0 Vout
0 0 0.80V
0 1 0.85V
1 0 1V
20090421
http://hobi-elektronika.net
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RT8202A VGA CORE
Size A3
Document Number
JV71
Rev -2
Date: Thursday, July 02, 2009
Sheet 49 of 60


DCBATOUT
EC61 Do Not Stuff
EC62 SCD1U50V3KX-GP
EC63 Do Not Stuff
EC64 Do Not Stuff
EC65 Do Not Stuff
DY
1D05V_S0
-1 0622
EC67 Do Not Stuff
EC111 EC112 EC113 EC114 EC115 EC116
5V_S0
EC127 EC128 EC129
DCBATOUT
TC24
SE100U25VM-L1-GP
DCBATOUT
SB 0520
EC85 EC86 EC87 EC88 EC89 EC90 EC91 EC92 EC93 EC94 EC95 EC96
SCD1U50V3KX-GP
2ND = 79.10112.3JL
79.10712.L02
-1 0622
3D3V_S0
EC125 EC126 EC123 EC124 EC121 EC122
1D8V_S3
EC119 EC120 EC110
DDR_VREF_S3
EC97 EC98
5V_S5
EC99 EC100 EC101 EC102 EC103
FBVDD
EC104 EC105 EC106 EC107 EC108 EC109
CPU
H1
34.4V802.001
H2 Do Not Stuff
H3 Do Not Stuff
HOLE355X355R111-S1-GP
NB
H4 Do Not Stuff
VGA
H5 Do Not Stuff
H6 Do Not Stuff
MDC
H7 Do Not Stuff
MINICARD
H8
34.4V802.001
H9 Do Not Stuff
H10 Do Not Stuff
-1 0622
SPRING_GND26 Do Not Stuff
SPRING_GND27 Do Not Stuff
SPRING_GND28 Do Not Stuff
SPRING_GND29 Do Not Stuff
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND9 GND10 GND11 GND12 GND13 GND14
34.4V802.001
34.4B417.001
DIS
HOLE355X355R111-S1-GP
SB 0520
H60 H61
SPRING_GND16 Do Not Stuff
SPRING_GND17 SPRING-62-GP
SPRING_GND18 Do Not Stuff
SPRING_GND19 Do Not Stuff
SPRING_GND20 Do Not Stuff
SPRING_GND14 Do Not Stuff
SPRING_GND15 Do Not Stuff
SPRING_GND21 Do Not Stuff
SPRING_GND22 Do Not Stuff
SPRING_GND23 Do Not Stuff
SPRING_GND24 Do Not Stuff
SPRING_GND25 Do Not Stuff
34.4C322.001
http://hobi-elektronika.net
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
JV71
Rev
-2
Date: Thursday, July 02, 2009
Sheet 50 of 60

# Check test point




**Test Point放在Dimm Door打開可量測處**



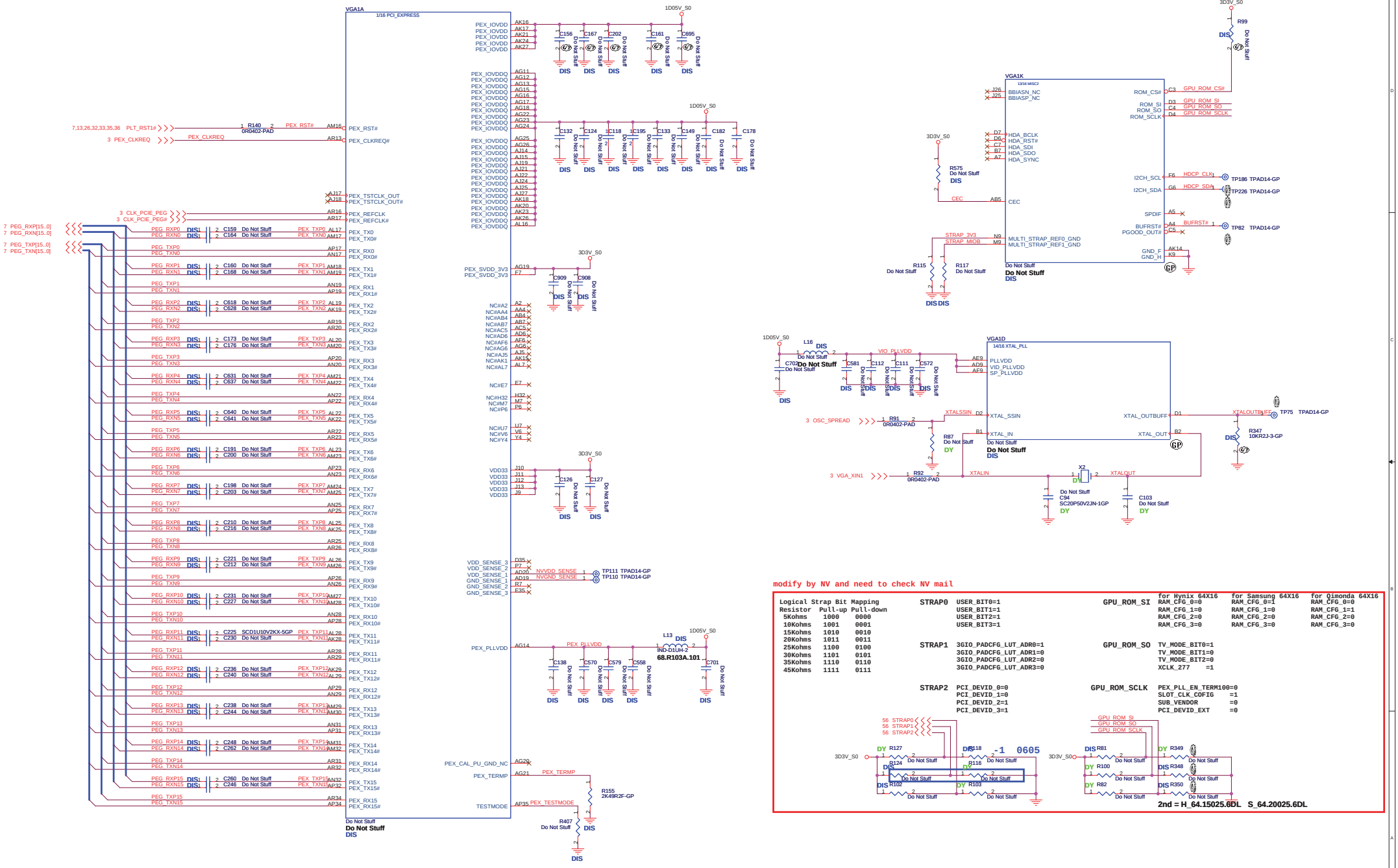
UMA

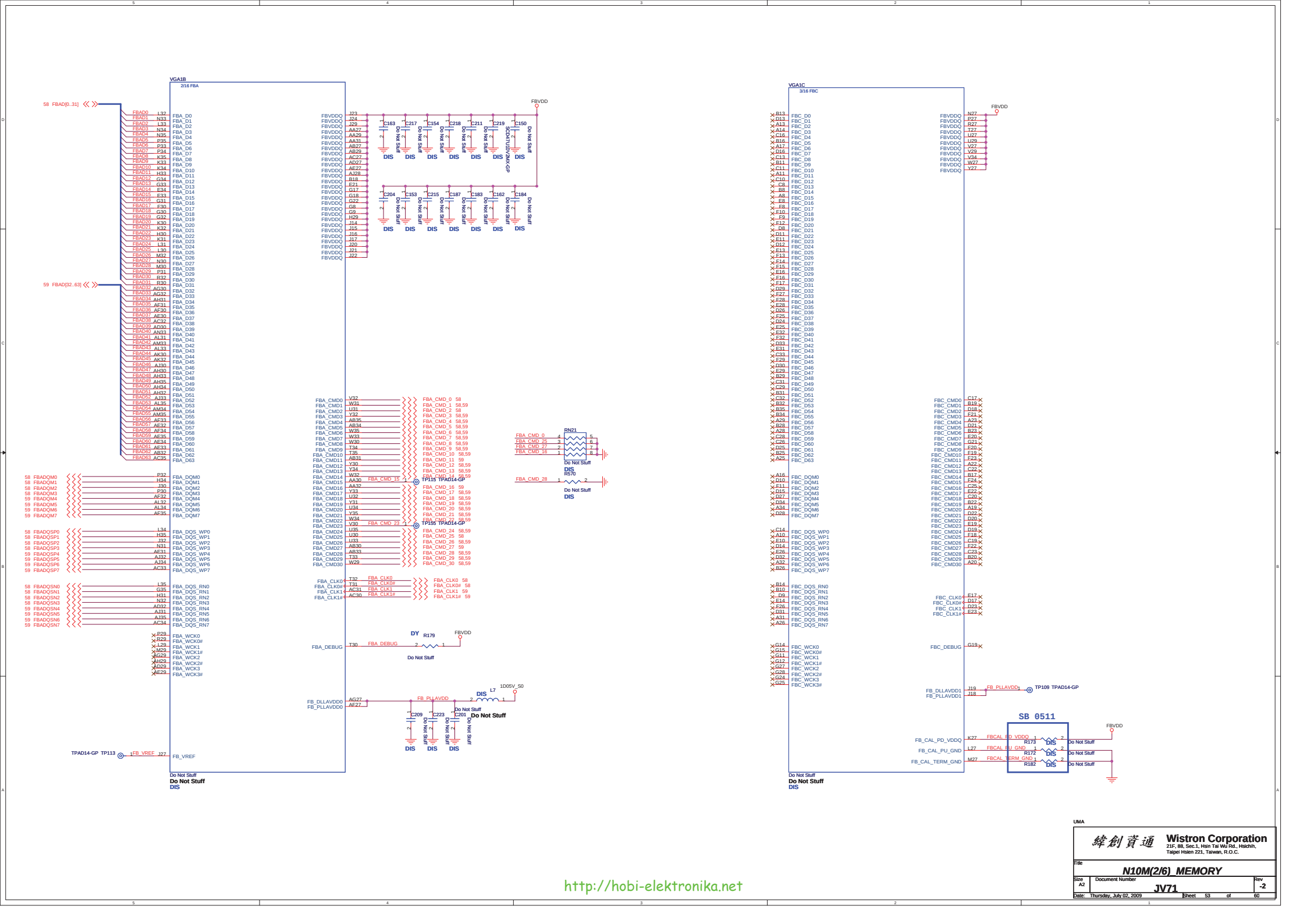
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AFTE_TP***

| Size | Document Number | Rev |
|---|---|---|
| A3 | JV71 | -2 |

Date: Thursday, July 02, 2009 Sheet 51 of 60







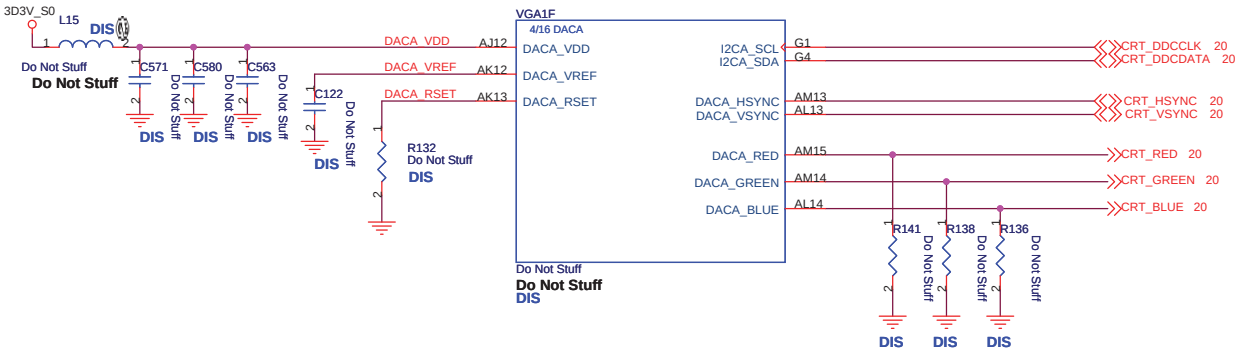

UMA

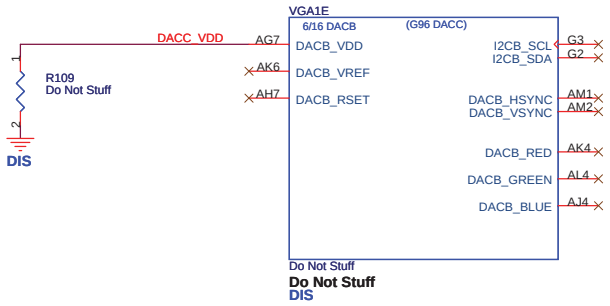
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N10M(2/6)_MEMORY

Size: A2 | Document Number: JV71 | Rev: -2

Date: Thursday, July 02, 2009 | Sheet 53 of 60





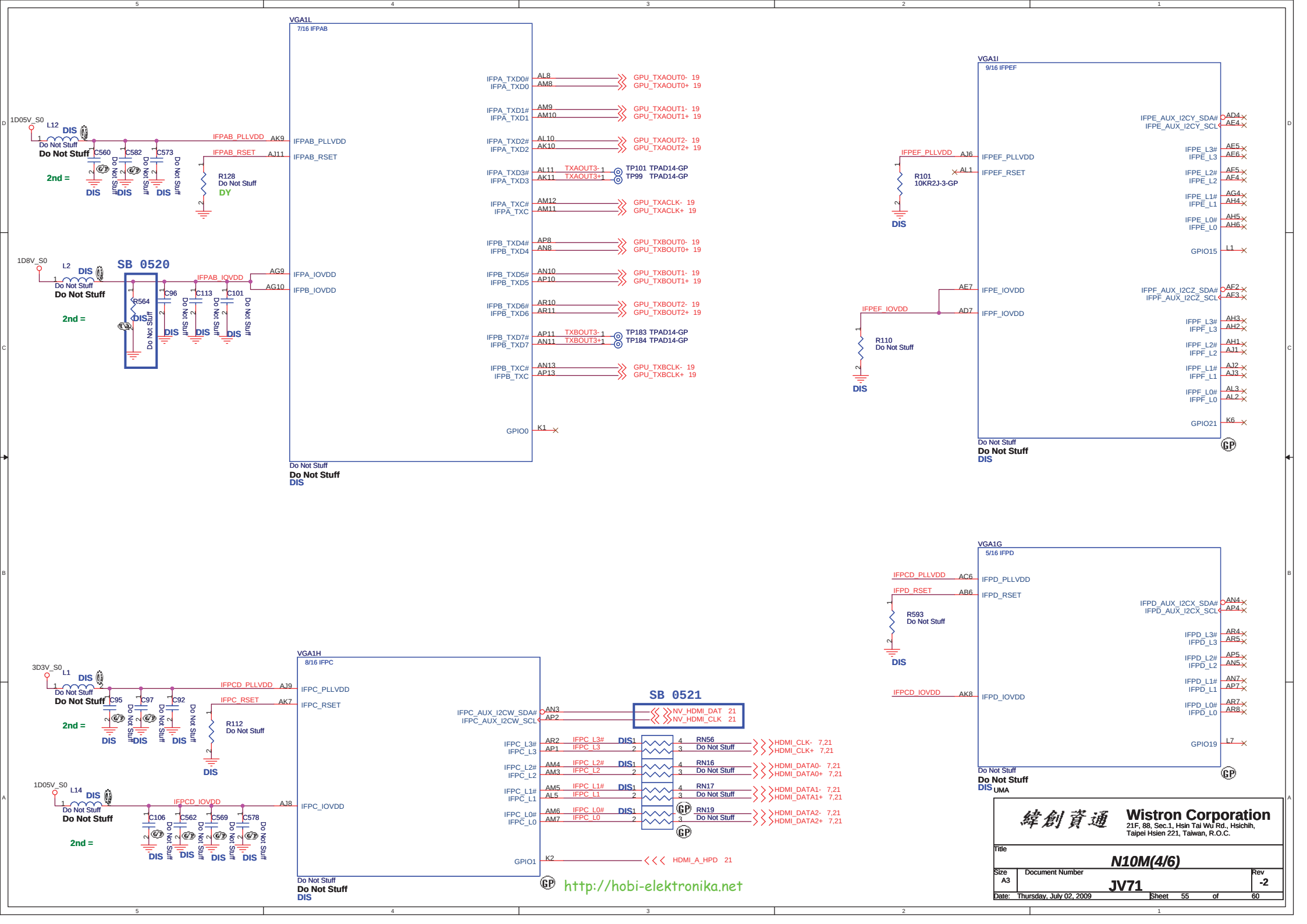

UMA

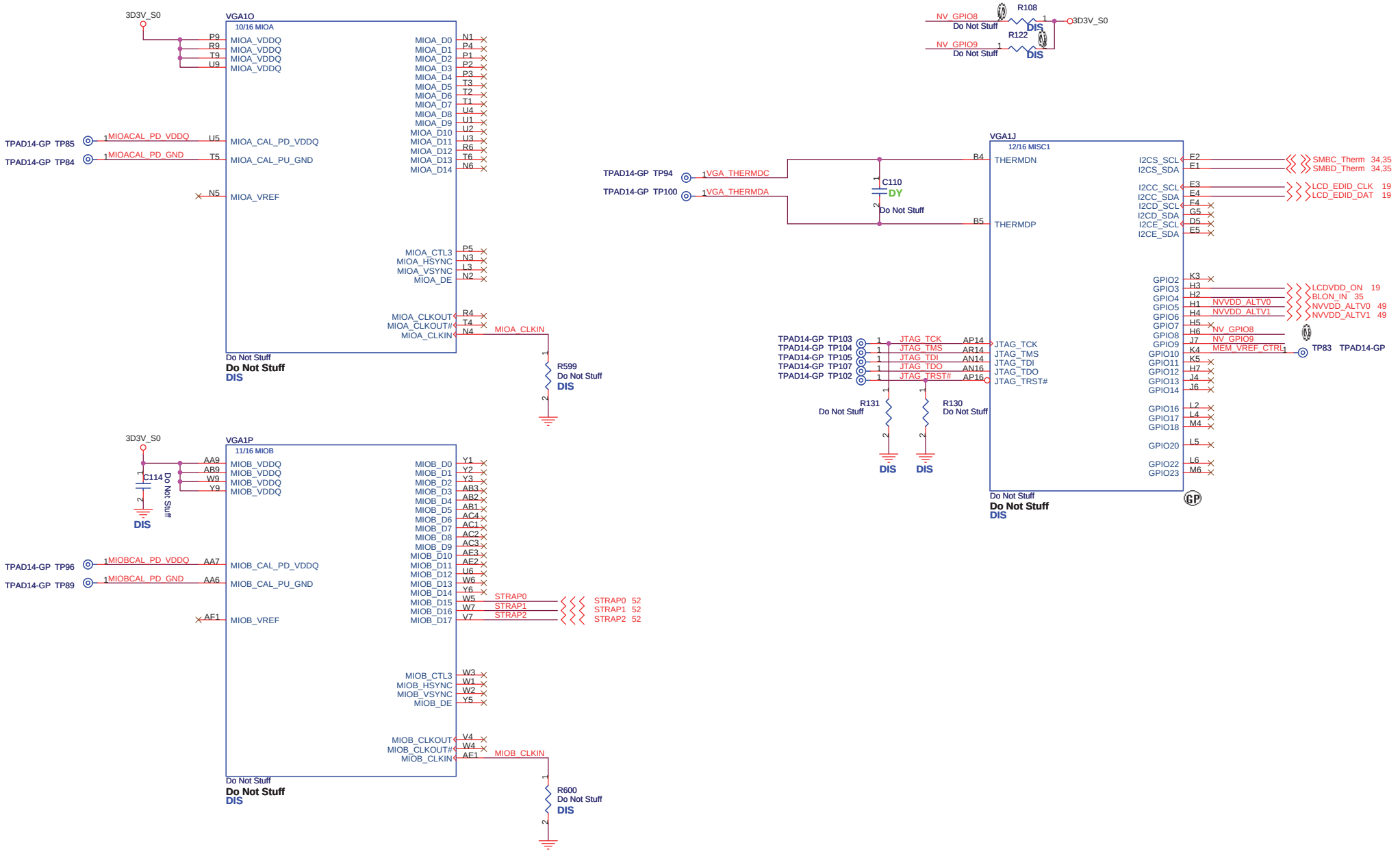
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: N10M(3/6) DAC

Size: A3 | Document Number: JV71 | Rev: -2

Date: Thursday, July 02, 2009 | Sheet 54 of 60


VGA1L
7/16 IFPAB
1D05V_S0
L12
DIS
Do Not Stuff
Do Not Stuff
C560
C582
C573
2nd =
DIS
IFPAB_PLLVDD
AK9
IFPAB_PLLVDD
IFPAB_RSET
AJ11
IFPAB_RSET
R128
Do Not Stuff
DY
1D8V_S0
L2
SB 0520
IFPAB_IOVDD
AG9
AG10
IFPA_IOVDD
IFPB_IOVDD
R564
C96
C113
C101
IFPA_TXD0#
IFPA_TXD0
AL8
AM8
GPU_TXAOUT0- 19
GPU_TXAOUT0+ 19
IFPA_TXD1#
IFPA_TXD1
AM9
AM10
GPU_TXAOUT1- 19
GPU_TXAOUT1+ 19
IFPA_TXD2#
IFPA_TXD2
AL10
AK10
GPU_TXAOUT2- 19
GPU_TXAOUT2+ 19
IFPA_TXD3#
IFPA_TXD3
AL11
AK11
TXAOUT3-
TXAOUT3+
TP101 TPAD14-GP
TP99 TPAD14-GP
IFPA_TXC#
IFPA_TXC
AM12
AM11
GPU_TXACLK- 19
GPU_TXACLK+ 19
IFPB_TXD4#
IFPB_TXD4
AP8
AN8
GPU_TXBOUT0- 19
GPU_TXBOUT0+ 19
IFPB_TXD5#
IFPB_TXD5
AN10
AP10
GPU_TXBOUT1- 19
GPU_TXBOUT1+ 19
IFPB_TXD6#
IFPB_TXD6
AR10
AR11
GPU_TXBOUT2- 19
GPU_TXBOUT2+ 19
IFPB_TXD7#
IFPB_TXD7
AP11
AN11
TXBOUT3-
TXBOUT3+
TP183 TPAD14-GP
TP184 TPAD14-GP
IFPB_TXC#
IFPB_TXC
AN13
AP13
GPU_TXBCLK- 19
GPU_TXBCLK+ 19
GPIO0
K1
Do Not Stuff
Do Not Stuff
DIS
VGA1I
9/16 IFPEF
IFPEF_PLLVDD
AJ6
IFPEF_PLLVDD
IFPEF_RSET
AL1
R101
10KR2J-3-GP
IFPEF_IOVDD
AE7
AD7
IFPE_IOVDD
IFPF_IOVDD
R110
Do Not Stuff
IFPE_AUX_I2CY_SDA#
IFPE_AUX_I2CY_SCL
AD4
AE4
IFPE_L3#
IFPE_L3
AE5
AE6
IFPE_L2#
IFPE_L2
AF5
AF4
IFPE_L1#
IFPE_L1
AG4
AH4
IFPE_L0#
IFPE_L0
AH5
AH6
GPIO15
L1
IFPF_AUX_I2CZ_SDA#
IFPF_AUX_I2CZ_SCL
AF2
AF3
IFPF_L3#
IFPF_L3
AH3
AH2
IFPF_L2#
IFPF_L2
AH1
AJ1
IFPF_L1#
IFPF_L1
AJ2
AJ3
IFPF_L0#
IFPF_L0
AL3
AL2
GPIO21
K6
Do Not Stuff
Do Not Stuff
DIS
VGA1H
8/16 IFPC
3D3V_S0
L1
DIS
Do Not Stuff
Do Not Stuff
C95
C97
C92
2nd =
DIS
IFPCD_PLLVDD
AJ9
IFPC_PLLVDD
IFPC_RSET
AK7
IFPC_RSET
R112
Do Not Stuff
1D05V_S0
L14
DIS
Do Not Stuff
Do Not Stuff
C106
C562
C569
C578
2nd =
DIS
IFPCD_IOVDD
AJ8
IFPC_IOVDD
SB 0521
IFPC_AUX_I2CW_SDA#
IFPC_AUX_I2CW_SCL
AN3
AP2
NV_HDMI_DAT 21
NV_HDMI_CLK 21
IFPC_L3#
IFPC_L3
AR2
AP1
IFPC_L2#
IFPC_L2
AM4
AM3
IFPC_L1#
IFPC_L1
AM5
AL5
IFPC_L0#
IFPC_L0
AM6
AM7
DIS1
RN56
RN16
RN17
RN19
Do Not Stuff
HDMI_CLK- 7,21
HDMI_CLK+ 7,21
HDMI_DATA0- 7,21
HDMI_DATA0+ 7,21
HDMI_DATA1- 7,21
HDMI_DATA1+ 7,21
HDMI_DATA2- 7,21
HDMI_DATA2+ 7,21
GPIO1
K2
HDMI_A_HPD 21
Do Not Stuff
Do Not Stuff
DIS
VGA1G
5/16 IFPD
IFPCD_PLLVDD
AC6
IFPD_PLLVDD
IFPD_RSET
AB6
IFPD_RSET
R593
Do Not Stuff
IFPCD_IOVDD
AK8
IFPD_IOVDD
IFPD_AUX_I2CX_SDA#
IFPD_AUX_I2CX_SCL
AN4
AP4
IFPD_L3#
IFPD_L3
AR4
AR5
IFPD_L2#
IFPD_L2
AP5
AN5
IFPD_L1#
IFPD_L1
AN7
AP7
IFPD_L0#
IFPD_L0
AR7
AR8
GPIO19
L7
Do Not Stuff
Do Not Stuff
DIS
UMA
http://hobi-elektronika.net
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N10M(4/6)
Size
A3
Document Number
JV71
Rev
-2
Date: Thursday, July 02, 2009
Sheet 55 of 60





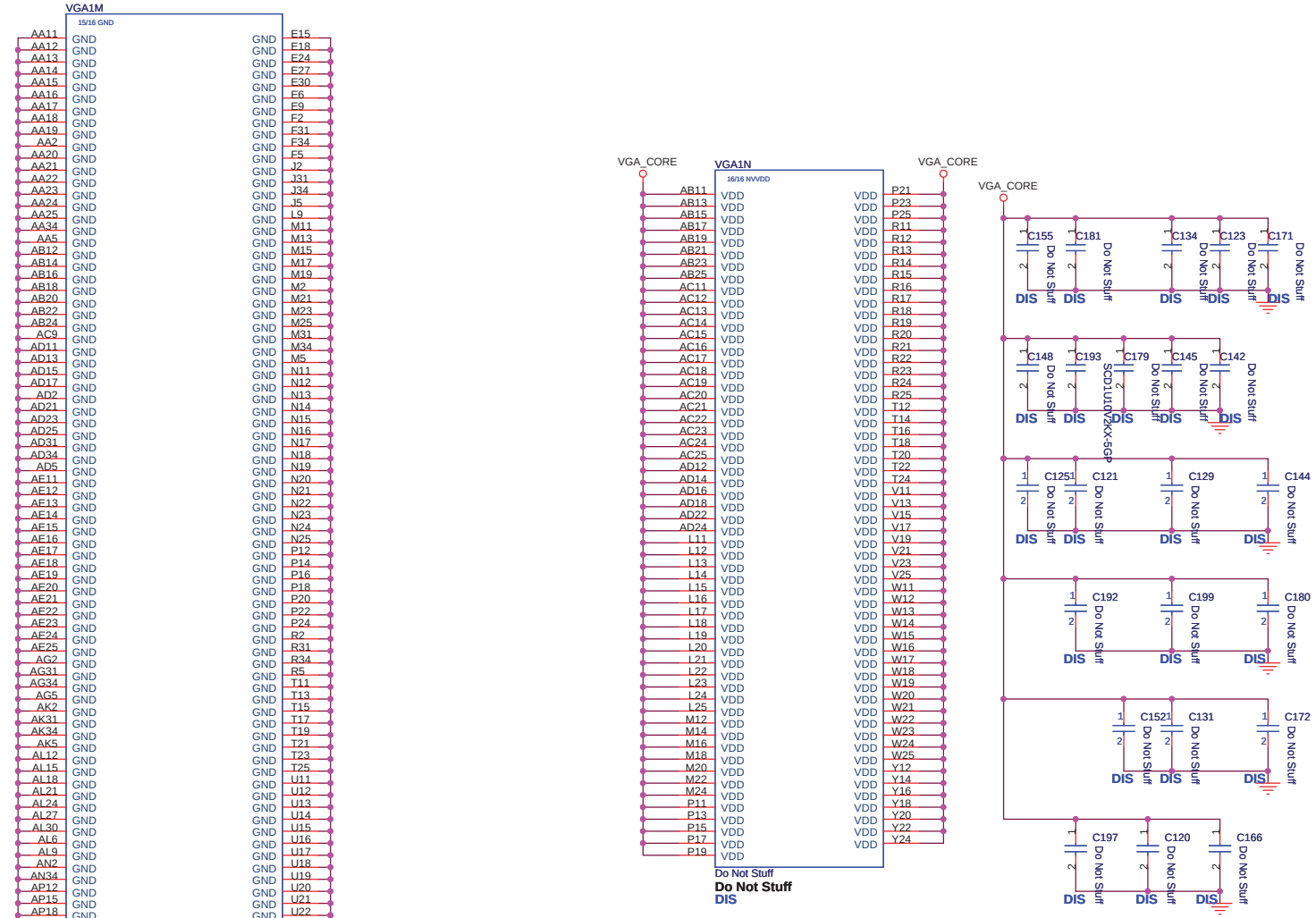

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***N10M(5/6) MIO/ GPIO***

| Size | Document Number | Rev |
|---|---|---|
| A3 | JV71 | -2 |

Date: Thursday, July 02, 2009 Sheet 56 of 60





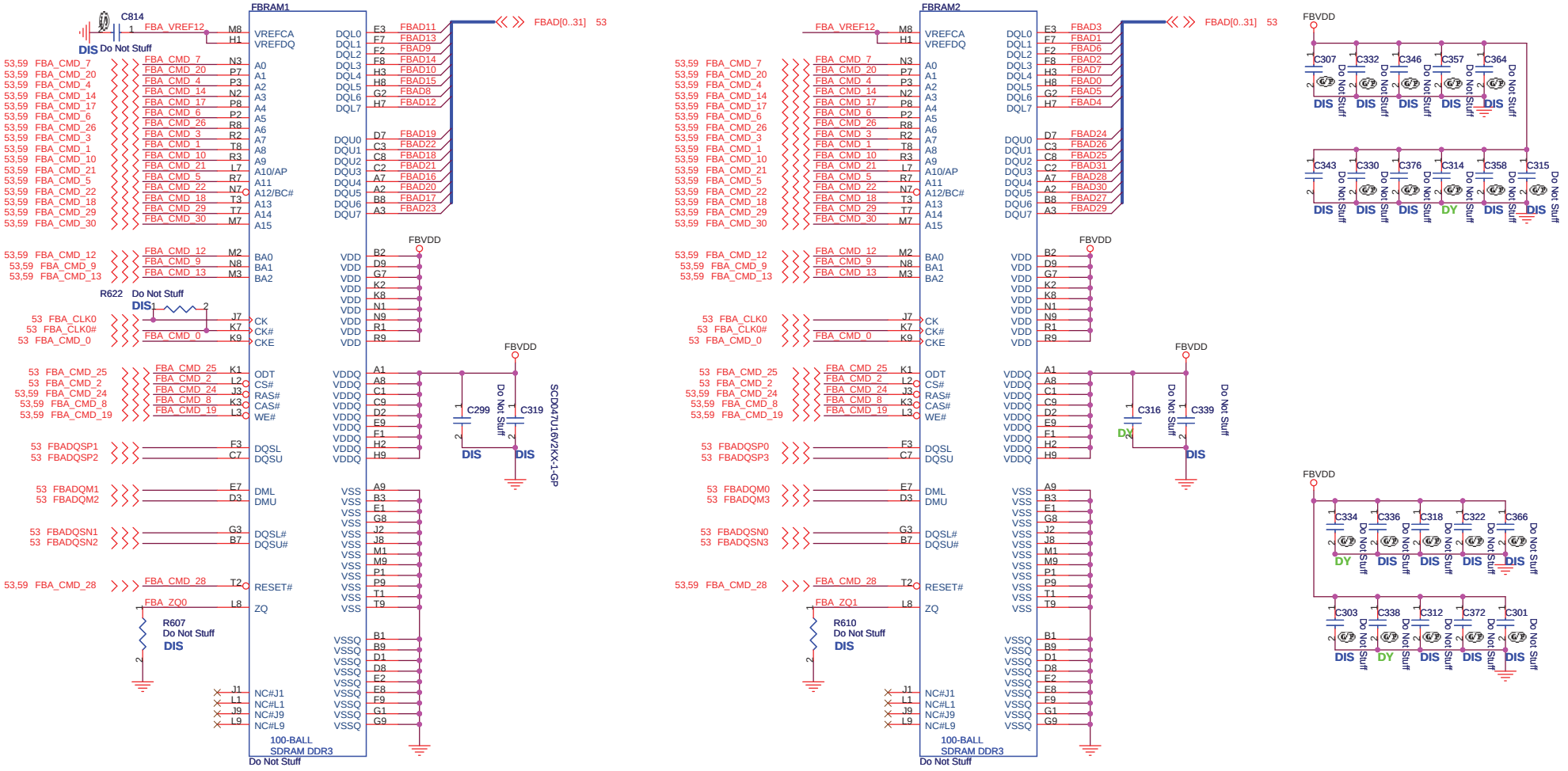

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **N10M(6/6) POWER**

| Size | Document Number | Rev |
|---|---|---|
| A3 | JV71 | -2 |

Date: Thursday, July 02, 2009 Sheet 57 of 60




**FB CMD mapping Mode C-N10M**
**<Mirror Mode>**

**DDR3 Power consumption 1.5V@800MHz**
**Hynix :IDD4W=220.4mA**
**Samsung :IDD7=150.4mA (calcurated)**



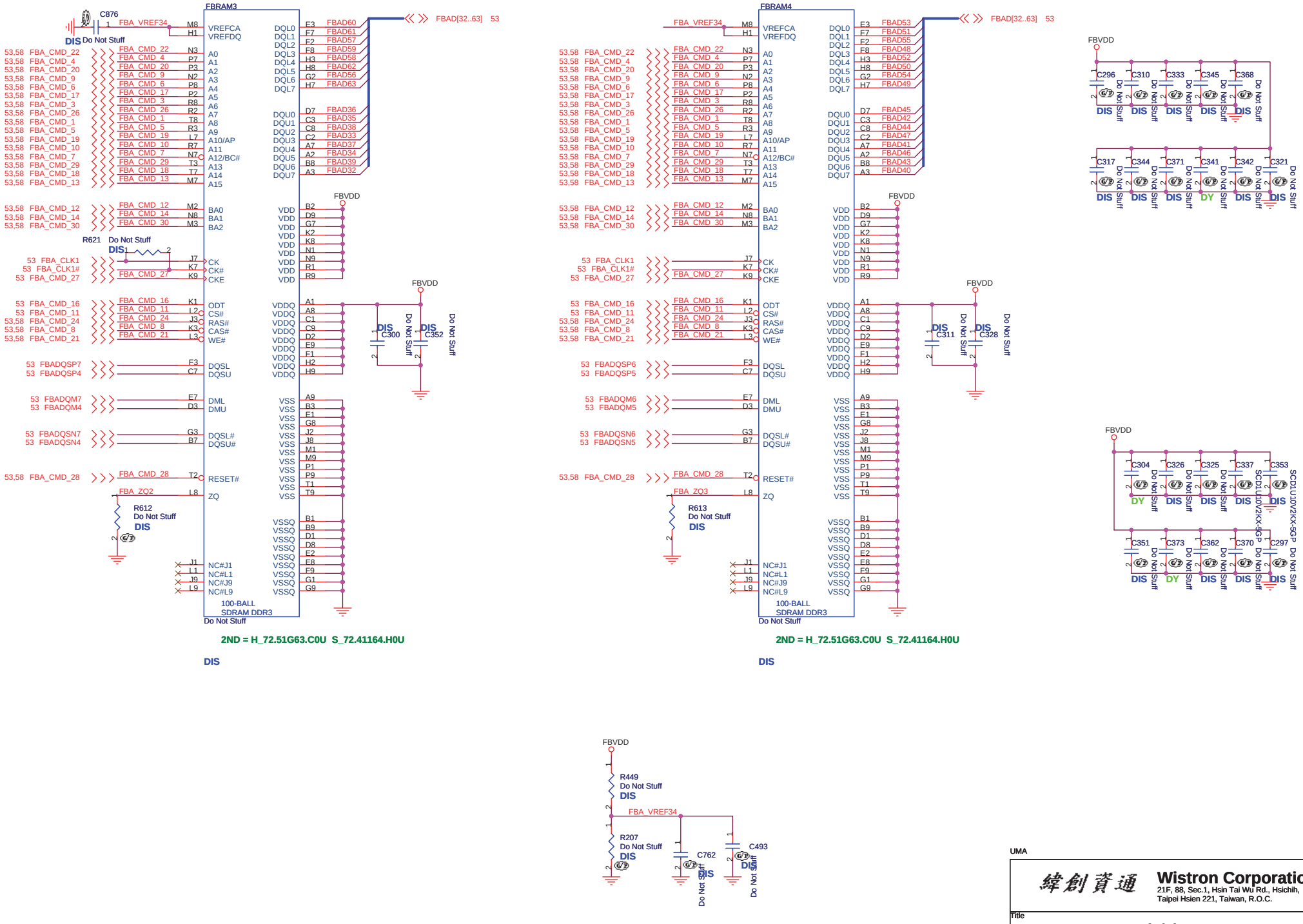
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM(1/2)***

| Size | Document Number | Rev |
|---|---|---|
| A3 | JV71 | -2 |

Date: Thursday, July 02, 2009 Sheet 58 of 60



SA SB SC -1



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HISTORY***

| Size | Document Number | Rev |
|---|---|---|
| A2 | JV71 | -2 |

Date: Thursday, July 02, 2009 Sheet 60 of 60