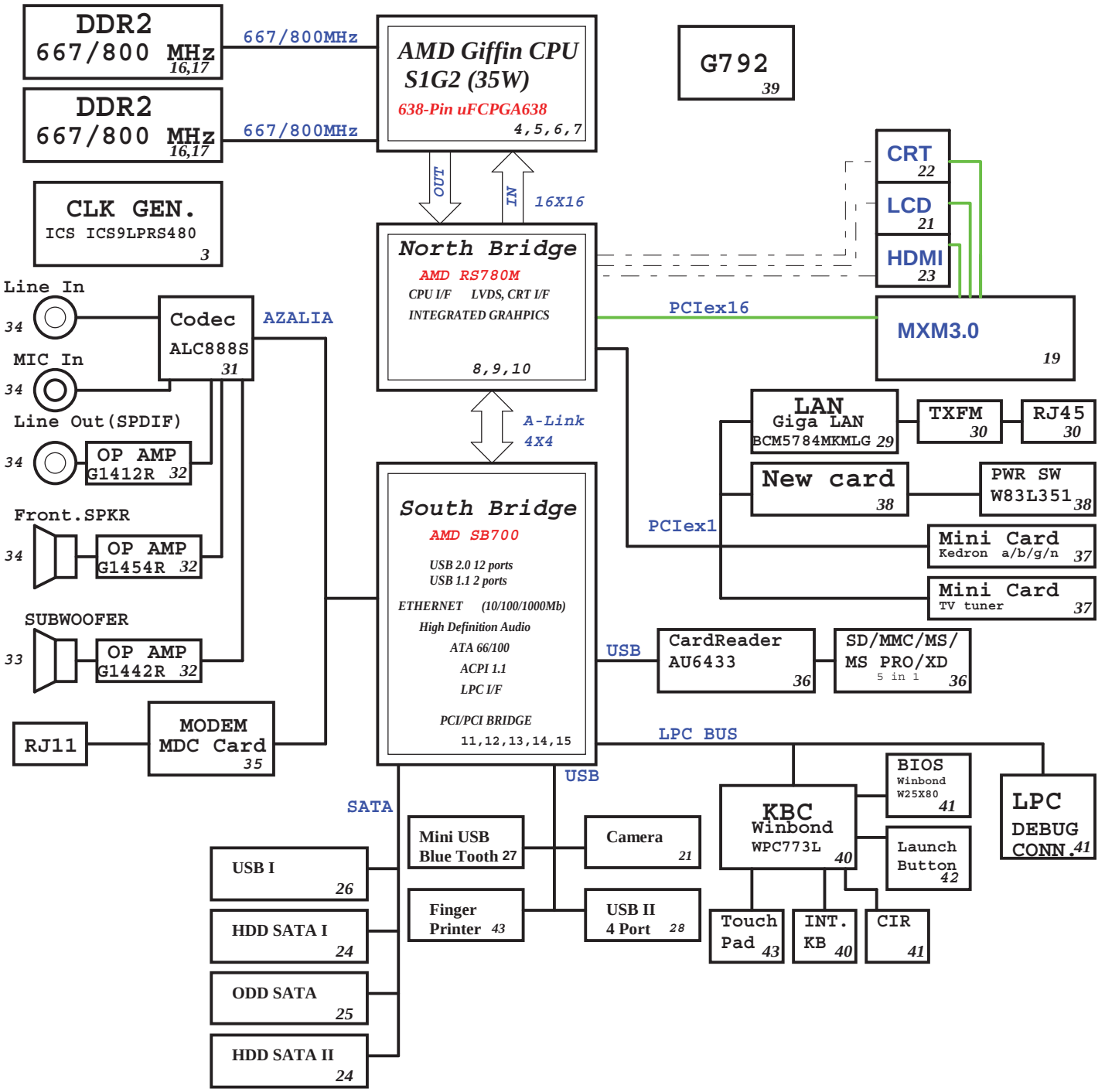
JM70-PU (AS 17") Block Diagram

Project code: 91.4CE01.001
PCB P/N : 48.4CE01.0SC
REVISION : 08255-SC



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 49

INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)

SYSTEM DC/DC TPS51124 50

INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(8A) 1D2V_S0(5A)

SYSTEM DC/DC TPS51117 52

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(10A)

RT9026PFP 51

1D8V_S3	DDR_VREF_S3 0D9V_S3(1A)

RT9166 51

3D3V_S0	2D5V_S0 (300mA)

G957 51

3D3V_S0	1D5V_S0(1A)

G9161(UMA) 51

3D3V_S5	1D2V_S5 (400mA)

G9131(DIS) 51

3D3V_S5	1D2V_S5 (300mA)

CHARGER MAX8731A 53

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 48

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: JM70-PU | Rev: -2
Date: Monday, March 02, 2009 | Sheet 1 of 56

<Core Design>

緯創資通 **Wistron Corporation**

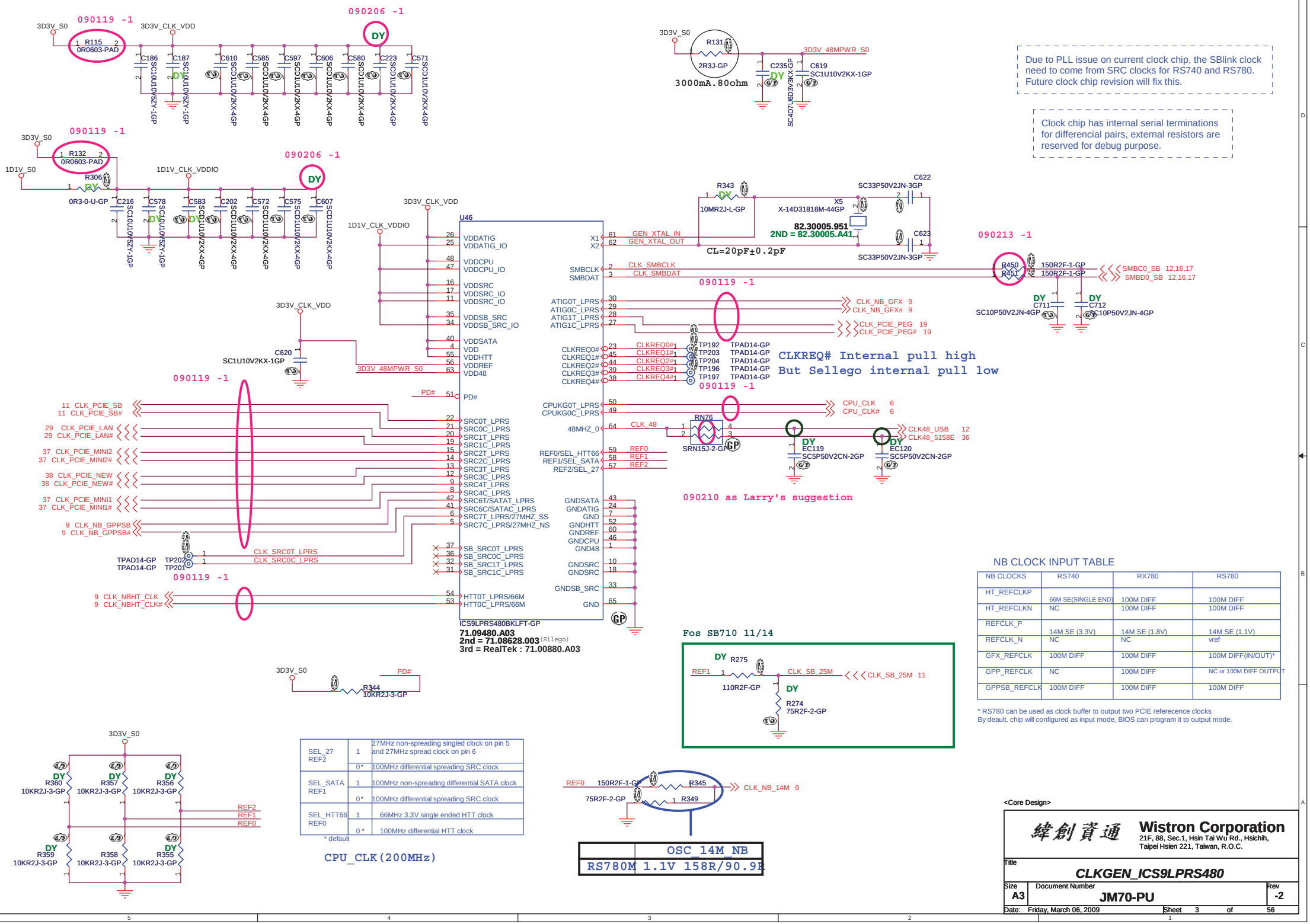
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY

Size	Document Number	Rev
A3	JM70-PU	-2

Date: Monday, March 02, 2009 Sheet 2 of 56



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

<Core Design>

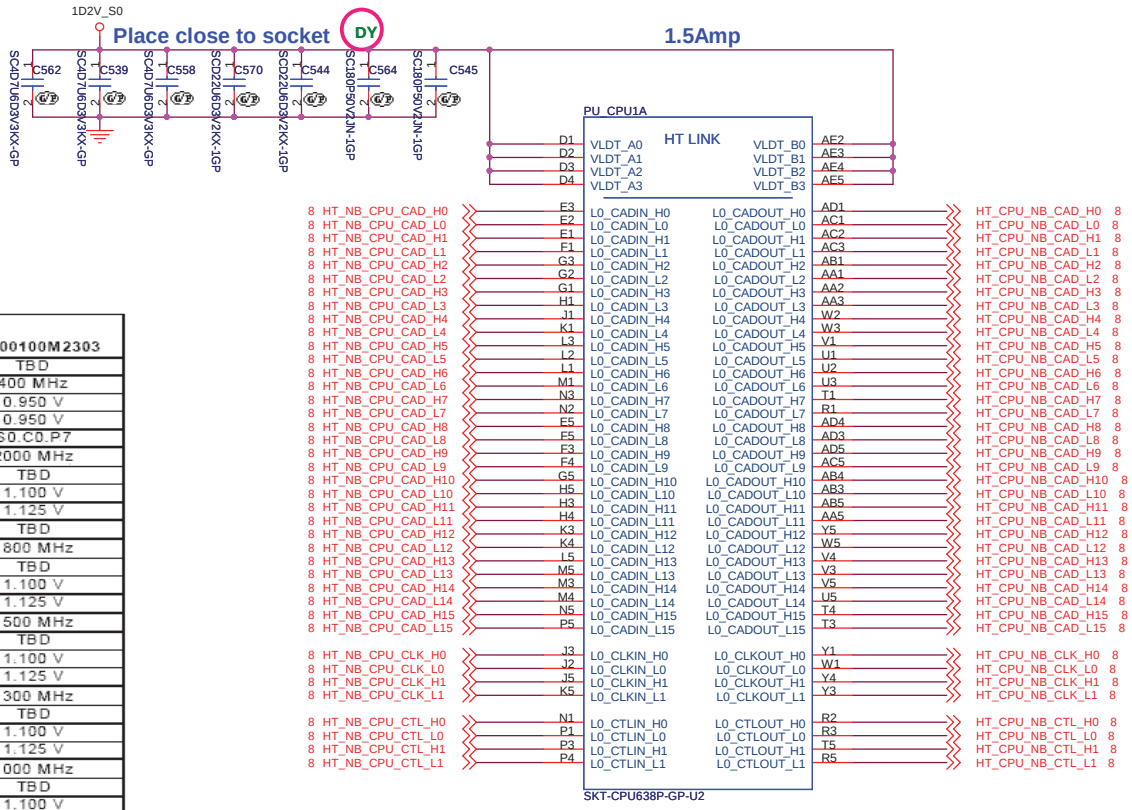
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS9LPRS480

Size: A3 | Document Number: JM70-PU | Rev: -2

Date: Friday, March 06, 2009 | Sheet 3 of 56

090206 -1



62.10055.111
2ND = 62.10055.251

090109 SC

SKT-BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_HT_LINK I/F_(1/4)

Size	Document Number	Rev
A3	JM70-PU	-2

Date: Friday, March 06, 2009 Sheet 4 of 56

090206 -1

Place near to CPU

4.7u x 4 | 0.22u X 2 | 180P x 6

C215 SC4D7U6D3V3KX-GP
C600 SC4D7U6D3V3KX-GP
C203 SC4D7U6D3V3KX-GP
C204 SC4D7U6D3V3KX-GP
C212 SCD22U6D3V2KX-1GP
C208 SCD22U6D3V2KX-1GP
C210 SC180P50V2JN-1GP
C211 SC180P50V2JN-1GP
C206 SC180P50V2JN-1GP
C213 SC180P50V2JN-1GP
C209 SC180P50V2JN-1GP
C207 SC180P50V2JN-1GP

CLOSE TO CPU

1D8V_S3
C250 SCD1U10V2KX-4GP
VREF_DDR_CLAW
RN20 SRN1KJ-7-GP
C246 SC1KP50V2KX-1GP
C240 SCD1U10V2KX-4GP

0D9V_S3

R376 39D2R2F-L-GP
R379 39D2R2F-L-GPTP137

MEMZP
MEMZN
MEM_RSVD_M1
VTT_SENSE → TP132TPAD14-GP
MEM_RSVD_M2 → TP138

PU_CPU1B

MEM:CMD/CTRL/CLK

D10	VTT1	VTT5	W10
C10	VTT2	VTT6	AC10
B10	VTT3	VTT7	AB10
AD10	VTT4	VTT8	AA10
		VTT9	A10
AE10	MEMZP		
AE10	MEMZN	VTT_SENSE	Y10
H16	RSVD_M1	MEMVREF	W17
		RSVD_M2	B18

T19	MA0_ODT0	MB0_ODT0	W26
V22	MA0_ODT1	MB0_ODT1	W23
U21	MA1_ODT0	MB1_ODT0	Y26
V19	MA1_ODT1		
T20	MA0_CS_L0	MB0_CS_L0	V26
U19	MA0_CS_L1	MB0_CS_L1	W25
U20	MA1_CS_L0	MB1_CS_L0	U22
V20	MA1_CS_L1		
J22	MA_CKE0	MB_CKE0	J25
J20	MA_CKE1	MB_CKE1	H26
N19	MA_CLK_H5	MB_CLK_H5	P22
N20	MA_CLK_L5	MB_CLK_L5	R22
E16	MA_CLK_H1	MB_CLK_H1	A17
F16	MA_CLK_L1	MB_CLK_L1	A18
Y16	MA_CLK_H7	MB_CLK_H7	AF18
AA16	MA_CLK_L7	MB_CLK_L7	AF17
P19	MA_CLK_H4	MB_CLK_H4	R26
P20	MA_CLK_L4	MB_CLK_L4	R25

N21	MA_ADD0	MB_ADD0	P24
M20	MA_ADD1	MB_ADD1	N24
N22	MA_ADD2	MB_ADD2	P26
M19	MA_ADD3	MB_ADD3	N23
M22	MA_ADD4	MB_ADD4	N26
L20	MA_ADD5	MB_ADD5	L23
M24	MA_ADD6	MB_ADD6	N25
L21	MA_ADD7	MB_ADD7	L24
L19	MA_ADD8	MB_ADD8	M26
K22	MA_ADD9	MB_ADD9	K26
R21	MA_ADD10	MB_ADD10	T26
L22	MA_ADD11	MB_ADD11	L26
K20	MA_ADD12	MB_ADD12	L25
V24	MA_ADD13	MB_ADD13	W24
K24	MA_ADD14	MB_ADD14	J23
K19	MA_ADD15	MB_ADD15	J24

R20	MA_BANK0	MB_BANK0	R24
R23	MA_BANK1	MB_BANK1	U26
J21	MA_BANK2	MB_BANK2	J26
R19	MA_RAS_L	MB_RAS_L	U25
T22	MA_CAS_L	MB_CAS_L	U24
T24	MA_WE_L	MB_WE_L	U23

SKT-CPU638P-GP-U2

62.10055.111
2ND = 62.10055.251
090109 SC

PU_CPU1C

MEM:DATA

G12	MA_DATA0	MB_DATA0	C11
F12	MA_DATA1	MB_DATA1	A11
H14	MA_DATA2	MB_DATA2	A14
G14	MA_DATA3	MB_DATA3	B14
H11	MA_DATA4	MB_DATA4	G11
H12	MA_DATA5	MB_DATA5	E11
C13	MA_DATA6	MB_DATA6	D12
E13	MA_DATA7	MB_DATA7	A13
H15	MA_DATA8	MB_DATA8	A15
E15	MA_DATA9	MB_DATA9	A16
E17	MA_DATA10	MB_DATA10	A19
H17	MA_DATA11	MB_DATA11	A20
E14	MA_DATA12	MB_DATA12	C14
F14	MA_DATA13	MB_DATA13	D14
C17	MA_DATA14	MB_DATA14	C18
G17	MA_DATA15	MB_DATA15	D18
G18	MA_DATA16	MB_DATA16	D20
C19	MA_DATA17	MB_DATA17	A21
D22	MA_DATA18	MB_DATA18	D24
E20	MA_DATA19	MB_DATA19	C25
E18	MA_DATA20	MB_DATA20	B20
F18	MA_DATA21	MB_DATA21	C20
B22	MA_DATA22	MB_DATA22	B24
C23	MA_DATA23	MB_DATA23	C24
F20	MA_DATA24	MB_DATA24	E23
F22	MA_DATA25	MB_DATA25	E24
H24	MA_DATA26	MB_DATA26	G25
J19	MA_DATA27	MB_DATA27	G26
E21	MA_DATA28	MB_DATA28	C26
E22	MA_DATA29	MB_DATA29	D26
H20	MA_DATA30	MB_DATA30	G23
H22	MA_DATA31	MB_DATA31	G24
Y24	MA_DATA32	MB_DATA32	AA24
AB24	MA_DATA33	MB_DATA33	AA23
AB22	MA_DATA34	MB_DATA34	AD24
AA21	MA_DATA35	MB_DATA35	AE24
W22	MA_DATA36	MB_DATA36	AA26
W21	MA_DATA37	MB_DATA37	AA25
Y22	MA_DATA38	MB_DATA38	AD26
AA22	MA_DATA39	MB_DATA39	AE25
Y20	MA_DATA40	MB_DATA40	AC22
AA20	MA_DATA41	MB_DATA41	AD22
AA18	MA_DATA42	MB_DATA42	AE20
AB18	MA_DATA43	MB_DATA43	AF20
AB21	MA_DATA44	MB_DATA44	AF24
AD21	MA_DATA45	MB_DATA45	AF23
AD19	MA_DATA46	MB_DATA46	AC20
Y18	MA_DATA47	MB_DATA47	AD20
AD17	MA_DATA48	MB_DATA48	AD18
W16	MA_DATA49	MB_DATA49	AE18
W14	MA_DATA50	MB_DATA50	AC14
Y14	MA_DATA51	MB_DATA51	AD14
Y17	MA_DATA52	MB_DATA52	AF19
AB17	MA_DATA53	MB_DATA53	AC18
AB15	MA_DATA54	MB_DATA54	AF16
AD15	MA_DATA55	MB_DATA55	AF15
AB13	MA_DATA56	MB_DATA56	AF13
AD13	MA_DATA57	MB_DATA57	AC12
Y12	MA_DATA58	MB_DATA58	AB11
W11	MA_DATA59	MB_DATA59	Y11
AB14	MA_DATA60	MB_DATA60	AE14
AA14	MA_DATA61	MB_DATA61	AE14
AB12	MA_DATA62	MB_DATA62	AF11
AA12	MA_DATA63	MB_DATA63	AD11

E12	MA_DM0	MB_DM0	A12
C15	MA_DM1	MB_DM1	B16
E19	MA_DM2	MB_DM2	A22
F24	MA_DM3	MB_DM3	E25
AC24	MA_DM4	MB_DM4	AB26
Y19	MA_DM5	MB_DM5	AE22
AB16	MA_DM6	MB_DM6	AC16
Y13	MA_DM7	MB_DM7	AD12

G13	MA_DQS_H0	MB_DQS_H0	C12
H13	MA_DQS_L0	MB_DQS_L0	B12
G16	MA_DQS_H1	MB_DQS_H1	D16
G15	MA_DQS_L1	MB_DQS_L1	C16
C22	MA_DQS_H2	MB_DQS_H2	A24
C21	MA_DQS_L2	MB_DQS_L2	A23
G22	MA_DQS_H3	MB_DQS_H3	F26
G21	MA_DQS_L3	MB_DQS_L3	E26
AD23	MA_DQS_H4	MB_DQS_H4	AC25
AC23	MA_DQS_L4	MB_DQS_L4	AC26
AB19	MA_DQS_H5	MB_DQS_H5	AF21
AB20	MA_DQS_L5	MB_DQS_L5	AE22
Y15	MA_DQS_H6	MB_DQS_H6	AE16
W15	MA_DQS_L6	MB_DQS_L6	AD16
W12	MA_DQS_H7	MB_DQS_H7	AE12
W13	MA_DQS_L7	MB_DQS_L7	AE12

SKT-CPU638P-GP-U2

62.10055.111
2ND = 62.10055.251
<Core Design>
090109 SC

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size	Document Number	Rev
A3	JM70-PU	-2

Date: Friday, March 06, 2009 Sheet 5 of 56

LYAOUT:ROUTE VDDA TRACE APPROX.
40 mils WIDE
(USE 2X25 mil TRACES TO EXIT BALL FIELD)
& 500 mils LONG.

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

090206 -1

090119 -1

SB with 0402 PAD

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

081223 SC

Near CPU PIN

CPU exceeds to 125℃

2ND = 84.03904.L06

2ND = 62.10055.251

090109 SC

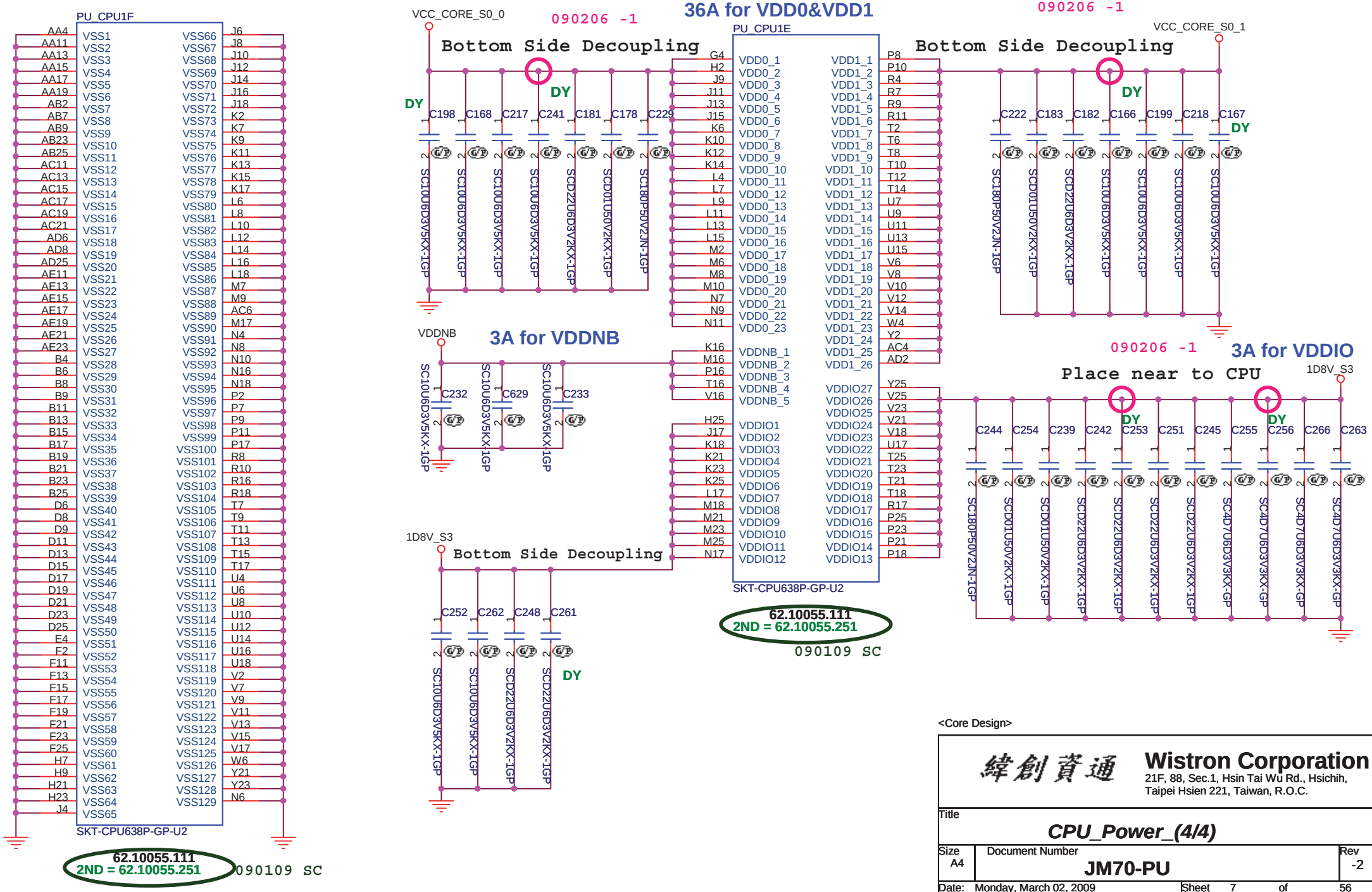
090113 -1

HDT Connectors

SMC-CONN26A-FP

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU_Control&Debug_(3/4)		
Size: A3	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 6 of 56	


PU_CPU1F
SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10055.251
090109 SC
VCC_CORE_S0_0
090206 -1
Bottom Side Decoupling
DY
C198 C168 C217 C241 C181 C178 C229
SC10U6D3V5KX-1GP
SCD22U6D3V2KX-1GP
SCD01U50V2KX-1GP
SC180P50V2JN-1GP
36A for VDD0&VDD1
PU_CPU1E
SKT-CPU638P-GP-U2
62.10055.111
2ND = 62.10055.251
090109 SC
VCC_CORE_S0_1
090206 -1
Bottom Side Decoupling
C222 C183 C182 C166 C199 C218 C167
VDDNB
3A for VDDNB
C232 C629 C233
1D8V_S3
Bottom Side Decoupling
C252 C262 C248 C261
090206 -1
3A for VDDIO
Place near to CPU
C244 C254 C239 C242 C253 C251 C245 C255 C256 C266 C263
SC4D7U6D3V3KX-GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU_Power_(4/4)
Size A4
Document Number
JM70-PU
Rev -2
Date: Monday, March 02, 2009
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PU_NB1A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

RS780M-GP-U2

Place < 100mils from pin C23 and A24

Place < 100mils from pin B25 and B24

PU_NB1B

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS780M-GP-U2

PCIE As SW request 11/17
Port 1 => Onboard LAN
Port 2 => Mini Card WLAN
Port 3 => Mini Card#2
Port 4 => New Card
Port 5,6 => NC

090119 -1

LAN
MINICARD
MINICARD TV
NEW CARD

A-LINK

Place < 100mils from pin AC8 and AB8

RS780M Display Port Support(muxed on GFX)

DP0	GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1	GFX_TX4,TX5,TX6,TX7,AUX1,HPD1

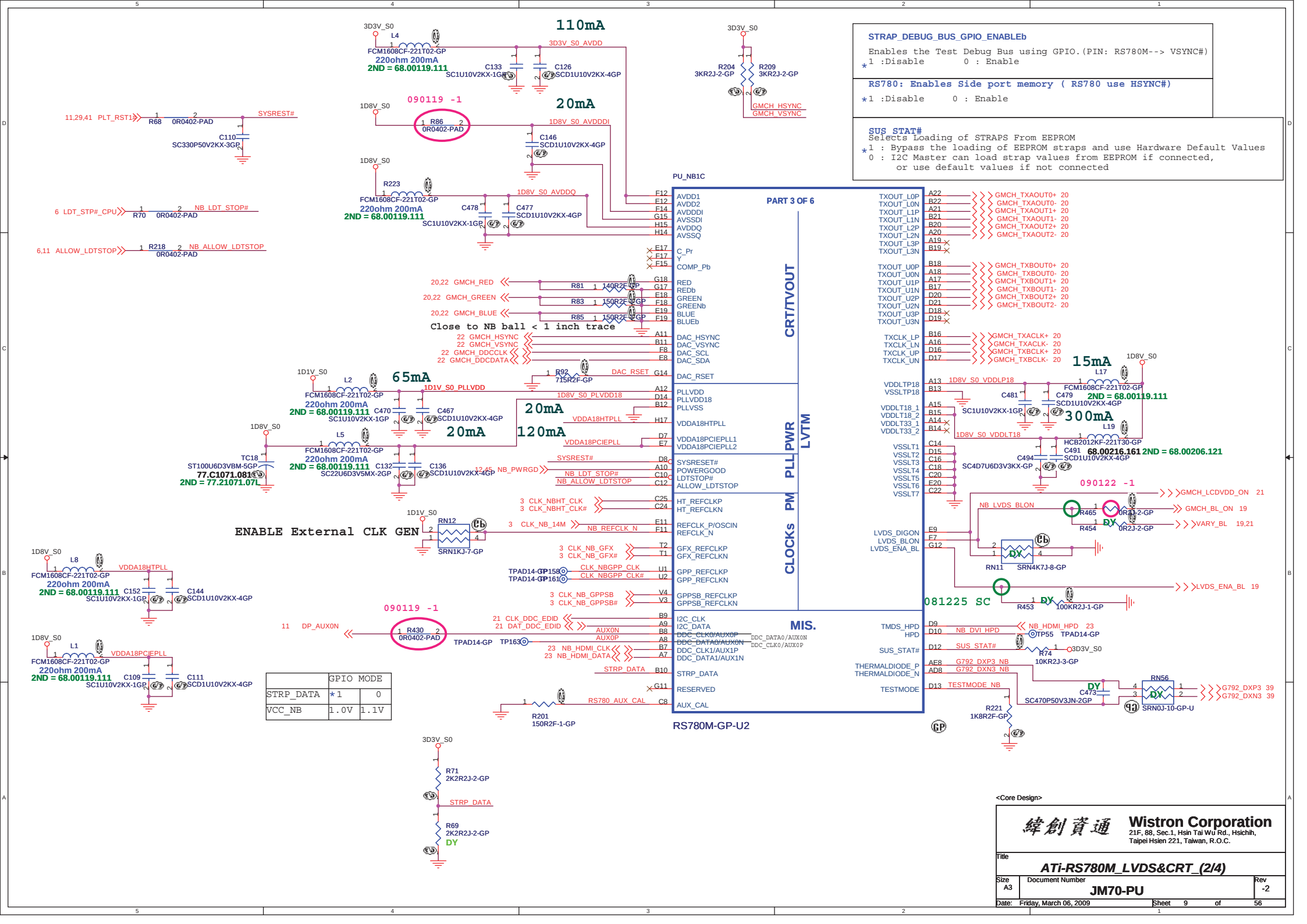
<Core Design>

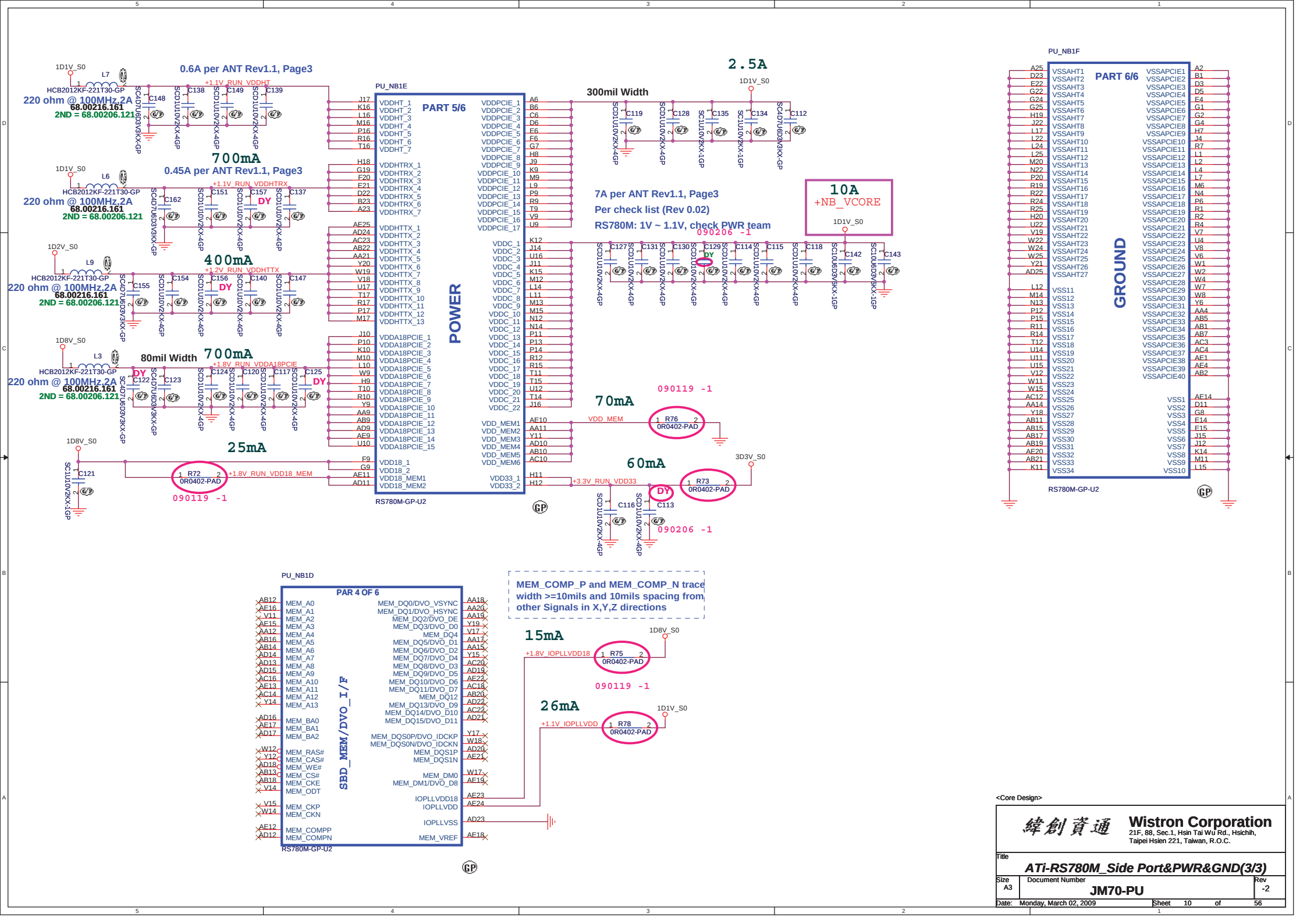
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_HT LINK&PCIe(1/3)

Size: A3 | Document Number: JM70-PU | Rev: -2

Date: Friday, March 06, 2009 | Sheet 8 of 56


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
PU_NB1C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
PWR
LVTM
PLL
PM
CLOCKs
MIS.
Close to NB ball < 1 inch trace
ENABLE External CLK GEN
110mA
20mA
65mA
120mA
15mA
300mA
090119 -1
090122 -1
081225 SC
GPIO MODE
STRP_DATA *1 0
VCC_NB 1.0V 1.1V
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_LVDS&CRT_(2/4)
Size A3
Document Number JM70-PU
Rev -2
Date: Friday, March 06, 2009
Sheet 9 of 56



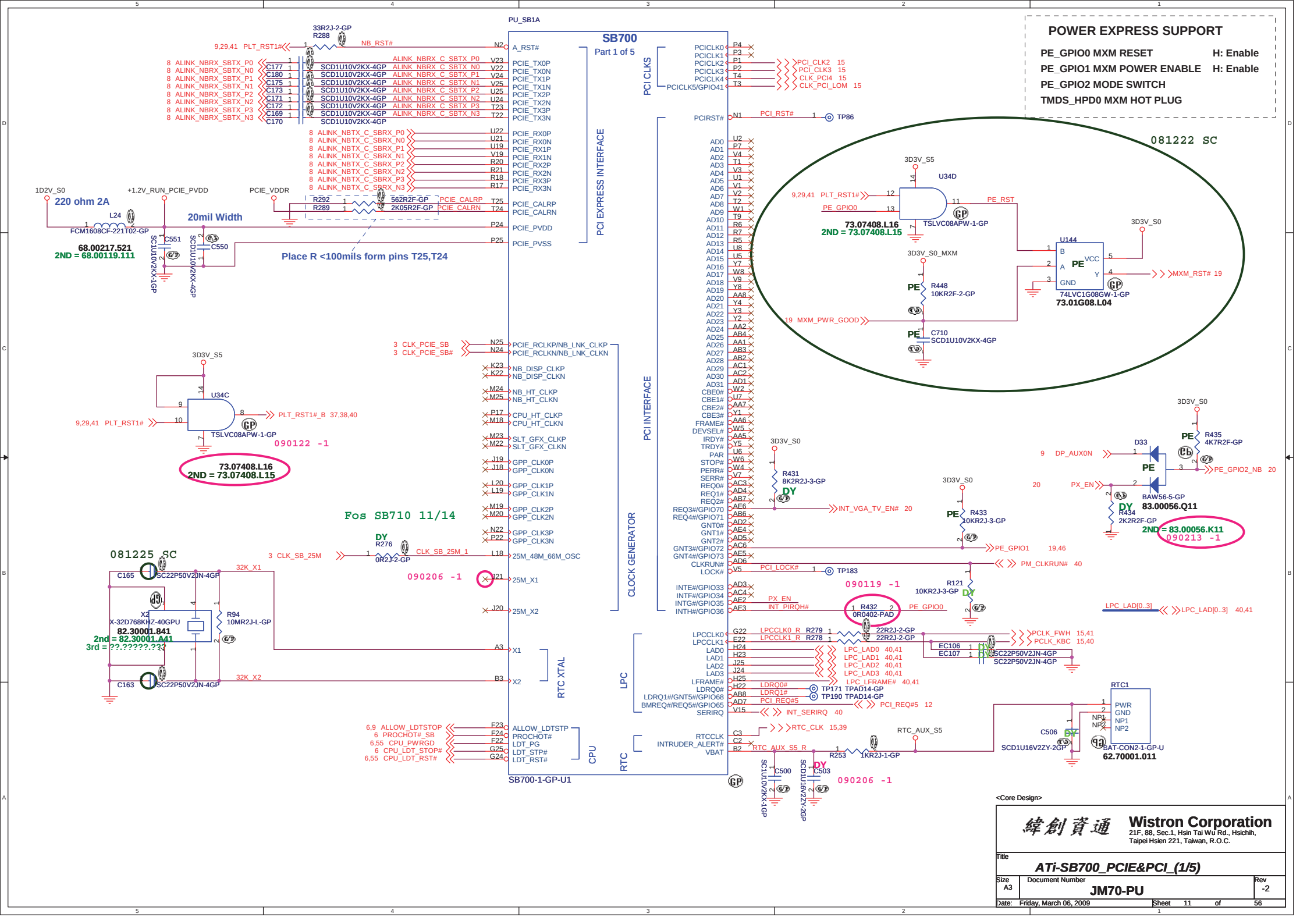
<Core Design>

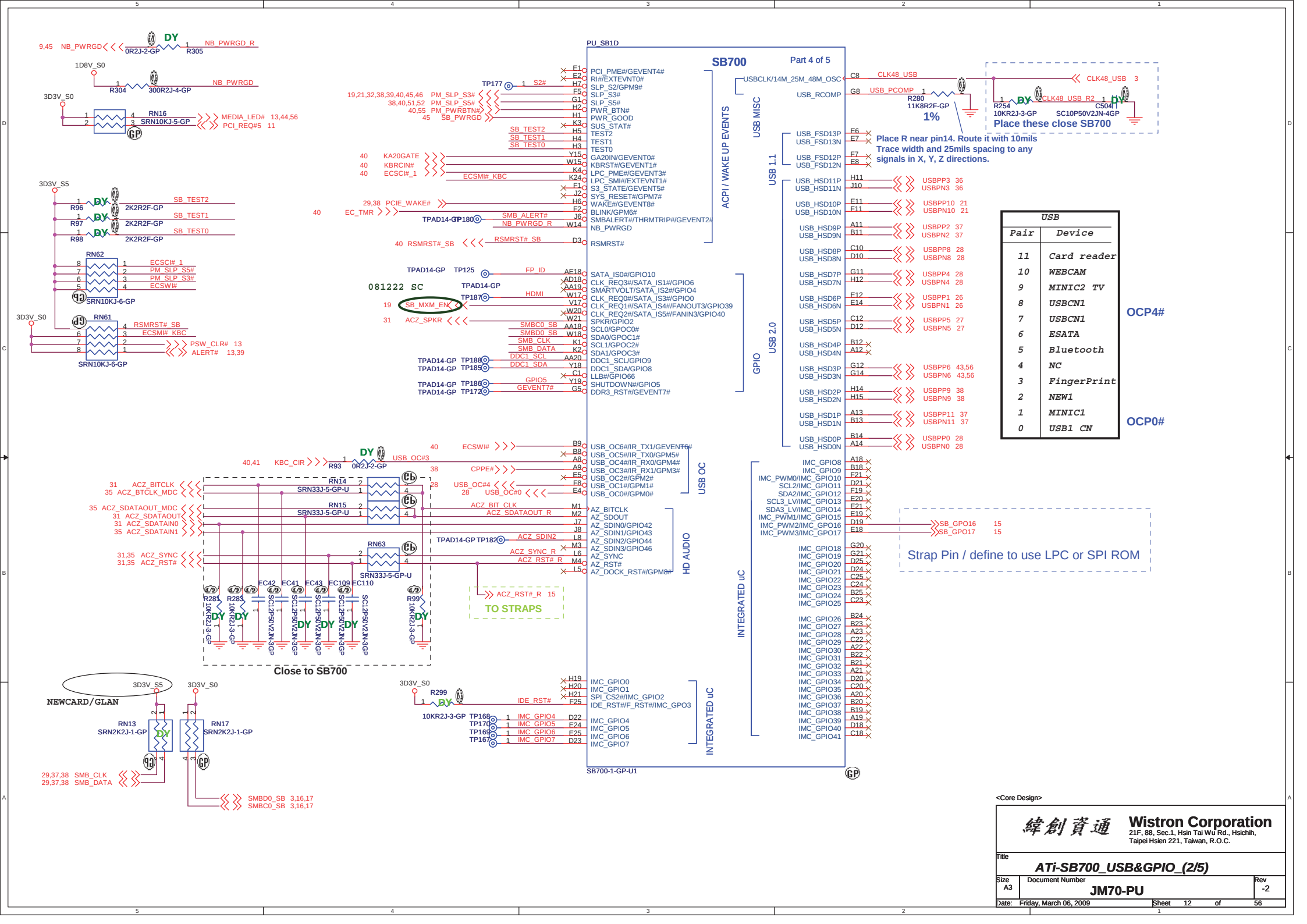
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

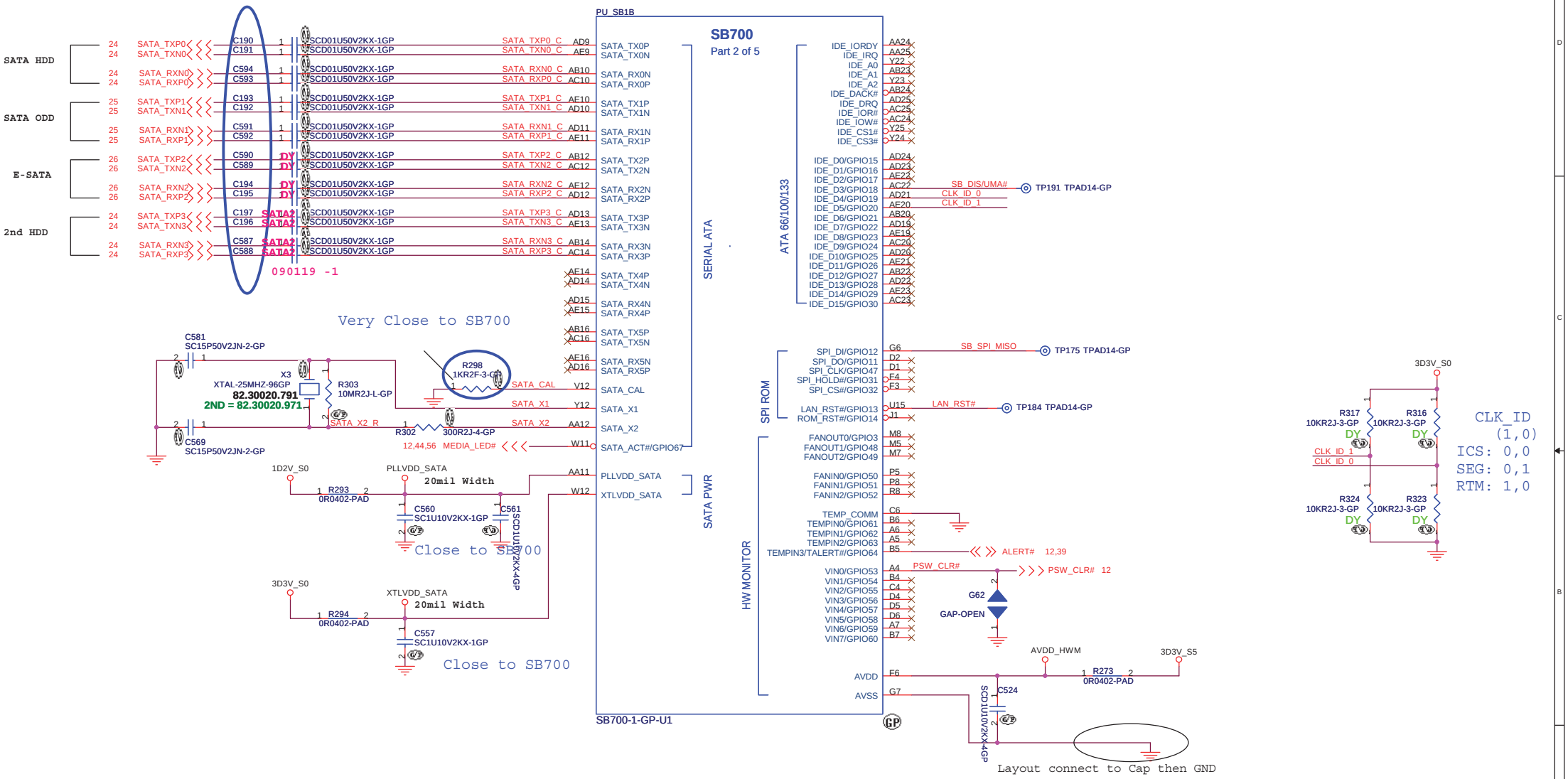
Title: ATi-RS780M_Side Port&PWR&GND(3/3)

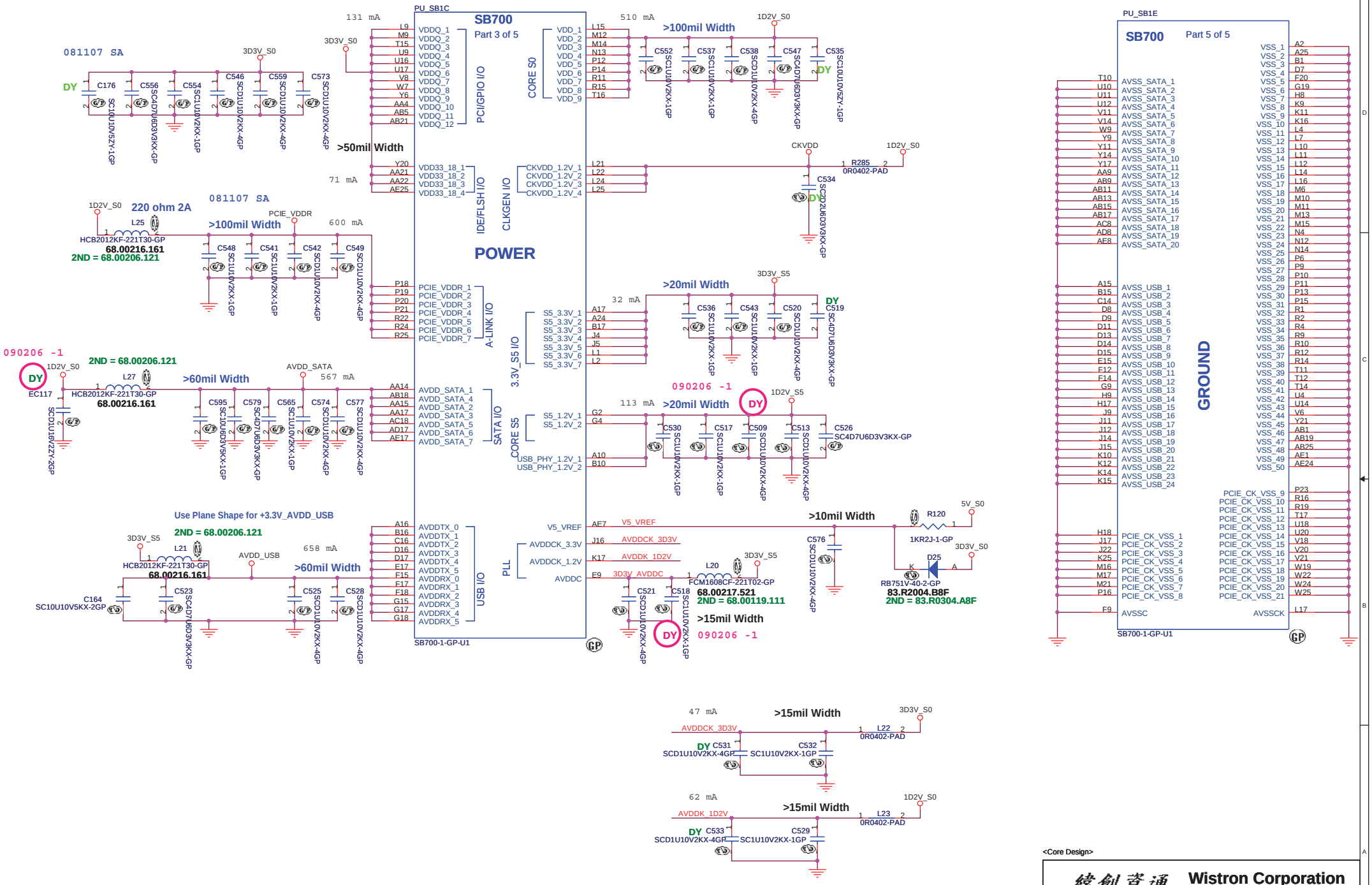
Size	Document Number	Rev
A3	JM70-PU	-2

Date: Monday, March 02, 2009 Sheet 10 of 56


POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMDS_HPD0 MXM HOT PLUG
SB700
Part 1 of 5
PU_SB1A
SB700-1-GP-U1
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
081222 SC
081225 SC
090122 -1
090206 -1
090119 -1
090213 -1
Fos SB710 11/14
220 ohm 2A
20mil Width
Place R <100mils form pins T25,T24
73.07408.L16
2ND = 73.07408.L15
68.00217.521
2ND = 68.00119.111
82.30001.841
2nd = 82.30001.A41
3rd = ??.?????.???
73.01G08.L04
83.00056.Q11
2ND = 83.00056.K11
62.70001.011
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_PCIE&PCI_(1/5)
Size A3
Document Number JM70-PU
Rev -2
Date: Friday, March 06, 2009
Sheet 11 of 56

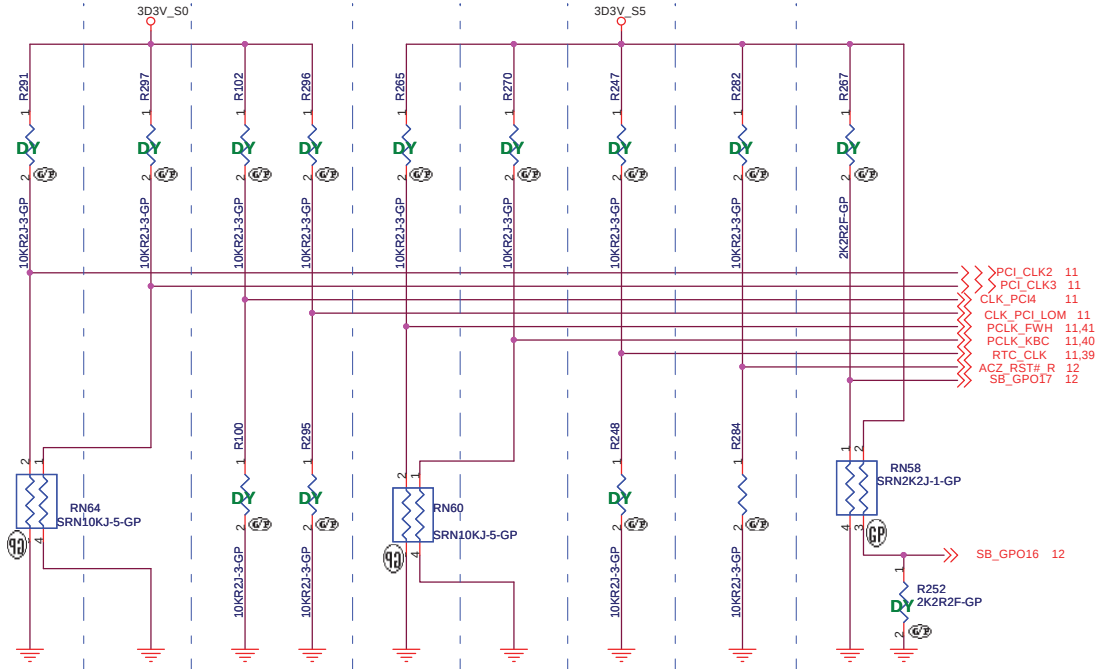

SB700
Part 4 of 5
PU_SB1D
SB700-1-GP-U1
USB MISC
USB 1.1
USB 2.0
GPIO
ACPI / WAKE UP EVENTS
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
USB
Pair Device
11 Card reader
10 WEBCAM
9 MINIC2 TV
8 USBCN1
7 USBCN1
6 ESATA
5 Bluetooth
4 NC
3 FingerPrint
2 NEW1
1 MINIC1
0 USB1 CN
OCP4#
OCP0#
Place these close SB700
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
1%
Strap Pin / define to use LPC or SPI ROM
TO STRAPS
Close to SB700
NEWCARD/GLAN
081222 SC
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_USB&GPIO_(2/5)
Size A3
Document Number JM70-PU
Rev -2
Date: Friday, March 06, 2009
Sheet 12 of 56


PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700
SATA HDD
SATA ODD
E-SATA
2nd HDD
090119 -1
PU_SB1B
SB700
Part 2 of 5
SERIAL ATA
SATA PWR
ATA 66/100/133
SPI ROM
HW MONITOR
SB700-1-GP-U1
Very Close to SB700
Close to SB700
Close to SB700
20mil Width
20mil Width
Layout connect to Cap then GND
CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_SATA-IDE_(3/5)
Size A3
Document Number JM70-PU
Rev -2
Date: Friday, March 06, 2009
Sheet 13 of 56


PU_SB1C
SB700
Part 3 of 5
POWER
SB700-1-GP-U1
PU_SB1E
SB700
Part 5 of 5
GROUND
SB700-1-GP-U1
081107 SA
090206 -1
220 ohm 2A
>100mil Width
>50mil Width
>60mil Width
>20mil Width
>10mil Width
>15mil Width
Use Plane Shape for +3.3V_AVDD_USB
2ND = 68.00206.121
68.00216.161
2ND = 68.00216.121
68.00217.521
2ND = 68.00119.111
83.R2004.B8F
2ND = 83.R0304.A8F
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_POWER&GND_(4/5)
Size A3
Document Number JM70-PU
Rev -2
Date: Monday, March 02, 2009
Sheet 14 of 56

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved; H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM; L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

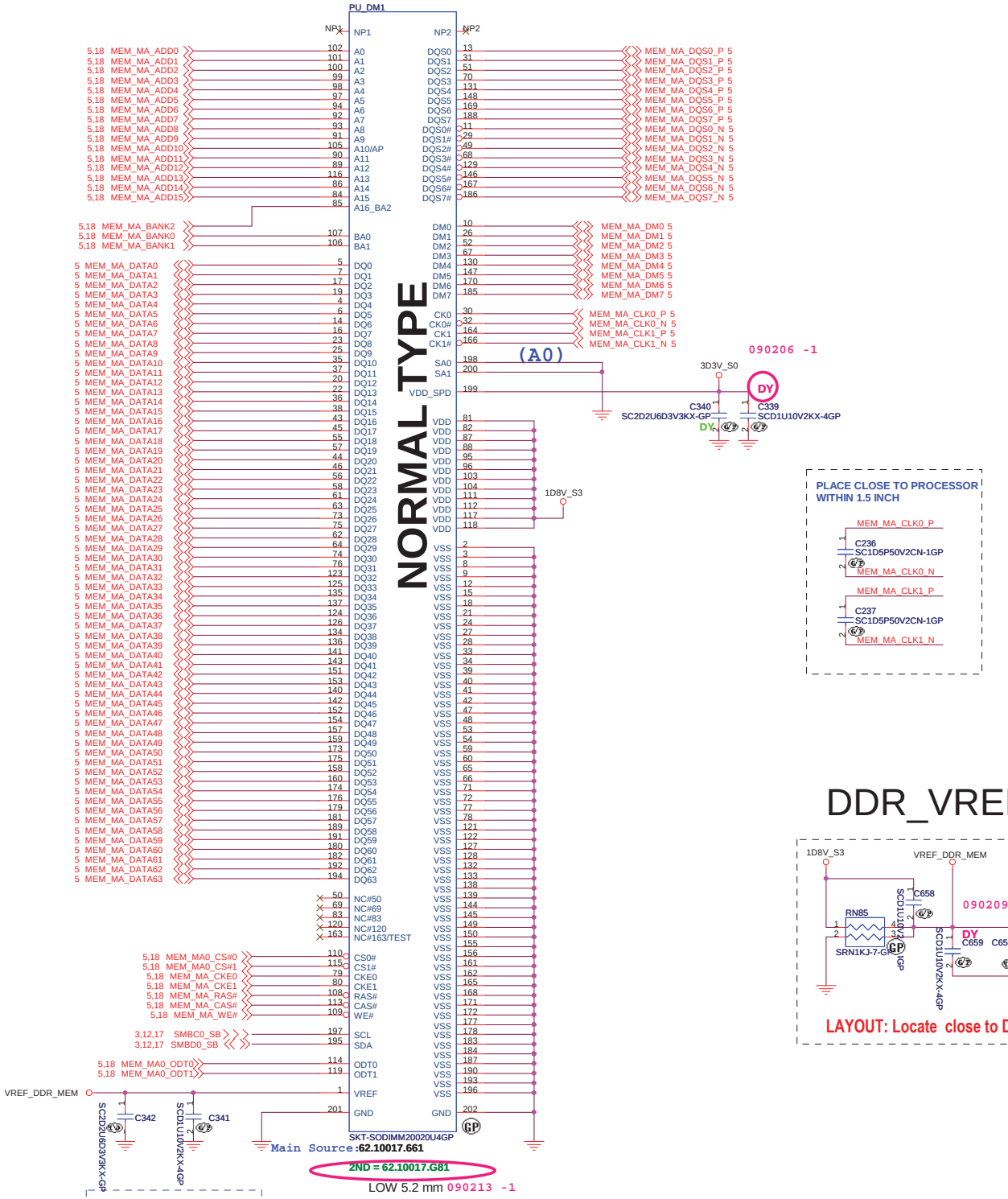
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: JM70-PU | Rev: -2

Date: Friday, March 06, 2009 | Sheet 15 of 56

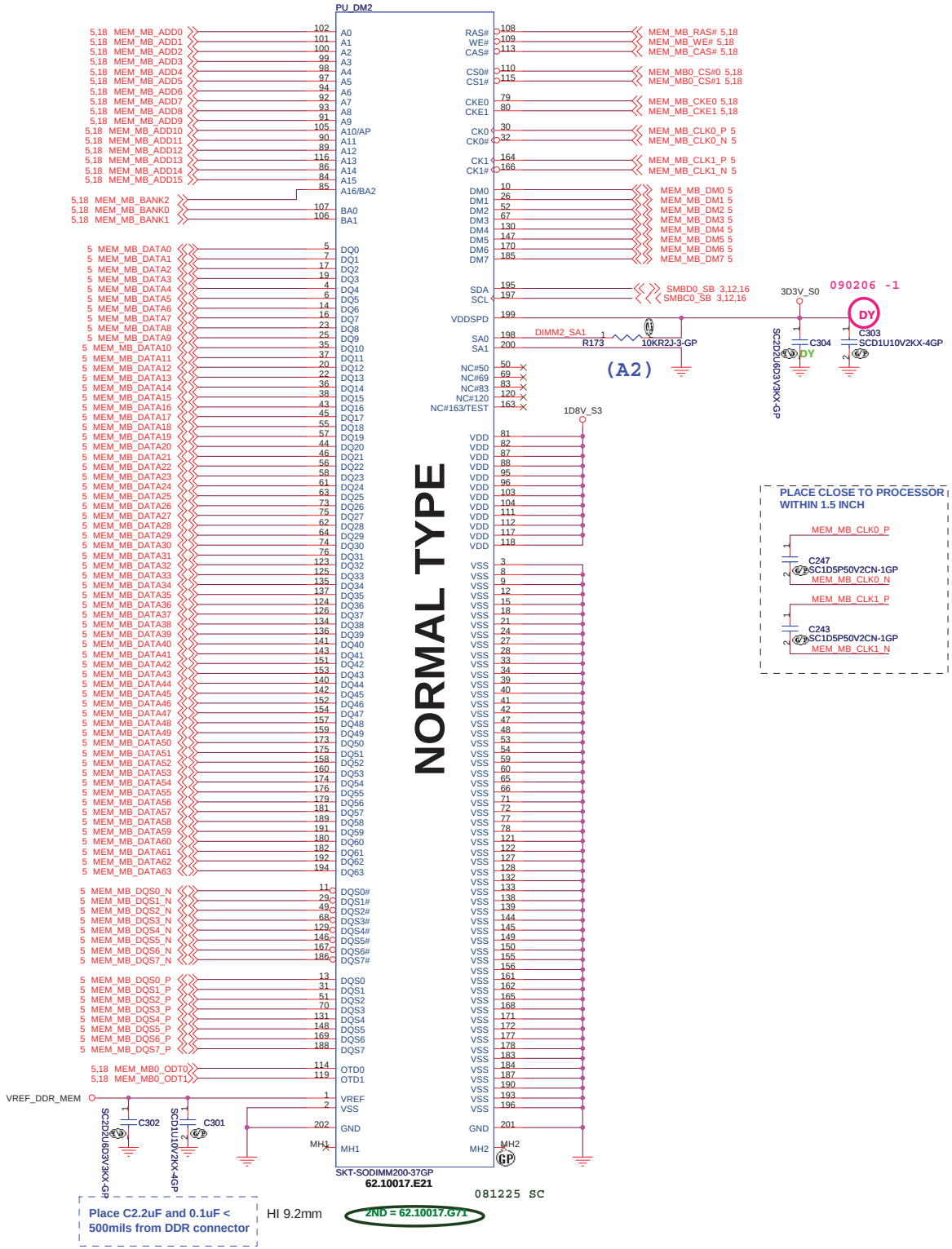


<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	JM70-PU	-2

Date: Friday, March 06, 2009 Sheet 16 of 56



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_2

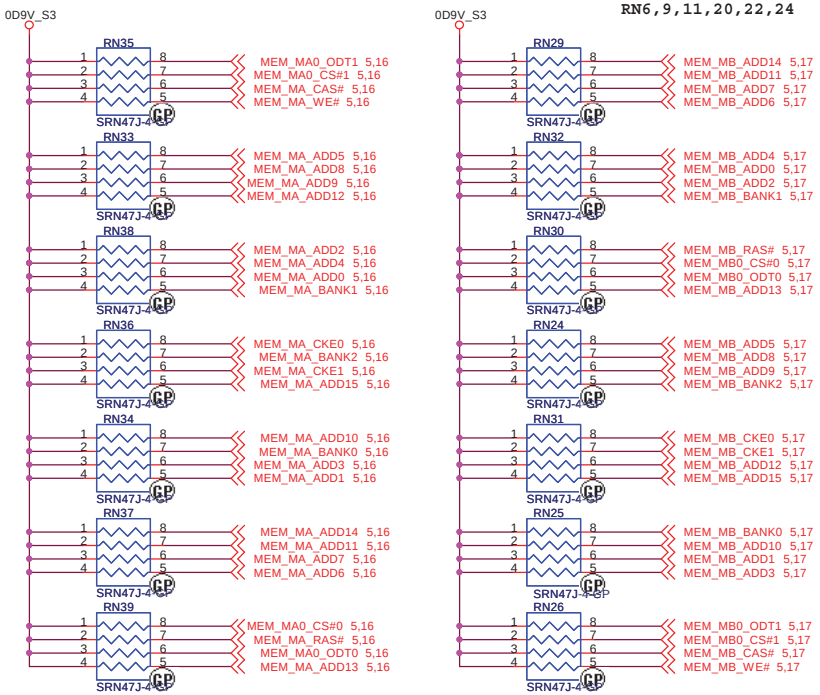
Size	Document Number	Rev
Custom	JM70-PU	-2

Date: Friday, March 06, 2009 Sheet 17 of 56

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

Net swap 11/14
RN6,9,11,20,22,24

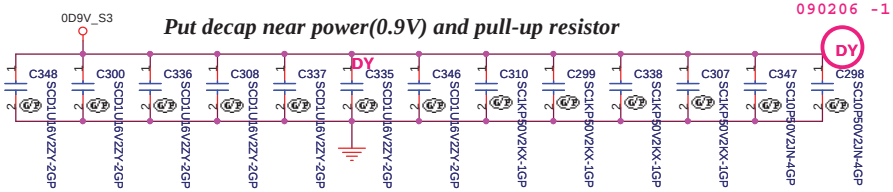


Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

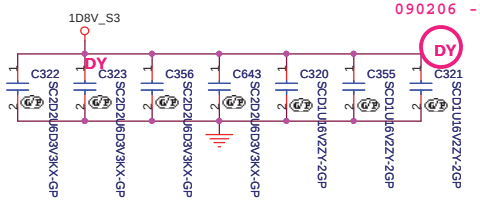
Put decap near power(0.9V) and pull-up resistor

090206 -1



Place these Caps near DM1

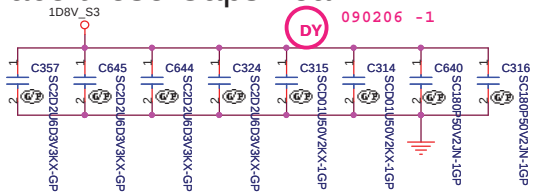
090206 -1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

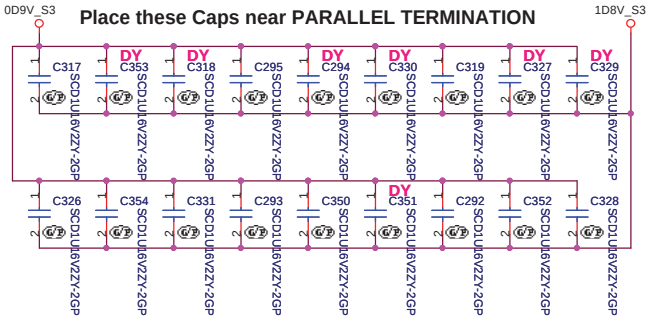
Place these Caps near DM2

090206 -1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

090209 -1



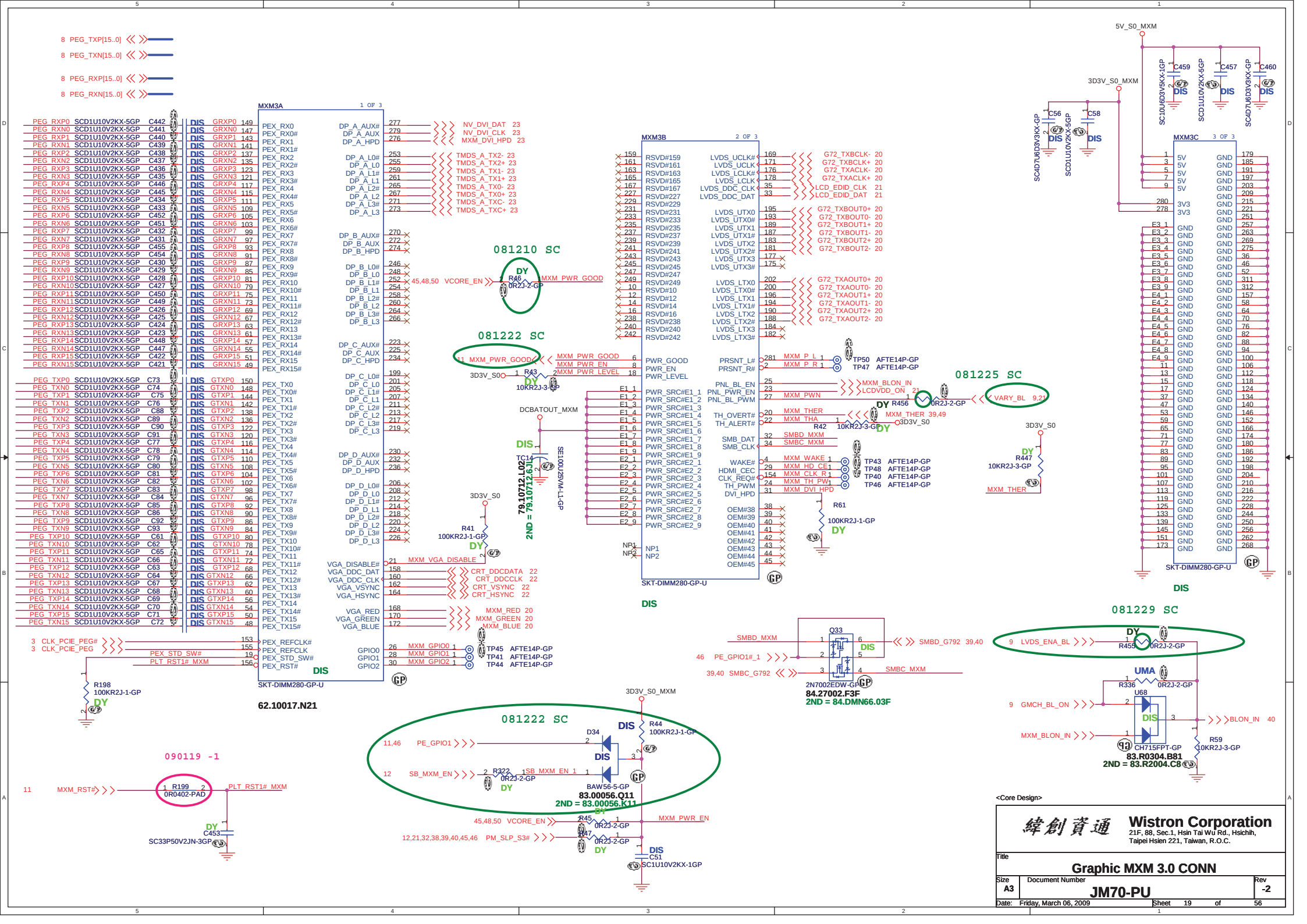
<Core Design>

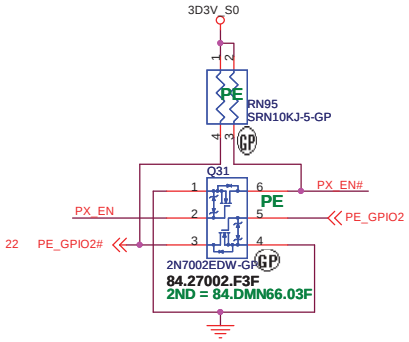
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

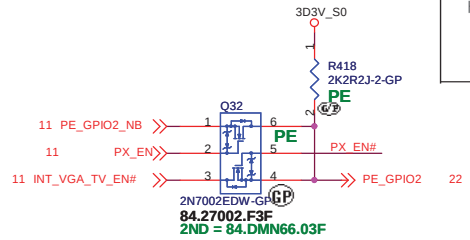
Title: DDR_DAMPING & TERMINATION

Size	Document Number	Rev
A3	JM70-PU	-2

Date: Friday, March 06, 2009 Sheet 18 of 56

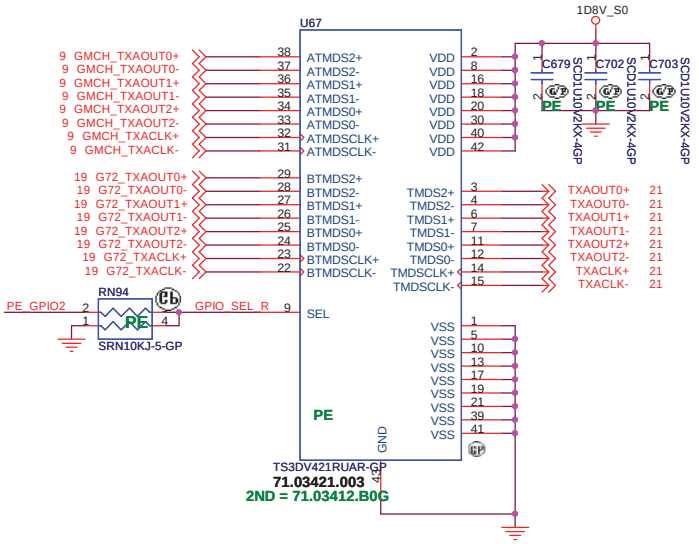

MXM3A
MXM3B
MXM3C
SKT-DIMM280-GP-U
SKT-DIMM280-GP-U
SKT-DIMM280-GP-U
081210 SC
081222 SC
081222 SC
081225 SC
081229 SC
090119 -1
62.10017.N21
83.00056.Q11
2ND = 83.00056.K11
84.27002.F3F
2ND = 84.DMN66.03F
83.R0304.B81
2ND = 83.R2004.C8
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Graphic MXM 3.0 CONN
JM70-PU
Friday, March 06, 2009

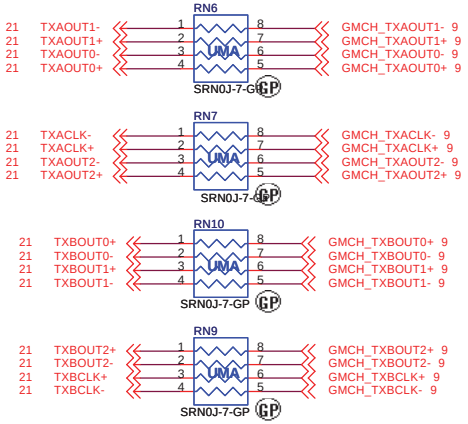


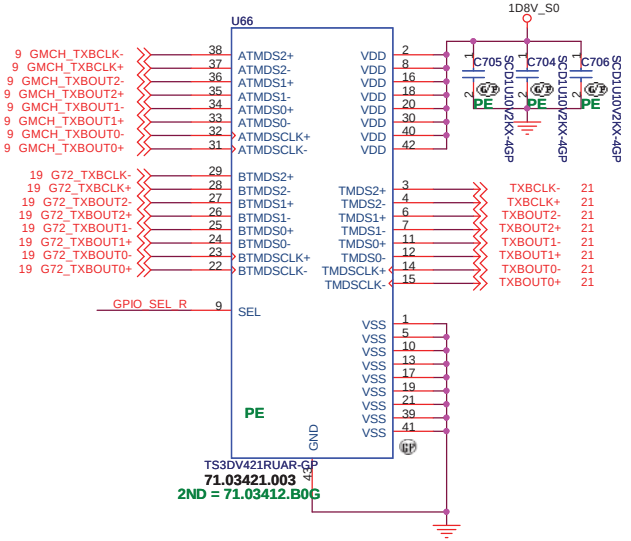


FUNCTION TABLE

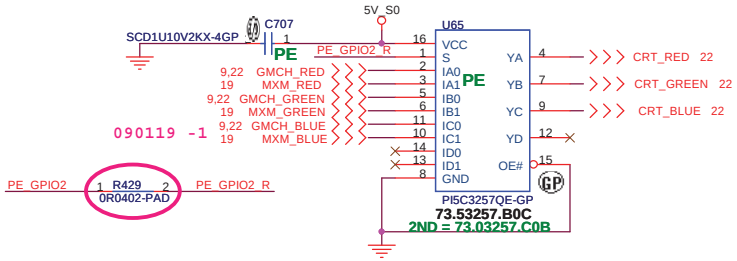
SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-







$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1



DISPLAY SUPPORT TABLE

	PX_EN	PE_GPIO2_NB	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	0	X	0	IGP(LVDS,VGA,HDMI,DP)
MXM only mode	0	X	1	MXM(LVDS,VGA,HDMI,DP)
Power Express mode	1	0/1	X	*MXM(VGA,HDMI,DP); MXM/IGP(LVDS)
IGP + MXM	0	X	0	IGP(LVDS,VGA,HDMI)

<Core Design>

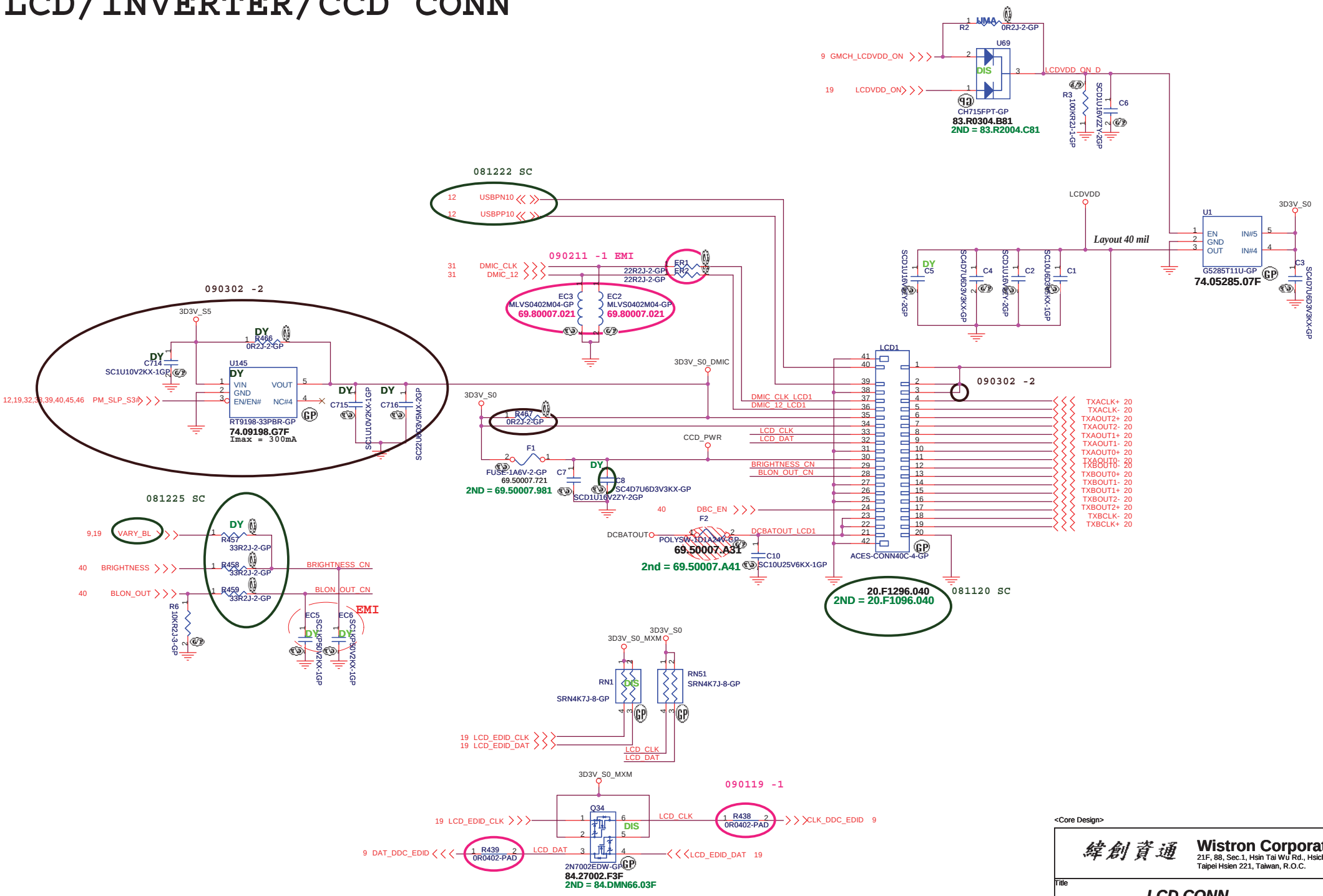
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SWITCH

Size | Document Number: JM70-PU | Rev: -2

Date: Friday, March 06, 2009 | Sheet 20 of 56

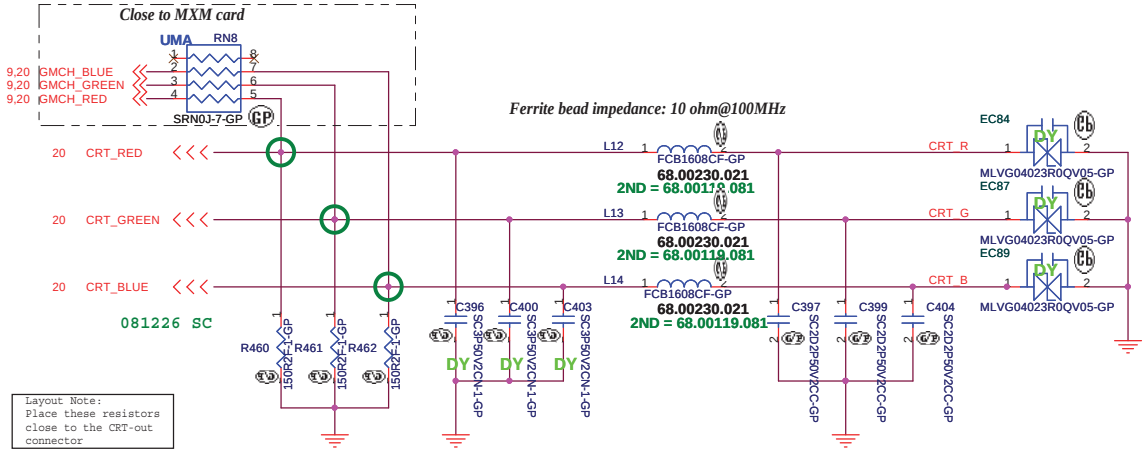
LCD/INVERTER/CCD CONN



<Core Design>

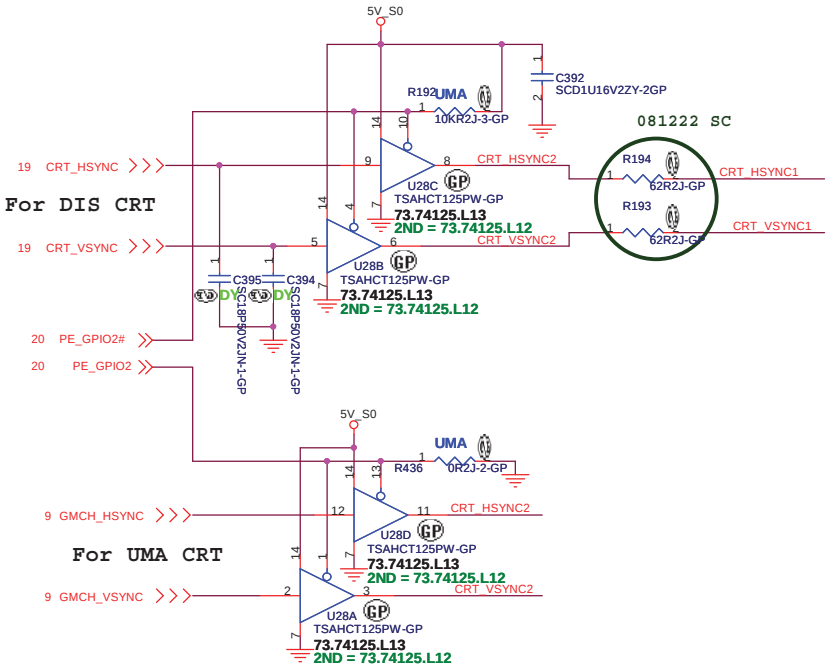
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LCD CONN	
Size A3	Document Number JM70-PU	Rev -2
Date: Friday, March 06, 2009	Sheet 21 of 56	

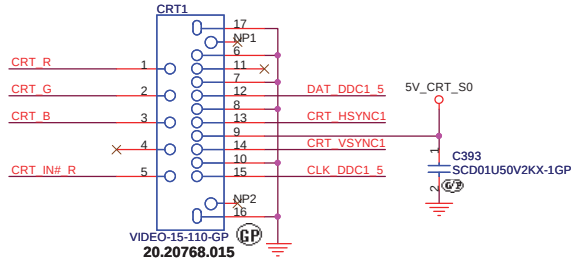


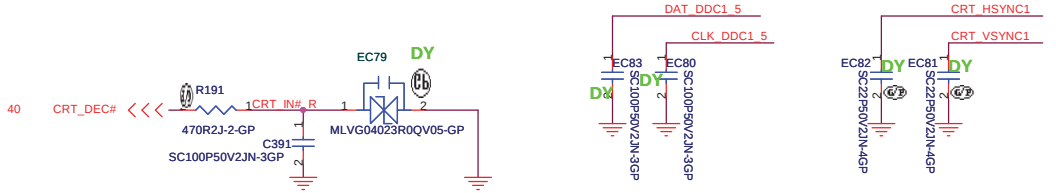
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

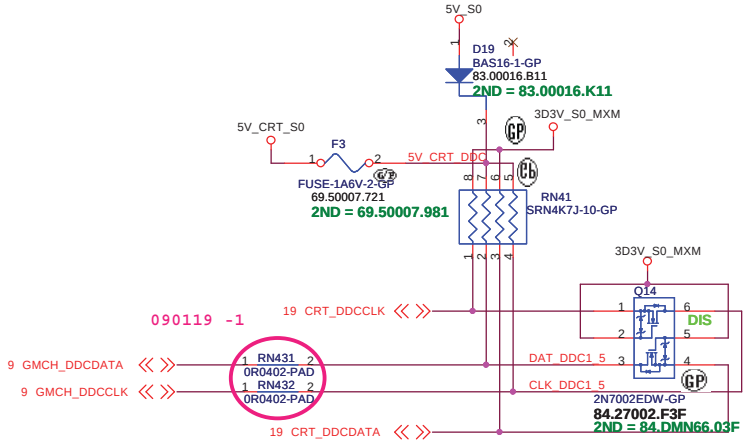


CRT I/F & CONNECTOR





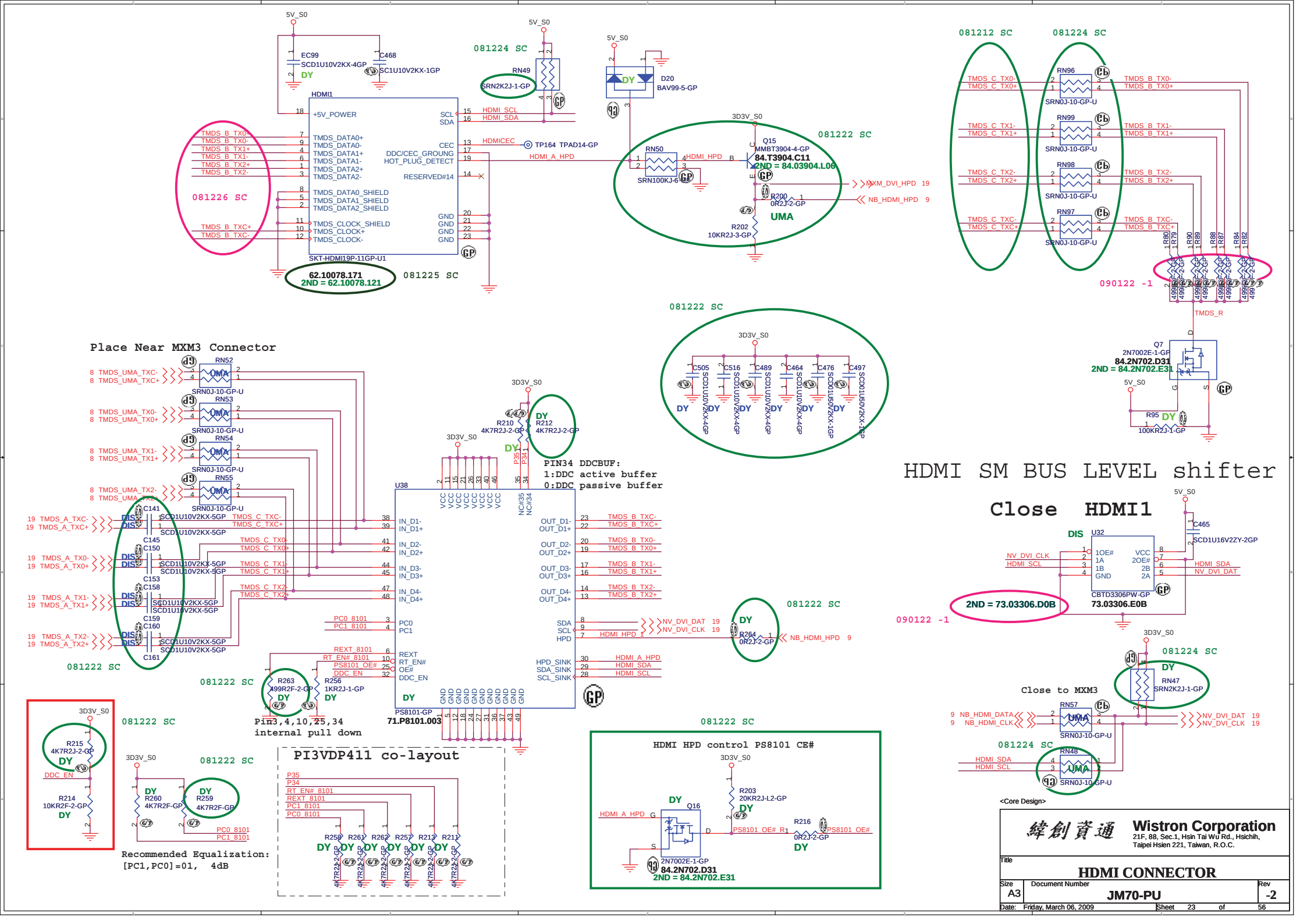
DDC_CLK & DATA level shift



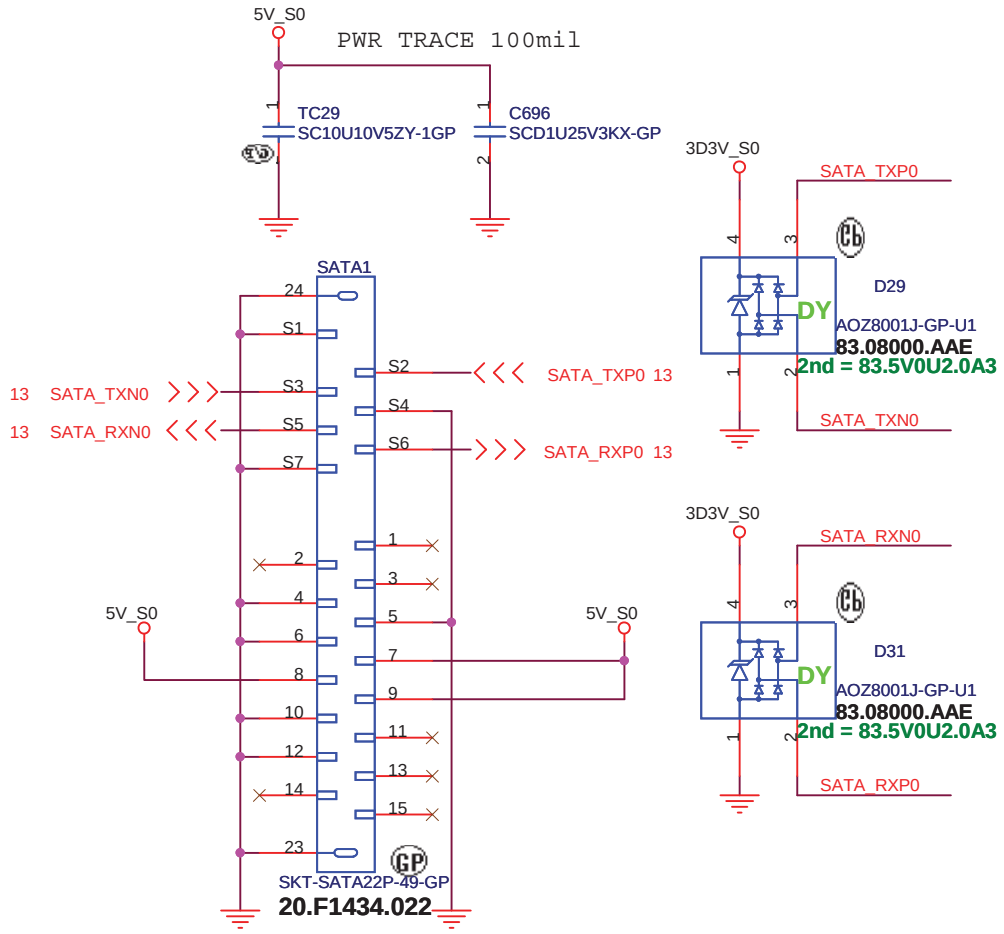
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT Connector	
Size	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 22 of 56	

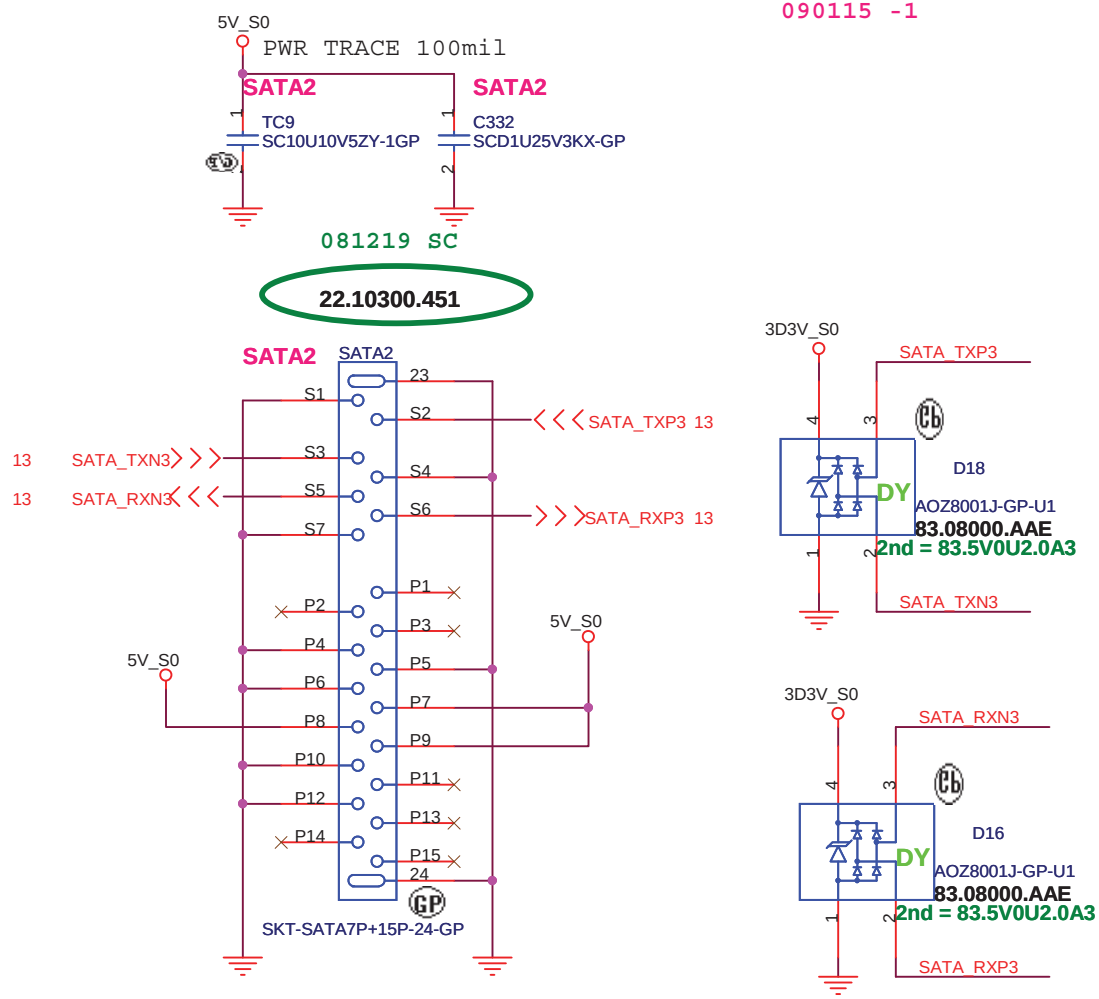

HDMI SM BUS LEVEL shifter
Close HDMI1
Place Near MXM3 Connector
PI3VDP411 co-layout
HDMI HPD control PS8101 CE#
Close to MXM3
Recommended Equalization:
[PC1,PC0]=01, 4dB
Pin3,4,10,25,34
internal pull down
PIN34 DDCBUF:
1:DDC active buffer
0:DDC passive buffer
HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
2ND = 62.10078.121
U38
PS8101-GP
71.P8101.003
U32
CBTD3306PW-GP
73.03306.E0B
2ND = 73.03306.D0B
Q15
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.L06
Q7
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
Q16
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
HDMI CONNECTOR
JM70-PU
Size A3
Rev -2
Date: Friday, March 06, 2009
Sheet 23 of 56

SATA HDD Connector



2ND SATA HDD Connector

090115 -1

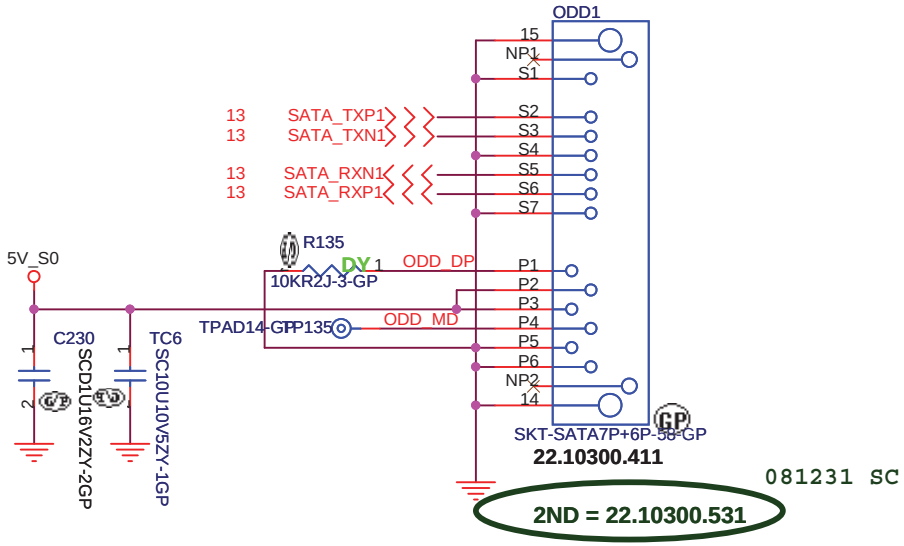


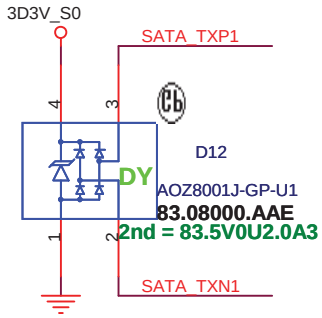
<Core Design>

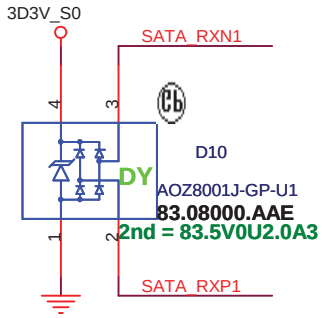
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	HDD	
Size: A4	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 24 of 56	

ODD Connector







<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CDROM

Size	Document Number	Rev
A4	JM70-PU	-2

Date: Friday, March 06, 2009 Sheet 25 of 56

090115 -1

090213 -1

5V_USB1_S5

USB1

6
1
2
3
4
5

SKT-1394-4P-27-GP-U

22.10218.T51

2ND = 22.10218.W51

090120 -1

USBPN1 12

USBPP1 12

3D3V_S0

SATA_RXP2 13

U74

AOZ8001J-GP-U1

83.08000.AAE

2nd = 83.5V0U2.0A3

SATA_RXN2 13

3D3V_S0

SATA_TXN2 13

U75

AOZ8001J-GP-U1

83.08000.AAE

2nd = 83.5V0U2.0A3

SATA_TXP2 13

090210 -1

5V_USB1_S5

USBPP1

U54

AOZ8001J-GP-U1

83.08000.AAE

2nd = 83.5V0U2.0A3

USBPN1

<Core Design>

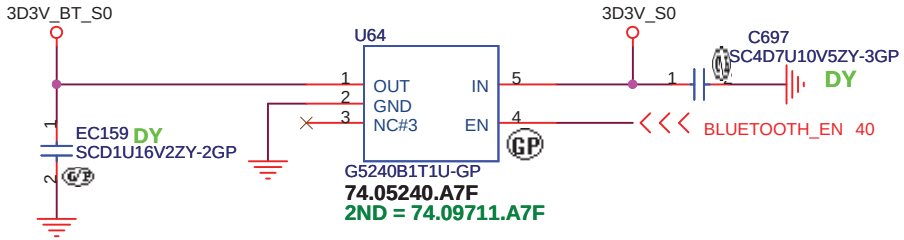
緯創資通

Wistron Corporation

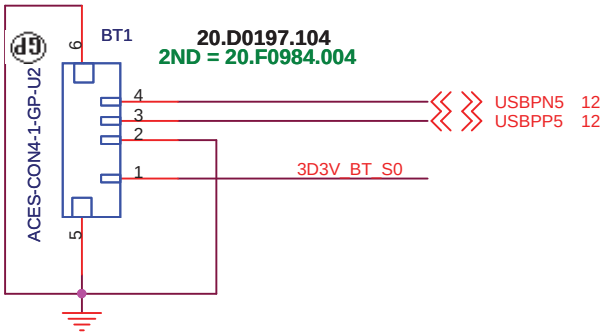
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***USB1***	
Size: A4	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 26 of 56	

BLUETOOTH MODULE



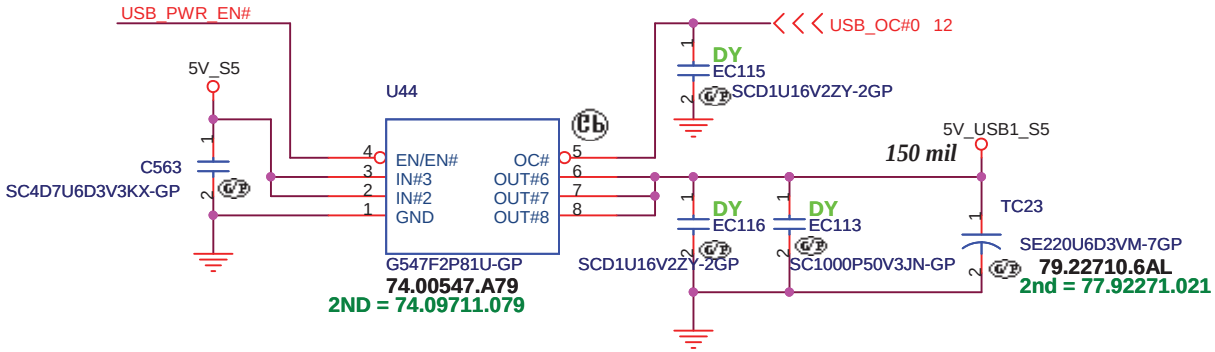
EC40 put near BLUE1 / all USB put one choke near connector by EMI request



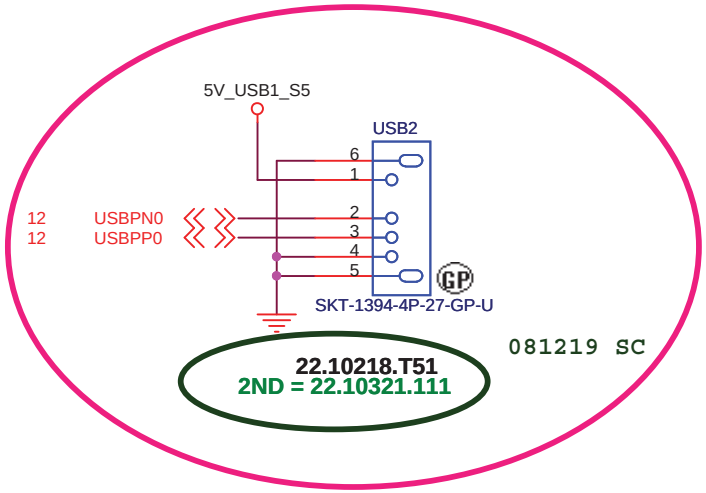
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BLUETOOTH	
Size: A4	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 27 of 56	

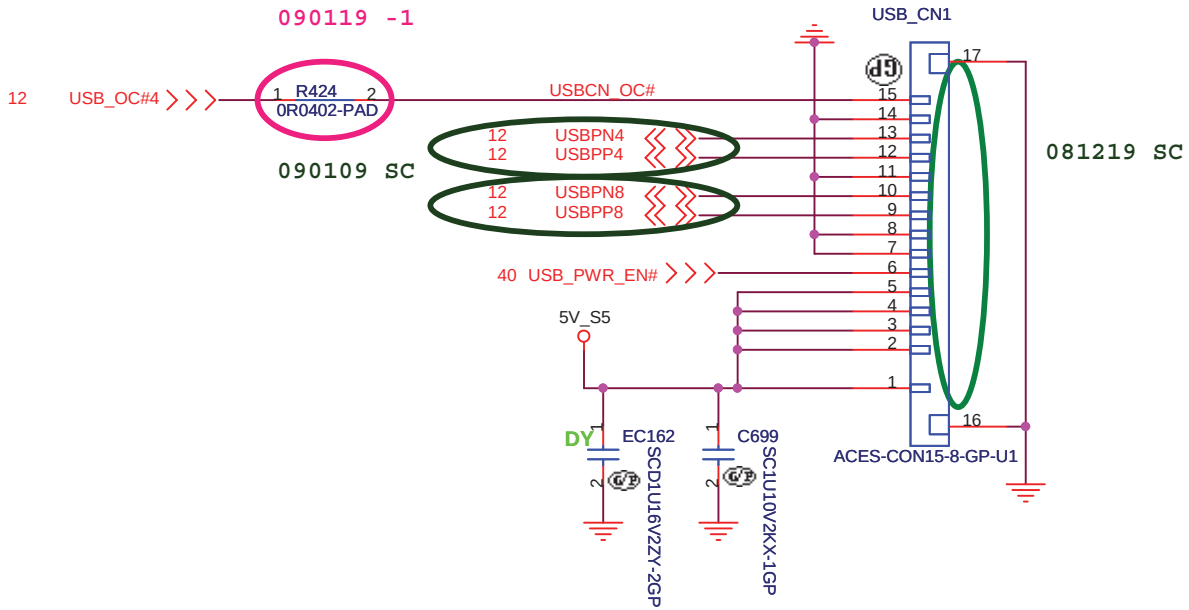


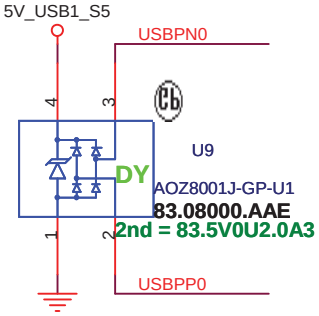
090115 -1



20.F1290.015
2ND = 21.D0214.115

090119 -1





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB2**

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Note: SI, SO, $\overline{CS}$, and SCLK have internal pull-ups.

Table 7: NVRAM Pin Strapping (EEPROM)

NVRAM Type	SO	SI	$\overline{CS}$	SCLK
EEPROM—24c64–376 KHz	1	1	0	1
EEPROM—24c512–376 KHz	1	1	0	1
Microchip 24LC02—376 KHz	1	0	0	0
Microchip 24LC04—376 KHz	1	0	0	0
Microchip 24LC08—376 KHz	1	0	0	0

U4

BCM5784MKMLG-GP

71.05784.M03

U27 AT24C02BN-SH-T-GP

72.24C02.R01

2ND = 72.24C02.M01

Q13 BCP69-GP

84.00069.B1B

2ND = 84.DCP69.01B

X1 XTAL-25MHZ-96GP

82.30020.791

2ND = 82.30020.971

FCM1608K-601T03GP

68.00217.241

2ND = 68.00248.011

Place PLLVDD/AVDDL CKT as close to chip as possible

081223 SC

081222 SC

R349 change to Bead for Transmitter Distortion

<Core Design>

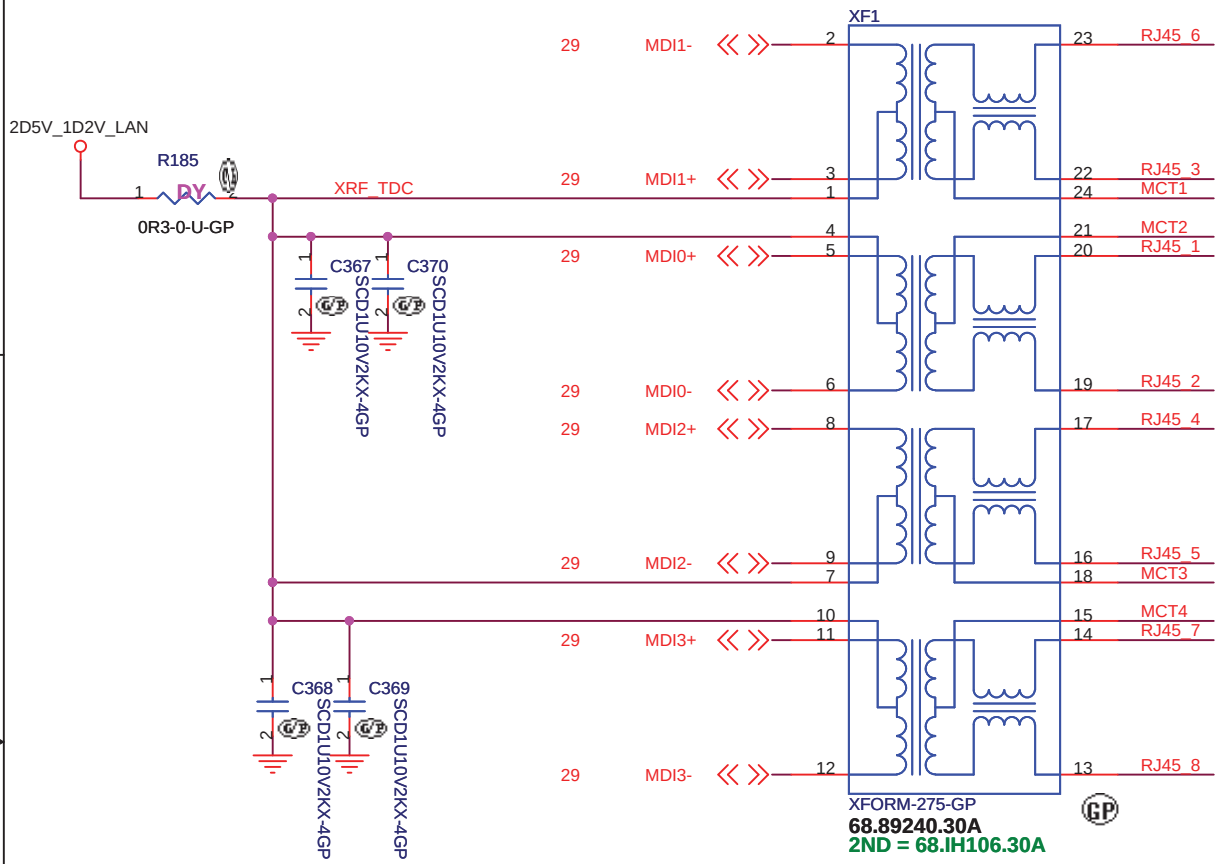
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BCM5784MKMLG

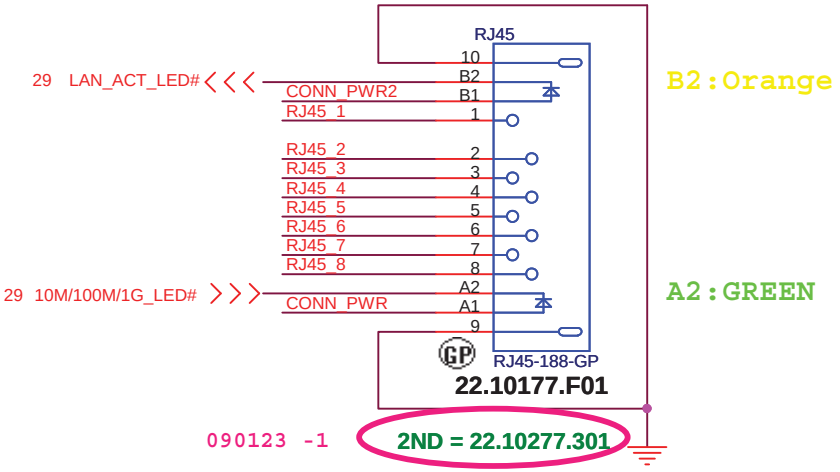
Size: A3 | Document Number: JM70-PU | Rev: -2

Date: Friday, March 06, 2009 | Sheet 29 of 56

LAN Connector

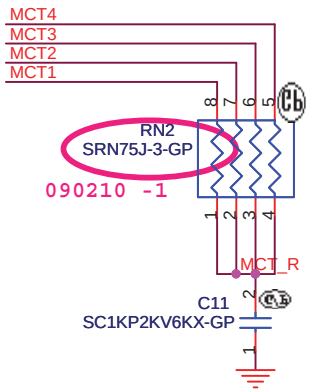


Soucrer want to add 3rd source 11/10
68.05009.301 GST5009-R LF
Angela Chi 0955-314886

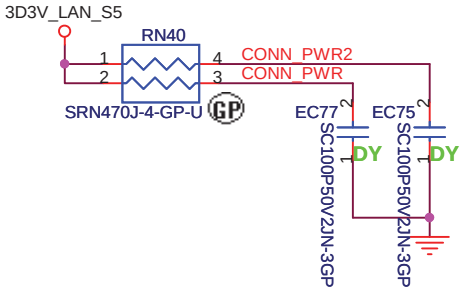


LAN Link: Green(A2), behavior is the same for 10/100/1000 bits

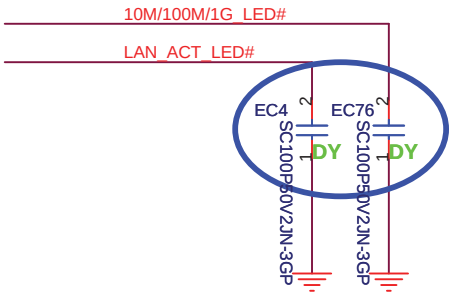
LAN Data: Yellow(B2), when LAN is transfering data.



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



For EMI Near LAN1 CONN



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

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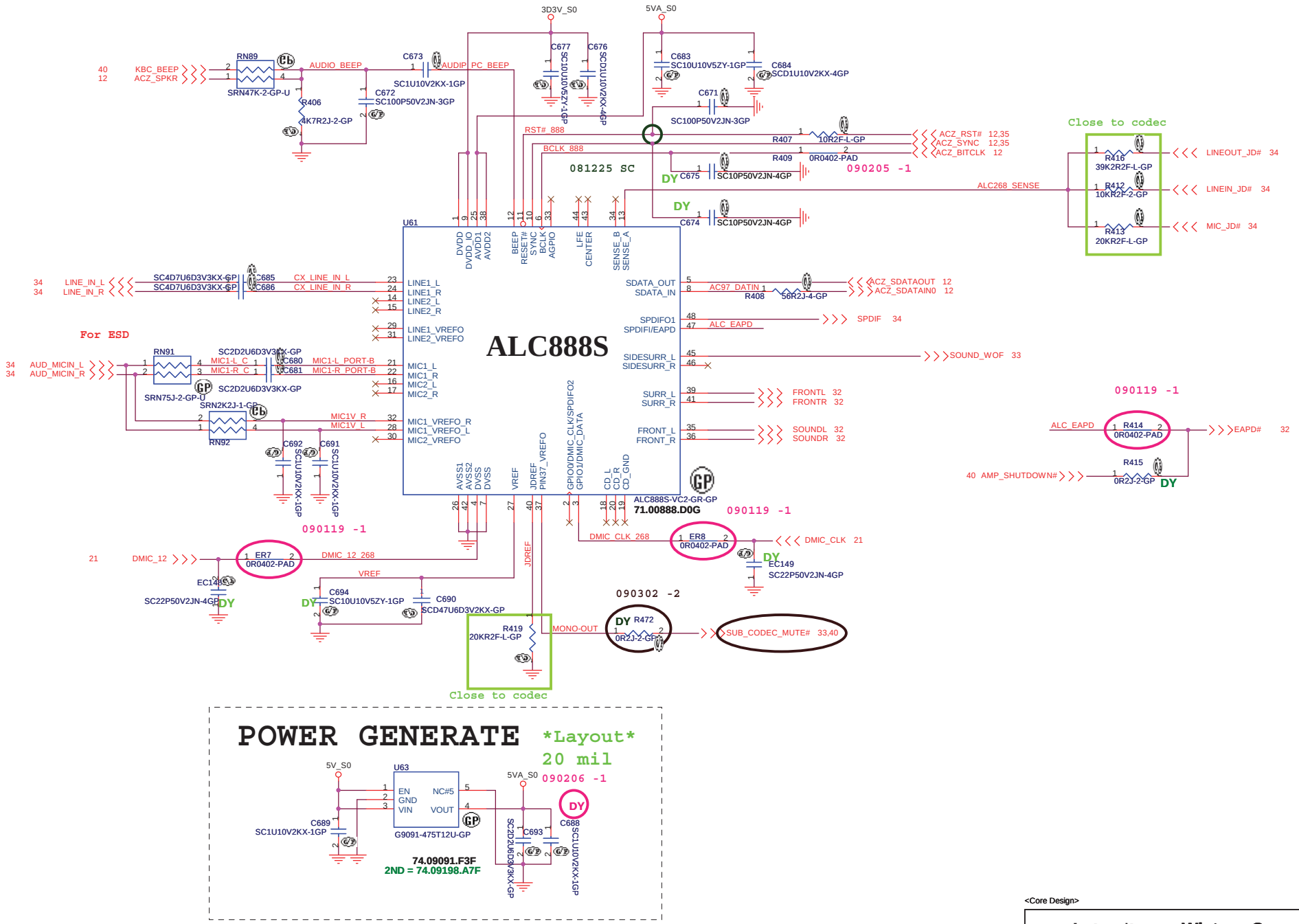

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Azalia codec ALC268***	
Size: A3	Document Number: **JM70-PU**	Rev: **-2**
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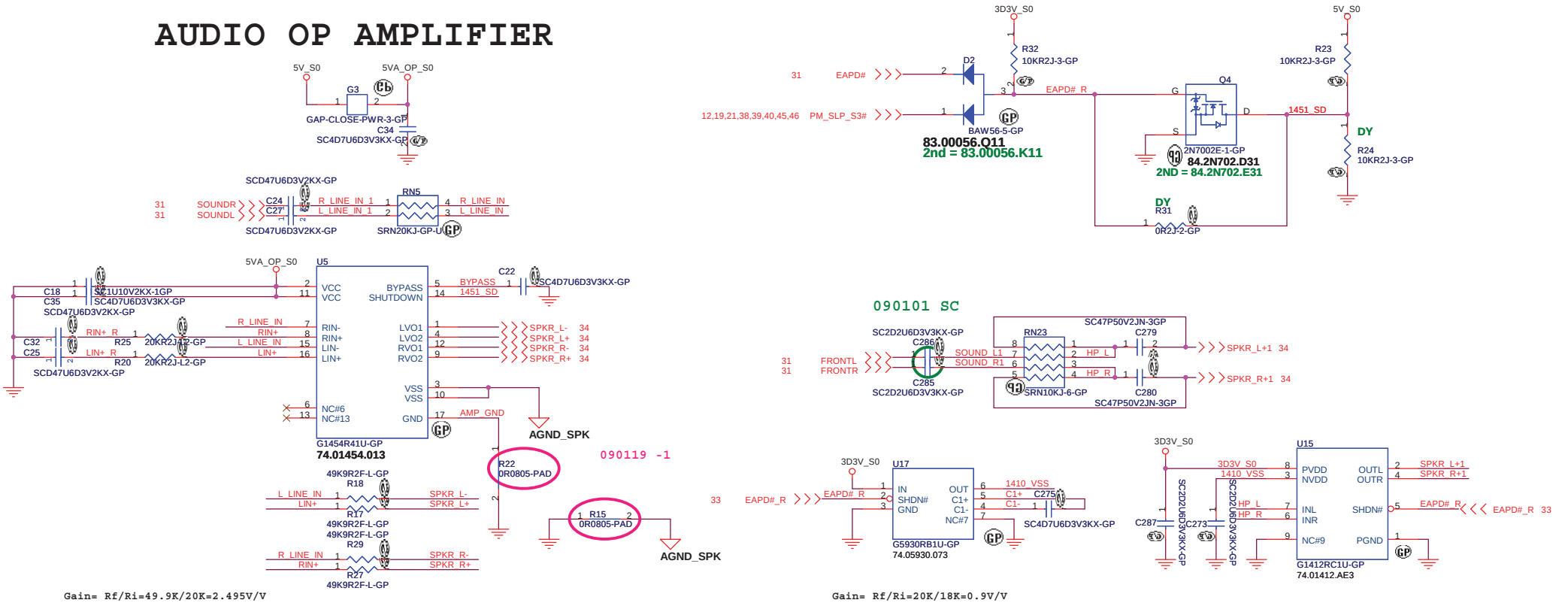
AUDIO OP AMPLIFIER



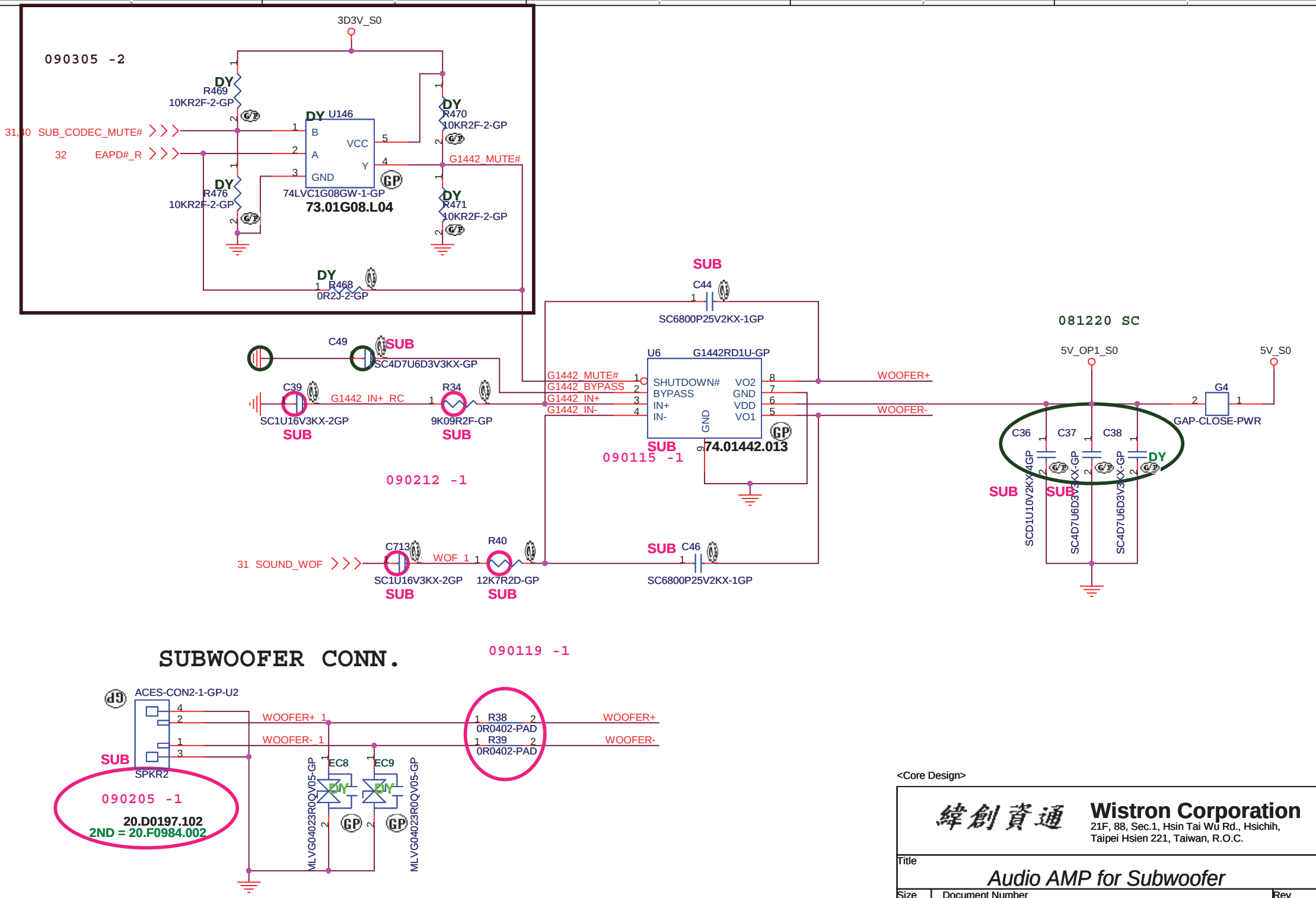
Gain= Rf/Ri=49.9K/20K=2.495V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V
V(rms)=2.828V
Power= 2.828^2/4=1.999W

Gain= Rf/Ri=20K/18K=0.9V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=0.9V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= ?

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP		
Size: A3	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 32 of 56	



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Audio AMP for Subwoofer*		
Size: A4	Document Number: JM70-PU	Rev: -2
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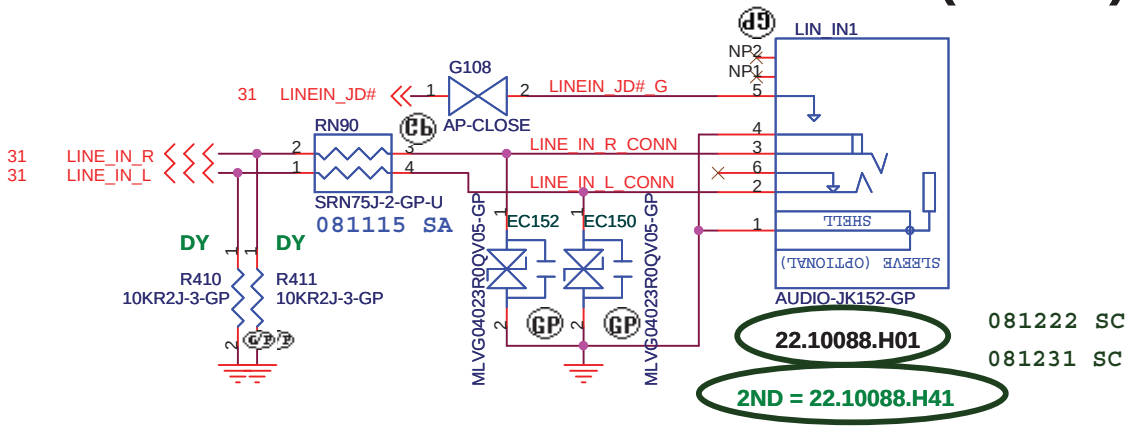
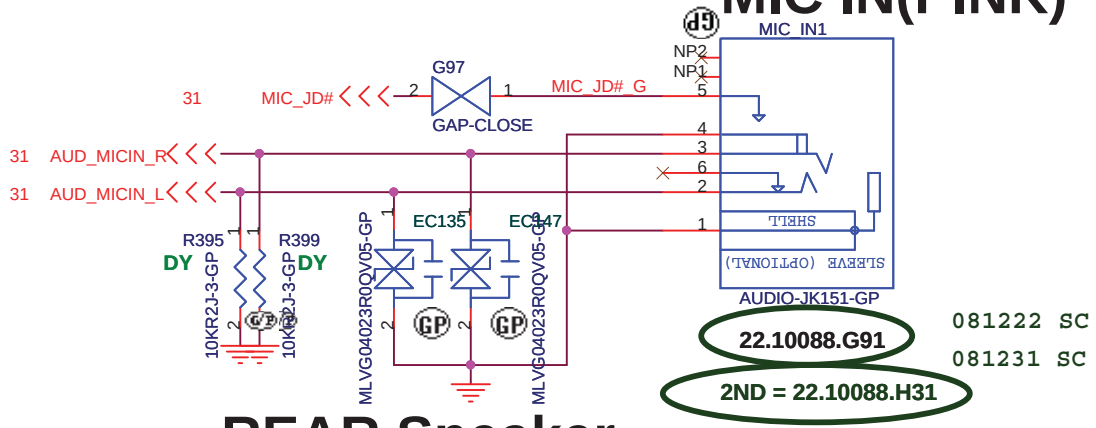
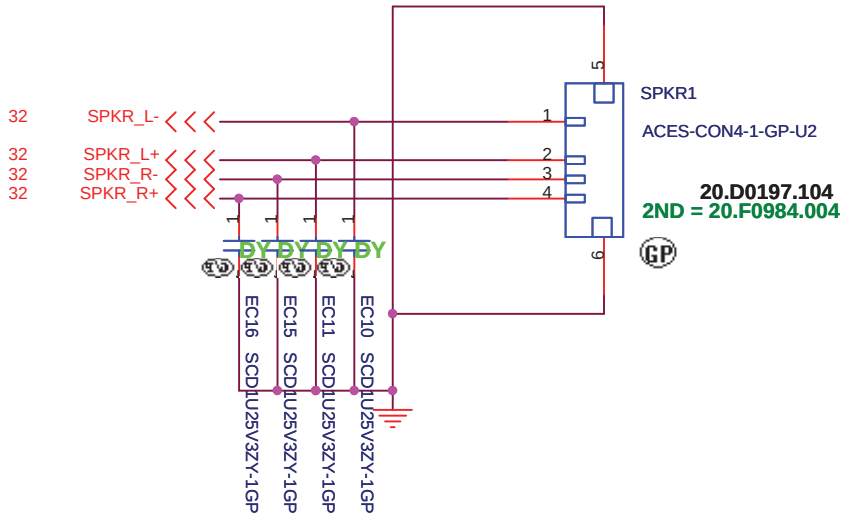
LINE IN(BLUE)



MIC IN(PINK)

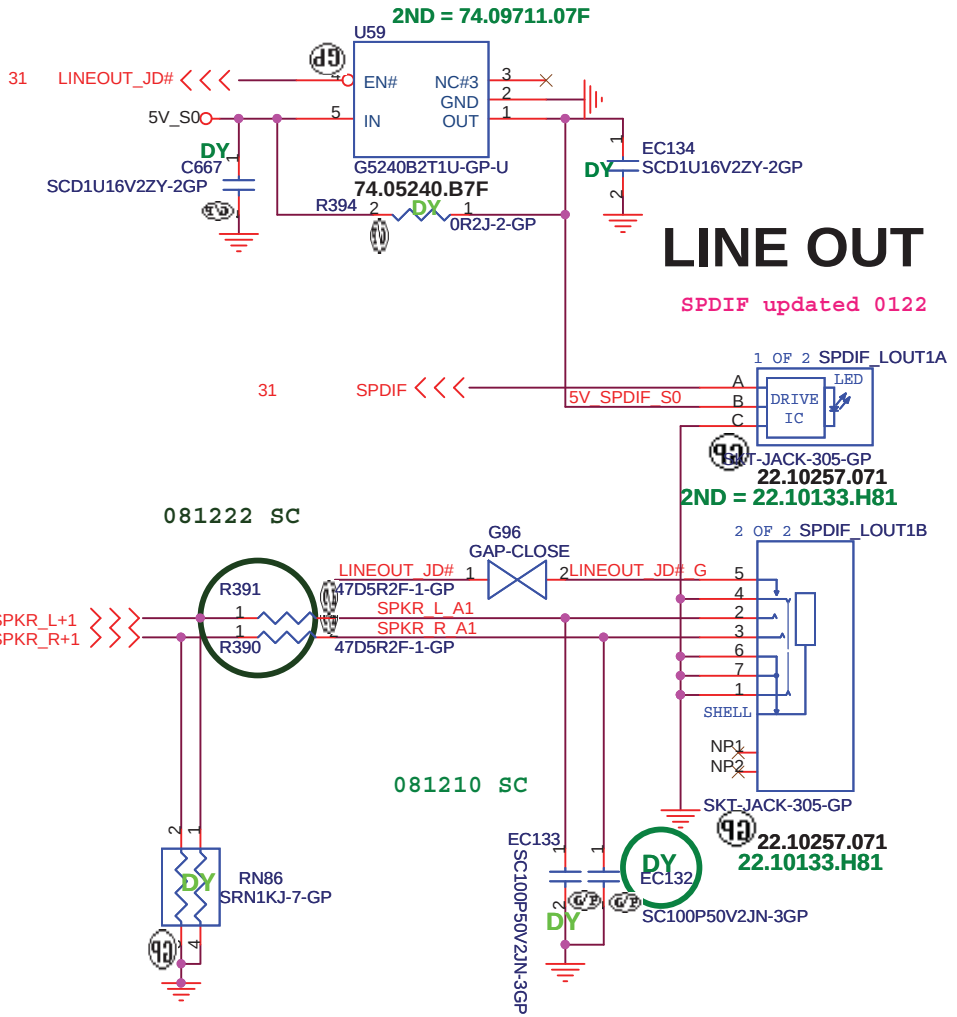


REAR Speaker



LINE OUT

SPDIF updated 0122



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO JACK		
Size: A4	Document Number: JM70-PU	Rev: -2
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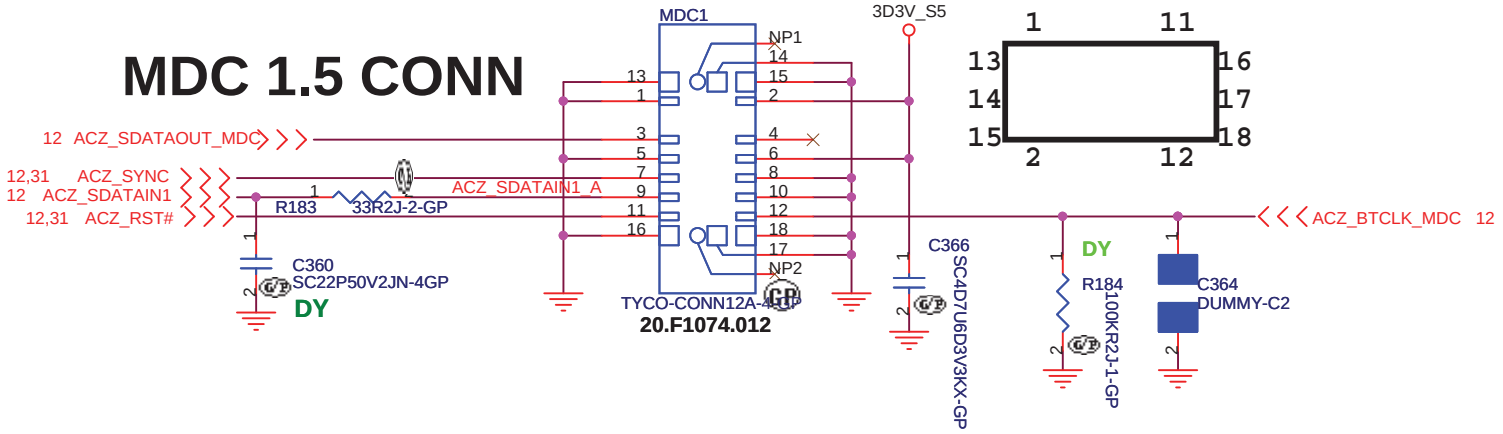
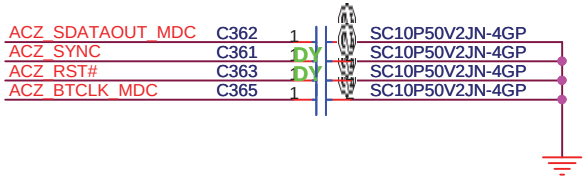
MDC 1.5 CONN



090211 -1 EMI
Stuff C362,C365(10P)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MDC

Size	Document Number	Rev
A4	JM70-PU	-2

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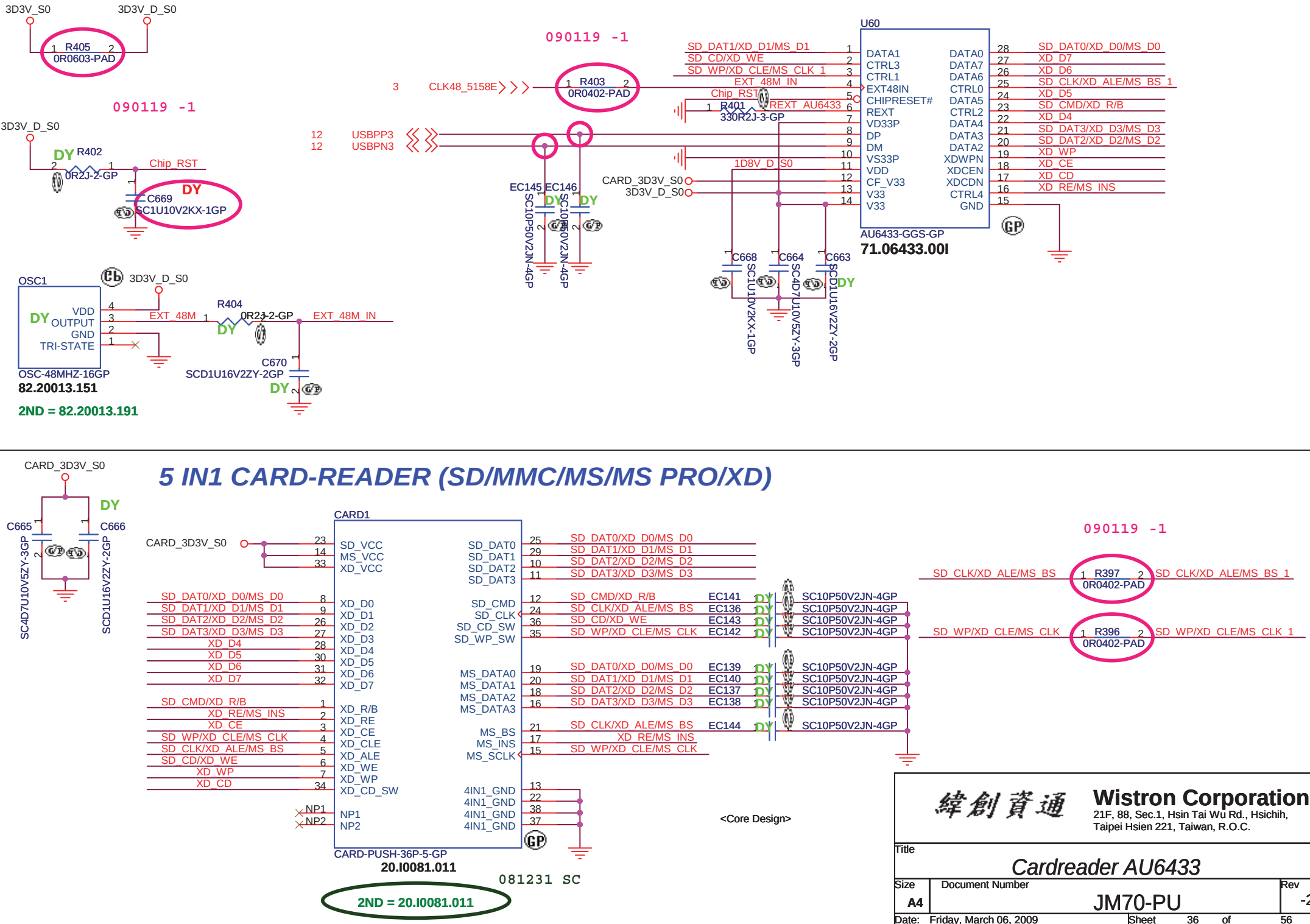
3D3V_S0
3D3V_D_S0
R405
0R0603-PAD
090119 -1
3D3V_D_S0
DY R402
0R2J-2-GP
Chip_RST
DY
C669
SC1U10V2KX-1GP
CLK48_5158E
R403
0R0402-PAD
USBPP3
USBPN3
SD_DAT1/XD_D1/MS_D1
SD_CD/XD_WE
SD_WP/XD_CLE/MS_CLK_1
EXT_48M_IN
Chip_RST
R401
330R2J-3-GP
REXT_AU6433
1D8V_D_S0
CARD_3D3V_S0
3D3V_D_S0
EC145 EC146
DY DY
SC10P50V2JN-4GP
U60
DATA1
CTRL3
CTRL1
EXT48IN
CHIPRESET#
REXT
VD33P
DP
DM
VS33P
VDD
CF_V33
V33
V33
DATA0
DATA7
DATA6
CTRL0
DATA5
CTRL2
DATA4
DATA3
DATA2
XDWPN
XDCEN
XDCDN
CTRL4
GND
SD_DAT0/XD_D0/MS_D0
XD_D7
XD_D6
SD_CLK/XD_ALE/MS_BS_1
XD_D5
SD_CMD/XD_R/B
XD_D4
SD_DAT3/XD_D3/MS_D3
SD_DAT2/XD_D2/MS_D2
XD_WP
XD_CE
XD_CD
XD_RE/MS_INS
AU6433-GGS-GP
71.06433.00I
C668
SC1U10V2KX-1GP
C664
SC4D7U10V5ZY-3GP
C663
DY
SCD1U16V2ZY-2GP
OSC1
3D3V_D_S0
DY
VDD
OUTPUT
GND
TRI-STATE
EXT_48M
R404
0R2J-2-GP
DY
EXT_48M_IN
C670
SCD1U16V2ZY-2GP
DY
OSC-48MHZ-16GP
82.20013.151
2ND = 82.20013.191
CARD_3D3V_S0
DY
C665
C666
SC4D7U10V5ZY-3GP
SCD1U16V2ZY-2GP
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)
CARD1
CARD_3D3V_S0
SD_VCC
MS_VCC
XD_VCC
SD_DAT0/XD_D0/MS_D0
SD_DAT1/XD_D1/MS_D1
SD_DAT2/XD_D2/MS_D2
SD_DAT3/XD_D3/MS_D3
XD_D4
XD_D5
XD_D6
XD_D7
SD_CMD/XD_R/B
XD_RE/MS_INS
XD_CE
SD_WP/XD_CLE/MS_CLK
SD_CLK/XD_ALE/MS_BS
SD_CD/XD_WE
XD_WP
XD_CD
NP1
NP2
XD_D0
XD_D1
XD_D2
XD_D3
XD_D4
XD_D5
XD_D6
XD_D7
XD_R/B
XD_RE
XD_CE
XD_CLE
XD_ALE
XD_WE
XD_WP
XD_CD_SW
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
SD_CMD
SD_CLK
SD_CD_SW
SD_WP_SW
MS_DATA0
MS_DATA1
MS_DATA2
MS_DATA3
MS_BS
MS_INS
MS_SCLK
4IN1_GND
4IN1_GND
4IN1_GND
4IN1_GND
EC141
EC136
EC143
EC142
EC139
EC140
EC137
EC138
EC144
SC10P50V2JN-4GP
CARD-PUSH-36P-5-GP
20.I0081.011
081231 SC
2ND = 20.I0081.011
090119 -1
SD_CLK/XD_ALE/MS_BS
R397
0R0402-PAD
SD_CLK/XD_ALE/MS_BS_1
SD_WP/XD_CLE/MS_CLK
R396
0R0402-PAD
SD_WP/XD_CLE/MS_CLK_1
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Cardreader AU6433
Size
A4
Document Number
JM70-PU
Rev
-2
Date: Friday, March 06, 2009
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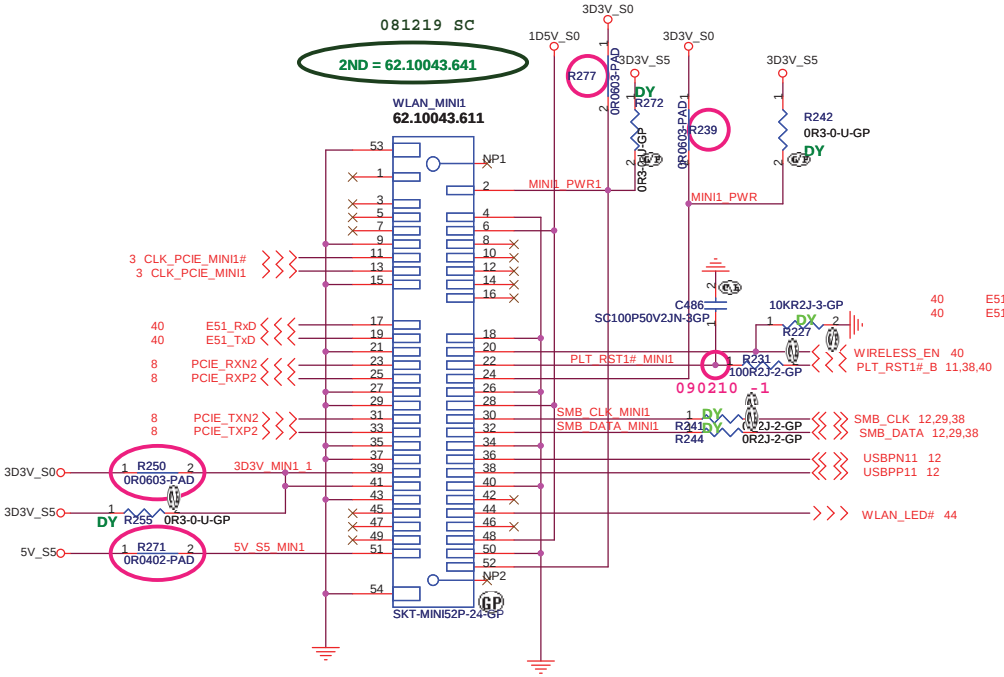
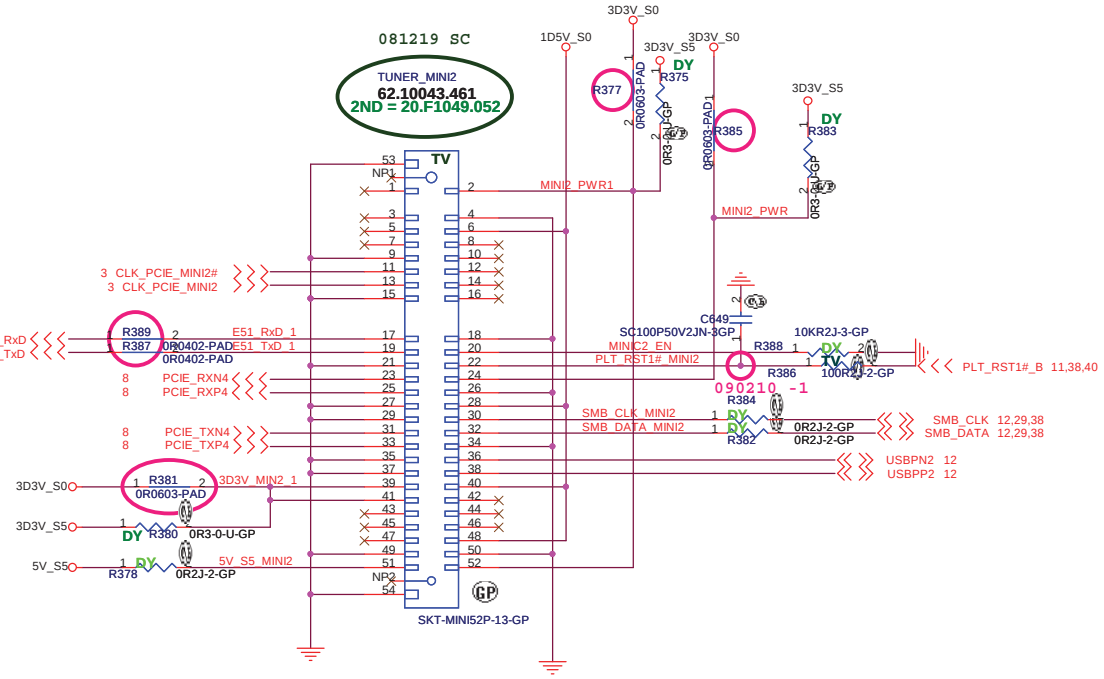
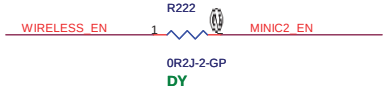
Mini1 Card Connector(WLAN)
Support debug-card

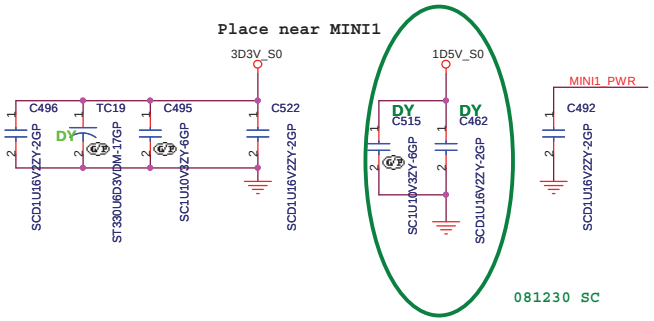
090119 -1

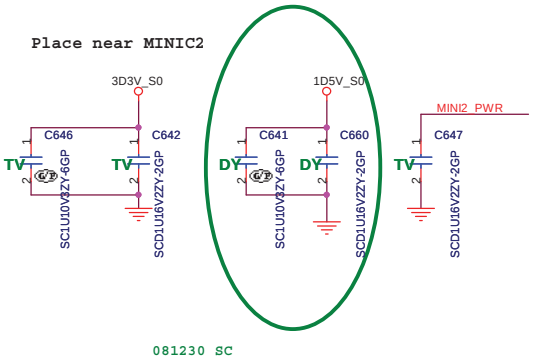


Mini2 Card Connector(TV tuner)









<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini Card

Size: A3 | Document Number: JM70-PU | Rev: -2

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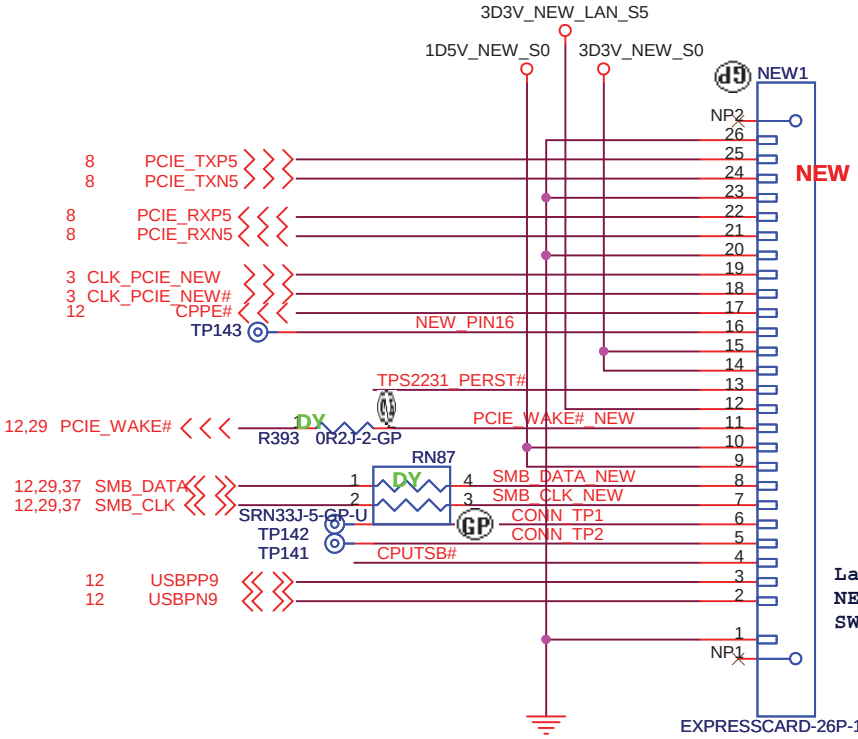
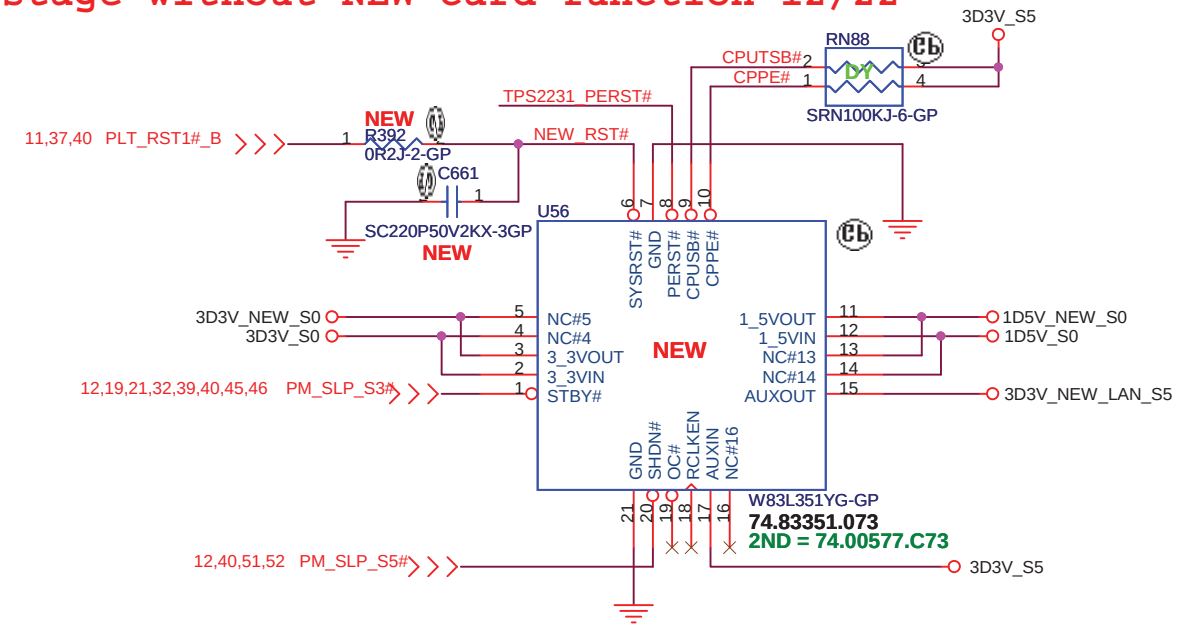
NEWCARD Connector

ENG stage without NEW card function 12/22

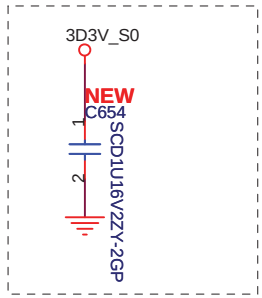




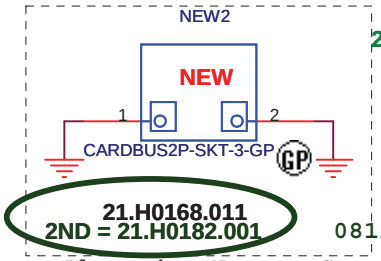
Layout Request 1226
NEW1 & NEW2
SWAP 1st & 2nd

74.00577.C73
new card power switch
GMT cost down solution

Place them Near to Chip



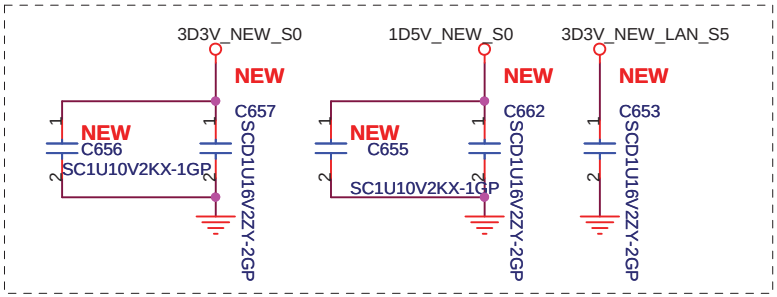
TOP VIEW



62.10081.151 081219 SC
2ND = 62.10081.131

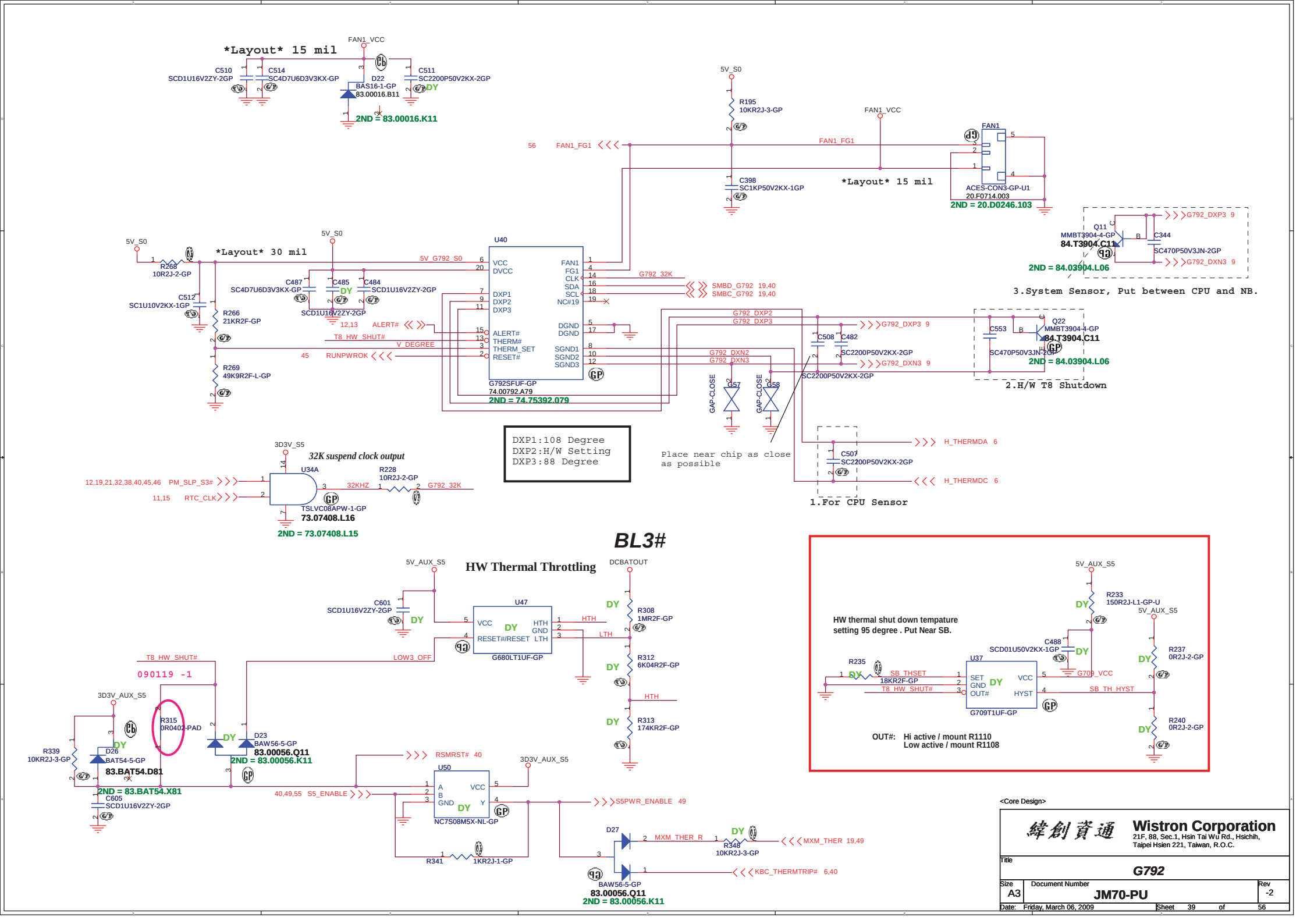
21.H0168.011
2ND = 21.H0182.001 081219 SC

Place them Near to Connector



<Core Design>

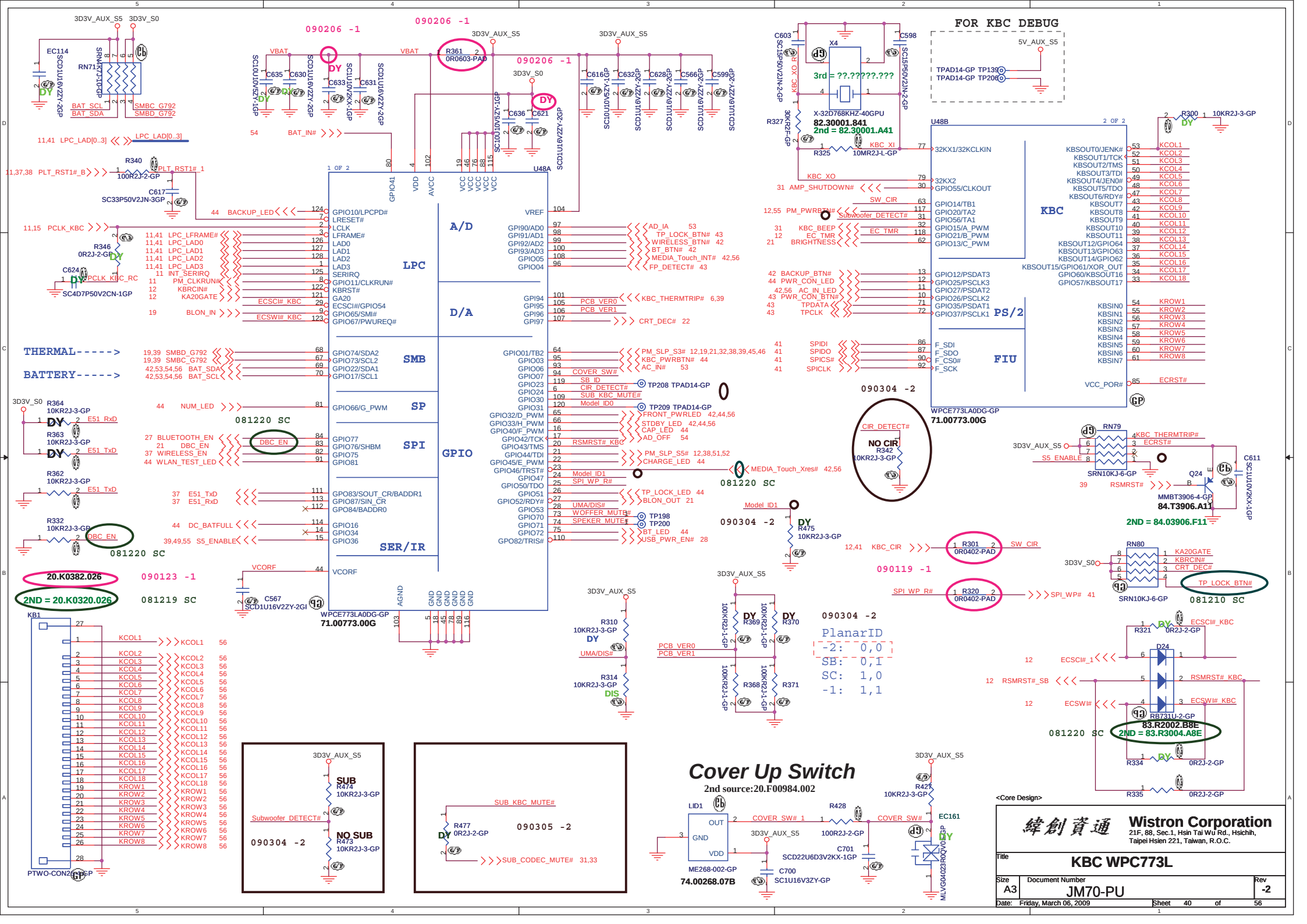
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **NEW CARD**		
Size: A4	Document Number: JM70-PU	Rev: -2
Date: Friday, March 06, 2009	Sheet 38 of 56	



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G792	
Size A3	Document Number JM70-PU	Rev -2
Date: Friday, March 06, 2009	Sheet 39 of 56	


FOR KBC DEBUG
U48A
WPCE773LA0DG-GP
71.00773.00G
U48B
KBC
PS/2
FIU
GPIO
A/D
LPC
D/A
SMB
SP
SPI
SER/IR
THERMAL----->
BATTERY----->
Cover Up Switch
2nd source:20.F00984.002
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773L
JM70-PU
Date: Friday, March 06, 2009
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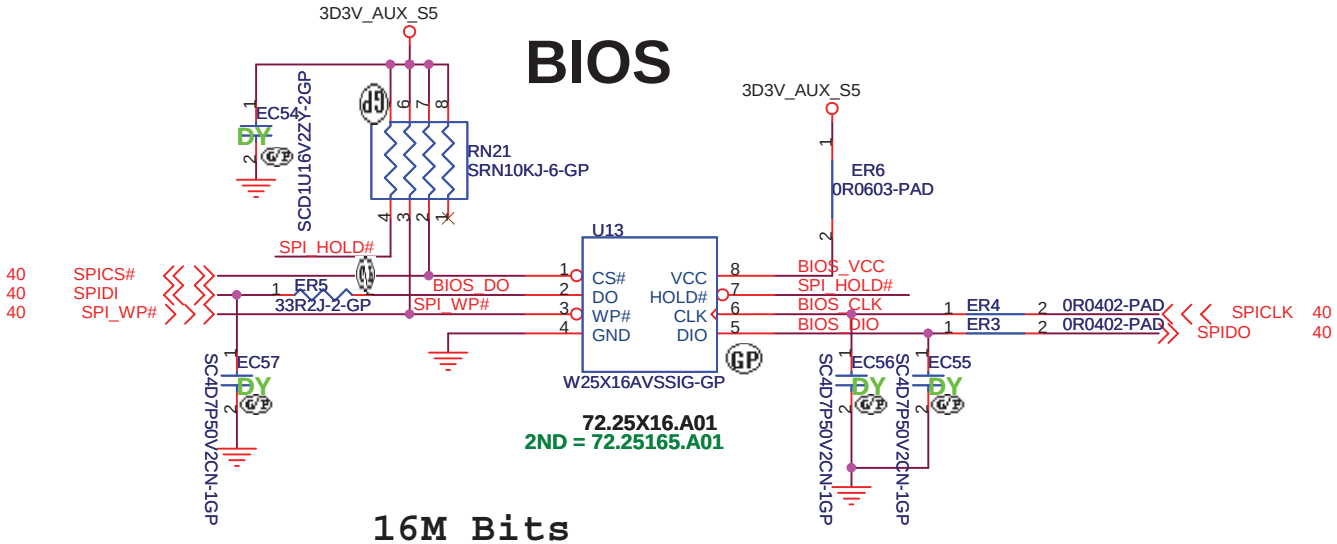
BIOS

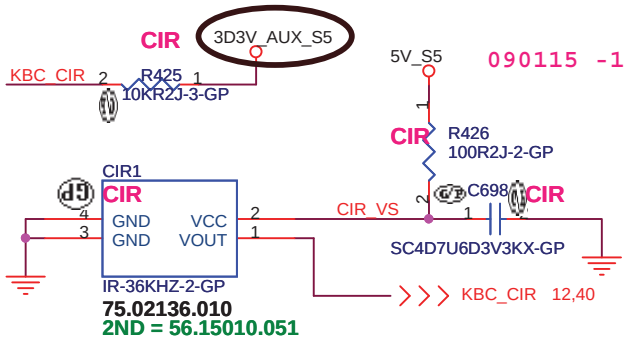


16M Bits

SPI FLASH ROM

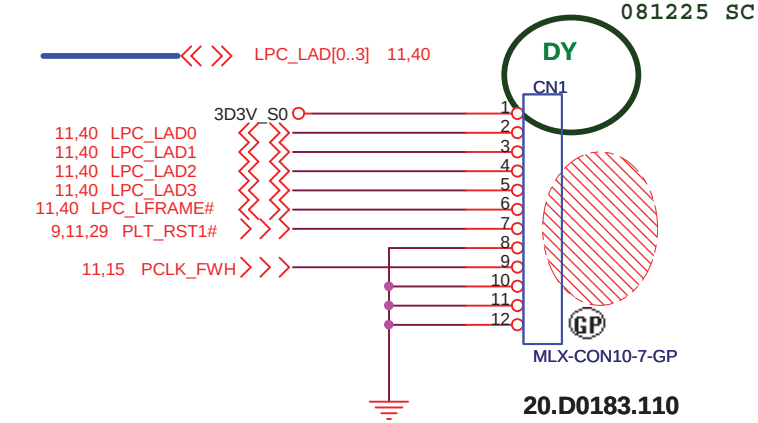
CIR Module

090304 -2



GOLDEN FINGER FOR DEBUG BOARD

081225 SC



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BIOS & CIR		
Size: A4	Document Number: JM70-PU	Rev: -2
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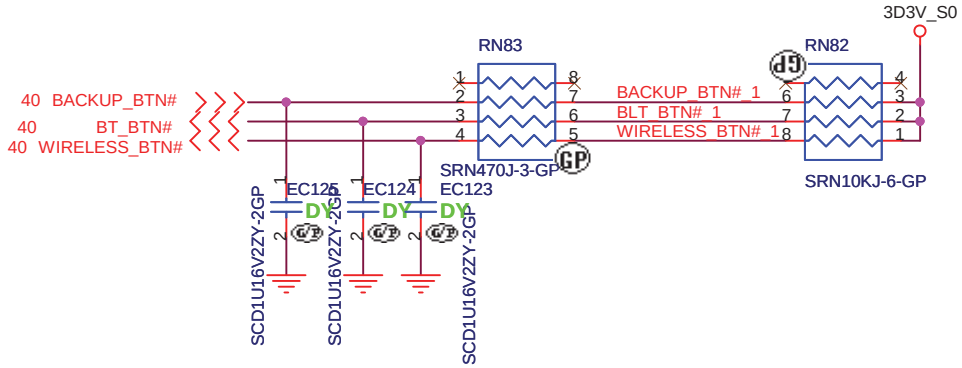
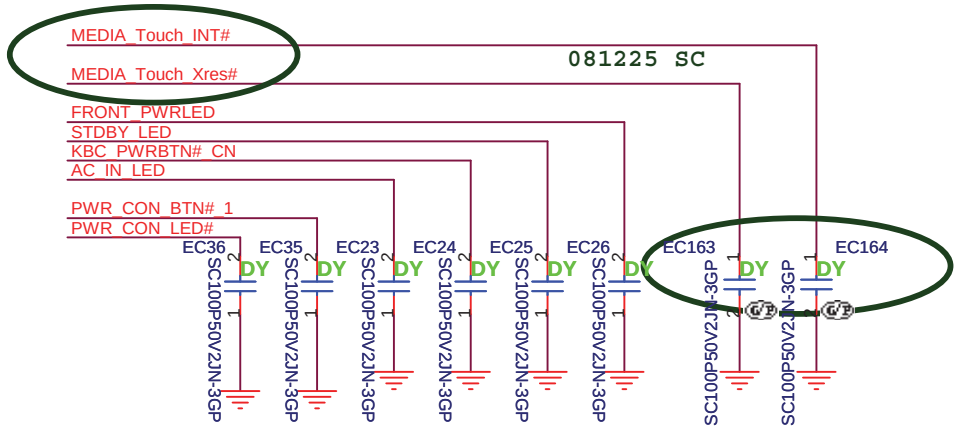
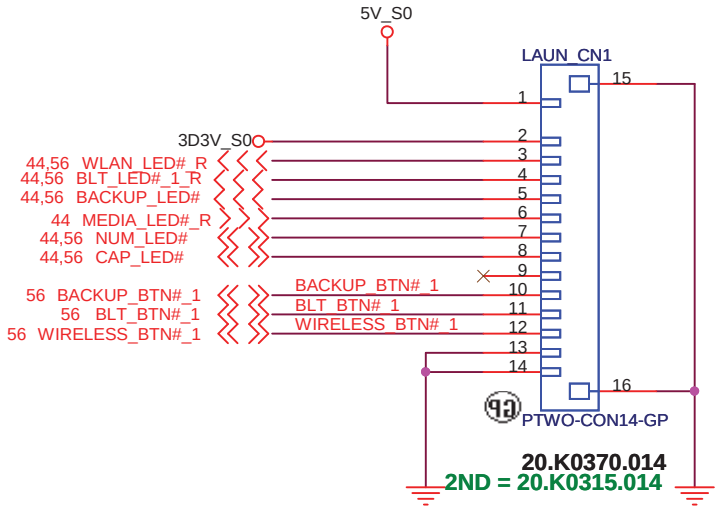
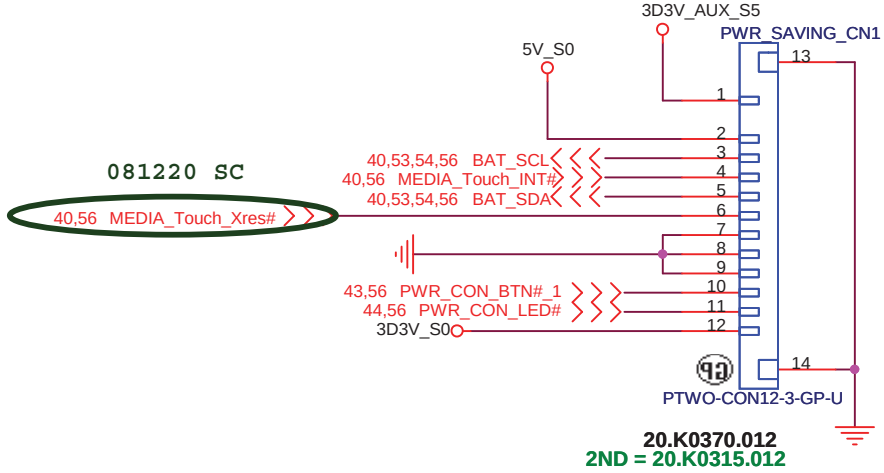
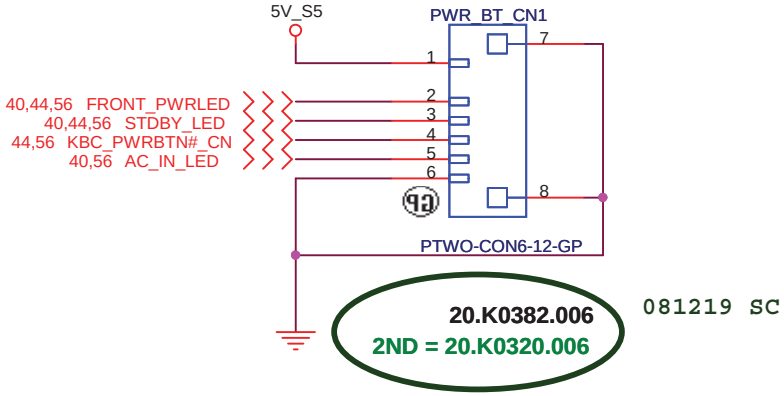
LAUNCH











<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAUNCH & LID**

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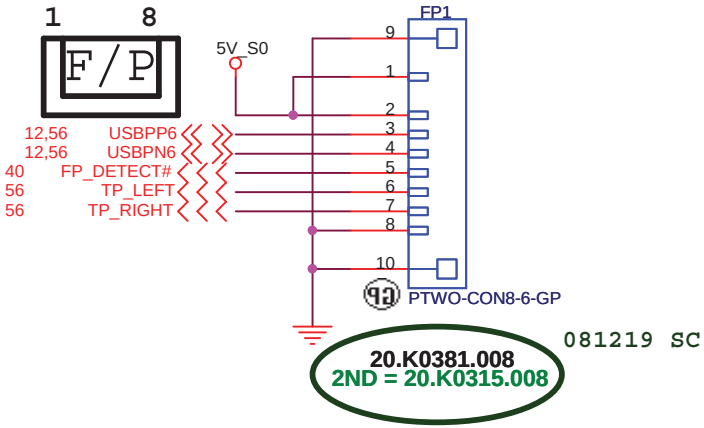
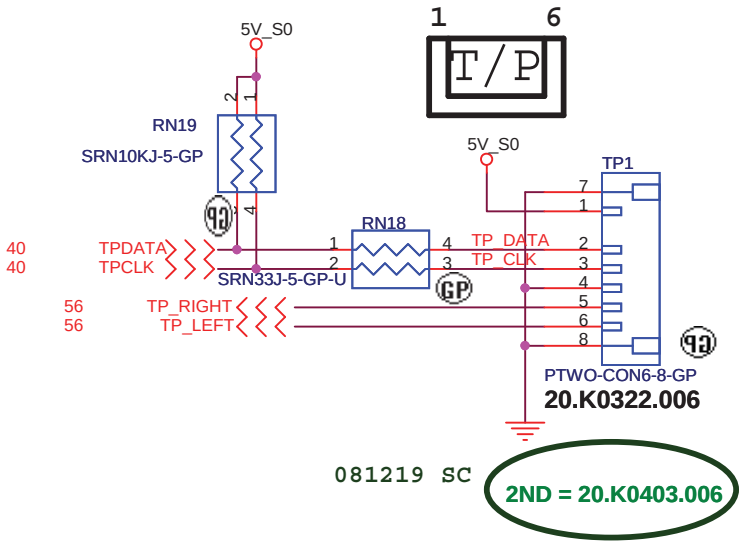
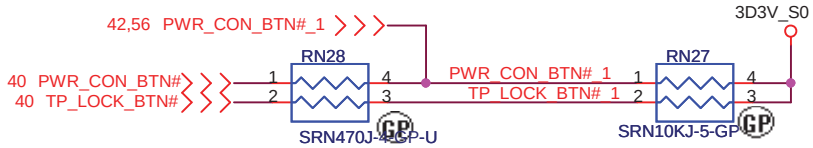
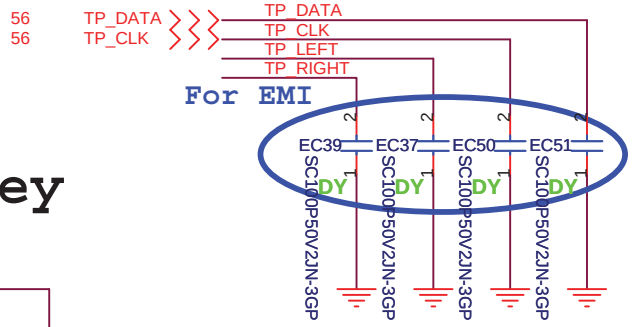
Finger printer



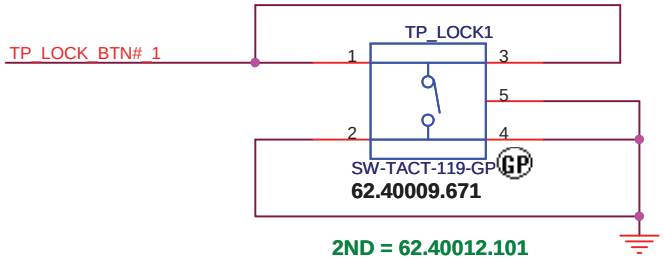
TOUCH PAD







TP_LOCK key



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	Finger Printer	
Size: A4	Document Number: JM70-PU	Rev: -2
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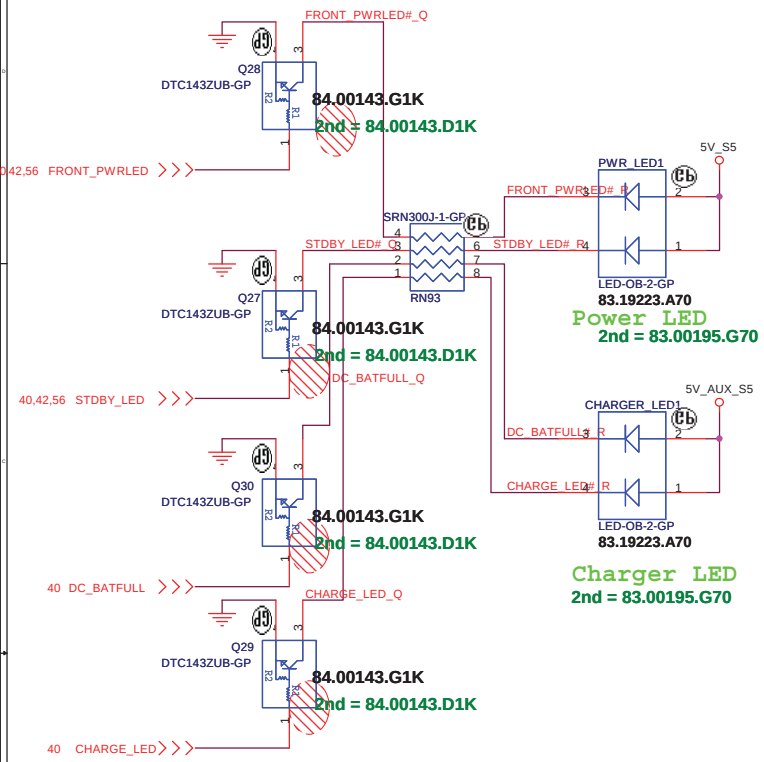
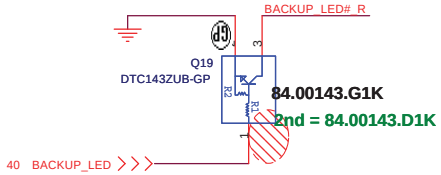
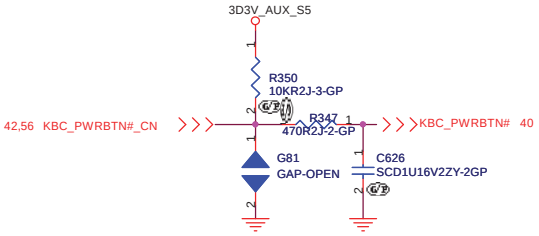
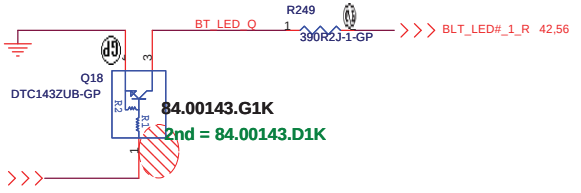
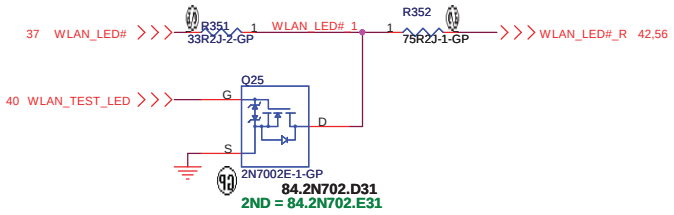
LED

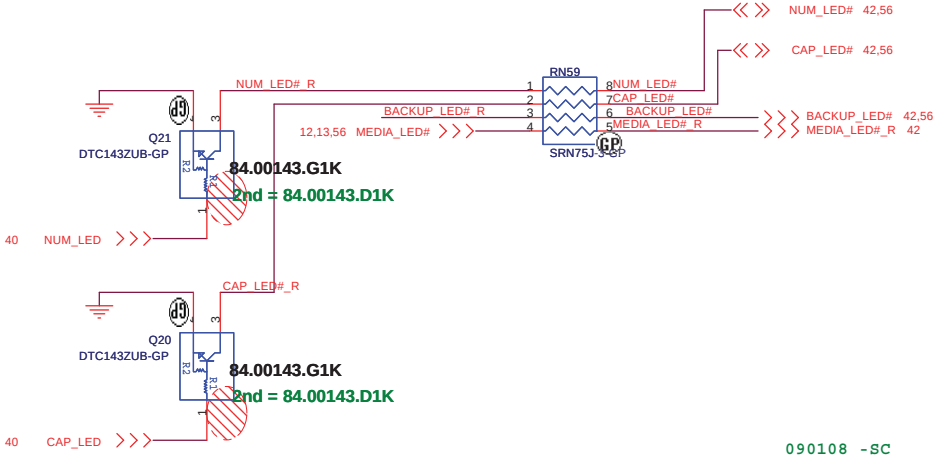


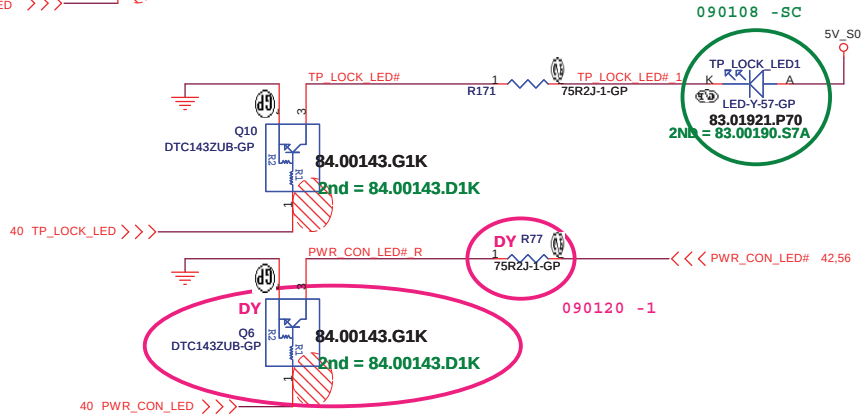












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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED & LAUNCH	
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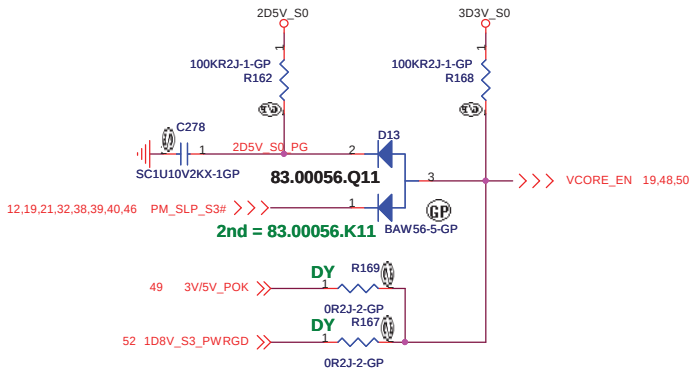
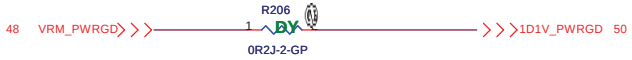
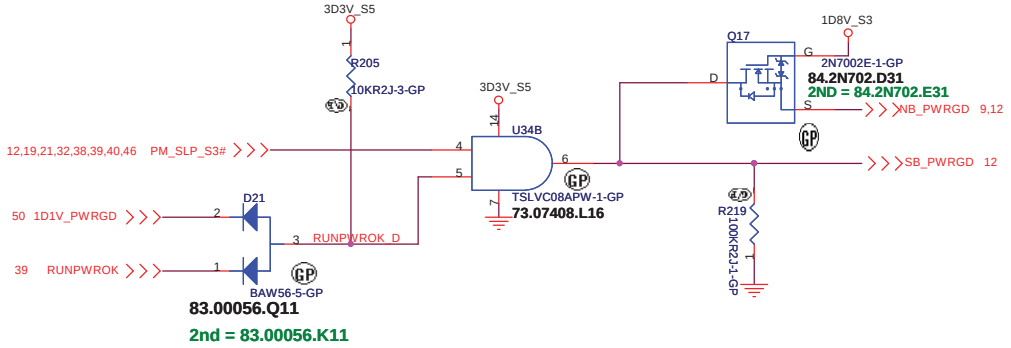


P/H @ 1D8V_S3 PAGE



Reference schematic recommend



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER ON LOGIC

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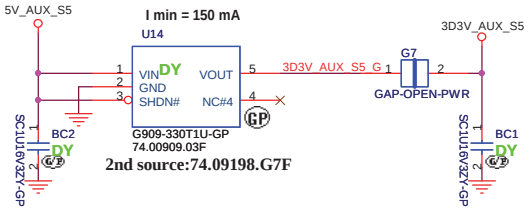
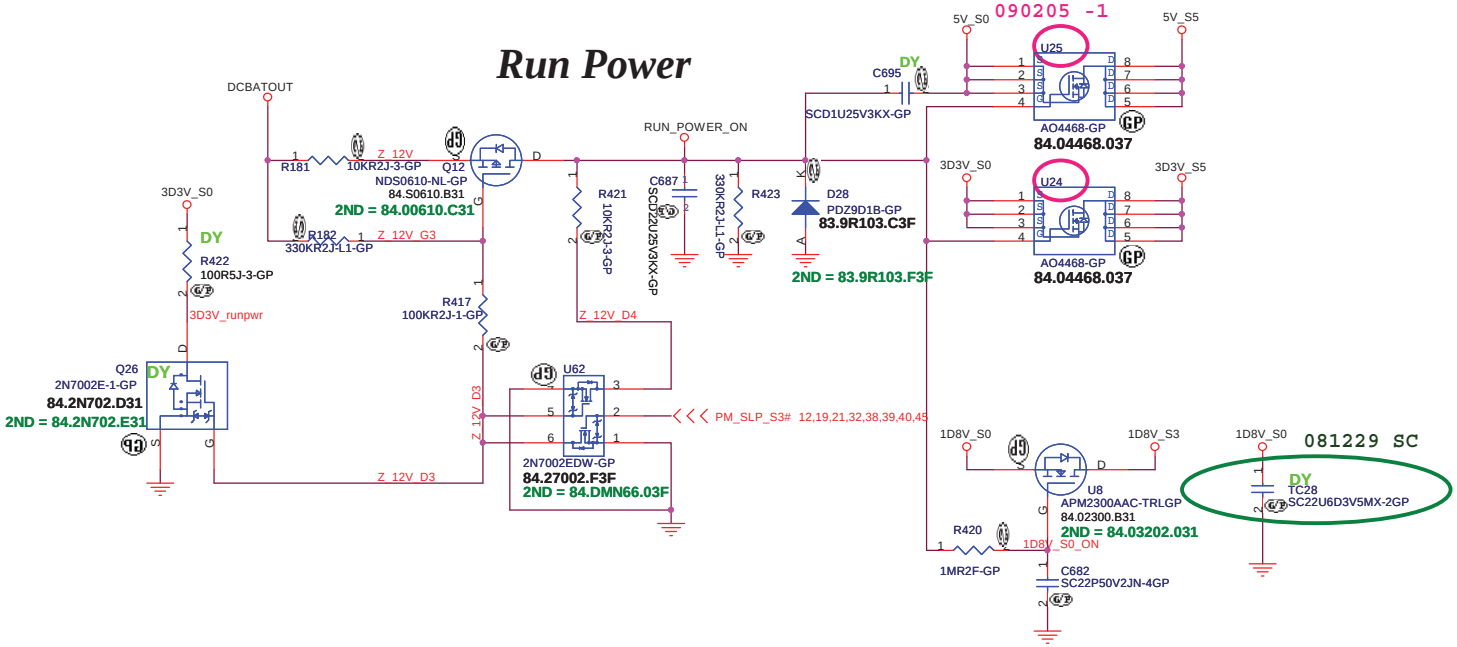
Aux Power

3D3V_AUX_S5

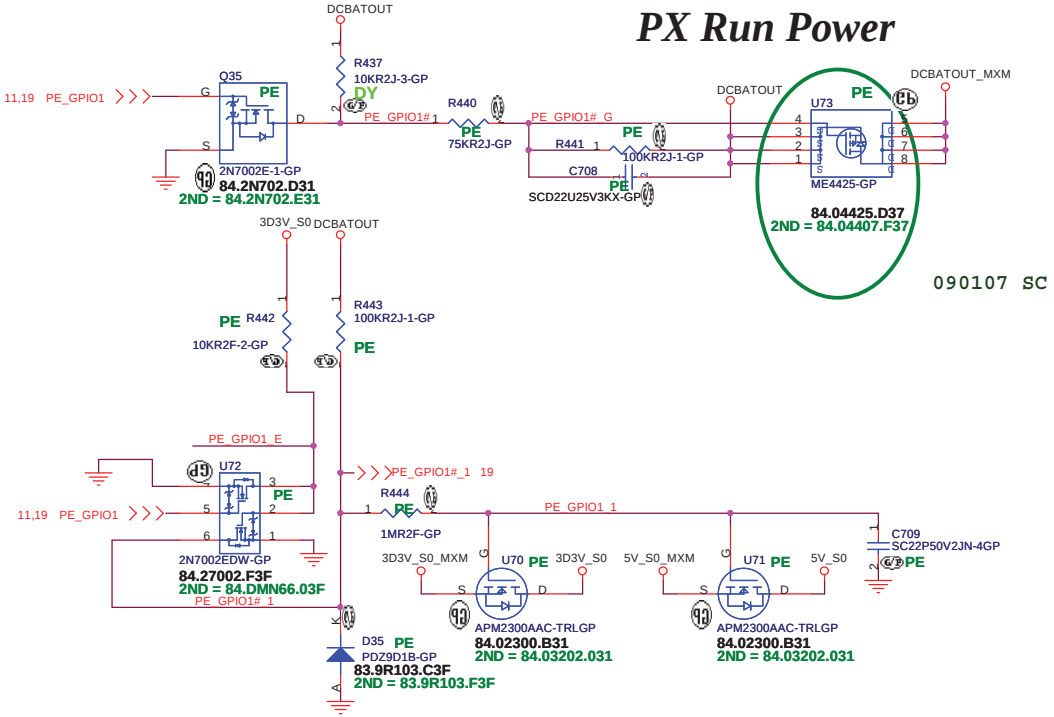


Run Power

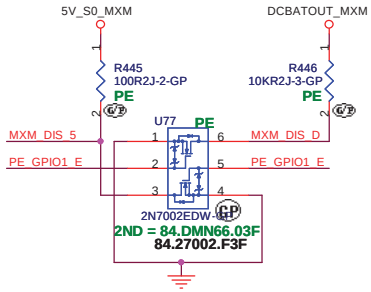
090205 -1



PX Run Power



PX Run Power Discharge circuit



<Core Design>

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Title	RUN POWER and 3D3V_AUX_S5	
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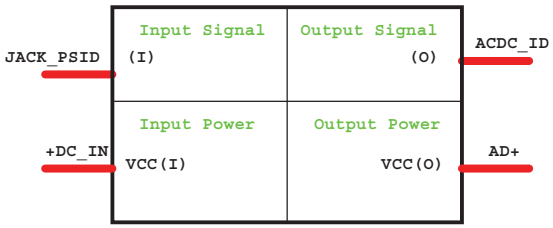
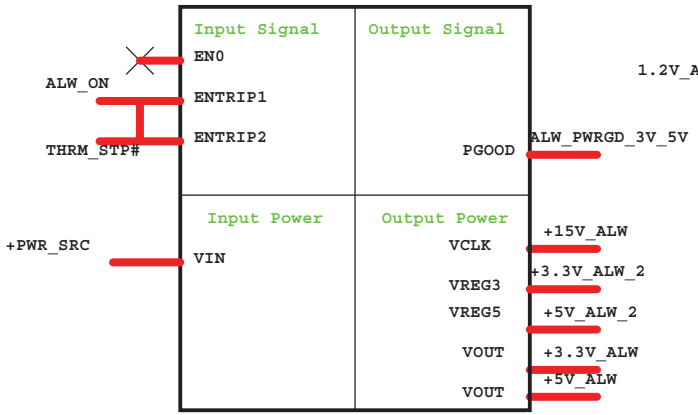
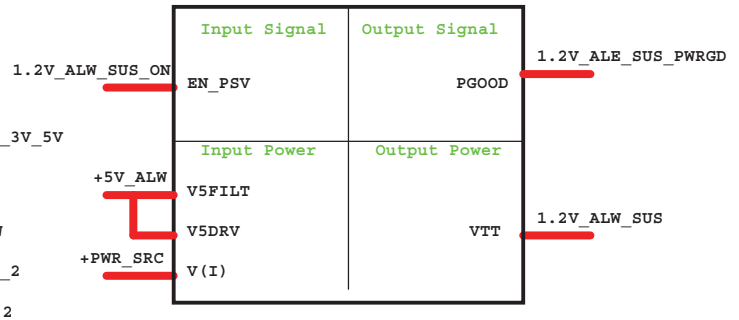
Adapter



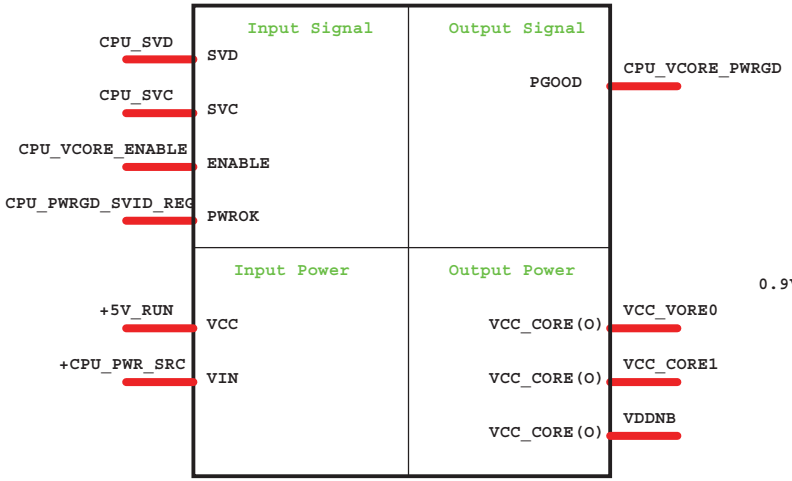
SN0608098



DCDC 1D2V(TPS5117)

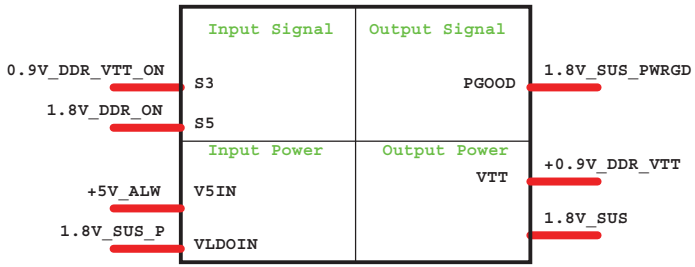


CPU_CORE
ISL6265HRTZ

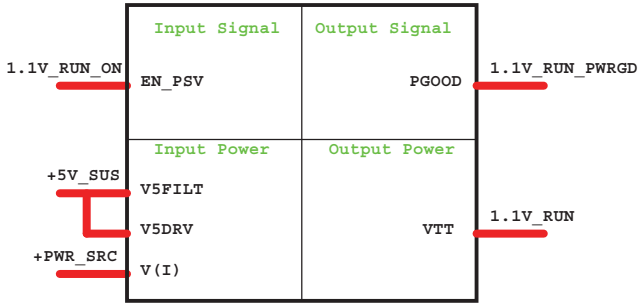


	S3	S5	VDDQ	VTTREF	VTT
S0 S3	1	1	1	1	1
S4 S5	0	0	0	0	0

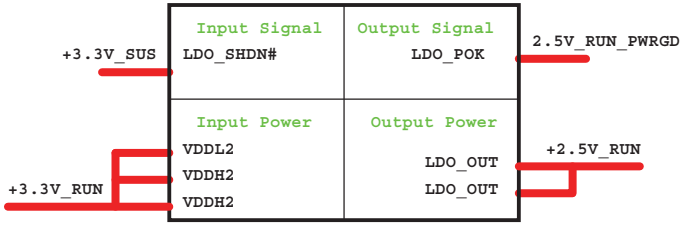
1D8V/0D9V(TPS5116)



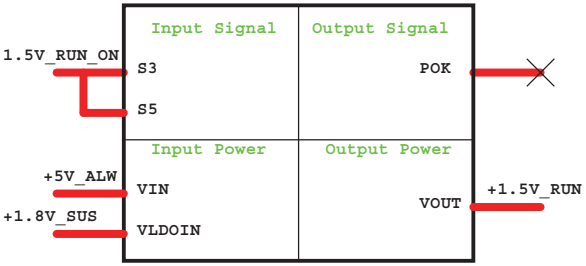
1D1V(TPS5117)



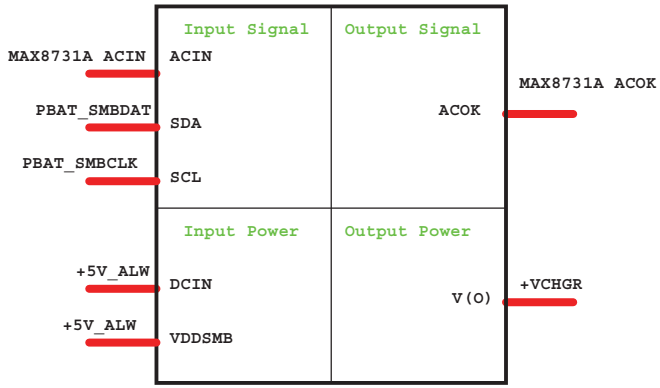
2.5V LDO
EMC4002



1.5V_LDO



CHARGER BQ24745



<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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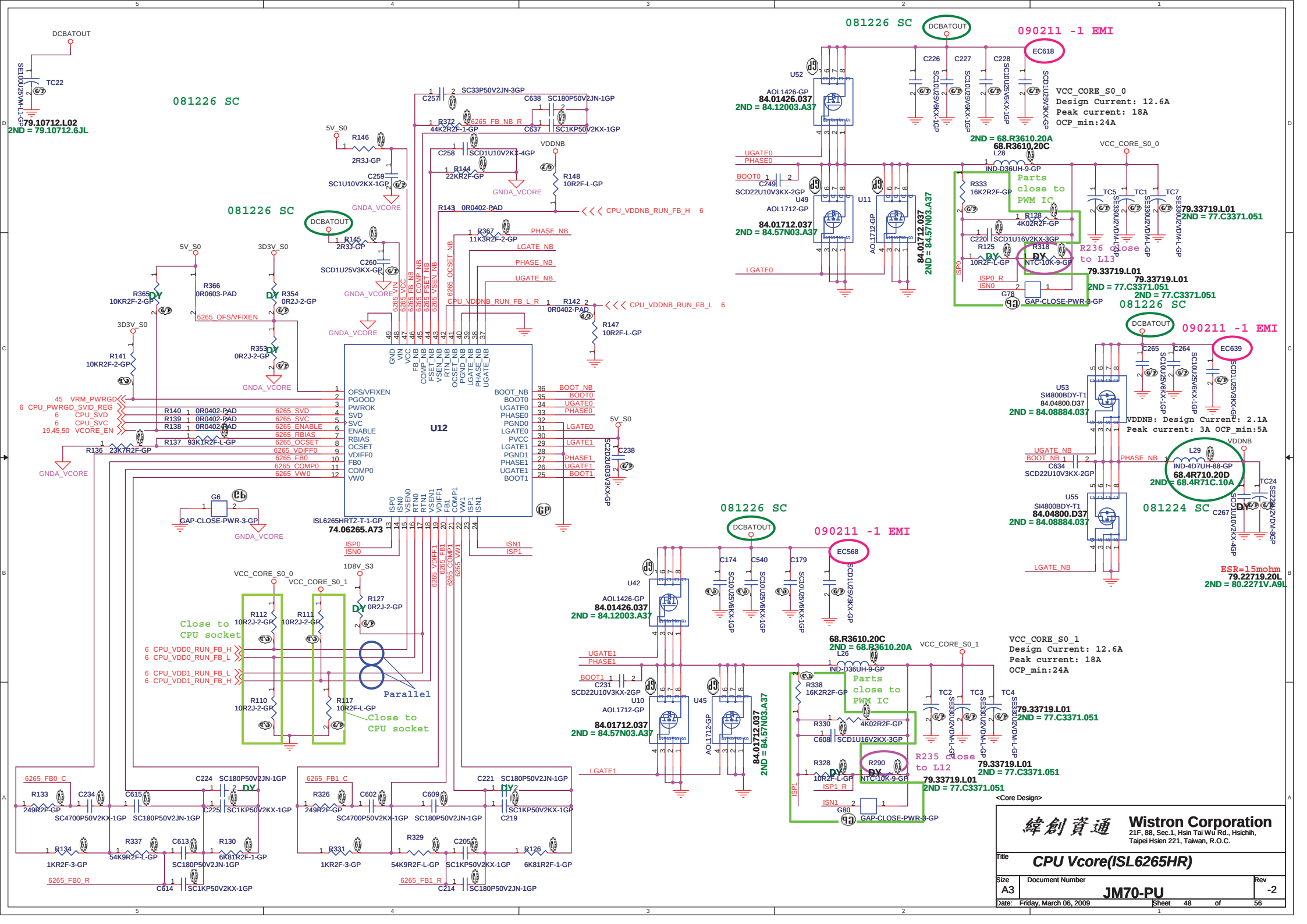
081226 SC
090211 -1 EMI
DCBATOUT
U12
ISL6265HRTZ-T-1-GP
74.06265.A73
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
Parts close to PWM IC
R235 close to L12
R236 close to L13
Close to CPU socket
Parallel
081224 SC
ESR=15mohm
79.22719.20L
2ND = 80.2271V.A9L
79.33719.L01
2ND = 77.C3371.051
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JM70-PU
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Rev -2
Date: Friday, March 06, 2009
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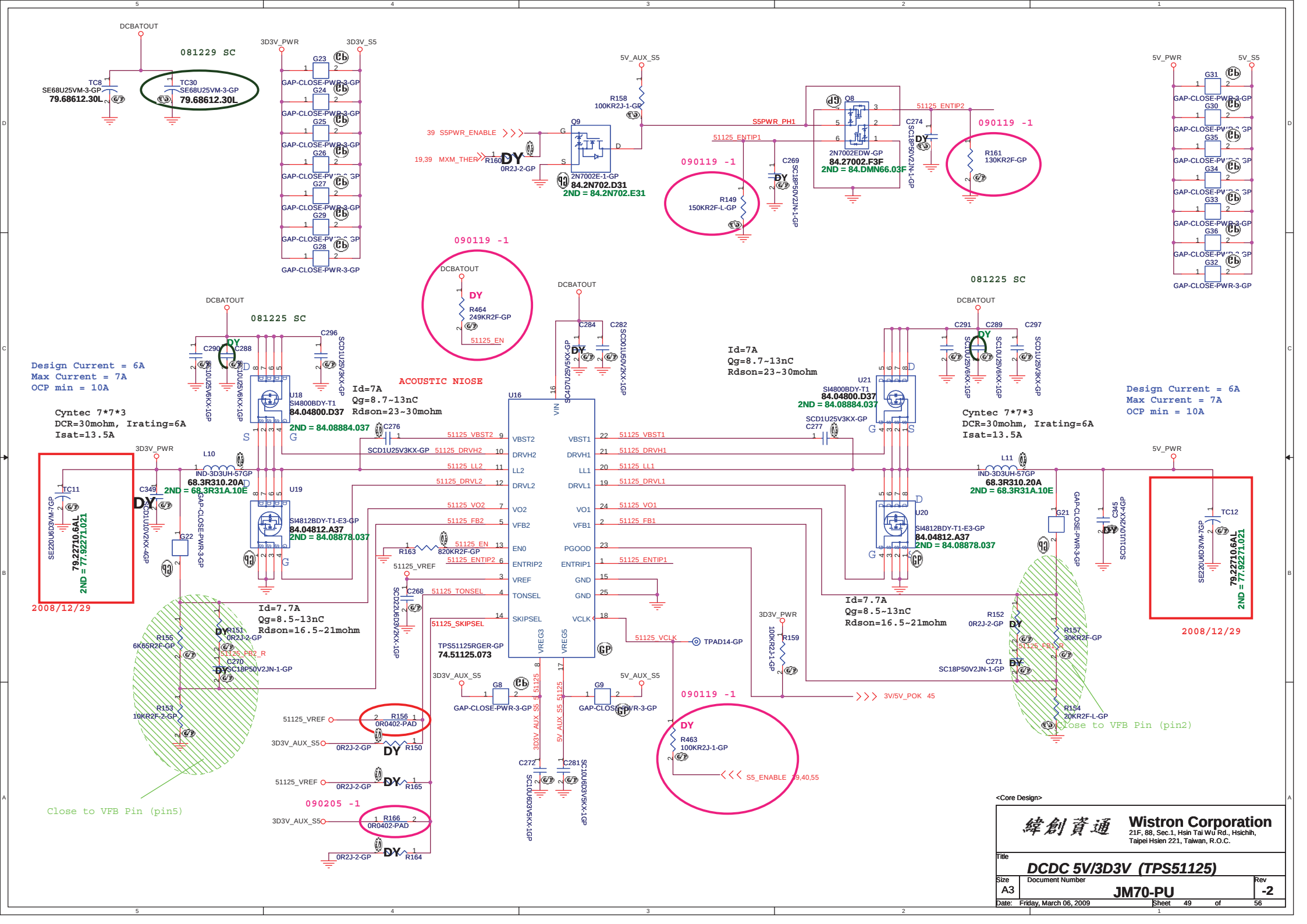
DCBATOUT
081229 SC
TC8
SE68U25VM-3-GP
79.68612.30L
TC30
SE68U25VM-3-GP
79.68612.30L
3D3V_PWR
3D3V_S5
G23
G24
G25
G26
G27
G29
G28
GAP-CLOSE-PWR-3-GP
5V_AUX_S5
R158
100KR2J-1-GP
39 S5PWR_ENABLE
19,39 MXM_THER
R160
0R2J-2-GP
Q9
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
S5PWR_PH1
Q8
2N7002EDW-GP
84.27002.F3F
2ND = 84.DMN66.03F
51125_ENTIP2
51125_ENTIP1
C274
SC18P50V2JN-1-GP
C269
SC18P50V2JN-1-GP
090119 -1
R161
130KR2F-GP
R149
150KR2F-L-GP
5V_PWR
5V_S5
G31
G30
G35
G34
G33
G36
G32
R464
249KR2F-GP
51125_EN
081225 SC
C290
C288
C296
SCD1U25V6KX-1GP
SCD1U25V3KX-GP
U18
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
ACOUSTIC NIOSE
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
C276
SCD1U25V3KX-GP
L10
IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10E
TC11
SE220U6D3VM-7GP
79.22710.6AL
2ND = 77.92271.021
2008/12/29
C349
SCD1U10V2KX-4GP
U19
SI4812BDY-T1-E3-GP
84.04812.A37
2ND = 84.08878.037
G22
GAP-CLOSE-PWR-3-GP
U16
TPS51125RGER-GP
74.51125.073
VIN
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
ENTRIP1
GND
VCLK
VREG3
VREG5
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_ENTIP1
51125_VCLK
R163
820KR2F-GP
51125_VREF
C268
SCD22U6D3V2KX-1GP
TPAD14-GP
R155
6K65R2F-GP
R151
0R2J-2-GP
51125_FB2_R
C270
SC18P50V2JN-1-GP
R153
10KR2F-2-GP
Close to VFB Pin (pin5)
3D3V_AUX_S5
5V_AUX_S5
G8
G9
GAP-CLOSE-PWR-3-GP
R156
0R0402-PAD
R150
0R2J-2-GP
R165
0R2J-2-GP
090205 -1
R166
0R0402-PAD
R164
0R2J-2-GP
C272
C281
SC10U6D3V5KX-1GP
090119 -1
R463
100KR2J-1-GP
S5_ENABLE 19,40,55
3V/5V_POK 45
R159
100KR2J-1-GP
R152
0R2J-2-GP
R157
30KR2F-GP
C271
SC18P50V2JN-1-GP
R154
20KR2F-L-GP
Close to VFB Pin (pin2)
C291
C289
C297
SCD1U25V6KX-1GP
SC10U25V6KX-1GP
SCD1U25V3KX-GP
U21
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
U20
SI4812BDY-T1-E3-GP
84.04812.A37
2ND = 84.08878.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Design Current = 6A
Max Current = 7A
OCP min = 10A
L11
IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10E
C345
SCD1U10V2KX-4GP
TC12
SE220U6D3VM-7GP
79.22710.6AL
2ND = 77.92271.021
2008/12/29
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (TPS51125)
Size
A3
Document Number
JM70-PU
Rev
-2
Date: Friday, March 06, 2009
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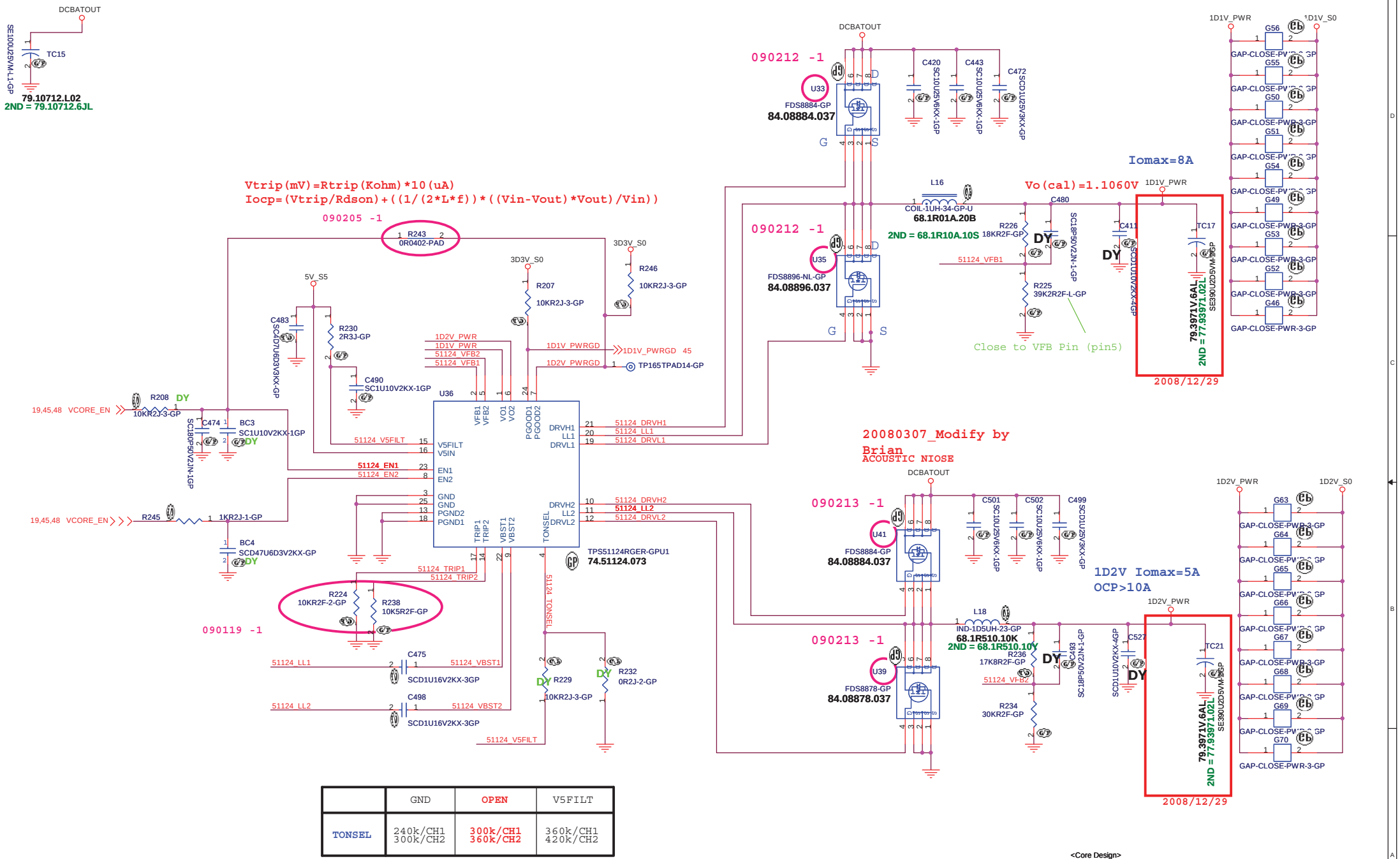


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

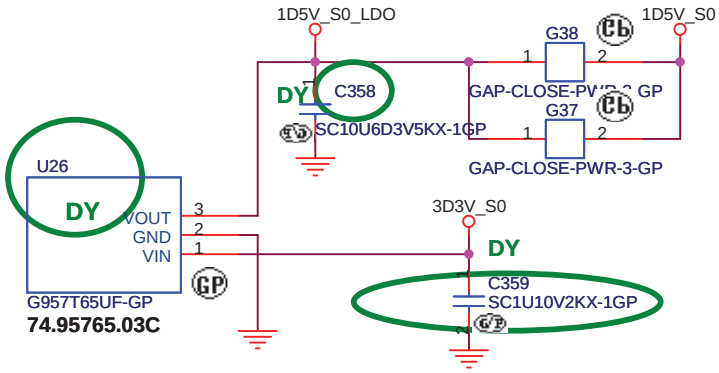
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51124_1D1V_1D2V	
Size A3	Document Number JM70-PU	Rev -2
Date: Friday, March 06, 2009	Sheet 50 of 56	

G957

1D5V_S0
Iomax=1A



081230 SC

1D2V_S5
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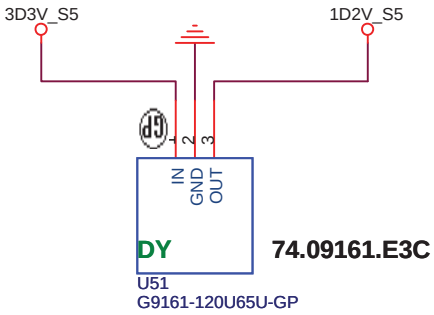

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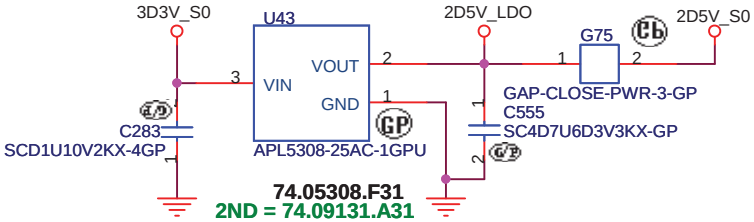
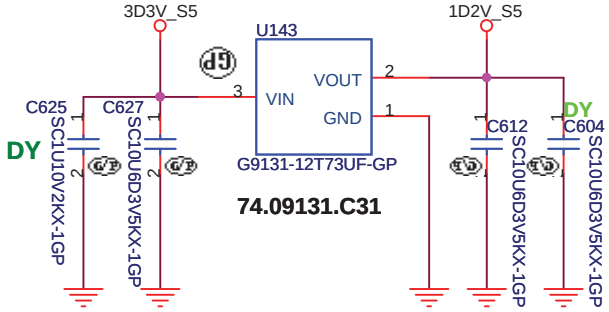
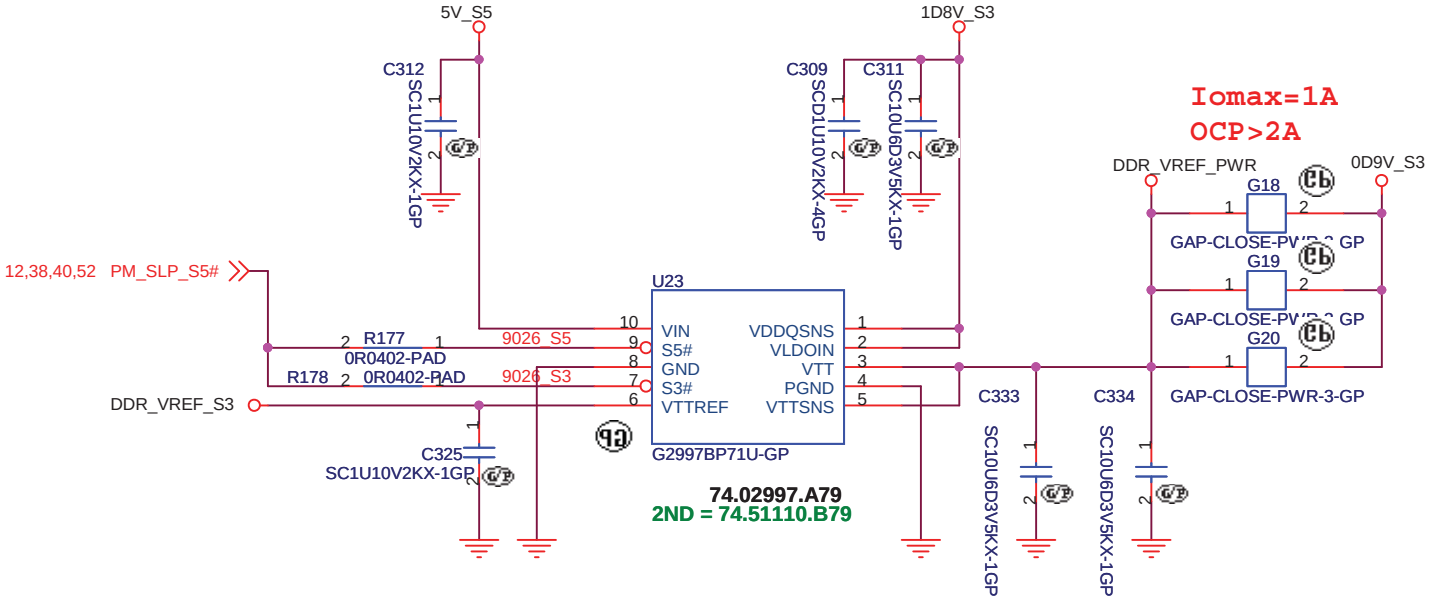


Place near to SB700





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Title: 0D9V&2D5V&1D25V&1D5V

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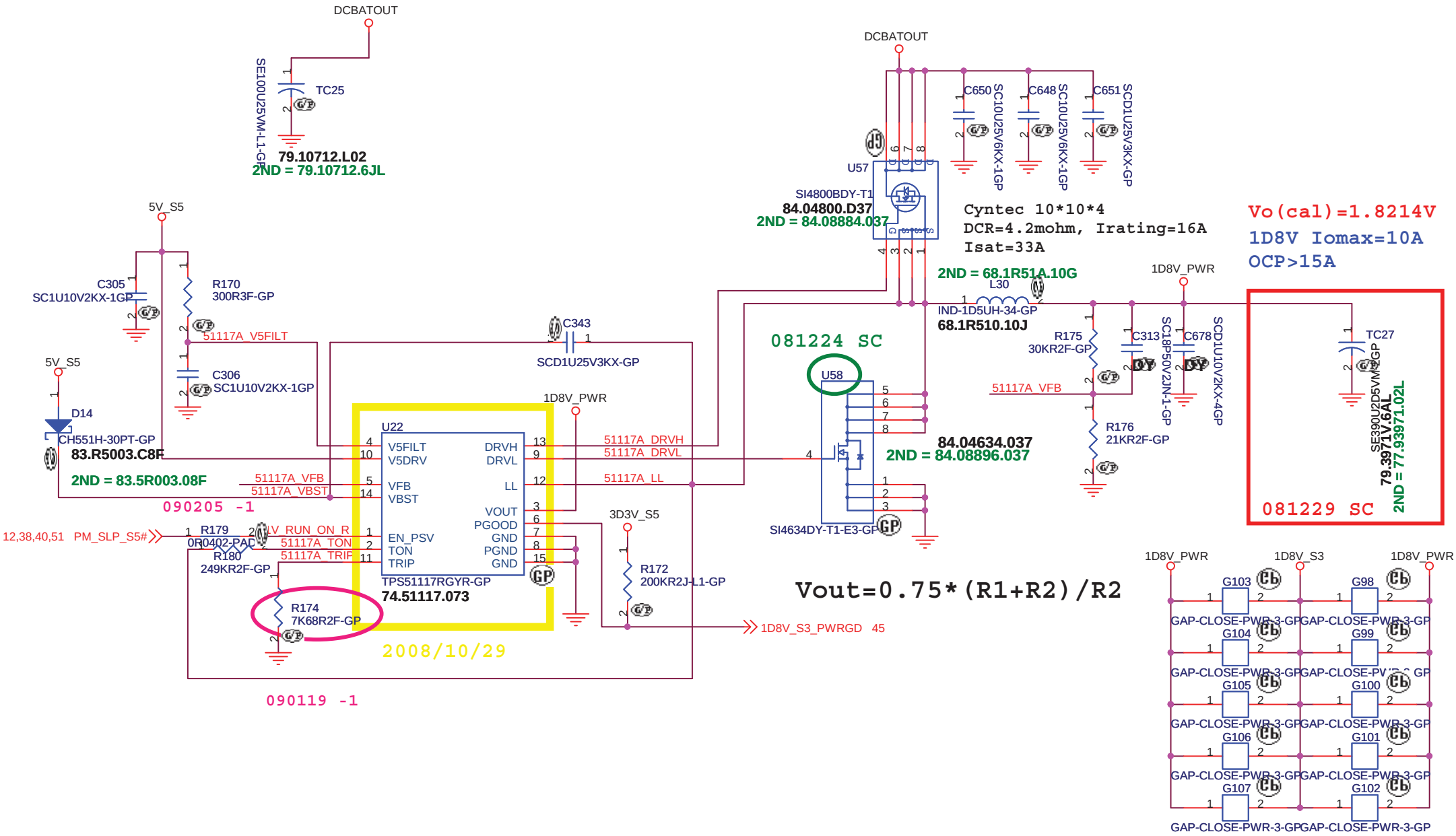

<Core Design>

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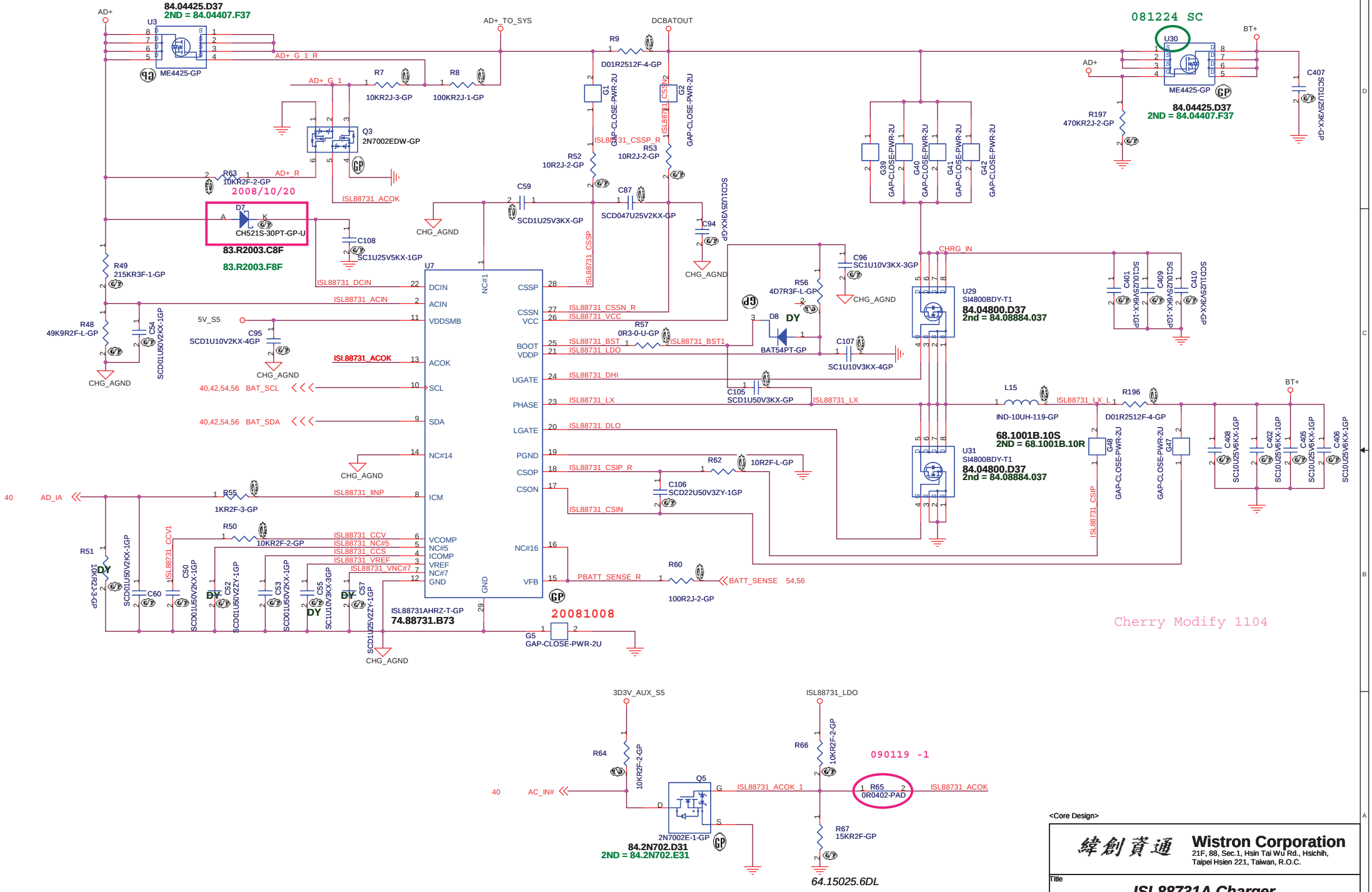
Title	***1D8V(TPS5117)***	
Size: A4	Document Number: **JM70-PU**	Rev: -2
Date: Friday, March 06, 2009	Sheet 52 of 56	



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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *ISL88731A Charger*

Size	Document Number	Rev
A3	JM70-PU	-2

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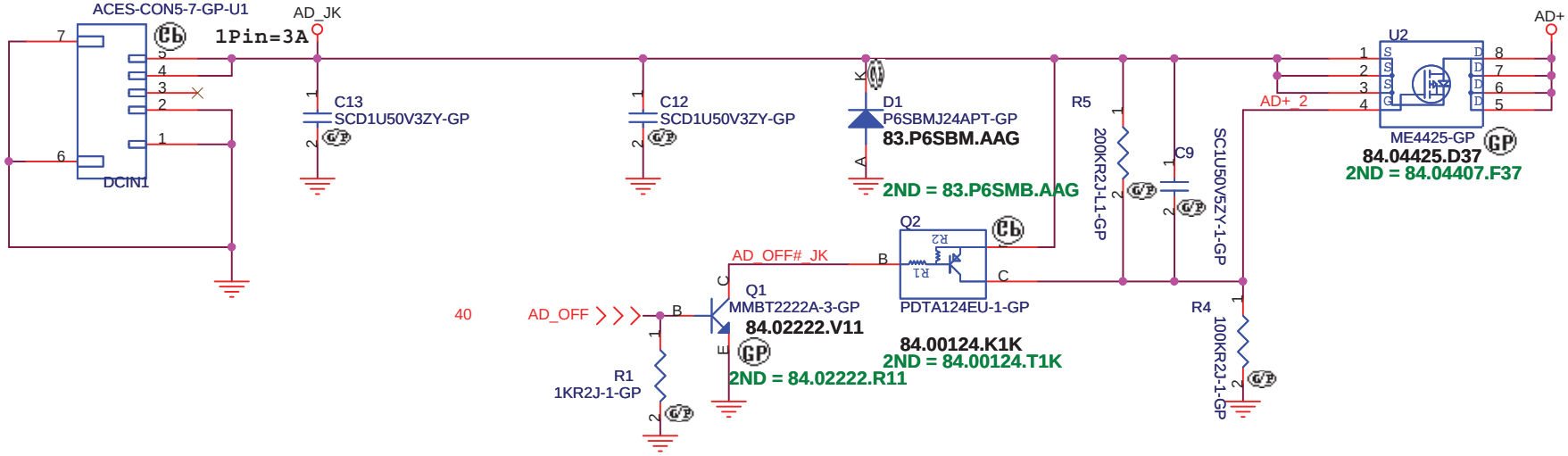
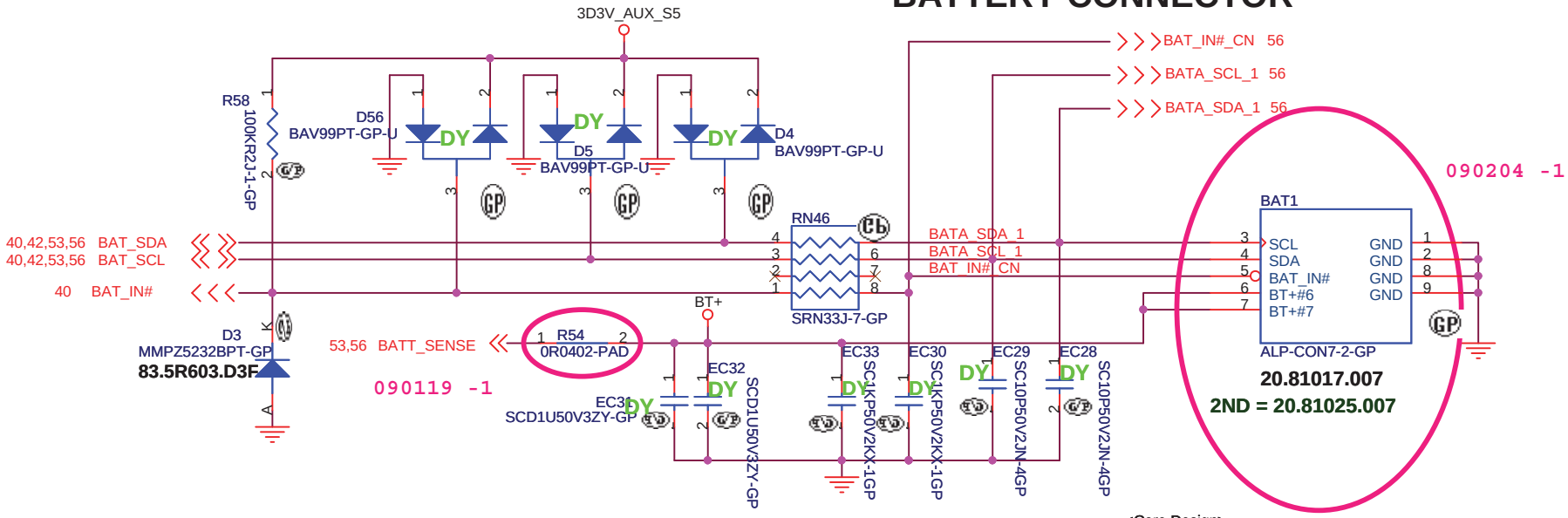
20.F1002.005

Adaptor in to generate DCBATOUT

2ND = 20.F1170.005

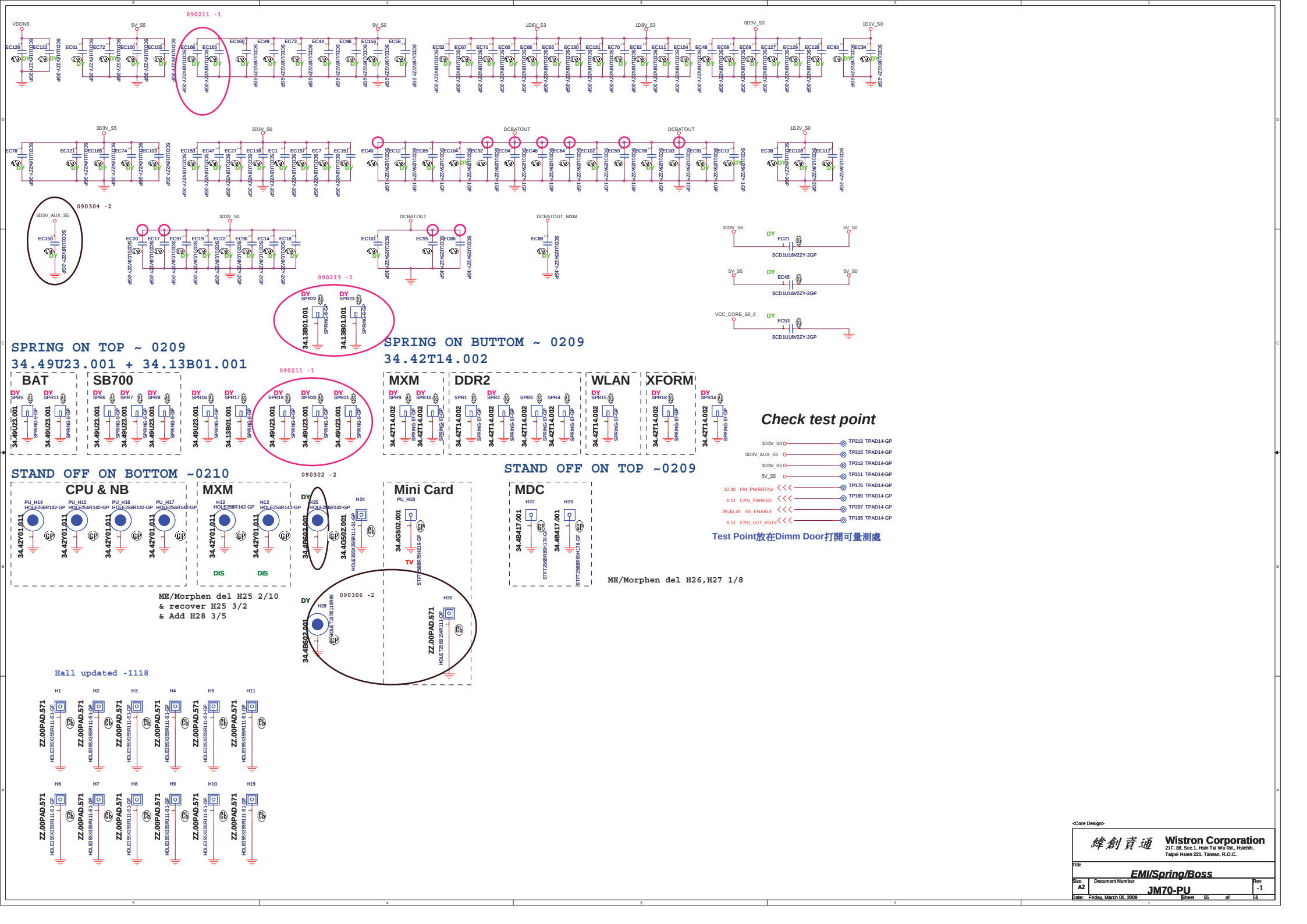


BATTERY CONNECTOR



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***AD/BATT CONN***	
Size **A4**	Document Number **JM70-PU**	Rev -2
Date: Friday, March 06, 2009	Sheet 54 of 56	



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size	Document Number	Rev
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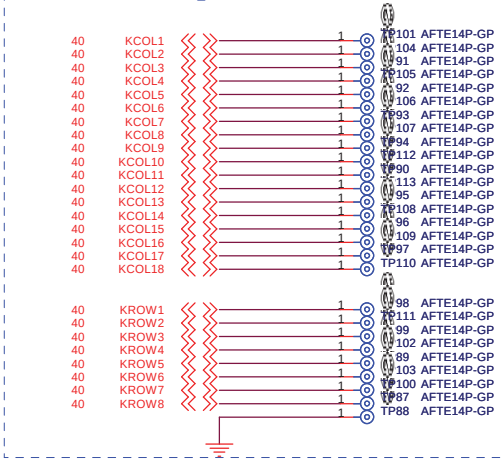
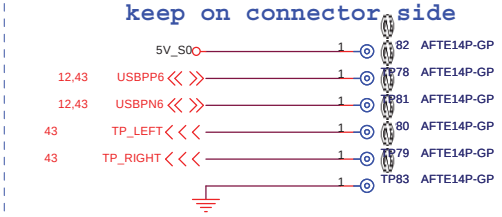
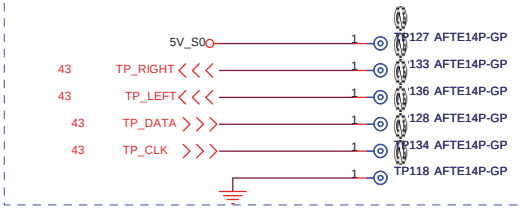
KB1 Conn. Test Point keep on connector side



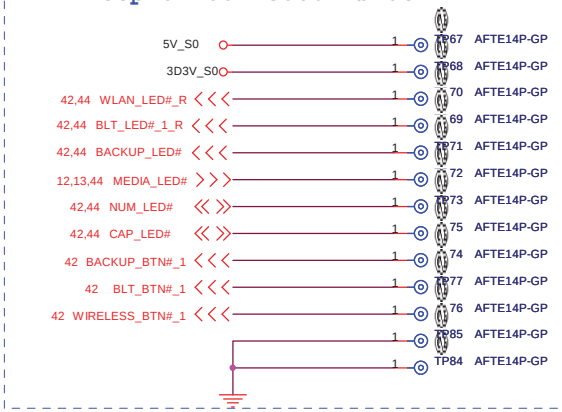
FP test Point keep on connector side



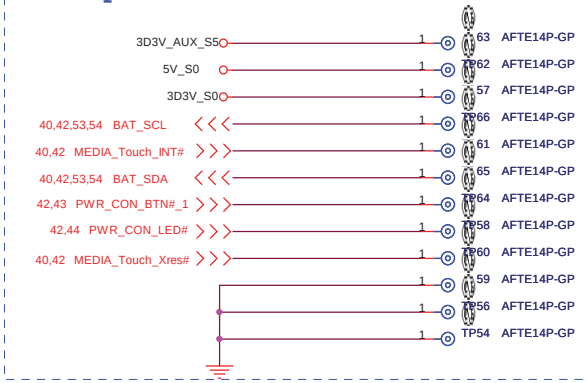
TOUCH PAD Conn. Test Point keep on connector side



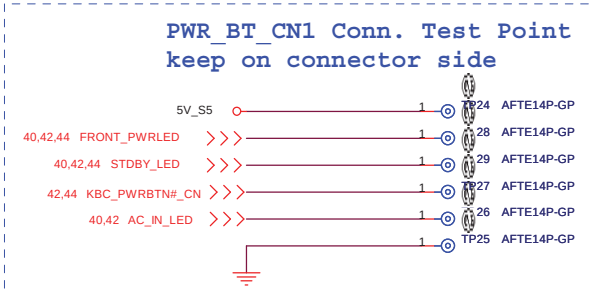
LAUN_CN1 Conn. Test Point keep on connector side



PWR_SAVING_CN1 Conn. Test Point keep on connector side

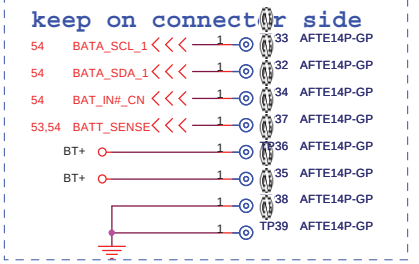


PWR_BT_CN1 Conn. Test Point keep on connector side

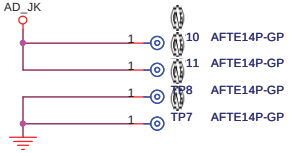


FAN1

BAT1 Conn. Test Point keep on connector side



DC1 Test Point keep on connector side



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AFTE**

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