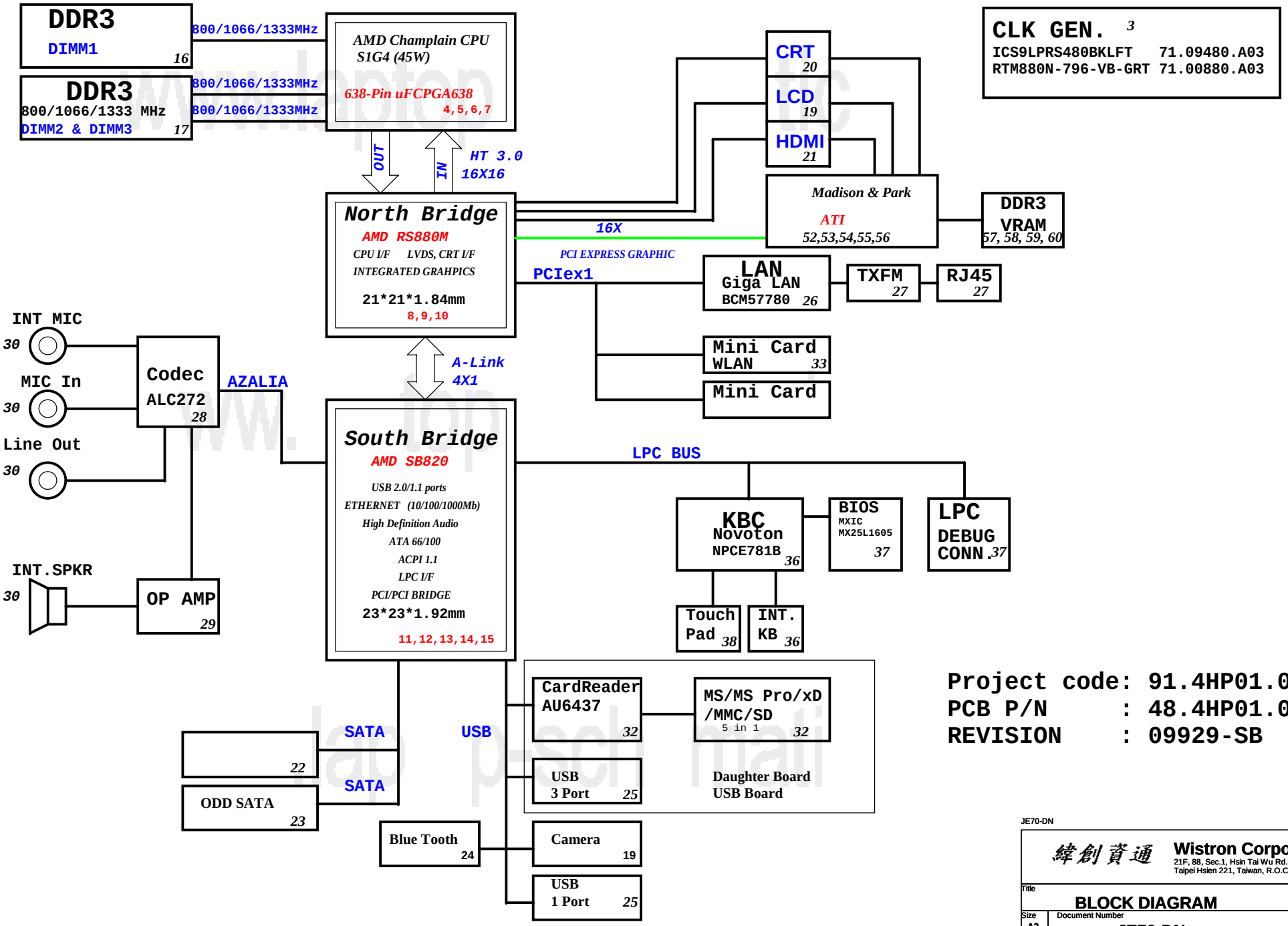
Block Diagram



Project code: 91.4HP01.001
PCB P/N : 48.4HP01.0SB
REVISION : 09929-SB

JE70-DN

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Monday, December 07, 2009 Sheet 1 of 63

page36

EC Functional Strap Definitions

Signal	Comment
TEST# pin110	Test Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to determine the device operation mode as follows: **No pull-down resistor: Normal operation mode (XORTR and TRIST strap pins are ignored).** 10 KΩ external pull-down resistor:Test mode (ICT or XOR-Tree Test mode, according to XORTR and TRIST strap pins).
XORTR# pin111	XOR-Tree Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the XOR-Tree Test mode, if TEST is strapped low: No pull-down resistor: Not allowed if TEST pin is strapped low. **10 KΩ external pull-down resistor:XOR-Tree Test mode .Note: TRIST strap pin must be left unconnected.**
TRIST# pin112	ICT Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the ICT Test mode, if TEST is strapped low: **No pull-down resistor: Not allowed if TEST pin is strapped low.** 10 KΩ external pull-down resistor:ICT Test mode (see Section 3.4.1 on page 53), forces the device to float its output and I/O pins.Note: XORTR strap pin must be left unconnected.
JEN0#, JENK# pin49,53	JTAG Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the JTAG signals to device pins (see Table 4 on page 35 for details). **Both JEN0 and JENK, are pulled to 1 by an internal resistor** The external 10 KΩ pull-down resistor must be connected to GND.
SHBM pin83	Shared Host BIOS Memory. Sampled at VCC Power-Up reset or VCC_POR Input reset, to determine the state of the shared BIOS memory. **No pull-down resistor:Disable the shared BIOS memory.** 10 KΩ external pull-down resistor:Enable the shared BIOS memory
SDP_VIS# pin41	Port80 (SDP) Visibility Mode Select. Sampled at VCC Power-Up reset or VCC_POR Input reset, to select the Visibility mode for the Port80 (SDP). **No pull-down resistor: SDP in Normal mode** 10 KΩ external pull-down resistor:SDP in Visibility mode.
XOR_OUT pin35	XOR-Tree Output. The device pins are internally connected in a XOR-tree structure

page9

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)

*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS880 use HSYNC#)

*1 :Disable 0 : Enable

dware Default Values

SUS_STAT#

Selects Loading of STRAPS From EEPROM

*1 : Bypass the loading of EEPROM straps and use Har

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

page15

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

page15

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

page12

	USB	
	Pair	Device
	12	MINI2 CARD
	11	NC
	10	NC
	9	CCD
	8	NC
	7	Bluetooth
	6	USB3
OCP3#	5	USB2
	4	CardReader
	3	NC
OCP2#	2	USB4
	1	MINI1 CARD
OCP0#	0	USB1

SYSTEM DC/DC RT8223 *45*

INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)

SYSTEM DC/DC RT8209E *46*

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC RT8015A *47*

INPUTS	OUTPUTS
DCBATOUT	1D8V_S0

RT9025 *48*

5V_S5	1D05V_S0

RT9161 *48*

3D3V_S0	2D5V_S0 (200mA)

RT9025 *48*

3D3V_S0	1V_VGA (1.2A)

RT9025,RT8209E *47*

3D3V_S5	1D1V_S5
5V_S5	1D1V_S0

CHARGER BQ24745 *49*

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR *44*

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

PCB STACKUP

TOP

VCC

S

S

GND

BOTTOM

Daughter Board
Power Board(09744-SB)

Daughter Board
Power Board(09741-SB)

Daughter Board
Power Board(09742-SB)

JE70-DN

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Title: Reference

Size: A3 | Document Number: JE70-DN | Rev: SB

Date: Thursday, November 19, 2009 | Sheet 2 of 63

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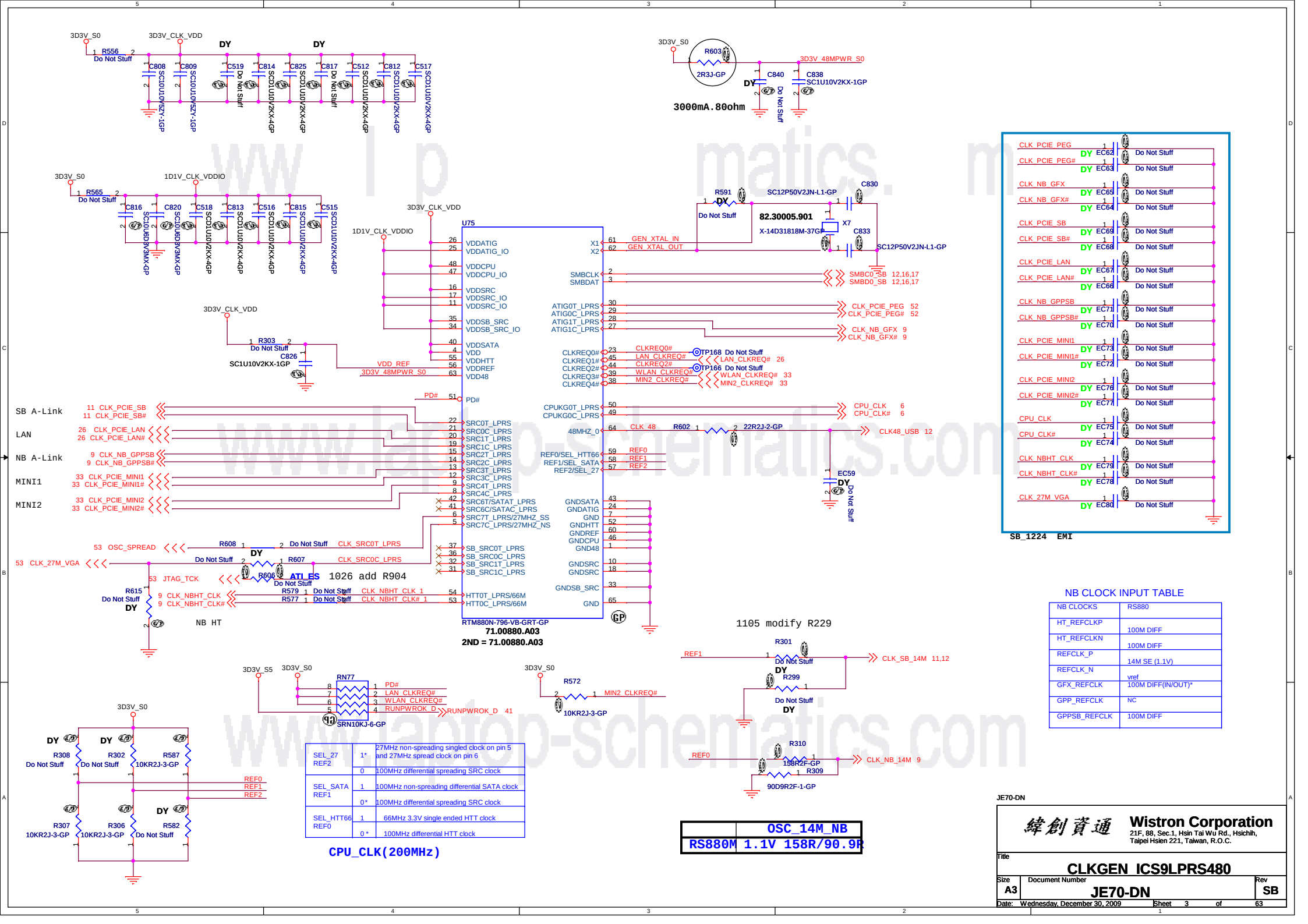
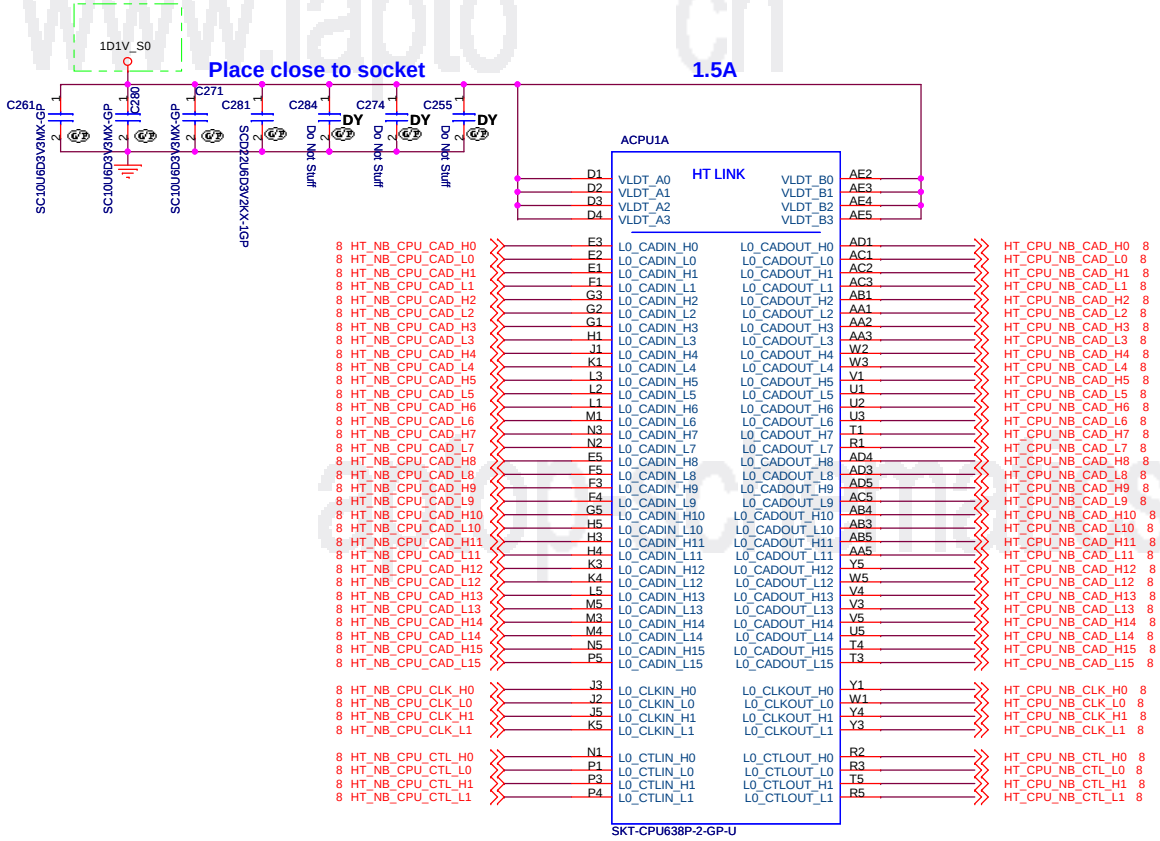


NB CLOCKS	RS880
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC
GPPSB_REFCLK	100M DIFF

SEL_27 REF2	1*	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0*	100MHz differential HTT clock

OSC_14M_NB
RS880M 1.1V 158R/90.9R

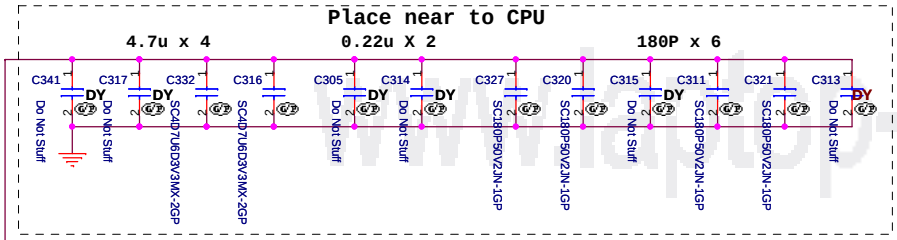


62.10055.181

SKT-BGA638H176

JE70-DN

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **CPU_HT_LINK I/F (1/4)**		
Size: A3	Document Number: **JE70-DN**	Rev: SB
Date: Wednesday, December 30, 2009	Sheet 4 of 63	



1D05V_S0

1500 mA

CLOSE TO CPU

1D5V_S3

C364 SCD1U10V2KX-4GP

VREF_DDR_CLAW

SRN1KJ-7-GP RN13

C359 SC1KP50V2KX-1GP

C358 SCD1U10V2KX-4GP

1110 swap RN48

R429 39D2R2F-L-GP

R432 39D2R2F-L-GP

TP49 Do Not Stuff

ACPU1B

MEM:CMD/CTRL/CLK

VDDR

SKT-CPU638P-2-GP-U

62.10055.181

ACPU1C

MEM:DATA

SKT-CPU638P-2-GP-U

JE70-DN

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Title: CPU_DDR_(2/4)	
Size: A3	Document Number: JE70-DN	Rev: SB
Date: Wednesday, December 30, 2009	Sheet 5 of 63

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

1026 modify RN84,R612,R611

1029 delete R612

SB_1218

S1G3&S1G4 not support LDTREQ_L(CPU_LDT_REQ#_CPU)

Cloce To CPU

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

For HDT DBG

1105 modify R366

internal pull high 300 ohm

1105 modify Q8,R81,R375,C205

Near CPU PIN

1105 delete R104,R105,R108,R110
1105 add RN137,RN138
1107 swap RN137

LAYOUT: Route FBCLKOUT_H/L

differentially impedance 80

1026 modify R364
1029 delete R364 and add RN127,R946

1102 swap these nets

1026 modify RN42

CPU exceeds to 125℃

2ND = 84.03904.L06

HDT Connectors

ACPU1D

SKT-CPU638P-2-GP-U

www.lap-schematics.com
top-schematics.com

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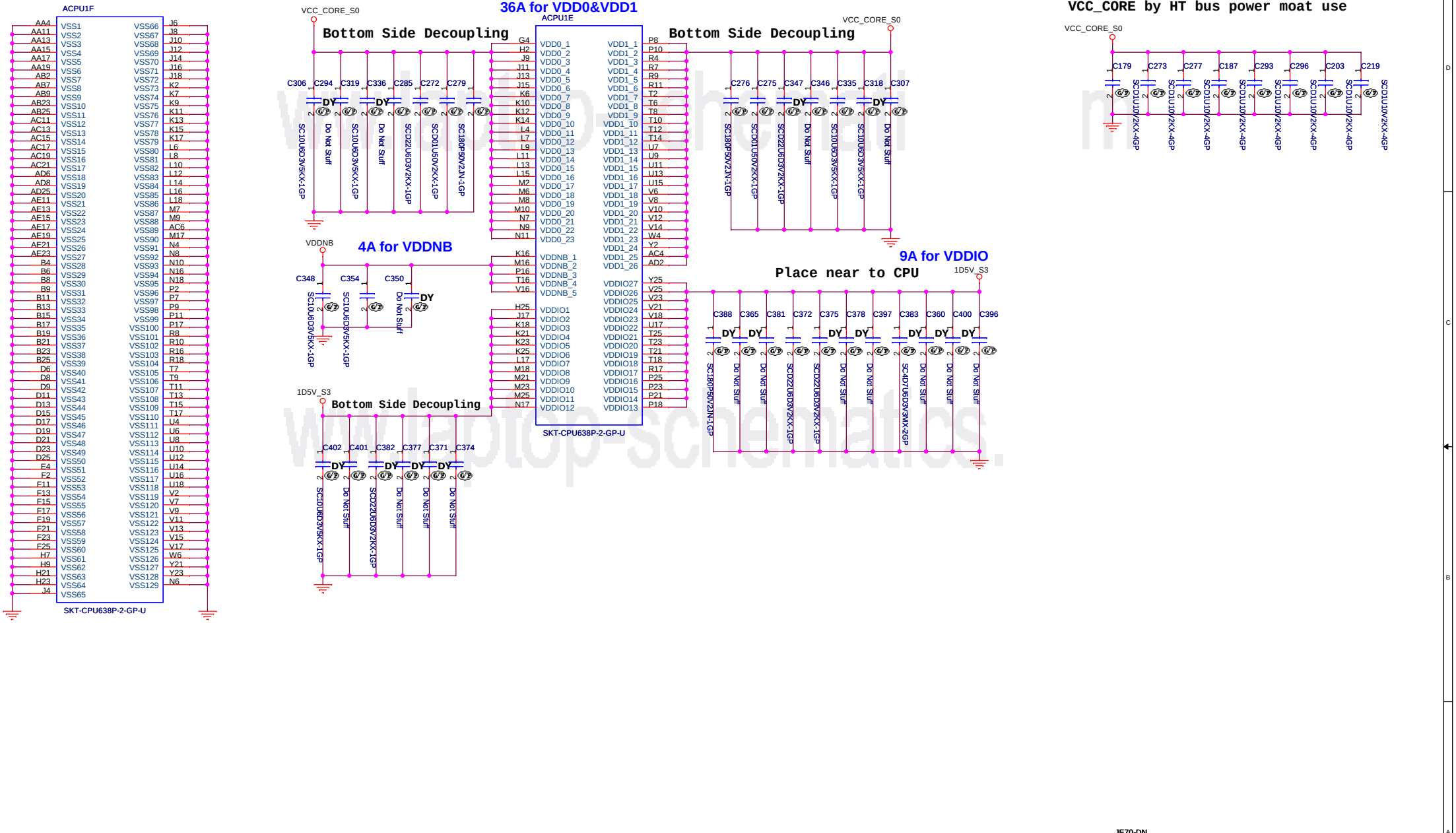
Title: CPU_Control&Debug_(3/4)

Size: A3 | Document Number: JE70-DN | Rev: SB

Date: Wednesday, December 30, 2009 | Sheet 6 of 63



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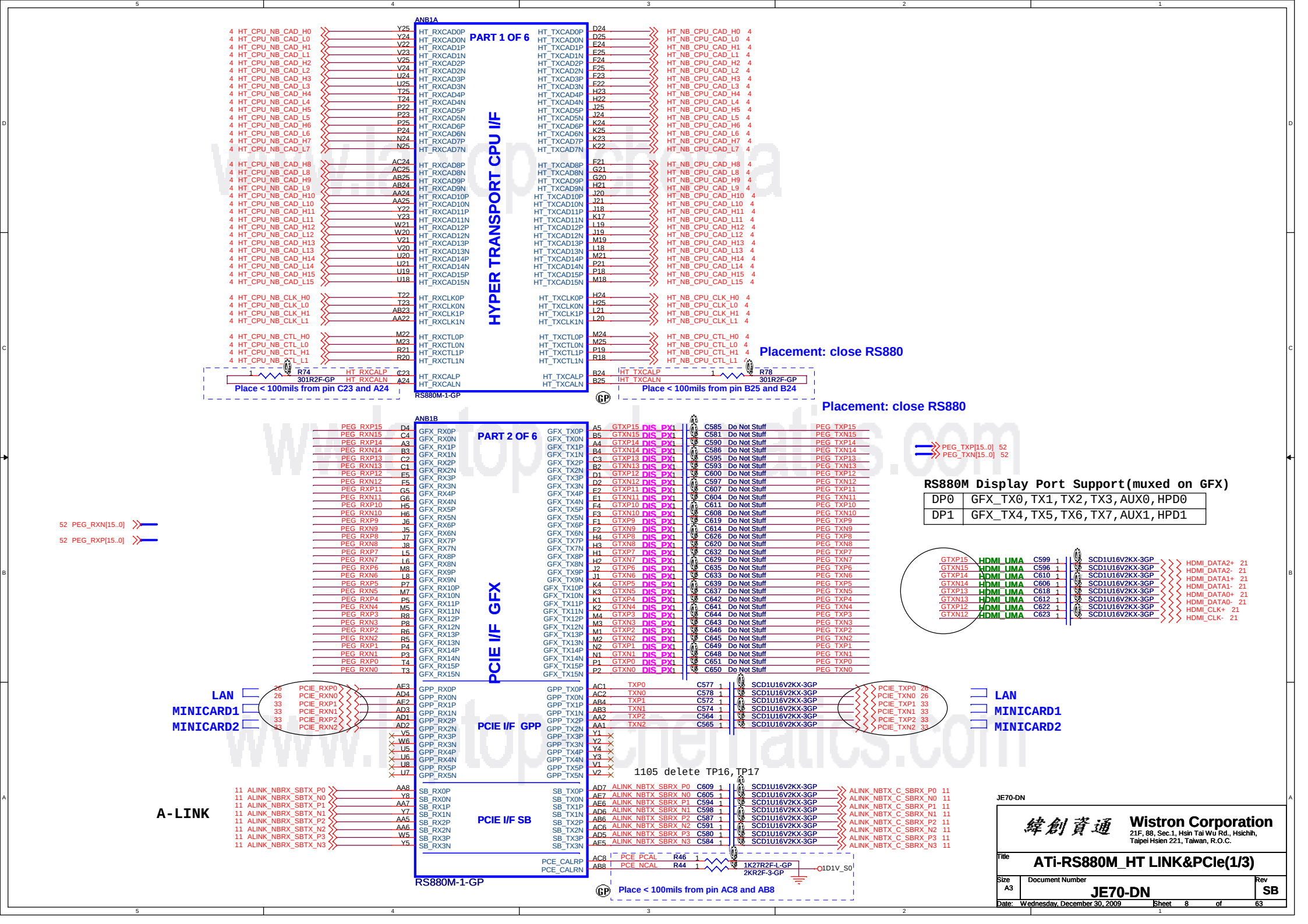
Title: CPU_Power_(4/4)

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Thursday, December 24, 2009 Sheet 7 of 63


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS880M-1-GP
Placement: close RS880
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS880M-1-GP
RS880M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
LAN
MINICARD1
MINICARD2
A-LINK
1105 delete TP16,TP17
Place < 100mils from pin AC8 and AB8
JE70-DN
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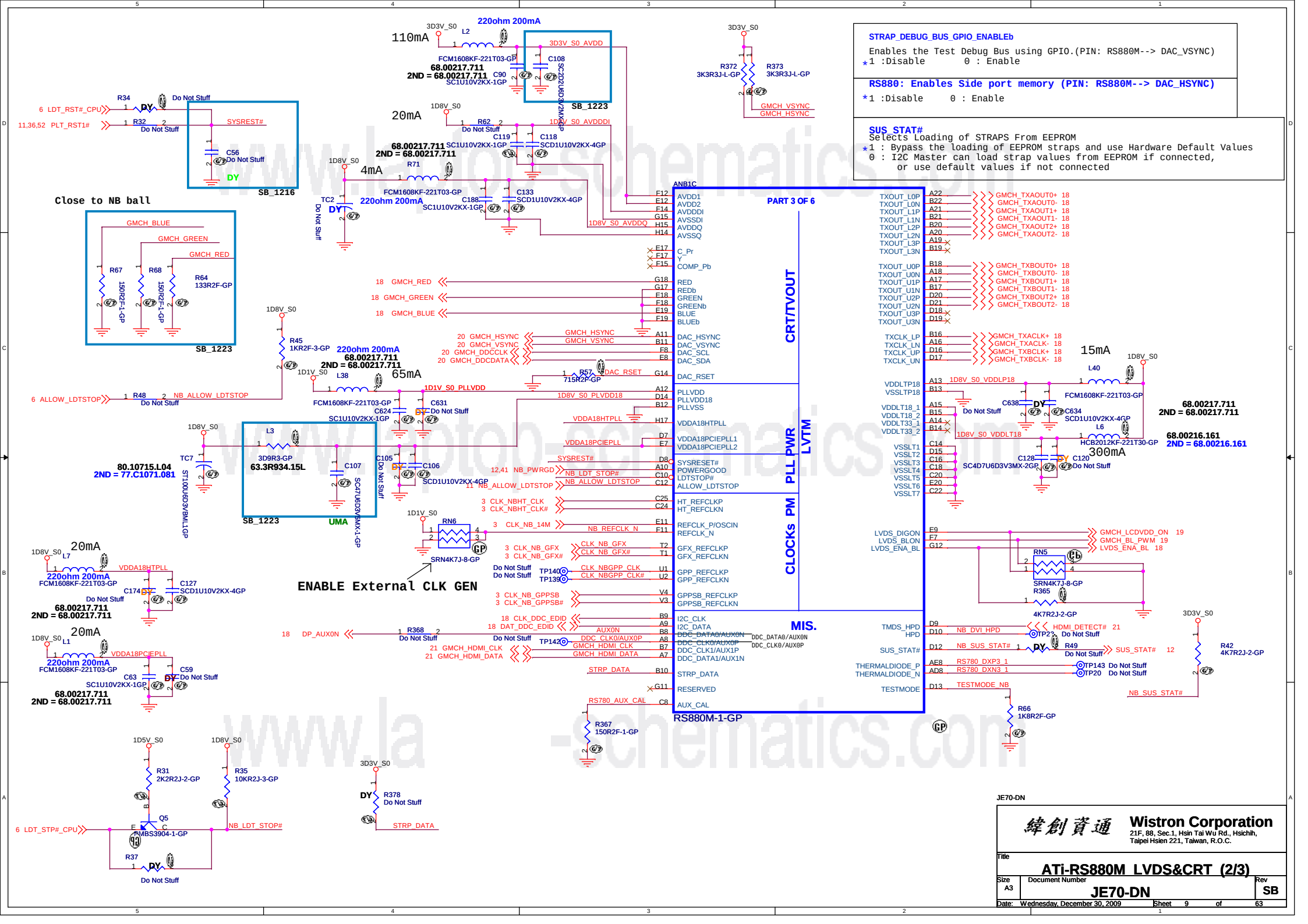
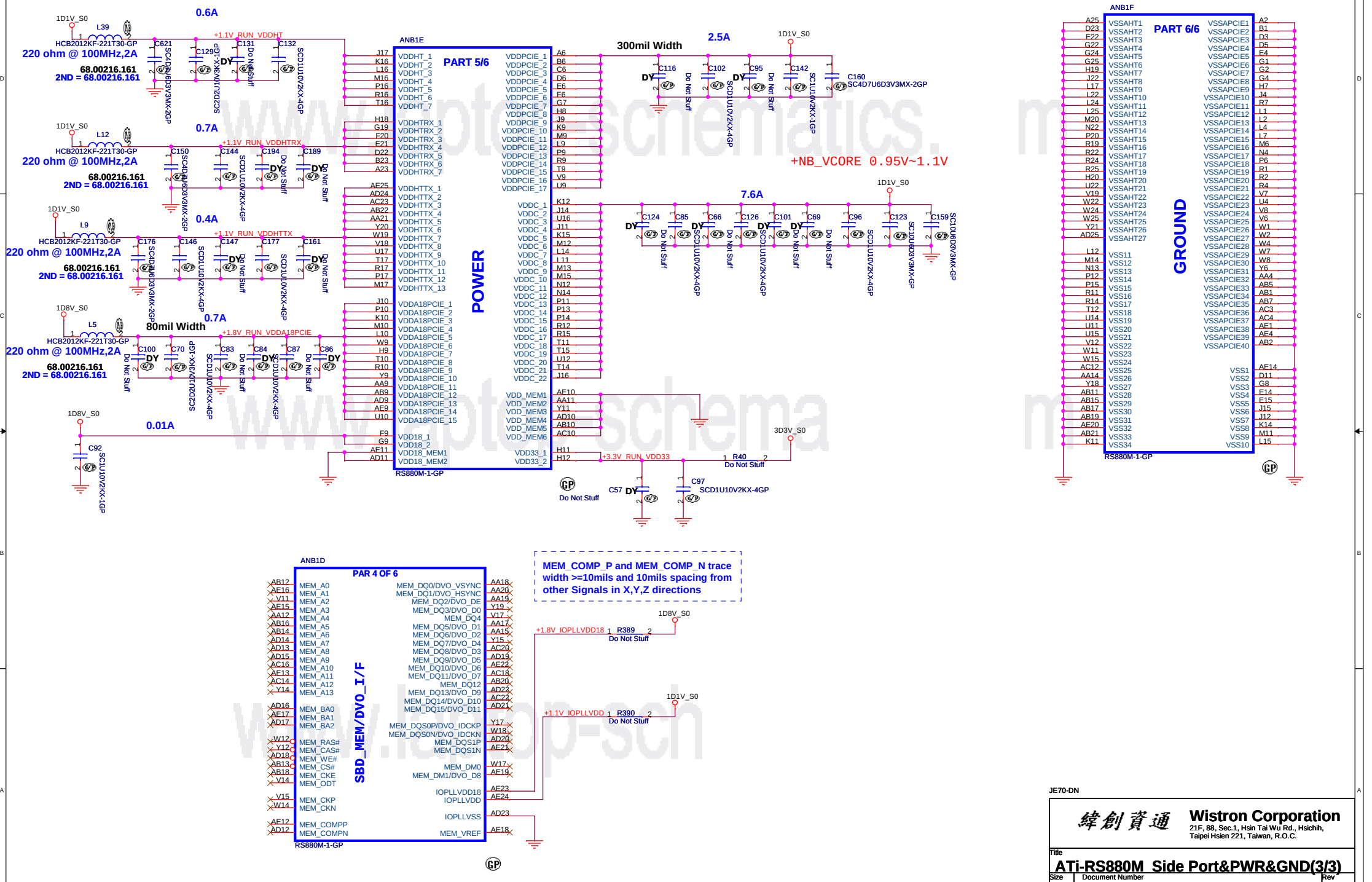
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_HT LINK&PCIe(1/3)
Size A3
Document Number JE70-DN
Rev SB
Date: Wednesday, December 30, 2009
Sheet 8 of 63


STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS880M--> DAC_VSYNC)
*1 :Disable 0 : Enable
RS880: Enables Side port memory (PIN: RS880M--> DAC_HSYNC)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
Close to NB ball
ENABLE External CLK GEN
RS880M-1-GP
PART 3 OF 6
CRT/TVOUT
PLL PWR
LVTM
CLOCKs PM
MIS.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
JE70-DN
ATi-RS880M LVDS&CRT (2/3)
Size A3
Document Number JE70-DN
Rev SB
Date: Wednesday, December 30, 2009
Sheet 9 of 63



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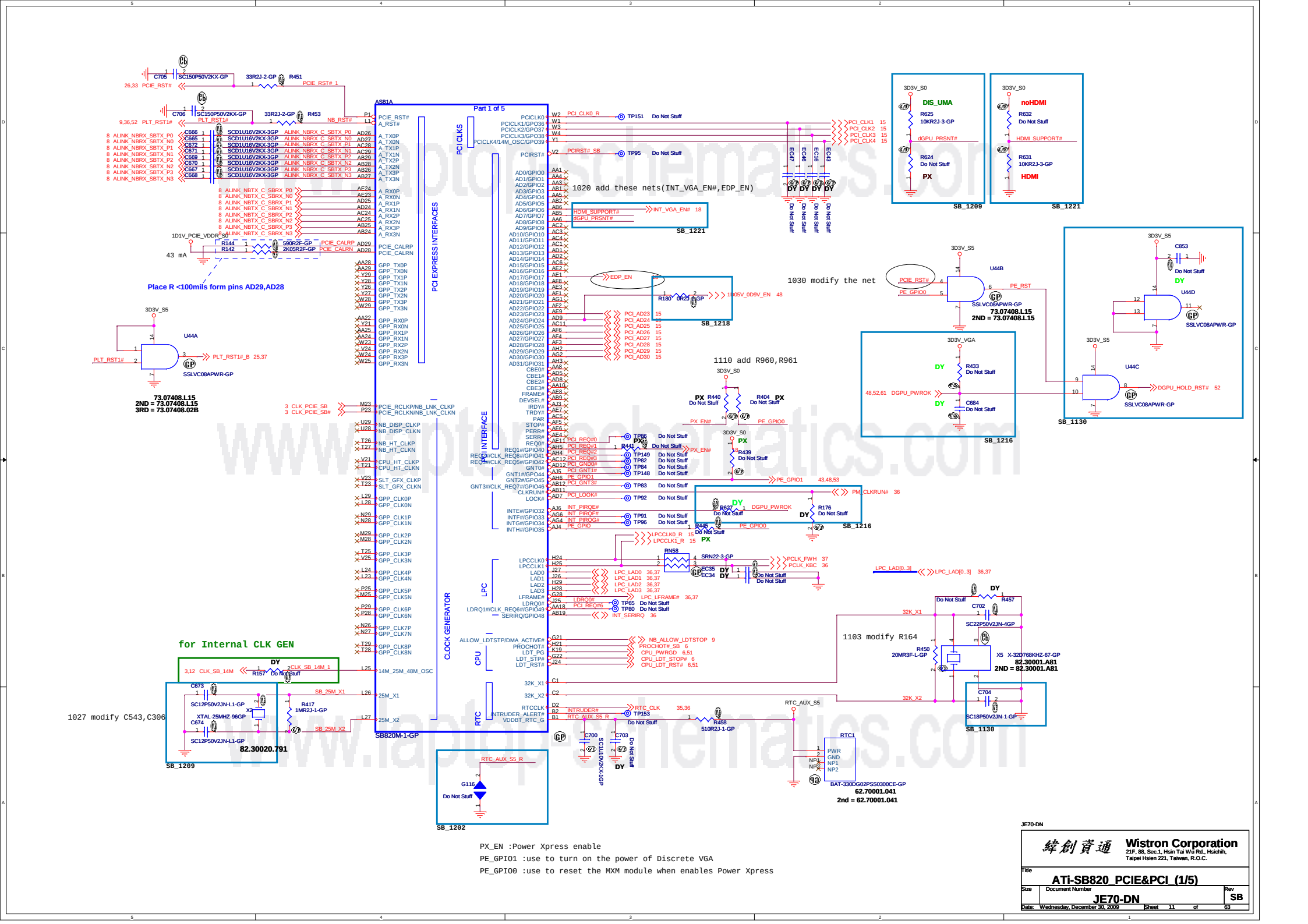
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS880M_Side Port&PWR&GND(3/3)

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Thursday, December 24, 2009 Sheet 10 of 63


Part 1 of 5
ASB1A
SB820M-1-GP
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
1020 add these nets(INT_VGA_EN#,EDP_EN)
1030 modify the net
1110 add R960,R961
1103 modify R164
1027 modify C543,C306
for Internal CLK GEN
Place R <100mils form pins AD29,AD28
73.07408.L15
2ND = 73.07408.L15
3RD = 73.07408.02B
82.30020.791
82.30001.A81
2ND = 82.30001.A81
62.70001.041
2nd = 62.70001.041
PX_EN :Power Xpress enable
PE_GPIO1 :use to turn on the power of Discrete VGA
PE_GPIO0 :use to reset the MXM module when enables Power Xpress
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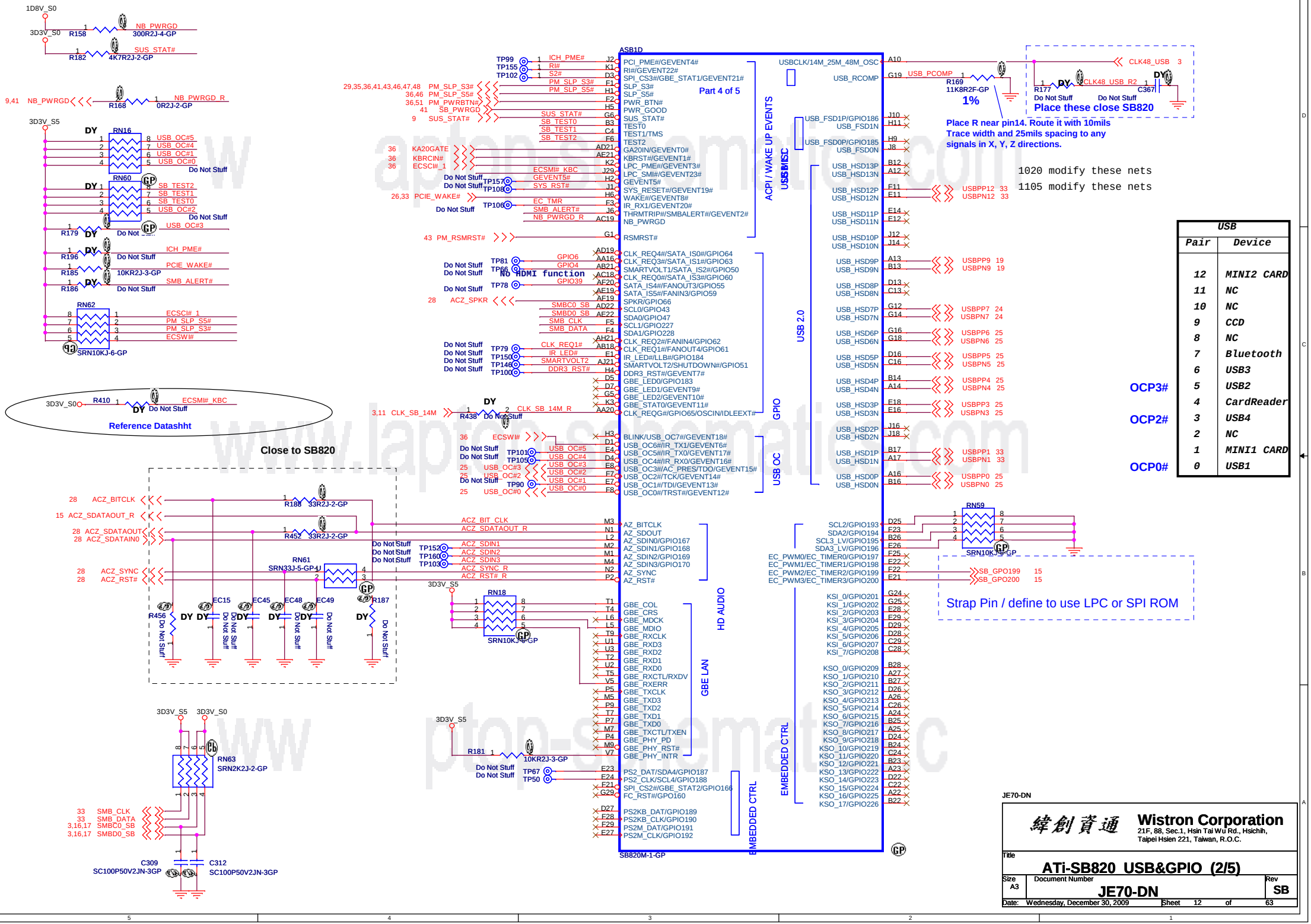
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB820_PCIE&PCI_(1/5)
JE70-DN
Wednesday, December 30, 2009
Sheet 11 of 63


ASB1D
Part 4 of 5
SB820M-1-GP
ACPI / WAKE UP EVENTS
USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
Close to SB820
No HDMI function
Reference Datashht
Place these close SB820
Place R near pin14. Route it with 10mils
Trace width and 25mils spacing to any
signals in X, Y, Z directions.
1020 modify these nets
1105 modify these nets
OCP3#
OCP2#
OCP0#
Strap Pin / define to use LPC or SPI ROM
USB
Pair Device
12 MINI2 CARD
11 NC
10 NC
9 CCD
8 NC
7 Bluetooth
6 USB3
5 USB2
4 CardReader
3 USB4
2 NC
1 MINI1 CARD
0 USB1
JE70-DN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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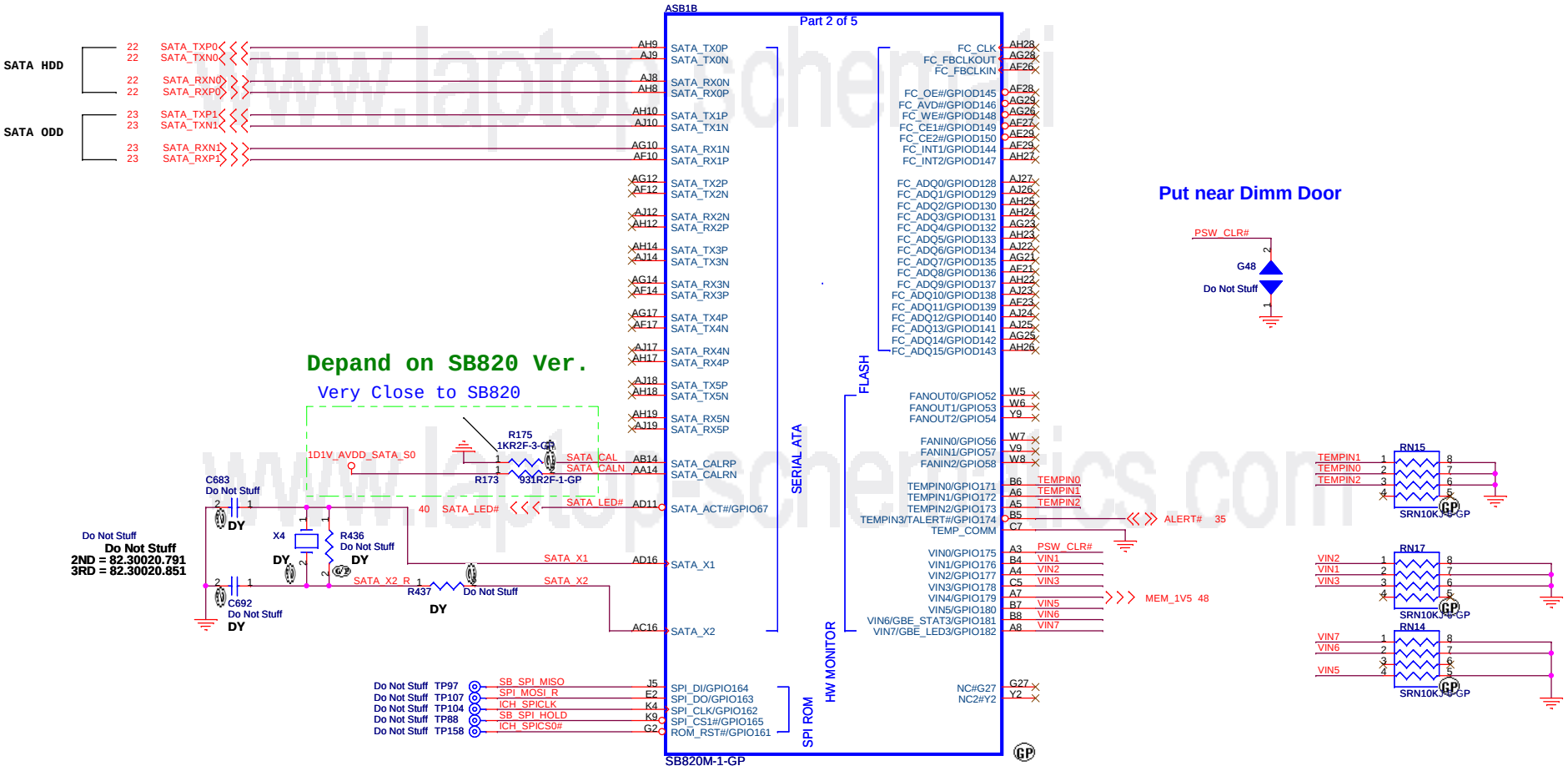
Title
ATi-SB820 USB&GPIO (2/5)
Size A3
Document Number JE70-DN
Rev SB
Date: Wednesday, December 30, 2009
Sheet 12 of 63



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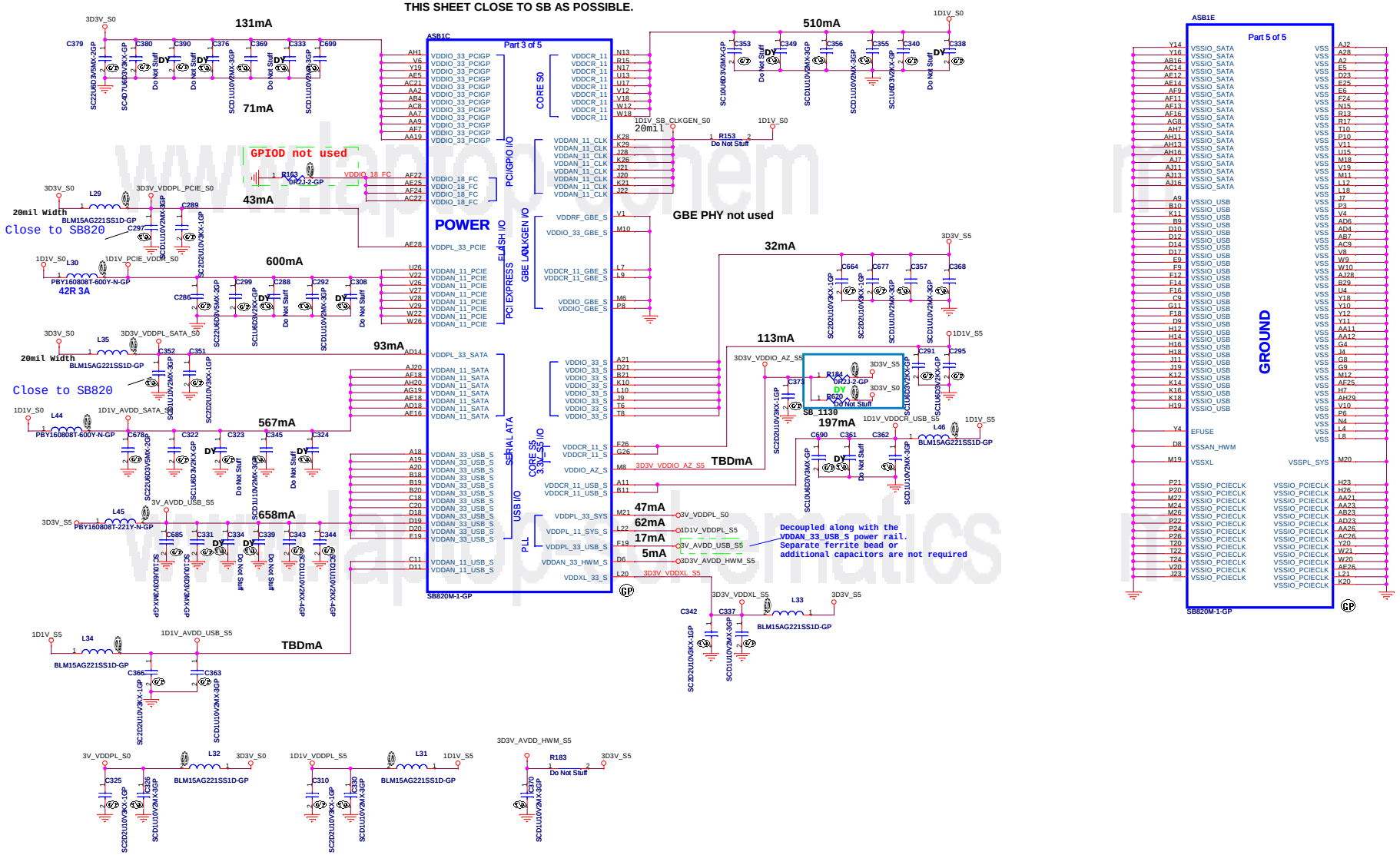
Title: ATi-SB820 SATA-IDE (3/5)

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Wednesday, December 30, 2009 Sheet 13 of 63

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.



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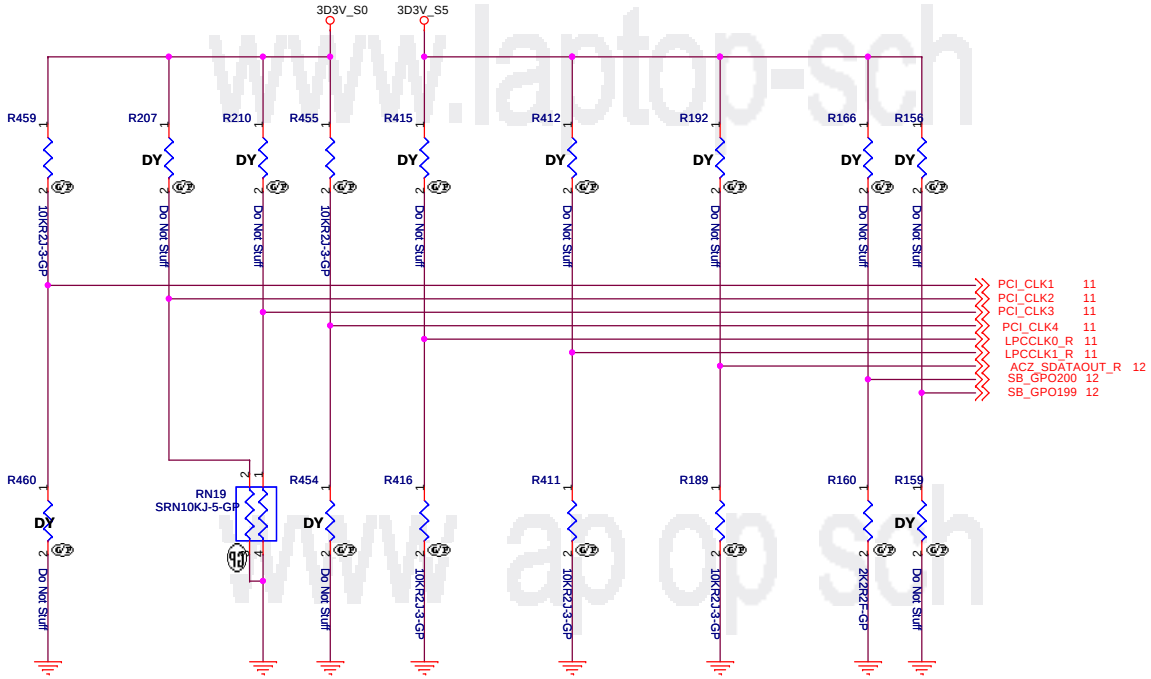
Title: ATi-SB820 POWER&GND (4/5)

Size	Document Number	Rev
Custom	JE70-DN	SB

Date: Friday, December 25, 2009 Sheet 14 of 63

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS

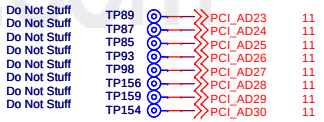


1118 modify R412,R411

	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200 GPIO199
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED	LOW POWER MODE	H,H = Reserved H,L = SPI ROM
PULL LOW	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	PERFORMANCE MODE DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

NOTE: SB820 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Note: SB820 has 15K internal PU FOR PCI_AD[27:23]

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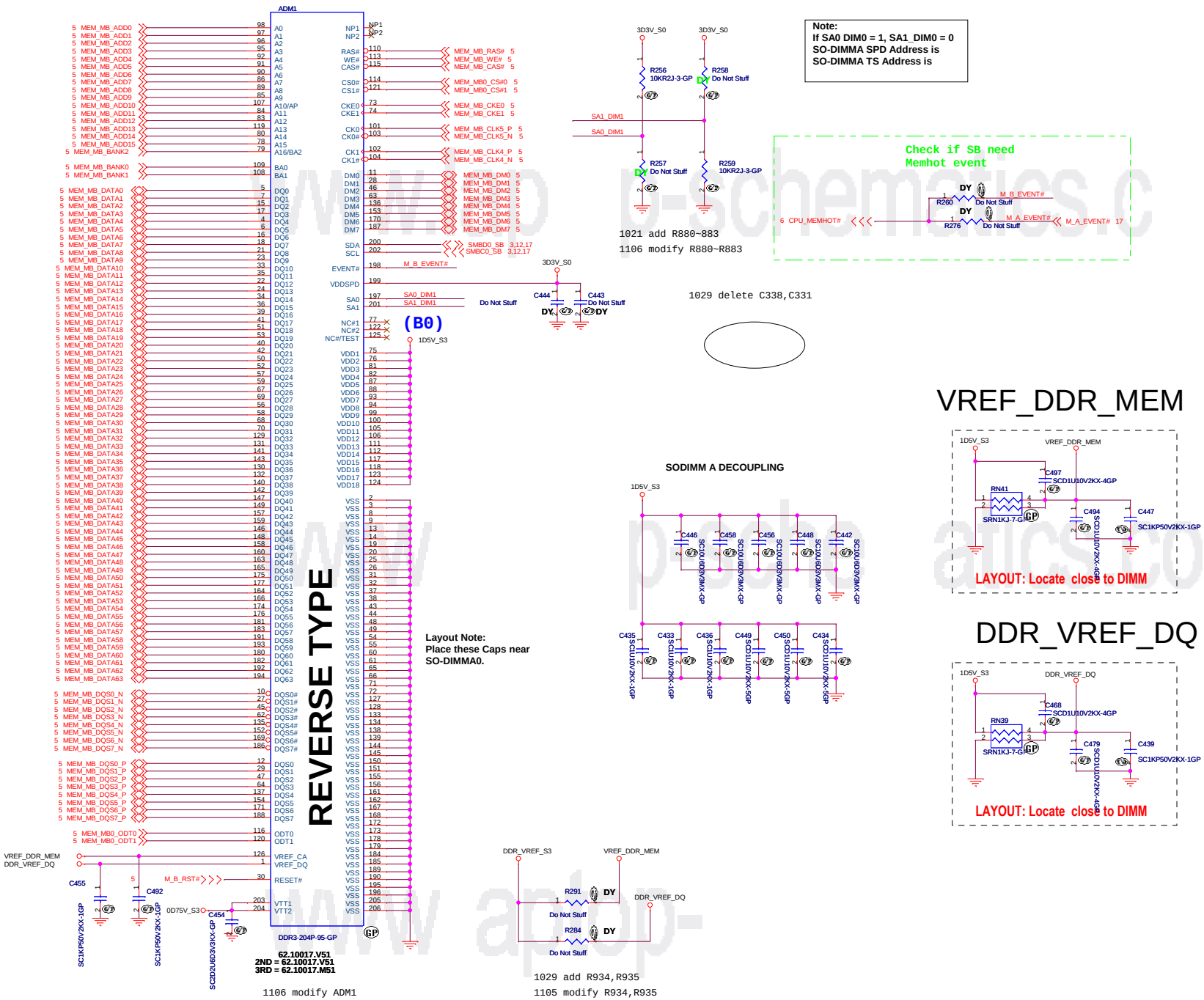
Title: ATi-SB820 STRAPPING (5/5)

Size	Document Number	Rev
A3	JE70-DN	SB

Date: Wednesday, December 30, 2009 Sheet 15 of 63



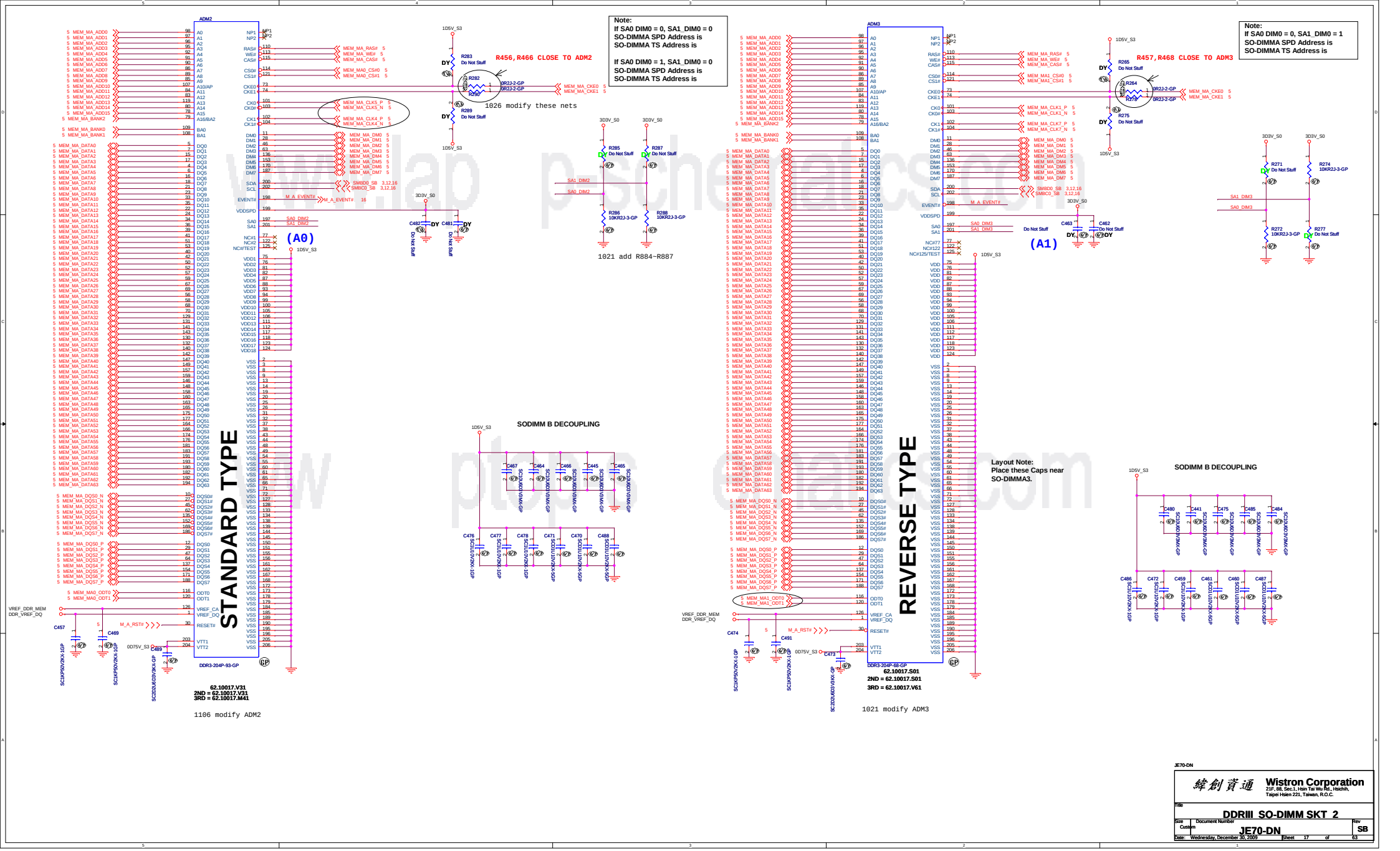
JE70-DN

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	JE70-DN	SB

Date: Wednesday, December 30, 2009 Sheet 16 of 63



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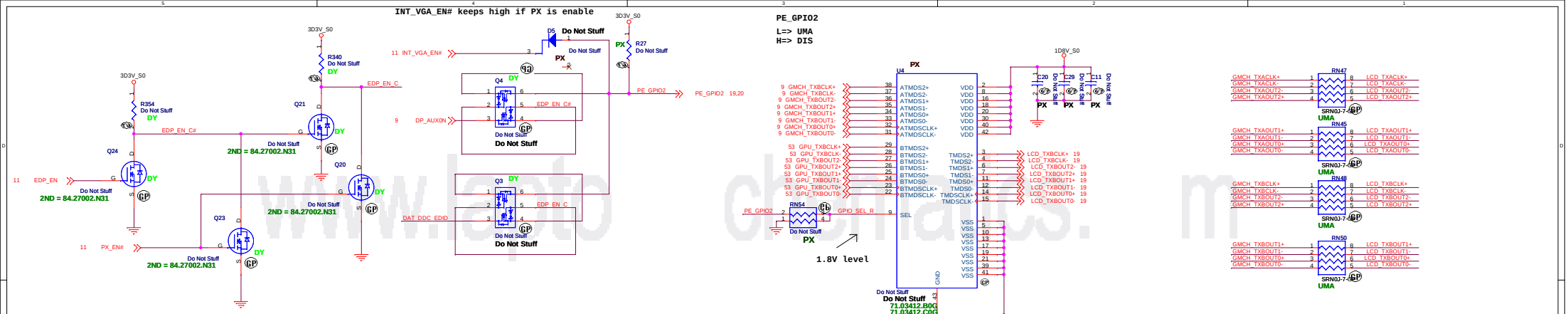
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDRIII SO-DIMM SKT 2
Size: Custom	Document Number: JE70-DN
Rev	SB
Date: Wednesday, December 30, 2009	Sheet 17 of 63



DISPLAY SUPPORT TABLE

	PX_EN#	DP_AUX0N EDP diabled	I2C_DATA EDP diabled	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	1	X	X	0	IGP(LVDS,EDP,VGA,DP)
MXM only mode	1	X	X	1	MXM(LVDS,EDP,VGA,DP)
Power Express(muxed)	0	0/1	0/1	1	MXM/IGP(LVDS,EDP,VGA);MXM(DP)
Power Express(muxless)	0	X	X	0	IGP(LVDS,EDP,VGA,DP)

PX mode display device auto detection method:
VGA:I2C interface to NB
DP:HPD

LVDS

Function	SEL
An to nB1	L
An to nB2	H

CRT

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

EDID

Function Table

Input (S)	Function
L	B_0 Connected to A
H	B_1 Connected to A

H = HIGH Logic Level L = LOW Logic Level

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Title: PX			
Size: A2	Document Number: JE70-DN		Rev: SB
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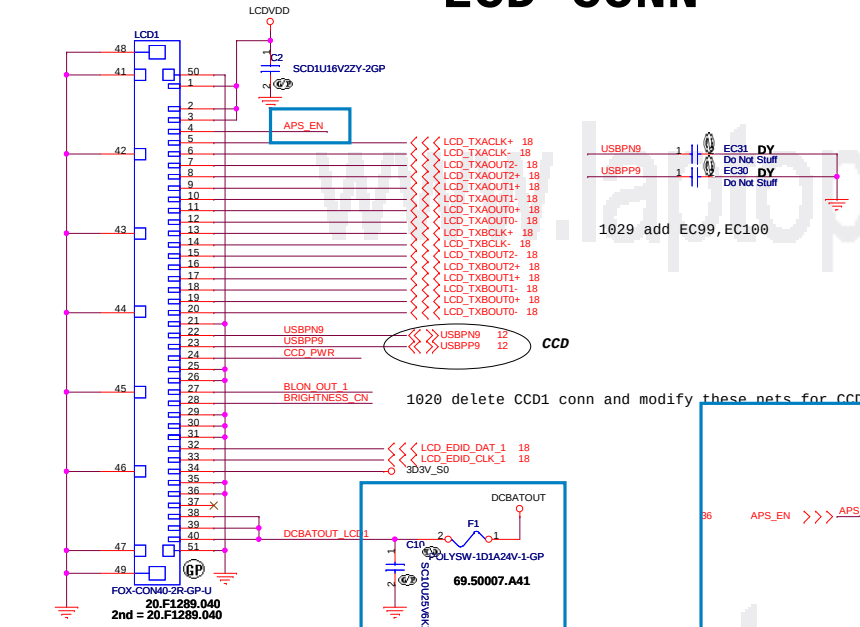
LCD CONN

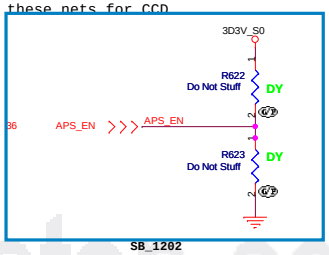
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

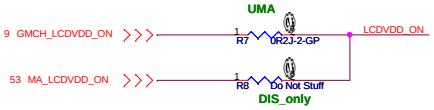
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

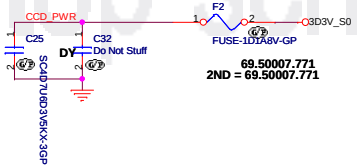


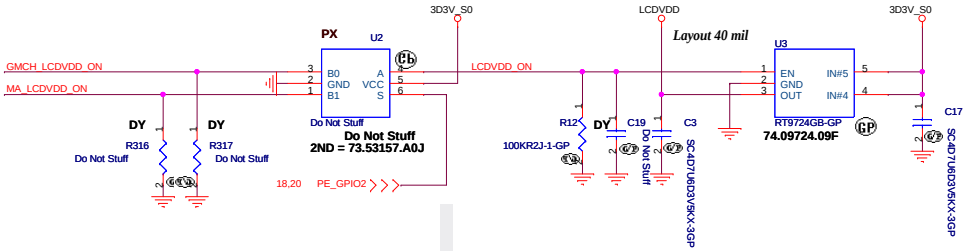
1029 add EC99,EC100

1020 delete CCD1 conn and modify these nets for CCD



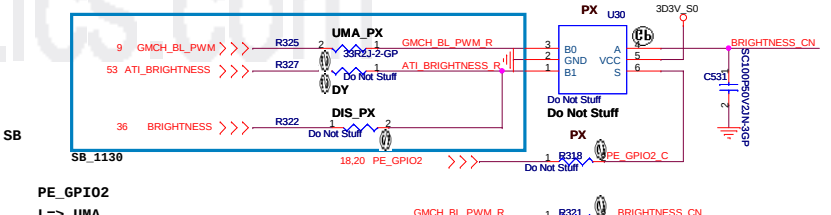




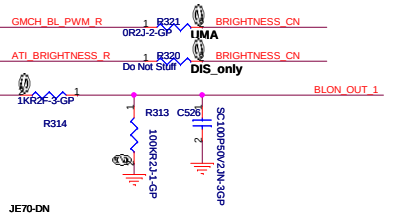


PE_GPIO2
L=> UMA
H=> DIS

Reserve direct connector to KBC



PE_GPIO2
L=> UMA
H=> DIS



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Title: LCD CONN

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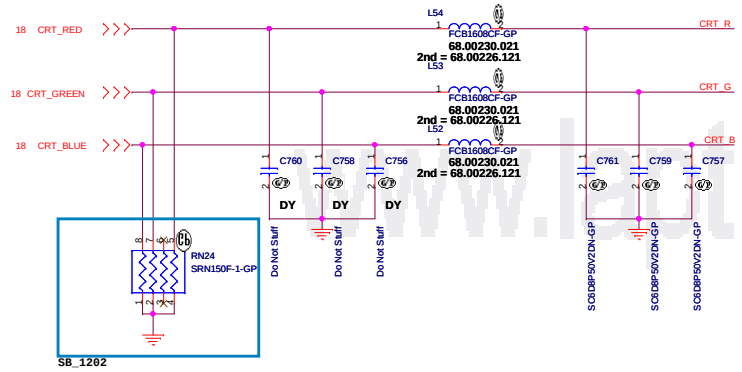
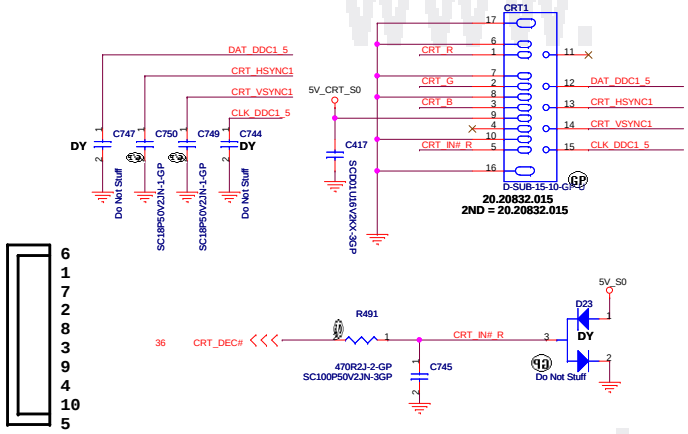
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz



Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

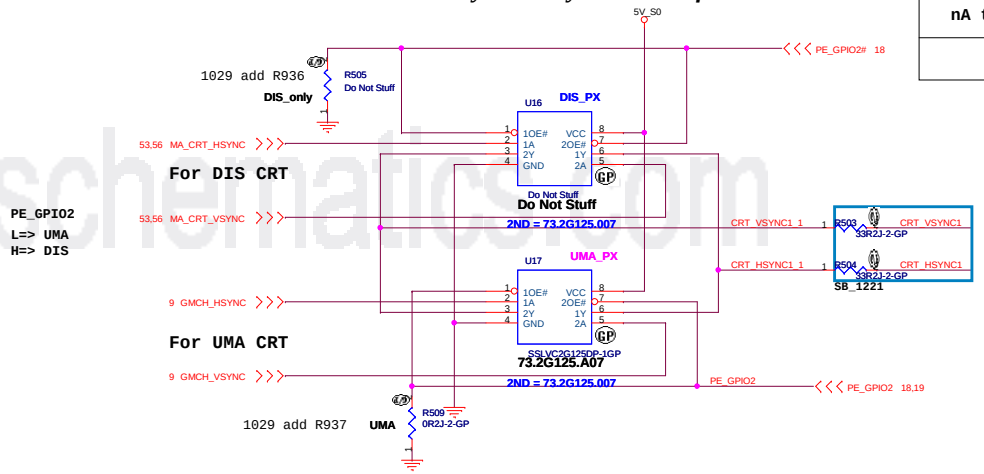
CRT I/F & CONNECTOR



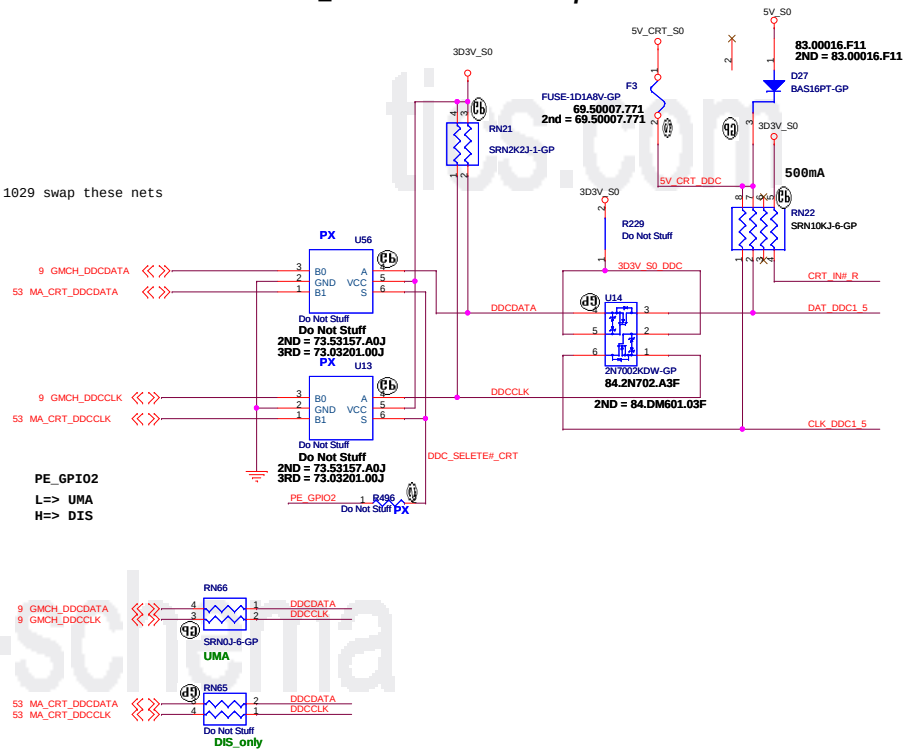
6 1 7 2 8 3 9 4 10 5

Hsync & Vsync level shift

Function	OE#
nA to nY	L
X	H



DDC_CLK & DATA level shift



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Title	CRT Connector
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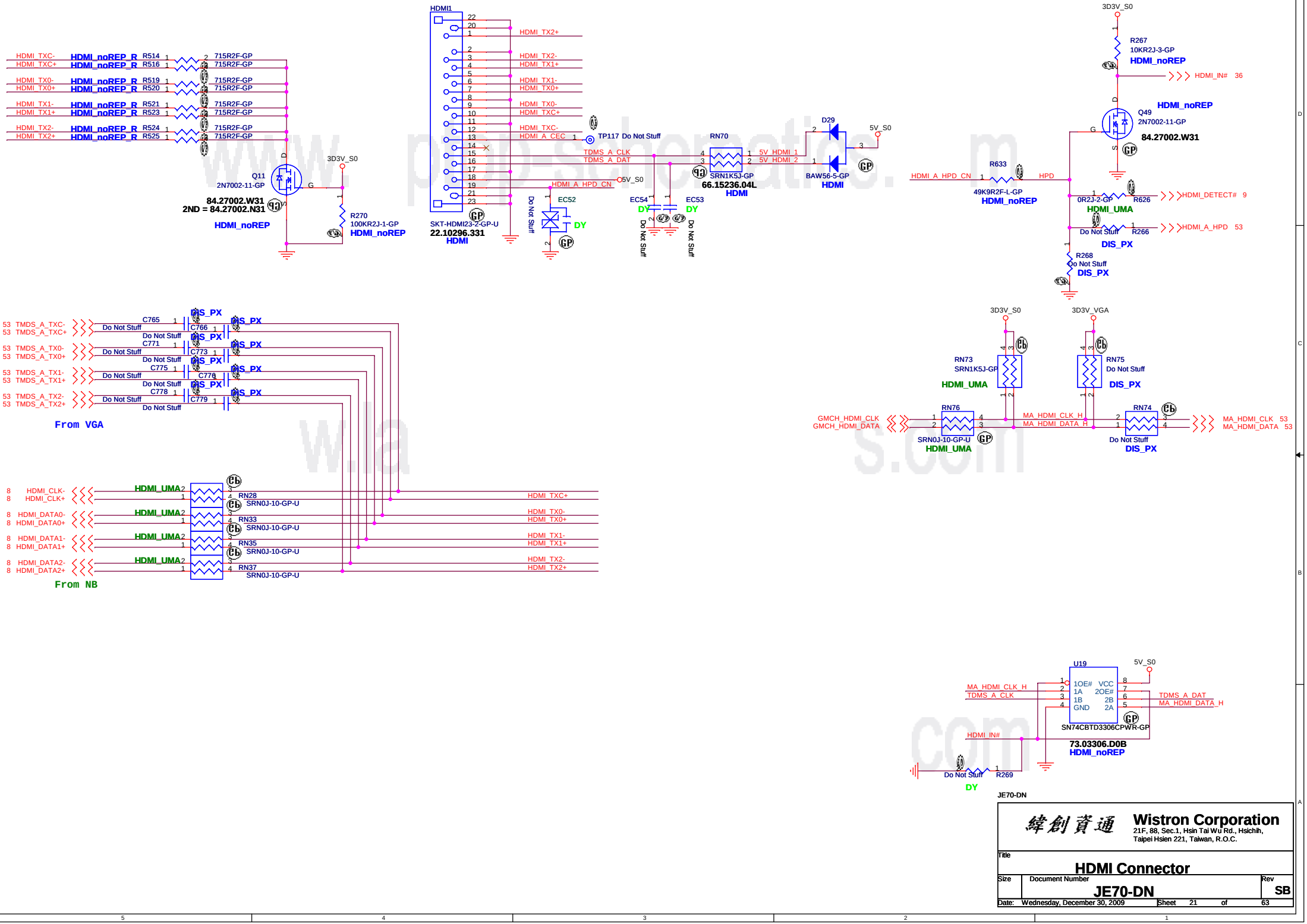
HDMI_TXC- HDMI_noREP_R R514 715R2F-GP
HDMI_TXC+ HDMI_noREP_R R516 715R2F-GP
HDMI_TX0- HDMI_noREP_R R519 715R2F-GP
HDMI_TX0+ HDMI_noREP_R R520 715R2F-GP
HDMI_TX1- HDMI_noREP_R R521 715R2F-GP
HDMI_TX1+ HDMI_noREP_R R523 715R2F-GP
HDMI_TX2- HDMI_noREP_R R524 715R2F-GP
HDMI_TX2+ HDMI_noREP_R R525 715R2F-GP
Q11
2N7002-11-GP
84.27002.W31
2ND = 84.27002.N31
HDMI_noREP
3D3V_S0
R270
100KR2J-1-GP
HDMI_noREP
HDMI1
SKT-HDMI23-2-GP-U
22.10296.331
HDMI
HDMI_TX2+
HDMI_TX2-
HDMI_TX1+
HDMI_TX1-
HDMI_TX0+
HDMI_TX0-
HDMI_TXC+
HDMI_TXC-
HDMI_A_CEC
TP117 Do Not Stuff
TDMS_A_CLK
TDMS_A_DAT
HDMI_A_HPD_CN
5V_S0
EC52
DY
Do Not Stuff
EC54
EC53
RN70
SRN1K5J-GP
66.15236.04L
HDMI
5V_HDMI_1
5V_HDMI_2
D29
BAW56-5-GP
HDMI
5V_S0
3D3V_S0
R267
10KR2J-3-GP
HDMI_noREP
HDMI_IN# 36
Q49
2N7002-11-GP
84.27002.W31
HDMI_noREP
HDMI_A_HPD_CN
R633
49K9R2F-L-GP
HDMI_noREP
HPD
R626
0R2J-2-GP
HDMI_UMA
HDMI_DETECT# 9
R266
Do Not Stuff
DIS_PX
HDMI_A_HPD 53
R268
Do Not Stuff
DIS_PX
From VGA
53 TMDS_A_TXC-
53 TMDS_A_TXC+
53 TMDS_A_TX0-
53 TMDS_A_TX0+
53 TMDS_A_TX1-
53 TMDS_A_TX1+
53 TMDS_A_TX2-
53 TMDS_A_TX2+
C765
C766
C771
C773
C775
C776
C778
C779
Do Not Stuff
DIS_PX
From NB
8 HDMI_CLK-
8 HDMI_CLK+
8 HDMI_DATA0-
8 HDMI_DATA0+
8 HDMI_DATA1-
8 HDMI_DATA1+
8 HDMI_DATA2-
8 HDMI_DATA2+
HDMI_UMA
RN28
RN33
RN35
RN37
SRN0J-10-GP-U
HDMI_TXC+
HDMI_TX0-
HDMI_TX0+
HDMI_TX1-
HDMI_TX1+
HDMI_TX2-
HDMI_TX2+
3D3V_S0
3D3V_VGA
RN73
SRN1K5J-GP
HDMI_UMA
RN75
Do Not Stuff
DIS_PX
RN76
SRN0J-10-GP-U
HDMI_UMA
RN74
Do Not Stuff
DIS_PX
GMCH_HDMI_CLK
GMCH_HDMI_DATA
MA_HDMI_CLK_H
MA_HDMI_DATA_H
MA_HDMI_CLK 53
MA_HDMI_DATA 53
U19
SN74CBTD3306CPWR-GP
73.03306.D0B
HDMI_noREP
5V_S0
MA_HDMI_CLK_H
TDMS_A_CLK
TDMS_A_DAT
MA_HDMI_DATA_H
HDMI_IN#
Do Not Stuff
R269
DY
JE70-DN
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Connector
Size
Document Number
JE70-DN
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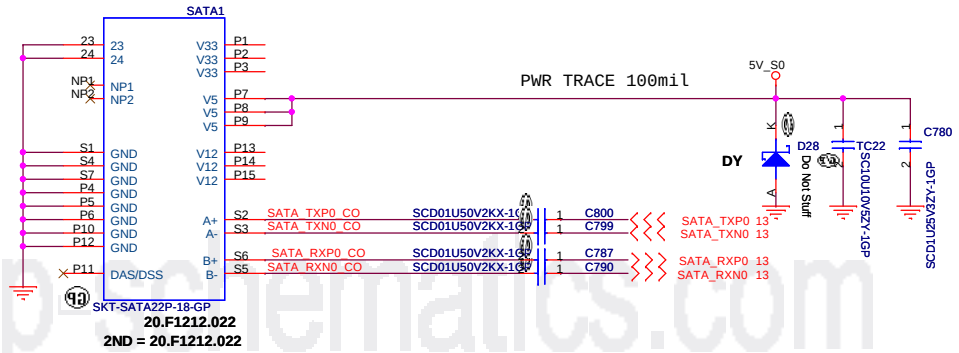
SATA Connector



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Title		
HDD		
Size	Document Number	Rev
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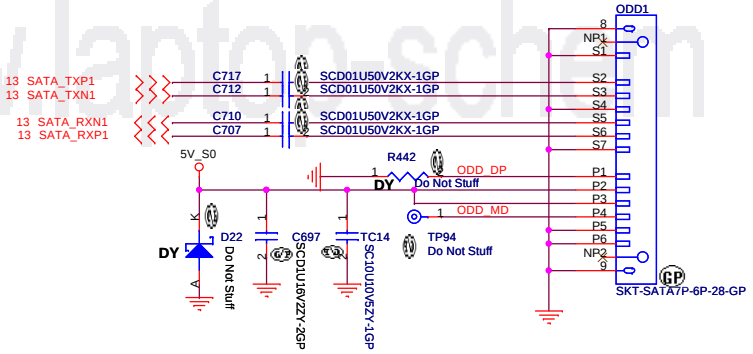
ODD Connector



62.10065.D71
2ND = 62.10065.D71

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Title: ODD

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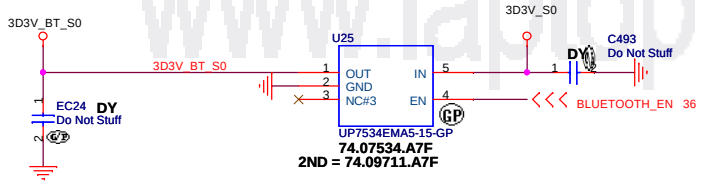
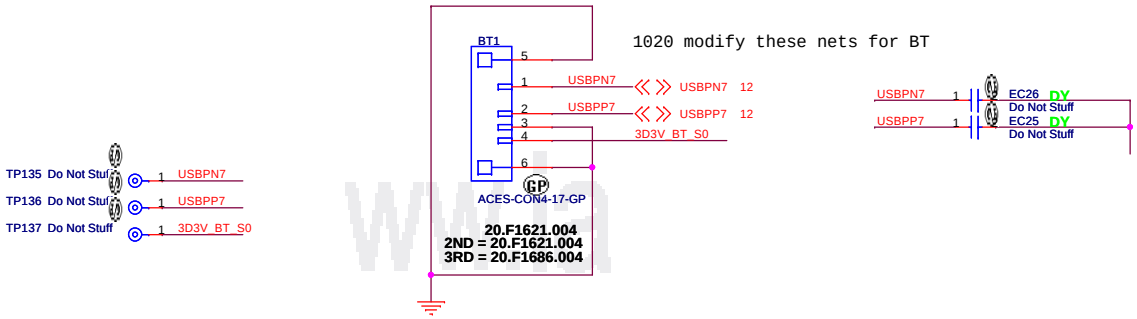
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



1020 modify these nets for BT



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Title: **BLUETOOTH**		
Size	Document Number: **JE70-DN**	Rev: **SB**
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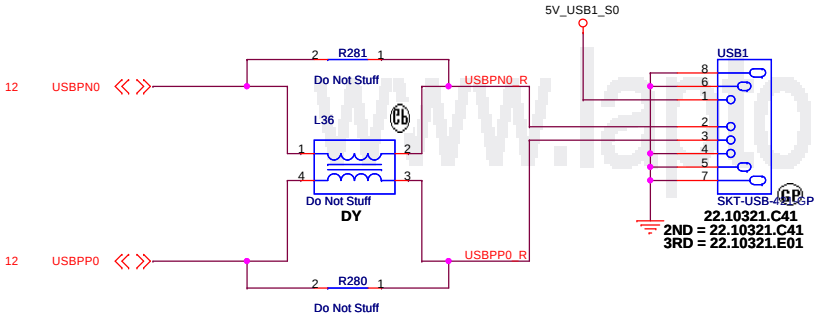

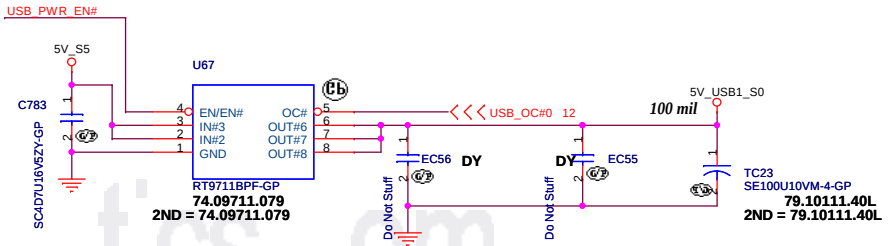

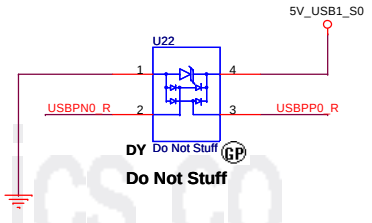

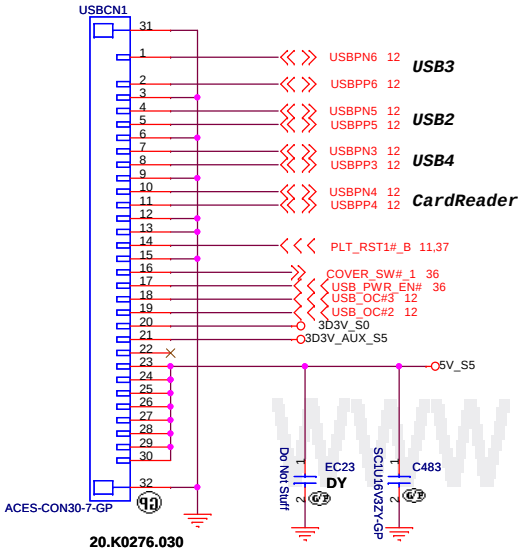

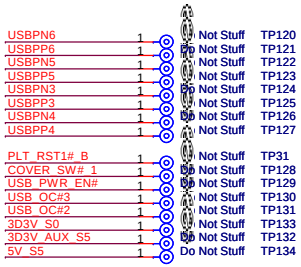

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Title: **USB**		
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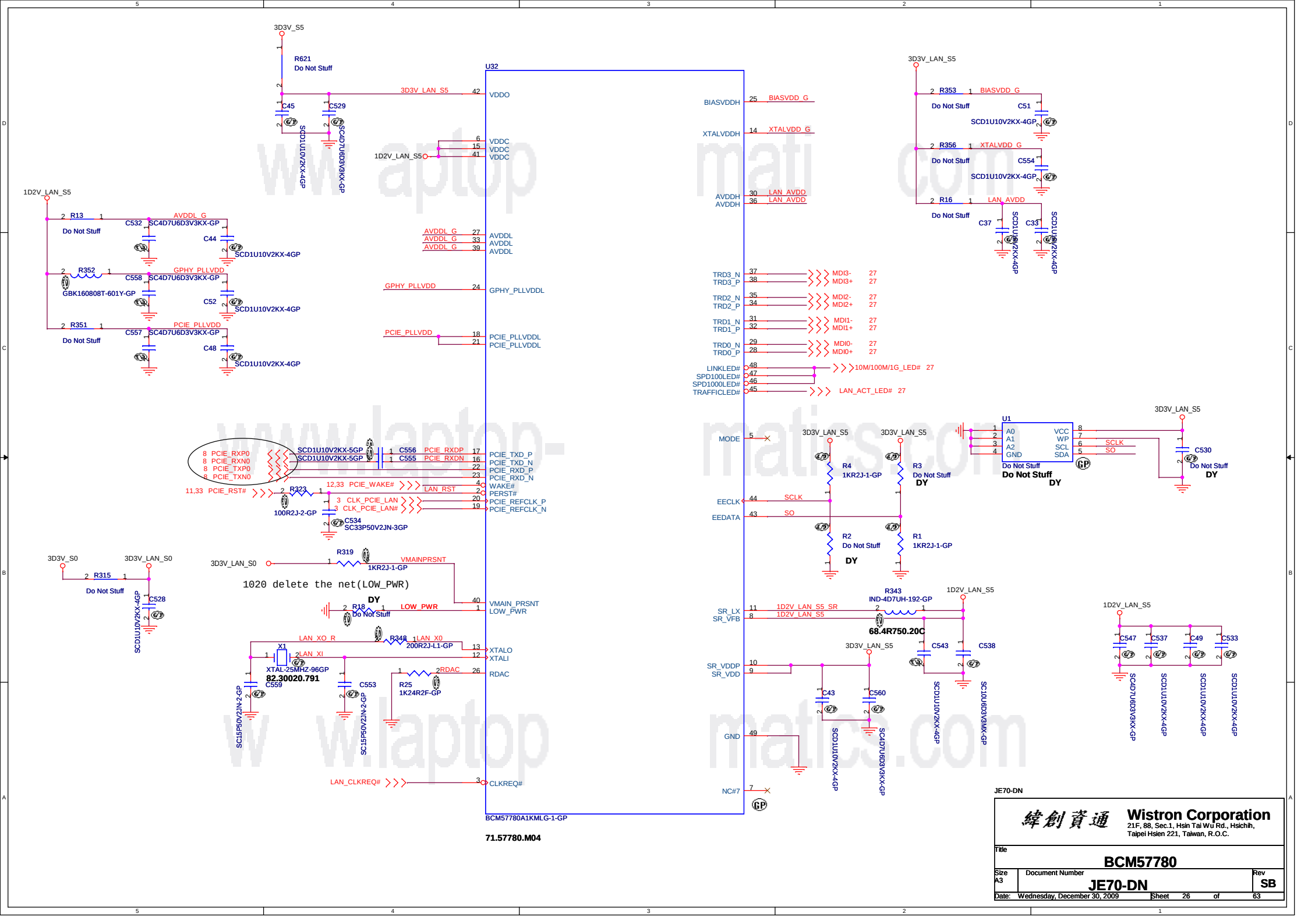
U32
BCM57780A1KMLG-1-GP
71.57780.M04
1020 delete the net(LOW_PWR)
1D2V_LAN_S5
3D3V_S5
3D3V_LAN_S5
3D3V_S0
3D3V_LAN_S0
1D2V_LAN_S5_SR
R621
Do Not Stuff
R13
R352
R351
R315
R319
R18
R323
R348
R343
IND-4D7UH-192-GP
68.4R750.20C
R353
R356
R16
R4
1KR2J-1-GP
R3
R2
R1
R25
1K24R2F-GP
200R2J-L1-GP
100R2J-2-GP
1KR2J-1-GP
C45
C529
C532
C44
C558
C52
C557
C48
C528
C556
C555
C534
SC33P50V2JN-3GP
C559
C553
C543
C538
C560
C43
C51
C554
C37
C33
C530
C547
C537
C49
C533
X1
XTAL-25MHZ-96GP
82.30020.791
U1
SC4D7U6D3V3KX-GP
SCD1U10V2KX-4GP
SC10U6D3V3MX-GP
SC15P50V2JN-2GP
GBK160808T-601Y-GP
DY
3D3V_LAN_S5
VDDO
VDDC
VDDC
VDDC
AVDDL
AVDDL
AVDDL
GPHY_PLLVDDL
PCIE_PLLVDDL
PCIE_PLLVDDL
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
WAKE#
PERST#
PCIE_REFCLK_P
PCIE_REFCLK_N
VMAIN_PRSNT
LOW_PWR
XTALO
XTALI
RDAC
CLKREQ#
BIASVDDH
XTALVDDH
LAN_AVDD
LAN_AVDD
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
10M/100M/1G_LED# 27
LAN_ACT_LED# 27
MODE
EECLK
EEDATA
SR_LX
SR_VFB
SR_VDDP
SR_VDD
GND
NC#7
SCLK
SO
LAN_CLKREQ#
LAN_XO_R
LAN_XI
LAN_RST
CLK_PCIE_LAN
CLK_PCIE_LAN#
PCIE_RXP0
PCIE_RXN0
PCIE_TXP0
PCIE_TXN0
PCIE_RST#
PCIE_WAKE#
VMAINPRSNT
LOW_PWR
BIASVDD_G
XTALVDD_G
AVDDL_G
GPHY_PLLVDD
PCIE_PLLVDD
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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BCM57780
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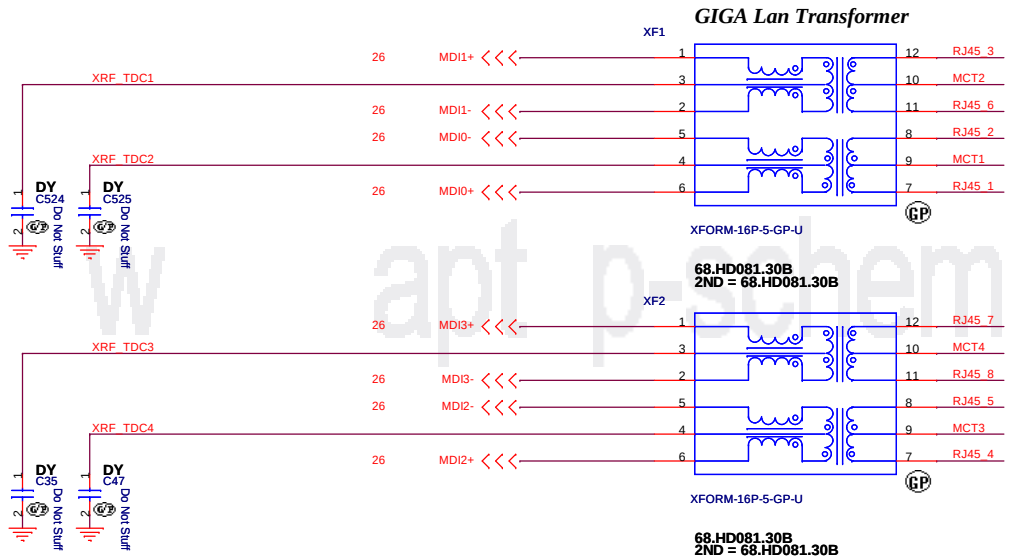
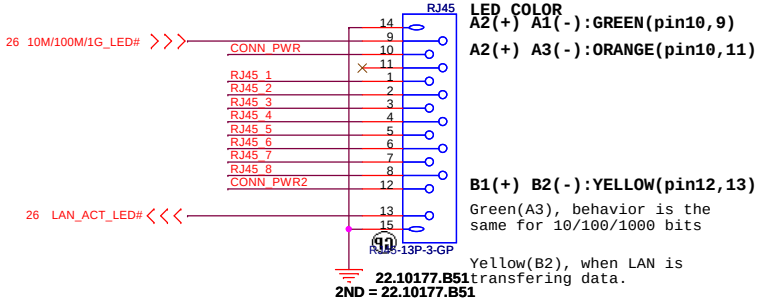
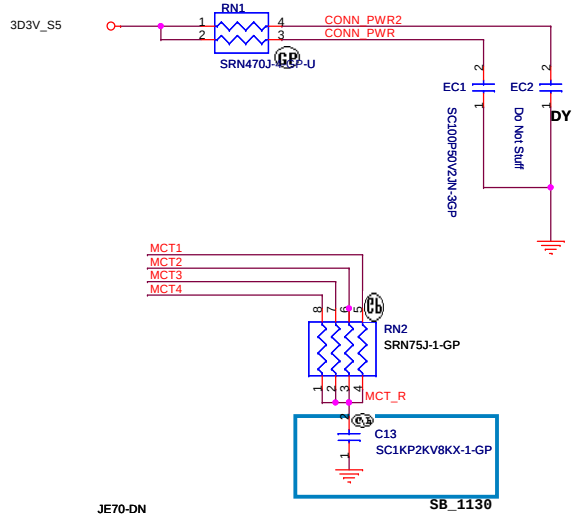
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

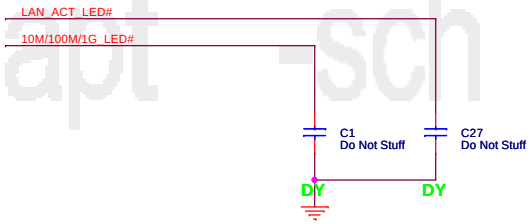
LAN Connector

LAN Connector









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Title		
LAN CONN		
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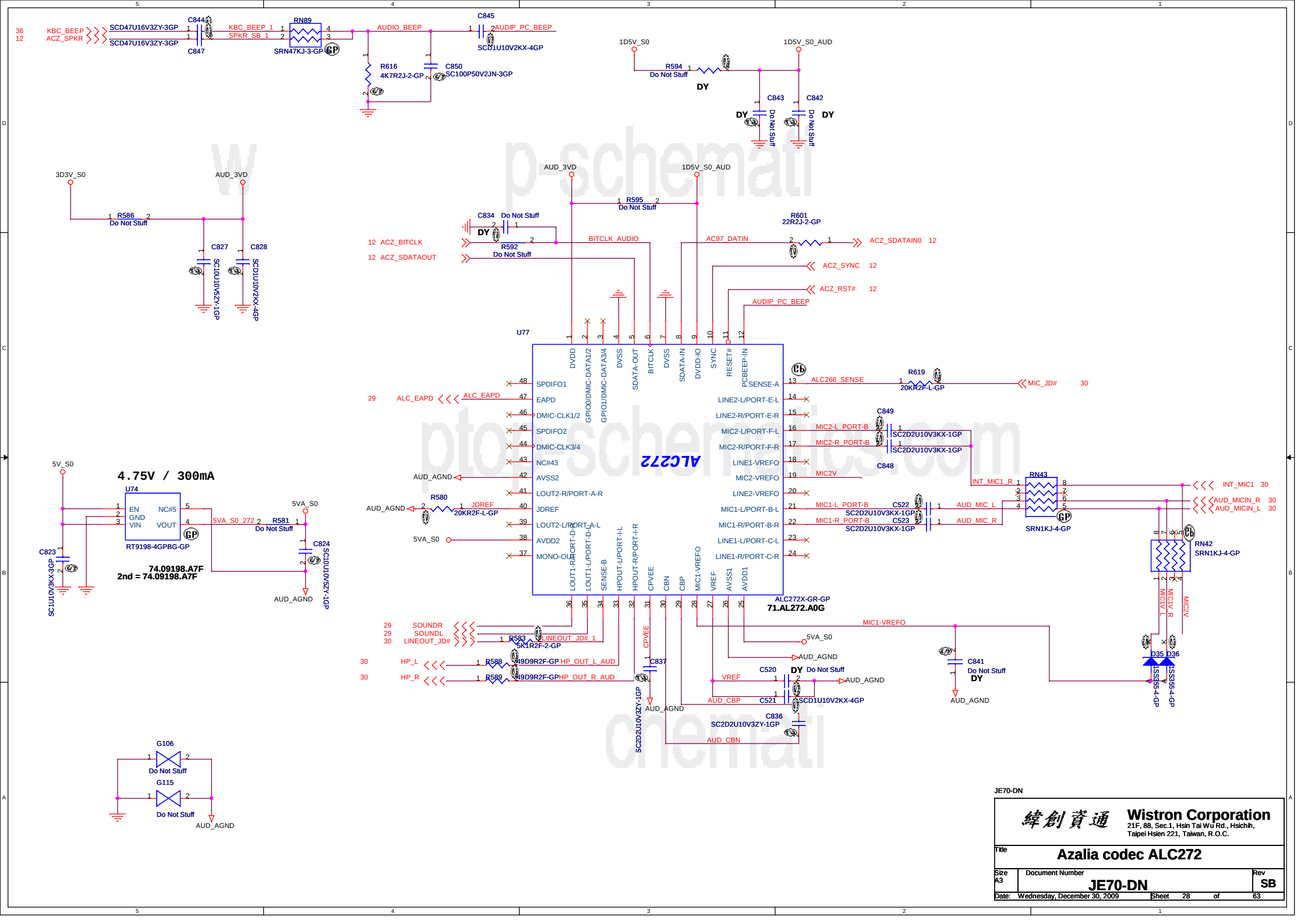
ALC272
ALC272X-GR-GP
71.AL272.A0G
U77
4.75V / 300mA
U74
RT9198-4GPBG-GP
74.09198.A7F
2nd = 74.09198.A7F
SRN47KJ-3-GP
SRN1KJ-4-GP
RN42
SRN1KJ-4-GP
RN43
SRN1KJ-4-GP
Do Not Stuff
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Azalia codec ALC272
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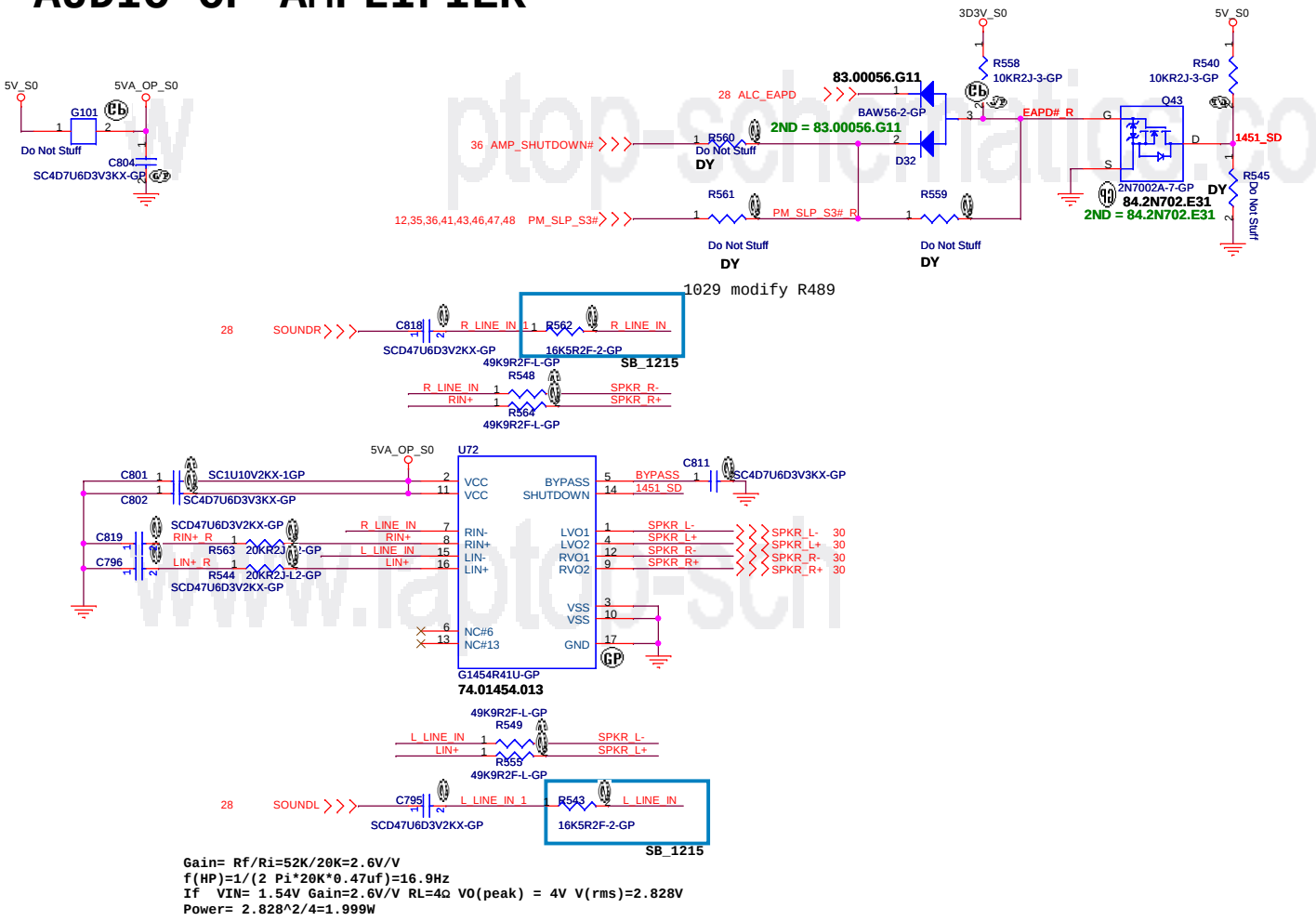
AUDIO OP AMPLIFIER



Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.828^2/4=1.999W

JE70-DN

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Title: AUDIO AMP

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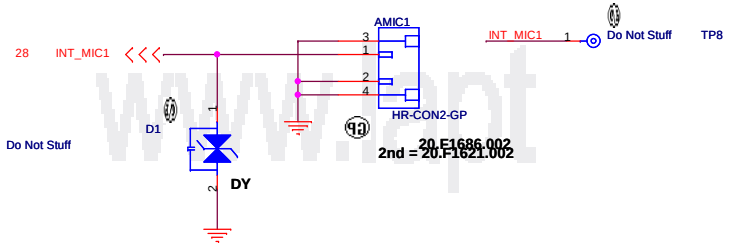
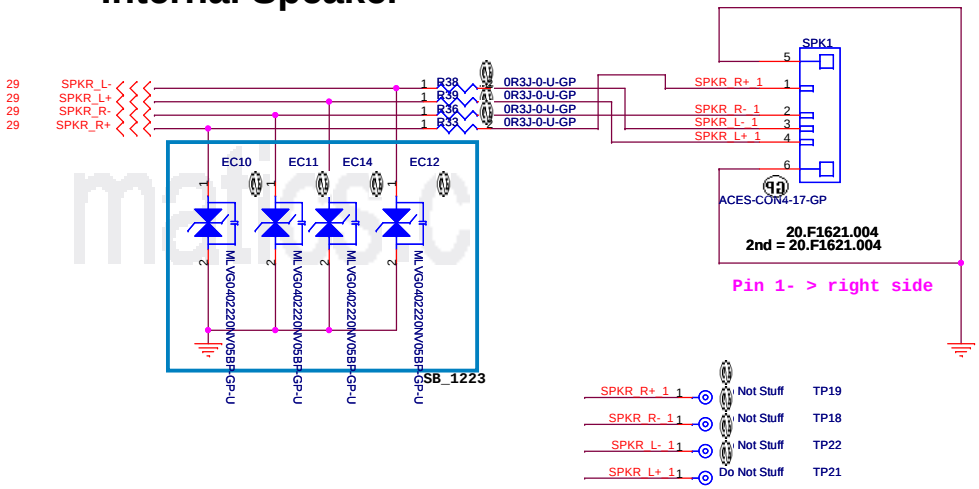
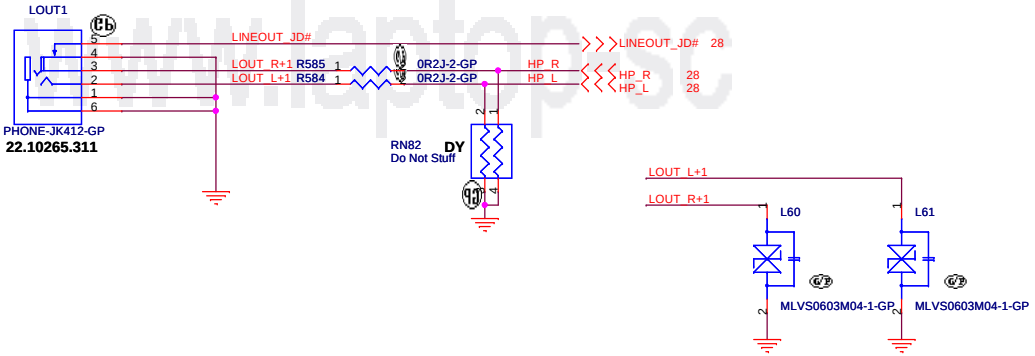
Internal Mic



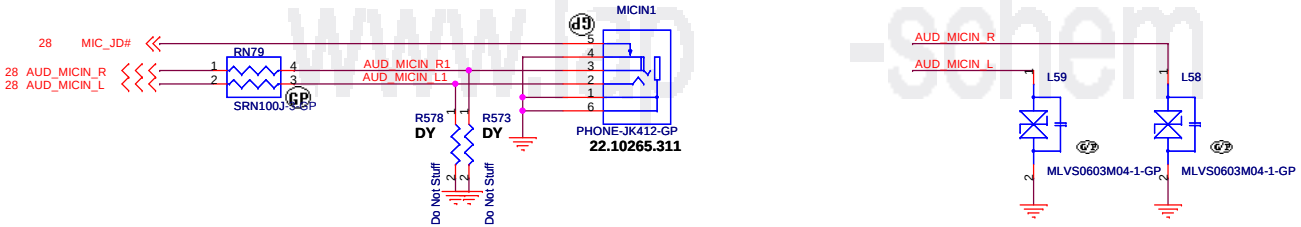
Internal Speaker



LINE OUT



MIC IN



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Title	**AUDIO JACK**
Size	Document Number: **JE70-DN** — Rev: **SB**
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No Modem Function

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Title: **MDC**

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5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD) on USB board

JE70-DN

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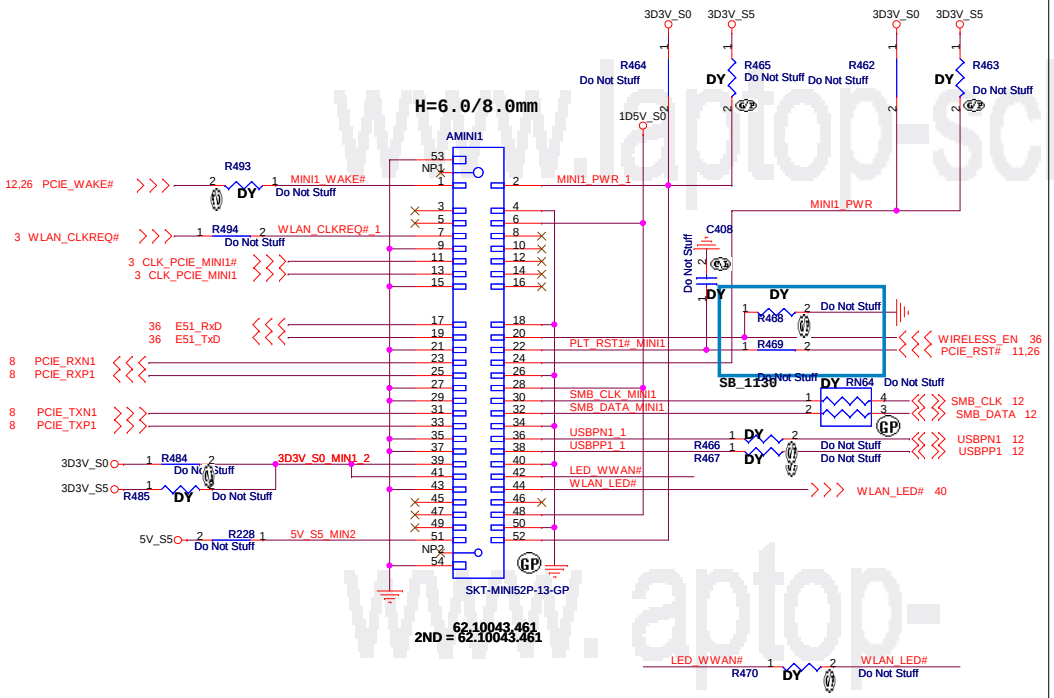
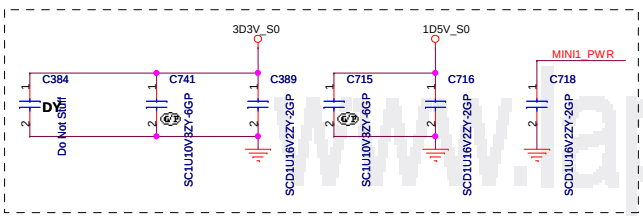
Title: **CARDREADER**		
Size	Document Number: **JE70-DN**	Rev: **SB**
Date: Thursday, November 19, 2009	Sheet 32 of 63	

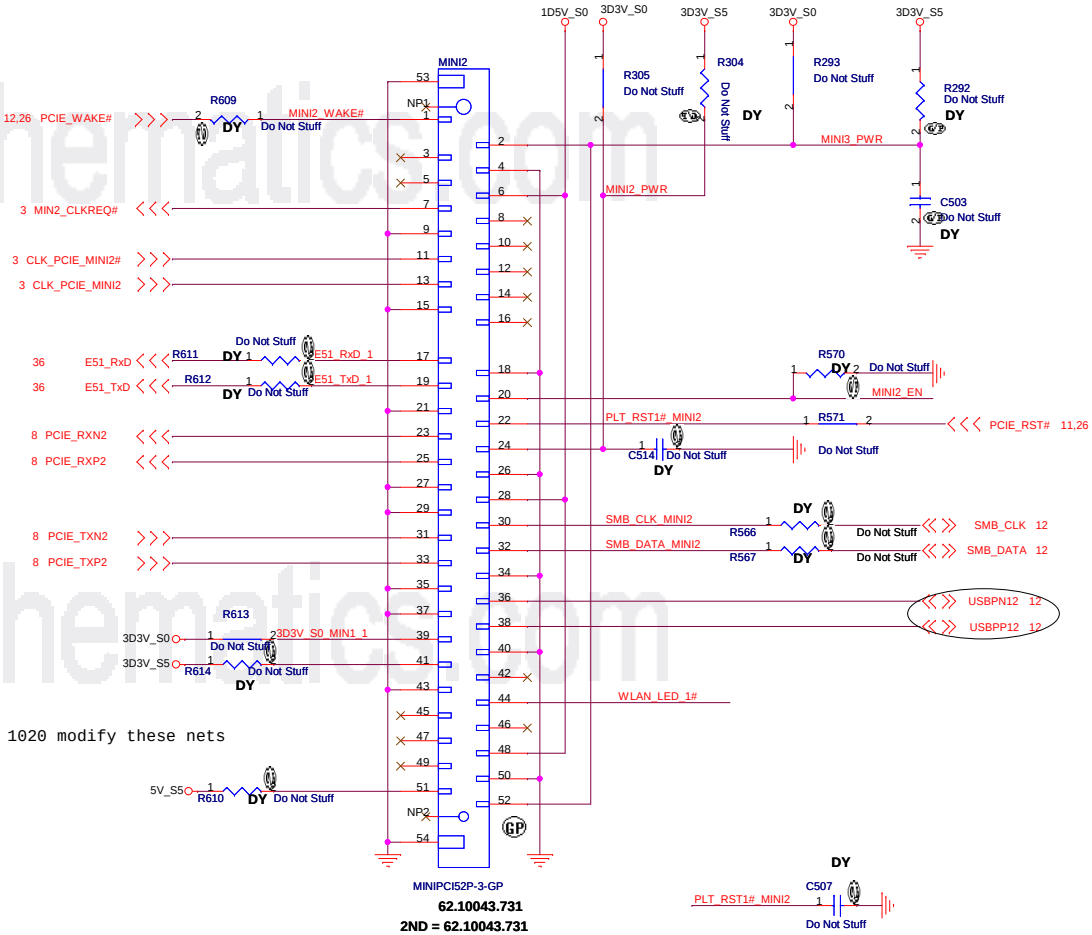
Mini Card Connector(WLAN)



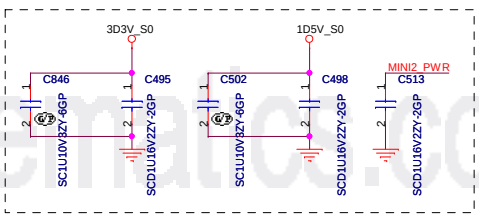
Place near AMINI1

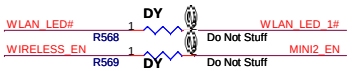


Mini Card Function



Place near MINIC2





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Title		
MINI CARD		
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No NEWCARD Function

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Title: NEW CARD		
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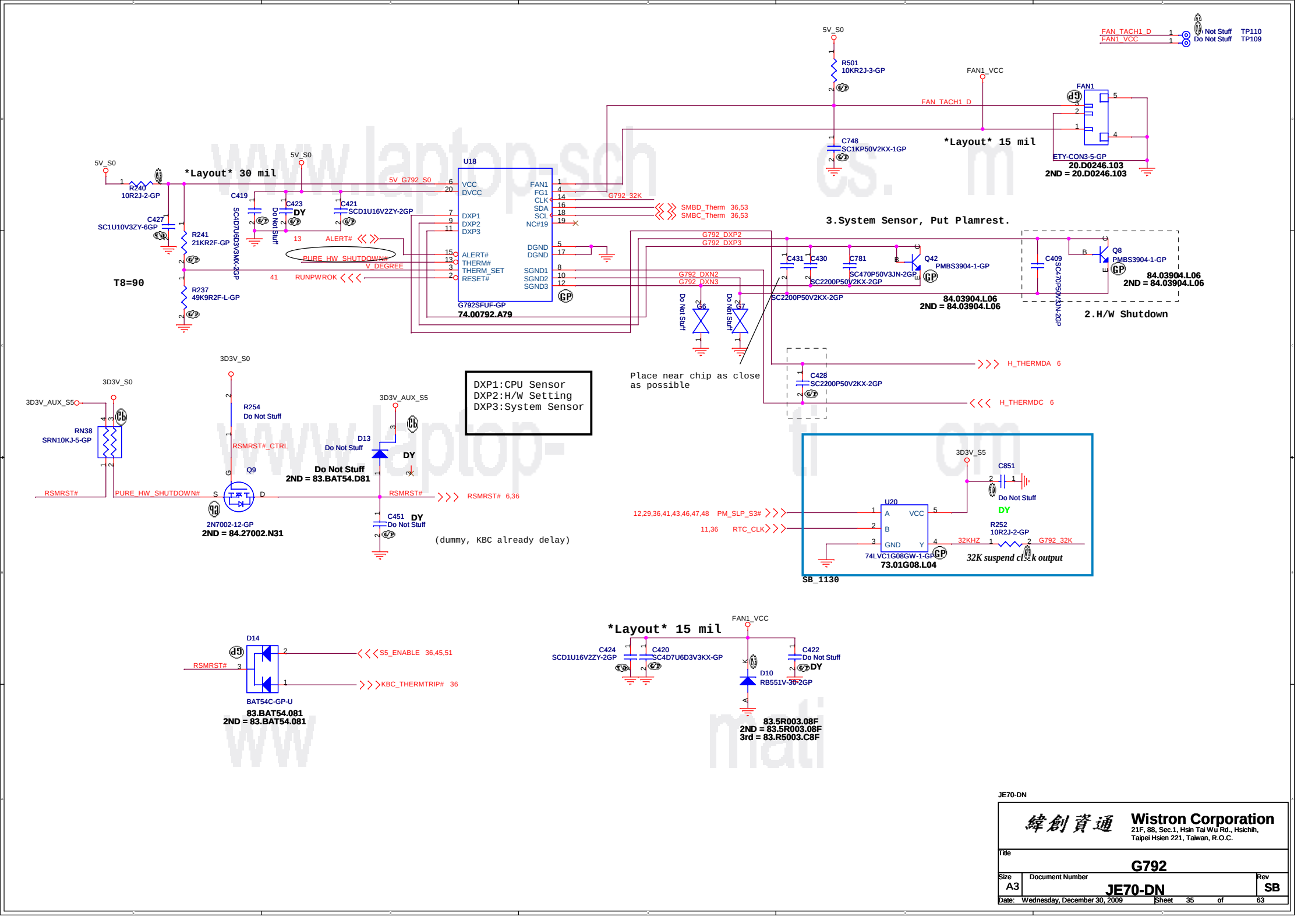

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Title		
G792		
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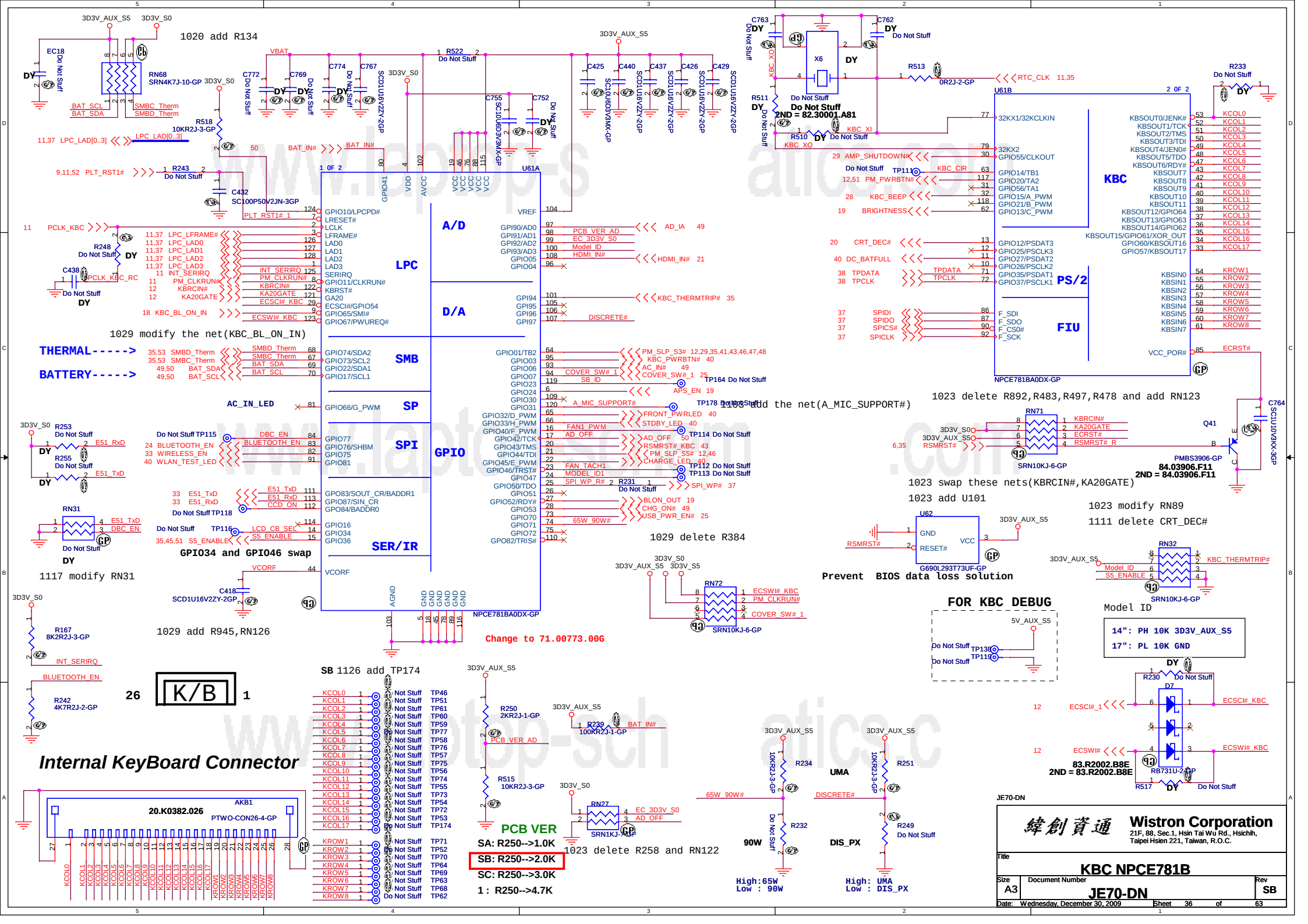
1020 add R134
1029 modify the net(KBC_BL_ON_IN)
THERMAL----->
BATTERY----->
1029 add R945,RN126
GPIO34 and GPIO46 swap
1117 modify RN31
1029 delete R384
Change to 71.00773.00G
SB 1126 add TP174
1023 delete R258 and RN122
1103 add the net(A_MIC_SUPPORT#)
1023 delete R892,R483,R497,R478 and add RN123
1023 swap these nets(KBRCIN#,KA20GATE)
1023 add U101
1023 modify RN89
1111 delete CRT_DEC#
Prevent BIOS data loss solution
FOR KBC DEBUG
Model ID
"14": PH 10K 3D3V_AUX_S5
"17": PL 10K GND
Internal KeyBoard Connector
PCB VER
SA: R250-->1.0K
SB: R250-->2.0K
SC: R250-->3.0K
1 : R250-->4.7K
High:65W
Low : 90W
High: UMA
Low : DIS_PX
Wistron Corporation
KBC NPCE781B
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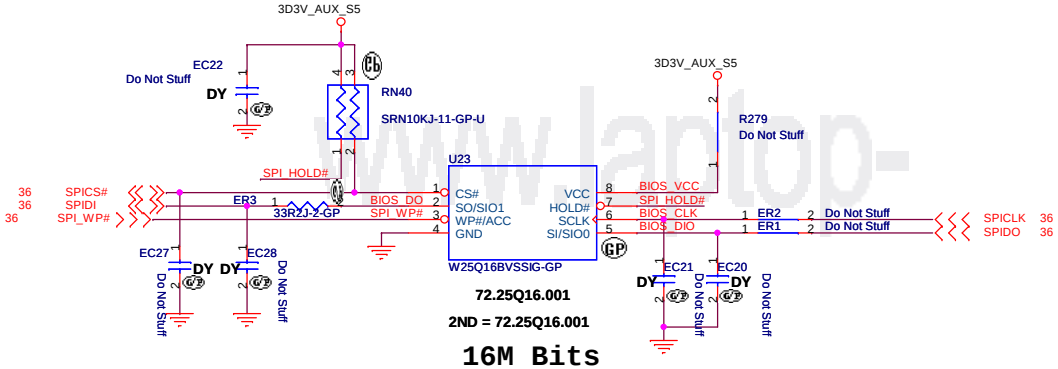
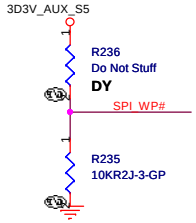
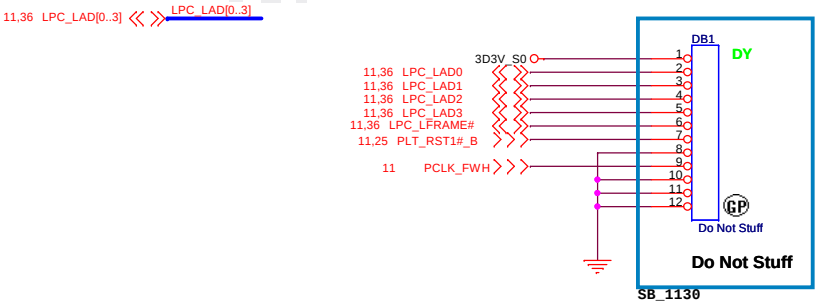


16M Bits

SPI FLASH ROM



GOLDEN FINGER FOR DEBUG BOARD



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Title: **BIOS**

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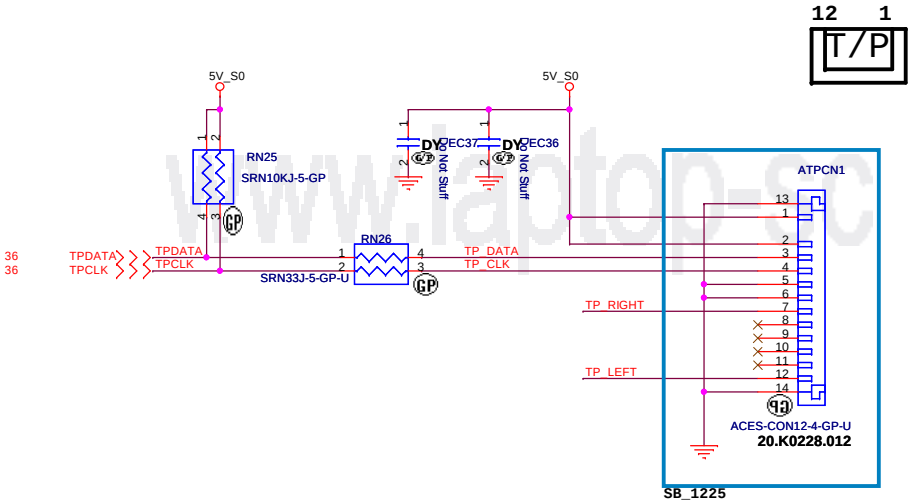

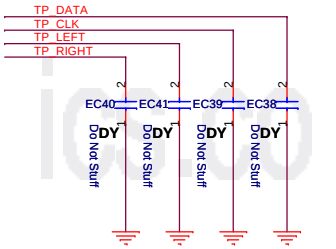

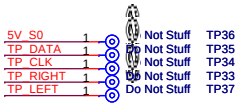

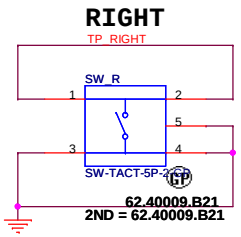

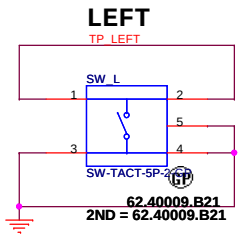

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Title: **Touch PAD**

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NONE BOARD

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Title: NONE BOARD

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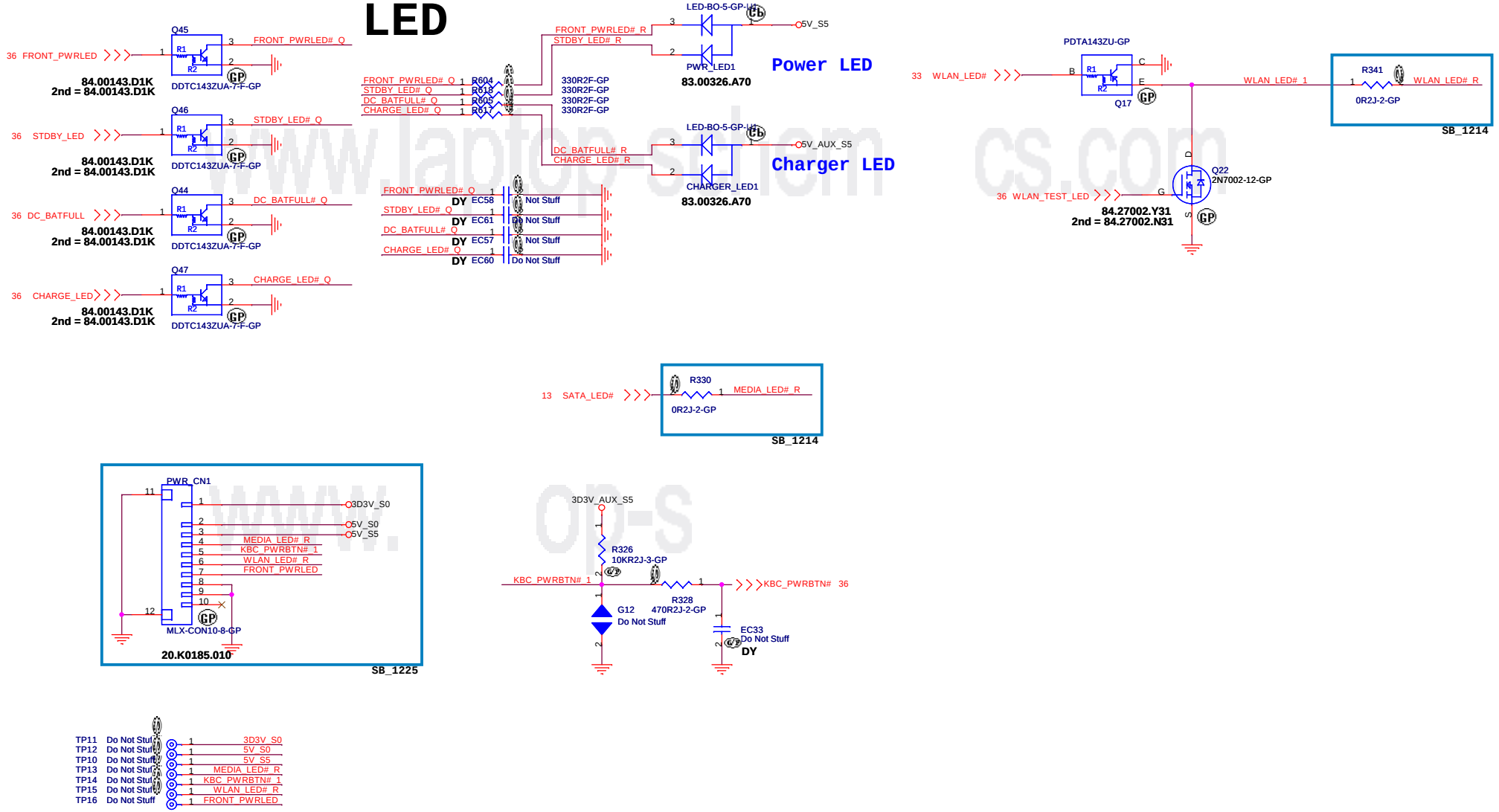
LED



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Title: LED		
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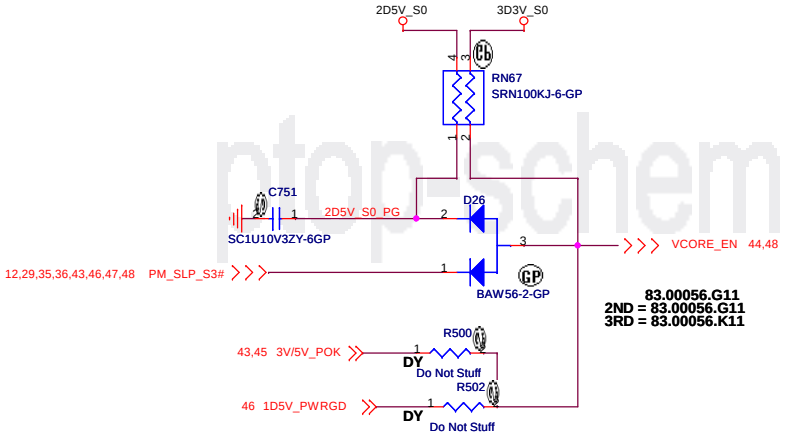
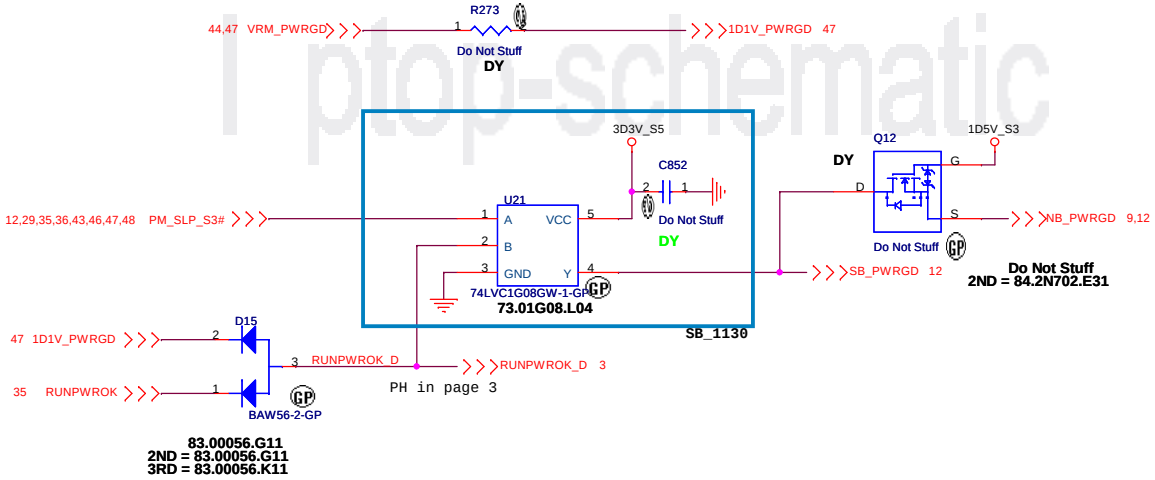


1D5V_S3_PWRGD

P/H @ 1D8V_S3 PAGE



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Title: POWER ON LOGIC

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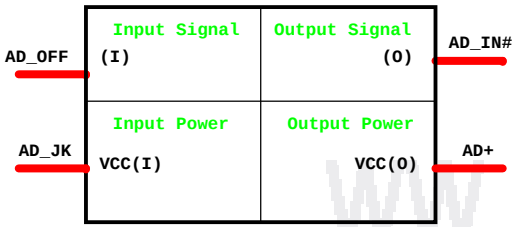
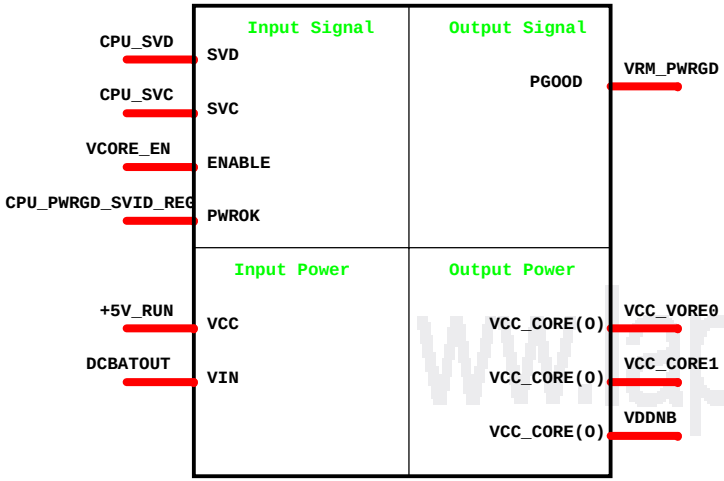
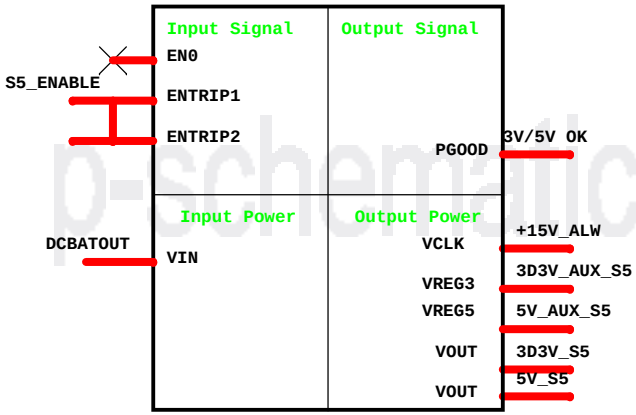
Adapter



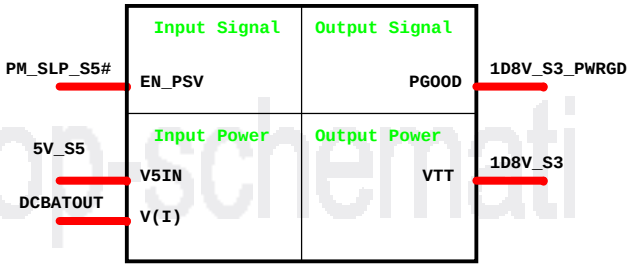
CPU_CORE
ISL6265HRTZ



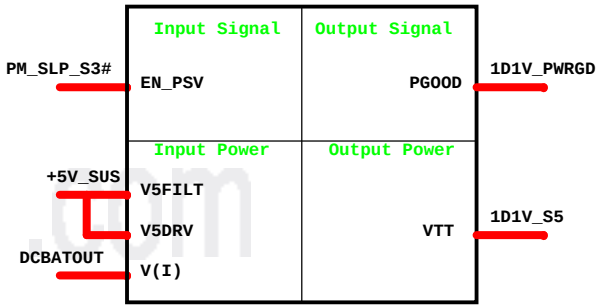
DCDC 5V/3D3V(RT8205A)



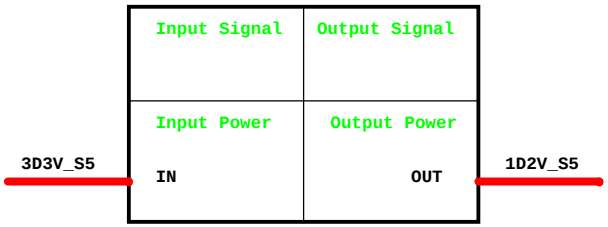
DCDC 1D8V(RT8209B)



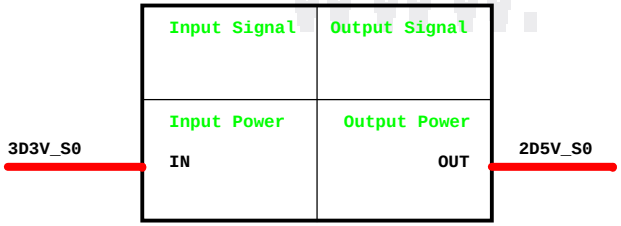
DCDC 1D1V(RT8209)



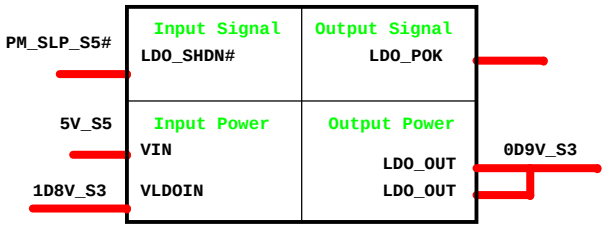
1D2V LDO G9161



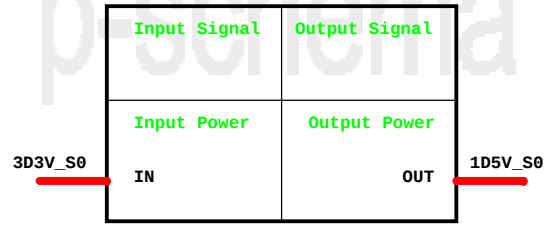
2D5V LDO R9161



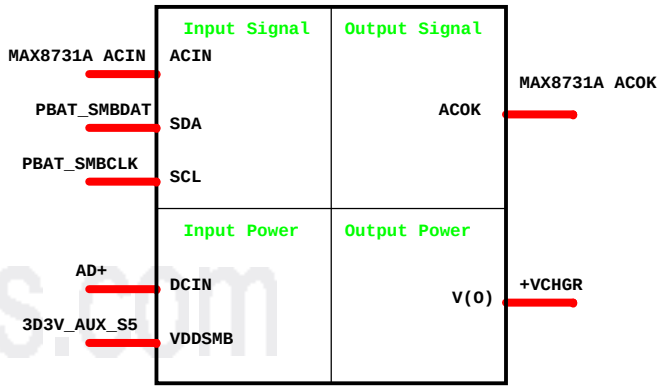
0D9V LDO RT9026



1D5V LDO G9571



CHARGER MAX8731



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Title: **Power Block Diagram**

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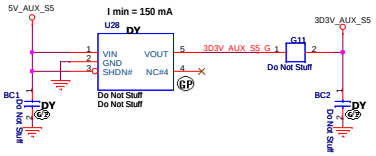
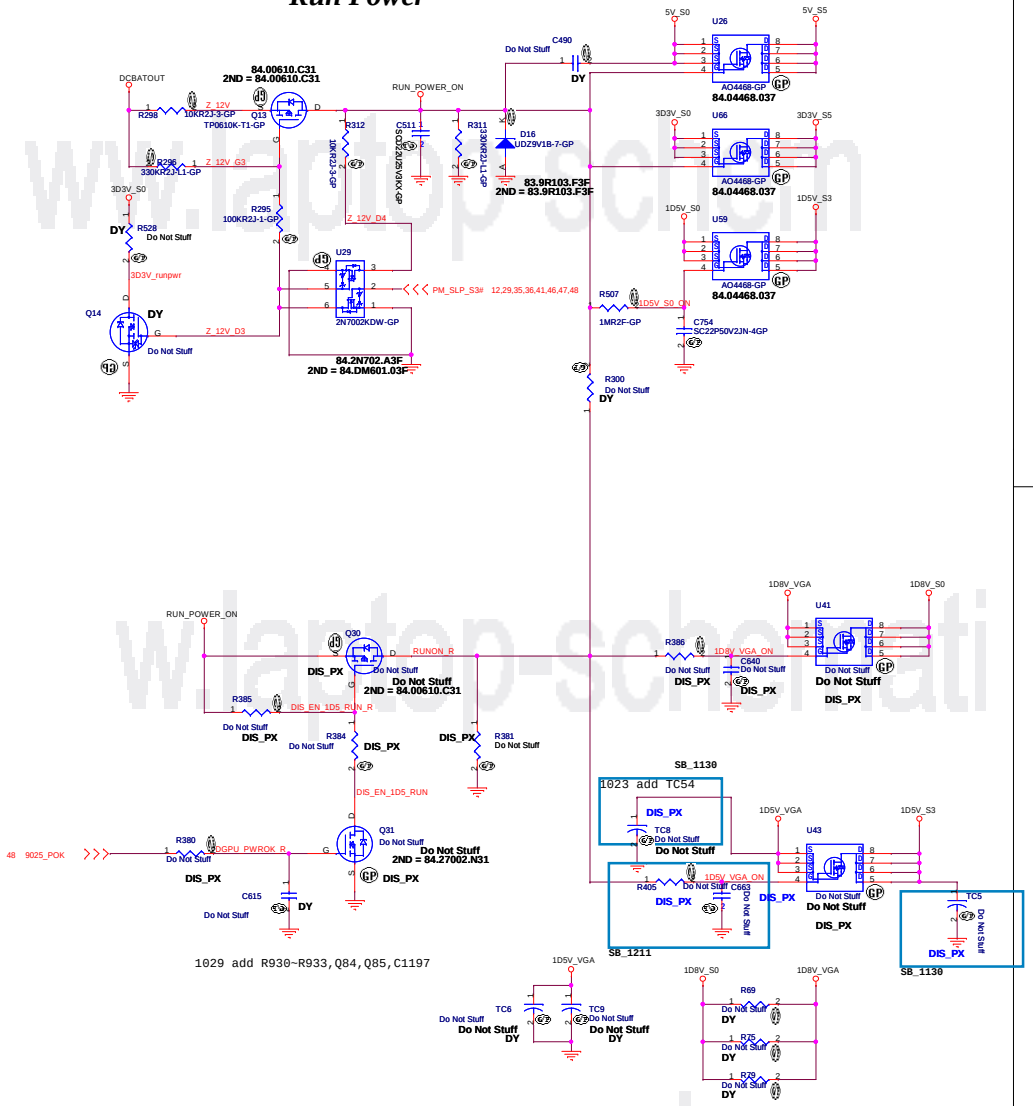
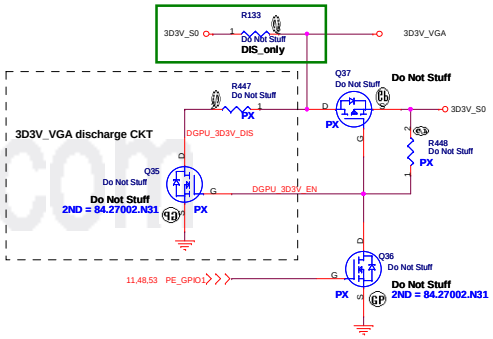
Aux Power 3D3V_AUX_S5

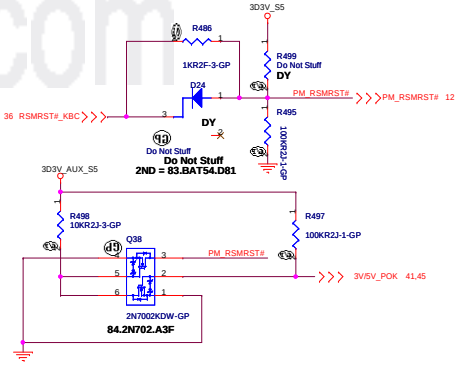


Run Power



+3VS to 3.3V_DELAY Transfer





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Title: RUN AND AUX POWER

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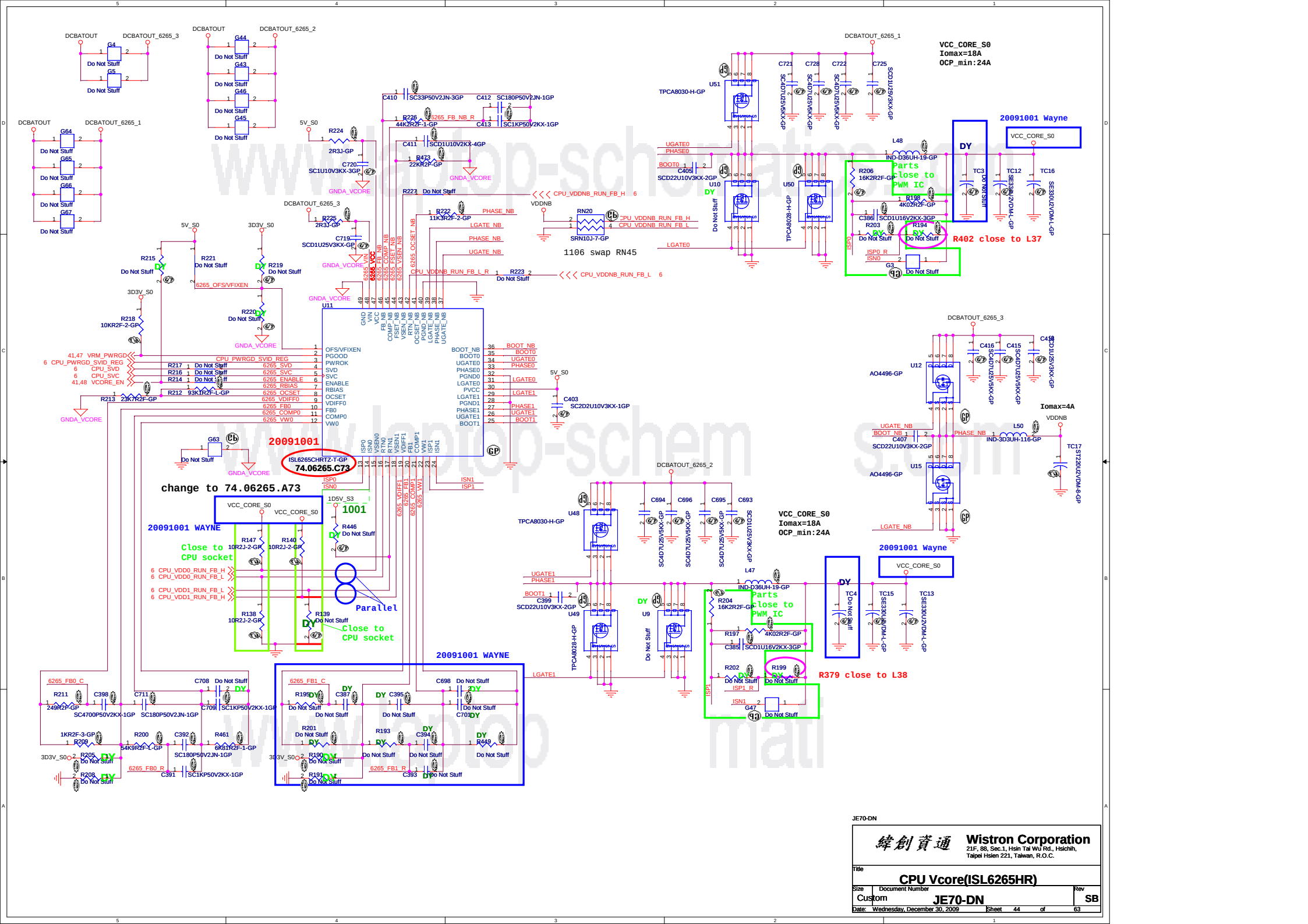
VCC_CORE_S0
Iomax=18A
OCP_min:24A
20091001 Wayne
Parts close to PWM IC
R402 close to L37
1106 swap RN45
20091001
ISL6265CHRTZ-T-GP
74.06265.C73
change to 74.06265.A73
20091001 WAYNE
Close to CPU socket
Parallel
R379 close to L38
Iomax=4A
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Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
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Custom
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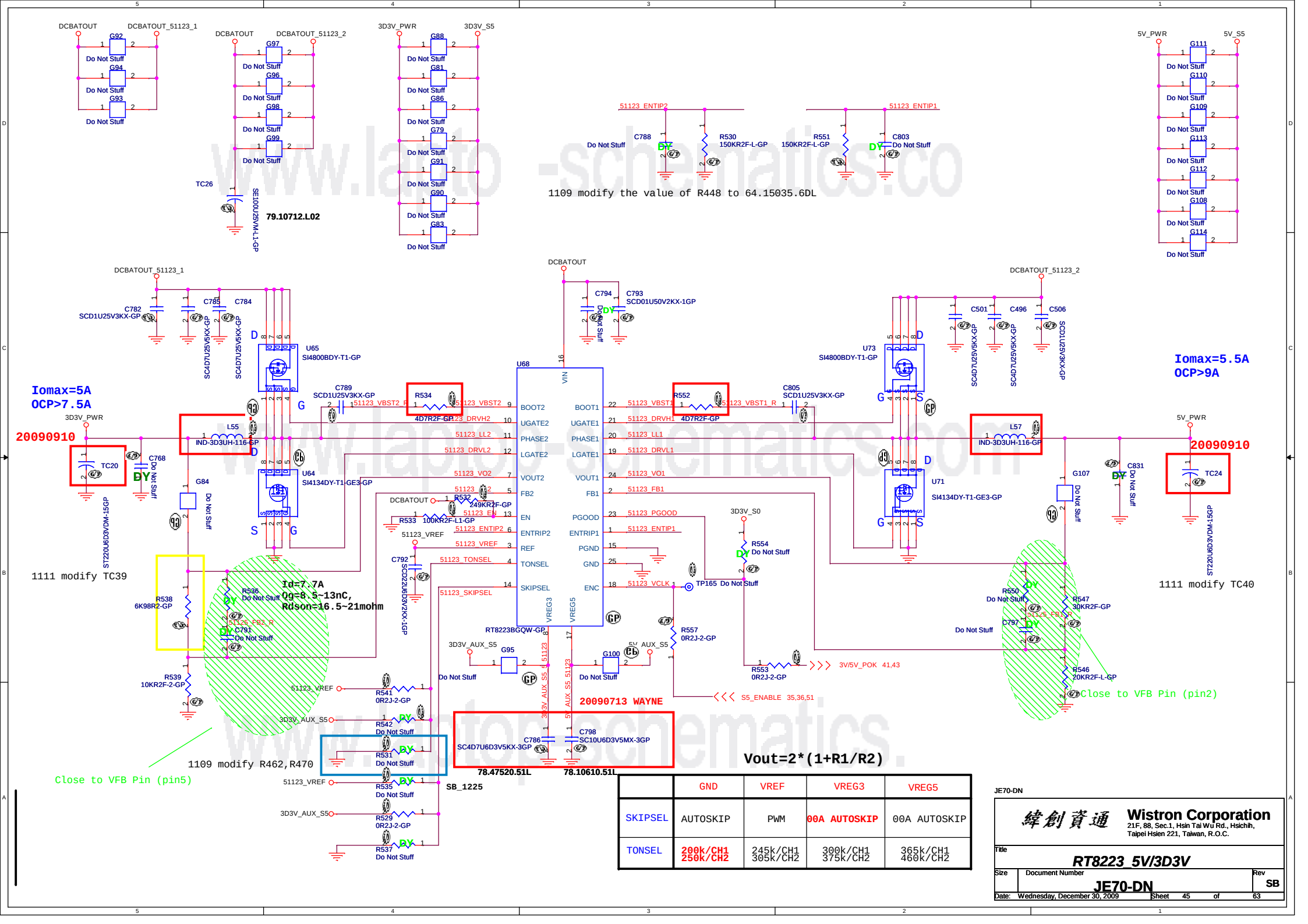

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

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Title: RT8223_5V/3D3V

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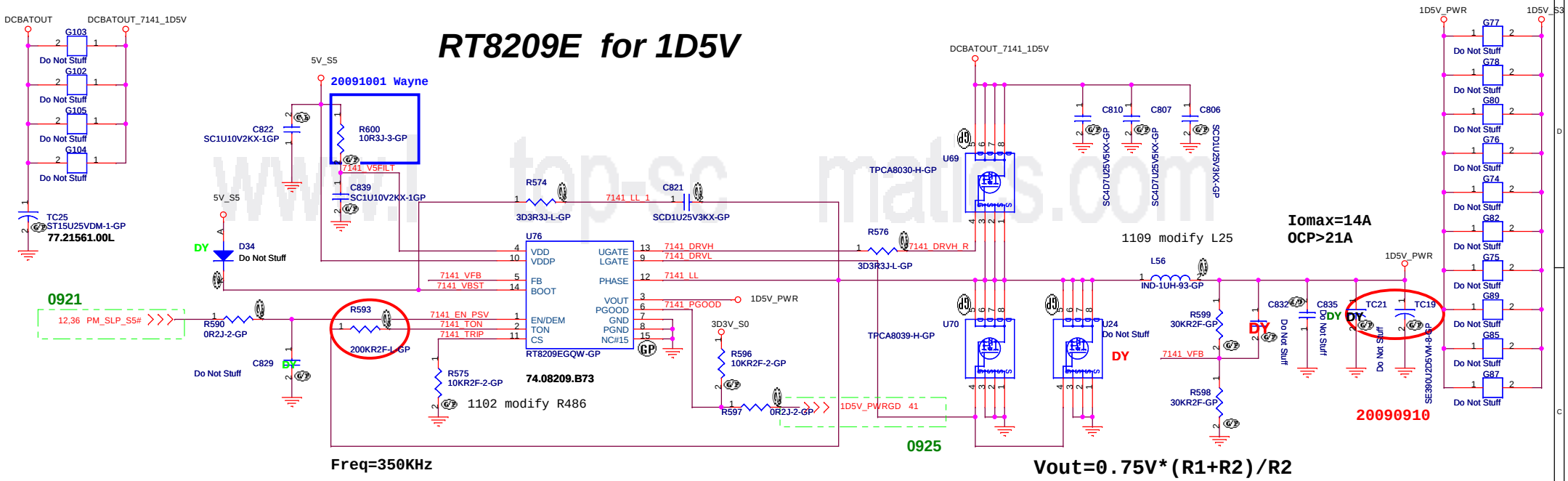
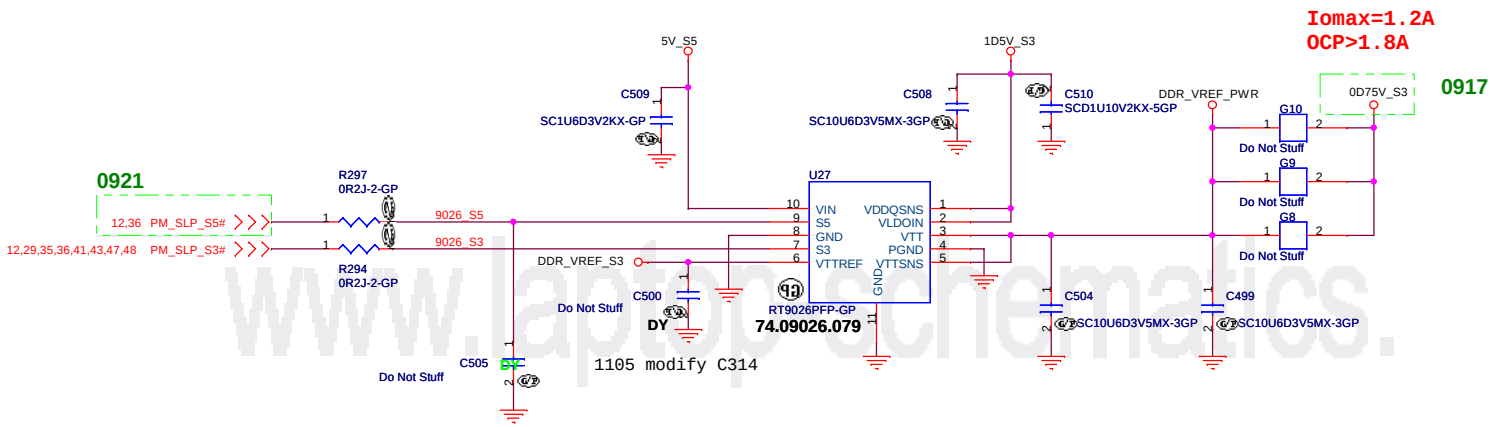
RT8209E for 1D5V



RT9026 for 0D75V_S3



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Title	RT8209E 1D5V	
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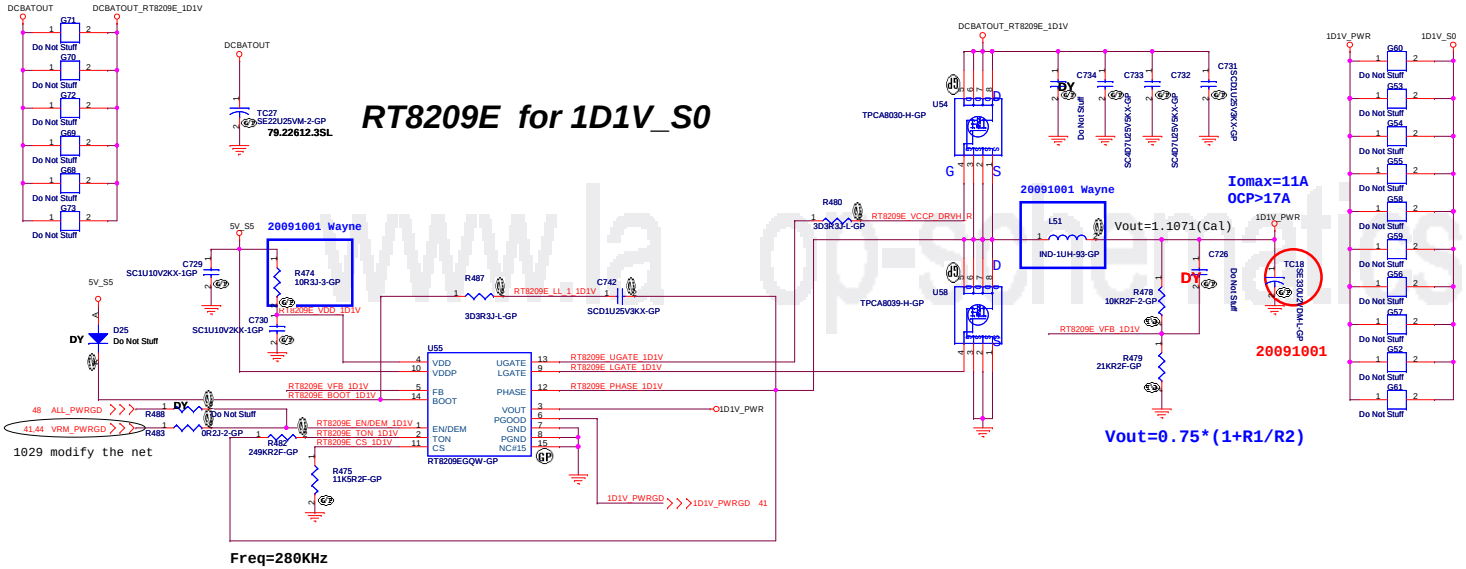

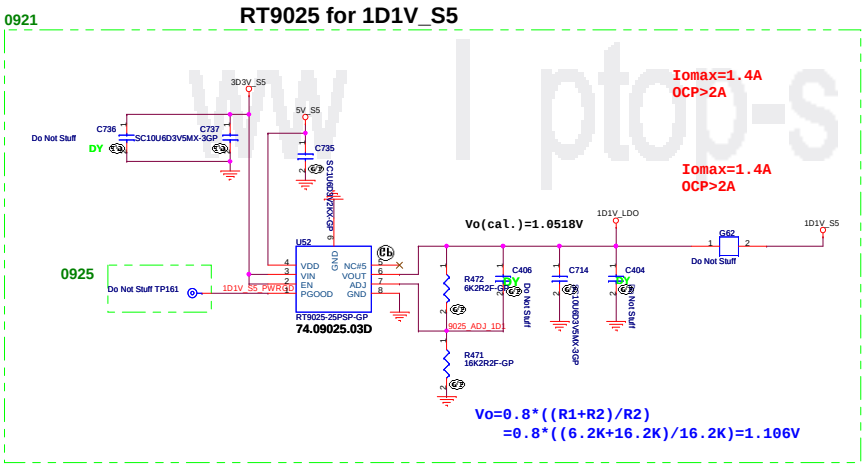

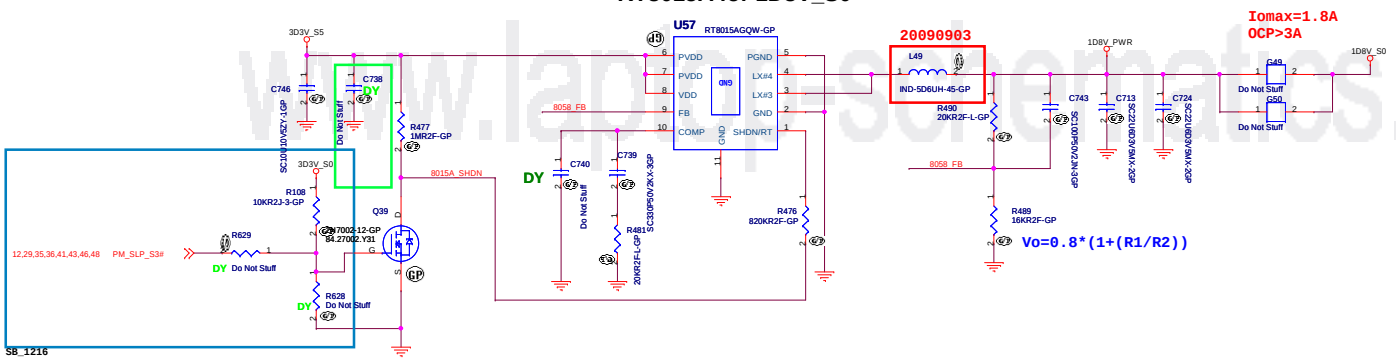

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Title: 1D1V_S0 & 1D1V_S5 & 1D8V_S0

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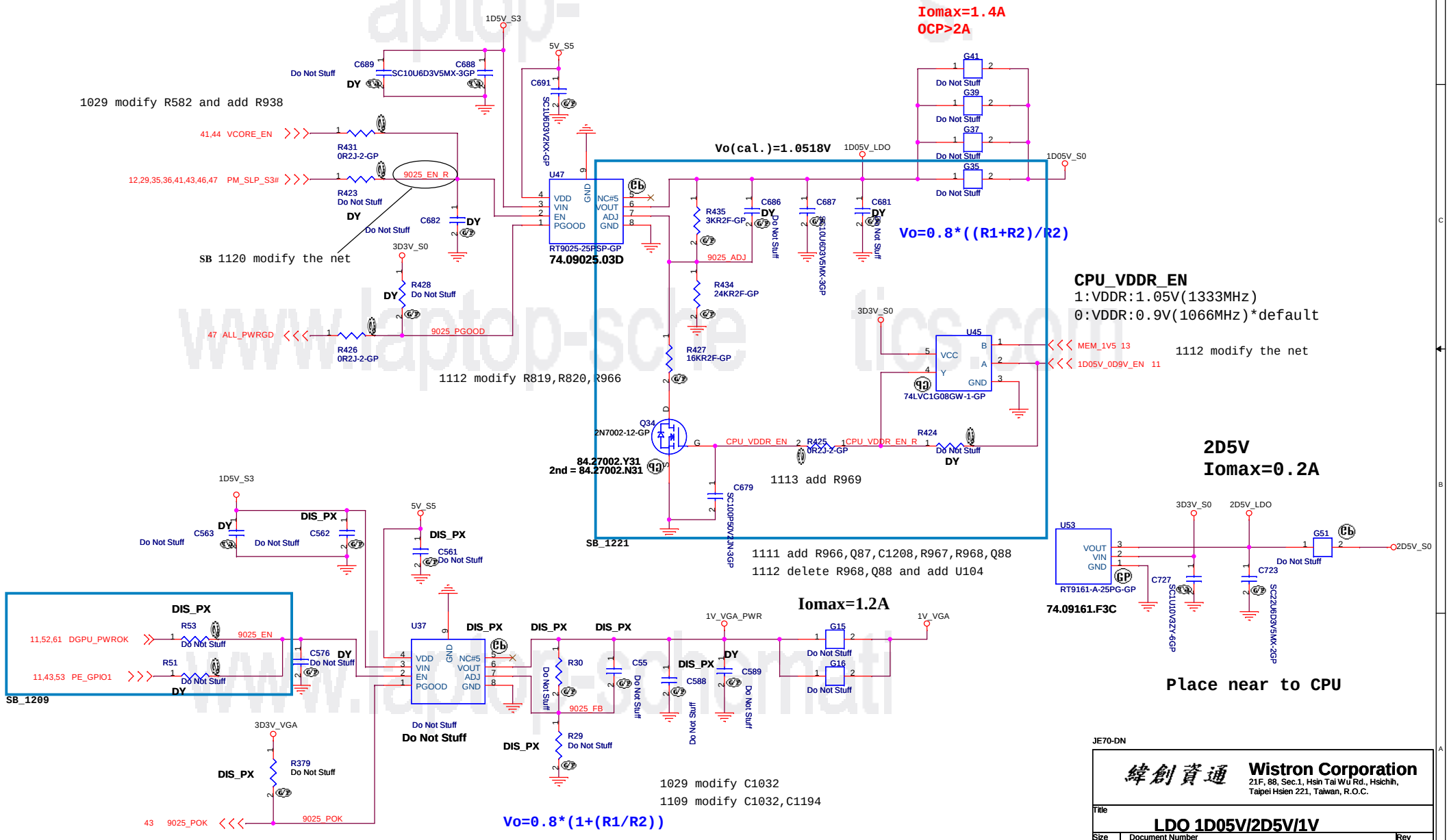
RT9025 for 1D05V_S0



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Title: LDO 1D05V/2D5V/1V		
Size: A3	Document Number: JE70-DN	Rev: SB
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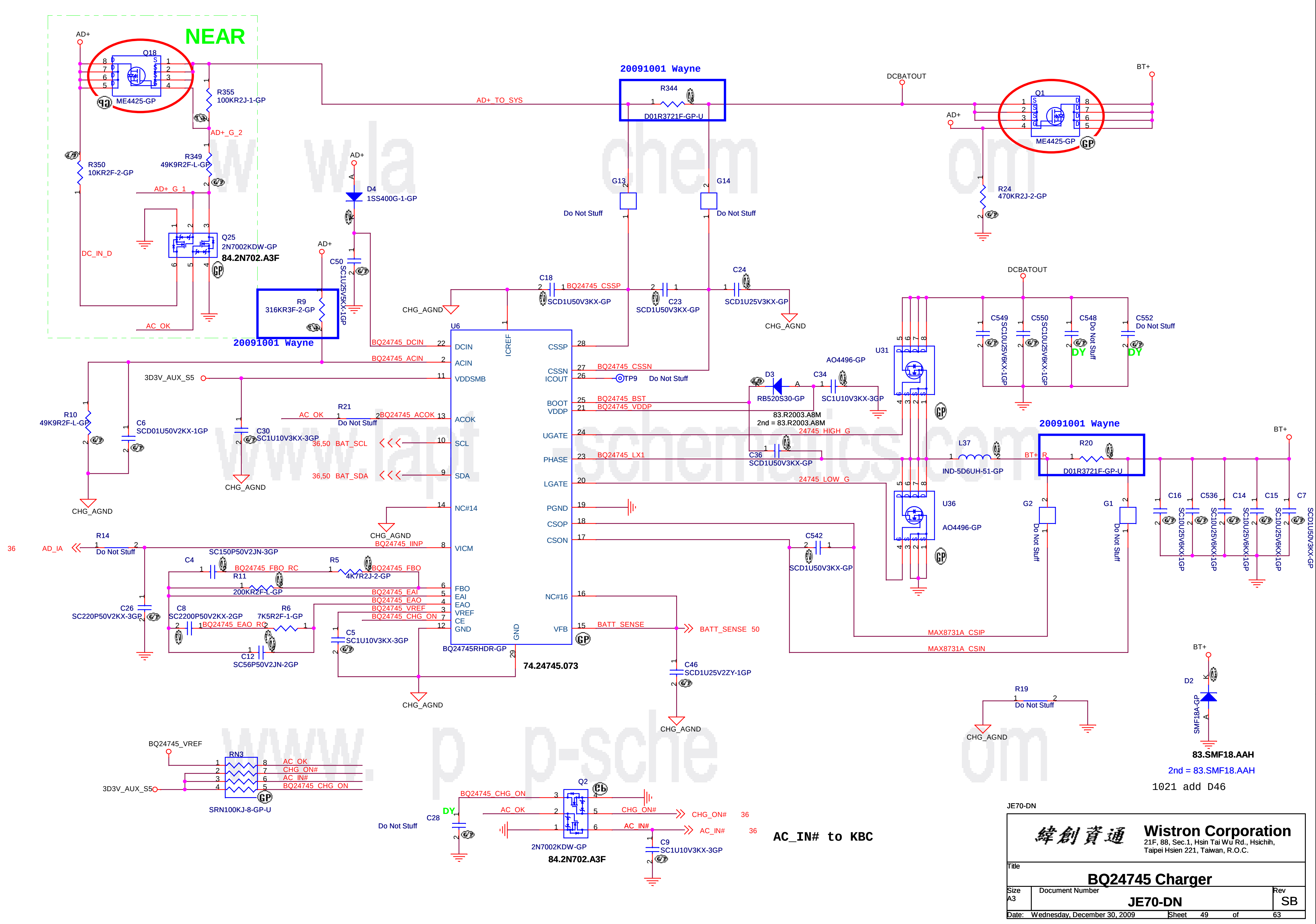
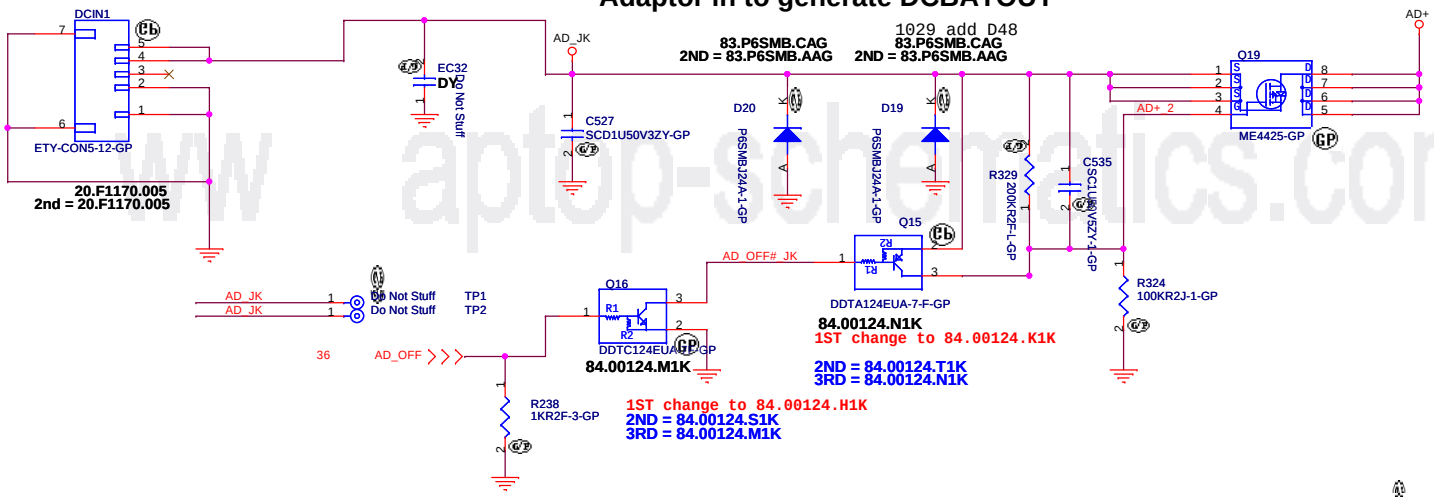

NEAR
AD+
Q18
ME4425-GP
R355
100KR2J-1-GP
AD+_G_2
R350
10KR2F-2-GP
R349
49K9R2F-L-GP
AD+_G_1
Q25
2N7002KDW-GP
84.2N702.A3F
DC_IN_D
AC_OK
AD+_TO_SYS
20091001 Wayne
R344
D01R3721F-GP-U
DCBATOUT
BT+
Q1
ME4425-GP
R24
470KR2J-2-GP
D4
1SS400G-1-GP
C50
SC1U25V5KX-1GP
R9
316KR3F-2-GP
G13
G14
Do Not Stuff
C18
BQ24745_CSSP
SCD1U50V3KX-GP
C23
C24
SCD1U25V3KX-GP
CHG_AGND
C549
C550
C548
C552
SC10U25V6KX-1GP
DY
U6
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
ICREF
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
BQ24745RHDR-GP
74.24745.073
BQ24745_CSSN
TP9
BQ24745_BST
BQ24745_VDDP
24745_HIGH_G
BQ24745_LX1
24745_LOW_G
D3
RB520S30-GP
83.R2003.A8M
2nd = 83.R2003.A8M
C34
SC1U10V3KX-3GP
AO4496-GP
U31
U36
C36
SCD1U50V3KX-GP
L37
IND-5D6UH-51-GP
R20
D01R3721F-GP-U
G2
G1
C16
C536
C14
C15
C7
SCD1U50V3KX-GP
R10
49K9R2F-L-GP
C6
SCD01U50V2KX-1GP
C30
SC1U10V3KX-3GP
R21
BQ24745_ACOK
36,50 BAT_SCL
36,50 BAT_SDA
R14
36 AD_IA
BQ24745_IINP
SC150P50V2JN-3GP
C4
BQ24745_FBO_RC
R5
BQ24745_FBO
4K7R2J-2-GP
R11
200KR2F-L-GP
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
C26
SC220P50V2KX-3GP
C8
SC2200P50V2KX-2GP
BQ24745_EAO_RC
R6
7K5R2F-1-GP
C5
SC1U10V3KX-3GP
C12
SC56P50V2JN-2GP
C542
SCD1U50V3KX-GP
BATT_SENSE
BATT_SENSE 50
C46
SCD1U25V2ZY-1GP
MAX8731A_CSIP
MAX8731A_CSIN
R19
D2
SMF18A-GP
83.SMF18.AAH
2nd = 83.SMF18.AAH
1021 add D46
BQ24745_VREF
RN3
SRN100KJ-8-GP-U
AC_OK
CHG_ON#
AC_IN#
BQ24745_CHG_ON
Q2
2N7002KDW-GP
84.2N702.A3F
C28
CHG_ON# 36
AC_IN# 36
C9
SC1U10V3KX-3GP
AC_IN# to KBC
JE70-DN
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size A3
Document Number
JE70-DN
Rev SB
Date: Wednesday, December 30, 2009
Sheet 49 of 63

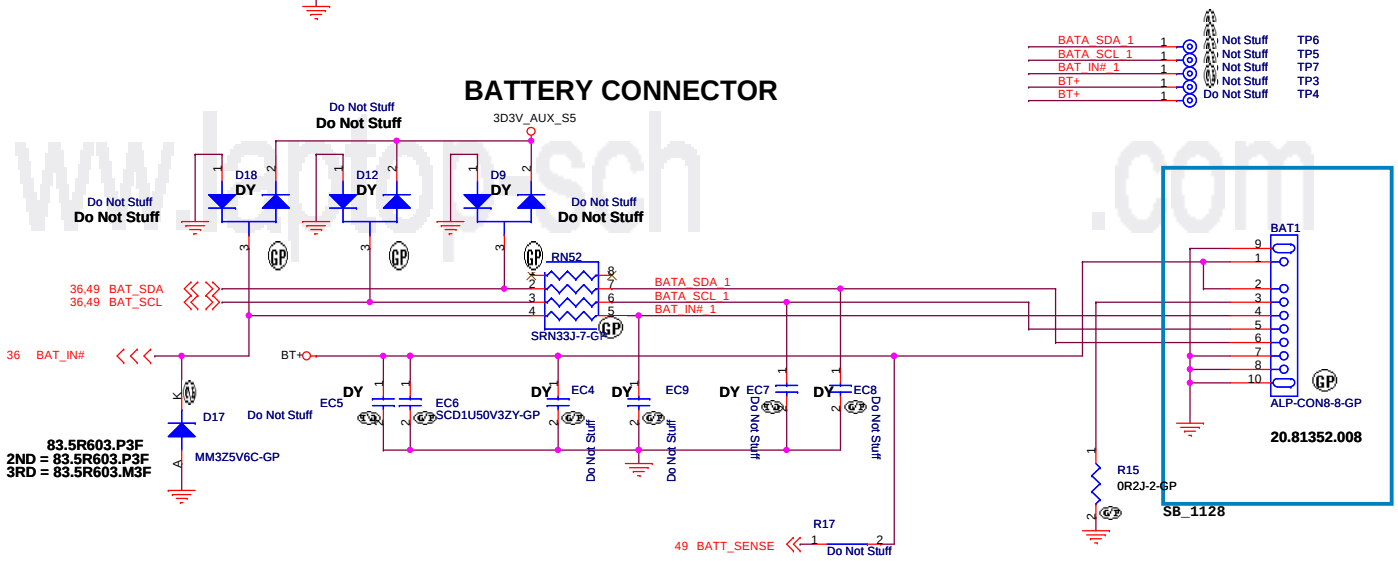
1021 modify DCIN1

1Pin=3A

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Pin NO	Symbol
1	GND
2	GND
3	SMD
4	SMC
5	TS
6	B/I
7	BT+
8	BT+

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Title: **AD/BATT CONN**

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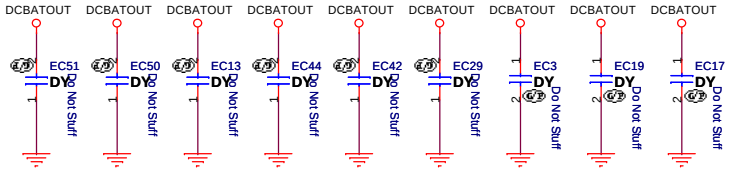

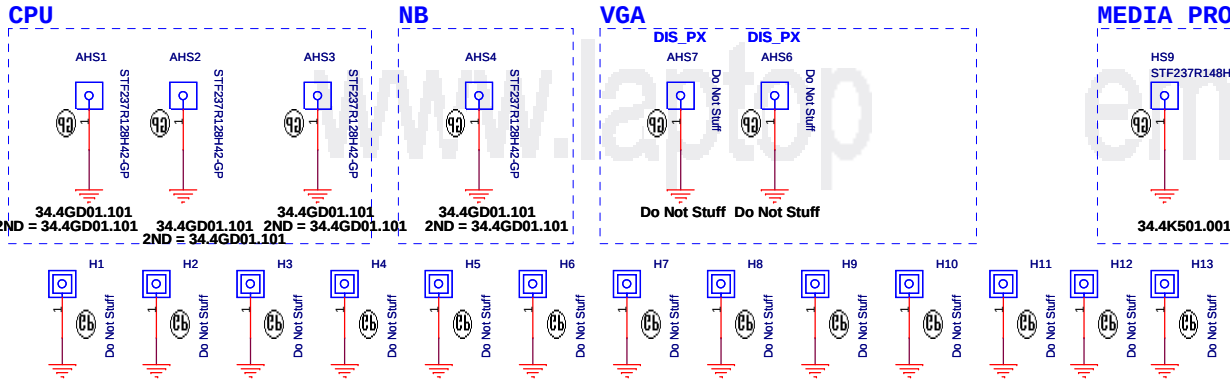

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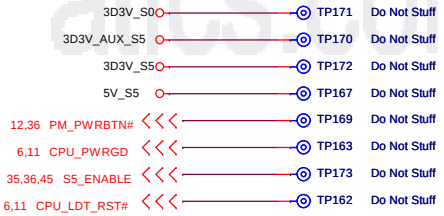
atics.com

Check test point



Test Point放在Dimm Door打開可量測處

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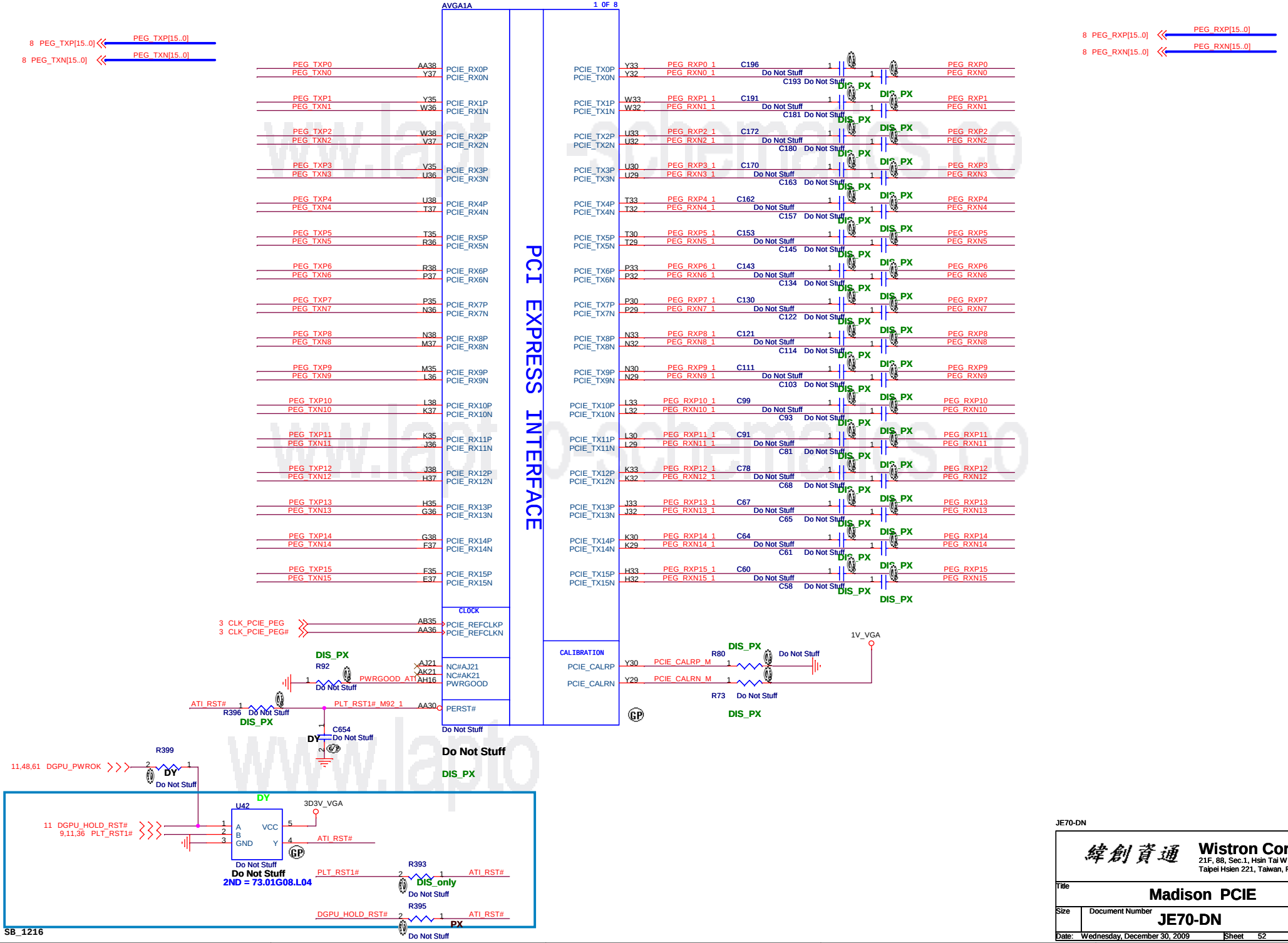
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size | Document Number: JE70-DN | Rev: SB

Date: Wednesday, December 30, 2009 | Sheet 51 of 63



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Taipei Hsien 221, Taiwan, R.O.C.

Title	Madison PCIE	
Size	Document Number JE70-DN	Rev SB
Date: Wednesday, December 30, 2009	Sheet 52 of 63	

JV50-CP_JV70-CP_SJV50-CP / Madsion-Pro

0 1 0 0 Hynix Orion-die(H5TQ1G63BFR-12C,800MHz)64*16 x 8 pcs1GB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 8 pcs1GB
1 1 0 0 Reserve64*16 x 8 pcs1GB

JV50-CP_JV70-CP_SJV50-CP / Park-XT

0 1 0 0 Hynix Orion-die (H5TQ1G63BFR-12C, 800MHz)64*16 x 4 pcs512MB
1 0 0 0 Samsung E-die (K4W1G1646E-HC12, 800MHz)64*16 x 4 pcs512MB
1 1 0 0 Reserve64*16 x 4 pcs512MB

1113 delete TP103,TP122,TP160,TP178

1029 add R940,R941

1026 add R905,R906

1113 add R968

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

For Thermal sensor

PE_GPIO1
L=>
H=>

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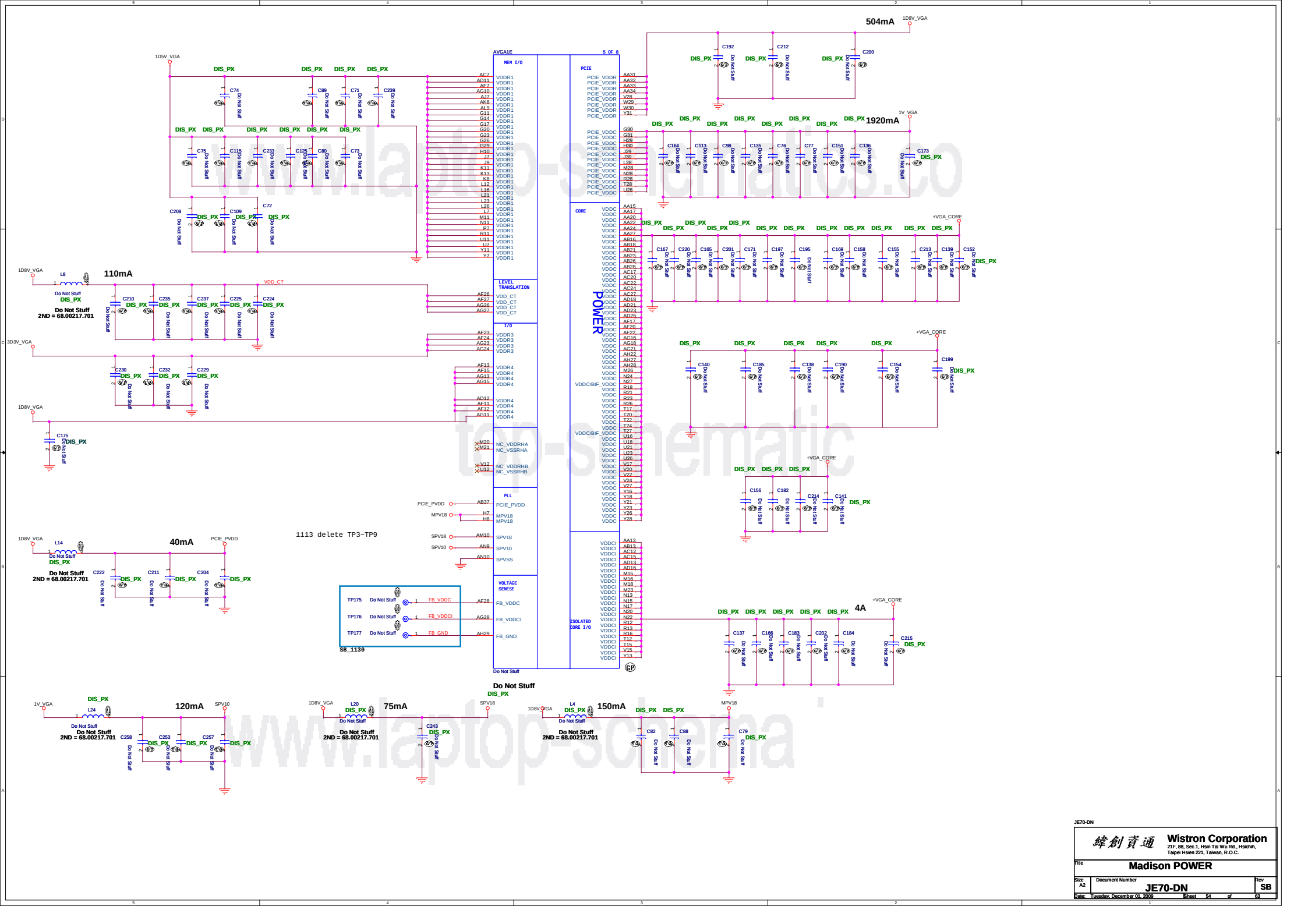
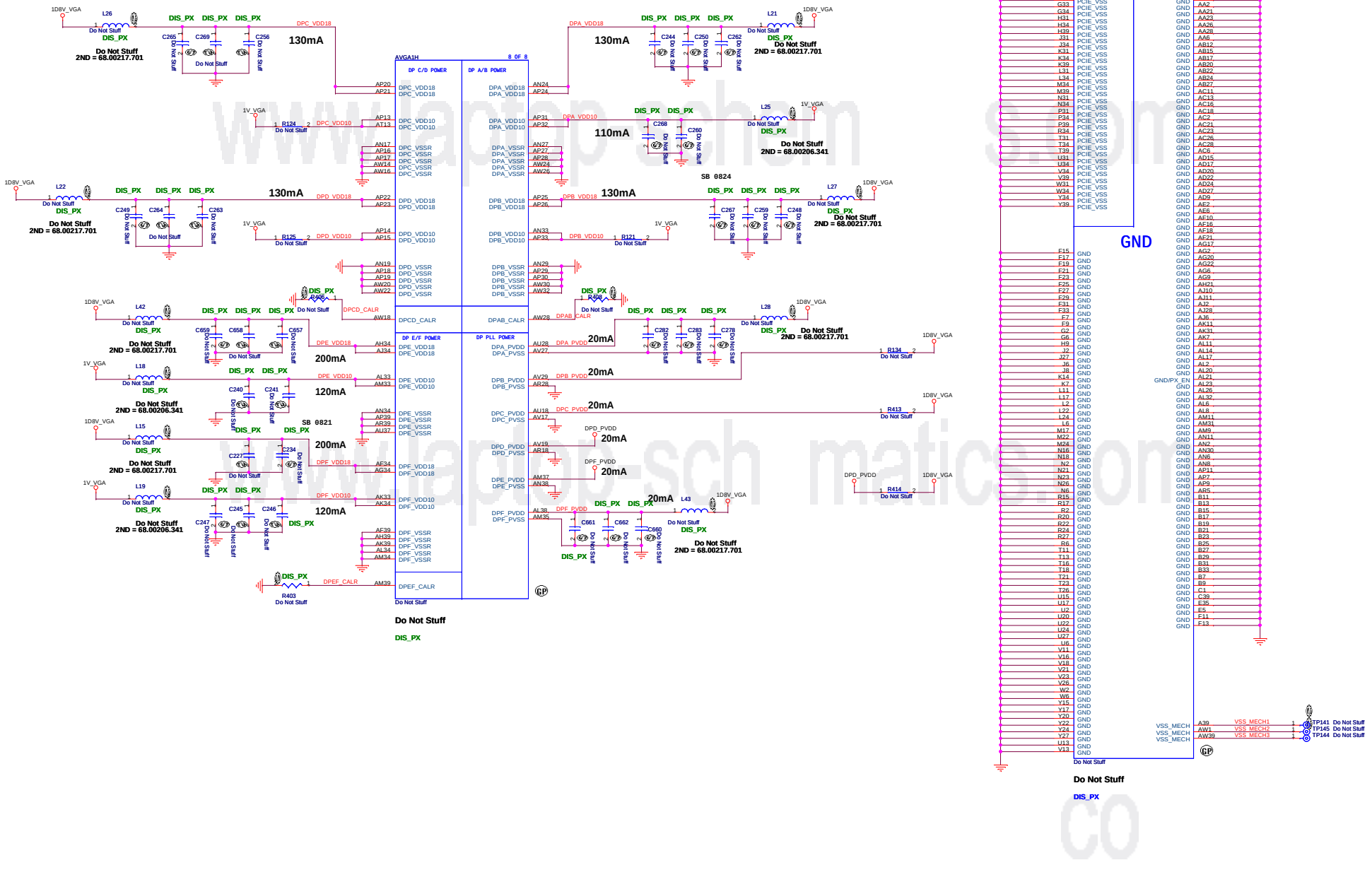
JE70-DN	
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Madison IO
Size	Document Number JE70-DN Rev SB
Date: Wednesday, December 30, 2009	Sheet 53 of 63


504mA
1920mA
110mA
40mA
120mA
75mA
150mA
4A
1D8V_VGA
1V_VGA
1D5V_VGA
3D3V_VGA
+VGA_CORE
AVGA1E
MEM I/O
PCIE
CORE
POWER
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENESE
ISOLATED CORE I/O
Do Not Stuff
DIS_PX
1113 delete TP3~TP9
SB_1130
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison POWER
JE70-DN
Size A2
Rev SB
Date: Tuesday, December 01, 2009
Sheet 54 of 63



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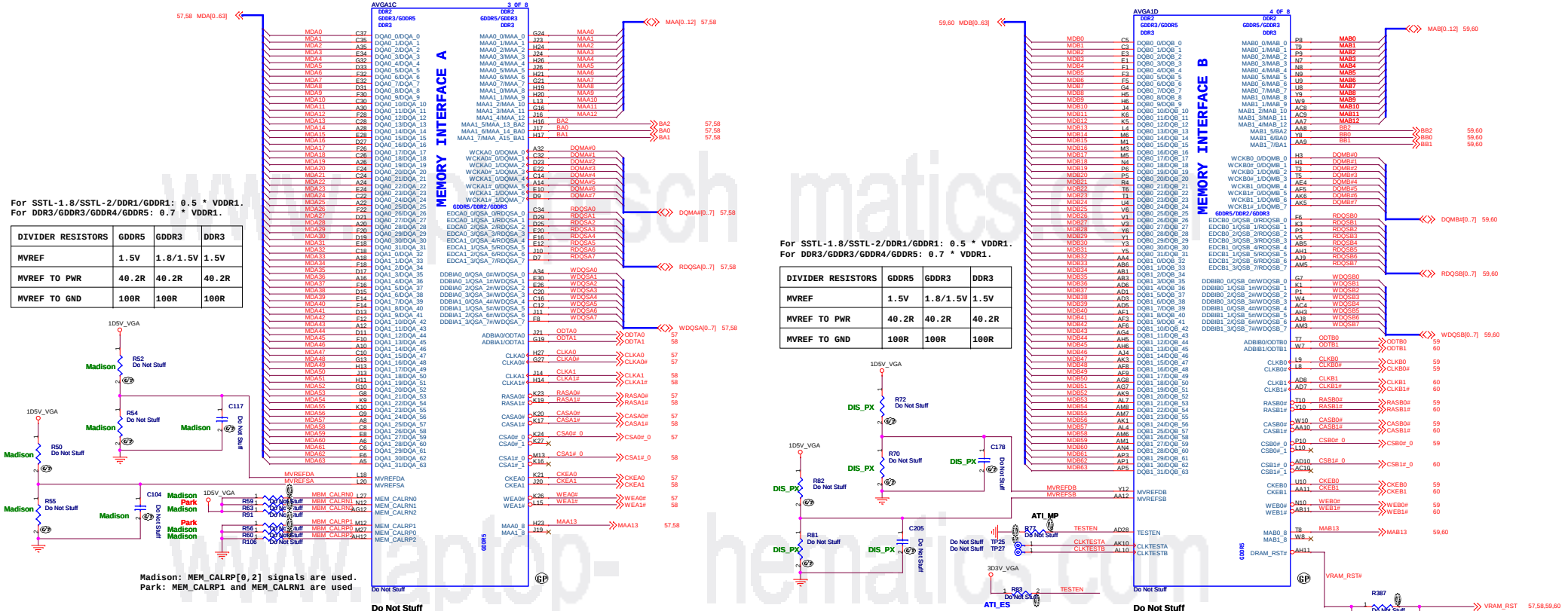
Taipei Hsien 221, Taiwan, R.O.C.

Title: DP POWER_GND

Size	Document Number	Rev
A2	JE70-DN	SB

Date: Thursday, December 24, 2009 Sheet 55 of 63



STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter_Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison Memory / Straps

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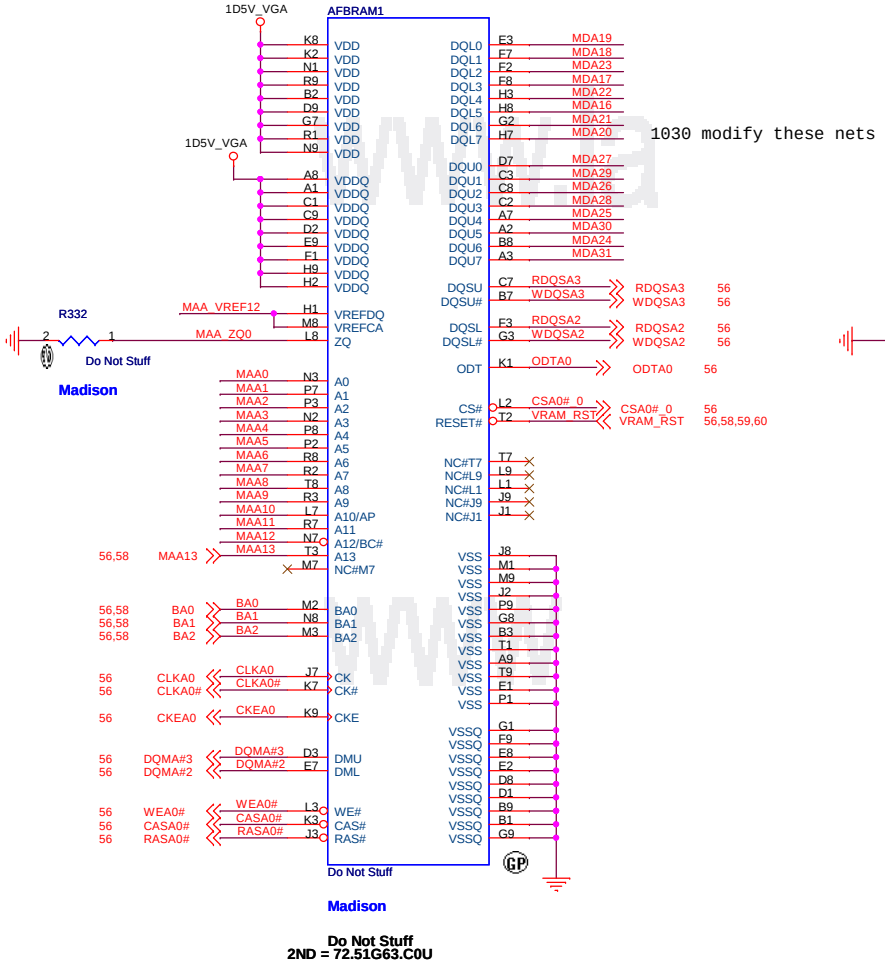
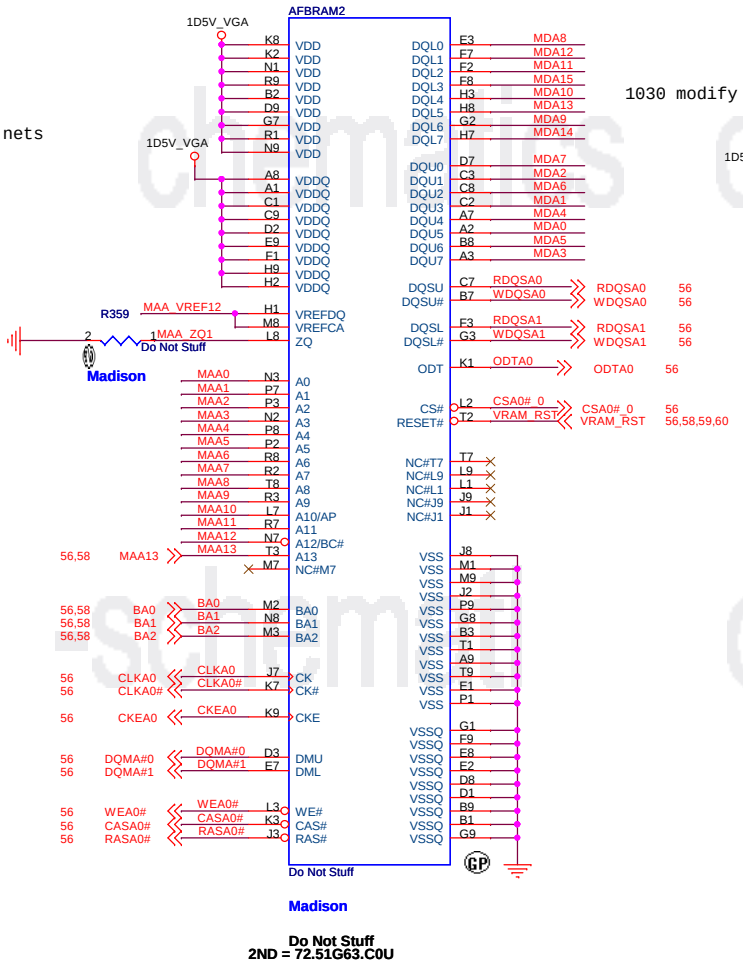
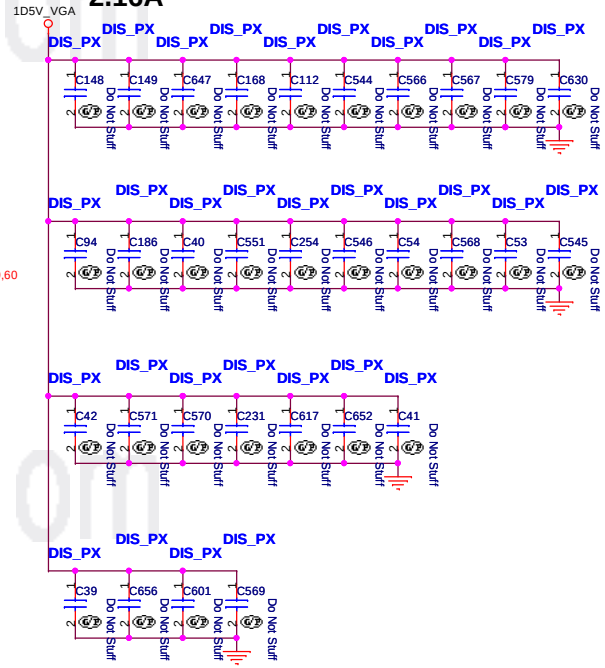
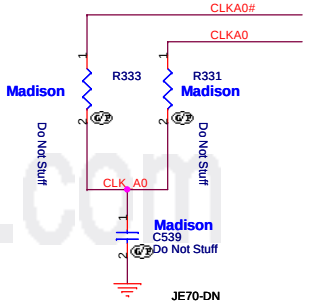
Date: Wednesday, December 30, 2009 | Sheet 56 of 63

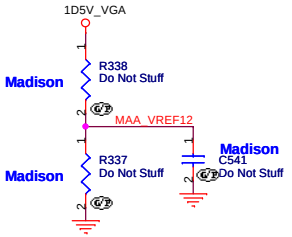
DDR3











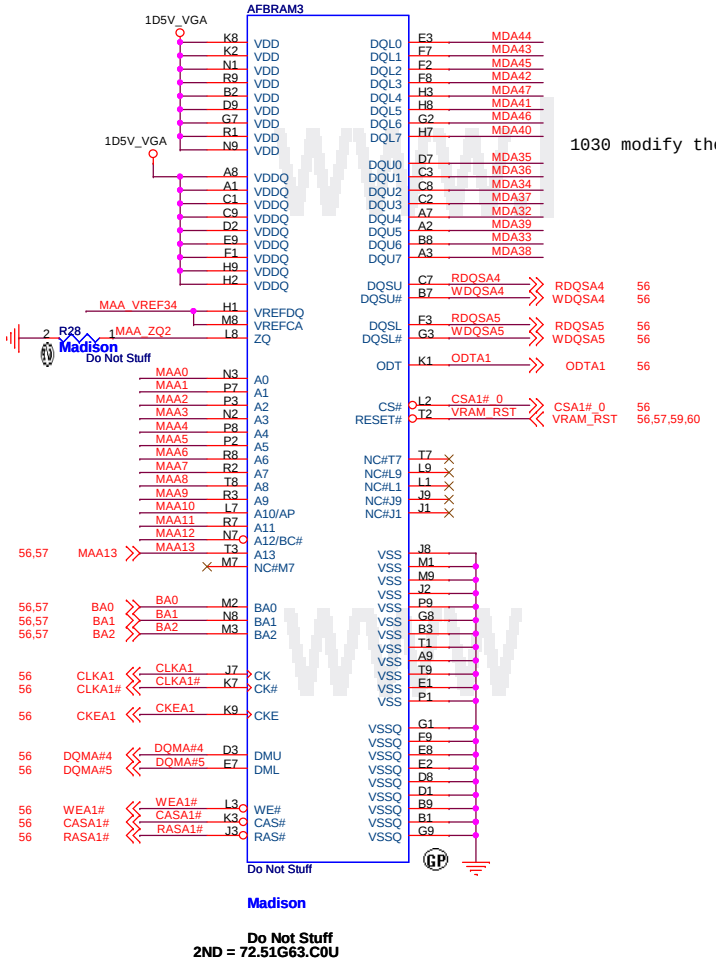
SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)

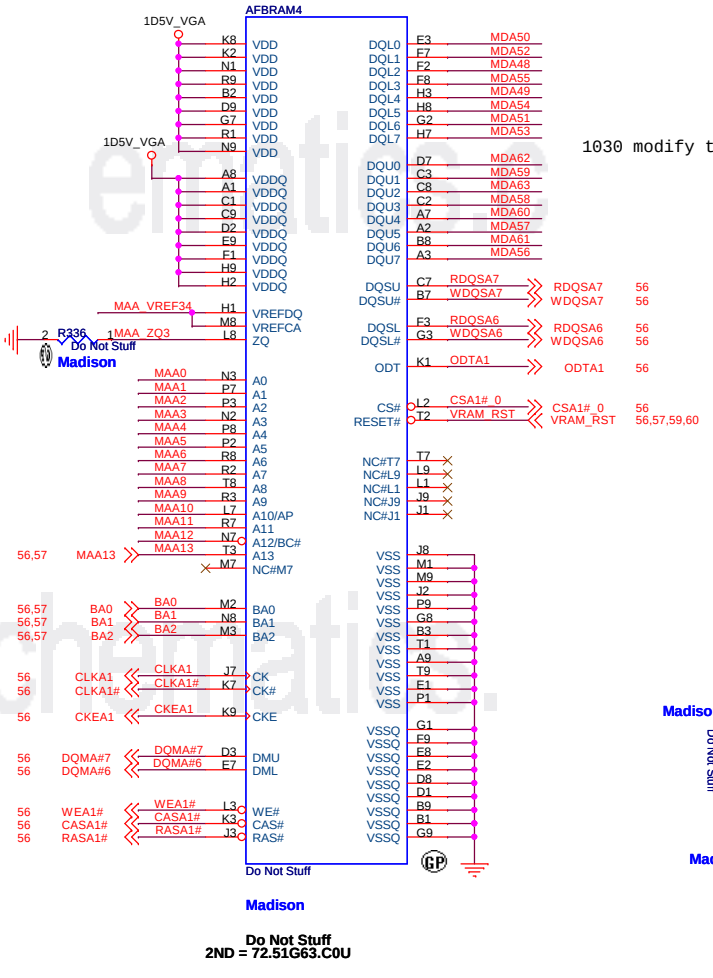
56,58 DQMA#[0..7]
56,58 RDQSA[0..7]
56,58 WDQSA[0..7]
56,58 MAA[0..12] MAA[0..12]
56,58 MDA[0..63] MDA[0..63]

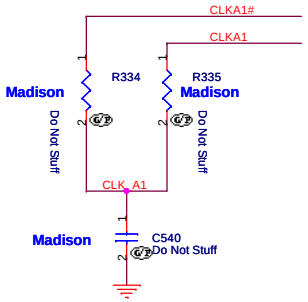
JE70-DN

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(1/4)***	
Size A3	Document Number **JE70-DN**	Rev SB
Date: Wednesday, December 30, 2009	Sheet 57 of 63	

DDR3







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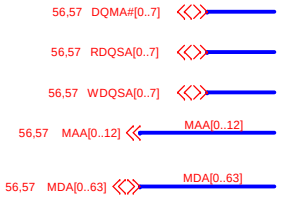
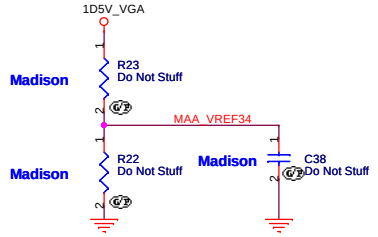
HYNIX: 72.51G63.C0U(VR.1GB0G.004)





JE70-DN

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Title: *VRAM(2/4)*

Size	Document Number	Rev
A3	JE70-DN	SB

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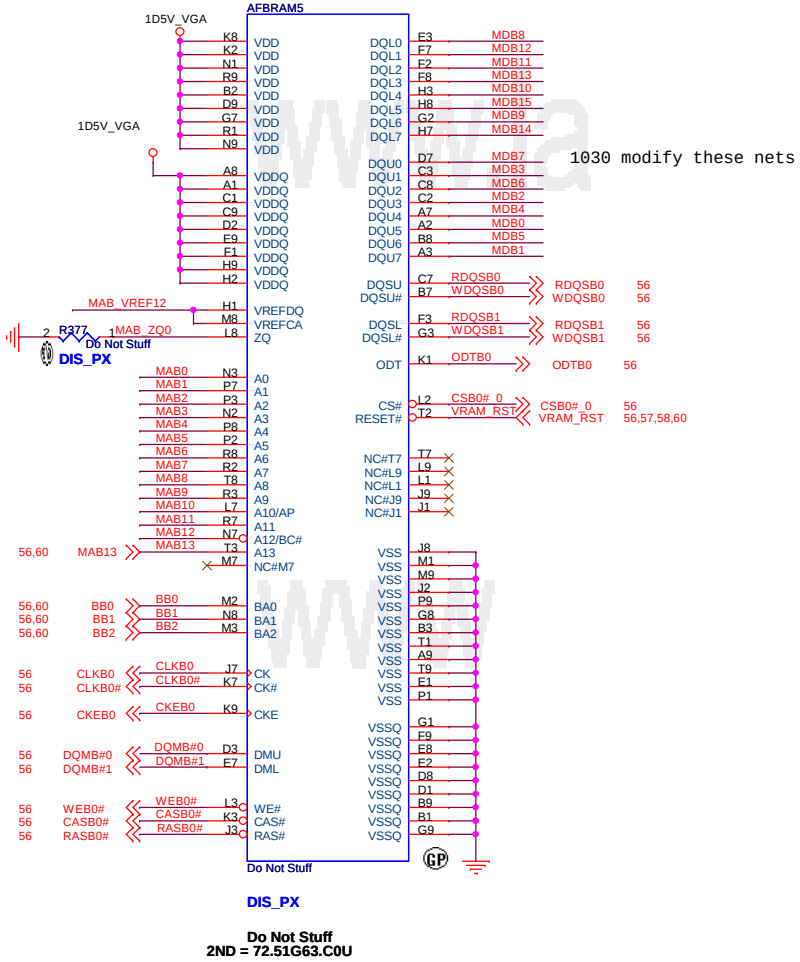
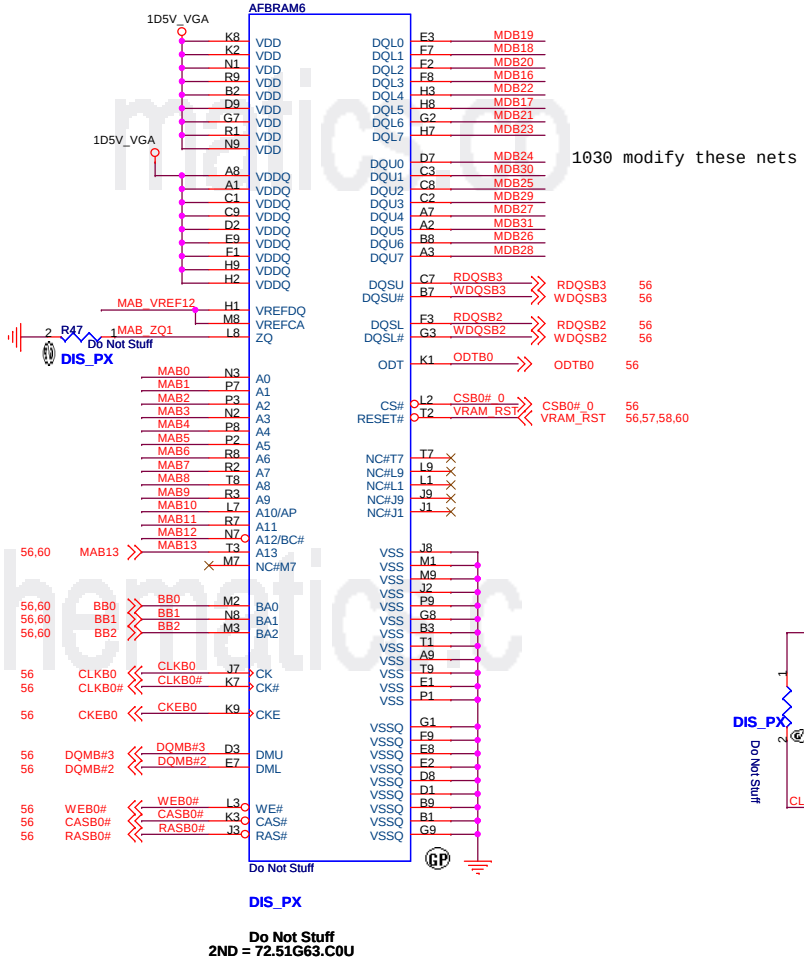
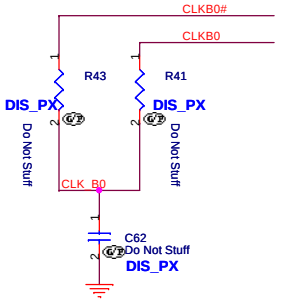
DDR3







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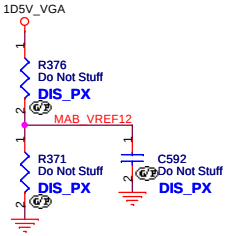
HYNIX: 72.51G63.C0U(VR.1GB0G.004)



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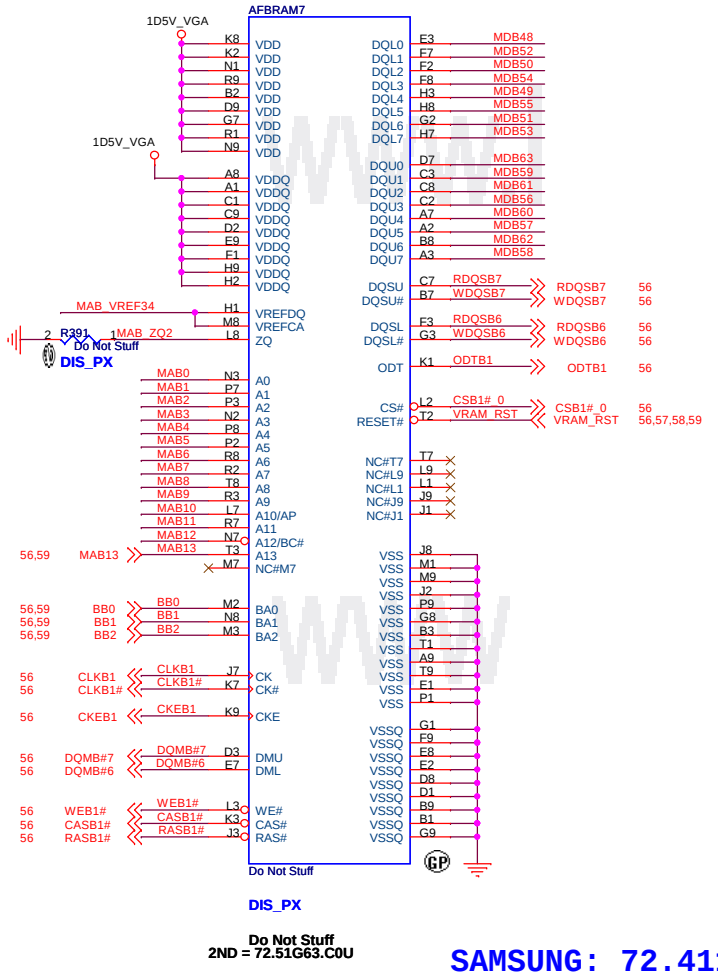
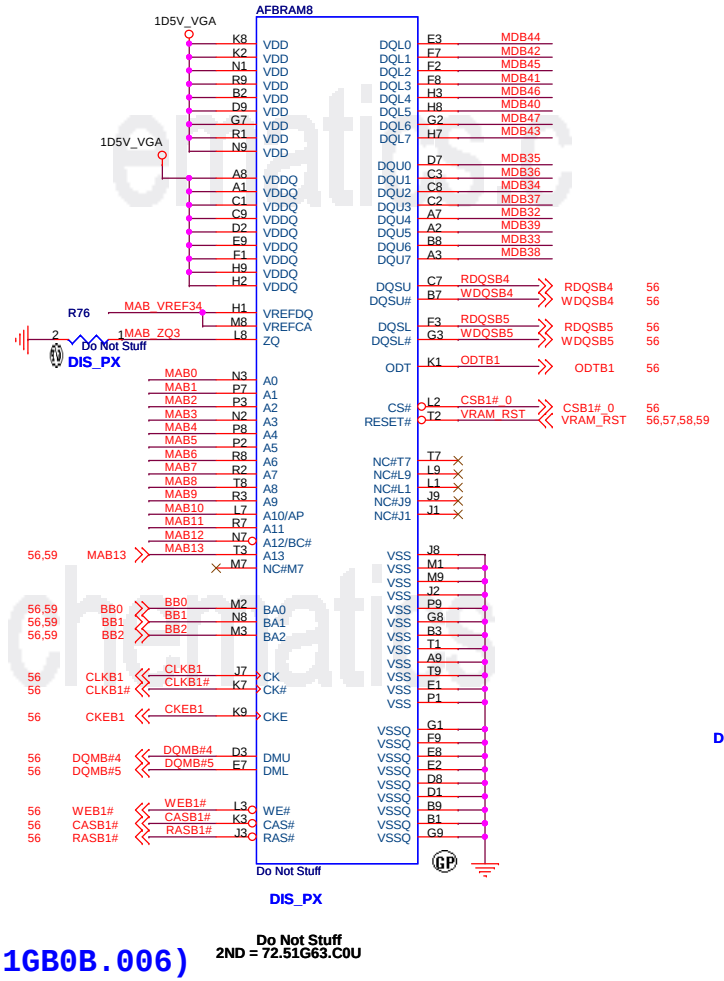
56,60 RDQSB[0..7]
56,60 WDQSB[0..7]
56,60 MAB[0..12] MAB[0..12]
56,60 MDB[0..63] MDB[0..63]

JE70-DN

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM(3/4)		
Size: A3	Document Number: JE70-DN	Rev: SB
Date: Wednesday, December 30, 2009	Sheet 59 of 63	

DDR3

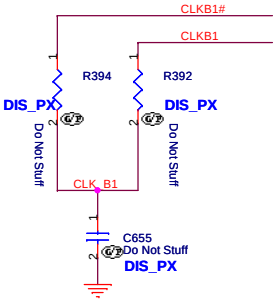


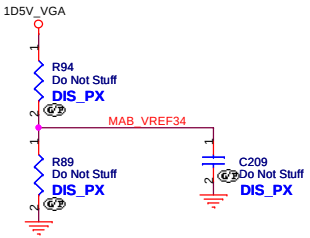


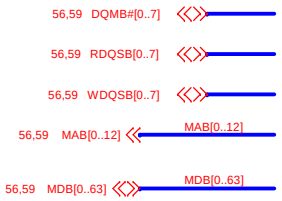
Do Not Stuff
2ND = 72.51G63.C0U

Do Not Stuff
2ND = 72.51G63.C0U

SAMSUNG: 72.41164.H0U(VR.1GB0B.006)
HYNIX: 72.51G63.C0U(VR.1GB0G.004)







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Taipei Hsien 221, Taiwan, R.O.C.

Title: *VRAM(4/4)*

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A3	JE70-DN	SB

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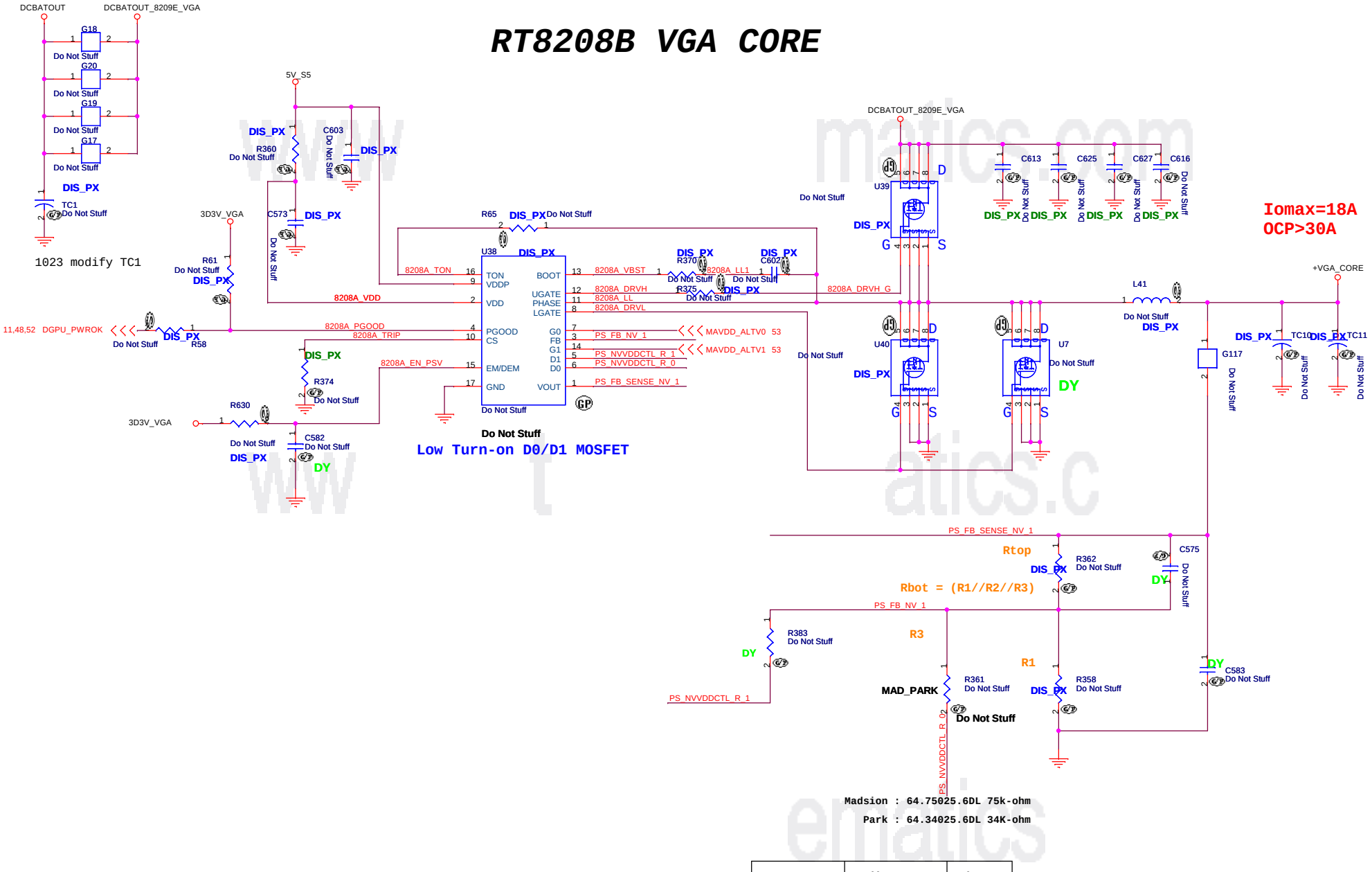
RT8208B VGA CORE



MAVDD_ALTV0	Madison Pro	Park XT
0	1.00V	1.12V
1	0.90V	0.90V

JE70-DN

Wistron Corporation
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Title: RT8209E_VGA_CORE

Size: A3 | Document Number: JE70-DN | Rev: SB

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1020

Page8: modify these nets for PCIE ports
Page11:add these nets(INT_VGA_EN#,EDP_EN)
Page11:add the net(PX_EN#) and R861
Page11:delete D41,R437,R435
Page12:modify these nets for USB ports
Page14:modify L45,L48,L52,L57,L58,L60
Page18:delete RN95,R423 and add Q73~Q76,R862~R864,D45
Page19:delete CCD1 conn and modify these nets for CCD
Page19:add R865,R866,U100
Page20:add Q77,R867
Page24:add modify these nets for BT
Page25:add modify these nets for USB board
Page26:modify these nets for PCIE port(LAN)
Page26:delete the net(LOW_PWR)
Page33:modify these nets for PCIE ports(MINI1,MINI2
Page33:modify these part's names
Page33:modify these nets for USB port(MINI2)
Page40:1020 modify PWR_LED1,CHARGER_LED1
Page51:add screw holes

1021

Page5:modify these nets
Page6:delete HDT1 conn and add TP246~255
Page16:modify these nets of ADM1
Page16:add R880~883
Page17:modify these nets of ADM2 and ADM3
Page17:add R884~R891
Page18:add RN114~117
Page23:modify ODD1
Page25:modify the net(COVER_SW#_1)
Page30:modify LOUT1,AMIC1 and MICIN1
Page33:modify AMINI1 and MINI2
Page36:modify these nets and add R873~878
Page38:modify these devices(ATPCN1,SW_R,SW_L)
Page40:modify PWR_LED1,CHARGER_LED1
Page49:add D46
Page50:modify DCIN1, BAT1 and add R879

1021

Page26:modify U6(LAN IC)

1023

Page12:delete R538,R539 and add RN118
Page12:delete R442,R443,R445 and add RN119
Page12:delete R570~R572 and add RN120
Page12:delete C368~C371,C446,C449,C686,C687
Page18:swap these nets
Page21:add R892~R900,Q78
Page25:delete TC29,TC24,EC79,EC83
Page25:modify the net of USBCN1 pin32
Page36:delete R258 and RN89,RN122
Page36:delete R382 and add U101
Page36:delete R892,R483,R497,R478 and add RN123
Page36:delete R410,R416 and add RN121,R892
Page37:add R901,R902
Page40:modify the pin5 define of PWR_CN1 and Q11
Page43:add TC53,TC54,U44
Page61:modify TC52, R295 and add R903,Q79

1026

Page3: add R904 and modify C509,R232,R235
Page6: add R913,RN124
Page6: modify RN42,RN84,R612,R611,R364
Page17:modify these nets
Page19:modify R588
Page21:modify U73 and delete R504
Page22:modify SATA1
Page35:delete R311 and modify FAN1
Page36:modify RN121
Page36:modify AKB1
Page37:modify RN94 and the net(SPI_WP#)
Page43:add R097~R911,D47,Q80
Page53:add R905,R906

1027

Page10:delete C651,R320,R316
Page11:modify C543,C306,C424,C433
Page11:delete R148
Page12:modify the net(PM_RSMRST#)
Page43:modify the net(PM_RSMRST#)

1028

Page3:add the net(LAN_CLKREQ#)to RN70
Page4:modify C704~C706
Page4:modify R401
Page9:delete R576,R578
Page10:modify C62,C91
Page11:delete R207,C337,D5,R208
Page11:delete the net(PCI_REQ#6)
Page12:delete RN120 and add R570
Page13:modify the net(SATA_LED#)
Page14:add C1198,C1199 and modify C815,C811
Page16:add R934,R935
Page18:add U102,R915~R919
Page18:modify R432,U3,U8
Page19:add U103,R920~R922 and delete D35
Page20:add R936,R937 and modify R325,R323,R354
Page21:delete RN8,RN13,RN15,RN19
Page21:modify C819~C821,C823,C824,C826~C828
Page25:add L82,R924,R925
Page29:modify R489
Page30:modify R622,R619 and add RN125
Page36:delete R384 and modify the net(KBC_BL_ON_IN)
Page36:add R926
Page43:delete R583,D33,U74,R340,Q34,R584
Page43:add R930~R933,Q84,Q85,C1197
Page43:add R927~R929,Q8~Q83
Page43:delete R591~R595
Page48:modify these nets(DGPU_PWROK,9025_POK)

1029

Page6:delete R364,R612 and add RN127,R946
Page16:delete C331,C338
Page17:delete C348,C340,C350,C342
Page18:modify these nets
Page19:add EC99,EC100
Page24:add EC101,EC102
Page25:add L82,R924,R925,R939,EC103
Page35:delete D17,D18,U39,U43,R298,R322,R330,R338,R337,C646,C656
Page35:delete U38,R321,R308,R309,R314,C645
Page36:add R945,RN126
Page43:delete U44,R342,C675
Page47:modify the net
Page48:modify R582 and add R938
Page50:add D48
Page53:add R940~R943
Page61:add R944,Q86

1030

Page3:modify these nets
Page8:modify these nets
Page11:modify the net
Page12:add R949
Page14:delete C760,C721,C805,C800,C769,L64 and add R948
Page18:modify these nets
Page30:add R950~R953 and modify EC24,EC51
Page57:swap these nets
Page58:swap these nets
Page59:swap these nets
Page60:swap these nets

1102

Page3:swap these nets
Page6:swap these nets
Page12:swap these nets
Page13:swap these nets
Page18:swap these nets
Page25:modify USBCN1
Page30:modify these names of these nets

1103

Page3:modify X5,C508,C509
Page11:modify R164
Page14:modify L51,L59
Page21:modify these names of nets
Page21:add RN8,RN13,RN15,RN19
Page36:add the net(A_MIC_SUPPORT#)

1104

Page6:delete TP246~255 and add HDT1
Page9:modify the value of RN11
Page24:add AFTP(TP256~TP258)
Page24:add AFTP(TP259~TP263)
Page25:add AFTP(TP264~TP280)
Page35:add AFTP(TP281,TP282)
Page36:add AFTP(TP283~TP307)
Page38:add AFTP(TP308~TP312)
Page40:add AFTP(TP313~TP319)
Page56:modify these values of R724,R725

1105

Page3:delete R191~R194,R198~R200,R204~R206
Page3:delete R214,R213,R187~R190,R220,R222
Page3:add RN128~RN136
Page3:modify R215,R197,R238,R229
Page6:delete R104,R105,R108,R110
Page6:add RN137,RN138,R954
Page6:modify R366
Page6:modify Q8,R81,R375,C205
Page8:delete TP16,TP17,TP20,TP21
Page9:add R955,R956 and modify R29
Page11:delete R144,R141,R137,R138
Page12:add the net(SUS_STAT#) and R957
Page12:modify these nets
Page21:swap these nets
Page28:modify C713,R634 and delete R626
Page33:modify these nets
Page33:modify R879

1106

Page3:modify these values of R169,R170
Page12:add R957,R958
Page12:add these nets(USB_OC#0,USB_OC#2,USB_OC#3)
Page16:modify R880~R883,ADM1
Page17:modify R888,R890,ADM2
Page21:add R959
Page35:modify FAN1
Page35:modify PWR_CN1
Page35:modify ATPCN1
Page36:swap these nets(KBRCIN#,KA20GATE)
Page37:swap RN94
Page44:swap RN45
Page51:add EC104~EC112 for EMI demand

1107

Page3:swap RN129,RN130,RN132
Page6:swap RN137
Page51:add EC104~EC112 for EMI demand

1109

Page45:modify the value of R448 to 64.15035.6DL for Power team demand
Page45:modify R462,R470 for Power team demand
Page46:modify L25 for Power team demand
Page48:modify C1032,C1194

1110

Page5:swap RN48
Page7:add C1200~C1207
Page11:add R960,R961
Page25:modify USB1
Page43:add TC55,TC56
Page52:add R962

1111

Page11:add R965
Page21:modify HDMI1
Page28:add R626
Page33:delete C550,C549 and add R963
Page36:delete RN121 and add R964
Page45:modify TC39,TC40
Page48:add R966,Q87,C1208,R967,R968,Q88

1112

Page13:modify the net
Page48:delete R968,Q88
Page48:modify R819,R820,R966
Page48:modify the net

1113

Page3:delete R170,EC50
Page25:delete R939,TP272,EC103
Page46:modify TC43
Page48:add R969
Page53:add R968
Page53:delete TP103,TP122,TP160,TP178
Page53:delete these TP(TP157,TP145...)
Page54:delete TP3~TP9

1117(Rename)

Page18:swap these nets
Page22:delete D29~D31,D33
Page36:modify RN31
Page61:delete G24~G29
Page61:modify the net

1118

Page14:add R620 and modify R184
Page15:modify R412,R411
Page36:swap AKB1 pin1~pin26

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Title: HISTORY(1/2)

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1120

Page19: modify these nets
Page48: modify the net(9025_EN)

1124

Page38: modify ATPCN1

1126

Page25: modify these nets
Page36: add TP174

ENG UMA

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Title: *HISTORY(2/2)*		
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