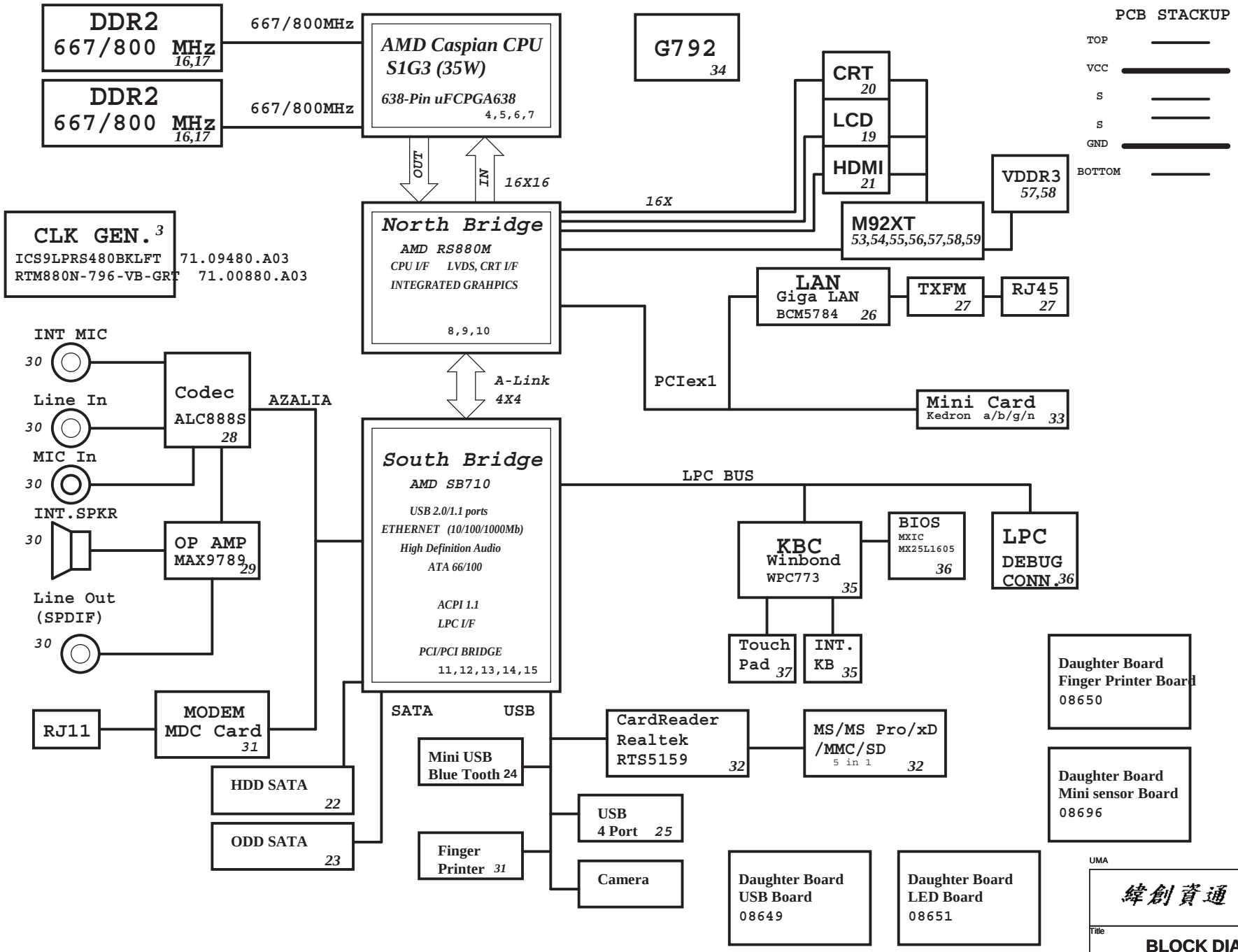
JV71-TR Block Diagram

Project code: 91.4FP01.001
PCB P/N : 48.4FP02.0SB
REVISION : 09243-SB



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC RT8205A 46

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47

INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC RT8209B 48

INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)

RT9025 49

5V_S5	1D1V_M92

RT9161 49

3D3V_S0	2D5V_S0 (200mA)

G957 49

3D3V_S0	1D5V_S0 (1A)

G9161 49

3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 45

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

UMA

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	JV71-TR	SB

Date: Monday, July 06, 2009 Sheet 1 of 61

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB/PCIE Routing**

Size	Document Number	Rev
A3	JV71-TR	SA

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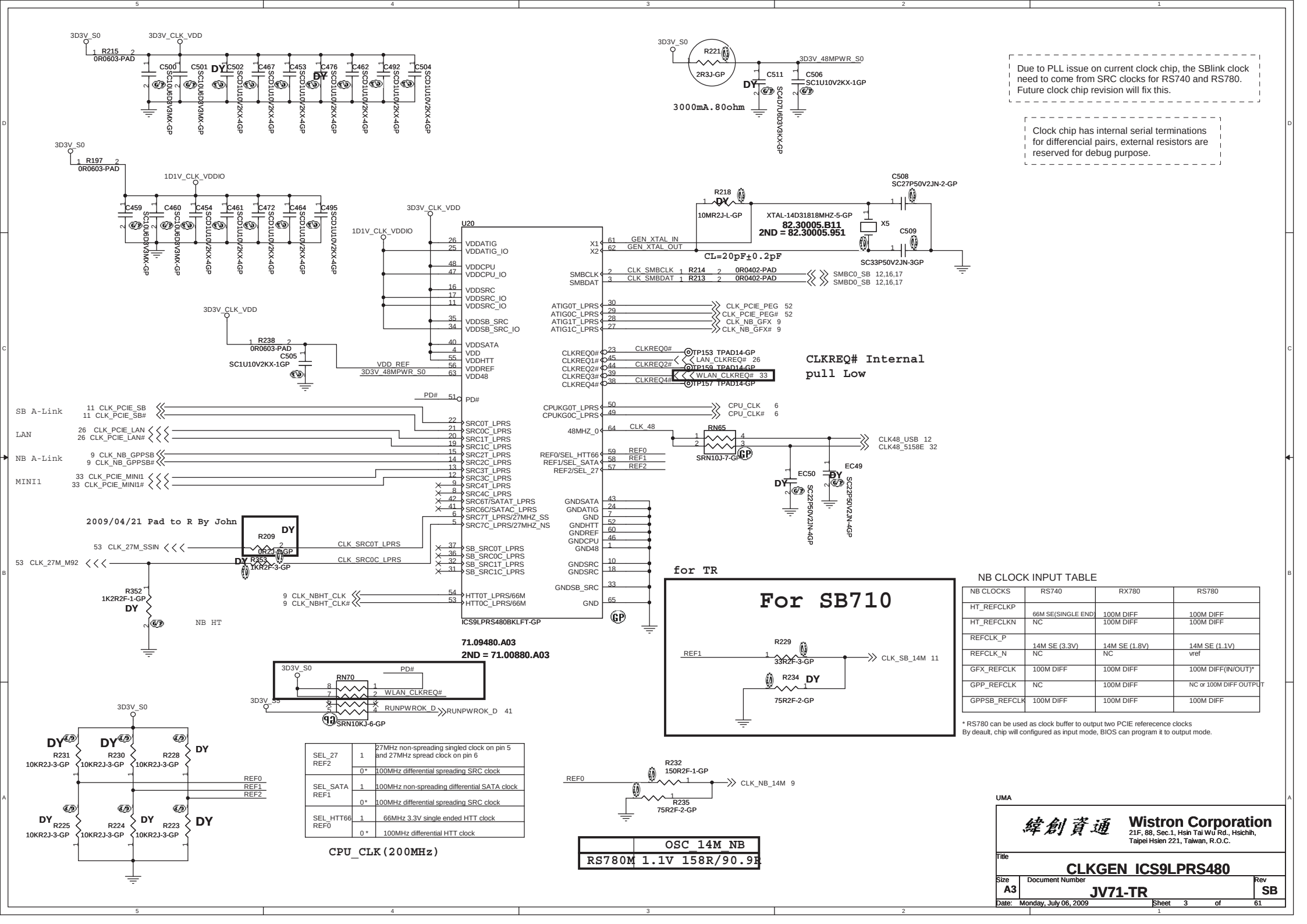
3D3V_S0
3D3V_CLK_VDD
R215 0R0603-PAD
C500 SC1U06D3V3MX-GP
C501 SC1U06D3V3MX-GP
C502 SC1U10V2KX-4GP
C467 SC1U10V2KX-4GP
C453 SC1U10V2KX-4GP
C476 SC1U10V2KX-4GP
C462 SC1U10V2KX-4GP
C492 SC1U10V2KX-4GP
C504 SC1U10V2KX-4GP
DY
R221 2R3J-GP
C511 SC4D7U6D3V3KX-GP
3D3V_48MPWR_S0
C506 SC1U10V2KX-1GP
3000mA.80ohm
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
R197 0R0603-PAD
1D1V_CLK_VDDIO
C459 SC1U06D3V3MX-GP
C460 SC1U06D3V3MX-GP
C454 SC1U10V2KX-4GP
C461 SC1U10V2KX-4GP
C472 SC1U10V2KX-4GP
C464 SC1U10V2KX-4GP
C495 SC1U10V2KX-4GP
U20
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDD
VDDHTT
VDDREF
VDD48
PD#
SRC0T_LPRS
SRC0C_LPRS
SRC1T_LPRS
SRC1C_LPRS
SRC2T_LPRS
SRC2C_LPRS
SRC3T_LPRS
SRC3C_LPRS
SRC4T_LPRS
SRC4C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
SRC7T_LPRS/27MHZ_SS
SRC7C_LPRS/27MHZ_NS
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
HTT0T_LPRS/66M
HTT0C_LPRS/66M
GNDSATA
GNDATIG
GND
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSRC
GNDSB_SRC
GND
ICS9LPRS480BKLFT-GP
X1
X2
GEN_XTAL_IN
GEN_XTAL_OUT
R218 10MR2J-L-GP
XTAL-14D31818MHZ-5-GP
82.30005.B11
2ND = 82.30005.951
X5
C508 SC27P50V2JN-2-GP
C509 SC33P50V2JN-3GP
CL=20pF±0.2pF
SMBCLK
SMBDAT
CLK_SMBCLK
CLK_SMBDAT
R214 0R0402-PAD
R213 0R0402-PAD
SMBC0_SB 12,16,17
SMBD0_SB 12,16,17
ATIG0T_LPRS
ATIG0C_LPRS
ATIG1T_LPRS
ATIG1C_LPRS
CLK_PCIE_PEG 52
CLK_PCIE_PEG# 52
CLK_NB_GFX 9
CLK_NB_GFX# 9
R238 0R0603-PAD
C505 SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
TP153 TPAD14-GP
TP159 TPAD14-GP
TP157 TPAD14-GP
LAN_CLKREQ# 26
WLAN_CLKREQ# 33
CLKREQ# Internal pull Low
PD#
SB A-Link
LAN
NB A-Link
MINI1
11 CLK_PCIE_SB
11 CLK_PCIE_SB#
26 CLK_PCIE_LAN
26 CLK_PCIE_LAN#
9 CLK_NB_GPPSB
9 CLK_NB_GPPSB#
33 CLK_PCIE_MINI1
33 CLK_PCIE_MINI1#
CPUKG0T_LPRS
CPUKG0C_LPRS
CPU_CLK 6
CPU_CLK# 6
48MHZ_0
CLK_48
RN65 SRN10J-7-GP
CLK48_USB 12
CLK48_5158E 32
REF0/SEL_HTT66
REF1/SEL_SATA
REF2/SEL_27
REF0
REF1
REF2
EC50 SC22P50V2JN-4GP
EC49 SC22P50V2JN-4GP
2009/04/21 Pad to R By John
R209 0R2J-2-GP
R353 1KR2F-3-GP
53 CLK_27M_SSIN
53 CLK_27M_M92
CLK_SRC0T_LPRS
CLK_SRC0C_LPRS
R352 1K2R2F-1-GP
NB HT
9 CLK_NBHT_CLK
9 CLK_NBHT_CLK#
71.09480.A03
2ND = 71.00880.A03
for TR
For SB710
R229 33R2F-3-GP
R234 75R2F-2-GP
REF1
CLK_SB_14M 11
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
RN70 SRN10KJ-6-GP
PD#
WLAN_CLKREQ#
RUNPWROK_D
RUNPWROK_D 41
R231 10KR2J-3-GP
R230 10KR2J-3-GP
R228 10KR2J-3-GP
R225 10KR2J-3-GP
R224 10KR2J-3-GP
R223 10KR2J-3-GP
REF0
REF1
REF2
SEL_27 REF2
1 27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
0* 100MHz differential spreading SRC clock
SEL_SATA REF1
1 100MHz non-spreading differential SATA clock
0* 100MHz differential spreading SRC clock
SEL_HTT66 REF0
1 66MHz 3.3V single ended HTT clock
0* 100MHz differential HTT clock
CPU_CLK(200MHz)
R232 150R2F-1-GP
R235 75R2F-2-GP
REF0
CLK_NB_14M 9
OSC_14M_NB
RS780M 1.1V 158R/90.9R
UMA
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
CLKGEN_ICS9LPRS480
Size A3
Document Number JV71-TR
Rev SB
Date: Monday, July 06, 2009
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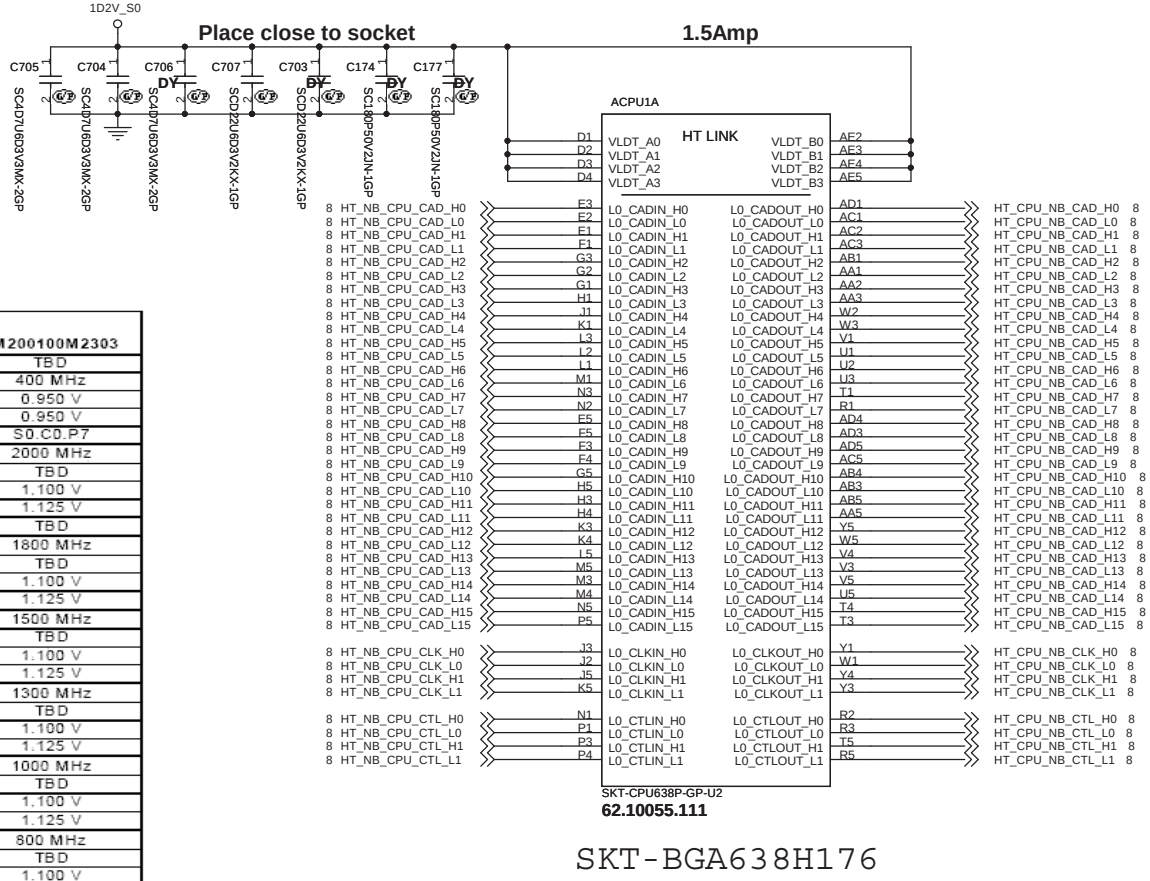

SKT-BGA638H176

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

UMA

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Title: CPU HT LINK I/F (1/4)

Size: A3 | Document Number: JV71-TR | Rev: SA

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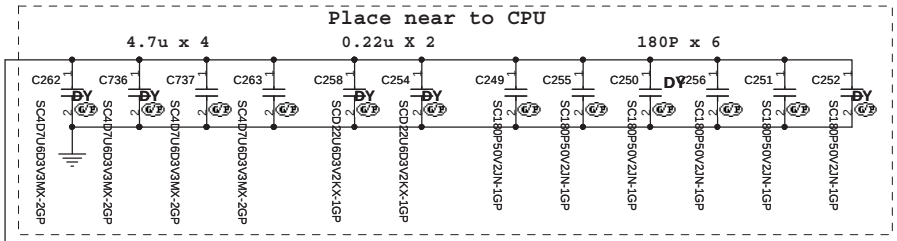
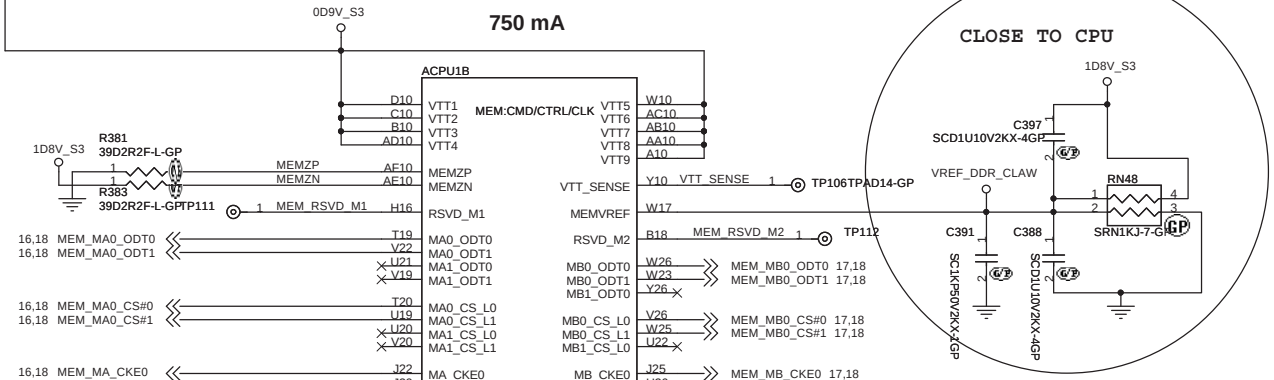


750 mA

CLOSE TO CPU



ACPU1B

MEM:CMD/CTRL/CLK

	D10	VTT1	VTT5	W10	
	C10	VTT2	VTT6	AC10	
	B10	VTT3	VTT7	AB10	
	AD10	VTT4	VTT8	AA10	
			VTT9	A10	
	AE10	MEMZP			
	AE10	MEMZN	VTT_SENSE	Y10	VTT_SENSE
	H16	RSVD_M1	MEMVREF	W17	
			RSVD_M2	B18	MEM_RSVD_M2
16,18 MEM_MA0_ODT0	T19	MA0_ODT0			
16,18 MEM_MA0_ODT1	V22	MA0_ODT1			
	U21	MA1_ODT0	MB0_ODT0	W26	MEM_MB0_ODT0 17,18
	V19	MA1_ODT1	MB0_ODT1	W23	MEM_MB0_ODT1 17,18
			MB1_ODT0	Y26	
16,18 MEM_MA0_CS#0	T20	MA0_CS_L0			
16,18 MEM_MA0_CS#1	U19	MA0_CS_L1	MB0_CS_L0	V26	MEM_MB0_CS#0 17,18
	U20	MA1_CS_L0	MB0_CS_L1	W25	MEM_MB0_CS#1 17,18
	V20	MA1_CS_L1	MB1_CS_L0	U22	
16,18 MEM_MA_CKE0	J22	MA_CKE0	MB_CKE0	J25	MEM_MB_CKE0 17,18
16,18 MEM_MA_CKE1	J20	MA_CKE1	MB_CKE1	H26	MEM_MB_CKE1 17,18
	N19	MA_CLK_H5	MB_CLK_H5	P22	
	N20	MA_CLK_L5	MB_CLK_L5	R22	
16 MEM_MA_CLK0_P	E16	MA_CLK_H1	MB_CLK_H1	A17	MEM_MB_CLK0_P 17
16 MEM_MA_CLK0_N	F16	MA_CLK_L1	MB_CLK_L1	A18	MEM_MB_CLK0_N 17
16 MEM_MA_CLK1_P	Y16	MA_CLK_H7	MB_CLK_H7	AF18	MEM_MB_CLK1_P 17
16 MEM_MA_CLK1_N	AA16	MA_CLK_L7	MB_CLK_L7	AE17	MEM_MB_CLK1_N 17
	P19	MA_CLK_H4	MB_CLK_H4	R26	
	P20	MA_CLK_L4	MB_CLK_L4	R25	
16,18 MEM_MA_ADD0	N21	MA_ADD0	MB_ADD0	P24	MEM_MB_ADD0 17,18
16,18 MEM_MA_ADD1	M20	MA_ADD1	MB_ADD1	N24	MEM_MB_ADD1 17,18
16,18 MEM_MA_ADD2	N22	MA_ADD2	MB_ADD2	P26	MEM_MB_ADD2 17,18
16,18 MEM_MA_ADD3	M19	MA_ADD3	MB_ADD3	N23	MEM_MB_ADD3 17,18
16,18 MEM_MA_ADD4	M22	MA_ADD4	MB_ADD4	N26	MEM_MB_ADD4 17,18
16,18 MEM_MA_ADD5	L20	MA_ADD5	MB_ADD5	L23	MEM_MB_ADD5 17,18
16,18 MEM_MA_ADD6	M24	MA_ADD6	MB_ADD6	N25	MEM_MB_ADD6 17,18
16,18 MEM_MA_ADD7	L21	MA_ADD7	MB_ADD7	L24	MEM_MB_ADD7 17,18
16,18 MEM_MA_ADD8	L19	MA_ADD8	MB_ADD8	M26	MEM_MB_ADD8 17,18
16,18 MEM_MA_ADD9	K22	MA_ADD9	MB_ADD9	K26	MEM_MB_ADD9 17,18
16,18 MEM_MA_ADD10	R21	MA_ADD10	MB_ADD10	T26	MEM_MB_ADD10 17,18
16,18 MEM_MA_ADD11	L22	MA_ADD11	MB_ADD11	L26	MEM_MB_ADD11 17,18
16,18 MEM_MA_ADD12	K20	MA_ADD12	MB_ADD12	L25	MEM_MB_ADD12 17,18
16,18 MEM_MA_ADD13	V24	MA_ADD13	MB_ADD13	W24	MEM_MB_ADD13 17,18
16,18 MEM_MA_ADD14	K24	MA_ADD14	MB_ADD14	J23	MEM_MB_ADD14 17,18
16,18 MEM_MA_ADD15	K19	MA_ADD15	MB_ADD15	J24	MEM_MB_ADD15 17,18
16,18 MEM_MA_BANK0	R20	MA_BANK0	MB_BANK0	R24	MEM_MB_BANK0 17,18
16,18 MEM_MA_BANK1	R23	MA_BANK1	MB_BANK1	U26	MEM_MB_BANK1 17,18
16,18 MEM_MA_BANK2	J21	MA_BANK2	MB_BANK2	J26	MEM_MB_BANK2 17,18
16,18 MEM_MA_RAS#	R19	MA_RAS_L	MB_RAS_L	U25	MEM_MB_RAS# 17,18
16,18 MEM_MA_CAS#	T22	MA_CAS_L	MB_CAS_L	U24	MEM_MB_CAS# 17,18
16,18 MEM_MA_WE#	T24	MA_WE_L	MB_WE_L	U23	MEM_MB_WE# 17,18

SKT-CPU638P-GP-U2

62.10055.111

ACPU1C

MEM:DATA

16 MEM_MA_DATA0	G12	MA_DATA0	MB_DATA0	C11	MEM_MB_DATA0 17
16 MEM_MA_DATA1	F12	MA_DATA1	MB_DATA1	A11	MEM_MB_DATA1 17
16 MEM_MA_DATA2	H14	MA_DATA2	MB_DATA2	A14	MEM_MB_DATA2 17
16 MEM_MA_DATA3	G14	MA_DATA3	MB_DATA3	B14	MEM_MB_DATA3 17
16 MEM_MA_DATA4	H11	MA_DATA4	MB_DATA4	G11	MEM_MB_DATA4 17
16 MEM_MA_DATA5	H12	MA_DATA5	MB_DATA5	E11	MEM_MB_DATA5 17
16 MEM_MA_DATA6	C13	MA_DATA6	MB_DATA6	D12	MEM_MB_DATA6 17
16 MEM_MA_DATA7	F13	MA_DATA7	MB_DATA7	A13	MEM_MB_DATA7 17
16 MEM_MA_DATA8	H15	MA_DATA8	MB_DATA8	A15	MEM_MB_DATA8 17
16 MEM_MA_DATA9	F15	MA_DATA9	MB_DATA9	A16	MEM_MB_DATA9 17
16 MEM_MA_DATA10	E17	MA_DATA10	MB_DATA10	A19	MEM_MB_DATA10 17
16 MEM_MA_DATA11	H17	MA_DATA11	MB_DATA11	A20	MEM_MB_DATA11 17
16 MEM_MA_DATA12	E14	MA_DATA12	MB_DATA12	C14	MEM_MB_DATA12 17
16 MEM_MA_DATA13	F14	MA_DATA13	MB_DATA13	D14	MEM_MB_DATA13 17
16 MEM_MA_DATA14	C17	MA_DATA14	MB_DATA14	C18	MEM_MB_DATA14 17
16 MEM_MA_DATA15	G17	MA_DATA15	MB_DATA15	D18	MEM_MB_DATA15 17
16 MEM_MA_DATA16	G18	MA_DATA16	MB_DATA16	D20	MEM_MB_DATA16 17
16 MEM_MA_DATA17	C19	MA_DATA17	MB_DATA17	A21	MEM_MB_DATA17 17
16 MEM_MA_DATA18	D22	MA_DATA18	MB_DATA18	D24	MEM_MB_DATA18 17
16 MEM_MA_DATA19	E20	MA_DATA19	MB_DATA19	C25	MEM_MB_DATA19 17
16 MEM_MA_DATA20	E18	MA_DATA20	MB_DATA20	B20	MEM_MB_DATA20 17
16 MEM_MA_DATA21	F18	MA_DATA21	MB_DATA21	C20	MEM_MB_DATA21 17
16 MEM_MA_DATA22	B22	MA_DATA22	MB_DATA22	B24	MEM_MB_DATA22 17
16 MEM_MA_DATA23	C23	MA_DATA23	MB_DATA23	C24	MEM_MB_DATA23 17
16 MEM_MA_DATA24	F20	MA_DATA24	MB_DATA24	E23	MEM_MB_DATA24 17
16 MEM_MA_DATA25	F22	MA_DATA25	MB_DATA25	E24	MEM_MB_DATA25 17
16 MEM_MA_DATA26	H24	MA_DATA26	MB_DATA26	G25	MEM_MB_DATA26 17
16 MEM_MA_DATA27	J19	MA_DATA27	MB_DATA27	G26	MEM_MB_DATA27 17
16 MEM_MA_DATA28	E21	MA_DATA28	MB_DATA28	C26	MEM_MB_DATA28 17
16 MEM_MA_DATA29	F22	MA_DATA29	MB_DATA29	D26	MEM_MB_DATA29 17
16 MEM_MA_DATA30	H20	MA_DATA30	MB_DATA30	G23	MEM_MB_DATA30 17
16 MEM_MA_DATA31	H22	MA_DATA31	MB_DATA31	G24	MEM_MB_DATA31 17
16 MEM_MA_DATA32	Y24	MA_DATA32	MB_DATA32	AA24	MEM_MB_DATA32 17
16 MEM_MA_DATA33	AB24	MA_DATA33	MB_DATA33	AA23	MEM_MB_DATA33 17
16 MEM_MA_DATA34	AB22	MA_DATA34	MB_DATA34	AD24	MEM_MB_DATA34 17
16 MEM_MA_DATA35	AA21	MA_DATA35	MB_DATA35	AE24	MEM_MB_DATA35 17
16 MEM_MA_DATA36	W22	MA_DATA36	MB_DATA36	AA26	MEM_MB_DATA36 17
16 MEM_MA_DATA37	W21	MA_DATA37	MB_DATA37	AA25	MEM_MB_DATA37 17
16 MEM_MA_DATA38	Y22	MA_DATA38	MB_DATA38	AD26	MEM_MB_DATA38 17
16 MEM_MA_DATA39	AA22	MA_DATA39	MB_DATA39	AE25	MEM_MB_DATA39 17
16 MEM_MA_DATA40	Y20	MA_DATA40	MB_DATA40	AC22	MEM_MB_DATA40 17
16 MEM_MA_DATA41	AA20	MA_DATA41	MB_DATA41	AD22	MEM_MB_DATA41 17
16 MEM_MA_DATA42	AA18	MA_DATA42	MB_DATA42	AE20	MEM_MB_DATA42 17
16 MEM_MA_DATA43	AB18	MA_DATA43	MB_DATA43	AE20	MEM_MB_DATA43 17
16 MEM_MA_DATA44	AB21	MA_DATA44	MB_DATA44	AE24	MEM_MB_DATA44 17
16 MEM_MA_DATA45	AD21	MA_DATA45	MB_DATA45	AE23	MEM_MB_DATA45 17
16 MEM_MA_DATA46	AD19	MA_DATA46	MB_DATA46	AC20	MEM_MB_DATA46 17
16 MEM_MA_DATA47	Y18	MA_DATA47	MB_DATA47	AD20	MEM_MB_DATA47 17
16 MEM_MA_DATA48	AD17	MA_DATA48	MB_DATA48	AD18	MEM_MB_DATA48 17
16 MEM_MA_DATA49	W16	MA_DATA49	MB_DATA49	AE18	MEM_MB_DATA49 17
16 MEM_MA_DATA50	W14	MA_DATA50	MB_DATA50	AC14	MEM_MB_DATA50 17
16 MEM_MA_DATA51	Y14	MA_DATA51	MB_DATA51	AD14	MEM_MB_DATA51 17
16 MEM_MA_DATA52	Y17	MA_DATA52	MB_DATA52	AE19	MEM_MB_DATA52 17
16 MEM_MA_DATA53	AB17	MA_DATA53	MB_DATA53	AC18	MEM_MB_DATA53 17
16 MEM_MA_DATA54	AB15	MA_DATA54	MB_DATA54	AE16	MEM_MB_DATA54 17
16 MEM_MA_DATA55	AD15	MA_DATA55	MB_DATA55	AE15	MEM_MB_DATA55 17
16 MEM_MA_DATA56	AB13	MA_DATA56	MB_DATA56	AE13	MEM_MB_DATA56 17
16 MEM_MA_DATA57	AD13	MA_DATA57	MB_DATA57	AC12	MEM_MB_DATA57 17
16 MEM_MA_DATA58	Y12	MA_DATA58	MB_DATA58	AB11	MEM_MB_DATA58 17
16 MEM_MA_DATA59	W11	MA_DATA59	MB_DATA59	Y11	MEM_MB_DATA59 17
16 MEM_MA_DATA60	AB14	MA_DATA60	MB_DATA60	AE14	MEM_MB_DATA60 17
16 MEM_MA_DATA61	AA14	MA_DATA61	MB_DATA61	AE14	MEM_MB_DATA61 17
16 MEM_MA_DATA62	AB12	MA_DATA62	MB_DATA62	AE11	MEM_MB_DATA62 17
16 MEM_MA_DATA63	AA12	MA_DATA63	MB_DATA63	AD11	MEM_MB_DATA63 17
16 MEM_MA_DM0	E12	MA_DM0	MB_DM0	A12	MEM_MB_DM0 17
16 MEM_MA_DM1	C15	MA_DM1	MB_DM1	B16	MEM_MB_DM1 17
16 MEM_MA_DM2	E19	MA_DM2	MB_DM2	A22	MEM_MB_DM2 17
16 MEM_MA_DM3	F24	MA_DM3	MB_DM3	E25	MEM_MB_DM3 17
16 MEM_MA_DM4	AC24	MA_DM4	MB_DM4	AB26	MEM_MB_DM4 17
16 MEM_MA_DM5	Y19	MA_DM5	MB_DM5	AE22	MEM_MB_DM5 17
16 MEM_MA_DM6	AB16	MA_DM6	MB_DM6	AC16	MEM_MB_DM6 17
16 MEM_MA_DM7	Y13	MA_DM7	MB_DM7	AD12	MEM_MB_DM7 17
16 MEM_MA_DQS0_P	G13	MA_DQS_H0	MB_DQS_H0	C12	MEM_MB_DQS0_P 17
16 MEM_MA_DQS0_N	H13	MA_DQS_L0	MB_DQS_L0	B12	MEM_MB_DQS0_N 17
16 MEM_MA_DQS1_P	G16	MA_DQS_H1	MB_DQS_H1	D16	MEM_MB_DQS1_P 17
16 MEM_MA_DQS1_N	G15	MA_DQS_L1	MB_DQS_L1	C16	MEM_MB_DQS1_N 17
16 MEM_MA_DQS2_P	C22	MA_DQS_H2	MB_DQS_H2	A24	MEM_MB_DQS2_P 17
16 MEM_MA_DQS2_N	C21	MA_DQS_L2	MB_DQS_L2	A23	MEM_MB_DQS2_N 17
16 MEM_MA_DQS3_P	G22	MA_DQS_H3	MB_DQS_H3	F26	MEM_MB_DQS3_P 17
16 MEM_MA_DQS3_N	G21	MA_DQS_L3	MB_DQS_L3	E26	MEM_MB_DQS3_N 17
16 MEM_MA_DQS4_P	AD23	MA_DQS_H4	MB_DQS_H4	AC25	MEM_MB_DQS4_P 17
16 MEM_MA_DQS4_N	AC23	MA_DQS_L4	MB_DQS_L4	AC26	MEM_MB_DQS4_N 17
16 MEM_MA_DQS5_P	AB19	MA_DQS_H5	MB_DQS_H5	AF21	MEM_MB_DQS5_P 17
16 MEM_MA_DQS5_N	AB20	MA_DQS_L5	MB_DQS_L5	AE22	MEM_MB_DQS5_N 17
16 MEM_MA_DQS6_P	Y15	MA_DQS_H6	MB_DQS_H6	AE16	MEM_MB_DQS6_P 17
16 MEM_MA_DQS6_N	W15	MA_DQS_L6	MB_DQS_L6	AD16	MEM_MB_DQS6_N 17
16 MEM_MA_DQS7_P	W12	MA_DQS_H7	MB_DQS_H7	AE12	MEM_MB_DQS7_P 17
16 MEM_MA_DQS7_N	W13	MA_DQS_L7	MB_DQS_L7	AE12	MEM_MB_DQS7_N 17

SKT-CPU638P-GP-U2

62.10055.111

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_DDR_(2/4)**

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 5 of 61

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

for TR

for TR

Near CPU PIN

84.T3904.C11
2ND = 84.03904.L06

84.T3904.C11
2ND = 84.03904.L06

CPU exceeds to 125℃

SKT-CPU638P-GP-U2

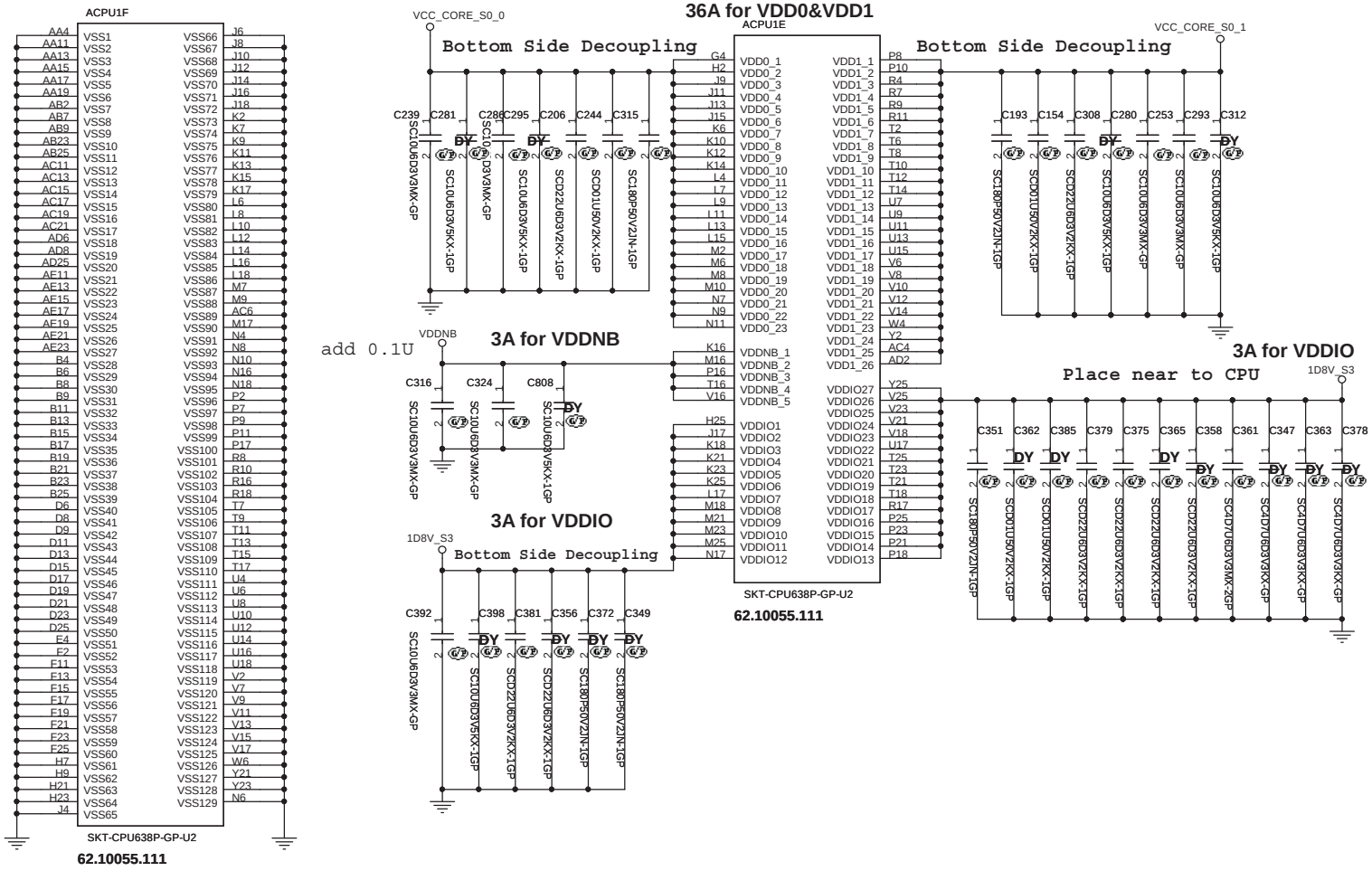
62.10055.111

HDT Connectors

SMC-CONN26A-FP

UMA

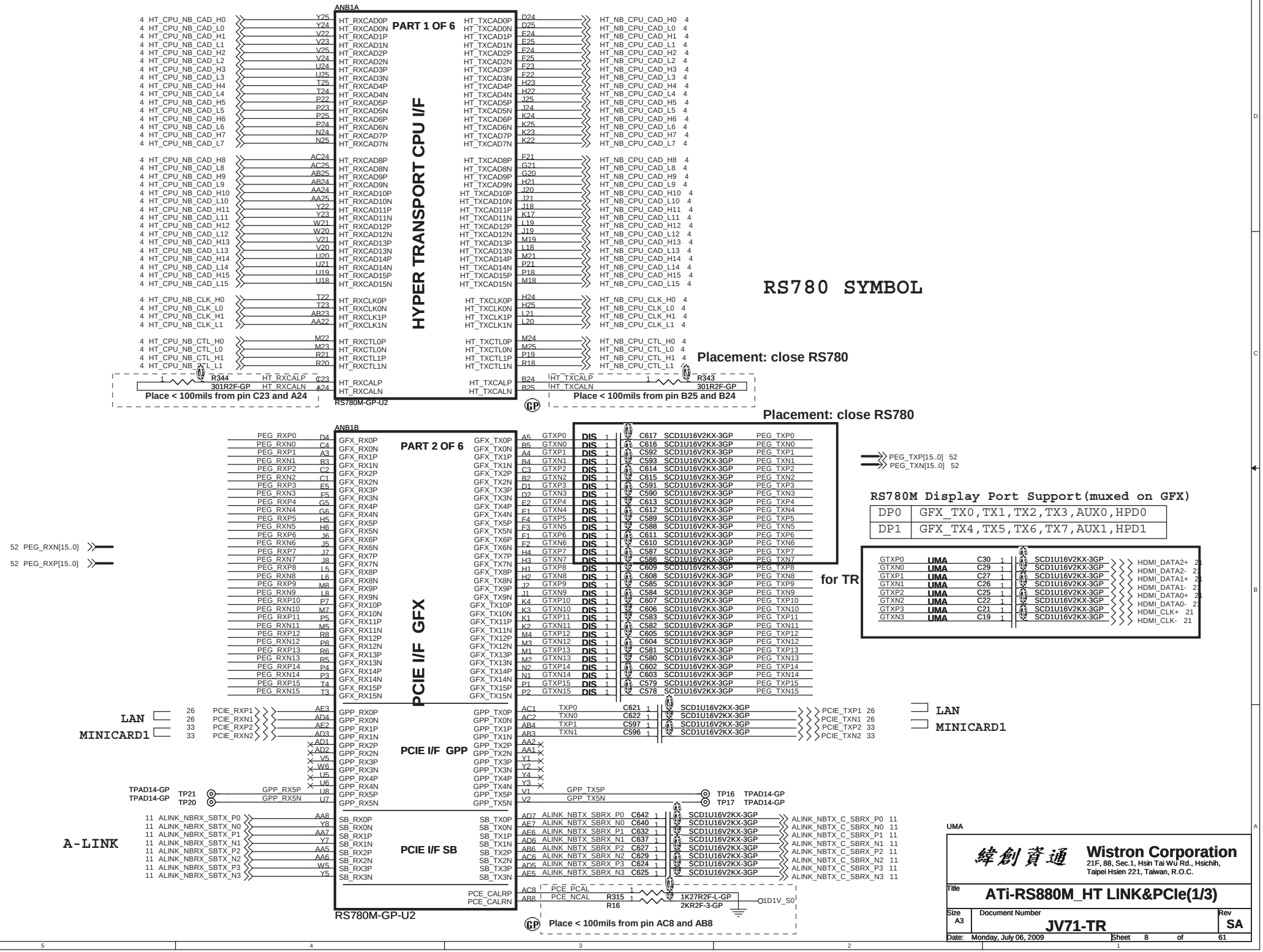
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU_Control&Debug_(3/4)		
Size: A3	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 6 of 61	



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_Power_(4/4)	
Size A3	Document Number JV71-TR	Rev SA
Date: Monday, July 06, 2009	Sheet 7 of 61	


ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
RS780 SYMBOL
Placement: close RS780
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
R344 301R2F-GP
R343 301R2F-GP
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
PEG_TXP[15..0] 52
PEG_TXN[15..0] 52
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
for TR
52 PEG_RXN[15..0]
52 PEG_RXP[15..0]
LAN
MINICARD1
A-LINK
TPAD14-GP
Place < 100mils from pin AC8 and AB8
1D1V_S0
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS880M_HT LINK&PCIe(1/3)
Size A3
Document Number JV71-TR
Rev SA
Date: Monday, July 06, 2009
Sheet 8 of 61

Reserve for EMI 0408

NB_PWRGD — DY — EC962 SC1KP50V2KX-1GP

STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

3D3V_S0 — L3 220ohm 100mA — SBK160808T-221Y-N-GP — 68.00119.111 — 3D3V_S0_AVDD — C70 SCD1U10V2KX-4GP — C71 SC1U10V2KX-1GP

3D3V_S0 — R563 3K3R2J-3-GP — R562 3K3R2J-3-GP — GMCH_VSYNC — GMCH_HSYNC

6 LDT_RST#_CPU — R21 0R2J-2-GP — DY
11,26,35 PLT_RST1# — R17 0R2J-2-GP — SYSREST# — C37 SC220P50V2KX-3GP

1D8V_S0 — R41 0R0603-PAD — 1D8V_S0_AVDDDI — C88 SC1U10V2KX-1GP — C89 SCD1U10V2KX-4GP — 68.00119.111

1D8V_S0 — 220ohm 200mA — R43 SBK160808T-221Y-N-GP — C80 SC1U10V2KX-1GP — C99 SCD1U10V2KX-4GP — 1D8V_S0_AVDDQ

TC2 ST100U6D3VBM-5GP — DY — 77.C1071.081

Close to NB ball

GMCH_BLUE — R36 150R2F-1-GP
GMCH_GREEN — R37 150R2F-1-GP
GMCH_RED — R38 140R2F-GP

2009/04/22 R609 Change to 1K By John

1D8V_S0 — for TR — R609 1KR2F-3-GP

6 LDT_STP#_CPU — R14 0R0402-PAD — NB_LDT_STOP#
6 ALLOW_LDTSTOP — R24 0R2J-2-GP — DY — NB_ALLOW_LDTSTOP

for TR

1D1V_S0 — L33 SBK160808T-221Y-N-GP — 1D1V_S0_PLLVDD — 220ohm 200mA — 68.00119.111 — C644 SC1U10V2KX-1GP — C643 SCD1U10V2KX-4GP DY

1D8V_S0 — 220ohm 200mA — L4 2R3J-GP — 2009/05/26 SB Change — C78 SC1U10V2KX-1GP — C77 SCD1U10V2KX-4GP DY — C82 SC47U6D3V5MX-1GP DY — TC1 ST100U6D3VBM-1GP

80.10715.L04
2ND = 77.C1071.081
3RD = 77.21071.09L

ENABLE External CLK GEN

1D1V_S0 — RN11 — SRN1KJ-7-GP

1D8V_S0 — L5 — 68.00119.111 — 220ohm 200mA — SBK160808T-221Y-N-GP — VDDA18HTPLL — C86 SC1U10V2KX-1GP DY — C97 SCD1U10V2KX-4GP

1D8V_S0 — L1 — 68.00119.111 — 220ohm 200mA — SBK160808T-221Y-N-GP — VDDA18PCIEPLL — C41 SC1U10V2KX-1GP DY — C42 SCD1U10V2KX-4GP

	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.1V	1.0V

3D3V_S0 — R19 2K2R2J-2-GP DY — STRP_DATA

ANB1C

RS780M-GP-U2

PART 3 OF 6

CRT/TVOUT
AVDD1 F12
AVDD2 F12
AVDDDI F14
AVSSDI G15
AVDDQ H15
AVSSQ H14
C_Pr E17
Y F17
COMP_Pb F15
20 GMCH_RED — RED G18
20 GMCH_GREEN — REDb G17 / GREEN E18
GREENb F18
20 GMCH_BLUE — BLUE E19
BLUEb F19
20 GMCH_HSYNC — DAC_HSYNC A11
20 GMCH_VSYNC — DAC_VSYNC B11
20 GMCH_DDCCLK — DAC_SCL F8
20 GMCH_DDCDATA — DAC_SDA E8
DAC_RSET G14 — R33 715R2F-GP

PLL PWR LVTM
PLLVDD A12
PLLVDD18 D14
PLLVSS B12
VDDA18HTPLL H17
VDDA18PCIEPLL1 D7
VDDA18PCIEPLL2 E7

SYSRESET# D8
POWERGOOD
LDTSTOP# A10
ALLOW_LDTSTOP C10 / C12
12,41 NB_PWRGD — NB_PWRGD
NB_LDT_STOP# — NB_LDT_STOP
11 NB_ALLOW_LDTSTOP — NB_ALLOW_LDTSTOP

CLOCKs PM
HT_REFCLKP C25
HT_REFCLKN C24
3 CLK_NBHT_CLK
3 CLK_NBHT_CLK#
REFCLK_P/OSCIN E11
REFCLK_N F11
3 CLK_NB_14M — NB_REFCLK_N
GFX_REFCLKP T2
GFX_REFCLKN T1
3 CLK_NB_GFX — CLK_NB_GFX
3 CLK_NB_GFX# — CLK_NB_GFX#
GPP_REFCLKP U1
GPP_REFCLKN U2
TPAD14-GP TP180 — CLK_NBGPP_CLK
TPAD14-GP TP181 — CLK_NBGPP_CLK#
GPPSB_REFCLKP V4
GPPSB_REFCLKN V3
3 CLK_NB_GPPSB
3 CLK_NB_GPPSB#

MIS.
I2C_CLK B9
I2C_DATA A9
DDC_CLK0/AUX0P
DDC_DATA0/AUX0N
DDC_CLK1/AUX1P
DDC_DATA1/AUX1N
TPAD14-GP TP188 — DDC_DATA0/AUX0N
TPAD14-GP TP239 — DDC_CLK0/AUX0P
DDC_DATA0/AUX0N
DDC_CLK0/AUX0P
19 CLK_DDC_EDID
19 DAT_DDC_EDID
21 GMCH_HDMI_CLK — GMCH_HDMI_CLK B7
21 GMCH_HDMI_DATA — GMCH_HDMI_DATA A7
STRP_DATA B10
RESERVED G11
AUX_CAL C8
RS780_AUX_CAL — R294 150R2F-1-GP

TXOUT_L0P A22 — GMCH_TXAOUT0+ 19
TXOUT_L0N B22 — GMCH_TXAOUT0- 19
TXOUT_L1P A21 — GMCH_TXAOUT1+ 19
TXOUT_L1N B21 — GMCH_TXAOUT1- 19
TXOUT_L2P B20 — GMCH_TXAOUT2+ 19
TXOUT_L2N A20 — GMCH_TXAOUT2- 19
TXOUT_L3P A19
TXOUT_L3N B19

TXOUT_U0P B18 — GMCH_TXBOUT0+ 19
TXOUT_U0N A18 — GMCH_TXBOUT0- 19
TXOUT_U1P A17 — GMCH_TXBOUT1+ 19
TXOUT_U1N B17 — GMCH_TXBOUT1- 19
TXOUT_U2P D20 — GMCH_TXBOUT2+ 19
TXOUT_U2N D21 — GMCH_TXBOUT2- 19
TXOUT_U3P D18
TXOUT_U3N D19

TXCLK_LP B16 — GMCH_TXACLK+ 19
TXCLK_LN A16 — GMCH_TXACLK- 19
TXCLK_UP D16 — GMCH_TXBCLK+ 19
TXCLK_UN D17 — GMCH_TXBCLK- 19

VDDLTP18 A13 — 1D8V_S0_VDDLP18 — L34 SBK160808T-221Y-N-GP — 68.00119.111
VSSLTP18 B13
VDDLT18_1 A15 — C649 SC1U10V2KX-1GP DY — C648 SCD1U10V2KX-4GP
VDDLT18_2 B15
VDDLT33_1 A14
VDDLT33_2 B14
1D8V_S0_VDDLT18 — L35 PBY201209T-221Y-N-GP — 68.00206.121
VSSLT1 C14
VSSLT2 D15
VSSLT3 C16
VSSLT4 C18
VSSLT5 C20
VSSLT6 F20
VSSLT7 C22
C652 — C653 SCD1U10V2KX-4GP DY
SC4D7U6D3V3MX-2GP

LVDS_DIGON E9 — GMCH_LCDVDD_ON 19
LVDS_BLON E7 — GMCH_BL_ON 35 — GMCH_BL_ON
LVDS_ENA_BL G12 — LVDS_ENA_BL — TP26 TPAD14-GP

RN10 — UMA — SRN4K7J-10-GP

TMDS_HPD D9
HPD D10 — NB_DVI_HPD — HDMI_DETECT# 21 — TP24 TPAD14-GP
SUS_STAT# D12 — SUS_STAT# — R29 10KR2J-3-GP — 3D3V_S0
THERMALDIODE_P AE8 — RS780_DXP3_1 — TP23 TPAD14-GP
THERMALDIODE_N AD8 — RS780_DXN3_1 — TP22 TPAD14-GP
TESTMODE D13 — TESTMODE_NB — R347 1K8R2F-GP

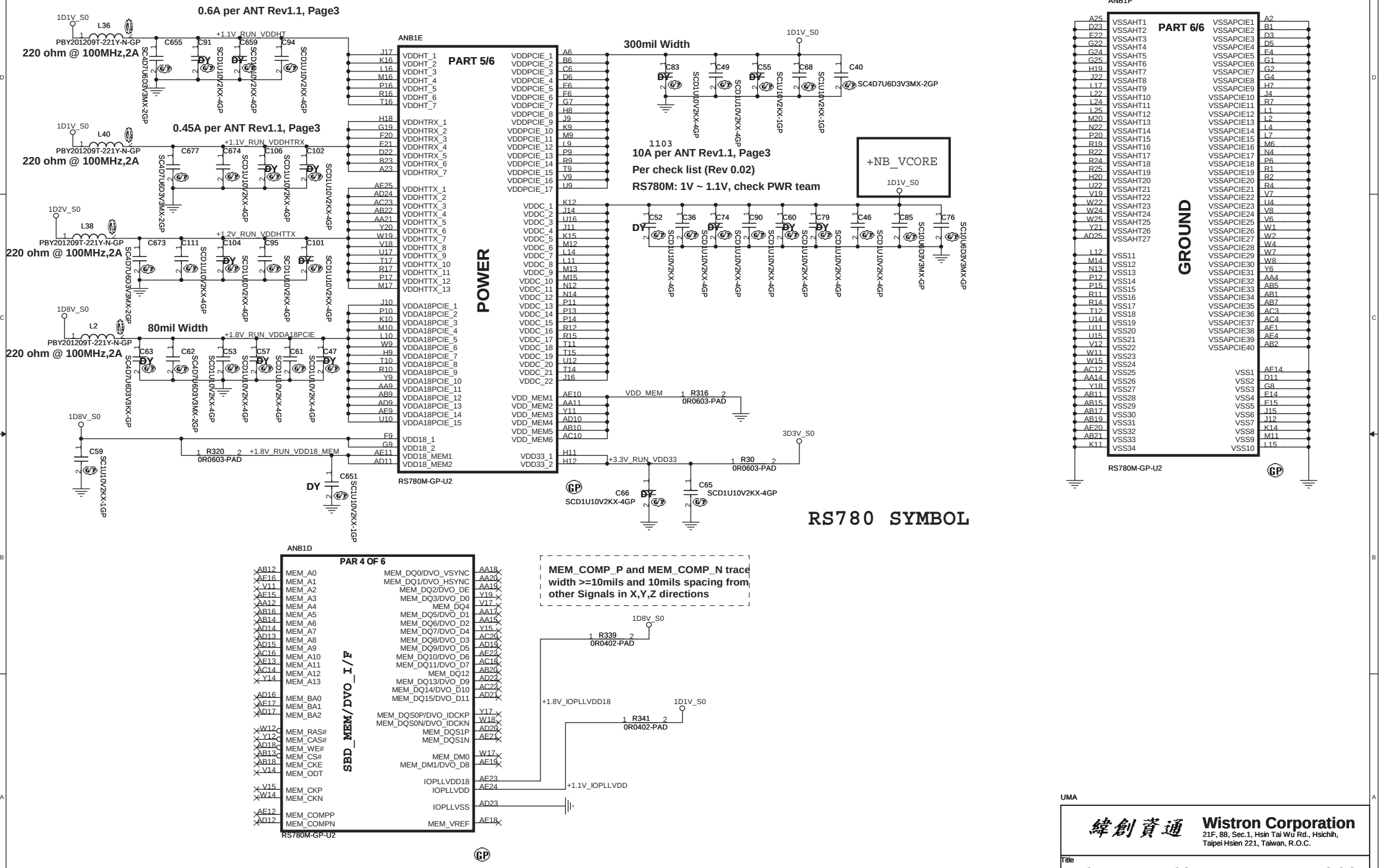
RS780 SYMBOL

35,53 BLON_IN
19,53 BRIGHTNESS_AMD
RN64 — LVDS_ENA_BL — GMCH_BL_ON — SRN0J-10-GP-UMA — UMA
for TR

UMA

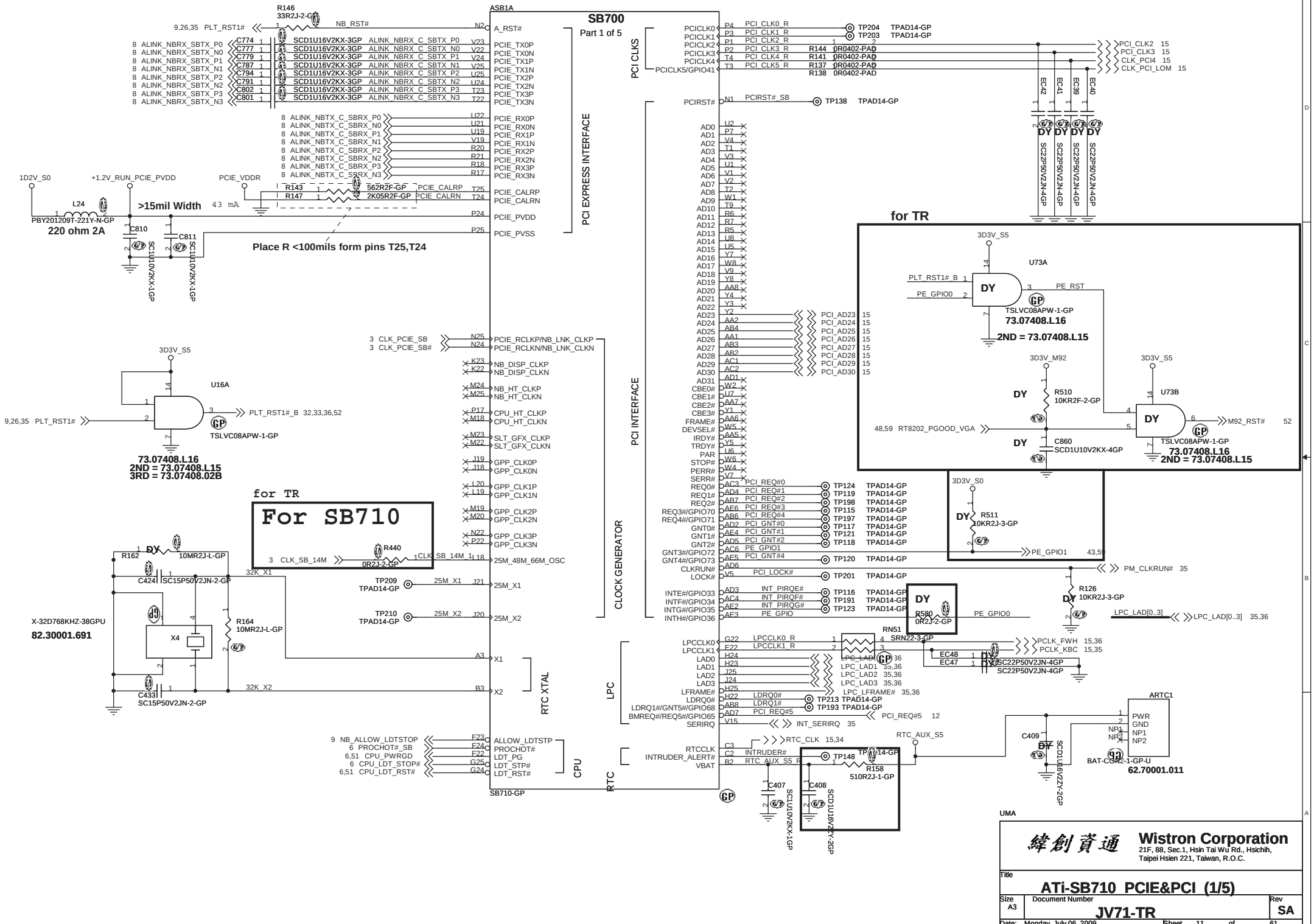
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

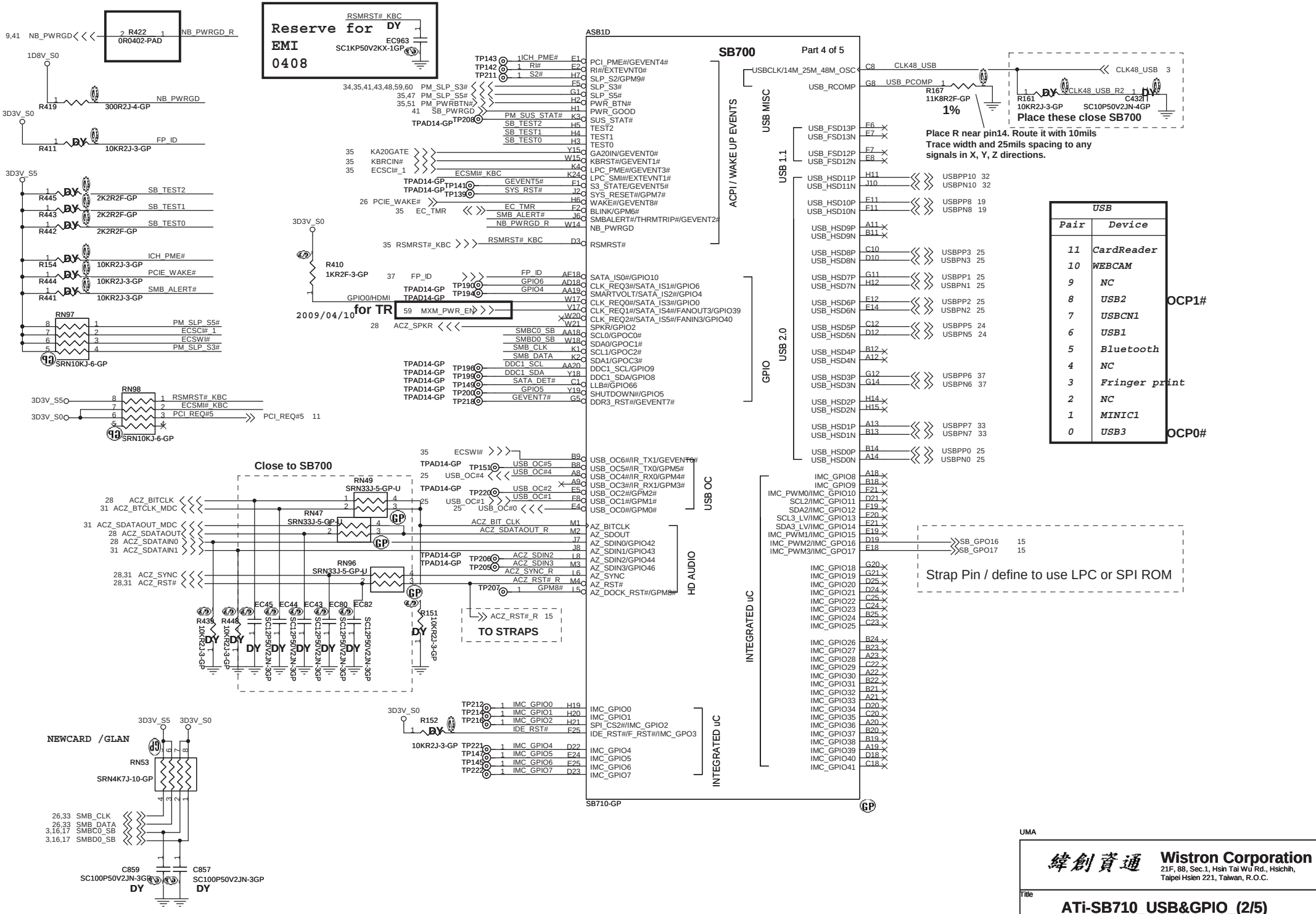
Title: ATi-RS880M LVDS&CRT (2/3)
Size: A3 | Document Number: JV71-TR | Rev: SA
Date: Monday, July 06, 2009 | Sheet 9 of 61



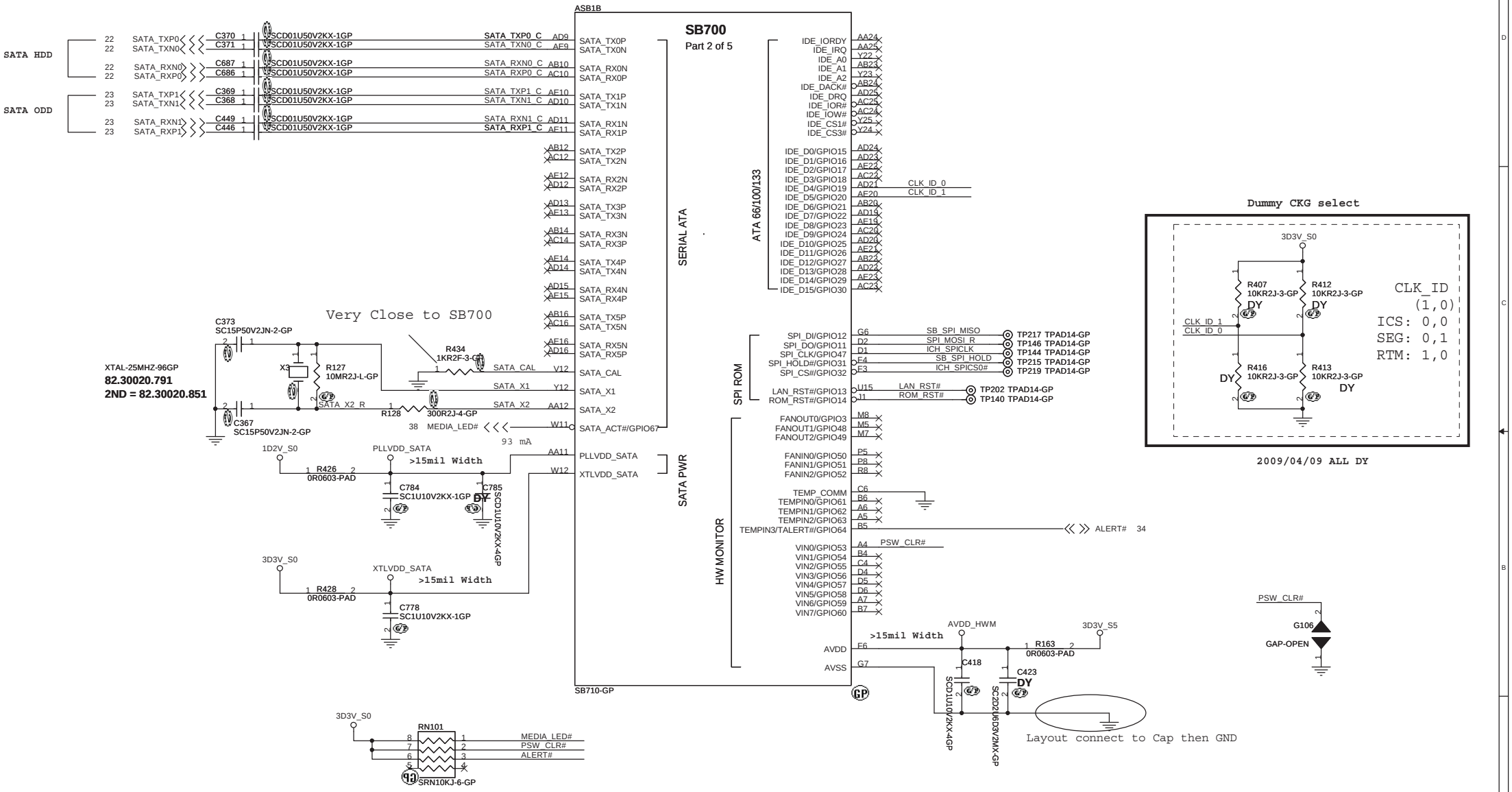
UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ATi-RS880M_Side Port&PWR&GND(3/3)**
Size: A3	Document Number: **JV71-TR**
Rev	**SA**
Date: Monday, July 06, 2009	Sheet 10 of 61


SB700
Part 1 of 5
ASB1A
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB710-GP
for TR
For SB710
for TR
>15mil Width
Place R <100mils form pins T25,T24
220 ohm 2A
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
82.30001.691
62.70001.011
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB710 PCIE&PCI (1/5)
JV71-TR
Size A3
Rev SA
Date: Monday, July 06, 2009
Sheet 11 of 61

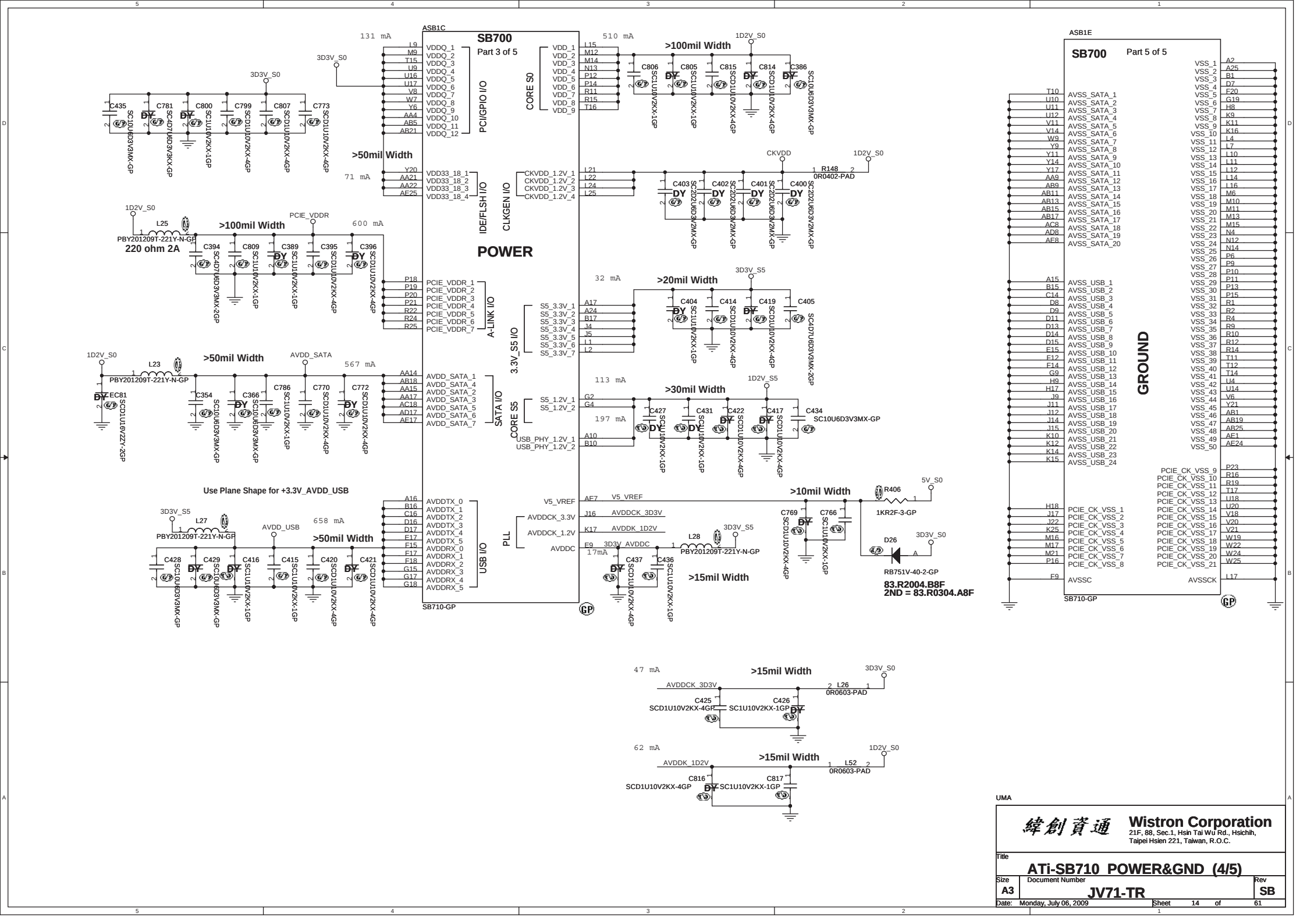

Reserve for EMI 0408
RSMRST# KBC
EC963 SC1KP50V2KX-1GP DY
ASB1D
SB700
Part 4 of 5
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#
SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#
USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#
IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7
USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N
IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41
ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC
SB710-GP
GP
USB
Pair Device
11 CardReader
10 WEBCAM
9 NC
8 USB2
7 USBCN1
6 USB1
5 Bluetooth
4 NC
3 Fringer print
2 NC
1 MINIC1
0 USB3
OCP1#
OCP0#
Strap Pin / define to use LPC or SPI ROM
TO STRAPS
Close to SB700
Place these close SB700
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
2009/04/10 for TR
NEWCARD /GLAN
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 USB&GPIO (2/5)
Size A3
Document Number JV71-TR
Rev SA
Date: Monday, July 06, 2009
Sheet 12 of 61

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700



UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	ATi-SB710 SATA-IDE (3/5)	
Size: A3	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 13 of 61	


ASB1C
SB700
Part 3 of 5
POWER
PCI/GPIO I/O
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
USB I/O
PLL
CORE S0
CORE S5
SB710-GP
ASB1E
SB700
Part 5 of 5
GROUND
SB710-GP
Use Plane Shape for +3.3V_AVDD_USB
>100mil Width
>50mil Width
>20mil Width
>30mil Width
>15mil Width
>10mil Width
220 ohm 2A
83.R2004.B8F
2ND = 83.R0304.A8F
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB710 POWER&GND (4/5)
Size
A3
Document Number
JV71-TR
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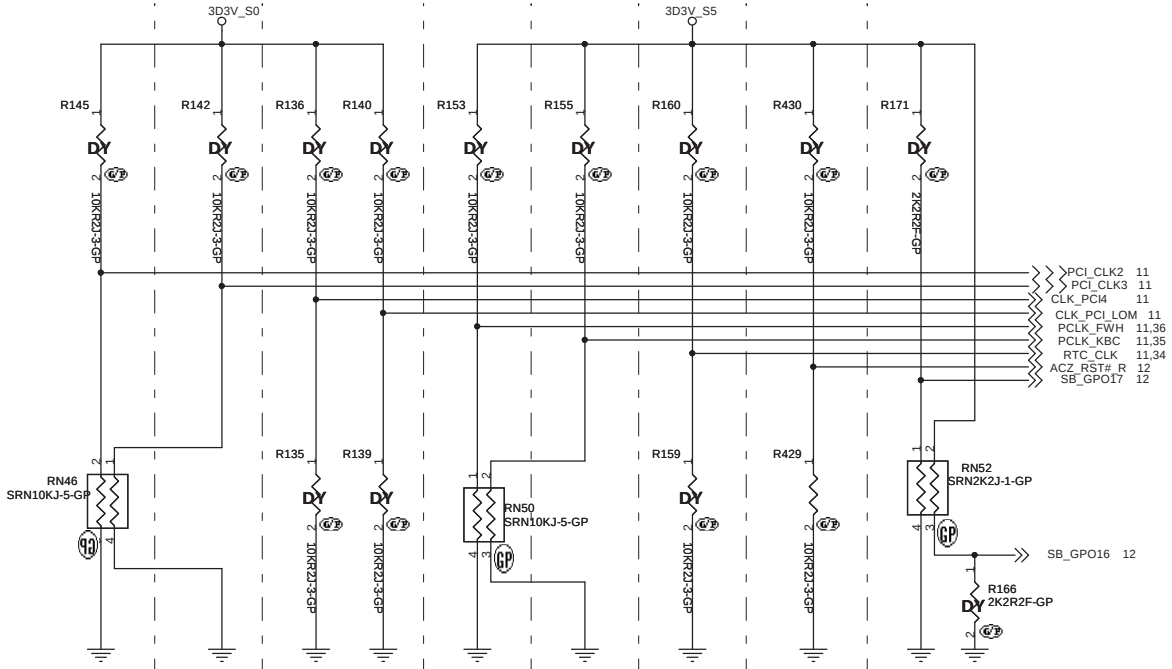
SB
Date: Monday, July 06, 2009
Sheet 14 of 61

REQUIRED STRAPS

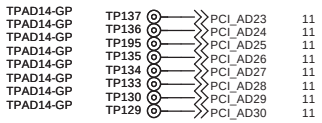
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16 ROM TYPE:
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	H, H = Reserved H, L = SPI ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM DEFAULT L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

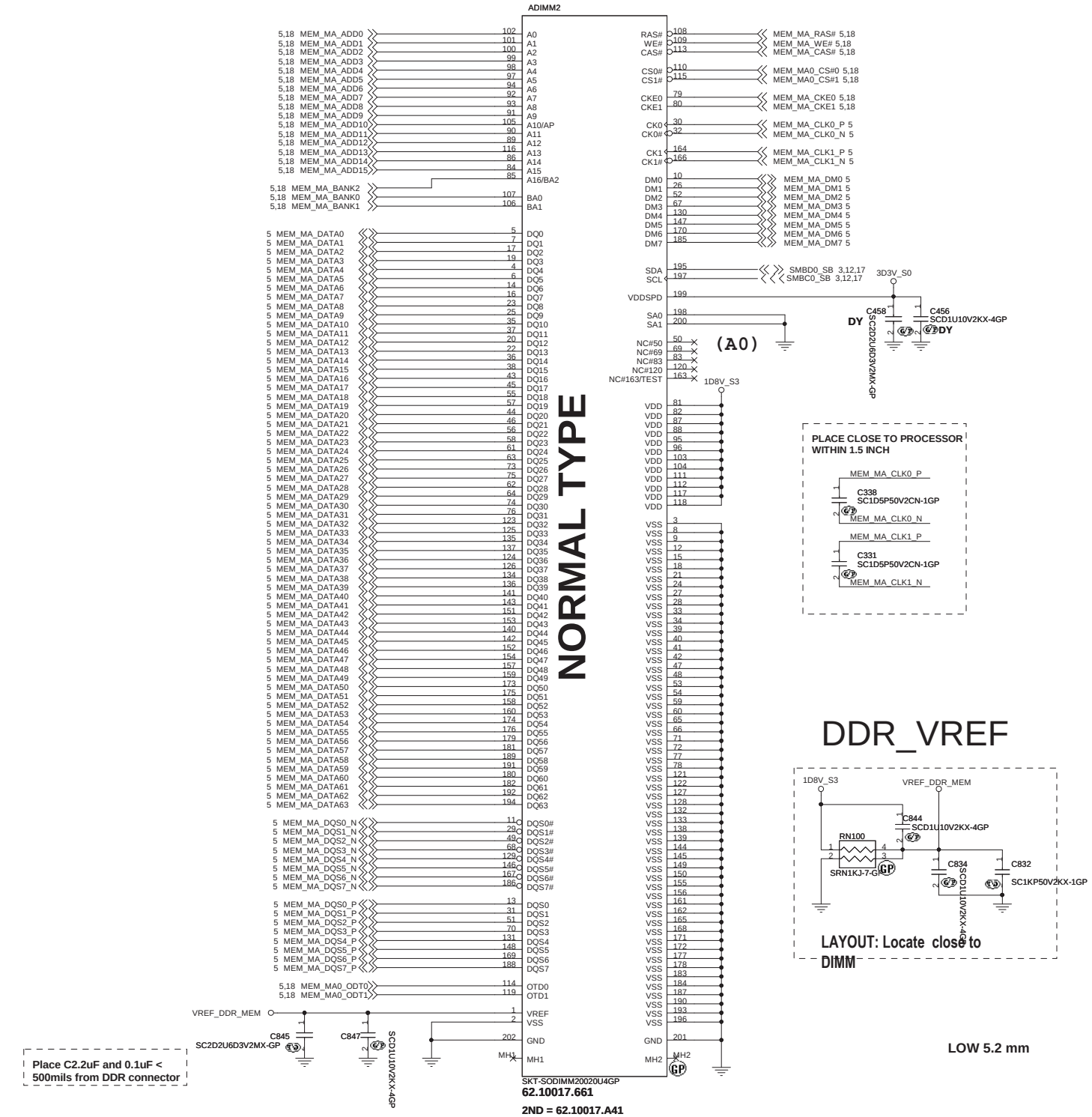
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATi-SB710 STRAPPING (5/5)**

Size	Document Number	Rev
A3	JV71-TR	SA

Date: Monday, July 06, 2009 Sheet 15 of 61



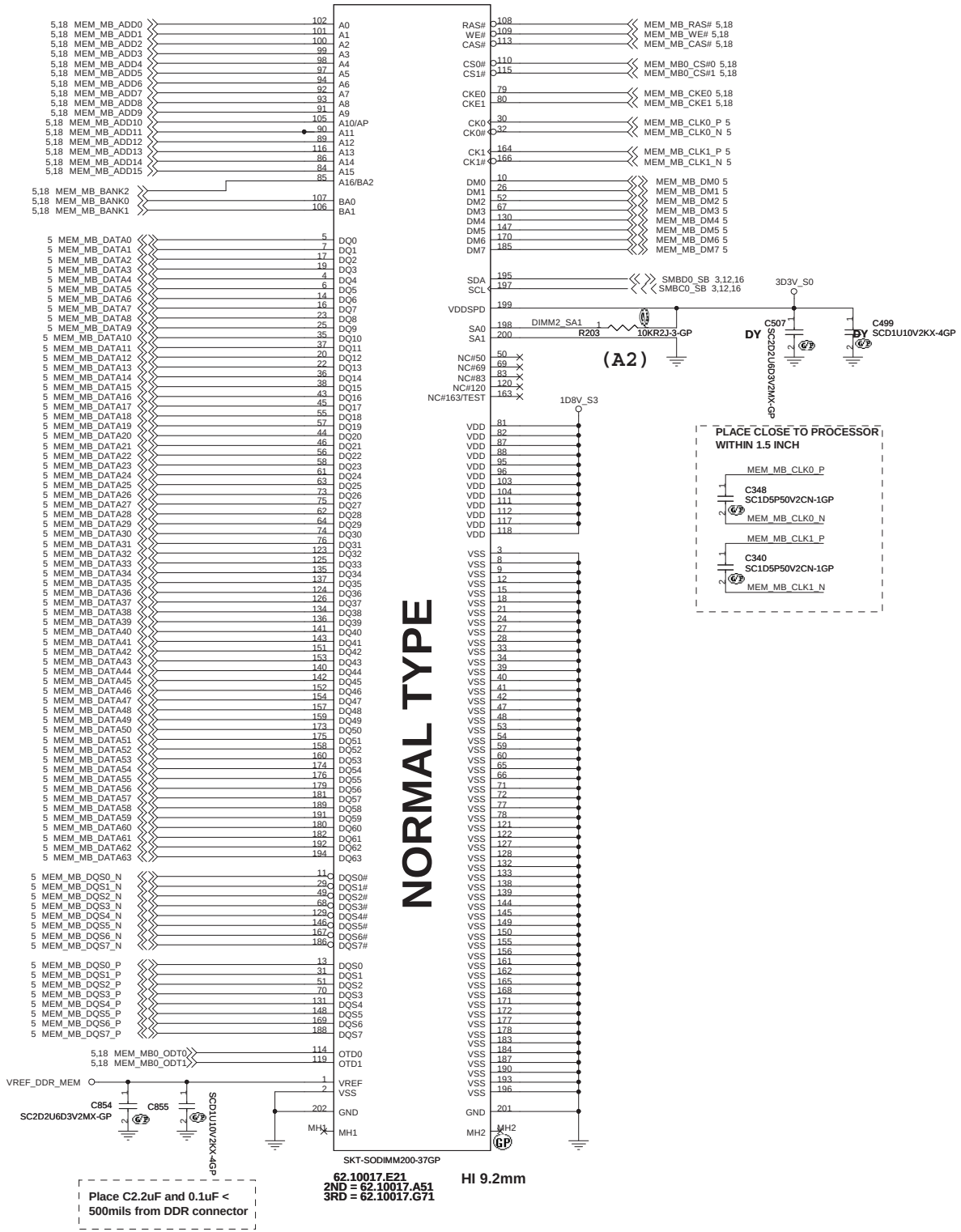
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	JV71-TR	SB

Date: Monday, July 06, 2009 Sheet 16 of 61

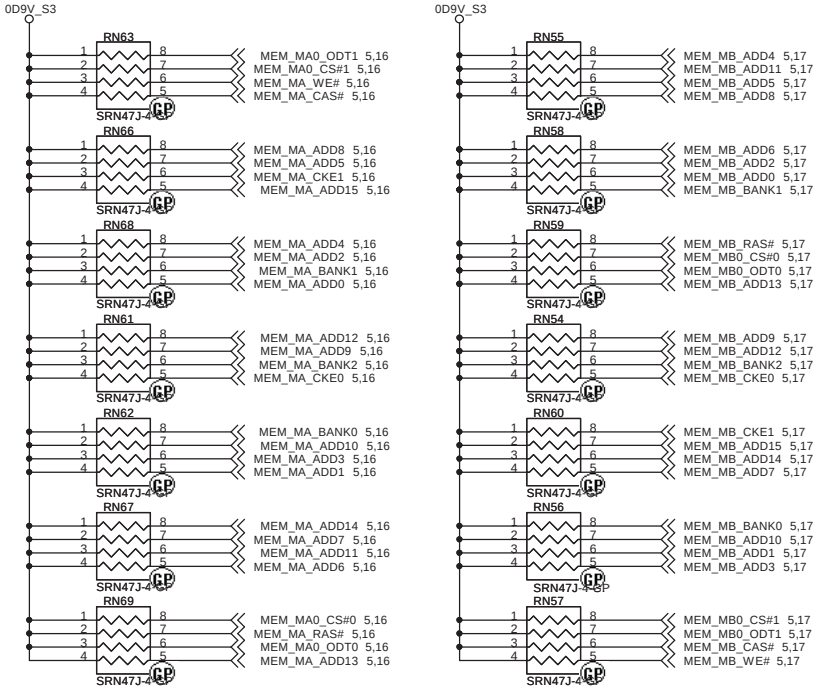


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**DDR_SO-DIMM SKT_2**	
Size: Custom	Document Number: **JV71-TR**	Rev: **SB**
Date: Monday, July 06, 2009	Sheet 17 of 61	

PARALLEL TERMINATION

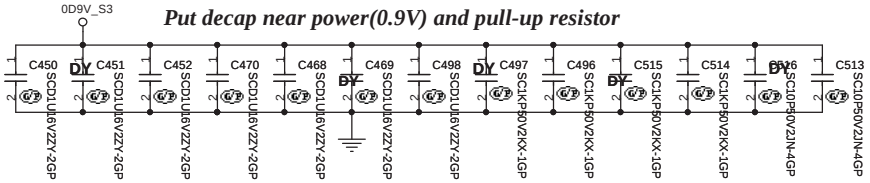
Put decap near power(0.9V) and pull-up resistor



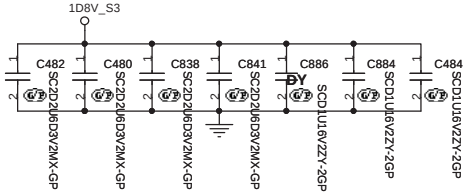
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

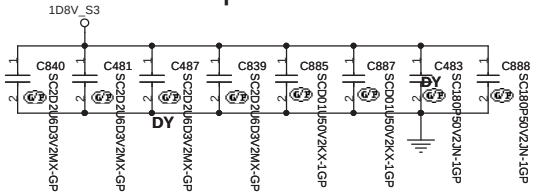


Place these Caps near DM1



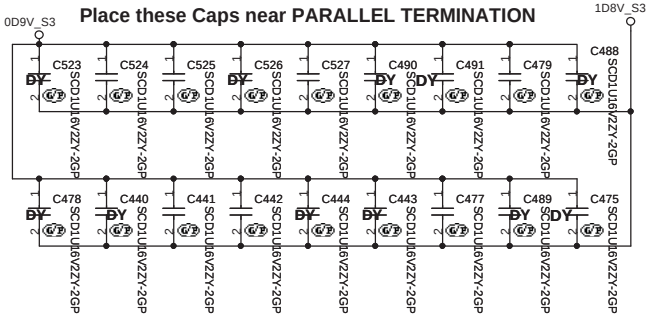
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



UMA

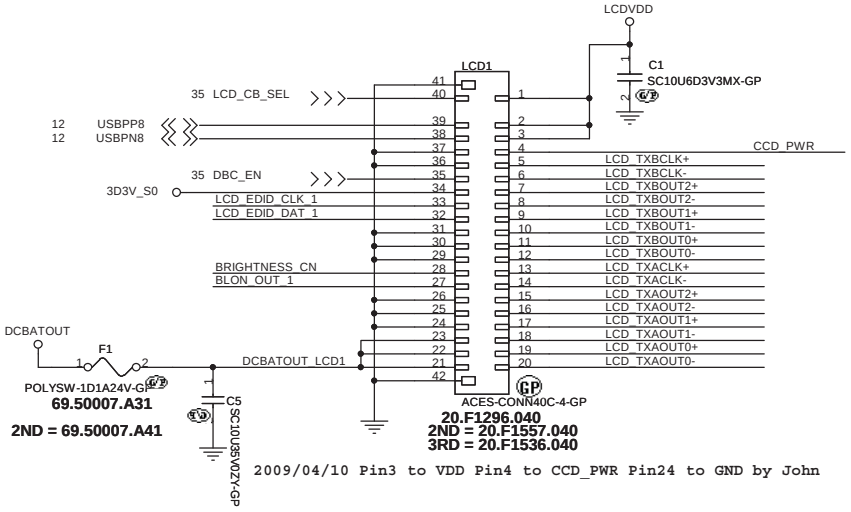
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR_DAMPING & TERMINATION**

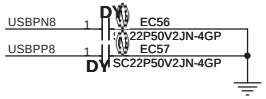
Size	Document Number	Rev
A3	JV71-TR	SB

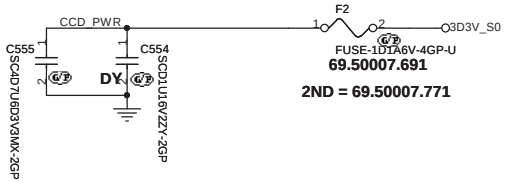
Date: Monday, July 06, 2009 Sheet 18 of 61

LCD/INVERTER/CCD CONN

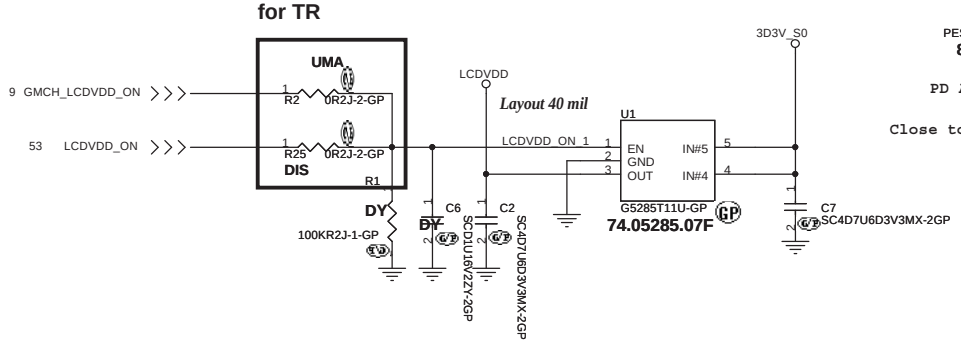


2009/04/10 Pin3 to VDD Pin4 to CCD_PWR Pin24 to GND by John

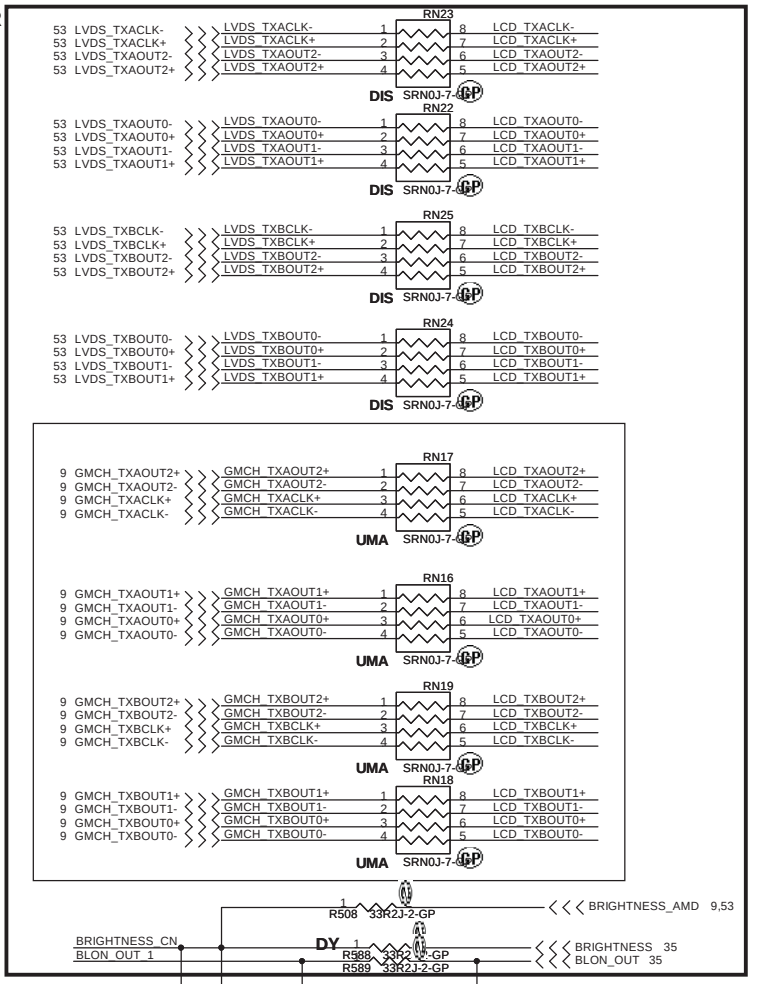


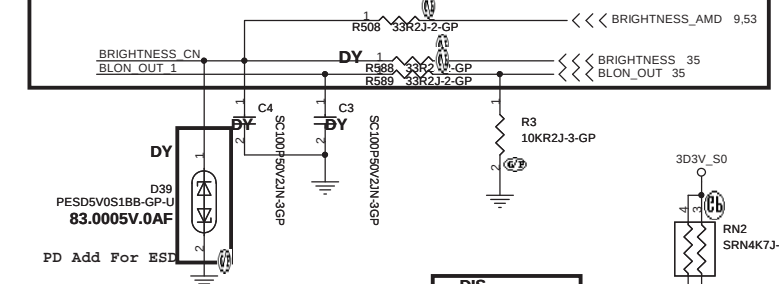


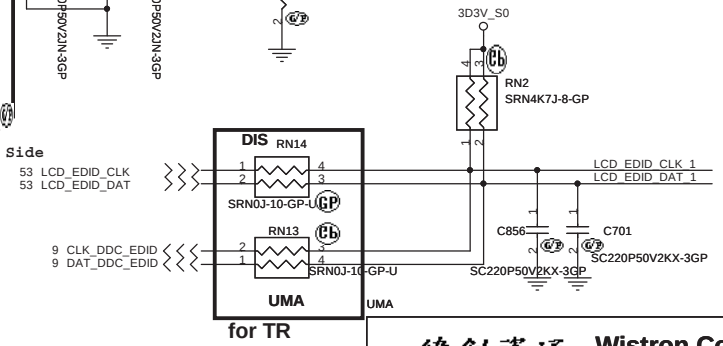
for TR



for TR







Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

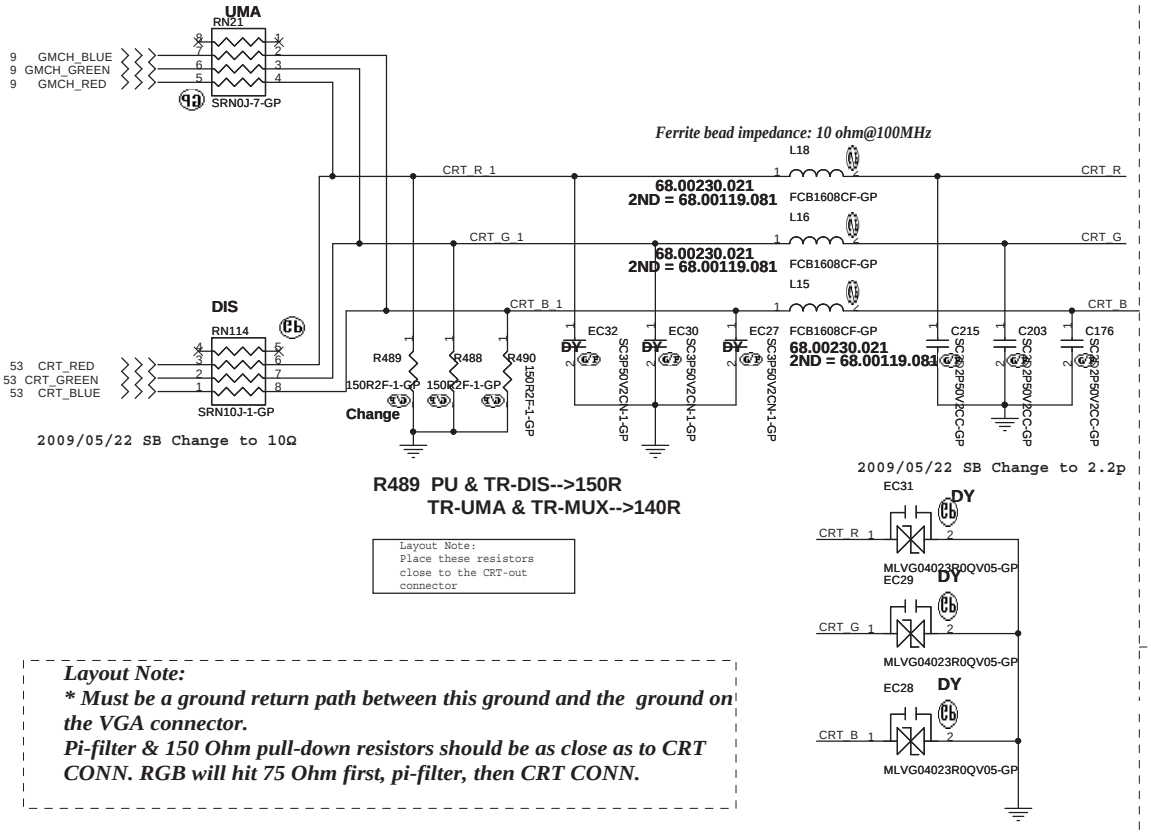
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

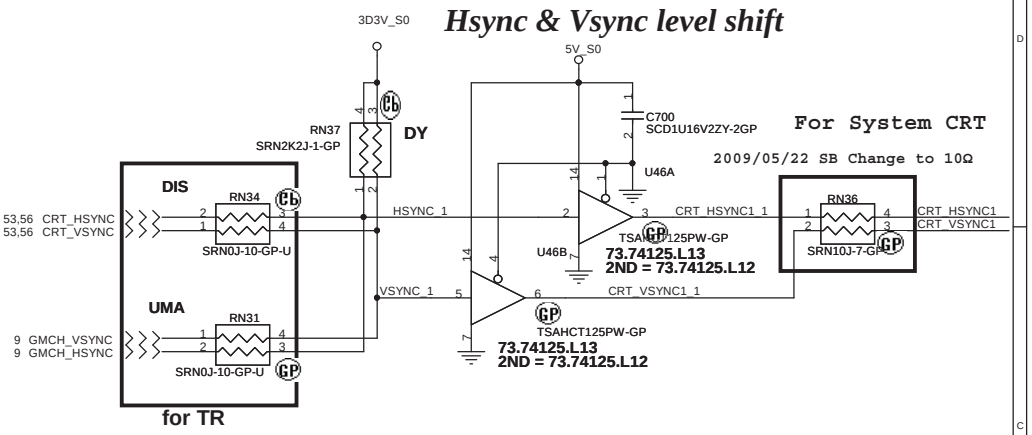
Title: **LCD CONN**

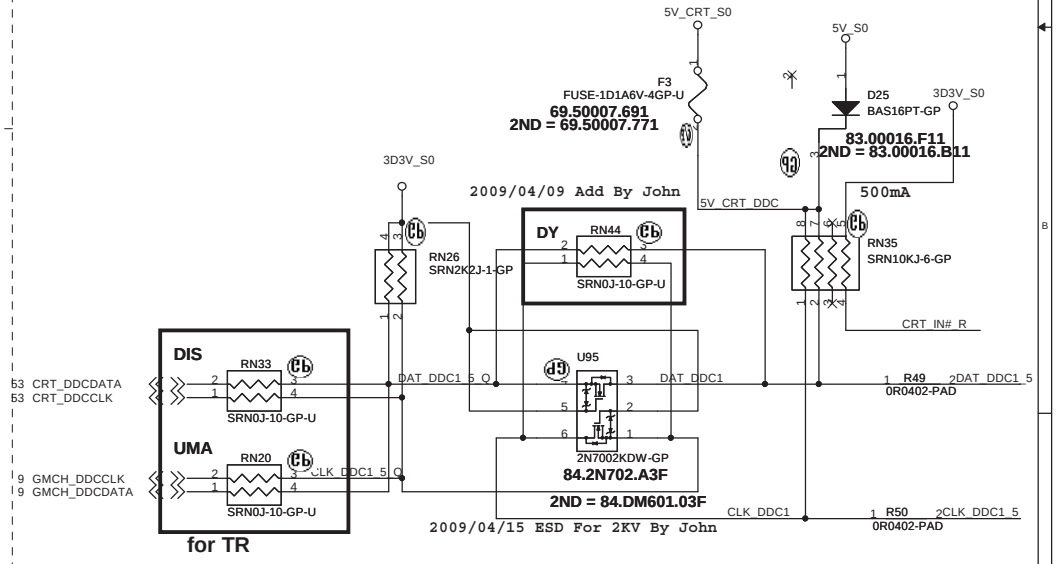
Size	Document Number	Rev
A3	JV71-TR	-1

Date: Monday, July 06, 2009 Sheet 19 of 61

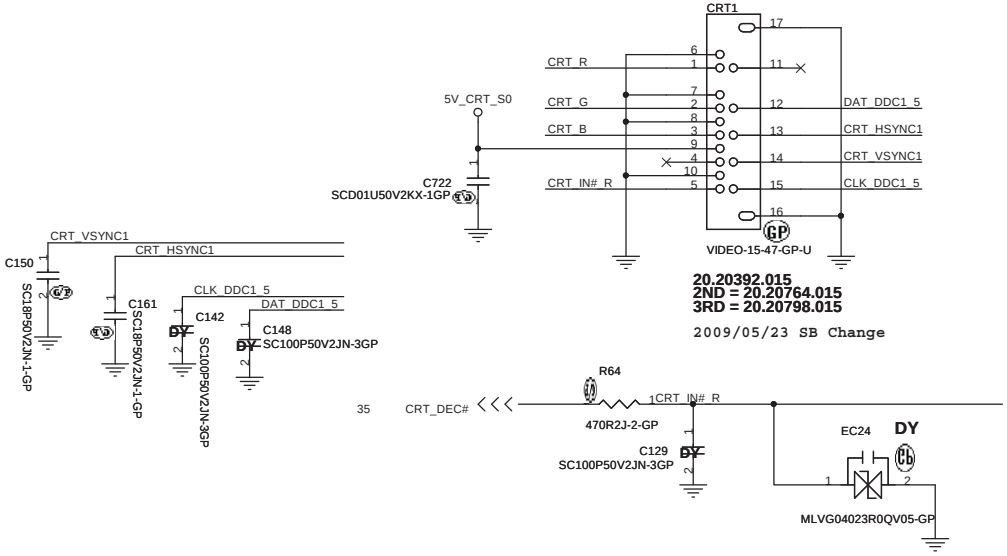


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

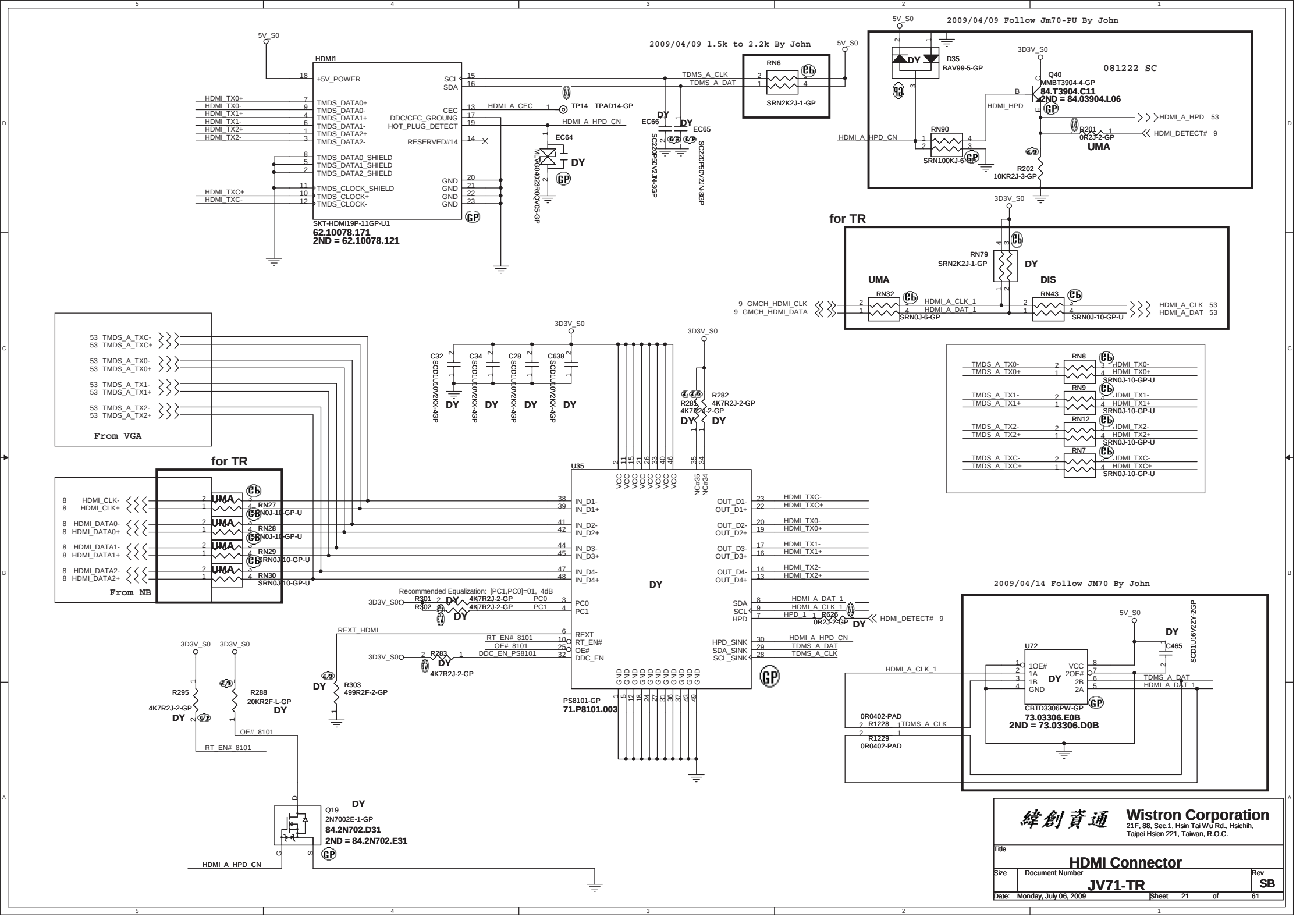




CRT I/F & CONNECTOR



UMA			
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	CRT Connector		
Size	Document Number: JV71-TR		Rev: SB
Date: Monday, July 06, 2009	Sheet 20 of 61		


2009/04/09 1.5k to 2.2k By John
2009/04/09 Follow Jm70-PU By John
081222 SC
HDMI1
SKT-HDMI19P-11GP-U1
62.10078.171
2ND = 62.10078.121
RN6
SRN2K2J-1-GP
D35
BAV99-5-GP
Q40
MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.L06
RN90
SRN100KJ-6-GP
R201
0R2J-2-GP
UMA
R202
10KR2J-3-GP
for TR
RN79
SRN2K2J-1-GP
DIS
RN32
RN43
SRN0J-6-GP
SRN0J-10-GP-U
From VGA
From NB
RN27
RN28
RN29
RN30
SRN0J-10-GP-U
RN8
RN9
RN12
RN7
U35
PS8101-GP
71.P8101.003
Recommended Equalization: [PC1,PC0]=01, 4dB
R282
4K7R2J-2-GP
R283
R301
R302
R303
499R2F-2-GP
R295
R288
20KR2F-L-GP
REXT_HDMI
OE# 8101
RT_EN# 8101
DDC_EN_PS8101
Q19
2N7002E-1-GP
84.2N702.D31
2ND = 84.2N702.E31
2009/04/14 Follow JM70 By John
U72
CBTD3306PW-GP
73.03306.E0B
2ND = 73.03306.D0B
R1228
R1229
0R0402-PAD
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI Connector
Size
Document Number
JV71-TR
Rev
SB
Date: Monday, July 06, 2009
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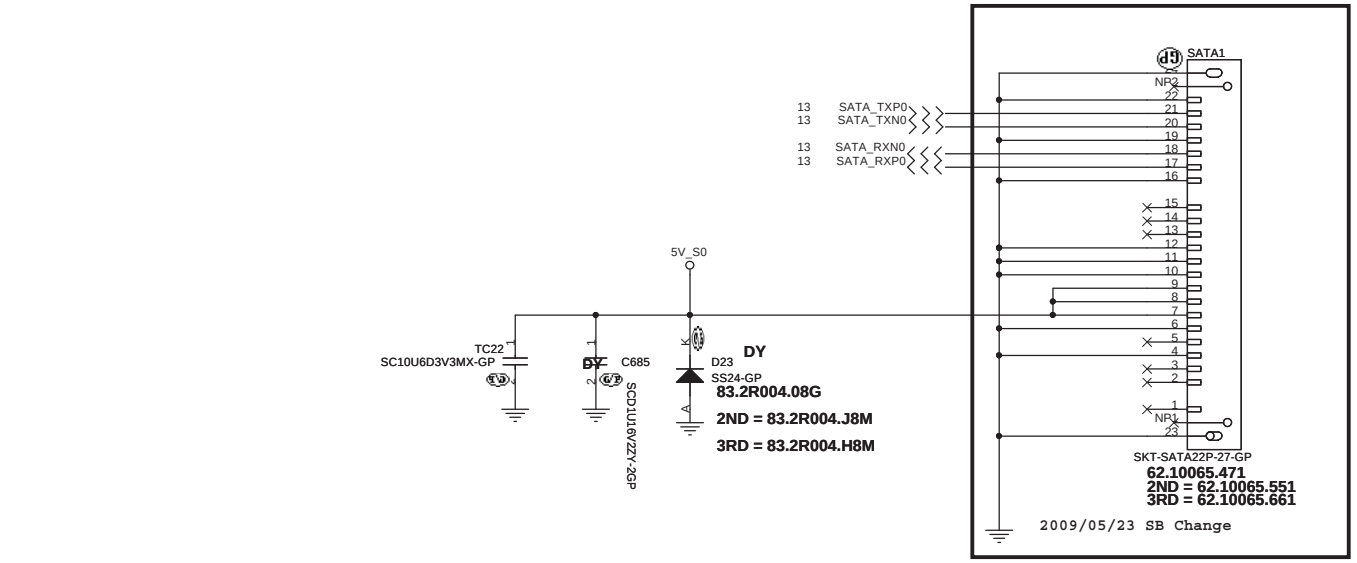
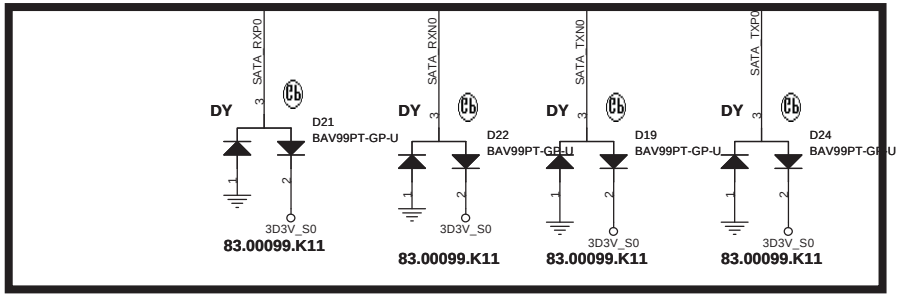
SATA Connector

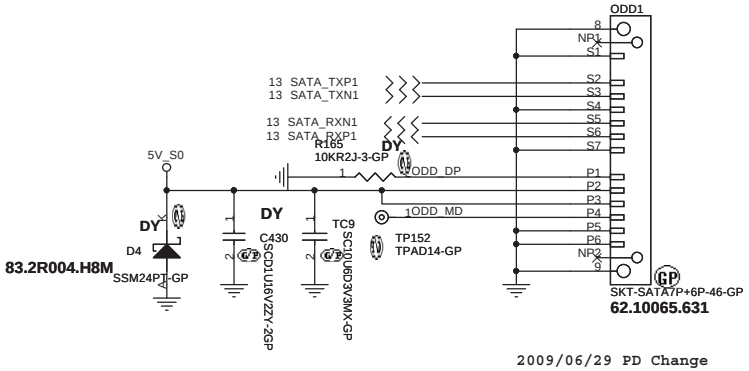


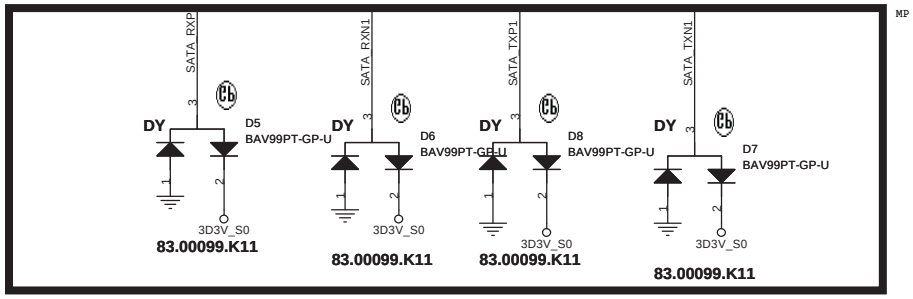


UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD		
Size	Document Number: JV71-TR	Rev: SB
Date: Monday, July 06, 2009	Sheet 22 of 61	

SATA ODD Connector





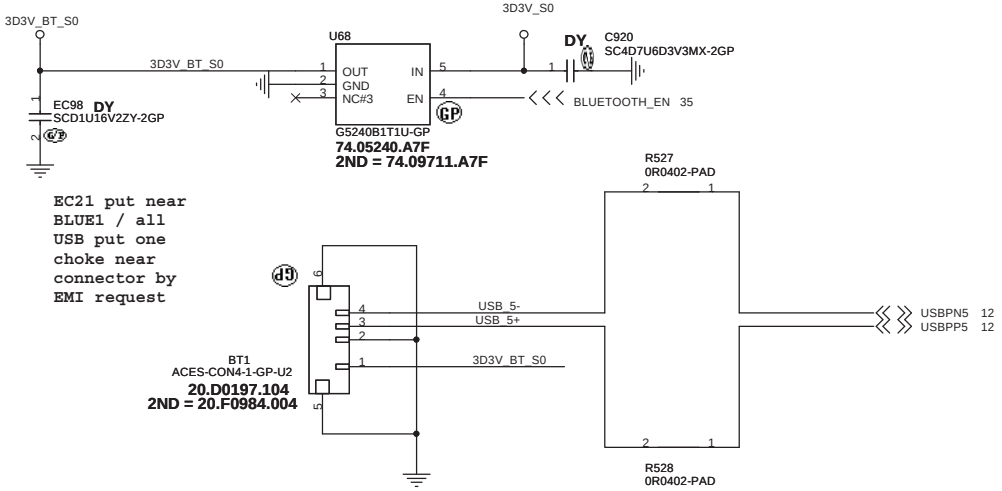
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ODD		
Size	Document Number	Rev
	JV71-TR	**SB**
Date: Monday, July 06, 2009	Sheet 23 of 61	

BLUETOOTH MODULE

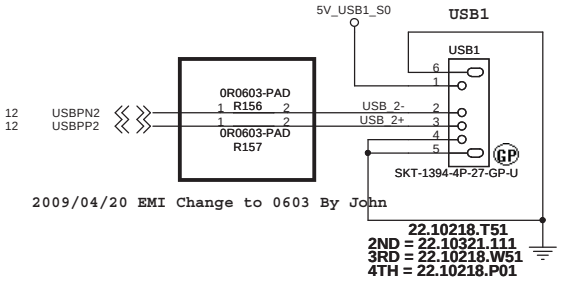
1.5A / High Active Voltage 2V

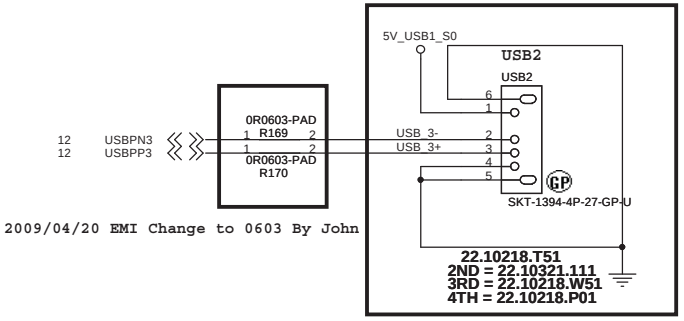


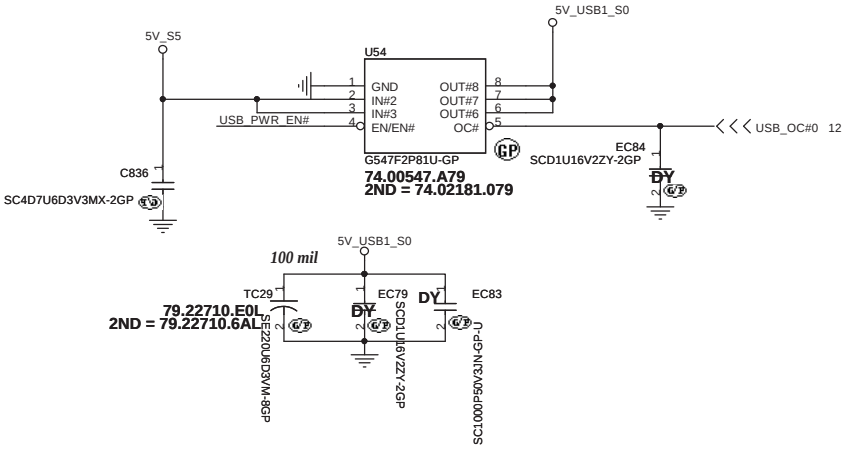
UMA

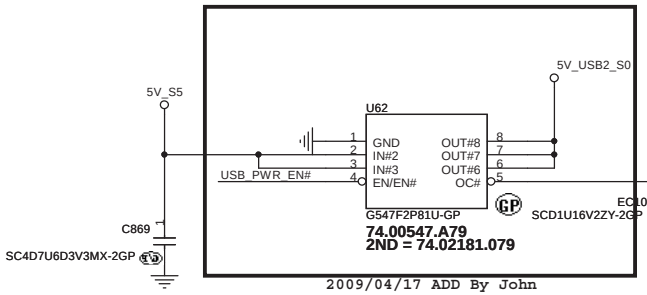
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

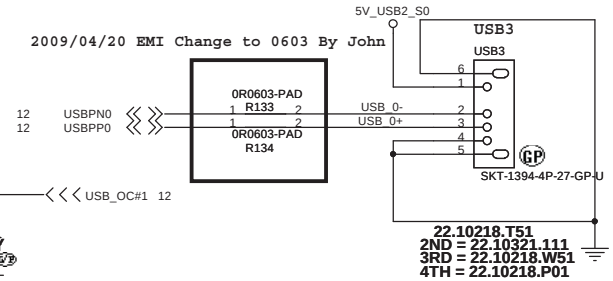
Title		
BLUETOOTH		
Size	Document Number **JV71-TR**	Rev **SA**
Date: Monday, July 06, 2009	Sheet 24 of 61	

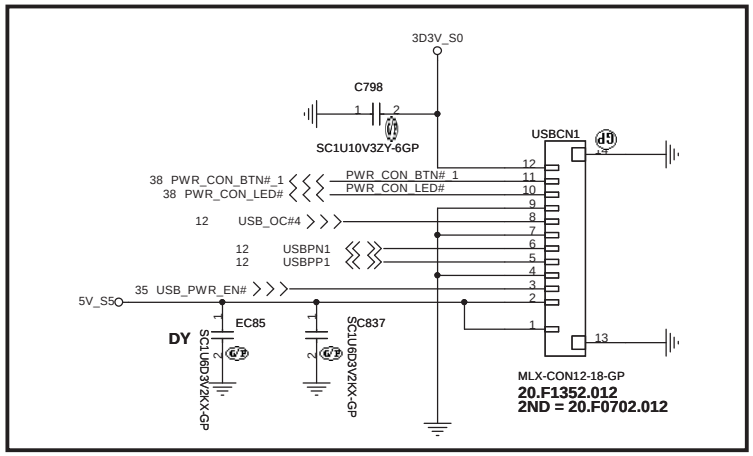


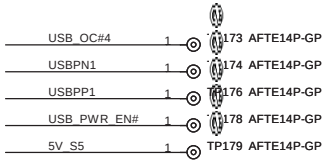


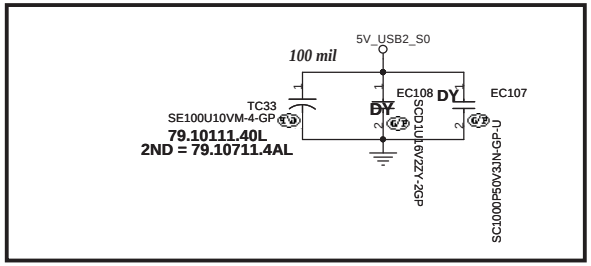








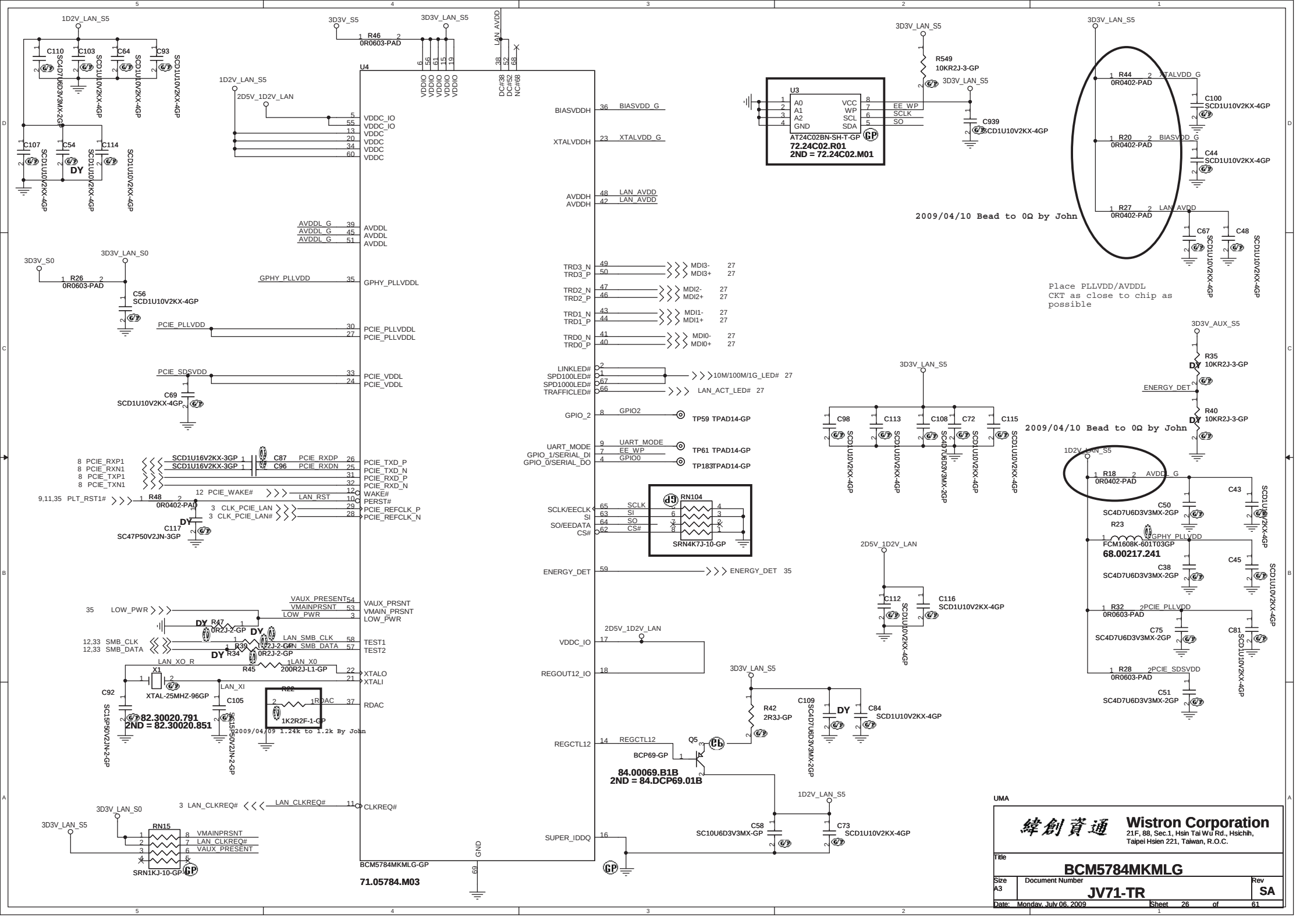




UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

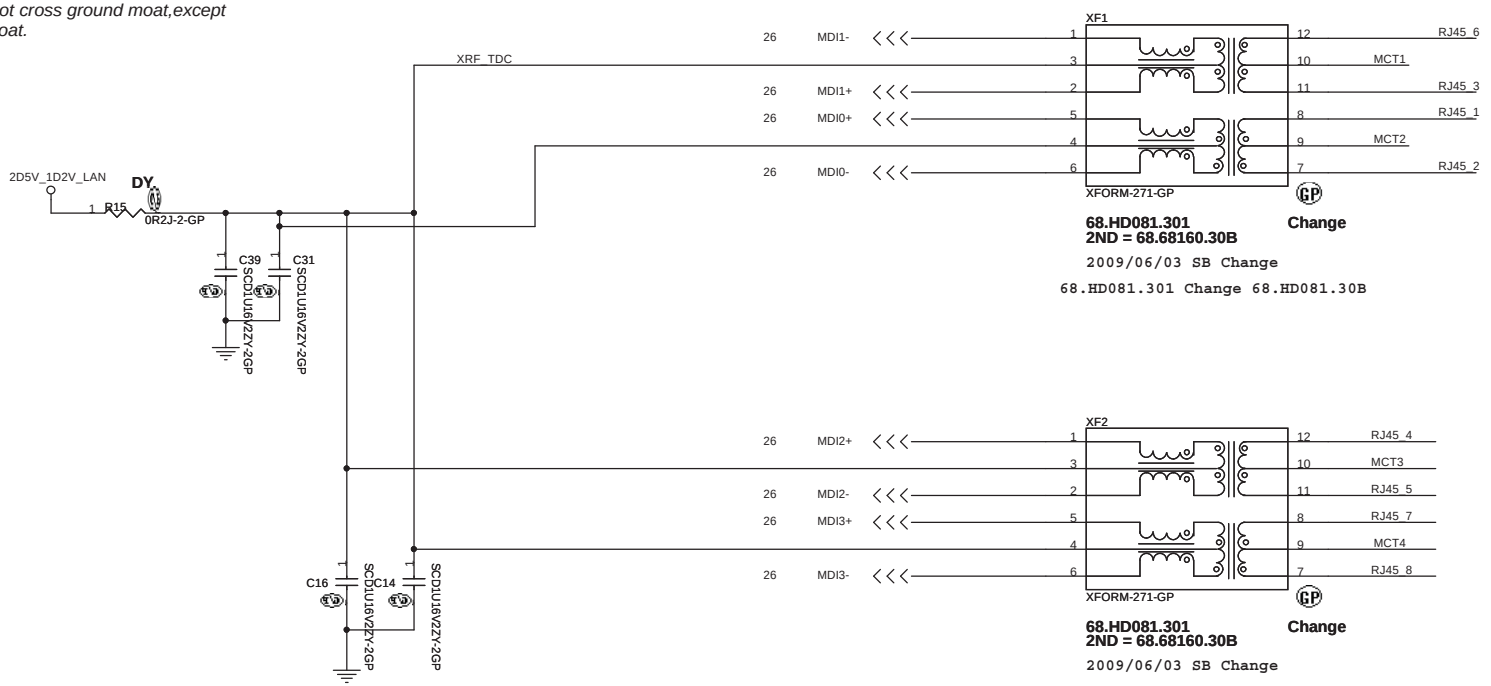
Title	USB	
Size	Document Number: JV71-TR	Rev: SA
Date: Monday, July 06, 2009	Sheet 25 of 61	

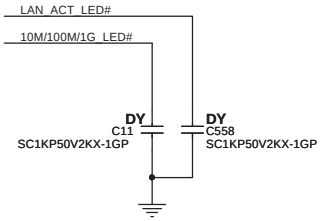

U4
BCM5784MKMLG-GP
71.05784.M03
2009/04/10 Bead to 0Ω by John
Place PLLVDD/AVDDL CKT as close to chip as possible
2009/04/10 Bead to 0Ω by John
82.30020.791
2ND = 82.30020.851
2009/04/09 1.24k to 1.2k By John
84.00069.B1B
2ND = 84.DCP69.01B
72.24C02.R01
2ND = 72.24C02.M01
AT24C02BN-SH-T-GP
SRN4K7J-10-GP
SRN1KJ-10-GP
BCP69-GP
FCM1608K-601T03GP
68.00217.241
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5784MKMLG
Size A3
Document Number JV71-TR
Rev SA
Date: Monday, July 06, 2009
Sheet 26 of 61

LAN Connector

GIGA Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

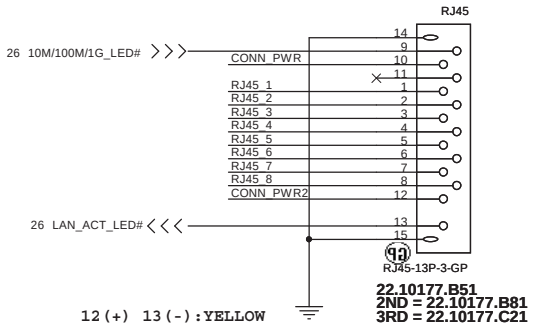




DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10(+) 9(-)::GREEN
10(+) 11(-):ORANGE

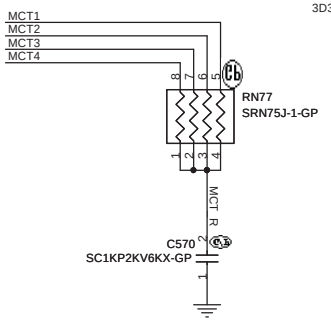
LAN Connector



22.10177.B51
2ND = 22.10177.B81
3RD = 22.10177.C21

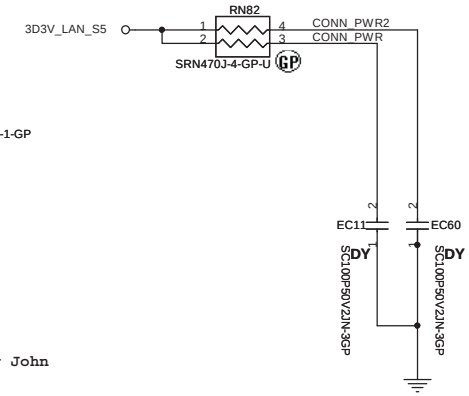
12(+) 13(-):YELLOW

2009/05/23 SB Change



2009/04/09 Follow JV70-PU By John

2009/04/09 Change 4P2R By John



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

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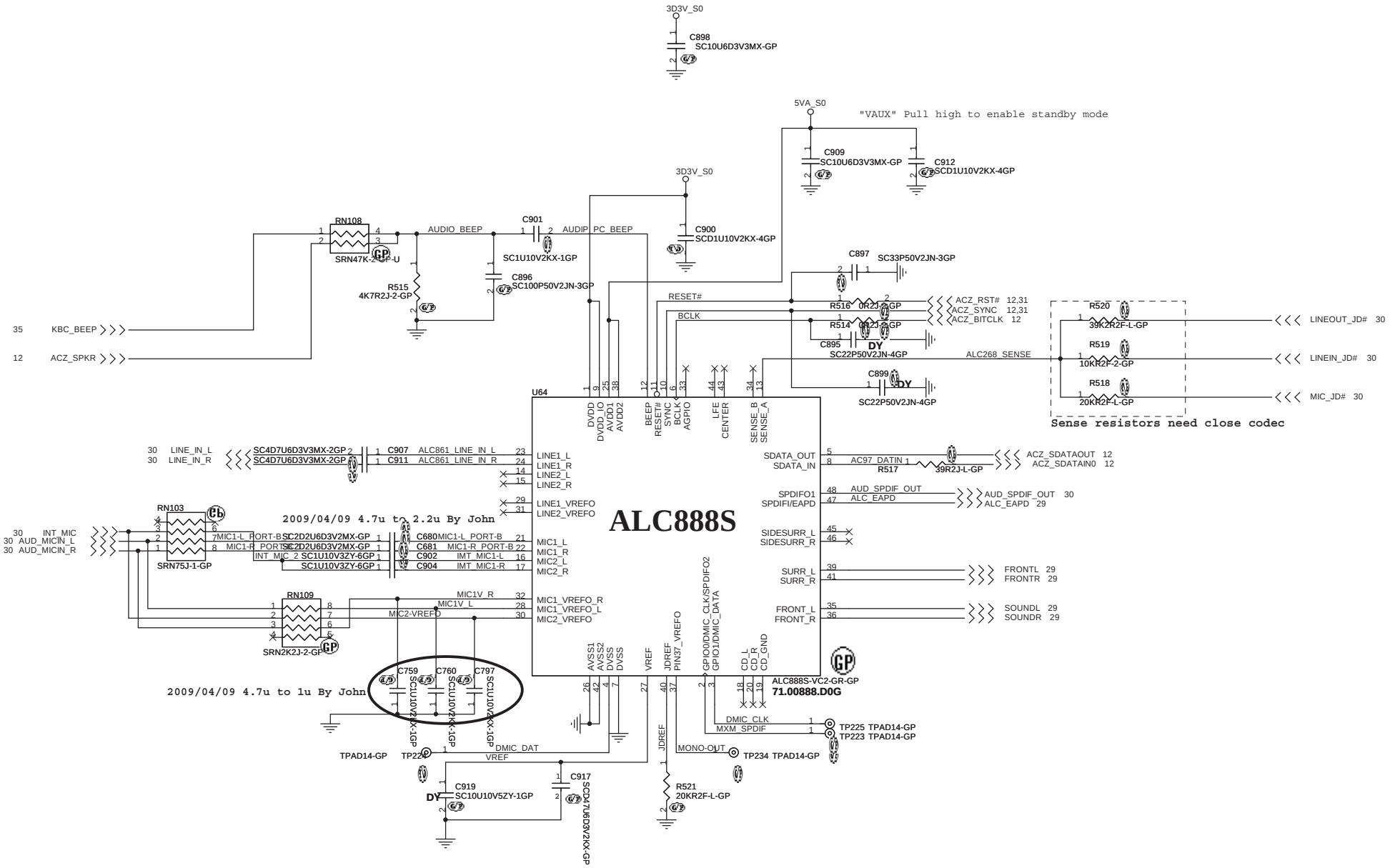

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Azalia codec ALC888**	
Size A3	Document Number **JV71-TR**	Rev **SB**
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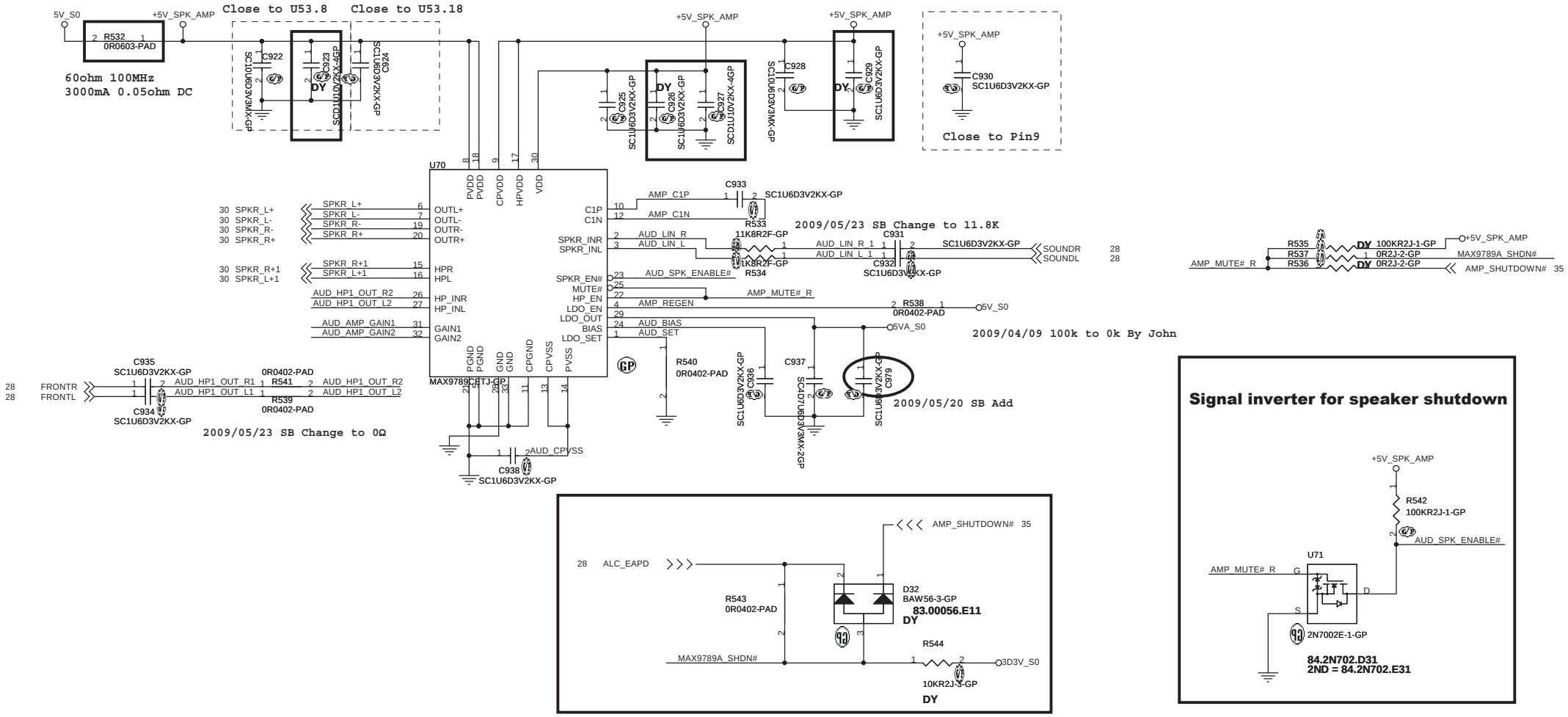

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

UMA

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP**

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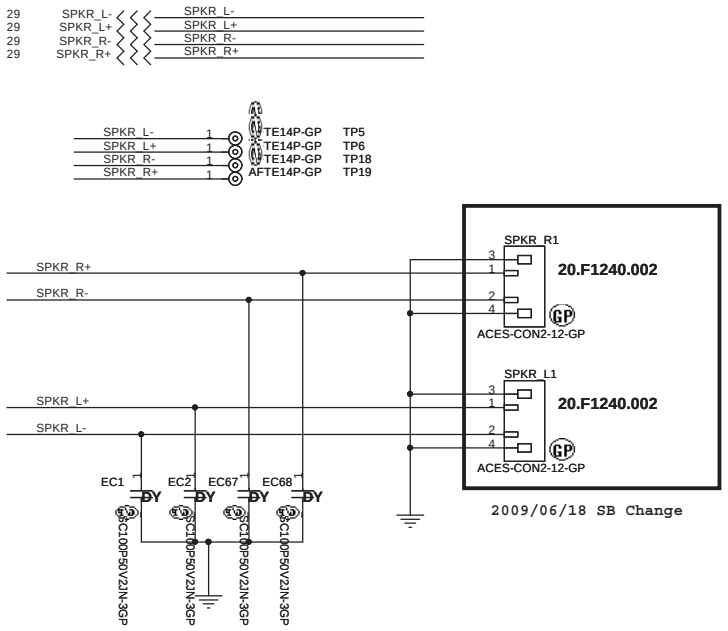
Internal Speaker



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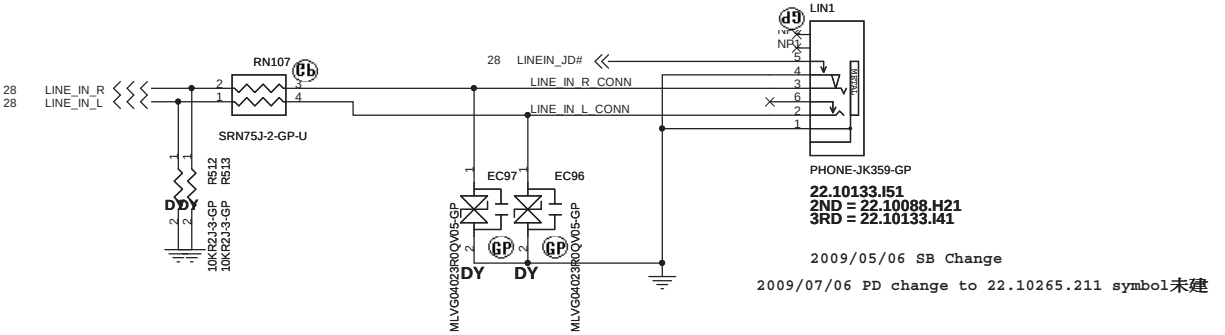

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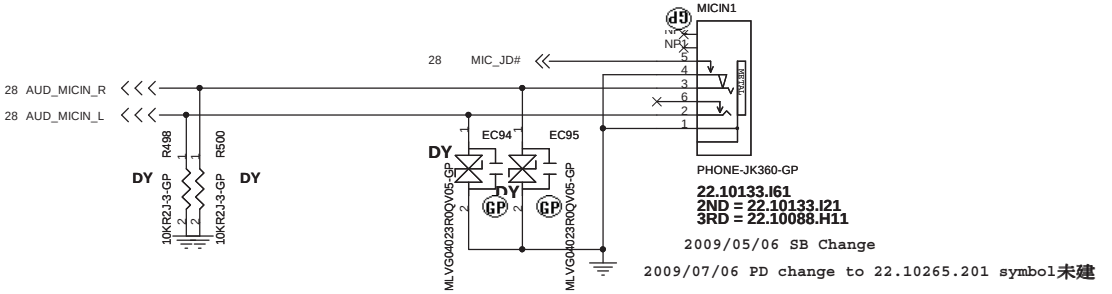

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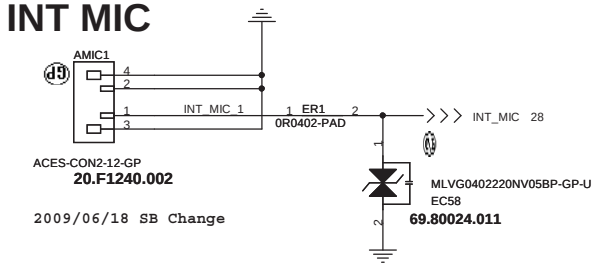

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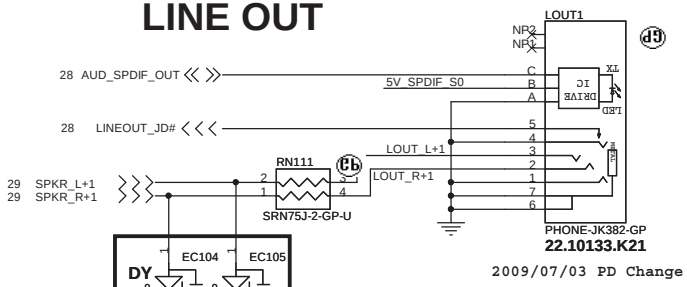

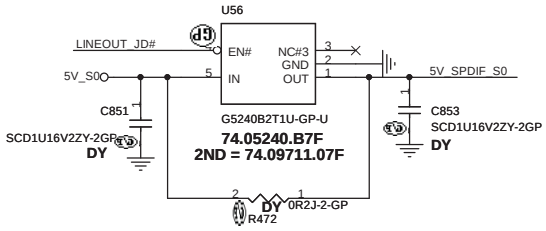

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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO JACK		
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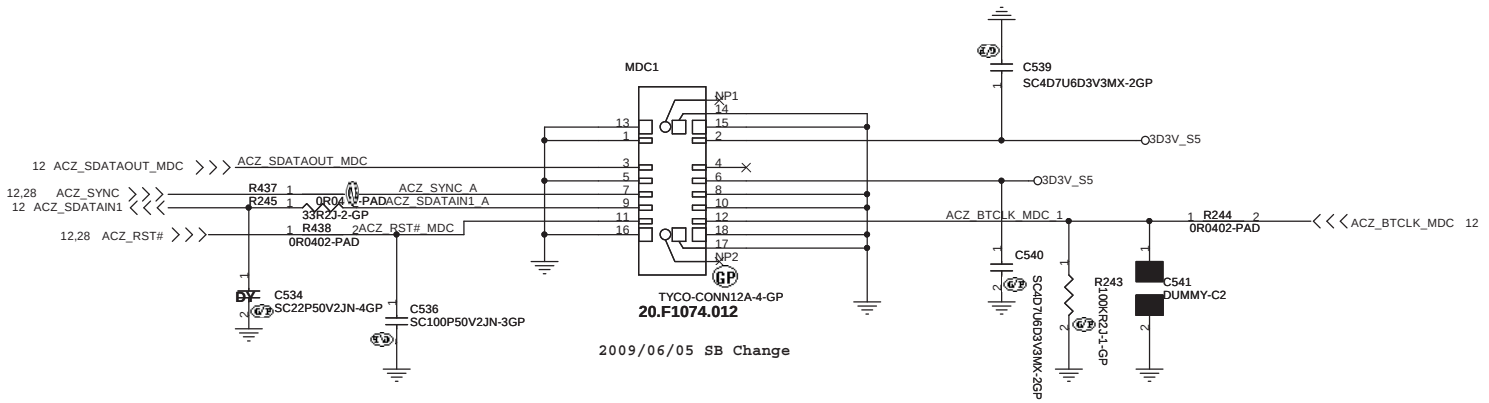
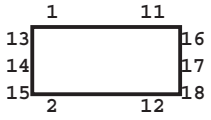
MDC 1.5 CONN





UMA

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Title: MDC		
Size	Document Number: JV71-TR	Rev: SB
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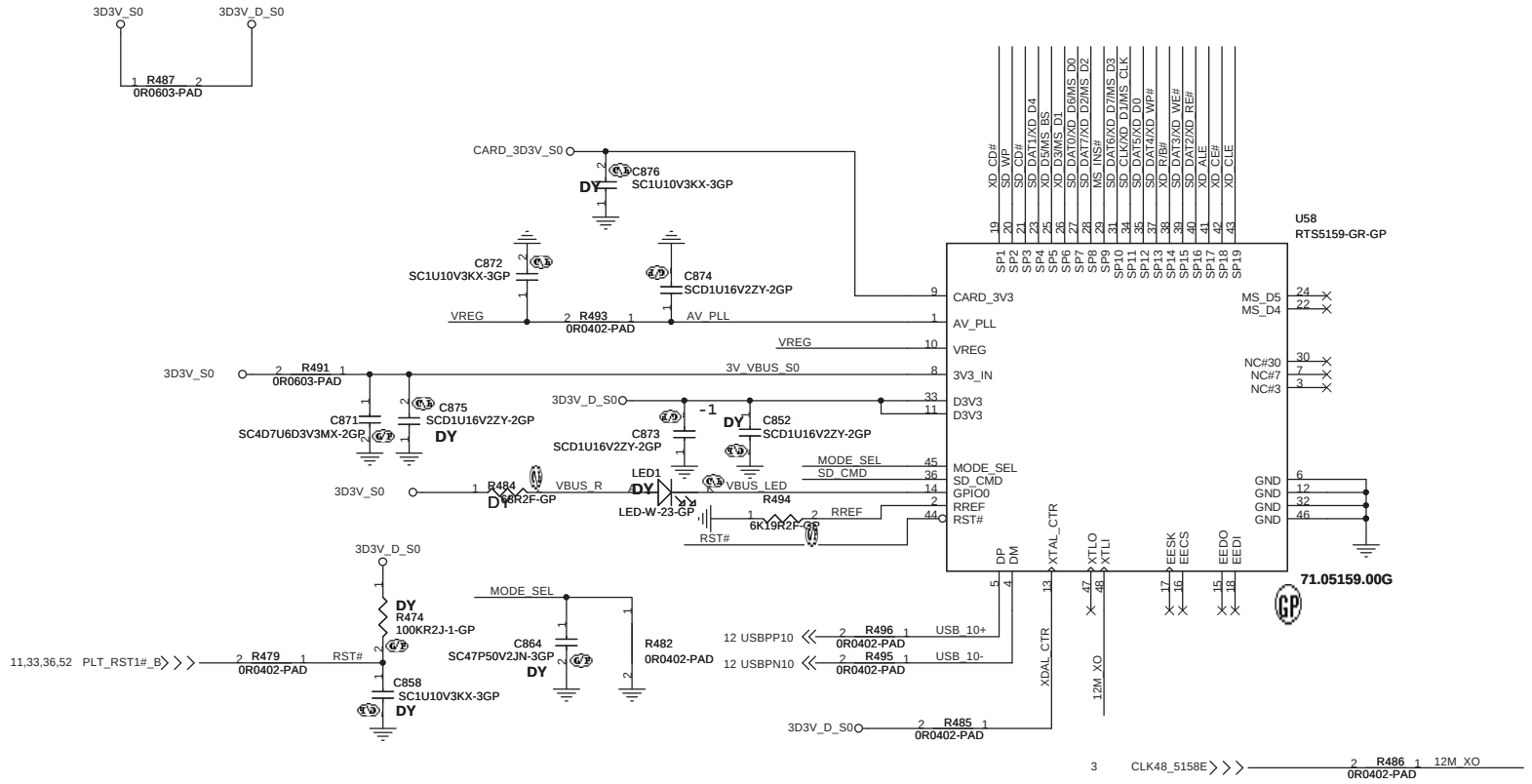
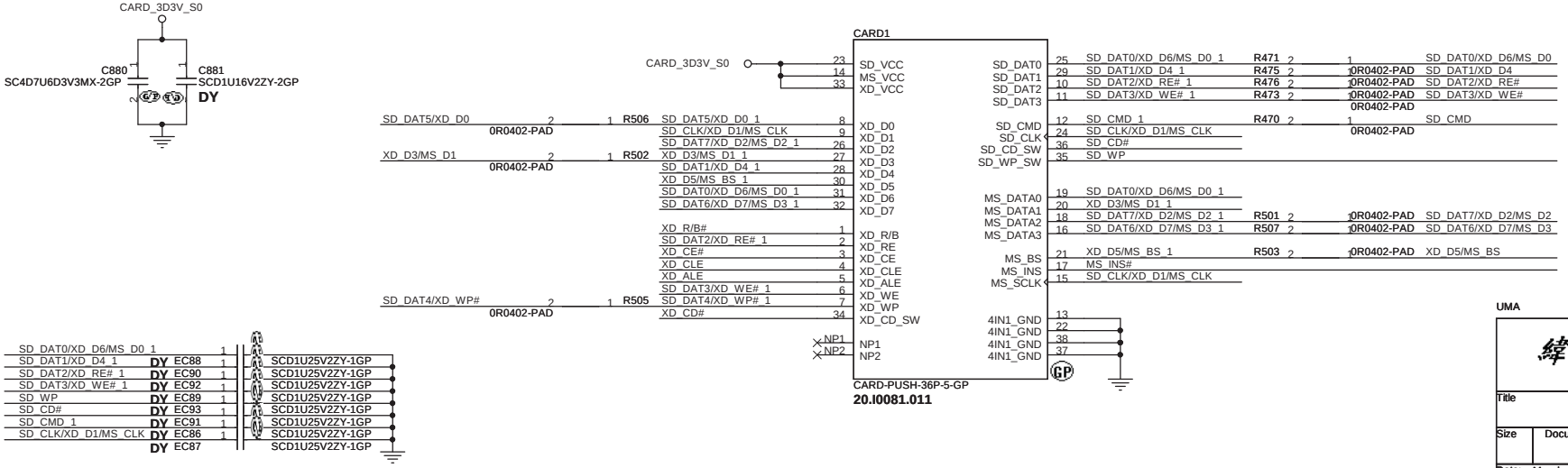


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	**CARDREADER- RTS5159**		
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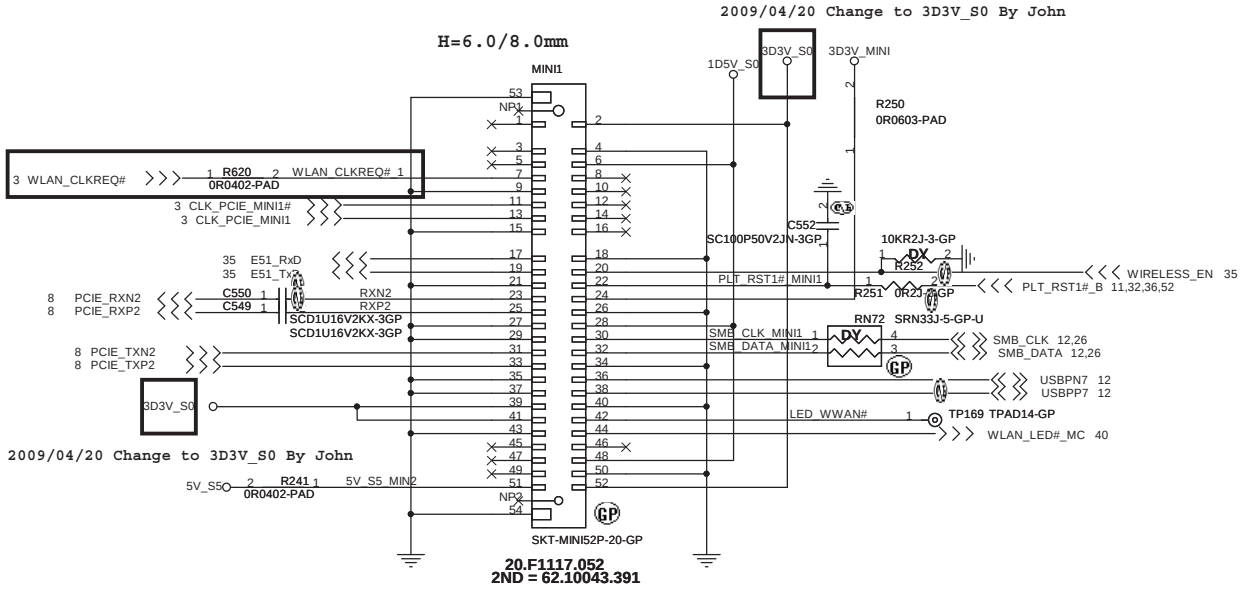
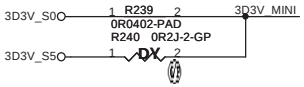
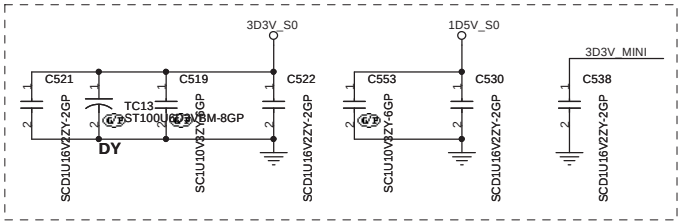
Mini Card Connector(WLAN)





Place near MINI1



UMA

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Title: MINI CARD		
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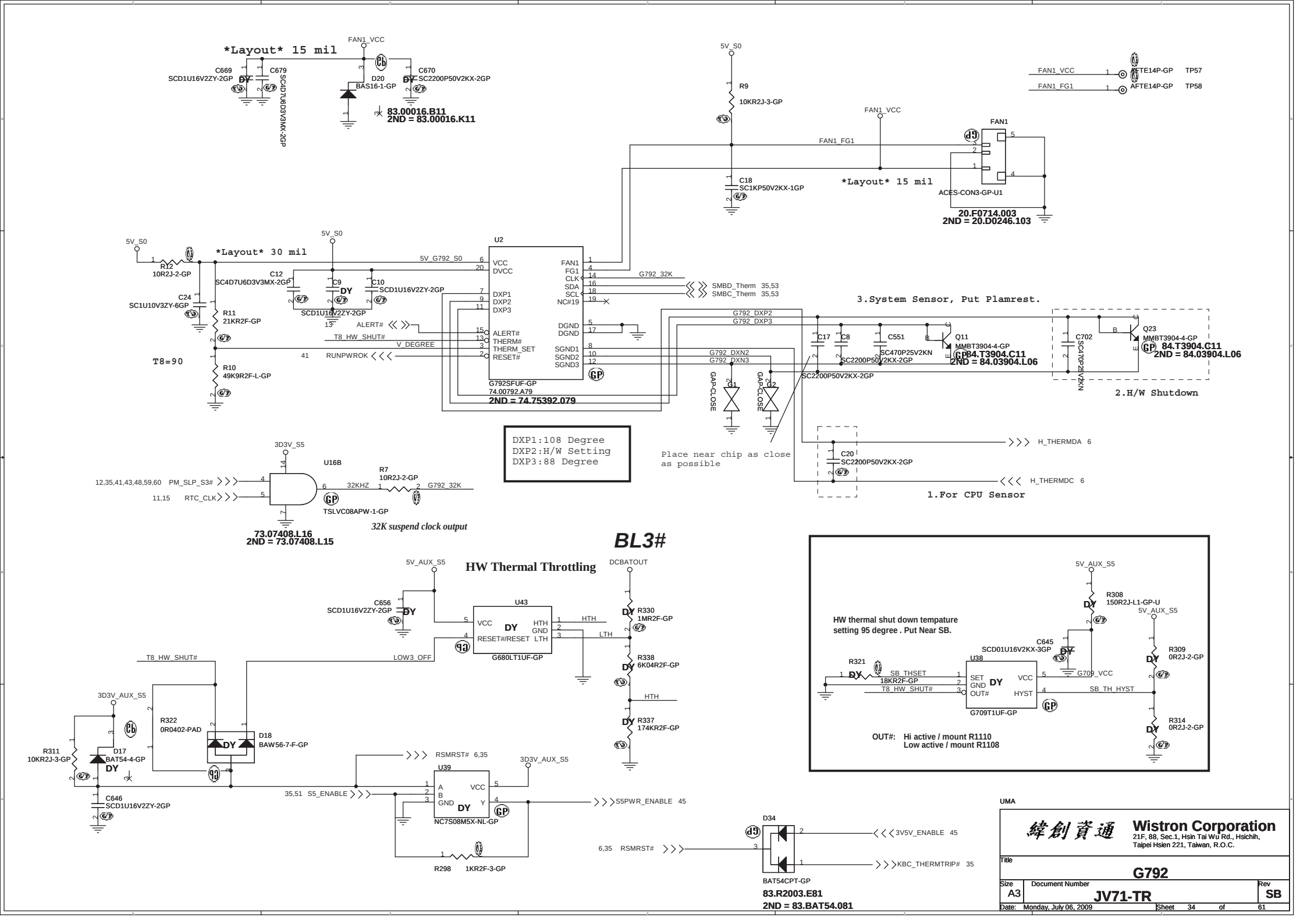

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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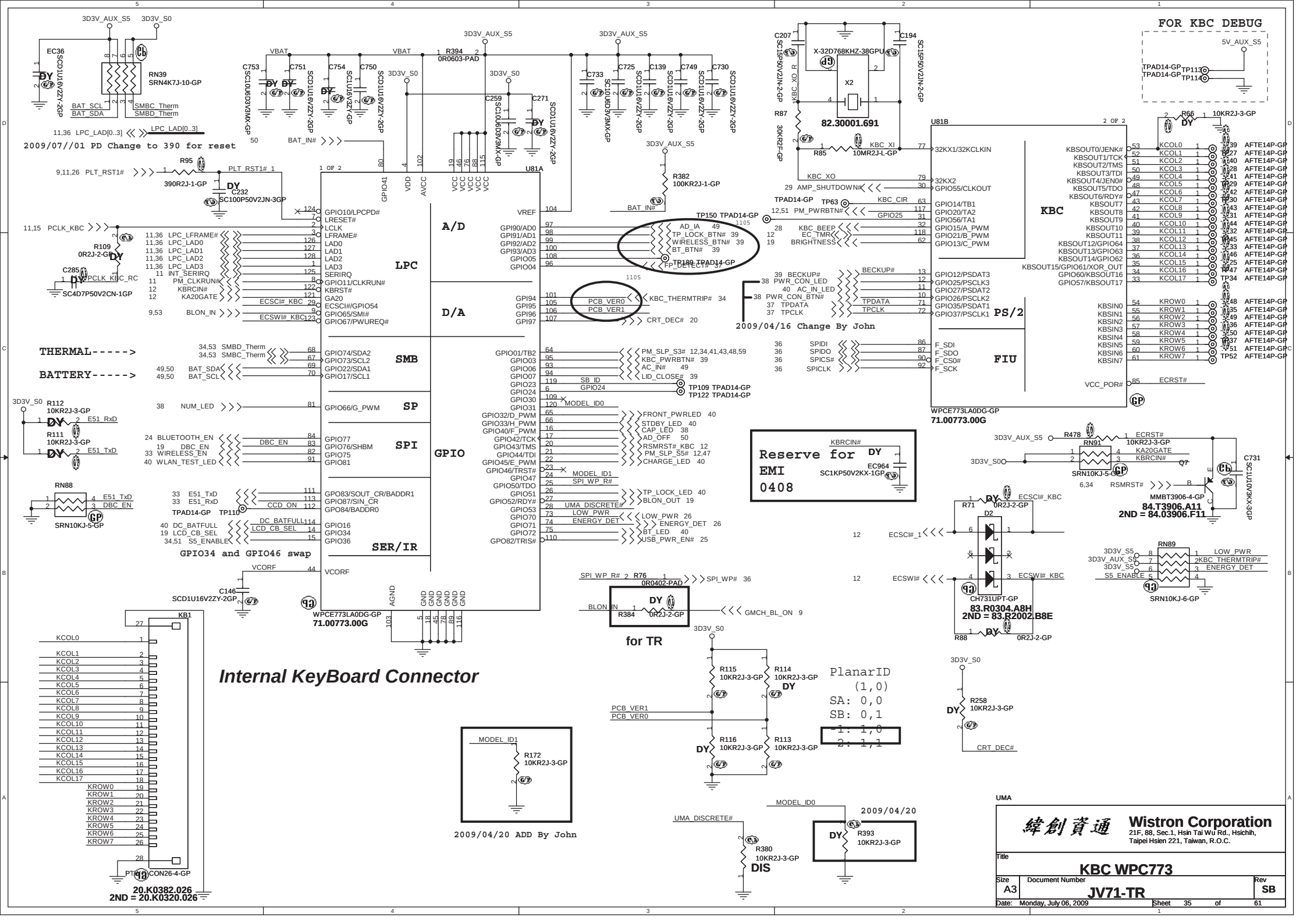
FOR KBC DEBUG
2009/07//01 PD Change to 390 for reset
2009/04/16 Change By John
THERMAL----->
BATTERY----->
GPIO34 and GPIO46 swap
Reserve for EMI 0408
for TR
2009/04/20 ADD By John
PlanarID (1,0)
SA: 0,0
SB: 0,1
-1: 1,0
2: 1,1
Internal KeyBoard Connector
KBC
PS/2
FIU
A/D
D/A
LPC
SMB
SP
SPI
GPIO
SER/IR
U81A
U81B
WPCE773LA0DG-GP
71.00773.00G
82.30001.691
X-32D768KHZ-38GPU
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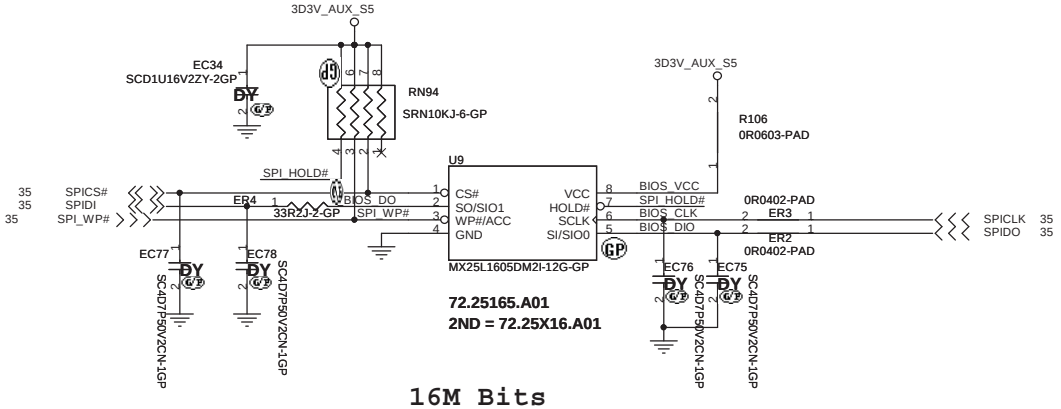
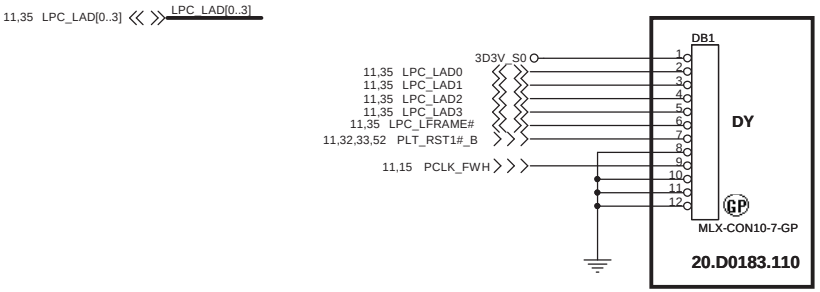
2ND = 84.03906.F11
83.R0304.A8H
2ND = 83.R2002.B8E
20.K0382.026
2ND = 20.K0320.026
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC773
JV71-TR
Monday, July 06, 2009



16M Bits

SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
BIOS		
Size: A3	Document Number: **JV71-TR**	Rev: **SA**
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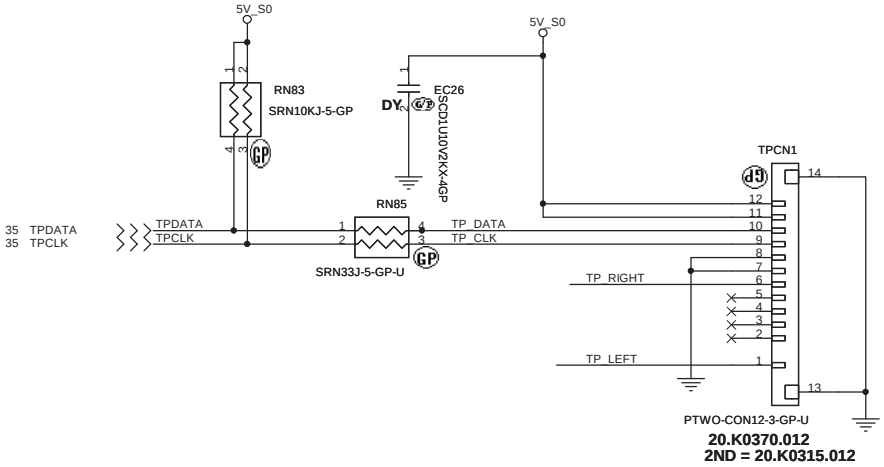
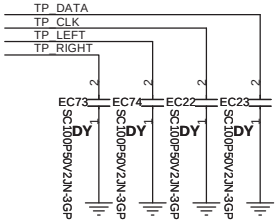
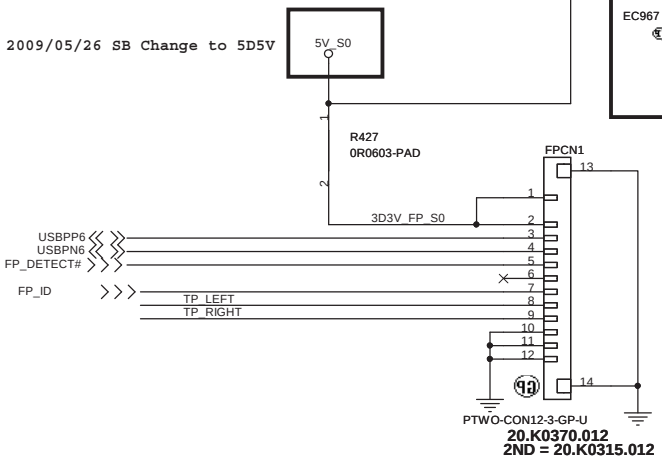
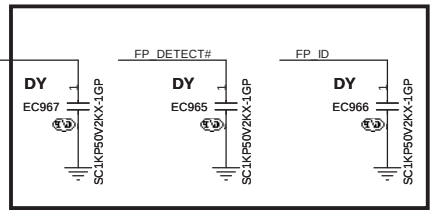
TOUCH PAD

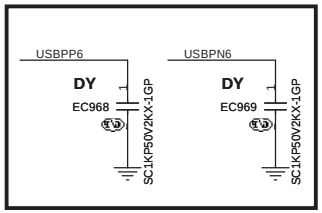




Finger printer







UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Touch PAD/Finger printer		
Size: A3	Document Number: **JV71-TR**	Rev: **SB**
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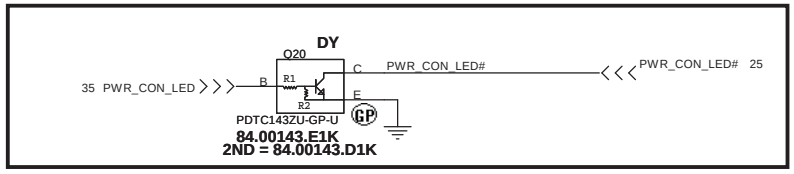
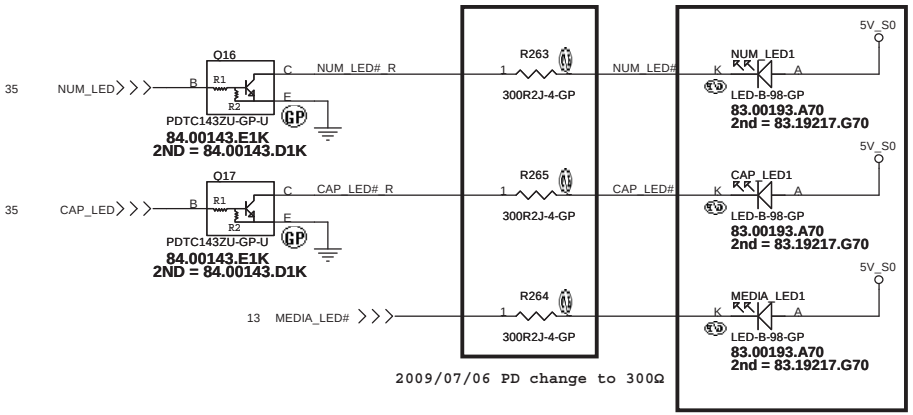
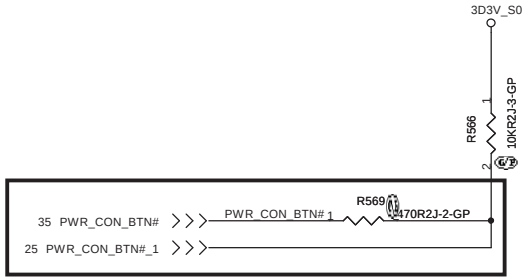
2009/04/16 Change By John

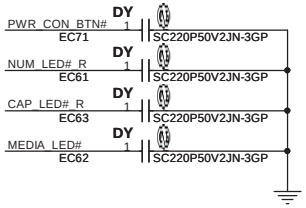




2009/07/06 PD change to 300Ω



2009/04/16 Change By John



緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
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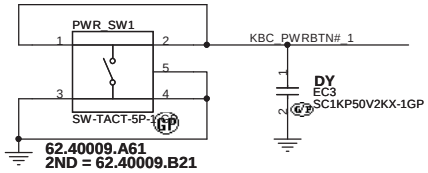
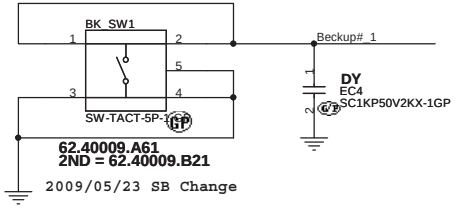
Cover Up Switch

Power Button



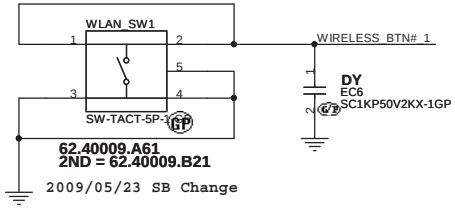
2009/05/23 SB Change

Beckup Button



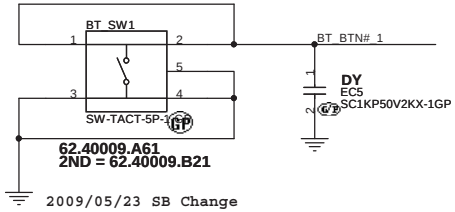
2009/05/23 SB Change

WIRELESS Button

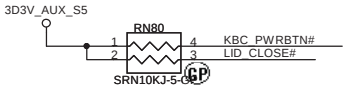


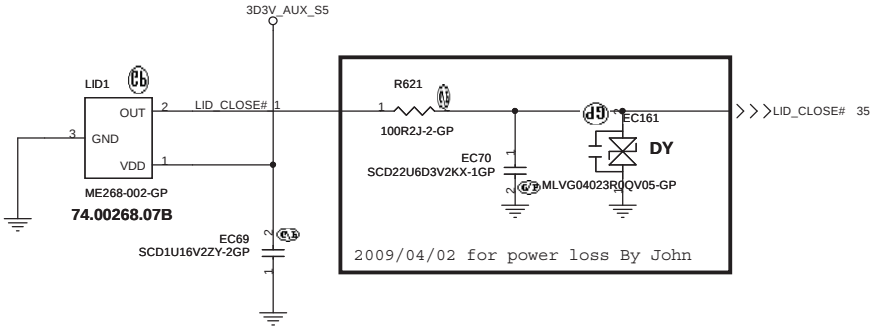
2009/05/23 SB Change

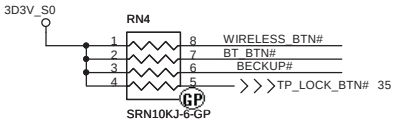
BT/3G Button

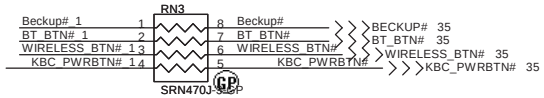


2009/05/23 SB Change

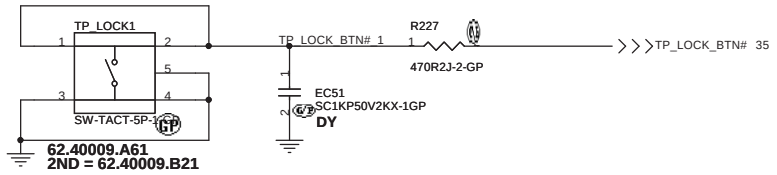








T/P lock Button



2009/05/23 SB Change

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SWITCH		
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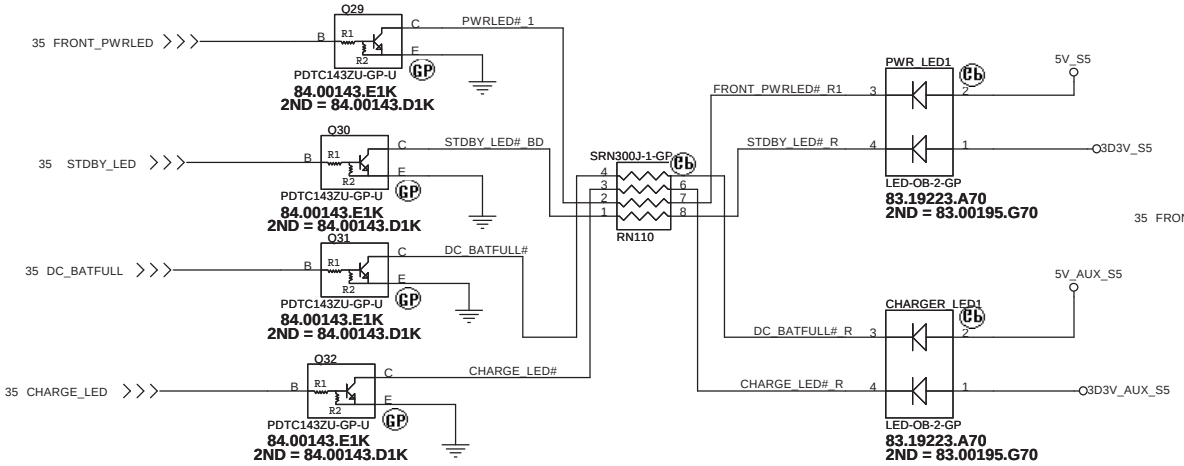

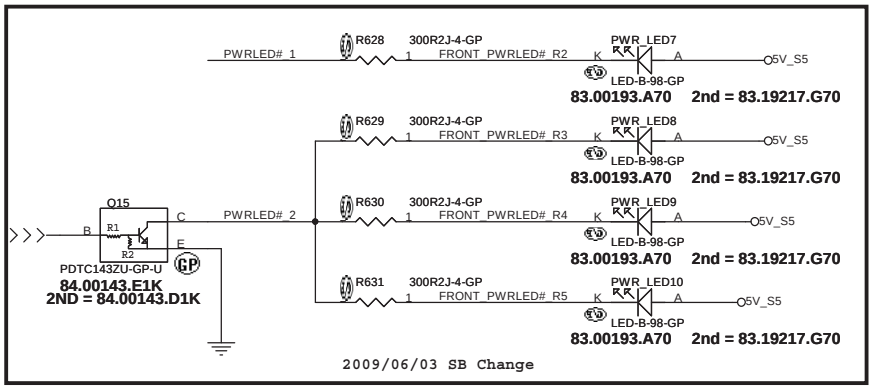

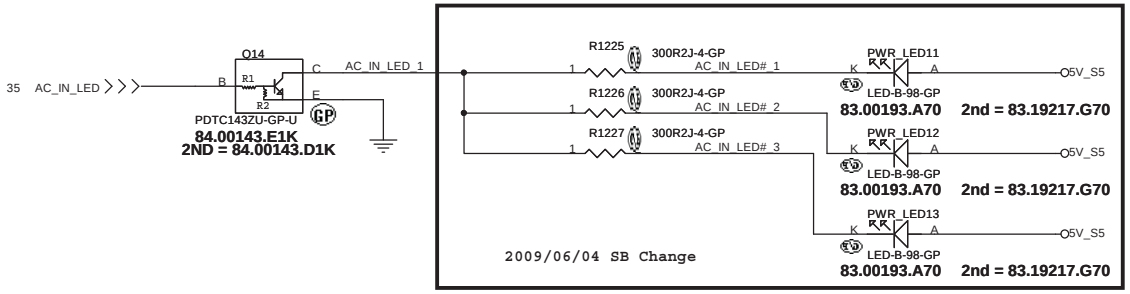

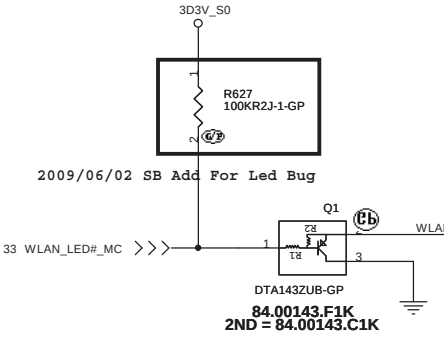

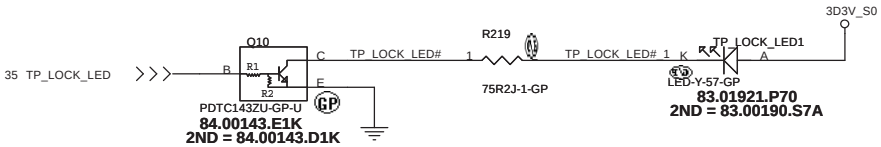

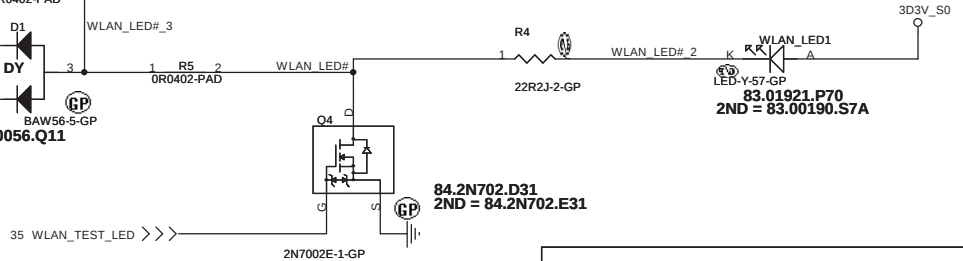

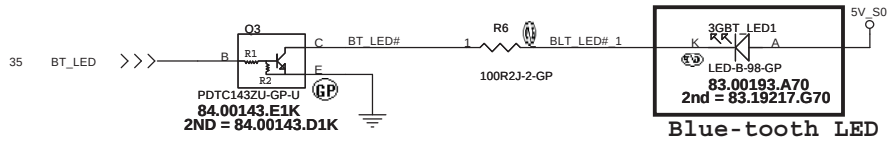

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LED**	
Size: A3	Document Number: **JV71-TR**	Rev: **SB**
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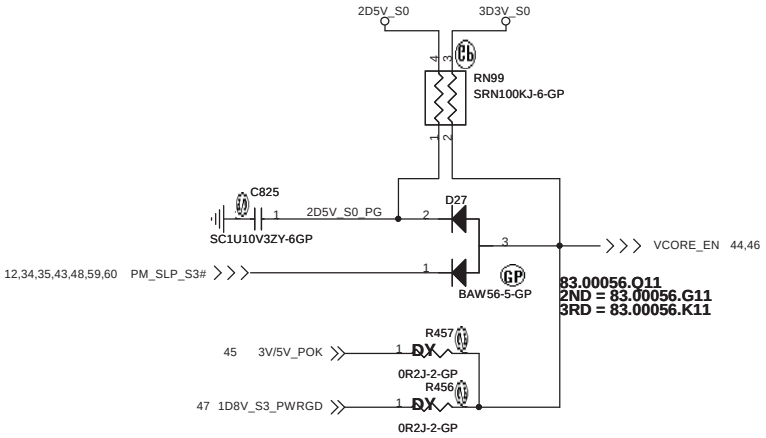
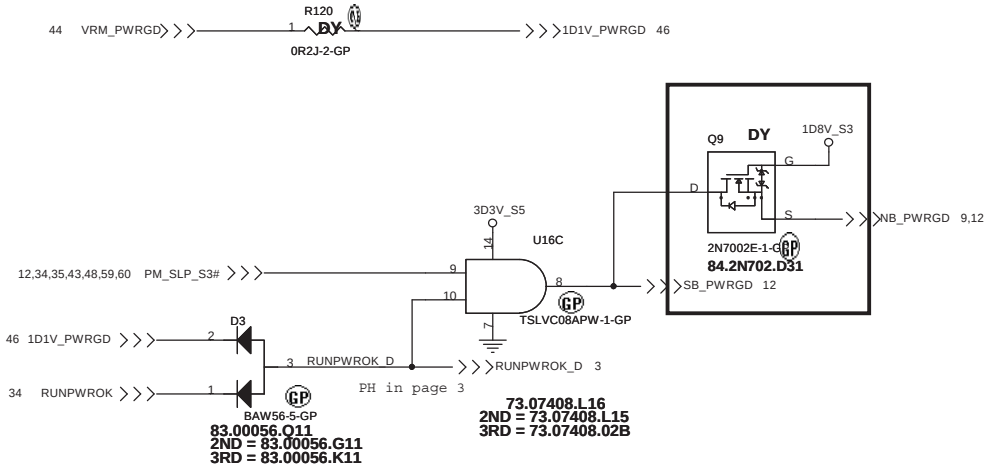


P/H @ 1D8V_S3 PAGE



UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER ON LOGIC**

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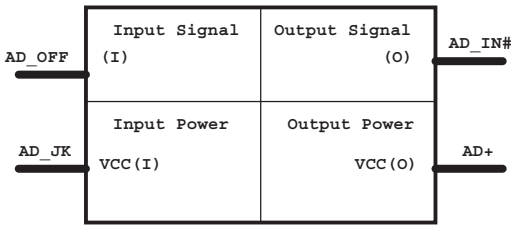
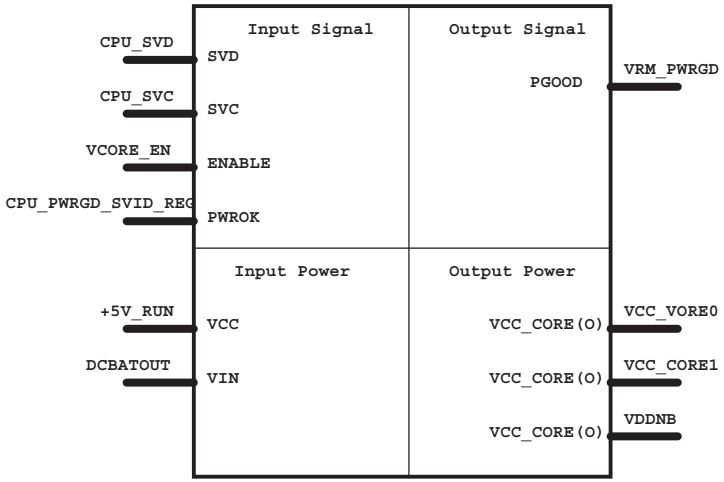
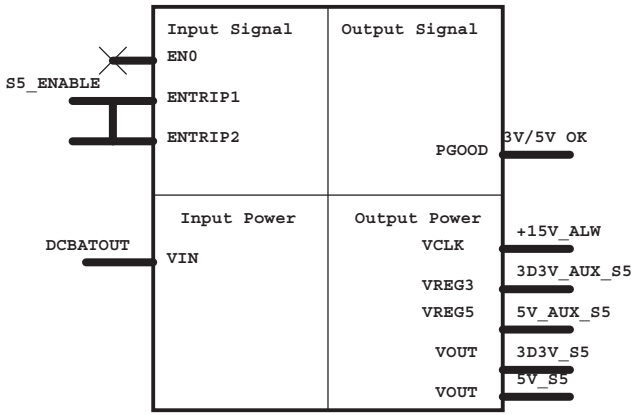
Adapter



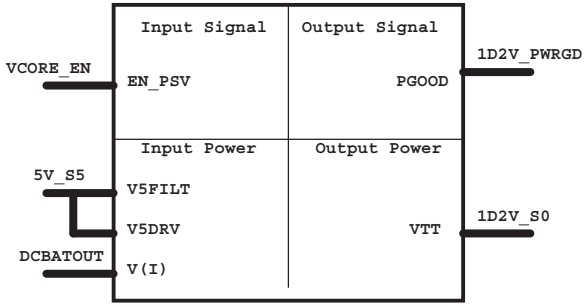
CPU_CORE
ISL6265HRTZ



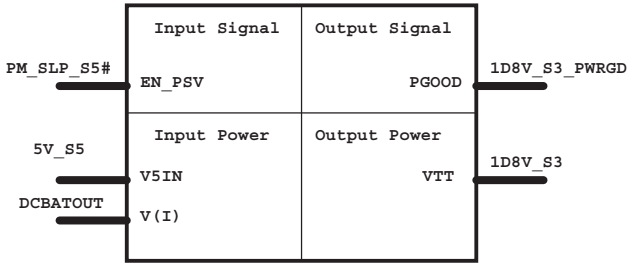
DCDC 5V/3D3V(RT8205A)



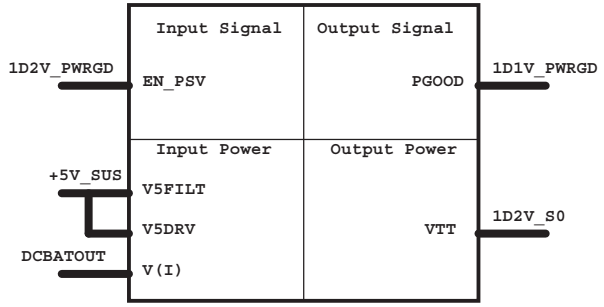
DCDC 1D2V(TPS51124)



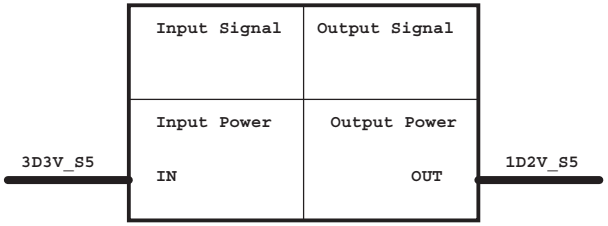
DCDC 1D8V(RT8209B)



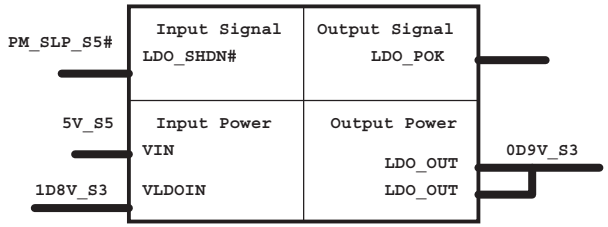
DCDC 1D1V(TPS51124)



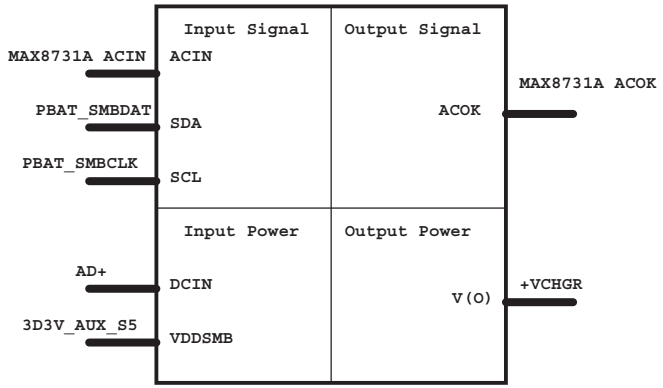
1D2V LDO G9161



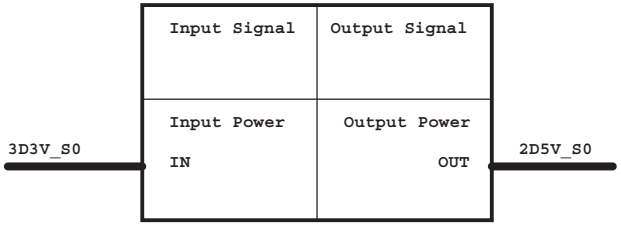
0D9V LDO RT9026



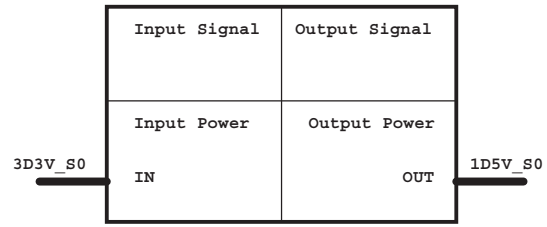
CHARGER MAX8731



2D5V LDO R9161



1D5V LDO G9571



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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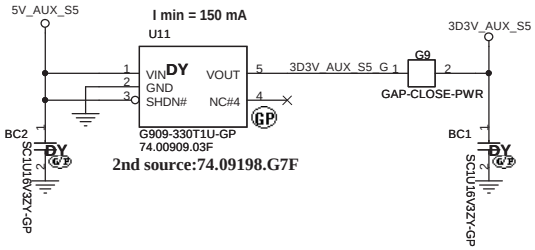
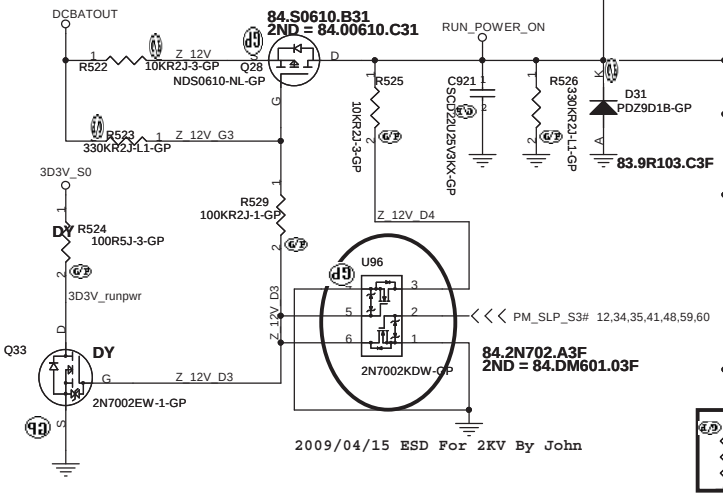
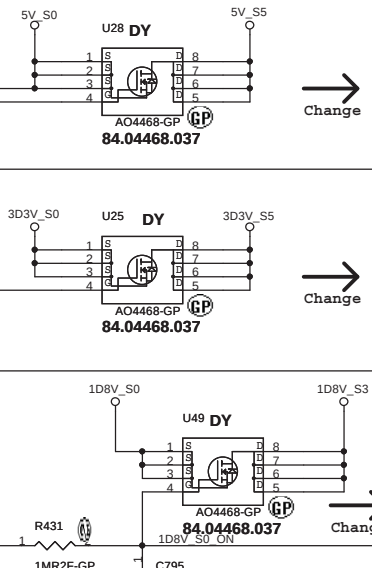
Aux Power 3D3V_AUX_S5



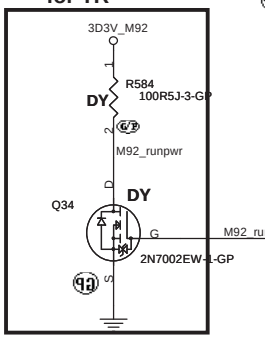
Run Power

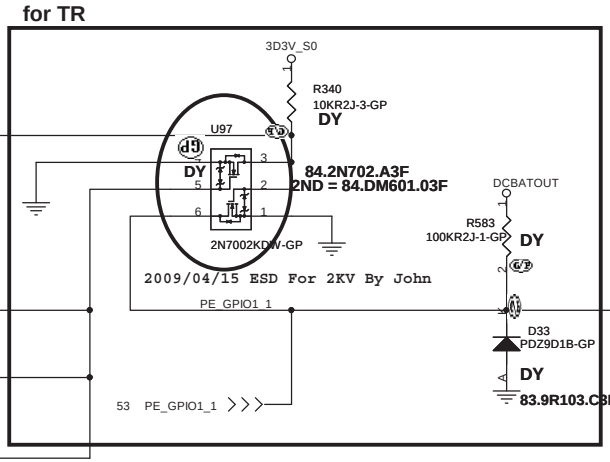


2009/04/15 ESD For 2KV By John

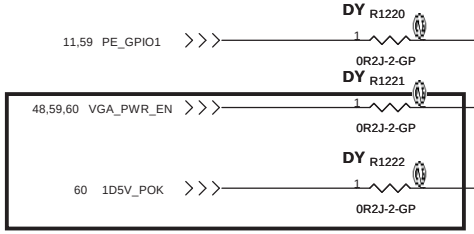


2009/04/21 Change By John

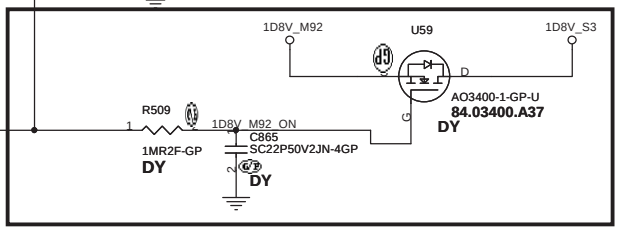


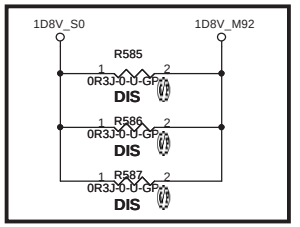


2009/04/15 ESD For 2KV By John



2009/04/21 ADD By John





R509,R342→10MΩ
C865→22pF
C675→1000pF
For VGA sequence issue

UMA

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Title: RUN AND AUX POWER

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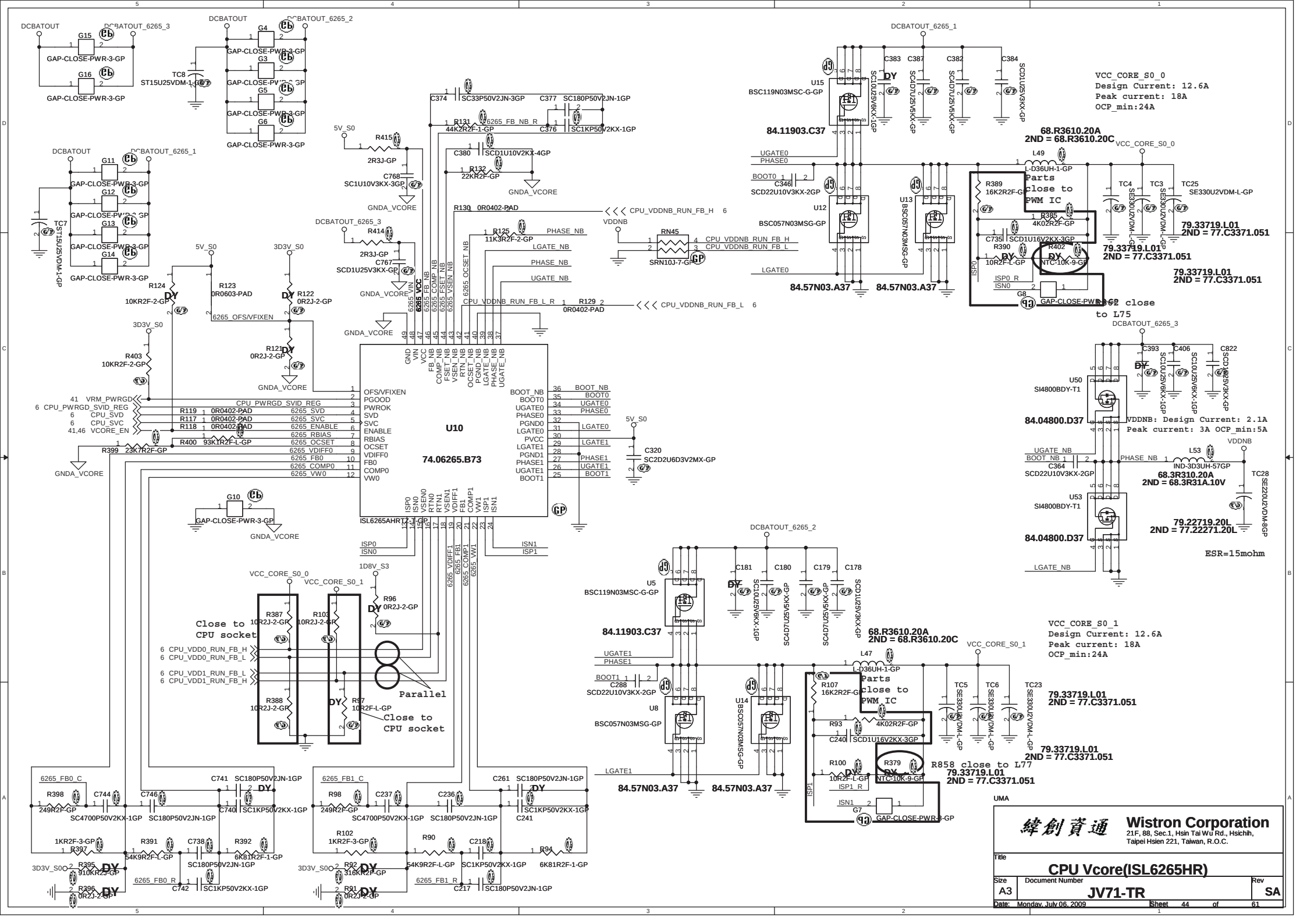
U10
74.06265.B73
ISL6265AHRTZ-T-GP
U15
BSC119N03MSC-G-GP
U12
BSC057N03MSG-GP
U13
BSC057N03MSG-GP
U50
SI4800BDY-T1
U53
SI4800BDY-T1
U5
BSC119N03MSC-G-GP
U8
BSC057N03MSG-GP
U14
BSC057N03MSG-GP
84.11903.C37
84.57N03.A37
84.04800.D37
68.R3610.20A
2ND = 68.R3610.20C
68.R310.20A
2ND = 68.3R31A.10V
79.33719.L01
2ND = 77.C3371.051
79.22719.20L
2ND = 77.22271.20L
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
ESR=15mohm
Parts close to PWM IC
Close to CPU socket
Parallel
R858 close to L77
R82 close to L75
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JV71-TR
Monday, July 06, 2009
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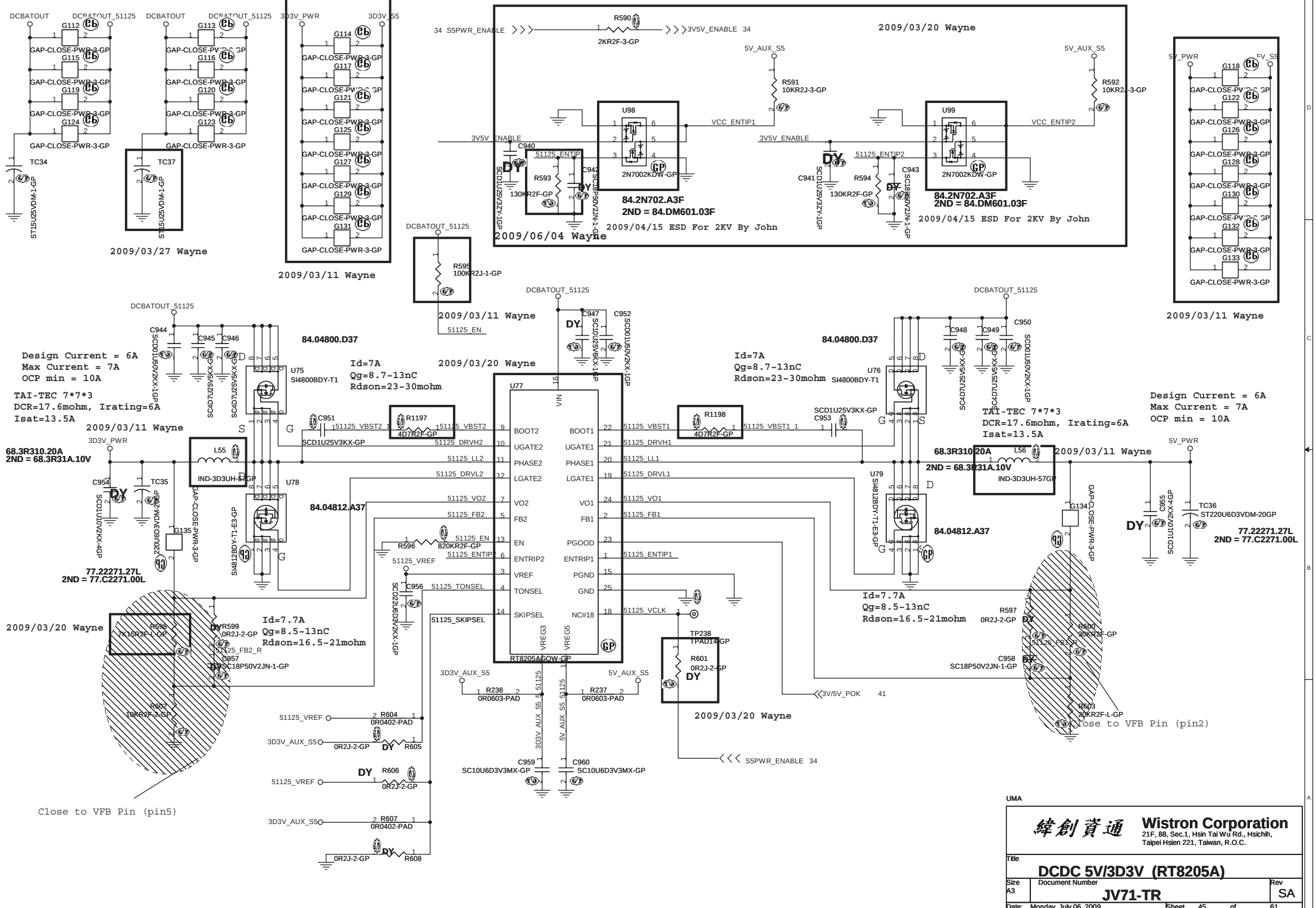
DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_PWR
5V_S5
5V_AUX_S5
3V5V_ENABLE
34 S5PWR_ENABLE
3V5V_ENABLE 34
VCC_ENTIP1
VCC_ENTIP2
51125_ENTIP
51125_ENTIP2
51125_EN
2009/03/20 Wayne
2009/03/27 Wayne
2009/03/11 Wayne
2009/06/04 Wayne
2009/04/15 ESD For 2KV By John
84.2N702.A3F
2ND = 84.DM601.03F
84.04800.D37
84.04812.A37
Design Current = 6A
Max Current = 7A
OCP min = 10A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
TAI-TEC 7*7*3
DCR=17.6mohm, Irating=6A
Isat=13.5A
68.3R310.20A
2ND = 68.3R31A.10V
77.22271.27L
2ND = 77.C2271.00L
U75 SI4800BDY-T1
U76 SI4800BDY-T1
U78 SI4812BDY-T1-E3-GP
U79 SI4812BDY-T1-E3-GP
U77 RT8205AGQW-GP
BOOT2 UGATE2 PHASE2 LGATE2 VO2 FB2 EN ENTRIP2 VREF TONSEL SKIPSEL
BOOT1 UGATE1 PHASE1 LGATE1 VO1 FB1 PGOOD ENTRIP1 PGND GND NC#18 VIN VREG3 VREG5
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_VREF
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_VCLK
3V/5V_POK 41
S5PWR_ENABLE 34
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V (RT8205A)
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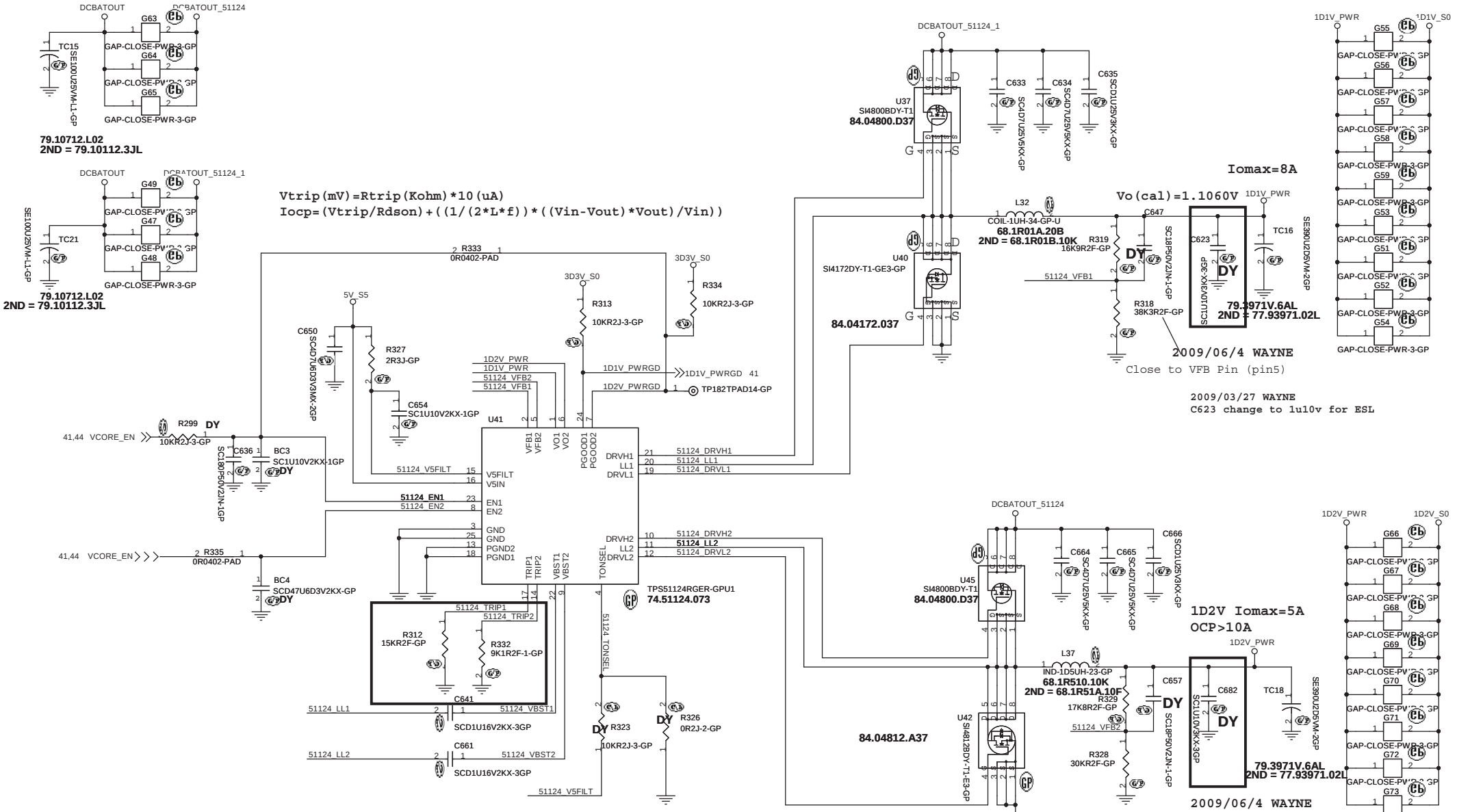

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	**300k/CH1** **360k/CH2**	360k/CH1 420k/CH2

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51124_1D1V_1D2V***

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A3	**JV71-TR**	**SA**

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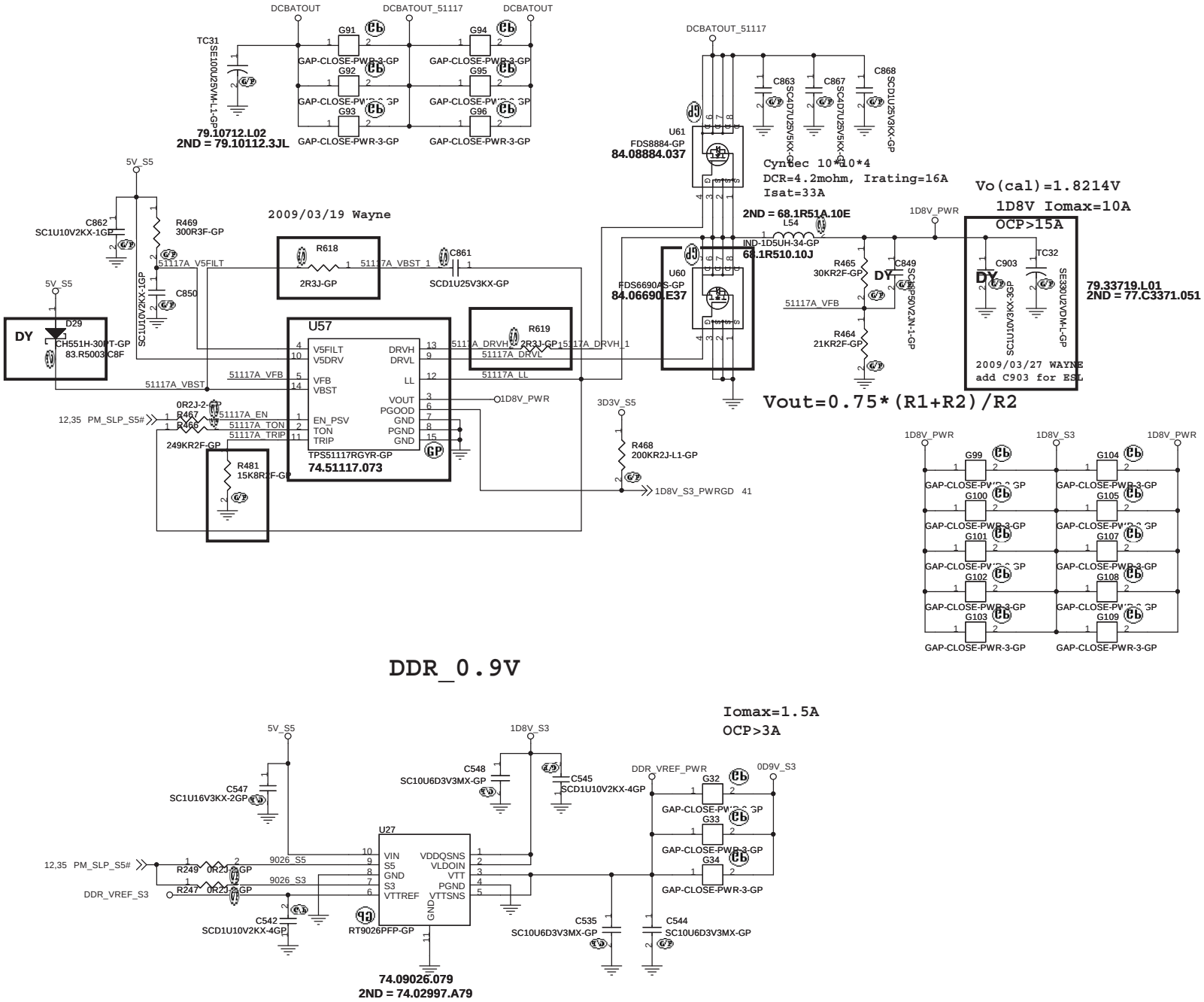

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DCDC_1D8V_APW7141/LDO 0D9V	
Size: A3	Document Number: JV71-TR	Rev: SA
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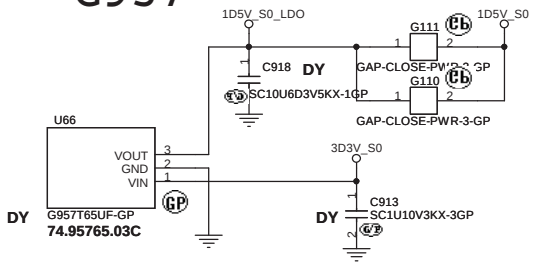
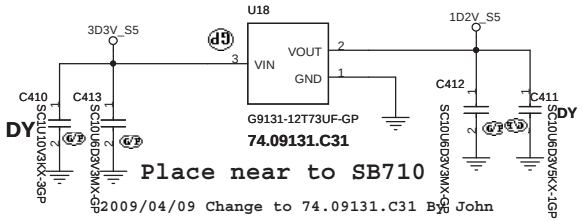
1D5V_S0
Iomax=1A

G957



For MINI Card.NEW Card power SW

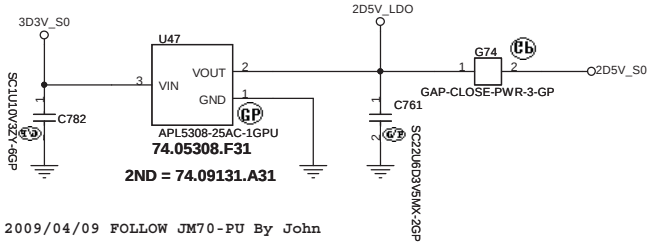
1D2V_S5
Iomax=400mA



Place near to SB710

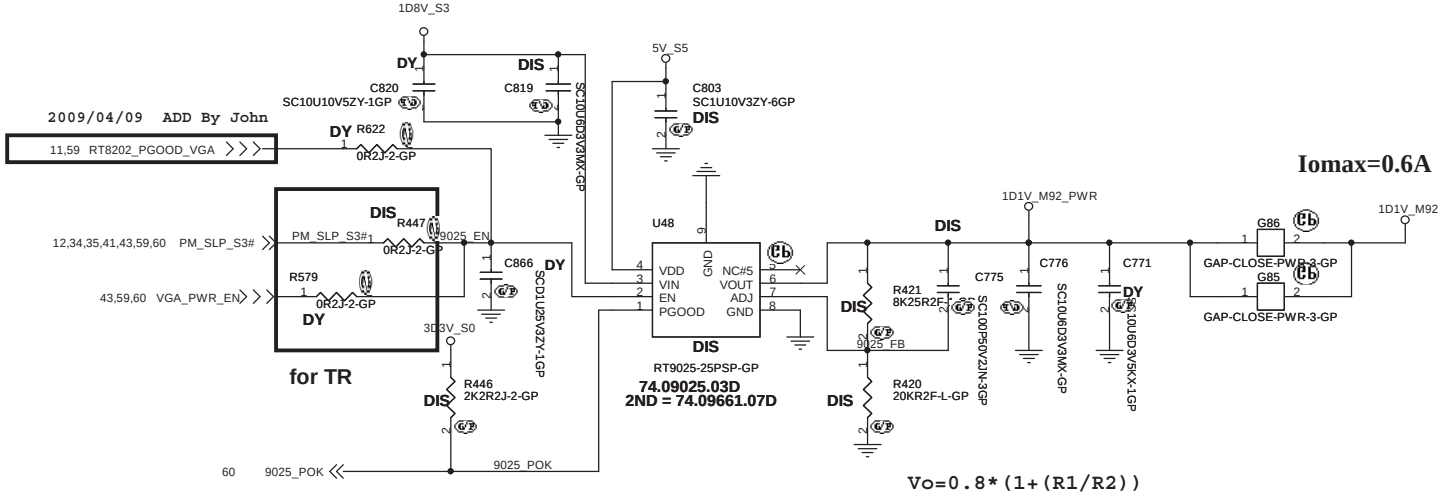
2009/04/09 Change to 74.09131.C31 By John

2D5V
Iomax=0.2A



2009/04/09 FOLLOW JM70-PU By John

Place near to CPU



Iomax=0.6A

Vo=0.8*(1+(R1/R2))

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 2D5V/1D5V/1D2V_S5/1D1V_M92

Size: A3 | Document Number: JV71-TR | Rev: SA

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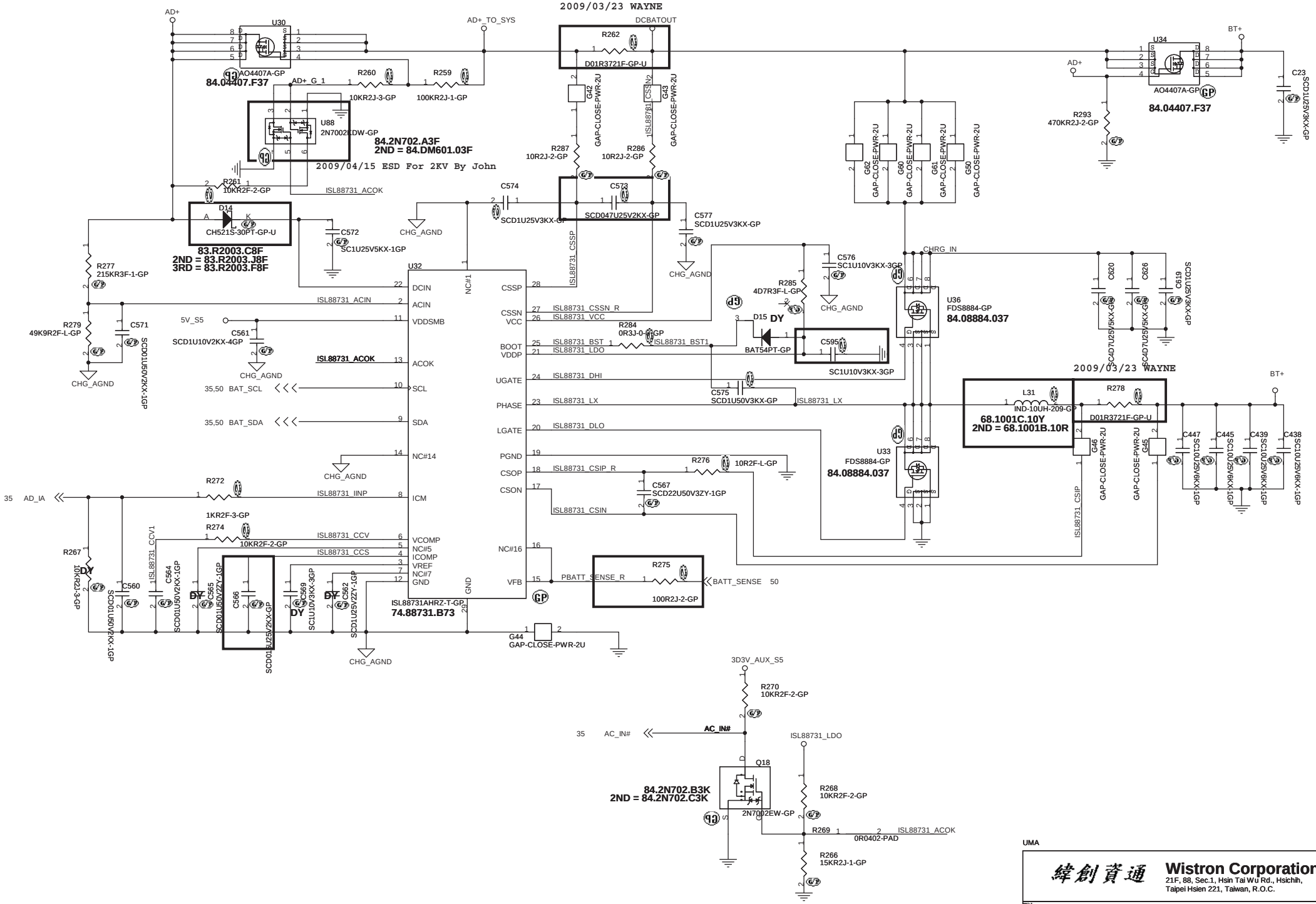

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ISL88731A Charger***

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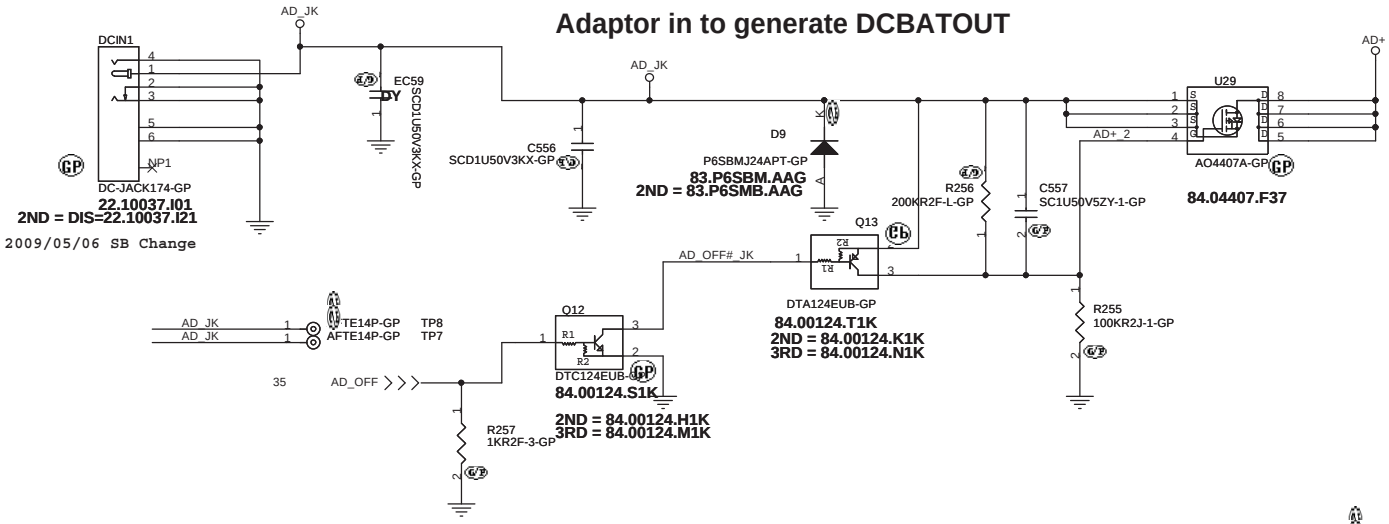
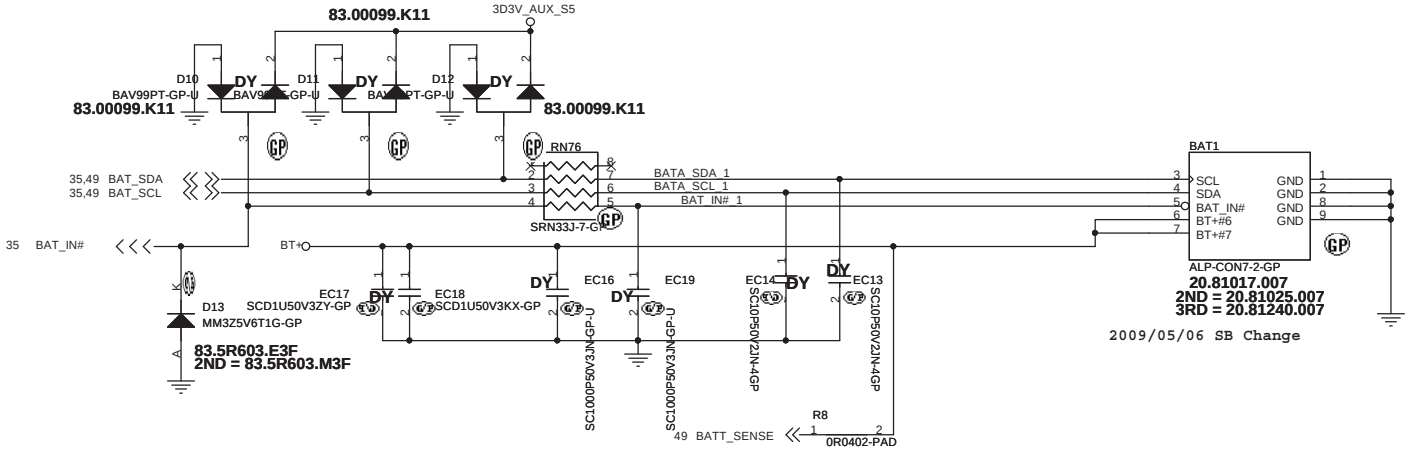
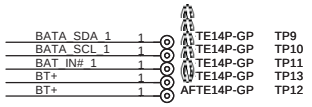
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR





UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size	Document Number: JV71-TR	Rev: SB
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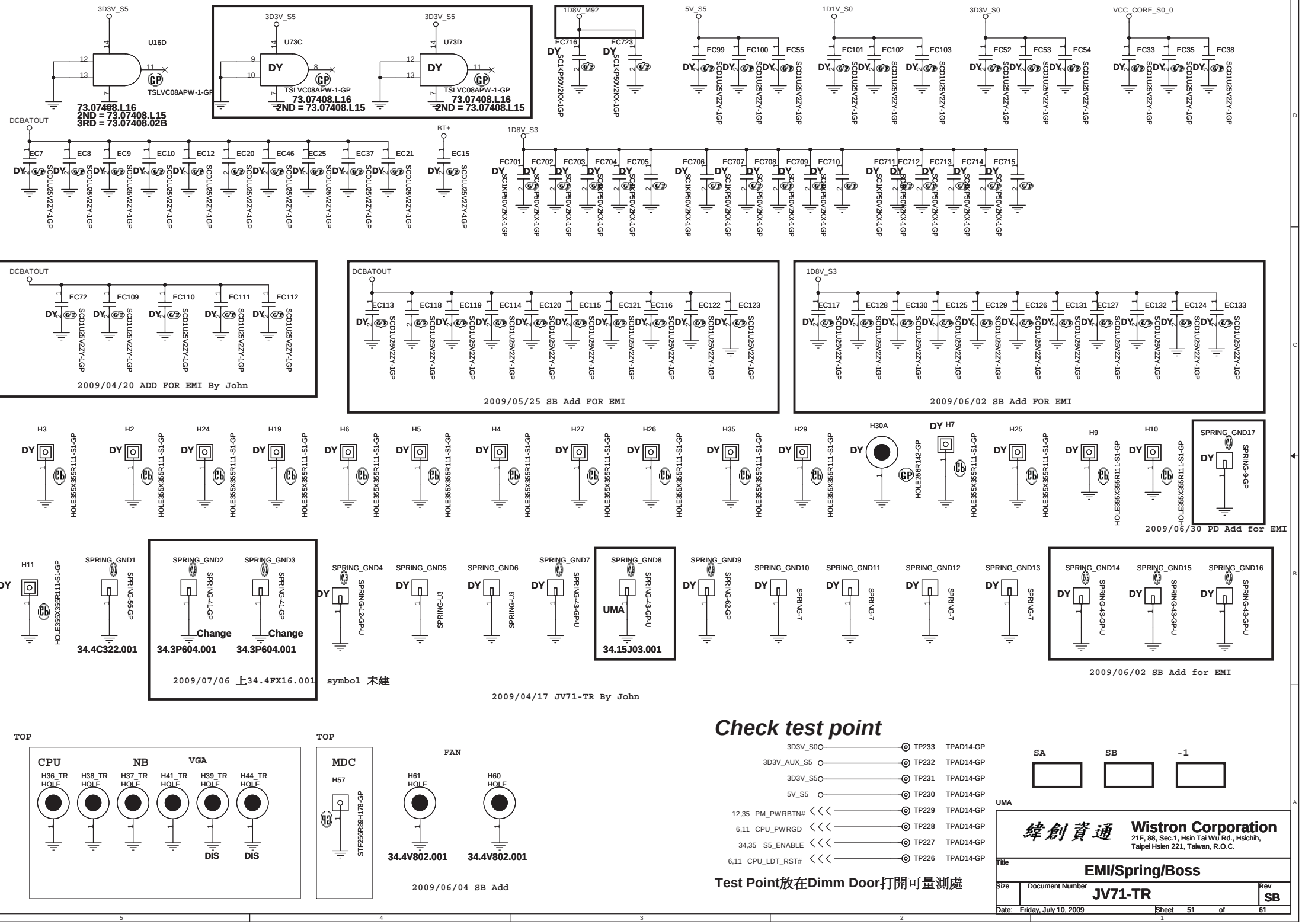
3D3V_S5
U16D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
U73C
U73D
1D8V_M92
5V_S5
1D1V_S0
3D3V_S0
VCC_CORE_S0_0
DCBATOUT
BT+
1D8V_S3
2009/04/20 ADD FOR EMI By John
2009/05/25 SB Add FOR EMI
2009/06/02 SB Add FOR EMI
2009/06/30 PD Add for EMI
2009/07/06 上34.4FX16.001 symbol 未建
2009/04/17 JV71-TR By John
2009/06/02 SB Add for EMI
34.4C322.001
34.3P604.001
34.15J03.001
UMA
Check test point
3D3V_S0 TP233 TPAD14-GP
3D3V_AUX_S5 TP232 TPAD14-GP
3D3V_S5 TP231 TPAD14-GP
5V_S5 TP230 TPAD14-GP
12,35 PM_PWRBTN# TP229 TPAD14-GP
6,11 CPU_PWRGD TP228 TPAD14-GP
34,35 S5_ENABLE TP227 TPAD14-GP
6,11 CPU_LDT_RST# TP226 TPAD14-GP
Test Point放在Dimm Door打開可量測處
TOP
CPU
NB
VGA
DIS
MDC
FAN
34.4V802.001
2009/06/04 SB Add
SA
SB
-1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
JV71-TR
Rev
SB
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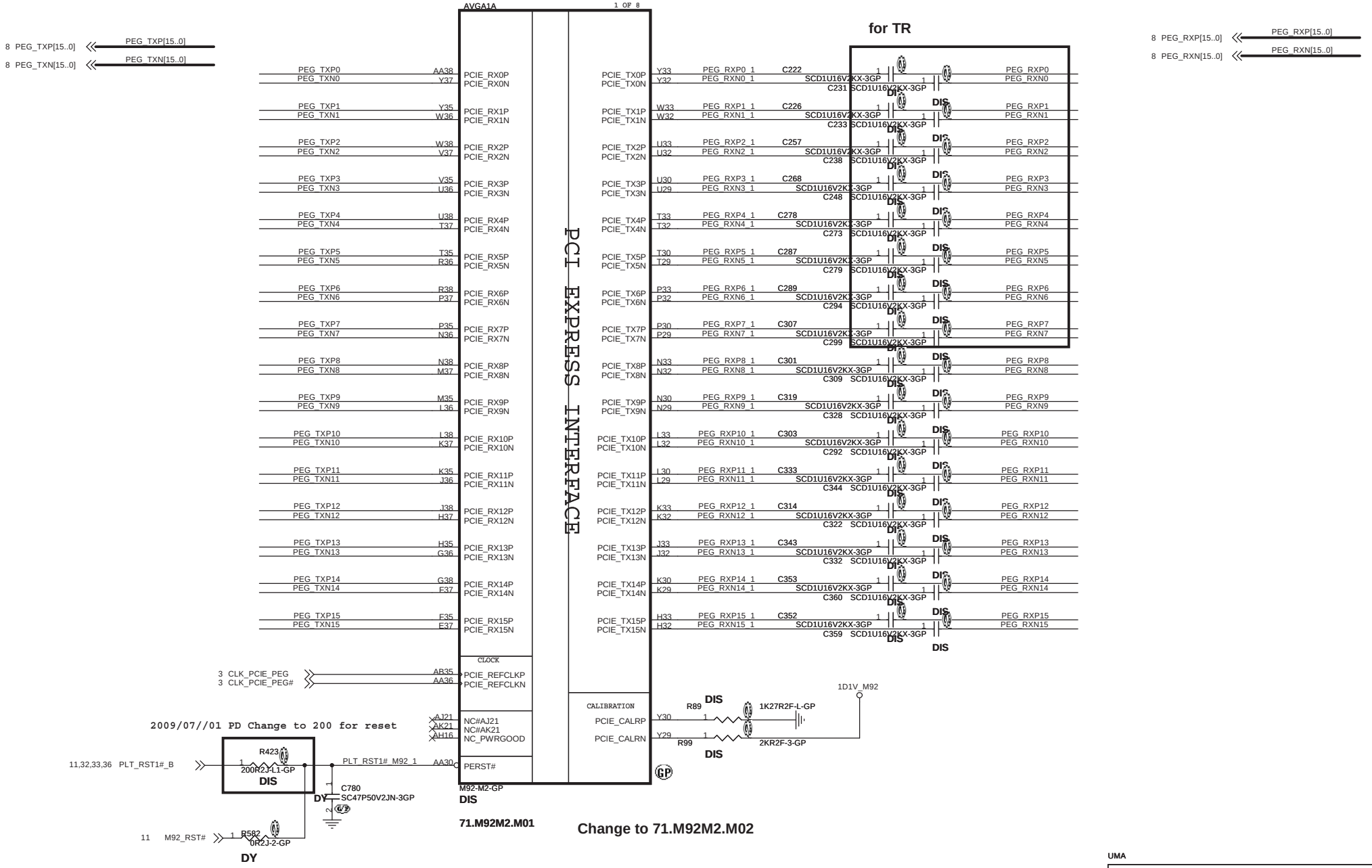

UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **M92 PCIE**		
Size: A3	Document Number: **JV71-TR**	Rev: **SB**
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Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type
selection H/W strap
Should provide VRAM Table for VBios
request

DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)

It's strap for GDDR3-136ball
Need to Clarify

Back Bias (body bias) which minimizes
power consumption in battery modes.
PD = Disable
PU = Enable

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

Depending on OSC used select voltage divider resist
values R25 R70 to ensure XTALIN voltage level of
1.8V

For Thermal sensor

84.2N702.B3K
2ND = 84.2N702.C3K

84.2N702.A3F
2ND = 84.DM601.03F

2009/04/15 ESD For 2KV By John

UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M92 IO

Size: A2 | Document Number: JV71-TR | Rev: SA

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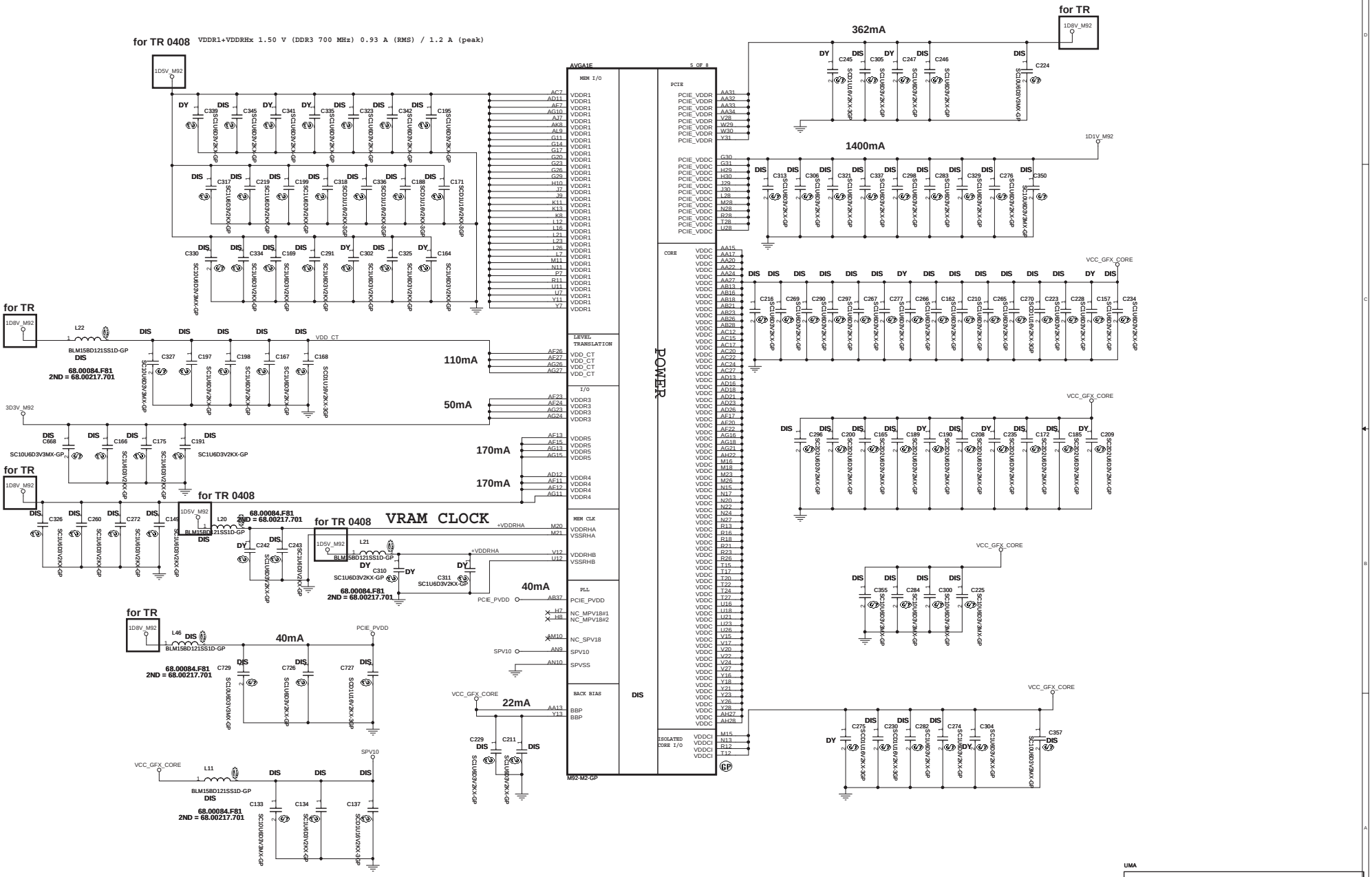

UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 POWER		
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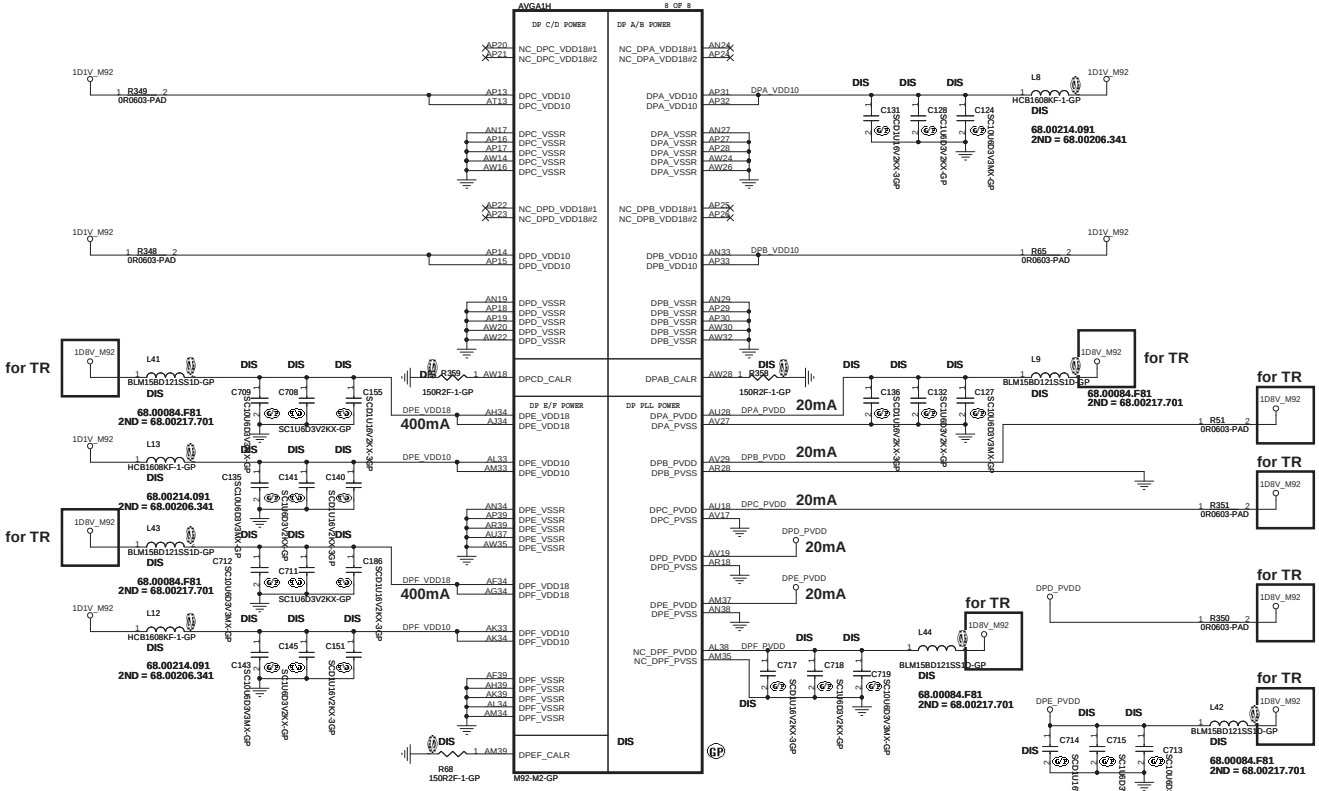

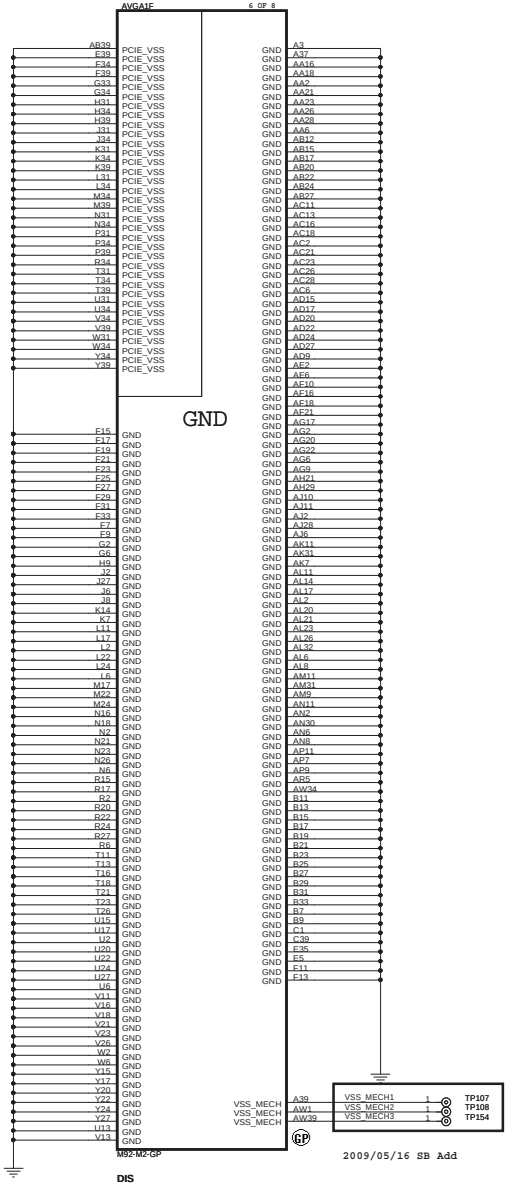

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Title	DP POWER_GND	
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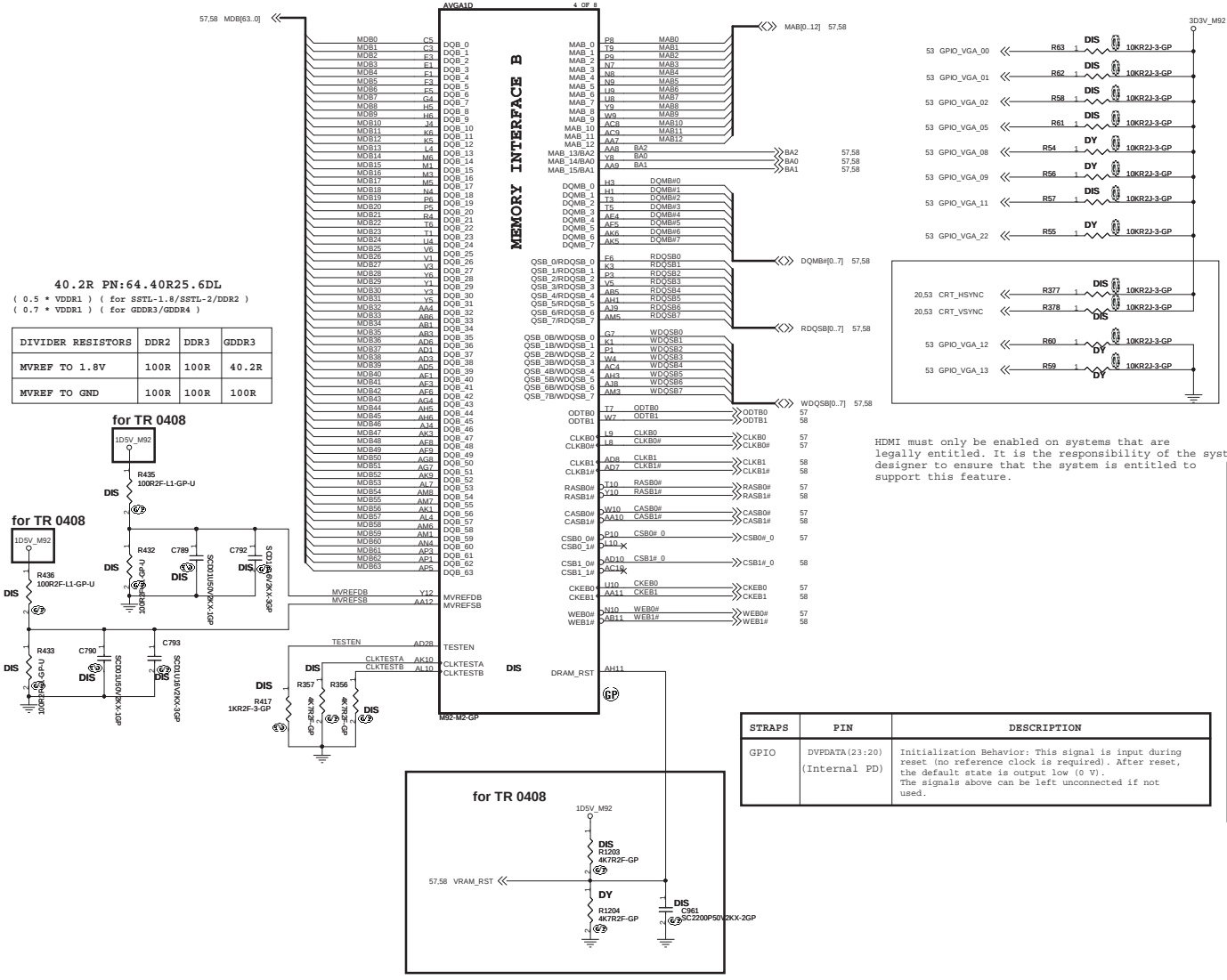
M92-M2 uses memory group B only



HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

40.2R PN:64.40R25.6DL

(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

DIVIDER RESISTORS	DDR2	DDR3	GDDR3
MVREF TO 1.8V	100R	100R	40.2R
MVREF TO GND	100R	100R	100R

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
V 256MB	x001		M25P10A	0101
V 64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x			
2GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
4GB	x		Pm25LV010A	0101

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory aperture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

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Title: Memory / Straps

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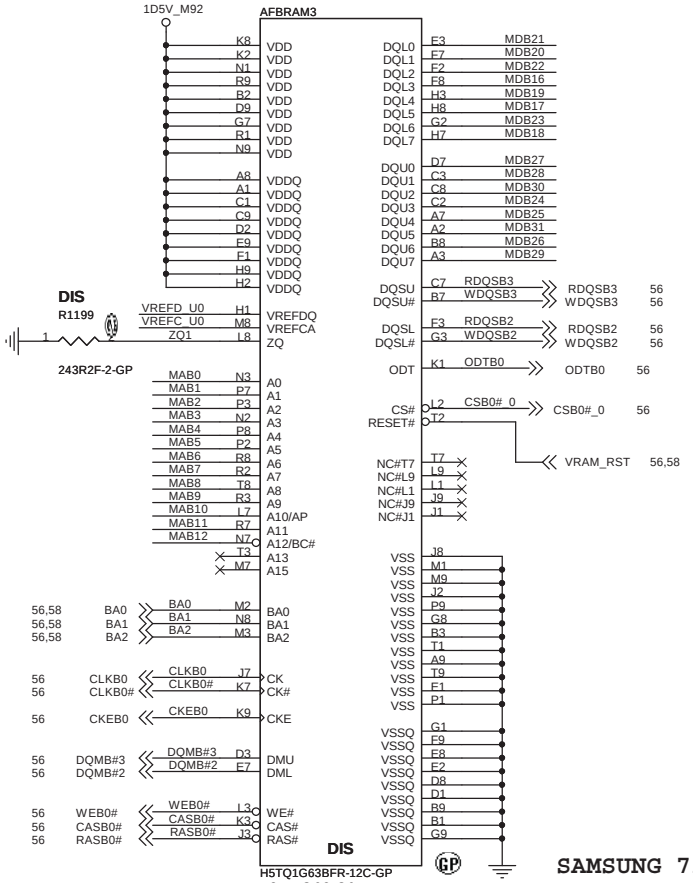
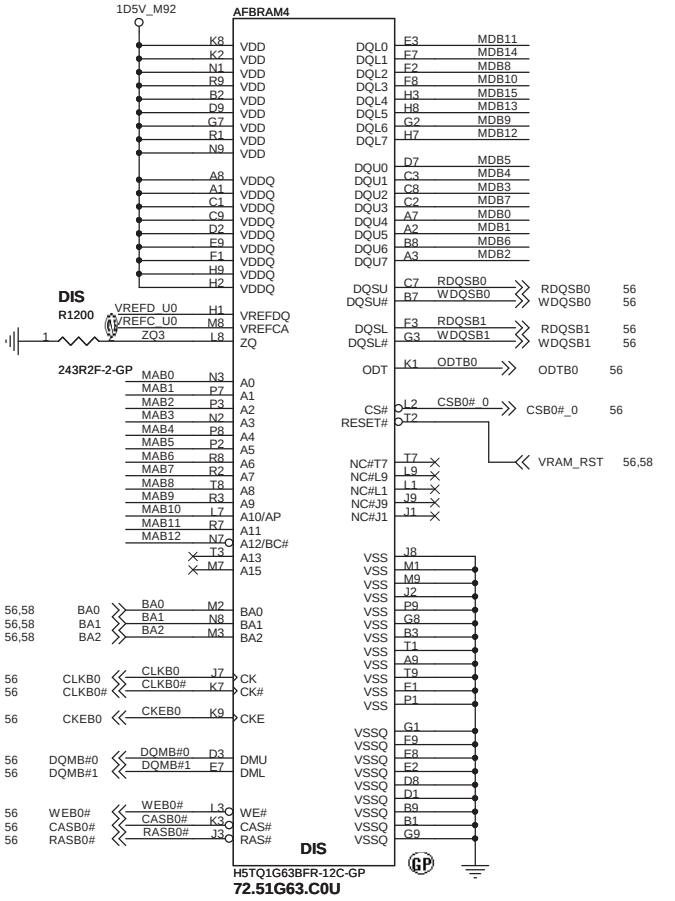
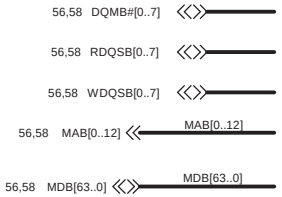
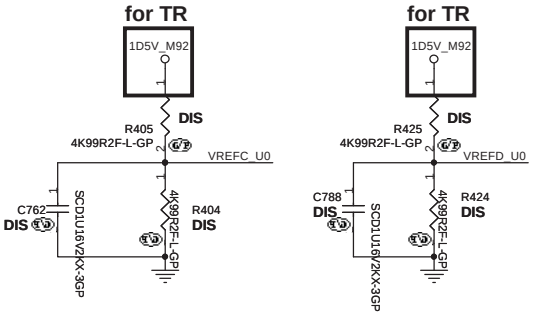
DDR3

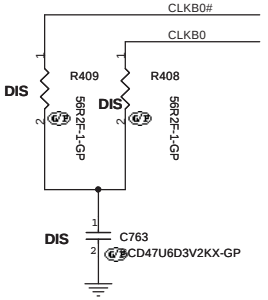


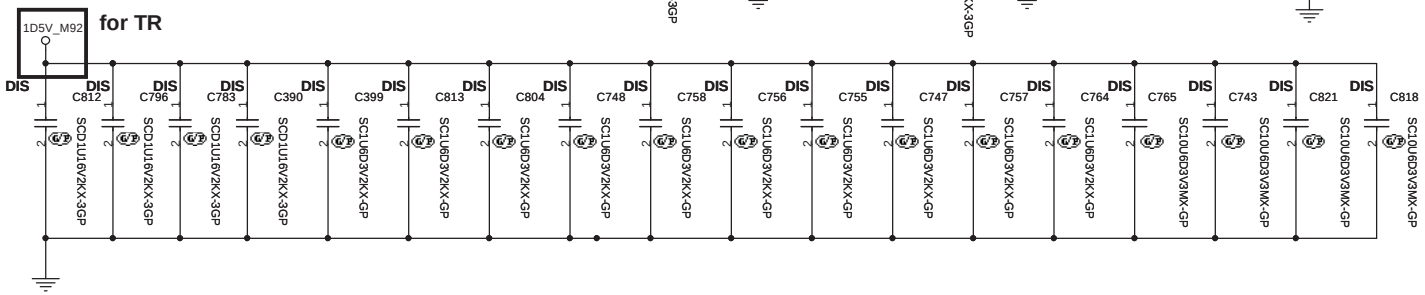


SAMSUNG 72.41164.H0U
HYUNIX 72.51G63.C0U









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Title: DDR3 B0		
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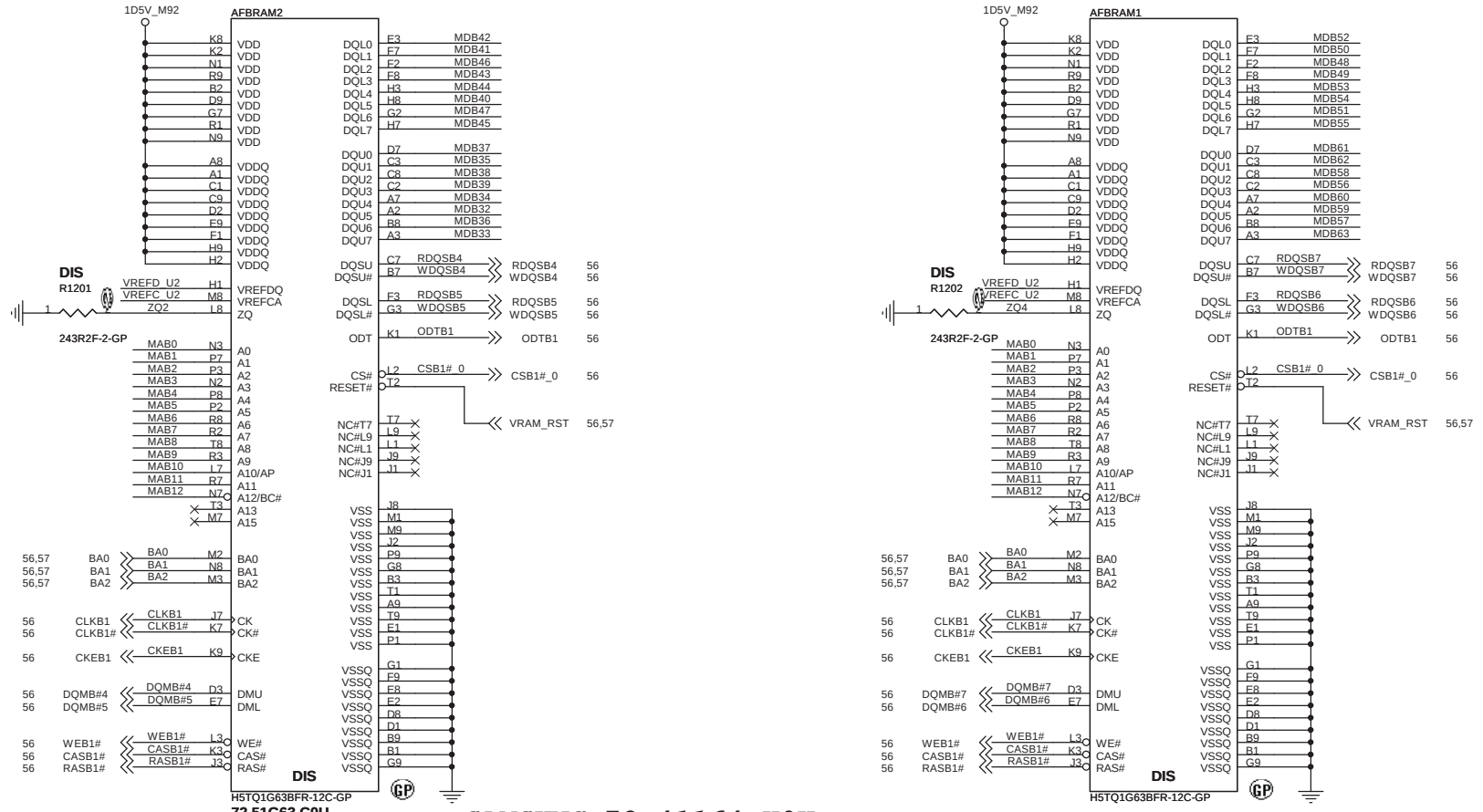
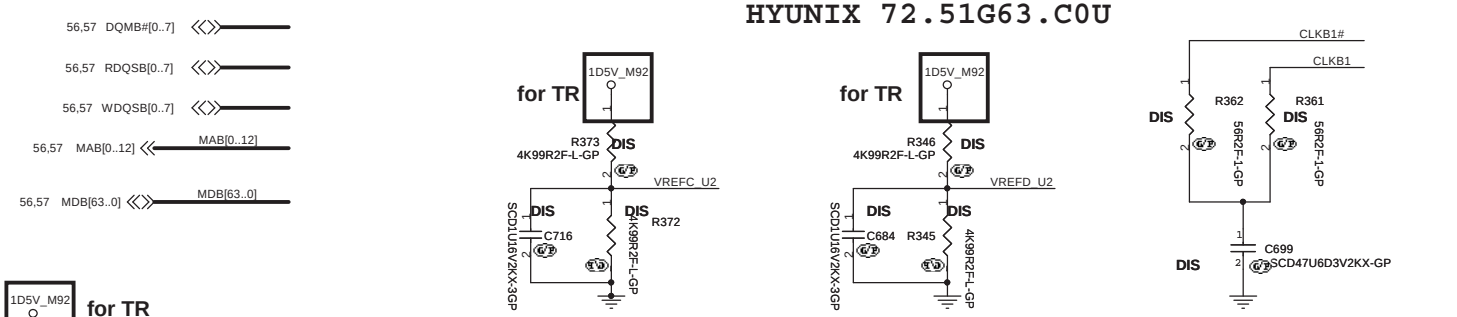
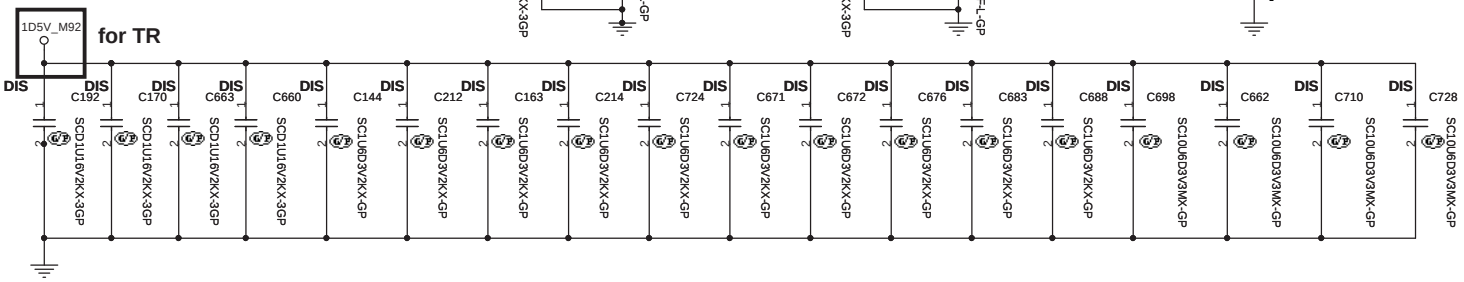


SAMSUNG 72.41164.H0U
HYUNIX 72.51G63.C0U





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Title: M92 DDR3 B1		
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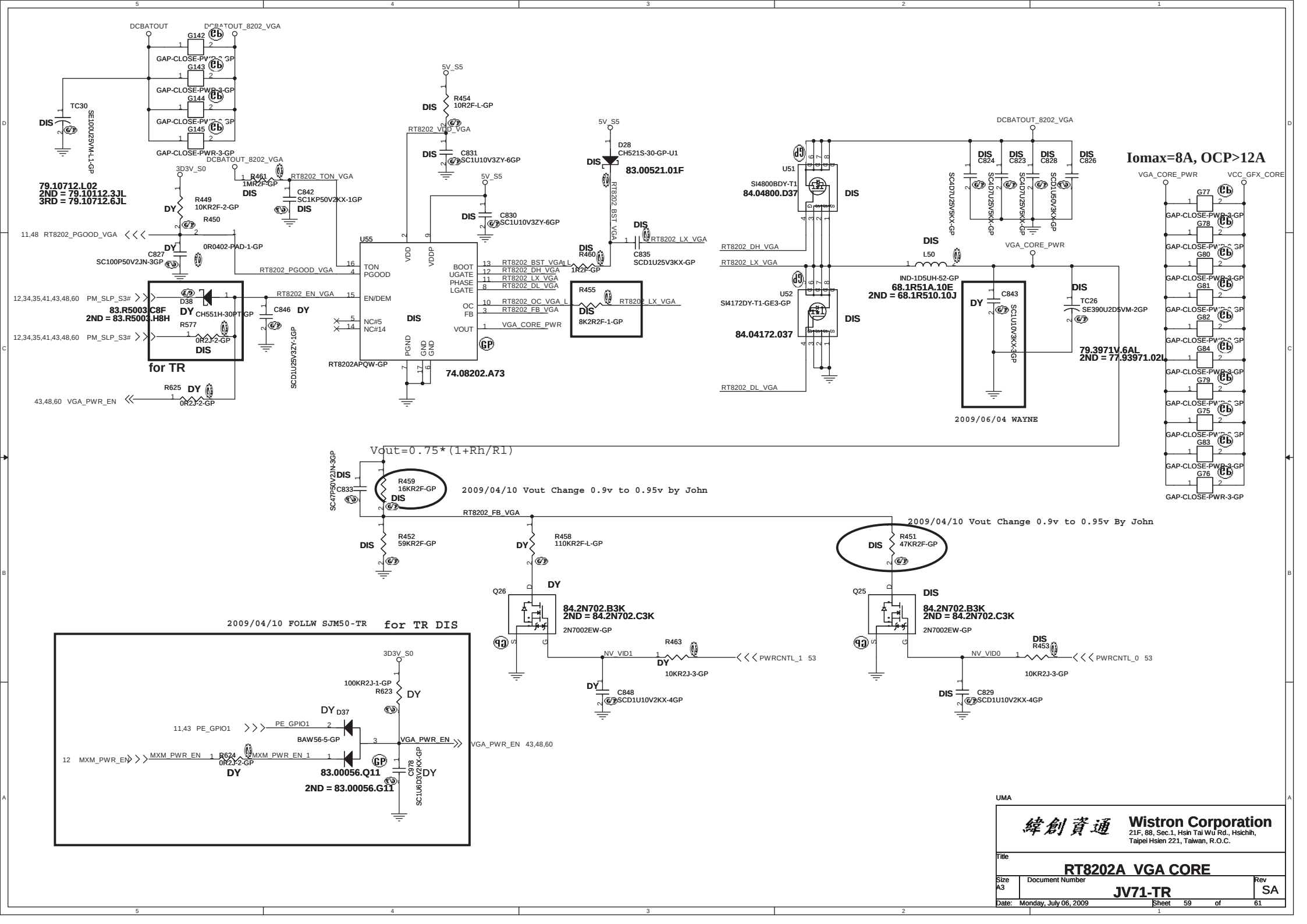

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Title: **RT8202A VGA CORE**

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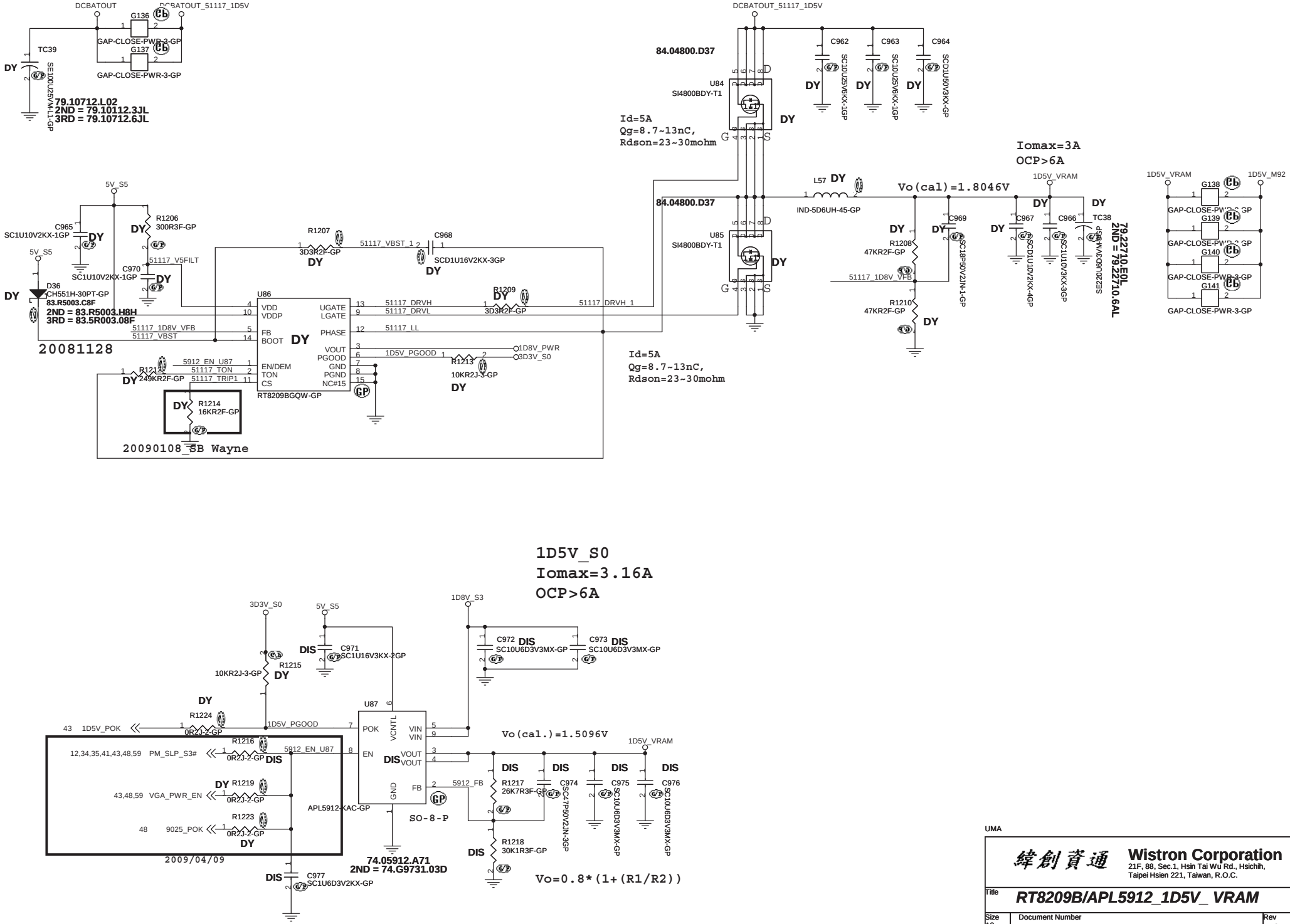

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Title	***RT8209B/APL5912_1D5V_ VRAM***	
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Title

HISTORY

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