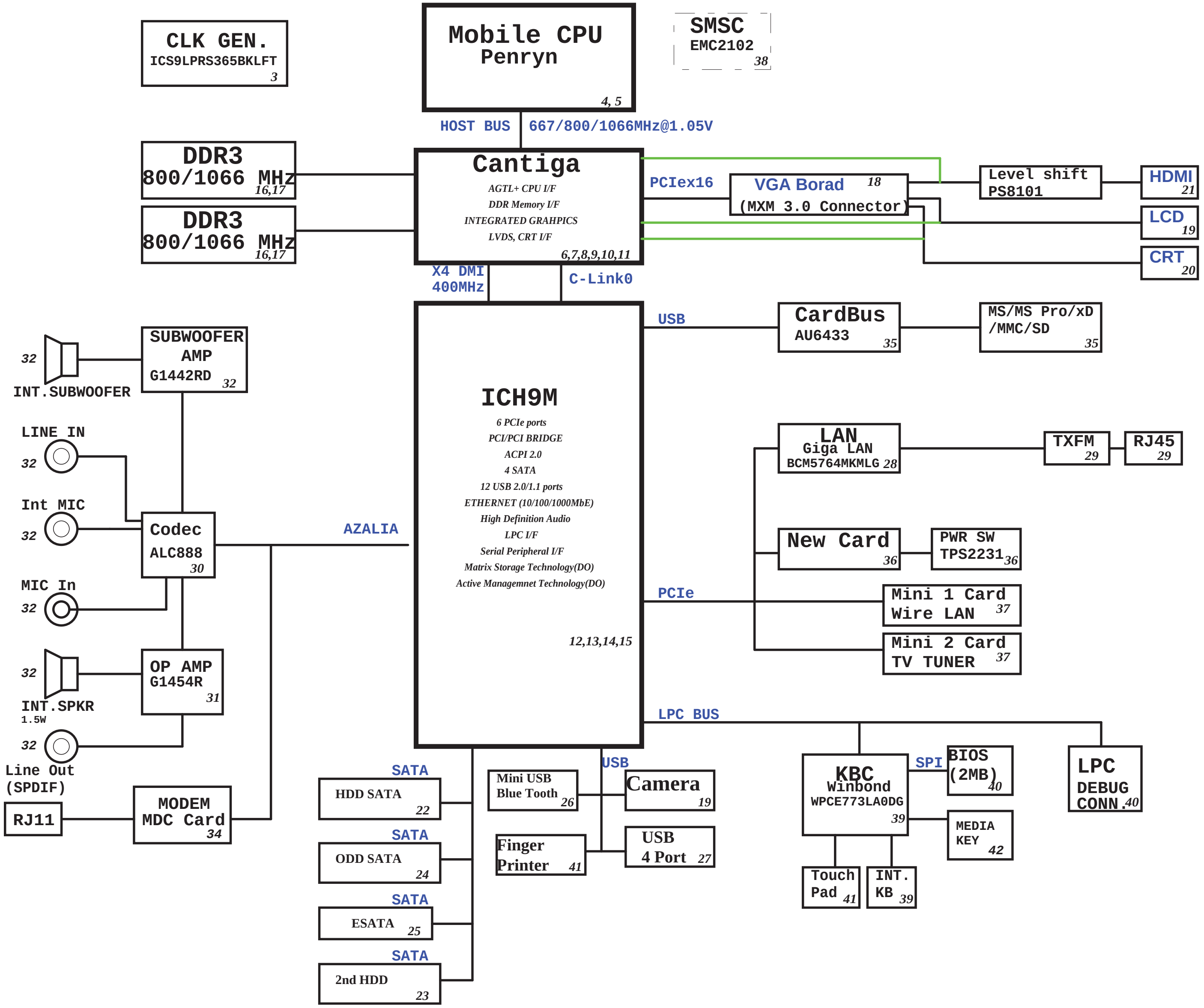
JM70 -MV Block Diagram

Project code: 91.4AN01.001
PCB P/N : 48.4AN01.0SA
REVISION : SB 08246



SYSTEM DC/DC ISL62392 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

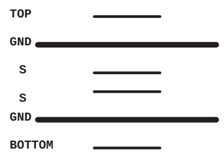
SYSTEM DC/DC TPS51124 46	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A) 1D5V_S3(10A)
RT9026	49
1.5V_S3	DDR_VREF_S3 (1.2A)
G9198-15	14
3D3V_S5	1D5V_S5 (300mA)

CHARGER ISL88731A 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ADP3208C 51	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A

GFX DC/DC ISL6263 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

PCB STACKUP



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Title	BLOCK DIAGRAM	
Size A2	Document Number JM70-MV	Rev SB
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ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

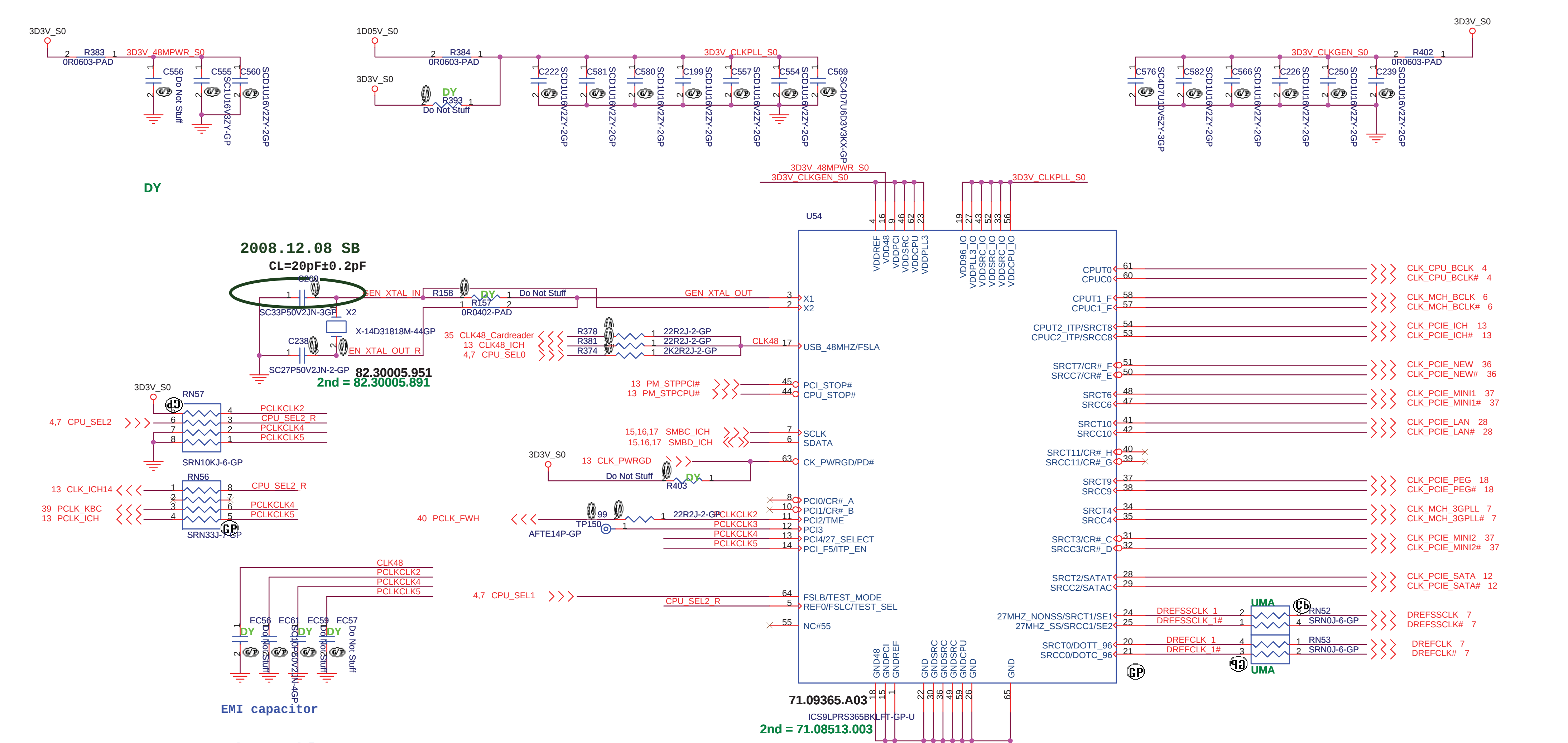
SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title	Clock Generator
Size / Document Number	JM70-MV
Rev	SB
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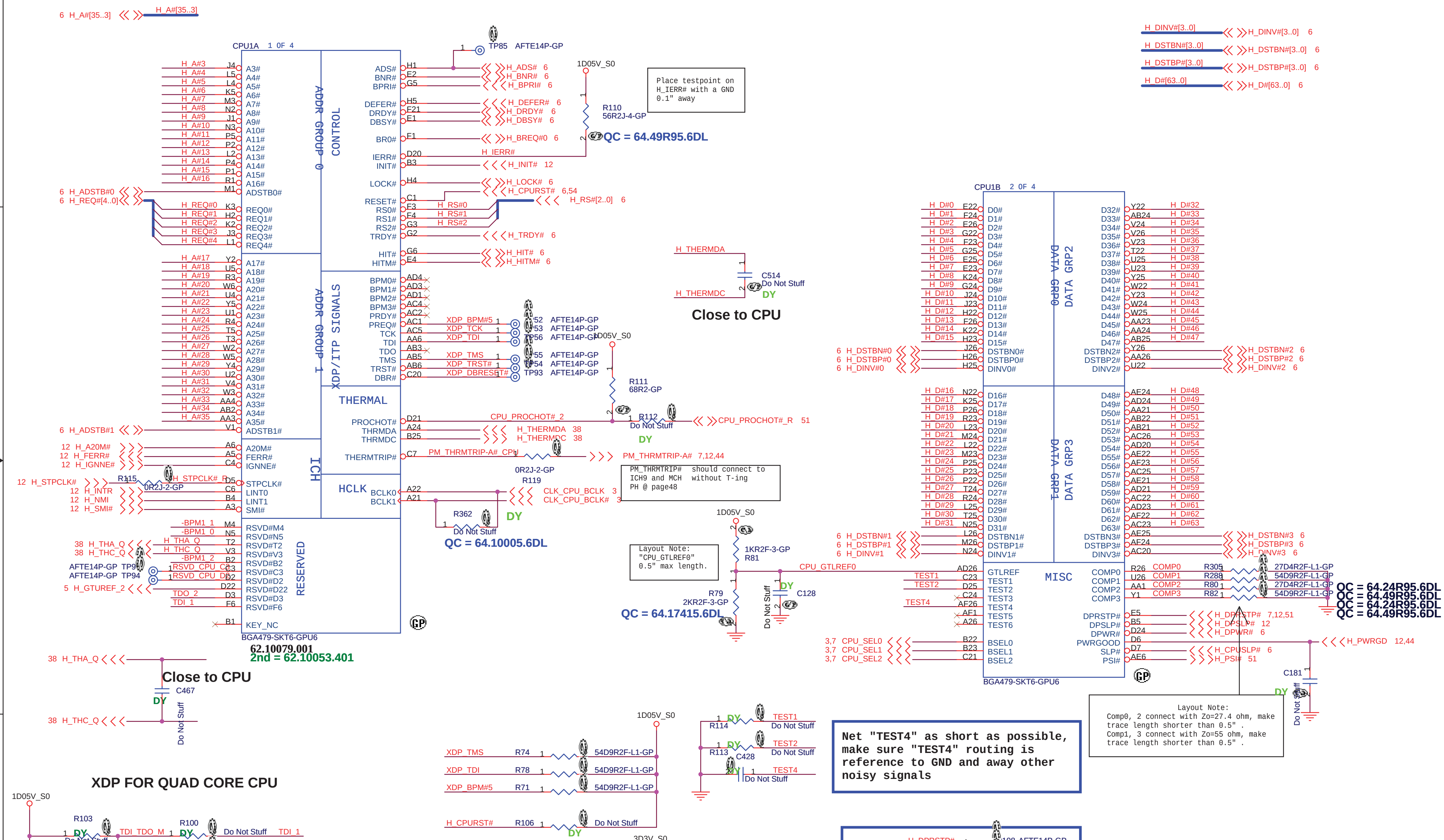

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Title		
CPU (1 of 2)		
Size	Document Number	Rev
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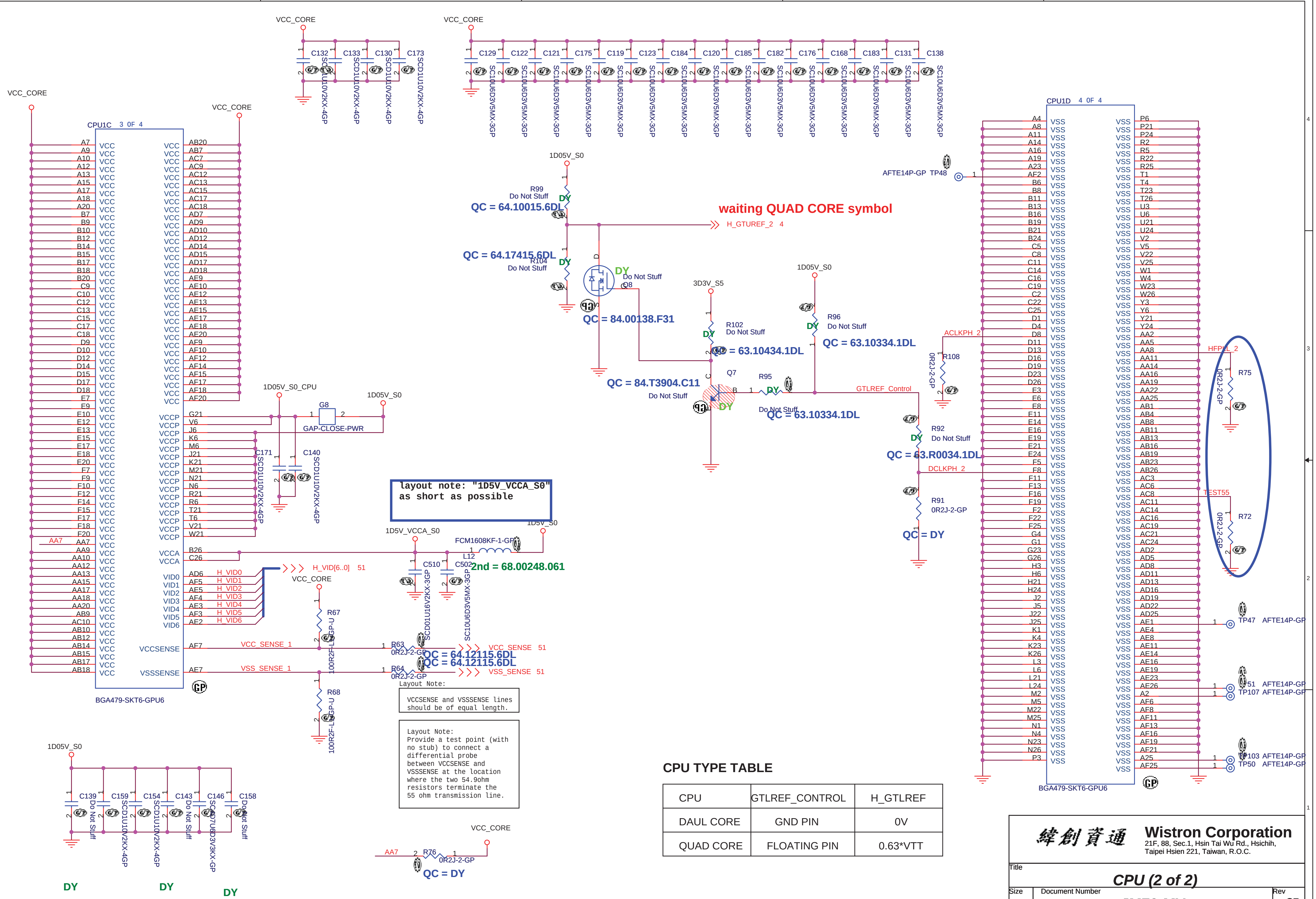

CPU TYPE TABLE

CPU	GTLREF_CONTROL	H_GTLREF
DAUL CORE	GND PIN	0V
QUAD CORE	FLOATING PIN	0.63*VTT

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Title: CPU (2 of 2)

Size | Document Number: JM70-MV | Rev: SB

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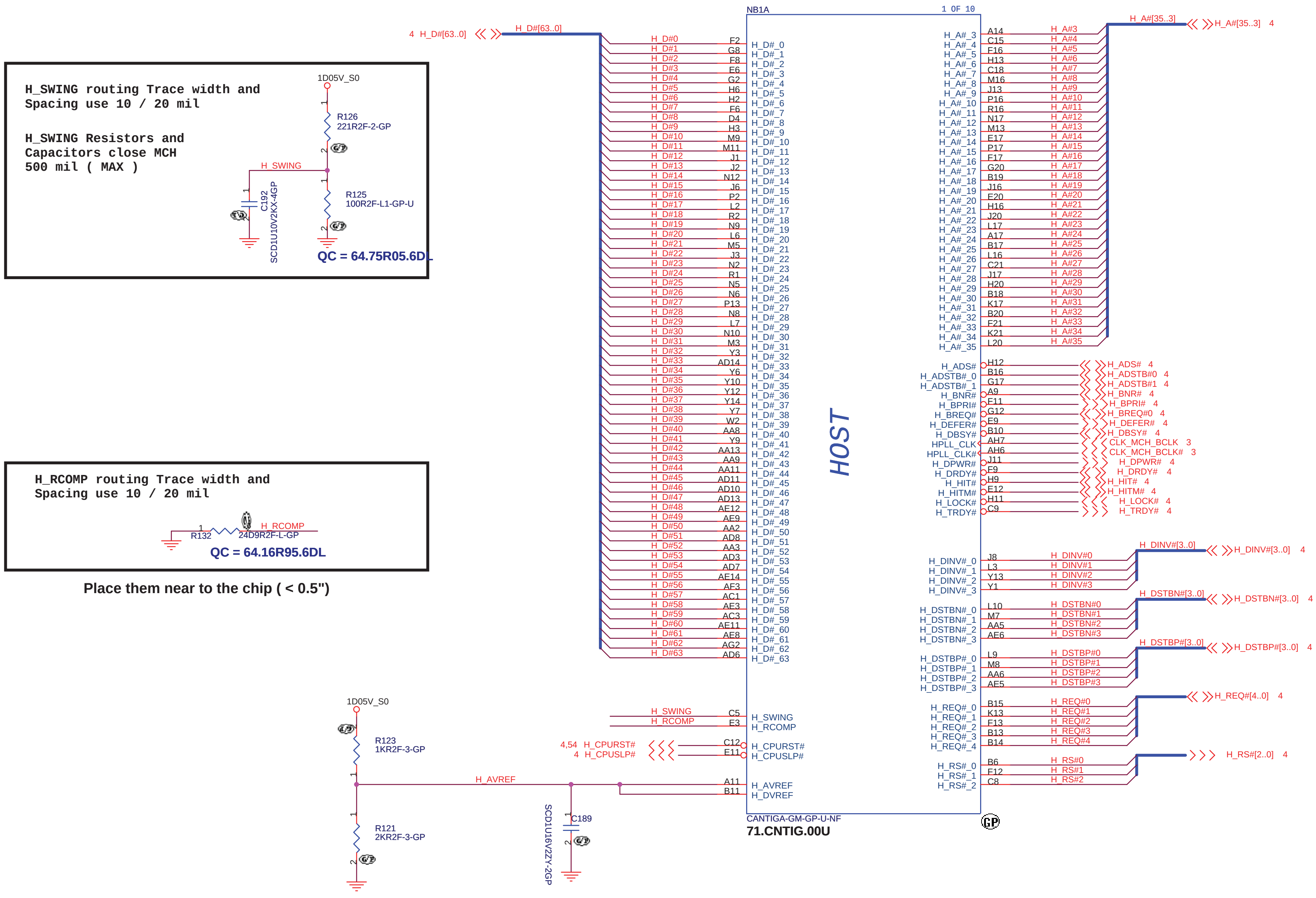

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Title			
	Cantiga (1 of 6)		
Size	Document Number: JM70-MV		Rev: SB
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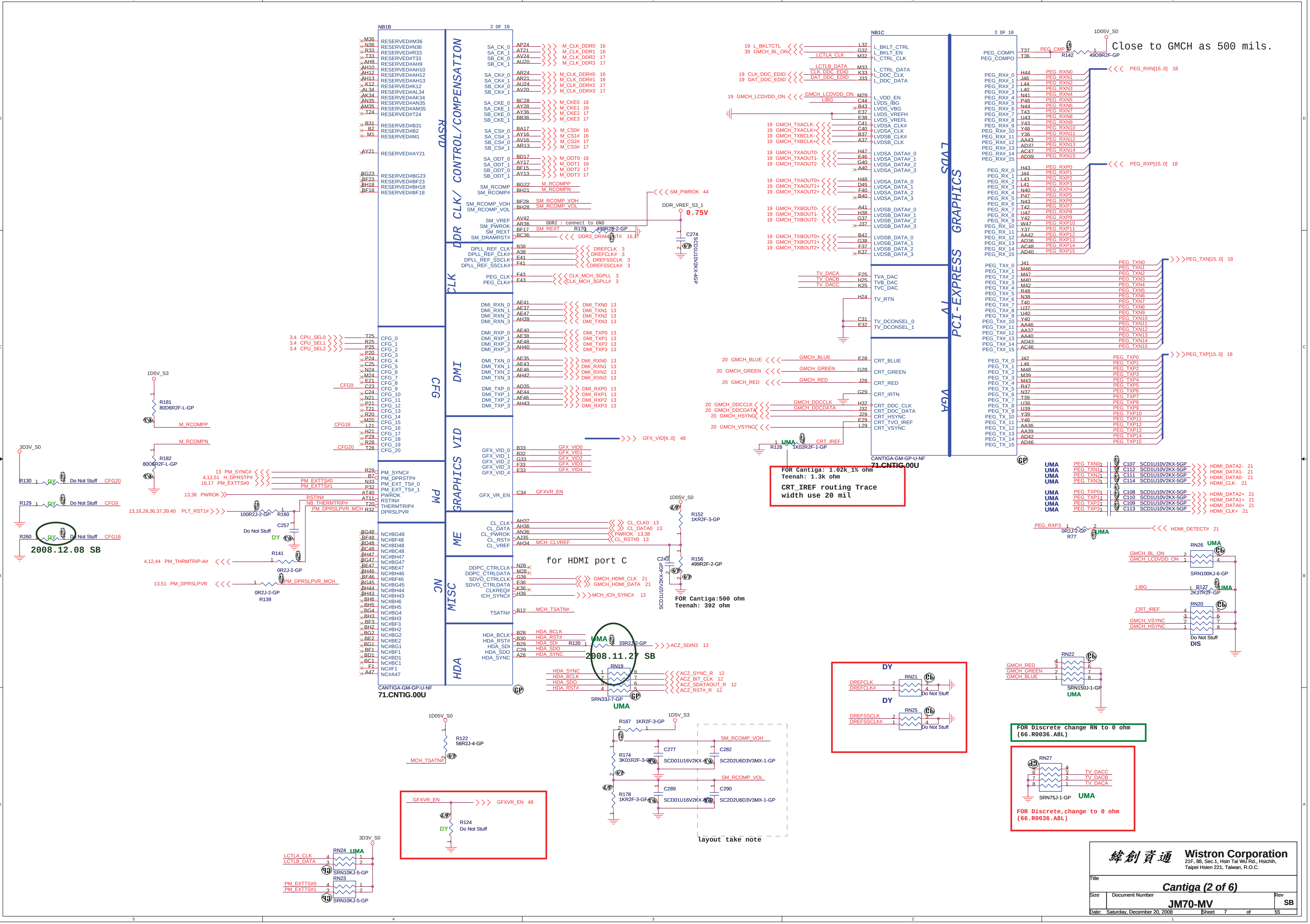

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Title	Cantiga (2 of 6)	
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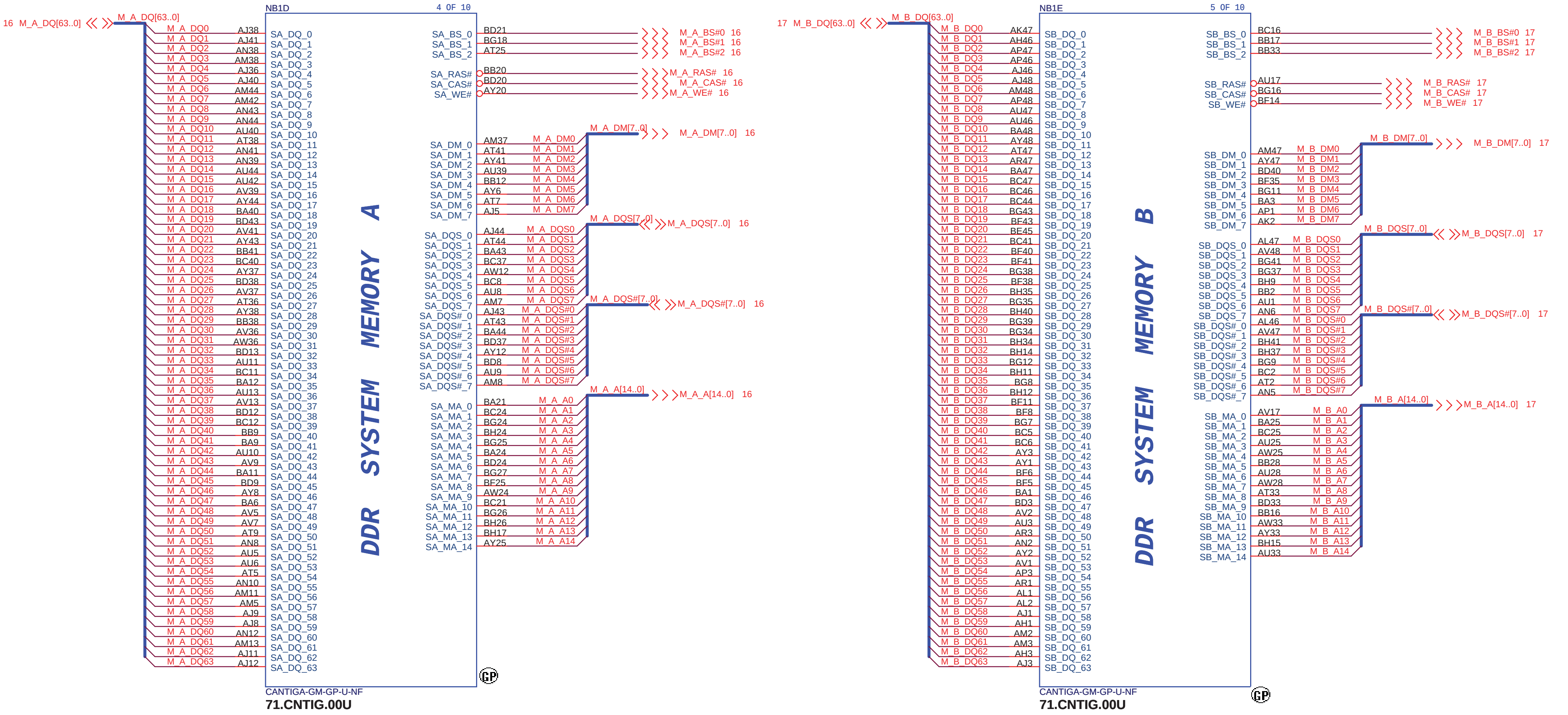

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Title	*Cantiga (3 of 6)*	
Size	Document Number: JM70-MV	Rev: SB
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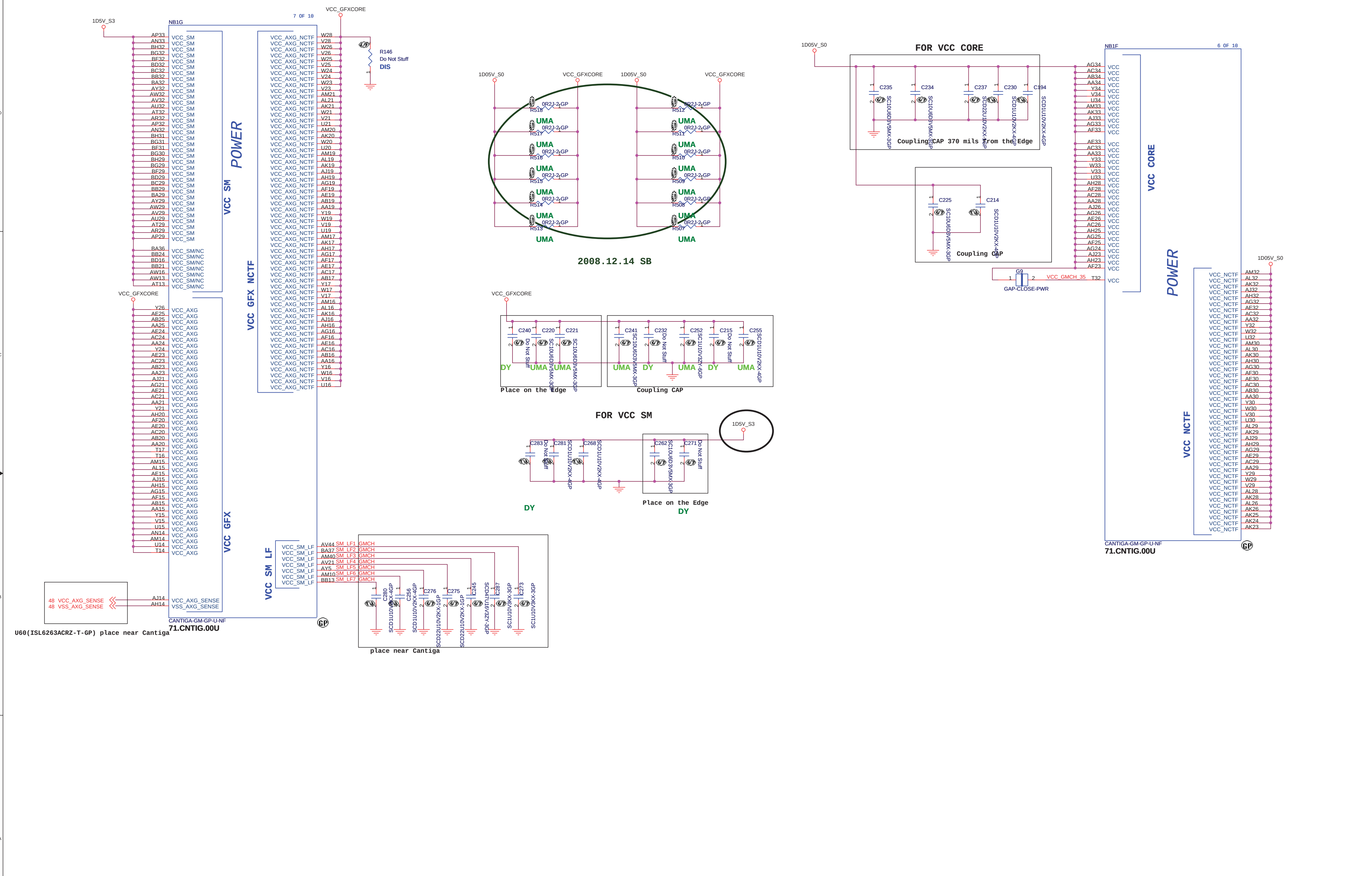

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Title	*Cantiga (4 of 6)*	
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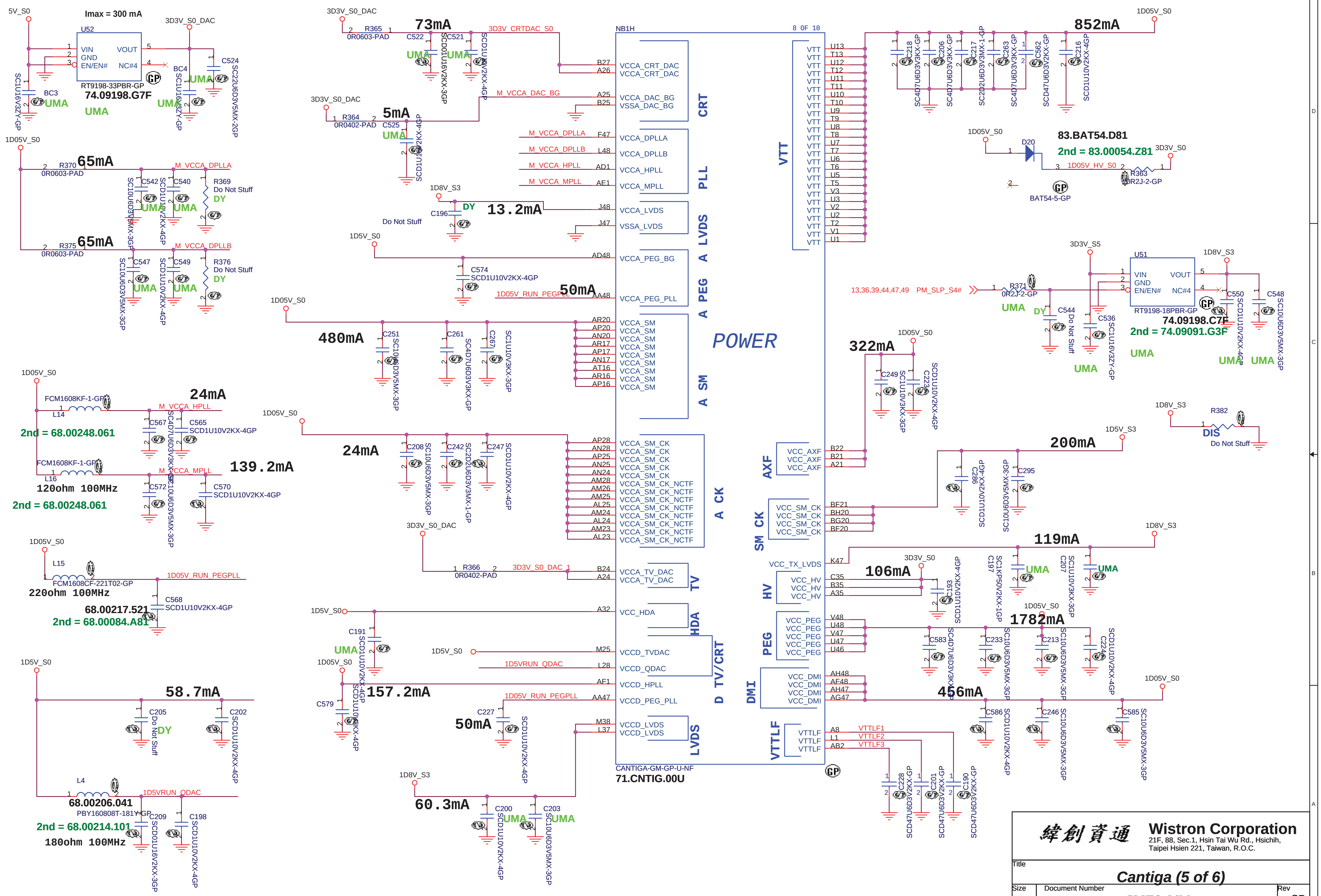
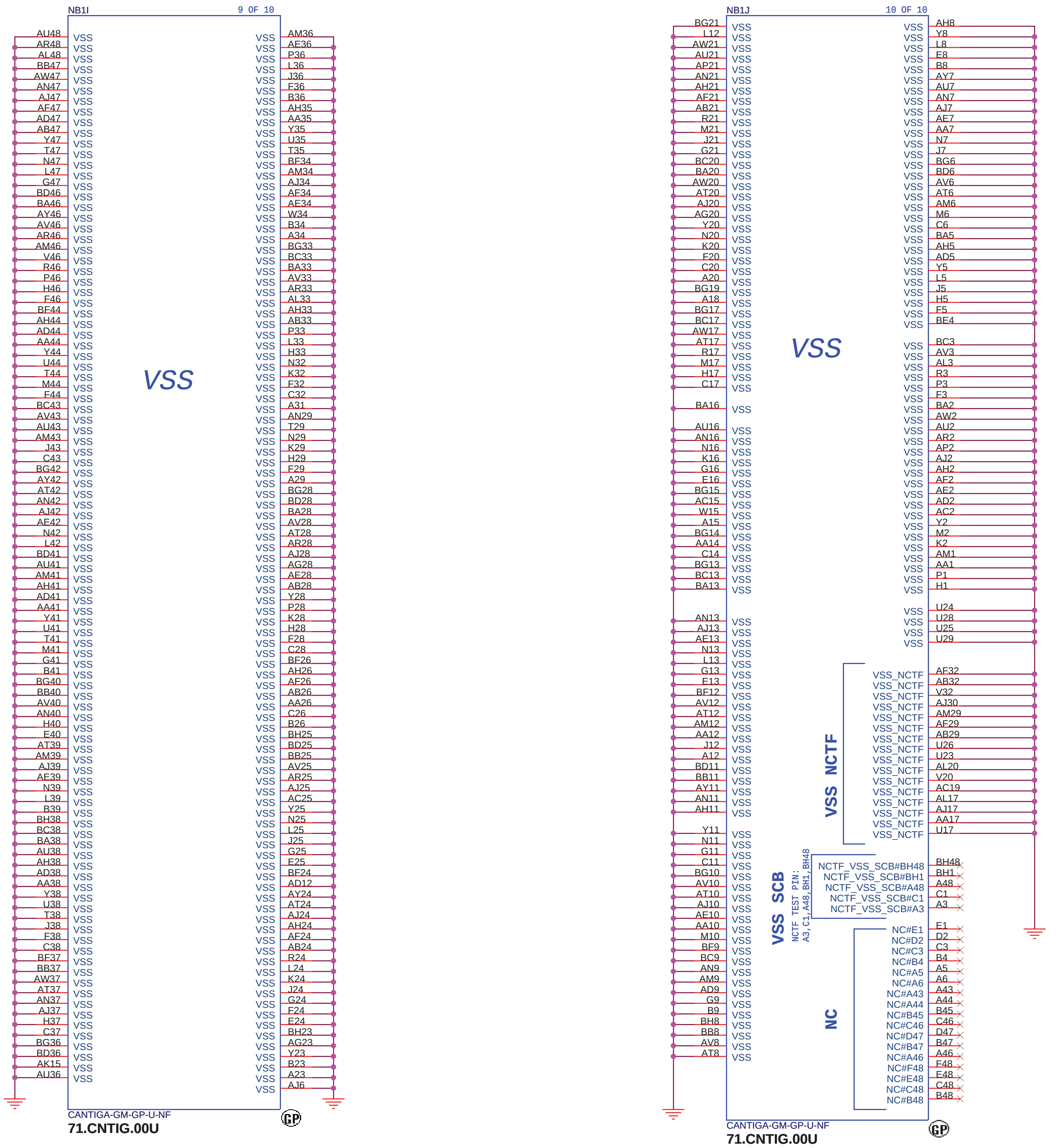

POWER
NB1H
8 OF 10
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
VCCA_CRT_DAC
VCCA_DAC_BG
VSSA_DAC_BG
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
VCCA_MPLL
VCCA_LVDS
VSSA_LVDS
VCCA_PEG_BG
VCCA_PEG_PLL
VCCA_SM
VCCA_SM_CK
VCCA_SM_CK_NCTF
VCCA_TV_DAC
VCC_HDA
VCCD_TVDAC
VCCD_QDAC
VCCD_HPLL
VCCD_PEG_PLL
VCCD_LVDS
VCC_AXF
VCC_SM_CK
VCC_TX_LVDS
VCC_HV
VCC_PEG
VCC_DMI
VTTLF
Imax = 300 mA
U52
RT9198-33PBR-GP
74.09198.G7F
73mA
5mA
13.2mA
50mA
480mA
24mA
65mA
65mA
24mA
139.2mA
120ohm 100MHz
2nd = 68.00248.061
220ohm 100MHz
68.00217.521
2nd = 68.00084.A81
58.7mA
157.2mA
50mA
60.3mA
68.00206.041
2nd = 68.00214.101
180ohm 100MHz
852mA
83.BAT54.D81
2nd = 83.00054.Z81
BAT54-5-GP
U51
RT9198-18PBR-GP
74.09198.C7F
2nd = 74.09091.G3F
322mA
200mA
119mA
106mA
1782mA
456mA
Do Not Stuff
UMA
DY
DIS



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Title	**Cantiga (6 of 6)**	
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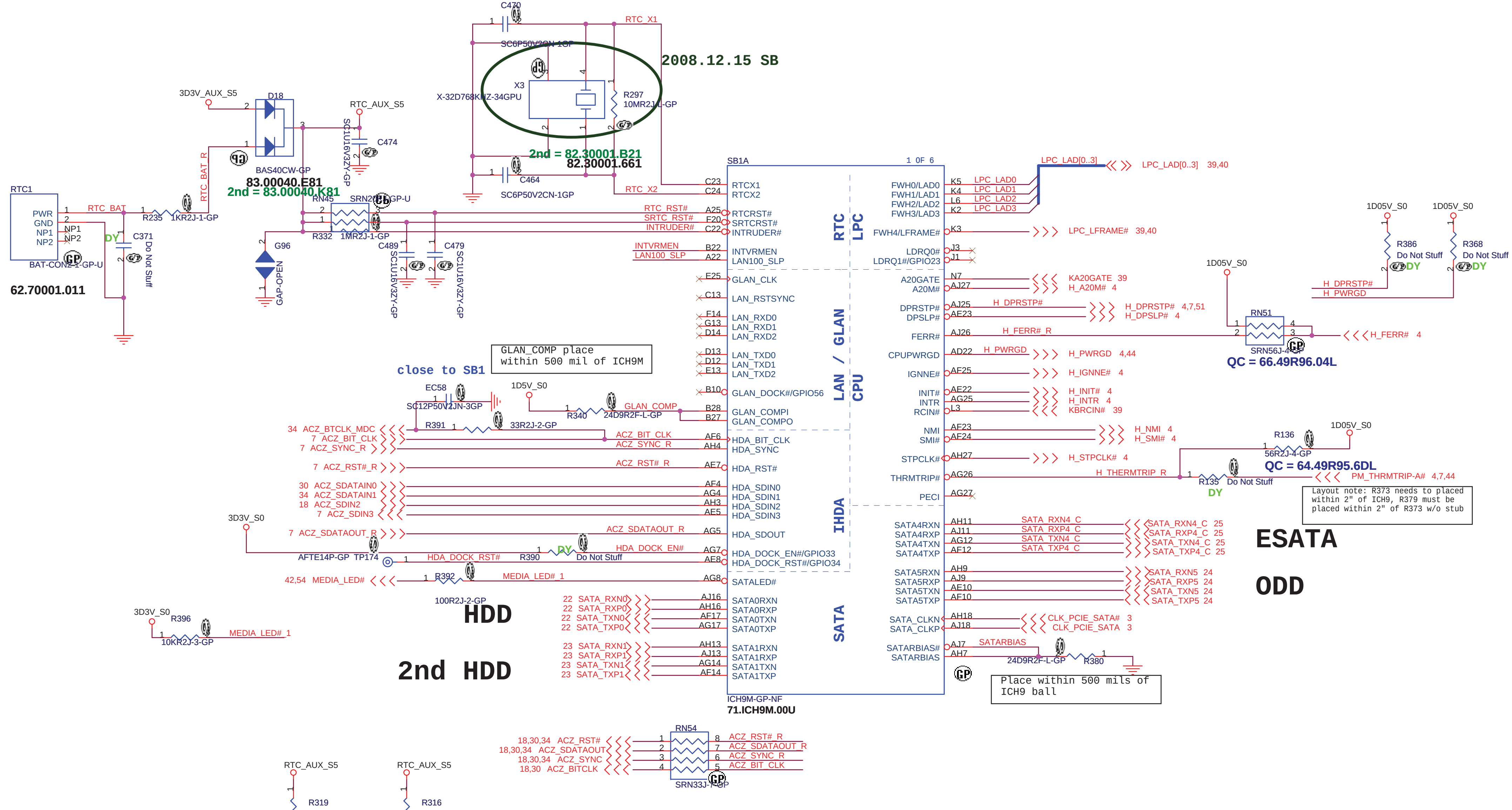

integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

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Title: ICH9-M (1 of 4)

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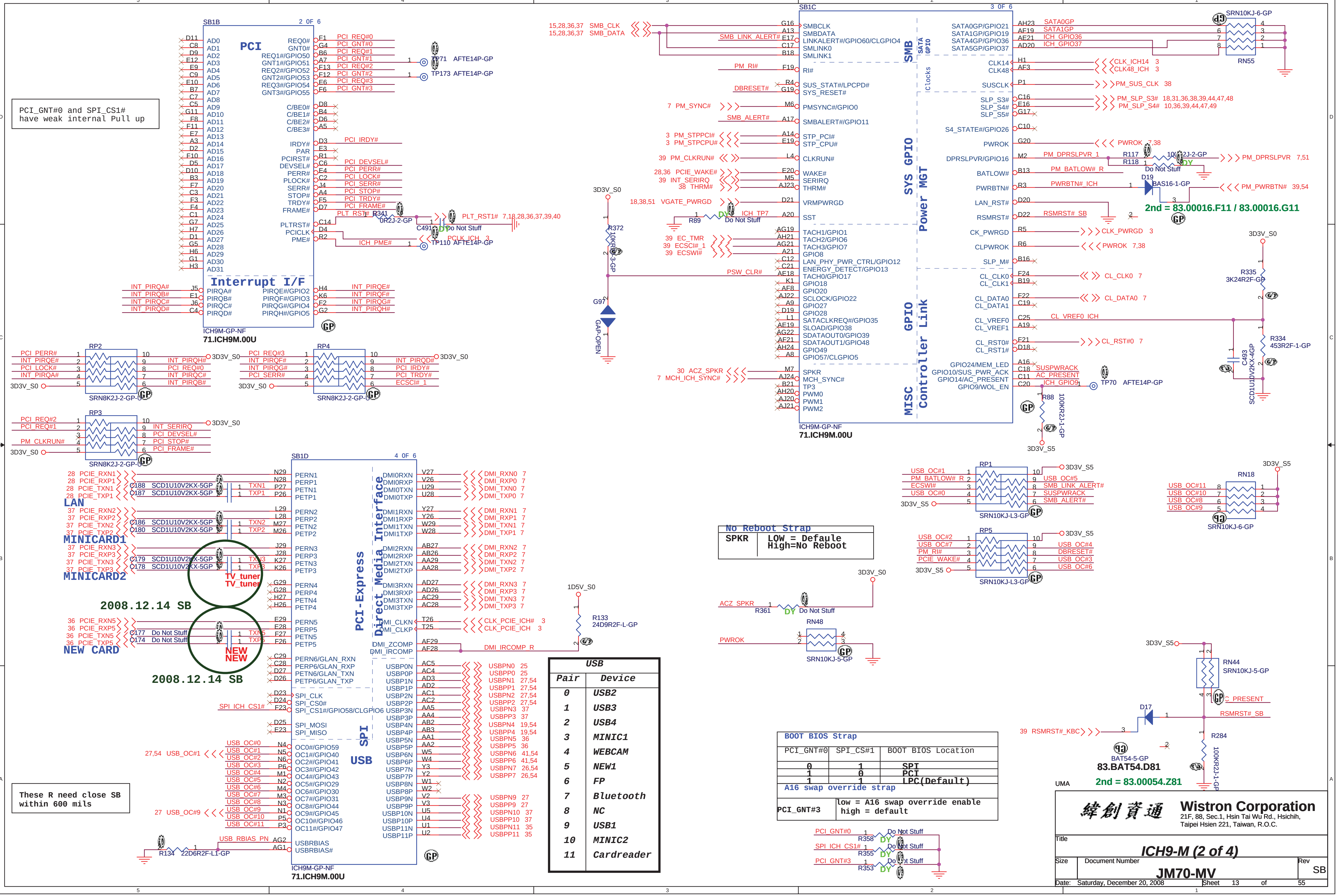

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINIC1
4	WEBCAM
5	NEW1
6	FP
7	Bluetooth
8	NC
9	USB1
10	MINIC2
11	Cardreader

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

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Title: ICH9-M (2 of 4)

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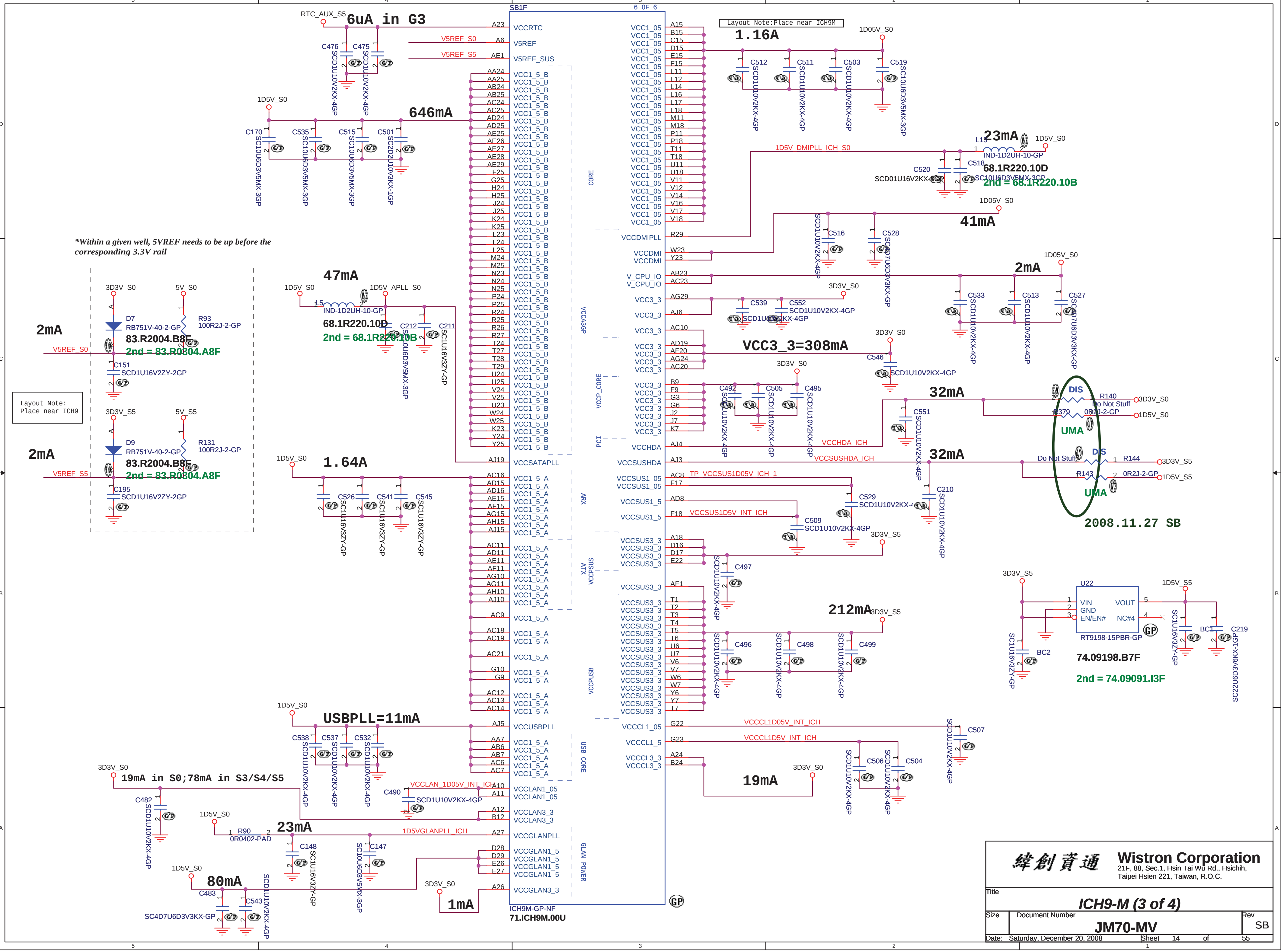
6uA in G3
RTC_AUX_S5
646mA
1.16A
Layout Note:Place near ICH9M
1D05V_S0
23mA
1D5V_DMIPLL_ICH_S0
IND-1D2UH-10-GP
68.1R220.10D
2nd = 68.1R220.10B
41mA
2mA
VCC3_3=308mA
32mA
DIS
UMA
Do Not Stuff
2008.11.27 SB
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
47mA
1D5V_APLL_S0
RB751V-40-2-GP
83.R2004.B8F
2nd = 83.R0304.A8F
V5REF_S0
V5REF_S5
Layout Note: Place near ICH9
1.64A
212mA
U22
RT9198-15PBR-GP
74.09198.B7F
2nd = 74.09091.I3F
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
19mA
VCCLAN_1D05V_INT_ICH
1D5VGLANPLL_ICH
VCCCL1D05V_INT_ICH
VCCCL1D5V_INT_ICH
VCCSUS1D5V_INT_ICH
TP_VCCSUS1D05V_ICH_1
VCCHDA_ICH
VCCSUSHDA_ICH
SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
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Title
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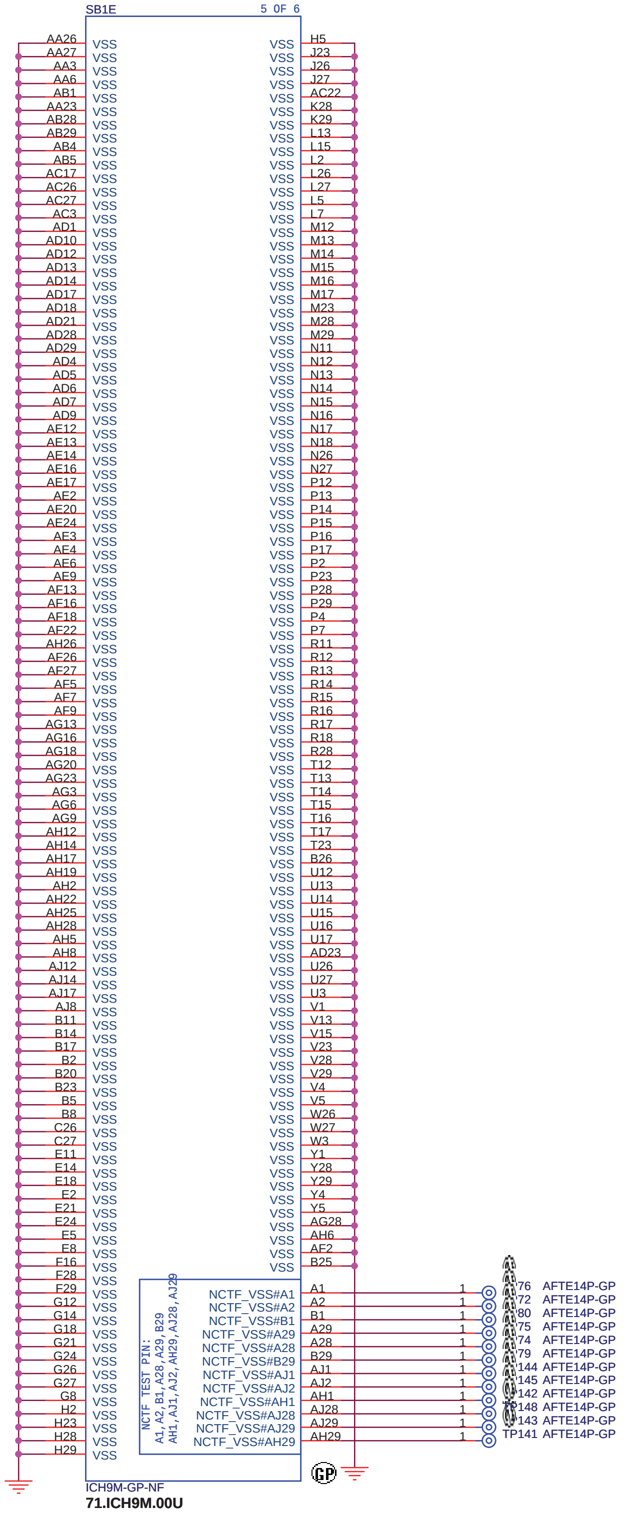

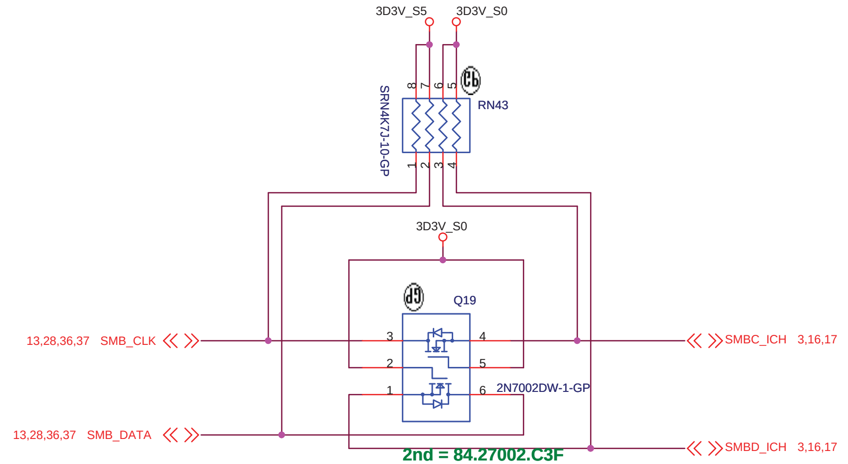

SMBUS

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Title		
ICH9-M (4 of 4)		
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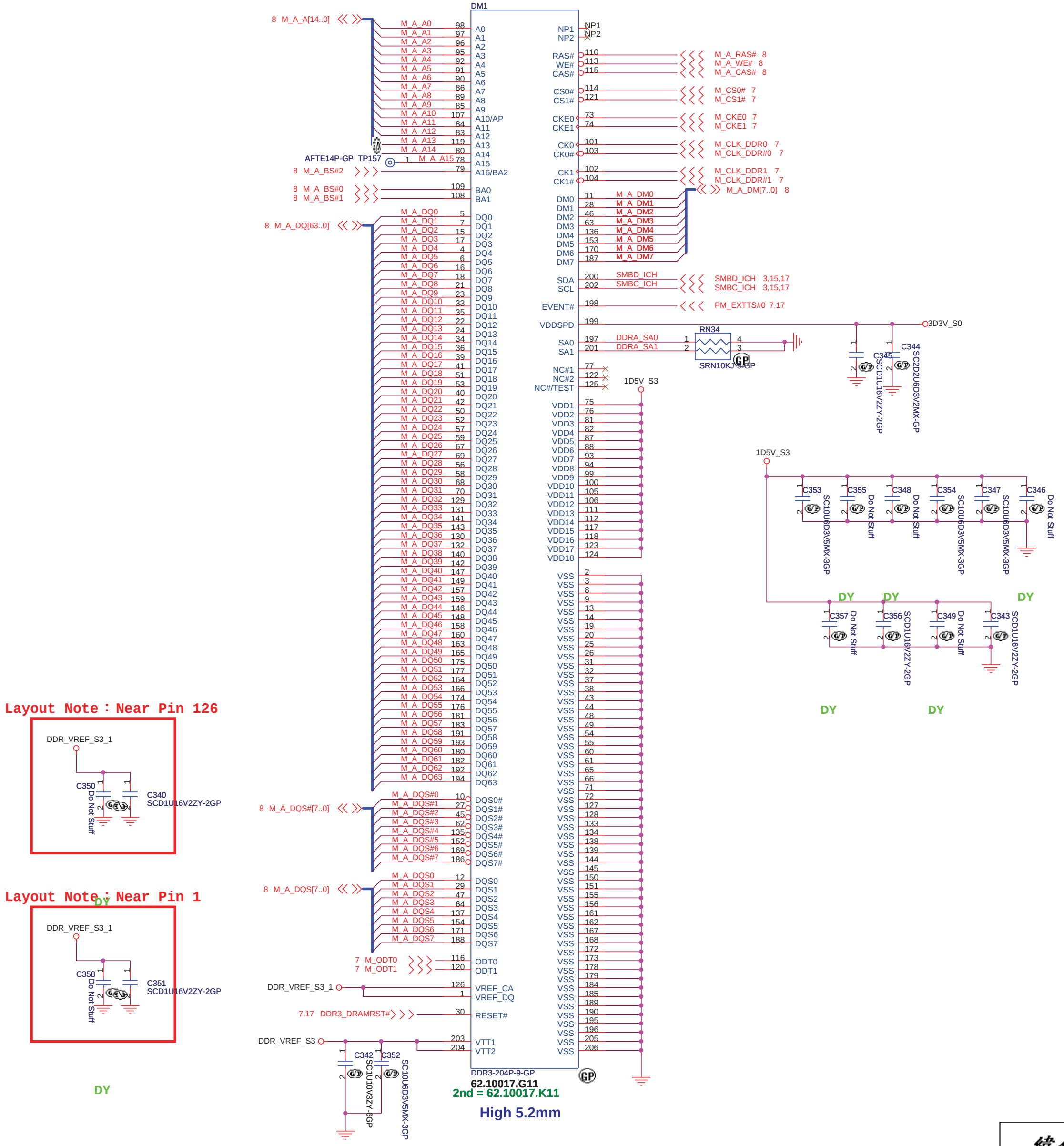
DDR3 SOCKET_1



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Title	DDR3 Socket	
Size	Document Number: JM70-MV	Rev: SB
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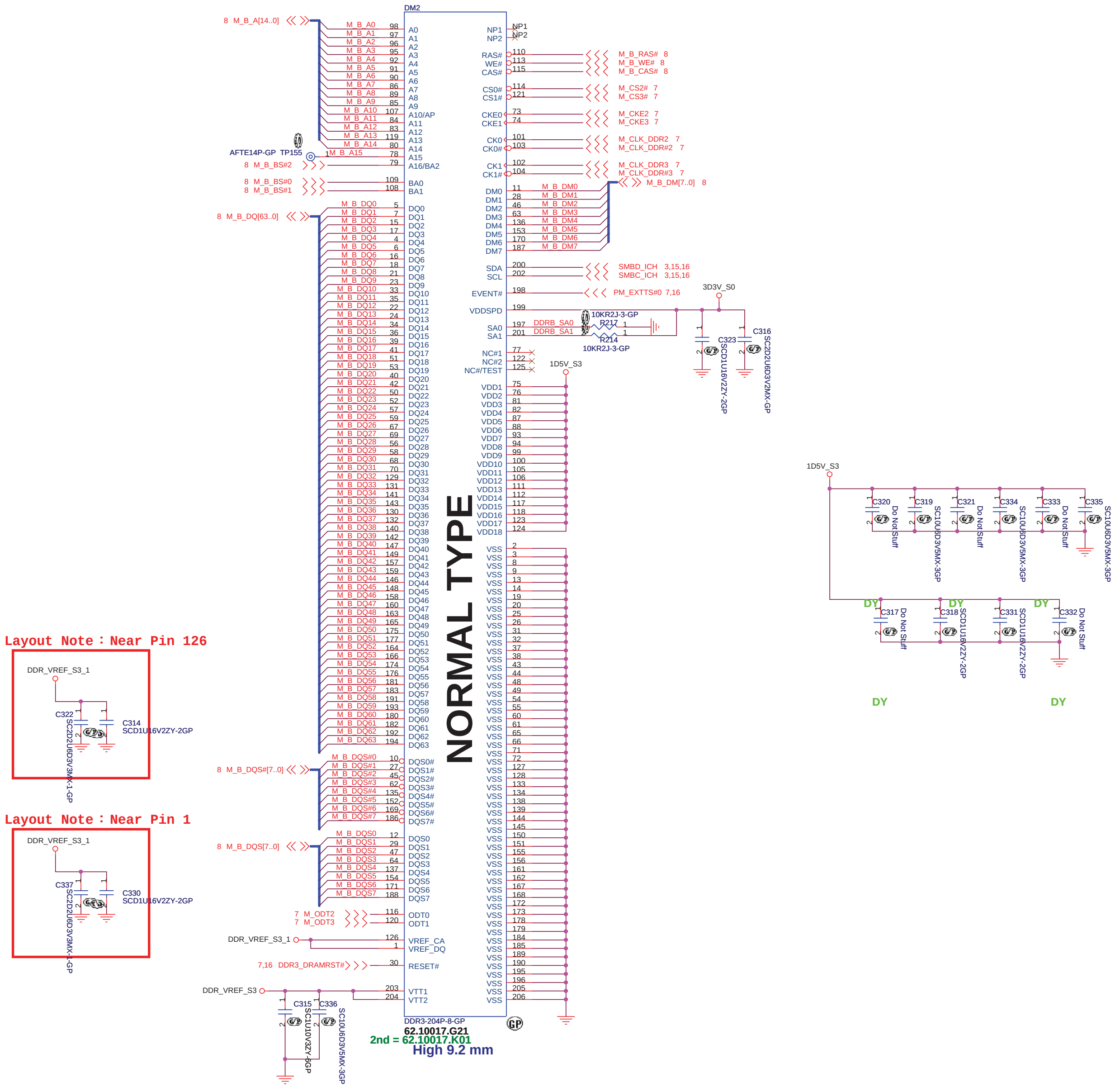
DDR3 SOCKET_2



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Title	DDR3 Socket2
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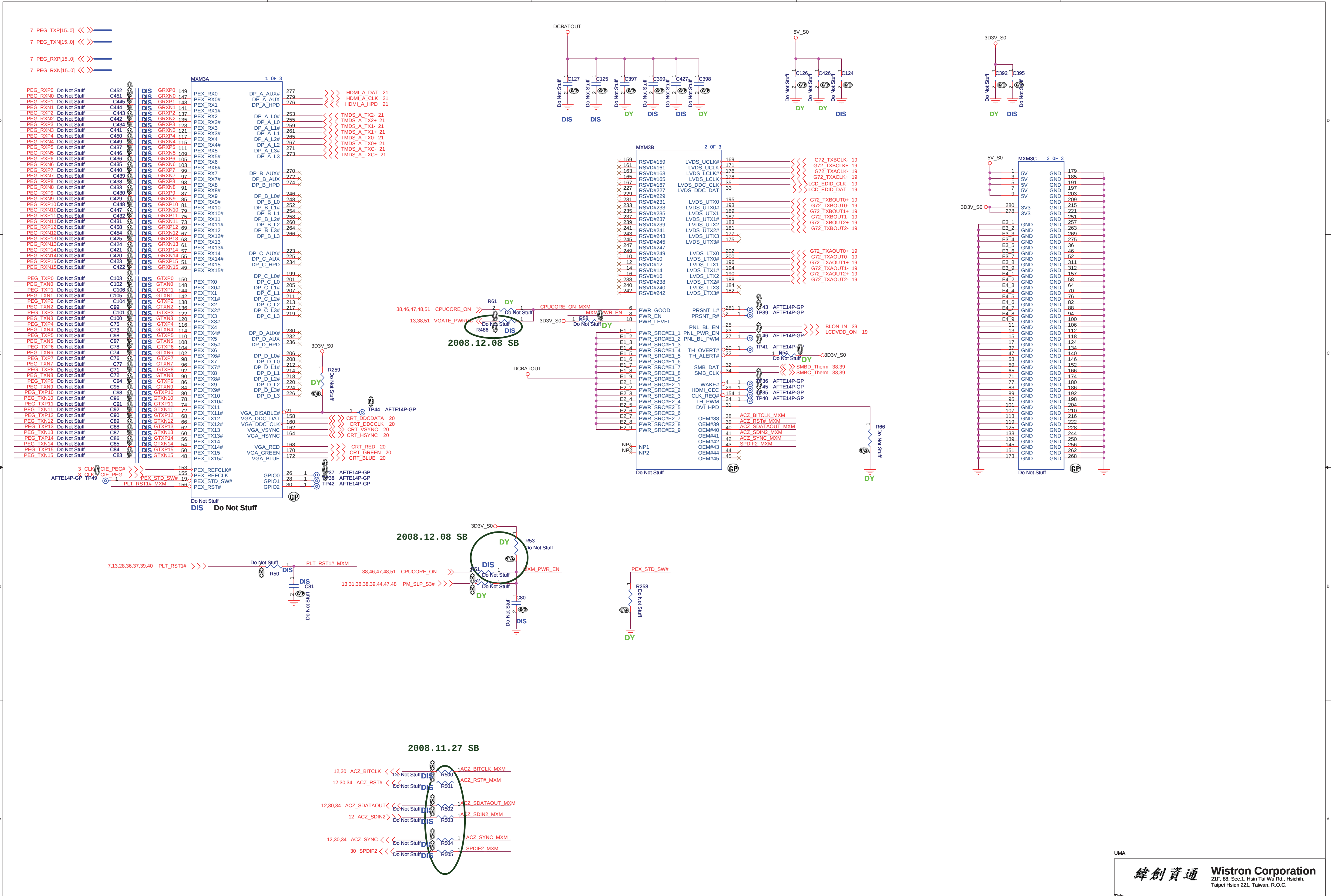

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Title
Graphic MXM 3.0 CONN

Size	Document Number	Rev
A2	JM70-MV	SB

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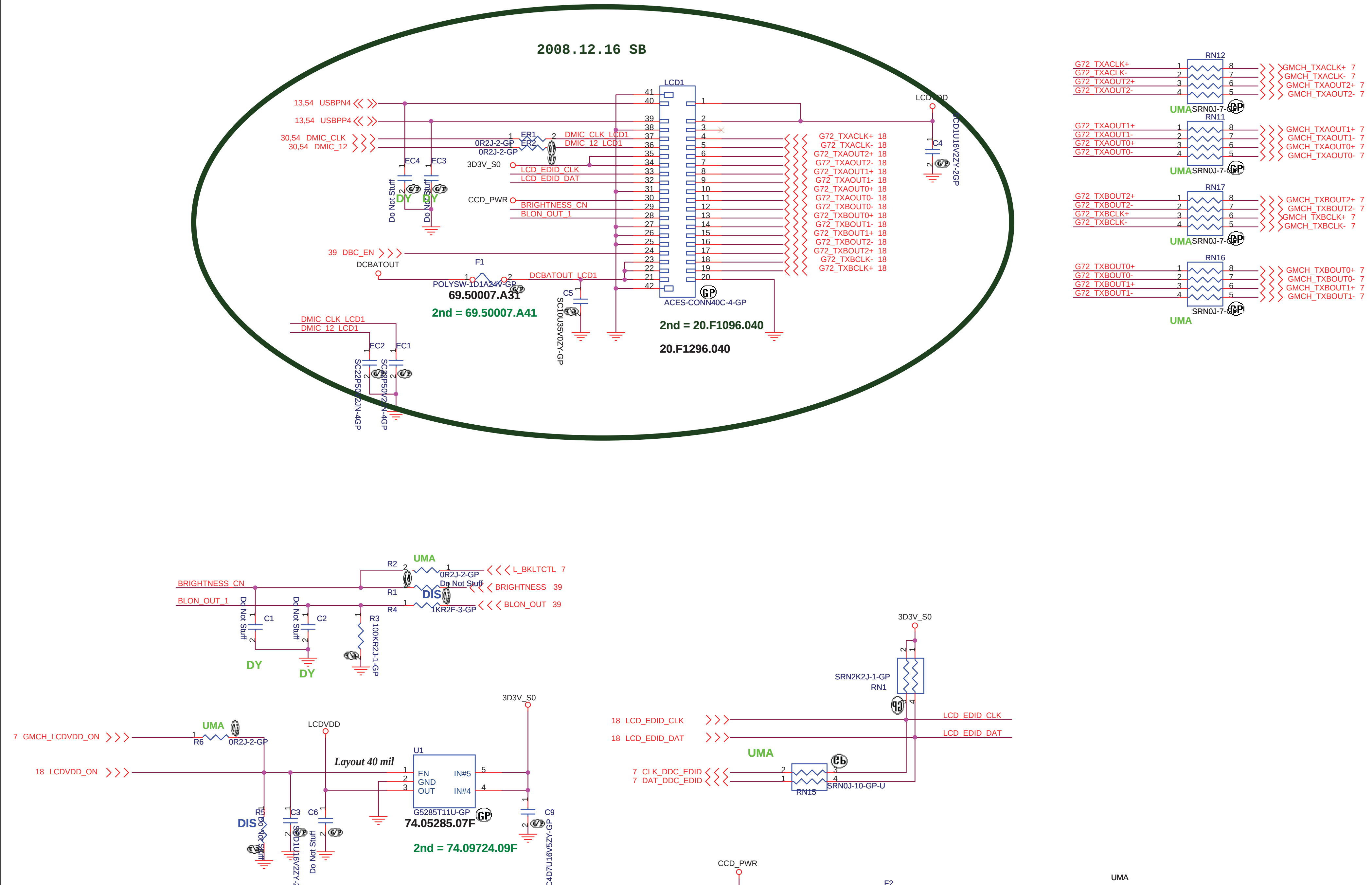

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Title		
LCD CONN		
Size	Document Number: **JM70-MV**	Rev: SB
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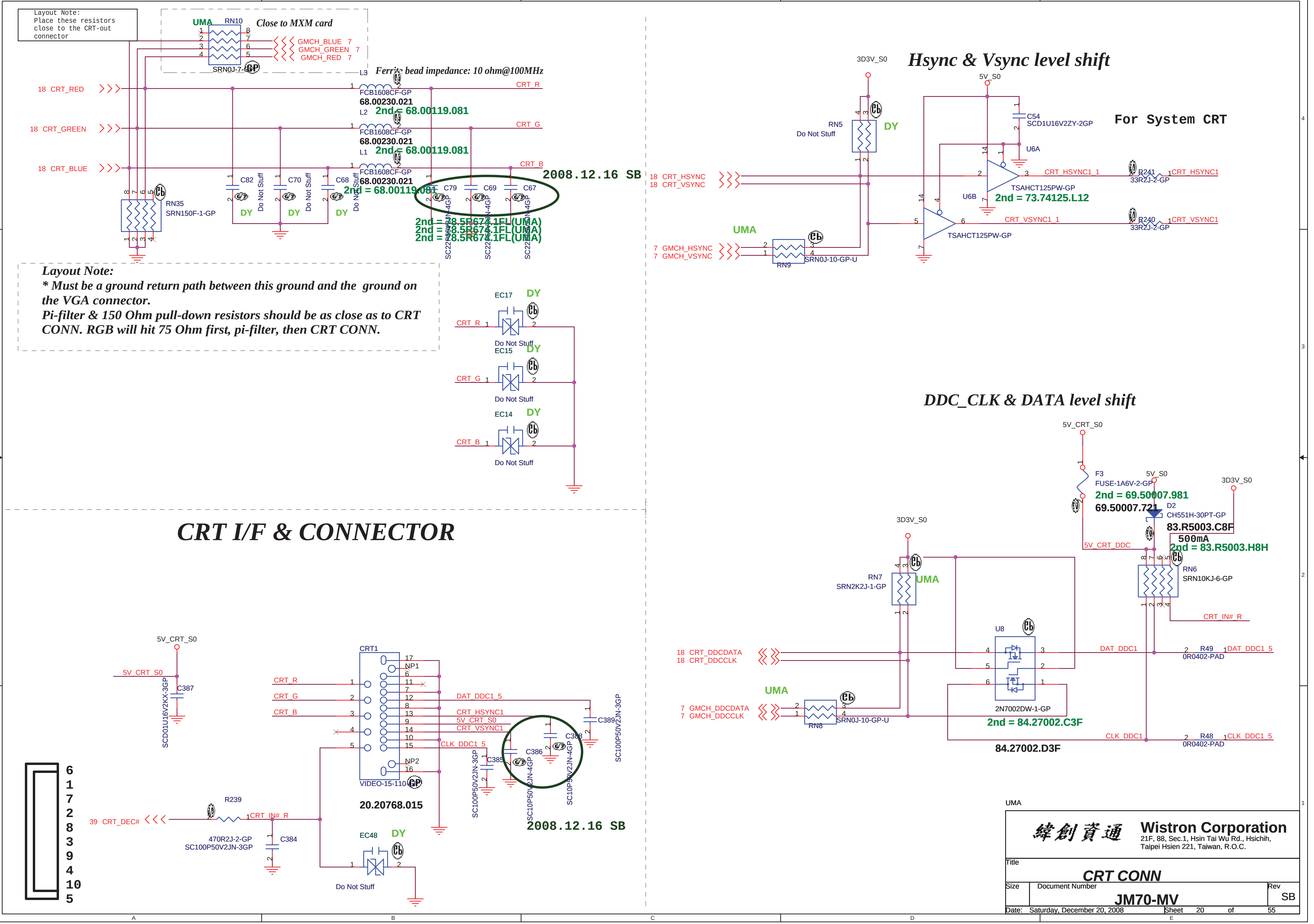

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT CONN**

Size | Document Number: **JM70-MV** | Rev: SB

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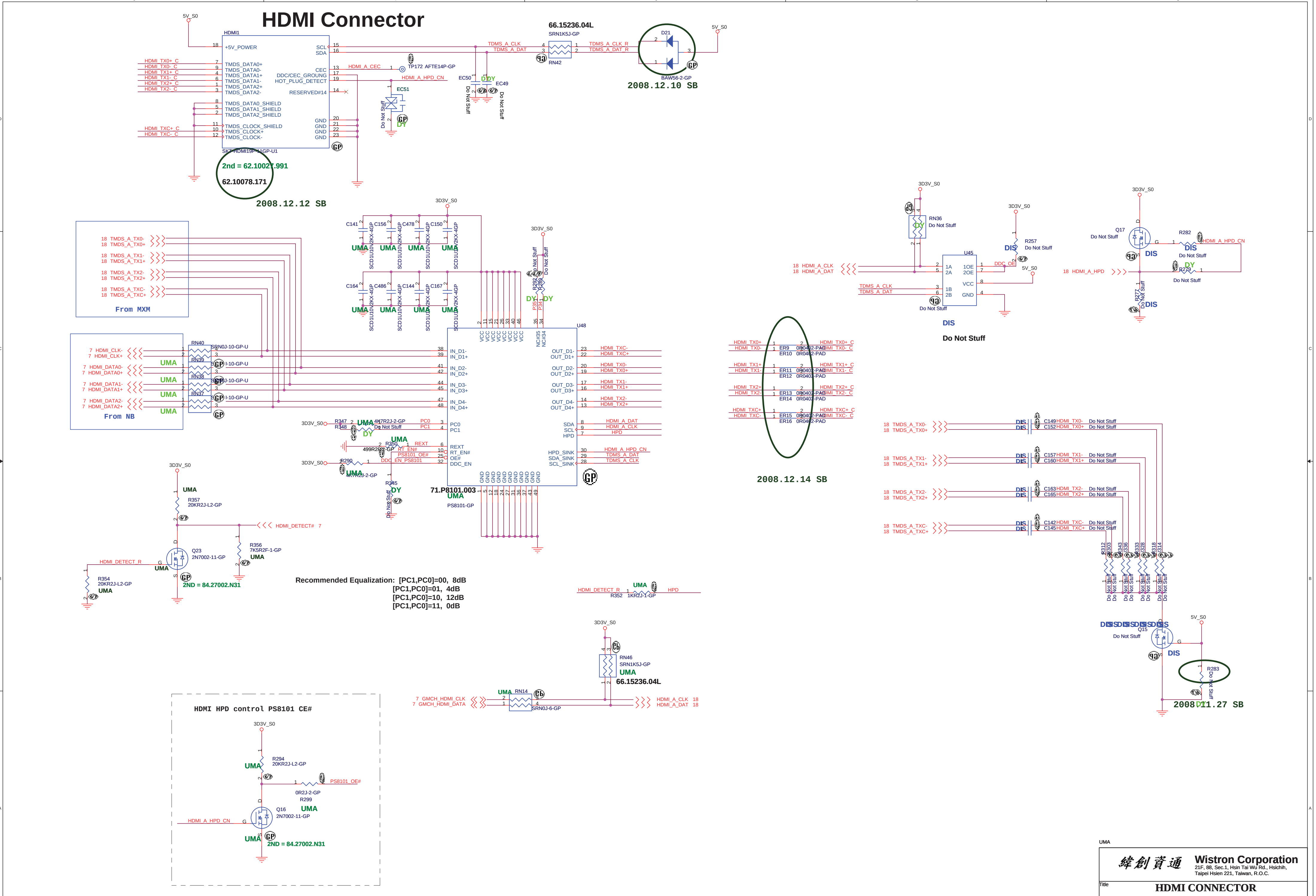
HDMI Connector



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDMI CONNECTOR		
Size A2	Document Number JM70-MV	Rev SB
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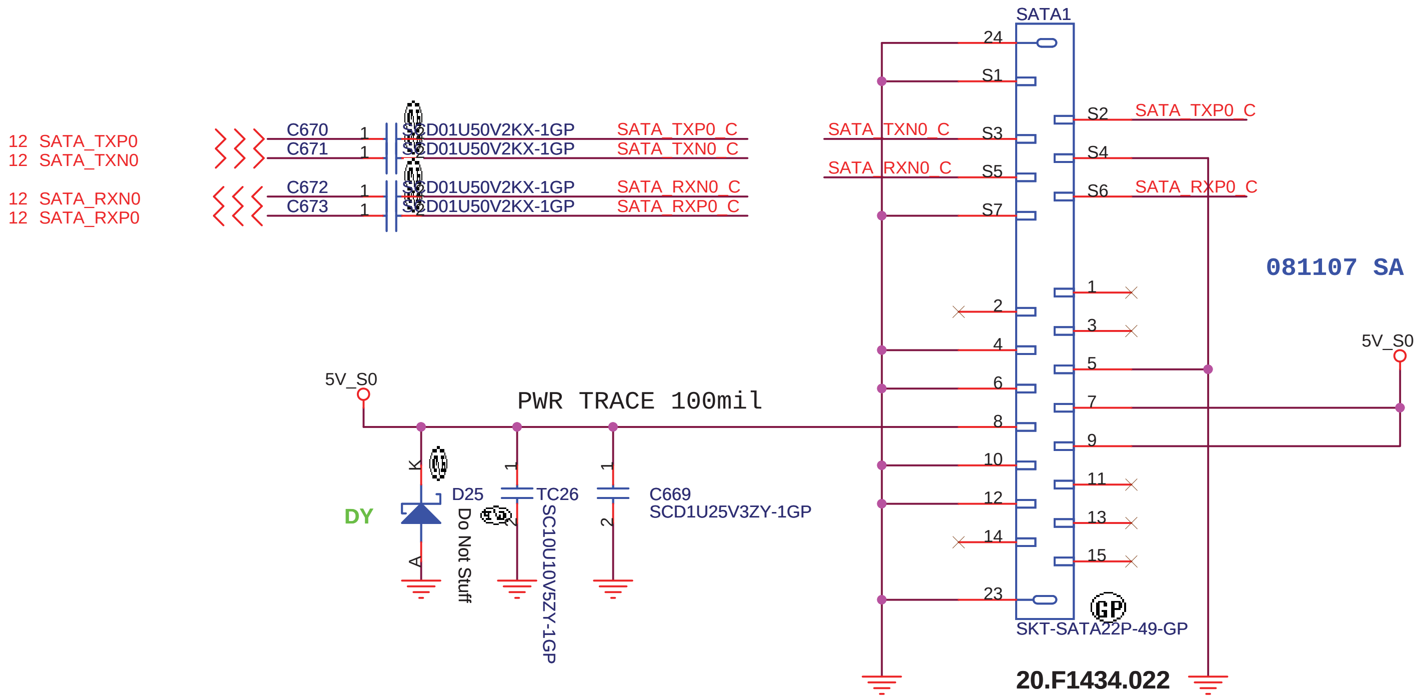
SATA Connector

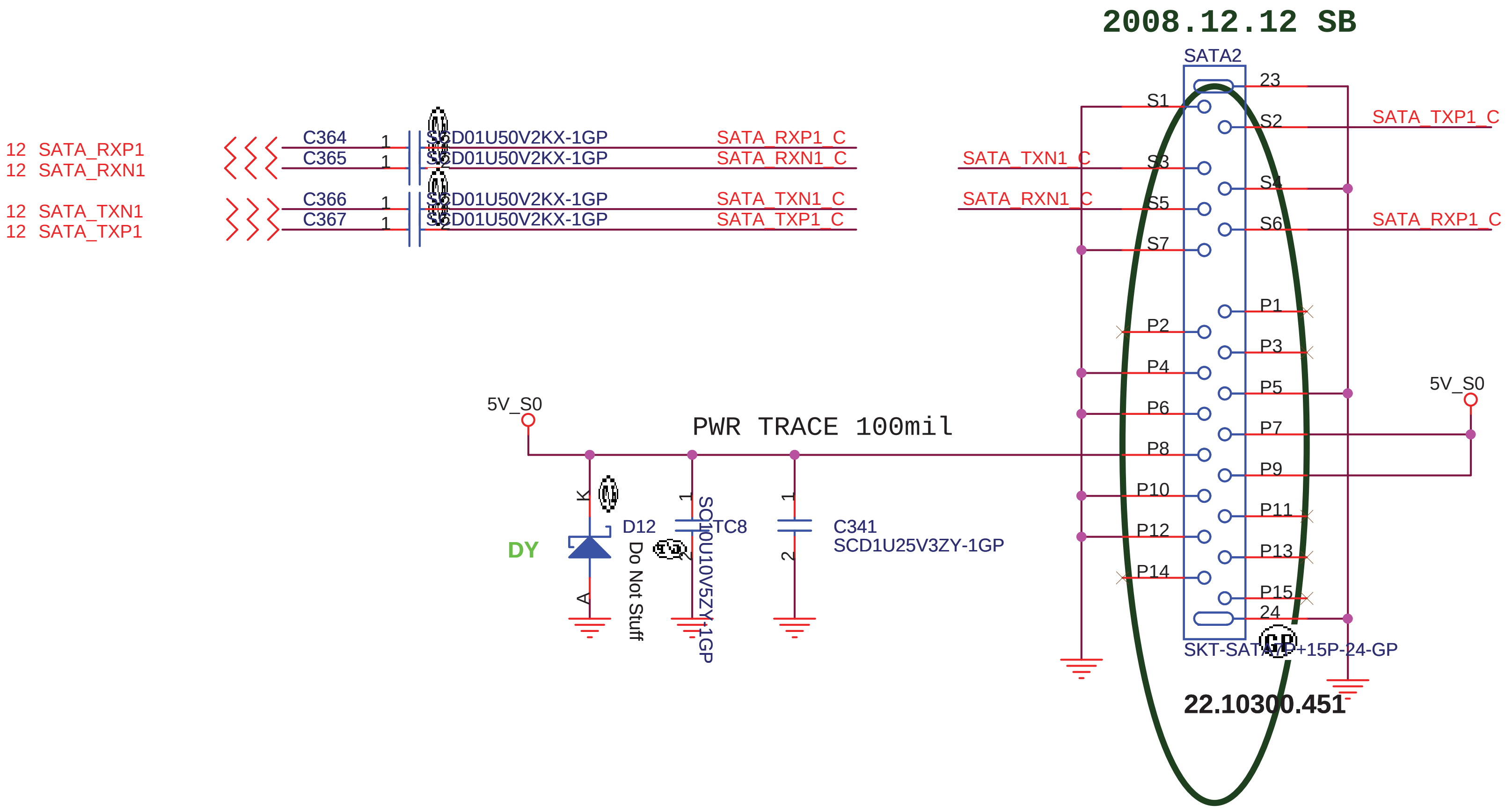


UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*HDD CONN*	
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 22 of 55	

2nd HDD SATA Connector

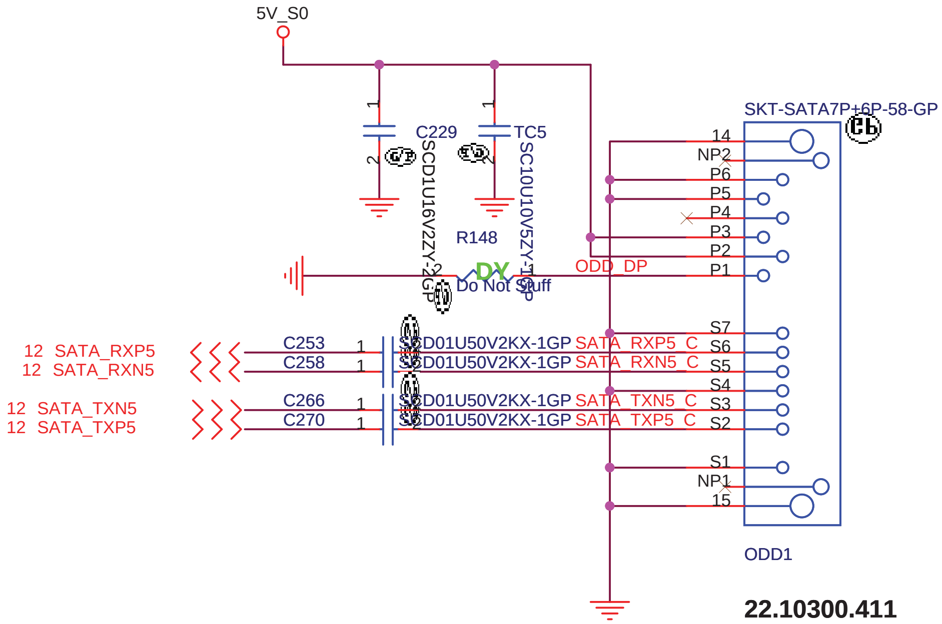


UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	2nd HDD		
Size	Document Number: JM70-MV		Rev: SB
Date: Saturday, December 20, 2008		Sheet 23	of 55

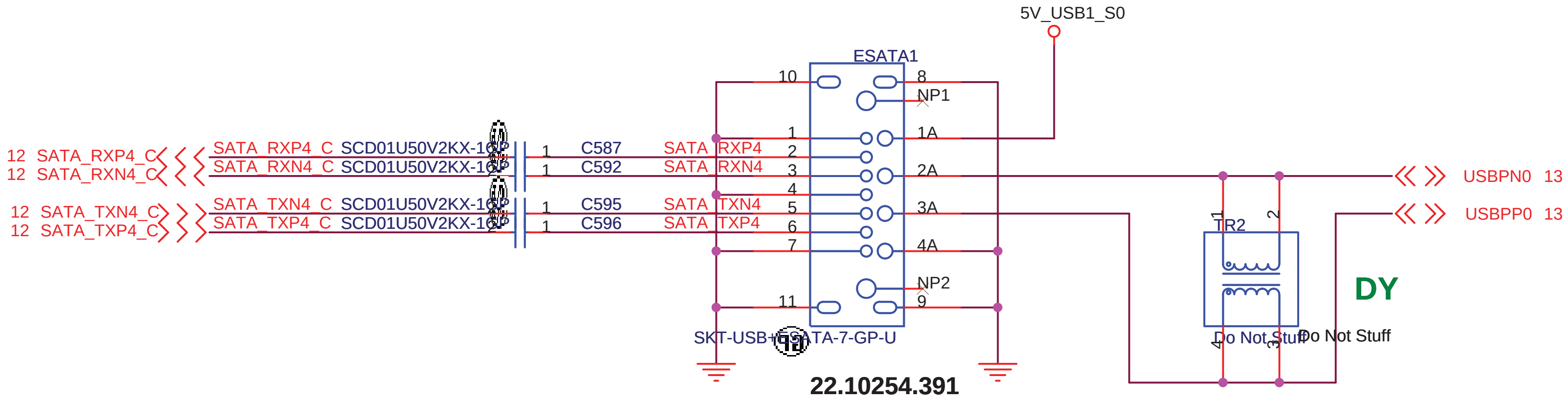
ODD Connector



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**ODD**
Size / Document Number	**JM70-MV**
Rev	SB
Date: Saturday, December 20, 2008	Sheet 24 of 55

ESATA Connector

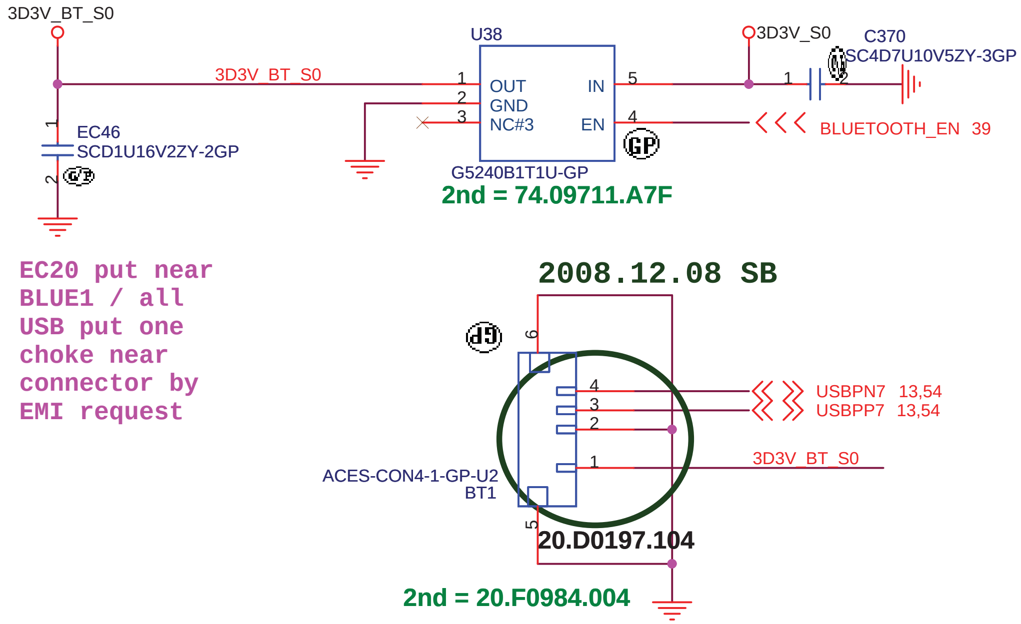


UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**ESATA**	
Size A4	Document Number **JM70-MV**	Rev **SB**
Date: Saturday, December 20, 2008	Sheet 25 of 55	

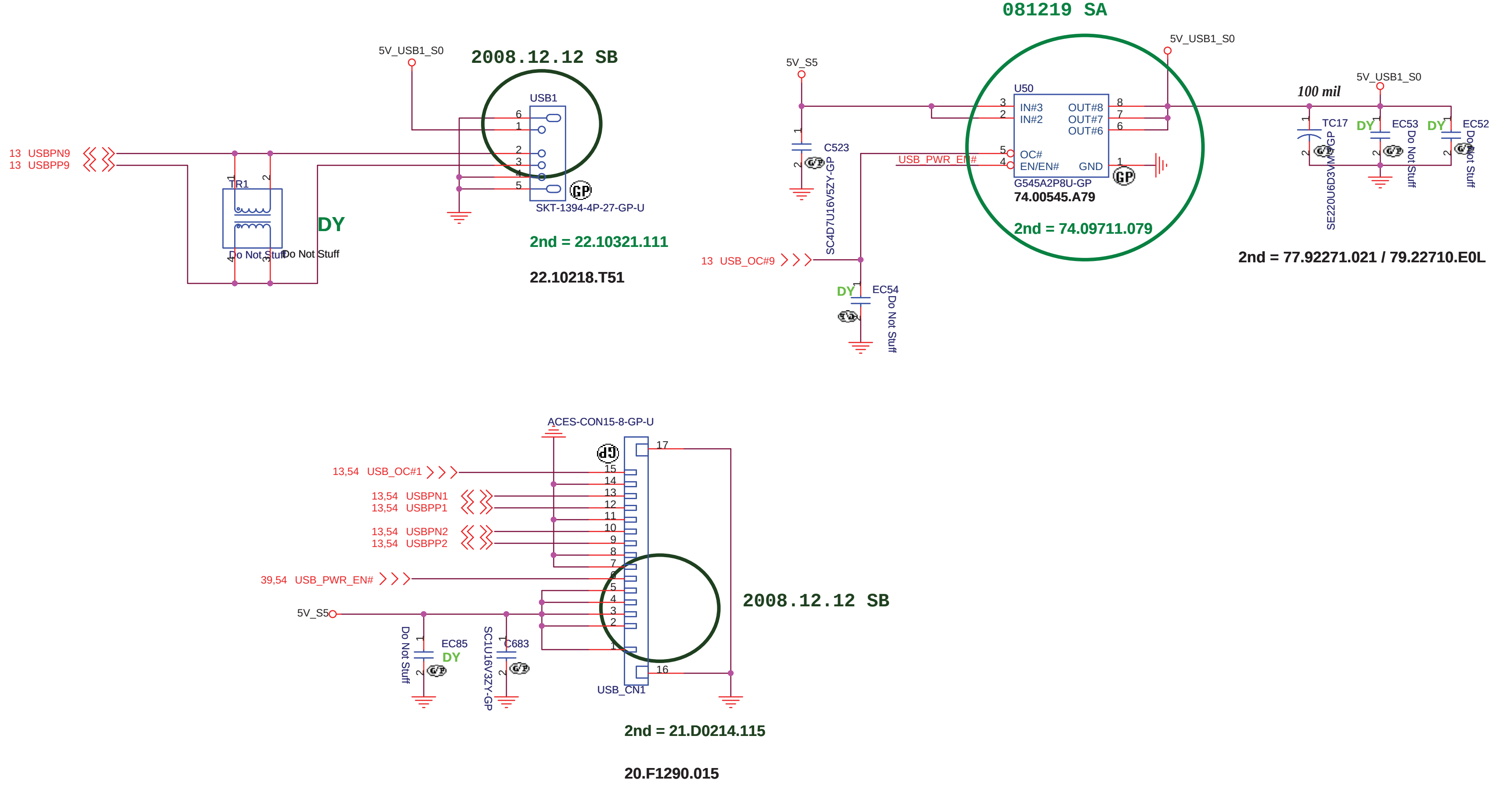
BLUETOOTH MODULE



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*BLUETOOTH*
Size	Document Number: JM70-MV — Rev: SB
Date: Saturday, December 20, 2008	Sheet 26 of 55

USB1 Connector



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB CONN	
Size	Document Number: JM70-MV	Rev: SB
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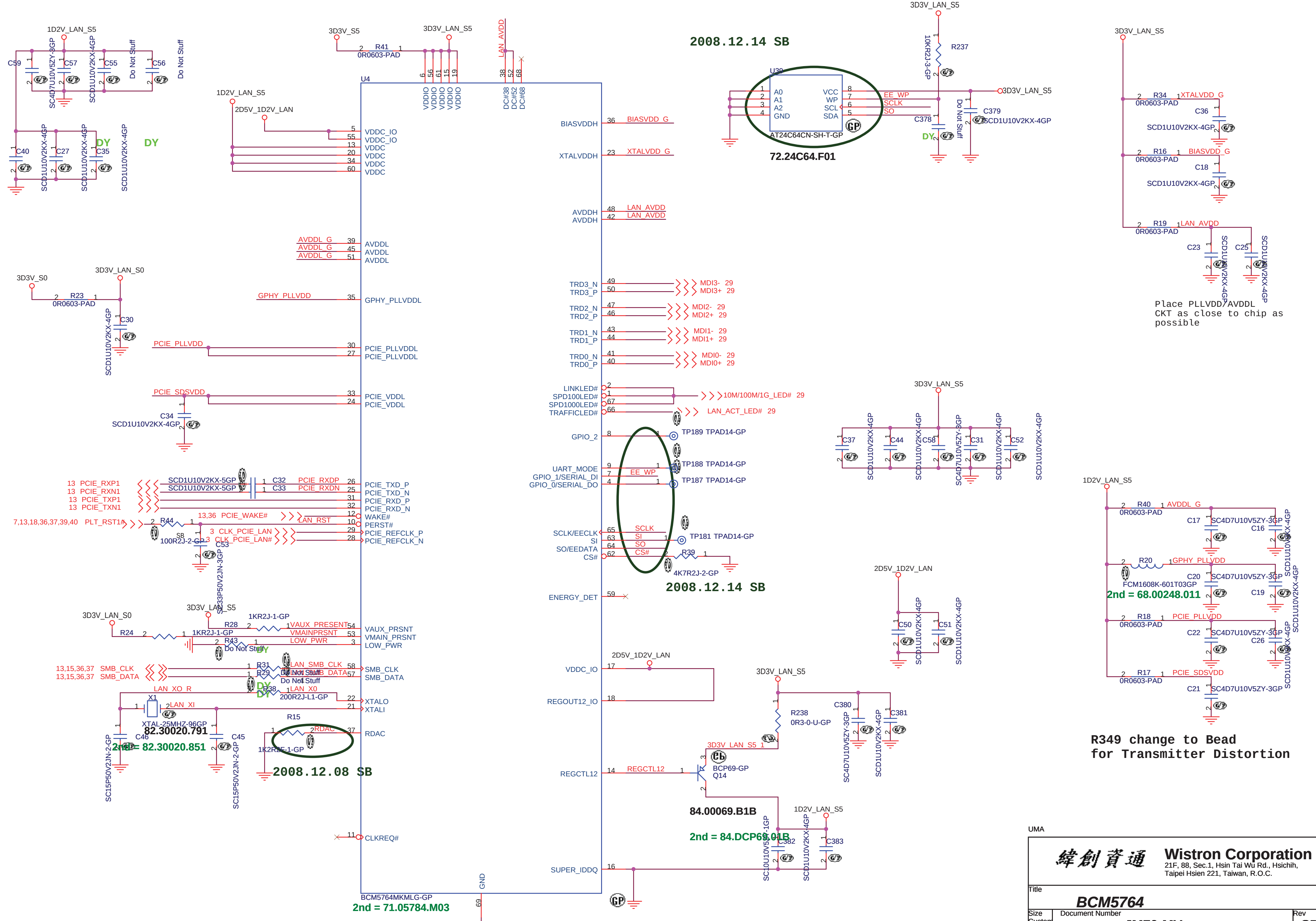

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	BCM5764	
Size: Custom	Document Number: JM70-MV	Rev: SB
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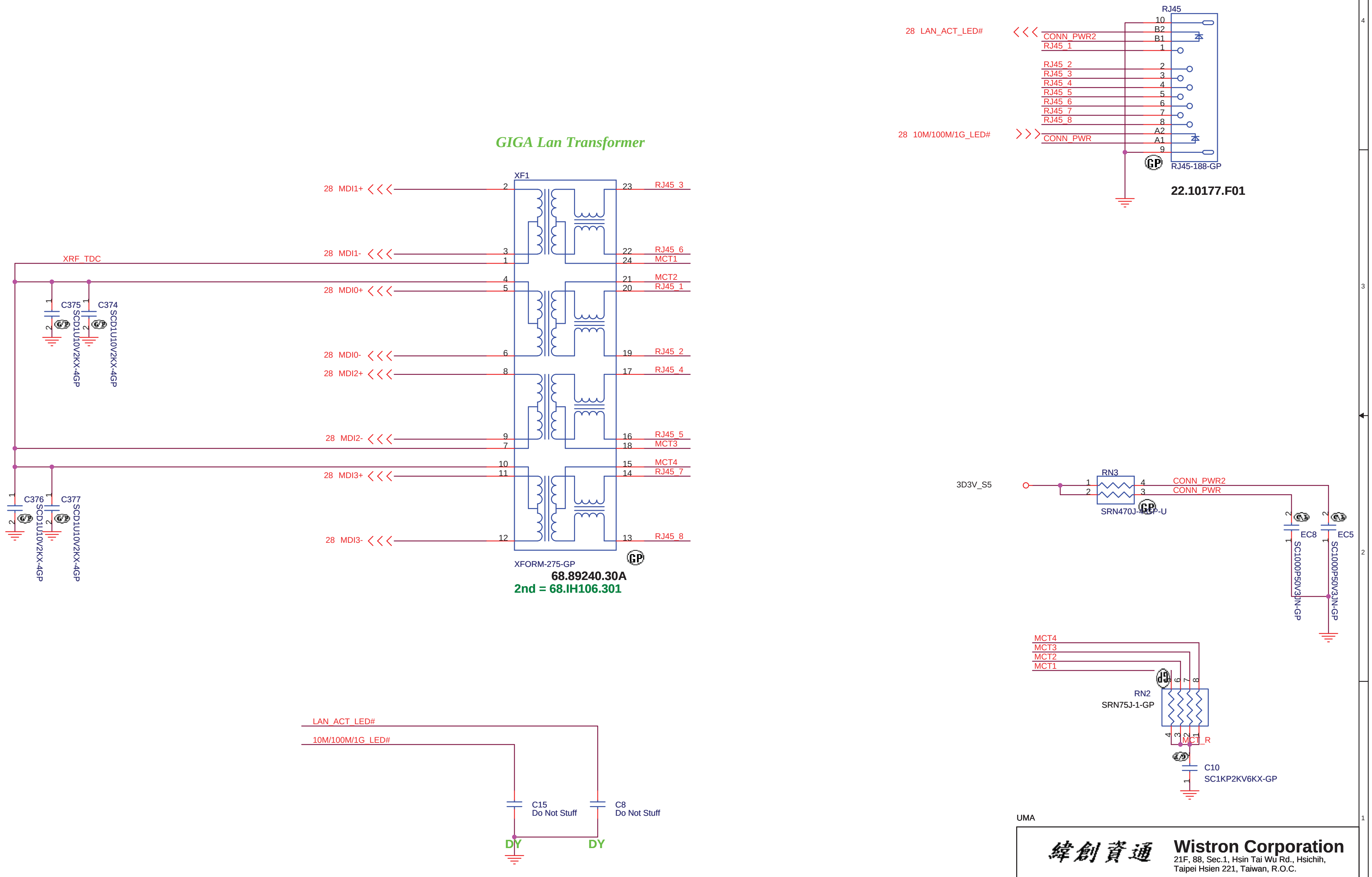
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

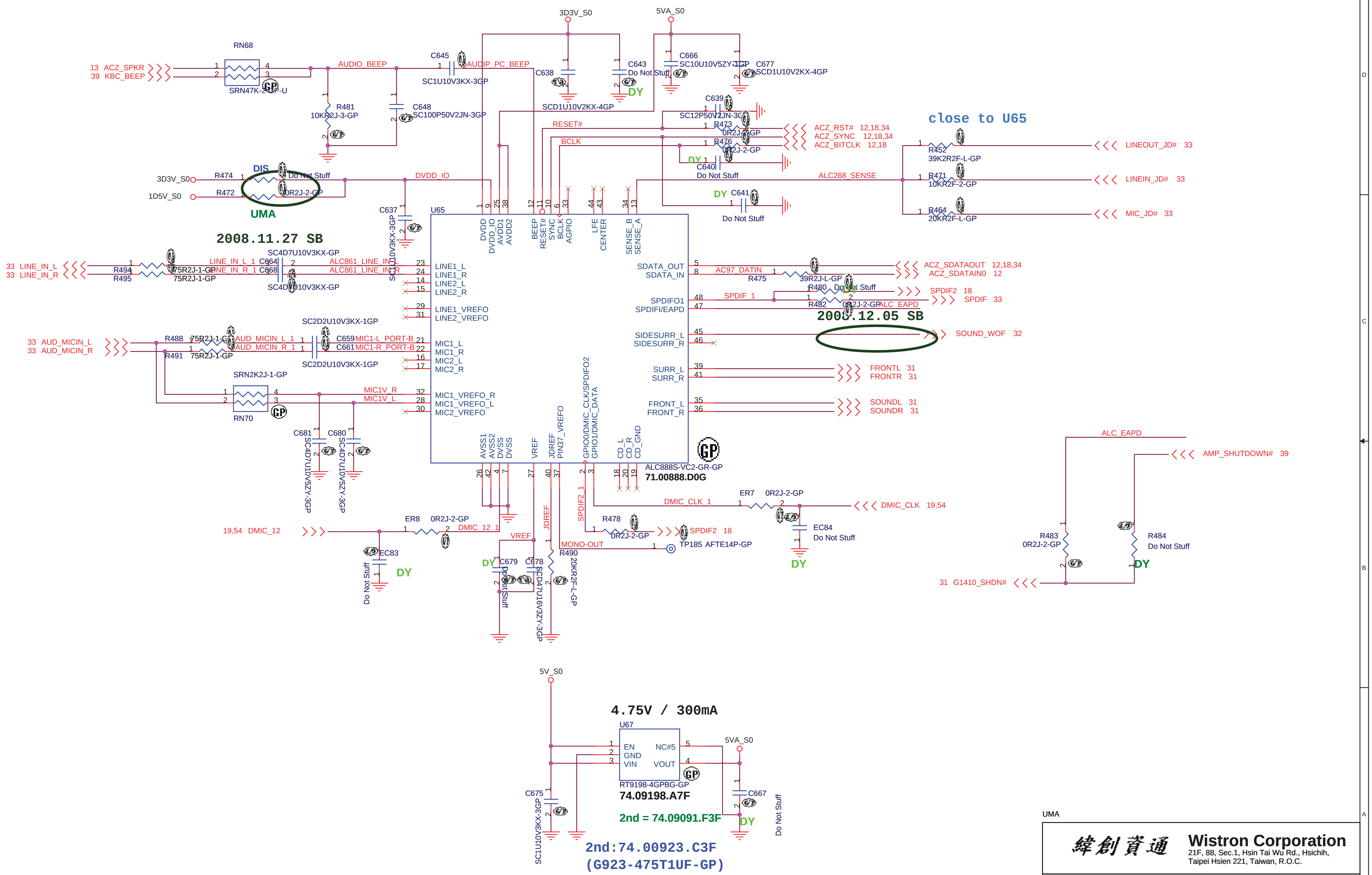
LAN Connector



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN CONN		
Size A3	Document Number JM70-MV		Rev SB
Date: Saturday, December 20, 2008	Sheet 29 of 55		



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Azalia codec ALC888	
Size A3	Document Number JM70-MV	Rev SB
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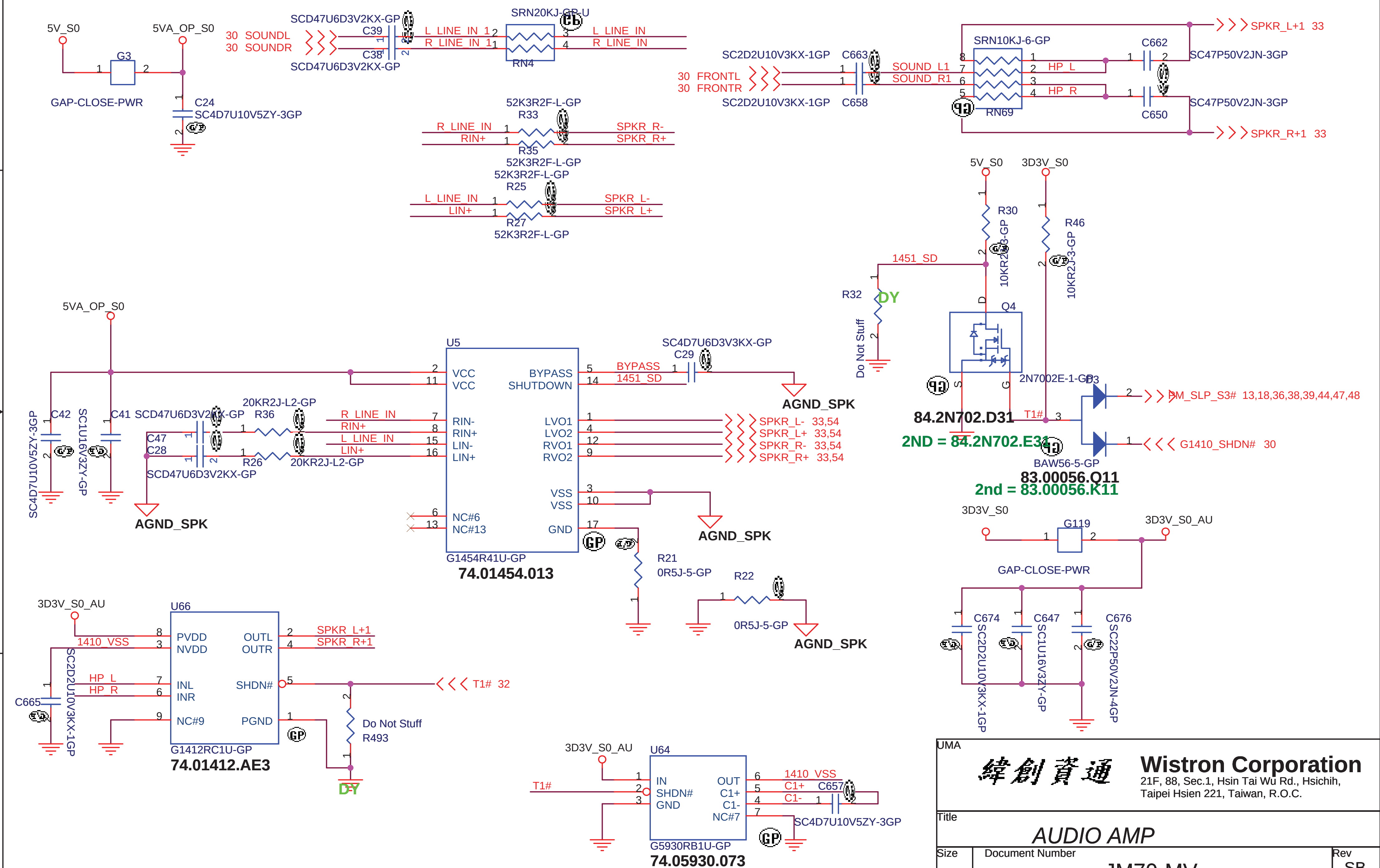
AUDIO OP AMPLIFIER



UMA

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO AMP	
Size	Document Number: JM70-MV	Rev: SB
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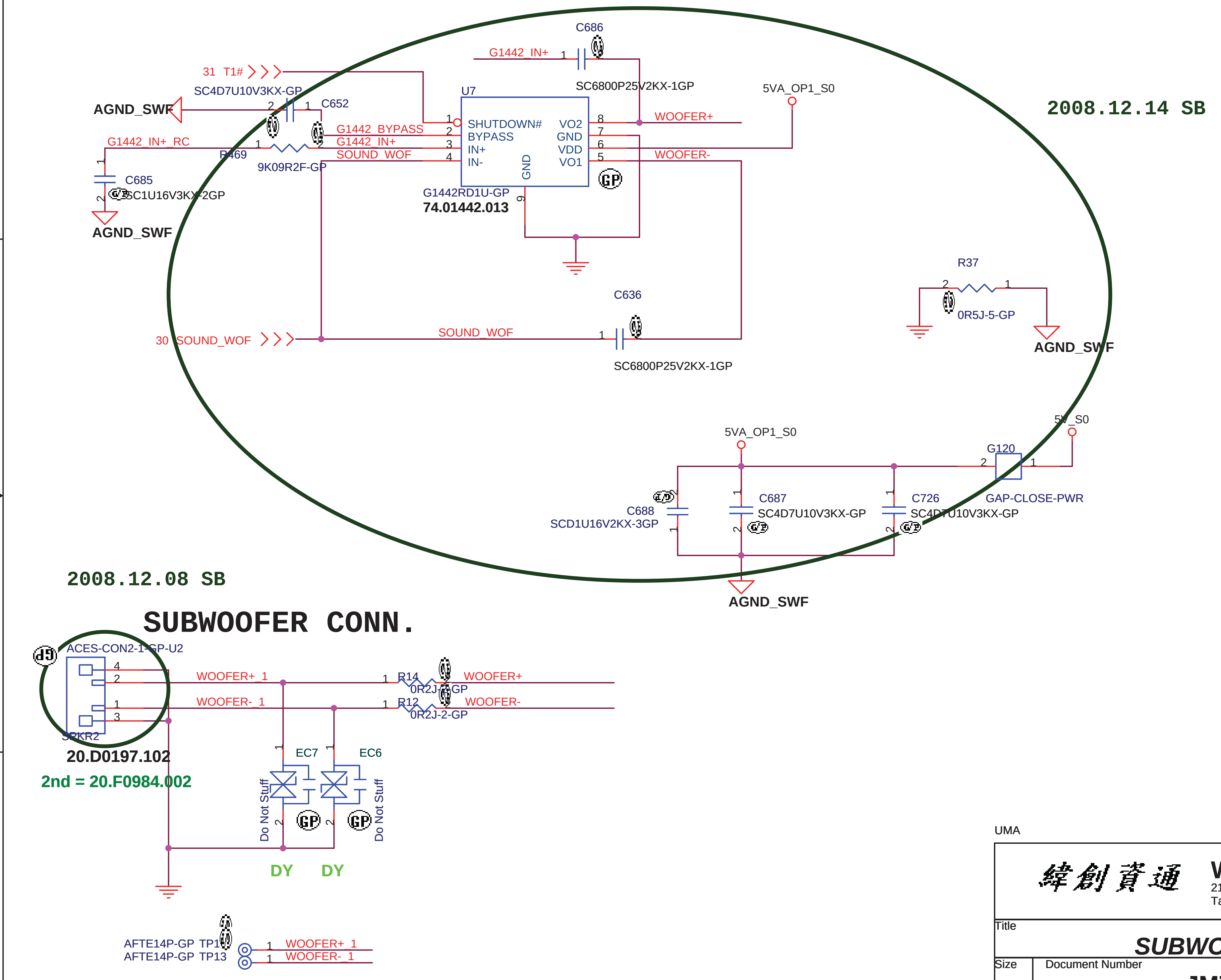
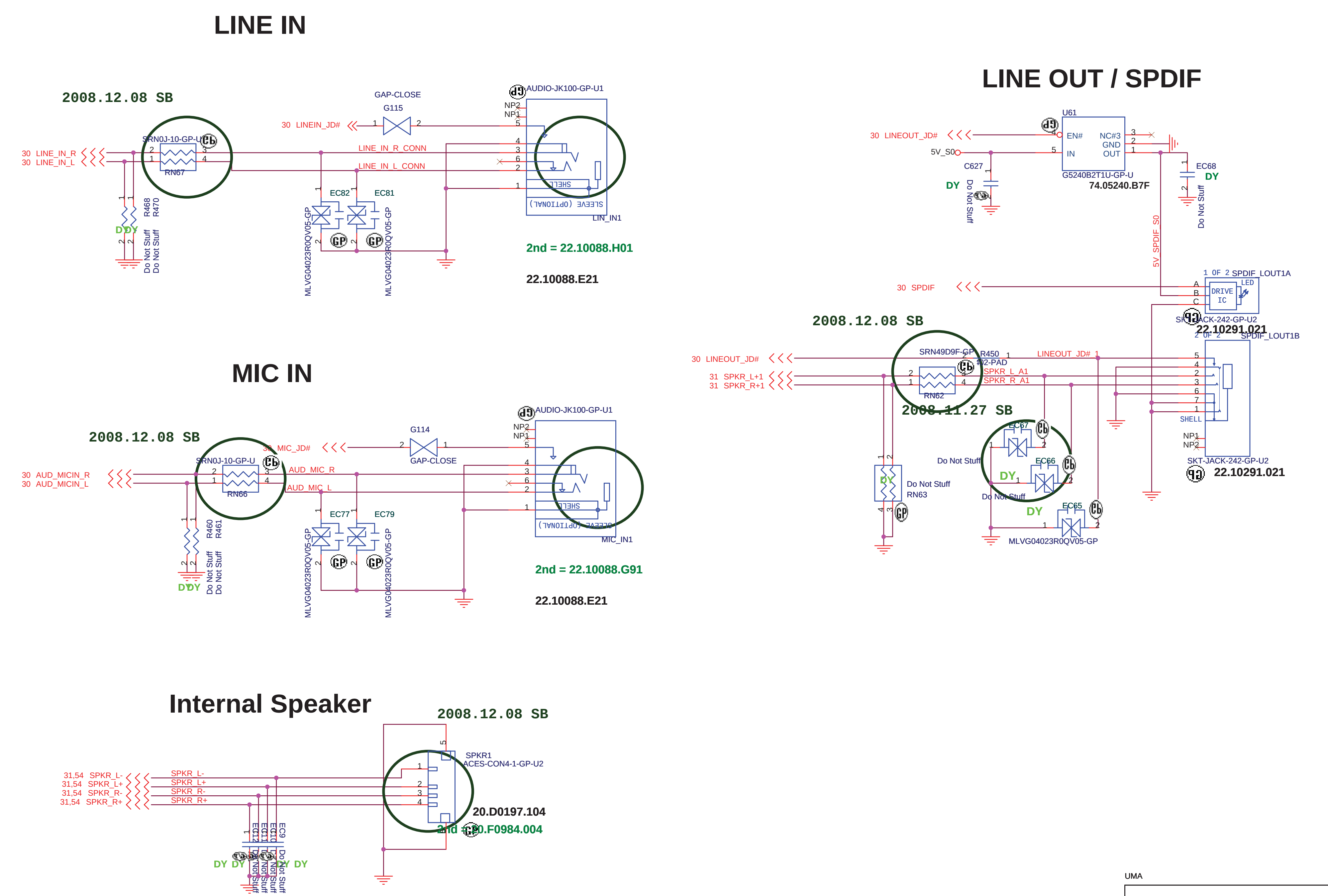


UMA

Wistron Corporation 緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SUBWOOFER CONN.	
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 32 of 55	



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*AUDIO_jack*	
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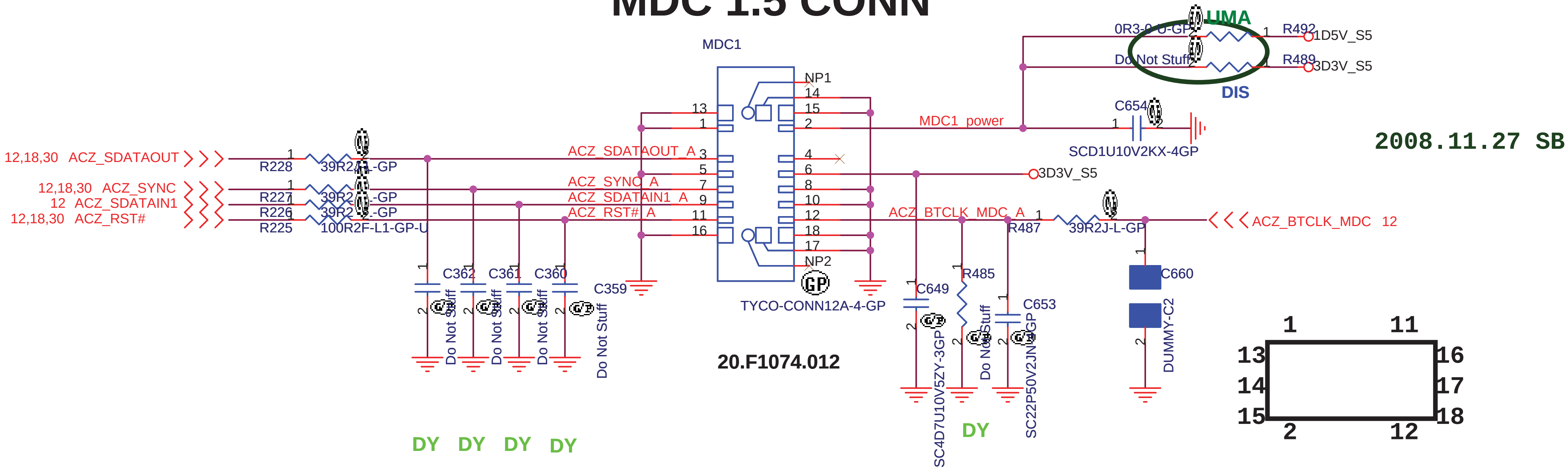
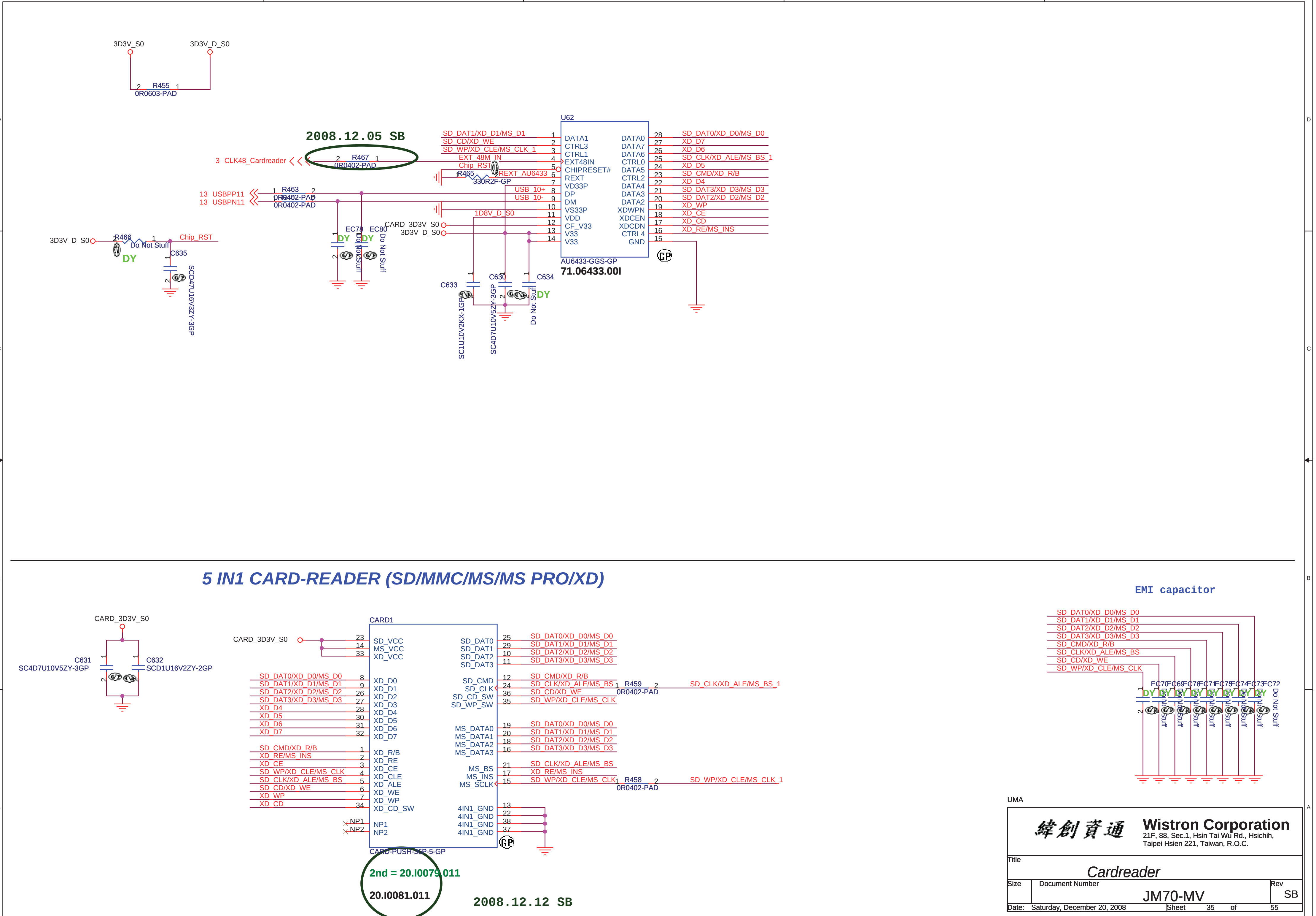
MDC 1.5 CONN



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MDC
Size	
Document Number	JM70-MV
Rev	SB
Date:	Saturday, December 20, 2008
Sheet	34 of 55



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	Cardreader
Size / Document Number	JM70-MV
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Date:	Saturday, December 20, 2008
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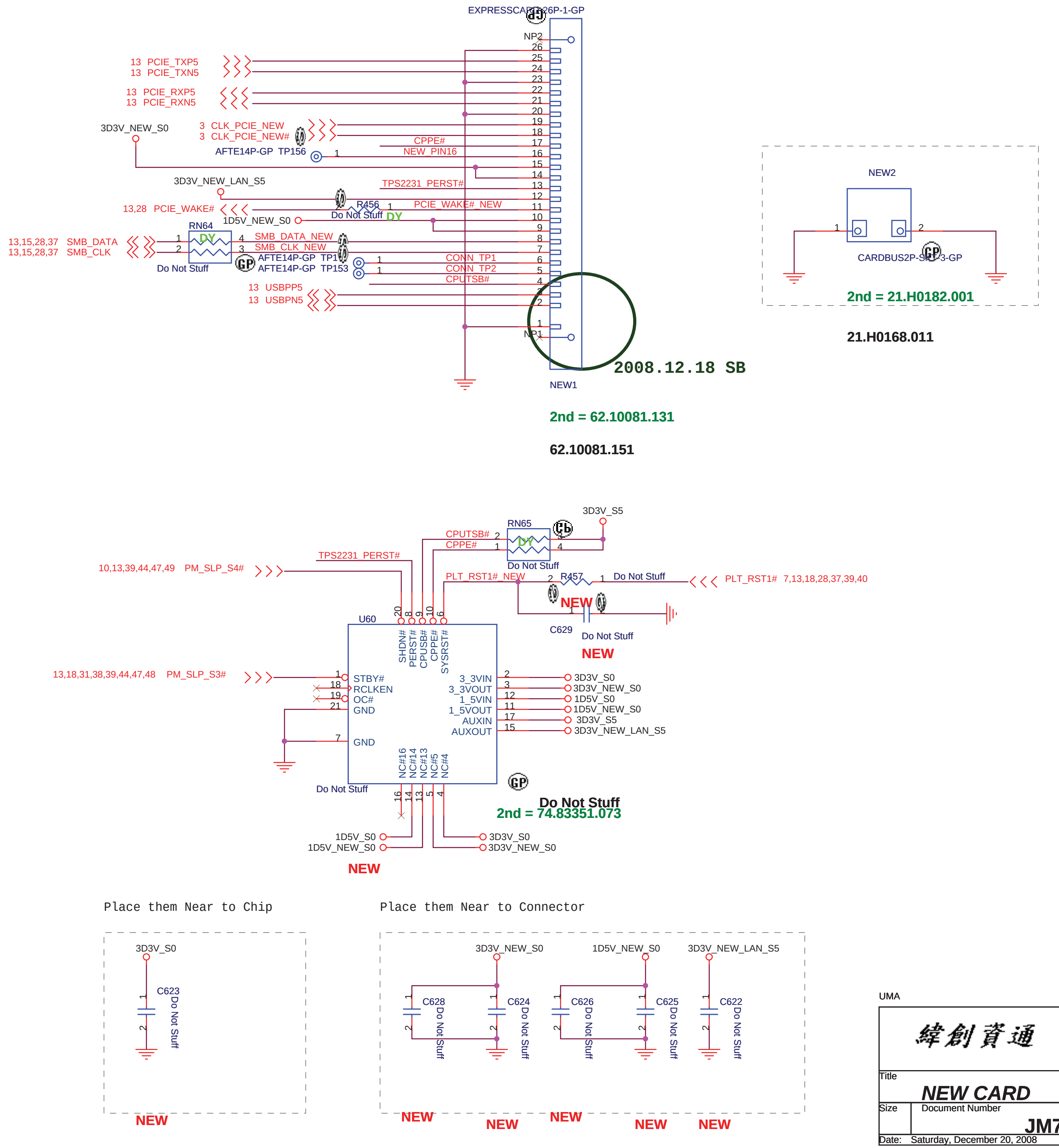

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NEW CARD	
Size	Document Number: JM70-MV	Rev: SB
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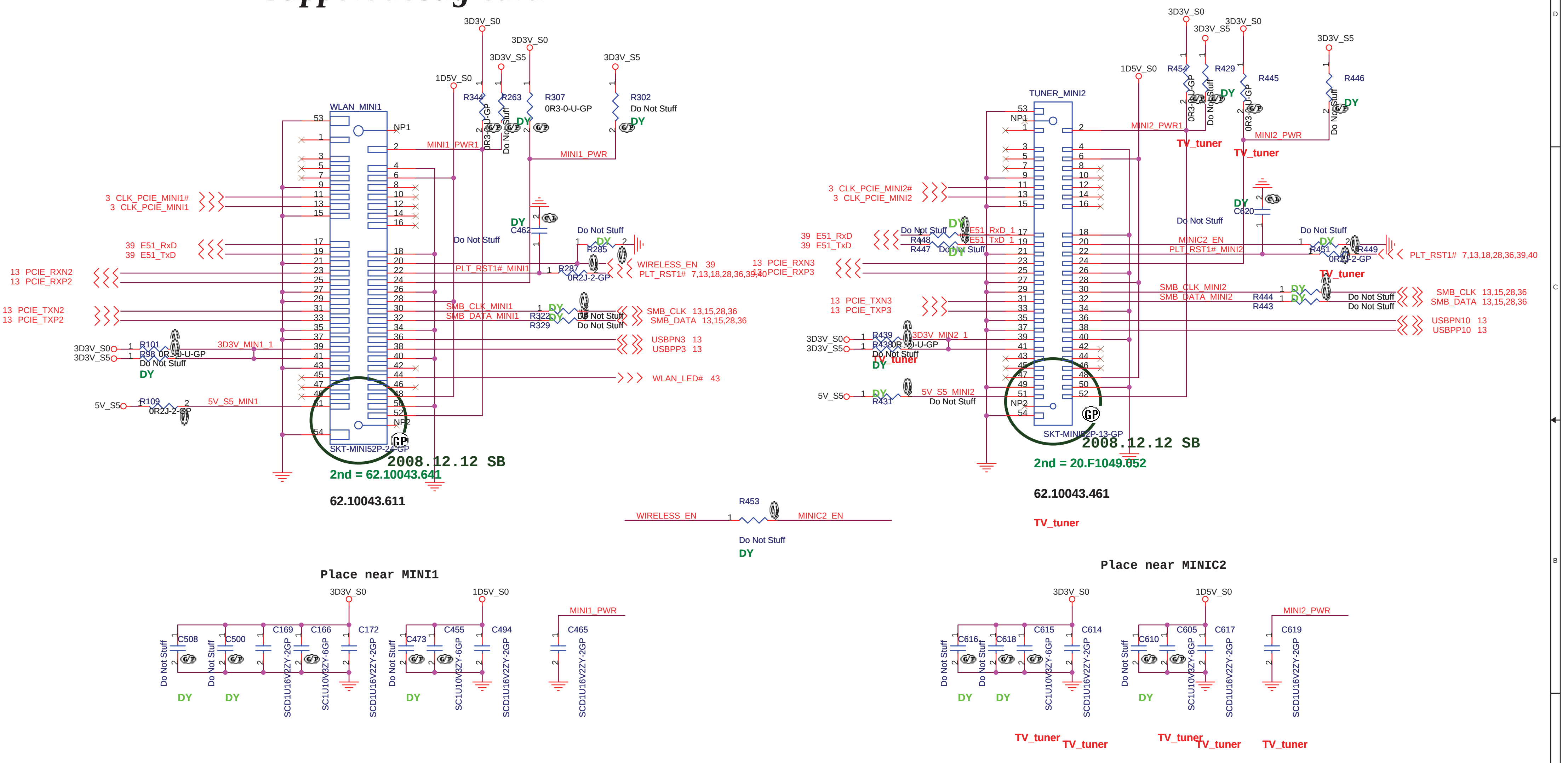
Mini1 Card Connector(WLAN) Support debug-card

Mini2 Card Connector(TV tuner)



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINI CARD	
Size A3	Document Number JM70-MV	Rev SB
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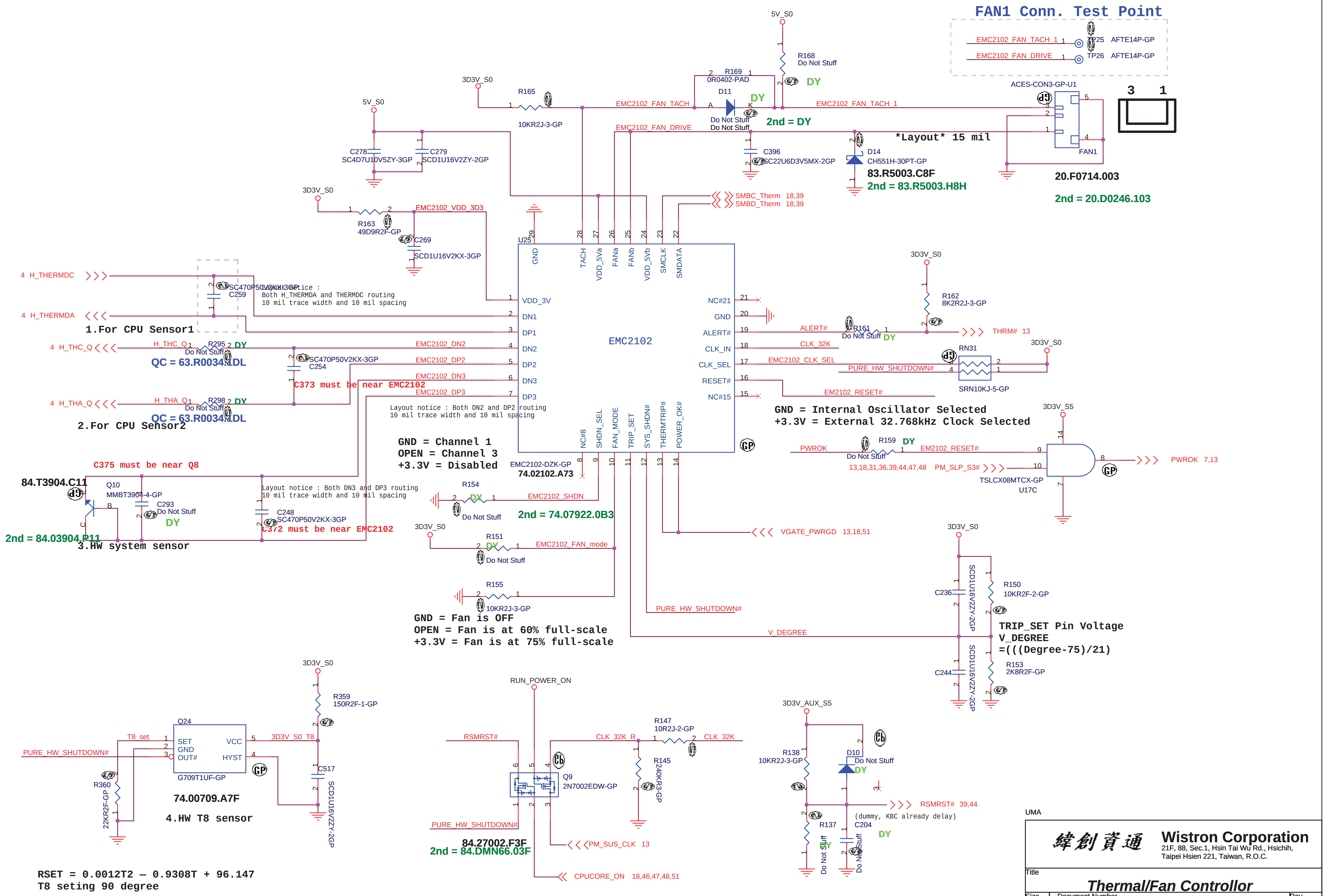

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Thermal/Fan Controllor		
Size	Document Number: JM70-MV	Rev: SB
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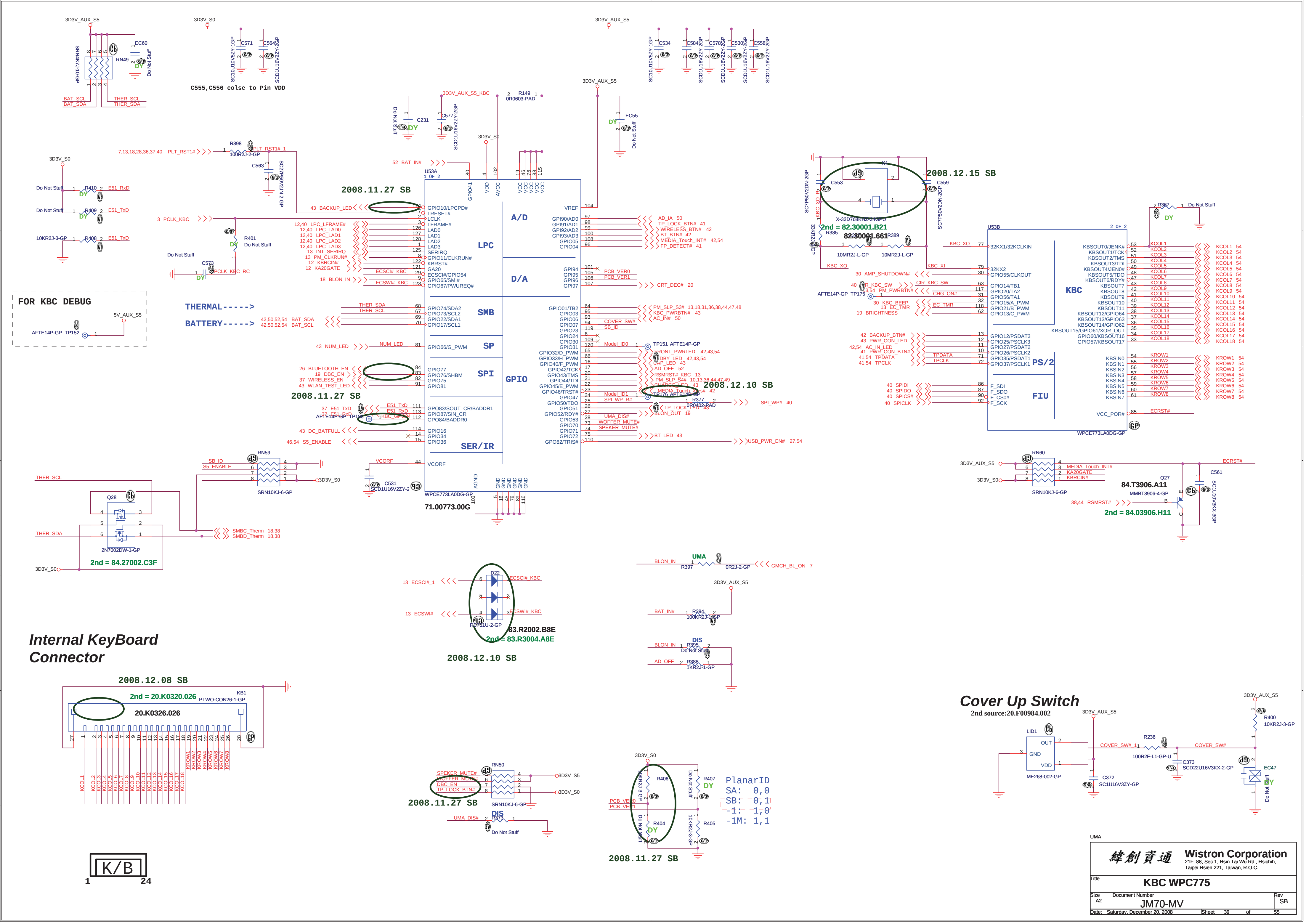

FOR KBC DEBUG
THERMAL----->
BATTERY----->
2008.11.27 SB
2008.12.15 SB
2nd = 82.30001.B21
82.30001.661
2008.12.10 SB
U53A
U53B
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
WPCE773LA0DG-GP
71.00773.00G
84.T3906.A11
2nd = 84.03906.H11
2nd = 84.27002.C3F
83.R2002.B8E
2nd = 83.R3004.A8E
Internal KeyBoard Connector
2008.12.08 SB
2nd = 20.K0320.026
20.K0326.026
PTWO-CON26-1-GP
K/B
1
24
Cover Up Switch
2nd source:20.F00984.002
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC WPC775
Size A2
Document Number
JM70-MV
Rev SB
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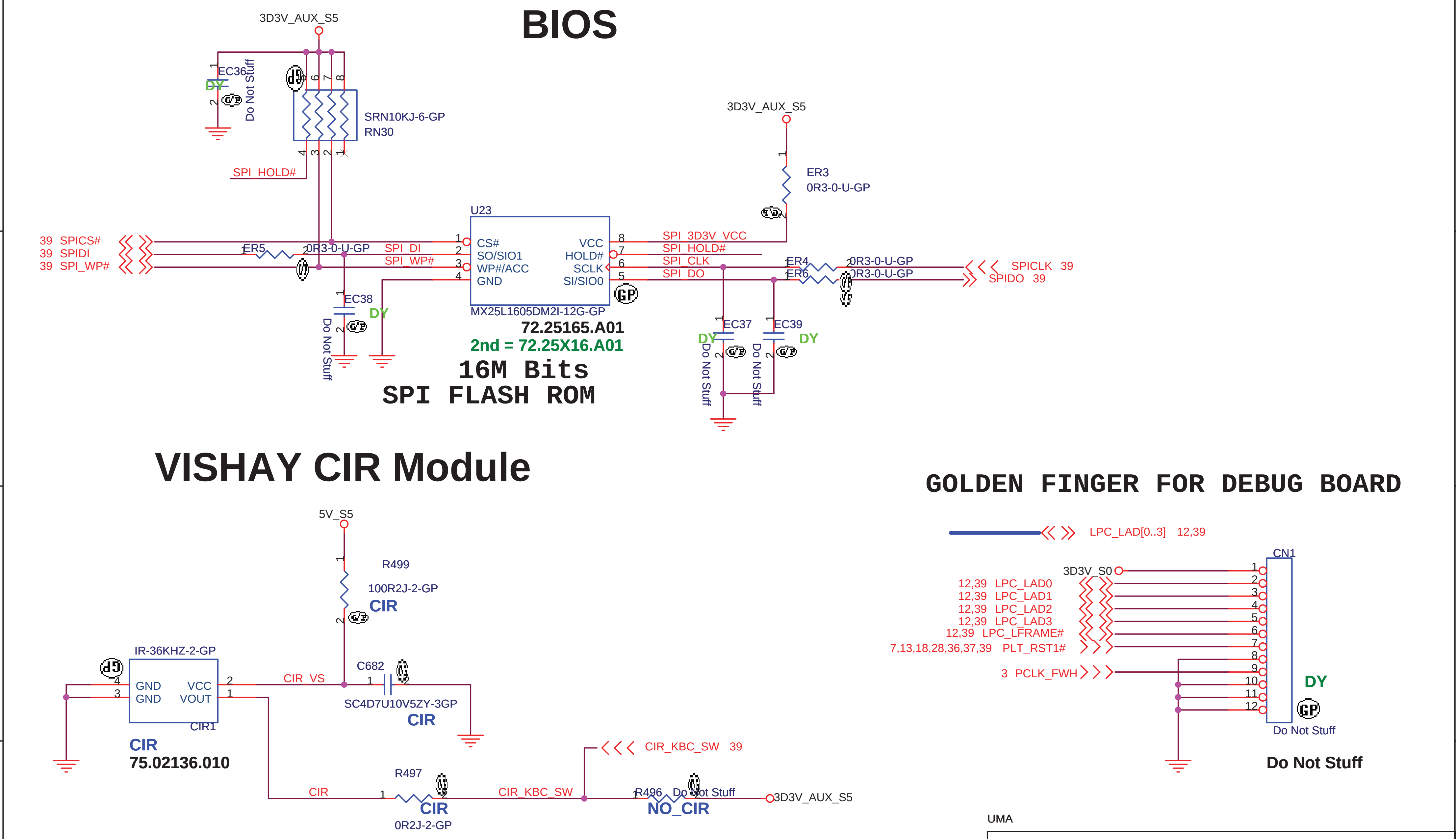
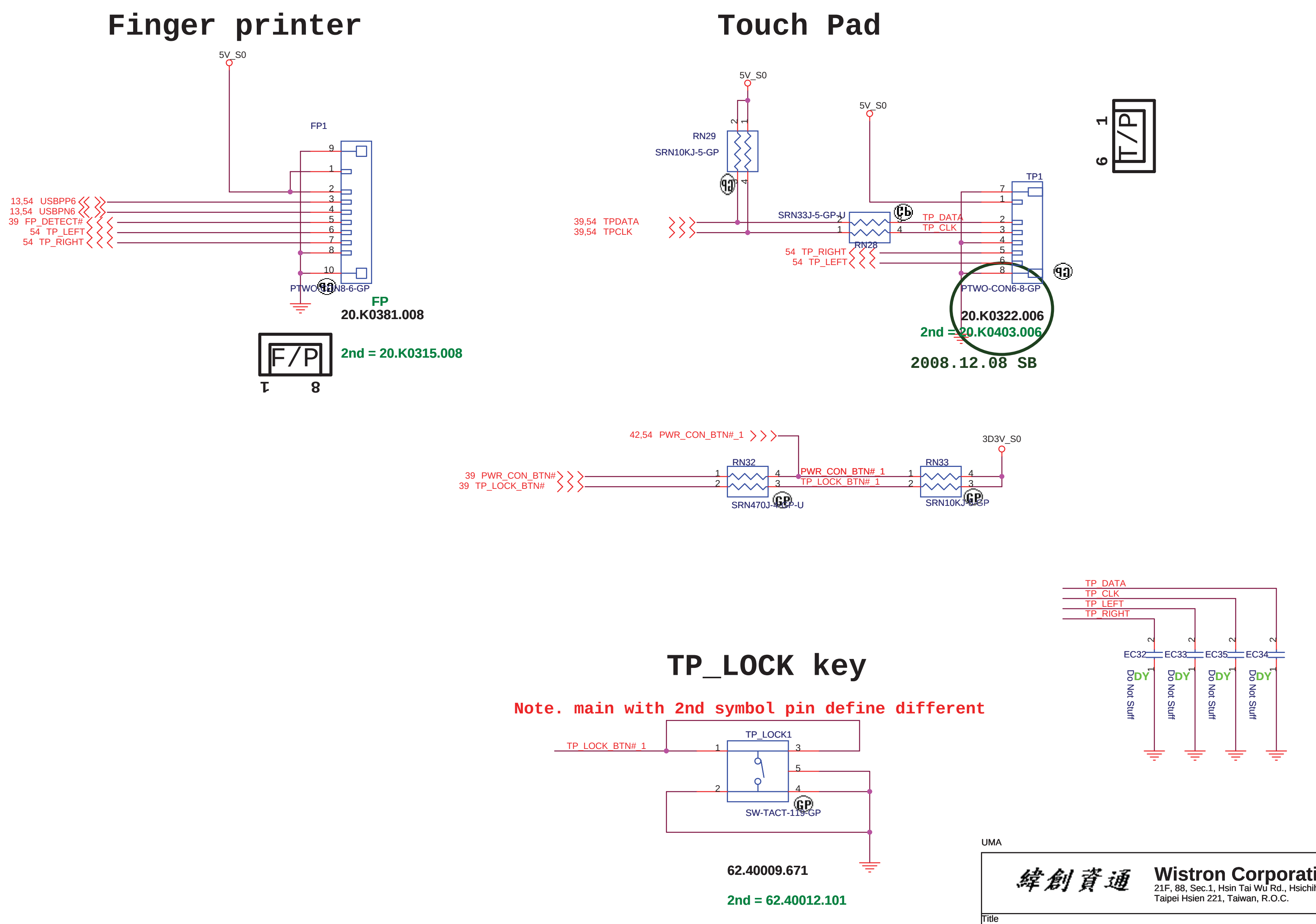
Sheet 39 of 55



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
	BIOS		
Size	Document Number: JM70-MV		Rev: SB
Date: Saturday, December 20, 2008		Sheet 40 of 55	



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Touch PAD and FP
Size / Document Number	JM70-MV
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Date:	Saturday, December 20, 2008
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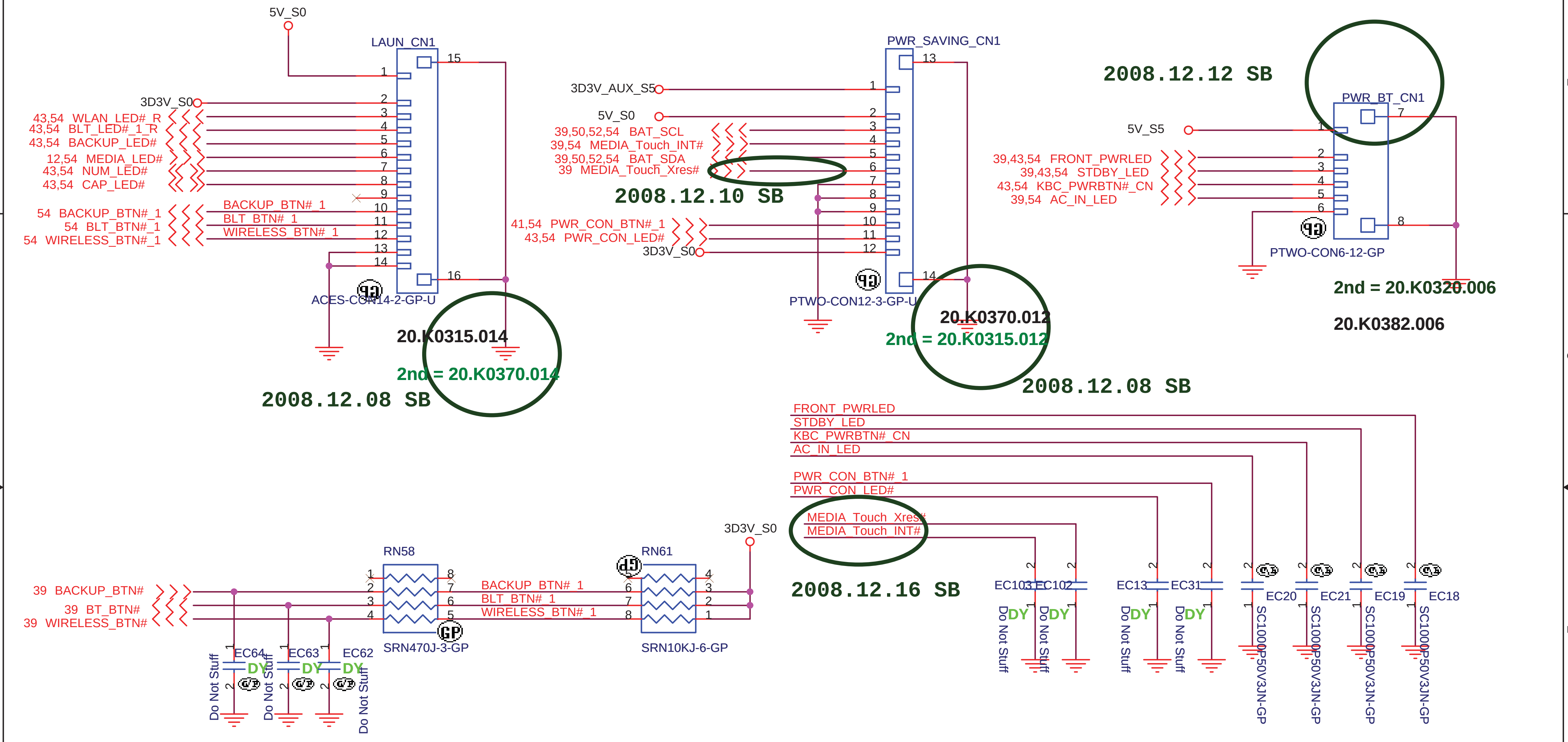

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Launch CN**	
Size A4	Document Number **JM70-MV**	Rev **SB**
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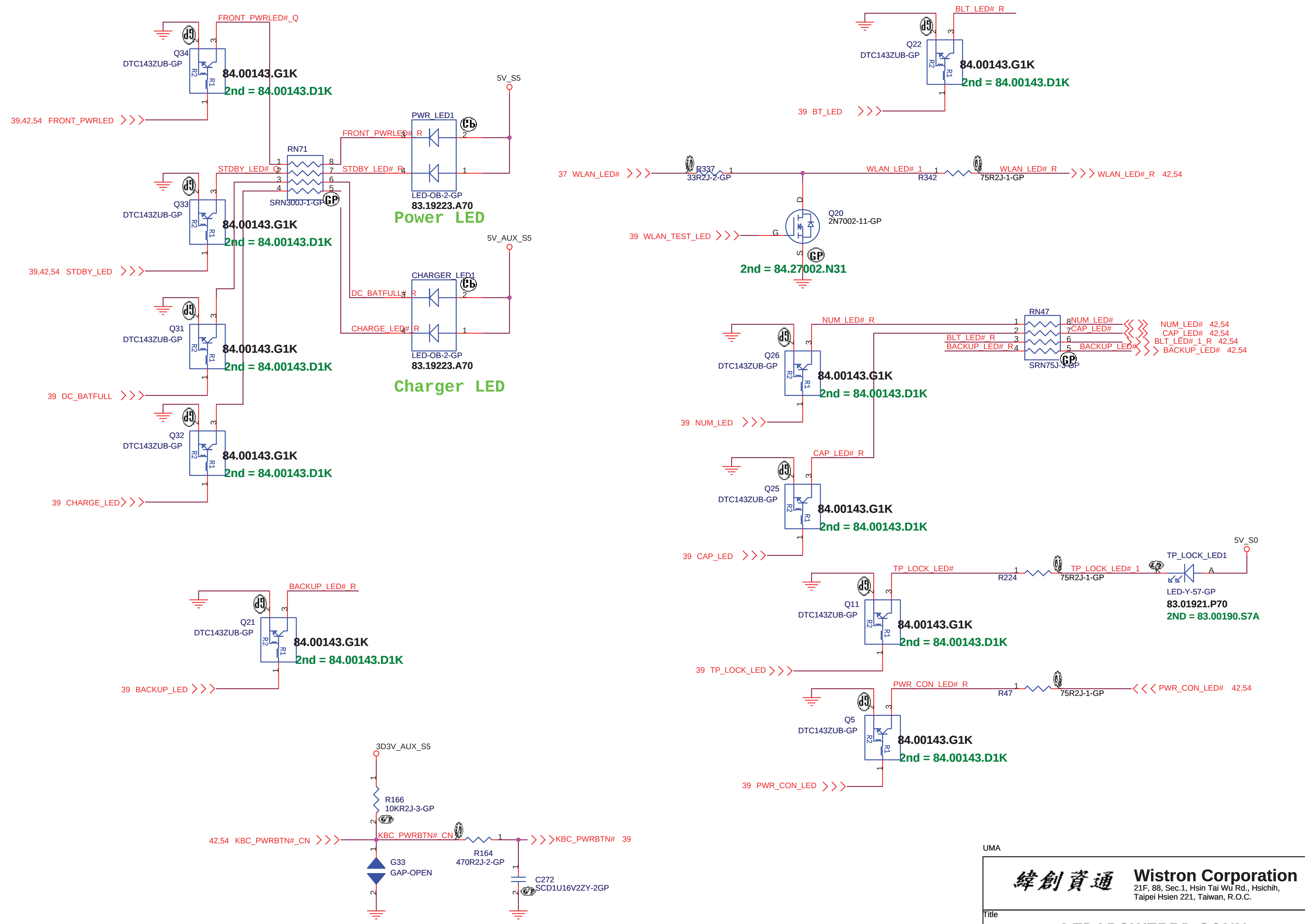
LED



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	LED&POWERBD CONN	
Size	Document Number: JM70-MV	Rev: SB
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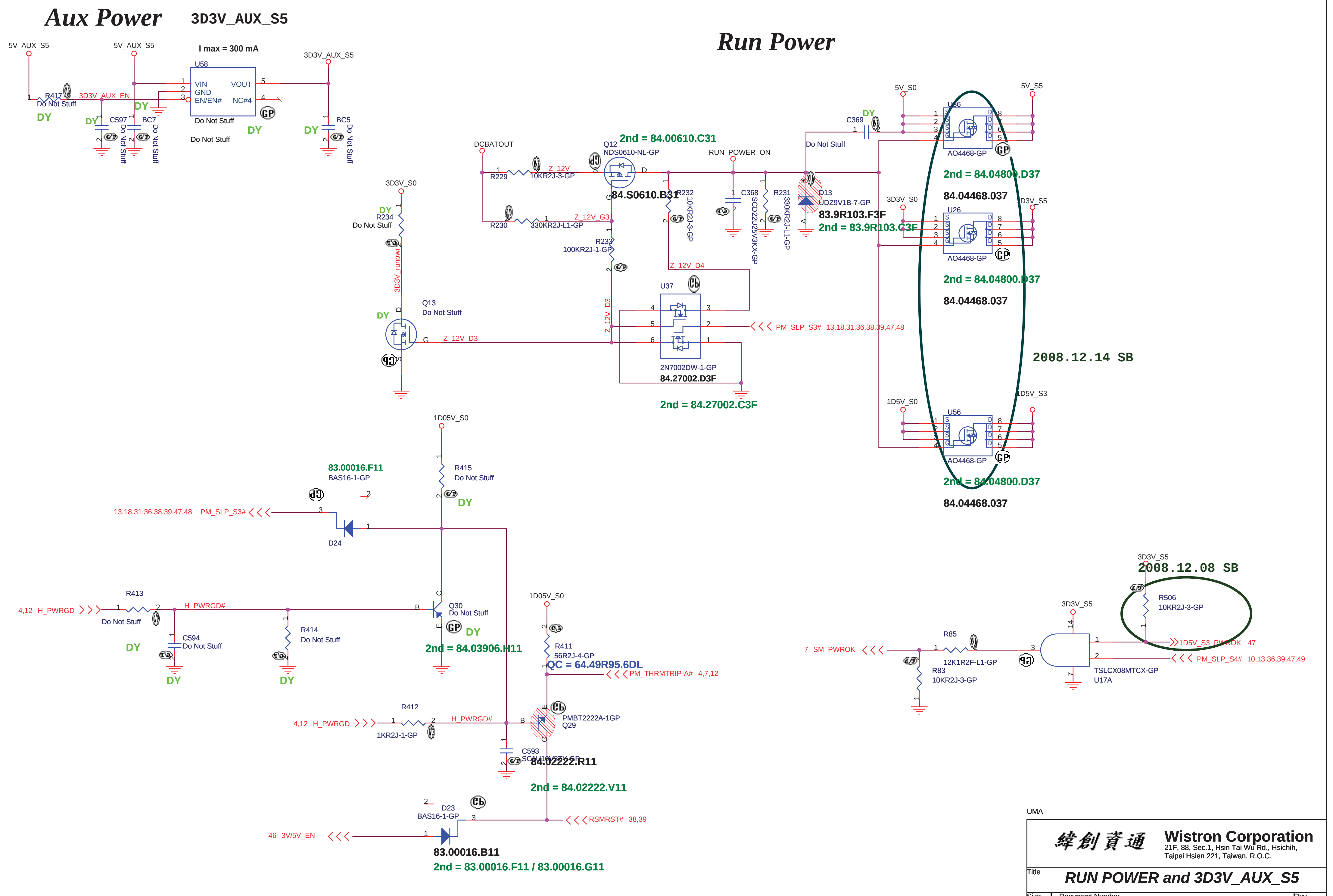

UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER and 3D3V_AUX_S5	
Size	Document Number: JM70-MV	Rev: SB
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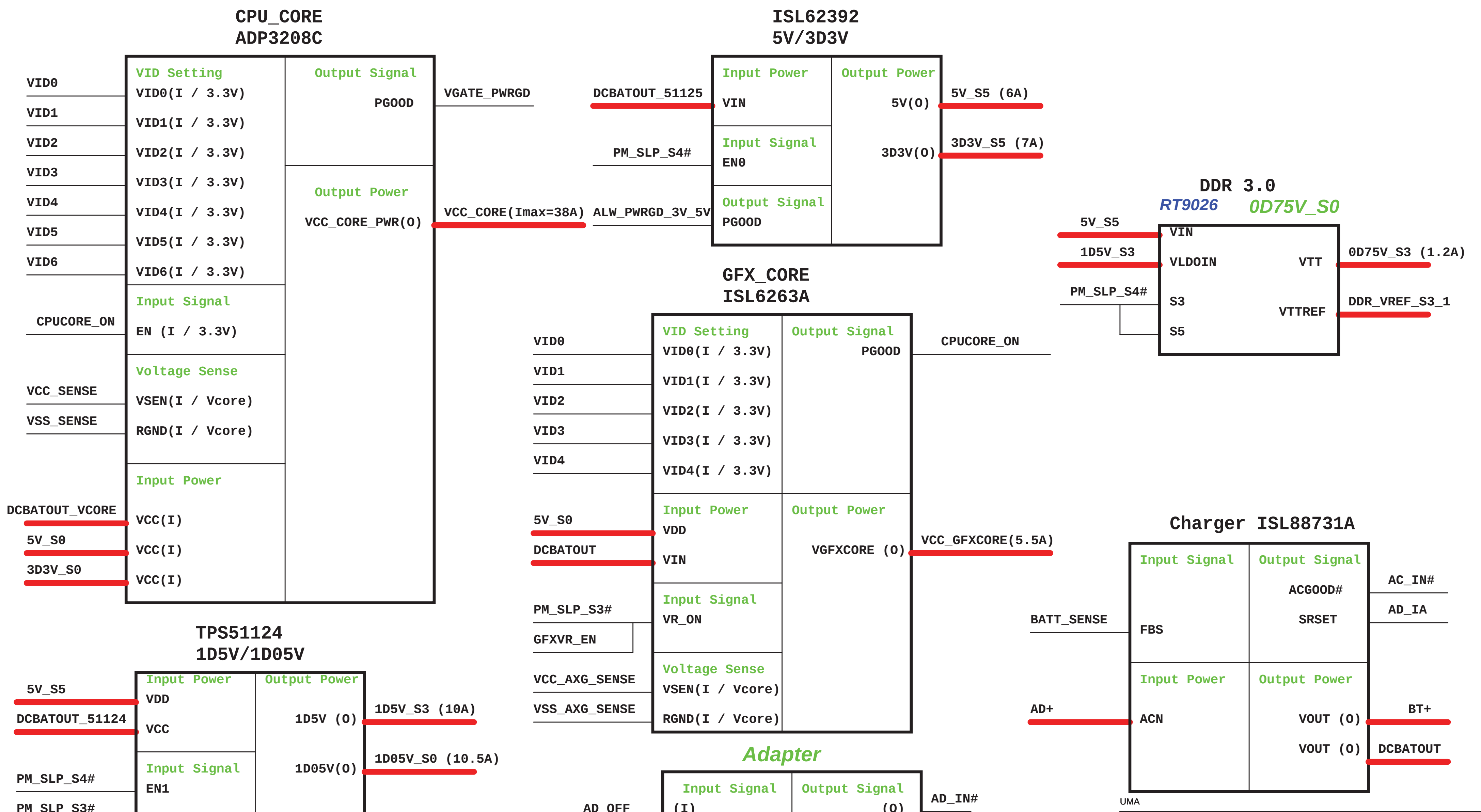

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power Block Diagram*

Size	Document Number	Rev
B	JM70-MV	SB

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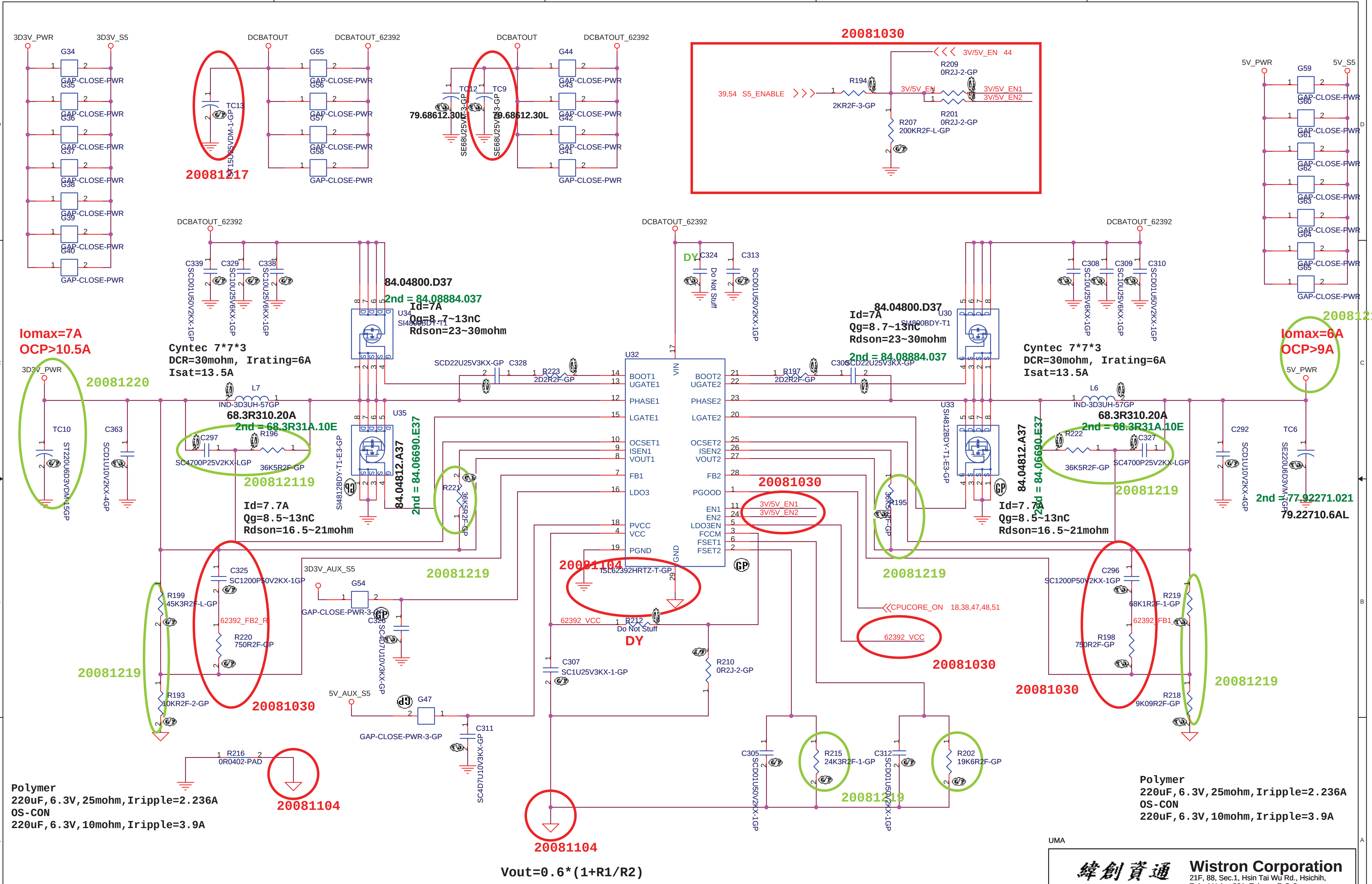

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ISL62392 5V/3D3V	
Size A3	Document Number JM70-MV	Rev SB
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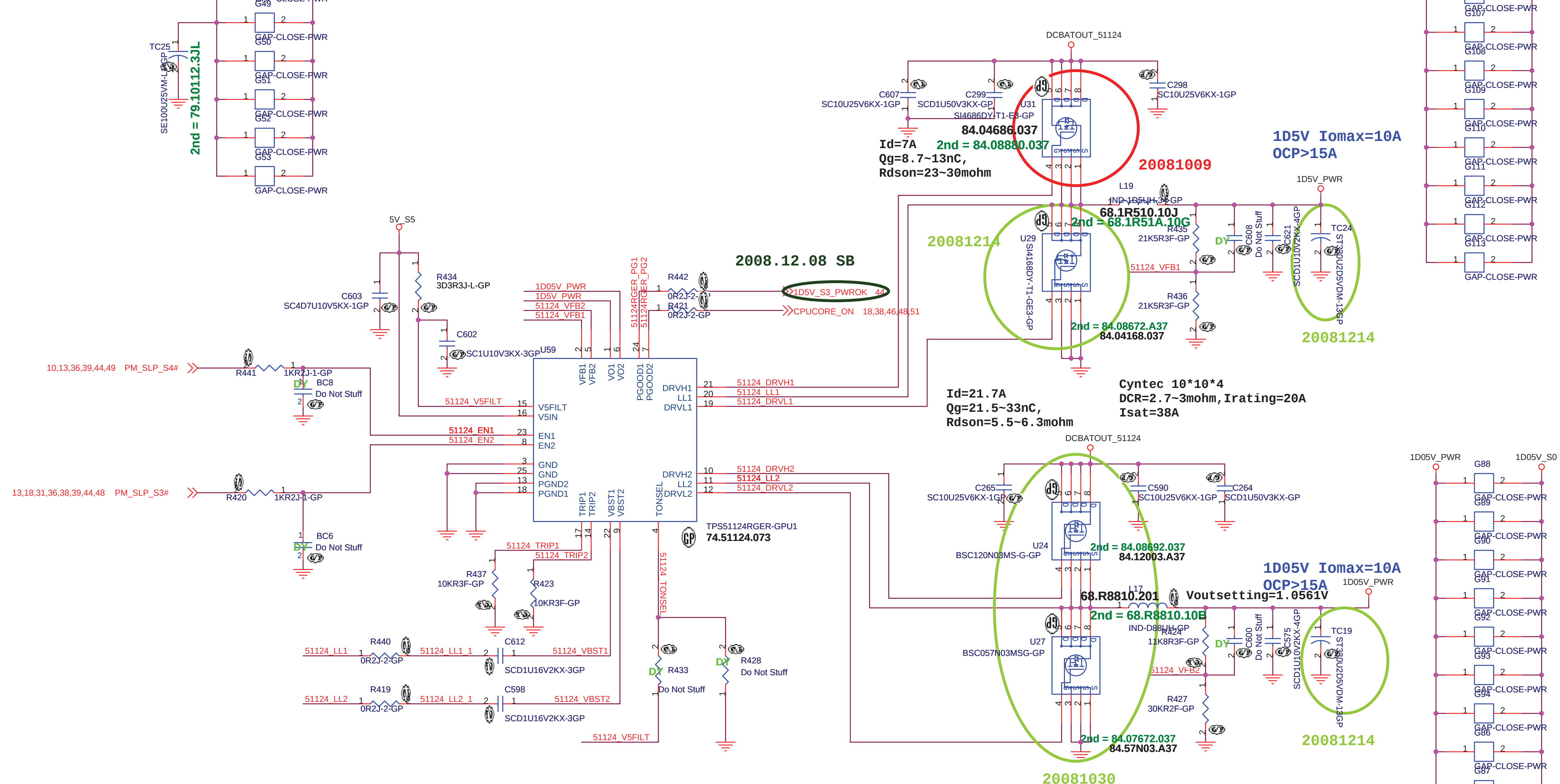
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

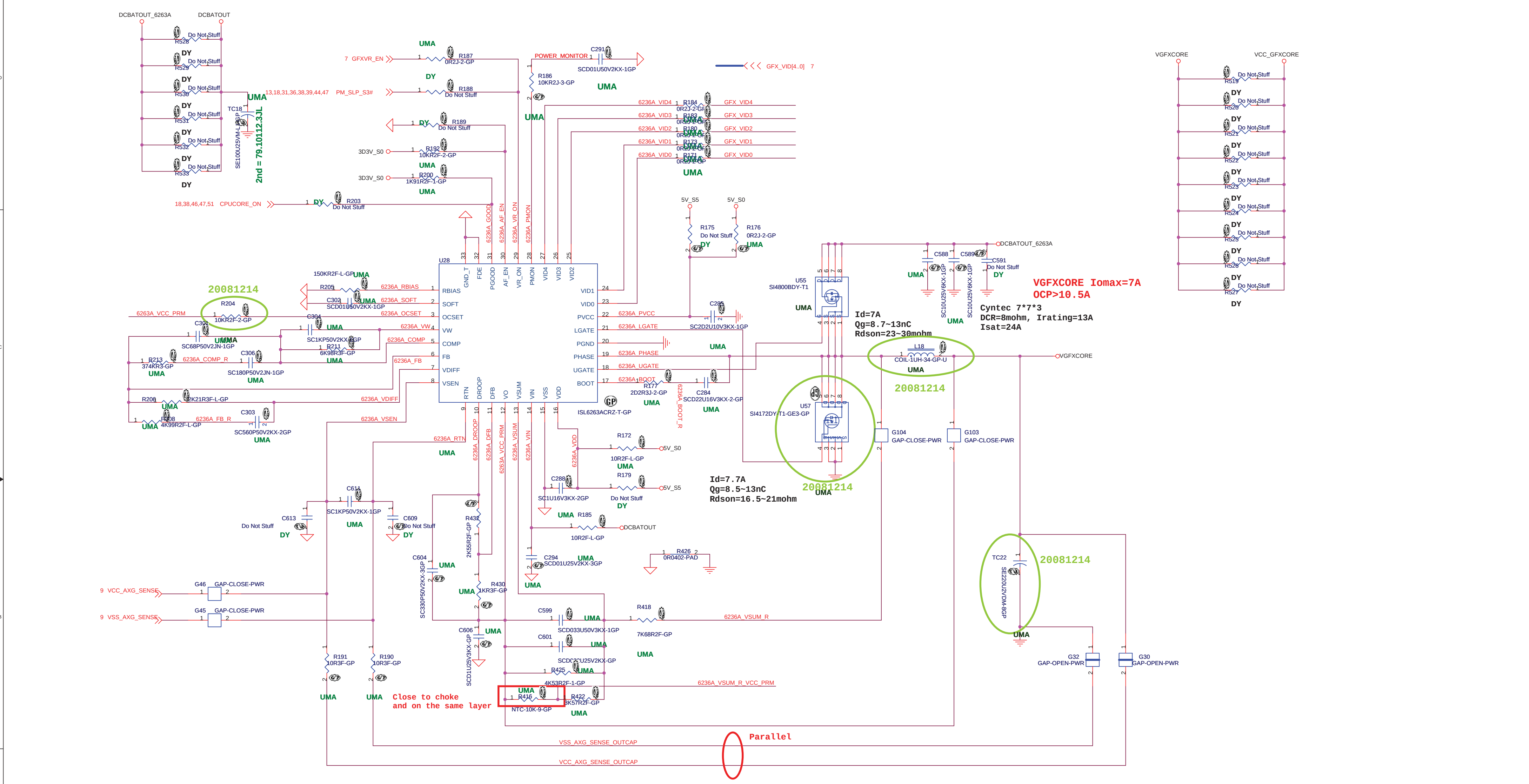
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D5V_1D05V

Size: A3 | Document Number: JM70-MV | Rev: SB

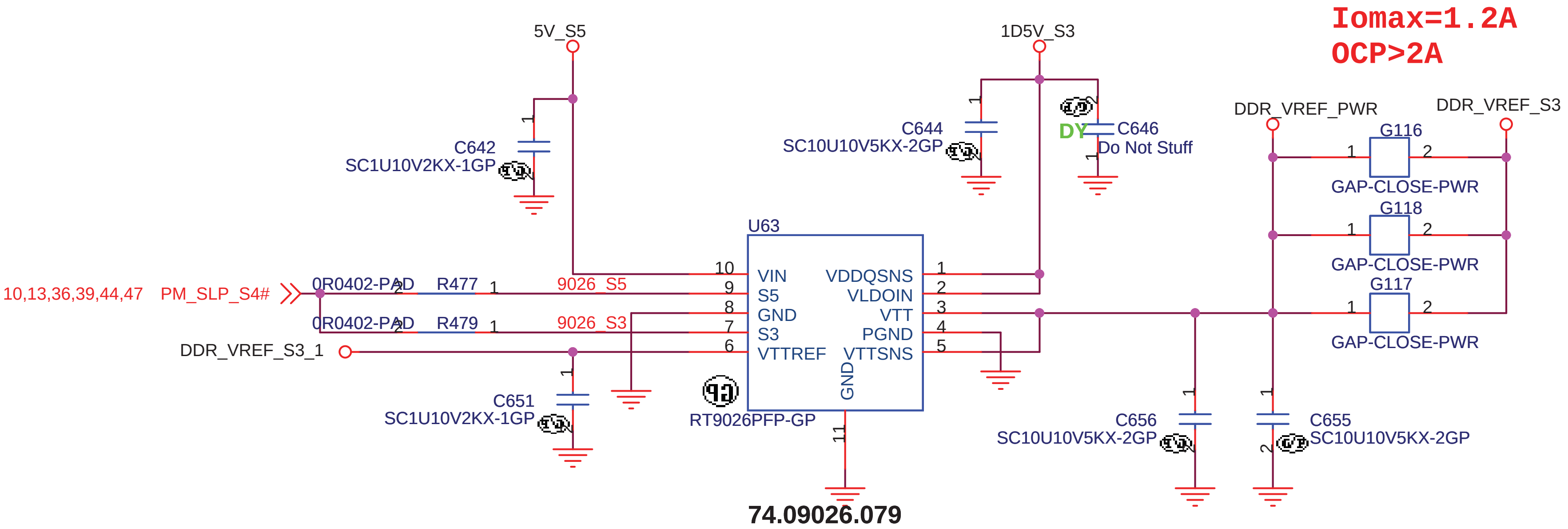
Date: Saturday, December 20, 2008 | Sheet 47 of 55



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ISL6263A_GFX CORE		
Size A2	Document Number JM70-MV		Rev SB
Date: Saturday, December 20, 2008	Sheet 48	of 55	



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **0D75V**

Size	Document Number	Rev
A	JM70-MV	SB

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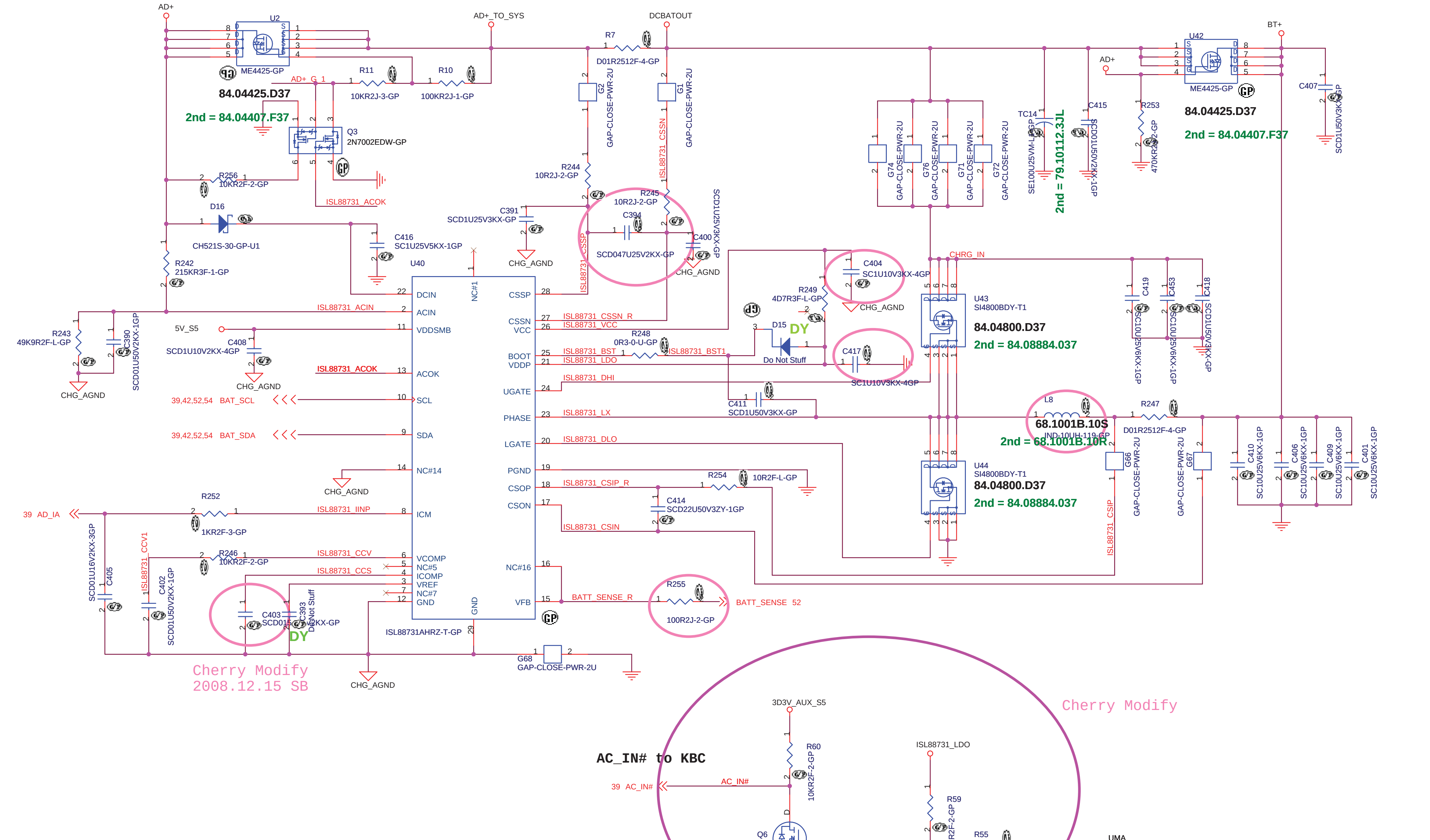
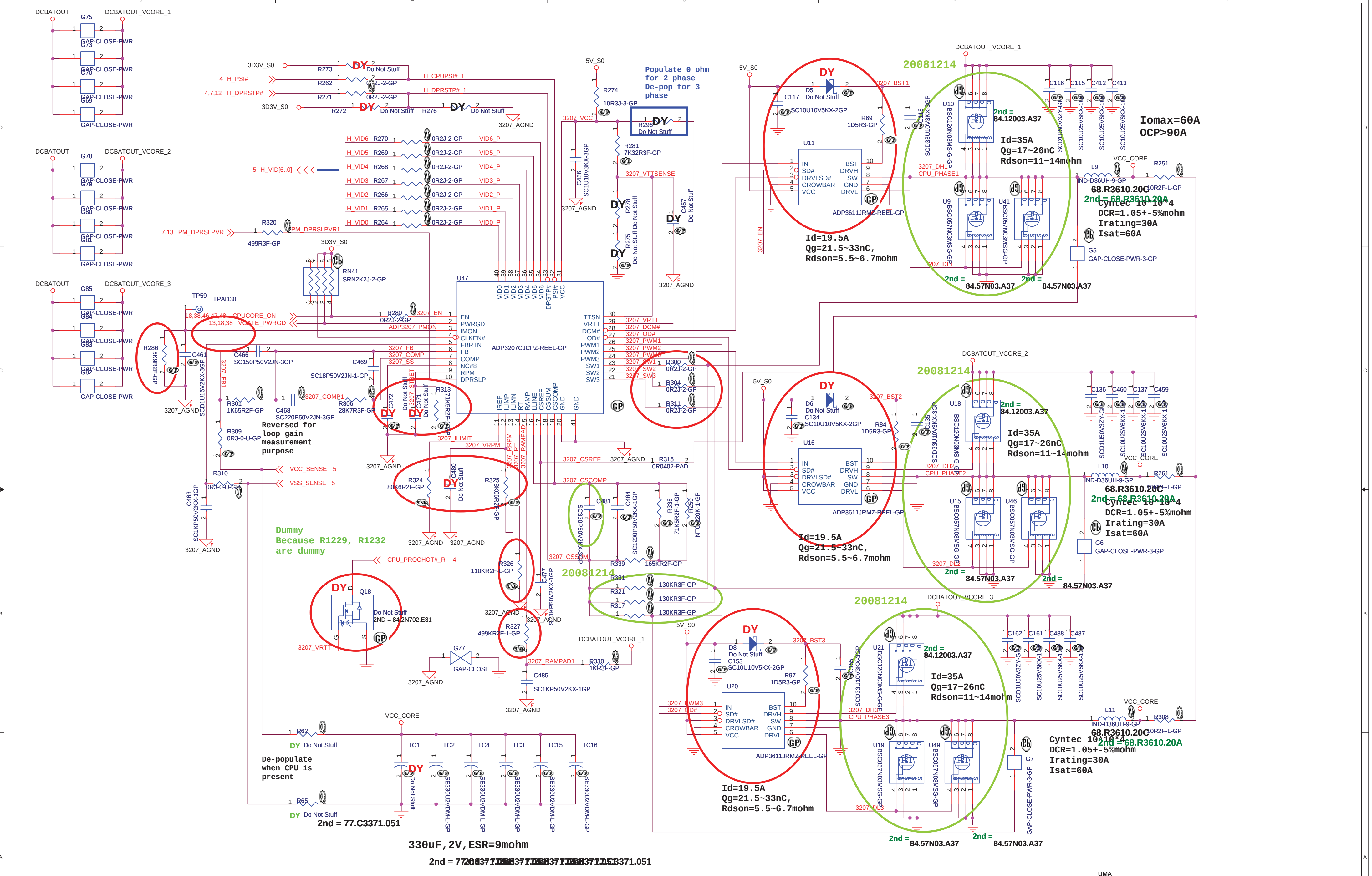


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	ISL88731A Charger	
Size A3	Document Number JM70-MV	Rev SB
Date: Saturday, December 20, 2008	Sheet 50 of 55	



UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP3207C_CPU CORE

Size: Custom | Document Number: JM70-MV | Rev: SB

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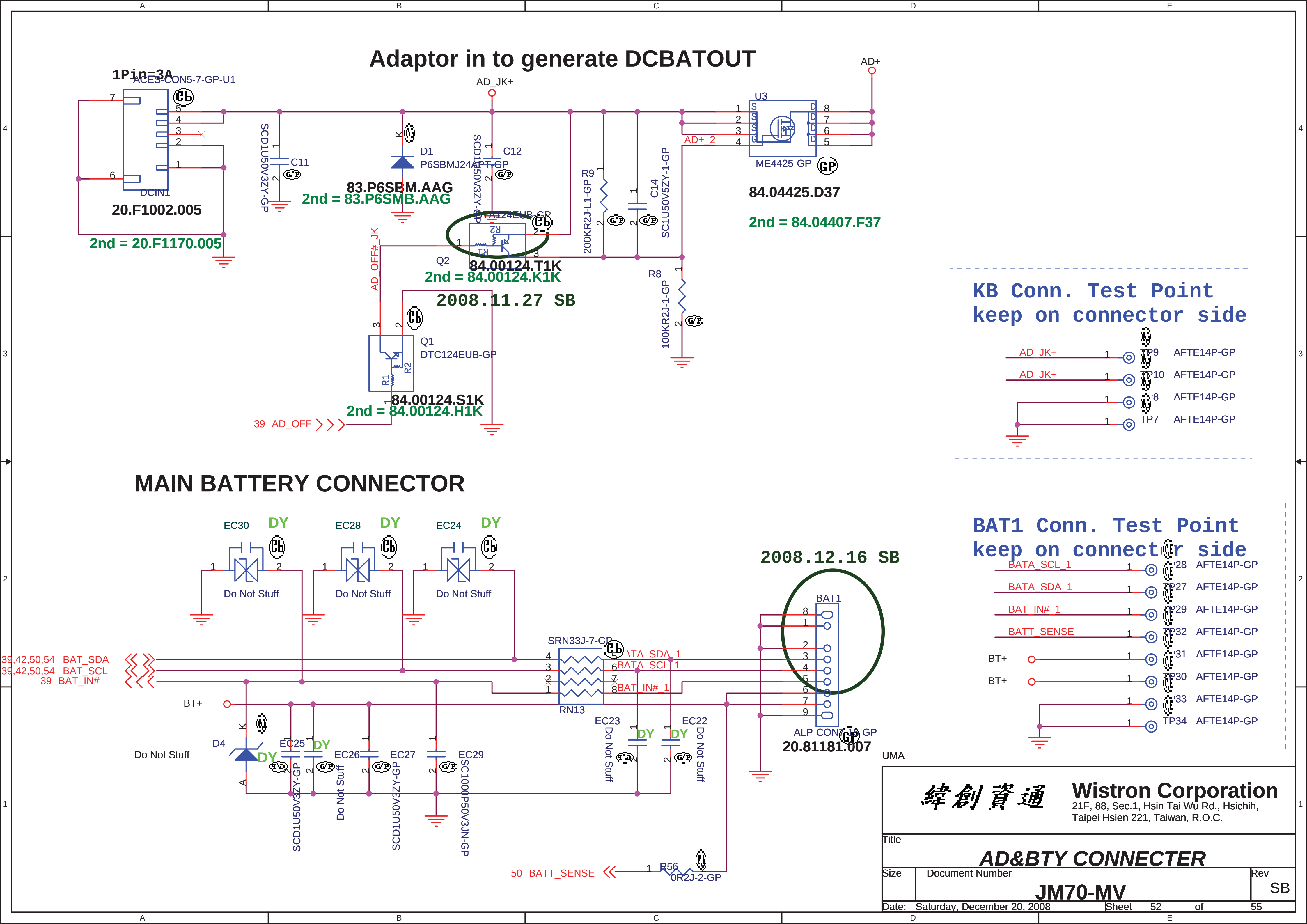

Adaptor in to generate DCBATOUT
1Pin=3A
ACES-CON5-7-GP-U1
DCIN1
20.F1002.005
2nd = 20.F1170.005
AD_JK+
AD+
D1
P6SBMJ24APT-GP
83.P6SBM.AAG
2nd = 83.P6SMB.AAG
C11
SCD1U50V3ZY-GP
C12
C14
SC1U50V5ZY-1-GP
R9
200KR2J-L1-GP
R8
100KR2J-1-GP
U3
ME4425-GP
84.04425.D37
2nd = 84.04407.F37
AD+_2
Q2
84.00124.T1K
2nd = 84.00124.K1K
2008.11.27 SB
AD_OFF#_JK
Q1
DTC124EUB-GP
84.00124.S1K
2nd = 84.00124.H1K
39 AD_OFF
KB Conn. Test Point
keep on connector side
AD_JK+
TP9 AFTE14P-GP
TP10 AFTE14P-GP
TP8 AFTE14P-GP
TP7 AFTE14P-GP
MAIN BATTERY CONNECTOR
EC30 DY Do Not Stuff
EC28 DY Do Not Stuff
EC24 DY Do Not Stuff
39,42,50,54 BAT_SDA
39,42,50,54 BAT_SCL
39 BAT_IN#
BT+
SRN33J-7-GP
RN13
BATA_SDA_1
BATA_SCL_1
BAT_IN#_1
2008.12.16 SB
BAT1
ALP-CON7-13-GP
20.81181.007
D4
Do Not Stuff
EC25 DY
EC26
EC27
EC29
SCD1U50V3ZY-GP
SC1000P50V3JN-GP
EC23 DY Do Not Stuff
EC22 DY Do Not Stuff
50 BATT_SENSE
R56
0R2J-2-GP
BAT1 Conn. Test Point
keep on connector side
BATA_SCL_1 TP28 AFTE14P-GP
BATA_SDA_1 TP27 AFTE14P-GP
BAT_IN#_1 TP29 AFTE14P-GP
BATT_SENSE TP32 AFTE14P-GP
BT+ TP31 AFTE14P-GP
BT+ TP30 AFTE14P-GP
TP33 AFTE14P-GP
TP34 AFTE14P-GP
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AD&BTY CONNECTER
Size Document Number Rev
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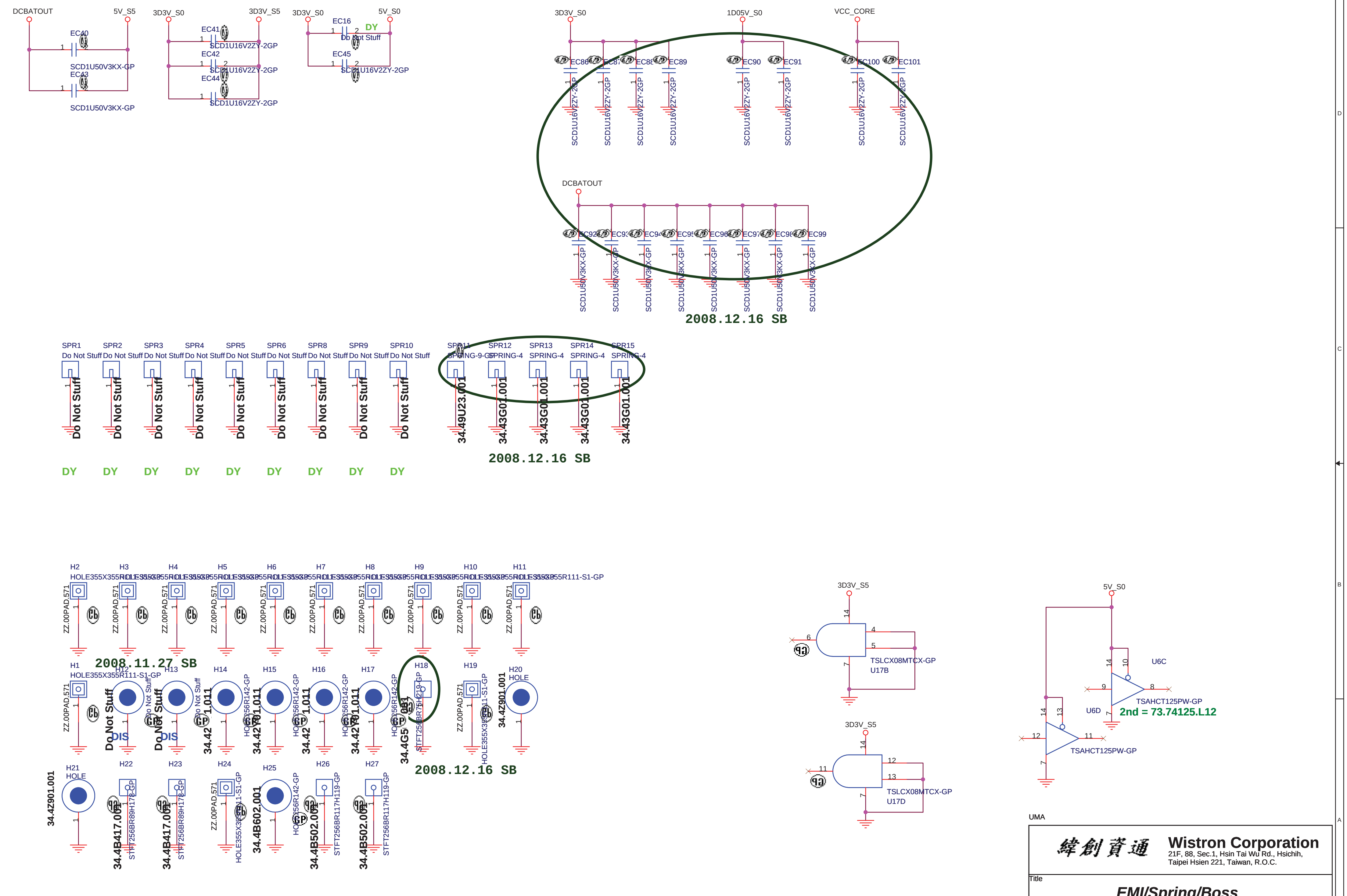

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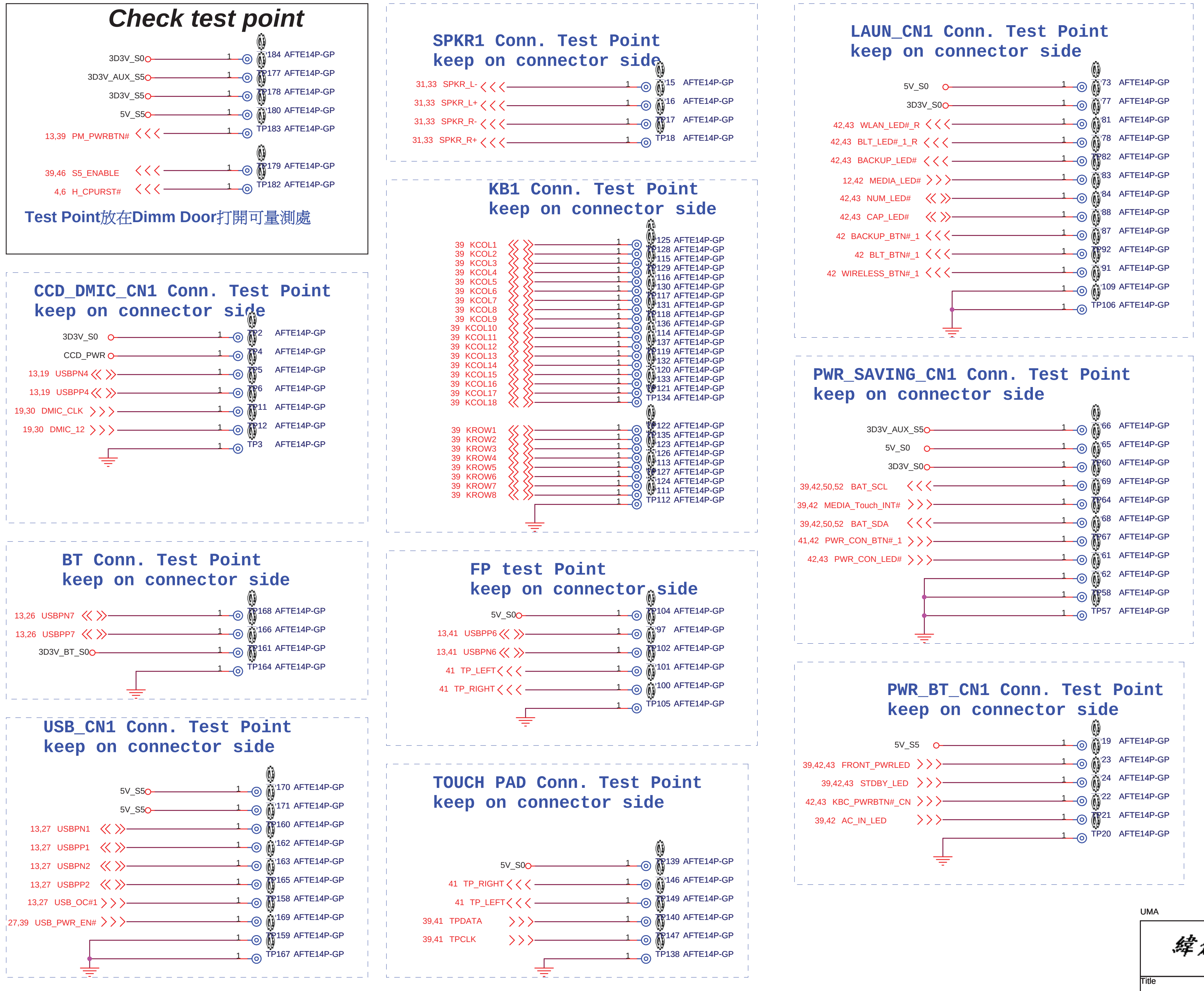

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