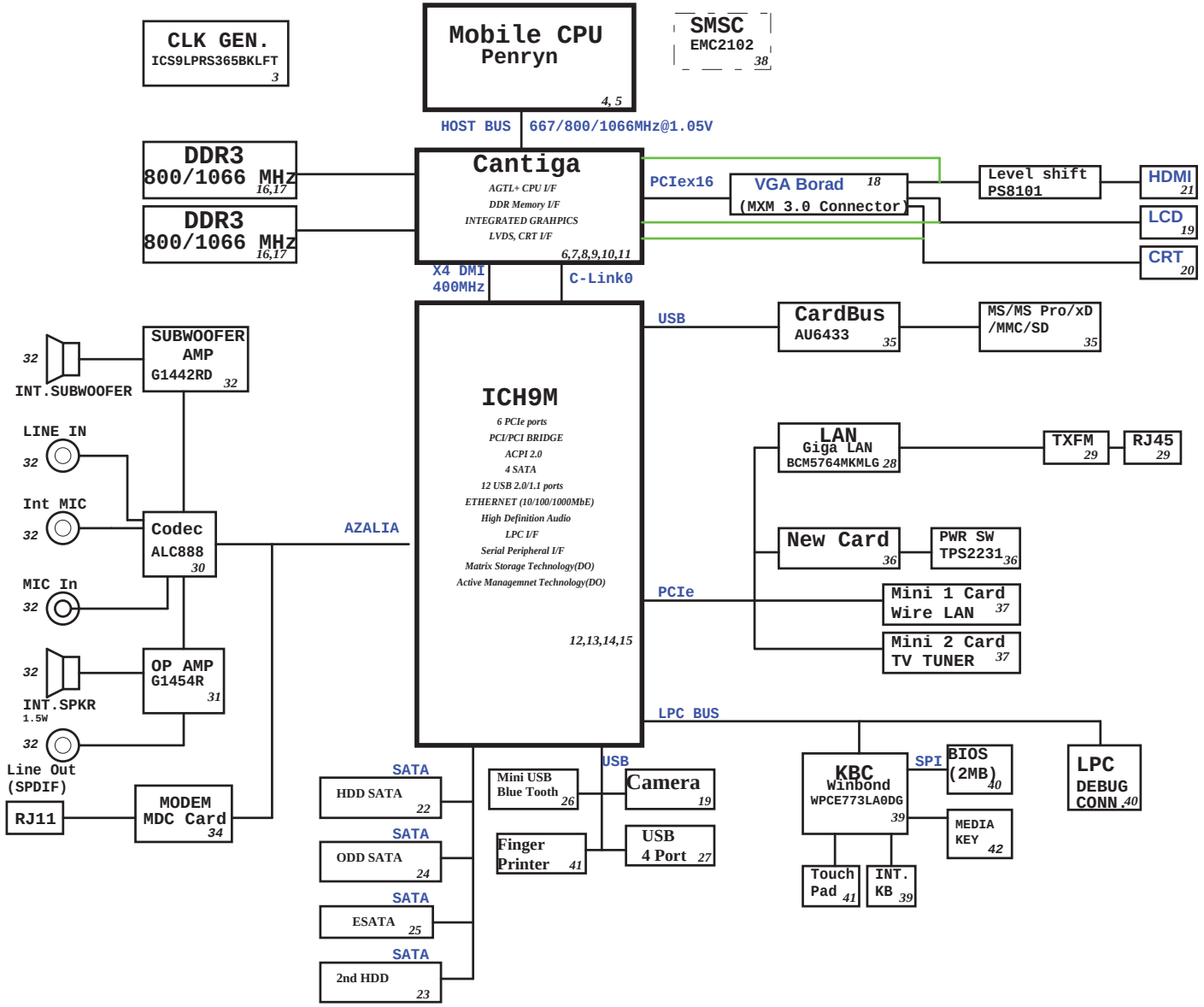
JM70 -MV Block Diagram

Project code: 91.4AN01.001
PCB P/N : 48.4AN01.0SA
REVISION : SB 08246



SYSTEM DC/DC ISL62392 46

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5

SYSTEM DC/DC TPS51124 46

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A) 1D5V_S3(10A)

RT9026 49

1.5V_S3	DDR_VREF_S3 (1.2A)

G9198-15 14

3D3V_S5	1D5V_S5 (300mA)

CHARGER ISL88731A 50

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A

CPU DC/DC ADP3208C 51

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A

GFX DC/DC ISL6263 48

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

PCB STACKUP

TOP
GND
S
S
GND
BOTTOM

UMA

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Title: BLOCK DIAGRAM

Size	Document Number	Rev
A2	JM70-MV	SB

Date: Saturday, December 20, 2008 Sheet 1 of 55

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

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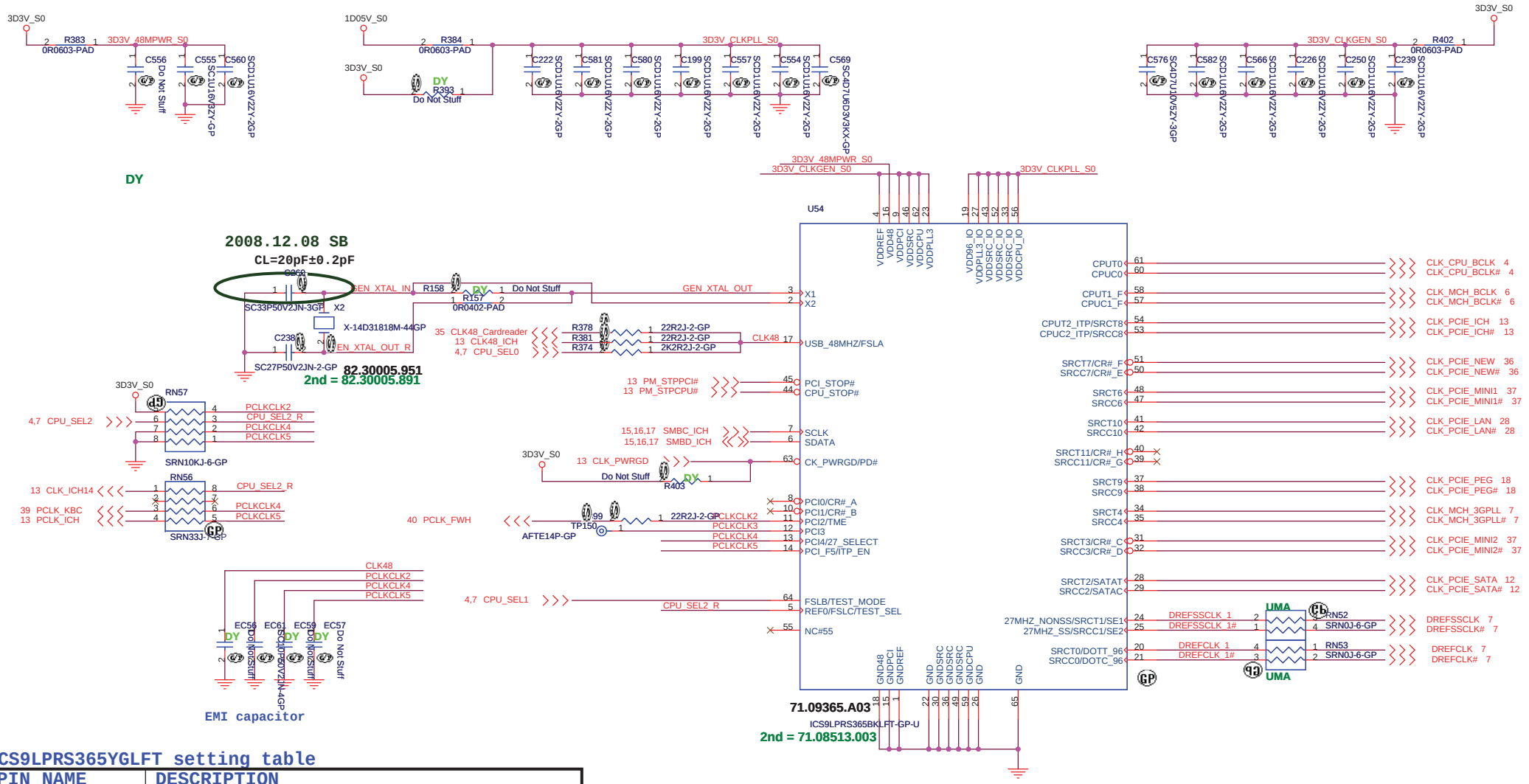
Title: Reference

Size: A3 | Document Number: JM70-MV | Rev: SB

Date: Saturday, December 20, 2008 | Sheet 2 of 55



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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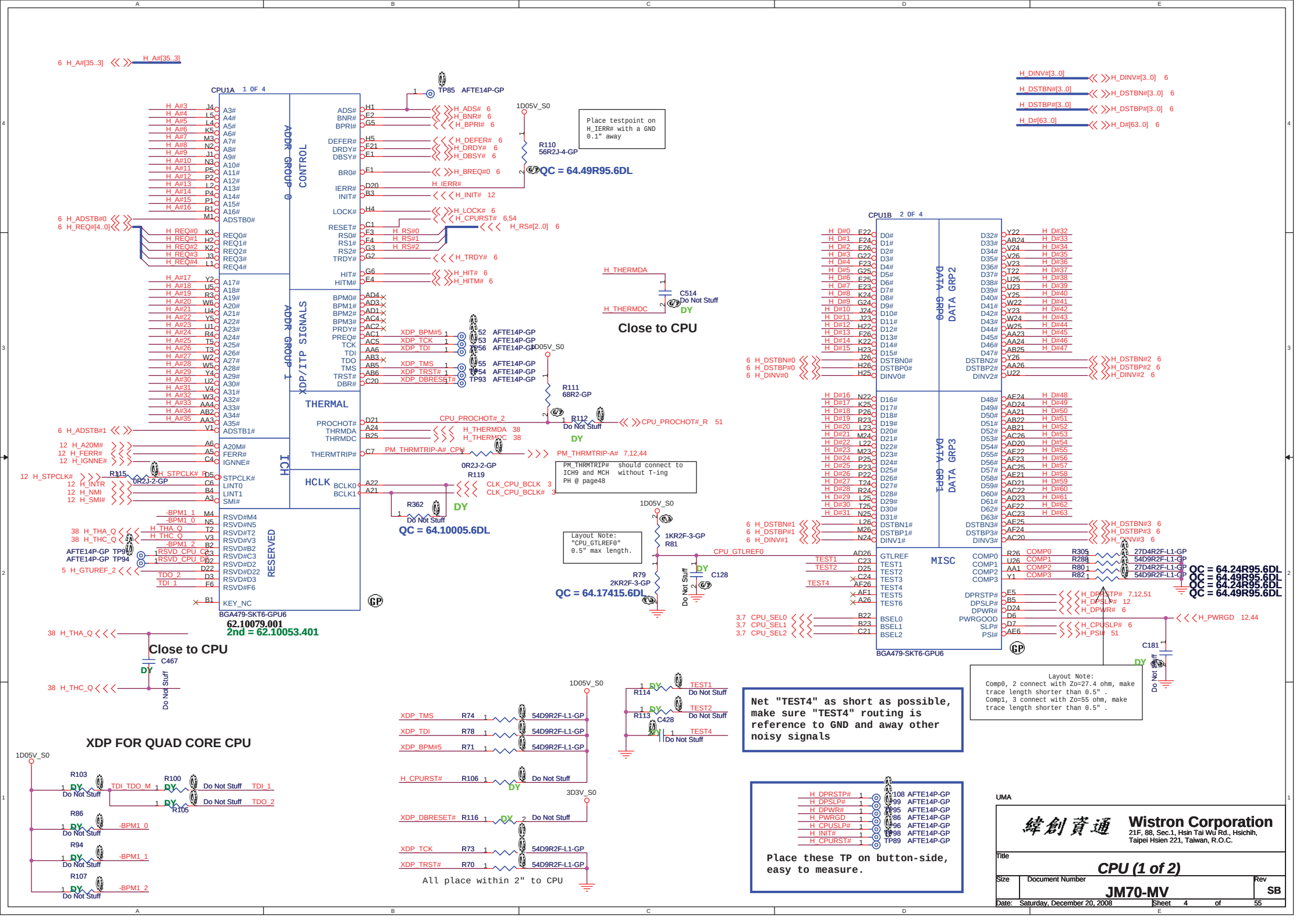
Title: Clock Generator

Size	Document Number	Rev
	JM70-MV	SB

Date: Saturday, December 20, 2008 Sheet 3 of 55


CPU1A 1 0F 4
CPU1B 2 0F 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
DATA GRP2
DATA GRP0
DATA GRP3
DATA GRP1
MISC
BGA479-SKT6-GPU6
TP85 AFTE14P-GP
Place testpoint on H_IERR# with a GND 0.1" away
QC = 64.49R95.6DL
Close to CPU
QC = 64.10005.6DL
QC = 64.17415.6DL
QC = 64.24R95.6DL
QC = 64.49R95.6DL
62.10079.001
2nd = 62.10053.401
Layout Note: "CPU_GTLREF0" 0.5" max length.
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
XDP FOR QUAD CORE CPU
All place within 2" to CPU
Place these TP on button-side, easy to measure.
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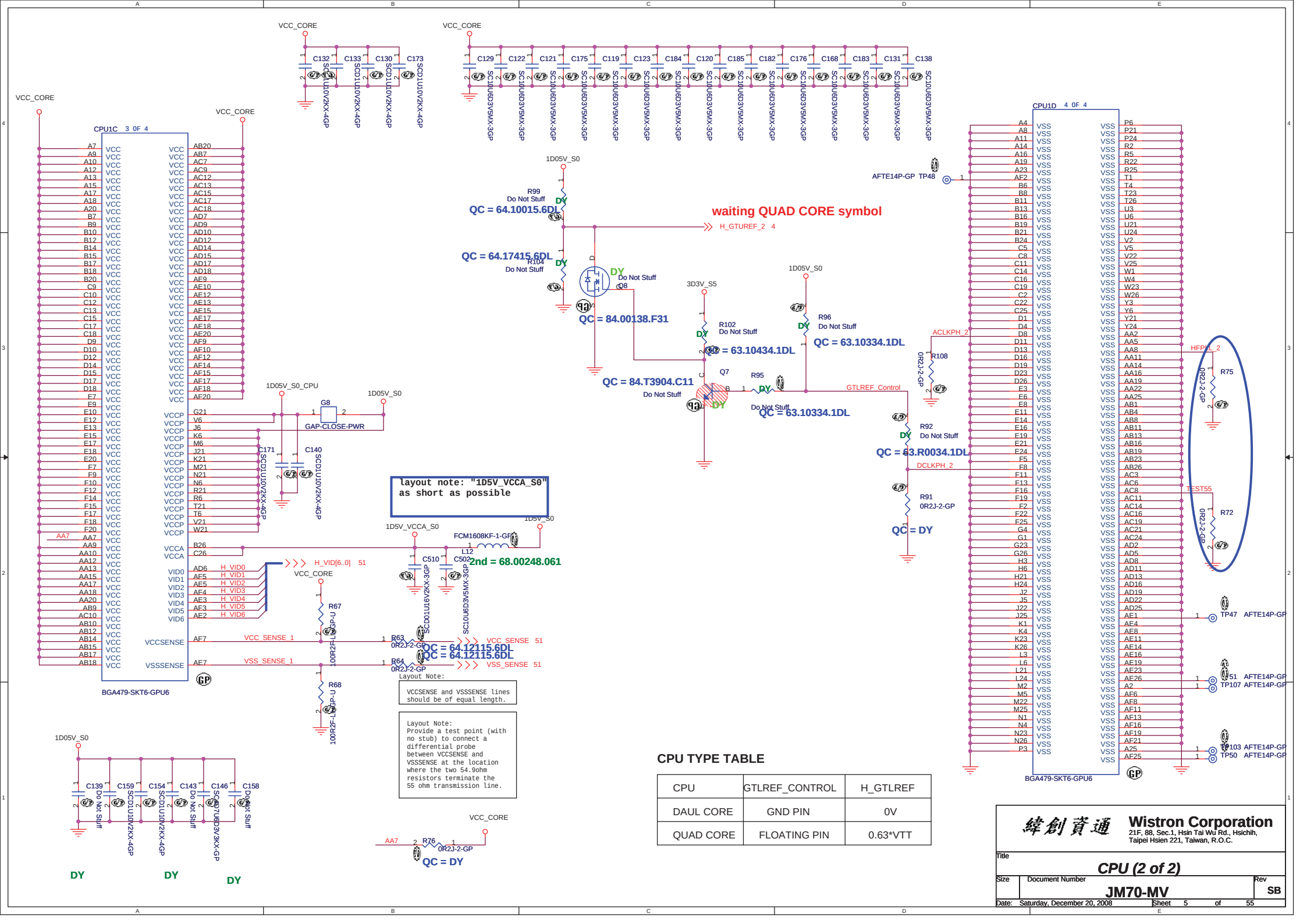
Title
CPU (1 of 2)
Size
Document Number
JM70-MV
Rev
SB
Date: Saturday, December 20, 2008
Sheet 4 of 55



CPU TYPE TABLE

CPU	GTLREF_CONTROL	H_GTLREF
DAUL CORE	GND PIN	0V
QUAD CORE	FLOATING PIN	0.63*VTT

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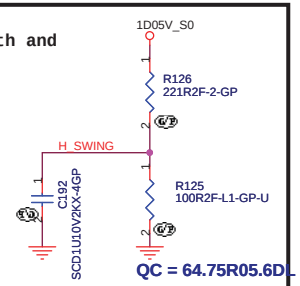
Size	Document Number	Rev
	JM70-MV	SB

Date: Saturday, December 20, 2008 Sheet 5 of 55

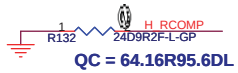
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



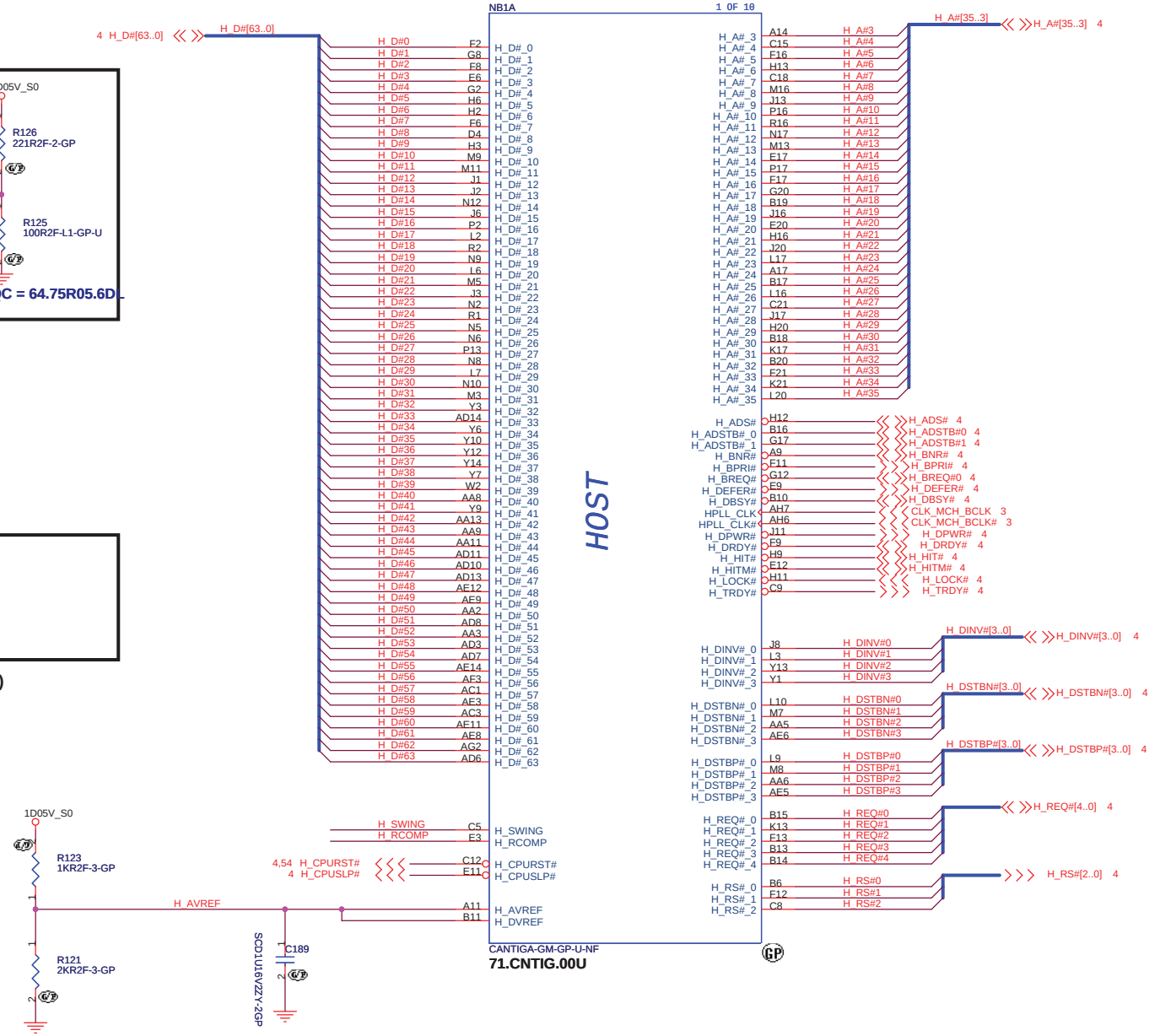
QC = 64.75R05.6DL

H_RCOMP routing Trace width and Spacing use 10 / 20 mil



QC = 64.16R95.6DL

Place them near to the chip (< 0.5")



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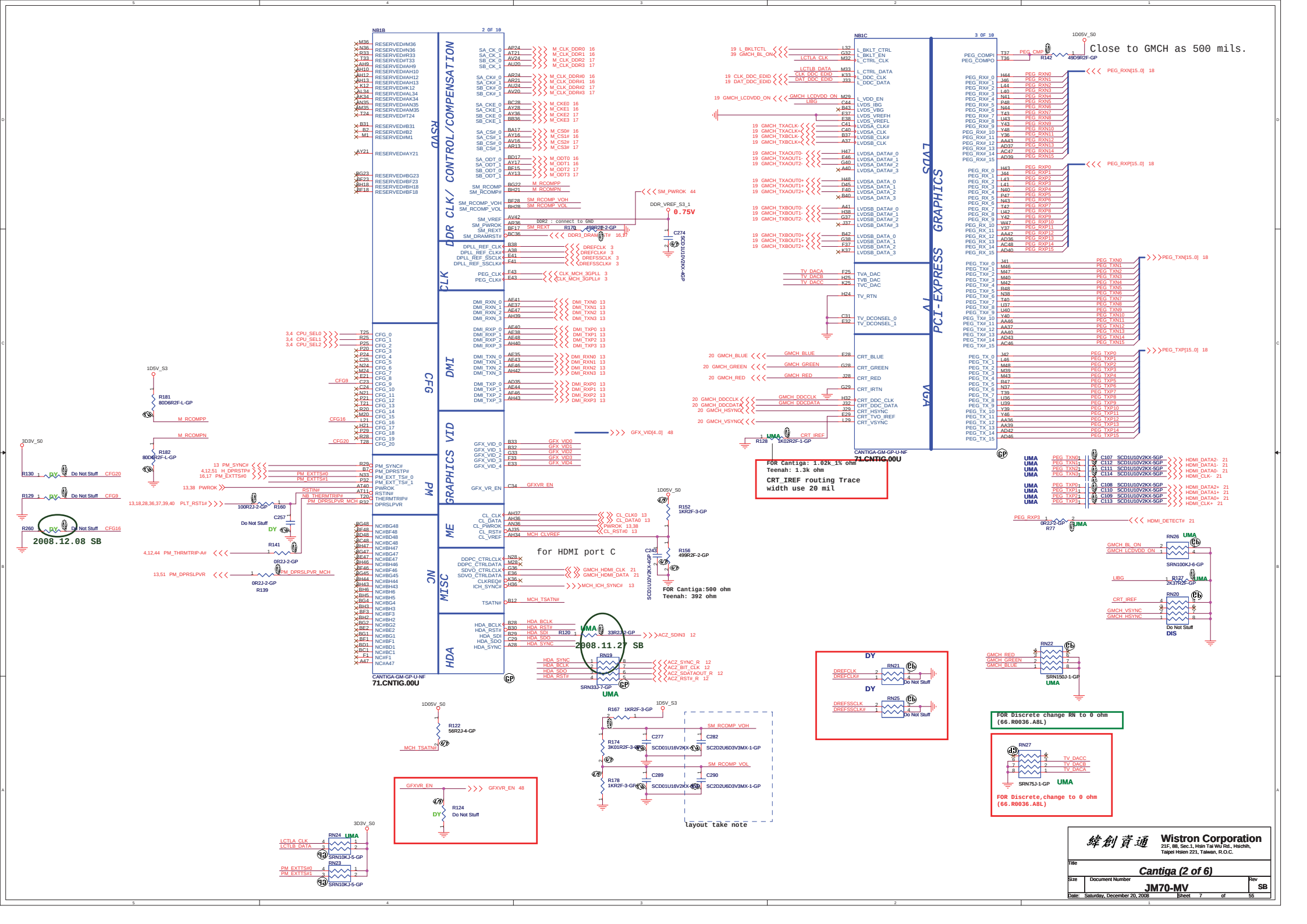
Title	Cantiga (1 of 6)	
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 6 of 55	


Close to GMCH as 500 mils.
2008.12.08 SB
2008.11.27 SB
for HDMI port C
FOR Cantiga:500 ohm
Teenah: 392 ohm
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace
width use 20 mil
FOR Discrete change RN to 0 ohm
(66.R0036.A8L)
FOR Discrete,change to 0 ohm
(66.R0036.A8L)
layout take note
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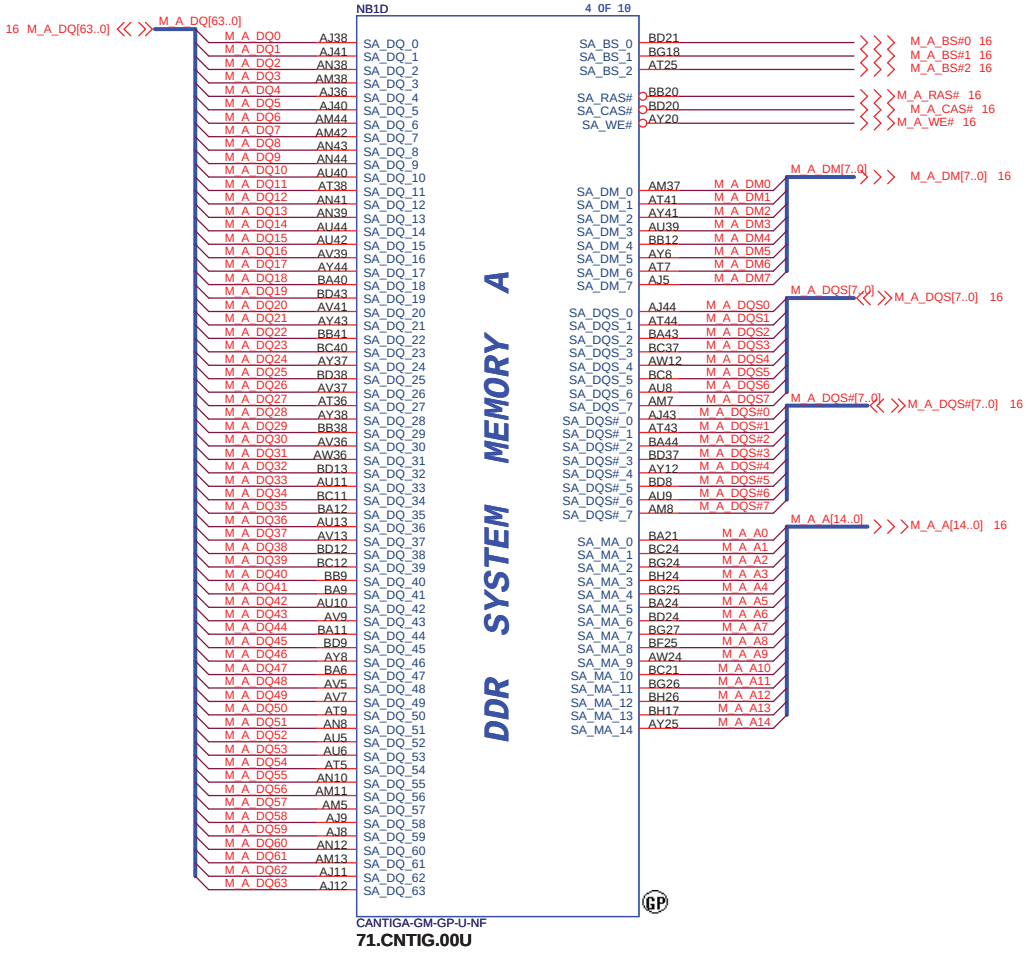
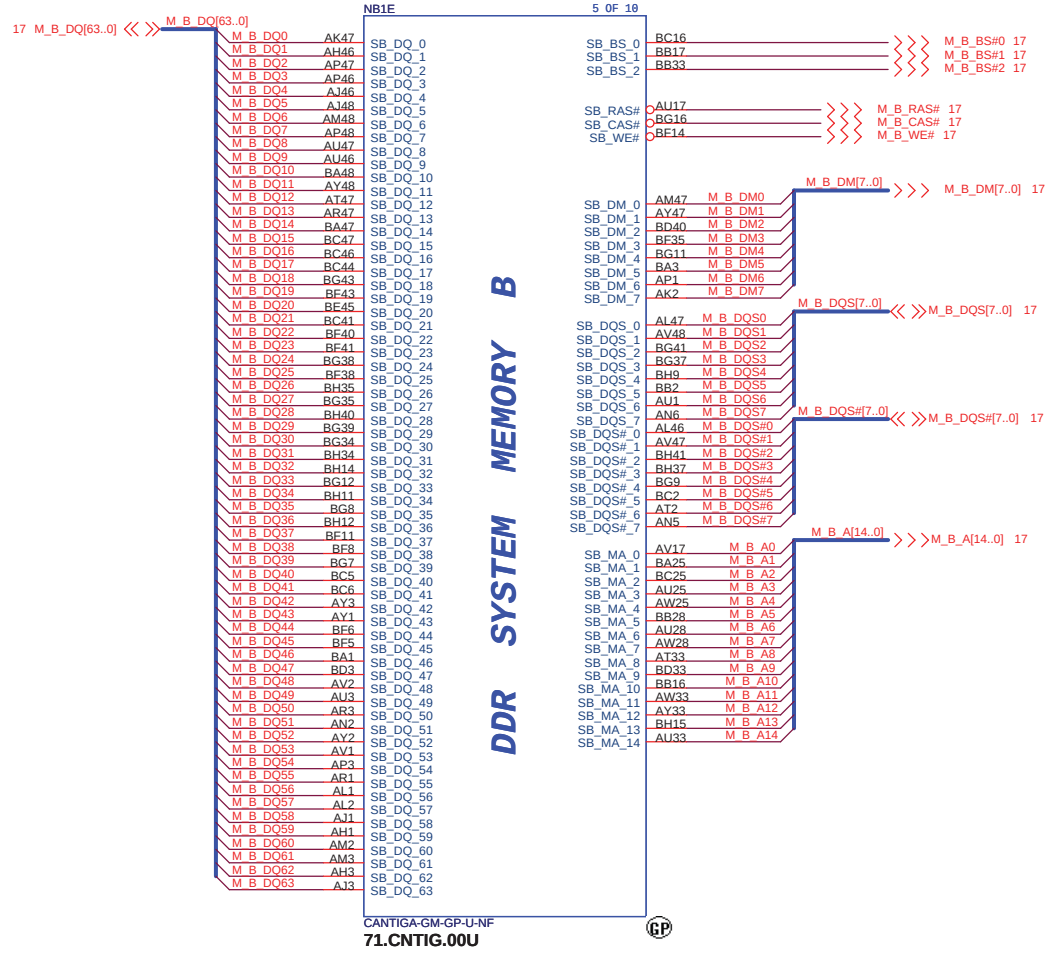
Cantiga (2 of 6)
JM70-MV
SB
Saturday, December 20, 2008





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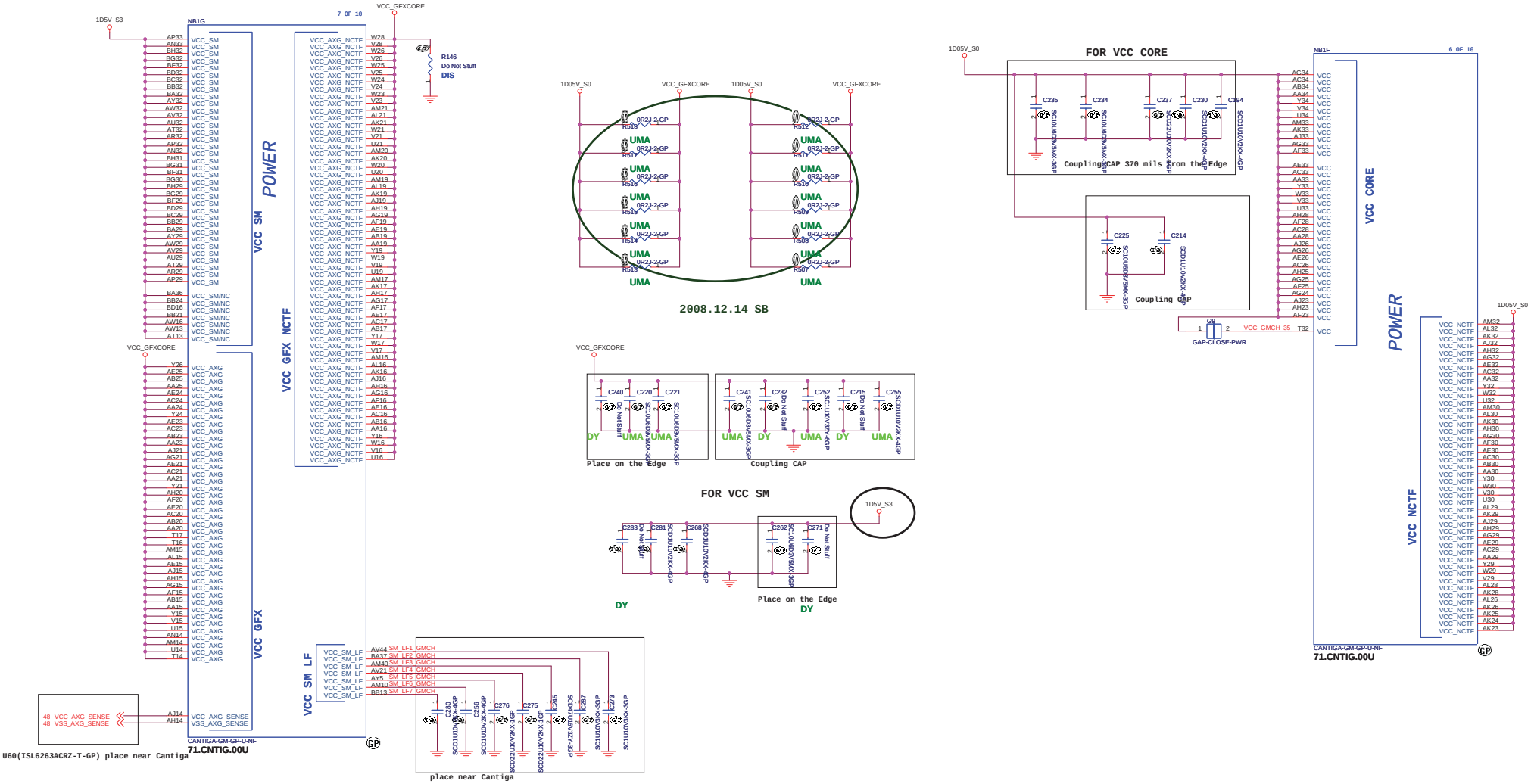
Title: Cantiga (3 of 6)

Size | Document Number: JM70-MV | Rev: SB

Date: Saturday, December 20, 2008 | Sheet 8 of 55



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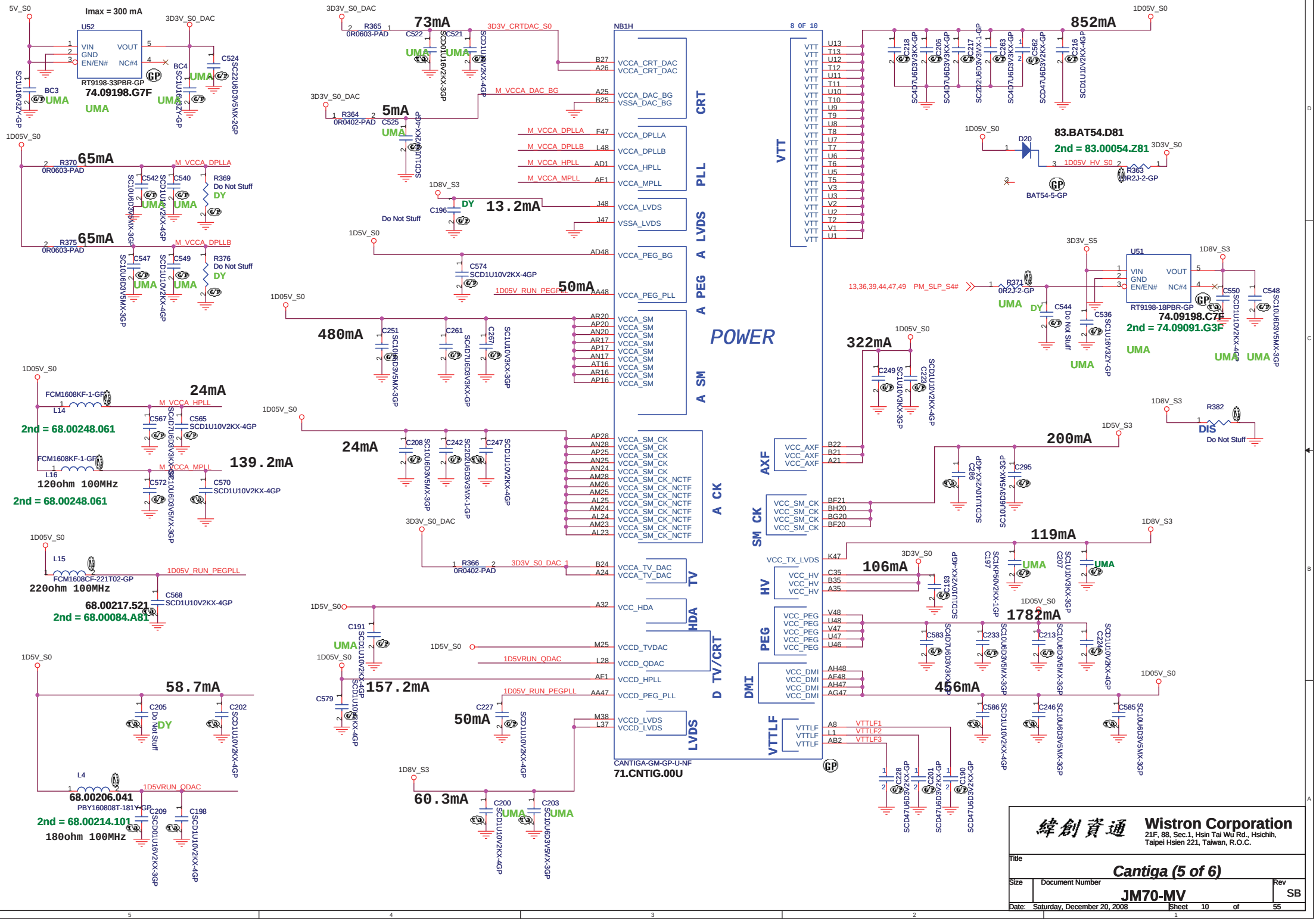
Title	Cantiga (4 of 6)		
Size	Document Number		Rev
	JM70-MV		SB
Date: Saturday, December 20, 2008	Sheet 9	of 55	


Imax = 300 mA
U52
RT9198-33PBR-GP
74.09198.G7F
73mA
5mA
65mA
65mA
13.2mA
50mA
480mA
24mA
139.2mA
24mA
58.7mA
157.2mA
50mA
60.3mA
852mA
83.BAT54.D81
2nd = 83.00054.Z81
322mA
200mA
119mA
106mA
1782mA
456mA
U51
RT9198-18PBR-GP
74.09198.C7F
2nd = 74.09091.G3F
NB1H
8 OF 10
CRT
PLL
LVDS
A LVDS
A PEG
A SM
A CK
AXF
SM CK
HV
PEG
DMI
VTTLF
HDA
TV
D TV/CRT
POWER
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
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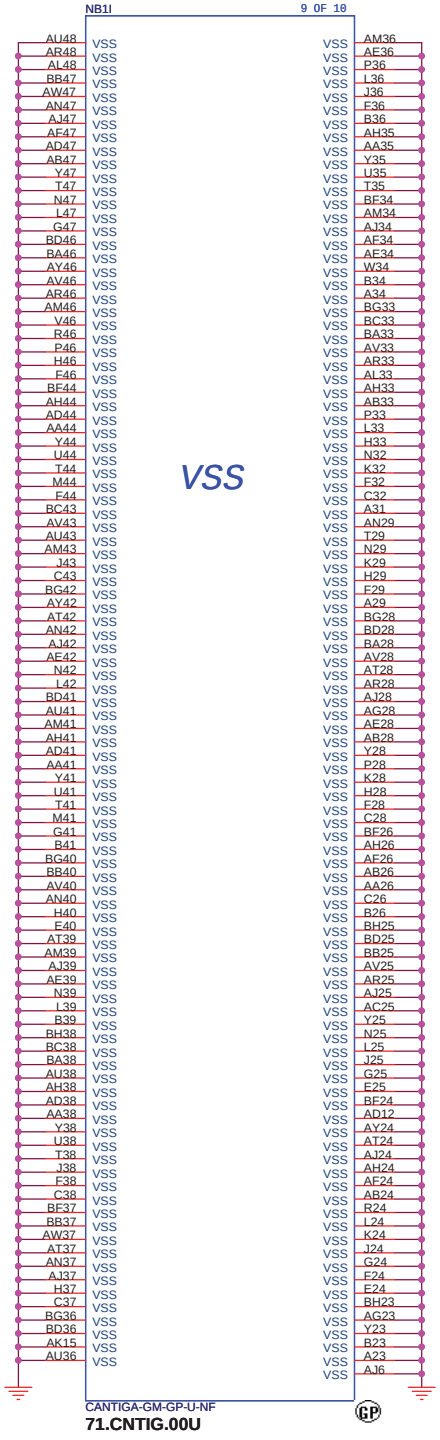
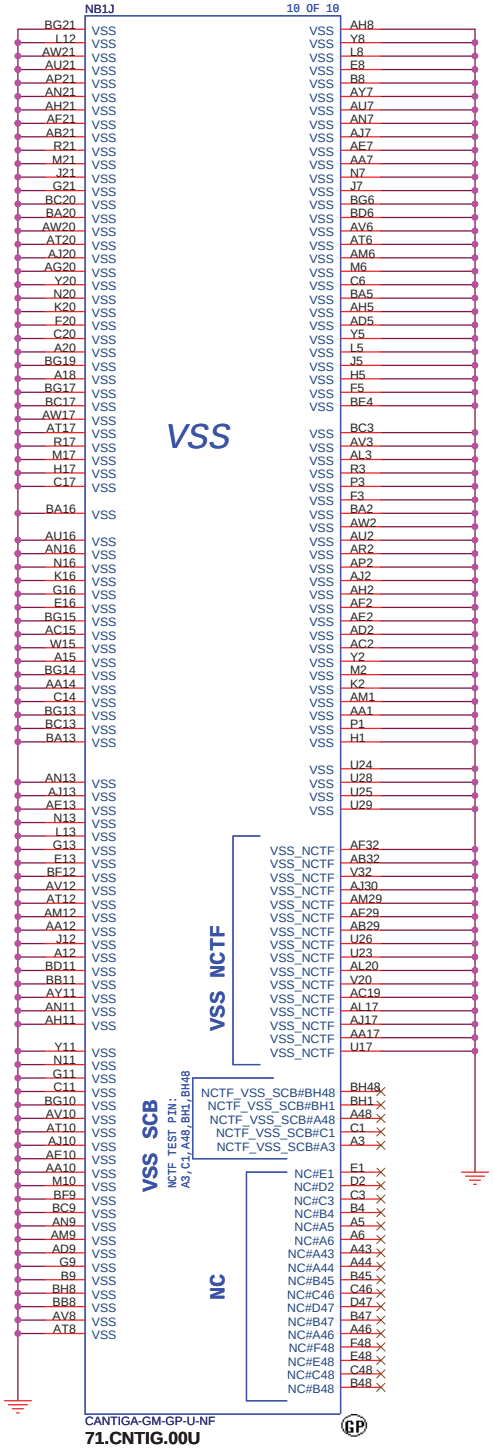
Title
Cantiga (5 of 6)
Size
Document Number
JM70-MV
Rev
SB
Date: Saturday, December 20, 2008
Sheet 10 of 55





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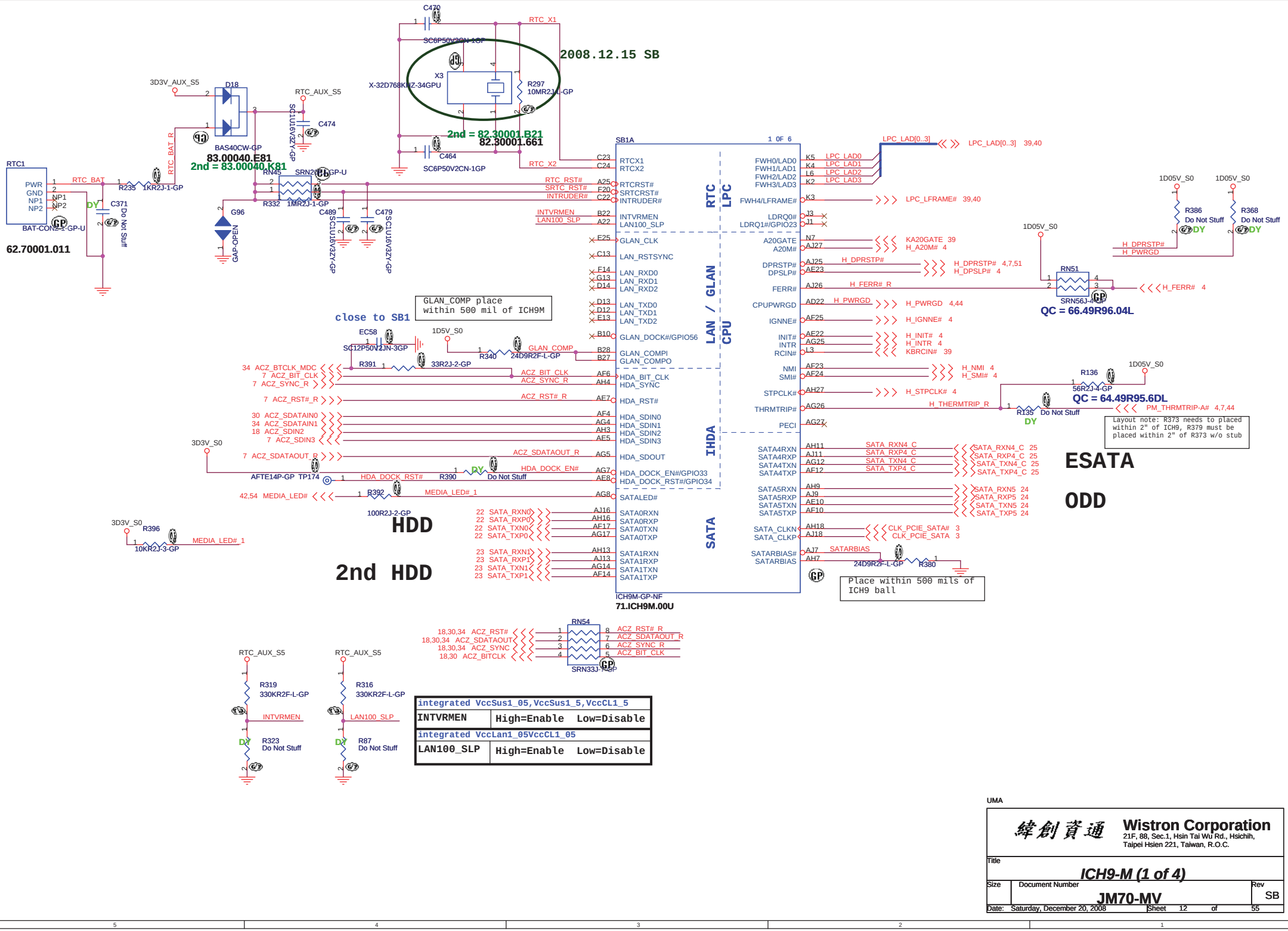
Title	***Cantiga (6 of 6)***	
Size	Document Number: **JM70-MV**	Rev: SB
Date: Saturday, December 20, 2008	Sheet 11 of 55	


2008.12.15 SB
2nd = 82.30001.B21
82.30001.661
83.00040.E81
2nd = 83.00040.K81
62.70001.011
GLAN_COMP place within 500 mil of ICH9M
close to SB1
HDD
2nd HDD
ESATA
ODD
QC = 66.49R96.04L
QC = 64.49R95.6DL
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
Place within 500 mils of ICH9 ball
ICH9M-GP-NF
71.ICH9M.00U
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
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ICH9-M (1 of 4)
JM70-MV
Date: Saturday, December 20, 2008
Sheet 12 of 55

PCI_GNT#0 and SPI_CS1# have weak internal Pull up

These R need close SB within 600 mils

SB1B 2 0F 6

PCI

Interrupt I/F

ICH9M-GP-NF
71.ICH9M.00U

SB1C 3 0F 6

SMB

SYS GPIO

Power MGT

GPIO

Controller Link

MISC

ICH9M-GP-NF
71.ICH9M.00U

SB1D 4 0F 6

PCI-Express

Direct Media Interface

SPI

USB

ICH9M-GP-NF
71.ICH9M.00U

LAN

MINICARD1

MINICARD2

TV_tuner
TV_tuner

2008.12.14 SB

NEW CARD
NEW
NEW

2008.12.14 SB

No Reboot Strap

SPKR	LOW = Defaule High=No Reboot

USB	
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINIC1
4	WEBCAM
5	NEW1
6	FP
7	Bluetooth
8	NC
9	USB1
10	MINIC2
11	Cardreader

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default

UMA

2nd = 83.00054.Z81

2nd = 83.00016.F11 / 83.00016.G11

83.BAT54.D81

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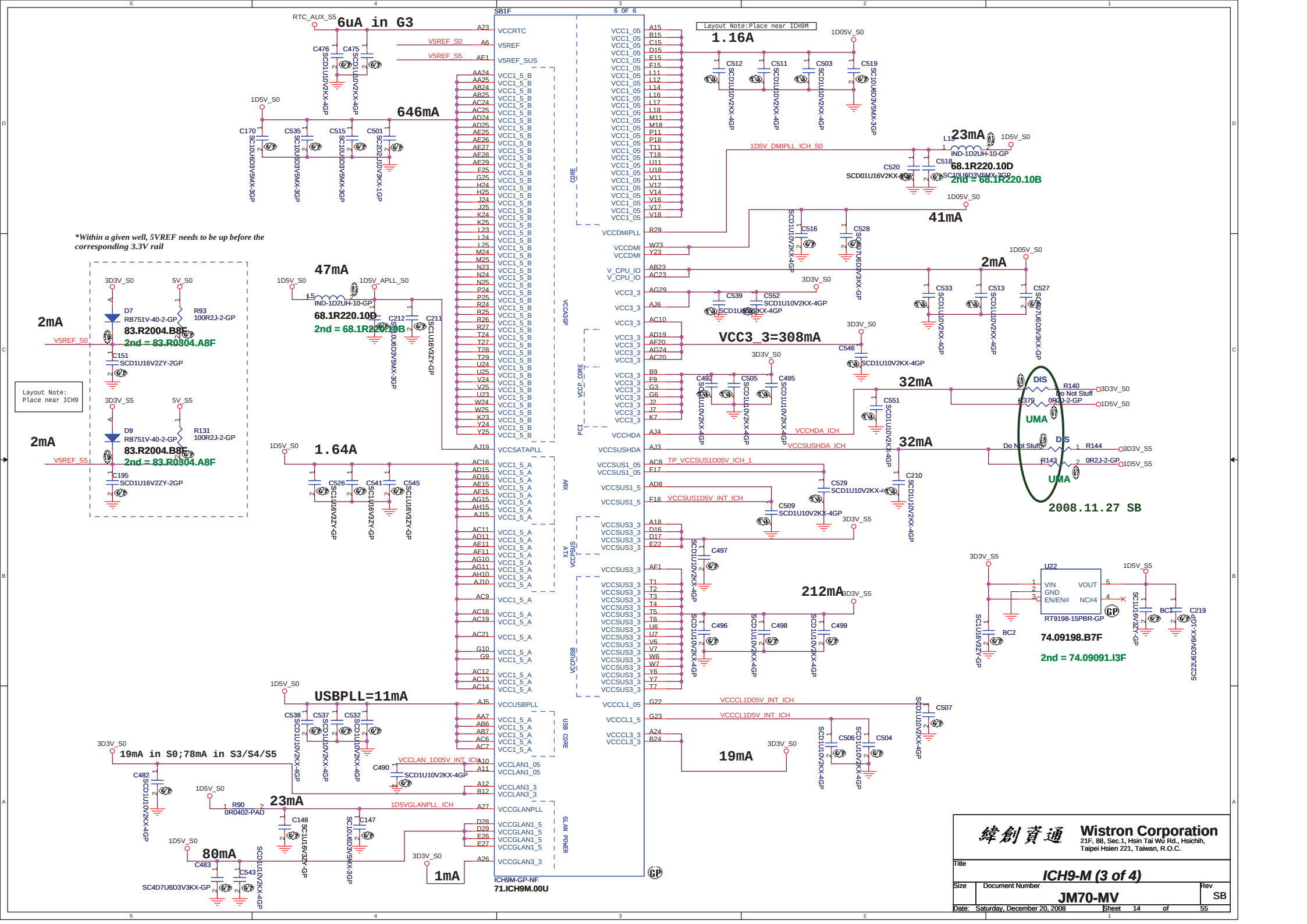
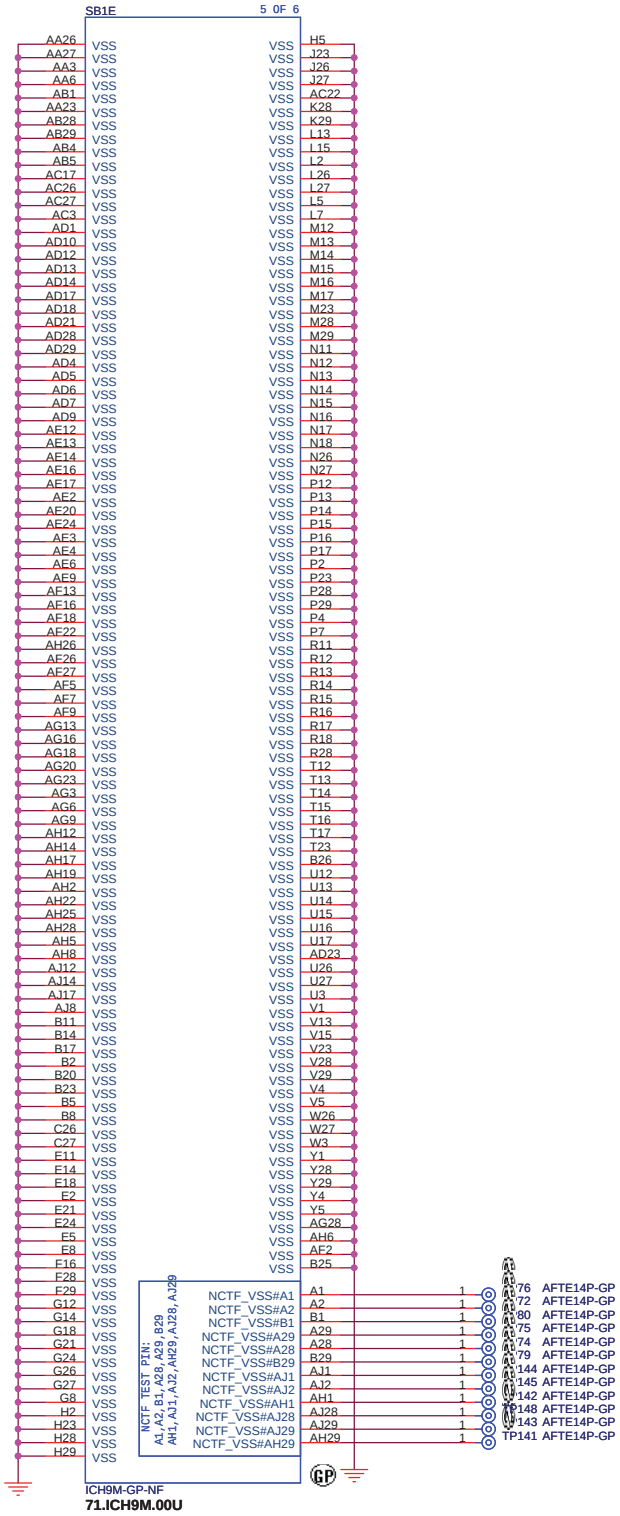
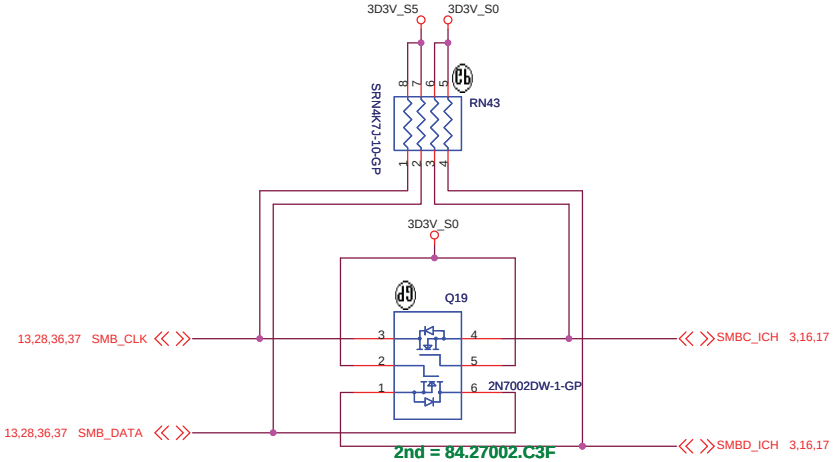
Title: ICH9-M (2 of 4)

Size: | Document Number: JM70-MV | Rev: SB

Date: Saturday, December 20, 2008 Sheet 13 of 55

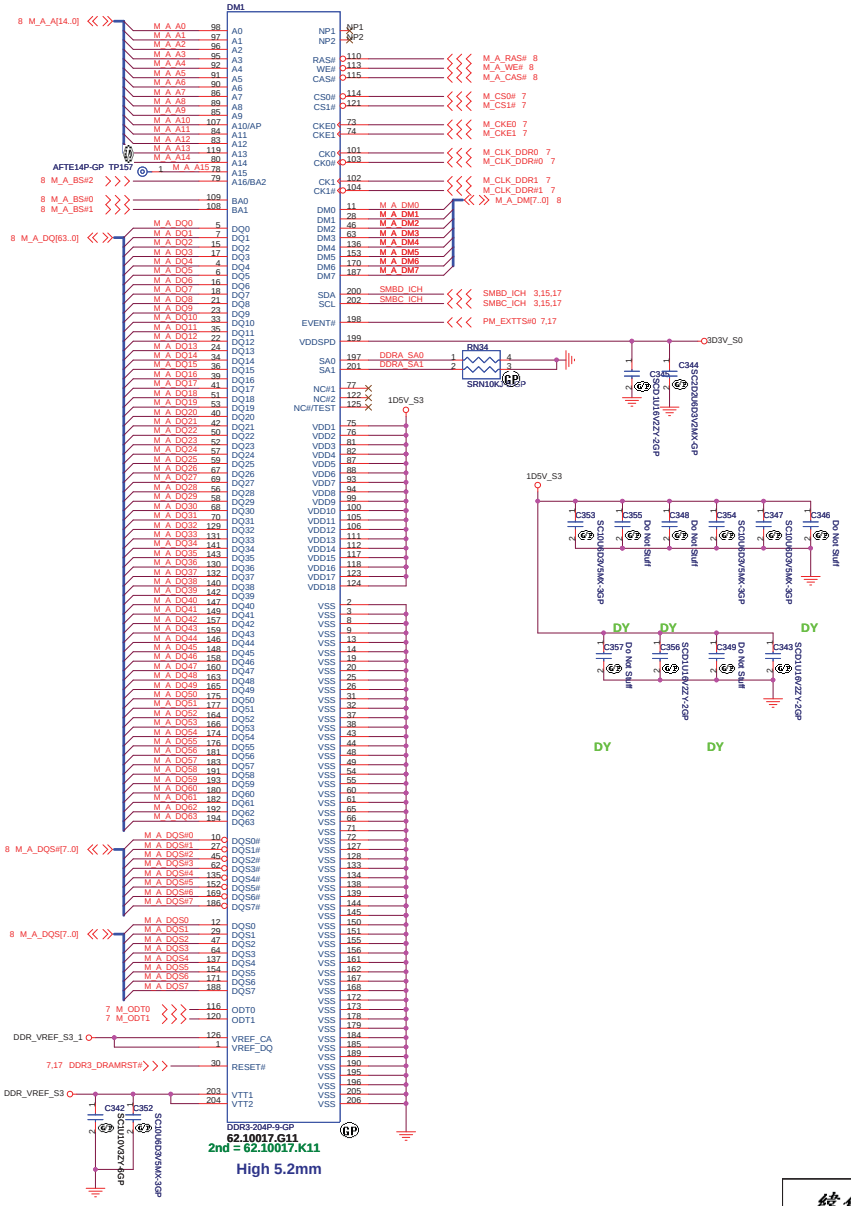

6uA in G3
646mA
1.16A
23mA
68.1R220.10D
2nd = 68.1R220.10B
41mA
2mA
47mA
68.1R220.10D
2nd = 68.1R220.10B
VCC3_3=308mA
32mA
32mA
DIS
UMA
DIS
UMA
2008.11.27 SB
1.64A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
212mA
19mA
74.09198.B7F
2nd = 74.09091.I3F
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
SB1F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
JM70-MV
SB
Saturday, December 20, 2008
14
55



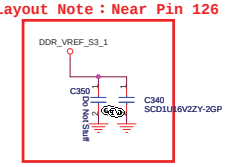


緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: *ICH9-M (4 of 4)*		
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 15 of 55	

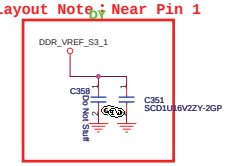
DDR3 SOCKET_1



Layout Note : Near Pin 126



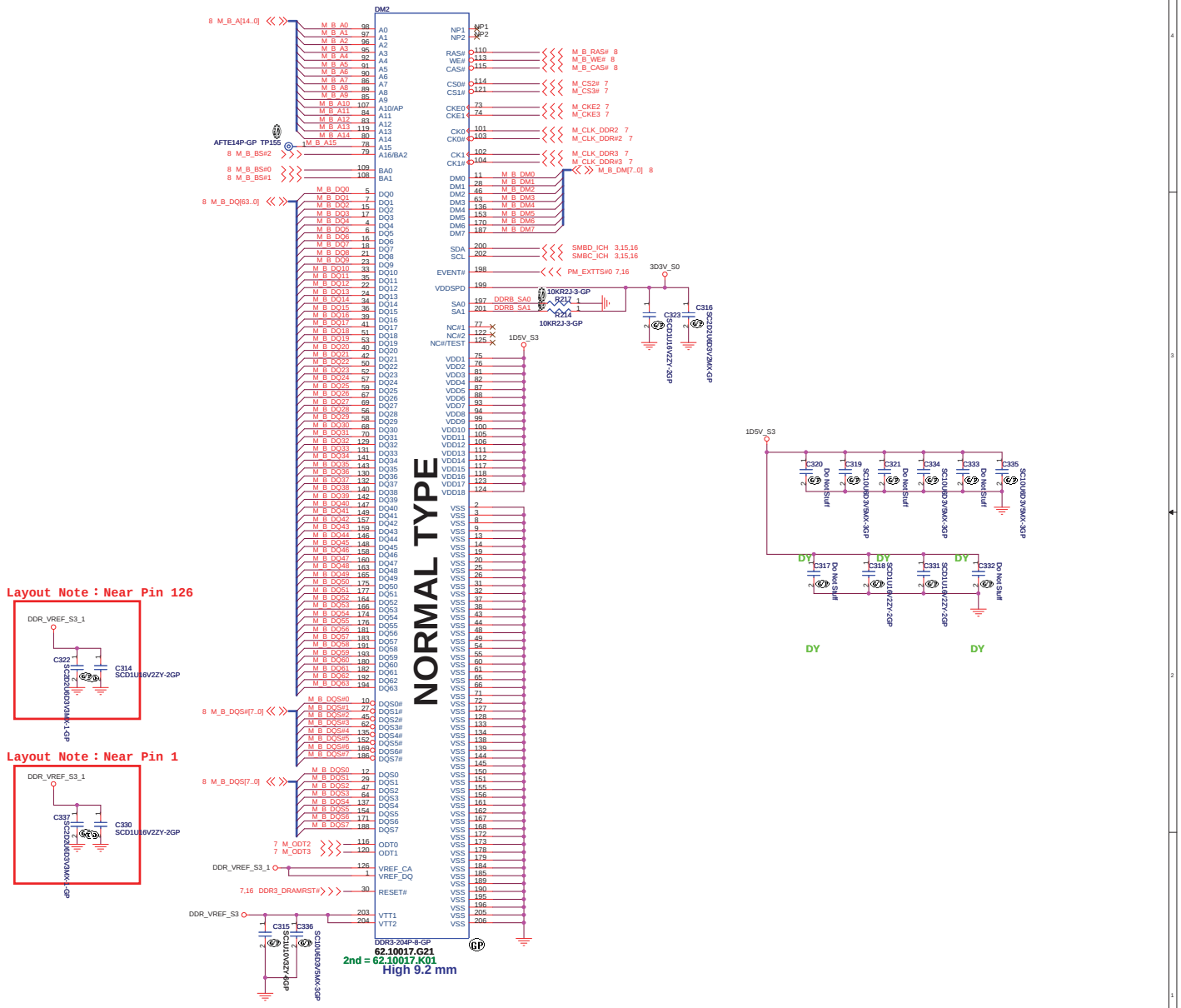
Layout Note : Near Pin 1



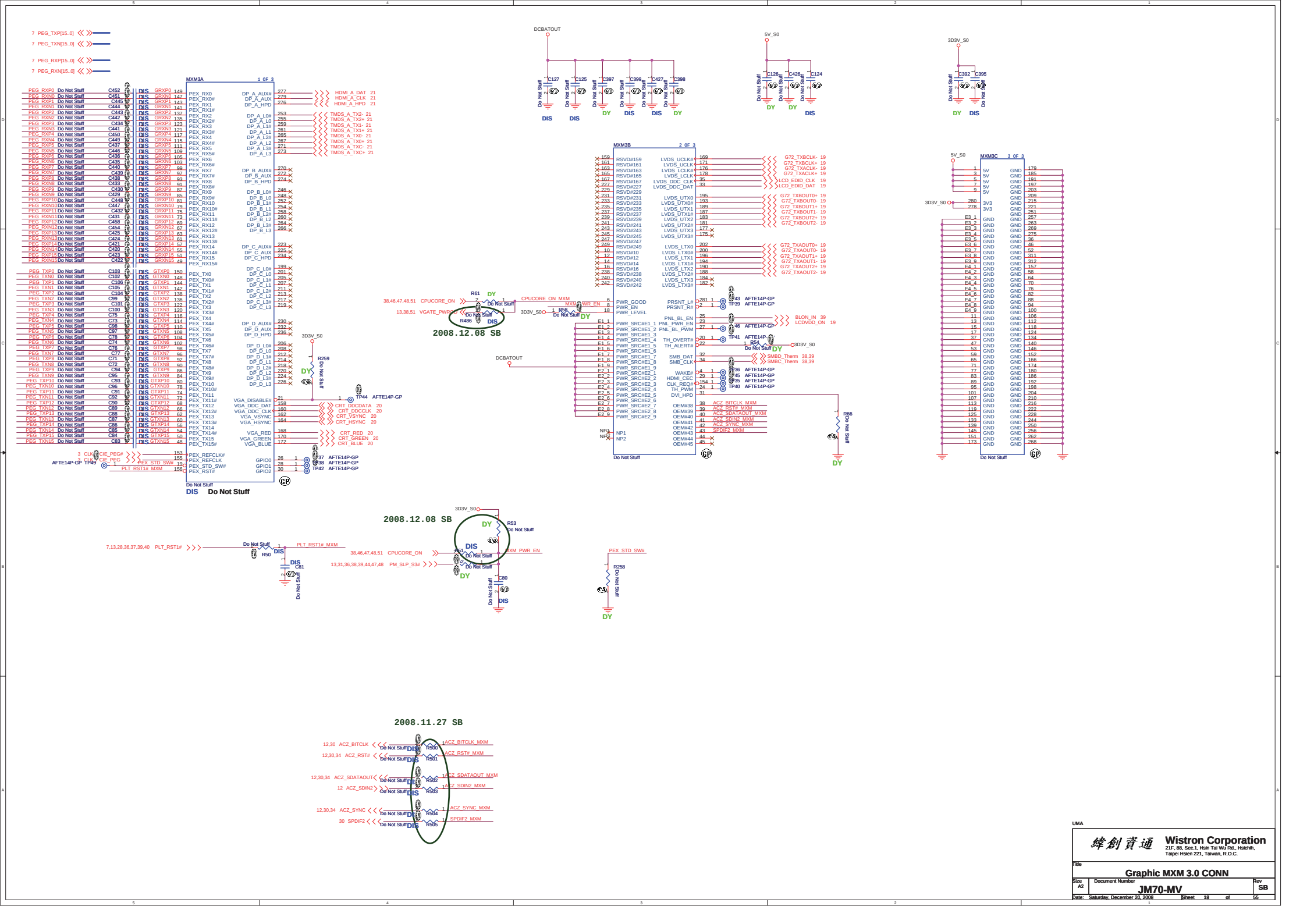
DY

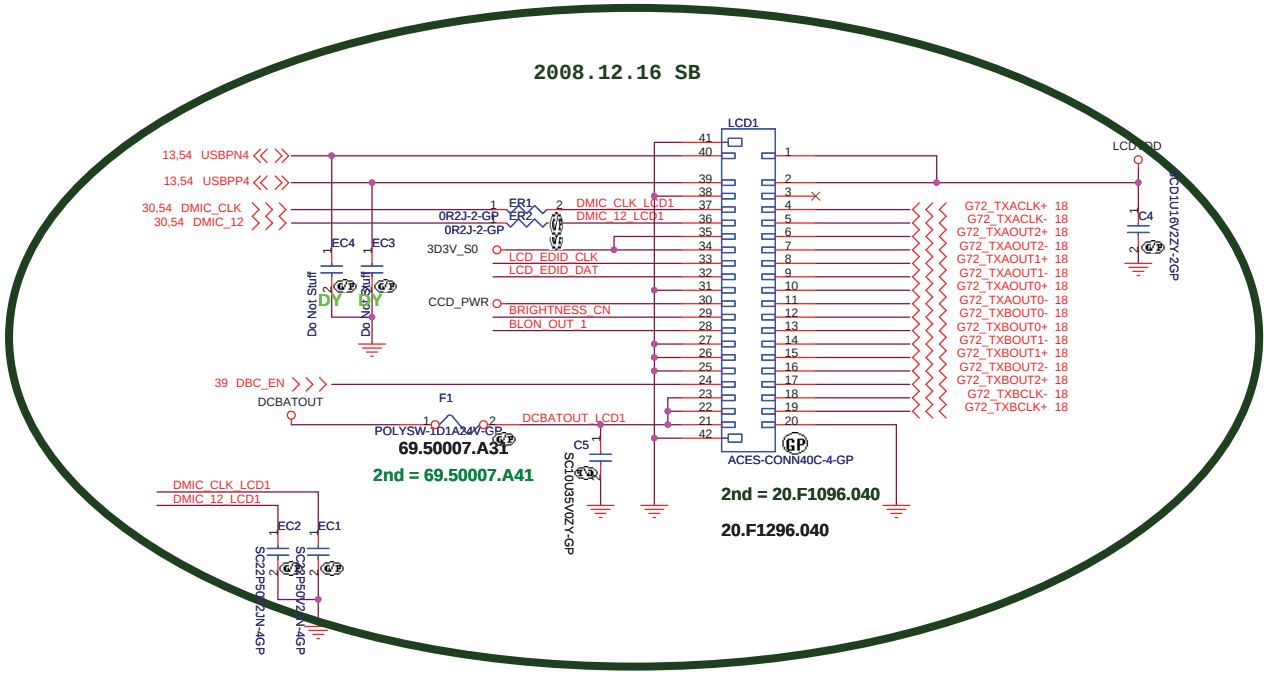
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DDR3 Socket		
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 16 of 55	

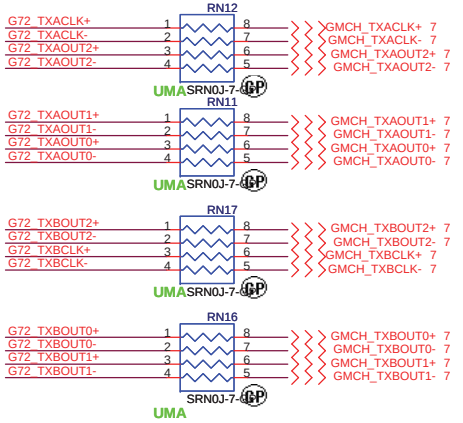
DDR3 SOCKET_2

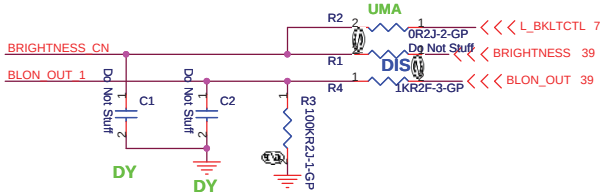


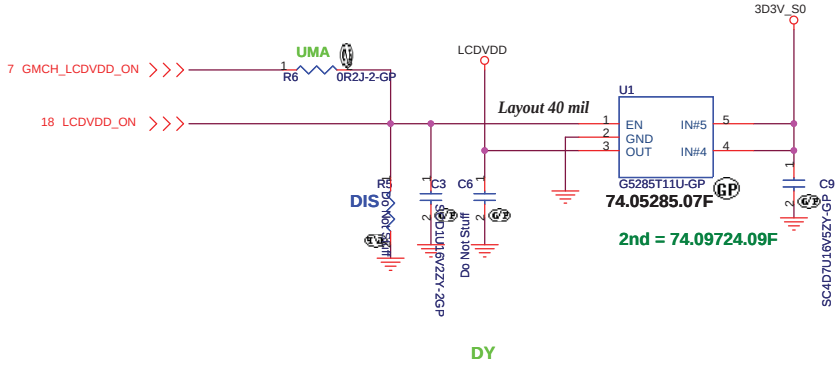
緯創資通 Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	DDR3 Socket2		
Size	Document Number		Rev
	JM70-MV		SB
Date: Saturday, December 20, 2008	Sheet 17 of 55		

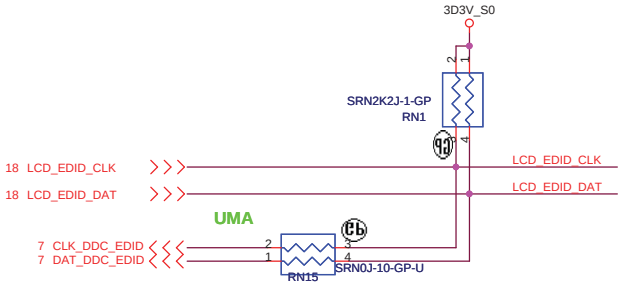

MXM3A
1 OF 3
MXM3B
2 OF 3
MXM3C
3 OF 3
DCBATOUT
5V_S0
3D3V_S0
2008.12.08 SB
2008.11.27 SB
Do Not Stuff
DIS
DY
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Graphic MXM 3.0 CONN
Size A2
Document Number JM70-MV
Rev SB
Date: Saturday, December 20, 2008
Sheet 18 of 55

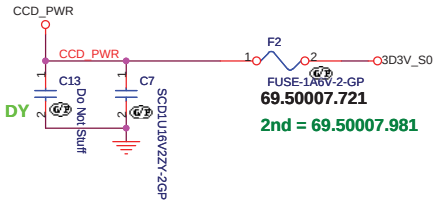








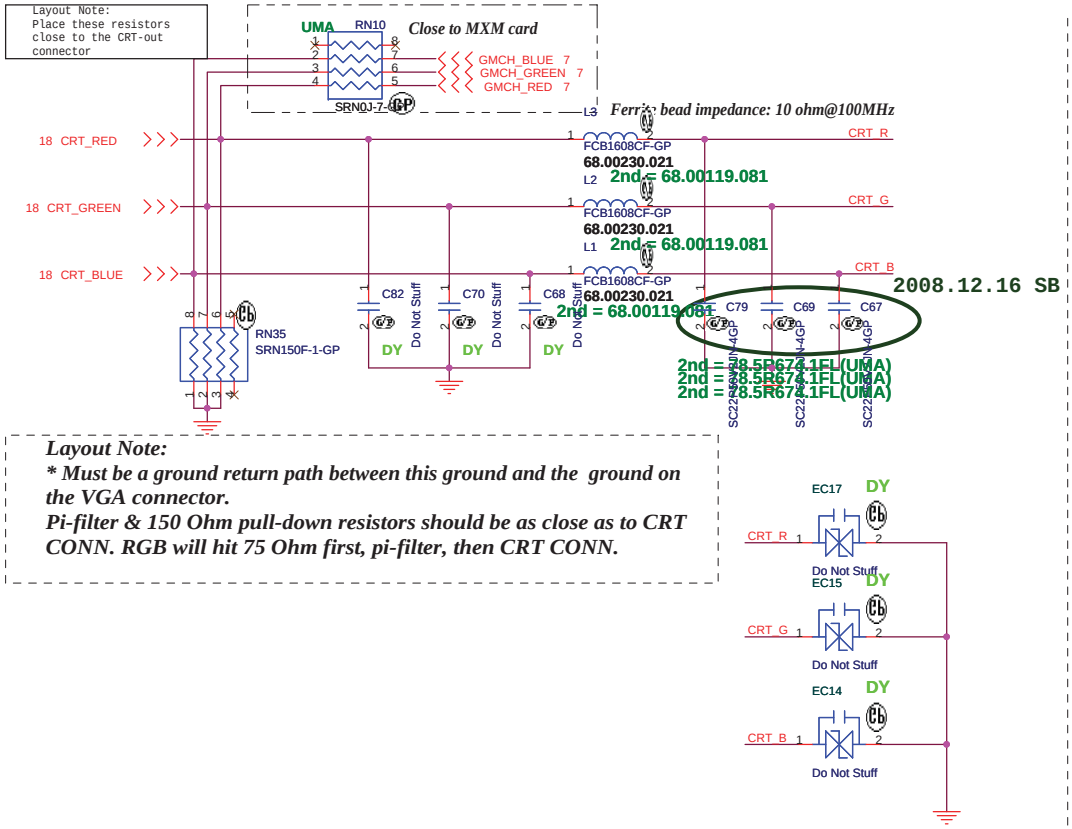


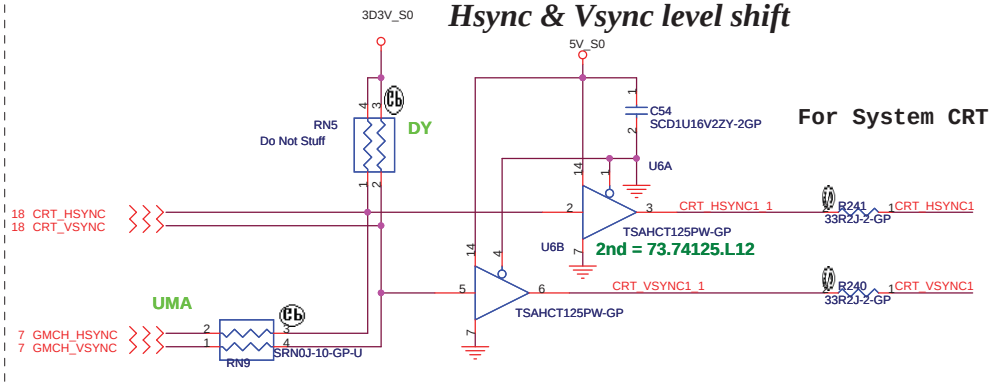


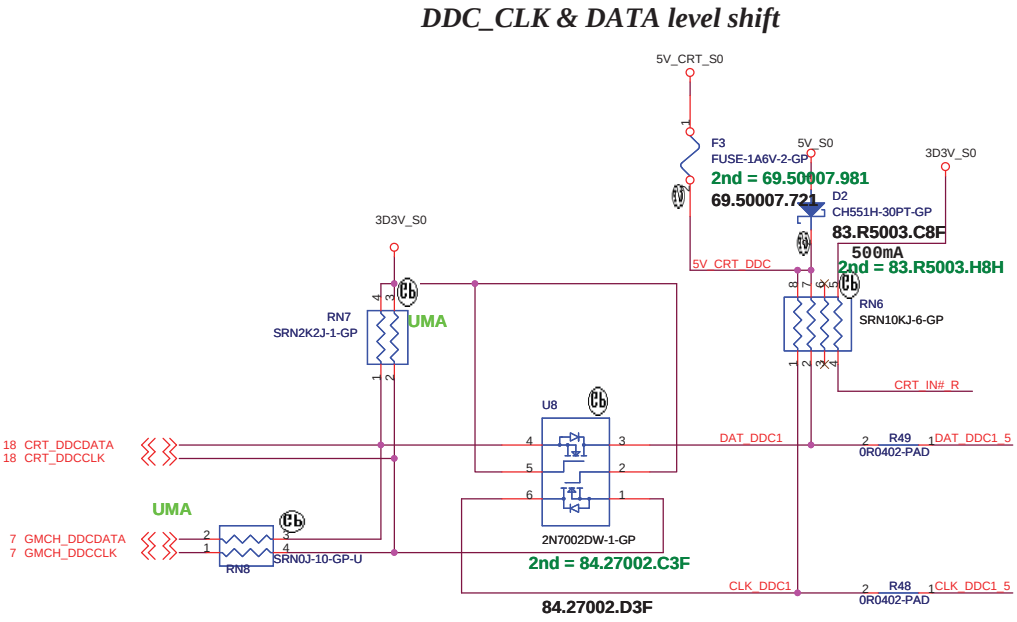
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

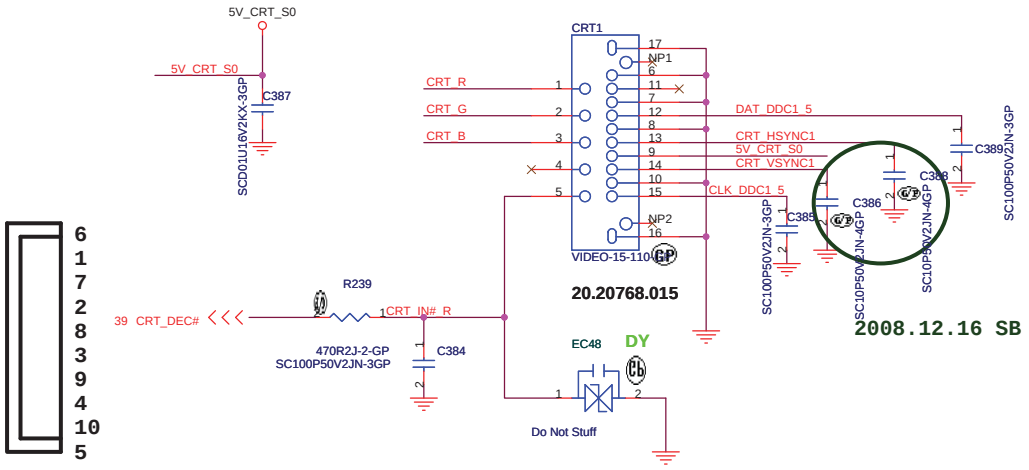
Title	**LCD CONN**	
Size	Document Number **JM70-MV**	Rev SB
Date: Saturday, December 20, 2008	Sheet 19 of 55	







CRT I/F & CONNECTOR



6 1 7 2 8 3 9 4 10 5

UMA

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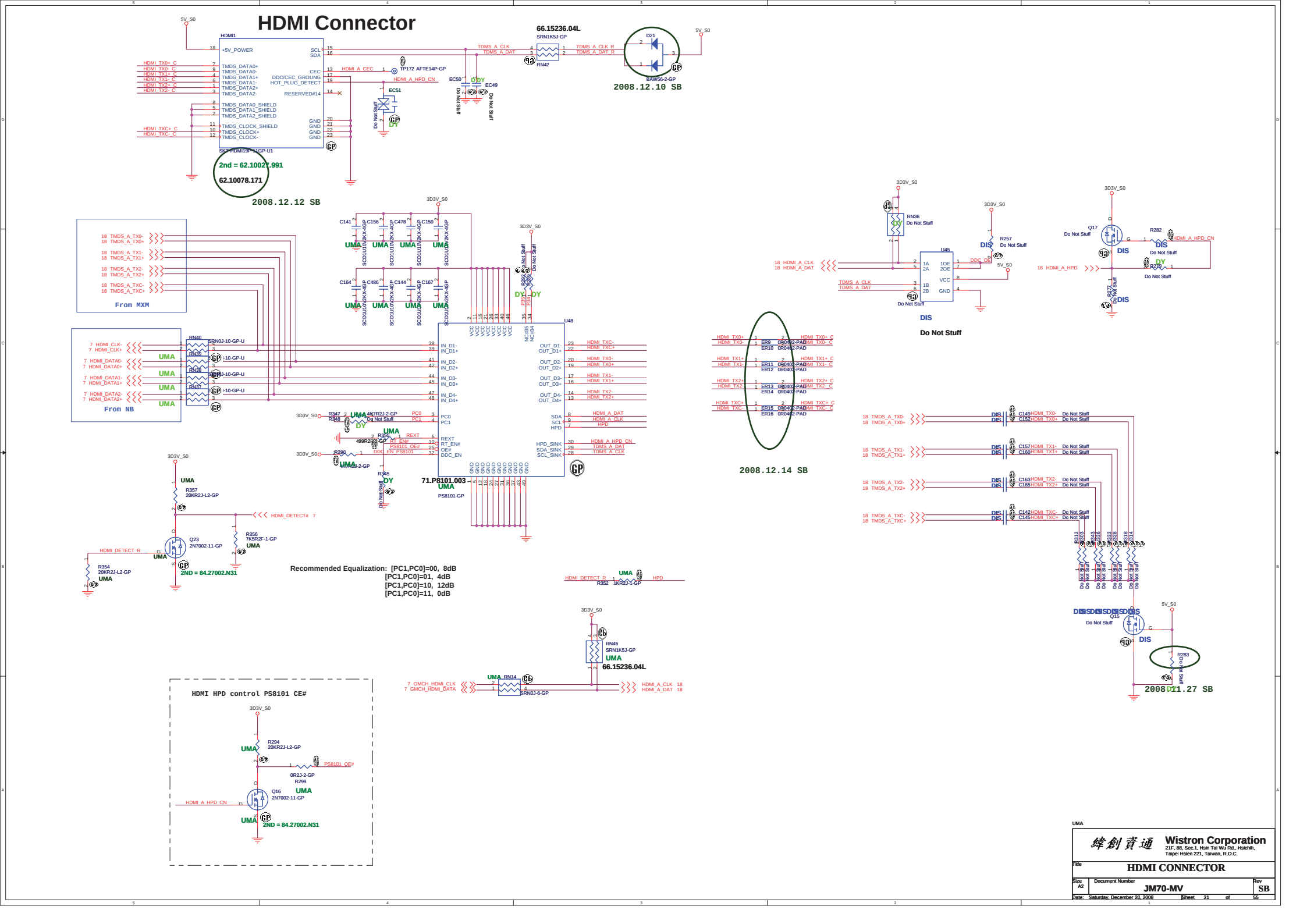
Title: CRT CONN		
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 20 of 55	

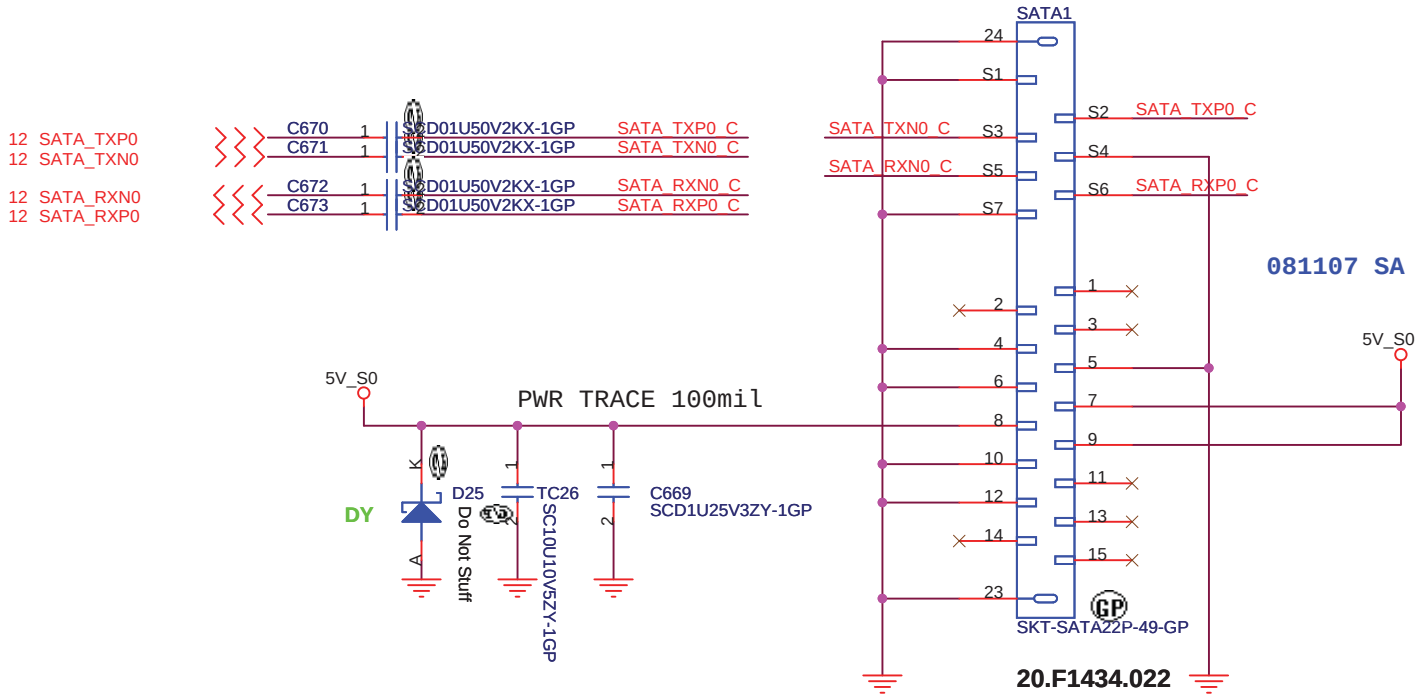
HDMI Connector



UMA

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: HDMI CONNECTOR	
Size: A2	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 21 of 55	

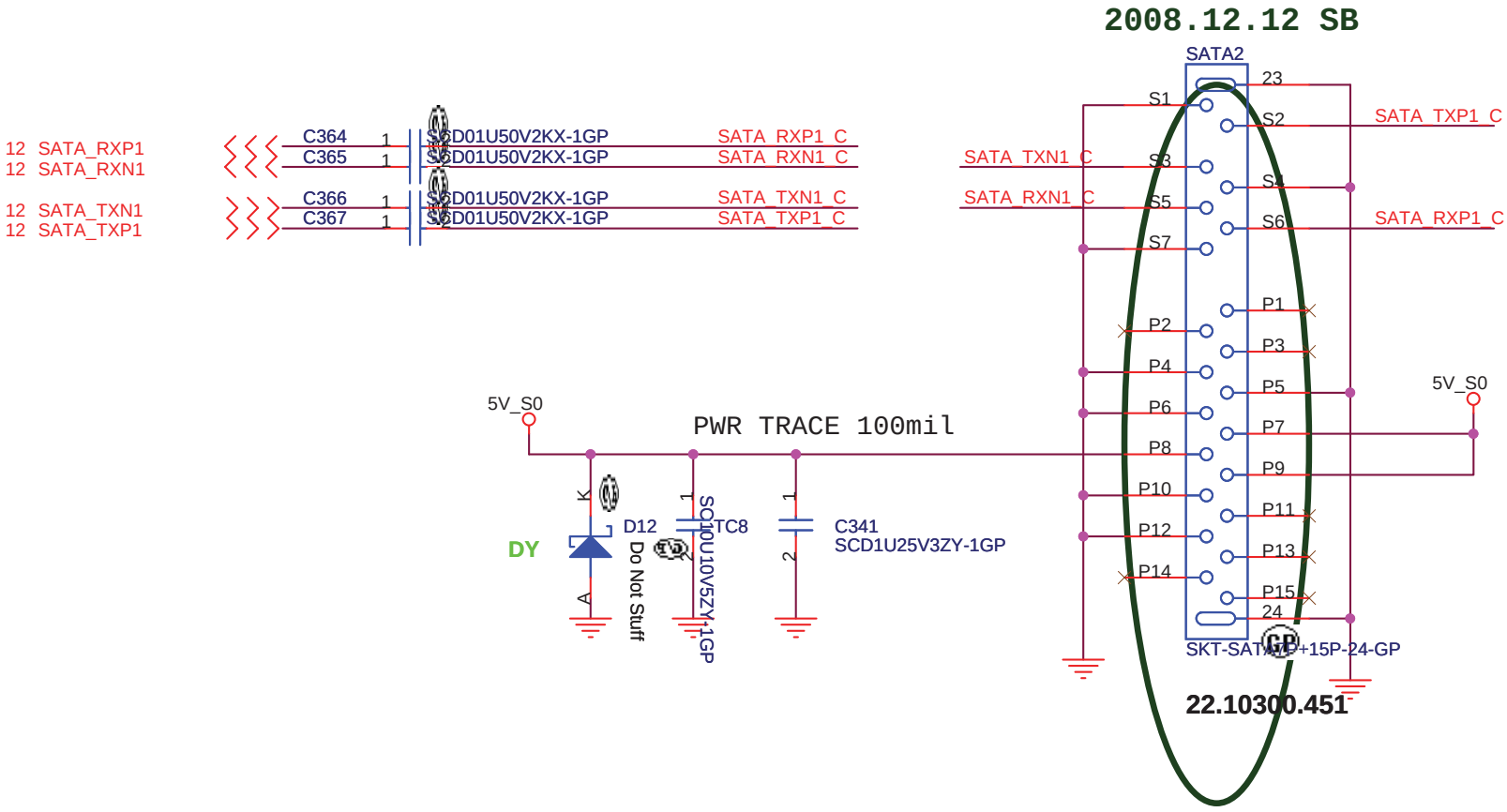
SATA Connector



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD CONN***	
Size	Document Number **JM70-MV**	Rev SB
Date: Saturday, December 20, 2008	Sheet 22 of 55	

2nd HDD SATA Connector



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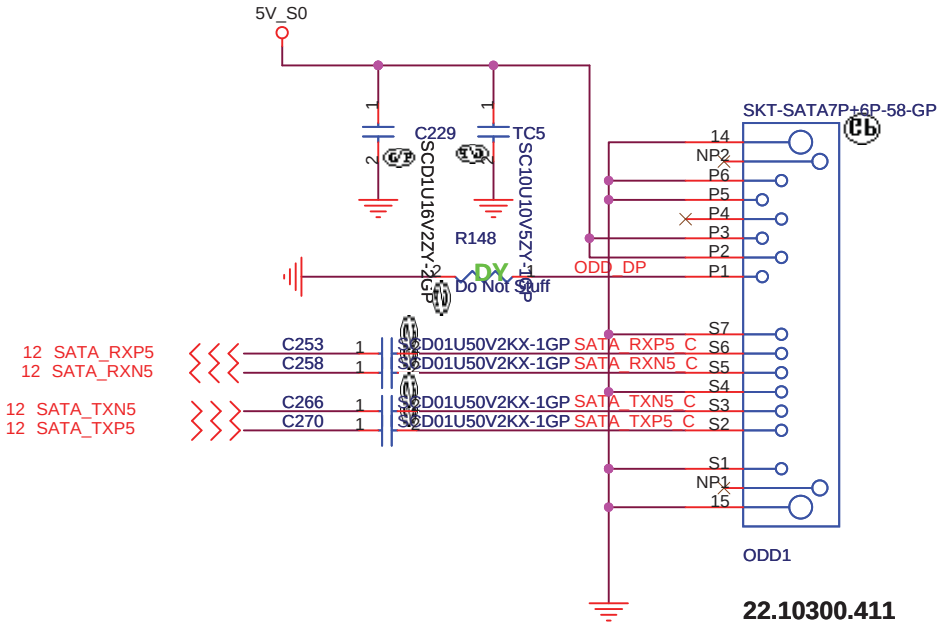
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *2nd HDD*		
Size	Document Number: **JM70-MV**	Rev: SB
Date: Saturday, December 20, 2008	Sheet 23 of 55	

ODD Connector



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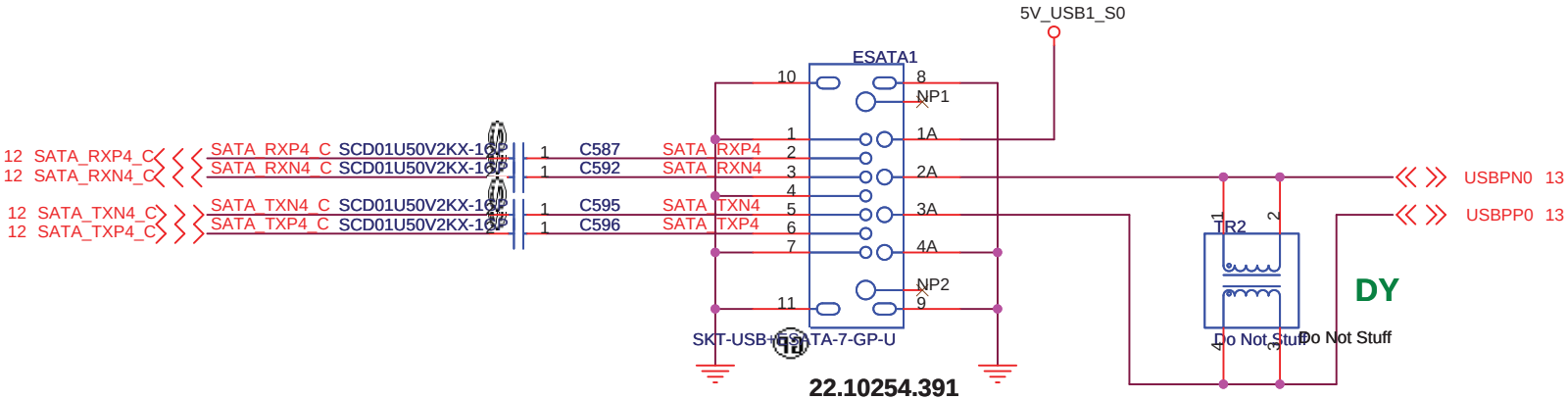
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***ODD***	
Size	Document Number **JM70-MV**	Rev SB
Date: Saturday, December 20, 2008	Sheet 24 of 55	

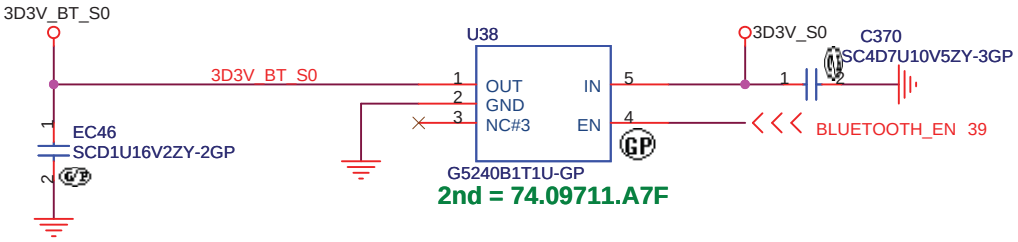
ESATA Connector



UMA

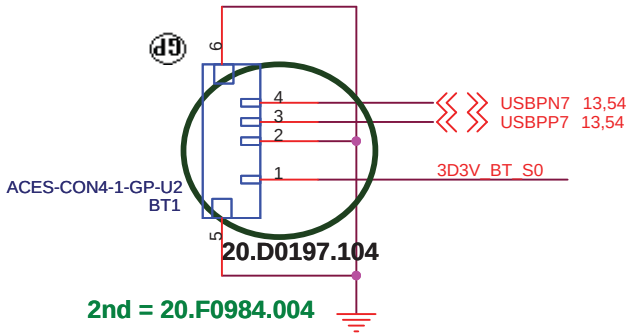
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *ESATA*		
Size: A4	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 25 of 55	

BLUETOOTH MODULE



EC20 put near BLUE1 / all USB put one choke near connector by EMI request

2008.12.08 SB

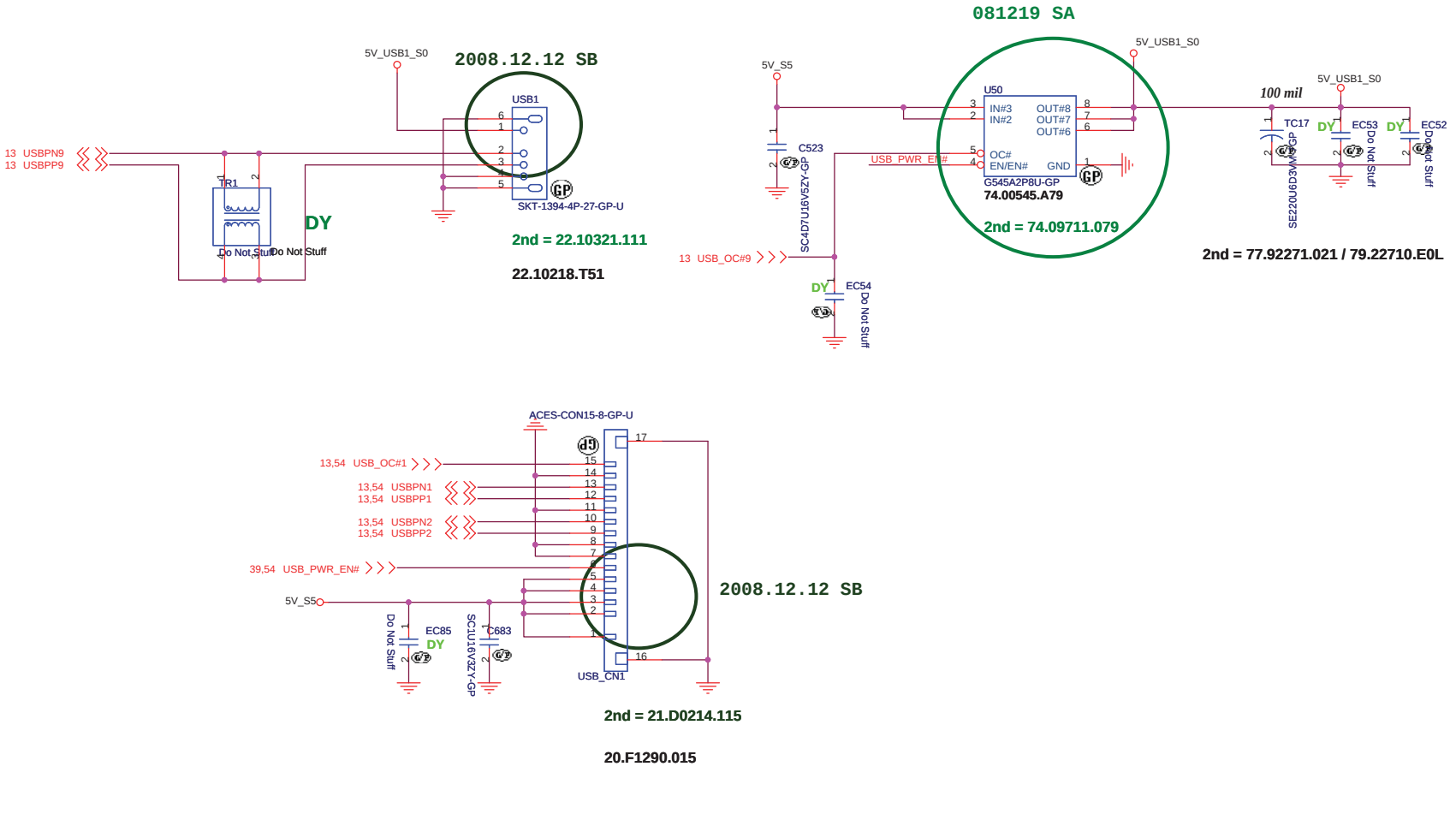


UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

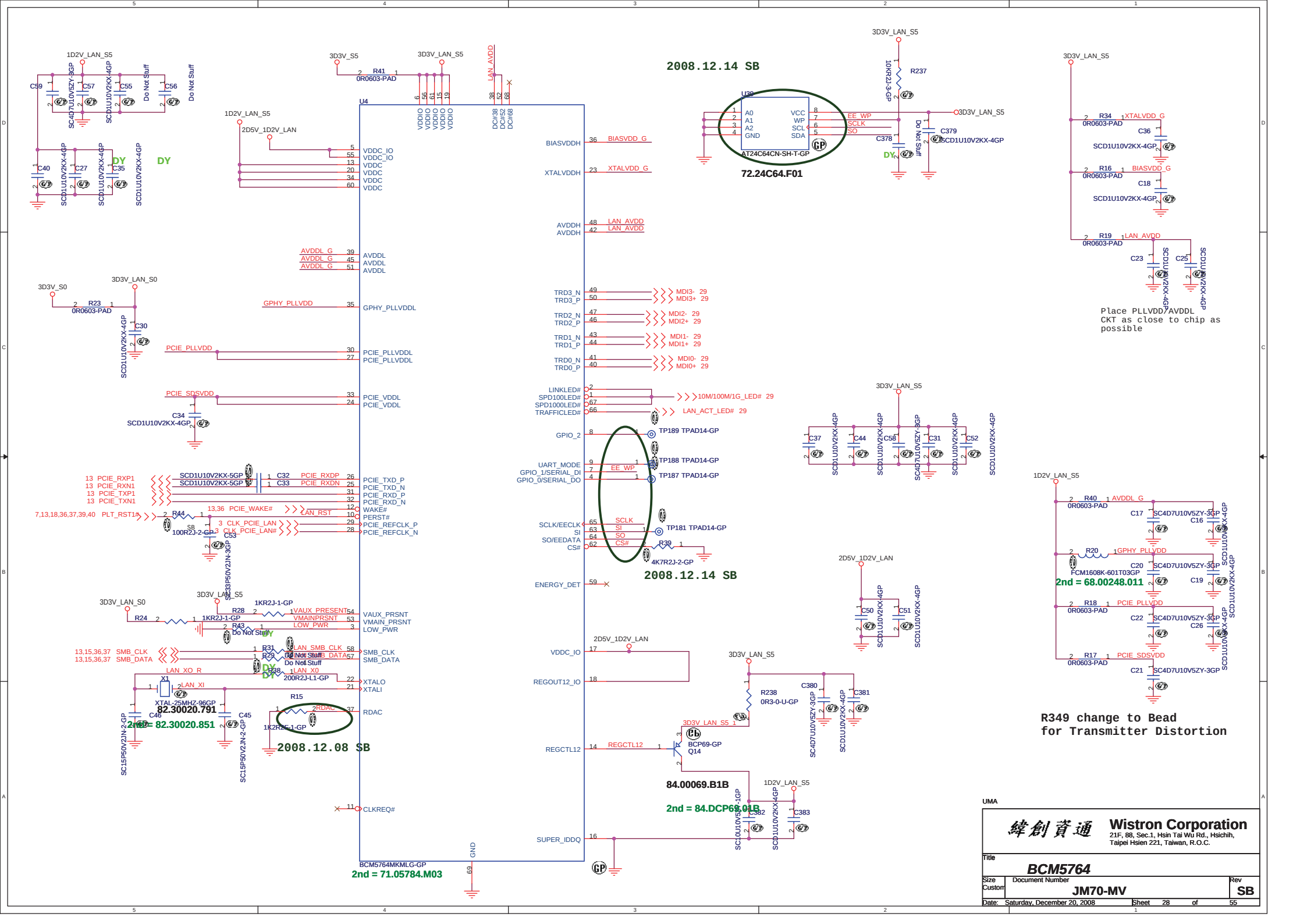
Title: ***BLUETOOTH***		
Size	Document Number: **JM70-MV**	Rev: SB
Date: Saturday, December 20, 2008	Sheet 26 of 55	

USB1 Connector



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *USB CONN*		
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 27 of 55	

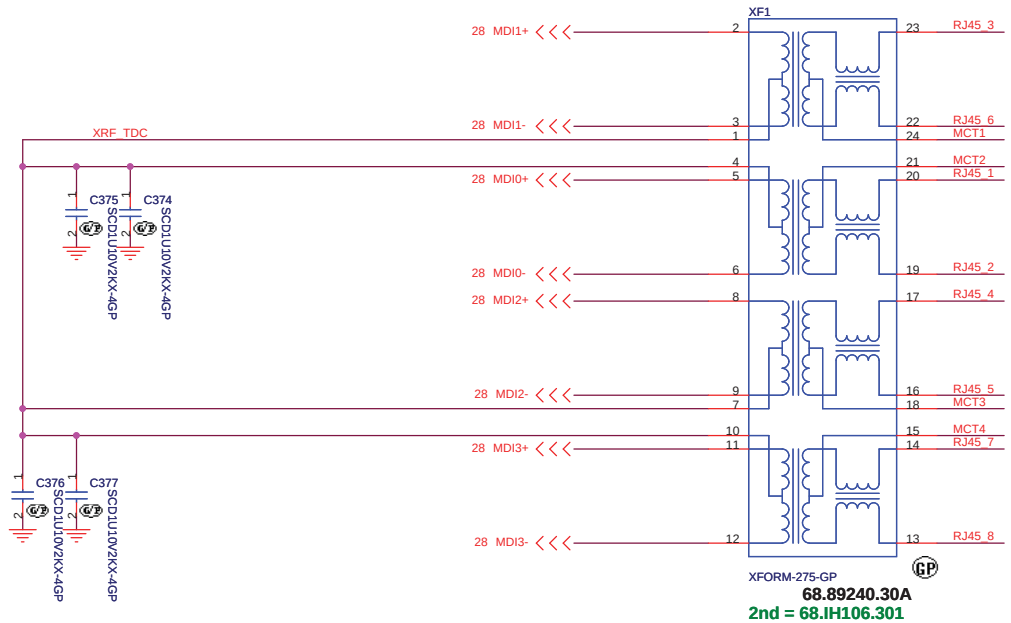

2008.12.14 SB
72.24C64.F01
BCM5764MKMLG-GP
2nd = 71.05784.M03
2008.12.14 SB
2008.12.08 SB
82.30020.791
2nd = 82.30020.851
84.00069.B1B
2nd = 84.DCP69.01B
2nd = 68.00248.011
Place PLLVDD/AVDDL CKT as close to chip as possible
R349 change to Bead for Transmitter Distortion
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5764
Size Custom
Document Number
JM70-MV
Rev
SB
Date: Saturday, December 20, 2008
Sheet 28 of 55

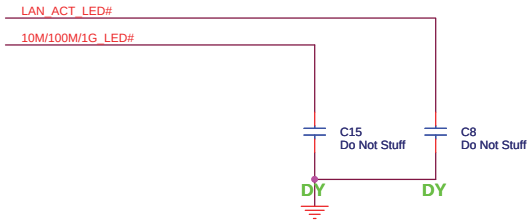
LAN Connector

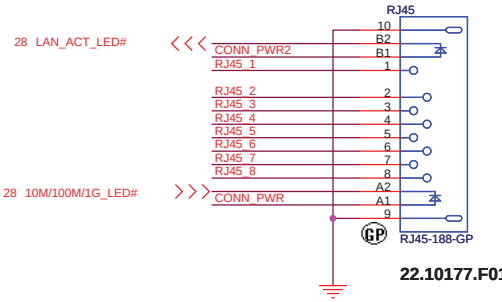
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

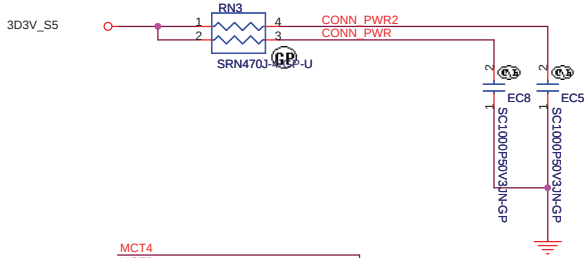
LAN Connector

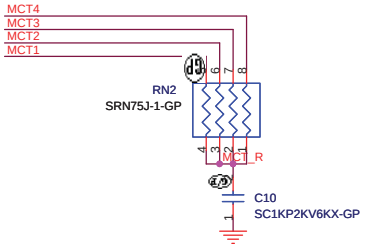
GIGA Lan Transformer





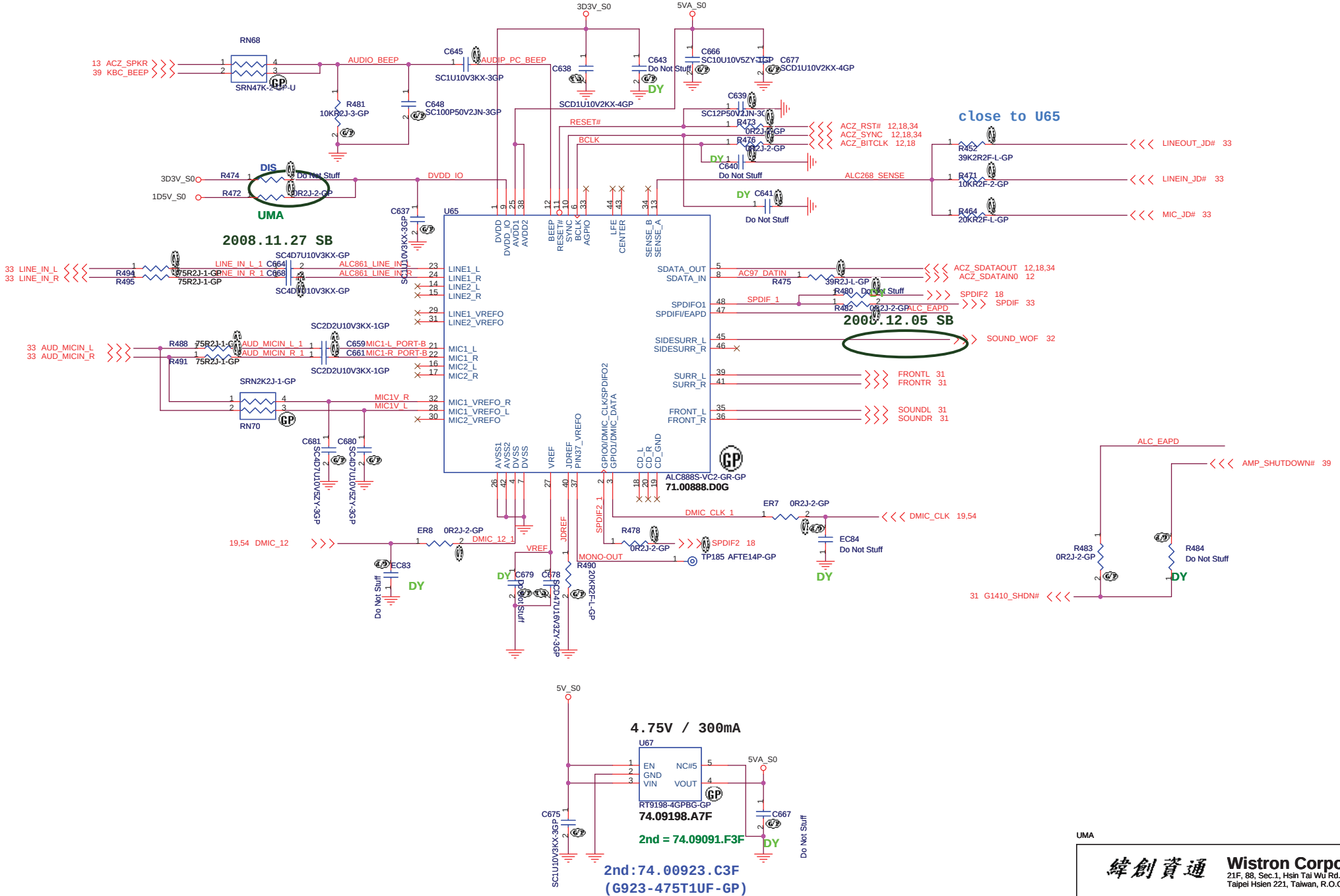






UMA

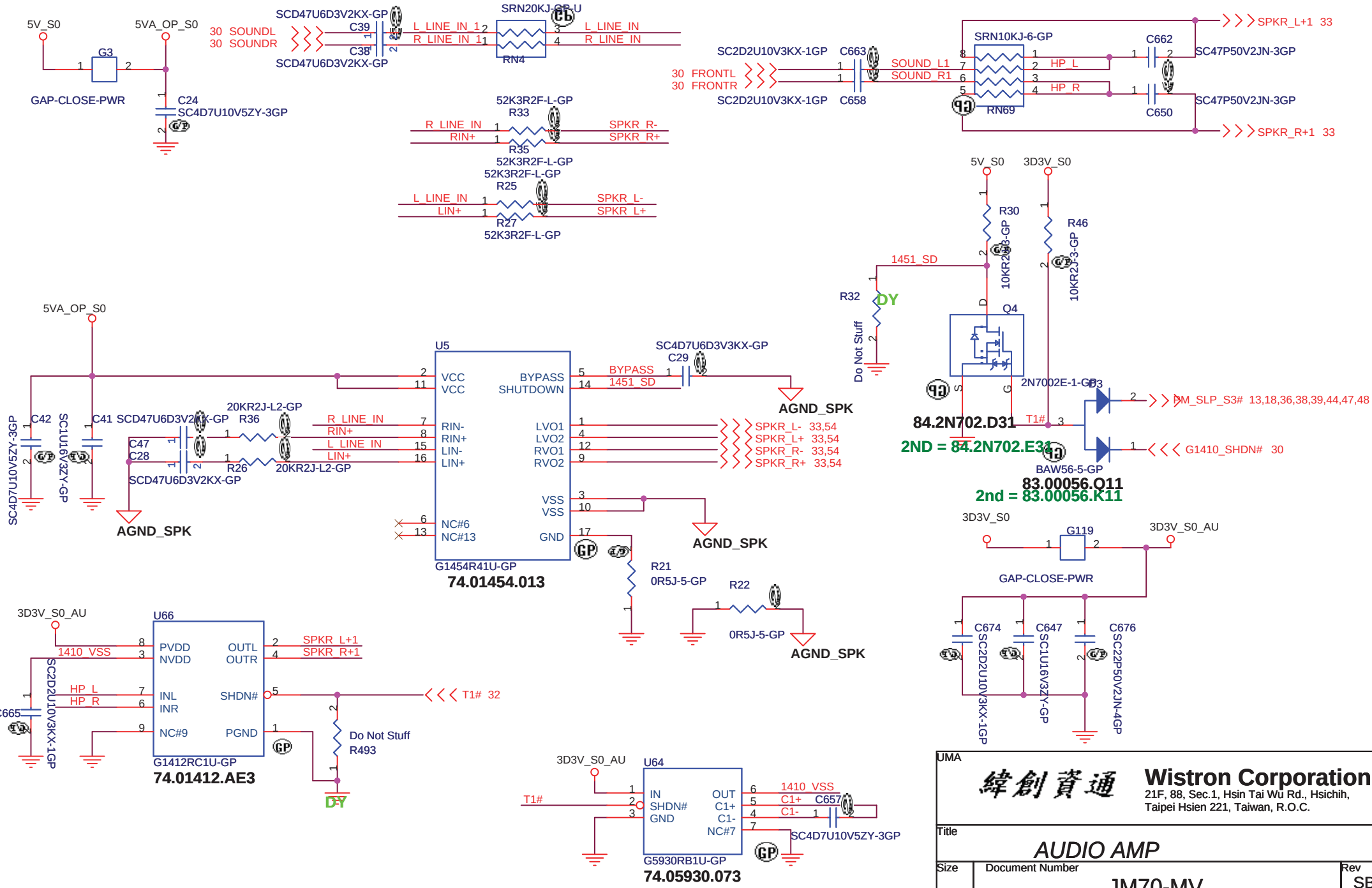
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN CONN		
Size: A3	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 29 of 55	



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Azalia codec ALC888***	
Size A3	Document Number **JM70-MV**	Rev **SB**
Date: Saturday, December 20, 2008	Sheet 30 of 55	

AUDIO OP AMPLIFIER



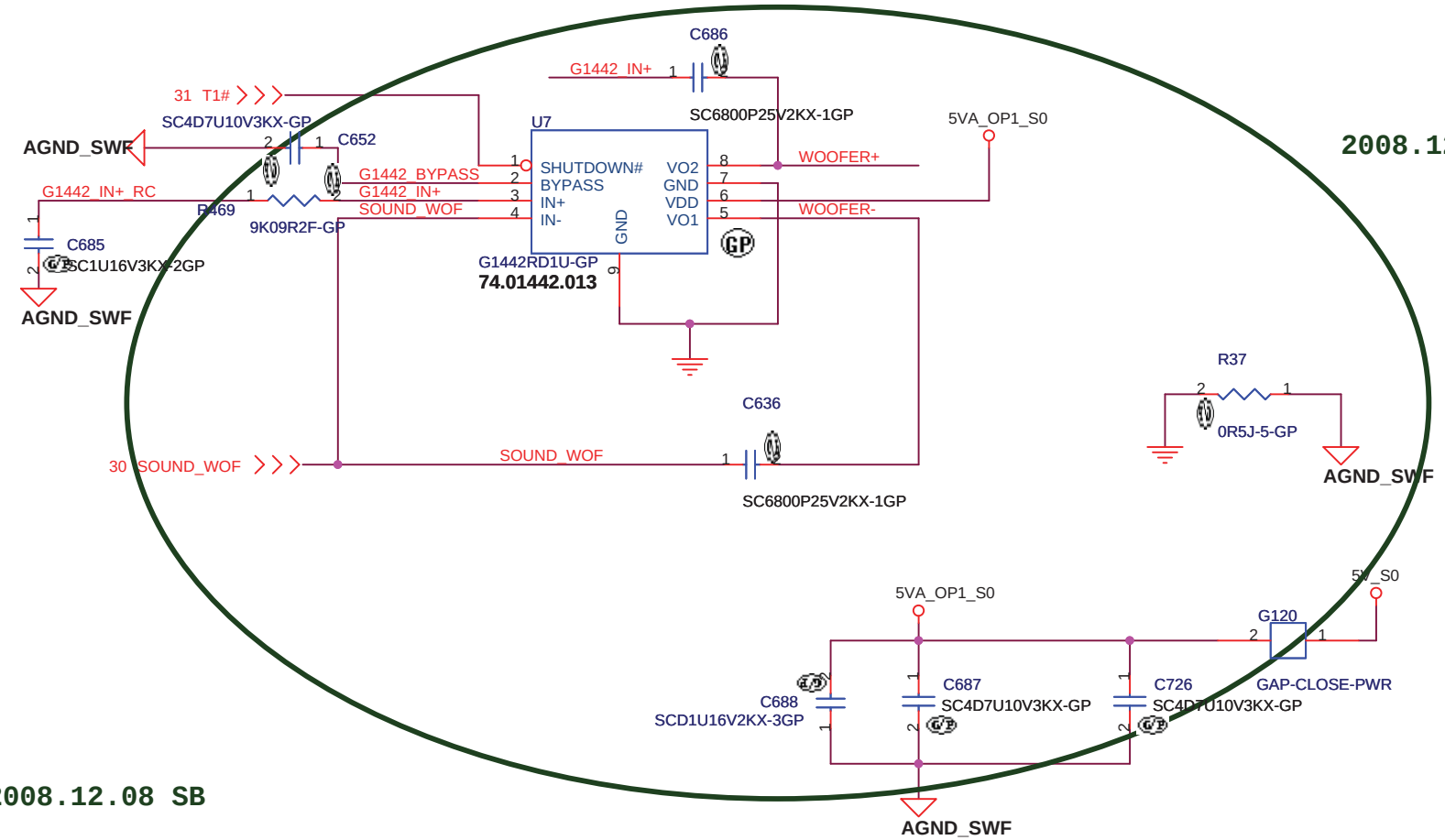
UMA

緯創資通

Wistron Corporation

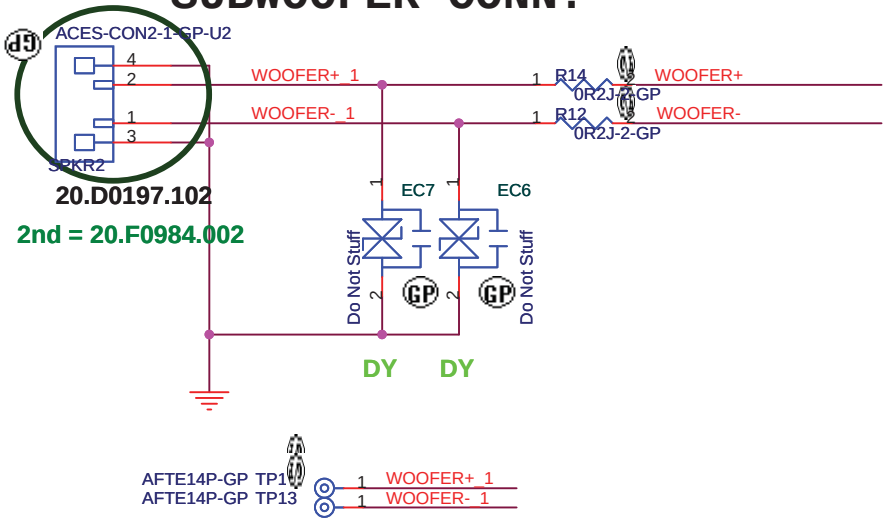
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO AMP	
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 31 of 55	



2008.12.08 SB

SUBWOOFER CONN.

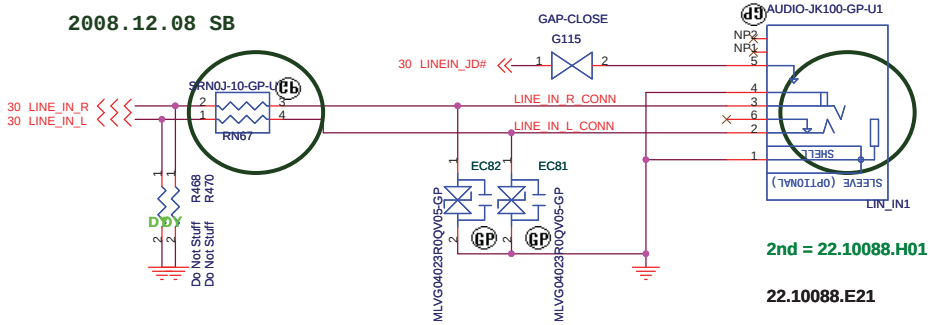


UMA

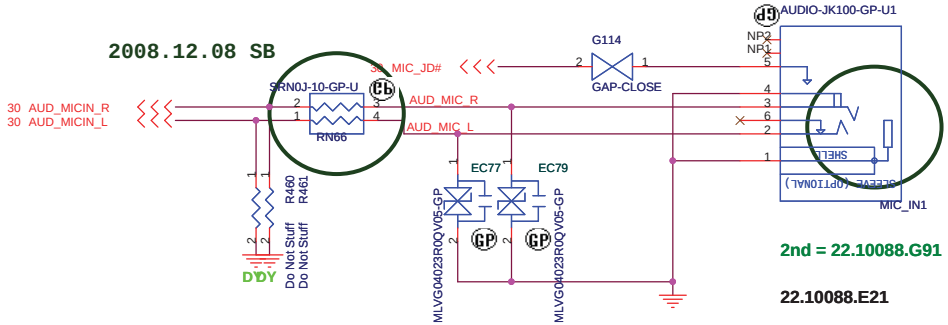
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	SUBWOOFER CONN.	
Size	Document Number JM70-MV	Rev SB
Date: Saturday, December 20, 2008	Sheet 32 of 55	

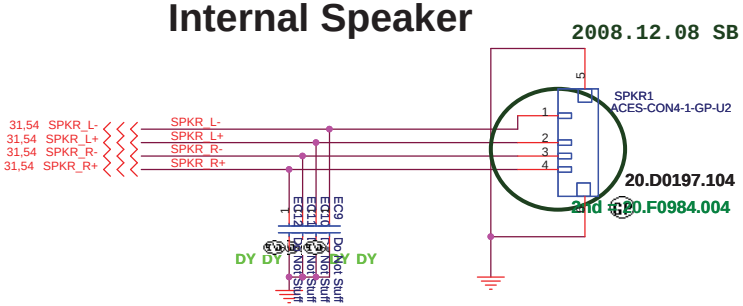
LINE IN



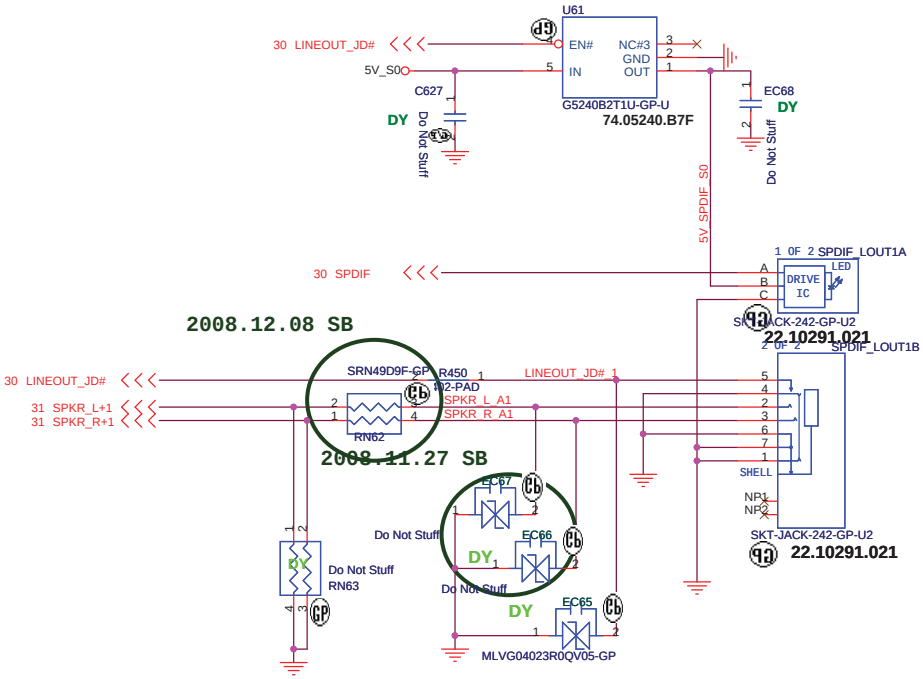
MIC IN



Internal Speaker



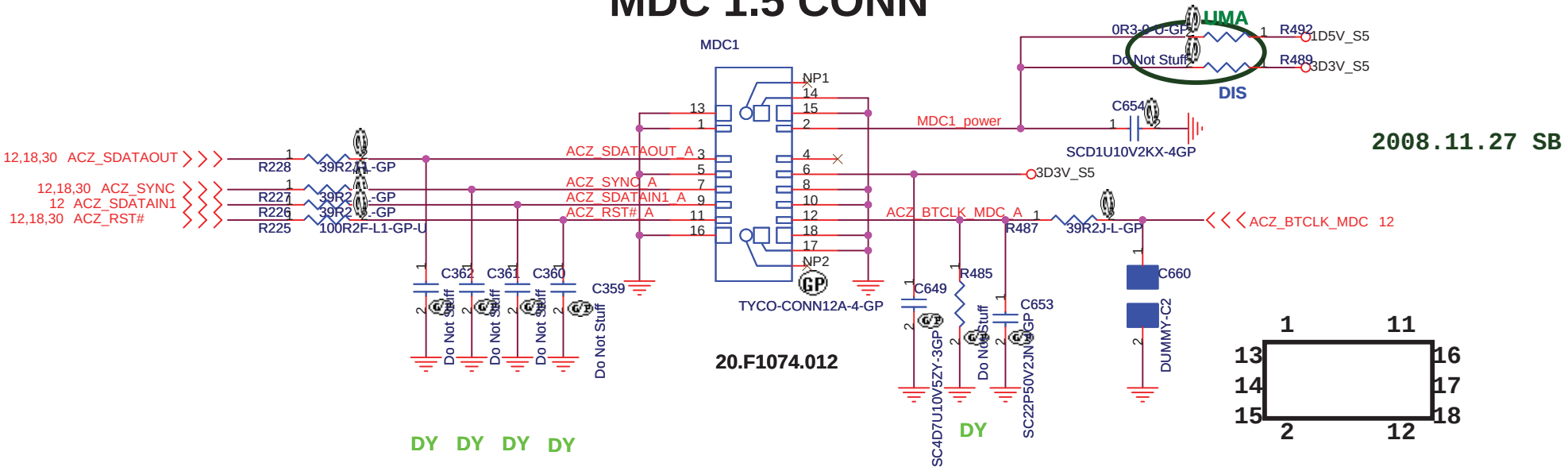
LINE OUT / SPDIF



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO jack		
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 33 of 55	

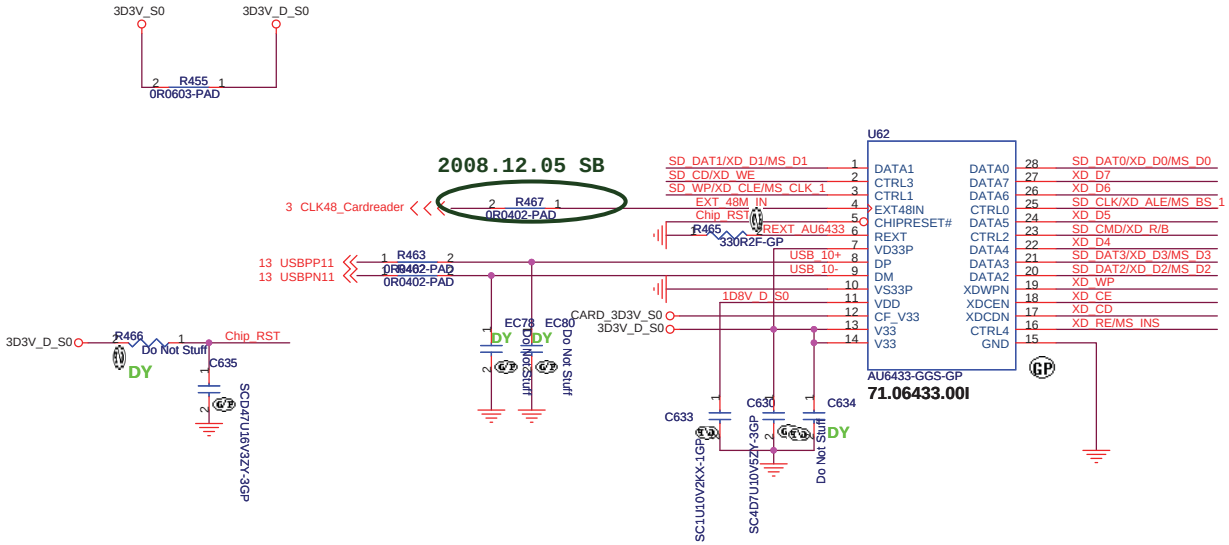
MDC 1.5 CONN



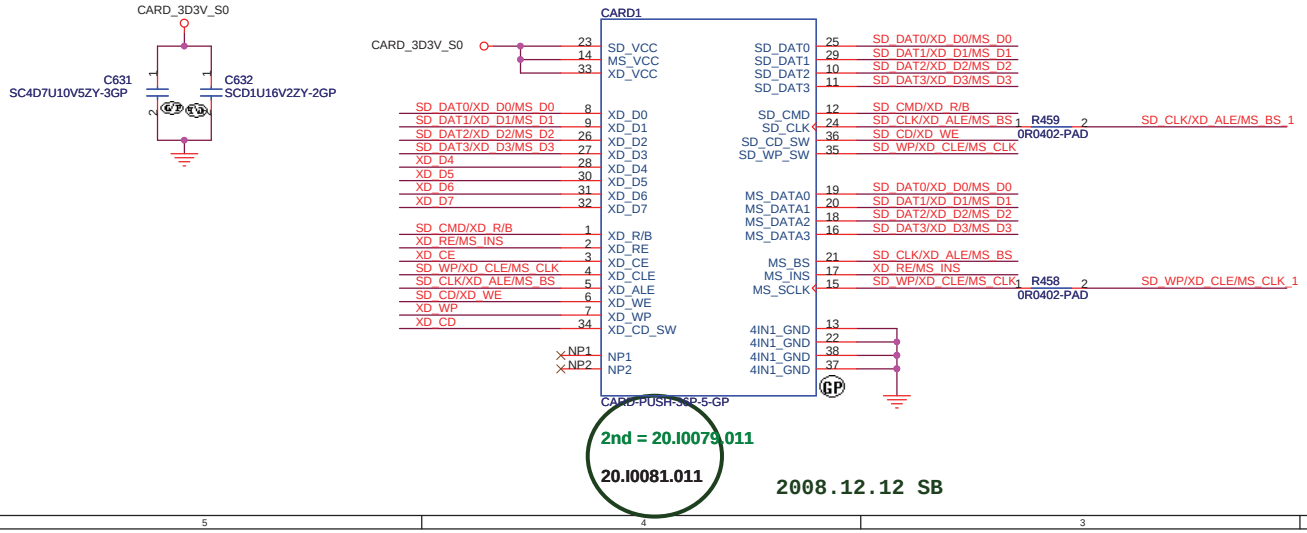
2008.11.27 SB

UMA

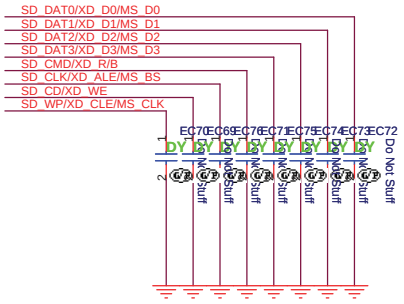
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC		
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 34 of	55



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)

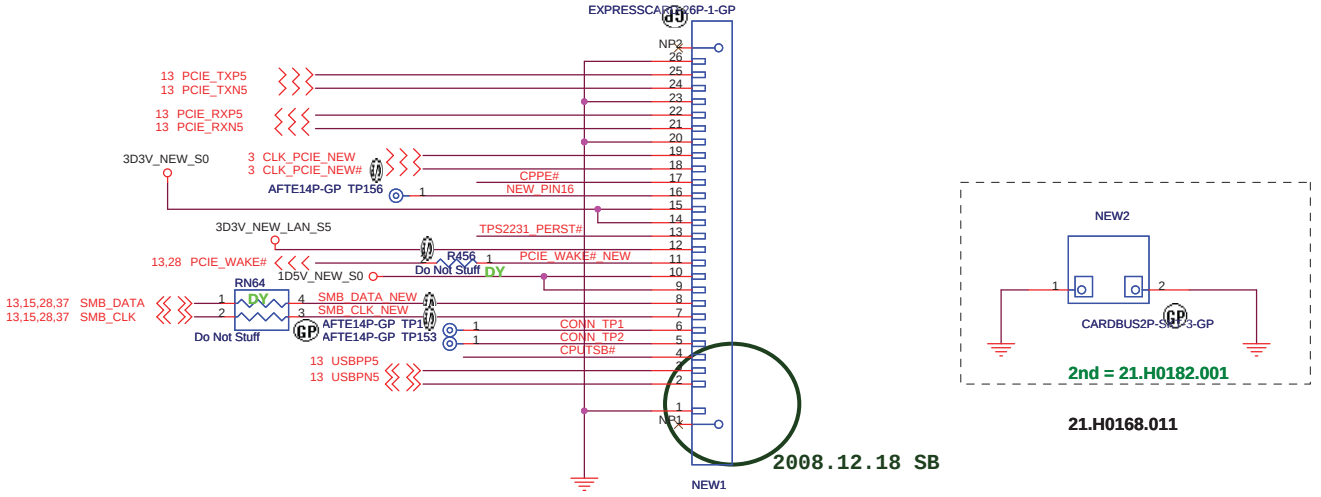


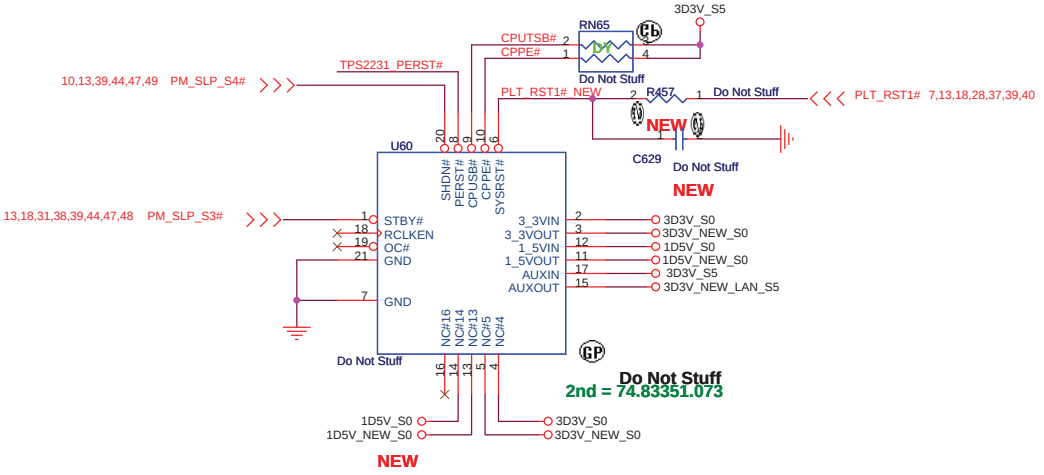
EMI capacitor



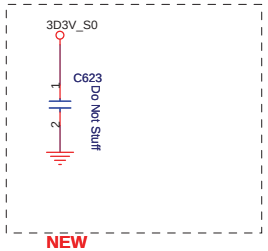
UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*Cardreader*	
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 35 of 55	

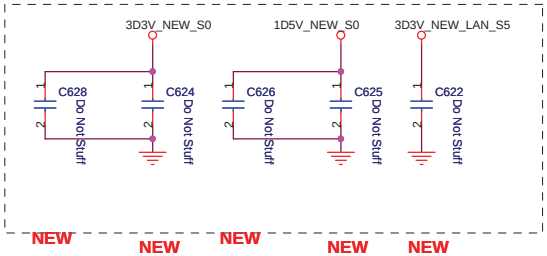




Place them Near to Chip



Place them Near to Connector



UMA

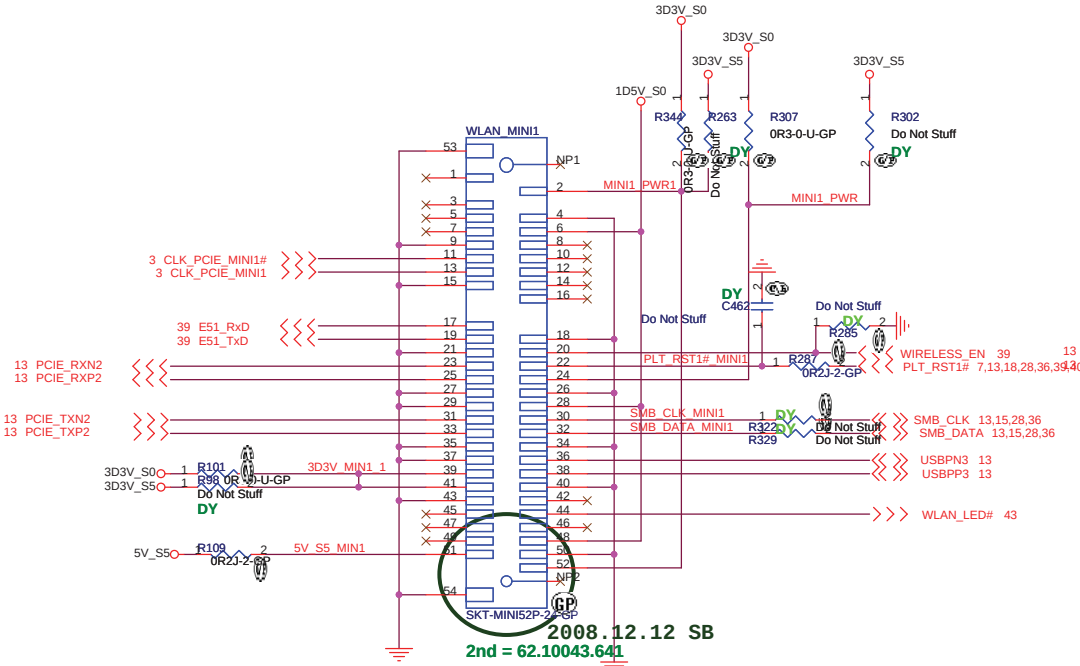
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **NEW CARD**

Size	Document Number	Rev
	JM70-MV	SB

Date: Saturday, December 20, 2008 Sheet 36 of 55

Mini1 Card Connector(WLAN)
Support debug-card

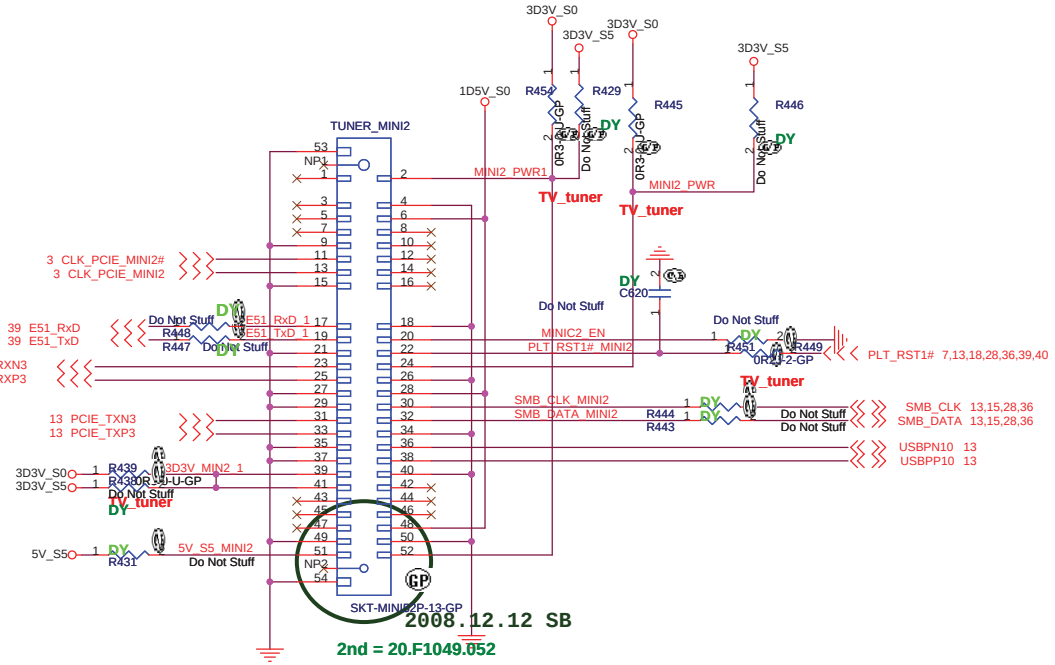


2008.12.12 SB

2nd = 62.10043.641

62.10043.611

Mini2 Card Connector(TV tuner)



2008.12.12 SB

2nd = 20.F1049.052

62.10043.461

TV_tuner

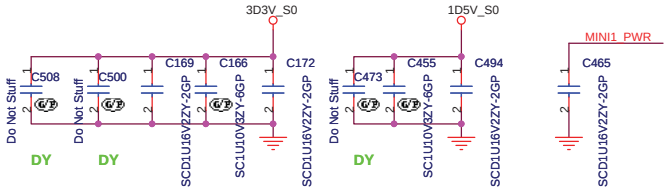
R453

WIRELESS_EN — MINIC2_EN

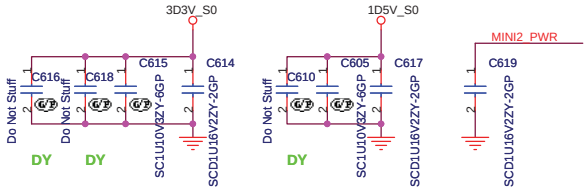
Do Not Stuff

DY

Place near MINI1

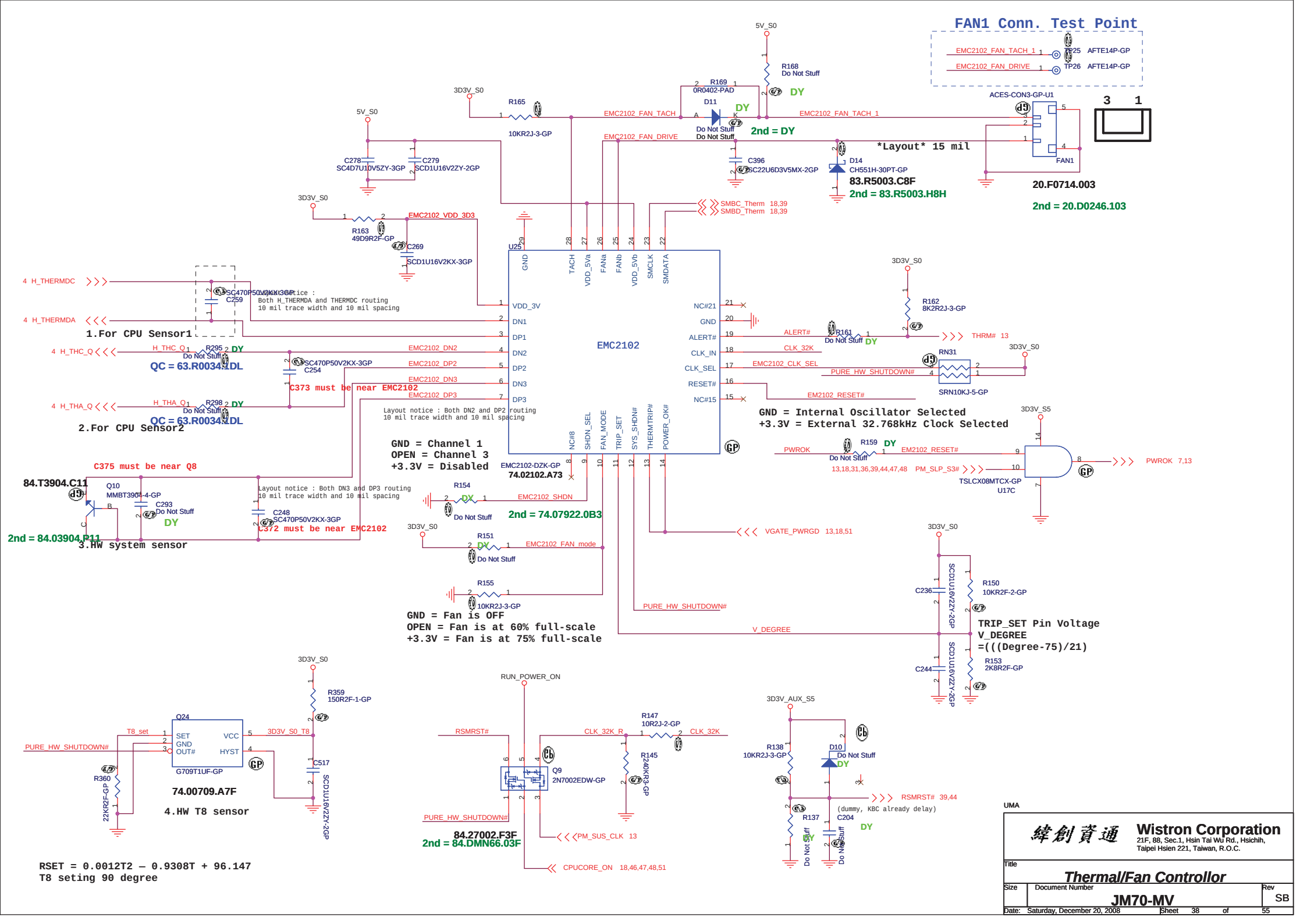


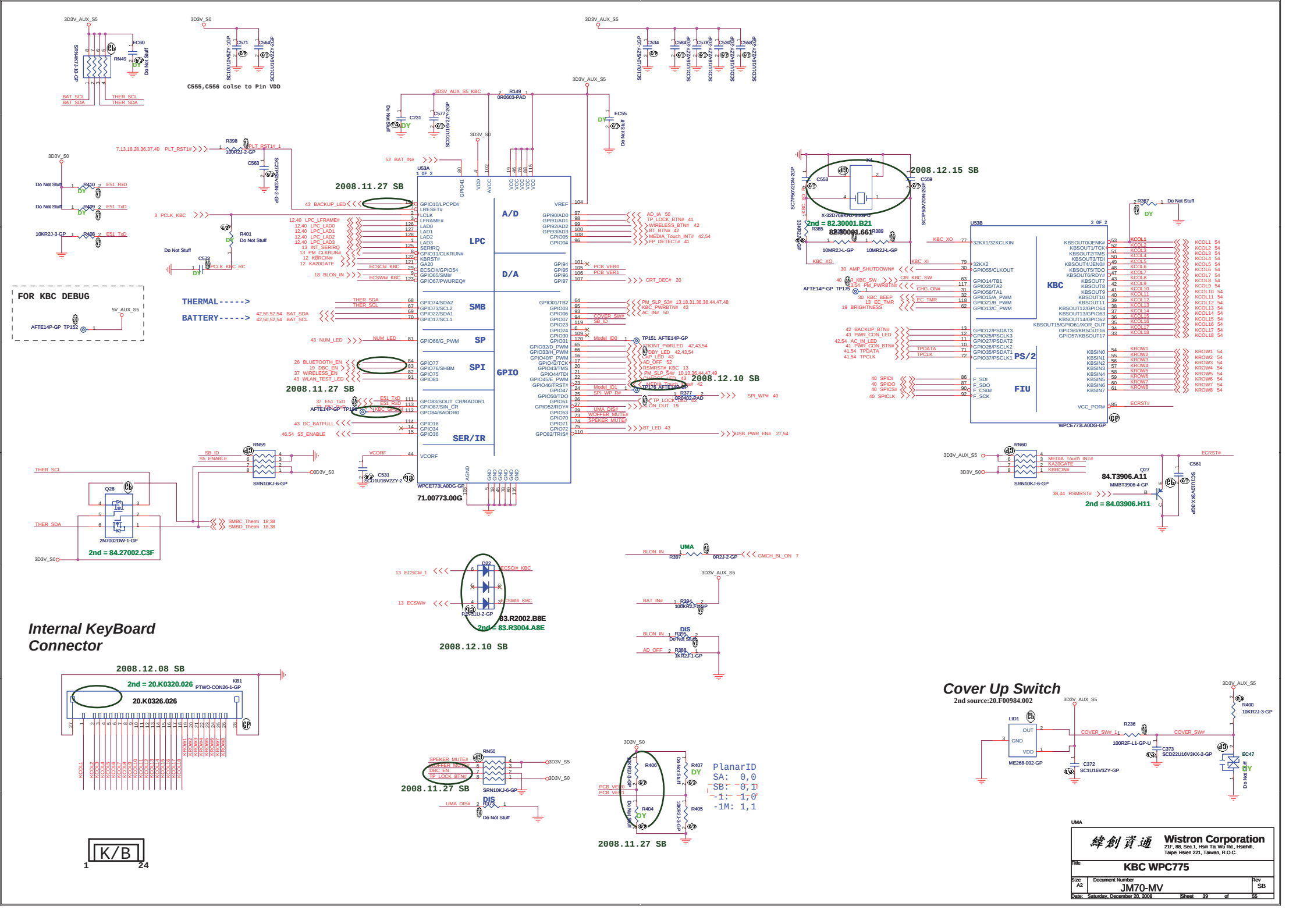
Place near MINIC2



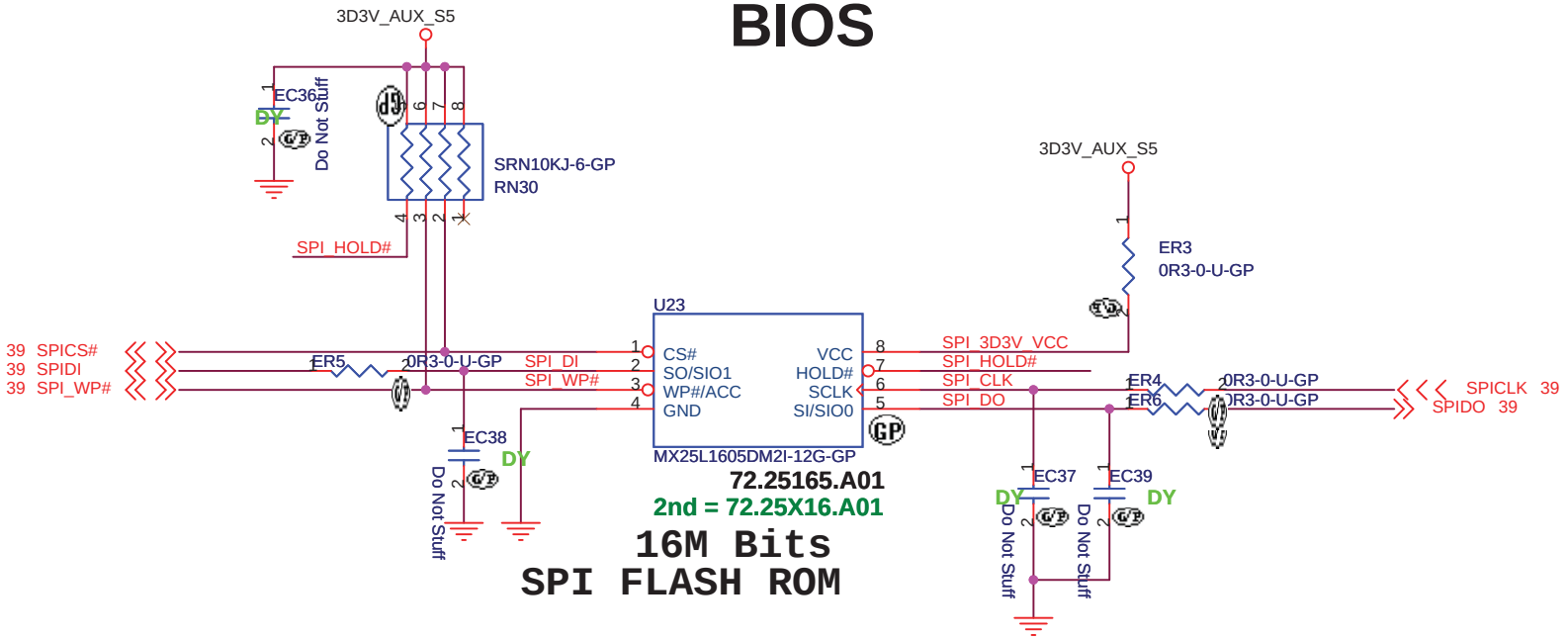
UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size: A3	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 37 of 55	

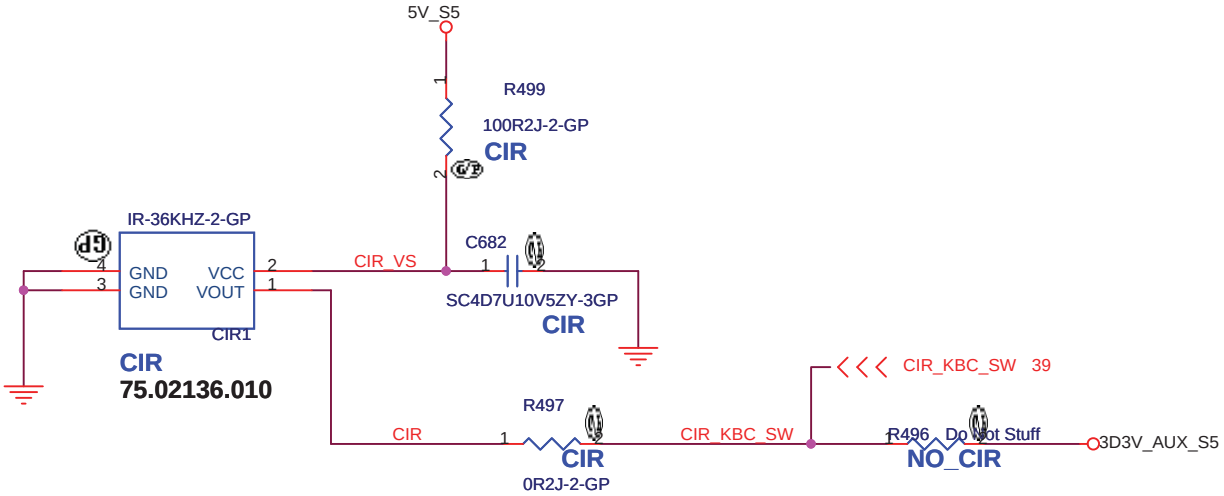

FAN1 Conn. Test Point
EMC2102_FAN_TACH_1
TP25 AFTE14P-GP
EMC2102_FAN_DRIVE
TP26 AFTE14P-GP
ACES-CON3-GP-U1
FAN1
Layout 15 mil
20.F0714.003
2nd = 20.D0246.103
83.R5003.C8F
2nd = 83.R5003.H8H
2nd = DY
EMC2102
U25
1.For CPU Sensor1
2.For CPU Sensor2
3.HW system sensor
4.HW T8 sensor
QC = 63.R0034.1DL
C373 must be near EMC2102
C375 must be near Q8
C372 must be near EMC2102
84.T3904.C11
2nd = 84.03904.P11
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled
2nd = 74.07922.0B3
EMC2102-DZK-GP
74.02102.A73
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale
TRIP_SET Pin Voltage
V_DEGREE
=(((Degree-75)/21)
74.00709.A7F
RSET = 0.0012T2 – 0.9308T + 96.147
T8 seting 90 degree
84.27002.F3F
2nd = 84.DMN66.03F
Layout notice : Both H_THERMDA and THERMDC routing 10 mil trace width and 10 mil spacing
Layout notice : Both DN2 and DP2 routing 10 mil trace width and 10 mil spacing
Layout notice : Both DN3 and DP3 routing 10 mil trace width and 10 mil spacing
SMBC_Therm 18,39
SMBD_Therm 18,39
VGATE_PWRGD 13,18,51
PURE_HW_SHUTDOWN#
V_DEGREE
PM_SUS_CLK 13
CPUCORE_ON 18,46,47,48,51
RSMRST# 39,44
PWROK 7,13
13,18,31,36,39,44,47,48 PM_SLP_S3#
THRM# 13
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Thermal/Fan Controllor
JM70-MV
SB
Date: Saturday, December 20, 2008
Sheet 38 of 55


FOR KBC DEBUG
THERMAL----->
BATTERY----->
U53A
WPCE773LA0DG-GP
71.00773.00G
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
U53B
KBC
PS/2
FIU
WPCE773LA0DG-GP
2008.11.27 SB
2008.12.10 SB
2008.12.15 SB
2nd = 82.30001.B21
82.30001.661
2nd = 84.27002.C3F
83.R2002.B8E
2nd = 83.R3004.A8E
2nd = 84.03906.H11
2nd = 20.K0320.026
20.K0326.026
2008.12.08 SB
Internal KeyBoard Connector
Cover Up Switch
2nd source:20.F00984.002
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
K/B
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775
JM70-MV
Size A2
Rev SB
Date: Saturday, December 20, 2008
Sheet 39 of 55

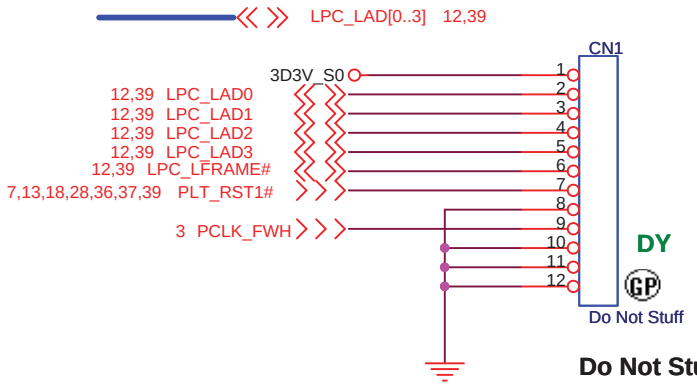
BIOS



VISHAY CIR Module



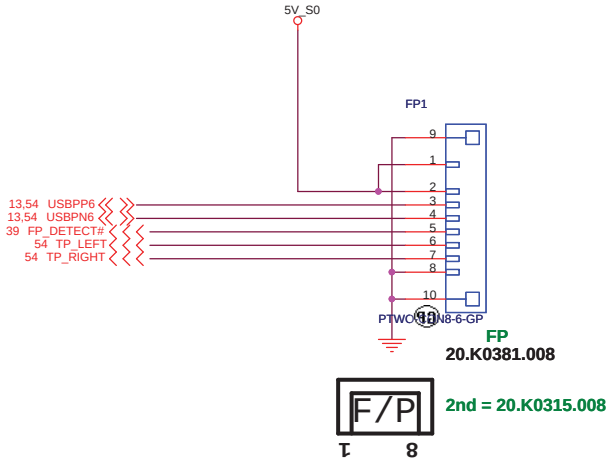
GOLDEN FINGER FOR DEBUG BOARD



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BIOS		
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 40 of 55	

Finger printer

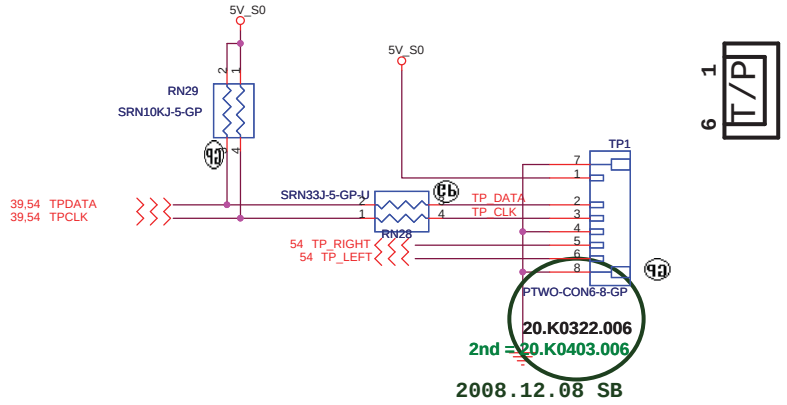


FP

20.K0381.008

2nd = 20.K0315.008

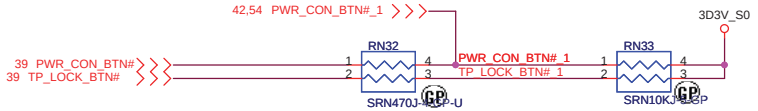
Touch Pad

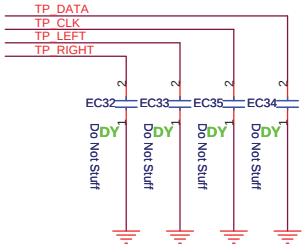


20.K0322.006

2nd = 20.K0403.006

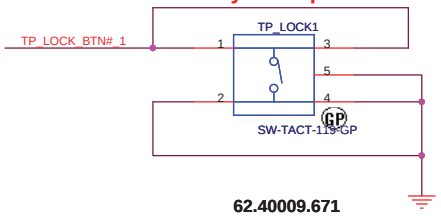
2008.12.08 SB





TP_LOCK key

Note. main with 2nd symbol pin define different



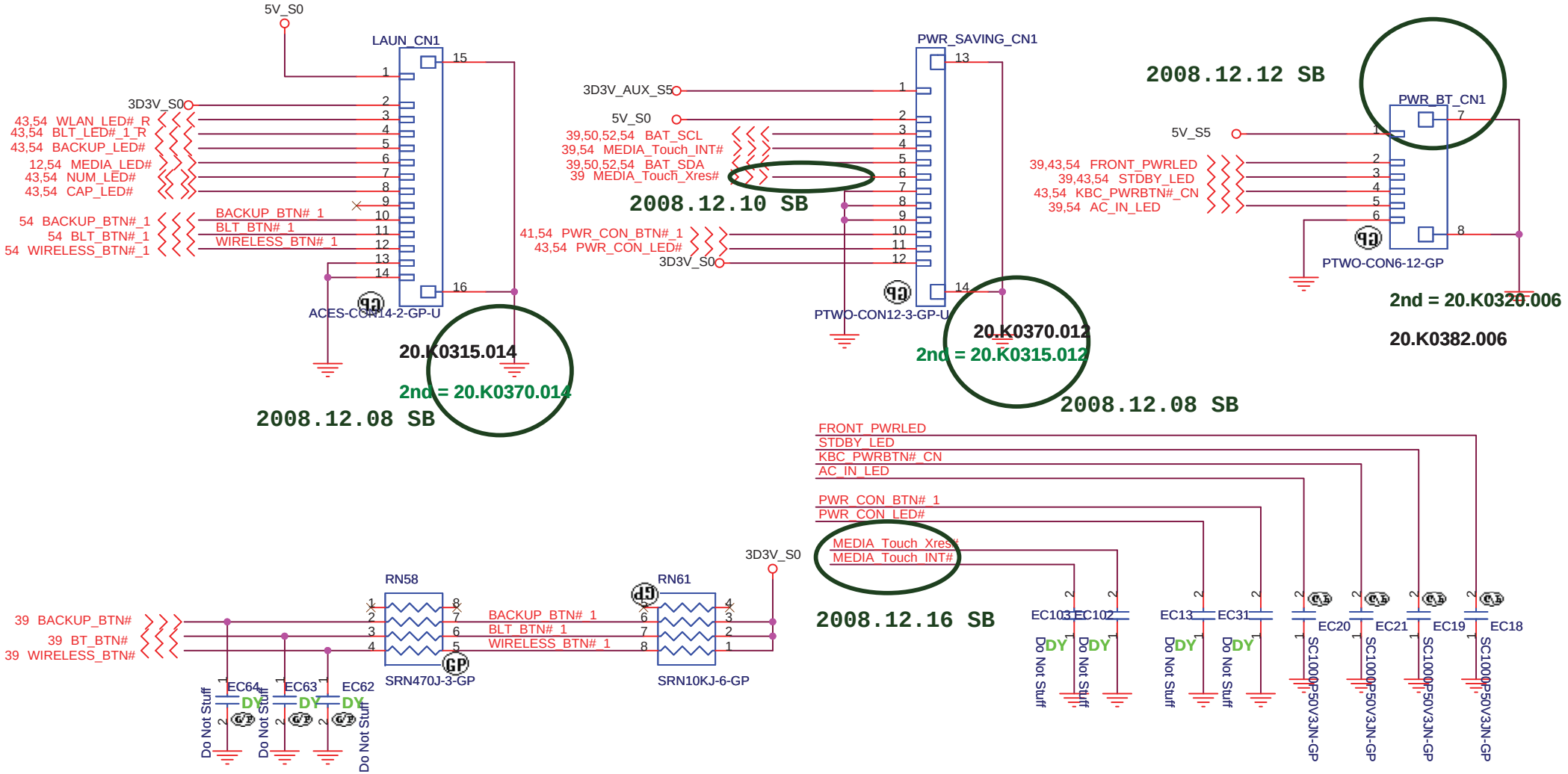
62.40009.671

2nd = 62.40012.101

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Touch PAD and FP	
Size	Document Number	Rev
	JM70-MV	SB
Date: Saturday, December 20, 2008	Sheet 41 of 55	

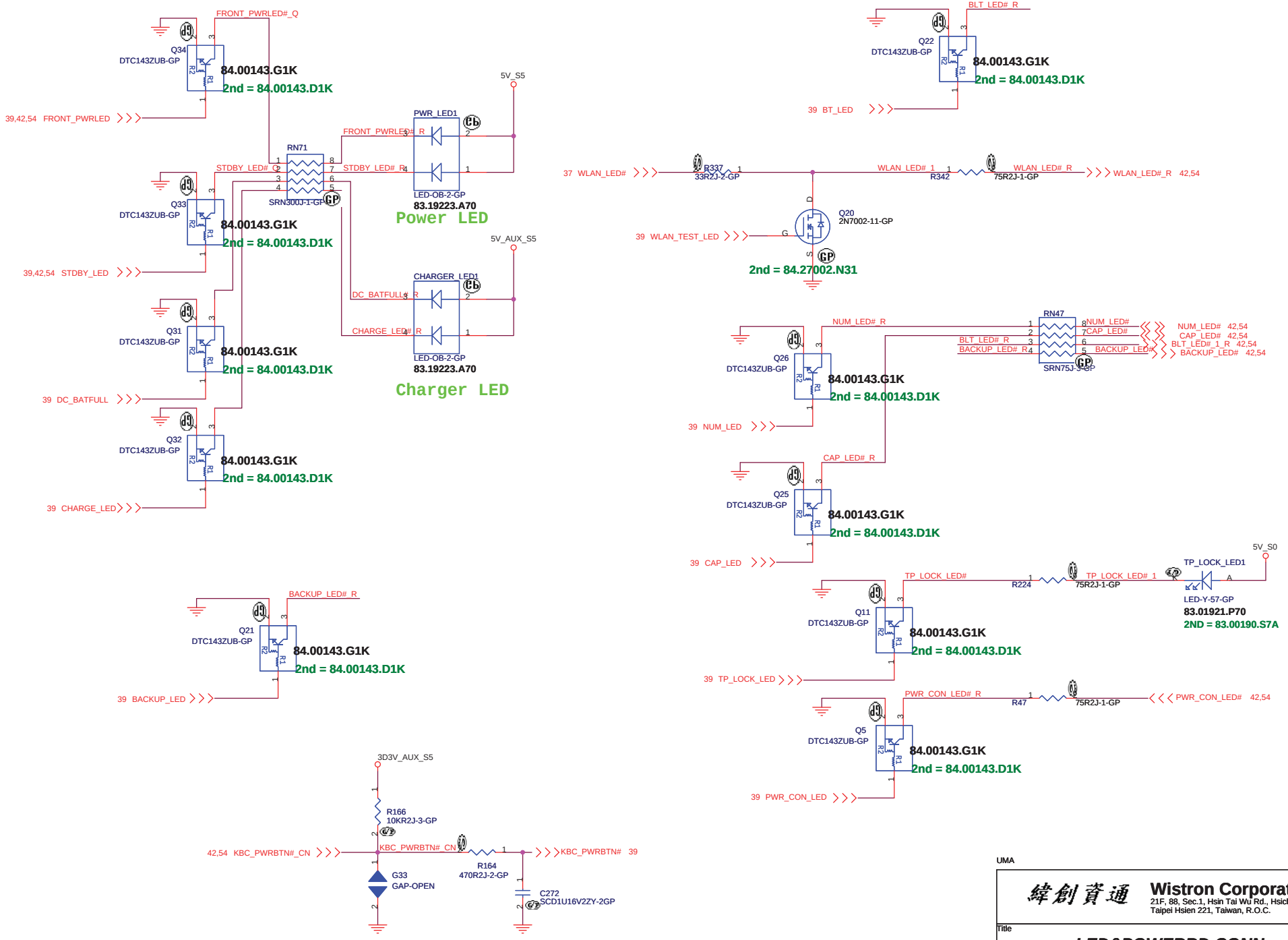


UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Launch CN*		
Size: A4	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 42 of 55	

LED



UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

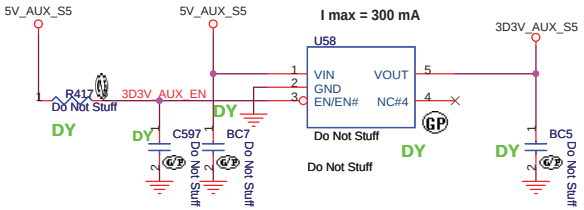
Title: ***LED&POWERBD CONN***

Size	Document Number	Rev
	JM70-MV	SB

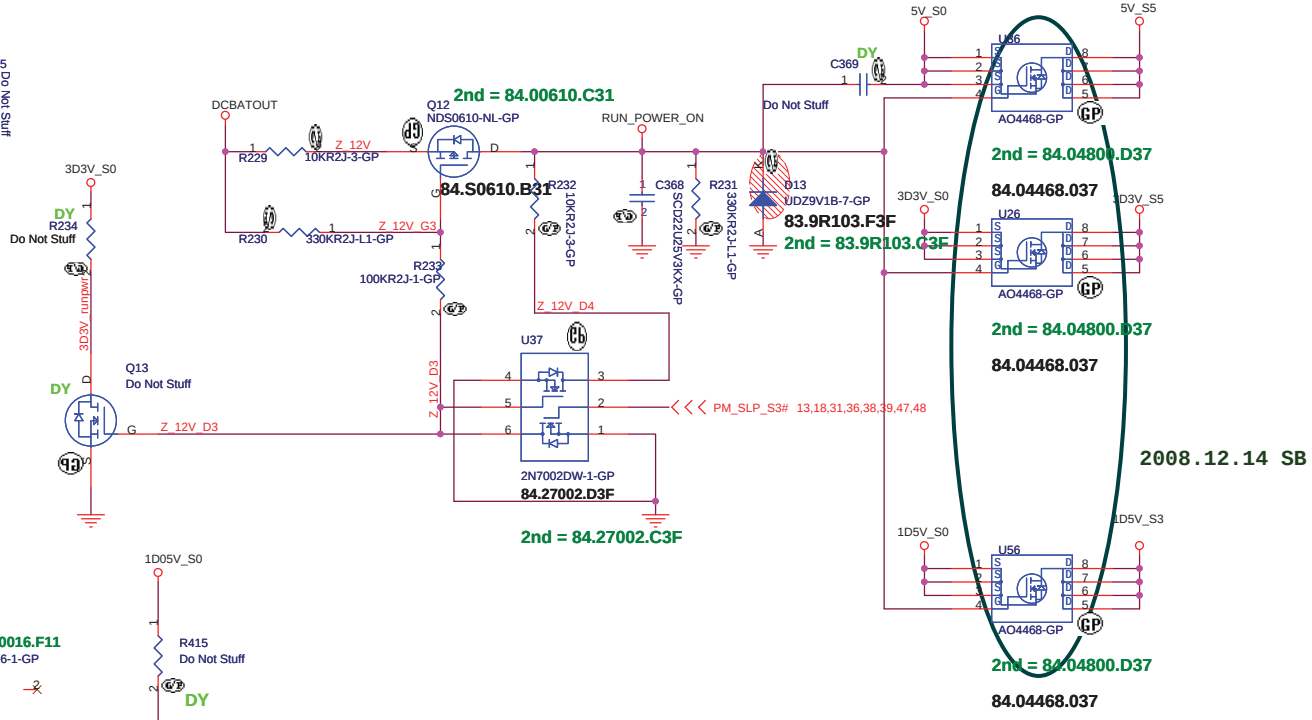
Date: Saturday, December 20, 2008 Sheet 43 of 55

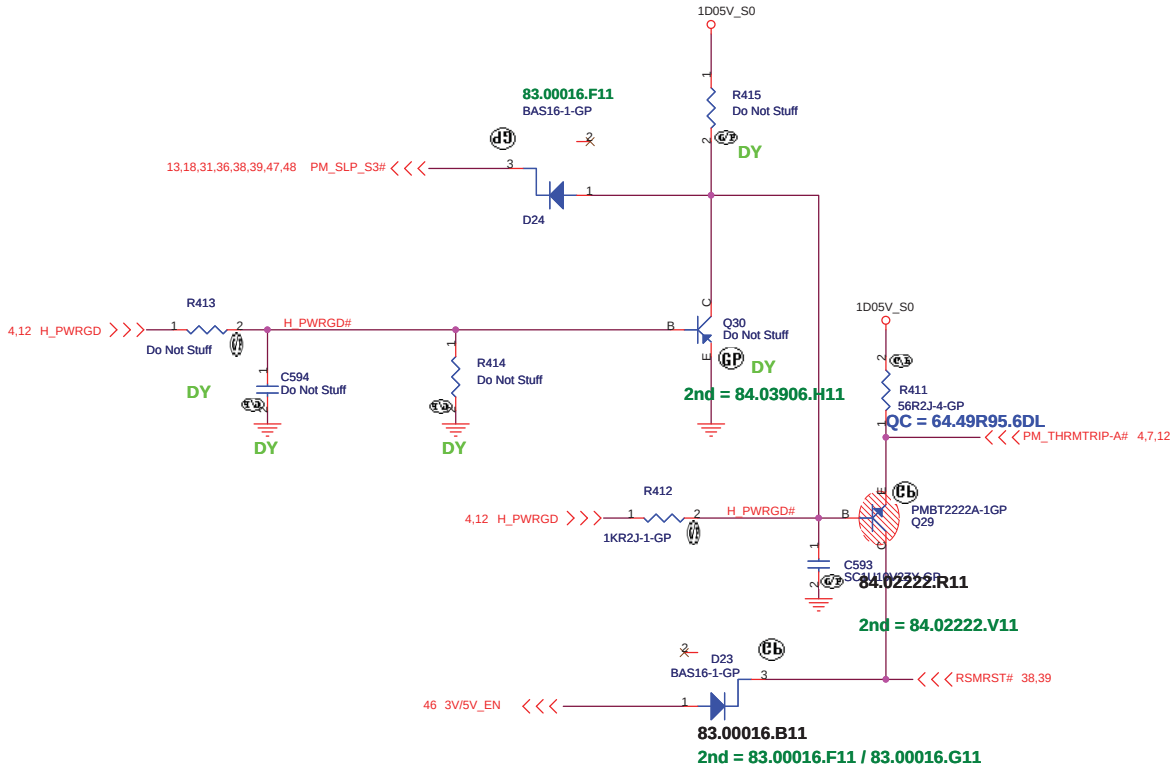
Aux Power

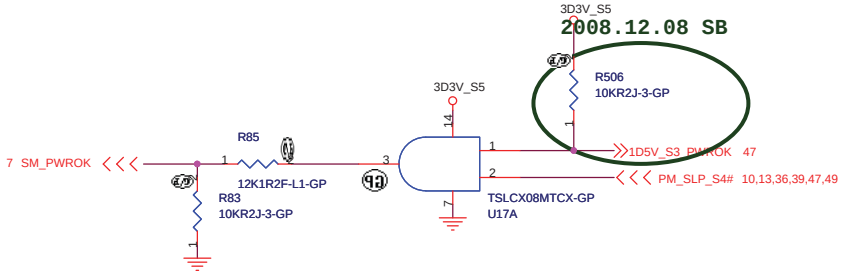
3D3V_AUX_S5



Run Power



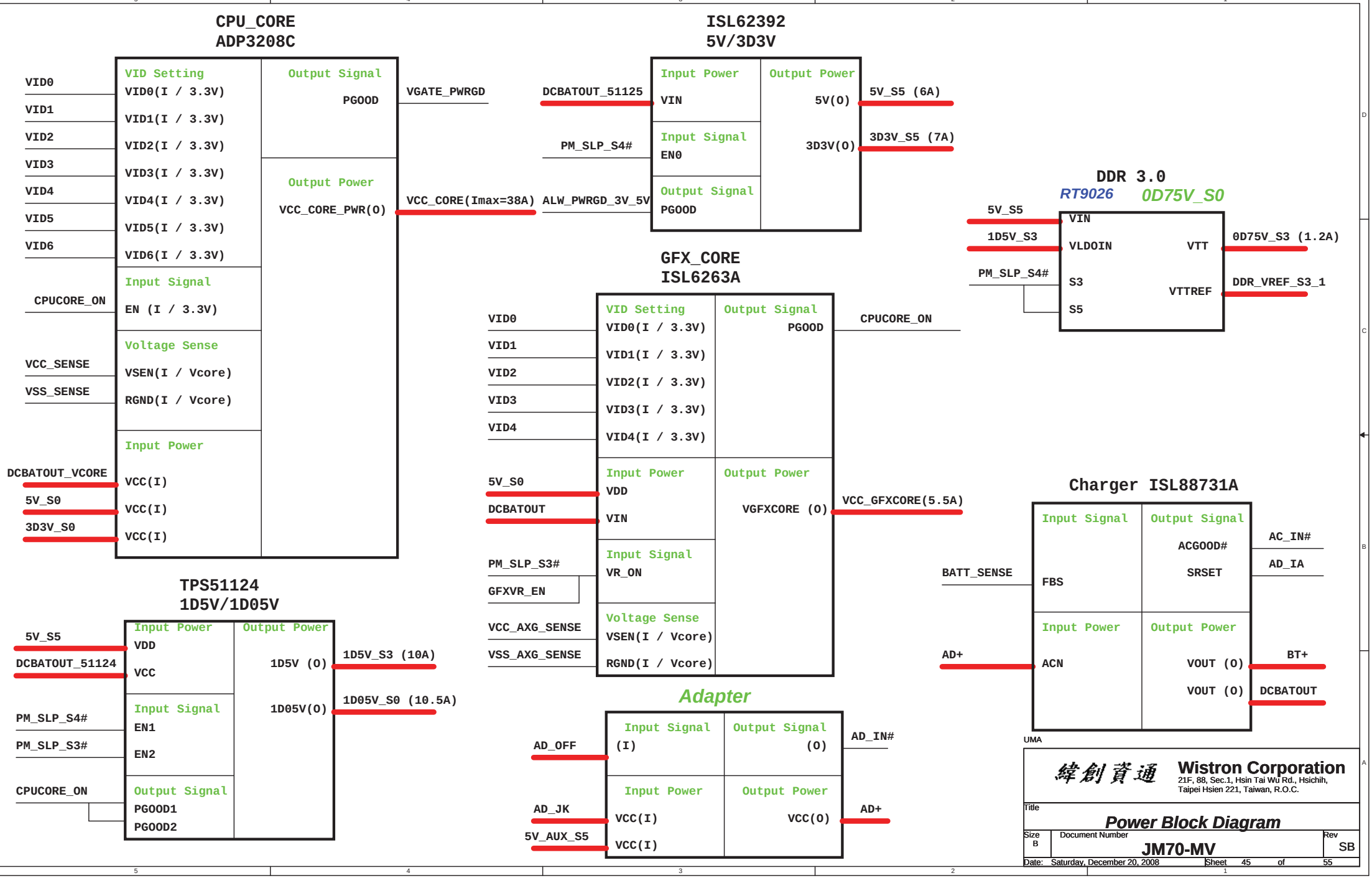




UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER and 3D3V_AUX_S5	
Size	Document Number: JM70-MV	Rev: SB
Date: Saturday, December 20, 2008	Sheet 44 of 55	



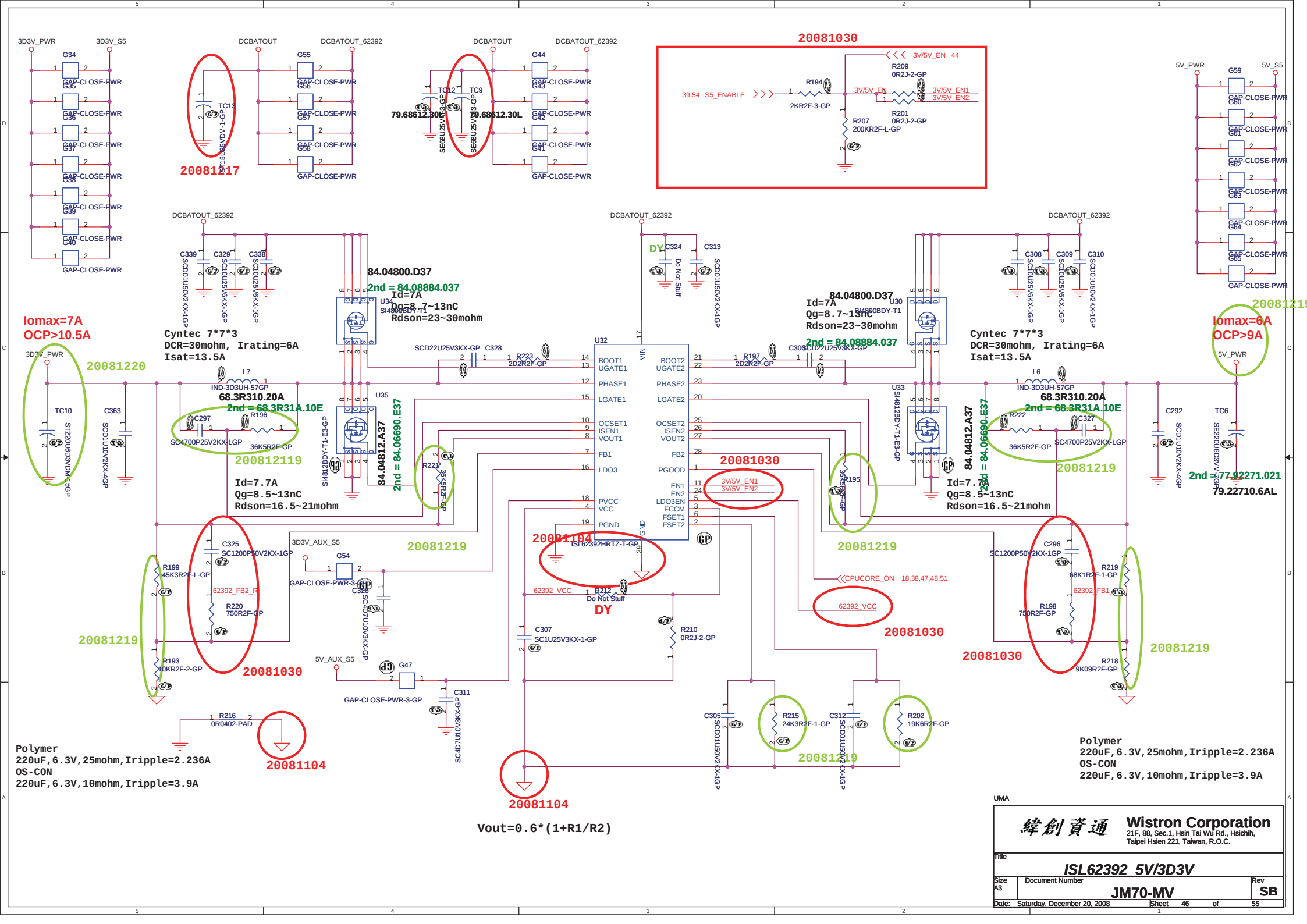
UMA

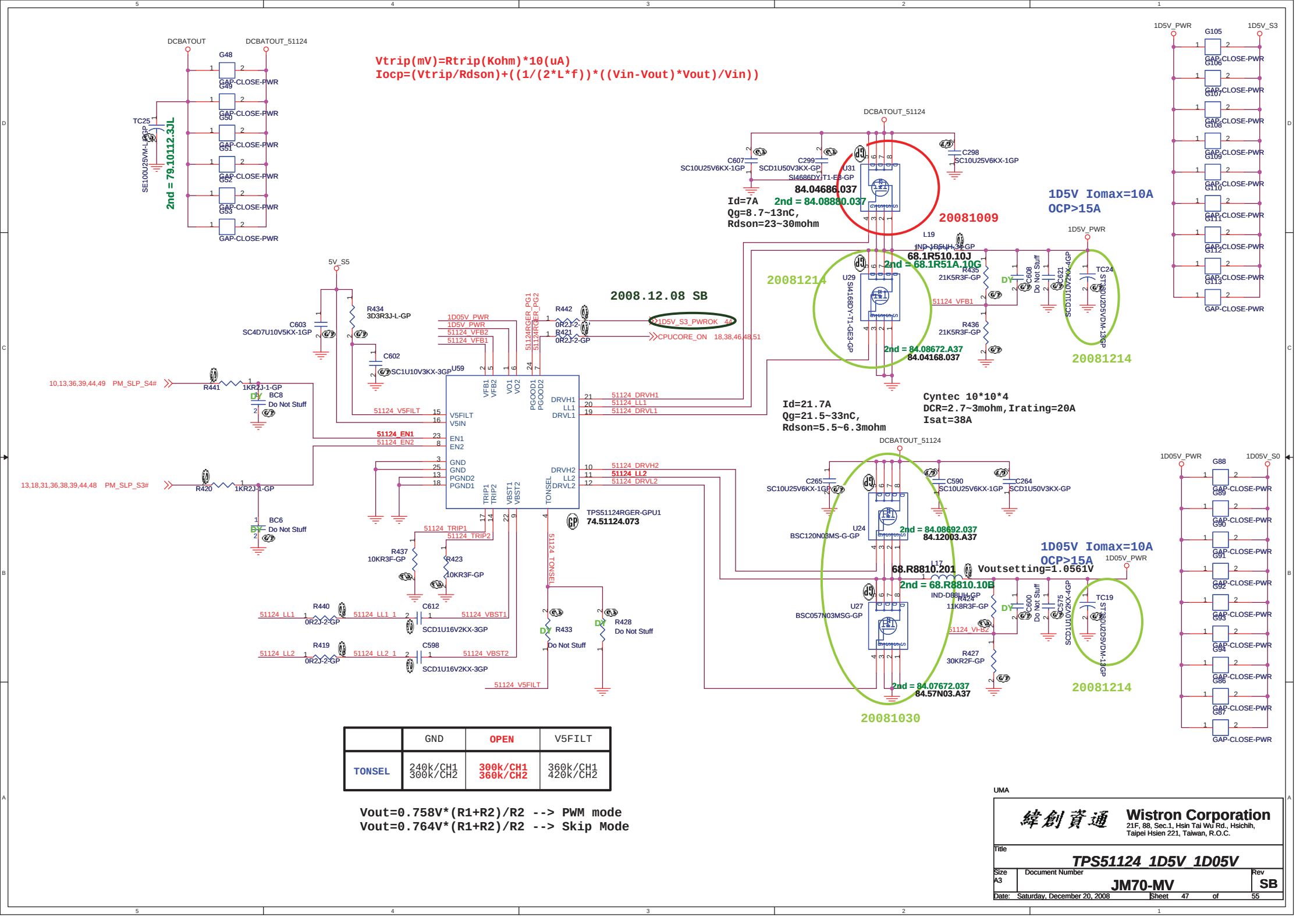
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
B	JM70-MV	SB

Date: Saturday, December 20, 2008 Sheet 45 of 55


20081030
3D3V_PWR
3D3V_S5
DCBATOUT
DCBATOUT_62392
20081217
79.68612.30L
39,54 S5_ENABLE
3V/5V_EN 44
3V/5V_EN1
3V/5V_EN2
5V_PWR
5V_S5
20081219
Iomax=7A
OCP>10.5A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
84.04800.D37
2nd = 84.08884.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
68.3R310.20A
2nd = 68.3R31A.10E
84.04812.A37
2nd = 84.06690.E37
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
20081220
200812119
20081104
20081030
20081219
Iomax=6A
OCP>9A
2nd =77.92271.021
79.22710.6AL
DY
Do Not Stuff
U32
ISL62392HRTZ-T-GP
62392_VCC
62392_FB2_R
62392_FB1
CPUCORE_ON 18,38,47,48,51
Vout=0.6*(1+R1/R2)
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62392 5V/3D3V
Size A3
Document Number
JM70-MV
Rev SB
Date: Saturday, December 20, 2008
Sheet 46 of 55



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

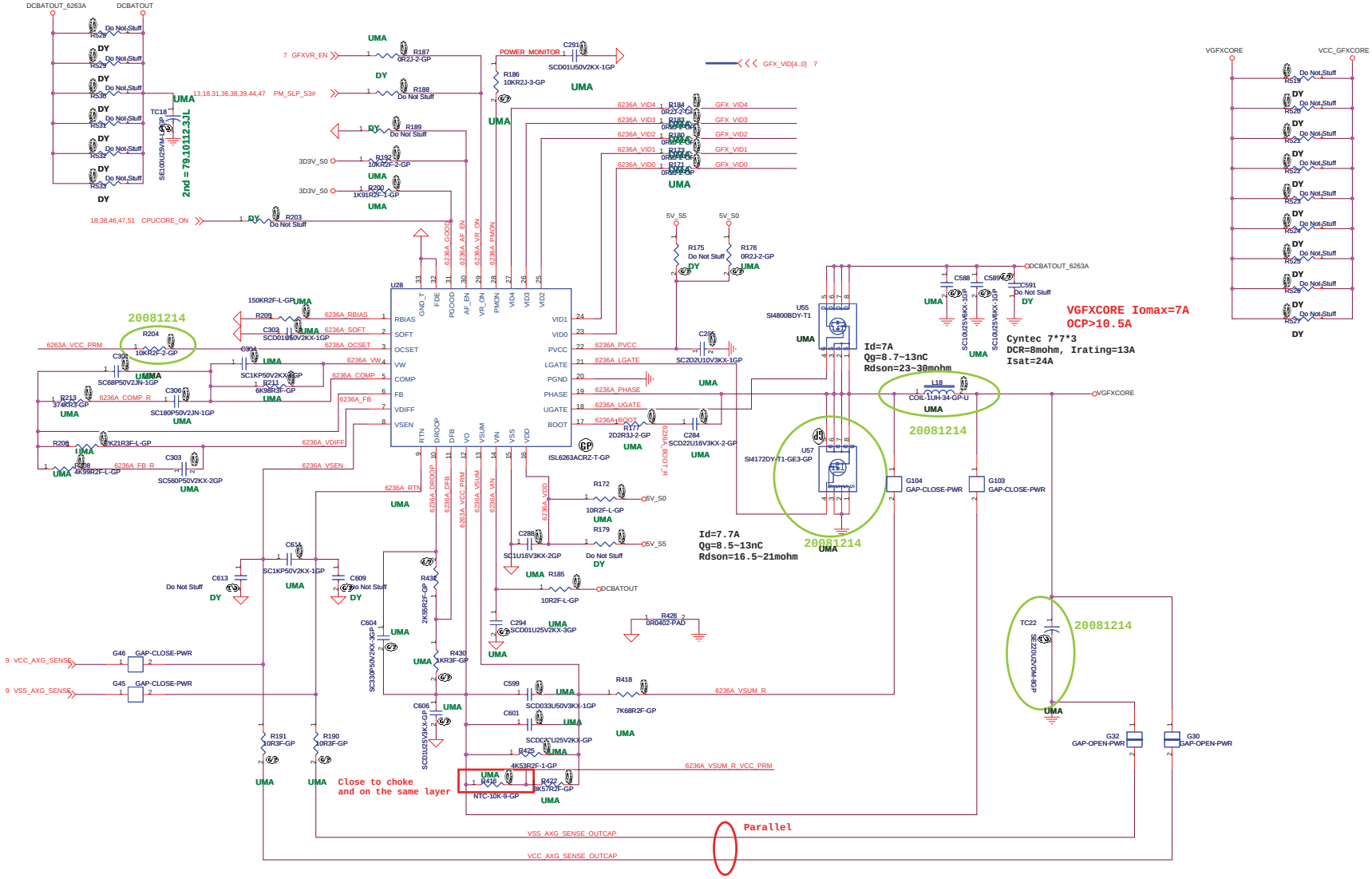
UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

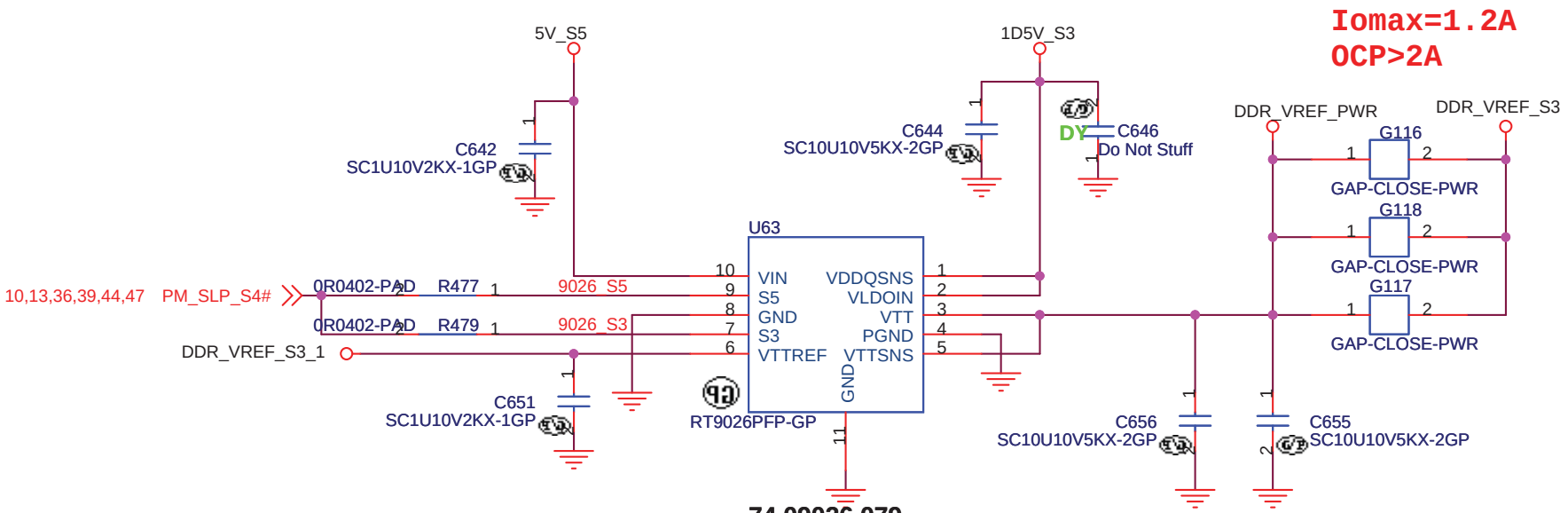
Title: TPS51124_1D5V_1D05V

Size	Document Number	Rev
A3	JM70-MV	SB

Date: Saturday, December 20, 2008 Sheet 47 of 55



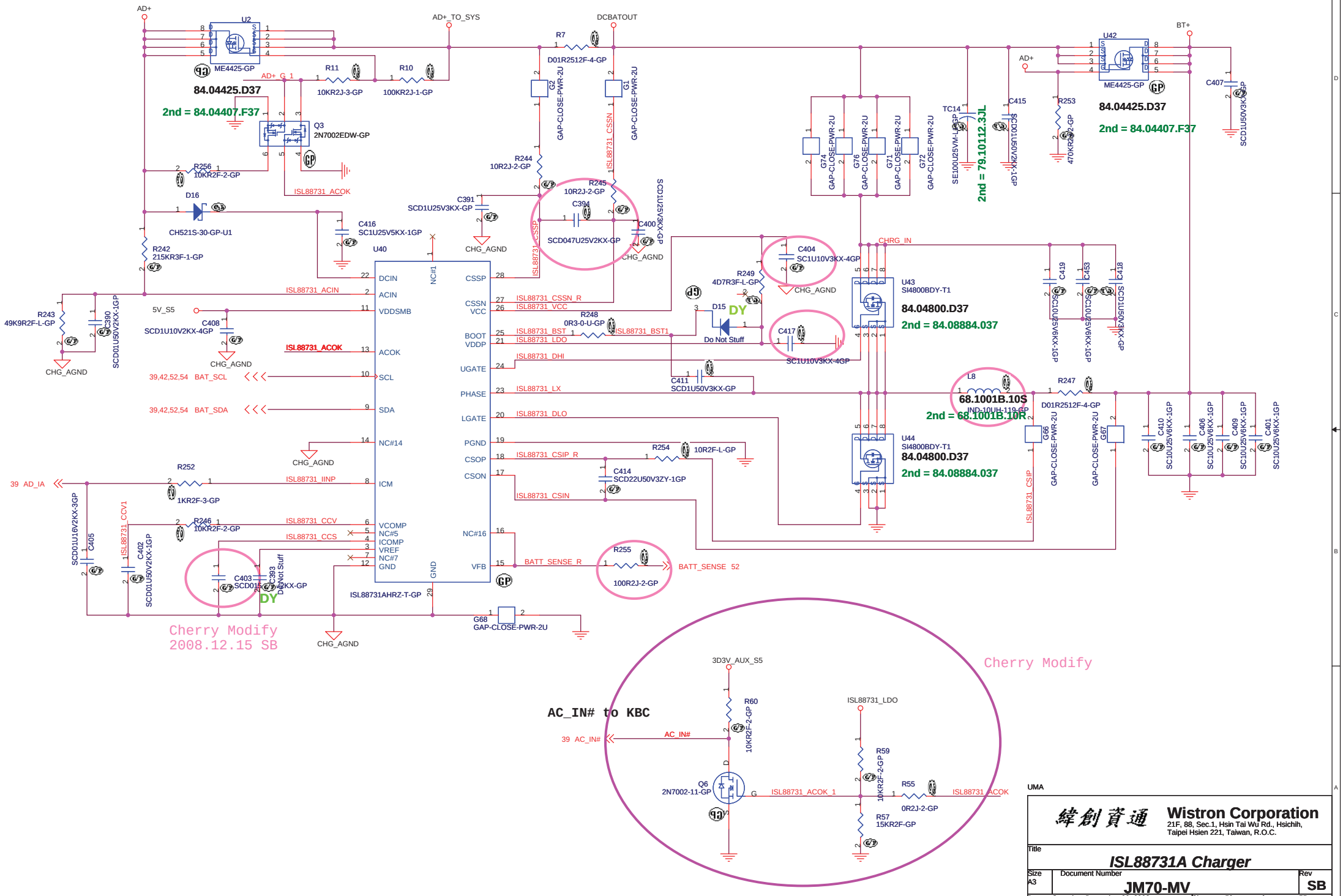
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL6263A_GFX CORE
Size A2	Document Number JM70-MV Rev SB
Date: Saturday, December 20, 2008	Sheet 48 of 55

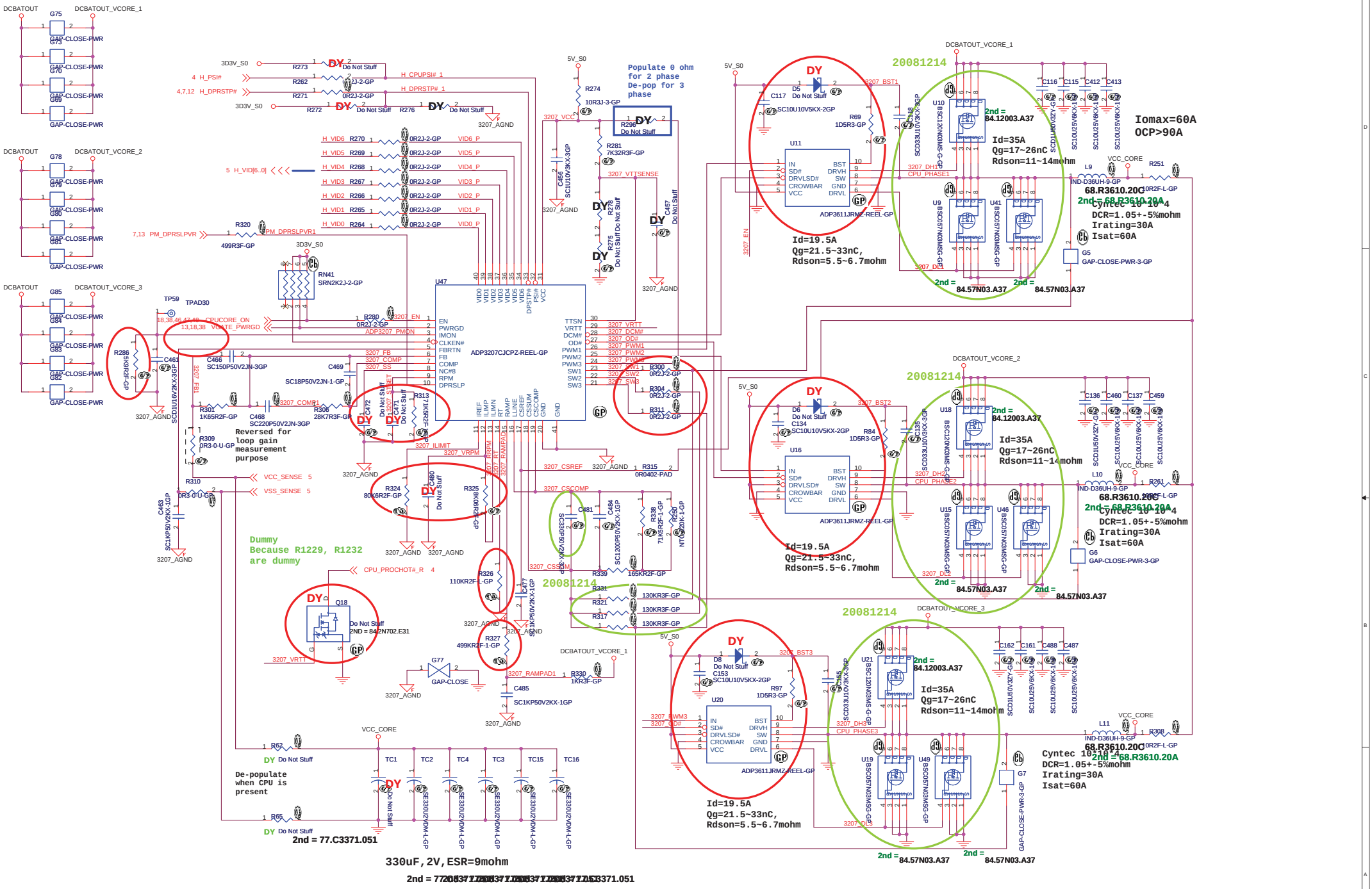


UMA

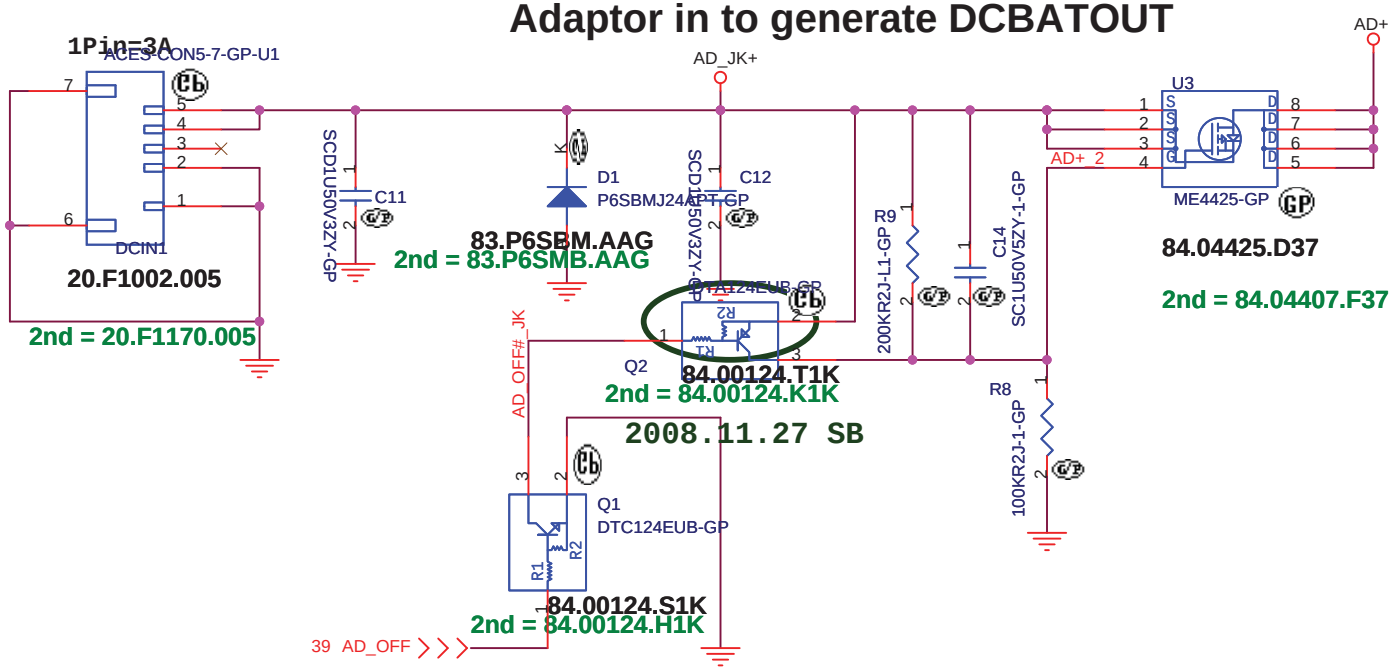
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***0D75V***	
Size: A	Document Number: **JM70-MV**	Rev: **SB**
Date: Saturday, December 20, 2008	Sheet 49 of 55	

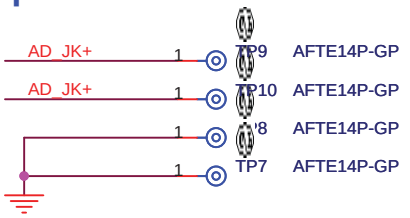

AD+
U2
ME4425-GP
84.04425.D37
2nd = 84.04407.F37
AD+_TO_SYS
DCBATOUT
R7
D01R2512F-4-GP
R11
10KR2J-3-GP
R10
100KR2J-1-GP
Q3
2N7002EDW-GP
R256
10KR2F-2-GP
ISL88731_ACOK
D16
CH521S-30-GP-U1
C416
SC1U25V5KX-1GP
R242
215KR3F-1-GP
U40
ISL88731AHRZ-T-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
R244
10R2J-2-GP
R245
10R2J-2-GP
C391
SCD1U25V3KX-GP
C394
SCD047U25V2KX-GP
C400
SCD1U25V3KX-GP
ISL88731_CSSP
ISL88731_CSSN
G2
GAP-CLOSE-PWR-2U
G1
GAP-CLOSE-PWR-2U
R249
4D7R3F-L-GP
D15
Do Not Stuff
DY
R248
0R3-0-U-GP
C404
SC1U10V3KX-4GP
C417
SC1U10V3KX-4GP
C411
SCD1U50V3KX-GP
ISL88731_BST
ISL88731_BST1
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
R254
10R2F-L-GP
C414
SCD22U50V3ZY-1GP
R255
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 52
C403
SCD015U25V2KX-GP
C393
Do Not Stuff
DY
R252
1KR2F-3-GP
R246
10KR2F-2-GP
R243
49K9R2F-L-GP
C390
SCD01U50V2KX-1GP
C408
SCD1U10V2KX-4GP
C405
SCD01U16V2KX-3GP
C402
SCD01U50V2KX-1GP
ISL88731_CCV1
ISL88731_CCV
ISL88731_CCS
5V_S5
CHG_AGND
39,42,52,54 BAT_SCL
39,42,52,54 BAT_SDA
39 AD_IA
G68
GAP-CLOSE-PWR-2U
Cherry Modify
2008.12.15 SB
U42
ME4425-GP
84.04425.D37
2nd = 84.04407.F37
BT+
C407
SCD1U50V3KX-GP
R253
470KR2J-2-GP
C415
SCD01U50V2KX-1GP
TC14
SE100U25VM-LGP
2nd = 79.10112.3JL
G74
G76
G71
G72
GAP-CLOSE-PWR-2U
CHRG_IN
U43
SI4800BDY-T1
84.04800.D37
2nd = 84.08884.037
U44
SI4800BDY-T1
84.04800.D37
2nd = 84.08884.037
C419
C453
C418
SCD1U25V6KX-1GP
L8
68.1001B.10S
IND-10UH-119-GP
2nd = 68.1001B.10R
R247
D01R2512F-4-GP
G66
G67
GAP-CLOSE-PWR-2U
C410
C406
C409
C401
SC10U25V6KX-1GP
AC_IN# to KBC
3D3V_AUX_S5
R60
10KR2F-2-GP
AC_IN#
39 AC_IN#
Q6
2N7002-11-GP
ISL88731_ACOK_1
R59
10KR2F-2-GP
R55
0R2J-2-GP
R57
15KR2F-GP
ISL88731_ACOK
Cherry Modify
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
JM70-MV
Rev
SB
Date: Saturday, December 20, 2008
Sheet 50 of 55


ADP3207C_CPU CORE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Size Custom
Document Number
JM70-MV
Rev SB
Date: Saturday, December 20, 2008
Sheet 51 of 55
UMA
ADP3207CJCPZ-REEL-GP
ADP3611JRMZ-REEL-GP
20081214
Iomax=60A
OCP>90A
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Cyntec 10 10 4
DCR=1.05+-5%mohm
Irating=30A
Isat=60A
68.R3610.20C
2nd = 68.R3610.20A
Reversed for loop gain measurement purpose
Dummy
Because R1229, R1232
are dummy
De-populate when CPU is present
2nd = 77.C3371.051
330uF,2V,ESR=9mohm
Populate 0 ohm for 2 phase
De-pop for 3 phase
2nd = 84.12003.A37
2nd = 84.57N03.A37

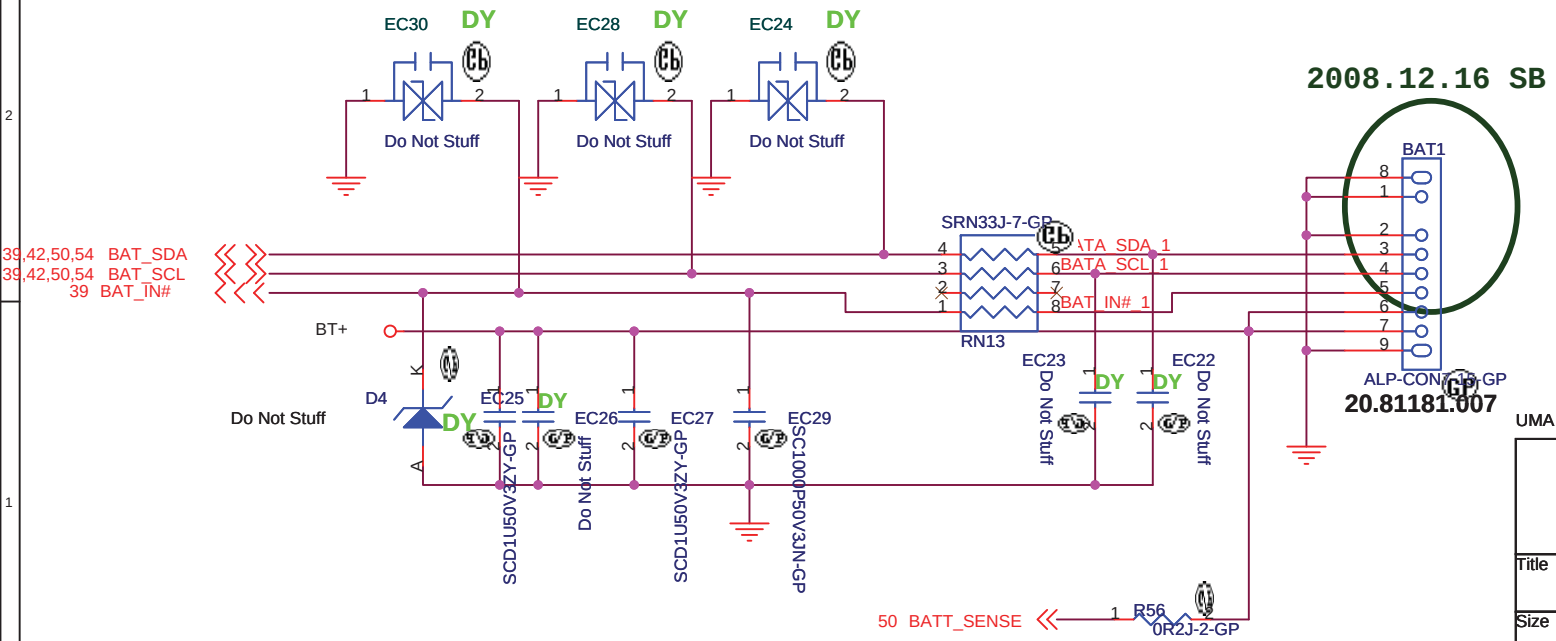
Adaptor in to generate DCBATOUT



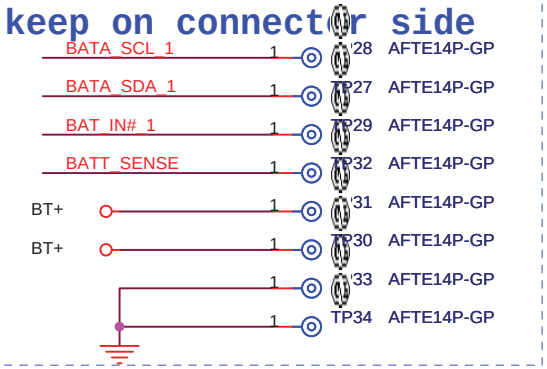
KB Conn. Test Point keep on connector side



MAIN BATTERY CONNECTOR



BAT1 Conn. Test Point keep on connector side



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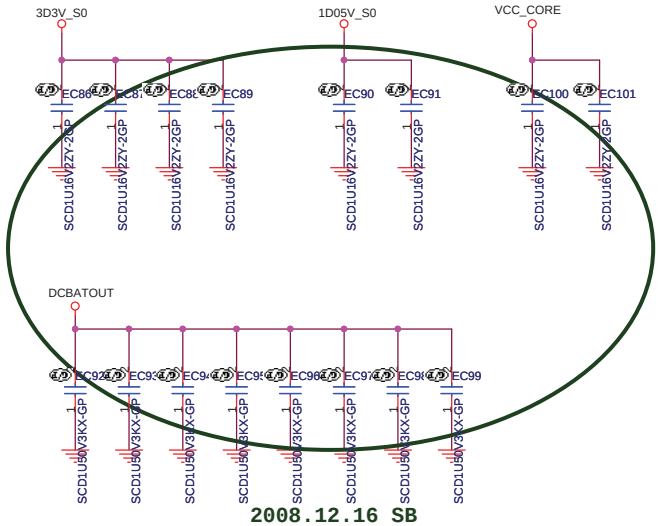
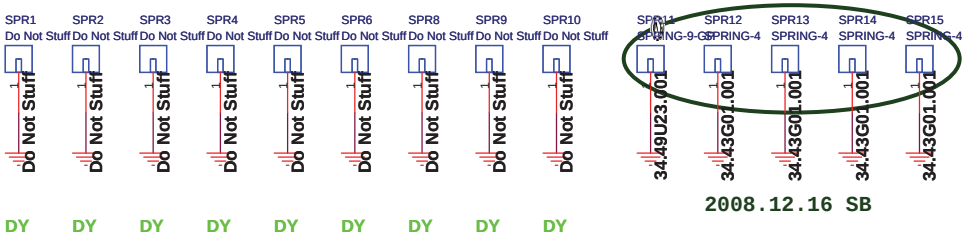
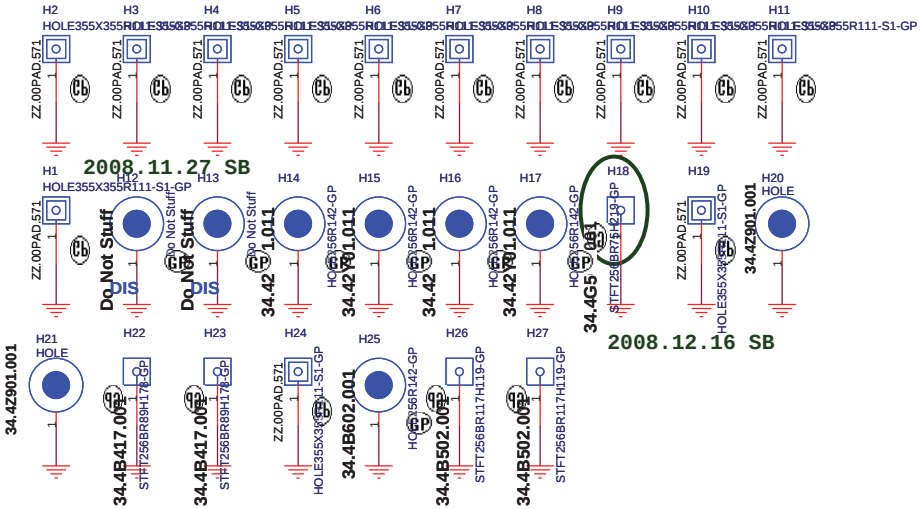
Title: **AD&BTY CONNECTER**

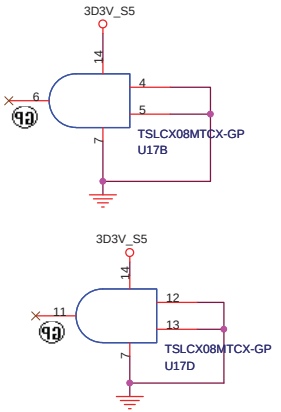
Size	Document Number	Rev
	JM70-MV	SB

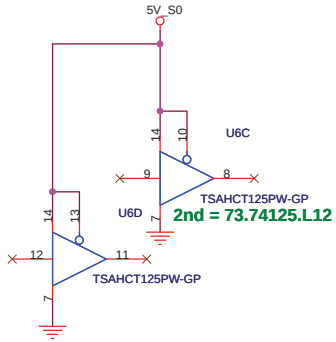
Date: Saturday, December 20, 2008 Sheet 52 of 55











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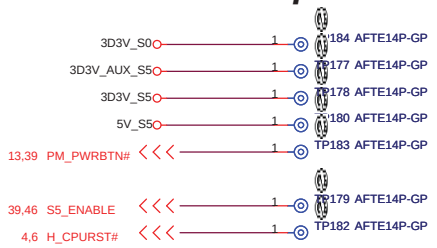
Title: ***EMI/Spring/Boss***

Size	Document Number	Rev
	JM70-MV	SB

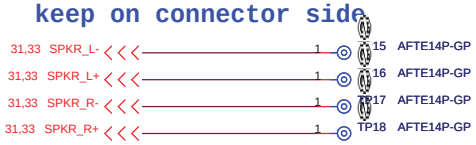
Date: Saturday, December 20, 2008 Sheet 53 of 55

Check test point

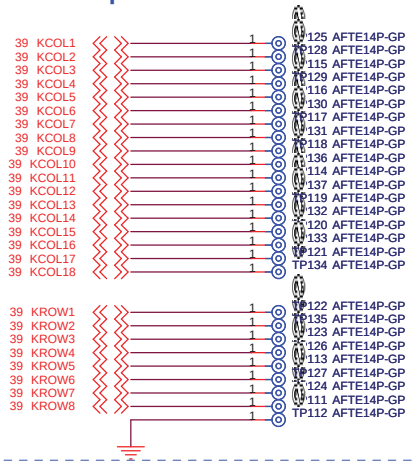


Test Point放在Dimm Door打開可量測處

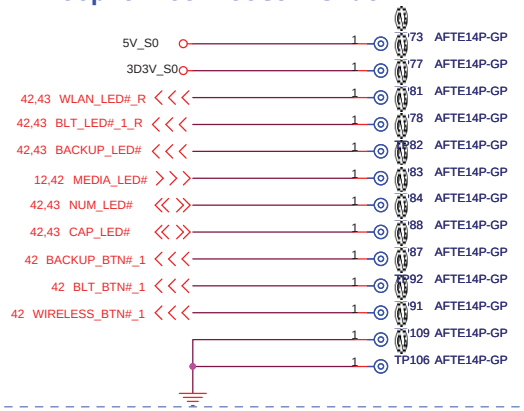
SPKR1 Conn. Test Point keep on connector side



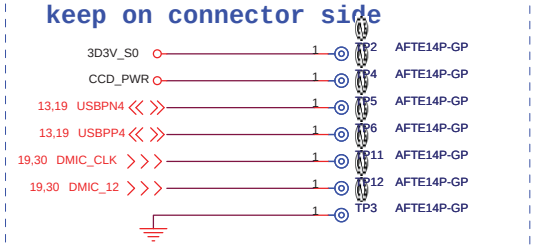
KB1 Conn. Test Point keep on connector side



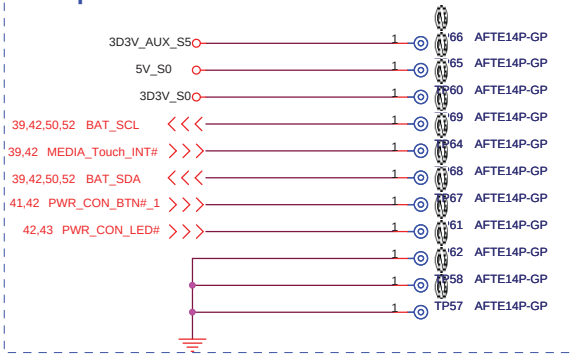
LAUN_CN1 Conn. Test Point keep on connector side



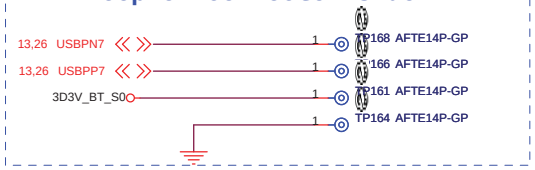
CCD_DMIC_CN1 Conn. Test Point keep on connector side



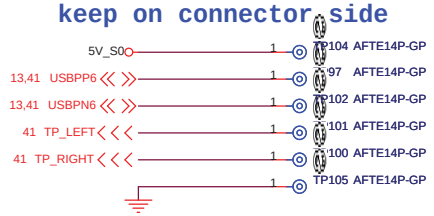
PWR_SAVING_CN1 Conn. Test Point keep on connector side



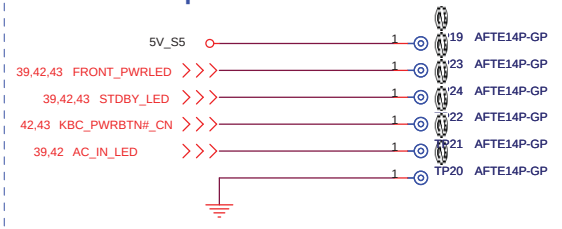
BT Conn. Test Point keep on connector side



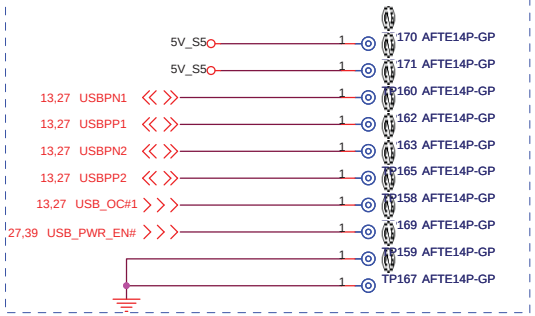
FP test Point keep on connector side



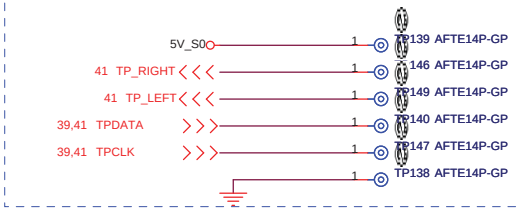
PWR_BT_CN1 Conn. Test Point keep on connector side



USB_CN1 Conn. Test Point keep on connector side



TOUCH PAD Conn. Test Point keep on connector side



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AFTE_TP**

Size	Document Number	Rev
A3	JM70-MV	SB

Date: Saturday, December 20, 2008 Sheet 54 of 55

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Title

HISTORY

Size	Document Number	Rev
A2	JM70-MV	SB

Date: Saturday, December 20, 2008 Sheet 55 of 55